Building Modulo N Counters Using ispLSI® Devices

Building counters where the terminal count is not a power of two can be accomplished using various logic configurations. Many designers simply decode the output of a binary counter and reset or load the counter when the modulo or terminal count is reached. If the reset or load is asynchronous, glitches may occur on the counter outputs. Synchronous resets and loads can eliminate the glitches, but they require more logic and may reduce the maximum count rate. The counter/decoder approach has an additional drawback on power-up. If the counter initializes to a count higher than the decoded terminal count, the first reset or load of the counter may not occur at the proper time.

By designing the modulo n counter as a state machine with each valid state defined, the glitch problem and the long count error on initialization are eliminated. This approach allows the four product term bypass in the ispLSI devices to be used to achieve high clock rates in prescalers and small counters.

The AND/OR/REGISTER architecture of the ispLSI devices provides an efficient means of forcing the all '1's state on the next clock edge after the terminal count is reached and forcing the counter outputs to '0's on the clock edge following invalid output states.

Figure 1. Bit Values For a 4-Bit Up Counter

MODULO	B3	B2	B1	B0
2	0	0	0	0
3	0	0	0	1
4	0	0	1	0
5	0	0	1	1
6	0	1	0	0
7	0	1	0	1
8	0	1	1	0
9	0	1	1	1
10	1	0	0	0
11	1	0	0	1
12	1	0	1	0
13	1	0	1	1
14	1	1	0	0
15	1	1	0	1
16	1	1	1	0
No count	1	1	1	1

The table in Figure 1 lists the bit values for a four-bit up counter with the values under the "Modulo" heading indicating which states should be included for various modulo counters.

The following design example is for a modulo 11 counter. Using the table in Figure 1, locate 11 under the modulo heading. The binary value to the right of the 11 indicates the terminal count that will be used to force the next state to be all ones. The counter states must include the terminal count state and all the states for lesser counts.

Figure 2. Unreduced Equations For a Modulo 11 Counter

```
B0  =  !B0 & !B1 & !B2 & !B3
    #  !B0 &  B1 & !B2 & !B3
    #  !B0 & !B1 &  B2 & !B3
    #  !B0 &  B1 &  B2 & !B3
    #  !B0 & !B1 & !B2 &  B3
    #   B0 & !B1 & !B2 &  B3

B1  =   B0 & !B1 & !B2 & !B3
    #  !B0 &  B1 & !B2 & !B3
    #   B0 & !B1 &  B2 & !B3
    #  !B0 &  B1 &  B2 & !B3
    #   B0 & !B1 & !B2 &  B3

B2  =   B0 &  B1 & !B2 & !B3
    #  !B0 & !B1 &  B2 & !B3
    #   B0 & !B1 &  B2 & !B3
    #  !B0 &  B1 &  B2 & !B3
    #   B0 & !B1 & !B2 &  B3

B3  =   B0 &  B1 &  B2 & !B3
    #  !B0 & !B1 & !B2 &  B3
    #   B0 & !B1 & !B2 &  B3
```

The unreduced equations for a modulo 11 counter are shown in Figure 2. A set of reduced equations for a modulo 11 counter are shown in Figure 3. When using the pDS® software to design the counter, either the FASTMIN or STRONGMIN option should be used to reduce the product terms to four or less per output if

Figure 3. Reduced Equations For a Modulo 11 Counter

```
B0  = !B0 & !B3
    # !B1 & !B2 &  B3

B1  =  B0 & !B1 & !B2
    # !B0 &  B1 & !B3
    #  B0 & !B1 &  B2 & !B3

B2  =  B0 &  B1 & !B2 & !B3
    # !B1 &  B2 & !B3
    # !B0 &  B1 &  B2 & !B3
    #  B0 & !B1 & !B2 &  B3

B3  =  B0 &  B1 &  B2 & !B3
    # !B1 & !B2 &  B3
```

counter speed is important. If speed is not critical, additional functions can be added to the counter by adding product terms.

The reduced equations each have four or fewer product terms and allow the ispLSI devices to utilize the four product term bypass to implement a fast counter. Counters from modulo two through 16 can be implemented to take advantage of the four product term bypass configuration. In prescaler applications, the outputs of the modulo n counter can be used to clock or enable additional counter stages to provide fast divider chains of any size. By controlling the modulo of additional stages, counters of any modulo can be constructed.

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