# PCMCIA Interface in an ispLSI® 2064 TQFP

## Introduction

The Personal Computer Memory Card International Association (PCMCIA) has developed standards for personal computer cards (PC cards) which are often referred to as PCMCIA cards. PC cards represent a key technology for adding memory, storage and I/O capabilities to portable systems. This application note provides an overview of the PC card interface and describes the in-system programmable (ISP™) Lattice ispLSI 2064 implementation in a single, space-saving TQFP (thin quad flat pack) package.

### Market Applications

The PCMCIA standard is now bringing the benefits of PC cards to a variety of industries and vertical applications, including smart cards, set-top boxes, automobiles and others. The PC card technology's compact size and durability make it the ideal technology for a wide variety of applications, including the growing hand-held storage market. Government data encryption systems are driving the adoption of PC cards as an interface for a variety of government and commercial uses.

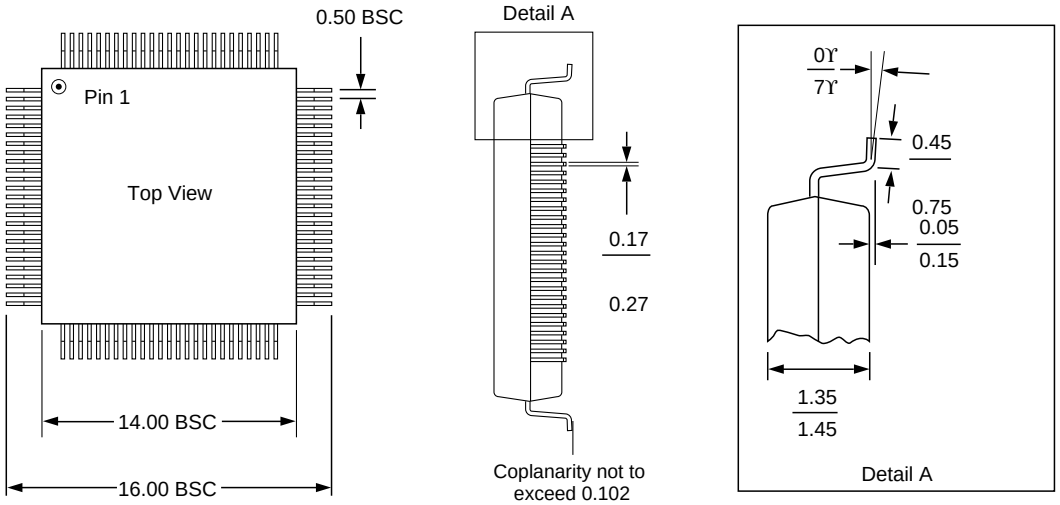
### PC Card Standard

The PCMCIA Electrical Specification describes the connector pinout, interface protocol, signaling environment, interface timing, programming model, and specifics of card insertion, removal, power up and configuration. It specifies both the 16-bit PC card and 32-bit CardBus interfaces. The PCMCIA specification defines three card sizes. All three types use the same 68-pin edge connector for attachment to the computer, and differ only in thickness. For details on the PCMCIA standards, access the Association's world-wide web site at **http://www.pccard.com**.

## Device Selection

In typical short design cycles such as for a PC Card, you usually can't wait for an ASIC design. Due to the small form factor of PC cards, the entire interface should be implemented in a single device. Using space-saving TQFP packages becomes practical with Lattice ISP high-density PLDs. Conventional programmer sockets damage the fragile leads of TQFP packages. Only Lattice offers the proven combination of ISP logic devices and TQFP. Lattice In-System Programmability™ will reduce your prototype time and eliminate stand-alone programming during the design phase of your system.

**Figure 1. 100-Pin TQFP Package with Dimensions in Millimeters, MIN/MAX.**



# PCMCIA Interface in an ispLSI 2064 TQFP

This application requires both high-density logic and a high device I/O count, as offered in the Lattice ispLSI 2000 family of devices. Combining the features of Lattice in-system programmability with the small size of a TQFP make the ispLSI 2064-80LT device an excellent choice for PCMCIA applications. See Figure 1 for the 100-pin TQFP dimensions.

## Interface Functions

Figure 2 shows a block diagram of the PCMCIA Interface Logic. This is the main PCMCIA Interface for a PC card. This logic integrates all the functions described below. The logic is designed to be generic and can be tailored to many applications.

### Input/Output Handler Function

This function generates control signals for a 16-bit I/O. INPACK is asserted when the I/O address is valid and is selected for reading. The IOIS16 signal is asserted when an I/O transfer is attempted. The bus-controller handles even and odd bytes individually for byte access in the 16-bit controller. IOCSE selects even addresses and IOCSO is used to select odd addresses.

### Common Memory Handler Function

This function decodes the address and generates CS, OE and WE control signals for Common Memory. The Common Memory is 16 bits wide. The High Byte and Low Byte Common Memory can be accessed individually. CMCSE selects even addresses and CMCSO selects odd addresses.

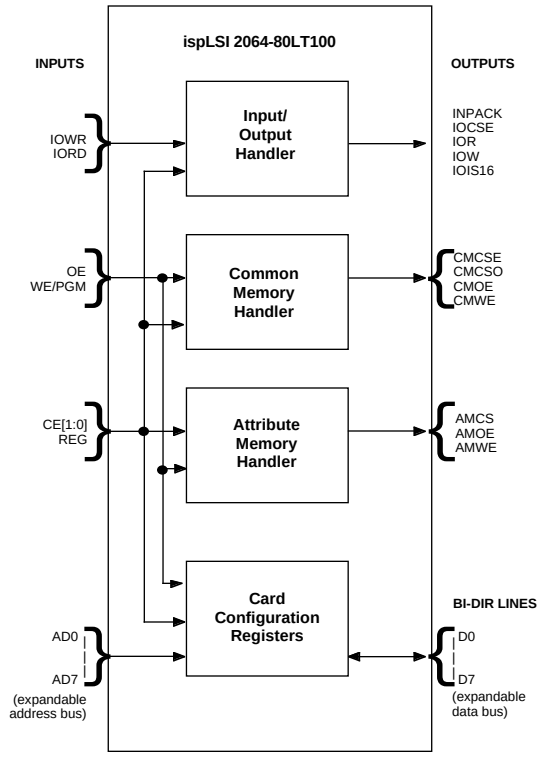
### Attribute Memory Handler Function

This function decodes Reg and Card enable signals and generates CS, OE and WE control signals for attribute memory. Locations 0100H, 0102H, 0104H and 0106H are reserved for Card Configuration registers.

### Card Configuration Registers Function

This function assumes four card configuration registers located at 10H, 12H, 14H and 16H. For an I/O card design, these registers would contain card configurable attributes including I/O address space, power requirements, and interrupt request. The addresses are decoded assuming a 256-bit ROM. However, this is expandable by modifying the register bank width.

**Figure 2. PCMCIA Interface Logic Block**




## Summary

Lattice In-System Programmability reduces prototype time and eliminates stand-alone programming during the design phase of a PC card. Combining these features with the small size of a TQFP package makes the Lattice ispLSI 2064-80LT device an excellent choice for PCMCIA applications. If you plan to expand your design with a wider address and data bus, use the ispLSI 2096-80LT device with 96 registers and 102 inputs and I/O pins in a space-saving 128-pin TQFP.

## Source File

The source file for this design is available in text format (file name: an8005.txt) on the ISP Encyclopedia CD-ROM and the Lattice web site. Please note that if you copy or download this file to another directory, this link will not work.



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