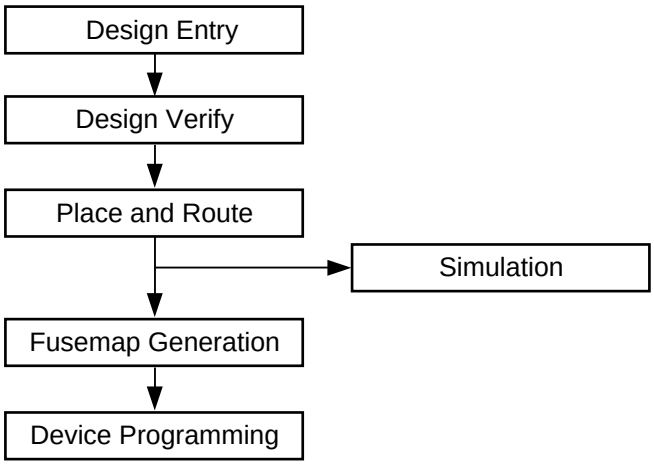
ispLSI and pLSI Design Flow

Introduction

Once the system design has been organized into functional components, and the logic functions which need to be incorporated in the selected components defined, the logic design phase begins. The general design flow is shown in figure 1. An ispLSI or pLSI design may be implemented from a number of design environments: including pLSI/ispLSI Development System (pDS) and numerous third-party CAE tools.

Figure 1. General Design Flow



These design environments offer various levels of design implementation from logic entry through programming the device. They support a variety of user interfaces and entry methods including: MS Windows GUI, Verilog-HDL, VHDL, truth tables, state machines and Boolean equations.

Design Entry

The pDS software allows the user to manually partition the logic to control design fit and performance. Using the MS Windows environment, logic functions are placed into Generic Logic Blocks (GLBs) and I/O Cells. This can be done by using the Edit, Cut, Copy, and Paste functions to enter Boolean equations and/or pre-defined functions from the LSC Macro and TTL libraries.

In addition to Boolean design entry, the pDS+ Fitters (in conjunction with third-party CAE tools) allow high-level descriptions of counters, adders, comparators, etc. High-level languages also support state machines, truth tables and case constructs for behavioral design implementations.

For standard CAE schematic designs, the pDS+ Fitters/ third-party CAE tools provide support for graphical and hierarchical logic implementations using the Lattice Semiconductor Corporation (LSC) libraries of primitives and macros. The integrated user interfaces also allow easy integration of system or user-created functions into a hierarchical schematic using a top-down or bottom-up design methodology.

Design Verification

Verification using the pDS software is accomplished in two steps after logic has been placed. First, each cell may be individually verified to ensure that the minimized logic will fit into the GLB architecture. After all GLB and I/O cells are incrementally checked, the entire design is then verified to ensure that all nets have proper sources and destinations.

Because the advanced pDS+ tools perform automatic partitioning, design verification is done at a higher-level (pre-partitioned). For example, in the ABEL environment, the Compile (ahdl2pla) function performs the syntax and design rule checks. After the Compile phase, the Optimize (plaopt) function (optionally) minimizes the design.

In the pDS+Viewlogic environment, pre-partitioned design verification is performed by the Design Analyzer which ensures the logic conforms to the LSC design rules. Other CAE tools may perform these functions differently, but each has been tested for completeness and accuracy.

Partitioning

Partitioning using the pDS software is done by the user as part of the design entry process. The advanced pDS+ tools incorporate LSC's automatic partitioner which accepts converted data from designs entered using the third-party CAE tool of choice. LSC specific attributes for design entry are available to guide the partitioner in order to optimize usage of device features and performance.

Place and Route

All LSC design tools offer automatic place and route. This entails placement of GLB and IOC logic and then routing (or interconnecting) the source signals to their destinations. In the ispLSI and pLSI devices, the Global

Routing Pool (GRP) provides fast interconnects from external inputs and GLB feedbacks to the GLB inputs. The Output Routing Pool (ORP) provides flexible interconnects from GLB outputs to external pins.

Post-Route Simulation

After place and route, a netlist for full timing and function simulation may be passed to the third-party simulator. Many of these simulators offer both textual and graphical input and interfaces. Board and system level simulation models are available from Synopsys Logic Modeling Division.

Documentation

Report files, containing partitioned equations and pin-out information, may be generated for routed or un-routed designs. The pDS software can also generate reports with post-route maximum timing delays. In addition, the design can be exported in a variety of design formats. This supports design interfaces to standard third-party CAE tools.

Device Programming

Programming information is generated on a routed design by the FuseMap Generator for a specific ispLSI and pLSI device. It is an ASCII file written in the JEDEC format.

Two programming methods are used to program the ispLSI and pLSI devices. The first method uses the Device Programming Mode for both types of devices. This method facilitates device programming support from third-party vendors. The second method uses the LSC In-System Programming Mode and applies to the ispLSI family of devices.

Both methods of device programming allow the user to program and read back the fuesmap from the programmed device for verification (if the security cell has not been set).

Figure 2. pDS Design Flow

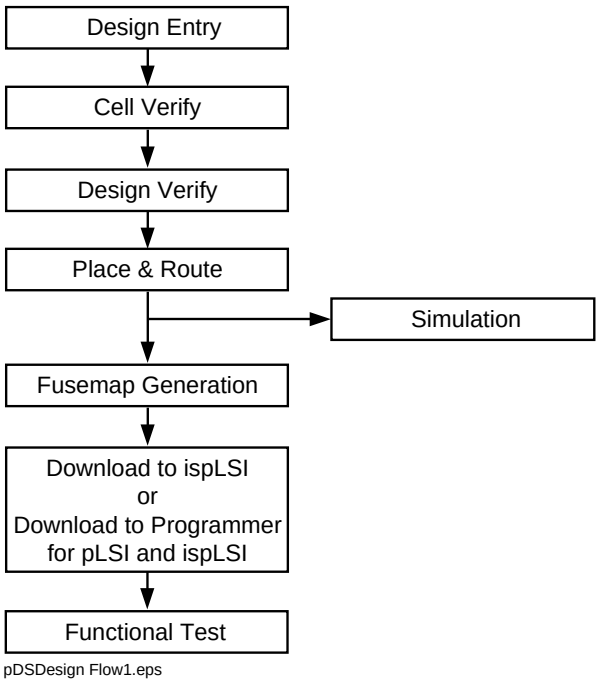
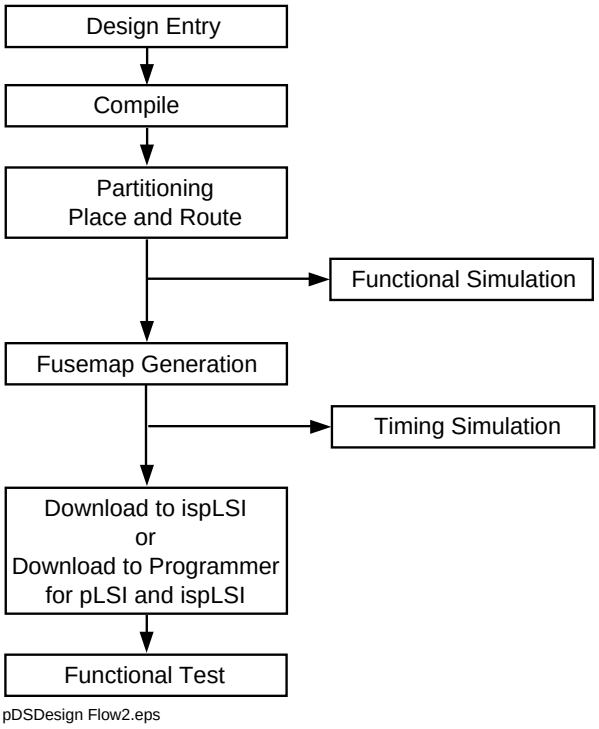


Figure 2a. Typical pDS+ Design Flow



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