Introduction to ispLSI® and pLSI® 2000/V Family

Introduction

Lattice Semiconductor Corporation's (LSC) ispLSI and pLSI families are high-density and high-performance E^2CMOS® programmable logic devices. They provide design engineers with a superior system solution for integrating high-speed logic on a single chip.

The ispLSI and pLSI 2000/V families are I/O intensive, programmable logic devices that combine the high performance and ease of use of PLDs with the density and flexibility of FPGAs.

The ispLSI and pLSI 2000/V families are ideal for designs needing high performance in conjunction with high I/O requirements.

The ispLSI family incorporates Lattice Semiconductor's innovative in-system programmable™ (ISP™) technology. ISP technology allows for real-time programming, less expensive manufacturing and end-user feature reconfiguration.

E^2CMOS technology features reprogrammability, the ability to program the device again and again to easily incorporate any design modifications. This same capability allows full parametric testability during manufacturing, which guarantees 100 percent programming and functional yield.

All necessary development tools are available from LSC and third-party vendors. Development tools offered range from LSC's low cost pDS® software, featuring Boolean entry in a graphical Windows™ based environment, to the pDS+™ family of fitters that interfaces with third-party development software packages. Design systems interfacing with pDS+ Fitters feature schematic capture, state machine and HDL design entry. Designs can now be completed in hours as opposed to days or weeks.

ispLSI and pLSI 2000 Family

- ❑ 180 MHz System Performance
- ❑ 5.0 ns Pin-to-Pin Delay
- ❑ Deterministic Performance
- ❑ High Density (1,000-6,000 PLD Gates)
- ❑ 44-Pin to 176-Pin Package Options
- ❑ Flexible Architecture
- ❑ Easy-to-Use
- ❑ In-System Programmable (ispLSI)
- ❑ Ideal for I/O Intensive Designs

ispLSI and pLSI 2000V Family

- ❑ 3.3V Operation
- ❑ 100 MHz System Performance
- ❑ 7.5 ns Pin-to-Pin Delay
- ❑ 3.3V In-System Programmable Using Boundary Scan Test Access Port (TAP)
- ❑ Programmable Open-Drain Output
- ❑ 3.3V/5V Compatible I/O

ispLSI and pLSI Technology

- ❑ UltraMOS E^2CMOS — the PLD Technology of Choice
- ❑ Electrically Erasable/Programmable/ Reprogrammable
- ❑ 100% Tested During Manufacture
- ❑ 100% Programming Yield
- ❑ Fast Programming

ispLSI and pLSI Development Tools

- ❑ Low Cost, Fully Integrated pDS Design System for the PC
- ❑ Boolean Equations and Macro Input
- ❑ HDL, VHDL, Boolean Equation, State Machine and Schematic Capture Entry
- ❑ pDS+ Support for Industry-Standard Third-Party Design Environments and Platforms
- ❑ Timing and Functional Simulation
- ❑ PC and Workstation Platforms

2000/V Family Overview

The ispLSI and pLSI 2000/V families of high-density devices address high-performance system logic needs, implementing logic functions ranging from registers, to counters, to multiplexers, to complex state machines.

Introduction to ispLSI and pLSI 2000/V Family

With PLD density ranging from 1,000 to 6,000 gates, the ispLSI and pLSI 2000/V family provides a wide range of programmable logic solutions which meet tomorrow's design requirements today.

Each device contains multiple Generic Logic Blocks (GLBs), which are designed to maximize system flexibility and performance. A balanced ratio of registers and I/O cells provides the optimum combination of internal logic and external connections. A global interconnect scheme ties everything together, enabling utilization of up to 80% of available logic. Table 1 describes the family attributes.

2000V Family

The high-perfomance 3.3-Volt ispLSI 2000V family features the same base architecture as the 5-Volt 2000 family and introduces an open-drain output option. This open-drain feature is user-programmable for each I/O pin and increases bus flexibility, allowing easy implementation of wired-OR logic such as bus arbitration or interrupt functions. Additionally, each 2000V family member also has the ability to accept 3.3V or 5V signals and is 3.3V in-system programmable using Boundary Scan Test Access Port (TAP).

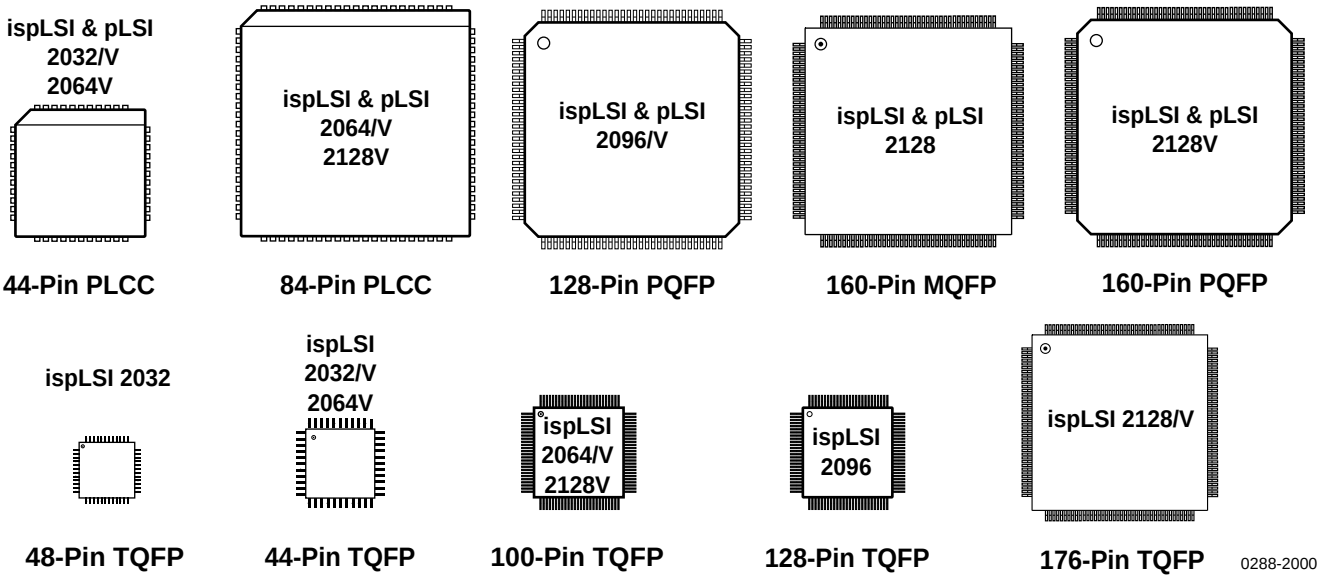
New also to the 2000V Family are multiple I/O options for the 2128V and 2064V. The 2128V is available in both 128 and 64 I/O versions and the 2064V is available in both 64 and 32 I/O versions.

Table 1. 2000 and 2000V (3.3V) Family Attributes

	2000 Family				2000V Family			
	2032	**2064**	**2096**	**2128**	**2032V**	**2064V**	**2096V**	**2128V**
Density (PLD Gates)	1,000	2,000	4,000	6,000	1,000	2,000	4,000	6,000
Speed: **f**max (MHz)	180	125	125	100	100	100	80	80
Speed: **t**pd (ns)	5.0	7.5	7.5	10	7.5	7.5	10	10
Macrocells	32	64	96	128	32	64	96	128
Registers	32	64	96	128	32	64	96	128
Inputs + I/O	35	70	104	138	35	70/37	104	138/74
Pin/Package	44-pin PLCC 44-pin TQFP 48-pin TQFP	84-pin PLCC 100-pin TQFP	128-pin PQFP 128-pin TQFP	160-pin MQFP 176-pin TQFP	44-pin PLCC 44-pin TQFP	44-pin PLCC 44-pin TQFP 84-pin PLCC 100-pin TQFP	128-pin PQFP 128-pin TQFP	84-pin PLCC 100-pin TQFP 160-pin MQFP 176-pin TQFP

Table 1-0003A/2K

Figure 1. 2000 Family Packages



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