ispLSI® 3192 to 6192 Design Conversion

Introduction

With the introduction of the ispLSI 6192, pDS® 3.0 software was also introduced to support the full capability of the device architecture. As an interim solution before ispLSI 6192 support on pDS+™ 3.0 or later versions becomes available, the PLD portion of the ispLSI 6192 design can be implemented in existing software as a ispLSI 3192 and then brought into the pDS environment for the ispLSI 6192 module configuration.

This application note describes the steps required to convert an ispLSI 3192 design into an ispLSI 6192 design for the pDS environment. It also assumes that the user is familiar with Lattice's pDS+ 3.0 or later and pDS 3.0 software.

The design is initiated in the pDS+ Fitter environment with third-party design tools and partitioned into an ispLSI 3192. pDS 3.0 is used to enter the ispLSI 6192 module configuration syntax. The module syntax is then merged with the partitioned logic and then the whole design is fitted into the ispLSI/pLSI 6192 using pDS 3.0.

ispLSI 3192 Versus ispLSI 6192

The ispLSI 3192 and 6192 devices contain an equal number of Twin GLBs™. In addition to GLBs, the ispLSI 6192 device contains memory and register/counter modules. The PLD portion of the ispLSI 6192 has half as many I/Os as the ispLSI 3192. This factor is important since the ispLSI 3192's extra I/O pins will be used to preserve the signals needed for the ispLSI 6192 modules.

Conversion Process

Partitioning the 3192 Device Using pDS+ 3.0 or Later

Any of the pDS+ Fitters (pDS+ Synopsys, pDS+ Mentor, pDS+ Viewlogic, pDS+ ABEL, etc.) can be used to partition the design for the ispLSI 3192 device.

The following are necessary for successful partitioning:

1. Connect all the module interface signals to I/O pins.
2. Do not use more than 96 I/O pins for the general-purpose logic portion of the design.
3. Only 96 I/O pins are available to connect module only interface signals.
4. Select "preroute_ldf" as output format for the dpm.
5. Pin locking approaches:

   a. First, try to partition the design without locking any pins. If this approach does not produce successful partition, try the pin locking method stated below.

   b. Lock all the pins (logic + interface). Unblocked I/O pins should be used for the logic signals and blocked I/O pins should be used for the interface signals. Unblocked I/O pins are those package pins that are connected to ispLSI 3192 I/Os that are available in ispLSI 6192 device. Blocked I/O pins are those package pins connected to ispLSI 3192 I/Os that are not available in ispLSI 6192 device. Blocked and unblocked I/O pins numbers for the ispLSI 3192 devices are listed at the end of this application note.

   Sample dpm command:

   ```
   dpm -if laf -I <design_name>.laf
   -of preroute_ldf
   ```

   This command generates the <design_name>.ldf file.

Entering Module Syntax Using pDS 3.0

Use pDS 3.0 to enter the module configuration for the design.

The recommended procedure to enter the module portion of the design is as follows:

1. Use a module syntax template to enter the module configuration and module port connection.
2. Enter MIOC syntax to connect signals to module I/O pins.
3. Enter IOC syntax to connect module only interface signals to regular I/O pins.
4. Verify
5. Export LDF

This procedure generates the <design_name_mod>.ldf. file.

Merging LDF Files

Changes to the exported <design_name>.ldf:

1. Change the device name to ispLSI 6192.
2. Comment IOC sections of all the I/O pins corresponding to the module only interface signals.
3. Remove lock property on all the pins.

To make changes to the <design_name_mod>.ldf file:

1. Comment GLB sections corresponding to module only interface signals.
2. Comment IOC sections corresponding to module only interface signals.
3. Comment Header section.
4. Comment Declare section.
5. Modify module only interface signal names to match the names in <design_name>.ldf.

Use any text editor to merge <design_name>.ldf and <design_name_mod>.ldf and create a new LDF file, <design_name_new>.ldf.

Setting NOTWINCHK Variable for pDS 3.0

Since the design rules are different for the pDS+ 3.0 and later and the pDS 3.0, set the NOTWINCHK variable in your autoexec.bat file and reboot the machine.

Setting the variable:

```
SET  NOTWINCHK=1
```

By setting this variable, the pDS 3.0 will not check certain Twin GLB specific design rules.

Fitting the Merged LDF File Into the 6192

Open the pDS 3.0 design software and import <design_name_new>.ldf.

The procedure to fit the design using the pDS 3.0 is as follows:

1. Open pDS 3.0
2. Import LDF
3. Verify
4. Route
5. Fuse Map

Use the download software to download the resulting fusemap into an ispLSI 6192 device.

Blocked Pins for ispLSI Device

Pins that should not be used in the ispLSI 3192 design for general-purpose I/O when targeting the ispLSI 6192 are:

1, 3, 4, 7, 10, 12, 14, 16, 19, 22, 23, 25, 37, 39, 40, 43, 46, 48, 50, 52, 55, 58, 59, 61, 65, 67, 68, 71, 74, 76, 78, 80, 83, 86, 87, 89, 93, 95, 96, 99, 102, 104, 106, 108, 111, 114, 115, 117, 121, 123, 124 , 127, 130, 132, 134, 136, 139, 142, 143, 145, 157, 159, 160, 163, 166, 168, 170, 172, 175, 178, 179, 181, 185, 187, 188, 191, 194, 196, 198, 200, 203, 206, 207, 209, 213, 215, 216, 219, 222, 224, 226, 228, 231, 234, 235, 237

Unblocked Pins for ispLSI Device

Pins that should be used in the ispLSI 3192 design for general-purpose I/O when targeting the ispLSI 6192 are:

2, 5, 8, 9, 11, 15, 17, 18, 21, 24, 26, 36, 38, 41, 44, 45, 47, 51, 53, 54, 57, 60, 62, 64, 66, 69, 72, 73, 75, 79, 81, 82, 85, 88, 90, 92, 94, 97, 100, 101, 103, 107, 109, 110, 113, 116, 118, 120 , 122, 125, 128, 129, 131, 135, 137, 138, 141, 144, 146, 156, 158, 161, 164, 165, 167, 171, 173, 174, 177, 180, 182, 184, 186, 189, 192, 193, 195, 199, 201, 202, 205, 208, 210, 212, 214, 217, 220, 221, 223, 227, 229, 230, 233, 236, 238, 240

Summary

The ispLSI 3192 to ispLSI 6192 conversion procedure stated here has been tested on multiple designs successfully. By following the above guidelines, a high rate of conversion success is possible. If you need a design example or if you have questions regarding this procedure, please contact a Lattice applications engineer.

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November 1996