Introduction to ispLSI® and pLSI® 3000 Family

Introduction

Lattice Semiconductor Corporation's (LSC) ispLSI and pLSI families are high-density and high-performance $E^2CMOS^®$ programmable logic devices. They provide design engineers with a superior system solution for integrating high-speed logic on a single chip.

The ispLSI and pLSI 3000 Families are the third generation to combine the performance and ease of use of PLDs with the density and flexibility of FPGAs. This family is ideal for high density designs, where integration of complete logic subsystems into a single device is necessary.

The ispLSI family incorporates Lattice Semiconductor's innovative in-system programmable™ (ISP™) technology. ISP technology allows for real-time programming, less expensive manufacturing and end-user feature reconfiguration.

E^2CMOS technology features reprogrammability, the ability to program the device again and again to easily incorporate any design modifications. This same capability allows full parametric testability during manufacturing, which guarantees 100 percent programming and functional yield.

All necessary development tools are available from LSC and third-party vendors. Development tools offered range from LSC's low cost pDS® software, featuring Boolean entry in a graphical Windows™ based environment, to the pDS+™ family of Fitters that interface with third party development software packages. pDS+ systems support schematic capture, state machine, Boolean, and HDL Design entry. Designs can now be completed in hours as opposed to days or weeks.

ispLSI and pLSI 3000 Family

- ❑ 125 MHz System Performance
- ❑ 7.5 ns Pin-to-Pin Delay
- ❑ Deterministic Performance
- ❑ High Density (7,000 - 14,000 PLD Gates)
- ❑ 160-Pin to 304-Pin Package Options
- ❑ Flexible Easy-to-Use Architecture
- ❑ In-System Programmable (ispLSI)
- ❑ Boundary Scan (IEEE 1149.1)

ispLSI and pLSI Technology

- ❑ UltraMOS E^2CMOS — the PLD Technology of Choice
- ❑ Electrically Erasable/Programmable/ Reprogrammable
- ❑ 100% Tested During Manufacture
- ❑ 100% Programming Yield
- ❑ Fast Programming

ispLSI and pLSI Development Tools

- ❑ Low Cost, Fully Integrated pDS Design System for the PC
- ❑ HDL, VHDL, Boolean Equation, State Machine and Schematic Capture Entry
- ❑ pDS+ Support for Industry-Standard Third-Party Design Environments and Platforms
- ❑ Timing and Functional Simulation
- ❑ PC and Workstation Platforms

Introduction to ispLSI and pLSI 3000 Family

3000 Family Overview

The ispLSI and pLSI 3000 family of high-density devices address high-performance system logic designs implementing logic functions, ranging from registers, to counters, to multiplexers, to complex state machines.

With up to 14,000 PLD gates density, the ispLSI and pLSI 3000 Family provides a wide range of programmable logic solutions which meet tomorrow's design requirements today.
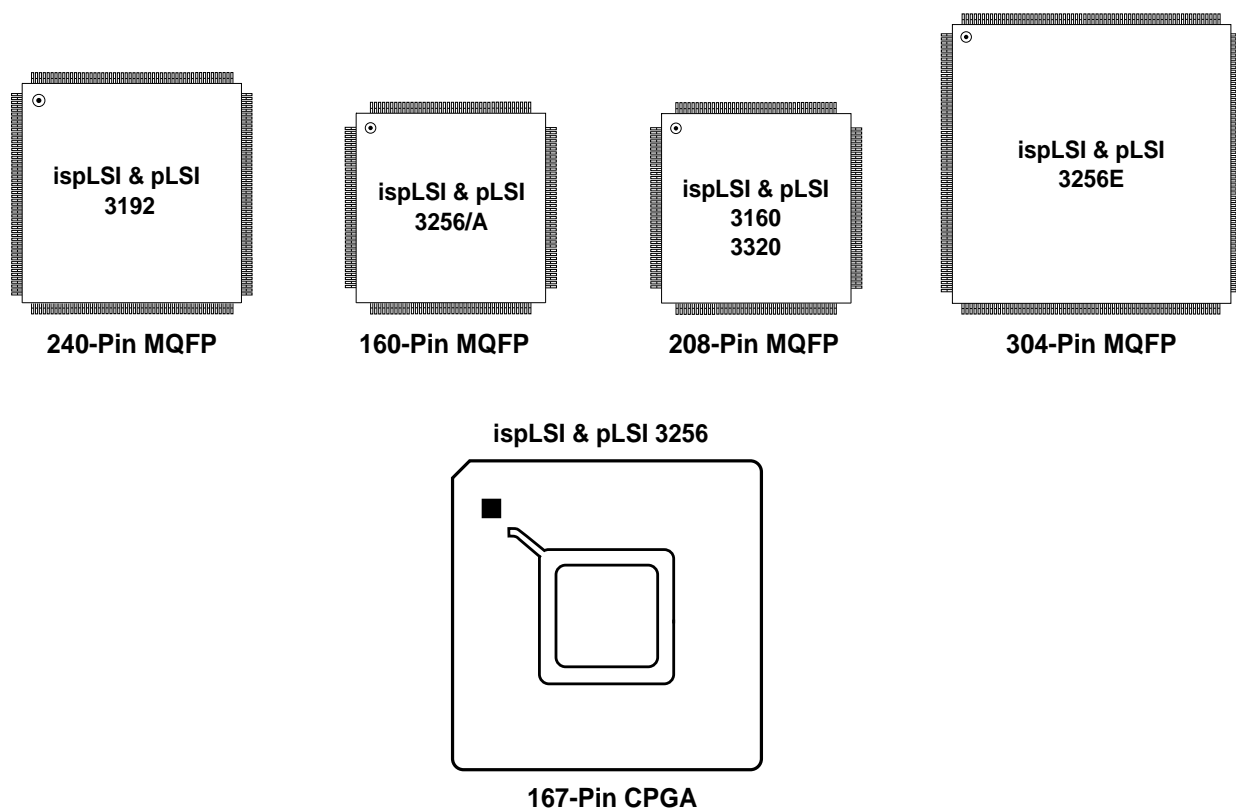
Each device contains multiple Generic Logic Blocks (GLBs), which are designed to maximize system flexibility and performance. A balanced ratio of registers and I/O cells provides the optimum combination of internal logic and external connections. A global interconnect scheme ties everything together, enabling utilization of up to 80% of available logic. Table 1 describes the family attributes.

Table 1. ispLSI and pLSI 3000 Family Attributes

Family Member	3160	3192	3256/A	3256E	3320
Density (PLD Gates)	7,000	8,000	11,000	12,000	14,000
Speed: f_{max} (MHz)	125	100	70/90	100	70
Speed: t_{pd} (ns)	7.5	10	15/12	10	15
Macrocells	160	192	256	256	320
Registers	320	384	384	512	480
Inputs + I/O	162	194	130	258	160
Pin/Package	208-pin MQFP	240-pin MQFP	160-pin MQFP 167-pin CPGA	304-pin MQFP	208-pin MQFP

Table 1-0003B/3K

Figure 1. 3000 Family Packages

ispLSI & pLSI 3192
240-Pin MQFP

ispLSI & pLSI 3256/A
160-Pin MQFP

ispLSI & pLSI 3160 3320
208-Pin MQFP

ispLSI & pLSI 3256E
304-Pin MQFP

ispLSI & pLSI 3256
167-Pin CPGA

0288-160C/3K

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