# Introduction to ispLSI® and pLSI® 6000 Family

## Introduction

Lattice Semiconductor Corporation's ispLSI® and pLSI® families are high-density, cell-based $E^2$CMOS® programmable logic devices. These devices provide design engineers with a superior system solution for integrating high-speed logic on a single chip.

The Lattice Semiconductor Corporation (LSC) ispLSI and pLSI 6000 Family combines high-density, general-purpose programmable logic with dedicated memory and register/counter modules. The result is a family of devices that support system-level integration of memory and logic functions with enhanced performance.

The ispLSI and pLSI 6000 family is ideal for high-density designs, where integration of complete logic subsystems into a single device is necessary. System applications include intelligent DMA controllers, serial controllers/ LAN controllers/UARTS, multimedia video/audio processors, video controllers, master bus interfaces and data acquisition controllers.

The ispLSI family incorporates Lattice Semiconductor's innovative in-system programmable™ (ISP™) technology. ISP technology allows for real-time programming, less expensive manufacturing and end-user feature reconfiguration.

LSC's $E^2$CMOS technology features reprogrammability, the ability to program a device again and again, to easily incorporate any design modifications. This capability allows full parametric testability during manufacturing, guaranteeing 100 percent programming and functional yield.

All necessary development tools are available from Lattice Semiconductor and third-party vendors. Development tools offered range from LSC's low-cost pDS® software, featuring Boolean entry in a graphical Windows™-based environment, to the pDS+™ family of Fitters that interface with third-party development software packages. pDS+ systems support schematic capture, state machine, Boolean, and HDL Design entry. Designs can now be completed in hours as opposed to days or weeks.

### ispLSI and pLSI 6000 Family

- ❑ 77 MHz System Performance
- ❑ 15 ns Pin-to-Pin Delay
- ❑ 20 ns Memory Access Time
- ❑ High Density General Purpose Programmable Logic Module (8,000 PLD Gates)
- ❑ 4K-Bit Memory FIFO/Dual-Port/Single-Port Memory Module
- ❑ 8 x 16-Bit Register/Counter Module
- ❑ 208-Pin Package with 157 User I/Os
- ❑ In-System Programmable (ispLSI)
- ❑ Boundary Scan Test (IEEE 1149.1 Standard)

### ispLSI and pLSI Technology

- ❑ UltraMOS $E^2$CMOS — the PLD Technology of Choice
- ❑ Electrically Erasable/Programmable/ Reprogrammable
- ❑ 100% Tested During Manufacture
- ❑ 100% Programming Yield
- ❑ Fast Programming

### ispLSI and pLSI Development Tools

- ❑ Low Cost, Fully Integrated pDS Design System for the PC
- ❑ HDL, VHDL, Boolean Equation, State Machine and Schematic Capture Entry
- ❑ pDS+ Support for Industry-Standard Third-Party Design Environments and Platforms*
- ❑ Timing and Functional Simulation
- ❑ PC and Workstation Platforms

*Note: pDS+ support in third-party CAE environments is scheduled for 1996 introduction. Contact Lattice Semiconductor for availability.

## 6000 Family Overview

The ispLSI and pLSI 6000 family of high-density devices address high-performance system integration needs, including registers, counters, multiplexers, complex state machines and memory all on a single device.

The first series of devices in the ispLSI and pLSI 6000 Family consists of the ispLSI and pLSI 6192FF, 6192DM and 6192SM. These devices vary only in the dedicated memory configuration: the 6192FF has a programmable 4K-Bit FIFO, the 6192DM has a dual-port memory, and the 6192SM has a single-port memory. Each device includes an 8 x 16-Bit programmable register/counter module and a 24 Twin GLB/192 macrocell programmable logic module based on the ispLSI and pLSI 3000 Family architecture.

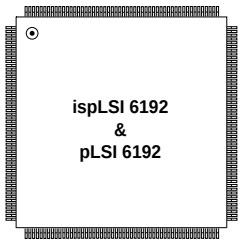
Each device contains multiple Generic Logic Blocks (GLBs) in the programmable logic module, which are designed to maximize system flexibility and performance. A balanced ratio of registers and I/O cells provides the optimum combination of internal logic and external connections. A global interconnect scheme ties all logic and memory together. An abundance of general-purpose and dedicated module I/O pins gives easy access to all resources externally. Table 1 describes the family attributes.

**Table 1. ispLSI and pLSI 6000 Family Attributes**

| Family Member | 6192FF | 6192SM | 6192DM |
|---|---|---|---|
| Memory Module | FIFO | Single-Port SRAM | Dual-Port SRAM |
| | Organization: 512 x 9 or 256 x 18 (FF, SM, DM); 256 x 9 or 128 x 18 (SM Only)<br>Speed: 20 ns Access Time | | |
| Register/Counter Module | Organization: 8 x 16-Bit Register/Counter/Timer/Shift Register<br>Speed: 125 MHz Counter Frequency | | |
| Programmable Logic Module | Organization: 192 Macrocell/24 Twin GLB<br>Speed: 15 ns Tpd/77 MHz Fmax | | |

6K Attributes

**Figure 1. 6000 Family Package**




**208-Pin MQFP**

0288-160C/6K



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