2000/V Family Architectural Description

ispLSI and pLSI 2000/V Family Introduction

The basic unit of logic of the ispLSI® and pLSI® 2000/V family is essentially the same as that of the ispLSI and pLSI 1000/E family. However, there are some specific architectural differences: global clock, I/O Cell and OE, and ORP structures. A functional block diagram of the 2032 device is shown in Figure 1. These architectural differences are described in detail below.

Global Clock Structure

The clock GLB distribution network of the 1000/E family has been eliminated and replaced by three dedicated global GLB clock input signals CLK0, CLK1, and CLK2. These three clocks are used for clocking all the GLBs configured as registers in the device. They feed directly to the GLB clock input via a clock multiplexer. CLK0 is associated with system clock pin Y0, CLK1 corresponds to system clock pin Y1, and CLK2 corresponds to system clock pin Y2. This is illustrated in Figure 2. The GLB global clocks do not have inversion capability, but all GLBs continue to have the capability of generating their own asynchronous clocks using the clock product term (PT12) with inversion capability. The GLB global clocks and the GLB product term clock feed to their corresponding clock multiplexer shown in Figure 3.

Figure 1. ispLSI 2032 Functional Block Diagram

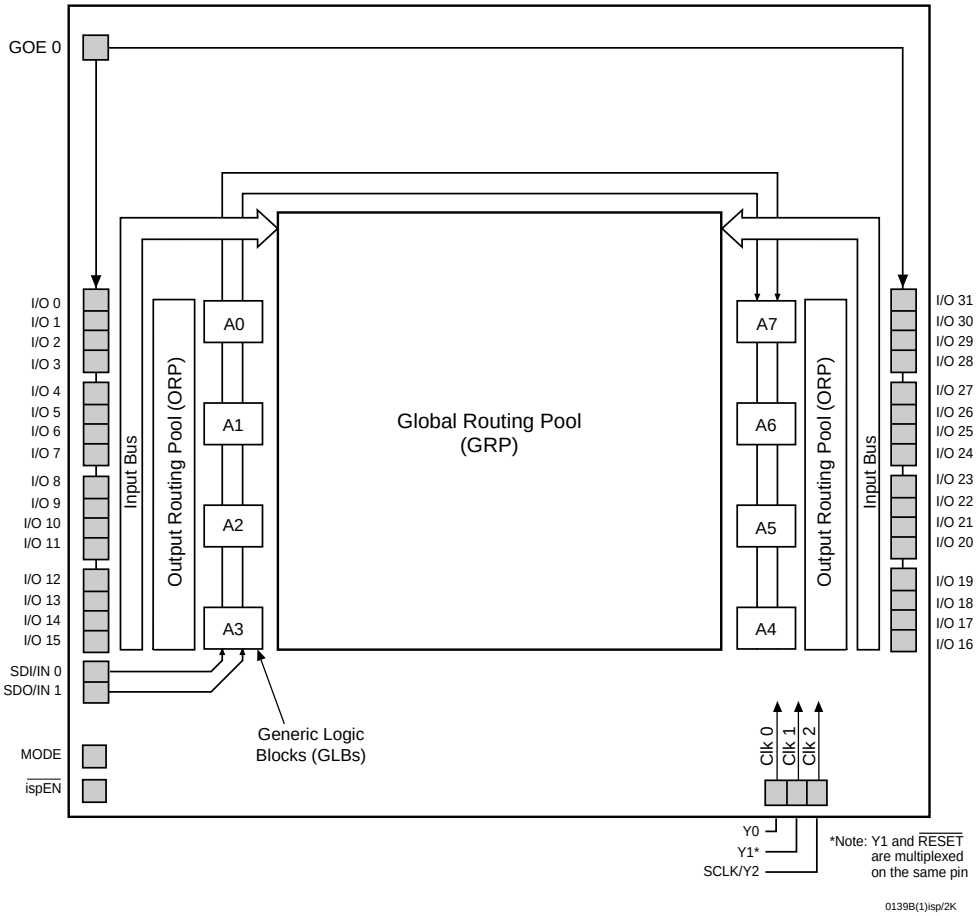
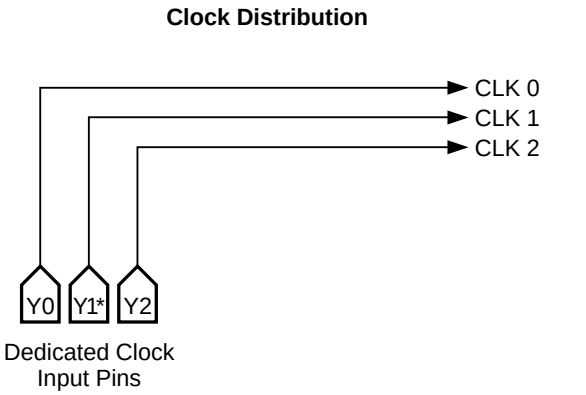


Figure 2. Global Clock Structure



*Note: Y1 and $\overline{\text{RESET}}$ are multiplexed on the same pin.

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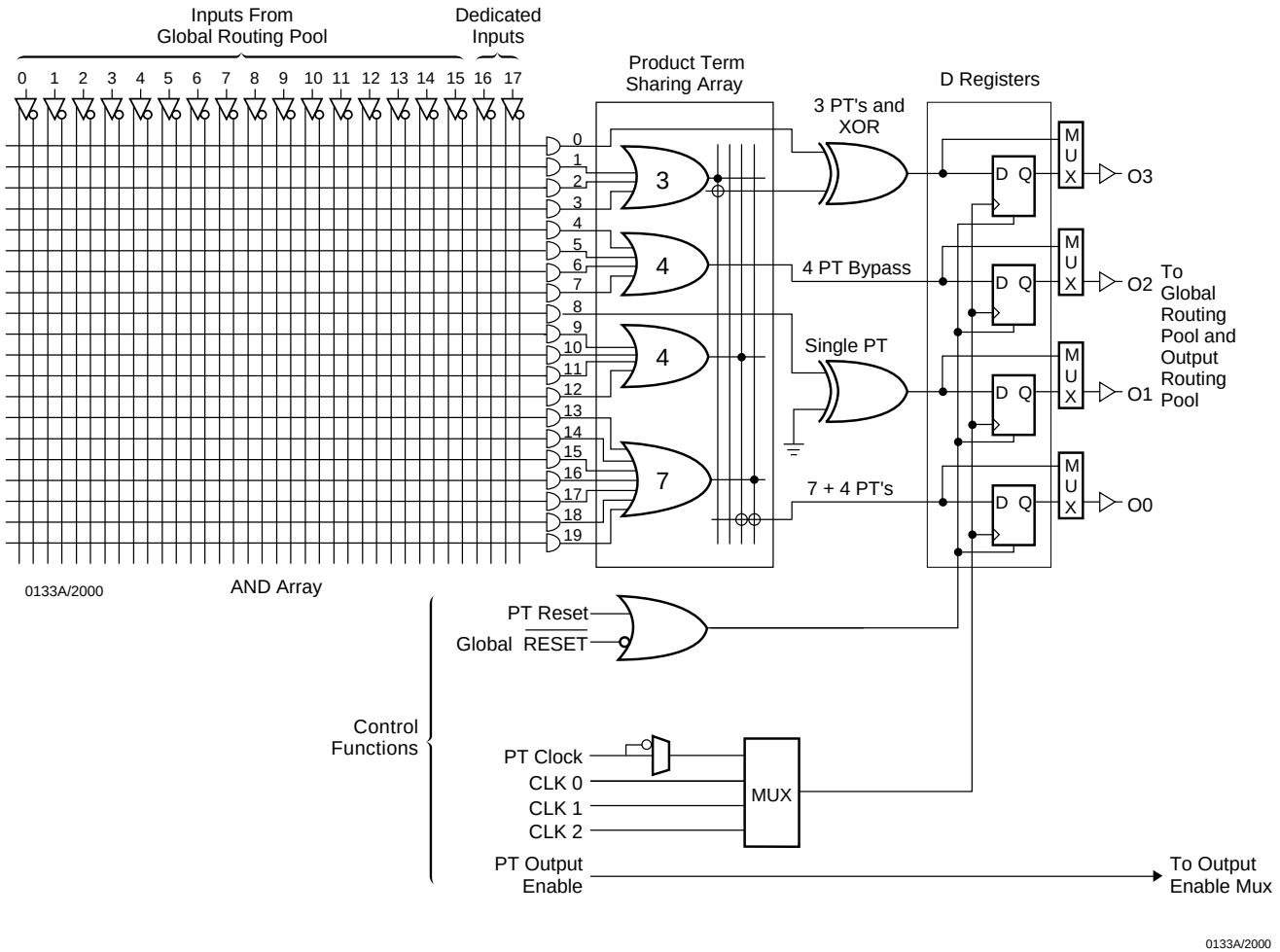
Figure 3. GLB with Clock Multiplexer Scheme

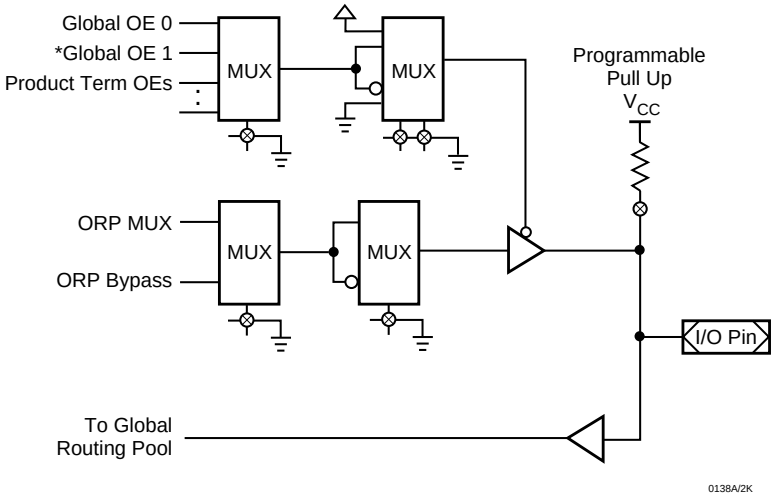


I/O Cell and OE Structure

The reconfigurable input register or latch has been removed to simplify the I/O cell architecture. Each I/O cell can be individually programmed to be a combinatorial input, combinatorial output, or a bidirectional I/O pin with 3-state control. With the simplified I/O cell architecture, the I/O clocks have also been removed. This is illustrated in Figure 4. The product term output enable (PTOE) signal is still generated within each GLB using product term 19. The PTOE is generated in one of the eight GLBs. In addition to the PTOE, there is a global output enable (GOE) pin which can control any of the device's 3-state output buffers. The multiplexing between the GOE and PTOE is illustrated in Figure 5. The 2032 device has one GOE and the 2064, 2096 and 2128 devices each have two GOEs.

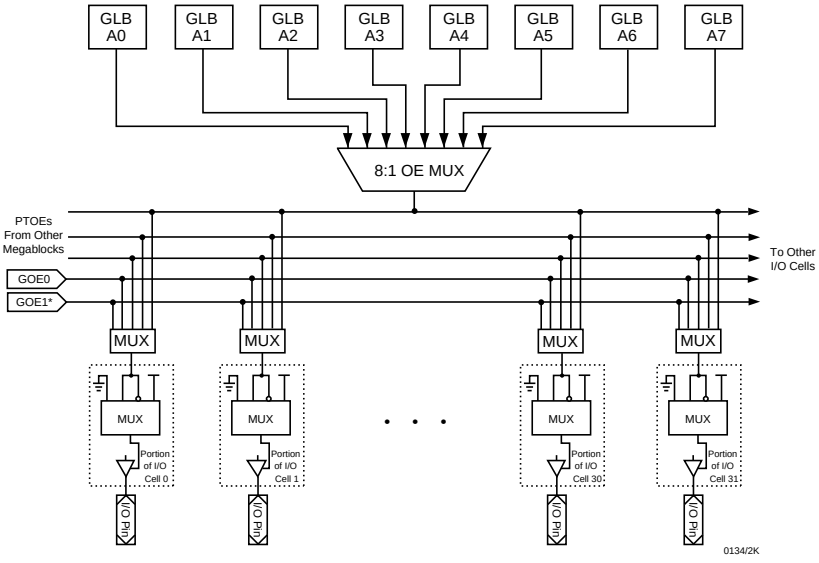
In addition to the standard output configuration, the outputs of the ispLSI and pLSI 2000V family are individually programmable either as standard totem-pole outputs or open-drain outputs.

Figure 4. ispLSI and pLSI 2000/V Family I/O Cell Architecture



⊗ Represents an E^2CMOS Cell.
* Except 2032

Figure 5. ispLSI and pLSI 2000/V Family Output Enable Controls



* Except 2032

Output Routing Pool (ORP)

For each ispLSI and pLSI 2000V device with full I/O, each megablock now contains two ORPs to increase output routability. A set of four GLBs is associated with one of the two ORPs within the megablock. The 16 outputs of the four GLBs within a megablock will feed to any of the 16 associated I/O cells. In the 1000/E family, the 32 GLB outputs feed only 16 associated I/O cells. In this device family, 32 GLB outputs of a megablock can feed 32 I/O cells. Output routability has doubled. This is illustrated in Figure 6. Each GLB output has an ORP bypass capability so more designs can have critical output signals. This is shown in Figure 7.

For ispLSI and pLSI 2000V devices with half I/O (one I/O pin per two GLB outputs), each megablock contains only one ORP which feeds 16 I/O pins.

Figure 6. ispLSI and pLSI 2000/V Family Output Routlng Pool (Full I/O Versions)

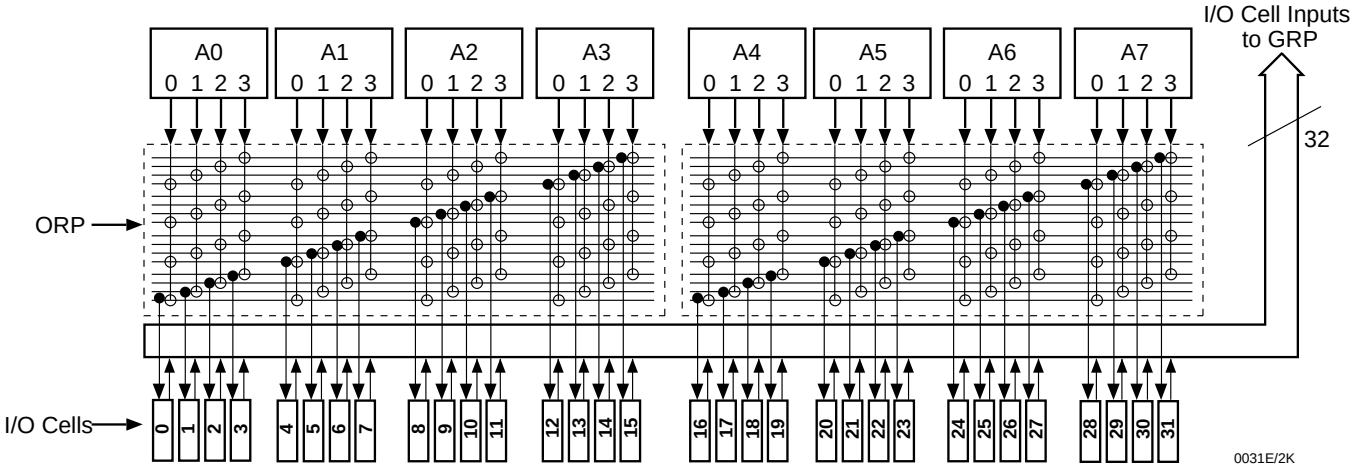
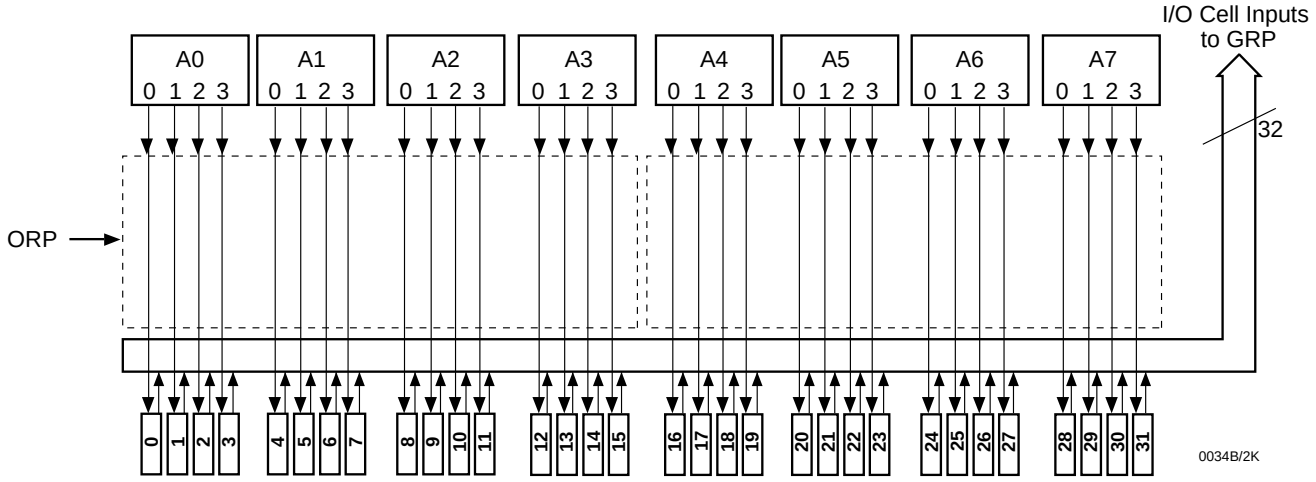


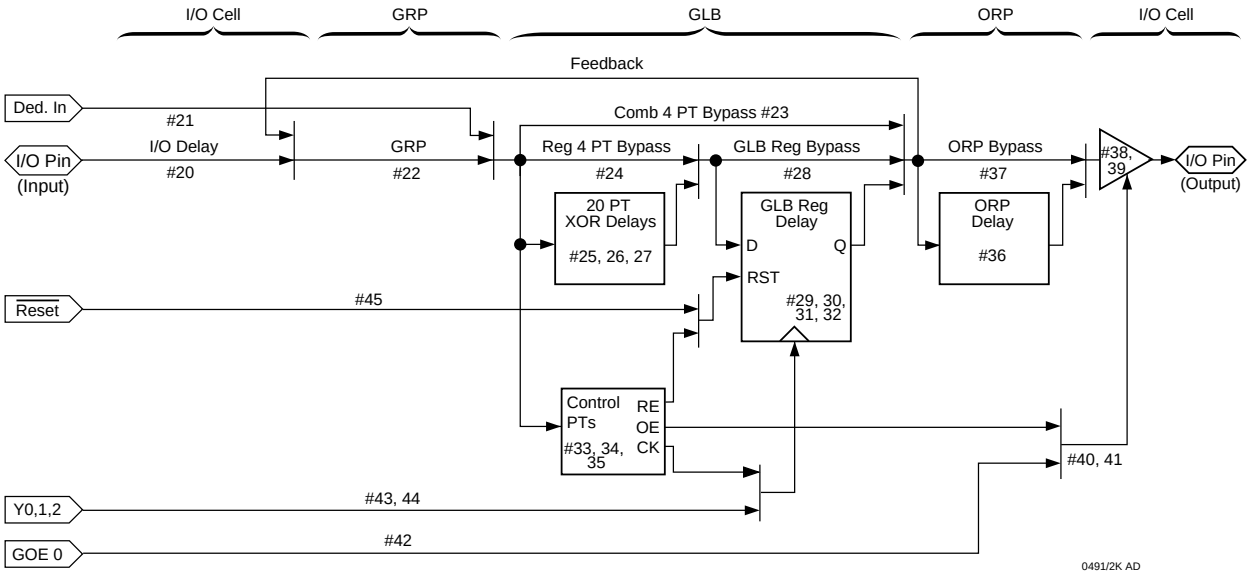
Figure 7. ispLSI and pLSI 2000/V Family Output Routlng Pool Showing Bypass



Timing Model

The task of determining the timing through the device is simple and straightforward. A device timing model is shown in Figure 8. To determine the time that it takes for data to propagate through the device, simply determine the path the data is expected to follow, and add the various delays together (Figure 8). Critical timing paths are shown in Figure 8, using data sheet parameters. Note that the Internal timing parameters are given for reference only, and are not tested. External timing parameters are tested and guaranteed on every device.

Figure 8. ispLSI and pLSI 2032 Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

tsu = Logic + Reg su - Clock (min)
= (**t**io + **t**grp + **t**20ptxor) + (**t**gsu) - (**t**io + **t**grp + **t**ptck(min))
= (#20+ #22+ #26) + (#29) - (#20+ #22+ #35)
1.9 ns = (1.1 + 1.3 + 5.1) + (0.3) - (1.1 + 1.3 + 2.9)

th = Clock (max) + Reg h - Logic
= (**t**io + **t**grp + **t**ptck(max)) + (**t**gh) - (**t**io + **t**grp + **t**20ptxor)
= (#20+ #22+ #35) + (#30) - (#20+ #22+ #26)
1.4 ns = (1.1 + 1.3 + 5.2) + (3.0) - (1.1 + 1.3 + 5.1)

tco = Clock (max) + Reg co + Output
= (**t**io + **t**grp + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
= (#20+ #22+ #35) + (#31) + (#36 + #38)
9.1 ns = (1.1 + 1.3 + 5.2) + (0.7) + (1.3 + 1.2)

Table 2-0042-16/2K AD

1. Calculations are based upon timing specifications for the ispLSI and pLSI 2032-135L.

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