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# ***ispLSI® and pLSI® 1000/E Families***

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## **Introduction**

Lattice Semiconductor Corporation's (LSC) ispLSI and pLSI families are high-density and high-performance E<sup>2</sup>CMOS<sup>®</sup> programmable logic devices. They provide design engineers with a superior system solution for integrating high-speed logic on a single chip.

The ispLSI and pLSI 1000 and 1000E families combine the performance and ease of use of PLDs with the density and flexibility of FPGAs.

The ispLSI and pLSI 1000 and 1000E families are ideal for designs requiring high speeds with highly integrated logic.

The ispLSI family incorporates Lattice Semiconductor's innovative in-system programmable<sup>™</sup> (ISP<sup>™</sup>) technology. ISP technology allows for real-time programming, less expensive manufacturing and end-user feature reconfiguration.

E<sup>2</sup>CMOS technology features reprogrammability, the ability to program the device again and again to easily incorporate any design modifications. This same capability allows full parametric testability during manufacturing, which guarantees 100 percent programming and functional yield.

All necessary development tools are available from LSC and third-party vendors. Development tools offered range from LSC's low cost pDS<sup>®</sup> software, featuring Boolean entry in a graphical Windows<sup>™</sup> based environment, to the pDS+<sup>™</sup> family of Fitters that interface with third party development software packages. Design systems interfacing with pDS+ Fitters feature schematic capture, state machine and HDL design entry. Designs can now be completed in hours as opposed to days or weeks.

## **ispLSI and pLSI 1000 and 1000E Families**

- ❑ 125 MHz System Performance
- ❑ 7.5 ns Pin-to-Pin Delay
- ❑ Deterministic Performance
- ❑ High Density (2,000-8,000 PLD Gates)
- ❑ 44-Pin to 133-Pin Package Options
- ❑ Flexible Architecture
- ❑ Easy-to-Use
- ❑ In-System Programmable (ispLSI)

## **ispLSI and pLSI Technology**

- ❑ UltraMOS E<sup>2</sup>CMOS — the PLD Technology of Choice
- ❑ Electrically Erasable/Programmable/Reprogrammable
- ❑ 100% Tested During Manufacture
- ❑ 100% Programming Yield
- ❑ Fast Programming

## **ispLSI and pLSI Development Tools**

- ❑ Low Cost, Fully Integrated pDS Design System for the PC
- ❑ pDS+ Support for Industry-Standard Third-Party Design Environments and Platforms
- ❑ HDL, VHDL, Boolean Equation, State Machine and Schematic Capture Entry
- ❑ Timing and Functional Simulation
- ❑ PC and Workstation Platforms

# Introduction to ispLSI and pLSI 1000/E Families

## 1000 and 1000E Families Overview

The ispLSI and pLSI 1000 and 1000E families of high-density devices address high-performance system logic needs, ranging from registers, to counters, to multiplexers, to complex state machines.

With PLD densities ranging from 2,000 to 8,000 gates, the ispLSI and pLSI 1000 and 1000E families provide a wide range of programmable logic solutions which meet tomorrow's design requirements today.

Each device contains multiple Generic Logic Blocks (GLBs), which are designed to maximize system flexibility and performance. A balanced ratio of registers and I/O cells provides the optimum combination of internal logic and external connections. A global interconnect scheme ties everything together, enabling utilization of up to 80% of available logic. Table 1 describes the family attributes.

**Table 1. ispLSI and pLSI 1000E Family Attributes**

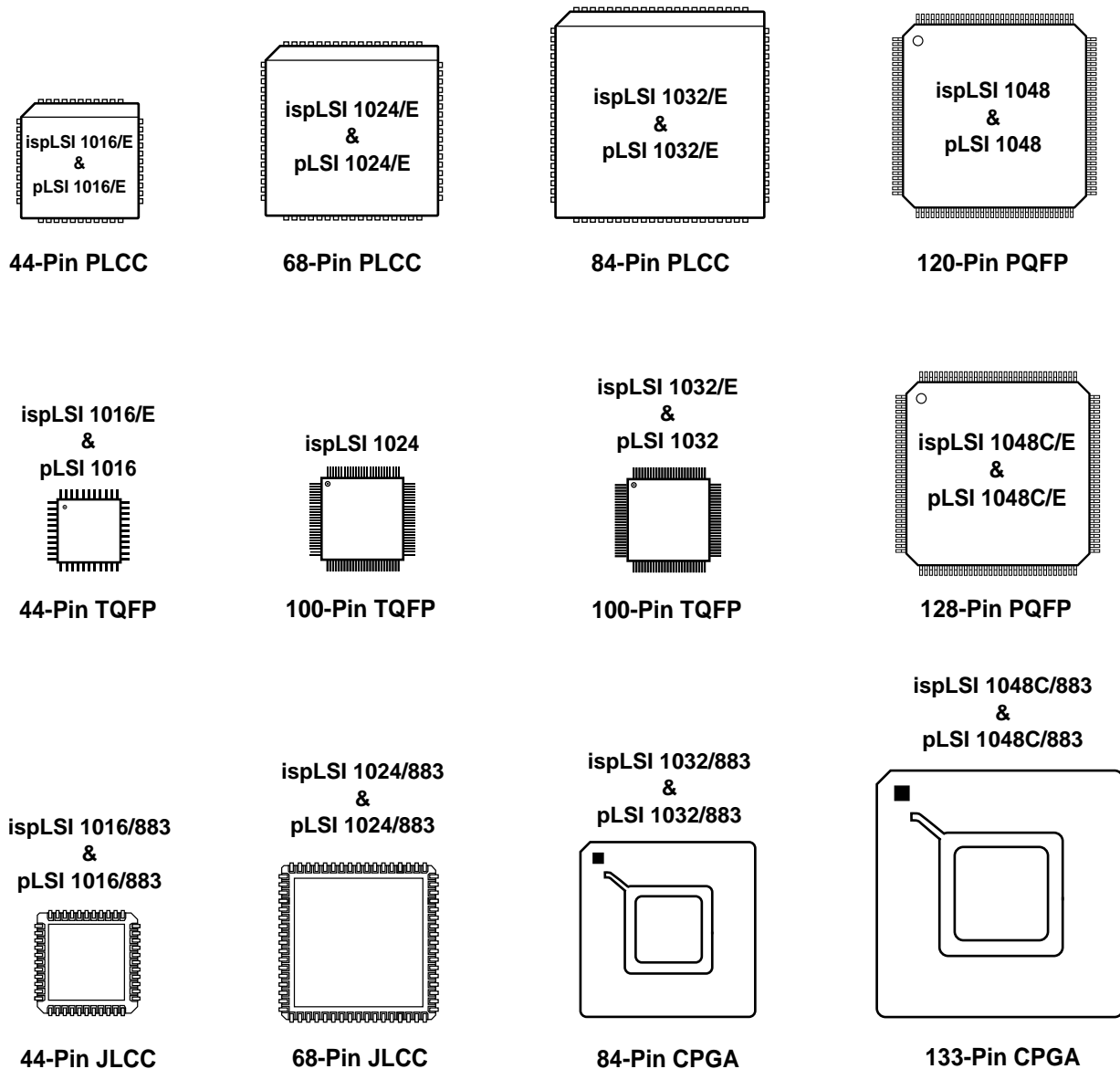
Family Member	1016/1016E	1024	1032/1032E	1048/1048C/1048E
Density (PLD Gates)	2,000	4,000	6,000	8,000
Speed: $f_{max}$ (MHz)	125	125	125	90
Speed: $t_{pd}$ (ns)	7.5	7.5	7.5	10
GLBs	16	24	32	48
Registers	96	144	192	288
Inputs + I/O	36	54	72	106*/110
Pin/Package	44-pin PLCC 44-pin TQFP 44-pin JLCC	68-pin PLCC 100-pin TQFP 68-pin JLCC	84-pin PLCC 100-pin TQFP 84-pin CPGA	120-pin PQFP* 128-pin PQFP 133-pin CPGA

\* ispLSI/pLSI 1048 Only

IK/E Attributes

# Introduction to ispLSI and pLSI 1000/E Families

Figure 1. 1000/E Family Packages



Pkgs. 1K Intro/2



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