░░ Lattice™
Semiconductor Corporation

pDS+™ Synopsys Software

Features

- **ispLSI® AND pLSI® DEVELOPMENT SYSTEM**
  - — **Supports ispLSI and pLSI 1000/E and 2000**
  - — **Upgrade to Support ispLSI and pLSI 3000**

- **SUPPORTS SYNOPSYS DESIGN COMPILER AND FPGA COMPILER TOOLS**
  - — **Lattice Semiconductor Corporation (LSC) Synopsys Technology Library for Synthesis**

- **DESIGN ENTRY USING VHDL OR VERILOG-HDL**
  - — **High-Level Language Entry**
  - — **Optimized Functions for Direct Instantiation**
  - — **Direct Path to pDS+ Synopsys Fitter**

- **LATTICE SEMICONDUCTOR pDS+™ SYNOPSYS FITTER**
  - — **Automated Device Fitter Ensures High Utilization and Performance**
  - — **Efficient Design Optimization and Minimization**
  - — **Automatic Partitioning with High Utilization**
  - — **Export Verilog and SDF for Verilog Simulation**
  - — **Export Wire File for Viewsim Simulation**

- **SUPPORTS CADENCE CONCEPT, VIEWLOGIC VIEWDRAW, AND MENTOR GRAPHICS DESIGN ARCHITECT SCHEMATIC CAPTURE TOOLS**
  - — **Design Import via Synopsys-Generated EDIF Design Netlist**
  - — **Design Property Entry Using Viewlogic, Cadence Concept or Mentor Graphics Tools**

- **DESIGN VERIFICATION WITH POPULAR THIRD-PARTY SIMULATORS, INCLUDING:**
  - — **VSS from Synopsys**
  - — **Verilog-XL™ Simulation from Cadence**
  - — **Viewsim Simulation from Viewlogic**
  - — **Quicksim II From Mentor Graphics**

- **STATIC TIMING ANALYSIS**
  - — **Design Time Static Timing Analyzer from Synopsys**

- **INDUSTRY STANDARD PROGRAMMING FILE GENERATION**
  - — **Standard JEDEC Fuse Map**

- **IN-SYSTEM PROGRAMMING SUPPORT**
  - — **ispCODE™ C Source Routines Included**
  - — **ISP Daisy Chain Download (PC)**
  - — **ispATE™ Board Test Programming Utility**

- **PLATFORMS SUPPORTED**
  - — **Sun O/S 4.x**
  - — **HP O/S UX 9.x and Above**

Introduction

The pDS+ Synopsys Fitter and Libraries from Lattice Semiconductor offer a powerful solution to fit high density logic designs into Lattice's ispLSI and pLSI devices.

Synopsys offers synthesis tools, called Design Compiler and FPGA Compiler, which use Verilog HDL or VHDL input formats for design entry. The Synopsys Synthesis Libraries support both Design Compiler and FPGA Compiler design environments.

Design entry is made simple by using device independent Verilog HDL or VHDL design languages. These designs are then synthesized by the Design Compiler or the FPGA Compiler, using Synopsys synthesis libraries, into an EDIF netlist.

A direct path from Synopsys into the pDS+ Synopsys fitter, using an EDIF netlist with an attribute file for fitter and design controls can also be used or the EDIF netlist/schematic can be imported into Cadence Concept, Viewlogic, or Mentor Graphics schematic environments. For more details, refer to the Design Flows section of this datasheet.

pDS+ Synopsys Fitter

The pDS+ Synopsys Fitter for ispLSI and pLSI devices is executed as a standalone program, using the EDIF output from Synopsys, Cadence Concept, Mentor Graphics Design Architect or wire files from Viewlogic as input. The pDS+ Synopsys Fitter provides hands-off design implementation through intelligent design optimization, logic partitioning, automatic place & route and fusemap generation in standard JEDEC format. Timing simulation input files for VSS, Verilog XL, Quicksim II, Viewsim and others are generated by the Fitter when requested by the user.

Design Optimization and Logic Minimization

The pDS+ Synopsys Fitter uses proprietary logic synthesis algorithms targeted for device-specific features. The fitter performs a thorough design optimization, utilizing logic minimization, product term sharing and XOR functions wherever necessary. In addition, the pDS+ Synopsys Fitter supports multiple fitting strategies to obtain the best device utilization and performance.

pDS+ Synopsys Macro Library

The Synopsys Synthesis Libraries come complete with a library of over 300 high level functions to simplify design entry. These macros enable the design engineer to use familiar predefined functions to build a design. Direct instantiation of these functions is provided to enhance device performance and utilization.

Figure 3. Macro Summary

Macro Type	Quantity
AND/NAND	29
OR/NOR	24
XOR/XNOR	12
I/Os	89
Flip-Flops	39
Latches	30
Arithmetic	33
Counters	65
Shift Registers	15
Miscellaneous	45

Automatic Partitioning

The pDS+ Synopsys Fitter incorporates a powerful Automatic Partitioner for hands-free synthesis of a design into Generic Logic Blocks (GLBs). The partitioner takes full advantage of the device's powerful features such as the hard XOR and product term sharing. The internal XOR can be utilized for Arithmetic functions, T-Type flip-flops, and on & off set optimization functions. The partitioner also makes extensive use of product term sharing. Product term sharing allows the Fitter to efficiently use device resources by sharing product terms across multiple logic functions. These features combine to maximize device resource utilization and increase design performance.

Automatic Place and Route

Automatic place and route eliminates the need for manual editing and accelerates the design cycle. The Router automatically generates pinouts based on the optimal design implementation or user assigned pinouts.

The Extended Route option performs a comprehensive route to maximize device resource utilization and ensure efficient design implementation. The result is that small design changes won't cause expensive PC board re-work.

Design Parameter Control

The pDS+ Synopsys Fitter offers extensive design control at the design entry level, letting the user optimize the design for maximum utilization and/or speed. All of the controls are specified using "Attributes" in the design property and parameter files. These controls fall into two categories:

— Fitter Controls
— Design Implementation Controls
    — Net Attributes
    — Pin Attributes
    — Path Attributes
    — Symbol Attributes

Fitter Control Options

Special properties can be passed to the pDS+ Synopsys Fitter providing complete control over critical design considerations. Fitter control over design partitioning and routing optimizes the design for speed and/or device utilization.

Feature	Description
PART	Determines device type to be used.
PARAM_FILE	Allows user to specify attributes in a text file.
STRATEGY	Choice of AREA (default), DELAY or NO_OPTIMIZE. AREA optimizes device space, DELAY keeps GLB levels to a minimum and NO_OPTIMIZE does not reduce equations.
USE_GLOBAL_RESET	Causes global reset to use dedicated routing for reset.
MAX_GLB_OUT	Specifies maximum number of outputs from a GLB. Default is 4.
MAX_GLB_IN	Controls maximum number of inputs to a GLB. Default is 16 for 1K and 2K devices and 24 for 3K devices.
EFFORT	Controls optimization of partitioner.
EXTENDED_ROUTE	Choice of OFF (fixed) or ON (extended, default).
PIN_FILE	Specifies locked pin assignments.

Design Implementation Controls

Design implementation controls are used for changing such design parameters as security and pull-ups. Some of the implementation controls are:

Feature	Description
ISP	Instructs Router to reserve in-system programming pins.
ISP_EXCEPT_Y2	Reserves all ISP pins except Y2 (ispLSI and pLSI 1016/E and 2032 only).
Y1_AS_RESET	Uses Y1 clock pin on ispLSI and pLSI 1016/E and 2032 as a global reset pin.
SECURITY	Sets the device security cell to prevent unauthorized fuse map read back.

Net Attributes

These properties control how the design is mapped into the specified features of the target device:

Feature	Description
CLK0-CLK2	Assigns a CLK signal to a dedicated CLK line.
IOCLK0-IOCLK1	Assigns a CLK signal to a dedicated IOCLK line if single fanout input pin.
FASTCLK	Fitter assigns CLK signal to CLK0-CLK2 or IOCLK0-IOCLK1.
SLOWCLK	Assigns the CLK signal to a GLB product term CLK.
PRESERVE	Prevents logic minimization on specified nets.
GROUP	Suggests grouping of functions in a GLB.

Pin Attributes

Feature	Description
CRIT	Specifies Output Routing Pool Bypass to minimize delay.
SLOWSLEW	Assigns slow slew rate on a specific I/O cell.
LOCK	Assigns device I/O pins to design I/O ports.
PULLUP	Specifies internal pull-up resistors.

Path Attributes

The following properties specify paths in the design that have special fitting requirements:

| Feature	Description
SAP/EAP	Defines asynchronous paths to prevent signal duplication.
SCP/ECP	Defines critical paths to reduce delays.
SNP/ENP	Defines logic paths for no logic minimization.

Symbol Attributes

Feature	Description
REGTYPE	Determines where a register is to be placed (IOC or GLB).
PROTECT	Prevents removal of a primitive or a macro during minimization.
OPTIMIZE	Selects either hard or soft macros.

Parameter File

The pDS+ Synopsys Fitter provides the ability to use a parameter file (design.par) feature which helps designers eliminate guesswork and optimize the designs for the right devices. It allows the user to try a number of design implementation options using all of the fitter control options in a batch mode. The parameter file instructs the partitioner and the router to maximize both device utilization and performance.

Figure 1. pDS+ Synopsys Design Flow

Figure 2. pDS+ Cadence Flow with Synopsys Option
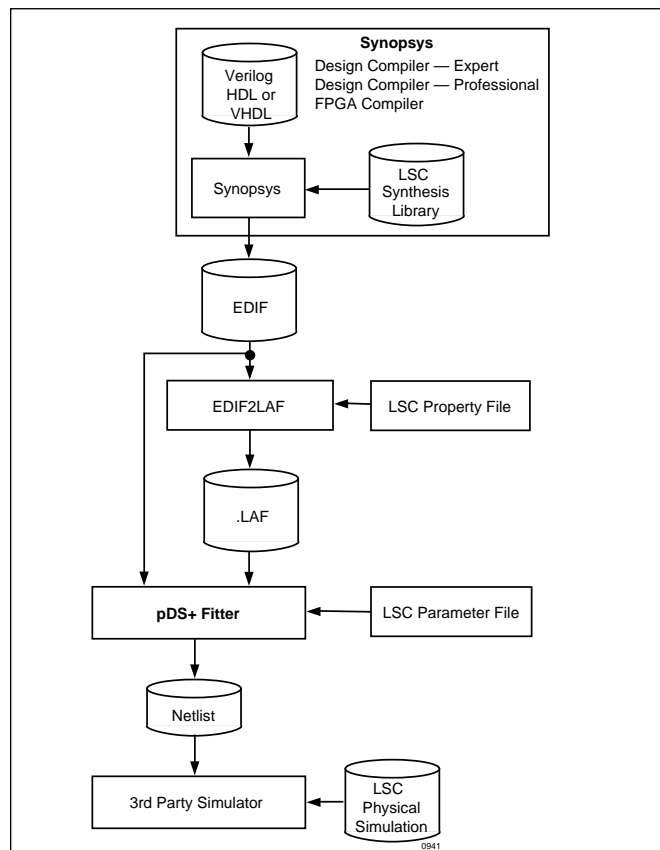
Property File

The pDS+ Synopsys Fitter also accepts a property file (design.prp) which allows the designer to assign specific features to signals and nets using all of the design attributes available. The property file helps guide the fitter in implementing the design in the best way.
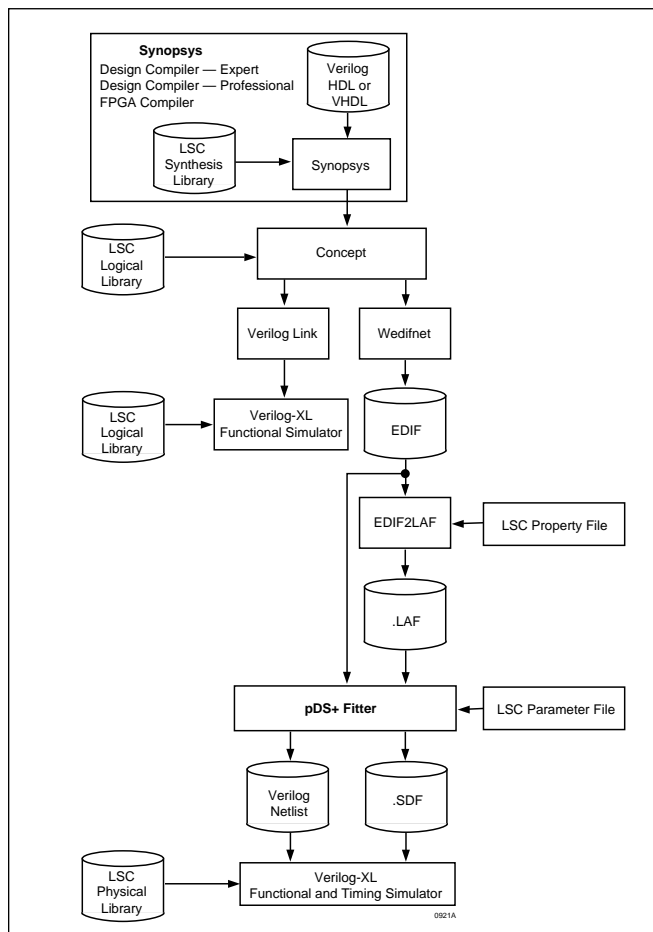
Design Verification

The pDS+ Synopsys Fitter provides a post route design file for optional timing simulation. pDS+ Synopsys software offers complete post route design verification using optional timing simulators, including VHDL simulation using Synopsys' VSS. The pDS+ Synopsys Fitter generates the files required for third-party simulation, and generates a "sim" file which can be used for simulaton with behavioral simulation models from Synopsys Logic Modeling Division.

Fusemap Generation

The pDS+ Synopsys software generates a device fuse map in standard JEDEC format. A security feature offers

protection of proprietary designs from unauthorized duplication. The Fitter also appends any design test vectors in JEDEC format to the device fusemap thus facilitating a quick, easy functional verification of a programmed device.

Design Flows

pDS+ Synopsys Design Flow

Designers can compile designs described in VHDL or Verilog HDL using Synopsys Design Compiler or FPGA Compiler and the Lattice Synopsys Synthesis Libraries. The EDIF netlist file from Synopsys can be read directly by the pDS+ Synopsys Fitter. If a property file (design.prp) exists, the EDIF2LAF translator must be run before the fitter is executed.

Design attributes and fitter control options can also be added to the design.par file.

Figure 3. pDS+ Mentor Graphics Design Flow with Synopsys Option

Figure 4. pDS+ Viewlogic Design Flow with Synopsys Option
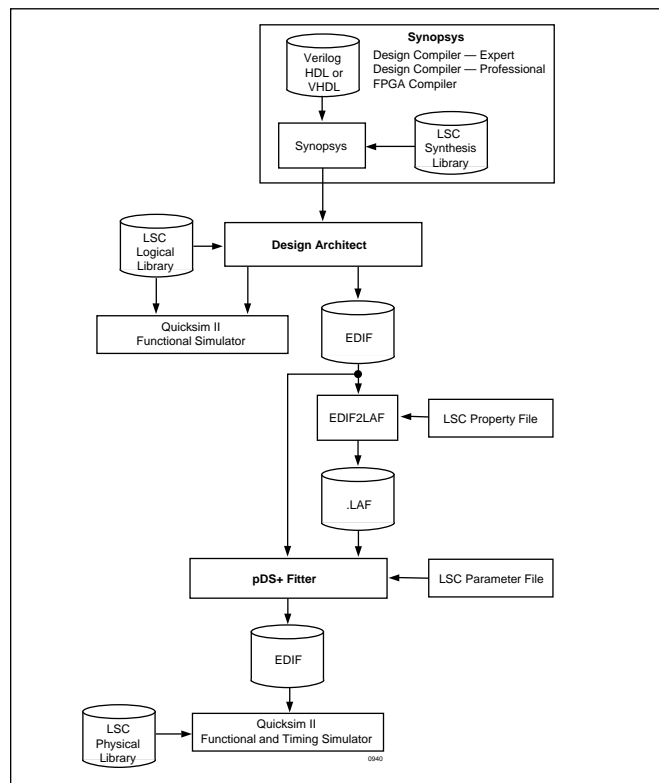
The EDIF output can then be read by the pDS+ Synopsys Fitter where the design is automatically partitioned, routed and a JEDEC file for device programming is generated (see Figure 1).
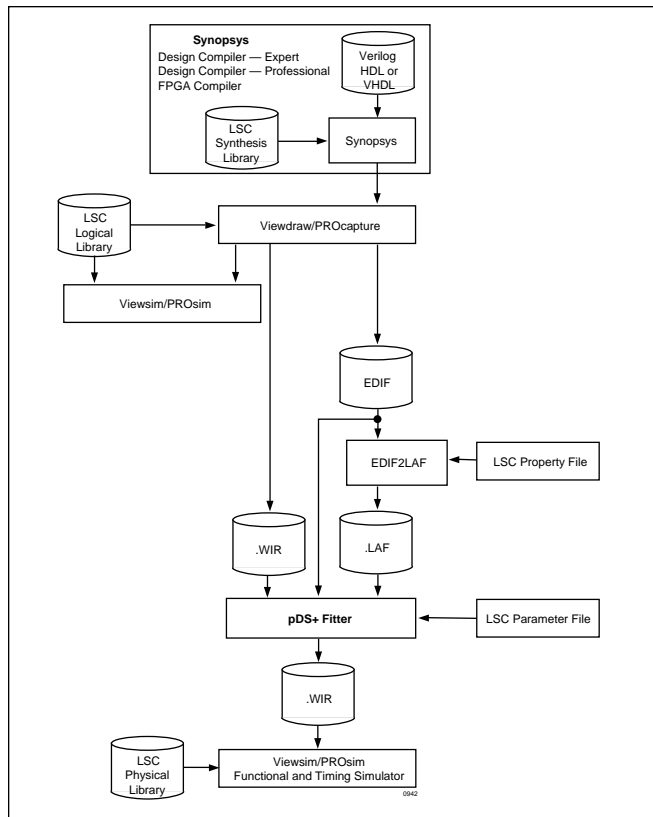
The VSS (VHDL) Simulation Library can be used for post-route timing simulation.

pDS+ Cadence Design Flow with Synopsys Option

Designers can compile designs described in VHDL or Verilog HDL using Synopsys Design Compiler or FPGA Compiler and the LSC Synopsys Synthesis Libraries. The EDIF netlist file or schematic file from Synopsys can be read into Concept, the Cadence schematic capture tool. Design attributes and fitter control options can be added in the schematic. The EDIF output from Concept can then be read by the pDS+ Cadence Fitter where the design is automatically partitioned, routed and a JEDEC file for device programming is generated.

Verilog-XL simulation library can be used to do both pre and post route simulation (see Figure 2).

pDS+ Mentor Graphics Design Flow with Synopsys Option

Designers can compile designs described in VHDL or Verilog HDL using Synopsys Design Compiler or FPGA Compiler and the LSC Synopsys Synthesis Libraries. Designs described in VHDL can also be compiled with the LSC Autologic Synthesis library.

The Mentor Graphics Design Architect (DA) can read the design database from the Synopsys synthesis tools.

The EDIF output from DA can then be read by the pDS+ Mentor Fitter where the design is automatically partitioned, routed and a JEDEC file for device programming is generated.

Quicksim II simulation libraries can be used to do both pre and post route simulations (see Figure 3).

pDS+ Viewlogic Design Flow with Synopsys Option

Designers can compile designs described in VHDL or Verilog HDL with Synopsys and the LSC Synopsys Synthesis Libraries. The EDIF netlist file or schematic file

from Synopsys can be read into Viewdraw, the Viewlogic schematic capture tool. Design attributes and fitter control options can be added in the schematic. The .WIR file from Viewdraw can then be read by the pDS+ Viewlogic Fitter where the design is automatically partitioned, routed and a JEDEC file for device programming is generated.

Pre and post route simulations can be performed using Viewsim (see Figure 4).

System Requirements (Sun Platform)

— Sun Sparc 4 and above
— Sun OS Version 4.x
— Open Windows 3.0
— 16 MB RAM with 30 MB Hard Disk Space
— Three-Button Mouse

System Requirements (HP Platform)

— HP 700 Workstation and Above
— HP O/S UX9.X and Above
— 16 MB RAM and 30 MB Hard Disk Space
— Three-Button Mouse

Programmer Support

All devices in the Lattice Semiconductor ispLSI device family can be programmed while installed on the target circuit board. In-system programming can be performed using an ispDOWNLOAD™ Cable and PC, by an on-board microprocessor or by ATE equipment during final board test. All LSC ispLSI and pLSI devices can be programmed using third-party programmers. These devices are currently supported by programmers from the following vendors:

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48

Programmer Vendor	Model
Logical Devices	Allpro 40
	Allpro 88
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30A/B
System General	TURPRO-1/FX

High pin-count socket adapters are available from Emulation Technology, EDI Corporation and PROCON.

Product Ordering Information

Product Code	Description
pDS1102-SN1	Viewlogic Viewsim and Viewdraw Libraries and Interface Files
pDS1131-SN1	VHDL and Verilog Simulation Libraries (SUN)
pDS1131-HP1	VHDL and Verilog Simulation Libraries (HP)
pDS1140-HP1	Lattice Semiconductor Synopsys Synthesis Libraries (HP)
pDS1140-SN1	Lattice Synopsys Synthesis Libraries
pDS1150-HP	Mentor Interface Kit (HP)
pDS1150-SN1	Mentor Interface Kit (Sun)
pDS1160-SN1	Cadence Libraries and Interface
pDS2101-SN1	pDS+ Viewlogic Fitter
pDS2101-3UP/SN1	3000 Family Upgrade for pDS+ Viewlogic Fitter
pDS2140-HP1	pDS+ Synopsys Fitter (HP)
pDS2140-3UP/HP1	3000 Family Upgrade for pDS+ Synopsys Fitter (HP)
pDS2140-SN1	pDS+ Synopsys Fitter and Libraries
pDS2140-3UP/SN1	3000 Family Upgrade for pDS+ Synopsys Fitter
pDS2150-HP1	pDS+ Mentor Fitter and Libraries (HP)
pDS2150-SN1	pDS+ Mentor Fitter and Libraries
pDS2150-3UP/HP1	3000 Family Upgrade for pDS+ Mentor Fitter
pDS2150-3UP/SN1	3000 Family Upgrade for pDS+ Mentor Fitter

pDS2160-SN1	pDS+ Cadence Fitter and Libraries
pDS2160-3UP/SN1	3000 Family Upgrade for pDS+ Cadence Fitter

Annual Maintenance**

pDS1102M-SN1	Maintenance for pDS1102-SN1
pDS1140M-HP1	Maintenance for pDS1140-HP1
pDS1140M-SN1	Maintenance for pDS1140-SN1
pDS1150M-HP1	Maintenance for pDS1150-HP1
pDS1150M-SN1	Maintenance for pDS1150-SN1
pDS1160M-SN1	Maintenance for pDS1160-SN1
pDS2101M-SN1	Maintenance for pDS2101-SN1
pDS2140M-HP1	Maintenance for pDS2140-HP1
pDS2140M-SN1	Maintenance for pDS2140-SN1
pDS2150M-HP1	Maintenance for pDS2150-HP1
pDS2150M-SN1	Maintenance for pDS2150-SN1
pDS2160M-SN1	Maintenance for pDS2160-SN1
pDS1131M-SN1	Maintenance for pDS1131-SN1
pDS1131M-HP1	Maintenance for pDS1131-HP1

**One year of maintenance is provided with every product purchase.

Warranty/Update Service

• 90-day warranty on disk media
• One-year maintenance support included with purchase
• Annual maintenance agreement available

Technical Support Assistance

Hotline:	1-800-LATTICE (Domestic)
	1-408-428-6414 (International)
BBS:	1-408-428-6417
FAX:	1-408-944-8450
email:	apps@latticesemi.com

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