6000 Family Architectural Description

ispLSI and pLSI 6000 Family Introduction

The ispLSI® and pLSI® 6192 devices are high-density, cell-based programmable logic devices that contain a dedicated Memory Module, a dedicated Register/Counter Module and an 8000-gate general-purpose Programmable Logic block. Output Routing Pools (ORP) and a Global Routing Pool (GRP) give complete interconnectivity between these elements. The dedicated modules have been added to enhance the functionality, performance and utilization of the device.

The ispLSI and pLSI 6192 is offered in three versions: the ispLSI and pLSI 6192FF (FIFO), 6192SM (Single Port RAM) and 6192DM (Dual Port RAM). All three devices employ the same general-purpose programmable logic module and register/counter module, with only the memory module functionality changing. The pinouts of the three devices are different only in the memory module control interface pins.

Memory Module

Lattice Semiconductor offers a dedicated dual-port FIFO module in the ispLSI and pLSI 6192FF devices. The FIFO is user configurable as a 256 x 18 or 512 x 9 block and is connected to the external world through dedicated FIFO I/O pins. The other data port of the FIFO goes to the GRP. A variety of FIFO control flags such as Full ($\overline{FF}$), Almost Full ($\overline{ALF}$), Almost Empty ($\overline{ALE}$) and Empty ($\overline{EF}$) are available as dedicated device outputs. These signals are also available as inputs to the GRP to facilitate use by on-chip logic.

The ispLSI and pLSI 6192SM feature a single-port memory module. The module can be organized either as a single 256 x 18 or 512 x 9 single port memory or as two smaller 128 x 18 or 256 x 9 single port memories. The external interface features memory address input pins (A0-A8), Read/Write (RWL/RWH), Chip Select ($\overline{CS}$), Output Enable ($\overline{OE}$) control lines, and 18 bidirectional data lines. The memory can be accessed from this external interface or from the internal GRP based on the user's design.

The ispLSI and pLSI 6192DM has functionality similar to the 6192SM, but access from the GRP or external pins is supported concurrently. Dedicated arbitration logic and Busy flags help to resolve issues arising from simultaneous access from both ports of the same memory location. The Busy signal from the external port ($\overline{BusyA}$) is available at a dedicated device pin.

Register/Counter Module

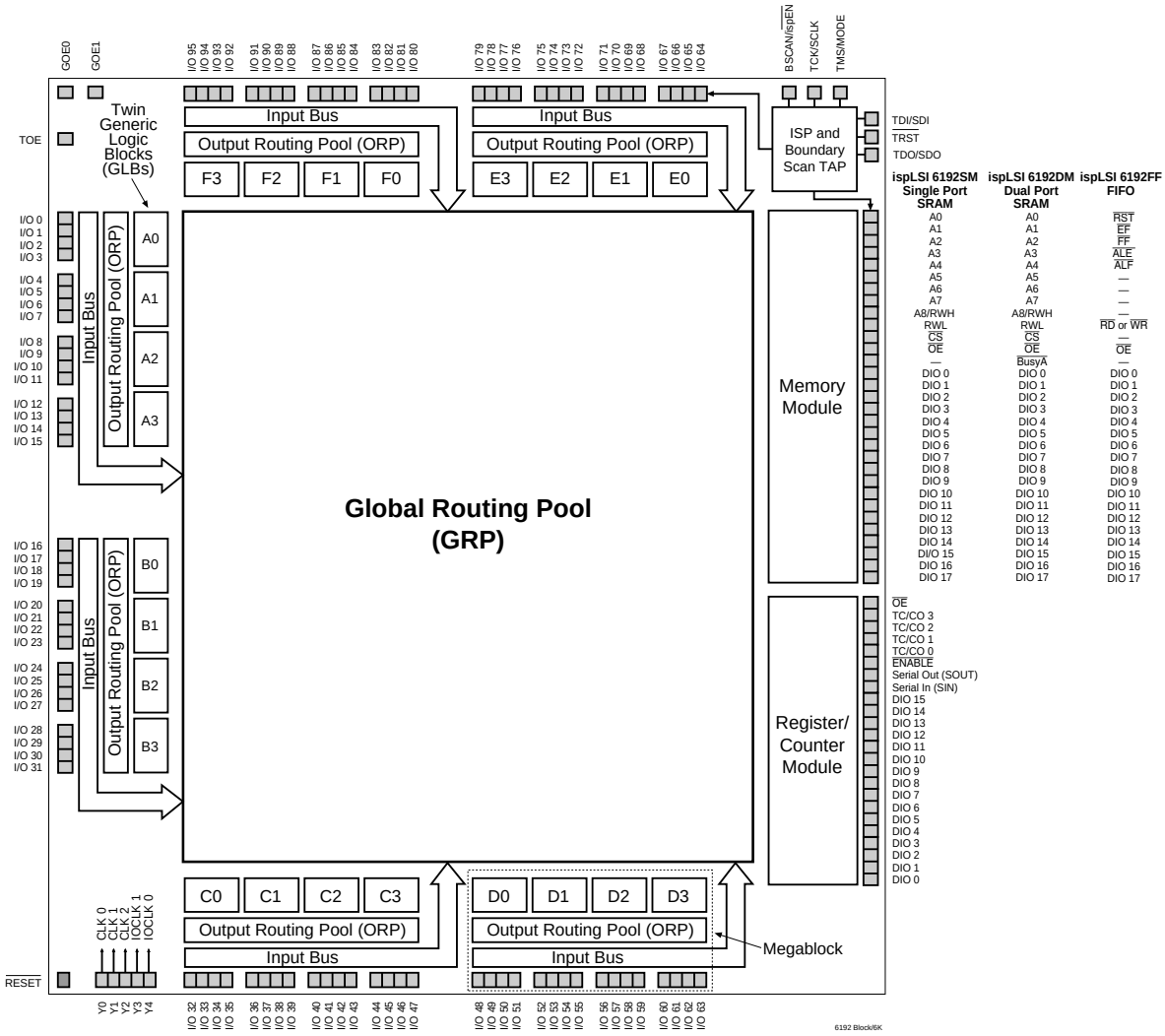
An additional feature of the ispLSI 6192 and pLSI devices is a dedicated Register/Counter module. Eight 16-bit blocks are available to function as registers or shift registers. In addition, four of these blocks can be programmed to operate as loadable Up/Down counters. These four blocks include carry-in and carry-out connections to allow counter cascading up to 64 bits. The

Table 1. ispLSI and pLSI 6192 Device Features

	Memory Module Options			Register/Counter Module	General Programmable Logic Module
Functions	FIFO 6192FF	Single-Port SRAM 6192SM	Dual-Port SRAM 6192DM	Programmable Register / Counter / Timer / Shift Register	Universal: Registered or Combinatorial
Organization	Programmable 512 x 9 or 256 x 18			Cascadeable 8 x 16 Bit Words	192 Macrocells
External Interface	18 I/O & 13 Control Pins			16 I/O & 8 Control Pin	96 I/O / 5 Clocks / 2 Global Output Enables
Performance	20ns Memory Access Time (Tacc)			125MHz Counter Frequency (Fcnt)	15ns Logic Delay (Tpd) 77MHz Frequency (Fmax)
Programmability	In-System Programmable				
Testability	IEEE 1149.1 Boundary Scan Test				
Package	208-Pin Metal Quad Flat Pack (MQFP)				

6000 Family Table.eps

Figure 1. ispLSI and pLSI 6192 Functional Block Diagram



ispLSI 6192SM Single Port SRAM	ispLSI 6192DM Dual Port SRAM	ispLSI 6192FF FIFO
A0	A0	$\overline{RST}$
A1	A1	$\overline{EF}$
A2	A2	$\overline{FF}$
A3	A3	$\overline{ALE}$
A4	A4	$\overline{ALF}$
A5	A5	—
A6	A6	—
A7	A7	—
A8/RWH	A8/RWH	—
RWL	RWL	$\overline{RD}$ or $\overline{WR}$
$\overline{CS}$	$\overline{CS}$	—
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
—	$\overline{BusyA}$	—
DIO 0	DIO 0	DIO 0
DIO 1	DIO 1	DIO 1
DIO 2	DIO 2	DIO 2
DIO 3	DIO 3	DIO 3
DIO 4	DIO 4	DIO 4
DIO 5	DIO 5	DIO 5
DIO 6	DIO 6	DIO 6
DIO 7	DIO 7	DIO 7
DIO 8	DIO 8	DIO 8
DIO 9	DIO 9	DIO 9
DIO 10	DIO 10	DIO 10
DIO 11	DIO 11	DIO 11
DIO 12	DIO 12	DIO 12
DIO 13	DIO 13	DIO 13
DIO 14	DIO 14	DIO 14
DI/O 15	DIO 15	DIO 15
DIO 16	DIO 16	DIO 16
DIO 17	DIO 17	DIO 17

$\overline{OE}$
TC/CO 3
TC/CO 2
TC/CO 1
TC/CO 0
$\overline{ENABLE}$
Serial Out (SOUT)
Serial In (SIN)
DIO 15
DIO 14
DIO 13
DIO 12
DIO 11
DIO 10
DIO 9
DIO 8
DIO 7
DIO 6
DIO 5
DIO 4
DIO 3
DIO 2
DIO 1
DIO 0

Note:
Since certain signal names are duplicated on Memory Module and Register/Counter Module pins ($\overline{OE}$, DIO), the notation:
$\overline{OE}$ (RAM)
$\overline{OE}$ (RC)
DIO (RAM)
DIO (RC)
will be used periodically in this data sheet to differentiate signals.

Register/Counter block also has a 16-bit data port connected to the GRP along with a variety of control inputs and status flag outputs.

Programmable Logic Module

The basic unit of general-purpose programmable logic on the ispLSI and pLSI 6192 devices is the Twin Generic Logic Block (Twin GLB™) labeled A0, A1....F3 in the block diagram. There are a total of 24 of these Twin GLBs in the ispLSI and pLSI 6192 devices. Each Twin GLB has 24 inputs, a programmable AND array and two OR/Exclusive-OR Arrays as well as eight outputs which can be configured independently to be combinatorial or registered. All Twin GLB logic inputs come from the GRP.

Four Twin GLBs, 16 I/O Cells and one ORP form a logic Megablock. The 16 I/O cells within a Megablock share one Product Term Output Enable and two Global Output Enable signals. The outputs of four Twin GLBs are connected to a set of 16 I/O cells by the ORP. The ispLSI and pLSI 6192 devices each contain six of these Megablocks.

The GRP has, as its inputs, the outputs from all of the Twin GLBs and all of the inputs from the bidirectional I/O cells as well as independent bidirectional data bus ports from the FIFO and Register/Counter blocks. Flag outputs from these modules as well as control inputs are also connected to the GRP. All these signals are made available to the inputs of the Twin GLBs. Delays through the GRP have been equalized to minimize timing skew and logic glitching.

GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other logic block on the device. The device has 96 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, a latched input, an output or a bidirectional I/O pin with 3-state control. Output signal levels are TTL compatible, and the output drivers can source 4mA and sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise. The devices are packaged in space saving 208-pin Metal Quad Flat Pack (MQFP) packages.

Clocks in the ispLSI and pLSI 6192 devices are provided through five dedicated clock pins. The five pins provide three clocks to the Twin GLBs and two clocks to the I/O cells.

In-System Programmability

The ispLSI 6192 devices also feature 5-Volt in-system programmability and in-system diagnostic capabilities. Consequently, the devices offer non-volatile “on-the-fly” reprogrammability of logic and memory to support truly reconfigurable systems.

Boundary Scan

The ispLSI and pLSI 6192 family also has Boundary Scan capability, consisting of dedicated cells connected between the on-chip system logic and the device’s input and output pins. All I/O pins have associated boundary scan registers, with 3-state I/O using three boundary scan registers and inputs using one. The device supports all IEEE 1149.1 mandatory instructions, which include BYPASS, EXTEST and SAMPLE.

For More Information

For a full description of the ispLSI and pLSI 6000 cell-based architecture, see the ispLSI and pLSI 6192 data sheet.

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