Lattice™ Semiconductor Corporation

ispLSI® and pLSI® 1048E

High-Density Programmable Logic

Features

- **HIGH DENSITY PROGRAMMABLE LOGIC**
  - **8,000 PLD Gates**
  - **96 I/O Pins, Twelve Dedicated Inputs**
  - **288 Registers**
  - **High-Speed Global Interconnects**
  - **Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **Small Logic Block Size for Random Logic**
- **HIGH PERFORMANCE E^{2}CMOS® TECHNOLOGY**
  - **$f$max = 90 MHz Maximum Operating Frequency**
  - **$t$pd = 10 ns Propagation Delay**
  - **TTL Compatible Inputs and Outputs**
  - **Electrically Eraseable and Reprogrammable**
  - **Non-Volatile**
  - **100% Tested at Time of Manufacture**
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - **In-System Programmable™ (ISP™) 5-Volt Only**
  - **Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality**
  - **Reprogram Soldered Devices for Faster Prototyping**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **Enhanced Pin Locking Capability**
  - **Four Dedicated Clock Input Pins**
  - **Synchronous and Asynchronous Clocks**
  - **Programmable Output Slew Rate Control to Minimize Switching Noise**
  - **Flexible Pin Placement**
  - **Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispLSI and pLSI DEVELOPMENT TOOLS**
  - **pDS® Software**
    - **Easy to Use PC Windows™ Interface**
    - **Boolean Logic Compiler**
    - **Manual Partitioning**
    - **Automatic Place and Route**
    - **Static Timing Table**
  - **pDS+™ Software**
    - **Industry Standard, Third Party Design Environments**
    - **Schematic Capture, State Machine, HDL**
    - **Automatic Partitioning and Place and Route**
    - **Comprehensive Logic and Timing Simulation**
    - **PC and Workstation Platforms**

Functional Block Diagram
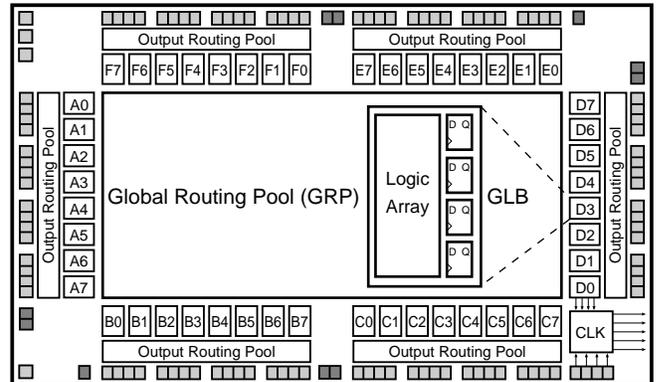
0139G1A-isp

Description

The ispLSI and pLSI 1048E are High-Density Programmable Logic Devices containing 288 Registers, 96 Universal I/O pins, 12 Dedicated Input pins, four Dedicated Clock Input pins, two dedicated Global OE input pins, and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 1048E features 5-Volt in-system programmability and in-system diagnostic capabilities. The ispLSI 1048E offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 1048E device, but multiplexes four of the dedicated input pins to control in-system programming. A functional superset of the ispLSI and pLSI 1048 architecture, the ispLSI and pLSI 1048E devices add two new global output enable pins and two additional dedicated inputs.

The basic unit of logic on the ispLSI and pLSI 1048E devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1…F7 (see figure 1). There are a total of 48 GLBs in the ispLSI and pLSI 1048E devices. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

Functional Block Diagram

Figure 1. ispLSI and pLSI 1048E Functional Block Diagram
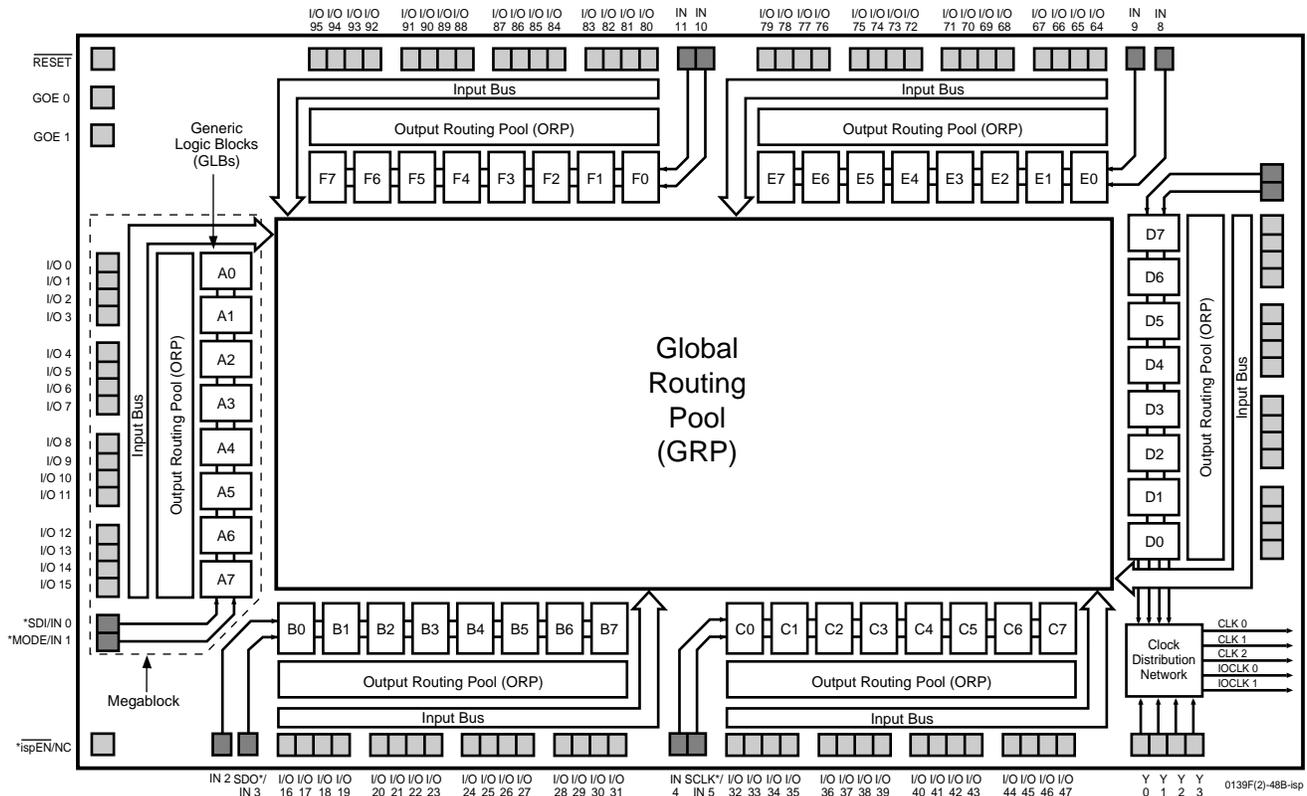
*ispLSI 1048E Only

The devices also have 96 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

Eight GLBs, 16 I/O cells, two dedicated inputs and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. Each ispLSI and pLSI 1048E device contains six Megablocks.

The GRP has, as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI and pLSI 1048E devices are selected using the Clock Distribution Network. Four dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (D0 on the ispLSI and pLSI 1048E devices). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Absolute Maximum Ratings [1]

Supply Voltage V_{CC}. .... -0.5 to +7.0V

Input Voltage Applied........................ -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature................................ -65 to 150°C

Case Temp. with Power Applied .... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	70	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	V_{CC} +1	V

Table 2 - 0005/2000

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_1	Dedicated Input, I/O, Y1, Y2, Y3, Clock Capacitance	8	pf	V_{CC} = 5.0V, V_{PIN} = 2.0V
C_2	Y0 Clock Capacitance	15	pf	V_{CC} = 5.0V, V_{PIN} = 2.0V

Table 2-0006a/1048C

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles
pLSI Erase/Reprogram Cycles	100	–	Cycles

Table 2-0008A-isp

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3 ns 10% to 90%
Input Timing Reference Levels	1.5V
Ouput Timing Reference Levels	1.5V
Output Load	See figure 2

Table 2-0003

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load

$^*C_L$ includes Test Fixture and Probe Capacitance.

0213a

Output Load Conditions (see Figure 2)

	TEST CONDITION	R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH}-0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL}+0.5V	470Ω	390Ω	5pF

Table 2-0004a

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL}= 8 mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH}= -4 mA	2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	$0V ≤ V_{IN} ≤ V_{IL}$ (Max.)	–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V ≤ V_{IN} ≤ V_{CC}$	–	–	10	µA
$I_{IL\text{-}isp}$	$\overline{ispEN}$ Input Low Leakage Current	$0V ≤ V_{IN} ≤ V_{IL}$	–	–	-150	µA
$I_{IL\text{-}PU}$	I/O Active Pull-Up Current	$0V ≤ V_{IN} ≤ V_{IL}$	–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC}= 5V, V_{OUT} = 0.5V	–	–	-200	mA
I_{CC}[2,4]	Operating Power Supply Current	V_{IL}= 0.0V, V_{IH}= 3.0V f_{CLOCK} = 1 MHz	–	175	–	mA

Table 2-0007a-48-isp

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2. Measured using twelve 16-bit counters.
3. Typical values are at V_{CC}= 5V and T_A= 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to Power Consumption section of this data sheet and Thermal Management section of this Data Book to estimate maximum I_{CC}.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[4] COND.	#[2]	DESCRIPTION[1]	-90 MIN.	-90 MAX.	-70 MIN.	-70 MAX.	-50 MIN.	-50 MAX.	UNITS
t_{pd1}	A	1	Data Propogation Delay, 4PT Bypass, ORP Bypass	–	10.0	–	15.0	–	20.0	ns
t_{pd2}	A	2	Data Propogation Delay, Worst Case Path	–	12.5	–	18.5	–	24.5	ns
f_{max} (Int.)	A	3	Clock Frequency with Internal Feedback [3]	90.9	–	70.0	–	50.0	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	71.0	–	56.0	–	42.0	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle $\left(\frac{1}{t_{wh} + t_{w1}}\right)$	125.0	–	100.0	–	77.0	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	6.5	–	9.0	–	12.0	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	6.5	–	7.0	–	9.5	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	7.5	–	11.0	–	14.5	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	7.5	–	9.0	–	12.0	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	13.5	–	15.0	–	20.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	6.5	–	10.0	–	13.0	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	15.0	–	18.0	–	24.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	15.0	–	18.0	–	24.0	ns
t_{goeen}	B	16	Global OE Output Enable	–	9.0	–	12.0	–	16.0	ns
t_{goedis}	C	17	Global OE Output Disable	–	9.0	–	12.0	–	16.0	ns
t_{wh}	–	18	External Synchronous Clock Pulse Duration, High	4.0	–	5.0	–	6.5	–	ns
t_{wl}	–	19	External Synchronous Clock Pulse Duration, Low	4.0	–	5.0	–	6.5	–	ns
t_{su3}	–	20	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	4.0	–	4.0	–	6.5	–	ns
t_{h3}	–	21	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	0.0	–	0.0	–	0.0	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

Table 2-0030-48E/90,70,50

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-90 MIN.	-90 MAX.	-70 MIN.	-70 MAX.	-50 MIN.	-50 MAX.	UNITS
Inputs									
t_{iobp}	22	I/O Register Bypass	–	0.5	–	0.6	–	0.7	ns
t_{iolat}	23	I/O Latch Delay	–	2.5	–	3.6	–	4.7	ns
t_{iosu}	24	I/O Register Setup Time before Clock	4.0	–	4.1	–	6.5	–	ns
t_{ioh}	25	I/O Register Hold Time after Clock	-0.5	–	-0.6	–	-0.7	–	ns
t_{ioco}	26	I/O Register Clock to Out Delay	–	5.0	–	6.0	–	7.0	ns
t_{ior}	27	I/O Register Reset to Out Delay	–	5.0	–	6.0	–	7.0	ns
t_{din}	28	Dedicated Input Delay	–	2.9	–	4.3	–	6.1	ns
GRP									
t_{grp1}	29	GRP Delay, 1 GLB Load	–	2.2	–	3.5	–	5.1	ns
t_{grp4}	30	GRP Delay, 4 GLB Loads	–	2.4	–	3.7	–	5.4	ns
t_{grp8}	31	GRP Delay, 8 GLB Loads	–	2.7	–	4.1	–	5.8	ns
t_{grp16}	32	GRP Delay, 16 GLB Loads	–	3.3	–	4.8	–	6.6	ns
t_{grp48}	33	GRP Delay, 48 GLB Loads	–	5.7	–	7.5	–	9.8	ns
GLB									
t_{4ptbpc}	34	4 Product Term Bypass Path Delay (Combinatorial)	–	5.4	–	8.5	–	10.7	ns
t_{4ptbpr}	35	4 Product Term Bypass Path Delay (Registered)	–	6.3	–	7.4	–	9.2	ns
t_{1ptxor}	36	1 Product Term/XOR Path Delay	–	6.5	–	8.4	–	10.5	ns
$t_{20ptxor}$	37	20 Product Term/XOR Path Delay	–	6.5	–	8.4	–	10.5	ns
t_{xoradj}	38	XOR Adjacent Path Delay [3]	–	7.3	–	9.4	–	11.7	ns
t_{gbp}	39	GLB Register Bypass Delay	–	0.4	–	1.6	–	2.2	ns
t_{gsu}	40	GLB Register Setup Time before Clock	0.1	–	0.1	–	0.0	–	ns
t_{gh}	41	GLB Register Hold Time after Clock	6.4	–	8.5	–	11.5	–	ns
t_{gco}	42	GLB Register Clock to Output Delay	–	2.0	–	2.0	–	3.0	ns
t_{gro}	43	GLB Register Reset to Output Delay	–	6.3	–	6.3	–	7.3	ns
t_{ptre}	44	GLB Product Term Reset to Register Delay	–	5.0	–	6.1	–	7.9	ns
t_{ptoe}	45	GLB Product Term Output Enable to I/O Cell Delay	–	5.7	–	6.8	–	10.0	ns
t_{ptck}	46	GLB Product Term Clock Delay	4.0	5.2	5.1	6.4	6.9	8.3	ns
ORP									
t_{orp}	47	ORP Delay	–	1.0	–	2.0	–	2.5	ns
t_{orpbp}	48	ORP Bypass Delay	–	0.0	–	0.0	–	0.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Table 2-0036-48E/90,70,50

Internal Timing Parameters[1]

PARAMETER	#	DESCRIPTION	-90 MIN.	-90 MAX.	-70 MIN.	-70 MAX.	-50 MIN.	-50 MAX.	UNITS
Outputs									
t_{ob}	49	Output Buffer Delay	–	1.7	–	2.2	–	3.2	ns
t_{sl}	50	Output Slew Limited Delay Adder	–	12.0	–	12.0	–	12.0	ns
t_{oen}	51	I/O Cell OE to Output Enabled	–	6.4	–	6.9	–	7.9	ns
t_{odis}	52	I/O Cell OE to Output Disabled	–	6.4	–	6.9	–	7.9	ns
t_{goe}	53	Global OE	–	2.6	–	5.1	–	8.1	ns
Clocks									
t_{gy0}	54	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	2.8	2.8	2.8	2.8	3.3	3.3	ns
$t_{gy1/2}$	55	Clock Delay, Y1 or Y2 to Global GLB Clock Line	2.8	2.8	2.8	2.8	3.3	3.3	ns
t_{gcp}	56	Clock Delay, Clock GLB to Global GLB Clock Line	0.8	1.8	0.8	1.8	0.8	1.8	ns
$t_{ioy2/3}$	57	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	0.0	0.5	0.1	0.6	0.0	0.7	ns
t_{iocp}	58	Clock Delay, Clock GLB to I/O Cell Global Clock Line	0.8	1.8	0.8	1.8	0.8	1.8	ns
Global Reset									
t_{gr}	59	Global Reset to GLB and I/O Registers	–	4.5	–	4.5	–	7.5	ns

1. Internal timing parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

Table 2-0037-48E/90,70,50

ispLSI and pLSI 1048E Timing Model

I/O Cell | GRP | GLB | ORP | I/O Cell

Feedback

Ded. In
#28
I/O Reg Bypass

I/O Pin (Input)
#22

Input Register Q
D RST
#23 - 27

#59

Reset

Clock Distribution
#55 - 58

Y1,2,3

Y0
#54

GOE 0,1
#53

GRP4
#30

GRP Loading Delay
#29, 31-33

#34 Comb 4 PT Bypass

Reg 4 PT Bypass
#35

20 PT XOR Delays
#36 - 38

#59

Control PTs
#44 - 46
RE OE CK

GLB Reg Bypass
#39

GLB Reg Delay
D Q
RST
#40 - 43

ORP Bypass
#48

ORP Delay
#47

#49, 50

I/O Pin (Output)

#51, 52

0491
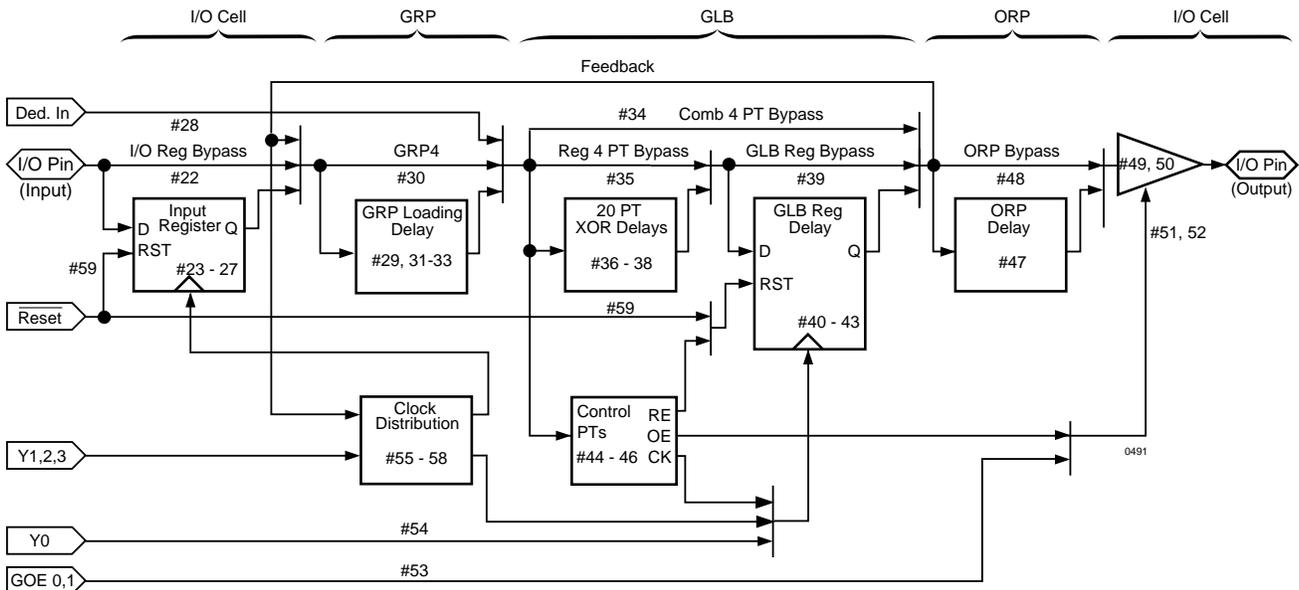
Derivations of tsu, th and tco from the Product Term Clock[1]

t_{su}
= Logic + Reg su - Clock (min)
= (t_{iobp} + t_{grp4} + $t_{20ptxor}$) + (t_{gsu}) - (t_{iobp} + t_{grp4} + $t_{ptck(min)}$)
= (#22 + #30 + #37) + (#40) - (#22 + #30 + #46)
2.6 ns = (0.5 + 2.4 + 6.5) + (0.1) - (0.5 + 2.4 + 4.0)

t_h
= Clock (max) + Reg h - Logic
= (t_{iobp} + t_{grp4} + $t_{ptck(max)}$) + (t_{gh}) - (t_{iobp} + t_{grp4} + $t_{20ptxor}$)
= (#22 + #30 + #46) + (#41) - (#22 + #30 + #37)
5.1 ns = (0.5 + 2.4 + 5.2) + (6.4) - (0.5 + 2.4 + 6.5)

t_{co}
= Clock (max) + Reg co + Output
= (t_{iobp} + t_{grp4} + $t_{ptck(max)}$) + (t_{gco}) + (t_{orp} + t_{ob})
= (#22 + #30 + #46) + (#42) + (#47 + #49)
12.8 ns = (0.5 + 2.4 + 5.2) + (2.0) + (1.0 + 1.7)

Derivations of tsu, th and tco from the Clock GLB[1]

t_{su}
= Logic + Reg su - Clock (min)
= (t_{iobp} + t_{grp4} + $t_{20ptxor}$) + (t_{gsu}) - ($t_{gy0(min)}$ + t_{gco} + $t_{gcp(min)}$)
= (#22 + #30 + #37) + (#40) - (#54 + #42 + #56)
3.9 ns = (0.5 + 2.4 + 6.5) + (0.1) - (2.8 + 2.0 + 0.8)

t_h
= Clock (max) + Reg h - Logic
= ($t_{gy0(max)}$ + t_{gco} + $t_{gcp(max)}$) + (t_{gh}) - (t_{iobp} + t_{grp4} + $t_{20ptxor}$)
= (#54 + #42 + #56) + (#41) - (#22 + #30 + #37)
3.6 ns = (2.8 + 2.0 + 1.8) + (6.4) - (0.5 + 2.4 + 6.5)

t_{co}
= Clock (max) + Reg co + Output
= ($t_{gy0(max)}$ + t_{gco} + $t_{gcp(max)}$) + (t_{gco}) + (t_{orp} + t_{ob})
= (#54 + #42 + #56) + (#42) + (#47 + #49)
11.3 ns = (2.8 + 2.0 + 1.8) + (2.0) + (1.0 + 1.7)

1. Calcuations are based upon timing specifications for the ispLSI and pLSI 1048E-90

Table 2-0042-1048E

## Maximum GRP Delay vs. GLB Loads
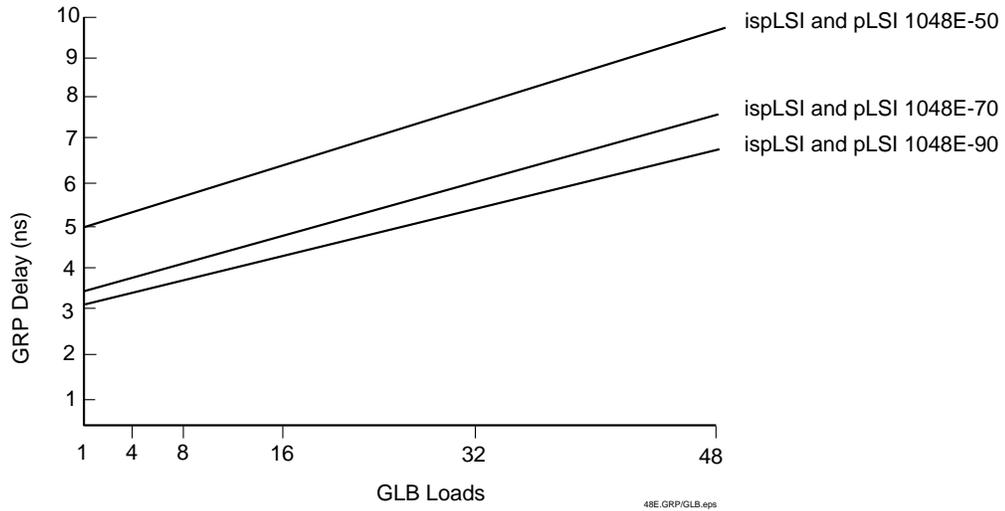
Power Consumption

Power Consumption in the ispLSI and pLSI 1048E device depends on two primary factors: the speed at which the device is operating and the number of Product Terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax
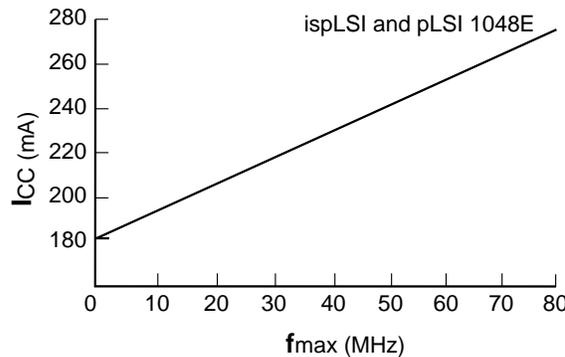
Notes: Configuration of twelve 16-bit counters
Typical current at 5V, 25°C

I_{CC} can be estimated for the ispLSI and pLSI 1048E using the following equation:

$$I_{CC} = 20 + (\# \text{ of PTs} * 0.42) + (\# \text{ of nets} * \text{Max. freq} * 0.100)$$

Where:
   # of PTs = Number of Product Terms used in design
   # of nets = Number of Signals used in device
   Max. freq = Highest Clock Frequency to the device

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of 4 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127A-48E-80-isp

In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice Semiconductor high density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^{2}CMOS cells will not lose the pattern even when the power is turned off.

All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The interface signals for the interface include isp Enable (ispEN), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 4 illustrates the block diagram of one possible scheme of the programming interface for the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the ISP Architecture and Programming section of this Data Book.

The device identifier for the ispLSI 1048E is 0000 1110 (0E hex). This code is the unique device identifier which is generated when a read ID command is performed.

Figure 4. ISP Programming Interface
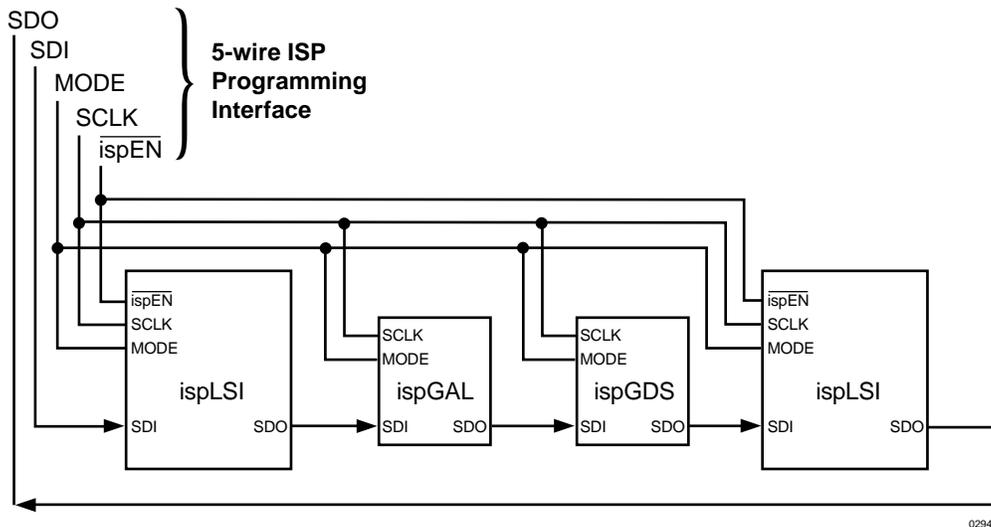
ispLSI 1048E Shift Register Layout

| Data In (SDI) | | 239... | High Order Shift Register | ...0 | SDO |
| | | 479... | Low Order Shift Register | ...240 | |

DATA

DATA

Address Shift Register

SDI

157

:

:

0

SDO

E^{2}CMOS Cell Array
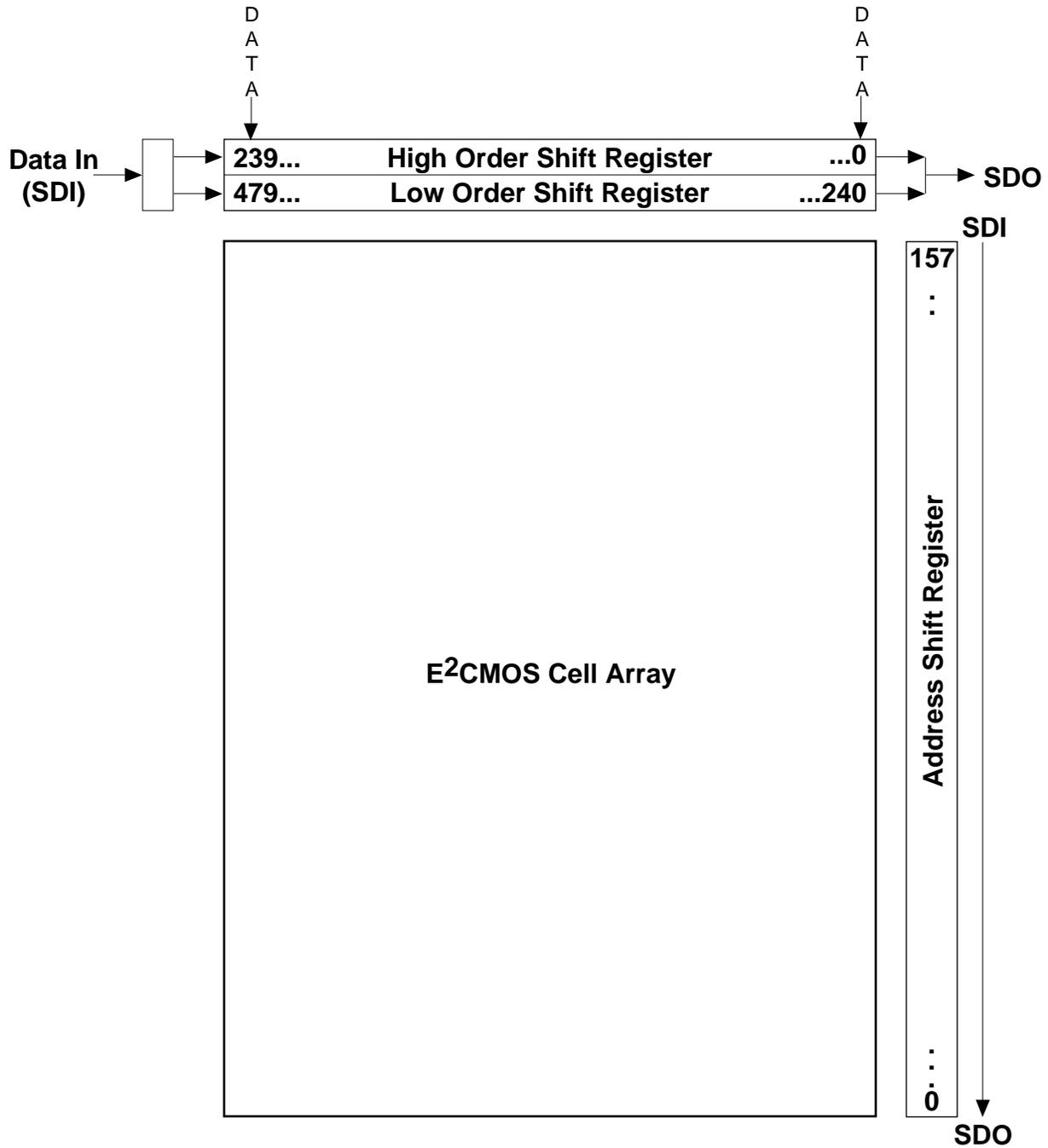
Note: A logic "1" in the Address Shift Register bit position enables the row for programming or verification. A logic "0" disables it.

Pin Description

| NAME	PQFP PIN NUMBERS						DESCRIPTION
I/O 0 - I/O 5 I/O 6 - I/O 11 I/O 12 - I/O 17 I/O 18 - I/O 23 I/O 24 - I/O 29 I/O 30 - I/O 35 I/O 36 - I/O 41 I/O 42 - I/O 47 I/O 48 - I/O 53 I/O 54 - I/O 59 I/O 60 - I/O 65 I/O 66 - I/O 71 I/O 72 - I/O 77 I/O 78 - I/O 83 I/O 84 - I/O 89 I/O 90 - I/O 95	21, 27, 34, 40, 52, 58, 66, 72, 85, 91, 98, 104, 117, 123, 2, 8,	22, 28, 35, 41, 53, 59, 67, 73, 86, 92, 99, 105, 118, 124, 3, 9,	23, 29, 36, 42, 54, 60, 68, 74, 87, 93, 100, 106, 119, 125, 4, 10,	24, 30, 37, 43, 55, 61, 69, 75, 88, 94, 101, 107, 120, 126, 5, 11,	25, 31, 38, 44, 56, 62, 70, 76, 89, 95, 102, 108, 121, 127, 6, 12,	26, 32, 39, 45, 57, 63, 71, 77, 90, 96, 103, 109, 122, 128, 7, 13	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE0, GOE1	64,	114					Global Output Enable input pins.
IN 2, IN 4 IN 6 - IN 11	47, 84,	51 110,	 111,	 115,	 116,	 14	Dedicated input pins to the device.
ispEN**/NC	18						Input - Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. When low, the MODE, SDI, SDO and SCLK controls become active.
SDI*/IN 0	20						Input - This pin performs two functions. When ispEN is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the ISP state machine. When ispEN is high, it functions as a dedicated input pin.
MODE*/IN 1	46						Input - This pin performs two functions. When ispEN is logic low, it functions as pin to control the operation of the isp state machine. When ispEN is high, it functions as a dedicated input pin.
SDO*/IN 3	50						Output/Input - This pin performs two functions. When ispEN is logic low, it functions as an output pin to read serial shift register data. When ispEN is high, it functions as a dedicated input pin.
SCLK*/IN 5	78						Input - This pin performs two functions. When ispEN is logic low, it functions as a clock pin for the Serial Shift Register. When ispEN is high, it functions as a dedicated input pin.
RESET	19						Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	15						Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	83						Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	80						Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	79						Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
GND	1, 97,	17, 112	33,	49,	65,	81,	Ground (GND)
VCC	16,	48,	82,	113			V_{CC}

Table 2 - 0002C-48E

* ispLSI 1048E only

** ispEN for ispLSI 1048E, NC for pLSI 1048E, must be left floating or tied to V_{CC}, must not be grounded or tied to any other signal.

Pin Configuration

ispLSI and pLSI 1048E 128-Pin PQFP Pinout Diagram

Top row (pins 128–97): I/O 83, I/O 82, I/O 81, I/O 80, I/O 79, I/O 78, I/O 77, I/O 76, I/O 75, I/O 74, I/O 73, I/O 72, IN 10, IN 9, GOE 1, VCC, GND, IN 8, IN 7, I/O 71, I/O 70, I/O 69, I/O 68, I/O 67, I/O 66, I/O 65, I/O 64, I/O 63, I/O 62, I/O 61, I/O 60, GND

Left column:
Pin	Signal
1	GND
2	I/O 84
3	I/O 85
4	I/O 86
5	I/O 87
6	I/O 88
7	I/O 89
8	I/O 90
9	I/O 91
10	I/O 92
11	I/O 93
12	I/O 94
13	I/O 95
14	IN 11
15	Y0
16	VCC
17	GND
18	* ispEN/NC
19	RESET
20	*SDI/IN 0
21	I/O 0
22	I/O 1
23	I/O 2
24	I/O 3
25	I/O 4
26	I/O 5
27	I/O 6
28	I/O 7
29	I/O 8
30	I/O 9
31	I/O 10
32	I/O 11

ispLSI 1048E pLSI 1048E Top View

Right column:
Pin	Signal
96	I/O 59
95	I/O 58
94	I/O 57
93	I/O 56
92	I/O 55
91	I/O 54
90	I/O 53
89	I/O 52
88	I/O 51
87	I/O 50
86	I/O 49
85	I/O 48
84	IN 6
83	Y1
82	VCC
81	GND
80	Y2
79	Y3
78	*SCLK/IN 5
77	I/O 47
76	I/O 46
75	I/O 45
74	I/O 44
73	I/O 43
72	I/O 42
71	I/O 41
70	I/O 40
69	I/O 39
68	I/O 38
67	I/O 37
66	I/O 36
65	GND

Bottom row (pins 33–64): GND, I/O 12, I/O 13, I/O 14, I/O 15, I/O 16, I/O 17, I/O 18, I/O 19, I/O 20, I/O 21, I/O 22, I/O 23, *MODE/IN 1, IN 2, VCC, GND, *SDO/IN 3, IN 4, I/O 24, I/O 25, I/O 26, I/O 27, I/O 28, I/O 29, I/O 30, I/O 31, I/O 32, I/O 33, I/O 34, I/O 35, GOE 0

*Pins have dual function capability for ispLSI 1048E only (except pin 18, which is ispEN only).

0124-48C

Part Number Description

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(is)pLSI   1048E − XX   X   X   X
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Device Family

Device Number

Speed
90 = 90 MHz **f**max
70 = 70 MHz **f**max
50 = 50 MHz **f**max

Grade
Blank = Commercial

Package
Q = PQFP

Power
L = Low

0212-80B-isp1048E
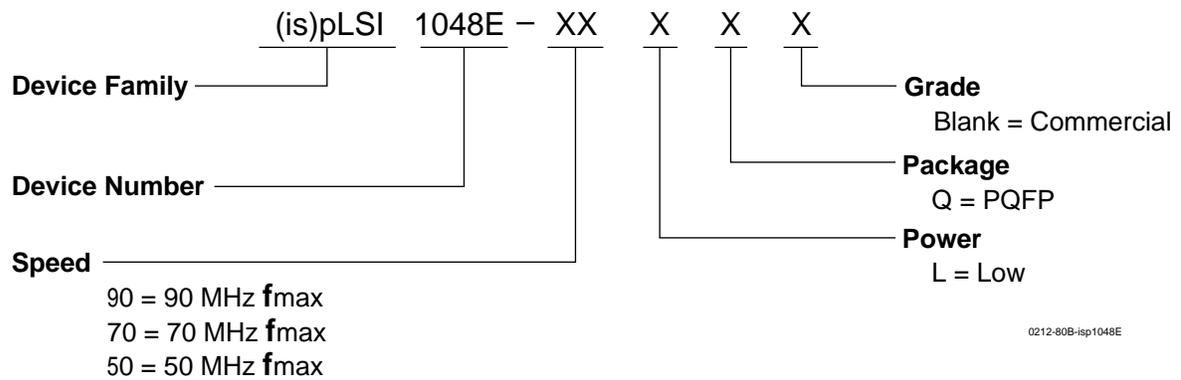
ispLSI and pLSI 1048E Ordering Information

FAMILY	Fmax (MHz)	Tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	90	10	ispLSI 1048E-90LQ	128-Pin PQFP
	70	15	ispLSI 1048E-70LQ	128-Pin PQFP
	50	20	ispLSI 1048E-50LQ	128-Pin PQFP
pLSI	90	10	pLSI 1048E-90LQ	128-Pin PQFP
	70	15	pLSI 1048E-70LQ	128-Pin PQFP
	50	20	pLSI 1048E-50LQ	128-Pin PQFP

Table 2-0041-48-isp

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