

Qualification Program

Introduction

Lattice Semiconductor Corporation (LSC) has an intensive qualification program for examining and testing new products, processes, and vendors in order to insure the highest levels of quality. LSC's Quality and Reliability Group is responsible for defining and implementing this qualification program.

The following table outlines the steps which must be performed before a new product, package or process is released. The requirements listed below are general guidelines. Detailed information on Lattice's qualification process is available to customers upon request.

Qualification Requirements

Test	Duration		
	New Product	New Wafer Process	New Package
125° C Operating Lifetest (5.25V)	1,000 Hours	1,000 Hours	1,000 Hours ¹
150° C Biased Retention Bake (5.25V)	1,000 Hours	1,000 Hours	1,000 Hours ¹
Endurance Cycling	10,000 Cycles	10,000 Cycles	N/A
ESD (CDM, HBM, MM)	End of Test	End of Test	N/A
Latch-Up Immunity	End of Test	End of Test	N/A
Temperature Cycling (-65 to 150° C)	1,000 Cycles	1,000 Cycles	1,000 Cycles
Biased 85/85 (5V)	N/A	1,000 Hours	1,000 Hours
Autoclave (121° C, 15psig)	N/A	168 Hours	168 Hours
Solderability	N/A	N/A	End of Test
Physical Dimensions	N/A	N/A	End of Test

1. Required for new assembly technologies only.

Qualification Program

Reliability Monitor Program

The Reliability Monitor Program provides for a periodic reliability monitor of LSC products. The program assures that all Lattice products comply on a continuing basis with established reliability and quality levels.

The Reliability Monitor Program is designed to monitor all fab and assembly facilities as well as each process technology in production. A summary of the program test and sampling plan is shown below.

Short Term Process Monitor (Bi-Weekly)

Test	# of Samples	Duration
125° C Operating Lifetest (6.50V)	70	160 Hours
150° C Biased Retention Bake (5.25V)	70	160 Hours
Autoclave (121° C, 15psig)	35	160 Hours
Temperature Cycling (-65 to 150° C)	35	250 Cycles

Long Term Process Monitor (Monthly)

Test	# of Samples	Duration
125° C Operating Lifetest (6.00V)	100	1000 Hours
150° C Biased Retention Bake (5.25V)	150	1000 Hours

Ongoing Package Monitor (Monthly)

Test	# of Samples	Duration
Temperature Cycling (-65 to 150° C)	50	1000 Cycles
85° C / 85% RH	75	1000 Hours



Copyright © 1996 Lattice Semiconductor Corporation.

E²CMOS, GAL, ispGAL, ispLSI, pLSI, pDS, Silicon Forest, UltraMOS, Lattice Logo, L with Lattice Semiconductor Corp. and L (Stylized) are registered trademarks of Lattice Semiconductor Corporation (LSC). The LSC Logo, Generic Array Logic, In-System Programmability, In-System Programmable, ISP, ispATE, ispCODE, ispDOWNLOAD, ispGDS, ispStarter, ispSTREAM, ispTEST, ispTURBO, Latch-Lock, pDS+, RFT, Total ISP and Twin GLB are trademarks of Lattice Semiconductor Corporation. ISP is a service mark of Lattice Semiconductor Corporation. All brand names or product names mentioned are trademarks or registered trademarks of their respective holders.

Lattice Semiconductor Corporation (LSC) products are made under one or more of the following U.S. and international patents: 4,761,768 US, 4,766,569 US, 4,833,646 US, 4,852,044 US, 4,855,954 US, 4,879,688 US, 4,887,239 US, 4,896,296 US, 5,130,574 US, 5,138,198 US, 5,162,679 US, 5,191,243 US, 5,204,556 US, 5,231,315 US, 5,231,316 US, 5,237,218 US, 5,245,226 US, 5,251,169 US, 5,272,666 US, 5,281,906 US, 5,295,095 US, 5,329,179 US, 5,331,590 US, 5,336,951 US, 5,353,246 US, 5,357,156 US, 5,359,573 US, 5,394,033 US, 5,394,037 US, 5,404,055 US, 5,418,390 US, 5,493,205 US, 0194091 EP, 0196771B1 EP, 0267271 EP, 0196771 UK, 0194091 GB, 0196771 WG, P3686070.0-08 WG. LSC does not represent that products described herein are free from patent infringement or from any third-party right.

The specifications and information herein are subject to change without notice. Lattice Semiconductor Corporation (LSC) reserves the right to discontinue any product or service without notice and assumes no obligation to correct any errors contained herein or to advise any user of this document of any correction if such be made. LSC recommends its customers obtain the latest version of the relevant information to establish, before ordering, that the information being relied upon is current.

LSC warrants performance of its products to current and applicable specifications in accordance with LSC's standard warranty. Testing and other quality control procedures are performed to the extent LSC deems necessary. Specific testing of all parameters of each product is not necessarily performed, unless mandated by government requirements.

LSC assumes no liability for applications assistance, customer's product design, software performance, or infringements of patents or services arising from the use of the products and services described herein.

LSC products are not authorized for use in life-support applications, devices or systems. Inclusion of LSC products in such applications is prohibited.

LATTICE SEMICONDUCTOR CORPORATION

5555 Northeast Moore Court
Hillsboro, Oregon 97124 U.S.A.

Tel.: (503) 681-0118

FAX: (503) 681-3037

<http://www.latticesemi.com>

November 1996
