Lattice Semiconductor Design Tool Strategy

Introduction

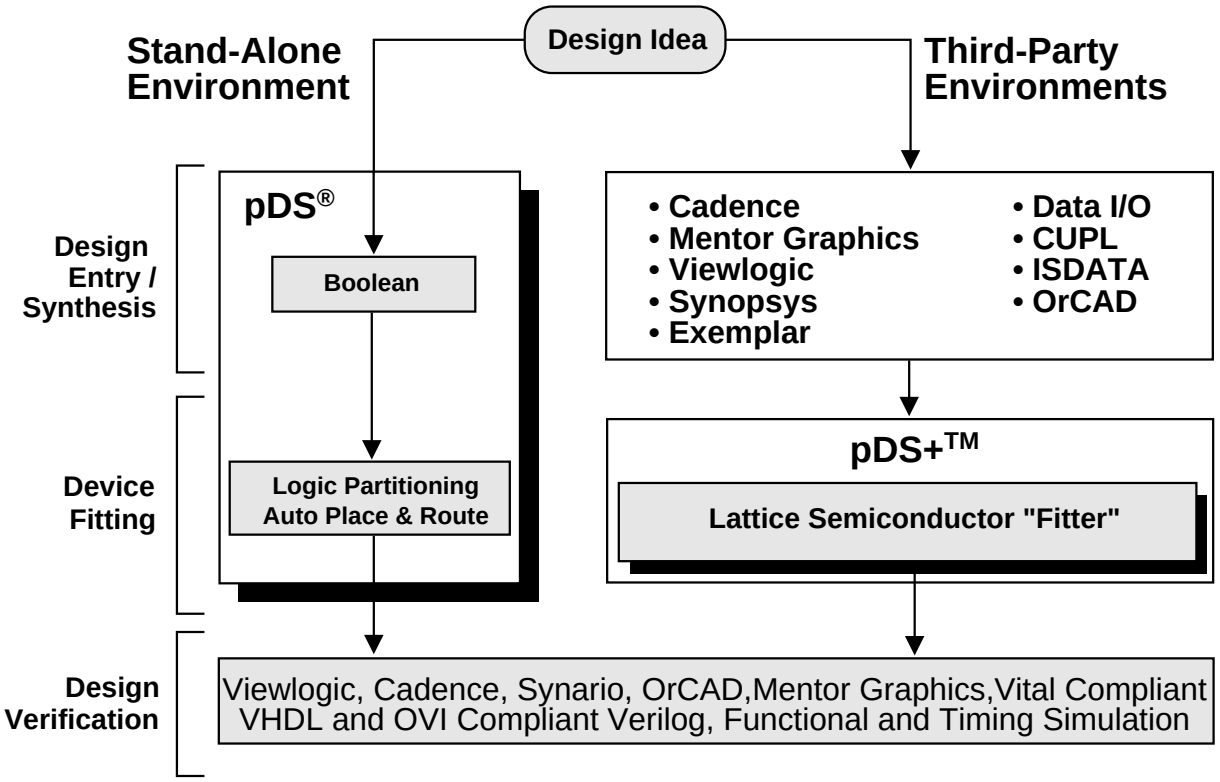
The Lattice Semiconductor Corporation (LSC) design tool strategy for the ispLSI and pLSI families is to support a wide range of design environments. LSC provides both a proprietary PC-based solution (pDS®) as well as third-party compatible CAE tools (pDS+™ Fitters) that run on PC, Sun and Hewlett Packard (HP) workstation platforms.

The LSC pDS pLSI/ispLSI software provides a comprehensive, high-performance, low-cost package for logic development. Developed and supported by LSC, pDS provides an easy-to-use Windows-based graphical interface using a mouse and pull-down menus. Design entry includes Boolean equations, standard and TTL macros. For simulation, timing tables are included as a standard offering. Additionally, pDS interfaces with third-party tools for full functional and timing simulation. pDS software generates industry standard JEDEC programming files and supports direct download into ispLSI devices.

LSC's pDS+ (pDS Plus) solution supports multiple third-party CAE tools, providing designers with the capability to design in familiar CAE environments. These third-party CAE tools offer schematic capture, hardware description language (such as VHDL), state machine language, Boolean equation, and macro design entry as well as functional and timing simulators for design verification.

LSC's pDS and pDS+ solutions give designers powerful, easy to use, cost-effective design tools to meet their development needs. Each third-party vendor must adhere to strict quality and certification requirements before becoming qualified, thus ensuring superior support.

Figure 1. pDS and pDS+ Design Flows



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Design Flow

There are three steps in the LSC ispLSI and pLSI design flow: design entry, device fitting (logic partitioning, place and route), and design verification. (See the pDS and pDS+ Design Flow). This section outlines the design flow of the pDS and pDS+ solutions.

pDS

LSC's pDS solution is a comprehensive, self-contained design solution which operates on a PC under Microsoft Windows™. pDS uses familiar ABEL-like Boolean equations, standard macros and a library of TTL macros for design entry, and provides manual partitioning, high speed automatic place and route, and simulation timing tables for design verification. A variety of simulators, such as Viewlogic's Viewsim simulation package, are compatible with pDS for functional and timing simulation.

After the development work has been completed, the design is ready to be programmed into a device. For third-party programming support, the pDS package generates a JEDEC fusemap . Alternatively, the ispLSI devices can be programmed directly from the PC with the LSC isp Engineering Kit.

The pDS development systems are ideal for designers who desire a cost-effective, user friendly approach to ispLSI and pLSI design.

pDS+

The pDS+ solution combines third-party CAE tools for design entry and verification with the LSC pDS+ Fitter for device fitting to offer a powerful and complete development solution. LSC pDS+ Fitters support a broad range of third party design tools, including:

Vendor	Design Tool
Cadence	Concept, Synergy, Verilog-XL, Leapfrog
Data I/O	ABEL, Synario
Exemplar Logic	Galileo Logic Explorer
ISDATA	LOG/iC Classic, LOG/iC 2
Mentor Graphics	Design Architect, Autologic & Autologic II, Quicksim II, Quick-VHDL, System V (Model Tech)
Logical Devices	CUPL
OrCAD	SDT, PLD, VST 386+, Capture for Windows, Simulate for Windows, Express
Synopsys	Design Compiler Expert & Professional, FPGA Compiler, VSS, Design Time
Viewlogic	PRO Series, Workview Plus, Powerview, Workview Office

The design entry step is typically performed with schematic capture, Boolean equations, state machines, truth tables or a Hardware Description Language (HDL). Once design entry is complete, the design is ready to be implemented into a LSC ispLSI or pLSI device.

The LSC pDS+ Fitter uses architecture-specific algorithms to synthesize a logic description into an ispLSI or pLSI device. Steps in the device fitting process include logic optimization and minimization, automatic logic partitioning, and automatic place and route.

pDS+ also supports design verification. Design verification options include both functional and timing simulation. Various combinations of graphical and text-based functional and timing simulators are supported by third-party CAE vendors.

Following design verification, the LSC pDS+ Fitter generates a JEDEC fusemap for device programming. The design can be programmed into a pLSI device using third-party programmers. In addition, the ispLSI devices can be programmed directly from a PC using LSC's isp Engineering Kit, or from dedicated logic designed into the end-system.

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