The GAL®18V10 Advantage

Introduction

Although the GAL16V8 is able to replace a number of different standard PLDs, such as the common PAL16L8 and PAL16R8, there are times when a designer needs more flexibility than standard 20-pin PLDs offer. Moving the PLD design to the next package size means using a 24-pin DIP or 28-pin PLCC package. Often the increase in functionality does not justify the increase in package size.

This application brief describes the most common limitations of a standard 20-pin PLD and how the GAL18V10's unique architecture allows the designer much greater functionality while maintaining the same 20-pin package. In addition, the architecture of the 18V10 is virtually the same as the industry-standard 22V10 device, which means that learning a new device architecture is not necessary.

More Inputs

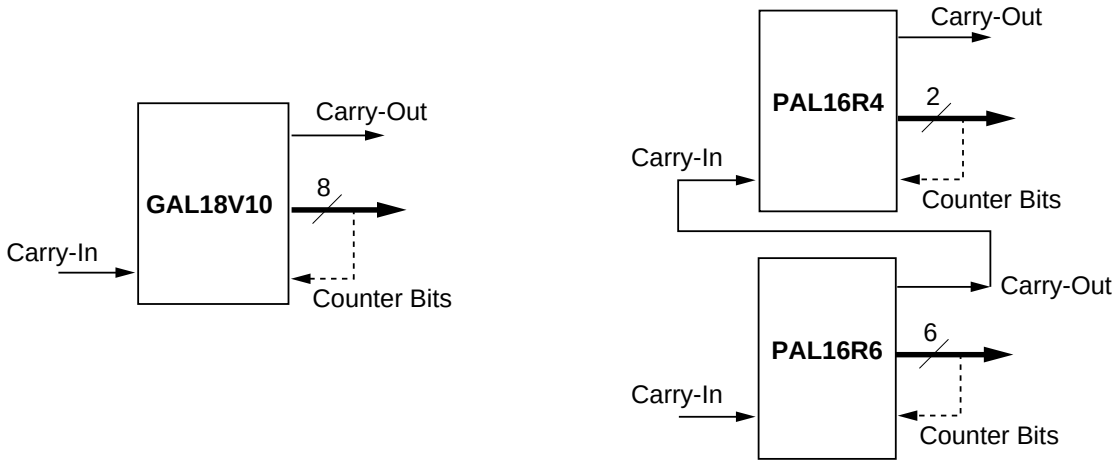
As with the GAL22V10, the GAL18V10 macrocell structure allows for greater flexibility than the common 20-pin PAL-type devices. Whereas the GAL16V8, because of its exact emulation of many PAL devices, must limit the I/O pins that can have feedback or be configured as inputs, the 18V10 has no such limitations. Each of the I/O pins on the GAL18V10 can be configured as registered or combinatorial, has feedback capability, and can be configured as a dedicated input or dynamic I/O pin.

GAL16V8 Emulation Mode	**No Feedback or Input**
Complex Mode (16L8)	pins 12, 19
Simple Mode (16H4, etc.)	pins 15, 16

More Outputs

As the name suggests, the GAL18V10 has a total of 10 possible outputs. In cases where more than eight outputs are needed on the standard PLD, a GAL18V10 is an ideal replacement. One demonstration of the additional capability of the GAL18V10 is an eight-bit counter with a carry-out signal. A GAL16V8 or PAL16R8 device can be used to build an eight-bit counter. However to provide a carry-out and/or carry-in signal, more outputs are required. The GAL18V10 fits the bill nicely, since it is a functional superset of the already flexible GAL16V8. Adding an few extra lines of equations in the source file and re-compiling produces a JEDEC file for a totally pin-compatible replacement, but with extra functionality. Other uses for the additional output macrocells include implementing nine or ten bit counters and decoded outputs from eight or nine bit counters. All of these functions could be done in a 22V10 as well (at extra cost), but could not be done in any of the common 20-pin PAL devices. Below is an example of two implementations of an eight-bit counter with carry-in and carry-out. While this design fits in one GAL18V10, it would require two different 20-pin PAL devices.

Figure 1. Eight-Bit Counter with Carry-In and Carry-Out



Reset and Preset

Another benefit of the 22V10 nature of the GAL18V10 is the inclusion of Asynchronous Reset and Synchronous Preset of the registers. These dedicated product terms can allow any pin or combination of inputs and/or feedbacks to trigger a global reset or preset to occur. In many other devices this can only be accomplished by using valuable product terms and extra design time to build this capability into the logic for each output. Since each output in these devices has only seven or eight product terms, the addition of the reset/preset logic may make it impossible to fit in the desired logic functions. Example 1 illustrates what the eighth output of an eight-bit counter may look like.

To add the capability for a synchronous preset would require the use of an additional product term, which may not be available. This same problem may come up in a complex state machine.

The Asynchronous Reset function cannot even be duplicated in the GAL16V8 or standard PAL devices. The GAL18V10 can be asynchronously reset, therefore simplifying the power-up routine by not requiring a clock cycle to put the device into a known state.

Flexible Output Enable

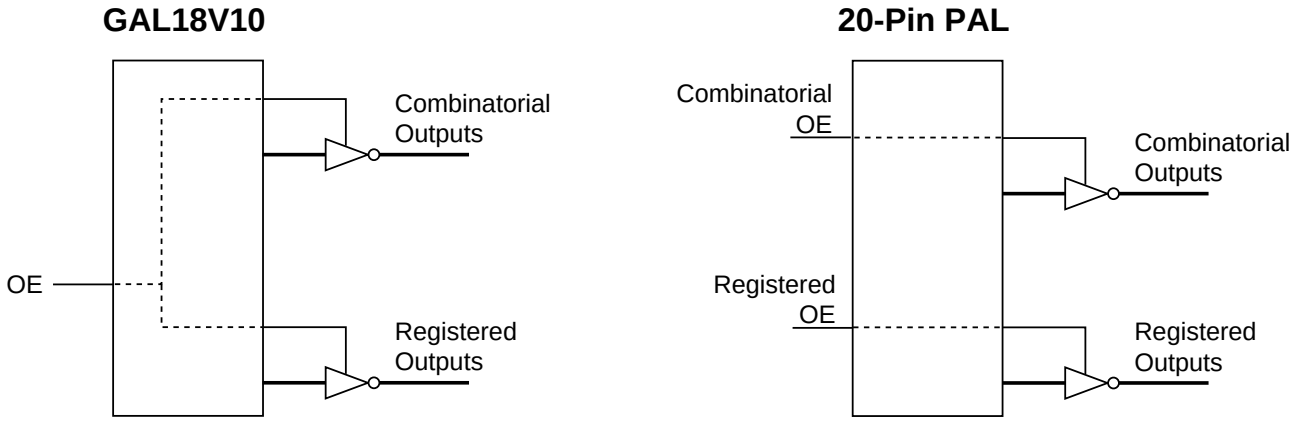
Again because of its exact emulation of the common 20-pin PAL devices, the GAL16V8 has limited options for placement of the Output Enable control pins. A GAL16V8 with any I/O macrocells configured in registered mode always has pin 11 dedicated to the output enable of the register. Pin 11 is then no longer available as an input to the array. This means that any combinatorial outputs that need output enable control must use an additional pin, since the output enable control of combinatorial outputs is through a product term. A design with a mix of registered and combinatorial outputs using a GAL16V8 (or 20-pin PAL device) must always use two pins to get

Example 1. Eighth Output of an Eight-Bit Counter

```
Q7 := ( Q0 & Q1 & Q2 & Q3 & Q4 & Q5 & Q6 & !Q7      "Product Term 1
    #   !Q6 & Q7                                    "Product Term 2
    #   !Q5 & Q7                                    "Product Term 3
    #   !Q4 & Q7                                    "Product Term 4
    #   !Q3 & Q7                                    "Product Term 5
    #   !Q2 & Q7                                    "Product Term 6
    #   !Q1 & Q7                                    "Product Term 7
    #   !Q0 & Q7 );                                 "Product Term 8

    #  !Synch_Preset      " NO MORE PRODUCT TERMS AVAILABLE!
```

Figure 2. Output Enable Pin Consolidation



output enable control on all outputs. The GAL18V10 has no such restrictions. All output enable control is from a product term, regardless of whether the output is configured as registered or combinatorial.

Saving one pin on a 20-pin device can mean the difference between keeping the design in a 20-pin device and having to go to a larger (and more expensive) device. Figure 2 illustrates how the GAL18V10 can use one less pin than a GAL16V8 or 20-pin PAL device when both registered and combinatorial outputs must be tri-stated.

Conclusion

It is clear that standard PAL architectures have definite limitations. Lattice Semiconductor first addressed this issue with the GAL16V8 and GAL20V8 devices, which were able to replace all standard 20 and 24-pin PAL devices. For replacing those same PAL devices, and adding some additional flexibility, the GAL16V8 and GAL20V8 devices are a vast improvement and have become an industry standard in their own right.

However, as the previous examples have pointed out, there are many cases where the old standby programmable logic architectures, and even the first-generation GAL replacements, don't have the flexibility required. For 20-pin devices, the GAL18V10 provides complete design flexibility by using the familiar 22V10 architecture, while maintaining the ability to provide a pin-compatible superset of the GAL16V8.

LATTICE SEMICONDUCTOR CORPORATION
5555 Northeast Moore Court
Hillsboro, Oregon 97124 U.S.A.
Tel.: (503) 681-0118
FAX: (503) 681-3037
http://www.latticesemi.com

November 1996