pDS+™ Exemplar Software

Features

- **ispLSI® and pLSI® DEVELOPMENT SYSTEM**
  - — **Supports ispLSI and pLSI 1000/E and 2000**
  - — **Upgrade to Support ispLSI and pLSI 3000 and 6000**
- **DESIGN ENTRY USING EXEMPLAR GALILEO LOGIC EXPLORER**
  - — **VHDL OR VERILOG-HDL Entry**
  - — **Library of Over 300 Macros**
  - — **Command Line Driven User Interface**
- **LATTICE SEMICONDUCTOR pDS+™ EXEMPLAR FITTER**
  - — **Multi-Level Logic Synthesis**
  - — **Efficient Design Optimization and Minimization**
  - — **Automatic Mapping and Device Fitting**
  - — **Automatic Partitioning with High Utilization**
  - — **Predictable Performance**
- **INDUSTRY STANDARD PROGRAMMING FILE GENERATION**
  - — **Standard JEDEC Device Fuse Map**
- **IN-SYSTEM PROGRAMMING SUPPORT**
  - — **ispCODE™ C Source Routines Included**
  - — **ISP Daisy Chain Download (PC Versions)**
  - — **ispATE™ Board Test Programming Utility**
- **PLATFORMS SUPPORTED**
  - — **PC DOS/Windows 3.1/Windows 95/Windows NT**
  - — **Sun Workstation, SUN O/S 4.1.3 and Above**

Introduction

pDS+ Exemplar software from Lattice Semiconductor Corporation (LSC) offers a powerful logic design solution for Lattice's ispLSI and pLSI families of high density PLDs.

Design entry is made simple by tight integration between Exemplar Logic's Galileo tool set and the pDS+ Exemplar Fitter for design implementation. Lattice Semiconductor's pDS+ Exemplar software offers multi-level design synthesis, automatic place and route, and efficient device utilization, delivering high performance for complex logic designs.

Exemplar's Galileo

Exemplar's Galileo Logic Explorer™ supports the description of more complex designs using standard VHDL and Verilog-HDL constructs for structural, data flow and RTL behavior. The high-level design paradigm supported by Exemplar Logic encompasses three distinct design steps: device-independent specification and simulation; constraint-independent, architecture-specific implementation; and gate-level verification.

Products in the Galileo family supporting Lattice Semiconductor ispLSI and pLSI device design include the Logic Explorer synthesis tool, the Time Explorer tool for timing analysis, schematic viewing, back annotation and the V-System VHDL simulator from Model Technology.

pDS+ Exemplar Fitter

The pDS+ Exemplar Fitter for ispLSI and pLSI devices is executed as a stand-alone program, using the EDIF output from Galileo as input. The pDS+ Fitter provides hands-off design implementation through an intelligent multi-level synthesis algorithm, logic partitioning, automatic place and route and standard JEDEC fuse map generation for device programming. Timing simulation input files for the V-System simulator are generated by the Fitter and are coupled with Lattice Semiconductor's VITAL-compliant VHDL Library as needed by the user.

Macro Library

The Lattice Semiconductor Exemplar Synthesis Libraries contain a library of over 300 high-level functions to simplify design entry. These macros enable the design engineer to use familiar, predefined functions to build a design. Direct instantiation of these functions is provided to enhance device performance and utilization.

Figure 3. Macro Summary

Macro Type	Quantity
AND/NAND	29
OR/NOR	24
XOR/XNOR	12
I/Os	89
Flip-Flops	39
Latches	30
Arithmetic	33
Counters	65
Shift Registers	15
Miscellaneous	45

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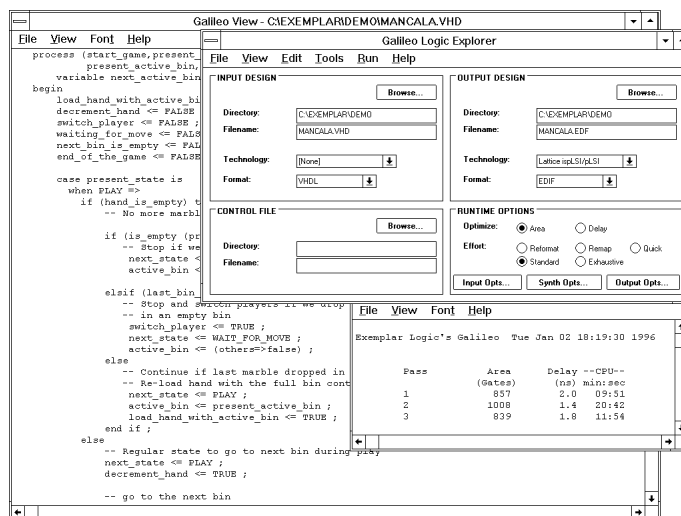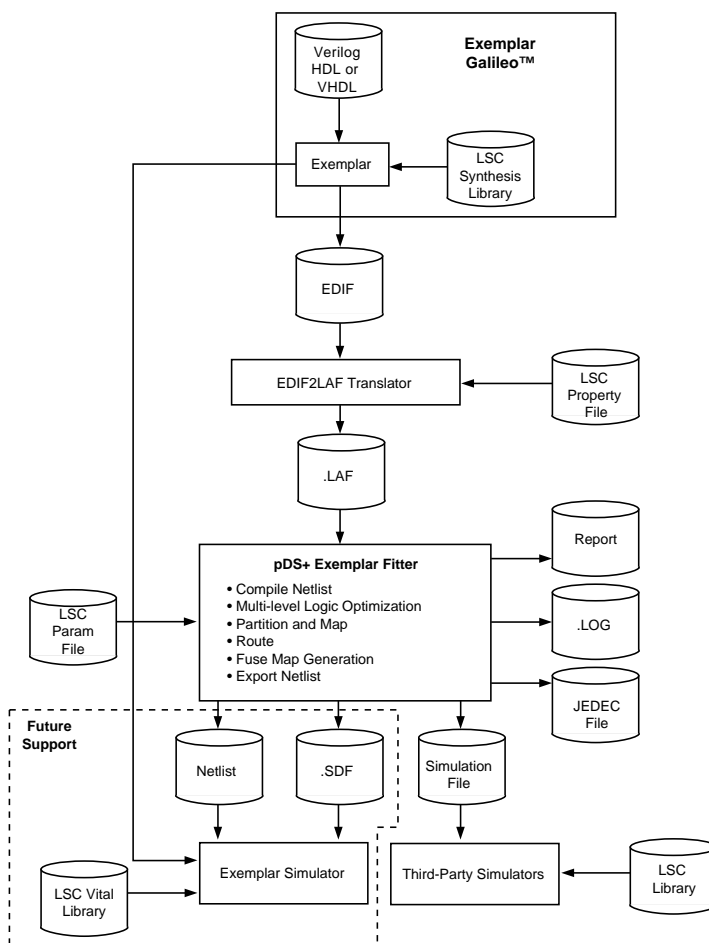
Figure 1. Exemplar Logic Design Interface

Figure 2. Lattice Semiconductor pDS+ Exemplar Design Flow

Design Optimization & Logic Minimization

The pDS+ Exemplar Fitter uses proprietary algorithms targeted for Lattice Semiconductor's device-specific architectural features. The Fitter optimizes the design thoroughly, utilizing logic minimization, product term sharing and XOR functions wherever possible. In addition, the pDS+ Exemplar Fitter supports multiple fitting strategies to obtain the best device utilization and performance.

Automatic Partitioning

The pDS+ Exemplar Fitter incorporates a powerful Automatic Partitioner for hands-free synthesis of a design into Generic Logic Blocks (GLBs). The partitioner takes full advantage of the ispLSI family's features such as the hard XOR and product term sharing. The internal XOR can be utilized for arithmetic functions, T-type flip-flops, and on and off set optimization functions. The partitioner also makes extensive use of product term sharing. Product term sharing allows the Fitter to efficiently use device resources by sharing product terms across multiple logic functions. These features combine to maximize device resource utilization and increase design performance.

Automatic Place and Route

Automatic place and route eliminates the need for manual editing and accelerates the design cycle. The Router automatically generates pinouts based on the optimal design implementation or user assigned pinouts.

The Extended Route option performs a comprehensive route to maximize device resource utilization and ensure efficient design implementation.

Design Parameter Control

The pDS+ Exemplar Fitter offers extensive design control at the design entry level, letting the user optimize the design for maximum utilization and/or speed. All of the controls are specified using "attributes" in the design property and parameter files. The parameter and property files contain:

    — Fitter Control Options
    — Design Implementation Controls
        — Net Attributes
        — Pin Attributes
        — Path Attributes
        — Symbol Attributes

Fitter Control Options

Special properties can be passed to the pDS+Exemplar Fitter providing complete control over critical design considerations. Fitter control over design partitioning and routing optimizes the design for speed and/or device utilization.

Feature	Description
PART	Determines device type to be used.
PARAM_FILE	Allows user to specify attributes in a text file.
STRATEGY	Choice of AREA (default), DELAY or NO_OPTIMIZE. AREA optimizes device space, DELAY keeps GLB levels to a minimum and NO_OPTIMIZE does not reduce equations.
USE_GLOBAL_RESET	Causes global reset to use dedicated routing for reset.
MAX_GLB_OUT	Specifies maximum number of outputs from a GLB. Default is 4.
MAX_GLB_IN	Controls maximum number of inputs to a GLB. Default is 16 for 1K and 2K devices and 24 for 3K devices.
EFFORT	Controls optimization of partitioner.
EXTENDED_ROUTE	Choice of OFF (fixed) or ON (extended, default).
PIN_FILE	Specifies locked pin assignments.

Design Implementation Controls

Device controls are used for changing design parameters such as security. Some of these implementation controls are:

Feature	Description
ISP	Instructs Router to reserve in-system programming pins.
ISP_EXCEPT_Y2	Reserves all ISP pins except Y2 (ispLSI and pLSI 1016/E and 2032 only).
Y1_AS_RESET	Uses Y1 clock pin on ispLSI and pLSI 1016/E and 2032 as a global reset pin.
SECURITY	Sets the device security cell to prevent unauthorized fuse map read back.

Net Attributes

These properties control how the design is mapped into the specified features of the target device:

Feature	Description
CLK0-CLK2	Assigns a CLK signal to a dedicated CLK line.
IOCLK0-IOCLK1	Assigns a CLK signal to a dedicated IOCLK line if single fanout input pin.
FASTCLK	Fitter assigns CLK signal to CLK0-CLK2 or IOCLK0-IOCLK1.
SLOWCLK	Assigns the CLK signal to a GLB product term CLK.
PRESERVE	Prevents logic minimization on specified nets.
GROUP	Suggests grouping of functions in a GLB.

Pin Attributes

Feature	Description
CRIT	Specifies Output Routing Pool Bypass to minimize delay.
SLOWSLEW	Assigns slow slew rate on a specific I/O cell.
LOCK	Assigns device I/O pins to design I/O ports.
PULLUP	Specifies internal pull-up resistors.

Path Attributes

The following properties specify paths in the design that have special fitting requirements:

Feature	Description
SAP/EAP	Defines asynchronous paths to prevent signal duplication.
SCP/ECP	Defines critical paths to reduce delays.
SNP/ENP	Defines logic paths for no logic minimization.

Symbol Attributes

Feature	Description
REGTYPE	Determines where a register is to be placed (IOC or GLB).
PROTECT	Prevents removal of a primitive or a macro during minimization.
OPTIMIZE	Selects either hard or soft macros.

Parameter File

The pDS+ Exemplar Fitter provides the ability to use a parameter file (design.par) feature which helps designers eliminiate guesswork and optimize the designs for the right devices. It allows the user to try a number of design implementation options using all of the fitter control options in a batch mode. The parameter file instructs the partitioner and the router to maximize both device utilization and performance.

Property File

The pDS+ Exemplar Fitter provides the ability to use a property file (design.prp) feature which allows the designer to control the fitter using all of the design attributes available. The property file helps guide the fitter in implementing the design in the best way.

Design Verification

The pDS+ Exemplar Fitter provides a post route design file for optional timing simulation. The pDS+ Exemplar software offers complete post route design verification using optional timing simulators. The pDS+ Exemplar Fitter generates the files required by third-party simulators, and generates a "sim" file which can be used for simulation with behavioral simulation models from Synopsys' Logic Modeling Division.

Fuse Map Generation

pDS+ Exemplar software generates a device fuse map in standard JEDEC format. A security feature offers protection of proprietary designs from unauthorized duplication. The Fitter appends any design test vectors in JEDEC format to the device fusemap, facilitating a quick, easy functional verification of a programmed device.

System Requirements (PC Platform)

— 486/Pentium™ IBM-Compatible PC
— Operating System
  — MSDOS Version 4.x or Later
  — Windows 3.1
  — Windows NT
  — Windows 95
— 16 MB RAM with 30MB Hard Disk Space
— Parallel Printer Port for Software Key

System Requirements (Sun Platform)

— Sun Sparc 4 and above
— Sun OS Version 4.x
— Open Windows 3.0
— 16 MB RAM with 30 MB Hard Disk Space
— 3 Button Mouse

Programmer Support

All devices in the Lattice Semiconductor ispLSI device family can be programmed while installed on the target circuit board. In-system programming can be performed using an ispDOWNLOAD Cable and PC, by an on-board microprocessor or by ATE systems during final board test.

All Lattice Semiconductor ispLSI and pLSI devices can be programmed using third-party programmers. These devices are currently supported by programmers from the following vendors:

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30A/B
System General	TURPRO-1/FX

High pin-count adapters are available from Emulation Technology, EDI Corporation and PROCON.

Product Ordering Information

Product Code	Description
pDS2110-PC1	pDS+ Exemplar Fitter and Synthesis Library (PC)
pDS2110-SN1	pDS+ Exemplar Fitter and Synthesis Library (Sun)
pDS1110-PC1	Lattice Semiconductor Exemplar Synthesis Library (PC)
pDS1110-SN1	Lattice Semiconductor Exemplar Synthesis Library (Sun)
pDS2110-3UP/PC1	3000 Family Upgrade (PC)
pDS2110-3UP/SN1	3000 Family Upgrade (Sun)
pDS1131-PC1	Verilog and VITAL Compliant VHDL Simulation Libraries (PC)
pDS1131-SN1	Verilog and VITAL Compliant VHDL Simulation Libraries (Sun)

Annual Maintenance**

pDS2110M-PC1	Maintenance for pDS2110-PC1
pDS2110M-SN1	Maintenance for pDS2110-SN1
pDS1110M-PC1	Maintenance for pDS1110-PC1
pDS1110M-SN1	Maintenance for pDS1110-SN1
pDS1131M-PC1	Maintenance for pDS1131-PC1
pDS1131M-SN1	Maintenance for pDS1131-SN1

**One year of maintenance is provided with every product purchase.

Warranty/Update Service

• 90-day warranty on disk media
• One-year maintenance support included with purchase
• Annual maintenance agreement available

Technical Support Assistance

Hotline:	1-800-LATTICE (Domestic)
	1-408-428-6414 (International)
BBS:	1-408-428-6417
FAX:	1-408-944-8450
email:	apps@latticesemi.com