# pDS® Software

## Features

- **ispLSI® AND pLSI® DEVELOPMENT SYSTEM**
  - **— Supports ispLSI and pLSI 1000/E and 2000/V/LV**
  - **— Upgrade to Support ispLSI and pLSI 3000 and 6000**
- **DESIGN ENTRY WITH EASY-TO-USE WINDOWS™ ENVIRONMENT**
  - **— ABEL-Like Boolean Equation Entry**
  - **— Logic Macro Entry with Over 275 "TTL-Like" Macros and Over 200 TTL Macros**
  - **— Manual Device Partitioning Ensures Tight Control of Performance and Utilization**
  - **— Multiple Edit Windows Support**
- **FAST DESIGN COMPILATION**
  - **— Multi-Level Logic Synthesis**
  - **— Efficient Design Optimization and Minimization**
  - **— "Hands-Free" Automatic Place and Route**
  - **— Predictable Performance**
- **COMPLETE DESIGN VERIFICATION**
  - **— Functional and Timing Simulation Options**
- **INDUSTRY STANDARD JEDEC PROGRAMMING FILE GENERATION**
  - **— Standard JEDEC Fuse Map**
- **IN-SYSTEM PROGRAMMING SUPPORT**
  - **— ispCODE™ C Source Routines Included**
  - **— ISP Daisy Chain Download**
  - **— ispATE™ Board Test Programming Utility**
- **PLATFORMS SUPPORTED**
  - **— PC Windows 3.1/Windows 95/ Windows NT**

## Introduction

The pDS software is a comprehensive design package for the Lattice Semiconductor Corporation (LSC) ispLSI and pLSI device families giving full design entry and device implementation capabilities under the Windows design environment. The pDS software provides the best solution for high performance designs which require direct control of the logic implementation. It offers designers complete control over the performance and utilization of the device. The pDS software allows designers to quickly move from concept to a programmed logic device.

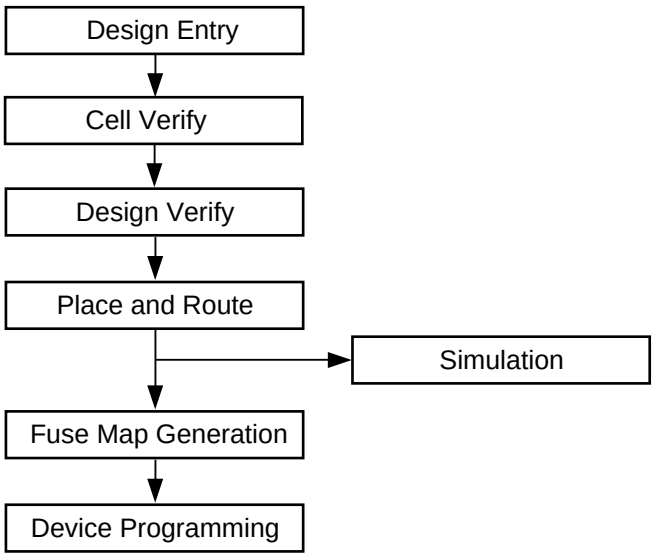
The pDS software also offers simulation options for full functional and timing simulation of designs using a variety of third-party simulators.

## pDS Software

Using the pDS software, designs can be defined completely using simple Boolean equations and "TTL-like" or TTL logic macros. Automated design capabilities shorten design cycles allowing designers to explore several design solutions before deciding on the one that provides the best solution.

Designs can be entered in two ways: either through the integrated edit windows within the pDS software, or by using a standard ASCII text editor to create a design file that can be imported into the pDS environment. The Place and Route software automatically places the logic and routes the interconnections. The fuse map program generates a fuse file which can then be downloaded into a device programmer or directly to an ispLSI device (see figure 1).

**Figure 1. pDS Design Flow**




## Design Entry

pDS software offers an easy to use interface as shown in figure 2. Designers can quickly enter the design into GLBs and I/O cells through this interface. An example of an edit window is shown in figure 3. Tables 1, 2 and 3 provide a condensed list of the different operations which are supported in the pDS software.

**Figure 2. pDS Software User Interface**

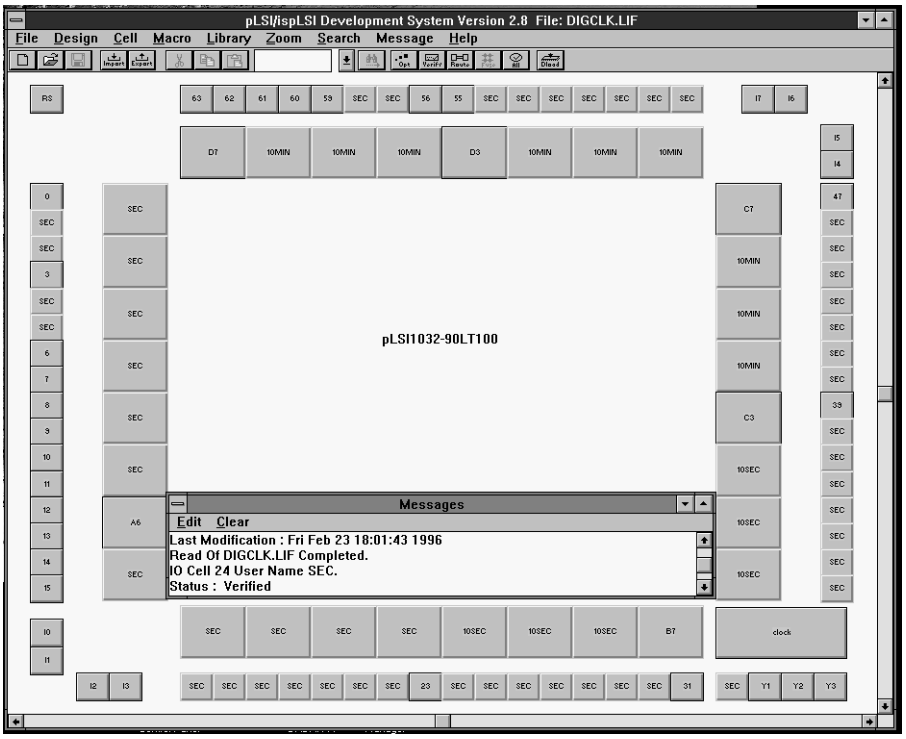



**Figure 3. Sample Edit Window Illustrating Boolean Equations and Macros**

```
SIGTYPE CO_P OUT;
SIGTYPE C1   REG OUT;
XOR4 (par, D1, D2, D3, D4)
EQUATIONS
     CO_P = CO_0 & CO_1 # CO_2;
     C1   = C1$$  C0;
     C1.CLK = SYSCLK;
END;
```

The following tables show some of the pDS software keywords, operators and dot extensions used.

**Table 1. Keywords**

| Keyword | Description |
|---|---|
| CONSTANT | Assigns a value to a signal |
| SET | Assigns a label to a group of signals |
| SIGTYPE | Assigns specific attributes to a GLB output |
| CRIT | Used for the 4 product term bypass |
| XPIN | Identifies external signal in the I/O cell |
| LOCK | Locks an I/O cell to a pin |
| EQUATIONS | Beginning of the Boolean description of the logic in a GLB |
| // | The text that follows is a comment |

**Table 2. Operators**

| Operator | Description |
|---|---|
| = | Assignment |
| ! | Inversion |
| $$ | Hardware exclusive OR |
| & | AND |
| # | OR |
| $ | Exclusive OR |
| !$ | Exclusive NOR |

**Table 3. Dot Extensions**

| Extension | Description |
|---|---|
| .D | Identifies the signal as the D input |
| .Q | Identifies the signal as the Q output |
| .RE | Identifies the product term reset signal for the GLB |
| .CLK | Identifies the system clock for the GLB |
| .PTCLK | Identifies the product term clock for the GLB |
| .OE | Identifies the output enable signal for the I/O cells within the megablock |

The pDS software offers an extensive selection (over 275) of TTL-like macros. These macros enable the design engineer to use familiar pre-defined functions to build a design. Table 4 shows a summary of the TTL macros also available in the pDS software.

## Logic Optimization

The pDS software provides extensive design rule checking during the optimization and fitting process. After the design has been checked, the software initiates logic minimization to reduce the number of product terms needed. There are two minimization options:

— Fast Min
— Strong Min

The Fast Min option performs quick minimization to reach the debugging stage sooner. The Strong Min option performs a comprehensive logic minimization to maximize device resource utilization and ensures efficient design implementation. With the Strong Min option, small design changes can generally be performed without expensive PC board rework.

## Automatic Place and Route

The pDS software provides an automatic place and route routine which eliminates the need for manual routing and provides a quicker design cycle time. The router automatically generates pinouts based on an optimal design implementation or it can use a user defined pinout.

Incremental place-and-route capability allows last-minute logic updates to be implemented without design pin-out changes.

## Post Route Simulation

Complete post route design verification can be peformed using optional third party timing simulators.

## Fuse Map Generation

The Lattice Semiconductor fuse map generation module outputs the file containing the fuse pattern used to implement the logic in the device. A security feature offers protection of proprietary designs from unauthorized duplication.

**Table 4. Macro Summary**

| Function Type | Number of Macros | Number of TTL Functions |
|---|---|---|
| AND/NAND | 20 | 11 |
| OR/NOR | 16 | 8 |
| XOR/XNOR | 4 | 2 |
| Decoder/Encoder | 17 | 16 |
| AND/OR | 8 | 7 |
| Flip/Flop | 28 | 19 |
| Latch | 10 | 6 |
| Arithmetic | 17 | 16 |
| Counter | 22 | 20 |
| Shift Register | 14 | 14 |
| MUX/DEMUX | 15 | 12 |
| Miscellaneous | 14 | 13 |

## System Requirements

— 486/Pentium IBM Compatible PC
— MS DOS Version 3.3 or Later
— MS Windows Version 3.1 or Later
— MS Windows 95
— MS Windows NT
— 8 MB RAM and 10 MB Hard Disk Space
— Parallel Printer Port for Software Key
— VGA or Higher Resolution Display
— Mouse (Windows Compatible)

## Product Ordering Information

| Product Code | Description |
|---|---|
| pDS1101-PC1 | pLSI/ispLSI Development System (pDS) |
| pDS1101-3UP/PC1 | pLSI and ispLSI Development System (pDS) 3000 and 6000 Family Upgrade |
| pDS3302-PC2 | Viewlogic Viewsim Timing & Functional Simulator |
| pDS1102-PC2 | Viewlogic Viewsim Simulation Libraries and Interface Files |
| pDS1170-PC1 | OrCAD VS386+ Simulation Libraries and Interface |
| pDS1131-PC1 | VHDL and Verilog Simulation Libraries |
| **Annual Maintenance*** | |
| pDS1101M-PC1 | Maintenance for pDS1101-PC1 |
| pDS1102M-PC2 | Maintenance for pDS1102-PC2 |
| pDS1170M-PC1 | Maintenance for pDS1170-PC1 |
| pDS1131M-PC1 | Maintenance for pDS1131-PC1 |
| pDS3302M-PC2 | Maintenance for pDS3302-PC2 |

*One year of maintenance is provided with every product purchase.

## Programmer Support

All devices in the ispLSI device families can be programmed while installed on the target circuit board. In-system programming can performed using an ispDOWNLOAD™ Cable and PC, by an on-board microprocessor or by ATE systems during final board test.

All ispLSI and pLSI devices can also be programmed using third-party PLD programmers. The devices are currently supported by programmers from the following vendors:

**Table 5. Programming Support**

| Programmer Vendor | Model |
|---|---|
| Advin Systems | Pilot-U84 |
| | Pilot-U40 |
| | Pilot-GL/GCE |
| BP Microsystems | PLD-1128 |
| | CP-1128 |
| Data I/O | 2900 |
| | 3900 |
| | Unisite 40/48 |
| Logical Devices | Allpro 40 |
| | Allpro 88 |
| SMS Micro Systems | Sprint Expert |
| Stag | System 3000 |
| | ZL30/A |
| System General | TURPRO-1 |

High pin-count socket adapters are available from Emulation Technology, EDI Corporation and PROCON.

## Warranty/Update Service

- 90-day warranty on disk media
- One-year maintenance support included with purchase
- Annual maintenance agreement available

## Technical Support Assistance

Hotline: 1-800-LATTICE (Domestic)
1-408-428-6414 (International)
BBS: 1-408-428-6417
FAX: 1-408-944-8450
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