Latch-up Protection

Introduction

Lattice Semiconductor's Programmable Logic Devices (PLDs) are manufactured using a high-performance $E^2CMOS^{®}$ process. CMOS processing provides maximum AC performance with minimal power consumption. A drawback common to all CMOS technologies is the potentially destructive phenomenon known as latch-up.

This application note defines latch-up, how it manifests itself, and what techniques have been used to control it. Also described are three device features, employed in Lattice devices constructed with E^2CMOS technology (up to and including UltraMOS IV), that prevent the occurrence of latch-up.

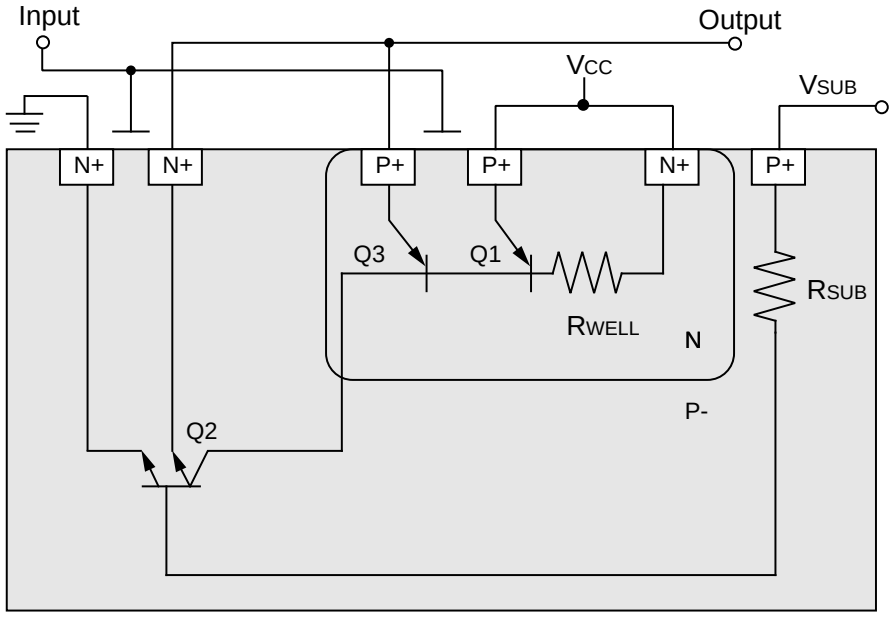
Latch-up is a destructive bipolar device action that can potentially occur in any CMOS-processed device. It is characterized by extreme runaway supply current and consequential smoking plastic packages. Latch-up is peculiar to CMOS technology, which integrates both P and N channel transistors on one chip.

In the doping profile of a CMOS inverter, parasitic bipolar (PNPN) silicon-controlled-rectifier (SCR) structures are formed. Figure 1 shows the process cross-section of a CMOS inverter, as well as the bipolar components to the parasitic SCR structure. In steady-state conditions, the SCR structure remains off. Destruction results when stray current injects into the base of either Q_1 or Q_2 (see Figure 1). The current is amplified with regenerative feedback (assuming that the beta product of Q_1 and Q_2 is greater than unity), driving both Q_1 and Q_2 into saturation and effectively turning on the SCR structure between the device supply and ground. With the parasitic SCR on, the CMOS inverter quickly becomes a nonrecoverable short circuit; metal trace lines melt and the device becomes permanently damaged.

Causes of Latch-Up

It has been explained that parasitic bipolar SCR structures are inherent in CMOS processing. If triggered, the SCR forms a very low-impedance path from the device supply to the substrate, resulting in the destructive event. Two conditions are necessary for the SCR to turn on: The beta product of Q_1 and Q_2 must be greater than unity, which, although minimized, is usually the case; and a trigger current must be present. The cause of latch-up is best understood by examining the mechanisms that produce the initial injection current to trigger the SCR

Figure 1. CMOS Inverter Cross-Section



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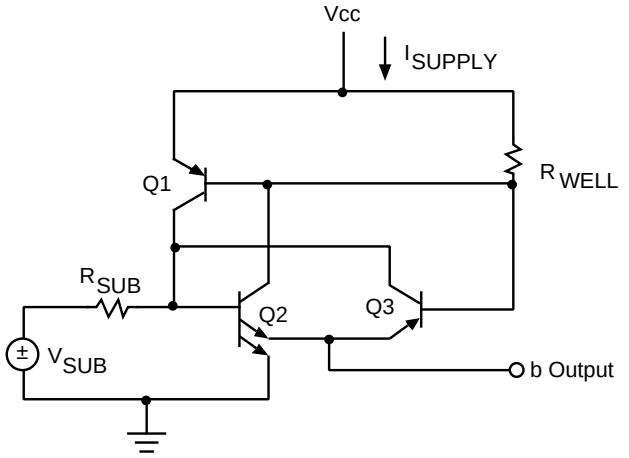
network. Figure 2 is a schematic of the parasitic bipolar network present in a CMOS inverter, where node "b" is the inverter output. It can be seen that two events might trigger latch-up: 1) the inverter output could overshoot the device supply, thereby turning on Q_3 and injecting current directly into the base of Q_2; and 2) the inverter output could undershoot the device ground, turning on Q_2 immediately. However, a third condition could also trigger latch-up; if the supply voltage to the P+ diffusion was to rise more quickly than the N-well bias, Q_1 could turn on. Within the device circuitry, overshoot and undershoot can be controlled by design. A problem area exists at the device inputs, outputs and I/Os because external conditions are not always perfect. Powering-up can also be a potential problem because of unknown bias conditions that may arise.

With CMOS processing, the possibility of latch-up is always present. The major causes of latch-up are understood and it is clear that if CMOS is to be used, solutions to latch-up will have to be created. As the technology evolves, solutions to latch-up are becoming more creative. Two of the more straightforward solutions are presented here.

One direct way to reduce the threat of latch-up is to inhibit Q_2 (Figure 1) from turning on. This has been accomplished by grounding the substrate and reducing the magnitude of Rsub through the use of wafers with a highly conductive epitaxial layer. While the technique is successful, the wafers are more expensive to manufacture, due to the extra processing required to form the epitaxial layers.

The extensive use of "guard rings" helps to collect stray currents which may inadvertently trigger an SCR structure. A disadvantage to heavy use of guard rings is the constraints placed on circuit design and topological layout, and the resulting increase in die size and cost.

Figure 2. Parasitic SCR Schematic



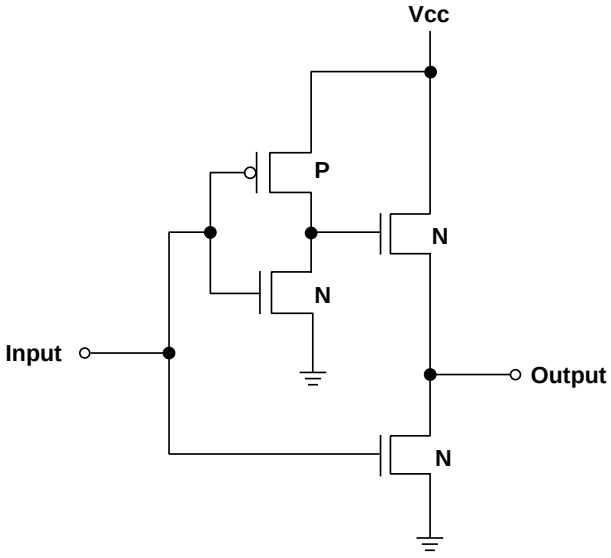
The Latch-Lock™ Approach

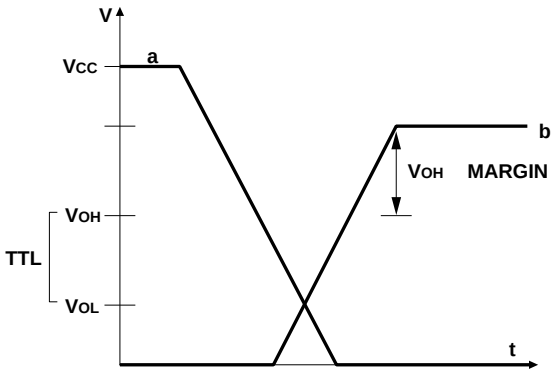
The intent of the GAL® family was to implement cost-effective solutions to each major cause of latch-up. The goal was met through three device features.

The most susceptible areas for latch-up are the device inputs, outputs and I/Os. Extreme externally applied voltages may cause a P+N junction to forward-bias, leading to latch-up. The inputs, by design, are safe; but outputs and I/Os present a danger.

To prevent latch-up by large positive swings on the device outputs or I/O pins, NMOS output drivers were

Figure 3. NMOS Output Driver





used. This eliminates the possibility of turning on Q_3 (Figure 2) with an output bias in excess of the device supply voltage. Figure 3 contains the effective NMOS output driver and its switching characteristics. Note that the output does not fully reach the supply voltage, but still provides adequate V_{OH} margin for TTL compatibility.

To prevent negative swings on device output and I/O pins from forward-biasing the base-emitter junction of Q_2, a substrate- bias generator was employed. By producing a V_{sub} of approximately -2.5v, undershoot margin is increased to about -3V.

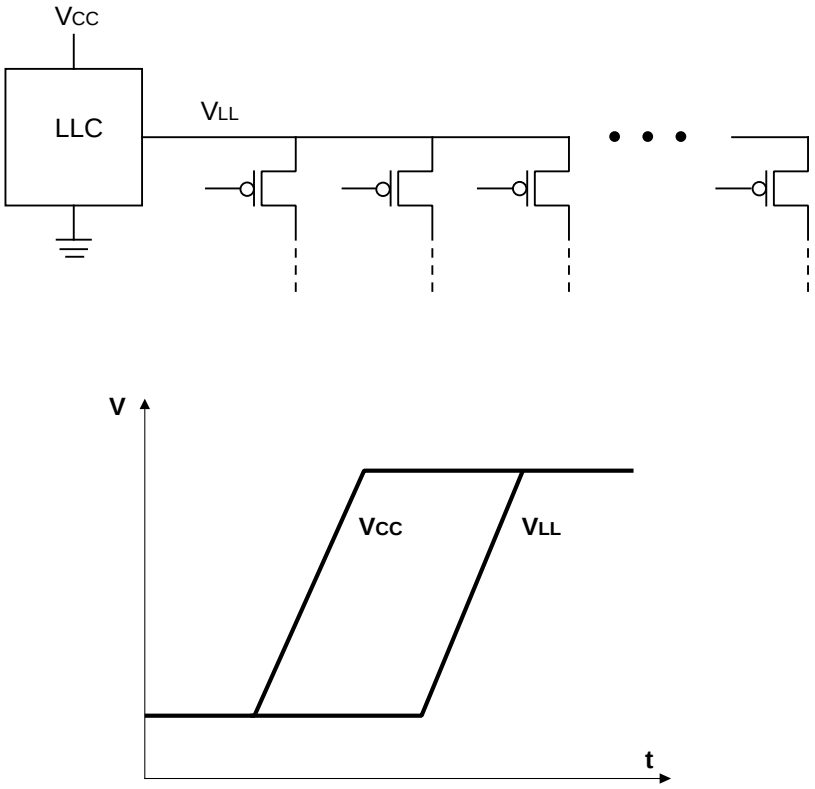
To insure that no undesired bias conditions occur with P+ diffusions, Lattice has developed proprietary Latch-Lock power-up circuitry, illustrated in Figure 4. In short, the drain of all P channel devices normally connected to the device supply is now connected to an alternate supply that powers up after the device N-wells have been biased and the substrate has reached its negative clamp value. This prevents any hazardous bias conditions from developing in the power-up sequence. After power-up is complete, the Latch-Lock circuitry becomes dormant until a full power-down has occurred. This eliminates the chance of an unwanted P channel power-down during device operation.

To determine the amount of latch-up immunity achieved with the three device features utilized in Lattice devices, an intensive investigation was carried out. Each step was conducted at 25° and 100°C; inputs, outputs, and I/Os were sequentially forced to -8V and +12V while the device underwent fast and slow power-ups; devices were repeatedly “hot socket” switched with up to 7.0V.

Even under the extreme conditions specified, no instance of latch-up occurred. In an attempt to provoke latch-up, ± 50mA was forced into each output and I/O pin. The device output drivers were damaged in the battle, and still latch-up was not induced.

Based on the data, it is evident that Lattice devices based on the Latch-Lock technology are completely immune to latch-up, even when subjected to a wide variety of extreme conditions, including current at inputs, outputs, and I/Os, power-supply rise time, hot-socket power-up and temperature.

Figure 4. Latch-Lock Power-Up Circuitry



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