ispATE™ Software

Vector Creation Utility for In-System Programming of ISP™ Devices on Automatic Test Equipment

Lattice Semiconductor Corporation

Features

- **TEST VECTOR CREATION UTILITY FOR IN-SYSTEM PROGRAMMING OF ISP DEVICES USING AUTOMATIC TEST EQUIPMENT (ATE)**
  - **Simplifies In-System Programming on a Tester**
  - **Generates Programming or Programming/ Verification Vectors**

- **SUPPORTS POPULAR AUTOMATIC TEST EQUIPMENT**
  - **Teradyne Z1800 Series of Board Testers**
  - **GenRad GR228X Series of Board Testers**
  - **Hewlett-Packard HP3065 and HP3070 Families of Board Testers**
  - **Additional Tester Support Planned**

- **PROGRAMMING OF SINGLE OR MULTIPLE ISP DEVICES IN A DAISY CHAIN PROGRAMMING CONFIGURATION**
  - **Single Set of ISP Programming Signals Programs Multiple Devices**
  - **Only TTL-Level Signals Needed to Program ISP Devices**

- **WINDOWS AND DOS VERSIONS FOR PC**
  - **Windows Version Provides Windows User Interface and On-Line Help**
  - **DOS Version Accepts Command Line Entry of Test Vector Parameters**

- **ACCEPTS PROGRAMMING FILES FROM LATTICE SEMICONDUCTOR'S DEVELOPMENT SYSTEMS**
  - **Supports pDS® and pDS+™ Software**
  - **Converts JEDEC or ispSTREAM™ Files into ISP Programming Vectors**
  - **Supports ispGAL22V10, ispGDS, and ispLSI 1000/E, 2000, 3000 and 6000 Families**

- **ISP DEVICES SIMPLIFY MANUFACTURING FLOW**
  - **Eliminate Stand-Alone Device Programming**
  - **Eliminate Unnecessary Device Handling**
  - **Eliminate Inventory Headaches**
  - **Eliminate Incorrect Device Placement on the PCB**

- **ISP DEVICES ENHANCE BOARD LEVEL TESTABILITY**
  - **Program Lattice Semiconductor ISP Devices On-Board with "Temporary" Test Patterns/Exercise Enhanced Test Functions/Re-Pattern ISP Devices with "Production" Patterns**

- **FULLY-INTEGRATED INTO THE LATEST VERSION OF ISP DAISY CHAIN DOWNLOAD SOFTWARE**

Introduction

Programming standard programmable logic devices (PLDs) is very time consuming using a stand-alone device programmer. Stand-alone programming adds costly steps to the production flow, as well as inventory headaches. By using your ATE equipment to program Lattice Semiconductor's revolutionary in-system programmable (ISP) PLDs, you can simply solder blank ISP devices onto your board like any standard component and eliminate special PLD production flows.

You can also enhance the testability of your product by developing custom logic configurations for your ISP devices specifically to enhance board test. The ISP devices can be subsequently reconfigured for their normal system functions after initial board test has been completed.

All Lattice Semiconductor Corporation (LSC) ISP devices can be easily programmed by using four or five TTL-level signals, referred to as the ISP interface. The ISP programming instructions control the serial downloading and programming of the ISP devices. Since this interface uses standard TTL-signals (no "supervoltages" required), it can easily be driven by an ATE tester.

The ispATE utility fits into the overall ISP implementation flow for programming LSC ISP devices using ATE as shown in Figure 1. One or more JEDEC files are created by LSC's pDS (proprietary) or pDS+ Fitter (third-party) development systems. These JEDEC files are then read by the ispATE utility and converted into programming vectors using the ATE's test vector format. The ATE then applies these vectors to the ISP interface pins to program or verify the ISP devices as part of the board test program.

The ispATE utility also supports the LSC daisy chain programming configuration, which allows one or more ISP devices to be programmed in a serial daisy chain through a single set of ISP programming signals.

ispATE Overview

ispATE creates ATE-compatible programming test vectors. Both DOS command line and DOS shell menu versions of ispATE are available. The ispATE utility

1996 Data Book

converts one or more JEDEC files into a series of test vectors compatible with either HP or Teradyne board testers. When the ATE drives the ISP interface of the ISP devices with the test-vector series, the ATE will program the ISP devices. Note that these vectors are not "functional test" vectors: their only purpose is to program the ISP devices with the JEDEC file contents.

Multiple ISP devices can be programmed through a single ISP interface (see Figure 2) if they are daisy chained together (see also the ISP Architecture and Programming section of this Data Book). The ispATE utility also supports ATE programming through this interface. To do so, the user must construct a configuration file, which lists the device type, order, and JEDEC file name, to determine the proper sequence of programming vectors. The configuration file is in an ISP Daisy Chain Download configuration file (.dld) format.

ISP Daisy Chain Download Configuration File (.dld)

The syntax of the ISP Daisy Chain Download format configuration file (.dld) is similar to the ispCODE configu-

ration file. The device type (the number only) is followed by the operation to perform (this is ignored by ispATE) and the JEDEC (.jed) file name. Note that a .dld configuration file does not support reading a Bitstream (.isp) file.
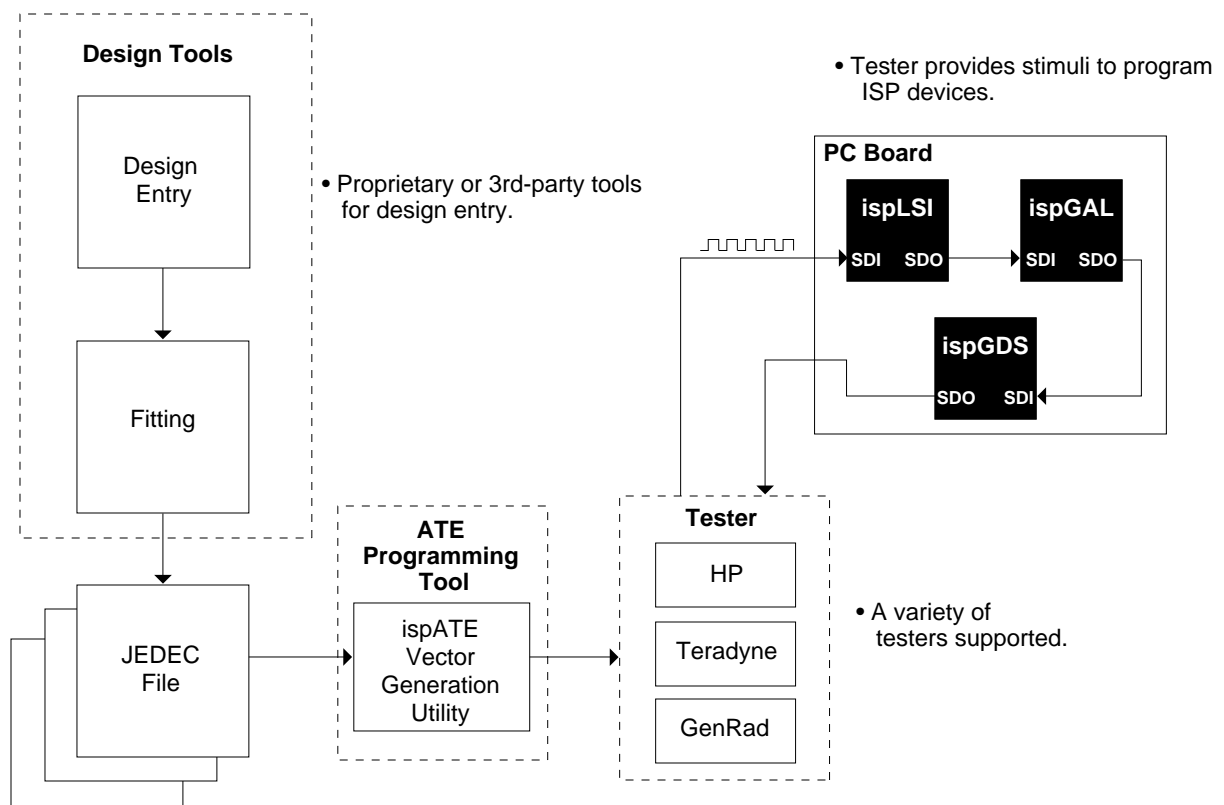
For example:

```
1024    V       1024F.JED
1016    PV      LAGO_16.JED
1032    V       1032HA.JED
1048C   PV      ADD16A.JED
```

Operation options are program (P) and verify (V).

The first device in the list is the device whose SDI pin is connected to the ISP programming hardware interface, i.e. devices are listed "first" to "last" in the chain.

Figure 1. ISP Implementation Flow Using ispATE

DOS Version of ispATE

The DOS version of ispATE accepts command line entry of test vector parameters. If you invoke ispATE without any parameters, ispATE will display a help message listing the available options, like the example in Listing 1.

The DOS dialog box interface of ispATE provides the same capability as the DOS command line version. It also provides on-line help for a more detailed explanation of the parameters.

Example Output

The vector files produced by both the DOS and Windows versions of ispATE are in ASCII format, with one vector per line. Examples of the HP-PCF format, Teradyne Table Format and GenRad Table Format are shown below:

HP-PCF Format

As an example, the HP-PCF test-vector format is shown in the listing below. Line 1 in the listing is an example of

Figure 2. Daisy Chain ISP Programming Configuration Example
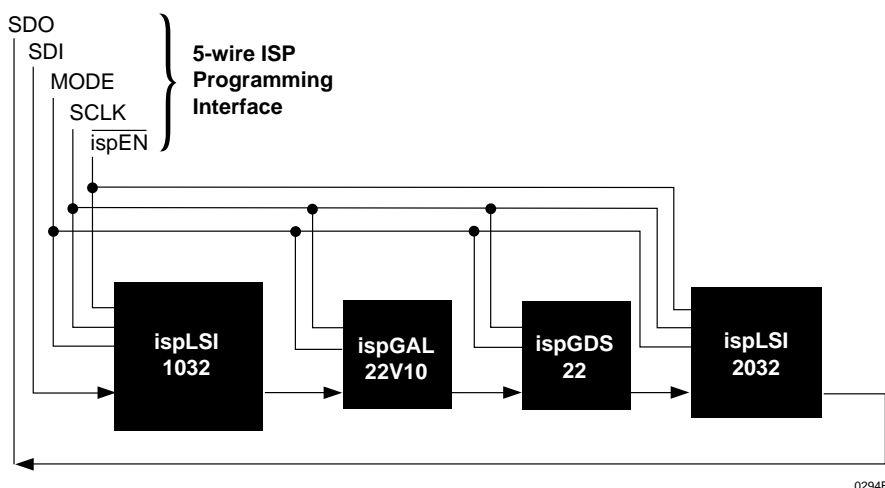
Note: The ispLSI 1032 would be the first device in the chain description for a .DLD configuration file.

Listing 1. ispATE help message listing available options.

```
USAGE        :  ispATE config_file tester num_vectors vec_file header
config_file  :  ISP Daisy Chain Download format .dld file.
tester       :  HP3070
                HP3065
                Ter1800 (Teradyne Z1800 series)
                Generic
num_vectors  :  The upper limit on how many vectors to use per file 0 for no limit.
vec_file     :  Name of the file(s) to contain the generated vectors
                Just enter the base name — the converter will add the rest
                For example, foo becomes foo01.pcf,foo02.pcf, ...
header       :  The name of the text file to paste at the start of each vector file
```

a test vector. The value of every pin in the ISP interface is defined in this line as a one (1), zero (0), or don't care (X). The tester will read this line and apply the indicated values. Not shown in this example is a mapping statement, which defines how the columns correspond to the ISP interface. In this example, the signals are mapped from left to right as ispEN, MODE, SCLK, SDI and SDO.

```
"0000X"
"0100X"
"0101X"
! Vector 70
"0111X"
"0101X"
"0100X"
"0000X"
"0000X"
"0010X"
"0000X"
end pcf
wait 300m
pcf
"0000X"
"0100X"
"0101X"
! Vector 80
end pcf
wait 500u
pcf
"0111X"
"0101X"
"0100X"
"0000X"
"0000X"
"0100X"
end pcf
wait 500u
pcf
"0110X"
"0100X"
"0000X"
"0000X"
```

Teradyne Format

The listing below is a section from a Teradyne Table format vector file. An "X" indicates a "don't care" state for a pin, an "L" indicates that the pin should be driven to a 0, and an "H" indicates that the pin should be driven to a 1.

The order of the signals is 10 ms Delay, 1 ms Delay, ispEN, MODE, SCLK, SDI and SDO.

```
LLLHHHX;
LLLHLHX;
LLLHLLX;
LLLLLLX;
LLLLLLX;
LLLLHLX;
LLLLLLX;
  'Waiting 300 milliseconds
  'Pulse the 10ms delay 1shot
Begin REPEAT 30;
HL——X;
LL——X;
End REPEAT;
LLLLLLX;
LLLHLLX;
  ' Vector 100
LLLHLHX;
  'Pulse the 1ms delay 1shot
Begin REPEAT 1;
LH——X;
LL——X;
End REPEAT;
LLLHHHX;
LLLHLHX;
LLLHLLX;
LLLLLLX;
LLLLLLX;
LLLHLLX;
  'Pulse the 1ms delay 1shot
Begin REPEAT 1;
LH——X;
LL——X;
End REPEAT;
LLLHHLX;
LLLHLLX;
LLLLLLX;
  ' Vector 110
LLLLLLX;
```

GenRad Format

The listing below is a section from the GenRad Table. An "X" indicates a "don't care", 0 and 1 indicates the logic low and high respectively, and a "C" indicates a clock pulse. The order of the signals are the same as the previous two format as follows: ispEN, MODE, SCLK, SDI, and SDO.

```
00C0X
0000X
0100X
0101X
0111X
0101X
0100X
0000X
0000X
0010X
0000X
+wait 300m
0000X
0100X
0101X
+wait 500u
0111X
0101X
0100X
0000X
0000X
0100X
+wait 500u
0110X
0100X
0000X
0000X
0100X
0101X
0111X
0101X
```

Partitioning Vectors into Individual Files

A large number of vectors are required for programming an ISP device, especially if you are programming and verifying the larger devices in the ispLSI families. You may find that your ATE requires that you partition the files into multiple file sets, due to the number of vectors and limitations imposed by the amount of available tester memory. The ispATE tool supports this by allowing you to enter a maximum number of vectors to be included in any one file.

Hardware Considerations

Maintaining Signal Values between Vector Files

Since the vector files may need to be split for ATE processing, it is critical that the ATE not inadvertently change the state of the ISP clock pin (SCLK) between files. The software will insure that the last vector of a file will have the SCLK pin held low. If the ATE allows the pins to float while the next file is being loaded, the SCLK pin should have a pull-down resistor connected to it to insure that the clock does not glitch and put the ISP device into an invalid state.

ISP Interface

Lattice Semiconductor also recommends that the ISP interface signals be held at their inactive state when not being driven by the tester. You can simply add pull-down resistors to the ISP interface programming fixture to accomplish this.

Timing

When you program LSC ISP devices, you must insure that the specified erase, programming, and verification times are met by the ATE (these timing parameters are specified in the LSC Data Book and data sheets for the appropriate devices). The ispATE utility will implement these programming delays in different ways, depending on your tester manufacturer and model (see vector file examples on previous page). However, you must insure that if you change the vector cycle time (for HP), or make one-shot delay changes (for Teradyne), that you will not violate the timing specifications that ispATE used when originally creating the vector file. Since these issues are model dependent, they are discussed in detail below.

HP

ispATE currently supports two families of HP ATE board testers (the HP3070 and the HP3065). The 3070 testers support delays by using a "WAIT" statement. For example, if "WAIT 80 ms" appears in the PCF vector file, then the ATE will wait 80 ms at that point.

The 3065 testers do not support the wait statement, so ispATE will use repeat loops to implement the required delays. ispATE assumes a 1 MHz test-vector rate, so if you later decide to change the cycle time, it is critical that you update the timing loops as well. Lattice Semiconductor also provides an AWK utility called FIXCYCLE to update repeat loop counters for other vector cycle times.

This utility is included with ispATE and is available as a DOS executable called FIXCYCLE.EXE, and as an AWK source file called FIXCYCLE.AWK if you need to run the conversion on a UNIX platform.

Teradyne Z1800

Since the Teradyne Z1800 family of board testers does not support timing through repeat loops, accurate timing requires the introduction of external delay "one-shots" to the test fixture. ispATE assumes that there will be a 10 ms and a 1 ms one-shot present in the test fixture, and generates strobe signals to trigger the one-shots to create the desired delays. Teradyne has built a custom test-fixture board for ISP programming which generates accurate delay pulses; contact Teradyne Applications Engineering at (510) 932-6900 for further information.

GenRad GR228X

LSC ispATE software generates a generic vector format for GenRad testers. The generic vector files must be converted to a specific GenRad Tester format by using the utilities provided by GenRad. The "+wait" statements are converted by the GenRad utility to properly time the ISP programming and verification pulse widths. Contact GenRad Inc. at (508) 287-7000 to obtain the GenRad utilities.

Optimizing for Programming Speed

Programming ISP devices can take several seconds per device. To minimize the programming time, ispATE programs the devices in the chain in parallel and uses the minimum test vector set.

Skipping Bulk Erase Verification Vectors

If you generate both programming and verification vectors, approximately one-third of the total number of vectors will be devoted to verification, or reading back of the device contents. Since verification has a 1 ms delay between rows, as opposed to the 80 ms delay for programming rows, verification vectors do not consume two thirds of the total amount of programming time. To reduce programming time, depending on your application, verification may be eliminated. You may be performing functional test of the board, which would make this verification step redundant. In this case, you can tell ispATE to generate vectors for programming only.

How to Obtain ispATE

The ispATE vector-creation utility is provided free of charge by Lattice Semiconductor. You can download it from the LSC BBS at (503) 693-0215. The file name is ispate.zip. The DOS version is included in the zip file, along with useful utilties.

Technical Support Assistance

Hotline:	1-800-LATTICE (Domestic)
	1-503-693-0201 (International)
BBS:	1-503-693-0215
FAX:	1-503-681-3037
email:	gal@latticesemi.com
Teradyne	1-510-932-6900
GenRad	1-508-287-7000
HP	1-800-452-4844

LATTICE SEMICONDUCTOR CORPORATION
5555 Northeast Moore Court
Hillsboro, Oregon 97124 U.S.A.
Tel.: (503) 681-0118
FAX: (503) 681-3037
http://www.latticesemi.com   November 1996