pDS+™ Mentor Software

Features

- **ispLSI® AND pLSI® DEVELOPMENT SYSTEM**
  - **— Supports ispLSI and pLSI 1000/E and 2000**
  - **— Upgrade to Support ispLSI and pLSI 3000**
- **DESIGN ENTRY USING MENTOR GRAPHICS DESIGN ARCHITECT SCHEMATIC CAPTURE, AUTOLOGIC AND AUTOLOGIC II SYNTHESIS AND QUICKSIM SIMULATOR**
  - **— VHDL or Verilog-HDL Entry**
  - **— Library of Over 300 Macros for Schematic Capture**
  - **— Functional and Full Timing Simulation**
  - **— Command Line Driven User Interface**
- **LATTICE SEMICONDUCTOR pDS+™ MENTOR FITTER**
  - **— Multi-Level Logic Synthesis**
  - **— Efficient Design Optimization and Minimization**
  - **— Automatic Mapping and Device Fitting**
  - **— Automatic Partitioning with High Utilization**
  - **— Predictable Performance**
- **INDUSTRY STANDARD PROGRAMMING FILE GENERATION**
  - **— Standard JEDEC Device Fuse Map**
- **IN-SYSTEM PROGRAMMING SUPPORT**
  - **— ispCODE™ C Source Routines Included**
  - **— ISP Daisy Chain Download (PC)**
  - **— ispATE™ Board Test Programming Utility**
- **PLATFORMS SUPPORTED**
  - **— HP O/S UX 9.X and Above**
  - **— Sun O/S 4.x**

Introduction

pDS+™ Mentor software from Lattice Semiconductor Corporation (LSC) offers a powerful logic design solution for Lattice Semiconductor's ispLSI and pLSI families of high density devices.

Design entry is made simple using the familiar Mentor Graphics' Design Architect schematic capture and/or Autologic synthesis tools and the pDS+ Mentor Fitter for design implementation. Lattice Semiconductor's pDS+ Mentor software offers multi-level design synthesis, automatic place and route, and efficient device utilization, delivering high performance for more complex designs. Once design implementation is complete, the pDS+ Mentor software creates the proper files for full timing simulation using Mentor Graphics' QuickSim II simulator.

Mentor Graphics Tools

Schematic capture can be completed using Mentor Graphics' Design Architect schematic editor and a Lattice Semiconductor library of over 300 macros. For top-down design, use Design Architect to capture the logic design at the architectural, logic and circuit levels. Support is also available for VHDL and Verilog-HDL design synthesis using the Autologic or Autologic II synthesis tools. Autologic synthesis can take complex high-level language or behavioral, datapath or functional descriptions and make them quick and easy. Once the schematic or synthesis netlist has been created, the interface to Lattice Semiconductor's pDS+ Mentor Fitter is through a standard EDIF file. The pDS+ Mentor Fitter also outputs a standard EDIF file for interfacing to the Mentor Graphics QuickSim II simulator. QuickSim II then allows you to accurately perform and integrate full timing simulations. Quick VHDL simulation support is expected 2Q96.

pDS+ Mentor Fitter

Lattice Semiconductor's pDS+ Mentor Fitter for ispLSI and pLSI devices is executed as a stand-alone program, using the EDIF output from Mentor Graphics tools as input. The Lattice Semiconductor Fitter provides hands-off design implementation through an intelligent multi-level synthesis algorithm, logic partitioning, automatic place and route and standard JEDEC fuse map generation for device programming. Timing simulation input files for the QuickSim simulator are generated by the Fitter and are coupled with Lattice Semiconductor's Mentor Graphics simulation library when needed by the user.

Macro Library

The Lattice Semiconductor Mentor Synthesis Libraries include over 300 high-level functions to simplify design entry. These macros enable the design engineer to use familiar, predefined functions to build a design. Direct instantiation of these functions is provided to enhance device performance and utilization.

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Figure 1. Lattice Semiconductor's pDS+ Mentor Design Flow

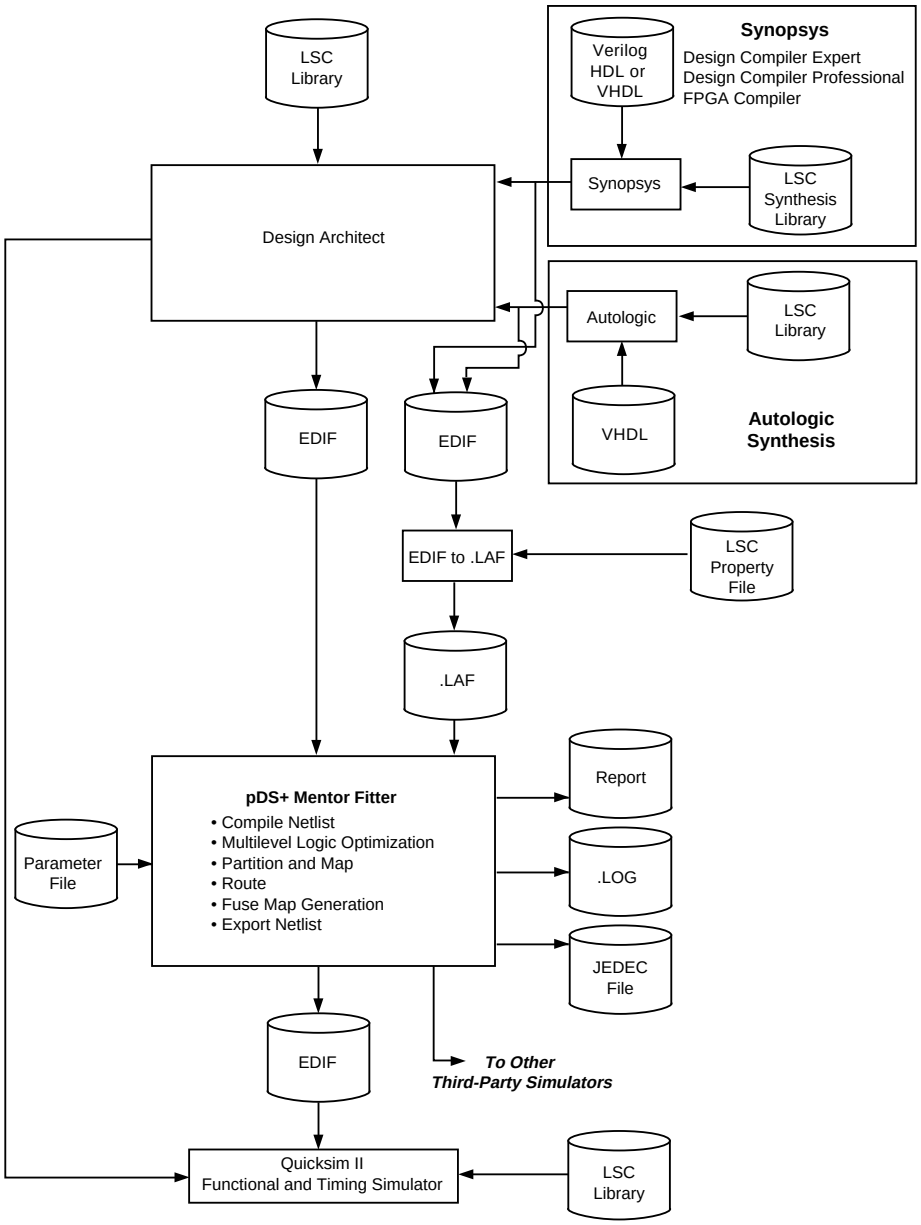

Table 1. Macro Summary

Macro Type	Quantity
AND/NAND	29
OR/NOR	24
XOR/XNOR	12
I/Os	89
Flip-Flops	39
Latches	30
Arithmetic	33
Counters	65
Shift Registers	15
Miscellaneous	45

Design Optimization & Logic Minimization

The pDS+ Mentor Fitter incorporates a powerful Automatic Partitioner for hands-free synthesis of a design into Generic Logic Blocks (GLBs). The partitioner takes full advantage of the ispLSI family's features such as the hard XOR and product term sharing. The internal XOR can be utilized for arithmetic functions, T-type flip-flops, and on and off set optimization functions. The partitioner also makes extensive use of product term sharing. Product term sharing allows the Fitter to efficiently use device resources by sharing product terms across multiple logic functions. These features combine to maximize device resource utilization and increase design performance.

Automatic Place and Route

Automatic place and route eliminates the need for manual editing and accelerates the design cycle. The Router automatically generates pinouts based on the optimal design implementation or user assigned pinouts.

The Extended Route option performs a comprehensive route to maximize device resource utilization and ensure efficient design implementation.

Design Parameter Control

The pDS+ Mentor Fitter offers extensive design control at the design entry level, letting the user optimize the design for maximum utilization and/or speed. All of the controls are specified using “attributes” in the design property and parameter files. The parameter and property files contain:

- — Fitter Control Options
- — Design Implementation Controls
  - — Net Attributes
  - — Pin Attributes
  - — Path Attributes
  - — Symbol Attributes

Fitter Control Options

Special properties can be passed to the pDS+ Mentor Fitter providing complete control over critical design considerations. Fitter control over design partitioning and routing optimizes the design for speed and/or device utilization.

Feature	Description
PART	Determines device type to be used.
PARAM_FILE	Allows user to specify attributes in a text file.
STRATEGY	Choice of AREA (default), DELAY or NO_OPTIMIZE. AREA optimizes device space, DELAY keeps GLB levels to a minimum and NO_OPTIMIZE does not reduce equations.
USE_GLOBAL_RESET	Causes global reset to use dedicated routing for reset.
MAX_GLB_OUT	Specifies maximum number of outputs from a GLB. Default is 4.
MAX_GLB_IN	Controls maximum number of inputs to a GLB. Default is 16 for 1K and 2K devices and 24 for 3K devices.
EFFORT	Controls optimization of partitioner.
EXTENDED_ROUTE	Choice of OFF (fixed) or ON (extended, default).
PIN_FILE	Specifies locked pin assignments.

Design Implementation Controls

Device controls are used for changing design parameters such as security. Some of these implementation controls are:

Feature	Description
ISP	Instructs Router to reserve in-system programming pins.
ISP_EXCEPT_Y2	Reserves all ISP pins except Y2 (ispLSI and pLSI 1016/E and 2032 only).
Y1_AS_RESET	Uses Y1 clock pin on ispLSI and pLSI 1016/E and 2032 as a global reset pin.
SECURITY	Sets the device security cell to prevent unauthorized fuse map read back.

Net Attributes

These properties control how the design is mapped into the specified features of the target device:

Feature	Description
CLK0-CLK2	Assigns a CLK signal to a dedicated CLK line.
IOCLK0-IOCLK1	Assigns a CLK signal to a dedicated IOCLK line if single fanout input pin.
FASTCLK	Fitter assigns CLK signal to CLK0-CLK2 or IOCLK0-IOCLK1.
SLOWCLK	Assigns the CLK signal to a GLB product term CLK.
PRESERVE	Prevents logic minimization on specified nets.
GROUP	Suggests grouping of functions in a GLB.

Pin Attributes

Feature	Description
CRIT	Specifies Output Routing Pool Bypass to minimize delay.
SLOWSLEW	Assigns slow slew rate on a specific I/O cell.
LOCK	Assigns device I/O pins to design I/O ports.
PULLUP	Specifies internal pull-up resistors.

Path Attributes

The following properties specify paths in the design that have special fitting requirements:

Feature	Description
SAP/EAP	Defines asynchronous paths to prevent signal duplication.
SCP/ECP	Defines critical paths to reduce delays.
SNP/ENP	Defines logic paths for no logic minimization.

Symbol Attributes

Feature	Description
REGTYPE	Determines where a register is to be placed (IOC or GLB).
PROTECT	Prevents removal of a primitive or a macro during minimization.
OPTIMIZE	Selects either hard or soft macros.

Parameter File

The pDS+ Mentor Fitter provides the ability to use a parameter file (design.par) feature which helps designers eliminiate guesswork and optimize the designs for the right devices. It allows the user to try a number of design implementation options using all of the fitter control options in a batch mode. The parameter file instructs the partitioner and the router to maximize both device utilization and performance.

Property File

The pDS+ Mentor Fitter provides the ability to use a property file (design.prp) feature which allows the designer to control the fitter using all of the design attributes available. The property file helps guide the fitter in implementing the design in the best way.

Design Verification

The pDS+ Mentor Fitter provides a post route design file for optional timing simulation. The pDS+ Mentor software offers complete post route design verification using optional timing simulators. The pDS+ Mentor Fitter generates the files required for third-party simulation with behavioral simulation models from Logic Modeling.

Fuse Map Generation

pDS+ Mentor software generates a device fuse map in standard JEDEC format. A security feature offers protection of proprietary designs from unauthorized duplication. The Fitter appends any design test vectors in JEDEC format to the device fusemap, facilitating a quick, easy functional verification of a programmed device.

System Requirements (Sun Platform)

— Sun Sparc 4 and above
— Sun OS Version 4.x
— Open Windows 3.0
— 16 MB RAM with 30 MB Hard Disk Space
— Three-Button Mouse

System Requirements (HP Platform)

— HP 700 Workstation and Above
— HP O/S UX9.x and Above
— 16 MB RAM and 30 MB Hard Disk Space
— Three-Button Mouse

Programmer Support

All devices in the Lattice Semiconductor ispLSI device family can be programmed while installed on the target circuit board. In-system programming can be performed using a DOWNLOAD™ Cable and PC, by an on-board microprocessor or by ATE systems during final board test. All Lattice Semiconductor ispLSI and pLSI devices can be programmed using third-party programmers. These devices are currently supported by programmers from the following vendors:

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30A/B
System General	TURPRO-1/FX

High pin-count adapters are available from Emulation Technology, EDI Corporation and PROCON.

Product Ordering Information

Product Code	Description
pDS2150-HP1	pDS+ Mentor Fitter and Libraries (HP)
pDS2150-SN1	pDS+ Mentor Fitter and Libraries (Sun)
pDS2150-3UP/HP1	pDS2150 3000 Family Upgrade (HP)
pDS2150-3UP/SN1	pDS2150 3000 Family Upgrade (Sun)
pDS1150-HP1	Mentor Libraries and Interface (HP)
pDS1150-SN1	Mentor Libraries and Interface (Sun)
pDS1155-HP1	Mentor Autologic Synthesis Library (HP)
pDS1155-SN1	Mentor Autologic Synthesis Library (Sun)

Annual Maintenance*

pDS2150M-HP1	Maintenance for pDS2150-HP1
pDS2150M-SN1	Maintenance for pDS2150-SN1
pDS1150M-HP1	Maintenance for pDS1150-HP1
pDS1150M-SN1	Maintenance for pDS1150-SN1
pDS1155M-HP1	Maintenance for pDS1155-HP1
pDS1155M-SN1	Maintenance for pDS1155-SN1

*One year of maintenance is provided with every product purchase.

Warranty/Update Service

- 90-day warranty on disk media
- One-year maintenance support included with purchase
- Annual maintenance agreement available

Technical Support Assistance

Hotline:	1-800-LATTICE (Domestic) 1-408-428-6414 (International)
BBS:	1-408-428-6417
FAX:	1-408-944-8450
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