Introduction to ispLSI® and pLSI® Families

The ispLSI and pLSI Families

Lattice Semiconductor Corporation's (LSC) in-system programmable Large Scale Integration (ispLSI) and programmable Large Scale Integration (pLSI) families are the logical choice for your next design project. They're the first programmable logic devices to combine the performance and ease of use of PLDs with the density and flexibility of FPGAs. And at 180 MHz system speed, and up to 25,000 PLD gates, they're the world's fastest and highest density programmable logic devices!

There are five ispLSI and pLSI families to fit your specific application needs. LSC's premier ispLSI and pLSI 1000 family implements high integration functions such as controllers, LANs and encoders at high speeds. The second generation ispLSI and pLSI 1000E family increases in-system performance with enhanced logic utilization. The high performance ispLSI and pLSI 2000 family with its large number of I/Os handles timers and counters, as well as timing critical interfaces to high speed RISC/CISC microprocessors. The highest density ispLSI and pLSI 3000 family integrates complete system logic, DSP functions, and entire encryption or compression logic into a single package, while delivering superior performance. Finally, the ispLSI and pLSI 6000 family combines dedicated FIFO or RAM memory modules with programmable logic in a cell-based architecture to yield single-chip solutions to the most complex system design problems.

The ispLSI family incorporates Lattice Semiconductor's innovative in-system programmable™ (ISP™) technology. ISP technology allows for real-time programming, less expensive manufacturing and end-user feature reconfiguration.

ispLSI and pLSI 1000 and 1000E: The Premier High Density Families

- ❑ 125 MHz system performance
- ❑ 7.5 ns pin-to-pin delay (maximum)
- ❑ 2,000-8,000 PLD gates
- ❑ 44-pin to 128-pin packages

ispLSI and pLSI 2000/V: Unparalleled System Performance

- ❑ 180 MHz system performance (World's Fastest!)
- ❑ 5.0 ns pin-to-pin delay (maximum)
- ❑ 1,000-6,000 PLD gates
- ❑ 5 Volt and 3.3 Volt Options
- ❑ 44-pin to 176-pin packages
- ❑ High I/O to logic ratio

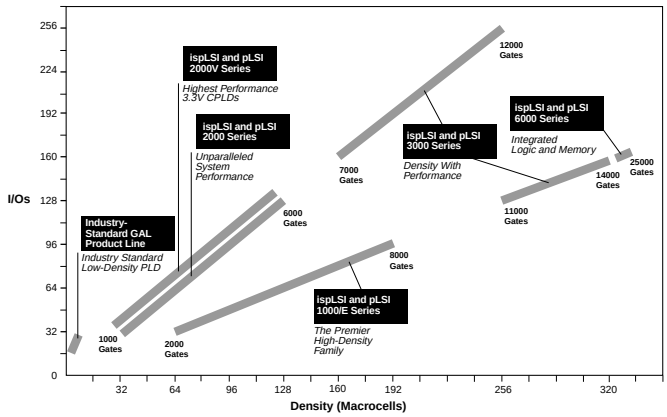
ispLSI and pLSI 3000: Density with Performance

- ❑ 100 MHz system performance
- ❑ 10 ns pin-to-pin delay (maximum)
- ❑ 7,000-14,000 PLD gates
- ❑ 208-pin to 304-pin packages
- ❑ Boundary scan for enhanced testability

ispLSI and pLSI 6000: Cell-Based Logic and Memory

- ❑ 70 MHz system performance
- ❑ 15 ns pin-to-pin delay (maximum)
- ❑ 25,000 PLD gates (including 4,000-bit dedicated memory module and eight-bank register/counter module)
- ❑ 20 ns FIFO/single-port/dual-port memory options
- ❑ 208-pin package
- ❑ Boundary scan for enhanced testability

Lattice Semiconductor's ispLSI and pLSI Families



Introduction to ispLSI and pLSI

Family Overview

From registers to counters, multiplexers to complex state machines, these families of high-density programmable logic will address your high-performance system logic needs.

Each device contains multiple Generic Logic Blocks (GLBs) designed to maximize system flexibility and performance. And a generous supply of registers and I/O cells provides the optimum balance of internal logic and external connections. A global interconnect scheme ties everything together, enabling high logic utilization.

ispLSI and pLSI Architecture

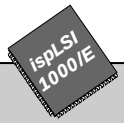
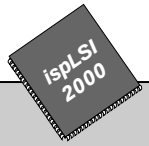
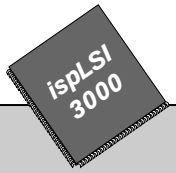
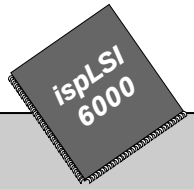
The ispLSI and pLSI architecture was constructed with real system design requirements in mind. Figure 1 shows the representation of the ispLSI 3256 architecture. This architecture provides the designer with the following advantages:

- ❑ High speed
- ❑ Predictable performance
- ❑ Low power
- ❑ Flexible architecture
- ❑ Easy to use
- ❑ Design portability across all the families
- ❑ Non-volatile in-system programmable (ispLSI)
- ❑ Advanced Global Clock Network
- ❑ Boundary Scan (3000 and 6000 families)
- ❑ Built-in memory (6000 family)

The Global Routing Pool

Central to the ispLSI and pLSI architecture is the Global Routing Pool (GRP), which connects all of the internal logic and makes it available to the designer. The GRP provides complete interconnectivity with fixed and predictable delays. This unique interconnect scheme

Table 1. ispLSI and pLSI Family Attributes

	ispLSI & pLSI 1000/E Family	ispLSI & pLSI 2000/V Families	ispLSI & pLSI 3000 Family	ispLSI & pLSI 6000 Family
				
Density (PLD Gates)	2,000 - 8,000	1,000 - 6,000	7,000 - 14,000	25,000
Speed: Fmax (MHz)	125 - 60	180 - 80	125 - 50	70 - 50
Speed: Tpd (ns)	7.5 - 20	5.0 - 15	7.5 - 20	15 - 20
Macrocells	64 - 192	32 - 128	160 - 320	192
Registers	96 - 288	32 - 128	320 - 512	416*
Memory (Bits)	—	—	—	4608
Inputs & I/Os	36 - 110	35 - 138	130 - 258	159
Pins/Package	44-, 68-, 84-pin PLCC 44-, 100-pin TQFP 120-,128-pin PQFP 44-, 68-pin JLCC 84-, 133-pin CPGA	44-, 84-pin PLCC 44-, 48-, 100-, 128-, 176-pin TQFP 128-, 160-pin PQFP 160-pin MQFP	160-, 208-, 240-, 304-pin MQFP 167-pin CPGA	208-pin MQFP

*Includes 8 x 16 Register/Counter Module

1/2/3000-2

consistently provides high performance and allows effortless implementation of complex designs.

The Output Routing Pool (ORP)

The Output Routing Pool (ORP) is a unique ispLSI and pLSI architectural feature which provides flexible connections between the GLB outputs and the output pins. This flexibility allows for "last minute" logic design changes to be implemented without changing the external pin-out.

Generic Logic Block (GLB)

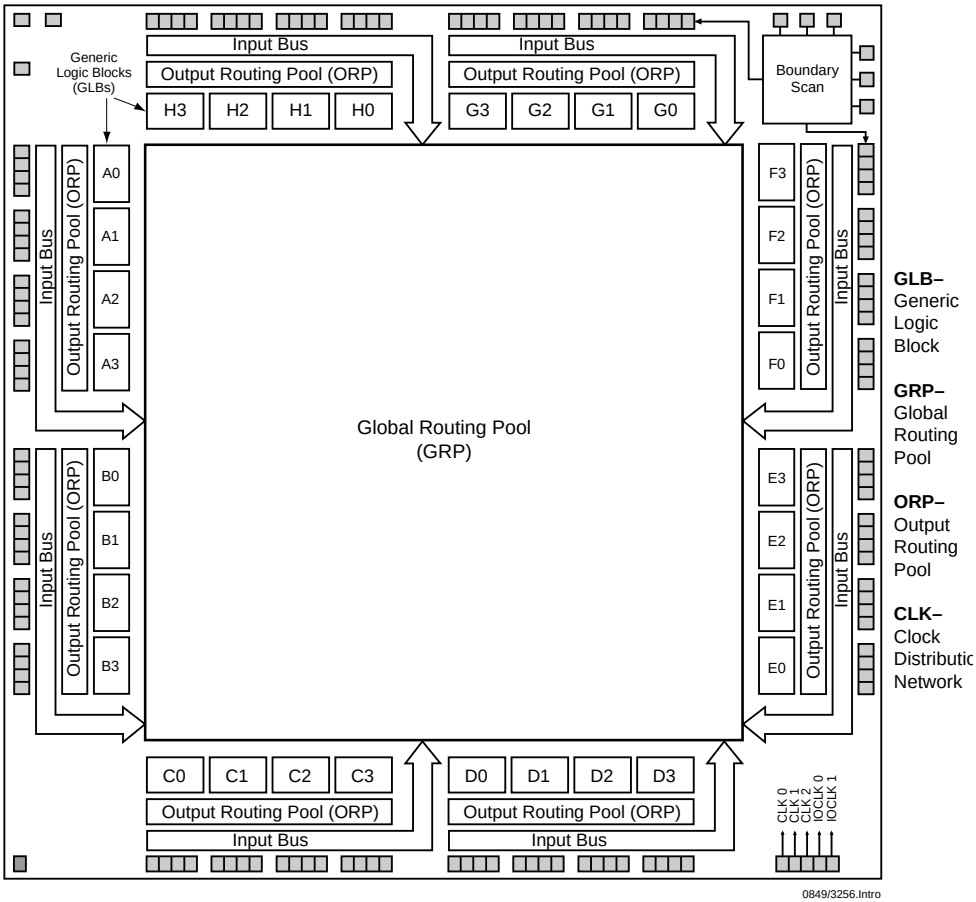
The key element in the ispLSI and pLSI architecture is the Generic Logic Block (GLB). This powerful logic block provides a high input-to-output ratio for best logic efficiency. The GLB (figure 2) used in the ispLSI and pLSI 1000/E and 2000 families feature 18 inputs which drive an array of 20 Product Terms (PTs). These product terms feed four outputs which effectively handle both wide and narrow gating functions. The ispLSI and pLSI 3000 family utilizes a Twin GLB which delivers wider logic functionality. The Twin GLB accepts 24 inputs and feeds two arrays of 20 Product Terms that ultimately drive two sets of four outputs.

The architectural flexibility of the ispLSI and pLSI GLB, combined with its optimum input-to-output ratio, allows the GLB to implement virtually all 4-bit and 8-bit MSI functions.

An additional element of architectural flexibility is the Product Term Sharing Array (PTSA). The PTSA allows the 20 PTs from the AND array to be shared with any and all of the four GLB outputs. This ability to share PTs between all of the four GLB outputs provides a highly efficient means to implement complex state machines by eliminating duplicate product term groups.

Each of the four outputs from the PTSA feeds into a flexible Output Logic Macrocell (OLMC), consisting of a D-type flip-flop with an Exclusive-OR gate on the input. The OLMC allows each GLB output to be configured as either combinatorial or registered. Combinatorial mode

Figure 1. ispLSI 3256 Functional Block Diagram



is available as AND-OR or Exclusive-OR. Registered mode is available as D, T or J-K.

The power of the GLB is further enhanced by a flexible clock distribution network. This network provides a choice of clock signals to each GLB: global synchronous clock signals or internally generated asynchronous product term clock signals.

Standard Configuration

- ❑ GLB outputs comprised of 4, 4, 5 and 7 product terms
- ❑ The PTSA can combine up to 20 product terms per GLB output to meet the needs of both wide and narrow logic functions

Figure 2. ispLSI and pLSI 1000, 1000E and 2000 Family GLB

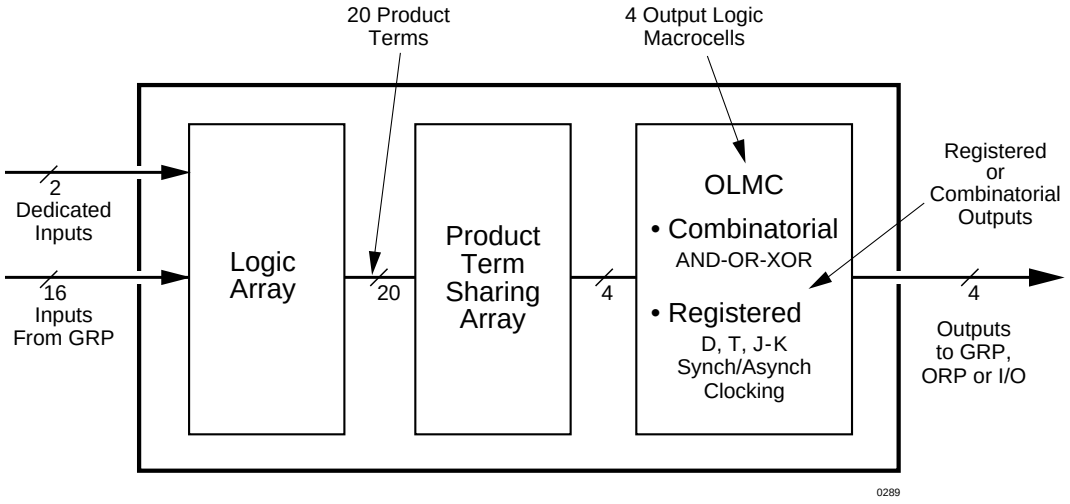
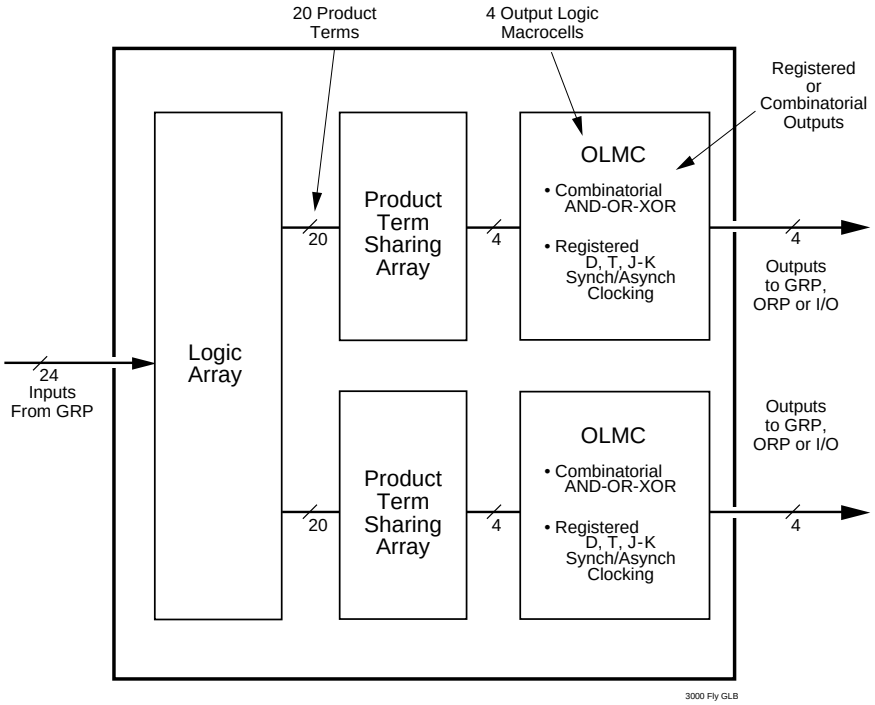


Figure 3. ispLSI and pLSI 3000 and 6000 Family "Twin GLB"



High-Speed Bypass Configuration

- ❑ For speed-critical timing paths
- ❑ Bypasses the PTSA and the Internal Exclusive-OR gate of the OLMC
- ❑ Provides four product terms per output
- ❑ Supports design of fast address decoders

Exclusive-XOR Configuration

- ❑ Utilizes powerful exclusive-XOR architecture
- ❑ Great for counters, comparators and ALU functions

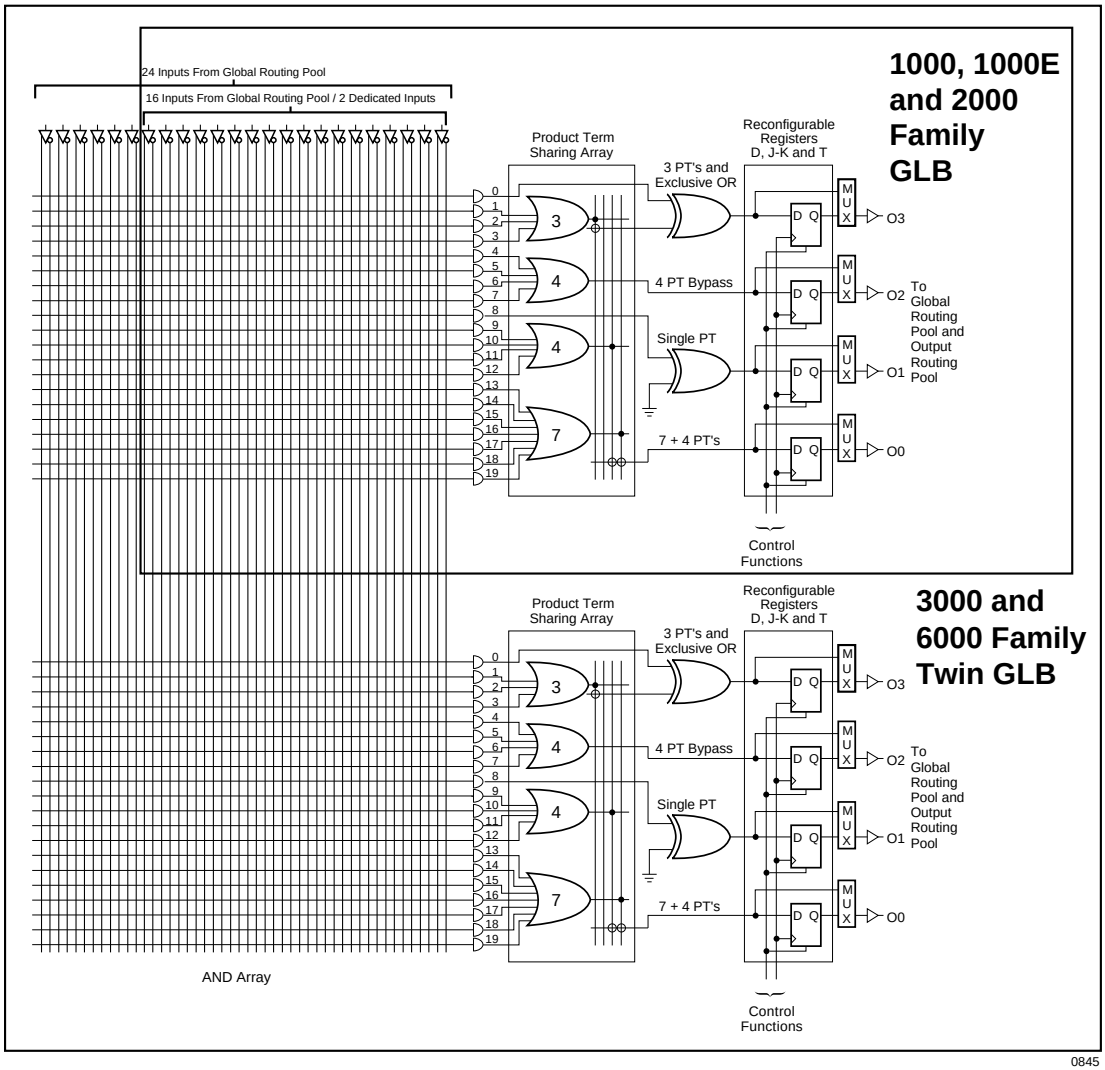
Single PT Configuration

- ❑ Small Logic Functions at Fast Speed

Multi-Mode Configuration

- ❑ Individual outputs are independently configurable
- ❑ PTSA gives flexibility in the number and selection of product terms per output

Figure 4. GLB: Multi-Mode Configuration



Security Cell

A security cell is provided in the ispLSI and pLSI devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by reprogramming the device, so the original configuration can never be examined once this cell is programmed.

Device Programming

ispLSI and pLSI devices can be programmed using a Lattice Semiconductor-approved device programmer, available from a number of third party manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is automatic and is completely transparent to the user. In-system programming is also available with ispLSI devices which allows programming on the circuit board using Lattice Semiconductor programming algorithms and standard 5V system power.

Latch-up Protection

ispLSI and pLSI devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the internal circuitry to latch-up. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups to eliminate any possibility of SCR induced latching.

In-System Programmability

LSC's ispLSI devices (in-system programmable) are the industry's only high-density programmable logic family offering non-volatile, in-system reconfigurability.

ispLSI devices are available in all five families: 1000, 1000E, 2000, 3000 and 6000. The ispLSI devices are 100 percent functionally and parametrically compatible with their pLSI counterparts, with the added capability for 5-volt in-system programmability and reprogrammability.

Complex logic functions can be implemented in multiple ispLSI devices with complete on-board configurability. In-system programming of a multiple ispLSI chip solution is easily achieved through a proprietary in-system erase/program/verify technique.

In-system programmability can revolutionize the way you design, manufacture and service systems.

Prototype Board Designs

In-system programming allows you to program and modify your logic designs "in-system" without removing the device(s) from the board. This accelerates the system and board-level debug process and enables you to define the board layout earlier in the design process.

Fine Pitch Package Handling

When programming traditional PLDs, manual handling is required during both design/debugging and manufacturing stages. When using PQFPs or TQFPs, fragile leads as thin as 0.5 mm can easily bend in the programmer socket causing coplanarity damage. With ispLSI, you can solder these packages onto your printed circuit board and still program and reprogram the devices during debugging and manufacturing – without ever losing a single part due to bent leads.

Reconfigurable Systems

Your options become boundless when you have the ability to change the functionality of devices already soldered on a PC board. You can now implement multiple hardware configurations with the same circuit board design. A variety of protocols or system interfaces can be implemented on a generic board as the last step in the manufacturing flow.

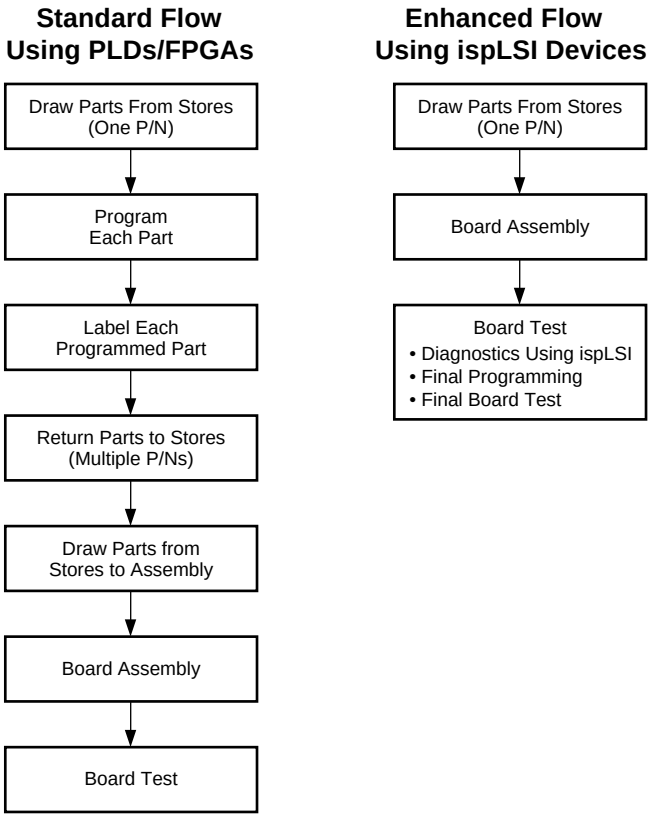
Easier Field Updates

With software reconfigurable systems, field updates are as easy as loading a new configuration from a floppy or downloading it through a modem.

Enhanced Manufacturing Flow with ispLSI

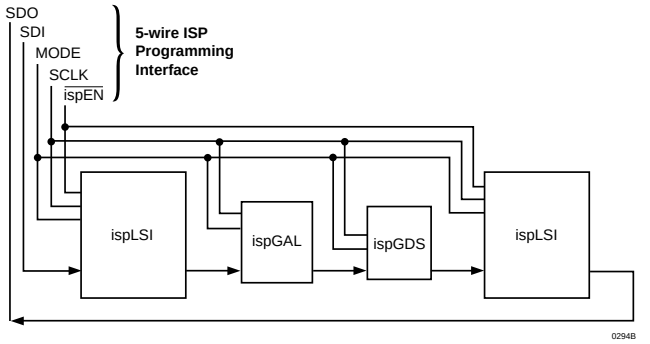
Perhaps the most exciting benefit of the ispLSI family is its potential to streamline the manufacturing process by eliminating the separate programming and labeling steps usually associated with PLDs. Quality is enhanced when product handling steps are reduced, in this case, those associated with programming, labeling and re-inventorying multiple device types. Eliminating socketing further improves quality and reduces board cost. Figure 6 shows the enhanced manufacturing with the ispLSI device.

Figure 6. Manufacturing Flow Comparison



All necessary programming is achieved via five TTL-level logic interface signals (see figure 7). These five signals control the on-chip programming circuitry, which protects against inadvertent reprogramming via on-chip state machines. The ispLSI family can also be programmed using popular third-party logic programmers.

Figure 7. In-System Programming Interface (Multi-Chip Solution)

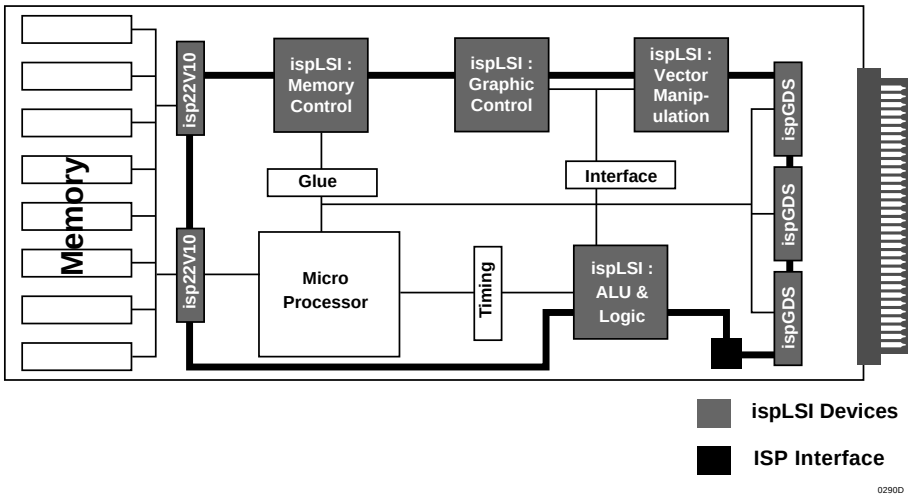


Boundary Scan

An emerging trend in board-level testing is boundary scan test, an attractive feature helping designers test system boards efficiently while lowering test and manufacturing costs. The ispLSI and pLSI 3000 and 6000 families offer dedicated IEEE 1149.1 boundary scan support for all test functions required by the standard. By using ispLSI and pLSI devices you not only eliminate expensive "bed-of-nails" testers but also simplify testing of surface-mount boards, multi-layer boards and boards using fine-pitch packages. Boundary scan is ideal wherever tight board layout limits access to logic signals.

It only takes four pins to implement the boundary scan interface. The ispLSI 3000 and 6000 devices share the four boundary scan signals with the in-system programming pins. This enhances the testability of system designs allowing logic to be reconfigured to improve controllability and observability.

Figure 5. In-System Programmable Graphics Board



Development Systems

The Lattice Semiconductor pLSI/ispLSI Development System (pDS) software is used to implement designs in ispLSI and pLSI devices. Design alternatives can be quickly implemented using LSC's low cost pDS software or the pDS+ family of Fitters that interface with third-party development software packages. This section describes the pDS and pDS+ Development Systems. Programmer support is also discussed.

pLSI/ispLSI Development System (pDS)

Features

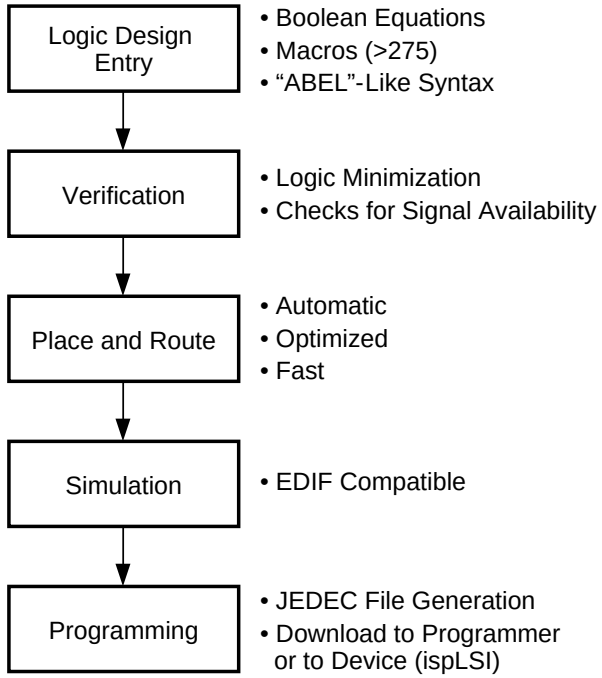
- ❑ High-performance, low-cost development environment
- ❑ Supports ispLSI and pLSI device families
- ❑ Boolean logic and text file design entry
- ❑ Windows-based graphical user interface
- ❑ Over 275 macros available
- ❑ Automatic place and route
- ❑ Static timing table
- ❑ Logic simulation with popular simulators
- ❑ JEDEC file download direct to programmer or ispLSI device

General Description

All ispLSI and pLSI families are supported by Lattice Semiconductor's low-cost pDS software. It runs on IBM-compatible (386/486/Pentium) PCs with Microsoft® Windows.

The graphical user interface employs an easy-to-use mouse and pull-down menu driven approach. Combined with Boolean logic data entry using an ABEL™-like syntax, pDS makes design entry with ispLSI and pLSI quick and straightforward (see figure 8).

Figure 8. pDS Design Flow



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The pDS software supports over 275 macros to assist the design process. These macros cover most TTL functions, from gate primitives to 16-bit counters. The software also supports user-definable macros which can be modifications of existing macros or custom creations.

The pDS software automatically verifies the design, performs logic minimization and checks for signal availability.

The LSC Place and Route software assigns pins and critical speed paths while routing the design.

Quick compilation speeds the design, debug and rework process dramatically. Incremental design techniques are also supported.

Timing and functional simulation is available from Lattice Semiconductor, using Viewsim simulation software.

The Windows graphical user interface makes programming easy, using pull-down menus, intuitive point-and-click commands and self explanatory instructions. Without any up-front training, designs can be completed within hours instead of days or weeks.

pLSI/ispLSI Development System Plus (pDS+)

Features

- ❑ Supports ispLSI and pLSI device families
- ❑ Schematic capture, state machine, design entry HDL, and Boolean equations
- ❑ Expanded macro library (>300)
- ❑ Automatic logic minimization and partitioning
- ❑ Automatic place and route
- ❑ Logic and timing simulation
- ❑ EDIF compatible
- ❑ JEDEC file download direct to programmer or ispLSI device

General Description

For higher level design entry environments, LSC offers pDS+ development software packages, which expand on the core capabilities of pDS. Schematic capture, state machine, HDL and Boolean entry are supported, along with an expanded macro library.

The pDS+ software utilizes industry standard third-party design environments such as Viewlogic's Pro Series, Data I/O's Synario and others.

Running on IBM compatible (486/Pentium) PCs or workstation platforms, pDS+ software supports automatic logic minimization and partitioning as well as place and route, resulting in high logic utilization.

For logic and timing simulation, support is available from Lattice through Viewlogic Viewsim and Data I/O Synario-Sim simulation tools.

Third Party Programming Support

The ispLSI and pLSI families are supported by popular third-party logic programmers including Data I/O, Logical Devices, BP-Microsystems, Stag, System General, SMS Micro Systems and Advin. Table 2 describes each vendor's specific programmer models that support the ispLSI and pLSI devices. No proprietary, expensive, high pin-count programmers are required.

High pin-count socket adapters are available from Emulation Technology, Procon Technology, EDI Corporation and Logical Systems Corporation.

Additionally, the ispLSI family can be programmed on the board (in-system), which eliminates the need for a stand-alone programmer. For specific details refer to the LSC Programming Tools Guide available from your local Sales Representative.

Table 2. Programming Support

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30/A
System General	TURPRO-1

isp Engineering Kit

The ispLSI family may also be programmed with Lattice Semiconductor's isp Engineering Kit Model 100 for PCs. The kit is designed for engineering purposes only and is not intended for production use. By connecting an eight-wire cable to the parallel printer port of a PC, JEDEC files can be easily downloaded into the ispLSI device. Additionally, this cable can be connected directly to the circuit board facilitating on-board in-system programming.

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