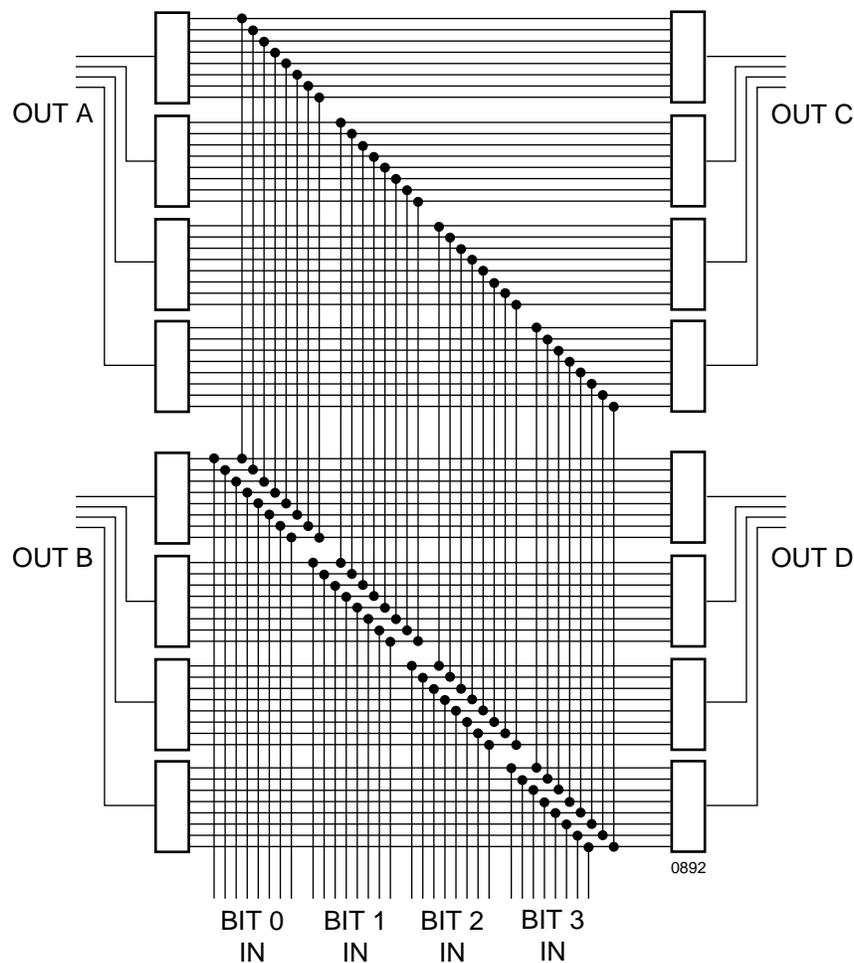


This application note describes a crosspoint switch that will allow any of four input busses to be connected to any or all of the four output busses. The input and output busses are eight bits wide. Wider busses can be accommodated by paralleling multiple ispLSI 1032 devices. By pairing the input and output busses, the design can be changed to a two-by-two-by-sixteen crosspoint switch.

The design provides for simplex data transfers but the addition of a second device will allow duplex operation with separate transmit and receive data paths. Figure 1 shows the basic switch architecture.

The actual implementation of the switch consists of 32 four-to-one multiplexers controlled in groups of eight. The input signal selection for each group of eight is controlled by a two-bit register. The data written into this register is provided by an external source on the SEL0 and SEL1 pins. The address of the register to which the SEL0 and SEL1 data is to be written is provided by an external source as an address on the SELA0 and SELA1 pins. The writing of the data to the register is controlled by a write signal on the WR pin. The data stored in the register is decoded to specify the source of the data appearing at the outputs of a group of eight multiplexers.

Figure 1. Switch Architecture



Crosspoint Switch Implementation Using the ispLSI 1032

A listing of the Lattice Design File (LDF) is shown on the following pages.

The signals brought in on the dedicated input pins needed to be provided to registers outside of the megablock in which the dedicated inputs were located. In order for the dedicated input signals to appear as a global signal in the global routing pool (GRP), they were routed through a generic logic block (GLB) with the output of the GLB appearing in the GRP. This implementation was used only on control paths where speed was not critical as on data paths.

The data paths all use the four product term bypass in the GLBs but do not bypass the output routing pool. The use of the four product term bypass does not affect routability in this design. The maximum propagation delay from the data input pins to the data output pins is 12ns when the ispLSI 1032-90 is used.

Design LDF Listing

```
// an_4.ldf generated using Lattice pDS
2.50
LDF 1.00.00 DESIGNLDF;
DESIGN XBAR_4X4X8;
REVISION 0;
PROJECTNAME Crossbar Application Note;

PART ispLSI1032-90J;

DECLARE

END; //DECLARE

SYM GLB D7 1 MD0D1;
SIGTYPE [D0,D1] OUT CRIT;
EQUATIONS
    D0 = AI0 & !DSEL1 & !DSEL0
        # BI0 & !DSEL1 & DSEL0
        # CI0 & DSEL1 & !DSEL0
        # DI0 & DSEL1 & DSEL0;
    D1 = AI1 & !DSEL1 & !DSEL0
        # BI1 & !DSEL1 & DSEL0
        # CI1 & DSEL1 & !DSEL0
        # DI1 & DSEL1 & DSEL0;

END
```

```
END;
SYM GLB B7 1 MB0B1;
SIGTYPE [B0,B1] OUT CRIT;
EQUATIONS
    B0 = AI0 & !BSEL1 & !BSEL0
        # BI0 & !BSEL1 & BSEL0
        # CI0 & BSEL1 & !BSEL0
        # DI0 & BSEL1 & BSEL0;
    B1 = AI1 & !BSEL1 & !BSEL0
        # BI1 & !BSEL1 & BSEL0
        # CI1 & BSEL1 & !BSEL0
        # DI1 & BSEL1 & BSEL0;
```

END

END;

```
SYM GLB C7 1 MC0C1;
SIGTYPE [C0,C1] OUT CRIT;
EQUATIONS
    C0 = AI0 & !CSEL1 & !CSEL0
        # BI0 & !CSEL1 & CSEL0
        # CI0 & CSEL1 & !CSEL0
        # DI0 & CSEL1 & CSEL0;
    C1 = AI1 & !CSEL1 & !CSEL0
        # BI1 & !CSEL1 & CSEL0
        # CI1 & CSEL1 & !CSEL0
        # DI1 & CSEL1 & CSEL0;
```

END

END;

```
SYM GLB A7 1 MA0A1;
SIGTYPE [A0,A1] OUT CRIT;
EQUATIONS
    A0 = AI0 & !ASEL1 & !ASEL0
        # BI0 & !ASEL1 & ASEL0
        # CI0 & ASEL1 & !ASEL0
        # DI0 & ASEL1 & ASEL0;
    A1 = AI1 & !ASEL1 & !ASEL0
        # BI1 & !ASEL1 & ASEL0
        # CI1 & ASEL1 & !ASEL0
        # DI1 & ASEL1 & ASEL0;
```

END

END;

Crosspoint Switch Implementation Using the ispLSI 1032

```
SYM GLB A6 1 MA2A3;
SIGTYPE [A2,A3] OUT CRIT;
EQUATIONS
    A2 = AI2 & !ASEL1 & !ASEL0
        # BI2 & !ASEL1 & ASEL0
        # CI2 & ASEL1 & !ASEL0
        # DI2 & ASEL1 & ASEL0;
    A3 = AI3 & !ASEL1 & !ASEL0
        # BI3 & !ASEL1 & ASEL0
        # CI3 & ASEL1 & !ASEL0
        # DI3 & ASEL1 & ASEL0;
```

END

END;

```
SYM GLB B6 1 MB2B3;
SIGTYPE [B2,B3] OUT CRIT;
EQUATIONS
    B2 = AI2 & !BSEL1 & !BSEL0
        # BI2 & !BSEL1 & BSEL0
        # CI2 & BSEL1 & !BSEL0
        # DI2 & BSEL1 & BSEL0;
    B3 = AI3 & !BSEL1 & !BSEL0
        # BI3 & !BSEL1 & BSEL0
        # CI3 & BSEL1 & !BSEL0
        # DI3 & BSEL1 & BSEL0;
```

END

END;

```
SYM GLB C6 1 MC2C3;
SIGTYPE [C2,C3] OUT CRIT;
EQUATIONS
    C2 = AI2 & !CSEL1 & !CSEL0
        # BI2 & !CSEL1 & CSEL0
        # CI2 & CSEL1 & !CSEL0
        # DI2 & CSEL1 & CSEL0;
    C3 = AI3 & !CSEL1 & !CSEL0
        # BI3 & !CSEL1 & CSEL0
        # CI3 & CSEL1 & !CSEL0
        # DI3 & CSEL1 & CSEL0;
```

END

END;

```
SYM GLB D6 1 MD2D3;
SIGTYPE [D2,D3] OUT CRIT;
EQUATIONS
    D2 = AI2 & !DSEL1 & !DSEL0
        # BI2 & !DSEL1 & DSEL0
        # CI2 & DSEL1 & !DSEL0
        # DI2 & DSEL1 & DSEL0;
    D3 = AI3 & !DSEL1 & !DSEL0
        # BI3 & !DSEL1 & DSEL0
        # CI3 & DSEL1 & !DSEL0
        # DI3 & DSEL1 & DSEL0;
```

END

END;

```
SYM GLB B0 1 GSEL;
SIGTYPE [SEL0,SEL1] OUT;
EQUATIONS
    SEL0 = ISEL0;
    SEL1 = ISEL1;
```

END

END;

```
SYM GLB A5 1 MA4A5;
SIGTYPE [A4,A5] OUT CRIT;
EQUATIONS
```

```
    A4 = AI4 & !ASEL1 & !ASEL0
        # BI4 & !ASEL1 & ASEL0
        # CI4 & ASEL1 & !ASEL0
        # DI4 & ASEL1 & ASEL0;
    A5 = AI5 & !ASEL1 & !ASEL0
        # BI5 & !ASEL1 & ASEL0
        # CI5 & ASEL1 & !ASEL0
        # DI5 & ASEL1 & ASEL0;
```

END

END;

```
SYM GLB A4 1 MA6A7;
SIGTYPE [A6,A7] OUT CRIT;
EQUATIONS
```

```
    A6 = AI6 & !ASEL1 & !ASEL0
        # BI6 & !ASEL1 & ASEL0
        # CI6 & ASEL1 & !ASEL0
        # DI6 & ASEL1 & ASEL0;
    A7 = AI7 & !ASEL1 & !ASEL0
        # BI7 & !ASEL1 & ASEL0
        # CI7 & ASEL1 & !ASEL0
        # DI7 & ASEL1 & ASEL0;
```

END

END;

Crosspoint Switch Implementation Using the ispLSI 1032

```
SYM GLB B5 1 MB4B5;
SIGTYPE [B4,B5] OUT CRIT;
EQUATIONS
    B4 = AI4 & !BSEL1 & !BSEL0
        # BI4 & !BSEL1 & BSEL0
        # CI4 & BSEL1 & !BSEL0
        # DI4 & BSEL1 & BSEL0;
    B5 = AI5 & !BSEL1 & !BSEL0
        # BI5 & !BSEL1 & BSEL0
        # CI5 & BSEL1 & !BSEL0
        # DI5 & BSEL1 & BSEL0;
```

END

END;

```
SYM GLB B4 1 MB6B7;
SIGTYPE [B6,B7] OUT CRIT;
EQUATIONS
    B6 = AI6 & !BSEL1 & !BSEL0
        # BI6 & !BSEL1 & BSEL0
        # CI6 & BSEL1 & !BSEL0
        # DI6 & BSEL1 & BSEL0;
    B7 = AI7 & !BSEL1 & !BSEL0
        # BI7 & !BSEL1 & BSEL0
        # CI7 & BSEL1 & !BSEL0
        # DI7 & BSEL1 & BSEL0;
```

END

END;

```
SYM GLB C5 1 MC4C5;
SIGTYPE [C4,C5] OUT CRIT;
EQUATIONS
    C4 = AI4 & !CSEL1 & !CSEL0
        # BI4 & !CSEL1 & CSEL0
        # CI4 & CSEL1 & !CSEL0
        # DI4 & CSEL1 & CSEL0;
    C5 = AI5 & !CSEL1 & !CSEL0
        # BI5 & !CSEL1 & CSEL0
        # CI5 & CSEL1 & !CSEL0
        # DI5 & CSEL1 & CSEL0;
```

END

END;

```
SYM GLB C4 1 MC6C7;
SIGTYPE [C6,C7] OUT CRIT;
EQUATIONS
    C6 = AI6 & !CSEL1 & !CSEL0
        # BI6 & !CSEL1 & CSEL0
        # CI6 & CSEL1 & !CSEL0
        # DI6 & CSEL1 & CSEL0;
    C7 = AI7 & !CSEL1 & !CSEL0
        # BI7 & !CSEL1 & CSEL0
        # CI7 & CSEL1 & !CSEL0
        # DI7 & CSEL1 & CSEL0;
```

END

END;

```
SYM GLB D5 1 MD4D5;
SIGTYPE [D4,D5] OUT CRIT;
EQUATIONS
    D4 = AI4 & !DSEL1 & !DSEL0
        # BI4 & !DSEL1 & DSEL0
        # CI4 & DSEL1 & !DSEL0
        # DI4 & DSEL1 & DSEL0;
    D5 = AI5 & !DSEL1 & !DSEL0
        # BI5 & !DSEL1 & DSEL0
        # CI5 & DSEL1 & !DSEL0
        # DI5 & DSEL1 & DSEL0;
```

END

END;

```
SYM GLB D4 1 MD6D7;
SIGTYPE [D6,D7] OUT CRIT;
EQUATIONS
    D6 = AI6 & !DSEL1 & !DSEL0
        # BI6 & !DSEL1 & DSEL0
        # CI6 & DSEL1 & !DSEL0
        # DI6 & DSEL1 & DSEL0;
    D7 = AI7 & !DSEL1 & !DSEL0
        # BI7 & !DSEL1 & DSEL0
        # CI7 & DSEL1 & !DSEL0
        # DI7 & DSEL1 & DSEL0;
```

END

END;

Crosspoint Switch Implementation Using the ispLSI 1032

```

SYM GLB  A3  1  CONA;
SIGTYPE [ASEL0,ASEL1] REG OUT;
EQUATIONS
    ASEL0.PTCLK = !WR & !SELA0 & !SELA1;
    ASEL0 = SEL0;
    ASEL1 = SEL1;
END
END;

SYM GLB  D0  1  GWR;
SIGTYPE WR OUT;
EQUATIONS WR = IWR;

END
END;

SYM GLB  B1  1  GSELA;
SIGTYPE [SELA0,SELA1] OUT;
EQUATIONS
    SELA0 = ISELA0;
    SELA1 = ISELA1;
END
END;

SYM GLB  B3  1  CONB;
SIGTYPE [BSEL0,BSEL1] REG OUT;
EQUATIONS
    BSEL0.PTCLK = !WR & SELA0 & !SELA1;
    BSEL0 = SEL0;
    BSEL1 = SEL1;
END
END;

SYM GLB  C3  1  CONC;
SIGTYPE [CSEL0,CSEL1] REG OUT;
EQUATIONS
    CSEL0.PTCLK = !WR & !SELA0 & SELA1;
    CSEL0 = SEL0;
    CSEL1 = SEL1;
END
END;

SYM GLB  D3  1  COND;
SIGTYPE [DSEL0,DSEL1] REG OUT;
EQUATIONS
    DSEL0.PTCLK = !WR & SELA0 & SELA1;
    DSEL0 = SEL0; DSEL1 = SEL1;
END
END;

SYM IOC  IO15  1  OA0;
OB11 (XA0,A
END;

SYM IOC  IO14  1  OA1;
OB11 (XA1,A1);
END;

SYM IOC  IO13  1  OA2;
OB11 (XA2,A2);
END;

SYM IOC  IO12  1  OA3;
OB11 (XA3,A3);
END;

SYM IOC  IO31  1  OB0;
OB11 (XB0,B0);
END;

SYM IOC  IO30  1  OB1;
OB11 (XB1,B1);
END;

SYM IOC  IO29  1  OB2;
OB11 (XB2,B2);
END;

SYM IOC  IO28  1  OB3;
OB11 (XB3,B3);
END;

SYM IOC  IO47  1  OC0;
OB11 (XC0,C0);
END;

SYM IOC  IO46  1  OC1;
OB11 (XC1,C1);
END;

SYM IOC  IO45  1  OC2;
OB11 (XC2,C2);
END;

SYM IOC  IO44  1  OC3;
OB11 (XC3,C3);
END;

SYM IOC  IO63  1  OD0;
OB11 (XD0,D0);
END;

```

Crosspoint Switch Implementation Using the ispLSI 1032

SYM IOC IO62 1 OD1;
OB11 (XD1,D1);
END;

SYM IOC IO61 1 OD2;
OB11 (XD2,D2);
END;

SYM IOC IO60 1 OD3;
OB11 (XD3,D3);
END;

SYM IOC IO11 1 IA0;
IB11 (AI0,XAI0);
END;

SYM IOC IO10 1 IA1;
IB11 (AI1,XAI1);
END;

SYM IOC IO9 1 IA2;
IB11 (AI2,XAI2);
END;

SYM IOC IO8 1 IA3;
IB11 (AI3,XAI3);
END;

SYM IOC IO24 1 IB3;
IB11 (BI3,XBI3);
END;

SYM IOC IO25 1 IB2;
IB11 (BI2,XBI2);
END;

SYM IOC IO26 1 IB1;
IB11 (BI1,XBI1);
END;

SYM IOC IO27 1 IB0;
IB11 (BI0,XBI0);
END;

SYM IOC IO43 1 IC0;
IB11 (CI0,XCI0);
END;

SYM IOC IO42 1 IC1;
IB11 (CI1,XCI1);
END;

SYM IOC IO41 1 IC2;
IB11 (CI2,XCI2);
END;

SYM IOC IO40 1 IC3;
IB11 (CI3,XCI3);
END;

SYM IOC IO56 1 ID3;
IB11 (DI3,XDI3);
END;

SYM IOC IO57 1 ID2;
IB11 (DI2,XDI2);
END;

SYM IOC IO58 1 ID1;
IB11 (DI1,XDI1);
END;

SYM IOC IO59 1 ID0;
IB11 (DI0,XDI0);
END;

SYM IOC IO0 1 IA7;
IB11 (AI7,XAI7);
END;

SYM IOC IO1 1 IA6;
IB11 (AI6,XAI6);
END;

SYM IOC IO2 1 IA5;
IB11 (AI5,XAI5);
END;

SYM IOC IO3 1 IA4;
IB11 (AI4,XAI4);
END;

SYM IOC IO4 1 OA7;
OB11 (XA7,A7);
END;

SYM IOC IO5 1 OA6;
OB11 (XA6,A6);
END;

SYM IOC IO6 1 OA5;
OB11 (XA5,A5);
END;

SYM IOC IO7 1 OA4;
OB11 (XA4,A4);
END;

SYM IOC IO16 1 IB7;
IB11 (BI7,XBI7);
END;

Crosspoint Switch Implementation Using the ispLSI 1032

```
SYM IOC IO17 1 IB6;
IB11 (BI6,XBI6);
END;

SYM IOC IO18 1 IB5;
IB11 (BI5,XBI5);
END;

SYM IOC IO19 1 IB4;
IB11 (BI4,XBI4);
END;

SYM IOC IO20 1 OB7;
OB11 (XB7,B7);
END;

SYM IOC IO21 1 OB6;
OB11 (XB6,B6);
END;

SYM IOC IO22 1 OB5;
OB11 (XB5,B5);
END;

SYM IOC IO23 1 OB4;
OB11 (XB4,B4);
END;

SYM IOC IO32 1 IC7;
IB11 (CI7,XCI7);
END;

SYM IOC IO33 1 IC6;
IB11 (CI6,XCI6);
END;

SYM IOC IO34 1 IC5;
IB11 (CI5,XCI5);
END;

SYM IOC IO35 1 IC4;
IB11 (CI4,XCI4);
END;

SYM IOC IO36 1 OC7;
OB11 (XC7,C7);
END;

SYM IOC IO37 1 OC6;
OB11 (XC6,C6);
END;

SYM IOC IO38 1 OC5;
OB11 (XC5,C5);
END;

SYM IOC IO39 1 OC4;
OB11 (XC4,C4);
END;

SYM IOC IO48 1 ID7;
IB11 (DI7,XDI7);
END;

SYM IOC IO49 1 ID6;
IB11 (DI6,XDI6);
END;

SYM IOC IO50 1 ID5;
IB11 (DI5,XDI5);
END;

SYM IOC IO51 1 ID4;
IB11 (DI4,XDI4);
END;

SYM IOC IO52 1 OD7;
OB11 (XD7,D7);
END;

SYM IOC IO53 1 OD6;
OB11 (XD6,D6);
END;

SYM IOC IO54 1 OD5;
OB11 (XD5,D5);
END;

SYM IOC IO55 1 OD4;
OB11 (XD4,D4);
END;

SYM IOC IO 1 IS0;
IB11 (ISEL0,XSEL0);
END;

SYM IOC IO1 1 IS1;
IB11 (ISEL1,XSEL1);
END;

SYM IOC IO2 1 ISA0;
IB11 (ISELA0,XSELA0);
END;

SYM IOC IO3 1 ISA1;
IB11 (ISELA1,XSELA1);
END;

SYM IOC IO4 1 IWR;
IB11 (IWR,XWR);
END; END; //LDF DESIGNLDF
```



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