pDS+™ Cadence Software

Features

- **ispLSI® AND pLSI® DEVELOPMENT SYSTEM**
  - **— Supports ispLSI and pLSI 1000/E and 2000**
  - **— Upgrade to Support ispLSI and pLSI 3000**
- **DESIGN ENTRY USING CADENCE CONCEPT™**
  - **— Schematic-Entry**
  - **— Verilog-HDL and VHDL Entry Using Synergy Synthesis Tool**
  - **— Over 300 "TTL-Like" Macros**
  - **— Design Verification Using Verilog Functional and Timing Simulation**
  - **— Command Line Driven User Interface**
- **LATTICE SEMICONDUCTOR pDS+ CADENCE FITTER**
  - **— Automatic Device Fitter Ensures High Utilization and Performance**
  - **— Efficient Design Optimization & Minimization**
  - **— Automatic Partitioning with High Utilization**
  - **— Extended Route Option for Maximizing Device Performance or Resources**
  - **— Predictable Performance**
- **COMPLETE DESIGN VERIFICATION**
  - **— Verilog-XL™ Logic Simulation**
  - **— Verilog Netlist Used for Functional Simulation**
  - **— Input Files (.vlo and .sdf) for Verilog TIming Simulator Created by Fitter**
- **INDUSTRY STANDARD PROGRAMMING FILE GENERATION**
  - **— Standard JEDEC Device Fuse Map**
- **IN-SYSTEM PROGRAMMING SUPPORT**
  - **— ispCODE™ C Source Routines Included**
  - **— ISP Daisy Chain Download (PC)**
  - **— ispATE™ Board Test Programming Utility**
- **PLATFORMS SUPPORTED**
  - **— SUN O/S 4.1.3 and Above**

Introduction

The pDS+ Cadence software from Lattice Semiconductor Corporation (LSC) offers a powerful solution to fit high density logic designs into Lattice Semiconductor's ispLSI and pLSI devices.

Design entry is made simple by using Concept software and or Synergy Synthesis from Cadence together with the pDS+ Cadence Fitter for design implementation. The Cadence software offers high-level, device independent design entry with efficient logic compilation, delivering unprecedented performance for the most complex designs.

Cadence Concept

The Cadence Concept schematic entry software allows the user to create designs without regard to any specific device dependencies. Cadence Concept offers features such as automatic symbol generation, cut and paste, unlimited pan and zoom, as well as many other features to help the user reach design verification quickly and easily. The menu-driven environment provides a simplified method of design entry, making use of multi-window operation for schematic, simulator and waveform windows to be opened concurrently. Verilog-HDL and VHDL high level language designs can be synthesized using Cadence's Synergy Synthesis tools. These powerful languages speed the design of both simple and complex logic functions. The design environment also includes the Verilog-XL logic simulator, which allows designs to be fully tested before device programming. Results can also be dynamically back annotated to the schematic window for design verification.

pDS+ Cadence Fitter

The pDS+ Cadence Fitter for ispLSI and pLSI devices is executed as a stand alone program, using the EDIF output from Concept or Synergy as input. The Fitter provides hands-off design implementation through intelligent design optimization, logic partitioning, automatic place & route and fusemap generation in standard JEDEC format. Timing simulation input files for Verilog are generated by the Fitter when needed by the user. The pDS+ Cadence software comes complete with a library of over 300 TTL-like macros to simplify design entry. Extensive top level design control is provided to optimize design implementation for speed and/or high device resource utilization.

Design Optimization and Logic Minimization

The pDS+ Cadence Fitter uses proprietary algorithms targeted for device specific features. The Fitter optimizes the design thoroughly, utilizing logic minimization, product term sharing and XOR functions wherever necessary. In addition, the pDS+ Cadence Fitter supports multiple fitting strategies to obtain the best device utilization and performance.

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Figure 1. pDS+ Cadence Design Interface

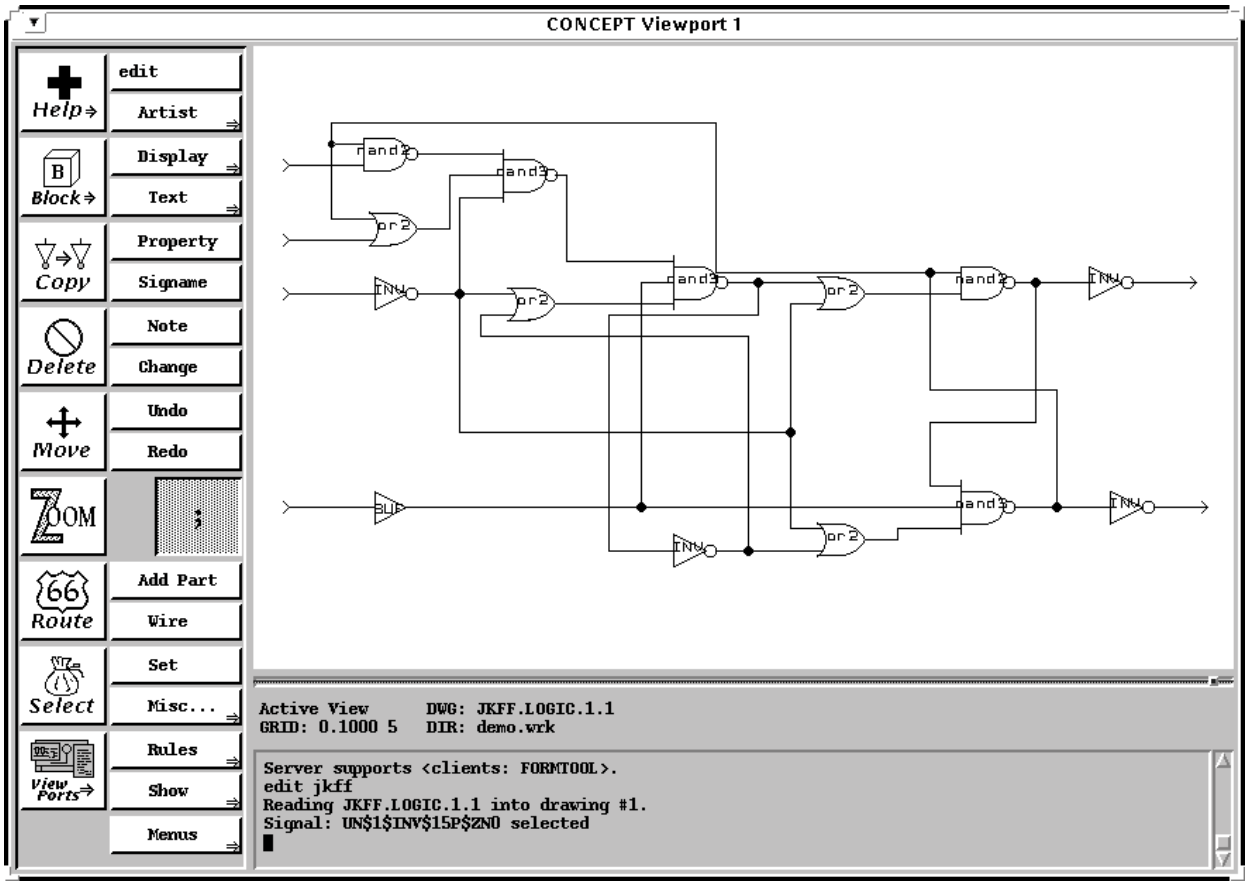
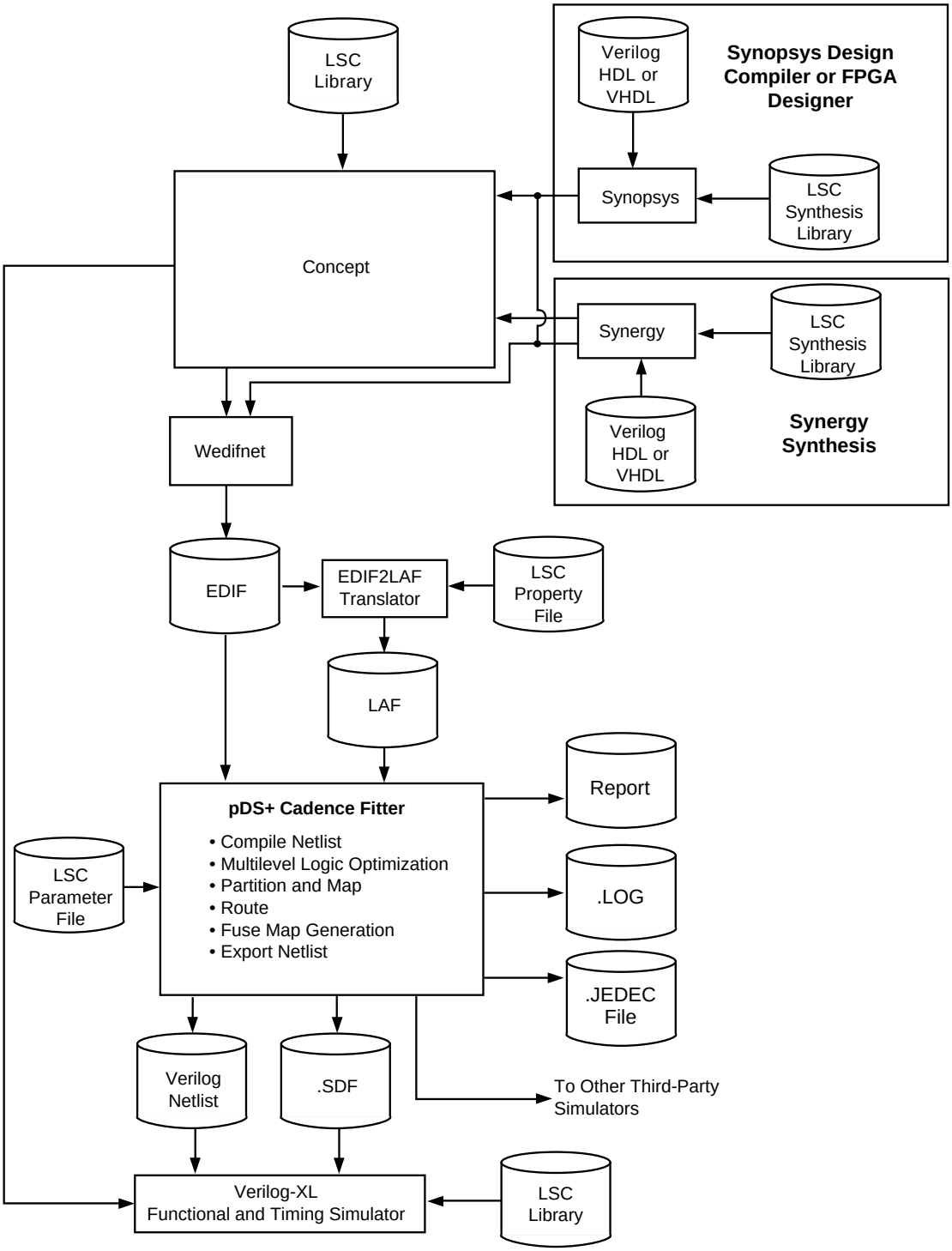


Figure 2. pDS+ Cadence Design Process



Automatic Partitioning

The pDS+ Cadence Fitter incorporates a powerful Automatic Partitioner for hands-free synthesis of a design into Generic Logic Blocks (GLBs). The partitioner takes full advantage of the device's powerful features, such as the hard XOR function and product term sharing. The internal XOR can be utilized for Arithmetic functions, T-Type flip-flops, and on & off set optimization functions. Common sub-expressions are extracted, and unused registers are eliminated. These features combine to maximize device resource utilization and increase design performance.

Automatic Place and Route

Automatic place and route eliminates the need for manual editing and accelerates the design cycle. The Router automatically generates pinouts based on the optimal design implementation or user assigned pinouts.

The Extended Route option performs a comprehensive route to maximize device resource utilization and ensure efficient design implementation. The result is that small design changes won't cause expensive PC board rework.

Design Parameter Control

Extensive design parameter control at the design entry level is possible with the pDS+ Cadence Fitter giving the user the option to optimize the design for maximum utilization and speed. Controls are specified using “property” statements in the property file or parameter file. The parameter file and property files contain:

- — Fitter Control Options
- — Design Implementation Controls
  - — Net Attributes
  - — Pin Attributes
  - — Path Attributes
  - — Symbol Attributes

Fitter Control Options

Special properties can be passed to the pDS+ Cadence Fitter providing complete control over critical design considerations. Fitter control over design partitioning and routing optimizes the design for speed and/or device utilization. Here are a few of the powerful features:

Feature	Description
PART	Determines device type to be used.
PARAM_FILE	Allows user to specify attributes in a text file.
STRATEGY	Choice of AREA (default), DELAY or NO_OPTIMIZE. AREA optimizes device space, DELAY keeps GLB levels to a minimum and NO_OPTIMIZE does not reduce equations.
USE_GLOBAL_RESET	Causes global reset to use dedicated routing for reset.
MAX_GLB_OUT	Specifies maximum number of outputs from a GLB. Default is 4.
MAX_GLB_IN	Controls maximum number of inputs to a GLB. Default is 16 for 1K and 2K devices and 24 for 3K devices.
EFFORT	Controls optimization of partitioner.
EXTENDED_ROUTE	Choice of OFF (fixed) or ON (extended, default).
PIN_FILE	Specifies locked pin assignments.

Design Implementation Controls

Device controls are used for changing design parameters such as security. Some of these implementation controls are:

Feature	Description
ISP	Instructs Router to reserve in-system programming pins.
ISP_EXCEPT_Y2	Reserves all ISP pins except Y2 (ispLSI and pLSI 1016/E and 2032 only).
Y1_AS_RESET	Uses Y1 clock pin on ispLSI and pLSI 1016/E and 2032 as a global reset pin.
SECURITY	Sets the device security cell to prevent unauthorized fuse map read back.

Net Attributes

These properties control how the design is mapped into the specified features of the target device:

Feature	Description
CLK0-CLK2	Assigns a CLK signal to a dedicated CLK line.
IOCLK0-IOCLK1	Assigns a CLK signal to a dedicated IOCLK line if single fanout input pin.
FASTCLK	Fitter assigns CLK signal to CLK0-CLK2 or IOCLK0-IOCLK1.
SLOWCLK	Assigns the CLK signal to a GLB product term CLK.
PRESERVE	Prevents logic minimization on specified nets.
GROUP	Suggests grouping of functions in a GLB.

Pin Attributes

Feature	Description
CRIT	Specifies Output Routing Pool Bypass to minimize delay.
SLOWSLEW	Assigns slow slew rate on a specific I/O cell.
LOCK	Assigns device I/O pins to design I/O ports.
PULLUP	Specifies internal pull-up resistors.

Path Attributes

The following properties specify paths in the design that have special fitting requirements:

Feature	Description
SAP/EAP	Defines asynchronous paths to prevent signal duplication.
SCP/ECP	Defines critical paths to reduce delays.
SNP/ENP	Defines logic paths for no logic minimization.

Symbol Attributes

Feature	Description
REGTYPE	Determines where a register is to be placed (IOC or GLB).
PROTECT	Prevents removal of a primitive or a macro during minimization.
OPTIMIZE	Selects either hard or soft macros.

Parameter File

The pDS+ Cadence Fitter uses a parameter file (.PAR file) feature to help designers optimize the design for the right device. It allows the user to try a number of design implementation options using the design implementation controls in batch mode. The parameter file instructs the partitioner and the router on how to maximize both device utilization and performance.

The pDS+ Cadence Fitter also provides post route equations showing exactly how the design is implemented in the selected device.

Design Verification

The pDS+ Cadence software provides functional and full timing simulation of ispLSI and pLSI designs using Verilog-XL Logic Simulation. Functional simulation is performed before fitting the design with a netlist is created using the Cadence Concept Verilog Netlister (vloglink). Lattice Semiconductor provides Verilog-compatible libraries to perform simulation. For timing simulation, the pDS+ Cadence Fitter generates a Verilog netlist (.vlo file) and Standard Delay Format (.sdf file) file for input to Verilog-XL, which is invoked from the command line. The test fixture file (.cmd) is used as stimulus for simulation.

Fuse Map Generation

The pDS+ Cadence Fitter generates a device fusemap in standard JEDEC format. The fusemap is automatically produced and inserted in the JEDEC file after a successful route. A security feature gives protection of proprietary designs from unauthorized duplication.

System Requirements

Sun Sparc 4 and above

- — Sun OS Version 4.x
- — Open Windows 3.0
- — 16 MB RAM with 30 MB Hard Disk space
- — 3 Button Mouse

Programmer Support

All devices in the ispLSI device family can be programmed while installed on the target circuit board. In-system programming can be performed using an ispDOWNLOAD™ Cable and PC, by an on-board microprocessor or by ATE systems during final board test.

All ispLSI and pLSI devices can be programmed using third-party PLD programmers. These devices are currently supported by programmers from the following vendors:

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30A/B
System General	TURPRO-1/FX

High pin-count socket adapters are available from Emulation Technology, EDI Corporation and PROCON.

Product Ordering Information

Product Code	Description
pDS2160-SN1	Fitter for Cadence Concept/ Verilog-XL, includes Libraries
pDS1160-SN1	Cadence Concept Schematic and Verilog Simulation Libraries and Interface
pDS1165-SN1	Cadence Synergy Synthesis Libraries
pDS2160-3UP/SN1	3000 Family Upgrade

Annual Maintenance*

pDS2160M-SN1	Maintenance for pDS2160-SN1
pDS1160M-SN1	Maintenance for pDS1160-SN1
pDS1165M-SN1	Maintainance for pDS1165-SN1

*One year of maintenance is provided with every product purchase.

Warranty/Update Service

- 90-day warranty on disk media
- One-year maintenance support included with purchase
- Annual maintenance agreement available

Technical Support Assistance

Hotline: 1-800-LATTICE (Domestic)
1-408-428-6414 (International)
BBS: 1-408-428-6417
FAX: 1-408-944-8450
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