High-Density PLD Solutions For High-Speed RISC/CISC Systems

Introduction

As the next generation Pentium™, PowerPC™ and Alpha™ processors reach new heights in speed, designers face increasingly difficult system design problems when trying to realize each processor's full speed capability. ASIC solutions are a viable option in terms of speed, but the decision to go with such a solution is influenced by another important variable — time-to-market.

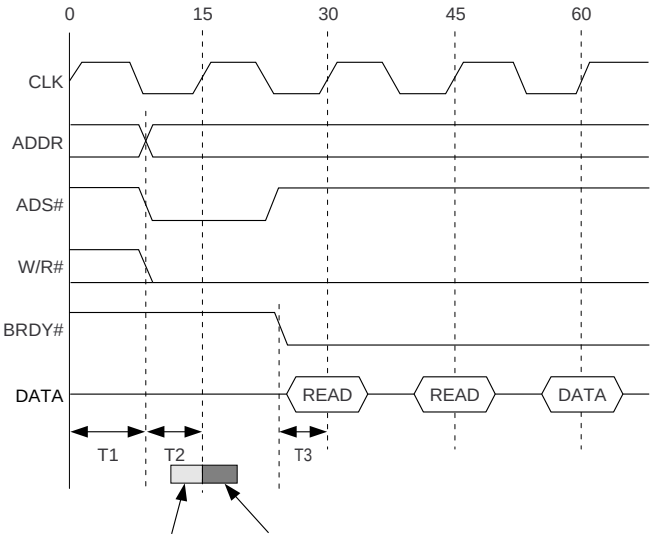
Winners of the race to introduce a new product stand to reap the lion's share of profits from the product's life-cycle. Although ASICs are capable of keeping pace with the new generation of processors, they are often losers in the race for time-to-market. Low-density PLDs are a popular choice because of their speed and ease of programming. Another option now exists which provides the benefits of low-density PLDs while supplying higher densities and more I/Os. Lattice Semiconductor offers two new families of high-speed programmable logic devices, the ispLSI and pLSI 2000 and 3000 families, to address these speed and time-to-market issues. Both families, as well as the ispLSI and pLSI 1000 family, are available as in-system reprogrammable devices, eliminating the need for sockets that often result in unreliable operation due to bent leads.

A Case For Speed

A rule of thumb for designers is that microprocessor systems typically require external logic to operate at twice the speed of the processor clock. It stands to reason that if the external logic was to consume the entire clock cycle for some computation, there would be no remaining time to satisfy any system setup requirements. This rule implies that Pentium, with its 15ns clock cycle, requires logic devices which have a speed rating of 7.5ns. If analyzed in more detail, Pentium, which has a maximum clock-edge to control-signal-valid delay of 8ns[1] (figure 1), retains 7ns of its clock cycle for external logic to perform a computation and satisfy setup requirements if a registered action is expected on the next clock edge. Logic devices with a 7.5ns Tpd rating typically have set-up times in the 4ns range. Thus, such devices can realistically conform to Pentium's bus specifications. Another constraint is that external logic is to provide valid output signals in time to meet Pentium's setup requirement of 5ns. This implies that logic devices must have a clock-to-out time of no more than 10ns. As seen in figure 1, 7.5ns logic devices have a clock-to-out time of 4ns to 5ns which easily satisfies Pentium's setup requirements. While 7.5ns speeds are attainable from fast low-density PLDs, the requirements of today's wide buses make it desirable to have higher levels of integration with more I/O. Address decoders and bus logic are examples of circuits which demand such speed, density and I/O.

Lattice's ispLSI and pLSI 2000 family specifically targets these applications. This family has devices which are able to integrate up to 10 traditional PLDs into a single package while supplying up to 102 I/Os. These devices, while being much higher density than PLDs, suffer no speed penalty. With propagation delays of 7.5ns and clock rates of 135 MHz, the ispLSI and pLSI 2000 family operates comfortably in systems which were once the sole domain of ASICs and the fastest low density PLDs. The set-up times of the 2000 family devices are within the 7ns requirement of the Pentium bus thus allowing the generation of registered control signals such as Bus Ready (BRDY#) (Figure 1).

Figure 1. Pentium Burst Read-Cycle With Relative Timings



Setup & Clock-to-Out for Lattice ispLSI/pLSI 2032

T1 = 8ns = Max time for Pentium™ signals valid.
T2 = 7ns = Time remaining for external logic setup to next clock edge.
T3 = 5ns = Bus Ready (BRDY#) min setup time.

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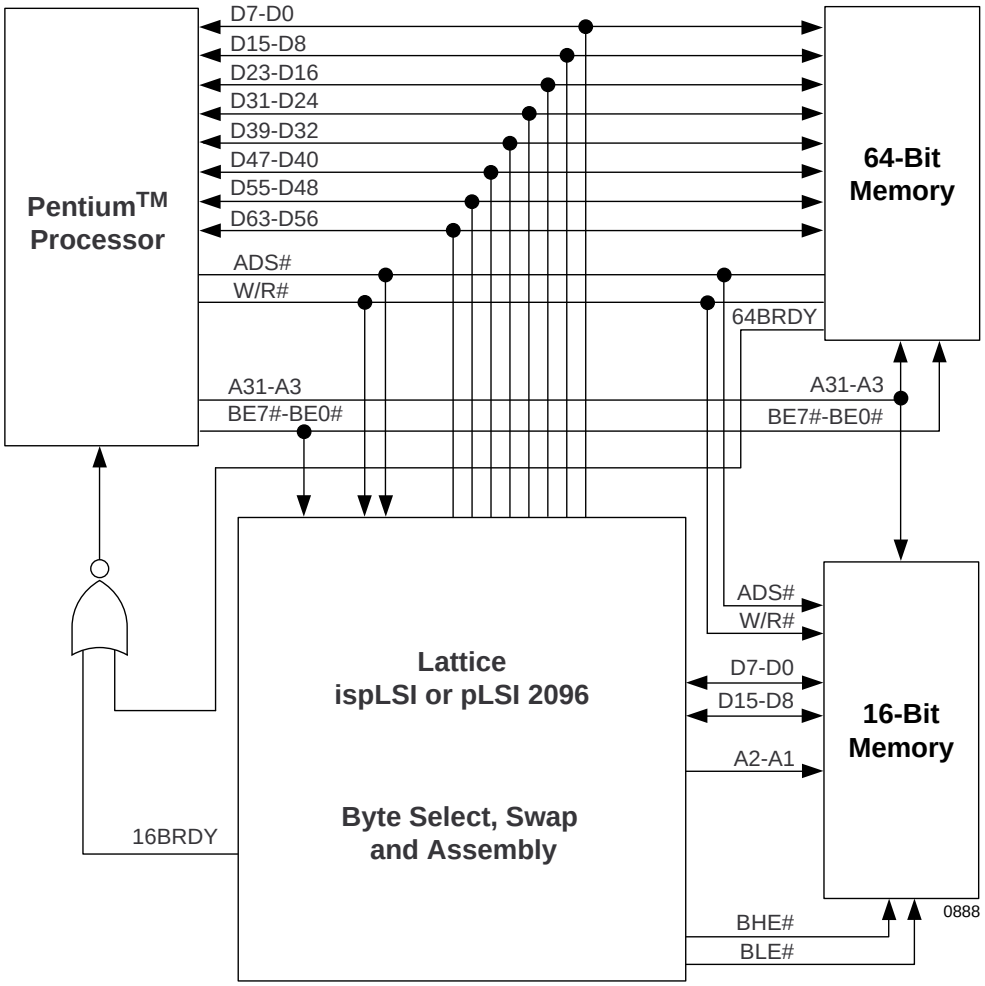
Address decoders are circuits which usually sit directly in the critical path of memory accesses. For this reason, Tpd is all important. For example, if we were to use Pentium with its 8ns Address-Valid time, a 7.5ns logic device for the address decoder, and a RAM with a 10ns Chip-Enable to Data-Out time, we would generate valid read data 25.5ns after the start of the read cycle. Pentium requires that read data be valid no later than 26.2ns (assuming no wait states). With a 7.5ns logic device, we have met Pentium's requirements with 0.7ns to spare. The ispLSI and pLSI 2032 and 2064 are designed to economically implement circuits such as this. These devices provide 32 and 64 macrocells respectively with 34 and 68 signal pins.

A Design Example

An example of a design which requires both high speed and a high degree of integration is a circuit to interface a 16-bit wide memory into a Pentium system with its 64-bit wide data bus. This 16-bit memory might possibly be a memory-mapped I/O device or a specialized RAM sub-system. The Lattice ispLSI and pLSI 2096 can be effectively used to integrate this 16-bit memory system into the Pentium's 64-bit environment while meeting all speed requirements. Figure 2 shows a block diagram of how this high-density PLD can be used to integrate the logic functions required for such an interface.

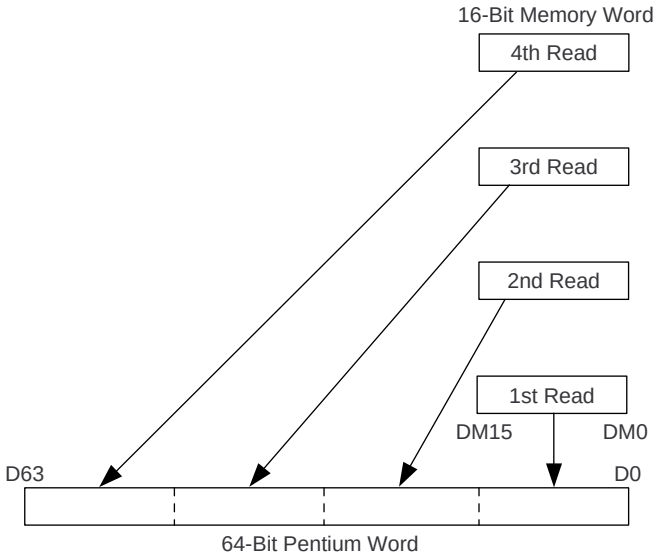
Figure 2. Interfacing A 16-bit Memory Sub-System To Pentium™



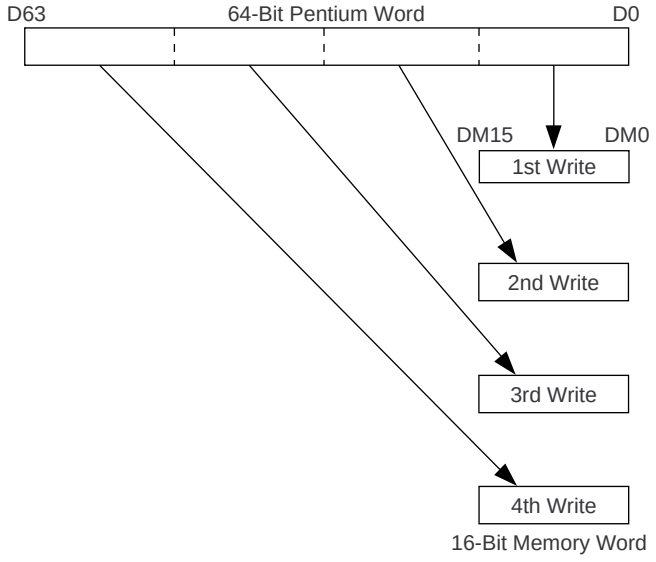
Intel specifies that to perform a read from a 16-bit memory, external logic is required to assemble four consecutive 16-bit reads into one 64-bit word. Writes require that the 64-bit word be broken into four 16 bit words which are consecutively written. These read and write operations are depicted in figure 3. In addition, the Pentium decodes the three least-significant address bits into eight unary byte-select signals. These byte select signals must be re-encoded into the binary A2-A1 address bits.

Figure 3. Read And Write Operations

Read Operation



Write Operation



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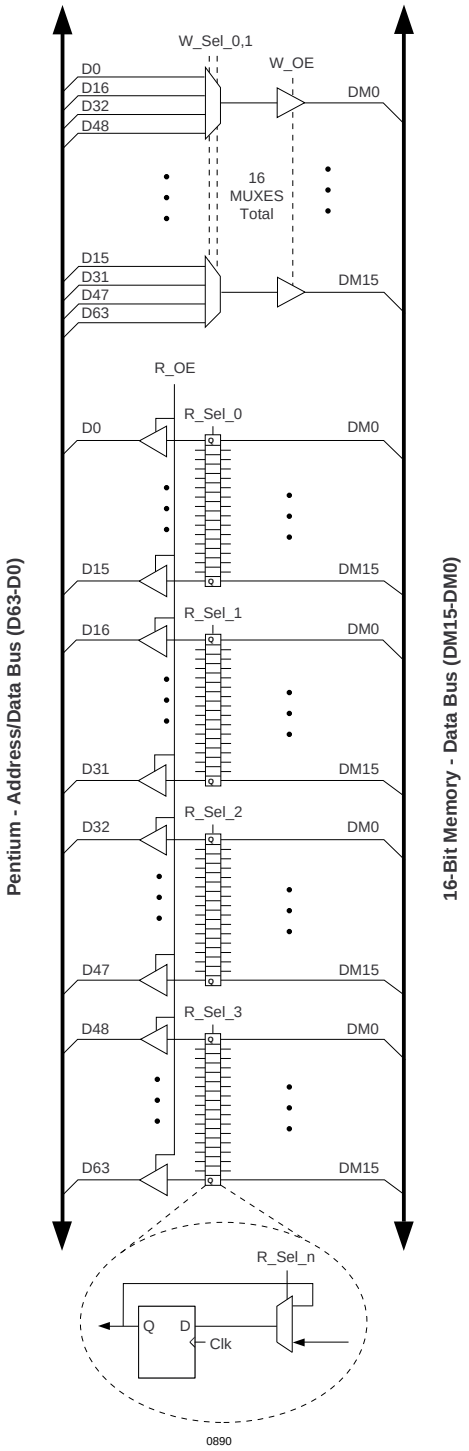
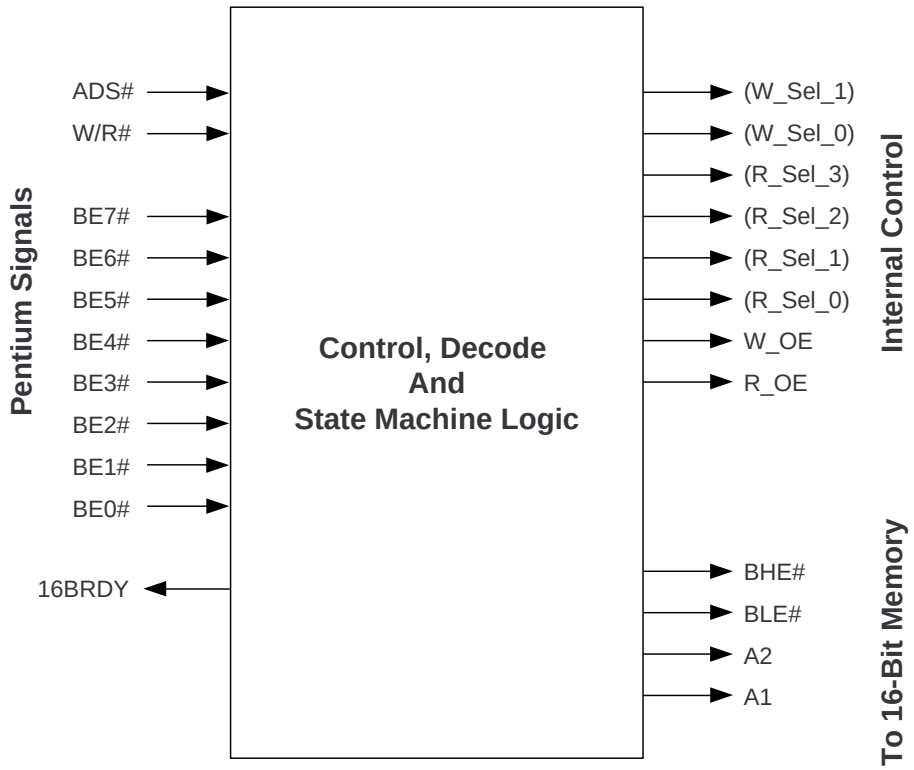
Within the 2096, the 16-bit write data path is created by the use of sixteen 4-to-1 multiplexers which select one of four Pentium byte pair bits. These multiplexer outputs form a 16-bit word which is written into the 16-bit memory. This circuit is shown in the upper portion of figure 4. Four such writes occur for every one 64-bit Pentium word. The 64-bit read data path is implemented with four sequential reads of the 16-bit memory into a 64 bit wide register. The read path is shown in the lower portion of figure 4.

Figure 4. Memory Interface Data Path



Control of the read and write operations is accomplished with a portion of the 2096 dedicated to control, decode and state machine functions. This control unit is shown as a block diagram in figure 5. The state machine conceptually generates the W_Sel_n and R_Sel_n control signals. These signals in actuality do not exist. Instead they are locally decoded from state bits in the 4 to 1 MUXes and in the read register. This is done to eliminate an additional pass through the HDPLD logic and thereby improves speed. The 16BRDY signal is generated by the state machine and signals that the Pentium can advance to the next transaction.

Figure 5. Memory Interface Control Logic



Note: Signals in parenthesis are shown for logical clarity.
In practice these signals are encoded as state-bits.

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For full 64-bit Pentium reads and writes, the BHE# and BLE# signals are always active. A2 and A1 are sequentially incremented to provide the read and write operations as shown in figure 3. For aligned 32-bit and 16-bit reads and writes, BHE# and BLE# also remain active and the BEn bits are decoded to generate appropriate A2 and A1 bits. The sequence of address counts is reduced to 2 counts for 32-bit operations and no counts for 16-bit operations. 8-bit operations require similar decoding but only the appropriate BHE# or BLE# signal is activated.

All these circuits can be efficiently and simply implemented in a single Lattice ispLSI and pLSI 2096 device. This interface requires 95 signal pins for which the 2096 provides 102 inputs and I/Os. 96 macrocells are available of which approximately 90 are required for this design.

For Higher Density Functions

Although the ispLSI and pLSI 2000 family addresses many of the needs in today's microprocessor systems, more complex subsystems may require a greater amount of logic than is available in the ispLSI and pLSI 2000 family. Such subsystems might include graphics functions, multiprocessor support, bus adapters, etc. For example, Intel does not at the time of this writing supply a Memory Bus Controller (MBC) for Pentium systems. Lattice has introduced the 3000 family of devices to specifically address such high density applications. This family, with clock rates of 110 MHz, pushes high density PLDs to new heights in terms of density, offering up to 14,000 gate equivalents. This new level of density offers microprocessor systems designers the ability to design gate-array class subsystems with the ease and time to market advantages of programmable logic devices. In addition, this family with its in-system reprogrammability and dedicated IEEE 1149.1 boundary scan test capability, is able to greatly enhance system test capabilities, thus improving system quality.

1. *"Bus Functional Description"*, Pentium™ Processor User's Manual, Volume One, Intel Literature Number 241428, 1993.

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