GAL22LV10Z
GAL22LV10ZD

Low Voltage, Zero Power E²CMOS PLD

FEATURES

- **3.3V LOW VOLTAGE, ZERO POWER OPERATION**
  - **— Interfaces with Standard 5V TTL Devices**
  - **— 50μA Typical Standby Current (100μA Max.)**
  - **— 40mA Typical Active Current (55mA Max.)**
  - **— Input Transition Detection on GAL22LV10Z**
  - **— Dedicated Power-down Pin on GAL22LV10ZD**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 15 ns Maximum Propagation Delay**
  - **— Fmax = 71.4MHz**
  - **— UltraMOS® Advanced CMOS Technology**
- **COMPATIBLE WITH STANDARD 22V10 DEVICES**
  - **— Fully Function/Fuse-Map/Parametric Compatible with Bipolar and CMOS 22V10 Devices**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **TEN OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
- **PRELOAD AND POWER-ON RESET OF REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— Battery Powered Systems**
  - **— DMA Control**
  - **— State Machine Control**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

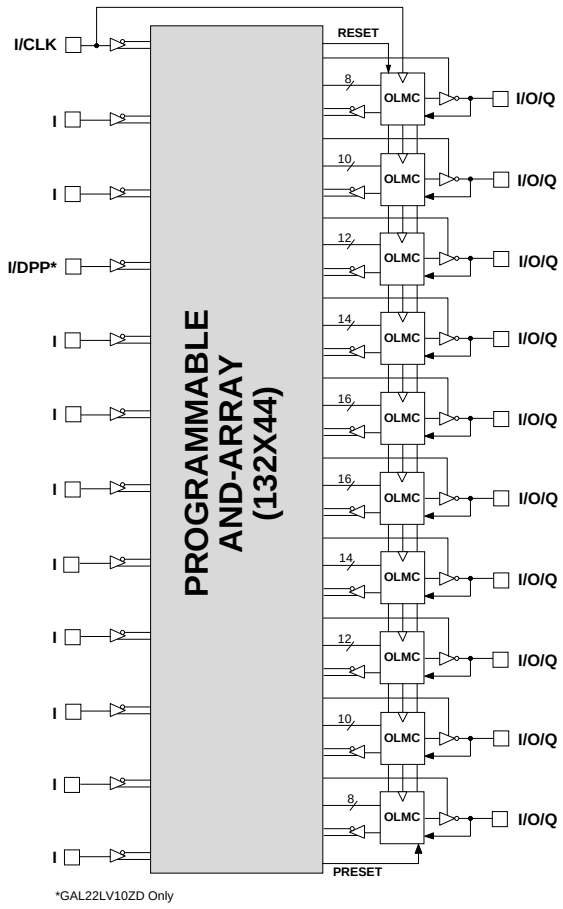
DESCRIPTION

The GAL22LV10Z and GAL22LV10ZD, at 15ns maximum propagation delay time and 100μA standby current, combine 3.3V CMOS process technology with Electrically Erasable (E²) floating gate technology to provide the best PLD solution to support today's new 3.3V systems. E² technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

The generic 22V10 architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL22LV10Z uses Input Transition Detection (ITD) to put the device into standby mode and is fully function/fuse map/parametric compatible with standard bipolar and CMOS 22V10 devices. The GAL22LV10ZD utilizes a Dedicated Power-down Pin (DPP) to put the device into standby mode.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor is able to guarantee 100% field programmability and functionality of all GAL® products. In addition,100 erase/rewrite cycles and data retention in excess of 20 years are guaranteed.

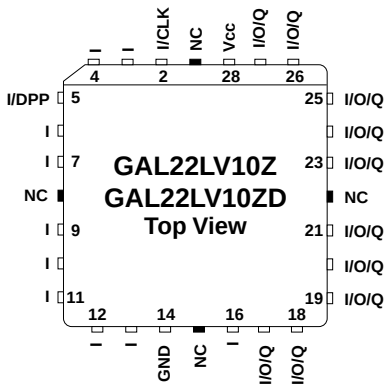
FUNCTIONAL BLOCK DIAGRAM



*GAL22LV10ZD Only

PACKAGE DIAGRAMS

PLCC



LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-888-ISP-PLDS; FAX (503) 681-3037; http://www.latticesemi.com

GAL22LV10Z AND GAL22LV10ZD ORDERING INFORMATION

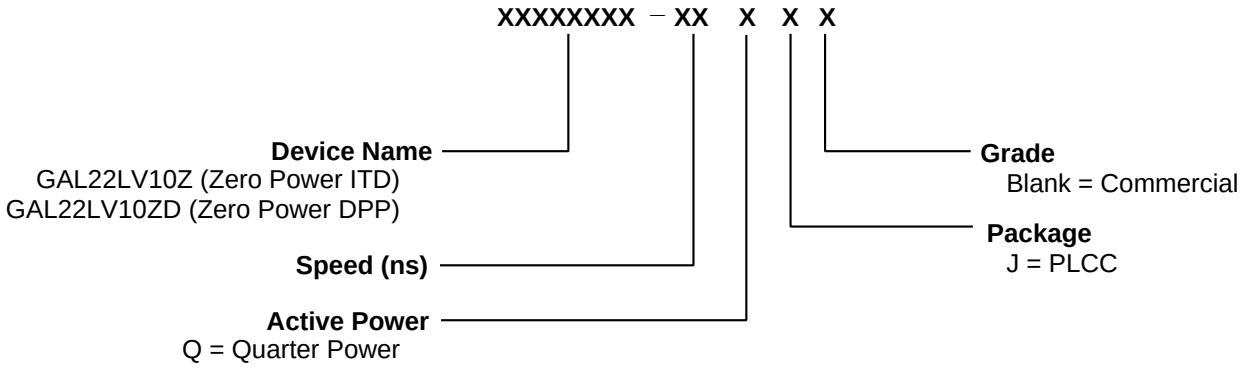
GAL22LV10Z: Commercial Grade Specifications

Tpd (ns)	Tsu1 (ns)	Tco (ns)	Icc (mA)	Isb (μA)	Ordering #	Package
15	10	10	55	100	GAL22LV10Z-15QJ	28-Lead PLCC
25	15	15	55	100	GAL22LV10Z-25QJ	28-Lead PLCC

GAL22LV10ZD: Commercial Grade Specifications

Tpd (ns)	Tsu1 (ns)	Tco (ns)	Icc (mA)	Isb (μA)	Ordering #	Package
15	10	10	55	100	GAL22LV10ZD-15QJ	28-Lead PLCC
25	15	15	55	100	GAL22LV10ZD-25QJ	28-Lead PLCC

PART NUMBER DESCRIPTION



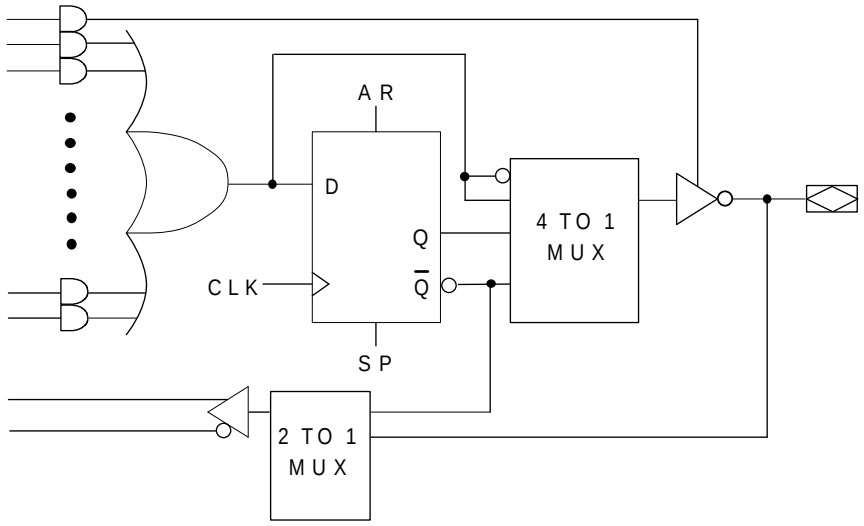
OUTPUT LOGIC MACROCELL (OLMC)

The GAL22LV10Z and GAL22LV10ZD have a variable number of product terms per OLMC. Of the ten available OLMCs, two OLMCs have access to eight product terms (pins 17 and 27), two have ten product terms (pins 18 and 26), two have twelve product terms (pins 19 and 25), two have fourteen product terms (pins 20 and 24), and two OLMCs have sixteen product terms (pins 21 and 23). In addition to the product terms available for logic, each OLMC has an additional product-term dedicated to output enable control.

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinatorial or registered mode. This allows each output to be individually configured as either active high or active low.

The GAL22LV10Z and GAL22LV10ZD have a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registers to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.



GAL22LV10Z AND GAL22LV10ZD OUTPUT LOGIC MACROCELL (OLMC)

OUTPUT LOGIC MACROCELL CONFIGURATIONS

Each of the Macrocells of the GAL22LV10Z and GAL22LV10ZD have two primary functional I/O modes: registered, and combinatorial. The modes and the output polarity are set by two bits (SO and S1), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the following page.

REGISTERED

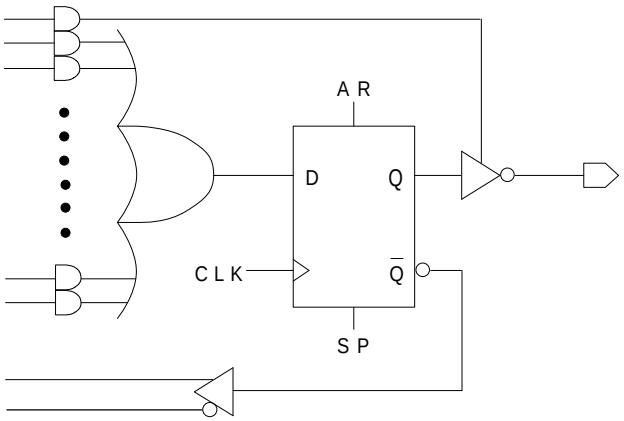
In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each OLMC, and can therefore be defined by a logic equation. The D flip-flop's $\overline{Q}$ output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array.

NOTE: In registered mode, the feedback is from the $\overline{Q}$ output of the register, and not from the pin; therefore, a pin defined as registered is an output only, and cannot be used for dynamic I/O, as can the combinatorial pins.

COMBINATORIAL I/O

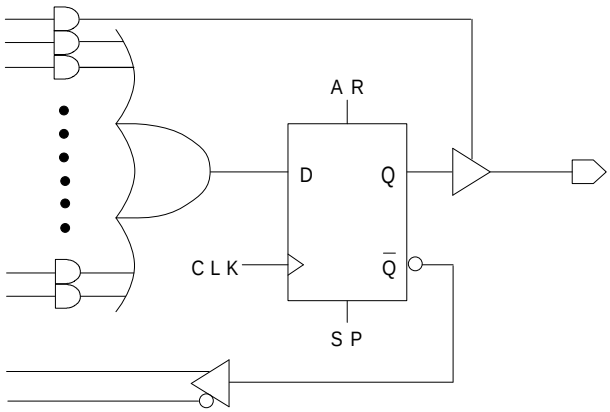
In combinatorial mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feedback into the AND array is from the pin side of the output enable buffer. Both polarities (true and inverted) of the pin are fed back into the AND array.

REGISTERED MODE



ACTIVE LOW

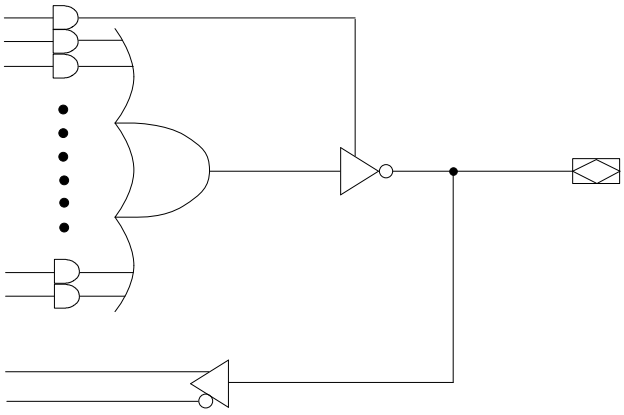
$S_0 = 0$
$S_1 = 0$



ACTIVE HIGH

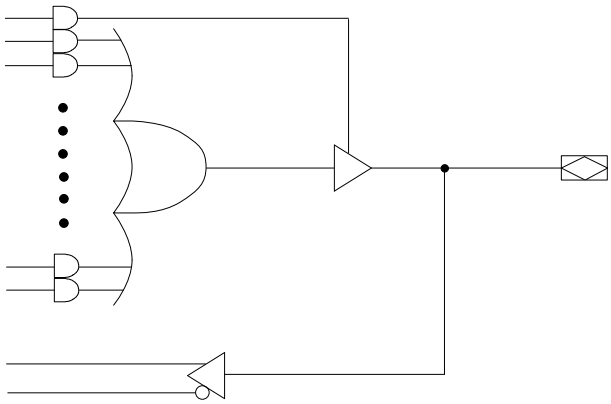
$S_0 = 1$
$S_1 = 0$

COMBINATORIAL MODE



ACTIVE LOW

$S_0 = 0$
$S_1 = 1$

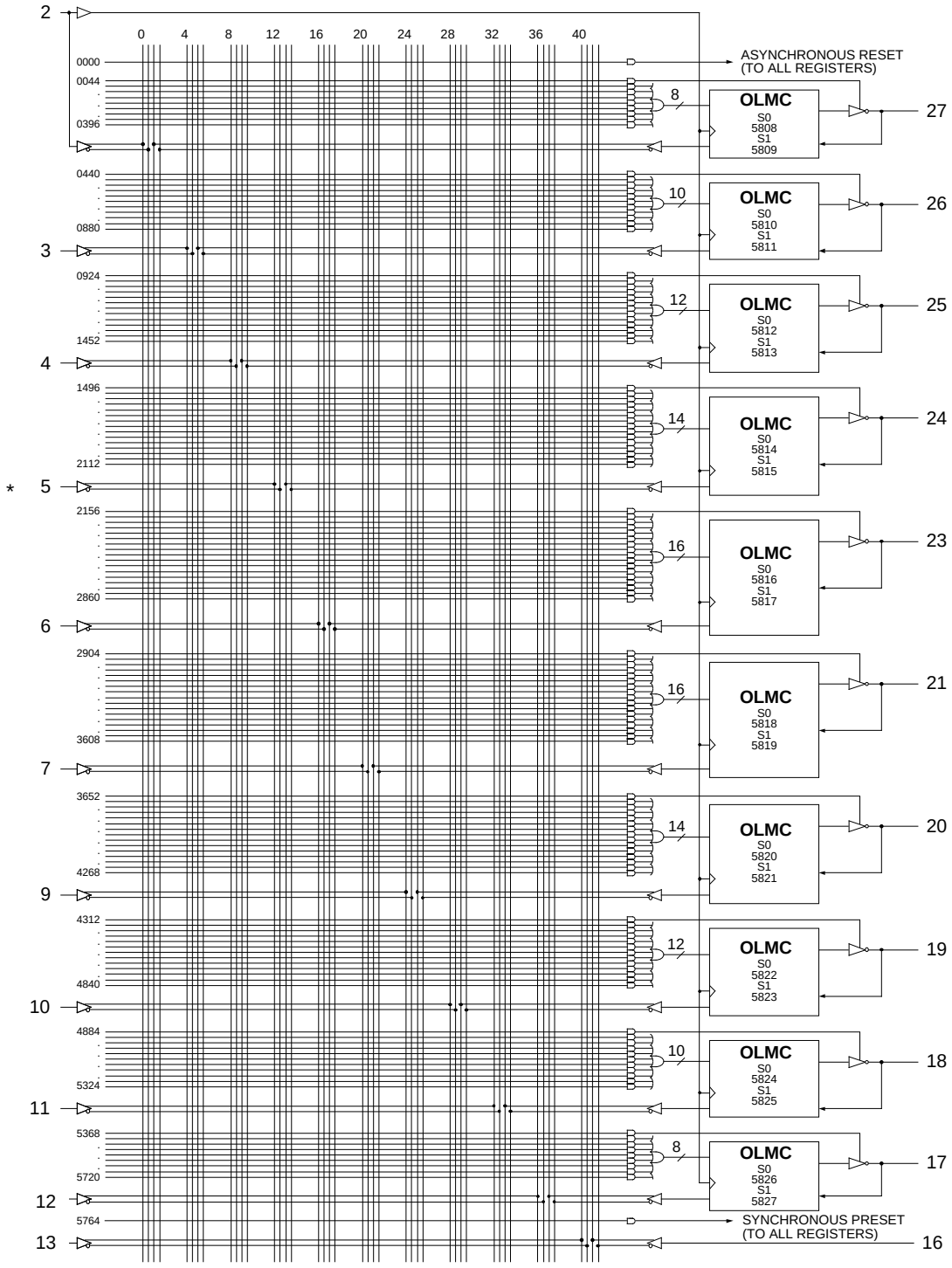


ACTIVE HIGH

$S_0 = 1$
$S_1 = 1$

GAL22LV10Z AND GAL22LV10ZD LOGIC DIAGRAM / JEDEC FUSE MAP

PLCC Package



5828, 5829 ... Electronic Signature ... 5890, 5891							
Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0

MSB LSB

* Note: Input not available on GAL22LV10ZD

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... -0.5 to +5.6V

Input voltage applied ..... -0.5 to +5.6V
Off-state output voltage applied ..... -0.5 to +5.6V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to +75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +3.0 to +3.6V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[2]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	5.25	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	-10	µA
I_{IH}	Input or I/O High Leakage Current	$(V_{CC} - 0.2)V \le V_{IN} \le V_{CC}$	—	—	10	µA
		$V_{CC} \le V_{IN} \le 5.25V$	—	—	1	mA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
		I_{OL} = 0.5 mA Vin = V_{IL} or V_{IH}	—	—	0.2	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
		I_{OH} = -0.5 mA Vin = V_{IL} or V_{IH}	Vcc-0.45	—	—	V
		I_{OH} = -100 µA Vin = V_{IL} or V_{IH}	Vcc-0.2	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	-8	mA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 3.3V V_{OUT} = 0.5V T_A = 25°C	-30	—	-130	mA

COMMERCIAL

I_{SB}	Stand-by Power Supply Current	V_{IL} = GND V_{IH} = Vcc Outputs Open	Z -15/-25 ZD -15/-25	—	50	100	µA
I_{CC}	Operating Power Supply Current	V_{IL} = GND V_{IH} = 3.0V f_{toggle} = 5 MHz Outputs Open	Z -15/-25 ZD -15/-25	—	40	55	mA

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2) Typical values are at Vcc = 3.3V and T_A = 25 °C

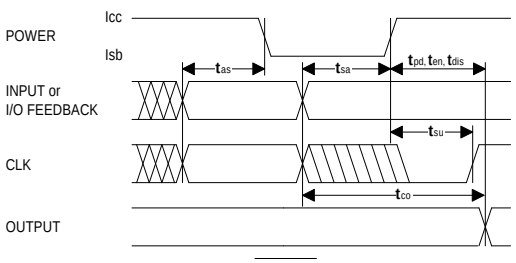
AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAM	TEST COND.[1]	DESCRIPTION	COM -15 MIN.	COM -15 MAX.	COM -25 MIN.	COM -25 MAX.	UNITS
tpd	A	Input or I/O to Combinatorial Output	3	15	3	25	ns
tco	A	Clock to Output Delay	2	10	2	15	ns
tcf[2]	—	Clock to Feedback Delay	—	10	—	10	ns
tsu1	—	Setup Time, Input or Fdbk before Clk↑	10	—	15	—	ns
tsu2	—	Setup Time, SP before Clk↑	14	—	20	—	ns
th	—	Hold Time, Input or Fdbk after Clk↑	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	50	—	33.3	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	50	—	40	—	MHz
	A	Maximum Clock Frequency with No Feedback	71.4	—	50	—	MHz
twh	—	Clock Pulse Duration, High	6	—	10	—	ns
twl	—	Clock Pulse Duration, Low	6	—	10	—	ns
ten	B	Input or I/O to Output Enabled	3	15	3	25	ns
tdis	C	Input or I/O to Output Disabled	3	15	3	25	ns
tar	A	Input or I/O to Asynch. Reset of Reg.	3	20	3	25	ns
tarw	—	Asynch. Reset Pulse Duration	15	—	25	—	ns
tarr	—	Asynch. Reset to Clk↑ Recovery Time	10	—	25	—	ns
tspr	—	Synch. Preset to Clk↑ Recovery Time	10	—	15	—	ns
tas	A	Last Active Input to Standby	100	250	100	250	ns
tsa[4]	A	Standby to Active Output	—	15	—	20	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from **f**max with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.
4) Add **t**sa to **t**pd, **t**su, **t**ar, **t**en and **t**dis when the device is transitioning from standby state to active state.

STANDBY POWER TIMING WAVEFORMS



AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAM	TEST COND.[1]	DESCRIPTION	COM -15		COM -25		UNITS
			MIN.	MAX.	MIN.	MAX.	
tpd	A	Input or I/O to Combinatorial Output	3	15	3	25	ns
tco	A	Clock to Output Delay	2	10	2	15	ns
tcf[2]	—	Clock to Feedback Delay	—	10	—	10	ns
tsu1	—	Setup Time, Input or Fdbk before Clk↑	10	—	15	—	ns
tsu2	—	Setup Time, SP before Clk↑	14	—	20	—	ns
th	—	Hold Time, Input or Fdbk after Clk↑	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	50	—	33.3	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	50	—	40	—	MHz
	A	Maximum Clock Frequency with No Feedback	71.4	—	50	—	MHz
twh	—	Clock Pulse Duration, High	6	—	10	—	ns
twl	—	Clock Pulse Duration, Low	6	—	10	—	ns
ten	B	Input or I/O to Output Enabled	3	15	3	25	ns
tdis	C	Input or I/O to Output Disabled	3	15	3	25	ns
tar	A	Input or I/O to Asynch. Reset of Reg.	3	20	3	25	ns
tarw	—	Asynch. Reset Pulse Duration	15	—	25	—	ns
tarr	—	Asynch. Reset to Clk↑ Recovery Time	10	—	25	—	ns
tspr	—	Synch. Preset to Clk↑ Recovery Time	10	—	15	—	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from **f**max with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.

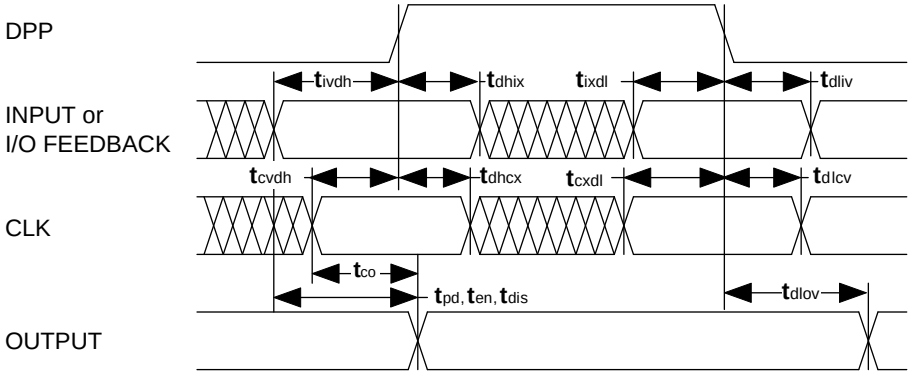
DEDICATED POWER-DOWN PIN SPECIFICATIONS

Over Recommended Operating Conditions

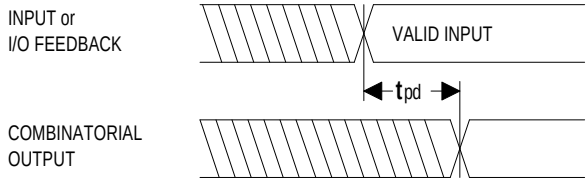
PARAMETER	TEST COND[1].	DESCRIPTION	COM -15 MIN.	COM -15 MAX.	COM -25 MIN.	COM -25 MAX.	UNITS
t_{whd}	—	DPP Pulse Duration High	40	—	40	—	ns
t_{wld}	—	DPP Pulse Duration Low	30	—	40	—	ns
ACTIVE TO STANDBY							
t_{ivdh}	—	Valid Input before DPP High	0	—	0	—	ns
t_{cvdh}	—	Valid Clock Before DPP High	0	—	0	—	ns
t_{dhix}	—	Input Don't Care after DPP High	—	15	—	25	ns
t_{dhcx}	—	Clock Don't Care after DPP High	—	15	—	25	ns
STANDBY TO ACTIVE							
t_{ixdl}	—	Input Don't Care before DPP Low	—	0	—	0	ns
t_{cxdl}	—	Clock Don't Care before DPP Low	—	0	—	0	ns
t_{dliv}	—	DPP Low to Valid Input or I/O	20	—	25	—	ns
t_{dlcv}	—	DPP Low to Valid Clock	30	—	35	—	ns
t_{dlov}	A	DPP Low to Valid Output	5	35	5	45	ns

1) Refer to **Switching Test Conditions** section.

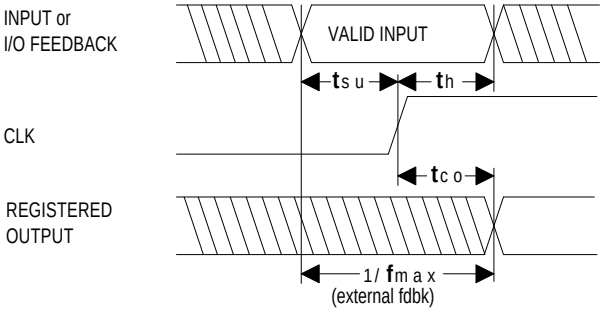
DEDICATED POWER-DOWN PIN (DPP) TIMING WAVEFORMS



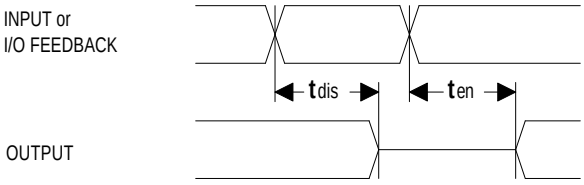
SWITCHING WAVEFORMS



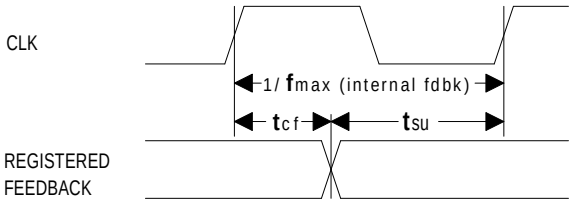
Combinatorial Output



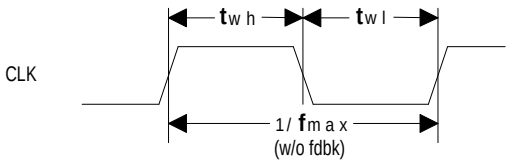
Registered Output



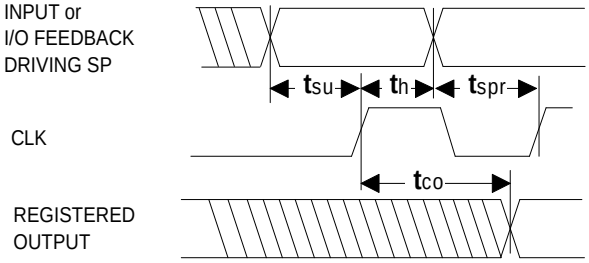
Input or I/O to Output Enable/Disable



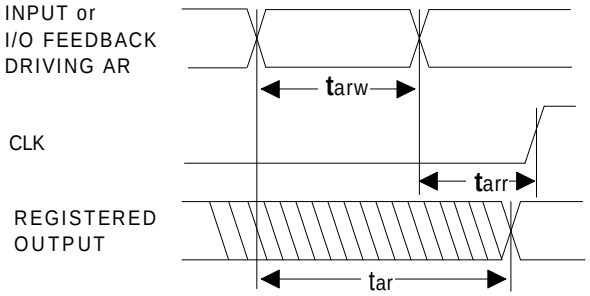
fmax with Feedback



Clock Width



Synchronous Preset

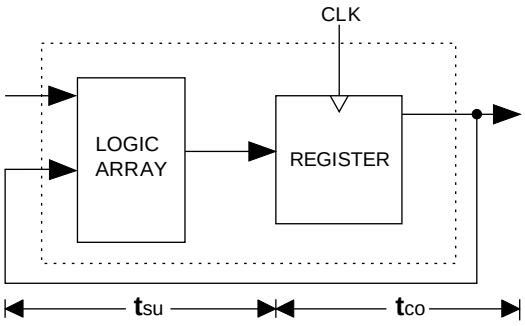


Asynchronous Reset

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

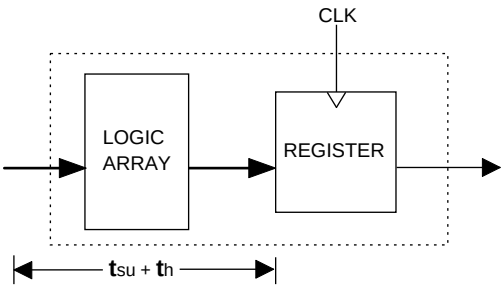
SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 3.3V, V_I = 0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 3.3V, $V_{I/O}$ = 0V

fmax DESCRIPTIONS



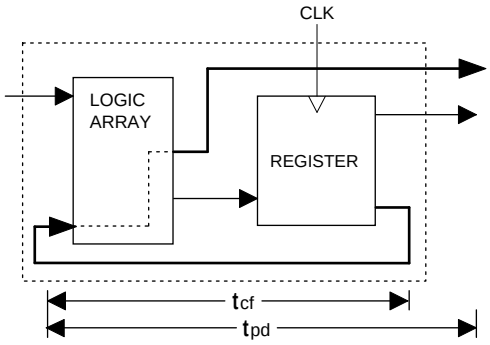
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured **t**su and **t**co.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting **t**su from the period of fmax w/internal feedback (**t**cf = 1/**f**max - **t**su). The value of **t**cf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to **t**cf + **t**pd.

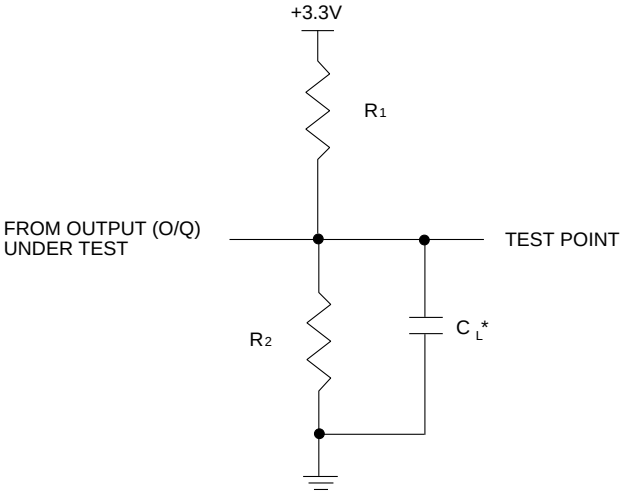
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	2ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

All 3-state levels are measured at (Voh - 0.5) V and (Vol + 0.5) V.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		270Ω	220Ω	35pF
B	Active High	270Ω	220Ω	35pF
	Active Low	270Ω	220Ω	35pF
C	Active High	270Ω	220Ω	5pF
	Active Low	270Ω	220Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided in every GAL22LV10Z and GAL22LV10ZD device. It contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

The electronic signature is an additional feature not present in other manufacturers' 22V10 devices. To use the extra feature of the user-programmable electronic signature it is necessary to choose a Lattice Semiconductor 22LV10 device type when compiling a set of logic equations. In addition, many device programmers have two separate selections for the device, typically a GAL22LV10 and a GAL22LV10-UES (UES = User Electronic Signature). This allows users to maintain compatibility with existing 22V10 designs, while still having the option to use the GAL device's extra feature.

The JEDEC map for the GAL22LV10Z and GAL22LV10ZD contains the 64 extra fuses for the electronic signature, for a total of 5892 fuses. However, GAL22LV10Z and GAL22LV10ZD devices can still be programmed with a standard 22V10 JEDEC map (5828 fuses) with any qualified device programmer.

SECURITY CELL

A security cell is provided in every GAL22LV10Z and GAL22LV10ZD device to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers (see the the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because certain events may occur during system operation that throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

GAL22LV10Z and GAL22LV10ZD devices include circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

INPUT BUFFERS

GAL22LV10Z and GAL22LV10ZD devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

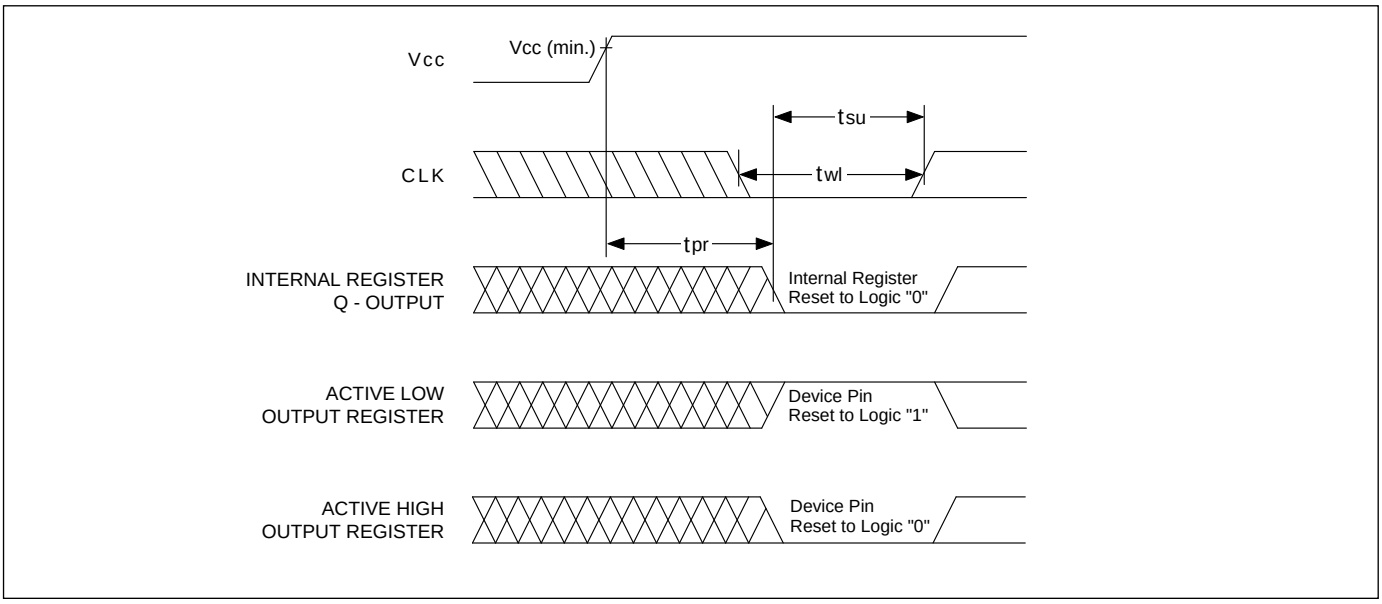
INPUT TRANSITION DETECTION (ITD)

The GAL22LV10Z relies on its internal input transition detection circuitry to put the device into power down mode. If there is no input transition for the specified period of time, the device will go into the power down state. Transition detection on any input or I/O will put the device back into the active state. Any input pulse widths greater than 5ns at an input transition voltage level of 1.5V will be detected as an input transition. The device will not detect input pulse widths less than 1ns measured at an input transition voltage level of 1.5V as an input transition.

DEDICATED POWER-DOWN PIN (DPP)

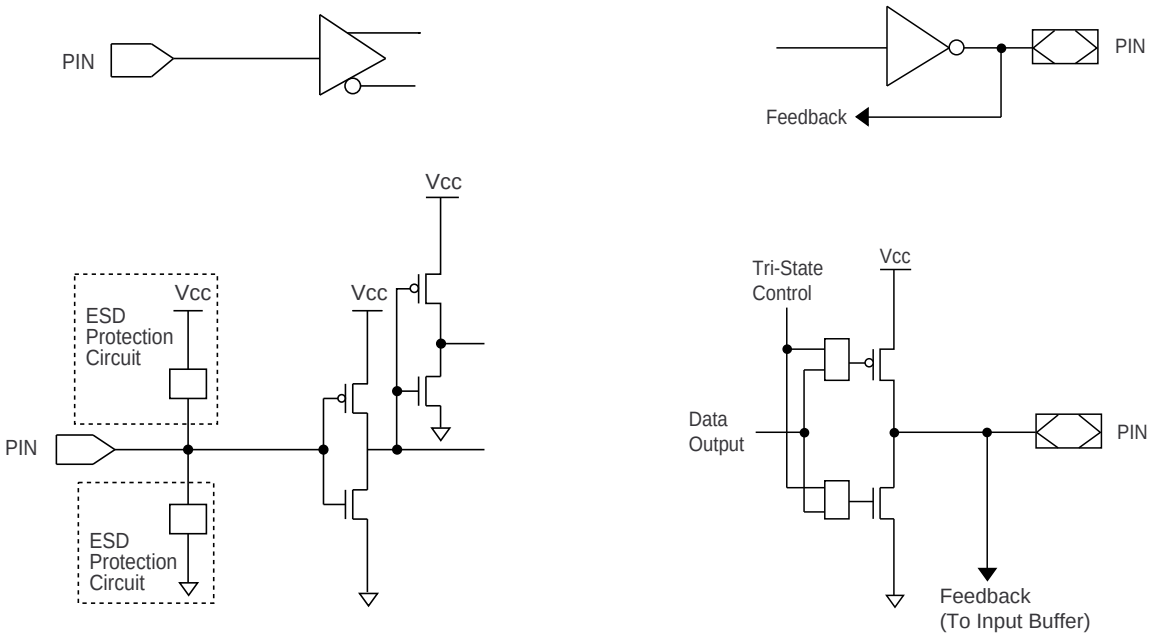
The GAL22LV10ZD uses pin 5 as the dedicated power-down signal to put the device into the standby state. DPP is an active high signal. A logic high driven onto this signal puts the device into the standby state. Input pin 5 cannot be used as a logic function input on this device.

POWER-UP RESET



Circuitry within the GAL22LV10Z and GAL22LV10ZD provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 10µs MAX). As a result, the state on the registered output pins (if they are enabled) will be either high or low on power-up, depending on the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the device. First, the V_{CC} rise must be monotonic. Second, the clock input must be at a static TTL level as shown in the diagram during power up. The registers will reset within a maximum of tpr time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

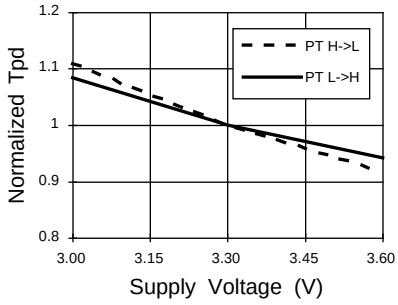
INPUT/OUTPUT EQUIVALENT SCHEMATICS



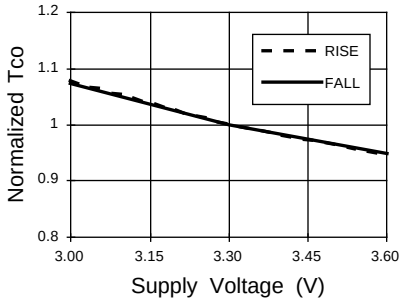
Typical Input **Typical Output**

GAL22LV10Z/ZD: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

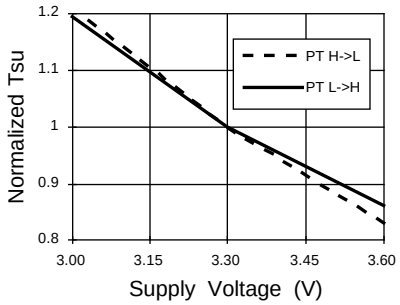
Normalized Tpd vs Vcc



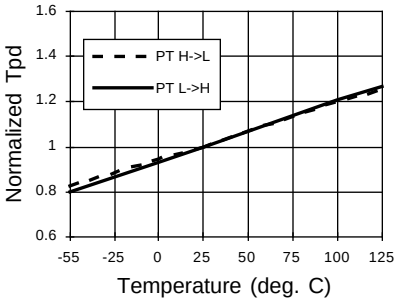
Normalized Tco vs Vcc



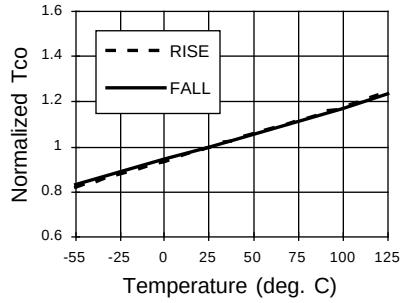
Normalized Tsu vs Vcc



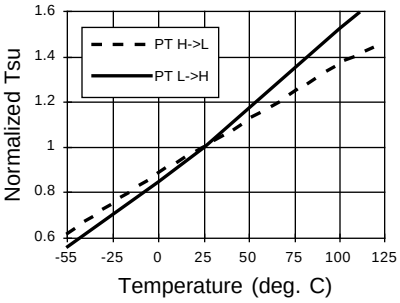
Normalized Tpd vs Temp



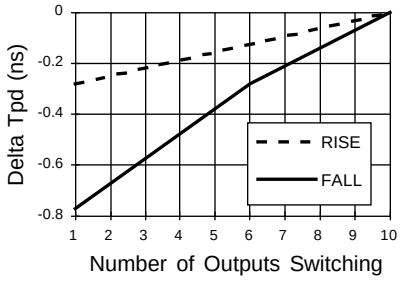
Normalized Tco vs Temp



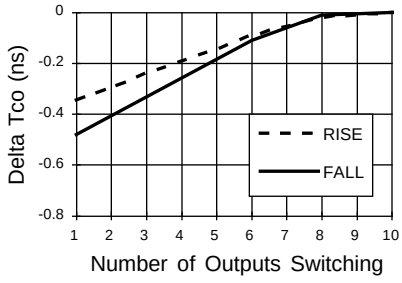
Normalized Tsu vs Temp



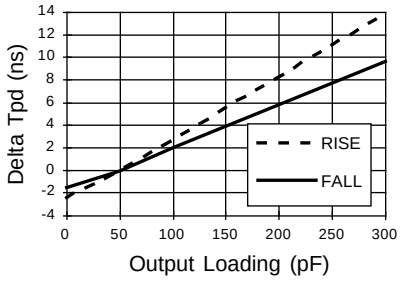
Delta Tpd vs # of Outputs Switching



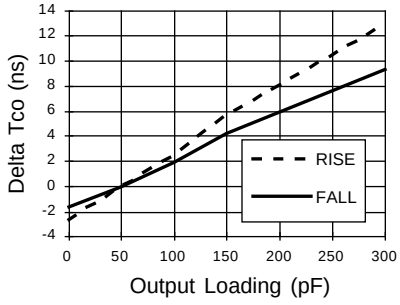
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

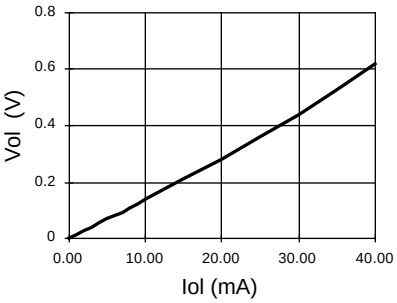


Delta Tco vs Output Loading

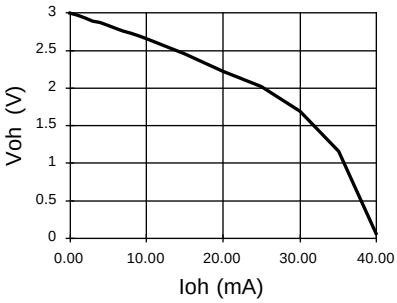


GAL22LV10Z/ZD: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

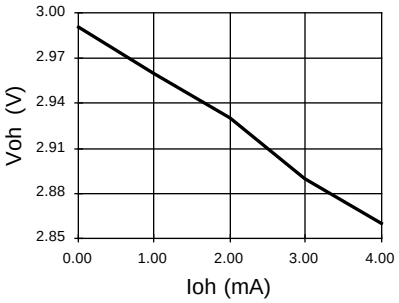
Vol vs Iol



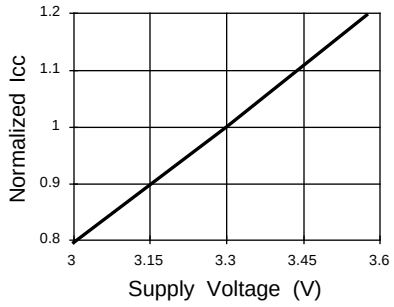
Voh vs Ioh



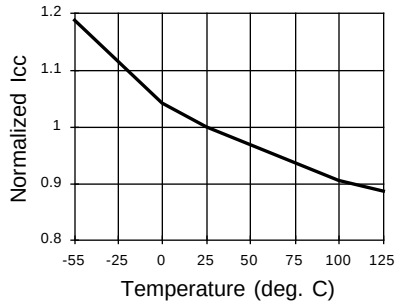
Voh vs Ioh



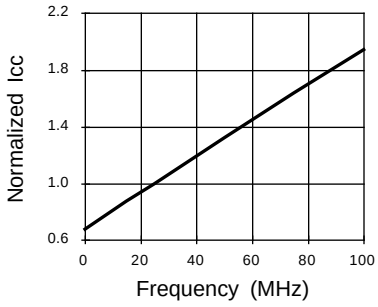
Normalized Icc vs Vcc



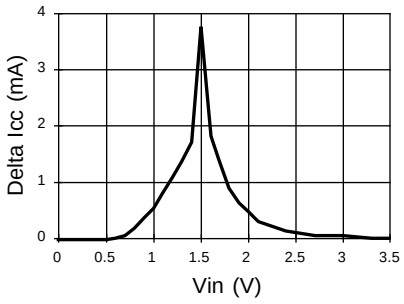
Normalized Icc vs Temp



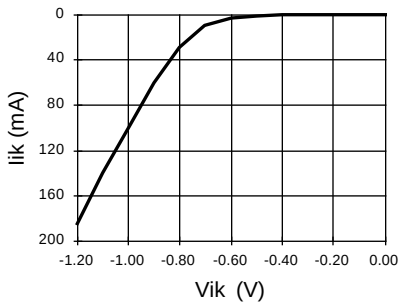
Normalized Icc vs Freq.



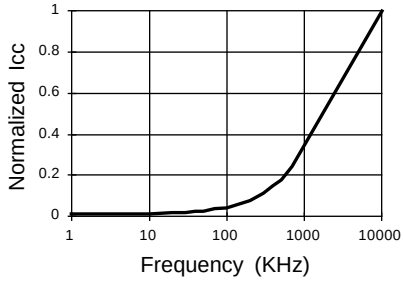
Delta Icc vs Vin (1 input)



Input Clamp (Vik)



Normalized Icc vs Freq. (ITD)



LATTICE SEMICONDUCTOR CORPORATION
5555 Northeast Moore Court
Hillsboro, Oregon 97124 U.S.A.
Tel.: (503) 681-0118
FAX: (503) 681-3037
http://www.latticesemi.com

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