pDS+™ Viewlogic Software

Features

- **ispLSI® AND pLSI® DEVELOPMENT SYSTEM**
  - **Supports ispLSI and pLSI 1000/E and 2000**
  - **Upgrade to Support ispLSI and pLSI 3000**

- **INTEGRATED PRO SERIES™, WORKVIEW PLUS™ AND POWERVIEW™ DEVELOPMENT ENVIRONMENT FOR DESIGN ENTRY**
  - **Schematic Entry**
  - **Synthesis VHDL Language Entry**
  - **Over 300 "TTL-Like" Macros**
  - **Graphical, Menu-Driven User Interface**
  - **Command Line-Driven User Interface**

- **LATTICE SEMICONDUCTOR pDS+ VIEWLOGIC FITTER**
  - **Multi-Level Logic Synthesis**
  - **Efficient Design Optimization and Minimization**
  - **Automatic Mapping and Device Fitting**
  - **Automatic Partitioning with High Utilization**
  - **Predictable Performance**

- **COMPLETE DESIGN VERIFICATION**
  - **Using Viewsim™/PROsim™ Timing Simulator**
  - **Using Vantage Speedwave Timing Simulator**

- **INDUSTRY STANDARD PROGRAMMING FILE GENERATION**
  - **Standard JEDEC Device Fuse Map**

- **IN-SYSTEM PROGRAMMING SUPPORT**
  - **ispCODE™ C Source Routines Included**
  - **ISP Daisy Chain Download (PC Versions)**
  - **ispATE™ Board Test Programming Utility**

- **PLATFORMS SUPPORTED**
  - **PC Windows 3.1/Windows 95/Windows NT**
  - **Sun O/S 4.x**
  - **Sun Solaris 2 O/S 2.3 and Above**

Introduction

The pDS+ Viewlogic Software from Lattice Semiconductor Corporation (LSC) offers a powerful solution to fit high density logic designs into Lattice Semiconductor Corporation's (LSC) ispLSI and pLSI devices.

Design entry and implementation is made simple using the software environments from Viewlogic Corporation. The pDS+ Viewlogic software supports high level, device independent design entry together with efficient logic compilation, delivering the most complex designs in the shortest time possible.

Viewlogic Software

Viewlogic supports schematic entry using Workview Plus or Powerview (Viewdraw) or PRO Series PROcapture software. Viewdraw/PROcapture works with a library of over 300 TTL-like macros to let you create designs without regard to any specific device dependencies. Viewdraw/PROcapture offer advanced features such as cut and paste, unlimited zoom and pan functions, automatic symbol generation as well as many other features to streamline and speed-up the design and verification process. Optional Viewsynthesis/PROsynthesis software supports VHDL language entry as well. The integrated design environment supports optional timing simulators, Viewsim/PROsim, so designs can be fully simulated before device programming. The Menu-driven environment makes design implementations as easy as a single click of the mouse button. The pDS+ Viewlogic design environment also offers the user multi-window operation, allowing schematic, simulator and waveform (Viewwave/PROwave) windows to be opened concurrently. Results can also be dynamically back annotated to the schematic for design verification.

The Viewwave/PROwave software are graphical editors for creating simulation input stimulus as well as analyzing waveforms. This graphical editor/analyzer also increases designer productivity through its speed and ease-of-use. Workview Office™ software support is scheduled. Contact Lattice Semiconductor for availability.

pDS+ Viewlogic Fitter

The pDS+ Viewlogic Fitter for ispLSI and pLSI devices is completely integrated within the Viewlogic environment. The pDS+ Viewlogic Fitter provides hands-off design implementation through intelligent design optimization, logic partitioning, automatic place and route and fusemap generation. Extensive top level design control is provided for design implementation optimized for speed and/or high device resource utilization.

1996 Data Book

pDS+ Viewlogic Macro Library

The pDS+ Viewlogic software offers an extensive selection (over 300) of TTL-like macros. These macros enable the design engineer to use familiar predefined functions to build a design. Table 1 shows a summary of the available macros in the pDS+ software.

Table 1. Macro Summary

Macro Type	Quantity
AND/NAND	29
OR/NOR	24
XOR/XNOR	12
I/Os	89
Flip-Flops	39
Latches	30
Arithmetic	33
Counters	65
Shift Registers	15
Miscellaneous	45

Design Optimization and Logic Minimization

The pDS+ Viewlogic Fitter uses proprietary logic synthesis algorithms targeted for device-specific features. The fitter performs a thorough design optimization, utilizing logic minimization, product term sharing and XOR functions wherever necessary. In addition, the pDS+ Viewlogic Fitter supports multiple fitting strategies to obtain the best device utilization and performance.

Automatic Partitioning

The pDS+ Viewlogic Fitter incorporates a powerful Automatic Partitioner for hands-free synthesis of a design into Generic Logic Blocks (GLBs). The partitioner takes full advantage of the device's powerful features such as the hard XOR and product term sharing. The internal XOR can be utilized for Arithmetic functions, T-Type flip-flops, and on & off set optimization functions. The partitioner also makes extensive use of product term sharing. Product term sharing allows the Fitter to efficiently use device

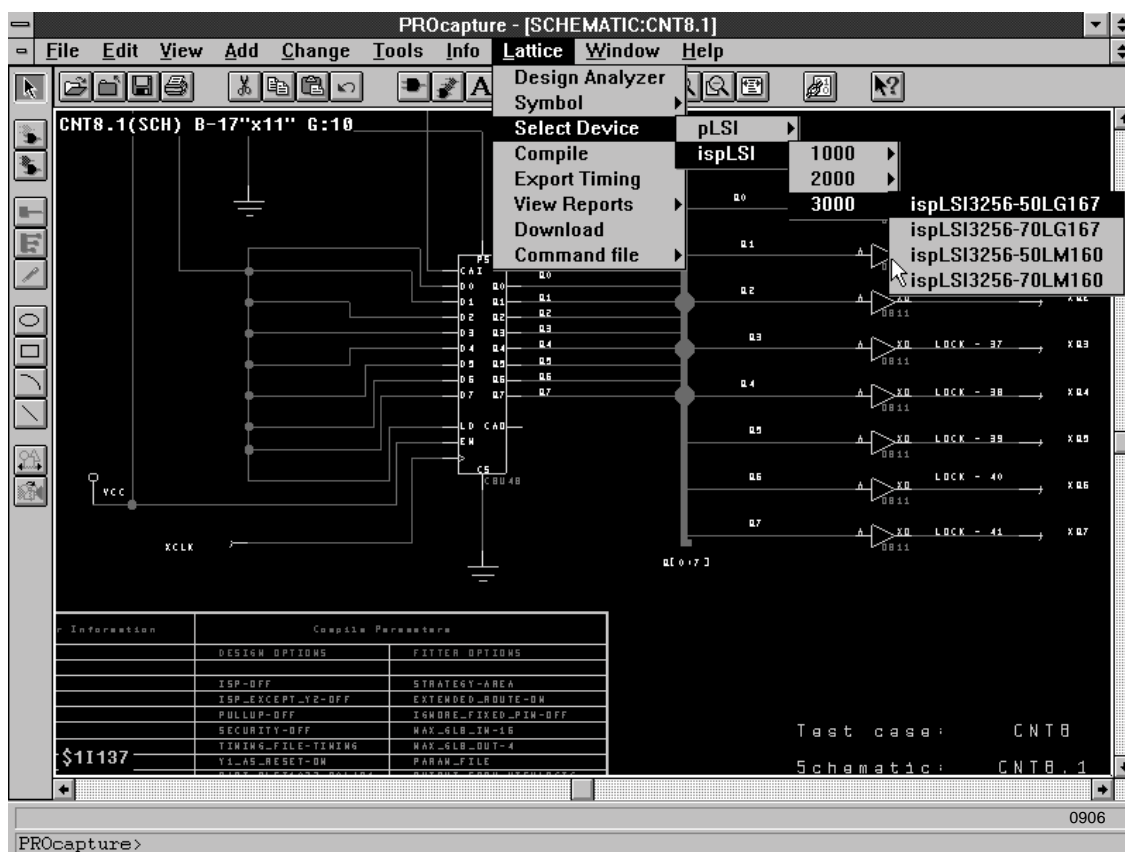**Figure 1. pDS+ Viewlogic PC Design Interface**

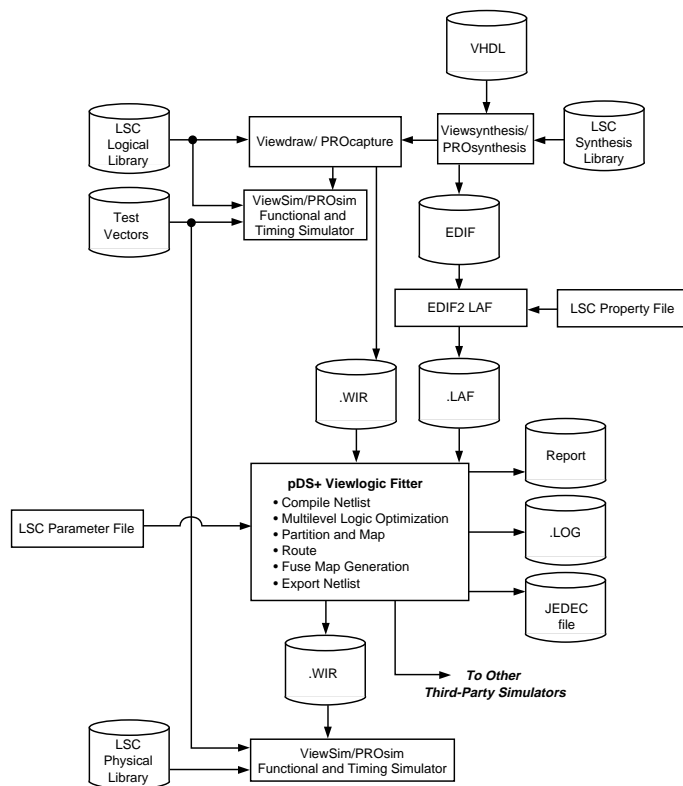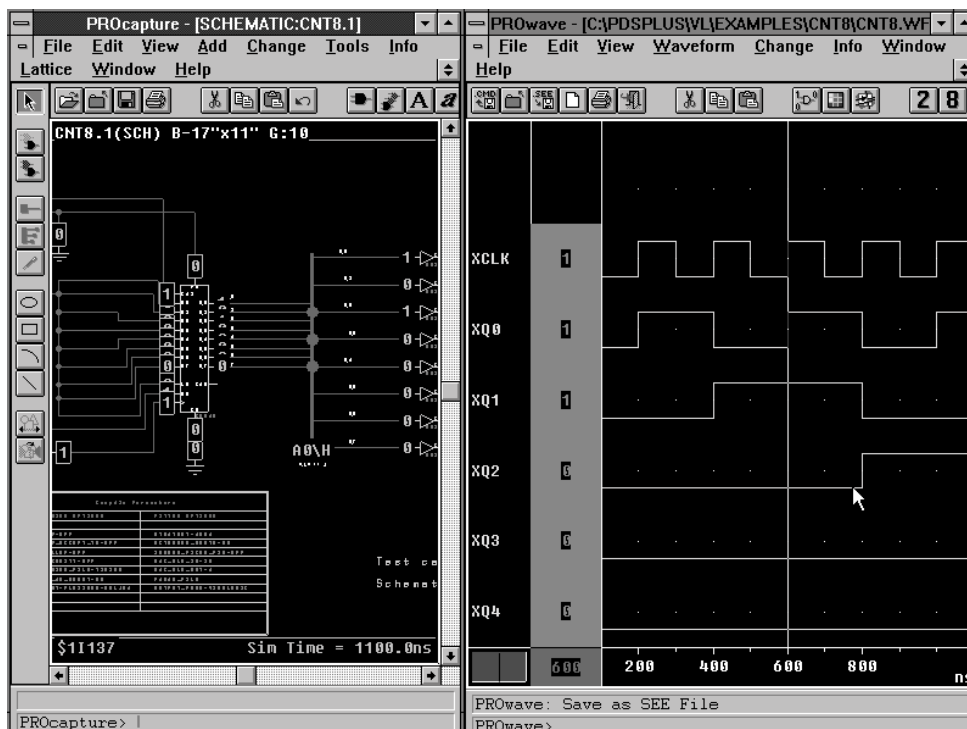**Figure 2. pDS+ Viewlogic Integrated Design Environment**

Figure 3. Viewlogic Multi-Window Design Environment

resources by sharing product terms across multiple logic functions. These features combine to maximize device resource utilization and increase design performance.

Automatic Place and Route

Automatic place and route eliminates the need for manual editing and accelerates the design cycle. The Router automatically generates pinouts based on the optimal design implementation or user assigned pinouts.

The Extended Route option performs a comprehensive route to maximize device resource utilization and ensure efficient design implementation. The result is that small design changes won't cause expensive PC board re-work.

Design Parameter Control

The pDS+ Viewlogic Fitter offers extensive design parameter control at the design entry level, letting the user optimize the design for maximum utilization and/or speed. All of the controls are specified using "Attributes" in the Viewdraw/PROcapture design file. These controls fall into two categories:

— Fitter Controls
— Design Implementation Controls
    — Net Attributes
    — Pin Attributes
    — Path Attributes
    — Symbol Attributes

Fitter Control Options

Special properties can be passed to the pDS+ Viewlogic Fitter providing complete control over critical design considerations. Fitter control over design partitioning and routing optimizes the design for speed and/or device utilization. Here are a few of the powerful features:

Feature	Description
PART	Determines device type to be used.
PARAM_FILE	Allows user to specify attributes in a text file.
STRATEGY	Choice of AREA (default), DELAY or NO_OPTIMIZE. AREA optimizes device space, DELAY keeps GLB levels to a minimum and NO_OPTIMIZE does not reduce equations.

Feature	Description
USE_GLOBAL_RESET	Causes global reset to use dedicated routing for reset.
MAX_GLB_OUT	Specifies maximum number of outputs from a GLB. Default is 4.
MAX_GLB_IN	Controls maximum number of inputs to a GLB. Default is 16 for 1K and 2K devices and 24 for 3K devices.
EFFORT	Controls optimization of partitioner.
EXTENDED_ROUTE	Choice of OFF (fixed) or ON (extended, default).
PIN_FILE	Specifies locked pin assignments.

Design Implementation Controls

Device controls are used for changing design parameters such as security. Some of these implementation controls are:

Feature	Description
ISP	Instructs Router to reserve in-system programming pins.
ISP_EXCEPT_Y2	Reserves all ISP pins except Y2 (ispLSI and pLSI 1016/E and 2032 only).
Y1_AS_RESET	Uses Y1 clock pin on ispLSI and pLSI 1016/E and 2032 as a global reset pin.
SECURITY	Sets the device security cell to prevent unauthorized fuse map read back.

Net Attributes

Feature	Description
CLK0-CLK2	Assigns a CLK signal to a dedicated CLK line.
IOCLK0-IOCLK1	Assigns a CLK signal to a dedicated IOCLK line if single fanout input pin.
FASTCLK	Fitter assigns CLK signal to CLK0-CLK2 or IOCLK0-IOCLK1.
SLOWCLK	Assigns the CLK signal to a GLB product term CLK.
PRESERVE	Prevents logic minimization on specified nets.
GROUP	Suggests grouping of functions in a GLB.

Pin Attributes

Feature	Description
CRIT	Specifies Output Routing Pool Bypass to minimize delay.
SLOWSLEW	Assigns slow slew rate on a specific I/O cell.
LOCK	Assigns device I/O pins to design I/O ports.
PULLUP	Specifies internal pull-up resistors.

Path Attributes

The following properties specify paths in the design that have special fitting requirements:

Feature	Description
SAP/EAP	Defines asynchronous paths to prevent signal duplication.
SCP/ECP	Defines critical paths to reduce delays.
SNP/ENP	Defines logic paths for no logic minimization.

Symbol Attributes

Feature	Description
REGTYPE	Determines where a register is to be placed (IOC or GLB).
PROTECT	Prevents removal of a primitive or a macro during minimization.
OPTIMIZE	Selects either hard or soft macros.

Parameter File

The pDS+ Viewlogic Fitter provides a parameter file feature which helps designers eliminate the guesswork and optimizes the design for the right device. It allows the user to try a number of design implementation options using all of the design implementation controls in a batch mode. The parameter file instructs the partitioner and the router to maximize both device utilization and performance.

Property File

The pDS+ Viewlogic Fitter also accepts a property file (design.prp) which allows the designer to assign specific features to signals and nets using all of the design attributes available. The property file helps guide the fitter in implementing the design in the best way.

Design Verification

The pDS+ Viewlogic software offers complete post route design verification using the optional Viewsim/PROsim timing simulators. The pDS+ Viewlogic Fitter generates the "sim" file which can be used with the Viewsim/PROsim simulators, or other design platforms with behavioral simulation models from Synopsys Logic Modeling Division. VHDL timing simulation is supported by the Vantage Speedwave Simulator. The Viewlogic and Vantage simulation libraries and the PROsim simulator are available from Lattice Semiconductor.

Fuse Map Generation

The pDS+ Viewlogic software generates a device fusemap in standard JEDEC format. A security feature offers protection of proprietary designs from unauthorized duplication JEDEC format to the device fusemap thus facilitating a quick, easy functional verification of a programmed device.

System Requirements (PC Platform)

— 486/Pentium IBM Compatible PC
— MS DOS Version 3.3 or Later
— Windows 3.1 or Later
— 16 MB RAM with 30 MB Hard Disk Space
— Serial Port for Mouse
— 3 Button Mouse (Mouse Systems Compatible)
— Parallel Printer Port for Software Key
— Workview Plus 4.3 or later
— PROseries 6.0 or later

System Requirements (Sun Platform)

— Sun Sparc 4
— Sun O/S Version 4.x or Solaris 2.3 or Later
— Open Windows 3.0
— Powerview 5.1 or Later
— 16 MB RAM with 30 MB Hard Disk Space
— 3 Button Mouse

Programmer Support

All devices in the ispLSI device families can be programmed while installed on the target circuit board. In-system programming can be performed using an ispDOWNLOAD™ Cable and PC, by an on-board microprocessor or by ATE systems during final board test.

All ispLSI and pLSI devices can also be programmed using third-party PLD programmers. The devices are currently supported by programmers from the following vendors:

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88

Programmer Vendor	Model
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30A/B
System General	TURPRO-1/FX

High pin-count socket adapters are available from Emulation Technology, EDI Corporation and PROCON.

Product Ordering Information

Product Code	Description
pDS1102-PC2	Viewlogic Viewsim/PROsim and Viewdraw/PROcapture Libraries and Interface Files (Direct Viewlogic Customers on the PC)
pDS1102-SN1	Viewlogic Viewsim/PROsim and Viewdraw/PROcapture Libraries and Interface Files (Direct Viewlogic Customers on the Sun)
pDS1102-SN2	Viewlogic Viewsim/PROsim and Viewdraw/PROcapture Libraries and Interface Files (Direct Viewlogic Customers on the Sun)
pDS1103-PC2	Viewlogic Viewsim/PROsim and Viewdraw/PROcapture Software Upgrade, Libraries, and Interface Files (Viewlogic Software from Other FPGA Suppliers on the PC)
pDS1104-PC2	Viewlogic Viewsim/PROsim and Viewdraw/PROcapture Software Upgrade, Libraries, and Interface Files (Viewlogic Software from Xilinx on the PC)
pDS1105-PC2	Viewlogic Viewsynthesis/ PROsynthesis Library (PC)
pDS1105-SN1	Viewlogic Viewsynthesis/ PROsynthesis Library (Sun)
pDS1131-SN1	Verilog and VHDL Simulation Libraries (Sun)
pDS1131-SN2	Verilog and VHDL Simulation Libraries (Sun Solaris 2)
pDS1131-PC1	Verilog and VHDL Simulation Libraries (PC)
pDS1301-PC2	Viewlogic PROcapture Schematic Editor
pDS2101-PC2	pDS+ Viewlogic Fitter (PC)
pDS2101-SN1	pDS+ Viewlogic Fitter (Sun)
pDS2101-SN2	pDS+ Viewlogic Fitter (Solaris 2)

pDS2101-3UP/SN1	3000 Family Upgrade for pDS2101-3UP/SN1
pDS2101-3UP/PC2	3000 Family Upgrade for pDS2101-3UP/PC2
pDS3302A-PC2	pDS+ Viewlogic PROsim Functional and Timing Simulator (PC) for PROcapture Users
pDS3302-PC2	pDS+ Viewlogic PROsim Functional and Timing Simulator (PC) for Simulation Users Only
pDS3305A-PC2	Viewlogic PROsynthesis VHDL Synthesis Tools

Annual Maintenance*

pDS1102M-PC2	Maintenance for pDS1102-PC2
pDS1102M-SN1	Maintenance for pDS1102-SN1
pDS1102M-SN2	Maintenance for pDS1102-SN2
pDS1103M-PC2	Maintenance for pDS1103-PC2
pDS1104M-PC2	Maintenance for pDS1104-PC2
pDS1105M-PC2	Maintenance for pDS1105-PC2
pDS1105M-SN1	Maintenance for pDS1105-SN1
pDS1131M-SN1	Maintenance for pDS1131-SN1
pDS1131M-SN2	Maintenance for pDS1131-SN2
pDS1131M-PC1	Maintenance for pDS1131-PC1
pDS1301M-PC2	Maintenance for pDS1301-PC2
pDS2101M-PC2	Maintenance for pDS2101-PC2
pDS2101M-SN1	Maintenance for pDS2101-SN1
pDS2101M-SN2	Maintenance for pDS2101-SN2
pDS3302M-PC2	Maintenance for pDS3302-PC2 or pDS3302A-PC2
pDS3305AM-PC2	Maintenance for pDS3305A-PC2

*One year of maintenance is provided with every product purchase.

Warranty/Update Service

• 90-day warranty on disk media
• One-year maintenance support included with purchase
• Annual maintenance agreement available

Technical Support Assistance

Hotline:	1-800-LATTICE (Domestic)
	1-408-428-6414 (International)
BBS:	1-408-428-6417
FAX:	1-408-944-8450
email:	apps@latticesemi.com