# Phase Locked Loops (PLL) in High-Speed Designs

## Introduction

This application note describes the construction of a Phase Detector (PD) in conjunction with a Voltage Controlled Oscillator (VCO) to create a frequency generator synthesizer. All of the logic except the VCO and "RC" (time constant) is implemented in the ispLSI® 2032 device. The logic consists of two four-bit loadable down counters and the phase detector.

The ispLSI 2032 device has been specified because of its performance and device size. The ispLSI 2032 device is the fastest high-density Programmable Logic Device (PLD) available today.

Phase Locked Loop (PLL) circuits are used in many applications ranging from communications to video and audio equipment. They are used to ensure that a clock and/or phase of that clock is stable and in sync with a reference signal.

## General Information

A PLL is a circuit that consists of a phase detector, a loop filter and a reference clock. A VCO is usually employed to generate the desired output frequency. Figure 1 is a block diagram of a simple PLL circuit.

**Figure 1. PLL Block Diagram**

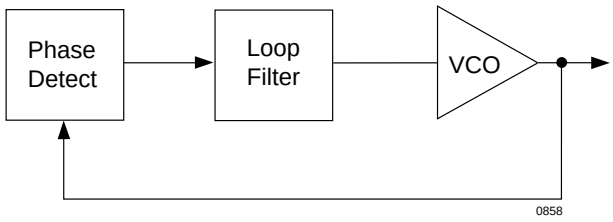
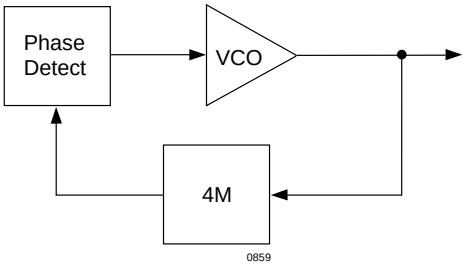



**Figure 2. DPLL Block Diagram**




When operating correctly, a PLL will "lock on" to an input and track its frequency and phase relationship. The circuit is used to synthesize or generate a frequency and maintain the phase of the generated signal to the reference. It can also be used to synchronize signals (clocks) to a reference.

In the digital design world, the PLL is more accurately a phase detector. With the ability to create digital circuits that emulate analog functions, more designers are moving away from analog. Many functions can now be implemented more easily and with more flexibility due to digital design techniques.

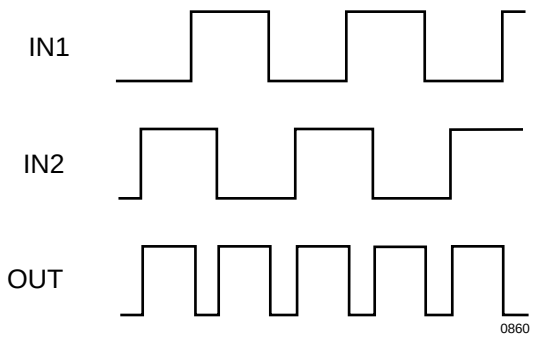
## Phase Detector

The phase detector circuit in Figure 2 is analogous to an analog PLL, it could be considered a Digital Phase Locked Loop (DPLL). The results of the PLL and the DPLL will be the same, even though the method of operation between the analog and digital versions is different.

There are different types of phase detectors. A phase detector must be able to detect a change in the state of one of the two inputs and tell which input stayed constant. This is important in the basic function of the phase detector. The circuit must have the ability to detect if the reference (or the feedback signal of the PLL) changed. As a result, the phase detector will adjust its output to cause the VCO to raise or lower the frequency and phase accordingly.

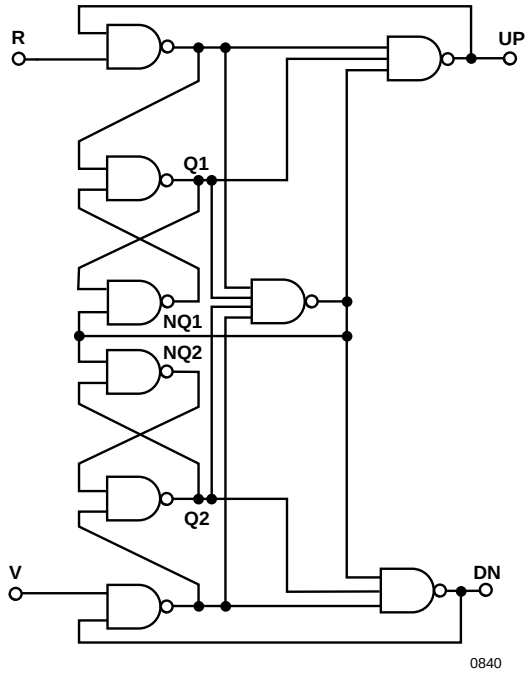
The most basic phase detector is an Exclusive Or gate (XOR). The XOR has a limited usefulness in feedback circuitry because of its inability to indicate which input changed first. Figure 3 shows the output relationship with respect to the input signals changing. This deficiency means a circuit with this type of PD would not be able to attain loop lock in some situations.

**Figure 3. XOR Input/Output Waveform**




A better way to implement a phase detector is with a cross-coupled latch. This single-ended phase detector can be either a rising or a falling edge detector, based on the polarity of the inputs. This circuit is adequate for most applications. Figure 4 is the falling edge phase detector, and is used in the example design of this application note. If a rising edge version of this detector is required, the inputs can be inverted to produce the desired result.

**Figure 4. Single Ended, Falling Edge Phase Detector**

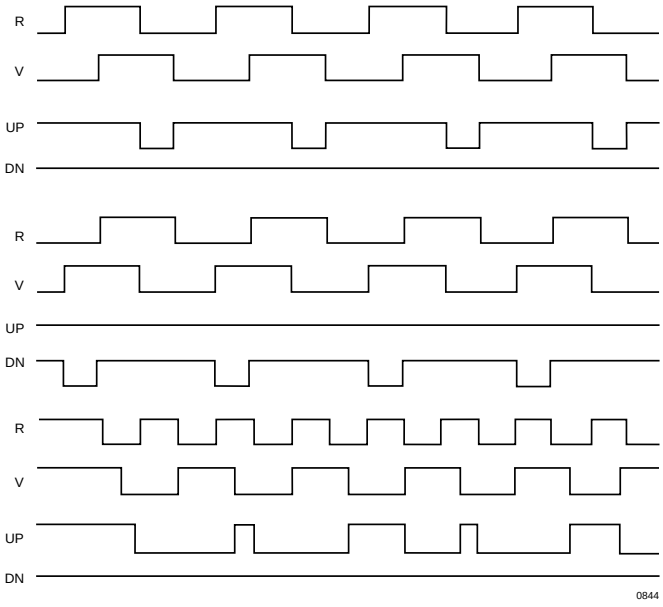



## Theory of Operation

A phase detector determines the difference in time of the edges of the two input signals. Those inputs are the reference (R) and the variable feedback (V). The difference causes the phase detector to generate pulses that cause the VCO to “correct” the frequency/phase. The loop filter is designed to allow small phase or frequency errors to be ignored. If the phase detector were to detect all changes, the PLL would go into an uncontrollable oscillation.

The PLL described in this application note uses a single ended, falling edge phase detector. This is a single ended phase detector because there is only one output for each cross-coupled NAND latch. The phase detector will detect a difference in the two input signals, however it will only react on the falling edge. The minimum phase error detected is approximately 3ns, which corresponds to the delay of the ispLSI 2032 device. The PLL will attain and remain in “loop lock” if both outputs (UP and DN) remain high. For use with a VCO, only one output is used, and the other is pulled up (if the output is an open drain). Phase error is independent of the input waveform duty cycle or its amplitude. The detector will only respond to transitions. Figure 5 shows the input and output waveform relationships of the phase detector.

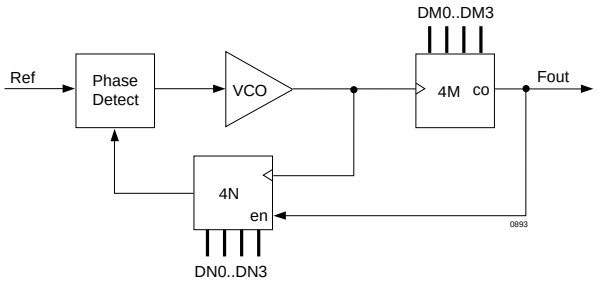
**Figure 5. Waveforms of the Phase Detector in Figure 4**



## Frequency Multiplier

As seen in Figure 2, the DPLL has a divider which is the feedback to the phase detector. This DPLL only has the ability to generate a frequency of equal to or less than the input or reference frequency. Figure 6 is a block diagram of the frequency multiplier. By having two counters, the output of the VCO can be multiplied by a number less than, greater than, or equal to 1. This enables the output of the DPLL to be a range of frequencies less than or greater than the input. Each counter input can be brought to an external pin on the ispLSI 2032 device to preset the counters to a value (which can change) by another device such as a microprocessor. If the inputs could be eliminated, the "load value" would be fixed.

**Figure 6. Frequency Multiplier**



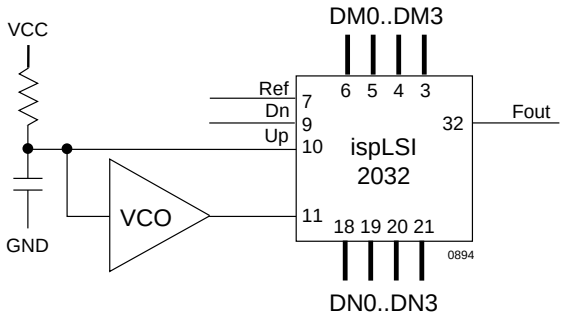

## Phase Detector Equations

The following equations describe the phase detector portion of the frequency multiplier. The equations have been demorganized to show the actual implementation in the ispLSI 2032.

```
NQ2 = (!DN & Q2.PIN & Q1.PIN & !UP)
      # (Q2.PIN)
      # (!V & Q2.PIN & Q1.PIN& !R)
      # (!V & Q2.PIN & Q1.PIN & !UP)
      # (!DN & Q2.PIN & Q1.PIN &!R);

NQ1 = (Q1.PIN)
      # (!V & Q2.PIN & Q1.PIN & !R)
      # (!V & Q2.PIN & Q1.PIN & !UP)
      # (!DN & Q2.PIN & Q1.PIN & !R)
      # (!DN & Q2.PIN & Q1.PIN &!UP);

Q2 = (!NQ2.PIN)
      # (!V) # (!DN);

Q1 = (!NQ1.PIN)
      # (!R) # (!UP);

DN = (!V & Q2 & !R & Q1)
      # (!V & Q2 & !UP.PIN & Q1)
      # (V &DN.PIN)
      # (!DN.PIN & Q2 & !R & Q1)
      # (!DN.PIN & Q2 & !UP.PIN & Q1)
      #(!Q2);

UP = (!DN.PIN & Q2 & !UP.PIN & Q1)
      # (R & UP.PIN) # (!Q1)
      # (!V & Q2& !R & Q1)
      # (!V & Q2 & !UP.PIN & Q1)
      # (!DN.PIN & Q2 & !R & Q1);
```

Figure 7 shows the pins used on the ispLSI 2032 device for the frequency multiplier. It also shows the external components needed to design the PLL.

**Figure 7. ispLSI 2032 Pin Connections for the PLL Design**




## Summary

With systems and devices increasing in speed and performance, faster and more accurate clocks are required. In many situations a clock must not only be accurate, it must also have error correcting capabilities. With a DPLL users can accomplish these requirements. By using an ispLSI 2032 device, the user can also achieve these required results with greater predictability. The ispLSI 2032 also provides the user with a more accurate circuit because of its high system performance.



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November 1996