Thermal Management

Introduction to Thermal Management

Thermal considerations are rarely an issue with low-density PLDs such as the Lattice Semiconductor GAL products, however, high-density PLDs often require consideration of thermal issues as part of any sound design methodology. To avoid reliability problems, Lattice Semiconductor specifies a maximum allowable junction temperature of 150 °C for its ispLSI and pLSI devices. The system designer should always complete a thermal analysis of their specific design to ensure that this temperature is not exceeded.

In addition to the device and package, the thermal characteristics of a circuit depend on the operating temperature, device power consumption, and the ability of the system to dissipate heat. The maximum junction temperature of a device can be calculated as shown:

$T_J = T_A + Power*\theta_{JA}$

or

$T_J = T_C + Power*\theta_{JC}$

Where :

T_J = Junction Temperature of the Device
T_A = Ambient Temperature
T_C = Case Temperature
θJ_A = Junction-to-Air Thermal Resistance (see table at the end of this section)
θJ_C = Case-to-Air Thermal Resistance (see table at the end of this section)
Power = $I_{CC} * V_{CC}$

Icc may be estimated as shown in the "Power Consumption" section of the individual data sheets. The parameters in the Icc equation may be found in the report file from the pDS or pDS+ development systems.

If the calculated T_J max exceeds 150°C, refer to the following hints to reduce overall power dissipation and package temperature.

Ways to Reduce Junction Temperature

1. Increase air flow in the system to reduce the case or ambient temperature.

2. Reduce power in one of the following ways:

    a. Reduce net utilization. Internal net utilization can be reduced by combining common input functions of the application into one logic block (GLB) The group feature of the pDS+ Fitter can be used to accomplish this task.

    b. Reduce the number of product terms (PT). The number of product terms can be reduced by either re-partitioning the device into multiple devices or carefully selecting how the logic function is implemented. For example, implementing a counter in a sum-of-product configuration will utilize more PT's than in an XOR implementation.

    c. Reduce the frequency of operation. ispLSI and pLSI architectures provide flexibility to control clock polarity to potentially reduce the overall clock speed.

3. Where possible, make use of the output slew rate control to reduce the output switching current of the device.

4. Make sure that programmable pull-ups are enabled to drive unused inputs to a proper logic level.

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Package Thermal Resistance

The following tables provide information on the package thermal resistance of Lattice Semiconductor (LSC) commercial and industrial grade devices. For information on the package thermal resistance of LSC military grade devices, please refer to "MIL-M-38510, Appendix C."

Testing was performed per SEMI TEST METHOD G38-87: "Still and Forced-Air Junction-to-Ambient Thermal Resistance Measurements of IC Packages" with devices mounted on a thermal test board conforming to SEMI SPECIFICATION G42-88: "Thermal Test Board Standardization for Measuring Junction-to-Ambient Thermal Resistance of Semiconductor Packages."

Table 1. Package Thermal Resistance for ispLSI and pLSI Products

Package	Pin Count	θ_{JA} 2-Layer Board (Still Air)	θ_{JA} 2-Layer Board (225 lfpm)	θ_{JA} 4-Layer Board (Still Air)	θ_{JA} 4-Layer Board (225 lfpm)	θ_{JC}
PLCC	44-pin	50	42	42.5	35	16
	68-pin	45	37	38	31	13
	84-pin	42	34	36	29	12
JLCC	44-pin	69	—	—	—	4
	68-pin	52	—	—	—	3
PQFP	120-pin	40	32	32	26	11
	128-pin	40	32	32	26	11
	160-pin	33	24	34	20	8
TQFP	44-pin	80	70	65	57	19
	48-pin	80	71	68	58	17
	100-pin	64	53	52	43	22
	128-pin	60	50	51	42	24
	176-pin	45	35	35	28	8
MQFP	160-pin	—	—	20	—	2
	208-pin	—	—	17	—	2
	240-pin	—	—	16	—	2
	304-pin	—	—	14	—	2
CPGA	84-pin	38	—	—	—	3
	133-pin	26	—	—	—	2
	167-pin	25	—	—	—	2

Table 2. Package Thermal Resistance for GAL, ispGAL and ispGDS Products

Package	Pin Count	θ_{JA} 2-Layer Board (Still Air)	θ_{JC}
Plastic DIP	20-pin	67	30
	24-pin	65	25
	28-pin	52	23
PLCC	20-pin	67	25
	28-pin	56	23
SOIC	20-pin	85	18
SSOP	28-pin	105	—
Ceramic DIP	20-pin	62	10
	24-pin	60	10
	28-pin	58	10
LCC	20-pin	65	8
	28-pin	62	7

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