ispLSI® and pLSI® 3160

High Density Programmable Logic

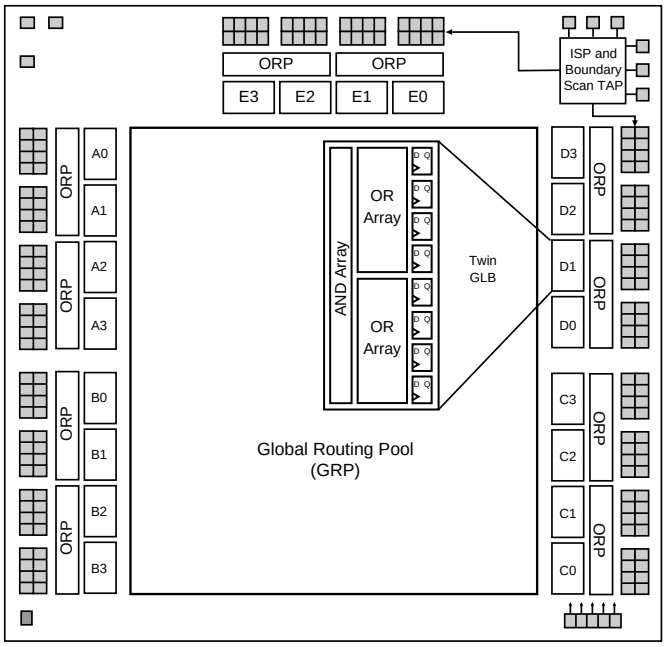
Features

- **HIGH-DENSITY PROGRAMMABLE LOGIC**
  - **— 160 I/O Pins**
  - **— 7000 PLD Gates**
  - **— 320 Registers**
  - **— High Speed Global Interconnect**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— f_{max} = 125 MHz Maximum Operating Frequency**
  - **— t_{pd} = 7.5 ns Propagation Delay**
  - **— TTL Compatible Inputs and Outputs**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile**
  - **— 100% Tested at Time of Manufacture**
  - **— Unused Product Term Shutdown Saves Power**
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - **— 5V In-System Programmability™ (ISP™) using Lattice ISP or Boundary Scan Test (IEEE 1149.1) Protocol**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market, and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Debugging**
- **100% IEEE 1149.1 BOUNDARY SCAN COMPATIBLE**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **— Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **— Five Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Programmable Output Slew Rate Control to Minimize Switching Noise**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispLSI AND pLSI DEVELOPMENT TOOLS**

  pDS® Software
  - **— Easy to Use PC Windows™ Interface**
  - **— Boolean Logic Compiler**
  - **— Manual Partitioning, Automatic Place and Route**

  pDS+™ Software
  - **— Industry Standard, Third-Party Design Environments**
  - **— Schematic Capture, State Machine, HDL**
  - **— Automatic Partitioning and Place and Route**
  - **— Comprehensive Logic and Timing Simulation**
  - **— PC and Workstation Platforms**

Functional Block Diagram



Description

The ispLSI and pLSI 3160 are High-Density Programmable Logic Devices which contain 320 Registers, 160 Universal I/O pins, five Dedicated Clock Input Pins, five Output Routing Pools (ORP), and a Global Routing Pool (GRP) which allows complete inter-connectivity between all of these elements. The ispLSI 3160 features 5-Volt in-system programmability and in-system diagnostic capabilities. The ispLSI 3160 offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 3160 devices.

The basic unit of logic on the ispLSI and pLSI 3160 devices is the Twin Generic Logic Block (Twin GLB™) labelled A0, A1...E3. There are a total of 20 of these Twin GLBs in the ispLSI and pLSI 3160 devices. Each Twin GLB has 24 inputs, a programmable AND array and two OR/Exclusive-OR Arrays, and eight outputs which can be configured to be either combinatorial or registered. All Twin GLB inputs come from the GRP.

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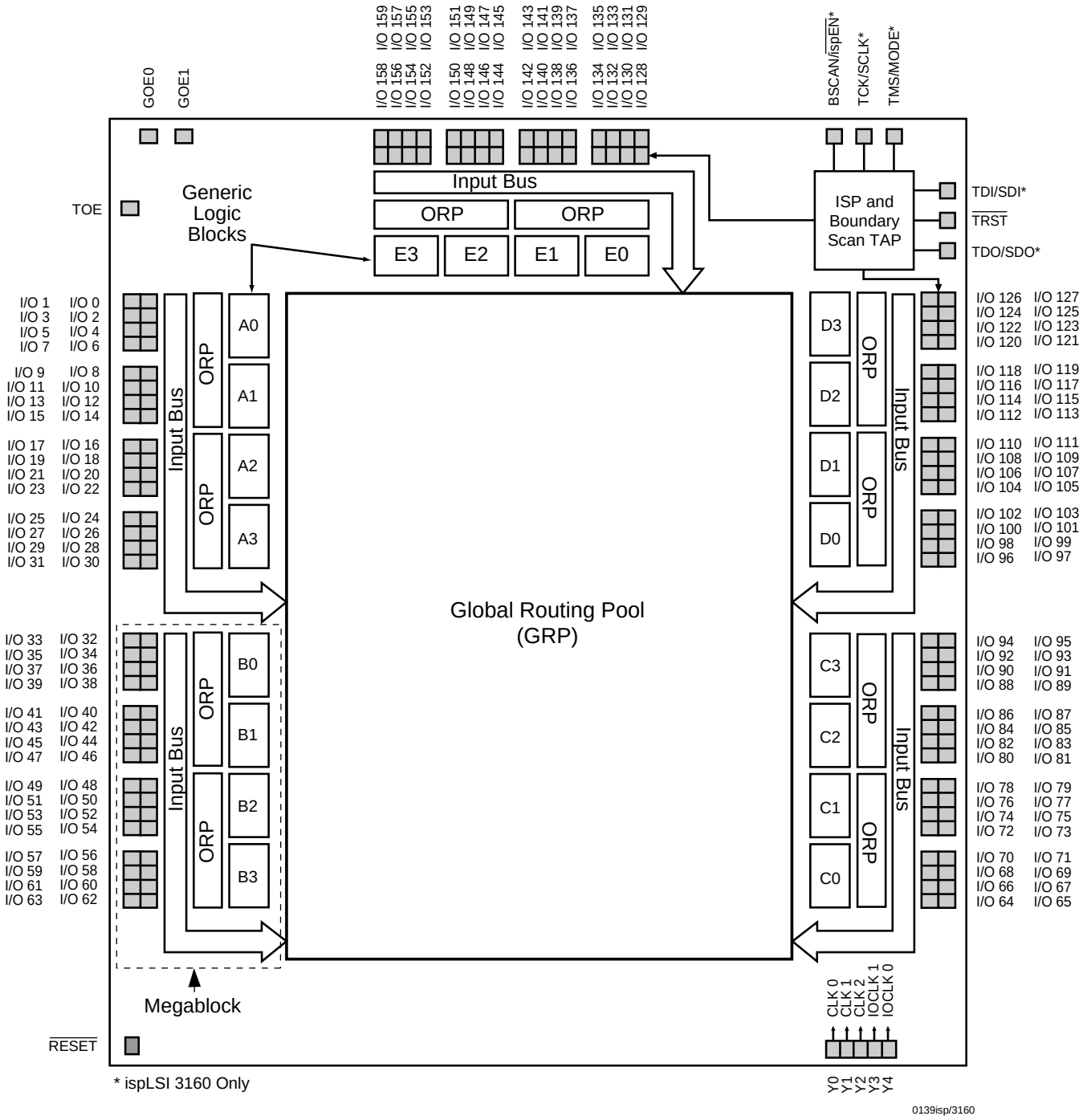
Functional Block Diagram

Figure 1. ispLSI and pLSI 3160 Functional Block Diagram



Description (Continued)

All local logic block outputs are brought back into the GRP so they can be connected to the inputs of any other logic block on the device. The device also has 160 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, a registered input, a latched input, an output or a bidirectional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

The 160 I/O Cells are grouped into ten sets of 16 bits. Pairs of these I/O groups are associated with a logic Megablock through the use of the ORP. Each Megablock is able to provide one Product Term Output Enable (PTOE) signal which is globally distributed to all I/O cells. The PTOE can be generated by any GLB in the Megablock. Each I/O cell can select one of the seven available OEs (two Global OEs and five PTOEs).

Four Twin GLBs, 32 I/O Cells and two ORPs are connected together to make a logic Megablock. The Megablock is defined by the resources that it shares. The outputs of one pair of Twin GLBs are connected to a set of 16 I/O cells by the ORP. The ispLSI and pLSI 3160 device contains five of these Megablocks.

The GRP has as its inputs the outputs from all of the Twin GLBs and all of the inputs from the bidirectional I/O cells. All of these signals are made available to the inputs of the Twin GLBs. Delays through the GRP have been equalized to minimize timing skew and logic glitching.

Clocks in the ispLSI and pLSI 3160 devices are provided through five dedicated clock pins. The five pins provide three clocks to the Twin GLBs and two clocks to the I/O cells.

The table below lists key attributes of the device along with the number of resources available.

An additional feature of the ispLSI and pLSI 3160 is the Boundary Scan capability, which is composed of cells connected between the on-chip system logic and the device's input and output pins. All I/O pins have associated boundary scan registers, with 3-state I/O using three boundary scan registers and inputs using one.

The ispLSI and pLSI 3160 supports all IEEE 1149.1 mandatory instructions, which include BYPASS, EXTEST and SAMPLE.

Key Attributes of the ispLSI and pLSI 3160

Attribute	Quantity
Twin GLBs	20
Registers	320
I/O Pins	160
Global Clocks	5
Global OE	2
Test OE	1

Table 1-0003A/3160

Absolute Maximum Ratings [1]

Supply Voltage V_{CC} .....-0.5 to +7.0V

Input Voltage Applied..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	70	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	V_{CC} +1	V

Table 2-0005/3160

Capacitance (T_A=25°C,f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_1	I/O Capacitance	10	pf	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V
C_2	Clock Capacitance	15	pf	V_{CC} = 5.0V, V_Y = 2.0V

Table 2-0006/3160

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles
pLSI Erase/Reprogram Cycles	100	–	Cycles

Table 2- 0008B

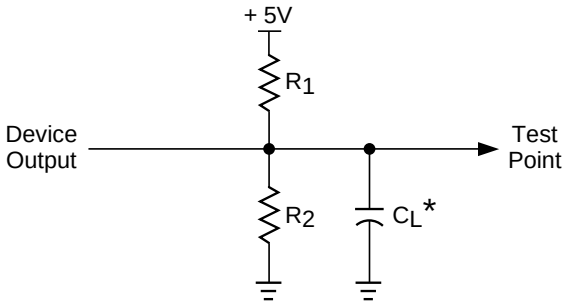
Switching Test Conditions

Input Pulse Levels	GND to 3.0V	
Input Rise and Fall Time 10% to 90%	-125	≤ 2 ns
	Others	≤ 3 ns
Input Timing Reference Levels	1.5V	
Ouput Timing Reference Levels	1.5V	
Output Load	See figure 2	

Table 2-0003/3160

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213A/3160

Output Load conditions (See figure 2)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH} -0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} +0.5V	470Ω	390Ω	5pF

Table 2 - 0004A

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA	2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)	–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}	–	–	10	µA
I_{IL-isp}	Bscan/$\overline{ispEN}$ Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V	–	–	-200	mA
I_{CC}[2,4]	Operating Power Supply Current	V_{IL} = 0.0V, V_{IH} = 3.0V f_{TOGGLE} = 1 MHz	–	275	–	mA

Table 2-0007/3160

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2. Measured using ten 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this datasheet and Thermal Management section of the 1996 Lattice Semiconductor Data Book to estimate maximum I_{CC}.

External Switching Characteristics[1, 2, 3]

Over Recommended Operating Conditions

PARA-METER	TEST[5] COND.	#[2]	DESCRIPTION[1]	-125		-100		-70		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd1	A	1	Data Prop. Delay, 4PT Bypass, ORP Bypass	—	7.5	—	10.0	—	15.0	ns
tpd2	A	2	Data Propagation Delay	—	10.0	—	13.0	—	18.0	ns
fmax	A	3	Clock Frequency with Internal Feedback[3]	125	—	100	—	70.0	—	MHz
fmax (Ext.)	—	4	Clock Freq. with Ext. Feedback,1/(tsu2 + tco1)	95.0	—	87.0	—	50.0	—	MHz
fmax (Tog.)	—	5	Clock Frequency, Max Toggle[4]	125	—	100	—	83.0	—	MHz
tsu1	—	6	GLB Reg. Setup Time before Clock, 4PT bypass	5.0	—	5.5	—	9.0	—	ns
tco1	A	7	GLB Reg. Clock to Output Delay, ORP bypass	—	4.5	—	5.0	—	9.0	ns
th1	—	8	GLB Reg. Hold Time after Clock, 4PT bypass	0.0	—	0.0	—	0.0	—	ns
tsu2	—	9	GLB Reg. Setup Time before Clock	6.0	—	6.5	—	11.0	—	ns
tco2	—	10	GLB Reg. Clock to Output Delay	—	5.0	—	5.5	—	10.0	ns
th2	—	11	GLB Reg. Hold Time after Clock	0.0	—	0.0	—	0.0	—	ns
tr1	A	12	Ext. Reset Pin to Output Delay	—	10.0	—	13.5	—	15.0	ns
trw1	—	13	Ext. Reset Pulse Duration	5.5	—	6.5	—	12.0	—	ns
tptoeen	B	14	Input to Output Enable	—	12.0	—	15.0	—	18.0	ns
tptoedis	C	15	Input to Output Disable	—	12.0	—	15.0	—	18.0	ns
tgoeen	B	16	Global OE Output Enable	—	7.0	—	9.0	—	12.0	ns
tgoedis	C	17	Global OE Output Disable	—	7.0	—	9.0	—	12.0	ns
ttoeen	—	18	Test OE Output Enable	—	8.0	—	12.0	—	15.0	ns
ttoedis	—	19	Test OE Output Disable	—	8.0	—	12.0	—	15.0	ns
twh	—	20	Ext. Sync. Clock Pulse Duration, High	4.0	—	5.0	—	6.0	—	ns
twl	—	21	Ext. Sync. Clock Pulse Duration, Low	4.0	—	5.0	—	6.0	—	ns
tsu3	—	22	I/O Reg. Setup Time before Ext. Sync. Clock (Y3, Y4)	4.0	—	4.5	—	5.0	—	ns
th3	—	23	I/O Reg. Hold Time after Ext. Sync. Clock (Y3, Y4)	0.0	—	0.0	—	0.0	—	ns

1. Unless noted otherwise, all parameters use 20 PTXOR path and ORP.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions section.

Timing Ext.3160.eps

Internal Timing Parameters[1]

Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-125		-100		-70		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs									
tiobp	24	I/O Register Bypass	—	0.8	—	1.3	—	4.0	ns
tiolat	25	I/O Latch Delay	—	4.1	—	4.4	—	7.5	ns
tiosu	26	I/O Register Setup Time before Clock	4.3	—	4.8	—	5.8	—	ns
tioh	27	I/O Register Hold Time after Clock	-1.6	—	-1.6	—	-2.5	—	ns
tioch	28	I/O Register Clock to Out Delay	—	6.0	—	6.7	—	9.4	ns
tior	29	I/O Register Reset to Out Delay	—	5.5	—	5.8	—	8.0	ns
GRP									
tgrp	30	GRP Delay	—	1.8	—	2.3	—	2.6	ns
GLB									
t4ptbp	31	4 Product Term Bypass Path Delay (Comb.)	—	3.1	—	3.1	—	4.2	ns
t4ptbr	32	4 Product Term Bypass Path Delay (Reg.)	—	3.2	—	3.2	—	3.4	ns
t1ptxor	33	1 Product Term/XOR Path Delay	—	3.9	—	4.1	—	4.6	ns
t20ptxor	34	20 Product Term/XOR Path Delay	—	4.0	—	4.0	—	4.5	ns
txoradj	35	XOR Adjacent Path Delay[3]	—	4.3	—	4.3	—	5.3	ns
tgbp	36	GLB Register Bypass Delay	—	0.6	—	1.6	—	1.7	ns
tgsu	37	GLB Register Setup Time before Clock	-0.2	—	-0.2	—	0.9	—	ns
tgh	38	GLB Register Hold Time after Clock	4.6	—	5.6	—	8.0	—	ns
tgco	39	GLB Register Clock to Output Delay	—	1.6	—	0.6	—	2.9	ns
tgro	40	GLB Register Reset to Output Delay	—	4.7	—	5.1	—	5.1	ns
tptre	41	GLB Product Term Reset to Register Delay	—	4.0	—	4.0	—	4.2	ns
tptoe	42	GLB Product Term Output Enable to I/O Cell Delay	—	5.5	—	5.5	—	5.3	ns
tptck	43	GLB Product Term Clock Delay	3.0	3.6	3.0	3.6	3.2	4.0	ns
ORP									
torp	44	ORP Delay	—	1.2	—	1.2	—	1.9	ns
torpbp	45	ORP Bypass Delay	—	0.2	—	0.7	—	0.9	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Timing Int.3160.eps

Internal Timing Parameters[1]

Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-125		-100		-70		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Outputs									
tob	46	Output Buffer Delay	—	1.6	—	2.6	—	3.3	ns
tobs	47	Output Buffer Delay, Slow Slew	—	11.6	—	12.6	—	13.3	ns
toen	48	I/O Cell OE to Output Enabled	—	3.9	—	5.9	—	6.1	ns
todis	49	I/O Cell OE to Output Disabled	—	3.9	—	5.9	—	6.1	ns
Clocks									
tgy0/1/2	50	Clock Delay, Y0 or Y1 or Y2 to Global GLB Clk Line	0.6	1.1	1.1	1.1	1.9	1.9	ns
tioy3/4	51	Clock Delay, Y3 or Y4 to I/O Cell Global Clock Line	0.3	1.6	0.3	1.6	0.8	2.5	ns
Global Reset									
tgr	52	Global Reset to GLB and I/O Registers	—	3.5	—	4.6	—	4.7	ns
tgoe	53	Global OE Pad Buffer	—	3.1	—	3.1	—	5.9	ns
ttoe	54	Test OE Pad Buffer	—	4.1	—	6.1	—	8.9	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

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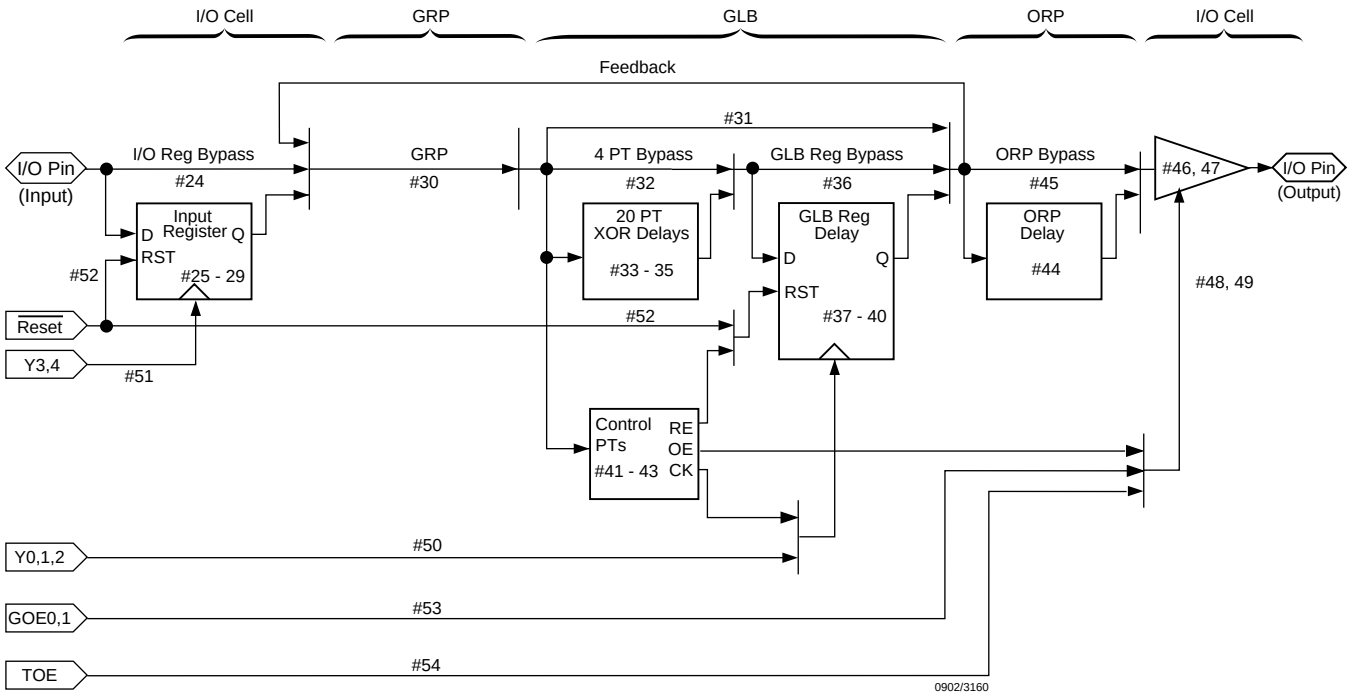
ispLSI and pLSI 3160 Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

tsu	=	Logic + Reg su - Clock (min)
	=	(**t**iobp + **t**grp + **t**20ptxor) + (**t**gsu) - (**t**iobp + **t**grp + **t**ptck(min))
	=	(#24+ #30+ #34) + (#37) - (#24+ #30+ #43)
0.8ns	=	(0.8 + 1.8 + 4.0) + (-0.2) - (0.8 + 1.8 + 3.0)
th	=	Clock (max) + Reg h - Logic
	=	(**t**iobp + **t**grp + **t**ptck(max)) + (**t**gh) - (**t**iobp + **t**grp + **t**20ptxor)
	=	(#24+ #30+ #43) + (#38) - (#24+ #30+ #34)
4.2ns	=	(0.8 + 1.8 + 3.6) + (4.6) - (0.8 + 1.8 + 4.0)
tco	=	Clock (max) + Reg co + Output
	=	(**t**iobp + **t**grp + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
	=	(#24 + #30 + #43) + (#39) + (#44 + #46)
10.1ns	=	(0.8 + 1.8 + 3.6) + (1.1) + (1.2 + 1.6)

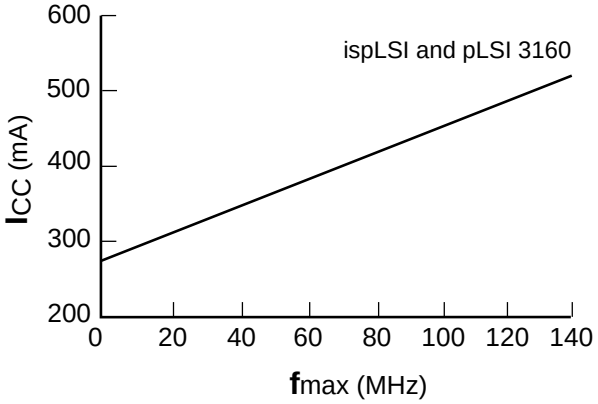
Table 2-0042/3160

Note: Calculations are based upon timing specifications for the ispLSI and pLSI 3160-125L.

Power Consumption

Power Consumption in the ispLSI and pLSI 3160 device depends on two primary factors: the speed at which the device is operating and the number of product terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of ten 16-bit Counters
Typical Current at 5V, 25° C

I_{CC} can be estimated for the ispLSI and pLSI 3160 using the following equation:

I_{CC} = 50 + (# of PTs * 0.73) + (# of nets * Max. freq * 0.0105) where:
# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max. freq = Highest Clock Frequency to the device

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

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In-System Programmability

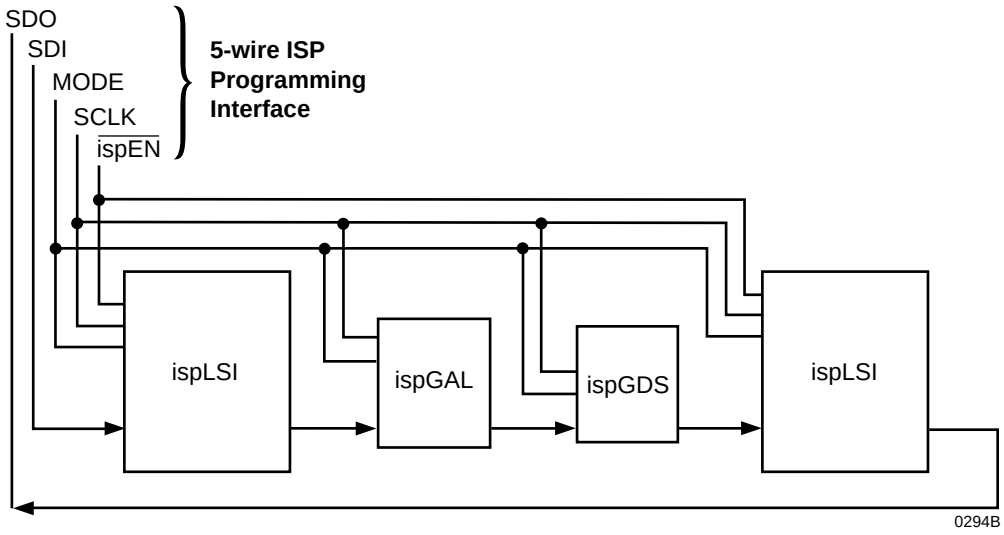
The ispLSI devices are the in-system programmable versions of the Lattice Semiconductor high density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^2CMOS cells will not lose the pattern even when the power is turned off.

The ispLSI 3160 may be programmed using either the Lattice ISP or boundary scan (IEEE 1149.1-compatible) protocols. The programming protocol is determined by the state of the BSCAN/$\overline{\text{ispEN}}$ pin.

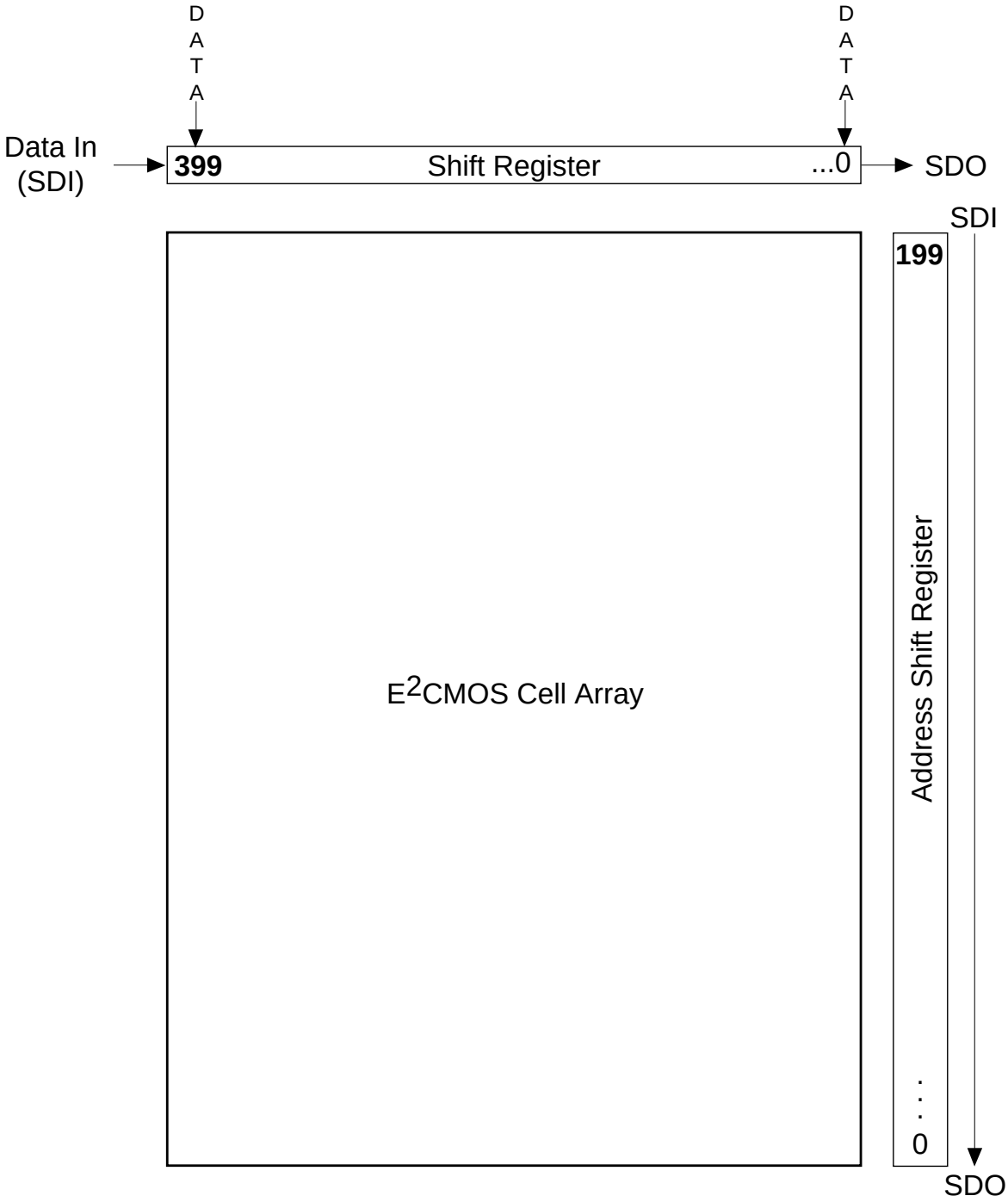
All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The simple signals for interface include isp Enable ($\overline{\text{ispEN}}$), Serial Data In (SDI/TDI), Serial Data Out (SDO/TDO), Serial Clock (SCLK/TCK) and Mode (MODE/TMS) control. Figure 4 illustrates the block diagram of one possible scheme of the programming interface for the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the ISP Architecture and Programming section in the 1996 Lattice Semiconductor Data Book.

The device identifier for the ispLSI 3160 is 0010 0100 (24 hex). This code is the unique device identifier which is generated when a read ID command is performed.

Figure 4. ISP Programming Interface



ispLSI 3160 Shift Register Layout



Note: A logic “1” in the address shift register enables the row for programming or verification. A logic “0” disables it.

0182A/3160

Pin Description

NAME	MQFP PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 5 I/O 6 - I/O 11 I/O 12 - I/O 17 I/O 18 - I/O 23 I/O 24 - I/O 29 I/O 30 - I/O 35 I/O 36 - I/O 41 I/O 42 - I/O 47 I/O 48 - I/O 53 I/O 54 - I/O 59 I/O 60 - I/O 65 I/O 66 - I/O 71 I/O 72 - I/O 77 I/O 78 - I/O 83 I/O 84 - I/O 89 I/O 90 - I/O 95 I/O 96 - I/O 101 I/O 102 - I/O 107 I/O 108 - I/O 113 I/O 114 - I/O 119 I/O 120 - I/O 125 I/O 126 - I/O 131 I/O 132 - I/O 137 I/O 138 - I/O 143 I/O 144 - I/O 149 I/O 150 - I/O 155 I/O 156 - I/O 159	31 32 33 34 35 36 37 38 40 41 43 44 45 46 47 48 49 50 51 52 54 55 56 57 59 60 61 62 63 64 66 67 68 69 70 71 72 73 74 75 82 83 84 85 86 87 88 89 90 91 93 94 95 96 97 98 100 101 102 103 105 106 107 108 109 110 111 112 113 114 116 117 119 120 121 122 123 124 125 126 135 136 137 138 139 140 141 142 144 145 147 148 149 150 151 152 153 154 155 156 158 159 160 161 163 164 165 166 167 168 170 171 172 173 174 175 176 177 178 179 186 187 188 189 190 191 192 193 194 195 197 198 199 200 201 202 204 205 206 207 1 2 3 4 5 6 7 8 9 10 12 13 15 16 17 18 19 20 21 22	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE0 and GOE1 TOE	133 and 134 30	Global Output Enable input pins. Test output enable pin.
$\overline{\text{RESET}}$ Y0, Y1 and Y2 Y3 and Y4	28 132, 130, 129 128, 127	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device. Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the GLBs on the device. Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the I/O cells in the device.
BSCAN/$\overline{\text{ispEN}}$** TDI/SDI* TCK/SCLK* TMS/MODE* $\overline{\text{TRST}}$ TDO/SDO*	27 25 24 23 29 185	Input – Dedicated in-system programming enable input pin. When this pin is high, the BSCAN TAP controller pins TMS, TDI, TDO and TCK are enabled. When this pin is brought low, the isp state machine control pins MODE, SDI, SDO and SLCK are enabled. Note: This pin does not enable the programming mode. Input – This pin performs two functions depending on the state of the BSCAN/$\overline{\text{ispEN}}$ pin. It is the Test Data input to the TAP Controller when the $\overline{\text{ispEN}}$ is logic high. TDI is used to load BSCAN test data or programming data. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the ISP state machine. Input – This pin performs two functions, depending on the state of the BSCAN/$\overline{\text{ispEN}}$ pin. It is the Test Clock input pin when BSCAN/$\overline{\text{ispEN}}$ is logic high. When BSCAN/$\overline{\text{ispEN}}$ is logic low, it functions as the clock for the ISP state machine. Input – This pin performs two functions, depending on the state of the BSCAN/$\overline{\text{ispEN}}$ pin. It is the Test Mode Select input pin when BSCAN/$\overline{\text{ispEN}}$ is logic high. When BSCAN/$\overline{\text{ispEN}}$ is logic low, it functions to control the operation of the ISP state machine. Input – Test Reset, active low to reset the Boundary Scan state machine. Output – This pin performs two functions, depending on the state of the BSCAN/$\overline{\text{ispEN}}$ pin. It is the Test Data Output pin when BSCAN/$\overline{\text{ispEN}}$ is logic high, and either BSCAN test data or programming data is shifted out. When BSCAN/$\overline{\text{ispEN}}$ is logic low, it is the Serial Data Output of the ISP state machine.
GND VCC	11, 26, 42, 53, 65, 78, 92, 104, 115, 131, 146, 157, 169, 183, 196, 208 14, 39, 58, 80, 99, 118, 143, 162, 181, 203	Ground (GND) V_{CC}

* ispLSI 3160 only

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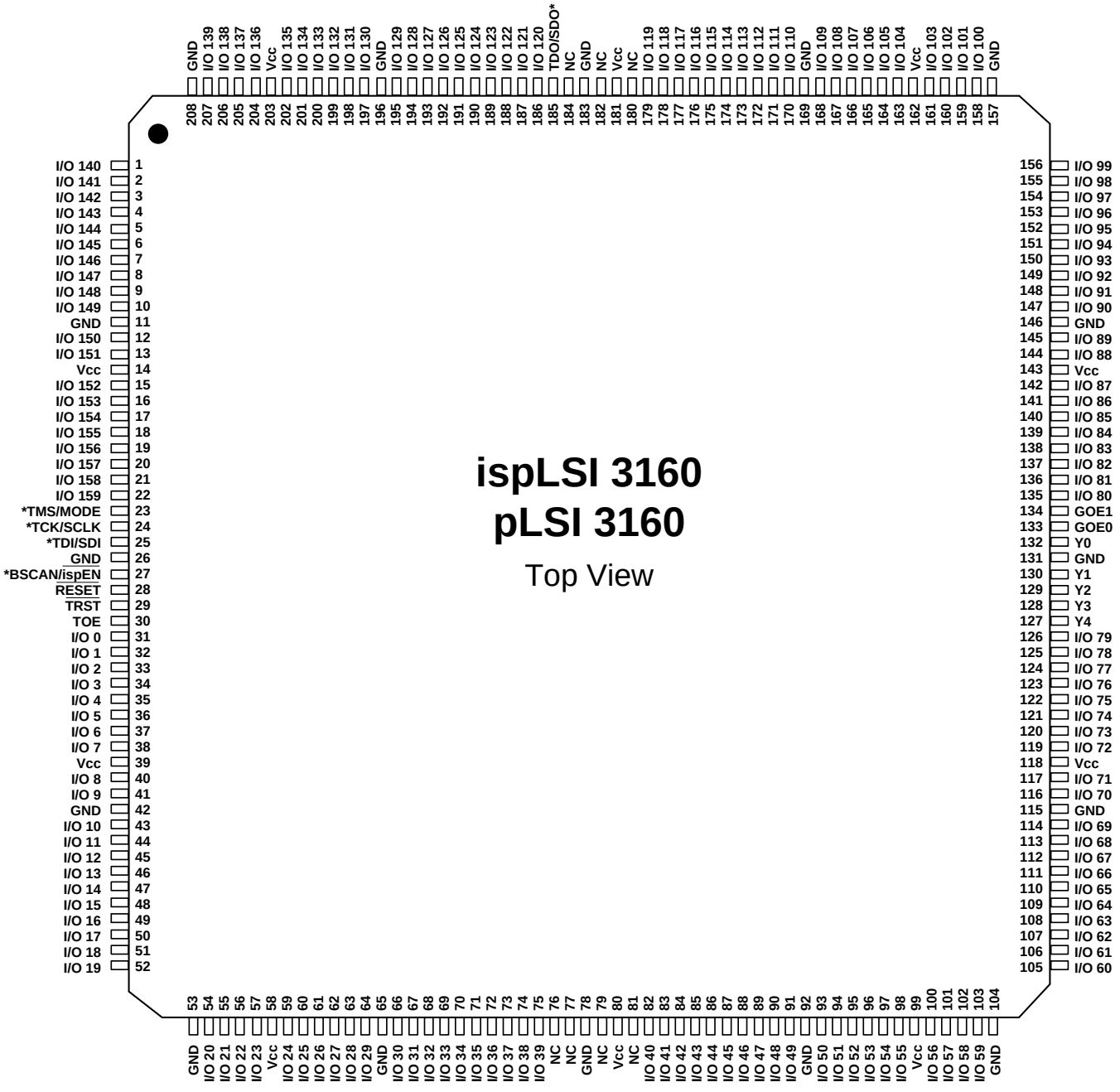
** $\overline{\text{ispEN}}$ for ispLSI 3160 only, NC for pLSI 3160 must be left floating or tied to Vcc, must not be grounded or tied to any other signal.

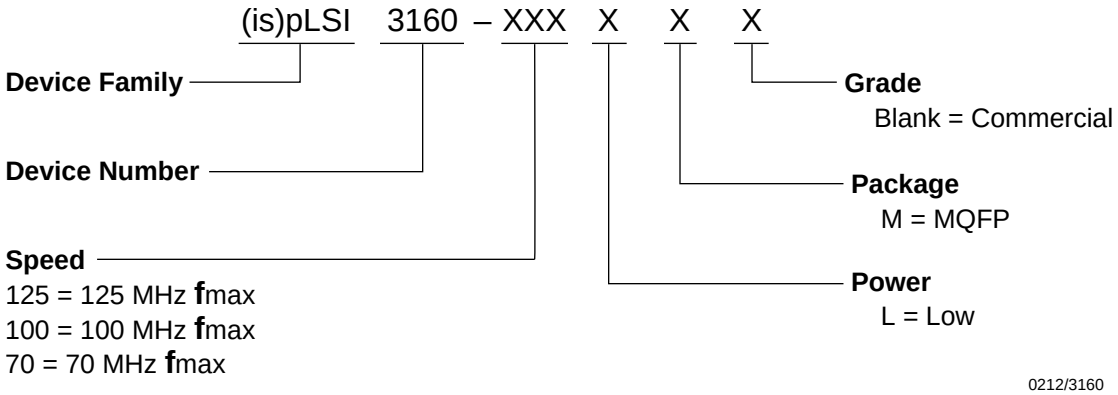
Pin Configuration

ispLSI and pLSI 3160 208-pin MQFP



* Pins have dual function capability for ispLSI 3160 only.

Part Number Description



0212/3160

Ordering Information

Family	fmax	tpd	Ordering Number	Package
ispLSI	125	7.5	ispLSI 3160-125 LM	208-Pin MQFP
	100	10	ispLSI 3160-100LM	208-Pin MQFP
	70	15	ispLSI 3160-70LM	208-Pin MQFP
pLSI	125	7.5	pLSI 3160-125LM	208-Pin MQFP
	100	10	pLSI 3160100LM	208-Pin MQFP
	70	15	pLSI 3160-70LM	208-Pin MQFP

Table 2-0041/3160

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