pDS+™ Synario Software

Features

- **ispLSI® AND pLSI® DEVELOPMENT TOOLS**
  - **— Supports ispLSI and pLSI 1000/E and 2000**
  - **— Upgrade to Support ispLSI and pLSI 3000**
  - **— Supports Lattice Semiconductor ispGAL® and GAL® Design-In**
- **DESIGN ENTRY USING DATA I/O'S SYNARIO**
  - **— ABEL-HDL Entry**
  - **— Schematic Capture**
  - **— Tightly Integrated User Interface**
- **LATTICE SEMICONDUCTOR pDS+™ SYNARIO FITTER**
  - **— Multi-Level Logic Synthesis**
  - **— Efficient Design Optimization and Minimization**
  - **— Automatic Mapping and Device Fitting**
  - **— Automatic Partitioning with High Utilization**
  - **— Predictable Performance**
- **INDUSTRY STANDARD PROGRAMMING FILE GENERATION**
  - **— Standard JEDEC Device Fuse Map**
- **IN-SYSTEM PROGRAMMING**
  - **— ispCODE™ C Source Routines Included**
  - **— ISP Daisy Chain Download**
  - **— ispATE™ Board Test Programming Utility**
- **PLATFORMS SUPPORTED**
  - **— PC Windows 3.1x, Windows 95 and Windows NT**

Introduction

pDS+ Synario software from Lattice Semiconductor offers a powerful logic design solution for Lattice Semiconductor's ispLSI and pLSI families of high density PLDs. The ISP Synario System, ISP Synario-Entry and ISP Synario-Simulate software products support Lattice Semiconductor's ispLSI and pLSI 1000, 2000 and 3000 high density families, as well as its ispGAL and GAL devices. Coupling these powerful tools with Lattice Semiconductor's pDS+ Synario Fitter provides tightly integrated front-to-back design capability.

The complete ISP Synario System supports smaller ispLSI and pLSI high density devices (including all 1000/E and 2000/V device families), ispGAL and GAL devices with complete schematic or language design entry, fitting and functional simulation. Lattice Semiconductor's pDS+ Synario software offers multi-level design synthesis, automatic place and route and efficient device utilization, delivering high performance, even for more complex designs.

ISP Synario System

The Lattice Semiconductor ISP Synario System contains everything needed to design and program with Lattice Semiconductor ispLSI devices. The full version of Data I/O's Synario-Entry tools for schematic capture and ABEL-HDL language logic design, a functional simulator and Data I/O's Project Navigator for easy design and logic debugging are included. The ISP Synario System supports high density design for Lattice Semiconductor's ispLSI and pLSI 1000, 1000E, 2000 and 2000V/LV devices. The tools included also support the full range of Lattice Semiconductor's industry standard ispGAL and GAL devices, including the ispGAL22V10, GAL16V8, GAL20V8 and GAL6001 devices, and others. In addition, the ISP Synario System includes device samples of the ispLSI 2032, isp GAL22V10 and ispGDS™, as well as an ispDOWNLOAD™ Cable to download designs to the PC board.

Project Navigator

Data I/O's Synario Project Navigator contains detailed, built-in knowledge of the Lattice Semiconductor design flow. The Project Navigator knows the processing status of all portions of the design. If the design is changed and the netlist regenerated, Project Navigator changes only the necessary items, since it knows that other parts of the design are current. Processing options are intelligently defaulted and detailed device-specific help is available for each step.

ISP Synario-Entry

All of Data I/O's Synario products are Windows-based and easy to use. For example, highlight a net and the net is highlighted throughout the design hierarchy. Run a rules check and errors appear in a box. Click on an error and the system jumps to the schematic or text containing the error. The ISP Synario-Entry tool is designed to allow you to describe even the most complex designs using familiar language constructs or by capturing the logic schematic using a library of Data I/O logic primitives. Synario Behavioral Entry with hierarchical support also

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Figure 1. Synario Design Interface

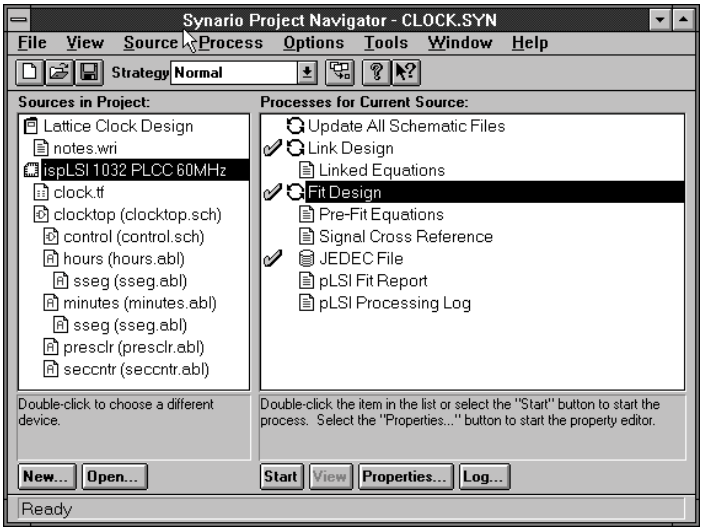
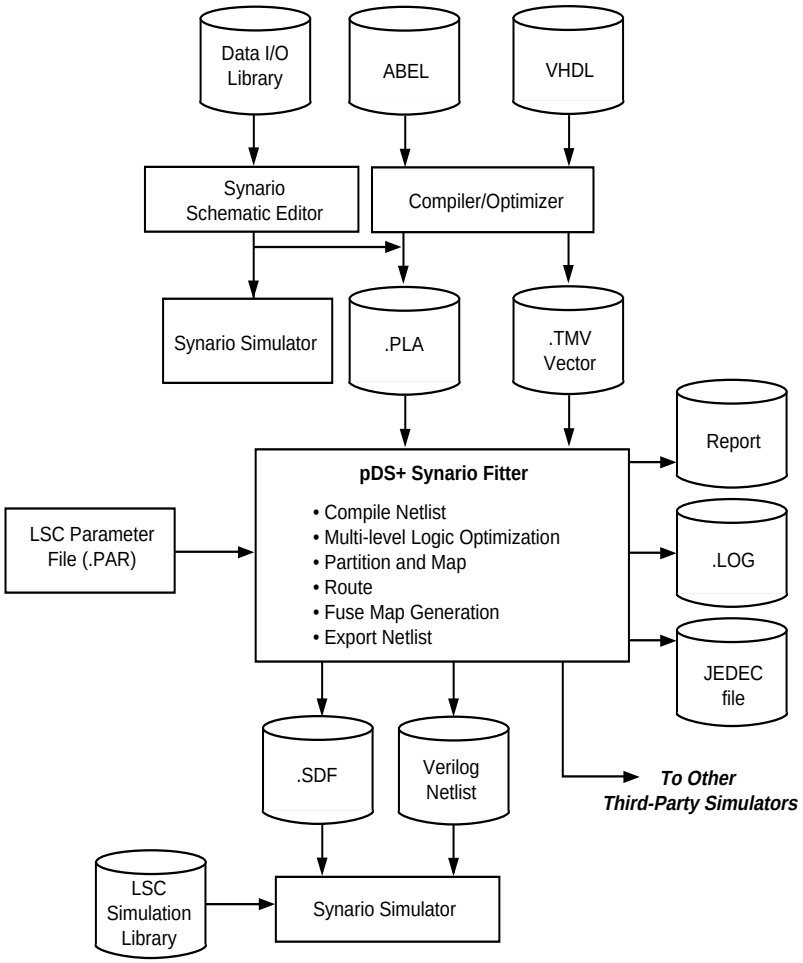


Figure 2. Lattice Semiconductor pDS+ Synario Design Flow



allows device-specific logic synthesis compatible with ABEL-HDL for easy retargeting of existing low density designs to high density Lattice Semiconductor ispLSI and pLSI architectures. Commonly referred to as Syn-Entry, a Lattice Semiconductor-only version of this tool – ISP Synario-Entry – is available directly from Lattice Semiconductor.

ISP Synario-Simulate

Data I/O's Synario-Simulator uses Synario source files to complete functional simulations quickly. After pDS+ Synario completes the fitting task, a compatible netlist and standard delay format (SDF) file are created for full delay-annotated timing simulations. The waveform viewer allows the user to display waveforms in a logic analyzer-like format. The Simulator's waveform viewer and the schematic communicate with one another. Once a simulation has run, the values beneath the cursor are displayed on the associated schematic nets. Simulation results are tied back to the source file when possible to save interpretation time and speed the debug process. Just like ISP Synario-Entry, a Lattice Semiconductor-only version of ISP Synario-Simulate is also available.

pDS+ Synario Fitter

Lattice Semiconductor's pDS+ Synario Fitter for ispLSI and pLSI devices is tightly integrated within the Synario environment and the Project Navigator, using the PLA output from Synario as input. The Lattice Semiconductor Fitter provides hands-off design implementation through an intelligent multi-level synthesis algorithm, logic partitioning, automatic place and route and standard JEDEC fuse map generation for device programming. Timing simulation input files for the Synario simulator are generated by the Fitter and can be coupled with Lattice Semiconductor's Synario Simulation Library by the user as needed.

Design Optimization & Logic Minimization

The pDS+ Synario Fitter uses proprietary algorithms targeted for Lattice Semiconductor's powerful device-specific architectural features. The Fitter optimizes the design thoroughly, using logic minimization, product term sharing and XOR functions wherever possible. In addition, the pDS+ Synario Fitter supports multiple fitting strategies to obtain the best device utilization and performance.

Design Parameter Control

The pDS+ Synario Fitter offers extensive design control at the design entry level, letting the user optimize the design for maximum utilization and/or speed. All of the controls are specified using "attributes" in the design property and parameter files. These controls fall into two categories:

- — Fitter Controls
- — Design Implementation Controls
  - — Net Attributes
  - — Pin Attributes
  - — Path Attributes
  - — Symbol Attributes

Fitter Control Options

Special properties can be passed to the pDS+Synario Fitter providing complete control over critical design considerations. Fitter control over design partitioning and routing optimizes the design for speed and/or device utilization.

Feature	Description
PART	Determines device type to be used.
PARAM_FILE	Allows user to specify attributes in a text file.
STRATEGY	Choice of AREA (default), DELAY or NO_OPTIMIZE. AREA optimizes device space, DELAY keeps GLB levels to a minimum and NO_OPTIMIZE does not reduce equations.
USE_GLOBAL_RESET	Causes global reset to use dedicated routing for reset.
MAX_GLB_OUT	Specifies maximum number of outputs from a GLB. Default is 4.
MAX_GLB_IN	Controls maximum number of inputs to a GLB. Default is 16 for 1K and 2K devices and 24 for 3K devices.
EFFORT	Controls optimization of partitioner.
EXTENDED_ROUTE	Choice of OFF (fixed) or ON (extended, default).
PIN_FILE	Specifies locked pin assignments.

Design Implementation Controls

Device controls are used for changing design parameters such as security. Some of these implementation controls are:

Feature	Description
ISP	Instructs Router to reserve in-system programming pins.
ISP_EXCEPT_Y2	Reserves all ISP pins except Y2 (ispLSI and pLSI 1016/E and 2032 only).
Y1_AS_RESET	Uses Y1 clock pin on ispLSI and pLSI 1016/E and 2032 as a global reset pin.
SECURITY	Sets the device security cell to prevent unauthorized fuse map read back.

Net Attributes

These properties control how the design is mapped into the specified features of the target device:

Feature	Description
CLK0-CLK2	Assigns a CLK signal to a dedicated CLK line.
IOCLK0-IOCLK1	Assigns a CLK signal to a dedicated IOCLK line if single fanout input pin.
FASTCLK	Fitter assigns CLK signal to CLK0-CLK2 or IOCLK0-IOCLK1.
SLOWCLK	Assigns the CLK signal to a GLB product term CLK.
PRESERVE	Prevents logic minimization on specified nets.
GROUP	Suggests grouping of functions in a GLB.

Pin Attributes

Feature	Description
CRIT	Specifies Output Routing Pool Bypass to minimize delay.
SLOWSLEW	Assigns slow slew rate on a specific I/O cell.
LOCK	Assigns device I/O pins to design I/O ports.
PULLUP	Specifies internal pull-up resistors.

Path Attributes

The following properties specify paths in the design that have special fitting requirements:

Feature	Description
SAP/EAP	Defines asynchronous paths to prevent signal duplication.
SCP/ECP	Defines critical paths to reduce delays.
SNP/ENP	Defines logic paths for no logic minimization.

Symbol Attributes

Feature	Description
REGTYPE	Determines where a register is to be placed (IOC or GLB).
PROTECT	Prevents removal of a primitive or a macro during minimization.
OPTIMIZE	Selects either hard or soft macros.

Parameter File

The pDS+ Synario Fitter provides the ability to use a parameter file (design.par) feature which helps designers eliminiate guesswork and optimize the designs for the right devices. It allows the user to try a number of design implementation options using all of the fitter control options in a batch mode. The parameter file instructs the partitioner and the router to maximize both device utilization and performance.

Property File

The pDS+ Synario Fitter provides the ability to use a property file (design.prp) feature which allows the designer to control the fitter using all of the design attributes available. The property file helps guide the fitter in implementing the design in the best way.

Design Verification

The pDS+ Synario Fitter provides a post route design file for optional timing simulation. The pDS+ Synario software offers complete post route design verification using optional timing simulators. The pDS+ Synario Fitter generates the files required for third-party simulation, and generates a "sim" file which can be used for simulation with behavioral simulation models from Synopsys' Logic Modeling Division.

Fuse Map Generation

pDS+ Synario software generates a device fuse map in standard JEDEC format. A security feature offers protection of proprietary designs from unauthorized duplication. The Fitter appends any design test vectors in JEDEC format to the device fusemap, facilitating a quick, easy functional verification of a programmed device.

System Requirements (PC Platform)

- 486/Pentium™ IBM Compatible PC
- Operating System
  - MSDOS Version 4.x or Later
  - Windows 3.1x
  - Windows NT
  - Windows 95
- 16 MB RAM with 30MB Hard Disk Space
- ABEL 4.1 or Later
- Parallel Printer Port for Software Key

Programmer Support

All devices in the ispLSI device families can be programmed while installed on the target circuit board. In-system programming can be performed using an ispDOWNLOAD™ Cable and PC, by an on-board microprocessor or by ATE systems during final board test.

All ispLSI and pLSI devices can also be programmed using third-party PLD programmers. The devices are currently supported by programmers from the following vendors:

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30A/B
System General	TURPRO-1/FX

High pin-count adapters are available from Emulation Technology, EDI Corporation and PROCON.

Product Ordering Information

Product Code	Description
pDS2120-PC1	pDS+ Synario Fitter (Includes Synario Interface Kit**)
pDS2120-3UP/PC1	pDS2120 3000 Family Upgrade
pDS1120-PC1	Synario Interface Kit**
pDS1401-PC1	ISP Synario-Entry
pDS3402-PC1	ISP Synario-Simulate
ISP-SYN2	ISP Synario System

Annual Maintenance*

pDS2120M-PC1	Maintenance for pDS2120-PC1
pDS1120M-PC1	Maintenance for pDS1120-PC1
pDS1401M-PC1	Maintenance for pDS1401-PC1
pDS3402M-PC1	Maintenance for pDS3402-PC1

*One year of maintenance is provided with every product purchase.

** Includes SYN-pLSI (Device Kit)

Warranty/Update Service

- 90-day warranty on disk media
- One-year maintenance support included with purchase
- Annual maintenance agreement available

Technical Support Assistance

Hotline:	1-800-LATTICE (Domestic) 1-408-428-6414 (International)
BBS:	1-408-428-6417
FAX:	1-408-944-8450
email:	apps@latticesemi.com

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