Implementing Lattice ISP™ and Boundary Scan Daisy Chains

Introduction

Over the last several years, the PLD industry has come to realize the importance of Lattice In-System Programmability (ISP). As other PLD vendors scramble to get silicon to market, Lattice Semiconductor Corporation (LSC) continues to provide a comprehensive ISP solution of silicon, software, documentation and applications support, referred to as "TOTAL ISP." All of Lattice's ISP devices are programmable over the entire commercial Vcc and temperature ranges (see Table 1). Stand-alone device programming is eliminated with Lattice ISP, which minimizes device handling and allows the use of the new TQFP packages with their fragile leads. Lattice guarantees 10,000 programming cycles on every ISP device, while most competitive solutions guarantee only 100. In addition to Lattice's ISP devices, LSC offers programming software for PC, ATE and embedded processors. Individual devices may be programmed using any of these tools, or multiple devices may be linked together in a serial daisy chain, simplifying the hardware interface. Lattice has been using daisy-chain programming for several years through it's proprietary ISP interface that programs multiple devices in seconds. The basic elements of this interface include mode control (MODE), serial data in (SDI), serial data out (SDO), and serial clock (SCLK) signals as well as a proprietary three-state programming state machine called the Lattice ISP state machine.

Boundary-scan is an emerging trend in board level test, offering lower test and manufacturing costs. The interface for boundary-scan testing includes the Test Data Input (TDI), Test Data Output (TDO), Test Clock (TCK), and Test Mode Select (TMS) signals as well as an integrated state machine called the Test Access Port (TAP) controller. As more manufacturers employ this technology for testing, the ability to use ISP through the boundary-scan TAP will become increasingly important to system design and manufacturing.

Table 1. Features of the Lattice ISP Device Families

	ispGDS, ispGAL22V10	ispLSI 1000/E and 2000 Families	ispLSI 3256	ispLSI 3000/A/E (except 3256) and 6000 Families	ispLSI 2000LV Family
LSC ISP State Machine for Programming	Yes	Yes	Yes	Yes	No
Boundary-Scan TAP Controller State Machine for Programming	No	No	No (use 3256A for Boundary Scan TAP Programming)	Yes	Yes
Boundary-Scan Test Operations Supported through the TAP Controller	No	No	Yes	Yes	No
Programming Signals	Lattice ISP	Lattice ISP	Lattice ISP/TAP	Lattice ISP/TAP	TAP
Command Shift Register Length	5 bits	5 bits	5 bits (Lattice ISP), 2 bits (TAP)	5 bits	5 bits
FLOWTHRU Instruction	Yes	Yes	Yes	Yes	Yes
$\overline{\text{ispEN}}$ Signal	No	Yes	Yes	Yes	Yes
Address and Data Shift Registers	Address and data shifted in one command.	Different shift instructions for address and data.	Different shift instructions for address and data.	Different shift instructions for address and data.	Different shift instructions for address and data.
Device ID	8-bit Lattice ISP	8-bit Lattice ISP	8-bit Lattice ISP	8-bit Lattice ISP	32-bit BSCAN TAP ID

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While most Lattice ISP devices program through the ISP state machine, Lattice has also become an ISP pioneer through the boundary-scan TAP. Several new families of Lattice ISP devices support the IEEE Standard 1149.1 specified TAP controller for boundary-scan test operations, In-System Programming or both. The goal of this application note is to explain how to implement ISP in new hardware designs that incorporate mixed combinations of ISP and boundary-scan devices.

Lattice ISP Overview for Daisy Chain

Similarities/Differences

For the purpose of cascading, Lattice ISP devices can be categorized into five device groups: ispGDS™ and ispGAL®22V10B/C; ispLSI® 1000/E and ispLSI 2000 families; ispLSI 3256; ispLSI 3000 (except ispLSI 3256) and ispLSI 6000 families; and the ispLSI 2000LV family of devices. Table 1 summarizes the features of these device groups.

The ispGDS and ispGAL22V10 devices use only the ISP state machine for programming. The I/Os of ispGDS and ispGAL22V10 devices are put into a high impedance state when the programming state machine goes into the Command Shift State. The ispGDS and ispGAL devices do not use a dedicated $\overline{\text{ispEN}}$ pin for this function.

The ispLSI 1000/E and ispLSI 2000 families of devices are programmed exclusively through the ISP state machine but also use a dedicated $\overline{\text{ispEN}}$ pin to enable the programming mode: by driving $\overline{\text{ispEN}}$ low, all of the device I/Os are put into a high-impedance state and the programming functions for SDI, SDO, MODE and SCLK are enabled.

The ispLSI 3256 is programmed through the ISP state machine but also is boundary-scan compliant for testing. A dedicated $\overline{\text{ispEN}}$ pin selects between the ISP state machine and the TAP controller. By driving $\overline{\text{ispEN}}$ low, all of the device I/Os are put into the high-impedance state and the programming functions for SDI, SDO, MODE and SCLK are enabled. When $\overline{\text{ispEN}}$ is high, the TAP controller is active and the functions for TDI, TDO, TMS and TCK are enabled.

The ispLSI 3000 (except the ispLSI 3256) and ispLSI 6000 families are programmable through either the ISP state machine or the boundary-scan TAP controller. By driving $\overline{\text{ispEN}}$ low, the device I/Os are put into the high-impedance state, the programming functions for SDI, SDO, MODE and SCLK are enabled and the device enters the programming mode. When $\overline{\text{ispEN}}$ is high, the TAP controller is active and the functions for TDI, TDO, TMS and TCK are enabled. With the TAP controller active, the device I/Os can also be put into the high-impedance state by loading and executing the Program Enable (ProgEN) instruction. To put the devices into the programming mode, the ProgEN instruction is loaded and executed three times in succession. When the TAP controller is active, boundary-scan test operations are available for the ispLSI 3000 and ispLSI 6000 families of devices.

The ispLSI 2000LV family of devices is programmed exclusively through the boundary-scan TAP controller. A dedicated $\overline{\text{ispEN}}$ pin multiplexes the functionality of the programming pins. When $\overline{\text{ispEN}}$ is held low, the TAP controller is active and the functions for TDI, TDO, TMS and TCK are enabled. The device enters the programming mode after the Program Enable instruction is loaded and executed three times in succession. Device I/Os go to the high-impedance state after the first ProgEN instruction is loaded.

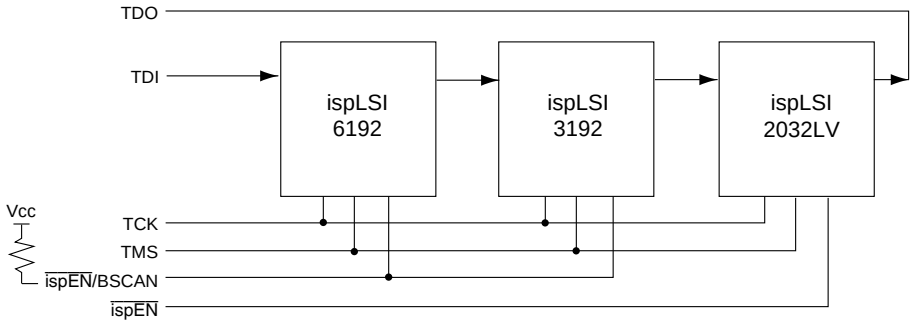
If devices that use the same state machine for programming are put in a serial daisy chain, it is possible to program multiple ISP devices by operating each of the device state machines in parallel. This synchronizes all the devices within the daisy chain to a known state. However, having all ISP devices in the same state does not mean that all devices are executing the same instruction. The ability of each device in the daisy chain to execute a different instruction makes it possible to selectively program one or multiple ISP devices at a time.

The internal device layout is the same for all ispLSI devices regardless of state machine interface used for programming. The ispLSI devices have separate address and data shift commands. The row(s) are selected by the address that is shifted-in prior to each programming command. The data can then be shifted with the "data shift" instruction. With ispGDS and ispGAL devices, both address and data are shifted-in with a single shift command (the address is part of the Data shift register). When executing commands that only require a row address, a dummy data stream or no data can be shifted in place of the data stream.

Mixed ISP and Boundary-Scan Systems

This section describes the hardware interface required when Lattice ISP devices are mixed with boundary-scan testable devices and boundary-scan TAP ISP programmable devices on the same board. Following the few simple procedures listed below will result in first time

Figure 1. Configuration for Programming and Boundary-Scan Test Operations for ispLSI 3000 Family (Except 3256), ispLSI 6000 Family and ispLSI 2000LV Family Devices on the Same Board.



success for programming ISP devices. Described here are the most typical configurations for system designs based on common ISP and testability goals.

In general, most of the signals from the Lattice ISP interface can be common with corresponding boundary-scan TAP ISP interface signals. This usually includes some or all of SDI and TDI, MODE and TMS, SDO and TDO, and SCLK and TCK. If a parallel programming configuration is used, where the boundary-scan and non-boundary-scan devices are in two separate chains both fed by SDI/TDI, and combining SDO/TDO at the end of the chains, the $\overline{\text{ispEN}}$ (ISP) and $\overline{\text{TRST}}$ (TAP) pins can be used to select which chain is active. For ispLSI devices, the $\overline{\text{ispEN}}$ pin can be used to select the devices for programming. When the devices are de-selected, the programming pins are in the high impedance state and will not affect the programming of active devices. Many boundary-scan devices include the optional $\overline{\text{TRST}}$ pin which holds the TAP controller in the Test-Logic-Reset state. For boundary-scan devices held in the Test-Logic-Reset state, the TDO pin will be in the high-impedance state and programming of the non-boundary-scan daisy chain will not be affected. This type of configuration requires that the ISP programming pins cannot be used for normal mode functions.

Systems using 3.3V ISP devices should use the ispDOWNLOAD™ cable. The cable operates with either a 3.3V or 5V VCC source. Lattice's Daisy Chain Download software makes the ISP software interface to 3.3V and mixed-voltage systems transparent to the user.

Boundary-scan devices, such as the ispLSI 3000 and 6000 families, can be put into a boundary-scan serial daisy chain for test and programming purposes. The configuration choice for the devices depends on the boundary-scan test operations needed, programming requirements and device combinations. For both boundary-scan test operations and programming through the boundary-scan TAP, the ispLSI 3000 family (except the ispLSI 3256) and the ispLSI 6000 family may be put in any order in a chain of boundary-scan devices. Boundary-scan test operations are available for the ispLSI 3256 through the boundary-scan TAP but programming is done through the ISP state machine (Note: Lattice has introduced the 3256A device which replaces the 3256 and supports boundary-scan TAP programming). Programming operations are conducted through the boundary-scan TAP for the ispLSI 2000LV family as well and they may also be put in any order within a boundary-scan chain.

A boundary-scan chain of devices is shown in Figure 1. In this configuration the $\overline{\text{ispEN}}$/BSCAN pin on the ispLSI 3192 and ispLSI 6192 devices is pulled up to Vcc either with the internal active pull-up or externally hardwired to Vcc through a 10 kΩ resistor. The $\overline{\text{ispEN}}$ pin on the ispLSI 2032LV is driven high for normal operations and driven low for boundary-scan programming operations. The ispDOWNLOAD cable connection to the $\overline{\text{ispEN}}$/BSCAN pin of the ispLSI 2032LV takes care of this operation.

The ispLSI 3256 may also be put into a serial daisy chain with other boundary-scan devices for test operations. However, since programming of the ispLSI 3256 is done through the ISP state machine, if in-system programming is required, the daisy chain must be altered to allow LSC ISP state machine operation independent of the boundary-scan operations.

Figure 2 shows a possible programming configuration that allows in-system programming of ispLSI 3256 devices in the same daisy chain as other boundary-scan devices that only use the TAP controller state machine. This configuration makes use of the optional boundary-

Figure 2. Boundary-Scan Test Daisy Chain Configuration Supporting Programming Through Both the ISP State Machine and the TAP Controller State Machine.

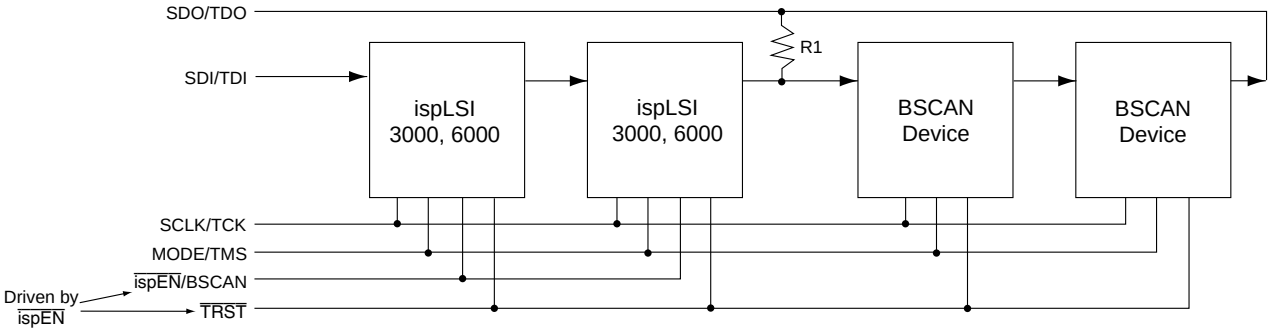
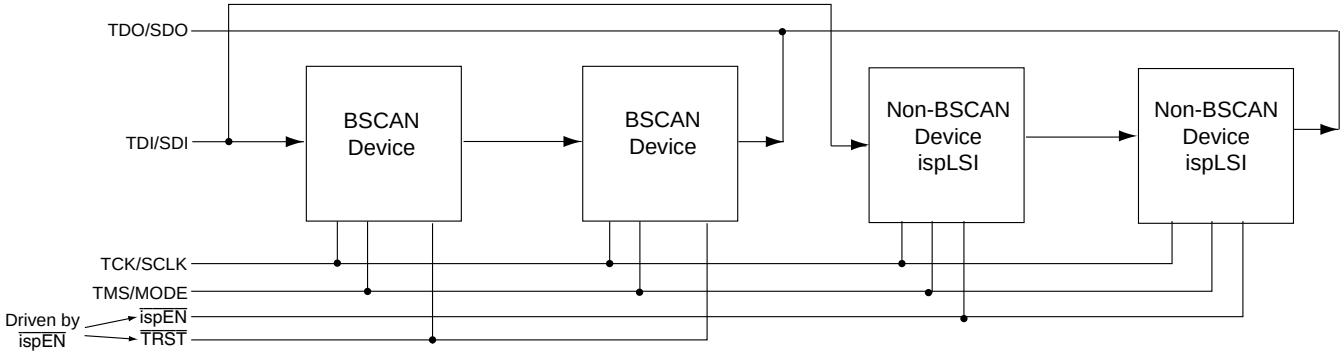


Figure 3. Parallel Programming Loops for Programming Boundary-Scan and LSC ISP Devices on the Same Board.



scan pin $\overline{\text{TRST}}$ that holds the TAP controller state machine in the Test-Logic-Reset state to split up the chain and allow ISP state machine operation in the first part of the chain. When $\overline{\text{TRST}}$ and $\overline{\text{ispEN}}$/BSCAN are held low, the TDO pin for the boundary-scan only devices will be in the high-impedance state and the SDO output of the last ispLSI 3256 device in the chain will drive back to the programmer through resistor R1. This will allow programming through the LSC ISP state machine with $\overline{\text{ispEN}}$/BSCAN held low for the ispLSI 3256 devices in the chain without affecting the boundary-scan only devices. When $\overline{\text{TRST}}$ and $\overline{\text{ispEN}}$/BSCAN are both high, boundary-scan test operations will be available for the entire chain of devices. In this configuration, other ispLSI 3000 and 6000 devices can be put in either part of the chain but must have $\overline{\text{ispEN}}$/BSCAN tied to Vcc if they are in the BSCAN part of the chain.

If LSC ISP programmable devices such as the ispLSI 1000/E and 2000 families will be put on the same board as boundary-scan devices, parallel daisy chain loops are required for successful in-system programming and boundary-scan operations. Figure 3 shows a sample configuration using parallel programming loops. This programming configuration again makes use of the $\overline{\text{TRST}}$ pin to hold the boundary-scan devices in the Test-Logic-Reset state while programming the ISP loop. When programming this configuration with ispDOWNLOAD software, the software automatically takes care of tri-stating the TDO of the boundary-scan devices. In this case, the $\overline{\text{TRST}}$ connection is optional. For boundary-scan operations the $\overline{\text{ispEN}}$ pin is pulled high to de-select the ISP programming loop. The advantage of this configuration is the ability to use one connector for both boundary-scan testing procedures and ISP programming operations.

The boundary-scan daisy chain can include any combination of ispLSI 2000LV, 3000 or 6000 family devices for ISP programming operations (Figure 3). If boundary-scan test and programming operations are required with ispLSI 3256 devices, simply replace the BSCAN devices in Figure 3 with the daisy chain configuration in Figure 2. For both the configurations in Figures 2 and 3, an alternative to controlling the $\overline{\text{TRST}}$ pin is to multiplex the MODE/TMS signal to isolate the two daisy chains.

Summary

Lattice continues to lead the way in In-System Programmable solutions. Not only has Lattice expanded its ISP coverage to include the TAP controller state machine, it has provided the software tools to support the transparent use of either the standard ISP state machine or the TAP controller state machine in the same daisy chain. With many ISP devices already in production, years of experience and easy-to-use software, Lattice is clearly the only choice for ISP.

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