E^2CMOS Testability Improves Quality

Introduction

The inherent testability of Lattice Semiconductor's E^2CMOS PLDs significantly improves their quality and reliability. By using electrically erasable EEPROM technology to produce GAL, pLSI and ispLSI devices, Lattice Semiconductor Corporation (LSC) is able to perform 100% AC/DC, functional, and parametric testing of every single device. In order to achieve the highest quality levels, LSC programs and tests each device repeatedly throughout the manufacturing process.

Actual Test vs. Simulated Test

Why is "actual test" so significant? PLDs, unlike most other semiconductor devices, have a programmable element that determines the final device functionality and AC/DC performance. These programmable elements can be fabricated from metal link fuses, programmable diodes or transistors, volatile static RAM cells, UV EPROM cells or electrically erasable EEPROM cells. Each of these technologies carries a different variability of programming success and a variance in the impact of the programming success on the performance and reliability of the device.

The most common programmable elements are the metal fuse, EPROM cell and EEPROM cell. Of these element types, only the EEPROM cell can be thoroughly tested by the manufacturer prior to shipment to an end user OEM.

EEPROM Allows Actual Test

Each of the technologies identified above can be programmed. In this manner they are all the same. The differences become apparent when the erase times are analyzed. Metal link and One-Time Programmable (OTP) devices cannot be erased. UV EPROM devices can be erased, however the time required is 20-30 minutes (in an expensive windowed package). EEPROM devices, on the other hand, offer instant erasability on the order of 50 ms (thousandth's of a second). The advantage of this instant erase for manufacturing test is significant. Instant erase allows instant re-patterning for additional testing.

EEPROM technology has been used for PLD manufacturing by LSC for more than a decade. LSC refers to their high performance EEPROM technology as E^2CMOS technology. Extensive reliability studies of the technology have been performed with industry-wide acceptance, including the military.

Other Methods Are Imprecise

All PLD devices must be tested to some degree to validate functionality and performance. Technologies that are not erasable or require lengthy erase times severely constrain the test flexibility. Since the normal "user" programmable elements cannot be programmed during manufacture (all elements must be available for end-user programming) the manufacturers of one-time programmable PLDs resort to using simulated and correlated performance of test rows, test columns and phantom or dummy-test arrays. At best, this is a statistical measure of the actual device performance. One need only look at the "normal" programming yield fallout of 0.5 to 3% or the "acceptable" post-programming test vector and board yield fallout of 0.5 to 2% to know that this correlation is weak. The quality systems of today are measuring defects in parts per million (PPM). A six sigma program requires less than 3.4 PPM, four orders of magnitude less than that achievable with non-testable PLDs.

Actual Matrix Patterning

The unique capability of E^2CMOS devices to be instantly electrically erased allows these devices to be patterned multiple times during LSC's manufacturing test. Normal array cells in the programmable matrix are patterned, erased and tested again and again. The test rows or columns, phantom arrays, etc., that are used with other technologies are not necessary with E^2CMOS devices. Programmability of every cell is checked dozens of times.

Historically, the checking of a successful programming operation consisted of no more than a pass/fail verification step. This digital, go/no go check is not adequate to assure that the cell is programmed properly with sufficient margin to guarantee long-term reliable performance of the device. LSC E^2CMOS devices are processed through a proprietary cell verification step that consists of an analog measure (to millivolt accuracy) of the actual cell threshold. This capability is used for extensive reliability and quality measurements and testing.

Worst Case AC/DC Testing

A PLD does not have a defined function until the engineer patterns the device with his custom pattern. The manufacturer, when considering the testing of a PLD, must consider the hundreds of different architecture and functional variations that can be created by the end user. Each configuration of architecture brings on a different set of worst case pattern and stimulus conditions. Quick application of a series of worst case patterns that cover

all of the permutations of input combinations, array load and switching, and output configuration is required.

E²CMOS devices offer instant erasability to address this reconfiguration and test problem. Testing each additional worst case configuration takes fractions of a second, allowing multiple patterns to be checked to assure performance to rated speeds. The final result is a device with defects reduced from PPH (parts per hundred) to PPM (parts per million).

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