Technology and Reliablity

Introduction

Lattice Semiconductor maintains a comprehensive reliability qualification program to assure that each product achieves its reliability goals. After initial qualification, data is continuously accumulated through monitor programs to further drive failure rates down. Each product's qualification plan is generated in conformance to Lattice's Qualification Policy with failure analysis in conformance to Lattice's Failure Analysis Procedures. Both documents are contained in Lattice's Quality Assurance Manual, available upon request. Failure rates in this reliability summary are expressed in FITS. Due to the very low failure rate of integrated circuits, it is convenient to refer to failures in a population during a period of 10^9 device hours; one failure in 10^9 device hours is defined as one FIT.

Process Overview

Lattice Semiconductor is using the fourth, fifth and sixth generations of its advanced UltraMOS® process in its current manufacturing (Figure 1).

Basic Theory of Operation

An E^{2}CMOS® cell is built around a MOS transistor with a floating gate which is externally charged or discharged by a small programming current. If the floating gate is charged up to a positive potential by removing electrons from the floating gate, the cell transistor is turned on, storing a binary '0' in the cell. If the floating gate is charged to a negative potential by placing electrons on the floating gate, the transistor is kept in the non-conducting or off state, which writes a binary '1' into the cell. In addition to the floating gate or sense device, an additional select transistor, or pass gate, is added in series with the cell to isolate it from the array during read and write operations. A schematic representation of this cell is shown in Figure 2. In addition to the conventional bit line and word line, the E^{2}CMOS cell also has an additional line for the matrix control gate (MCG) which controls the potential of the floating gate.

The cell is programmed by applying a programming pulse to either the matrix control gate or the bit line of a cell which has been selected by an applied high voltage on the word line. Programming takes place when electrons

Figure 1. Lattice UltraMOS Process Generations

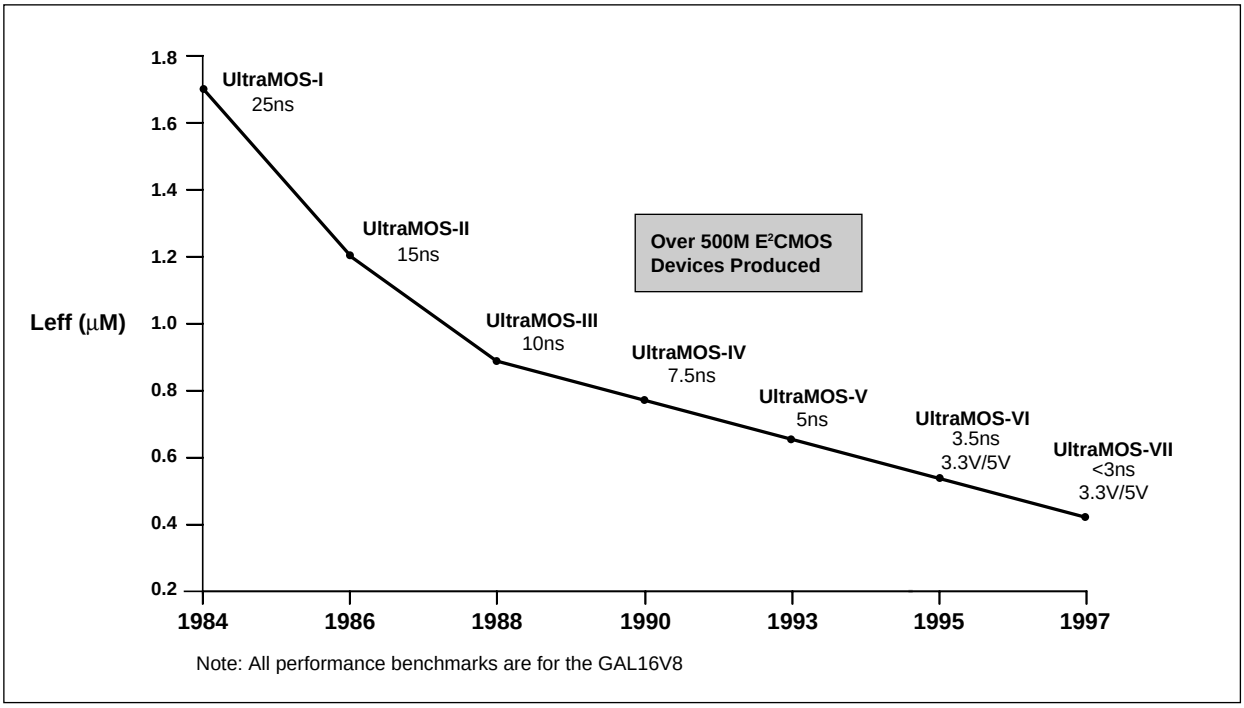
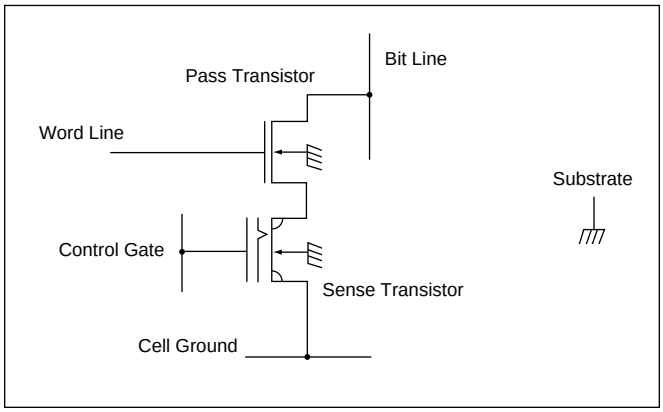


Figure 2. Erase Cycle Schematic



tunnel through the thin tunneling dielectric shown in the schematic by the small notch in the floating gate over the drain of the sense device. Before describing the detailed operation of the E^{2}CMOS cell, the requirements and tradeoffs of the process technology will be reviewed.

E^{2}CMOS Process Technology

Lattice's E^{2}CMOS technology is based upon a highly successful combination of CMOS and NMOS technologies. The requirements for both on-chip high voltage and high speed devices put severe restrictions on the process technology. By incorporating pumped substrate techniques from NMOS technology with low power CMOS devices, Lattice's E^{2}CMOS technology maintains high performance while meeting the high voltage requirements of programming.

In addition to combining the techniques of both NMOS and CMOS, Lattice's E^{2}CMOS technology incorporates an ultra-clean, ultra-thin tunneling oxide approximately 90-95 Angstroms thick. The requirements placed on these oxides will be much more apparent after the programming characteristics of the cell are examined.

Single Cell Programming

The E^{2}CMOS cell is programmed by placing a high voltage across the thin tunnel dielectric. The resulting tunneling current will tunnel electrons onto the floating gate turning off the sense transistor or, with a different applied potential, tunnel electrons off of the floating gate, turning on the sense transistor. Once the charge has been placed on the floating gate, the actual floating gate potential can be modulated by the voltage on the control gate through capacitive coupling. It is this capacitive coupling that is used to generate the high voltage across the tunnel dielectric at the beginning of a programming pulse.

During a programming cycle, the cell is first erased into the one, or non-conducting state and then selectively written to a '0', or conducting state by a write cycle. This prevents the sense device from conducting current during the write operation when voltage is applied to the drain of the device. Therefore, the programming characteristics will be explored by first examining the cell during an erase.

Erase Cycle Programming

During an erase cycle, a high voltage is applied to the control gate of the cell to be programmed, as shown in Figure 2. If all current through the tunnel oxide is neglected, the floating gate will simply track the applied voltage following the relationship of a capacitive divider,where C_{up} is the coupling ratio of the cell, and is typically between 0.7 and 0.8. At the end of the erase pulse, the floating gate would again couple negatively by the same amount, and end up back at the initial floating gate voltage $V_{fg}(0)$.

$$V^{1}fg = C_{up} * V^{2}cg + V^{3}fg \ (0)$$

1 floating gate voltage; 2 Control gate voltage; 3 Initial floating gate voltage

However, the high voltage applied across the tunnel dielectric causes tunneling current to flow, which will discharge the floating gate during the erase pulse. At the end of the erase pulse, the floating gate will end up at a potential that is lower than the initial floating gate voltage by the amount that the floating gate has decayed during the pulse. This negative voltage is sufficient to turn off the sense transistor during a read operation. The magnitude of the control gate voltage which is required to couple this negative floating gate voltage up to the threshold of the sense device and actually turn it on after the erase pulse is defined as the programmed high threshold Vt_{High}.

Write Cycle Programming

During the write cycle, a high voltage is applied to the bit line of the cell to be programmed. If all current through the tunnel oxide is again neglected, the floating gate will track the applied drain voltage following the relationship of a capacitive divider:

$$V_{fg} = C_d * V^{1}drain + V_{fg} \ (0)$$

1 Drain voltage applied during a write

C_d is the drain coupling ratio of the cell and is typically much lower than the coupling ratio to the control gate, ranging between 0.1 and 0.2. As in the erase case, the floating gate would again couple negatively by this same amount, and end up back at the initial floating gate voltage $V_{fg}(0)$ at the end of the write pulse. Also note that the pass transistor may have a voltage drop across it, lowering the voltage on the drain below the applied programming voltage V_{pp}.

However, instead of no current flowing through the tunnel oxide, the low coupling ratio keeps the floating gate at a low potential, which forces a high negative voltage to appear across the tunnel oxide. This high voltage causes tunneling current to flow which will charge the floating gate during the write pulse . At the end of the write pulse, the floating gate will end up at a potential that is higher than the initial floating gate voltage by the amount that the floating gate has charged during the pulse. This positive voltage is sufficient to turn on the sense transistor during a read operation. The magnitude of the control gate voltage which is required to couple this positive floating gate voltage down to the threshold of the sense device and actually turn it off is defined as the programmed low threshold Vt_{Low}.

Reading the Cell

After an erase cycle the charge on the floating gate has left the sense transistor in the off, or non-conducting '1' state. If the erase cycle is followed by a write cycle, then the floating gate charge leaves the sense device in the on or conducting '0' state. Therefore, the data in the cell can be read by simply sensing the cell current when biased with the control gate centered between the on and off states. This is shown schematically in Figure 3. The bit line and control gate voltages are selected to minimize the potential across the tunnel dielectric during a read in order to maximize the retention of the floating gate charge. The actual magnitude of the programmed thresholds, and thus the margins of the cell, are controlled by the programming voltage, the physical cell layout, and the tunnel oxide electrical characteristics. The key electrical properties of the tunnel oxide will be examined since they are critical in determining both the programming properties and the reliability of the E^2CMOS cell.

Tunnel Oxide Electrical Characteristics

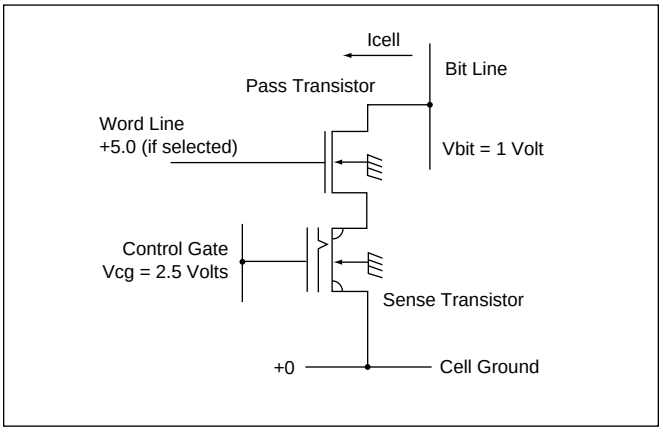
The E^2CMOS cell is programmed by placing a high voltage across the thin tunnel dielectric. The tunnel oxide is sufficiently thin, typically with a thickness between 80 and 120 Angstroms, that electrons will tunnel through the dielectric and program the cell. The exact nature of the tunneling mechanism is important because in addition to determining the amount of voltage required to get sufficient current through the oxide to program the cell, the tunnel characteristic also must be a very strong function of voltage to prevent the charge from leaking off of the floating gate during the low voltage, normal read, operation.

In addition to the electrical current voltage characteristics, thin tunneling dielectrics must also be characterized by the amount of charge that can pass through the oxide without altering its electrical properties. Electron traps located in the oxide will capture some of the electrons passing through the dielectric. As this trapped charge builds up in the oxide, the electrical properties change, and eventually the oxide wears out and ruptures. Thus, in addition to controlling the erase and write characteristics of an E^2CMOS cell, the tunnel oxide, and oxide quality, play a major role in the reliability of the technology.

I-V Characteristics of Thin Tunnel Dielectrics

A typical I-V characteristic of a thin tunnel oxide is shown in Figure 4. Since the current must flow through this oxide in both directions, the characteristic of the oxide is shown for both positive and negative polarities. Note that a higher negative voltage is required to get the same current as in the positive voltage case because of an additional voltage drop that occurs across a depletion region formed in the silicon for negative applied voltage. For a tunnel oxide of approximately 100 Angstroms in thickness, the maximum voltage developed during programming is roughly 10 volts, or a field strength of 10 MV/cm. This very high applied field stress, needed for the tunneling process requires very high quality oxides and very clean processing conditions. Optimizing the thickness of the tunneling dielectric and trading off between the programming characteristics and the oxide reliability is a requirement of the E^2CMOS technology.

Figure 3. E^2 Cell Read Cycle Schematic



The I-V characteristic is a very strong function of oxide thickness and follows the relationship of the Fowler-Nordheim tunneling equation, where A and B are the Fowler-Nordheim coefficients.

$$I_{tox}(V) = A * Area * \left(\frac{V^2}{Tox^2}\right) * Exp\left(\frac{-B * Tox}{V}\right)$$

This equation can be rewritten in terms of the field across the oxide as below, which is independent of oxide thickness.

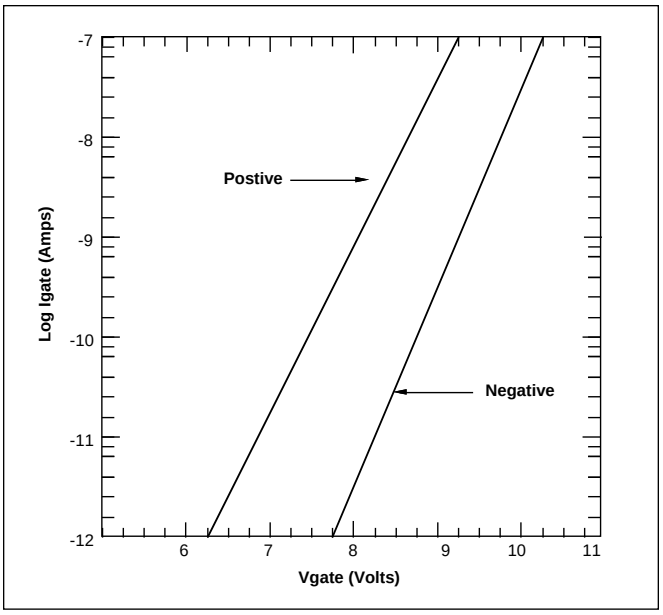
$$I_{tox}(E) = A * Area * E^2 * Exp\left(\frac{-B}{E}\right)$$

Charge-to-Breakdown of Thin Tunnel Oxides

The I-V characteristic shown in the previous section was measured at sufficiently low current densities such that no charge trapping occurred during the measurements. If, however, a large amount of charge is passed through the oxide, the trapped charge in the oxide will alter the electrical I-V characteristic. The increase in voltage required to get the same tunneling current after a large amount of charge passes through the oxide will reduce the amount of charge transferred into the cell during a programming cycle and therefore reduce the cell programming margins with continued cycling. The magnitude of the charge required to shift the I-V characteristic depends on the quality and the number of traps in the oxide.

In addition to this shift in the electrical properties of the tunnel dielectric, defects in the oxide, whose properties change as the charge passes through the oxide, will actually cause the oxide to rupture after a finite amount of charge has passed through the dielectric. The maximum charge that can be passed through the oxide prior to oxide breakdown, or the oxide fluence expressed in Coulombs/cm^2, can be determined by passing current through a tunnel dielectric until it ruptures. This physical limitation on the current that can be passed through the tunnel oxide places a limit on the number of programming cycles that can be performed on any E^2 device. This cycling limit, or endurance, is dependent on the quality of the tunnel dielectric and its associated defect density as well as the exact programming stress on the oxide. Lattice's technology maximizes the endurance of the devices through careful control of the requirements on the oxide as well as by optimizing the quality of the dielectric.

Figure 4. Tunnel Oxide I-V Characteristics



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