ISP™ Cost-of-Ownership Analysis

What is Cost-of-Ownership?

Cost-of-ownership is defined as the total of all costs incurred throughout the life and use of a component, that can be directly attributed to that component. The life of a programmable logic device (PLD) begins with the System Design Phase, extends through the System Manufacturing Phase, and goes beyond initial system shipments into the Field Repair and Update Phase. In most cases, the initial purchase price—the standard by which engineers and purchasing agents often judge component costs—is only a fraction of the total cost incurred by a component during its lifecycle.
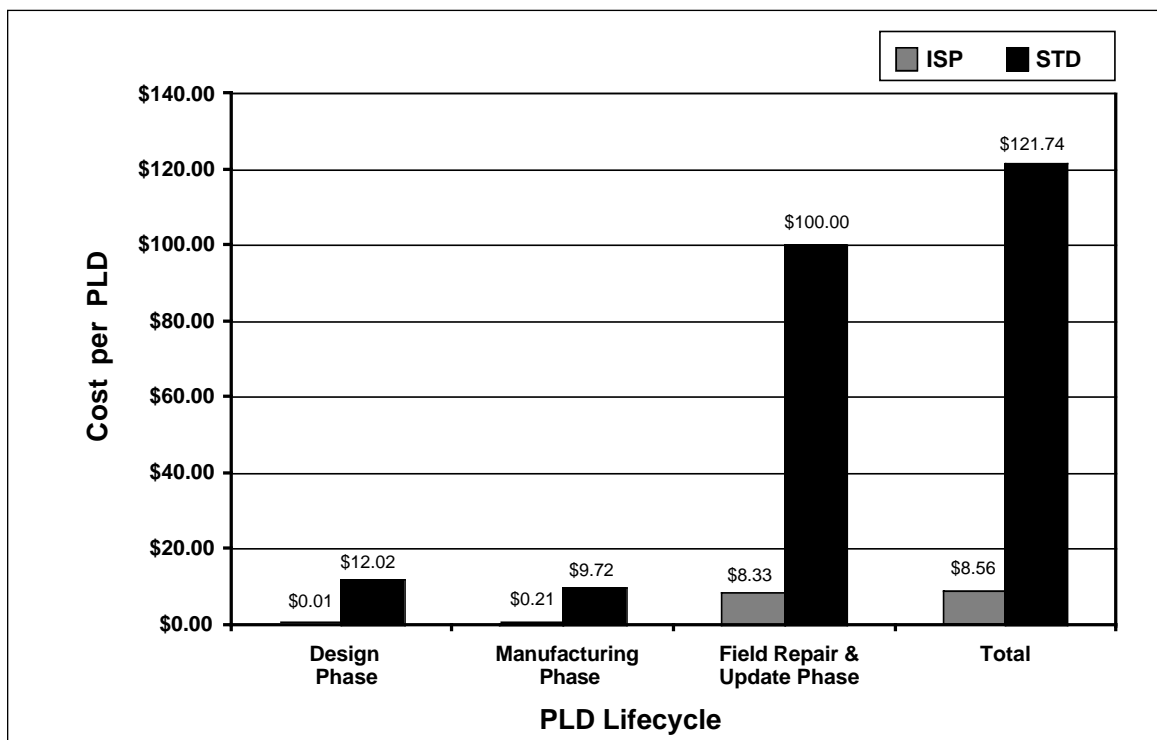
The ISP Cost-of-Ownership Model

This document uses the In-System Programmable™ (ISP™) Cost-of-Ownership Model (hereafter referred to as the "model") to compare the cost-of-ownership for ISP and standard PLDs at each stage of their lifecycles:

- During the **System Design Phase**, the model illustrates the direct costs of prototype PLDs and sockets as well as the associated prototype device programming costs. It also explores the less obvious, yet potentially more significant opportunity cost of time-to-market— the time it takes a product to move from idea to production.

- In the **System Manufacturing Phase**, the model describes five cost categories, including production programming, PLD inventory costs, obsolete PLD inventory costs, general manufacturing costs, and quality and reliability costs.

- The last phase of the model, the **Field Repair and Update Phase**, explores the cost of updating systems that use PLDs which have already been installed in the field.

This model has been developed largely from the input of Lattice Semiconductor Corporation (LSC) customers who have implemented ISP solutions in their systems and

Figure 1. Incremental PLD Cost-of-Ownership

> ## Use an Excel Worksheet to Calculate Your Own Cost-of-Ownership:
> ### isp_coo5.xlw (Excel v.5) or isp_coo4.xlw (Excel v.4)

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manufacturing environments. The model describes the overall PLD costs involved in the lifecycle of an average or typical system. However, no system is average or typical. Thus, it is expected that the reader will assign different levels of importance to the various elements of cost described. The reader is also encouraged to calculate cost estimates based on his or her own situation using the model as a template.

The ISP Cost-of-Ownership Metric

Figure 1 (see page 1) summarizes the cost elements associated with each phase of a component's lifecycle and the impact of these elements on total PLD cost-of-ownership. This figure illustrates the difference in overall PLD cost structure associated with the two PLD types. The balance of the model will document these cost elements and their calculations. Some calculations presented may contain slight rounding errors when a fixed number of decimal places is used (generally two or three).

PLD Categories Compared

This model divides PLDs (both low- and high-density) into two basic categories—in-system programmable PLDs and standard PLDs:

- **In-System Programmable (ISP) PLDs**—This category features PLDs which can be configured and reconfigured electrically while "in-system." LSC offers three ISP product families: ispLSI®, ispGAL®, and ispGDS™. These families share the same non-volatile ISP E²CMOS™ process technology and ISP programming algorithm.

- **Standard PLDs (STD)**—Standard PLDs consist of conventional PLD technologies which do not support in-system programmability. Primarily, this covers erasable technologies such as EPROM and EEPROM, but also extends to one-time programmable (OTP) technologies such as bipolar and anti-fuse.

The specific cost examples discussed in this model generally focus on standard PLDs which are electrically erasable but do not support in-system programmability. OTP PLD technologies such as anti-fuse, bipolar and EPROM in OTP plastic packages are not featured for a number of reasons:

- The vast majority of new PLD designs use either ISP, EPROM or EEPROM technology.

- The cost-of-ownership for OTP-based PLDs is dramatically higher than for any of these erasable PLDs:

    - By definition, OTP PLDs cannot be reconfigured. Thus, any code changes result in device scrap.

    - Programming yields are much lower; OTP PLDs cannot be 100% tested prior to user configuration.

    - Programming times for OTP PLDs are typically much longer than for other PLDs.

    - OTP PLDs offer none of the benefits of ISP.

Model Assumptions

- The end equipment is an electronic system with an average selling price of $5,000.

- The lifetime (three-year) system volume is 15,000 systems ($75,000,000 total revenue).

- Five prototype systems are required prior to production release.

- One of the boards in the system contains three 6,000-gate high density PLDs or field programmable gate arrays (FPGAs). The model assumes two versions of this board, requiring two separate sets of interface logic.

- The PLDs use a high pin-count quad flat pack (QFP) package.

- The PLD purchase price is $30 for prototypes, $15 in volume.

- The system lifetime PLD usage is 45,000 units (15,000 systems at three PLDs per system).

- The design engineering pay rate is $12,000 per month (or $3,000 per week), including salary and benefits.

- Board rework labor costs are $300 per board.

System Design Phase

As stated earlier, the purchase price of a PLD should be viewed only as the starting point for calculating the total cost-of-ownership. A designer's PLD choice can have a dramatic impact on costs incurred—or avoided—during the System Design Phase.

Prototype Sockets

ISP PLDs can be soldered directly onto the prototype circuit board and still accommodate design iterations by simply reconfiguring the devices in-system, eliminating the need for prototype sockets.

Standard PLDs, however, require sockets on the circuit board which must be removed and reprogrammed for each design iteration. The model assumes that the board's production configuration includes surface mounted PLDs, versus socketed (see Table 1). Surface mounted PLDs require the use of socket adapters during prototyping which are footprint compatible with the surface mount PLD package (QFP assumed). These socket adapters cost approximately $500 each (source: 100pc pricing from Emulation Technology). Standard through-hole socket adapters can also be used at a cost of approximately $75 each. However, a final respin of the board is required after debug to remove the socket adapters and layout the board for the PLD footprint. The respin costs at least $3,000 and is not without risk of error and project delay.

Table 1. Prototype Socket Costs

Prototype Socket Costs	ISP	STD
Quantity of prototype sockets (five prototype systems)	N/A	15
Prototype socket cost (PLD footprint compatible)	N/A	$500
Total prototype socket costs	N/A	$7,500
Prototype socket costs per 45,000 production PLDs	$0.000	$0.167

There are many designs whose critical timing requirements make using prototype sockets unacceptable. Sockets add extra loading on signal paths reducing performance. For these designs, the use of standard PLDs forces the designer to solder and desolder the prototype PLD for each revision of code. After two or three cycles, the prototype board is unworkable and must be replaced with a new prototype board and the associ-

ated board components. These costs—all of which are avoided with ISP PLDs—are not included in the model.

The use of standard PLDs results in the expenditure of $7,500 for prototype sockets, which when amortized over the 45,000 system lifetime PLD usage, adds almost $0.17 to the purchase price of each PLD.

Prototype Silicon

The number of prototype ISP PLDs required can be calculated by simply multiplying the required prototype systems by the number of PLDs per system. These devices can be soldered to the circuit board and reconfigured in-system as needed as the design matures. As a result, there is no device scrap.

Standard PLDs require two socketings for each pattern iteration (one socketing at the programmer and a second on the circuit board). In higher pin-count QFP packages with their fragile leads, two pattern iterations can cause enough lead damage to make them unusable. The model assumes a conservative 33% yield loss (five devices) over the course of the prototype phase (see Table 2).

Table 2. Prototype Silicon Costs

Prototype Silicon Costs	ISP	STD
Quantity of prototype PLDs (five prototype systems)	15	15
Handling/socketing fallout rate (QFP package)	0%	33%
Replacement PLDs (handling damage)	0	5
Total prototype PLDs required	15	20
Prototype PLD costs	$450	$600
Prototype PLD costs per per 45,000 production PLDs	$0.010	$0.013

During prototyping, ISP PLD users can achieve a savings of $150 over standard PLD users.

Prototype Programming Costs

One of the major costs incurred during the System Design Phase is the cost of device programming. A designer using ISP technology simply solders an ISP device onto the prototype board and downloads design iterations via a download cable. LSC offers the

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ispDOWNLOAD™ Cable for $65. This cable is also available at no cost with the purchase of any of LSC's Logic Development Systems.

With standard PLDs, a stand-alone, third-party PLD programmer (approximate cost, $5,000) is required to pattern the devices. The model assumes that the cost of the programmer will be depreciated over a five-year period (see Table 3).

Further, the model assumes that the programmer is shared by five designers, each working on four projects per year. The ISP designer is able to complete six projects per year, for reasons explained in the next section.

Table 3. Prototype Programming Costs

Prototype Programming Costs	ISP	STD
Programmer costs	$65.00	$5,000.00
Annual depreciation (assume five-year life)	$13.00	$1,000.00
Annual updates (15% of purchase price)	$0.00	$750.00
Programmer costs/year	$13.00	$1,750.00
Number of designers/programmer	1	5
Design projects/year/designer	6	4
Quantity of prototype PLDs/project	15	15
Total prototype PLDs/year	90	300
Programmer costs/prototype PLD	$0.14	$5.83
Programmer costs/project	$2.17	$87.50
Programmer costs per 45,000 production PLDs	$0.000	$0.002

With ISP, each designer is given his or her own $65.00 "programmer" at a per project cost of $2.17 versus the standard PLD approach costing over $87.00 per project.

> "Time is money! With Lattice ispLSI devices, we are able to do our development in one-fifth the time it would take with competitive FPGA solutions."
>
> —William A. Long, Vice President of Engineering, Micronet Corporation, winner of the 1990 and 1991 Storage Product of the Year Award from MacUser Magazine

> "Prototyping with the ispLSI 1032 cut more than 50% off our development and debug time. Design changes that once took half a day are now handled in minutes!"
>
> —Alan Beverly, Engineering Manager, Ziatech Corporation

Time-to-Market Opportunity Costs

The most significant advantage for ISP technology during the System Design Phase is its dramatic impact on reducing system design cycle time. Both Ziatech and Micronet can attest to this fact.

This model assumes a 33% ISP product development cycle time reduction from three months to two months, translating directly into a time-to-market advantage. Every day saved in system design equals a one-day gain in product availability, revenue generation, and corporate net margin contribution (assumed at 25% of revenue). With ISP, the system can be launched into the marketplace one month earlier than in the standard PLD scenario, resulting in $521,000 in incremental corporate profits. A decision to design with standard PLDs is a decision to forego these corporate profits.

Use of standard PLDs also requires a design engineer to remain on a project for an additional month (at a cost of $12,000), delaying his or her work on the next system generation.

Table 4. Time-To-Market Opportunity Cost

Time-to-Market Opportunity Cost	ISP	STD
Lifetime system revenue	$75,000,000	$75,000,000
System revenue/month	$2,083,833	$2,083,333
After tax contribution margin	25%	25%
Margin contribution/month	$520,833	$520,833
Design cycle time (months)	2	3
Product intro delay (months)	0	1
Cycle time opportunity cost	N/A	$520,833
Incremental engineering costs	N/A	$12,000
Total opportunity cost	N/A	$532,833
Opportunity cost per 45,000 production PLDs	$0.00	$11.84

Figure 2. System Design Cost-of-Ownership
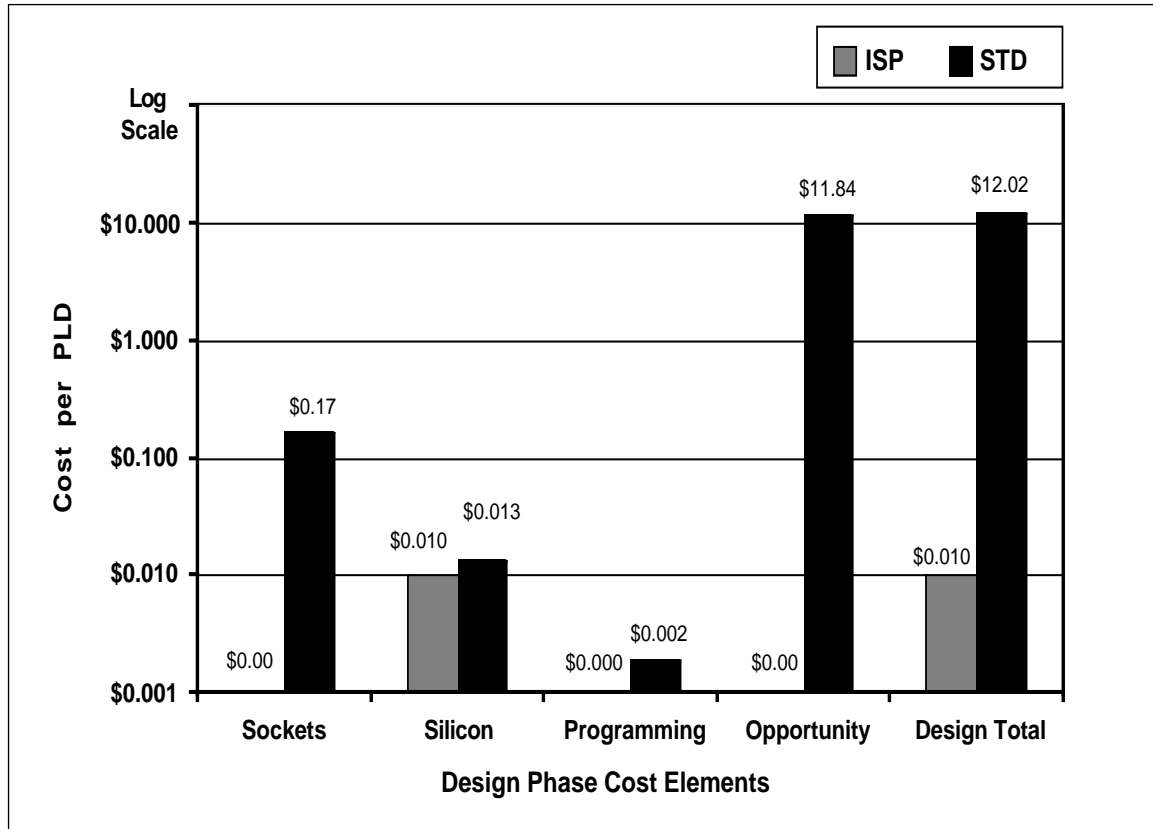
The opportunity cost of choosing the standard PLD approach is $533,000, adding $11.84 to the original purchase price of the standard PLD.

board/system process flow are used. Failures after board/system assembly are very expensive to detect and repair.

System Design Phase Summary

As shown in Figure 2, the most significant component cost incurred by the standard PLD during the System Design Phase is the opportunity cost, which contributes $533,000—almost an additional $12 to the $15 original purchase price of the PLD—for an increase of 80%. The standard PLD component cost contributions (prototype sockets, silicon and programming) are relatively small by comparison, but each is dramatically higher than for the ISP PLD scenario, adding over $8,000 to the overall project development costs.

System Manufacturing Phase

In the system manufacturing arena, costs continue to escalate if PLDs which do not integrate smoothly into the
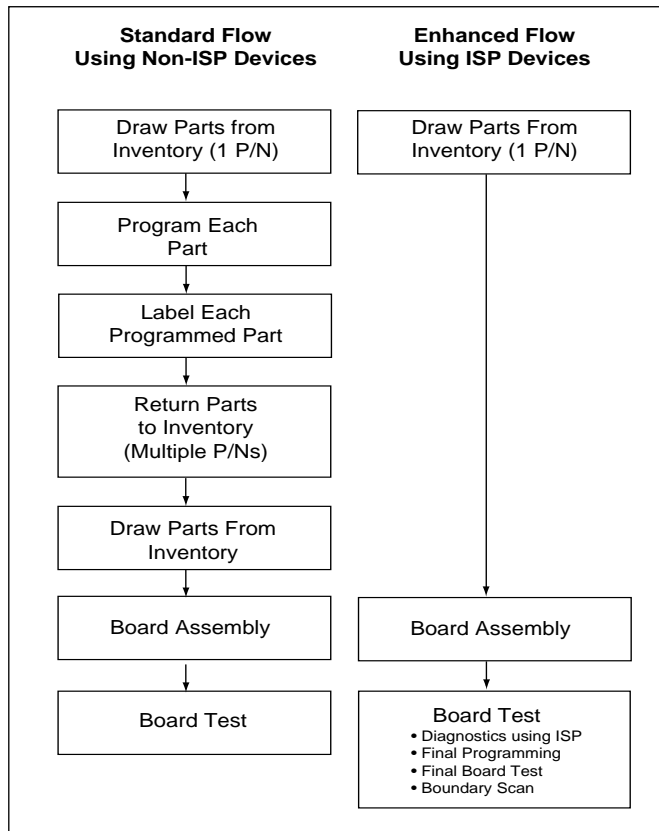
Programming Costs

One of the most exciting benefits of ISP PLDs is the ability to eliminate the stand-alone programming and mark steps from the manufacturing flow. As shown in Figure 3 (see next page), PLD device programming can be integrated into final board-level testing, thus eliminating the problems and expense inherent in the traditional PLD programming flow. Tables 5 through 9 outline the cost

Table 5. Base Programming/Mark Costs

Base Programming/ Mark Costs (QFP)	ISP	STD
Programming unit costs	$0.80	$0.50
Mark unit costs	$0.00	$0.15
Total program/mark costs per device	$0.80	$0.65

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Figure 3. ISP Manufacturing Flow

Standard Flow Using Non-ISP Devices	Enhanced Flow Using ISP Devices
Draw Parts from Inventory (1 P/N)	Draw Parts From Inventory (1 P/N)
Program Each Part	
Label Each Programmed Part	
Return Parts to Inventory (Multiple P/Ns)	
Draw Parts From Inventory	
Board Assembly	Board Assembly
Board Test	Board Test • Diagnostics using ISP • Final Programming • Final Board Test • Boundary Scan

elements associated with the production programming of ISP and standard PLDs.

The model establishes a base device programming and mark (or label) cost for ISP and standard PLDs (see Table 5, previous page). The standard PLD programming and mark costs were derived after consulting with a number of large electronics distributors. For high-density PLDs in QFP packages, the charges ranged from $0.50 to over $1.00. The model assumes a conservative $0.50 for programming and an additional $0.15 for marking a standard PLD.

For ISP PLDs, device programming occurs during final board testing using PC, workstation or standard ATE equipment (such as Hewlett Packard, Teradyne or GenRad). There is no need for device labeling since the blank ISP PLDs have already been soldered onto the board. ATE programming ensures that the correct device pattern is programmed into the correct PLD. An electrical device identification can be programmed into each device's user electronic signature (UES) for easy tracking of pattern revisions.

The model uses an $0.08 cost per device for programming ISP PLDs via ATE (see Table 6). A $200,000

Table 6. ATE Programming Costs

ATE Programming (QFP Package)	ISP
ATE board tester cost	$200,000
Annual depreciation (over five years)	$40,000
Annual maintenance (15% purchase price)	$30,000
Annual equipment/maintenance costs	$70,000
Base equipment cost/hour	$10.13
Operator wages/hour	$12.15
Total base programming costs	$22.28
Utilization cost adder (assume 80%)	$5.57
Efficiency cost adder (assume 80%)	$5.57
Net ATE programming costs/hour	$33.42
ATE programming costs/second	$0.0093
100-pin QFP programming time (seconds)	8.64
100-pin QFP programming cost	$0.080

combinational board tester (Hewlett Packard 3070 class) is assumed, depreciated over five years, including annual maintenance, for a total of $70,000 in annual equipment expenses. After adding operator wages, and utilization and efficiency adders (including tester "up time," shift changes, lunches, breaks etc.), the ATE costs $33.42 per hour. An ATE can program an ISP PLD in a little over eight seconds which drives the $0.08 per device ISP programming cost.

Table 7 documents the programming yield assumptions used in this cost analysis. The model recognizes that the 100% testability of both the ISP and electrically erasable standard PLD technologies makes programming and functional yield loss virtually nonexistent. This is not the case for OTP PLD technologies which cannot be fully tested prior to user programming. There is, however, a

Table 7. Programming Yield Assumptions

Programming Yield Assumptions	ISP	STD
Yield assumptions:		
First pass handling yield loss	0%	20%
Second pass handling yield loss (unrecoverable)	0%	30%
Net handling yield loss	0%	6%
Programming yield loss	0%	0%
Functional yield loss	0%	0%
Cumulative yield loss	0%	6%

significant element of programming yield loss associated with standard PLDs in QFP packages. With fragile leads requiring hand socketing in a stand-alone programmer, fallout rates of 30% and higher are common. The model assumes a 20% first pass handling yield loss with the further assumption that 70% of those failures can be successfully reworked and reprogrammed.

With these yield assumptions, the model examines the programming cycle costs, assuming a PLD quantity of 45,000 over the life of the system (see Table 8). The standard PLD scenario requires the purchase of an additional 2,700 devices to replace those irreparably damaged in handling. Programming and mark costs for standard PLDs are 10 times greater than for ISP PLDs ($31,000 vs. $3,600). The purchase of the extra 2,700 standard PLDs adds an additional $40,500 (2,700 units @ $15 per unit). The handling rework charges for the standard PLD approach add another $9,000 based on rescreening 9,000 devices, each incurring a $0.50 lead straightening and $0.50 programming charge.

Table 8. Program, Mark & Replacement Costs

Programming, Mark and Replacement PLD Costs	ISP	STD
First pass programming:		
Initial PLD quantity	45,000	45,000
Replacement PLDs (from yield loss)	0	2,700
Total quantity of PLDs required	45,000	47,700
Programming/mark costs	$3,608.93	$31,005.00
Incremental PLD purchase costs	$0.00	$40,500.00
Handling rework costs:		
Number of units needing rework	0	9,000
Lead straightening charge	N/A	$0.50
Programming charge	N/A	$0.50
Total rework charge/unit	N/A	$1.00
Total rework charges	$0.00	$9,000.00
Total programming/mark costs	$3,608.93	$80,505.00
Total programming costs per 45,000 production PLDs	$0.08	$1.79

Total programming costs for ISP PLDs add only $0.08 to overall cost-of-ownership, while programming costs for standard PLDs add an incremental $1.79 to the original component purchase price.

PLD Inventory Costs

ISP PLDs dramatically simplify PLD inventory strategies by requiring a single unprogrammed part number to be forecasted, ordered, received, inventoried and issued to manufacturing. When standard PLDs are procured in the pre-patterned state, six unique part numbers must be tracked from forecast through manufacturing. For standard PLDs programmed in-house, the single PLD part number becomes six separate part numbers after the programming step.

As illustrated in Figure 4 (see next page), ISP PLDs can reduce on-hand PLD inventories by half. For example, six weeks of standard PLD inventories can shrink to three weeks of ISP PLD inventories. And, ISP PLDs provide enhanced manufacturing flexibility since these inventories are not customized until final board test.
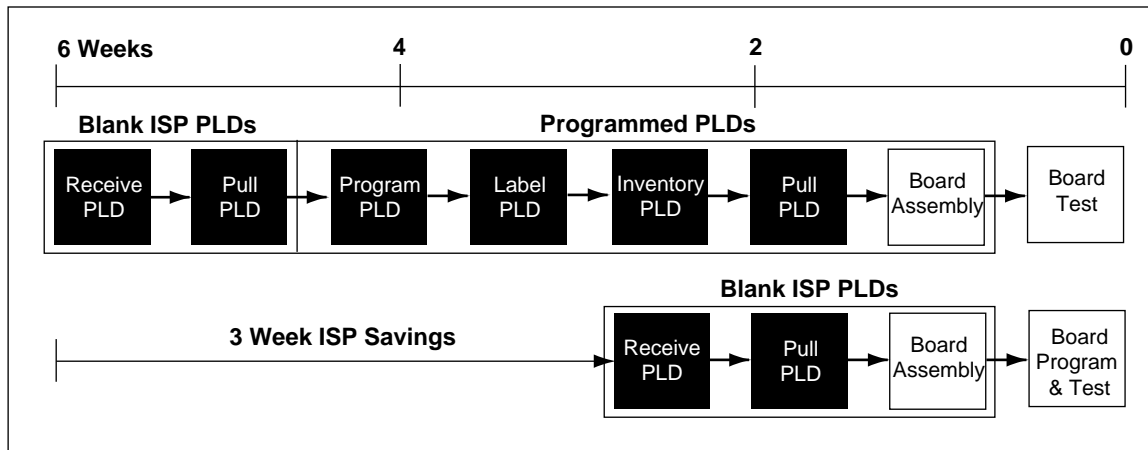
Table 9. PLD Inventory Costs

PLD Inventory Costs	ISP	STD
PLD consumption per week	288	288
Required weeks of PLD inventory	3	6
"On-hand" PLD inventory (units)	865	1,731
"On-hand" PLD inventory	$12,980.77	$25,961.54
Carrying cost rate (% per year)	15%	15%
System lifetime (years)	3	3
Total inventory carrying costs	$5,841.35	$11,682.69
Total carrying costs per 45,000 production PLDs	$0.13	$0.26

Needlessly carrying three weeks of standard PLD inventory represents an opportunity cost equal to the amount of interest those inventory dollars could have earned if they had been invested in other projects. Table 9 quantifies the on-hand inventory requirements and associated carrying costs for both ISP and standard PLDs (at the industry standard carrying cost of 15% for three years).

The inventory carrying costs for standard PLDs, at $0.26 per production device are twice that of ISP PLDs which add only $0.13 to the total cost-of-ownership.

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Figure 4. Reduced PLD Inventory WIP

Obsolete PLD Inventory Costs

What happens to PLD inventories when the engineering department issues an emergency request requiring new PLD patterns, to the manufacturing floor? What happens when the marketing department informs manufacturing that the sales forecast is incorrect—the market is now demanding Version B of the system instead the Version A currently being built?

In systems designed with standard PLDs, the manufacturing floor now has programmed component PLD inventories needing to be reprogrammed and remarked, and board inventories needing to be reworked. If the system has been designed with ISP PLDs, the manufacturing floor is instantly retooled by calling up the board test program for Version B on the ATE tester. Any Version A board inventories can be easily converted to Version B by reconfiguring the ISP PLDs in-system. These costs are described in detail in Table 10.

The model assumes that during the three-year life of this system, there will be six "events" in which the on-hand programmed PLD inventories will need to be reworked. Further, it is assumed that at each event, there will be three weeks of programmed component inventories on-hand (standard PLDs only), and one week of PLDs soldered on boards (both standard and ISP PLDs), all of which will need to be reworked to incorporate the new Version B device codes.

The standard PLD component inventories will incur the $0.65 programming and mark costs. The board rework is more involved, since replacement standard PLDs will be necessary due to the package damage caused by the de-solder process (6 events x 288 PLDs/event x $15/PLD = $25,900). These replacement PLDs must be programmed

Table 10. Obsolete PLD Inventory Costs

Obsolete PLD Inventory Costs	ISP	STD
Assumptions:		
Number of code or mix change "events" during system life	6	6
Weeks of programmed component inventory	N/A	3
Weeks of PLD inventory per event	1	1
Compoment PLD inventory per event	0	865
Board level PLD inventory per event	288	288
Boards requiring rework per event	96	96
Component rework:		
Program and remark unit charges	$0.08	$0.65
Total component rework costs	$0.00	$3,375.00
Board rework:		
New device costs	$0.00	$25,961.54
Programming/mark costs	$138.80	$1,125.00
Board rework labor (per board)	$0.00	$300.00
Board rework costs	$0.00	$173,076.92
Total board rework costs	$138.80	$200,163.46
Total obsolete PLD inventory costs	$138.80	$203,538.46
Obsolete inventory costs per 45,000 production PLDs	$0.003	$4.52

and marked. The labor alone required to desolder, resolder and retest each circuit board can easily total $300 each.

For ISP PLDs, reprogramming the PLDs is the only effort in reworking. Table 10 shows the board rework cost of $0.00 for the ISP scenario since all ISP costs are covered by the $0.08 programming charge.

Obsolete PLDs add $204,000 to the total system cost over the three-year system life or an additional $4.52 to the original purchase price of every standard PLD.

General Manufacturing Costs (Labor and Equipment)

ISP PLDs allow for several manufacturing efficiences not possible with the use of standard PLDs:

- ISP PLDs support multi-function hardware whereby a single board design can be configured in "real time", to multiple board configurations. For this model, the use of standard PLDs requires manufacturing to manage two unique board designs (at half the volume each) and alternate the line between boards periodically. With ISP PLDs, the manufacturing floor performs 50% fewer product change-overs.

- With ISP, only a single device track is required for all pick-and-place locations, no matter the board revision or device pattern. With standard PLDs, three device tracks must be devoted to PLDs (one for each pattern). For many operations, this capability can

Table 11. General Manufacturing Costs

General Manufacturing Costs (Labor and Equipment)	ISP	STD
Number of boards manufactured	15,000	15,000
Number of unique board designs	1	2
Boards built per design (assume 50/50 split)	15,000	7,500
Baseline manufacturing cost per board	$50.00	$50.00
Manufacturing cost savings (%)	5%	0%
Actual board manufacturing cost per board	$47.50	$50.00
Total board manufacturing costs	$712,500.00	$750,000.00
Incremental costs	$0.00	$37,500.00
Incremental manufacturing cost per 45,000 production PLDs	$0.00	$0.83

Table 12. Quality and Reliability Costs

Quality and Reliability Costs	ISP	STD
Board fallout due to PLD coplanarity	0%	2%
Boards requiring rework	0	300
Replacement PLDs required (at $15 each)	0	900
Board rework:		
New device costs	$0.00	$13,500.00
Programming/mark costs	$0.00	$585.00
Board rework costs		$90,000.00
Total board rework costs	$0.00	$104,085.00
Board rework costs per 45,000 production PLDs	$0.00	$2.31

help avoid the purchase of new pick-and-place equipment.

The model assumes a modest 5% savings in general manufacturing costs as a result of these efficiencies of scale (see Table 11).

The use of ISP saves $37, 500 over the standard PLD approach which adds an additional $0.83 to the standard PLD cost-of-ownership total.

Quality and Reliability Costs

ISP PLDs can dramatically reduce board quality and reliability problems and costs. Two common causes of board rework are poor solder joints from bent leads and incorrect devices or device patterns on the board.

Both of these problems are eliminated with ISP PLDs, since the devices go from stock to circuit board without the handling-intensive, stand-alone programming steps required of standard PLDs that can cause coplanarity and bent leads. ISP programming not only significantly reduces these problems, but also eliminates the possibility of placing patterned PLDs in the wrong locations on the board.

The model (Table 12) assumes a 2% board fallout for standard PLDs with high pin-count QFP packages. The excessive handling associated with the programming operation causes lead damage which can result in poor solder joints on the PCB. The board rework cost model was discussed in the Obsolete PLD Inventory Costs section on page 8 and will not be discussed in detail here.

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Figure 5. System Manufacturing Cost-of-Ownership
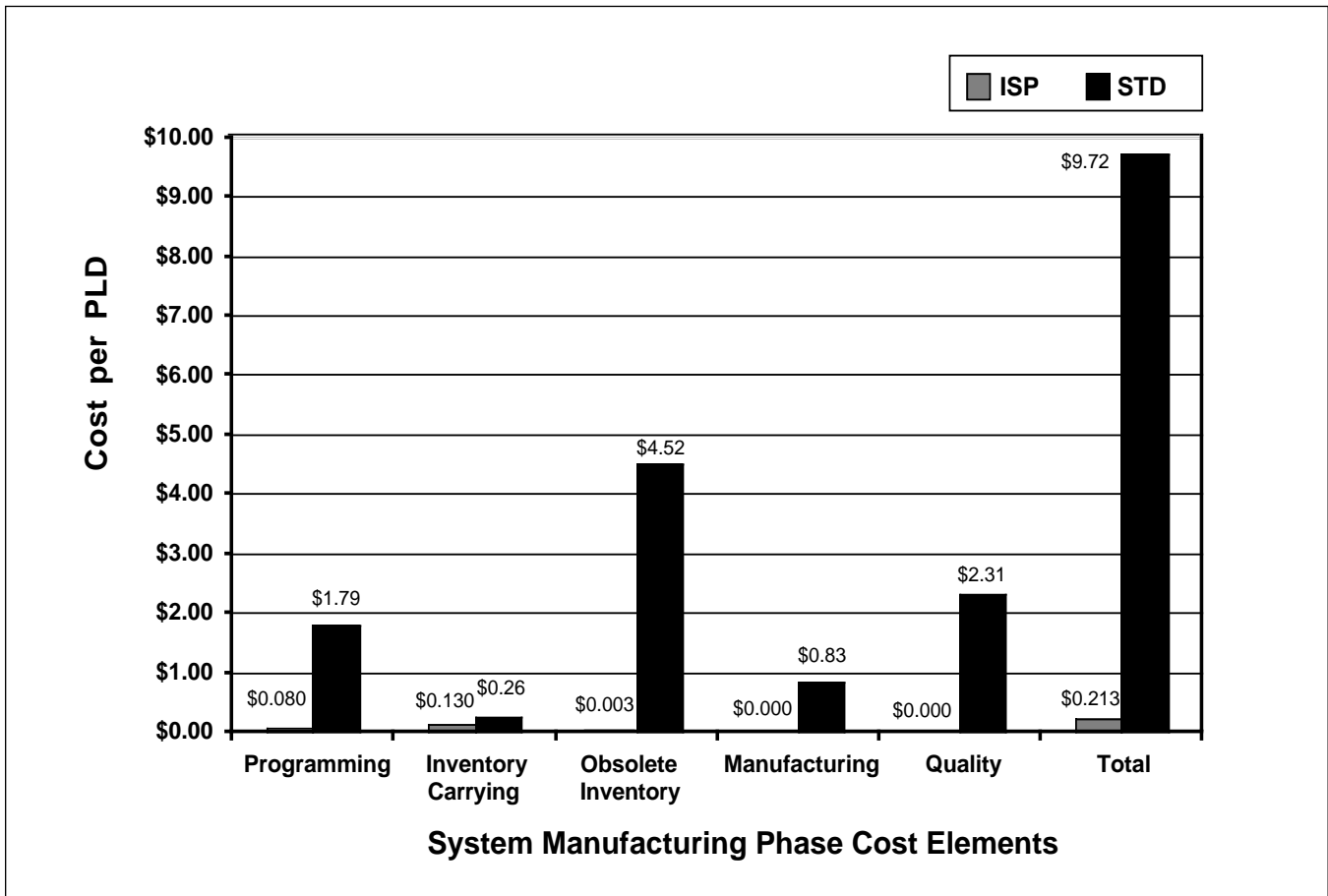
The standard PLD scenario adds $104,000 to the total system cost or an additional $2.31 to the standard PLD cost-of-ownership total.

System Manufacturing Summary

There are five areas in the System Manufacturing Phase in which the choice of PLD can have a significant impact on the overall PLD cost-of-ownership (see Figure 5). ISP PLDs offer consistently lower component costs across all five categories, and in two of the categories, add no incremental component costs to the cost-of-ownership totals.

In total, ISP PLDs add an additional $0.21 to the original $15.00 purchase price whereas standard PLDs add an additional $9.72 to the $15.00 purchase price.

Field Repair and/or Update Phase

This last phase of the System lifecycle highlights the ability of ISP PLDs to easily reconfigure system logic while the systems are installed in the field.

Field Repair Costs

Field replacement of defective PLDs is a rarity. ISP and electrically erasable standard PLDs enjoy 100% factory test coverage which eliminates infant mortality, unlike OTP PLDs which cannot be fully tested prior to user programming. Neither ISP nor electrically erasable standard PLDs incur field repair costs due to latent programming problems.

Table 14. Total Incremental Cost-of-Ownership (Over System Life)

Grand Total Costs over System Life Cycle	ISP	STD
System Design:		
Prototype socket costs	$0.00	$7,500.00
Prototype silicon costs	$450.00	$600.00
Prototype programming costs	$2.17	$87.50
Opportunity cost	$0.00	$532,833.33
System design subtotal	**$452.17**	**$541,020.83**
Manufacturing:		
Programming costs	$3,608.93	$80,505.00
PLD inventory costs	$5,841.35	$11,682.69
Obsolete PLD inventory costs	$138.80	$203,538.46
General board manufacturing costs	$0.00	$37,500.00
Quality and reliability costs	$0.00	$104,085.00
Manufacturing subtotal	**$9,589.08**	**$437,311.15**
Field Updates:		
Mass field update costs	$375,000.00	$4,450,000.00
Grand total ISP cost-of-ownership	**$385,041.24**	**$5,478,331.99**

Table 15. Total Incremental Cost-of-Ownership (per Production PLD)

Grand Total Costs per Production PLD	ISP	STD
System Design:		
Prototype socket costs	$0.000	$0.167
Prototype silicon costs	$0.010	$0.013
Prototype programming costs	$0.000	$0.002
Opportunity cost	$0.000	$11.841
System design subtotal	**$0.010**	**$12.023**
Manufacturing:		
Programming costs	$0.080	$1.789
PLD inventory costs	$0.130	$0.260
Obsolete PLD inventory costs	$0.003	$4.523
General board manufacturing costs	$0.000	$0.833
Quality and reliability costs	$0.000	$2.313
Manufacturing subtotal	**$0.213**	**$9.718**
Field Updates:		
Mass field update costs	$8.333	$100.000
Grand total ISP cost-of-ownership	**$8.56**	**$121.74**

Figure 6. Total Cost-of-Ownership
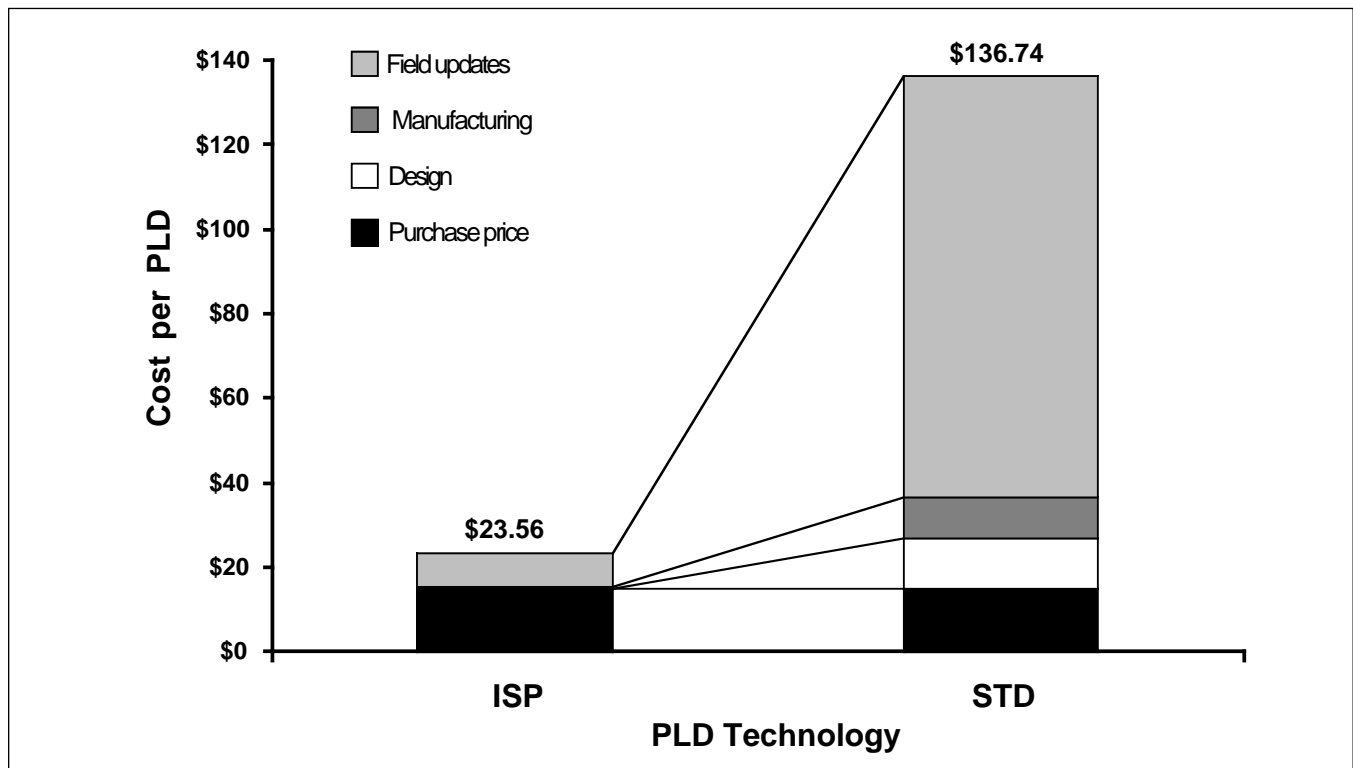
ISP™ Cost-of-Ownership Analysis

Field Upgrade/Update Costs

ISP is the only technology that makes mass hardware updates of installed systems practical. With ISP, installed systems can be upgraded by simply mailing a disk to the user, who downloads the upgrade code using the software provided (assume $25 per disk to generate and mail).

Update of a standard PLD-based systems require a board swap-out and at least a half day of a technician's time at a cost of $300 (not including the cost of the replacement circuit board). To update the entire installed system base of 15,000 systems would cost $375,000 with ISP PLD-based systems or $4.5 million for the standard PLD-based system (see Table 13). Field updates of standard PLD-based systems are simply cost-prohibitive and impractical. In short, ISP has emerged as the only technology which makes field updates and enhancements practical.

Table 13. Field Repair/Update Costs

Field Repair/Update Costs	ISP	STD
Total field repair costs	None	None
Number of updates	15,000	15,000
Cost/update	$25.00	$300.00
Total field update cost	$375,000.00	$4,500,000.00
Field repair/update cost per 45,000 production PLDs	$8.33	$100.00

Summary

ISP provides an overwhelming cost advantage over standard PLD-based designs when the total cost-of-ownership is examined. ISP PLDs provide the most cost competitive PLD solutions on the market today. ISP positively impacts every phase of the system lifecycle. Tables 14 and 15 (see page 11) summarize the total incremental cost-of-ownership incurred above and beyond the base purchase of the system lifetime requirement of 45,000 PLDs.

Figure 6 (page 11) demonstrates the impact of PLD programming technology on overall PLD cost-of-ownership. With ISP, the purchase price of $15 grew $8.56 for a total component cost of $23.56, whereas the cost of the standard PLD grew an astronomical $121.74 for a per device cost of $136.74.

As mentioned previously, it is expected that the reader may not find all elements of this model relevant to his or her situation, or may have different valuations for certain cost elements. However, portions of this analysis should be applicable to almost any PLD user. Examining a component's total cost-of-ownership is the best way to minimize overall cost. In-system programmable PLDs are clearly superior to standard PLDs in minimizing programmable logic costs and maximizing profits.

ISP Cost-of-Ownership Spreadsheet

A Microsoft Excel worksheet (Excel v.5 file name: isp_coo5.xlw and Excel v.4 file name: isp_coo4.xlw) is included on the ISP Encyclopedia CD-ROM and Lattice web site. This worksheet allows you to modify the cost-of-ownership assumptions made in this analysis to more closely model your own cost elements.

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