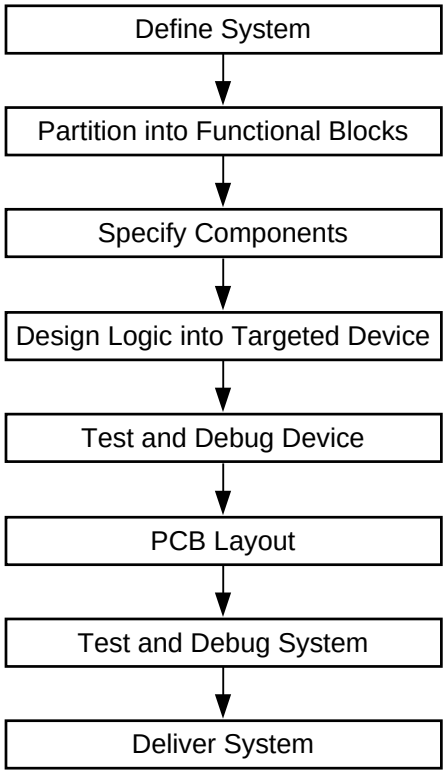
System Design Process

Introduction

Conceptually, system definition is the first step in the design process. This involves visualizing the PLD's interaction with the rest of the electronic system and defining a general flow diagram to determine the design's basic sequential behavior. This organizational flow, used to integrate an entire subsystem into high density devices, is described in the following topics and shown in figure 1.

Figure 1. System Design Flow



Partitioning

After completing the conceptual design, the designer partitions the system into modules or functional blocks. These blocks can be a few components or multiple circuit boards with numerous components. The designer organizes these functional blocks to match the capabilities of the devices being targeted, for example, the number of I/O pins, flip-flops and gates needed. The user should also consider the frequency at which the targeted device must operate, the number of clocks required, and the timing relationships of signals (AC specifications).

Specifying Components

After the partitioning is defined, the designer chooses the components which will be used to implement the desired functions. The design should meet the system specifications using the least number of components in order to keep the system cost as low as possible while keeping the system reliability as high as possible.

System specifications calling for low weight, low power and reduced size also drive designers to higher levels of logic integration. These added requirements can adversely affect the design schedule and project completion. The ispLSI and pLSI high-density devices can meet such design requirements while delivering excellent performance. The ispLSI and pLSI family of high-speed, high-density PLDs supported by easy-to-use effective software for fast design implementation and verification.

Design Entry and Optimization

After the functional partitioning and component specifications are completed, the logic necessary to implement the functions is defined block by block. The logic may include standard TTL functions, CMOS logic functions, or functions from a library, such as the Lattice Semiconductor Corporation (LSC) Macro or TTL library. The implementation of logic into a high density device is optimized for the targeted device by the design software. The partitioning also affects the optimization. Optimization can be for speed, utilization or a combination of both.

Logic entry for an LSC high-density device is done with the pLSI/ispLSI Development System (pDS) or with any of the third-party CAE tools supported by LSC's pDS+ Fitters. The pDS software utilizes the Graphical User Interface (GUI) of Microsoft's Windows™ to provide a complete design flow from logic entry to programming ispLSI/pLSI devices within hours. pDS+ Fitters, in conjunction with third-party CAE tools, support textual design entry using a Hardware Description Language (HDL); standard CAE schematic design entry; and/or Boolean, truth table or state machine entry.

Test and Debug

When designing a system, or a portion of a system, it is easier to test and debug pieces or modules rather than the entire system. In this manner, the designer can

confirm module designs, or functional blocks, and find problems earlier in the design cycle.

Logic can be verified by either timing simulation or actual testing of the programmed device. Simulation can be accomplished using a variety of logic simulators. Design errors detected by software simulation can be corrected by the designer before the printed circuit board is laid out and manufactured, which saves time and reduces cost. Board and system level simulation can be accomplished through behavioral simulation using Synopsys Logic Modeling Division models.

Reprogrammable devices allow the designer to test, debug, and modify logic right on the p.c. board. ispLSI and pLSI devices can be reprogrammed multiple times. This reprogrammability further assists the designers by allowing them to temporarily program the devices with diagnostic and design verification logic.

The designer should always attempt to design logic with testability in mind. Testability means different things to different designers. Key guidelines to be aware of are:

- ❑ Large counters should be segmented for quick and easy testing.
- ❑ Logic should be designed for controllability and observability.
- ❑ There should be no floating nets.
- ❑ All nets should be at a known state or are able to be set or reset.

To assist system testability, the ispLSI devices offer preload and verification features. These features allow register contents to be verified without using logic analyzers or other debugging tools.

Printed Circuit Board Layout

Once the logic has been verified, the Printed Circuit Board (PCB) is laid out and manufactured. Since the logic may be changed during design, this phase of the system design is usually executed after the logic has been validated. It is recommended that board design and layout be done after verifying designs using ispLSI and pLSI parts.

System Test and Debug

System test and debug is the final stage of the design process. The logic and the PCB are tested as a system and minor enhancements or bug fixes are implemented. Because of the flexibility of the ispLSI and pLSI devices, minor changes can be made without greatly affecting the layout of the PCB or the pinout of the device.

LATTICE SEMICONDUCTOR CORPORATION
5555 Northeast Moore Court
Hillsboro, Oregon 97124 U.S.A.
Tel.: (503) 681-0118
FAX: (503) 681-3037
http://www.latticesemi.com

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