Interfacing SDRAMs to Pentium Processors with 3.3V GAL® Devices

Introduction

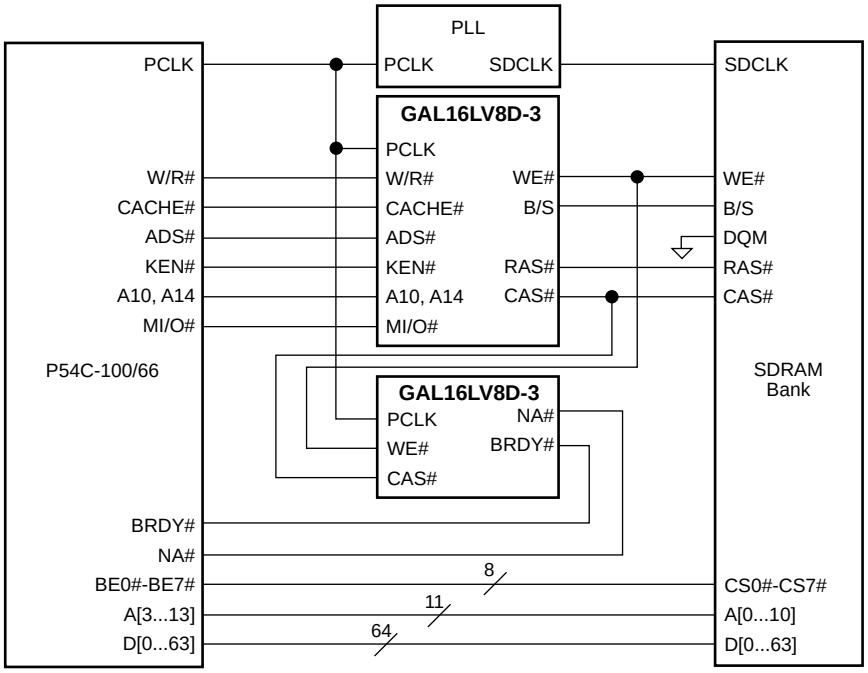
The blistering speed of today's leading-edge microprocessors necessitates the use of new memory and logic technologies. To keep up with the operating frequencies of these new microprocessors while still providing a clean memory interface, ultra-high-performance synchronous DRAMs and PLDs are required. This article discusses the design of a system based on an Intel Pentium microprocessor and Toshiba SDRAMs. The memory interface between the Pentium and the SDRAMs is implemented using Lattice 3.3 volt Generic Array Logic (GAL) programmable logic devices. For the purpose of this design, the Pentium P54C-100/66 processor, operating at a 100 MHz internal frequency and a 66 MHz bus frequency, was used. The bus frequency of the processor is vitally important in the design of the synchronous memory interface, as will be shown later in this article. A 2M x 64 SDRAM bank consisting of eight pieces of 2M x 8 SDRAM is used in the design. The design can be easily modified to support a 2M x 32 SDRAM bank, since the Pentium supports a 32-bit memory interface by connecting the Pentium's A2 address to the appropriate memory address.

Design Implementation

Due to the speed of the system, a phase-locked loop (PLL) circuit is used in the design (see Figure 1). The PLL can reside either on the motherboard or on the SDRAM memory module, if one exists. Note that the current JEDEC SDRAM dual in-line memory module (DIMM) specification recommends that a PLL be placed on the DIMM, between the processor clock and the SDRAM clocks. As for the choice of PLL, a Motorola MC952 is used. This device is used in some SDRAM modules currently available. The memory interface was designed using 3.3 volt Lattice GAL devices.

As mentioned earlier, the design uses a Pentium operating at a 66 MHz external bus, which translates to a 15.15 ns clock cycle time. The high-speed Toshiba SDRAM (part number TC59S1608AFT-10) clock frequency is 100 MHz, which is the equivalent of a 10 ns clock cycle time. The GAL devices need to be 5 ns or faster in order to incorporate two levels of logic into the 10 ns clock cycle. These timing requirements are easily met by the 3.5 ns 3.3 volt GAL16LV8D-3LJ devices from Lattice Semiconductor. This device is a registered GAL with 16 inputs and

Figure 1. Pentium/SDRAM Interface



8 outputs, 3.5 ns maximum propagation delay (Tpd), 2.5 ns maximum clock-to-output delay (Tco), and 200 MHz operating frequency (Fmax). Any one of the registered outputs may be bypassed. The memory interface logic was implemented using two GAL16LV8D-3LJ devices. The first GAL is used to generate the RAS# and CAS# signal to the memory bank. The second GAL device is used to generate NA# and BRDY#. The ABEL equations for the two GAL16LV8D devices are shown in Listing 1.

Other signals in the design do not require additional control logic. Each of the eight Pentium byte-enable signals is tied directly to the chip-select signal of one of the SDRAM banks. In this way, each SDRAM will provide the byte corresponding to its location when selected. Pentium addresses A3-A13 are connected to SDRAM addresses A0-A10 directly, and the 64 data lines on the SDRAM bus are directly connected to D0-D63 of the Pentium. Alternatively, the designer may consider isolating the memory bus by using a very fast bi-directional buffer, such as a 244 device. And, finally, the DQM signal is connected to ground since read data is not being tristated, and write data is not being masked. (The DQM signal, when sampled high, places the outputs in high-Z state in a Read cycle and acts as an out mask in a Write cycle.) Figure 2 shows an example of an interleaved bank read cycle. For the purposes of this article, the CAS latency (the number of clocks from the time the CAS# signal is asserted low until the time that the first byte of data is read) is set to three cycles, which is equivalent to 30 ns. Also, the burst length is set to 4.

Acknowledgement

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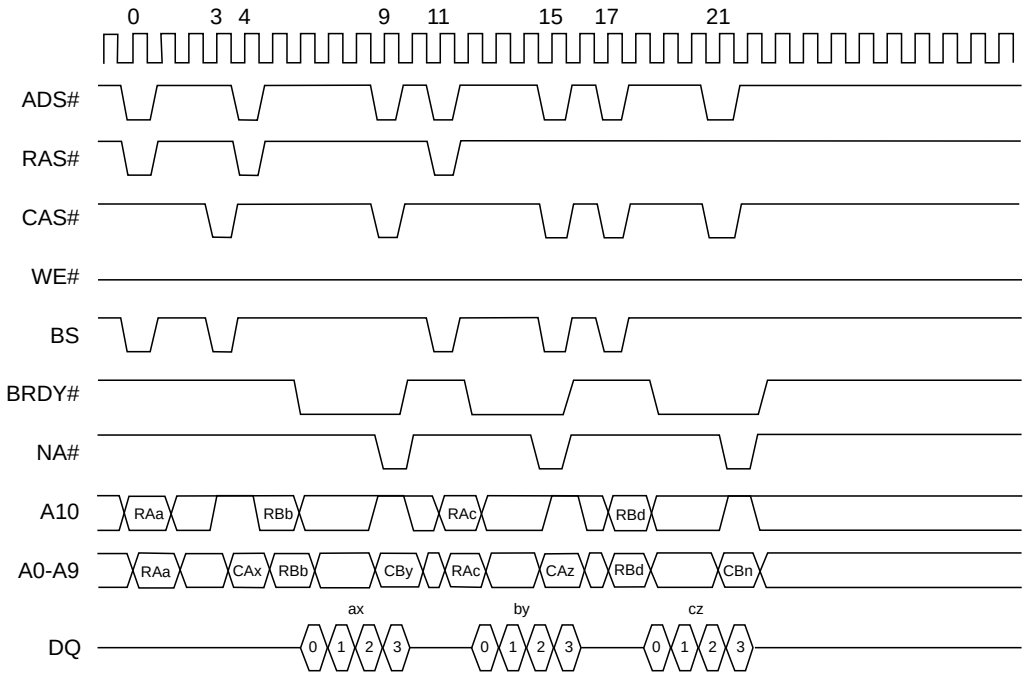
Figure 2. Interleaved Bank Read



Listing 1. ABEL Files for the Design Module

```
module psdram1
title 'pentium sdram interface 1
                                u1      device    'P16R8' ;
Pclk, !WR, !Cache, !ADS, !KEN           pin        1, 2, 3, 5, 6 ;
A10, A14                                pin        7, 8 ;
!WE                                     pin        19 ;
BS                                      pin        12 ;
!RAS                                    pin        13 ;
!CAS                                    pin        14 ;
Q2, Q3, Q4                              pin        16, 17, 18 ;
MIO                                     pin        4

equations

BS = A14 ;
!WE = !ADS & MIO & !Cache & KEN & WR ;
!RAS := !ADS & MIO & !Cache ;
!Q2 := !RAS ;
!Q3 := !Q2 ;
!Q4 := !Q3 ;
!CAS := (!WE & !Q2) # (WE & !Q4) ;

end psdram1

module psdram2
title 'pentium sdram interface 2

                                u2      device    'P16R8';
                   Pclk, !WE, !CAS      pin        1, 2, 3 ;
                        !BRDY, !NA      pin        12, 13 ;
                Q4, Q5, Q6, Q7, Q8      pin        14, 15, 16, 17, 18 ;

equations

!NA := (!WE & !Q6) # (WE & !Q9) ;
!BRDY := (WE & !Q6 & !Q7 & !Q8 & !Q9) # (!WE & !CAS & !Q4 & !Q5 & !Q6) ;
!Q4 := !CAS ;
!Q5 := !Q6 ;
!Q6 := !Q5 ;
!Q7 := !Q6 ;
!Q8 := !Q7 ;
!Q9 := !Q8 ;
```

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