pDS+™ OrCAD Software

Features

- **ispLSI® AND pLSI® DEVELOPMENT SYSTEM**
  - **— Supports ispLSI and pLSI 1000/E and 2000**
  - **— Upgrade to Support ispLSI and pLSI 3000**
- **SUPPORTS OrCAD SDT 386+ OR CAPTURE FOR WINDOWS DEVELOPMENT ENVIRONMENT FOR DESIGN ENTRY**
  - **— Schematic Entry**
  - **— Over 300 "TTL-Like" Macros**
  - **— Graphical, Menu-Driven Interface**
  - **— Command Line Driven User Interface**
- **SUPPORTS OrCAD PLD 386+ DESIGN ENVIRONMENT FOR BOOLEAN DESIGN ENTRY**
- **LATTICE SEMICONDUCTOR pDS+ OrCAD FITTER**
  - **— Multi-Level Logic Synthesis**
  - **— Efficient Design Optimization and Minimization**
  - **— Automatic Mapping and Device Fitting**
  - **— Automatic Partitioning with High Utilization**
  - **— Predictable Performance**
- **COMPLETE DESIGN VERIFICATION**
  - **— Using OrCAD's VST 386+ Simulator or Simulate for Windows**
- **INDUSTRY STANDARD PROGRAMMING FILE GENERATION**
  - **— Standard JEDEC Device Fuse Map**
- **IN-SYSTEM PROGRAMMING SUPPORT**
  - **— ispCODE™ C Source Routines Included**
  - **— ISP Daisy Chain Download**
  - **— ispATE™ Board Test Programming Utility**
- **PLATFORMS SUPPORTED**
  - **— PC DOS/WIndows 3.1/Windows 95/Windows NT**

Introduction

The pDS+ OrCAD Software from Lattice Semiconductor Corporation (LSC) offers a powerful solution to fit high density logic designs into Lattice Semiconductor's ispLSI and pLSI devices.

Design entry, simulation, and implementation are made simple using tools such as Capture for Windows from OrCAD (see figure 1). The OrCAD software and pDS+ Fitter support high level, device independent design entry together with efficient logic compilation, delivering the most complex designs in the shortest time possible.

OrCAD Software

OrCAD supports schematic entry using its Schematic Design Tools (SDT 386+) or Capture for Windows v6.1 software (see figure 2). The OrCAD capture tools work with Lattice Semiconductor's library of over 300 TTL-like macros to let you create designs without regard to any specific device dependencies. They offer advanced features such as cut and paste, unlimited zoom and pan functions, automatic symbol generation as well as many other features to streamline and speed-up the design and verification process. OrCAD also supports schematic/Boolean Equation entry using the PLD 386+ tool. Schematics, using an OrCAD primitive library, can be incorporated and processed by the PLD 386+ tool. A PLD 386+ file for Boolean Equation entry (using OrCAD HDL) can be generated and processed. The ESP environment also supports optional timing simulation, using the OrCAD Verification and Simulation software, so designs can be fully simulated before device programming. The menu-driven environment makes design implementation as easy as a single click of the mouse button. Results can also be dynamically back annotated to the schematic for design verification.

pDS+ OrCAD Fitter

The pDS+ OrCAD Fitter for ispLSI and pLSI devices is executed as a standalone program, using the OrCAD EDIF output from capture tools or the PLA output from PLD 386+ as an input. Figure 3 shows the design flow for pDS+ OrCAD. The design flow is as follows:

— Create a design using either Capture or PLD 386+.

— Perform a pre-route simulation utilizing the OrCad simulator.

— Create either an EDIF file or a PLA file.

— Compile either your EDIF or PLA file with the pDS+ OrCAD fitter to generate a .ifo and .dba file for simulation and JEDEC, LOG and report files for programming and device debug.

— Perform a post-route simulation in OrCAD using the Lattice Semiconductor timing simulation library and OrCAD's simulator.

— Program the selected device.

LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037; http://www.latticesemi.com

Figure 1. OrCAD Capture for Windows

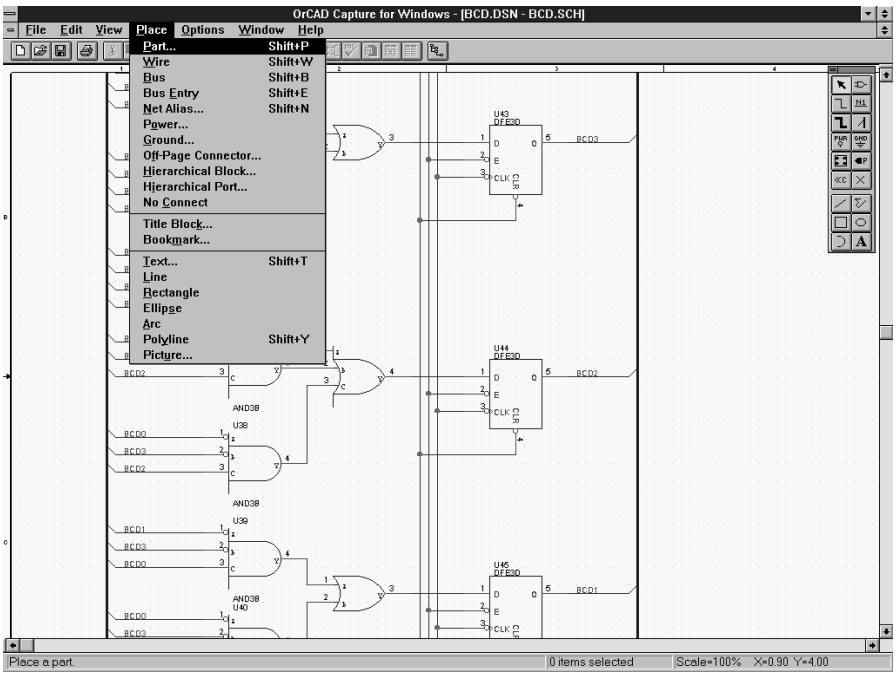


Figure 2. OrCAD SDT 386+ Environment

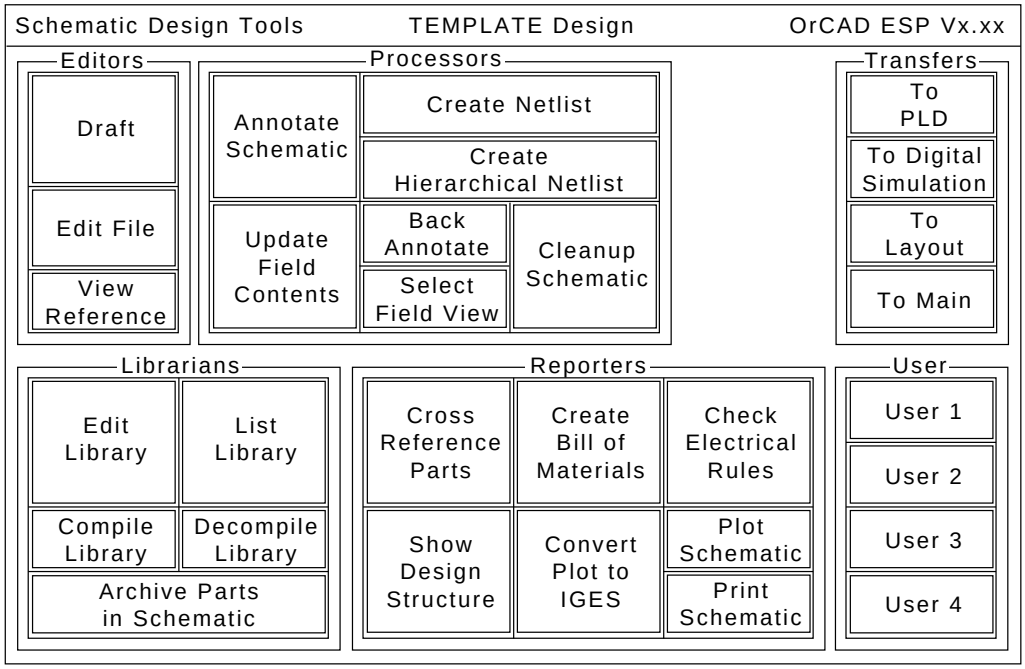
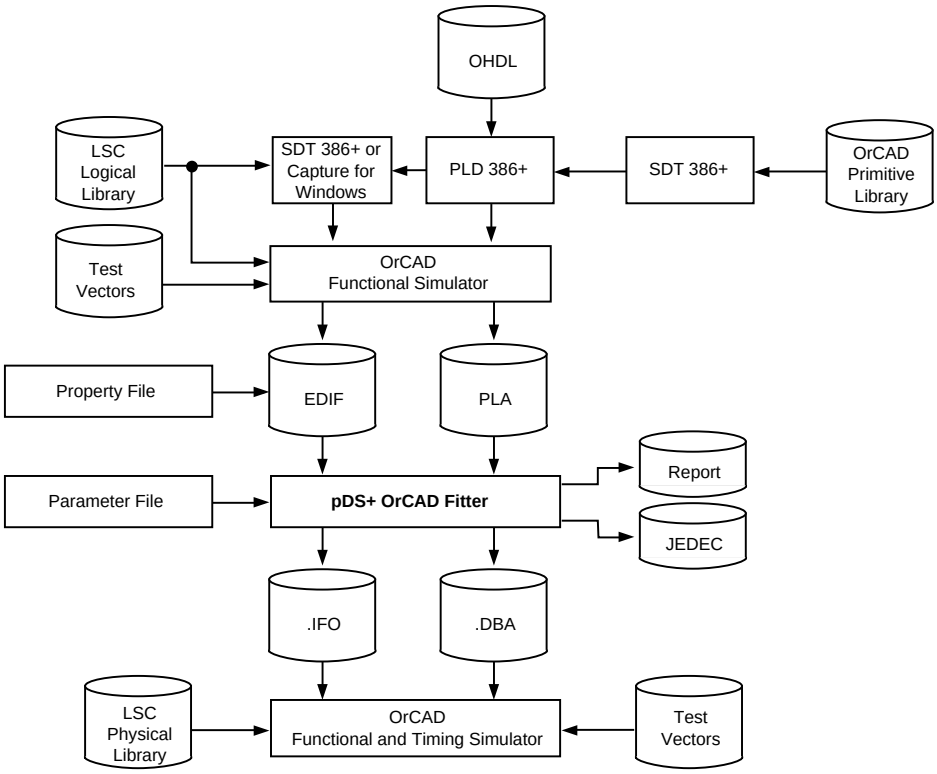


Figure 3. pDS+ OrCAD Design Flow



The pDS+ OrCAD Fitter provides hands-off design implementation through intelligent design optimization, logic partitioning, automatic place and route and fusemap generation for programming.

pDS+ OrCAD Macro Library

The pDS+ OrCAD software offers an extensive selection of over 300 TTL-like macros. These macros enable the design engineer to use familiar predefined functions to build a design. Table 1 shows a summary of the available macros in the pDS+ software.

Table 1. Macro Summary

Macro Type	Quantity
AND/NAND	29
OR/NOR	24
XOR/XNOR	12
I/Os	89
Flip-Flops	39
Latches	30
Arithmetic	33
Counters	65
Shift Registers	15
Miscellaneous	45

Design Optimization and Logic Minimization

The pDS+ OrCAD Fitter uses proprietary logic synthesis algorithms targeted for device-specific features. The fitter performs a thorough design optimization, utilizing logic minimization, product term sharing and XOR functions wherever necessary. In addition, the pDS+ OrCAD Fitter supports multiple fitting strategies to obtain the best device utilization and performance.

Automatic Partitioning

The pDS+ OrCAD Fitter incorporates a powerful Automatic Partitioner for hands-free synthesis of a design into Generic Logic Blocks (GLBs). The partitioner takes full advantage of the device's powerful features such as the hard XOR and product term sharing. The internal XOR can be utilized for arithmetic functions, T-Type flip-flops, and on and offset optimization functions. The partitioner also makes extensive use of product term sharing. Product term sharing allows the Fitter to efficiently use device resources by sharing product terms across multiple logic functions. These features combine to maximize device resource utilization and increase design performance.

Automatic Place and Route

Automatic place and route eliminates the need for manual editing and accelerates the design cycle. The Router automatically generates pinouts based on the optimal design implementation or user assigned pinouts.

The Extended Route option performs a comprehensive route to maximize device resource utilization and ensure efficient design implementation.

Design Parameter Control

The pDS+ OrCAD Fitter offers extensive design parameter control at the design entry level, letting the user optimize the design for maximum utilization and/or speed. All of the controls are specified using “Attributes” in the ESP or Capture for Windows design environment or in property and parameter files. These controls fall into two categories:

- — Fitter Controls
- — Design Implementation Controls
  - — Net Attributes
  - — Pin Attributes
  - — Path Attributes
  - — Symbol Attributes

Fitter Control Options

Special properties can be passed to the pDS+ OrCAD Fitter providing complete control over critical design considerations. Fitter control over design partitioning and routing optimizes the design for speed and/or device utilization. Here are a few of the powerful features:

Feature	Description
PART	Determines device type to be used.
PARAM_FILE	Allows user to specify attributes in a text file.
STRATEGY	Choice of AREA (default), DELAY or NO_OPTIMIZE. AREA optimizes device space, DELAY keeps GLB levels to a minimum and NO_OPTIMIZE does not reduce equations.
USE_GLOBAL_RESET	Causes global reset to use dedicated routing for reset.
MAX_GLB_OUT	Specifies maximum number of outputs from a GLB. Default is 4.
MAX_GLB_IN	Controls maximum number of inputs to a GLB. Default is 16 for 1K and 2K devices and 24 for 3K devices.
EFFORT	Controls optimization of partitioner.
EXTENDED_ROUTE	Choice of OFF (fixed) or ON (extended, default).
PIN_FILE	Specifies locked pin assignments.

Design Implementation Controls

Device controls are used for changing design parameters such as security. Some of these implementation controls are:

Feature	Description
ISP	Instructs Router to reserve in-system programming pins.
ISP_EXCEPT_Y2	Reserves all ISP pins except Y2 (ispLSI and pLSI 1016/E and 2032 only).
Y1_AS_RESET	Uses Y1 clock pin on ispLSI and pLSI 1016/E and 2032 as a global reset pin.
SECURITY	Sets the device security cell to prevent unauthorized fuse map read back.

Net Attributes

These properties control how the design is mapped into the specified features of the target device:

Feature	Description
CLK0-CLK2	Assigns a CLK signal to a dedicated CLK line.
IOCLK0-IOCLK1	Assigns a CLK signal to a dedicated IOCLK line if single fanout input pin.
FASTCLK	Fitter assigns CLK signal to CLK0-CLK2 or IOCLK0-IOCLK1.
SLOWCLK	Assigns the CLK signal to a GLB product term CLK.

Feature	Description
PRESERVE	Prevents logic minimization on specified nets.
GROUP	Suggests grouping of functions in a GLB.

Pin Attributes

Feature	Description
CRIT	Specifies Output Routing Pool Bypass to minimize delay.
SLOWSLEW	Assigns slow slew rate on a specific I/O cell.
LOCK	Assigns device I/O pins to design I/O ports.
PULLUP	Specifies internal pull-up resistors.

Path Attributes

The following properties specify paths in the design that have special fitting requirements:

Feature	Description
SAP/EAP	Defines asynchronous paths to prevent signal duplication.
SCP/ECP	Defines critical paths to reduce delays.
SNP/ENP	Defines logic paths for no logic minimization.

Symbol Attributes

Feature	Description
REGTYPE	Determines where a register is to be placed (IOC or GLB).
PROTECT	Prevents removal of a primitive or a macro during minimization.
OPTIMIZE	Selects either hard or soft macros.

Parameter File

The pDS+ OrCAD Fitter provides the ability to use a parameter file (design.par) feature which helps designers eliminate guesswork and optimize the designs for the right devices. It allows the user to try a number of design implementation options using all of the fitter control options in a batch mode. The parameter file instructs the partitioner and the router to maximize both device utilization and performance and helps speed the design process.

Property File

The pDS+ OrCAD Fitter also accepts a property file (design.prp) which allows the designer to assign specific features to signal and nets using all of the design attributes available. The property file helps guide the fitter in implementing the design in the most efficient way.

Design Verification

The pDS+ OrCAD Fitter also provides a post route design file for optional timing simulation. The pDS+ OrCAD software offers complete post route design verification using the optional OrCAD timing simulator. The pDS+ OrCAD Fitter generates the files required for simulation, and generates a "sim" file which can be used with behavioral simulation models from Synopsys Logic Modeling Division.

Fuse Map Generation

The pDS+ OrCAD software generates a device fuse map in standard JEDEC format. A security feature offers protection of proprietary designs from unauthorized duplication. The Fitter also appends any design test vectors in JEDEC format to the device fusemap thus facilitating a quick, easy functional verification of a programmed device.

System Requirements (PC Platform)

- 486/Pentium™ IBM Compatible PC
- Operating System
  - MSDOS Version 4.x or Later
  - Windows 3.1
  - Windows NT
  - Windows 95
- 16 MB RAM with 30MB Hard Disk Space
- Parallel Printer Port for Software Key

Programmer Support

All devices in the ispLSI device families can be programmed while installed on the target circuit board. In-system programming can be performed using an ispDOWNLOAD™ Cable and PC, by an on-board microprocessor or by ATE systems during final board test.

All ispLSI and pLSI devices can also be programmed using third-party PLD programmers. The devices are currently supported by programmers from the following vendors:

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30A/B
System General	TURPRO-1/FX

High pin-count socket adapters are available from Emulation Technology, EDI Corporation and PROCON.

Product Ordering Information

Product Code	Description
pDS2170-PC1	pDS+ OrCAD Fitter & Libraries (PC)
pDS1170-PC1	OrCAD Library & Interface (PC)
pDS2170-3UP/PC1	3000 Family Support for pDS+ OrCAD Fitter

Annual Maintenance*

pDS2170M-PC1	Maintenance for pDS2170-PC1
pDS1170M-PC1	Maintenance for pDS1170-PC1

*One year of maintenance is provided with every product purchase.

Warranty/Update Service

- 90-day warranty on disk media
- One-year maintenance support included with purchase
- Annual maintenance agreement available

Technical Support Assistance

Hotline:	1-800-LATTICE (Domestic) 1-408-428-6414 (International)
BBS:	1-408-428-6417
FAX:	1-408-944-8450
email:	apps@latticesemi.com

LATTICE SEMICONDUCTOR CORPORATION
5555 Northeast Moore Court
Hillsboro, Oregon 97124 U.S.A.
Tel.: (503) 681-0118
FAX: (503) 681-3037
http://www.latticesemi.com

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