# ispLSI® and pLSI® 3256E

## High Density Programmable Logic

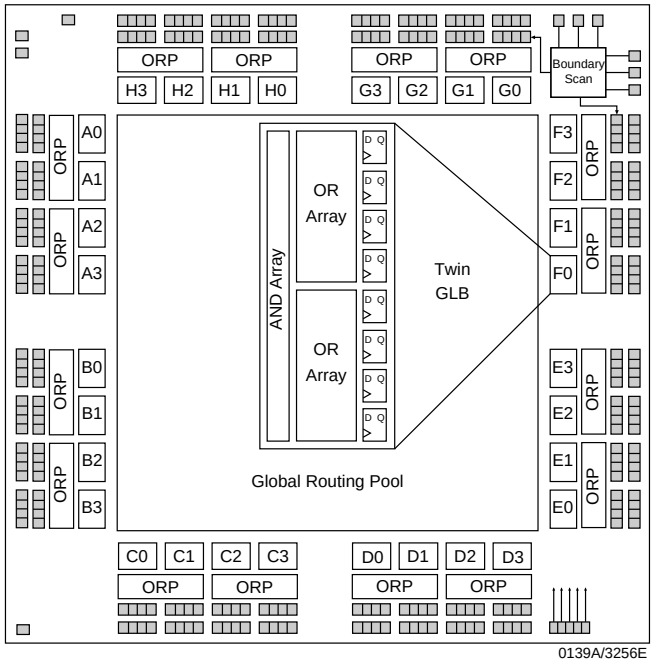
## Features

- **HIGH-DENSITY PROGRAMMABLE LOGIC**
  - **— 256 I/O Pins**
  - **— 11000 PLD Gates**
  - **— 512 Registers**
  - **— High Speed Global Interconnect**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— $f_{max}$ = 100 MHz Maximum Operating Frequency**
  - **— $t_{pd}$ = 10 ns Propagation Delay**
  - **— TTL Compatible Inputs and Outputs**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile**
  - **— 100% Tested at Time of Manufacture**
  - **— Unused Product Term Shutdown Saves Power**
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - **— In-System Programmable™ (ISP™) 5-Volt Only**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market, and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Debugging**
- **100% IEEE 1149.1 BOUNDARY SCAN COMPATIBLE**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **— Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **— Five Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Programmable Output Slew Rate Control to Minimize Switching Noise**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispLSI AND pLSI DEVELOPMENT TOOLS**

  **pDS® Software**
  - **— Easy to Use PC Windows™ Interface**
  - **— Boolean Logic Compiler**
  - **— Manual Partitioning**
  - **— Automatic Place and Route**
  - **— Static Timing Table**

  **pDS+™ Software**
  - **— Industry Standard, Third Party Design Environments**
  - **— Schematic Capture, State Machine, HDL**
  - **— Automatic Partitioning and Place and Route**
  - **— Comprehensive Logic and Timing Simulation**
  - **— PC and Workstation Platforms**

## Functional Block Diagram




0139A/3256E

## Description

The ispLSI and pLSI 3256E are High Density Programmable Logic Devices which contain 512 Registers, 256 Universal I/O pins, five Dedicated Clock Input Pins, sixteen Output Routing Pools (ORP), and a Global Routing Pool (GRP) which allows complete inter-connectivity between all of these elements. The ispLSI 3256E features 5-Volt in-system programmability and in-system diagnostic capabilities. The ispLSI 3256E offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 3256E devices.

The basic unit of logic on the ispLSI and pLSI 3256E devices is the Twin Generic Logic Block (Twin GLB) labelled A0, A1...H3. There are a total of 32 of these Twin GLBs in the ispLSI and pLSI 3256E devices. Each Twin GLB has 24 inputs, a programmable AND array and two OR/Exclusive-OR Arrays, and eight outputs which can be configured to be either combinatorial or registered. All Twin GLB inputs come from the GRP.



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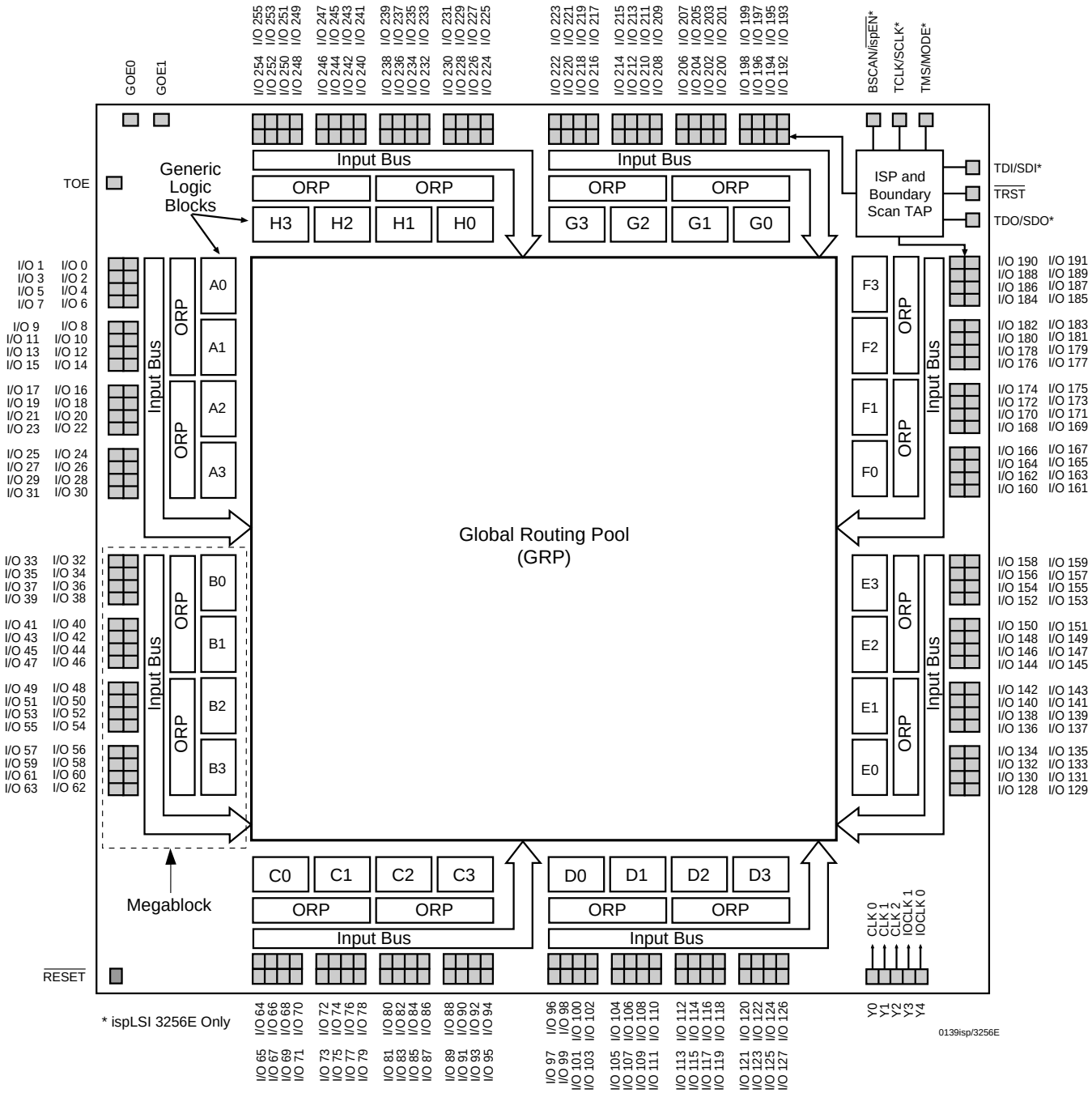
## Functional Block Diagram

**Figure 1. ispLSI and pLSI 3256E Functional Block Diagram**



## Description (continued)

All local logic block outputs are brought back into the GRP so they can be connected to the inputs of any other logic block on the device. The device also has 256 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, a registered input, a latched input, an output or a bidirectional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

The 256 I/O Cells are grouped into sixteen sets of 16 bits. Pairs of these I/O groups are associated with a logic Megablock through the use of the ORP. Each Megablock is able to provide one Product Term Output Enable (PTOE) signal which is globally distributed to all I/O cells. That PTOE signal can be generated within any GLB in the Megablock. Each I/O cell can select either a Global OE or a PTOE.

Four Twin GLBs, 32 I/O Cells and two ORPs are connected together to make a logic Megablock. The Megablock is defined by the resources that it shares. The outputs of the four Twin GLBs are connected to a set of 32 I/O cells by the ORP. The ispLSI and pLSI 3256E device contains eight of these Megablocks.

The GRP has as its inputs the outputs from all of the Twin GLBs and all of the inputs from the bidirectional I/O cells. All of these signals are made available to the inputs of the Twin GLBs. Delays through the GRP have been equalized to minimize timing skew and logic glitching.

Clocks in the ispLSI and pLSI 3256E devices are provided through five dedicated clock pins. The five pins provide three clocks to the Twin GLBs and two clocks to the I/O cells.

The table below lists key attributes of the device along with the number of resources available.

An additional feature of the ispLSI and pLSI 3256E is the Boundary Scan capability, which is composed of cells connected between the on-chip system logic and the device's input and output pins. All I/O pins have associated boundary scan registers, with 3-state I/O using three boundary scan registers and inputs using one.

The ispLSI and pLSI 3256E supports all IEEE 1149.1 mandatory instructions, which include BYPASS, EXTEST and SAMPLE.

## Key Attributes of the ispLSI and pLSI 3256E

| Attribute | Quantity |
|---|---|
| **Twin GLBs** | 32 |
| **Registers** | 512 |
| **I/O Pins** | 256 |
| **Global Clocks** | 5 |
| **Global OE** | 2 |
| **Test OE** | 1 |

Table - 003/3256E

## Absolute Maximum Ratings [1]

Supply Voltage $V_{cc}$ .....-0.5 to +7.0V

Input Voltage Applied..... -2.5 to $V_{CC}$ +1.0V

Off-State Output Voltage Applied ..... -2.5 to $V_{CC}$ +1.0V

Storage Temperature..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. ($T_J$) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

## DC Recommended Operating Condition

| SYMBOL | PARAMETER | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| $T_A$ | Ambient Temperature | 0 | 70 | °C |
| $V_{CC}$ | Supply Voltage | 4.75 | 5.25 | V |
| $V_{IL}$ | Input Low Voltage | 0 | 0.8 | V |
| $V_{IH}$ | Input High Voltage | 2.0 | $V_{CC}$ +1 | V |

Table 2 - 0005/3256

## Capacitance ($T_A$=25°C,f=1.0 MHz)

| SYMBOL | PARAMETER | TYPICAL [1] | UNITS | TEST CONDITIONS |
|---|---|---|---|---|
| $C_1$ | I/O Capacitance | 10 | pf | $V_{CC}$ = 5.0V, $V_{I/O}$ = 2.0V |
| $C_2$ | Clock Capacitance | 15 | pf | $V_{CC}$ = 5.0V, $V_Y$ = 2.0V |

Table 2 - 0006/3192

1. Guaranteed but not 100% tested.

## Data Retention Specifications

| PARAMETER | MINIMUM | MAXIMUM | UNITS |
|---|---|---|---|
| Data Retention | 20 | – | Years |
| ispLSI Erase/Reprogram Cycles | 10000 | – | Cycles |
| pLSI Erase/Reprogram Cycles | 100 | – | Cycles |

Table 2- 0008B

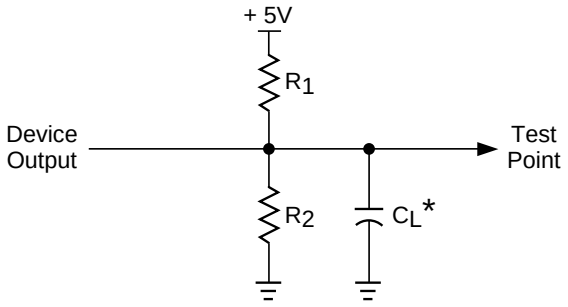
## Switching Test Conditions

| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input Rise and Fall Time | ≤ 3ns 10% to 90% |
| Input Timing Reference Levels | 1.5V |
| Ouput Timing Reference Levels | 1.5V |
| Output Load | See figure 2 |

Table 2 - 0003

3-state levels are measured 0.5V from steady-state active level.

**Figure 2. Test Load**




*$C_L$ includes Test Fixture and Probe Capacitance.

0213A

**Output Load conditions (See figure 2)**

| TEST CONDITION | | R1 | R2 | CL |
|---|---|---|---|---|
| A | | 470Ω | 390Ω | 35pF |
| B | Active High | ∞ | 390Ω | 35pF |
| | Active Low | 470Ω | 390Ω | 35pF |
| C | Active High to Z at $V_{OH}$ -0.5V | ∞ | 390Ω | 5pF |
| | Active Low to Z at $V_{OL}$ +0.5V | 470Ω | 390Ω | 5pF |

Table 2 - 0004A

## DC Electrical Characteristics

**Over Recommended Operating Conditions**

| SYMBOL | PARAMETER | CONDITION | MIN. | TYP.[3] | MAX. | UNITS |
|---|---|---|---|---|---|---|
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 8 mA | – | – | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -4 mA | 2.4 | – | – | V |
| $I_{IL}$ | Input or I/O Low Leakage Current | 0V ≤ $V_{IN}$ ≤ $V_{IL}$ (Max.) | – | – | -10 | µA |
| $I_{IH}$ | Input or I/O High Leakage Current | 3.5V ≤ $V_{IN}$ ≤ $V_{CC}$ | – | – | 10 | µA |
| $I_{IL\text{-}isp}$ | Bscan/$\overline{ispEN}$ Input Low Leakage Current | 0V ≤ $V_{IN}$ ≤ $V_{IL}$ | – | – | -150 | µA |
| $I_{IL\text{-}PU}$ | I/O Active Pull-Up Current | 0V ≤ $V_{IN}$ ≤ $V_{IL}$ | – | – | -150 | µA |
| $I_{OS}$[1] | Output Short Circuit Current | $V_{CC}$ = 5V, $V_{OUT}$ = 0.5V | – | – | -200 | mA |
| $I_{CC}$[2,4] | Operating Power Supply Current | $V_{IL}$ = 0.0V, $V_{IH}$ = 3.0V<br>$f_{TOGGLE}$ = 1 MHz | – | 300 | – | mA |

Table 2 - 0007isp/3256E

1. One output at a time for a maximum duration of one second. $V_{OUT}$ = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2. Measured using sixteen 16-bit counters.
3. Typical values are at $V_{CC}$ = 5V and $T_A$ = 25°C.
4. Maximum $I_{CC}$ varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this datasheet and Thermal Management section of the 1996 Lattice Semiconductor Data Book to estimate maximum $I_{CC}$.

## External Switching Characteristics[1, 2, 3]

**Over Recommended Operating Conditions**

| PARAMETER | TEST[5] COND. | #[2] | DESCRIPTION[1] | -100 | | -70 | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| tpd1 | A | 1 | Data Prop. Delay, 4PT Bypass, ORP Bypass | — | 10 | — | 15 | ns |
| tpd2 | A | 2 | Data Propagation Delay | — | 13 | — | 18 | ns |
| fmax | A | 3 | Clock Frequency with Internal Feedback[3] | 100 | — | 70 | — | MHz |
| fmax (Ext.) | — | 4 | Clock Freq. with Ext. Feedback,1/(tsu2 + tco1) | 77 | — | 50 | — | MHz |
| fmax (Tog.) | — | 5 | Clock Frequency, Max Toggle[4] | 100 | — | 83 | — | MHz |
| tsu1 | — | 6 | GLB Reg. Setup Time before Clock, 4PT bypass | 5.5 | — | 9 | — | ns |
| tco1 | A | 7 | GLB Reg. Clock to Output Delay, ORP bypass | — | 6.5 | — | 9 | ns |
| th1 | — | 8 | GLB Reg. Hold Time after Clock, 4PT bypass | 0 | — | 0 | — | ns |
| tsu2 | — | 9 | GLB Reg. Setup Time before Clock | 6.5 | — | 11 | — | ns |
| tco2 | — | 10 | GLB Reg. Clock to Output Delay | — | 7 | — | 10 | ns |
| th2 | — | 11 | GLB Reg. Hold Time after Clock | 0 | — | 0 | — | ns |
| tr1 | A | 12 | Ext. Reset Pin to Output Delay | — | 13.5 | — | 15 | ns |
| trw1 | — | 13 | Ext. Reset Pulse Duration | 6.5 | — | 12 | — | ns |
| tptoeen | B | 14 | Input to Output Enable | — | 16 | — | 19 | ns |
| tptoedis | C | 15 | Input to Output Disable | — | 16 | — | 19 | ns |
| tgoeen | B | 16 | Global OE Output Enable | — | 9 | — | 12 | ns |
| tgoedis | C | 17 | Global OE Output Disable | — | 9 | — | 12 | ns |
| ttoeen | — | 18 | Test OE Output Enable | — | 12 | — | 15 | ns |
| ttoedis | — | 19 | Test OE Output Disable | — | 12 | — | 15 | ns |
| twh | — | 20 | Ext. Sync. Clock Pulse Duration, High | 5 | — | 6 | — | ns |
| twl | — | 21 | Ext. Sync. Clock Pulse Duration, Low | 5 | — | 6 | — | ns |
| tsu3 | — | 22 | I/O Reg. Setup Time before Ext. Sync. Clock (Y3, Y4) | 4.5 | — | 5 | — | ns |
| th3 | — | 23 | I/O Reg. Hold Time after Ext. Sync. Clock (Y3, Y4) | 0 | — | 0 | — | ns |

1. Unless noted otherwise, all parameters use 20 PTXOR path and ORP.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions section.

Timing Ext.3256E.eps

## Internal Timing Parameters[1]

**Over Recommended Operating Conditions**

| PARAMETER | #[2] | DESCRIPTION | -100 | | -70 | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| **Inputs** | | | | | | | |
| tiobp | 24 | I/O Register Bypass | — | 2.4 | — | 4.0 | ns |
| tiolat | 25 | I/O Latch Delay | — | 4.4 | — | 7.0 | ns |
| tiosu | 26 | I/O Register Setup Time before Clock | 3.9 | — | 4.4 | — | ns |
| tioh | 27 | I/O Register Hold Time after Clock | -0.7 | — | -1.1 | — | ns |
| tioch | 28 | I/O Register Clock to Out Delay | — | 6.7 | — | 8.9 | ns |
| tior | 29 | I/O Register Reset to Out Delay | — | 5.8 | — | 7.5 | ns |
| **GRP** | | | | | | | |
| tgrp | 30 | GRP Delay | — | 2.3 | — | 3.2 | ns |
| **GLB** | | | | | | | |
| t4ptbp | 31 | 4 Product Term Bypass Path Delay (Comb.) | — | 3.2 | — | 3.6 | ns |
| t4ptbr | 32 | 4 Product Term Bypass Path Delay (Reg.) | — | 3.1 | — | 4.8 | ns |
| t1ptxor | 33 | 1 Product Term/XOR Path Delay | — | 4.0 | — | 5.1 | ns |
| t20ptxor | 34 | 20 Product Term/XOR Path Delay | — | 4.1 | — | 5.2 | ns |
| txoradj | 35 | XOR Adjacent Path Delay[3] | — | 4.3 | — | 5.7 | ns |
| tgbp | 36 | GLB Register Bypass Delay | — | 1.5 | — | 1.6 | ns |
| tgsu | 37 | GLB Register Setup Time before Clock | 0.3 | — | 1.2 | — | ns |
| tgh | 38 | GLB Register Hold Time after Clock | 5.0 | — | 7.6 | — | ns |
| tgco | 39 | GLB Register Clock to Output Delay | — | 1.6 | — | 3.0 | ns |
| tgro | 40 | GLB Register Reset to Output Delay | — | 5.2 | — | 5.2 | ns |
| tptre | 41 | GLB Product Term Reset to Register Delay | — | 4.0 | — | 4.4 | ns |
| tptoe | 42 | GLB Product Term Output Enable to I/O Cell Delay | — | 6.5 | — | 6.9 | ns |
| tptck | 43 | GLB Product Term Clock Delay | 3.0 | 3.6 | 3.4 | 4.2 | ns |
| **ORP** | | | | | | | |
| torp | 44 | ORP Delay | — | 1.2 | — | 1.9 | ns |
| torpbp | 45 | ORP Bypass Delay | — | 0.7 | — | 0.9 | ns |

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Timing Int.3256E.eps

## Internal Timing Parameters[1]

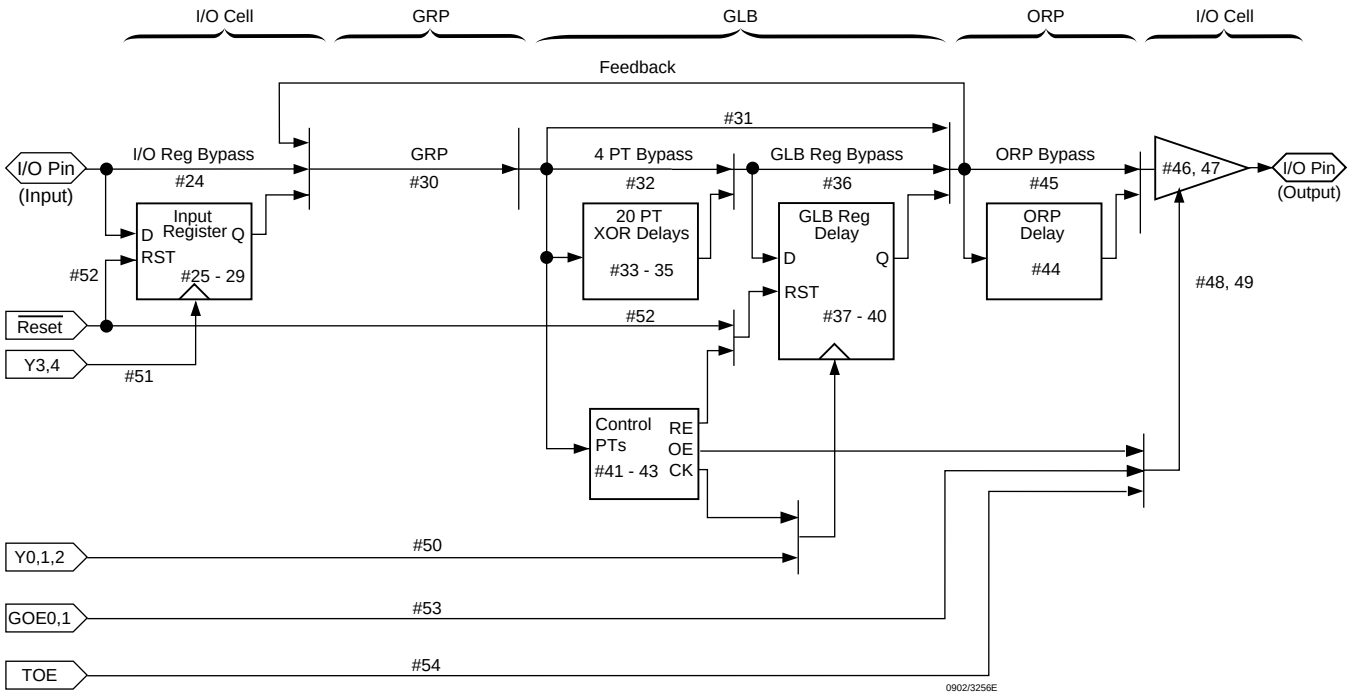
**Over Recommended Operating Conditions**

| PARAMETER | #[2] | DESCRIPTION | -100 | | -70 | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| **Outputs** | | | | | | | |
| **t**ob | 46 | Output Buffer Delay | — | 2.6 | — | 3.3 | ns |
| **t**obs | 47 | Output Buffer Delay, Slow Slew | — | 17.6 | — | 18.3 | ns |
| **t**oen | 48 | I/O Cell OE to Output Enabled | — | 5.5 | — | 5.7 | ns |
| **t**odis | 49 | I/O Cell OE to Output Disabled | — | 5.5 | — | 5.7 | ns |
| **Clocks** | | | | | | | |
| **t**gy0/1/2 | 50 | Clock Delay, Y0 or Y1 or Y2 to Global GLB Clk Line | 1.6 | 1.6 | 1.8 | 1.8 | ns |
| **t**ioy3/4 | 51 | Clock Delay, Y3 or Y4 to I/O Cell Global Clock Line | 0.3 | 1.6 | 0.8 | 2.5 | ns |
| **Global Reset** | | | | | | | |
| **t**gr | 52 | Global Reset to GLB and I/O Registers | — | 4.5 | — | 4.6 | ns |
| **t**goe | 53 | Global OE Pad Buffer | — | 5.9 | — | 7.5 | ns |
| **t**toe | 54 | Test OE Pad Buffer | — | 6.1 | — | 8.9 | ns |

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

Timing Int.2.3256E.eps

## ispLSI and pLSI 3256E Timing Model




### Derivations of tsu, th and tco from the Product Term Clock[1]

**t**su = Logic + Reg su - Clock (min)
= (**t**iobp + **t**grp + **t**20ptxor) + (**t**gsu) - (**t**iobp + **t**grp + **t**ptck(min))
= (#24+ #30+ #34) + (#37) - (#24+ #30+ #43)
1.4 ns = (2.4 + 2.3 + 4.1) + (0.3) - (2.4 + 2.3 + 3.0)

**t**h = Clock (max) + Reg h - Logic
= (**t**iobp + **t**grp + **t**ptck(max)) + (**t**gh) - (**t**iobp + **t**grp + **t**20ptxor)
= (#24+ #30+ #43) + (#38) - (#24+ #30+ #34)
4.5 ns = (2.4 + 2.3 + 3.6) + (5.0) - (2.4 + 2.3 + 4.1)

**t**co = Clock (max) + Reg co + Output
= (**t**iobp + **t**grp + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
= (#24 + #30 + #43) + (#39) + (#44 + #46)
13.7 ns = (2.4 + 2.3 + 3.6) + (1.6) + (1.2 + 2.6)

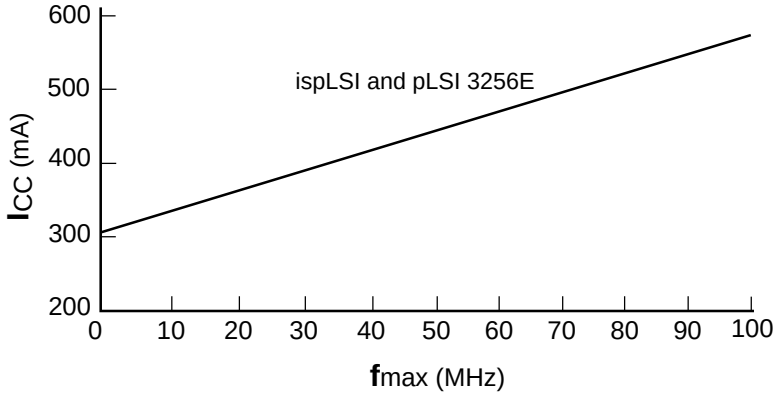
Table 2- 0042-3256E

Note: Calculations are based upon timing specifications for the ispLSI and pLSI 3256E-100L.

## Power Consumption

Power Consumption in the ispLSI and pLSI 3256E device depends on two primary factors: the speed at which the device is operating and the number of product terms used. Figure 3 shows the relationship between power and operating speed.

**Figure 3. Typical Device Power Consumption vs fmax**




Notes: Configuration of 16 16-bit Counters
Typical Current at 5V, 25° C

$I_{CC}$ can be estimated for the ispLSI and pLSI 3256E using the following equation:

$I_{CC}$ = 60 + (# of PTs * 0.48) + (# of nets * Max. freq * 0.0106) where:
# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max. freq = Highest Clock Frequency to the device

The $I_{CC}$ estimate is based on typical conditions ($V_{CC}$ = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of $I_{CC}$ is sensitive to operating conditions and the program in the device, the actual $I_{CC}$ should be verified.

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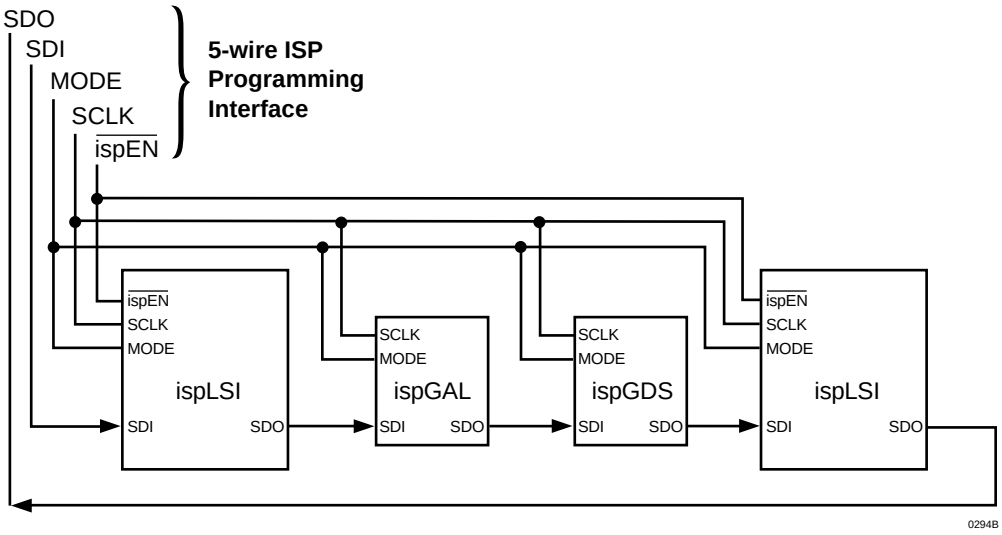
## In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice Semiconductor high density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile $E^2$CMOS cells will not lose the pattern even when the power is turned off.

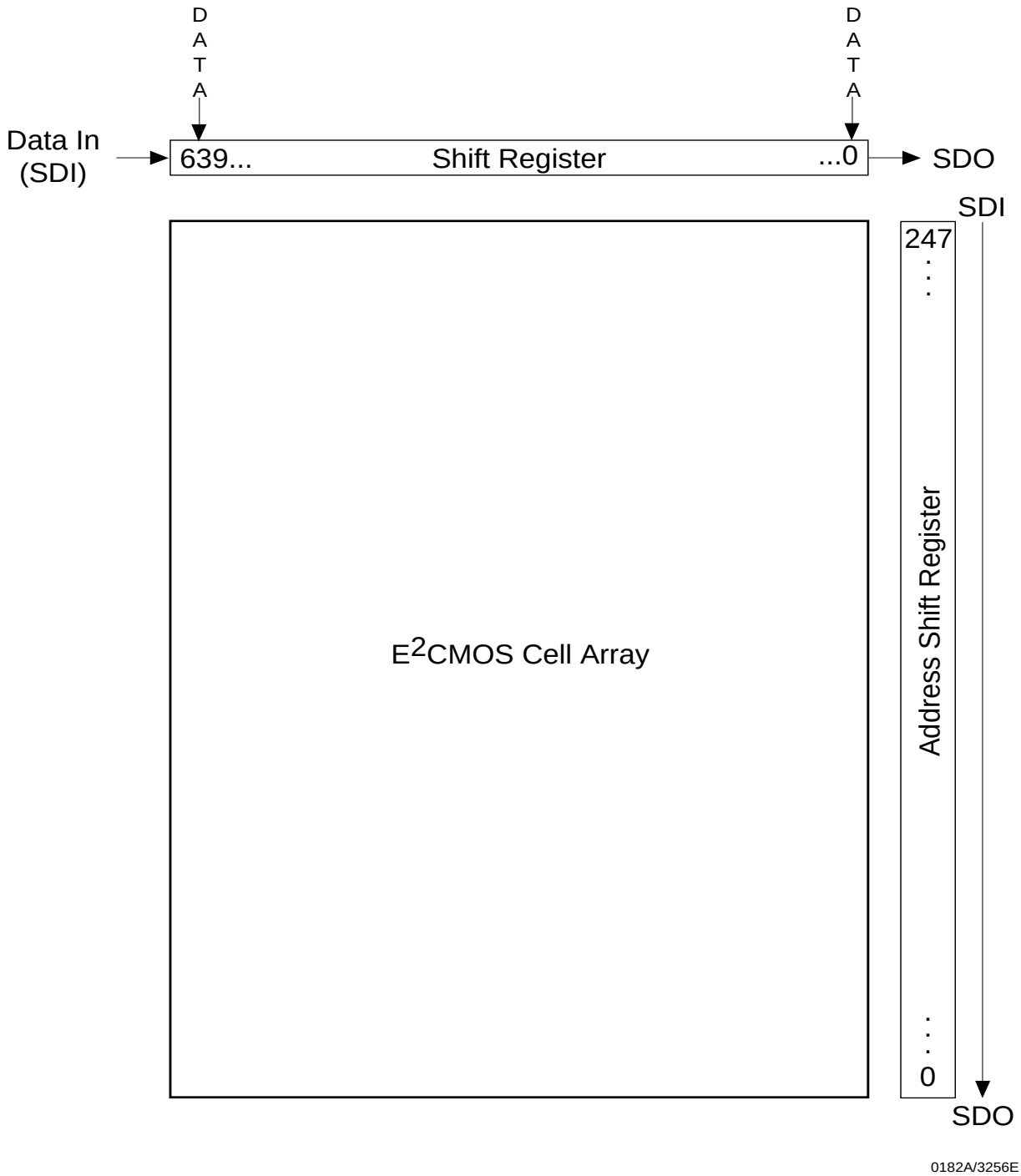
All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The simple signals for interface include isp™ Enable ($\overline{\text{ispEN}}$), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 4 illustrates the block diagram of one possible scheme of the programming interface for the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the ISP Architecture and Programming section in the 1996 Lattice Semiconductor Data Book.

The device identifier for the ispLSI 3256E is 0010 0011 (23 hex). This code is the unique device identifier which is generated when a read ID command is performed.

**Figure 4. ISP Programming Interface**



## ispLSI 3256E Shift Register Layout




Note: A logic “1” in the address shift register enables the row for programming or verification. A logic “0” disables it.

## Pin Description

| NAME | MQFP PIN NUMBERS | DESCRIPTION |
|---|---|---|
| I/O 0 - I/O 7 | 40 41 42 44 45 46 47 48 | Input/Output Pins - These are the general purpose I/O pins used by the logic array. |
| I/O 8 - I/O 15 | 50 51 52 54 55 56 57 58 | |
| I/O 16 - I/O 23 | 60 61 62 64 65 66 67 68 | |
| I/O 24 - I/O 31 | 70 71 72 74 75 76 78 79 | |
| I/O 32 - I/O 39 | 80 81 82 83 84 86 87 88 | |
| I/O 40 - I/O 47 | 89 90 91 92 93 94 96 97 | |
| I/O 48 - I/O 55 | 98 99 100 101 102 103 104 106 | |
| I/O 56 - I/O 63 | 107 108 109 110 111 112 113 114 | |
| I/O 64 - I/O 71 | 116 117 118 119 120 121 122 123 | |
| I/O 72 - I/O 79 | 124 126 127 128 129 130 131 132 | |
| I/O 80 - I/O 87 | 133 134 136 137 138 139 140 141 | |
| I/O 88 - I/O 95 | 142 143 144 146 147 148 149 150 | |
| I/O 96 - I/O 103 | 151 152 154 156 157 158 159 160 | |
| I/O 104 - I/O 111 | 162 163 164 166 167 168 169 170 | |
| I/O 112 - I/O 119 | 172 173 174 176 177 178 179 180 | |
| I/O 120 - I/O 127 | 182 183 184 186 187 188 189 190 | |
| I/O 128 - I/O 135 | 192 193 194 196 197 198 199 200 | |
| I/O 136 - I/O 143 | 202 203 204 206 207 208 209 210 | |
| I/O 144 - I/O 151 | 212 213 214 216 217 218 219 220 | |
| I/O 152 - I/O 159 | 222 223 224 226 227 228 230 231 | |
| I/O 160 - I/O 167 | 232 233 234 235 236 238 239 240 | |
| I/O 168 - I/O 175 | 241 242 243 244 245 246 248 249 | |
| I/O 176 - I/O 183 | 250 251 252 253 254 255 256 258 | |
| I/O 184 - I/O 191 | 259 260 261 262 268 264 265 266 | |
| I/O 192 - I/O 199 | 268 269 270 271 272 273 274 275 | |
| I/O 200 - I/O 207 | 276 278 279 280 281 282 283 284 | |
| I/O 208 - I/O 215 | 285 286 288 289 290 291 292 293 | |
| I/O 216 - I/O 223 | 294 295 296 298 299 300 301 302 | |
| I/O 224 - I/O 231 | 303 2 3 4 5 6 7 8 | |
| I/O 232 - I/O 239 | 10 11 12 14 15 16 17 18 | |
| I/O 240 - I/O 247 | 20 21 22 24 25 26 27 28 | |
| I/O 248 - I/O 255 | 30 31 32 34 35 36 37 38 | |
| GOE0 and GOE1 | 195 and 185 | Global Output Enable input pins. |
| TOE | 215 | Test output enable pin. |
| $\overline{\text{RESET}}$ | 53 | Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device. |
| Y0, Y1 and Y2 | 43, 33, 205 | Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the GLBs on the device. |
| Y3 and Y4 | 175, 165 | Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the I/O cells in the device. |
| BSCAN/$\overline{\text{ispEN}}$** | 63 | Boundary Scan Enable. Input - Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active. |
| TDI/SDI* | 23 | Input - This pin performs two functions. It is the Test Data input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI is also used as one of the two control pins for the isp state machine. |
| TCLK/SCLK* | 73 | Input - This pin performs two functions. It is the Test Clock input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. |
| TMS/MODE* | 13 | Input - This pin performs two functions. It is the Test Mode Select input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as pin to control the operation of the isp state machine. |
| $\overline{\text{TRST}}$ | 225 | Input - Test Reset, active low to reset the Boundary Scan State Machine. |
| TDO/SDO* | 155 | Output - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as the pin to read the isp data. When $\overline{\text{ispEN}}$ is high it functions as Test Data Out. |
| GND | 9, 19, 39, 49, 69, 85, 95, 115, 125, 145, 161, 171, 191, 201, 221, 237, 247, 267, 277, 297 | Ground (GND) |
| VCC | 1, 29, 59, 77, 105, 135, 153, 181, 211, 229, 257, 287, 304 | $V_{CC}$ |

Table 2 - 0002/3256E

* ispLSI 3256E only

** $\overline{\text{ispEN}}$ for ispLSI 3256E only, NC for pLSI 3256E must be left floating or tied to Vcc, must not be grounded or tied to any other signal.

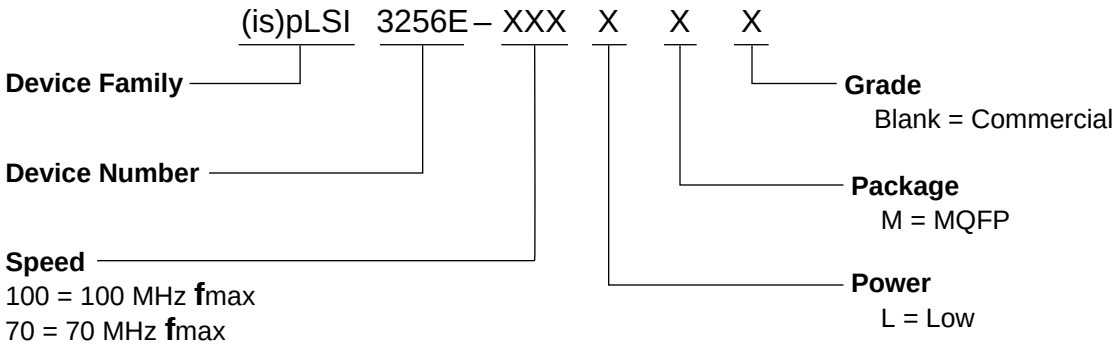
## Pin Configuration

### ispLSI and pLSI 3256E 304-pin MQFP


*Pins have dual function capability for ispLSI 3256E only.

304MQFP.3256E

## Part Number Description




0212/3256E

## Ordering Information

| Family | fmax | tpd | Ordering Number | Package |
|---|---|---|---|---|
| **ispLSI** | 100 | 10 | ispLSI 3256E-100LM | 304-Pin MQFP |
| | 70 | 15 | ispLSI 3256E-70LM | 304-Pin MQFP |
| **pLSI** | 100 | 10 | pLSI 3256E-100LM | 304-Pin MQFP |
| | 70 | 15 | pLSI 3256E-70LM | 304-Pin MQFP |

Table 2- 0041/3256E



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