GAL® 20RA10: Programmable Clocks Improve System Performance

Introduction

There is a growing need for innovative design techniques to increase the system throughput using the currently available Programmable Logic Devices (PLDs). One way of improving the system throughput is to make use of Lattice Semiconductor's GAL20RA10. By taking advantage of the unique architecture featuring an individually controlled clock on each of the Output Logic Macro Cell (OLMC) registers, the resolution of the control signals generated by a GAL20RA10-based state machine can be doubled. The design example shown in this application note takes advantage of this feature in a Dynamic RAM (DRAM) control logic design.

Design Example

The most common control signals generated by DRAM control logic are the Row Address Strobe (RAS) and the Column Address Strobe (CAS). The timing requirements of these control signals are strictly governed by the DRAM's timing requirements. Based on the DRAM's timing requirement, Figure 1a shows how the RAS and CAS control signals are generated from a standard PLD device which has only one dedicated active high clock signal driving all the output registers. The basic constraint of the high-to-low transition of RAS signal to the high-to-low transition of CAS signal for the 100ns DRAM is 15ns minimum (row address hold time after RAS).

As illustrated in Figure 1b, the activation of CAS signal is unnecessarily delayed because of the limitations of the standard PLD's single active-high clock driving all the output registers. This limitation is not a reflection of the DRAM's requirements but rather a limitation of the standard PLD.

Design engineers can improve this design method by using the GAL20RA10's independent OLMC clocks. Figure 2b shows the RAS and CAS signals being driven by both the rising and falling edges of the clock signal. This technique can be implemented in the GAL20RA10 by simply feeding the complement of the clock input from the RAS control register to the CAS control register, as shown in Figure 2a.

Figure 1a. Standard PLD Design with a Single Active-High Clock

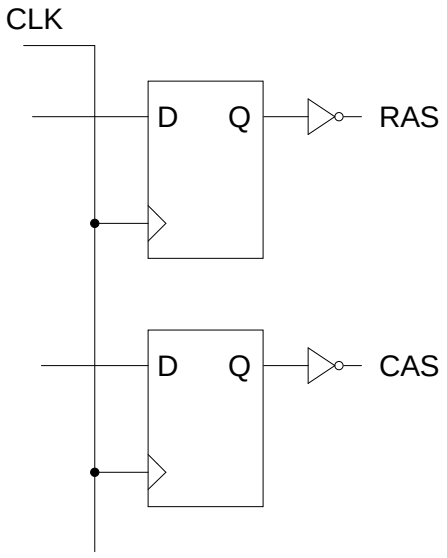
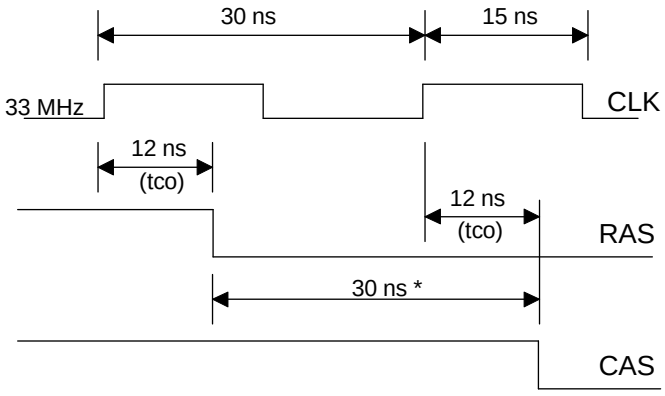


Figure 1b. Control Signal Generation with a Single Active-High Clock



* Only 15 ns needed for the row address hold time

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Summary

The individual clock control on the OLMC is one of several different individual product-term controlled features which are available on the GAL20RA10. Other individual product-term controlled signals of the GAL20RA10 include the Asynchronous Preset (AP) and Asynchronous Reset (AR). These signals can also be used, similar to the clock signal, to enhance system performance. In addition to these features, the GAL20RA10 has an external preload (PL) capability to improve the control over the register contents — especially in state machine design. The full GAL20RA10 macrocell architecture is shown below, in Figure 3.

Figure 2a. Standard PLD Design with Dual-Polarity Clocks

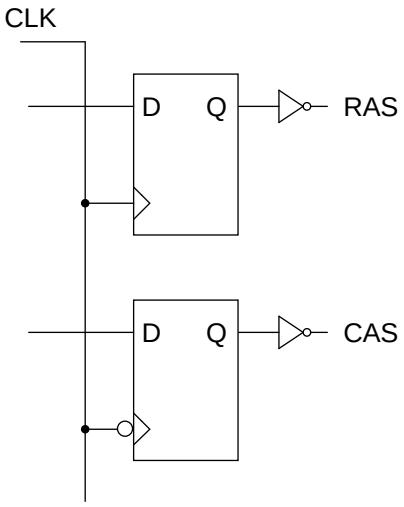
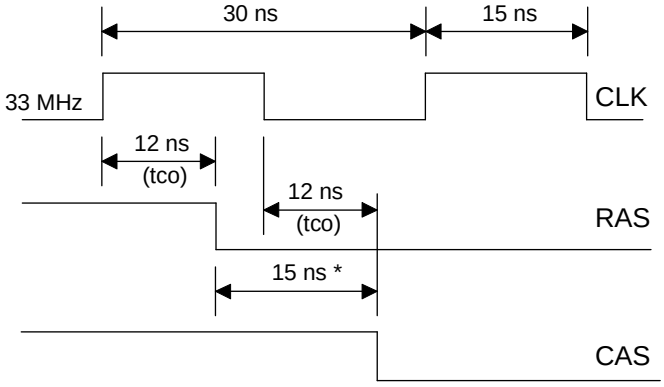
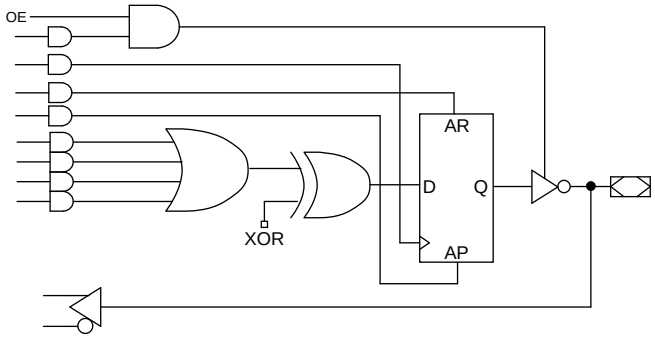


Figure 2b. Control Signal Generation Using a GAL20RA10



* Only 15 ns needed for the row address hold time

Figure 3. GAL20RA10 Macrocell



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