Zero-Power GAL® Devices

Introduction

The zero-power GAL16V8 and GAL20V8 families of devices provide the highest speed and lowest power combination available in the Programmable Logic Device (PLD) market today. They operate at a Tpd of 12ns and an Fmax of 83.3MHz, with a maximum Icc of 55mA and an Isb (standby current) of 50µA typical. These zero-power PLDs have industry standard GAL16V8 and GAL20V8 architectures, and are manufactured with Electrically Erasable CMOS (E^2CMOS®) technology, offering 100% programmability, functionality and testability.

This family offers two zero-power options for each architecture: An Input Transition Detection version and a Dedicated Power-Down Pin version. The GAL16V8Z and the GAL20V8Z use input transition detection to enter into the zero-power mode— if there are no input transitions for a specified interval, the device powers down. The GAL16V8ZD and GAL20V8ZD enter the zero-power mode by using a dedicated power-down pin which takes the place of a logic input.

Figure 1. ITD Standby Power Timing Waveform

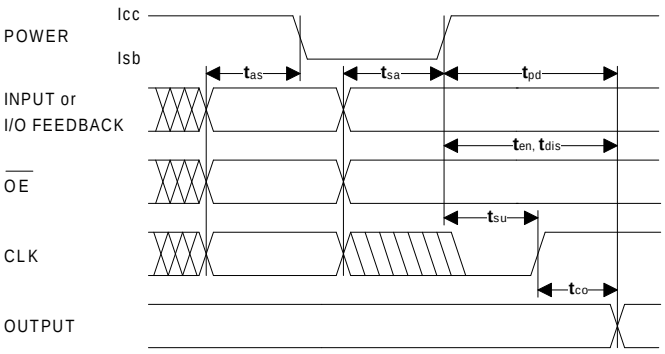
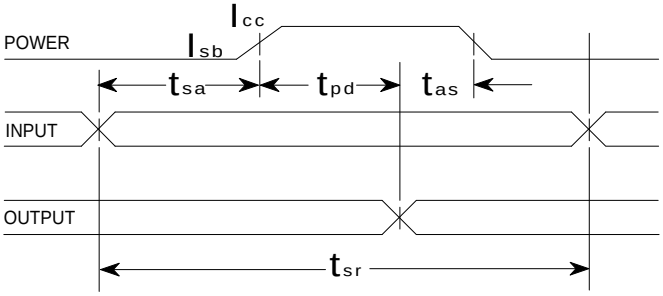


Figure 2. Power Timing Waveforms



Since these zero-power E^2CMOS PLDs have the same architectures as the GAL16V8 and GAL20V8, they can be used in similar applications. DMA control, state machines, and other standard 16/20V8 applications that become very power conscious when implemented in battery powered systems are ideal for the zero-power GAL families. Zero-power GAL devices help reduce overall system cost by allowing the user to specify smaller, less expensive power supplies and may even allow the system to be implemented without cooling fans.

This application note describes the timing parameters and architectural features of the zero-power GAL devices and describes a few applications for which these devices are particularly well suited.

GAL16V8Z and GAL20V8Z

Timing Parameters

Figure 1 illustrates the timing parameters of the GAL16/20V8Z devices associated with standby mode. The GAL16/20V8Z devices enter into standby mode if there is a lack of activity on their inputs or I/Os for a period of time greater than Tas (140 ns). This makes it possible for the GAL16/20V8Z devices to automatically go into standby mode when the system or any section of the system containing the zero-power devices goes dormant. Since the GAL16/20V8Z devices may or may not be in a dormant state at any given time, they have two different propagation delays depending on which state they are in. The first propagation delay is the time taken if the devices are not in standby mode: 12ns maximum for 12ns Tpd rated devices. The second propagation delay, as indicated in Figure 1, is for the first transition after sleep mode: 25ns (Tsa+Tpd) maximum for 12 ns devices.

Current Consumption

Figure 1 can be redrawn as shown in Figure 2 to better illustrate the calculation of average Icc current consumed by the devices. Figure 2 shows that the Icc current over time has a periodicity or cycle time (Tsr). There are two separate cases of current consumption to consider.

Case 1: If the transition timing on the I/Os or inputs is less than Tas+Tpd, the GAL16/20V8Z devices will not go into standby mode, and current consumption will be the Icc active specification (55mA).

Case 2: If the time between any successive transitions is greater than Tas+Tpd, then the GAL16/20V8 devices will go into standby mode. If the input signals are repetitive in nature, the average Icc current consumed will be given by the following equation:

Icc(Average) = ((Icc Active)x(Tas+Tpd)/Tsr)
+ (Icc Standby)x(1-((Tas+Tpd)/Tsr))

Architectural Features

The GAL16/20V8Z devices incorporate transition detection and timing circuitry on the inputs and I/Os to determine if the devices are to enter standby mode. A unique input buffer makes the inputs and I/Os less susceptible to noise that might be present, thus keeping the devices from leaving standby mode unnecessarily. The circuitry used can be thought of as a current barrier that is not of sufficient magnitude to interfere with normal logic operations; inputs or I/Os must either source or sink typically 30 μA of current for a state transition to occur.

The current barrier is useful as it functions as either a pull-up or pull-down resistor depending on the state of the input. Since the drive direction of these active resistors reverses when the signal passes through the threshold switching region, a monotonic input signal is latched. The current barrier also helps maintain the input logic level if the driver of the input goes into the high impedance state. This is valuable as it keeps the inputs out of the threshold voltage region.

Applications

Use of GAL16/20V8Z devices in systems with fast, free running clocks.

Systems that require the operation of a PLD device for small periods of time and are driven by fast, free running clocks can become energy misers through the use of GAL16/20V8Z devices. These devices can be selectively placed into standby mode by gating off of the system clock, while still retaining the capability to respond to asynchronous signals.

Figure 4 gives an example clock interface to GAL16/20V8Z devices that allows simple gating off of the system clock without false clocking of the devices. This clocking scheme supports high-performance systems that consume minimal amounts of power. Clocking of the GAL16/20V8Z devices can be turned off, yet the devices will still be able to respond to asynchronous inputs. This is impossible for dedicated power-down pin devices. The GAL16/20V8Z clock needs to be disabled while the source clock is in the high state to avoid false clocking; this has the effect of keeping the GAL16/20V8Z device clock frozen in the high state. However, the clock gating signal may be enabled at any time during the clock cycle. Note that the user must not violate setup and hold times to ensure proper operation of the circuits.

Use of GAL16/20V8Z devices in systems with slow, free running clocks.

For slow clock applications, where clock edge transitions are more than 140ns apart, circuits such as those shown in Figure 5 may be used as clock drivers to GAL16/20V8Z devices. Either circuit produces a clock signal that is rising edge sensitive; when a rising edge occurs, a negative going pulse is generated. Timing waveforms showing this are in Figure 6. Again, the user of such circuits is encouraged to look at the setup and hold time requirements to ensure proper circuit operation.

This negative going pulse has a falling edge which causes the GAL16/20V8Z device to go from standby mode to active mode, so that the rising edge of the negative pulse clocks the device. This circuit allows the system to be clocked down to 0 MHz. The width of the negative clock pulse, which is controlled by the delay introduced by the string of inverters, should have a minimum pulse width of Tsa+Tsu. It should be noted that the active rising clock edge is now delayed by the circuitry in its path. This should be taken into account in the system's timing analysis.

Figure 3. DPP Timing Waveform

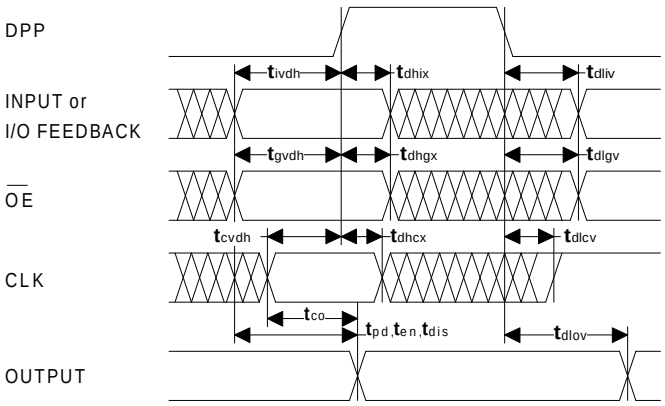
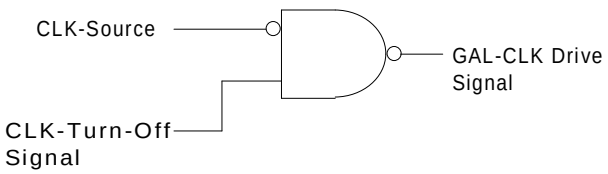


Figure 4. High Frequency Clock Drive Circuit



GAL16V8ZD and GAL20V8ZD

Timing Parameters

The GAL16/20V8ZD zero-power devices have a dedicated power-down pin (DPP). When this pin is placed into the active high (DPP=H) state, the GAL16/20V8ZD devices go into standby mode, and current consumption (Icc) decreases from 55mA to 100µA. The DPP pin is not available for logic input into the AND array, as it is with the GAL16/20V8Z devices. Since the GAL16/20V8ZD devices suspend their state when in standby mode, there are also setup and hold times on inputs to the devices with respect to the rising edge of the DPP signal. Figure 3 shows the AC timing diagrams for standby mode on the GAL16/20V8ZD devices.

The setup timing parameter for combinatorial signals is Tivdh, and the hold time is Tdhix. If these timing parameters are met, then a standard propagation delay will apply to the output. If the DPP pin is held high, the state of the output will be preserved independent of any changes to the inputs or I/Os, including the clock signal. The setup and hold times for the clock signal are Tcvdh and Tdhcx, respectively. Note that in all cases, if the timing parameters are violated then proper operation of the devices should not be expected.

Architectural Features

Operation of the DPP pin may be thought of as performing a “Chip Enable” type of function, with the exception that all of the I/Os retain the same configuration and drive state they had before going into standby mode.

Similarly, the DPP pin may be compared to a “Latch Enable” type of function, where taking the DPP pin to the high state will in effect freeze the state of the device, including all input and I/O pins. Therefore, latches on the PCB may be replaced by the functionality of the power-down pin. This double functionality of the GAL16/20V8ZD devices is beneficial as the overall part count of the system may be reduced, resulting in the benefits of lower cost, reduced board space and greater reliability.

Applications

The DPP lets the microprocessor or controller explicitly control how the battery or other energy sources are used. This is especially valuable when used in a system with other power-down devices and a global power-down control signal; power consumption can be reduced to nearly nothing. Also, the dedicated power-down pin can be effectively used for power management at critical times, such as during power drop out, when the processor or controller may be getting its power from the residual energy left in the electrolytic capacitors of the power supply. Since exercising the power-down pin puts

Figure 6. Low Frequency Clock Drive Circuit Timing Waveforms

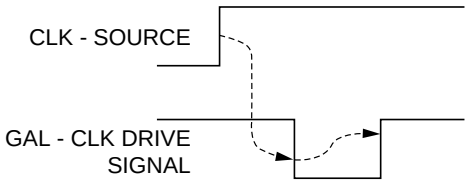
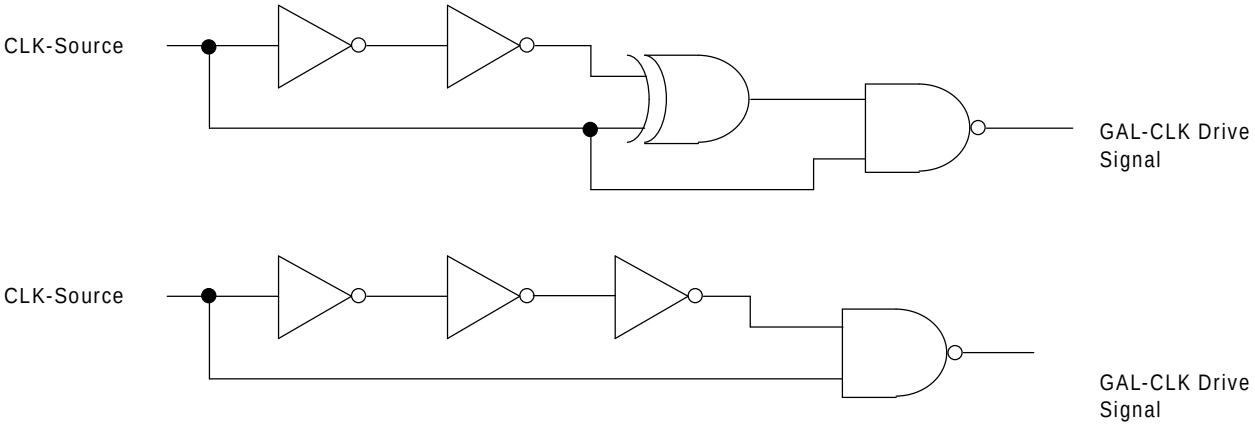


Figure 5. Low Frequency Clock Drive Circuits



the GAL16/20V8ZD devices in standby mode and a frozen state, by placing the power-down pin into standby mode (DPP=L), resuming operation from where the GAL16/20V8ZD operation was suspended can be easily accomplished. Therefore, the processor/controller can effectively execute a power-down routine when power drops out, suspend the routine when the power critical time has ended, and allow the GAL16/20V8ZD devices to be in the same state as before power drop out.

Conclusion

Having introduced the GAL16/20V8Z and GAL16/20V8ZD devices, Lattice Semiconductor makes available extremely low-power, high-performance components. Since power savings at the component level translates to power savings at the system level, existing high performance systems can now be converted to power misers without even changing JEDEC files.

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