pDS+™ CUPL Software

Features

- **ispLSI® AND pLSI® DEVELOPMENT SYSTEM**
  - **— Supports ispLSI and pLSI 1000/E and 2000**
  - **— Upgrade to Support ispLSI and pLSI 3000**
- **INTEGRATED DEVELOPMENT ENVIRONMENT FOR MIXED-MODE DESIGN ENTRY**
  - **— CUPL Hardware Description Language (CUPL-HDL) Syntax Supports Boolean Equations, Truth Tables and State Machine Entry**
- **pDS+ CUPL FITTER**
  - **— Multi-Level Logic Synthesis**
  - **— Efficient Design Optimization and Minimization**
  - **— Automatic Mapping and Device Fitting**
  - **— Automatic Partitioning with High Utilization**
  - **— Predictable Performance**
- **INDUSTRY STANDARD PROGRAMMING FILE GENERATION**
  - **— Standard JEDEC Device Fuse Map**
- **PLATFORMS SUPPORTED**
  - **— Windows 3.1/Windows 95/Windows NT**
- **IN-SYSTEM PROGRAMMING SUPPORT**
  - **— ispCODE™ C Source Routines Included**
  - **— ISP Daisy Chain Download (PC Versions)**
  - **— ispATE™ Board Test Programming Utility**

Introduction

The pDS+ CUPL software from Lattice Semiconductor offers a powerful solution to fit high-density logic designs into Lattice's ispLSI and pLSI devices.

Design entry is made simple by using CUPL software from Logical Devices together with the pDS+ CUPL Fitter for design implementation. The CUPL software and pDS+ CUPL Fitter offer high-level, device independent design entry with efficient logic compilation, delivering unprecedented performance for the most complex designs.

Logical Devices

The easy-to-use, menu-driven CUPL software packages provide a complete pre-fit design environment. Using CUPL-HDL from Logical Devices, Inc., complex designs can be quickly and efficiently described using a combination of Boolean Equations, Truth Tables, State Machine syntax or other HDL descriptions. The HDL syntax allows design creation without regard to any specific device dependencies. The built-in functional simulator allows designs to be fully verified before device fitting. The menu driven environment makes design implementation as easy as clicking a mouse button.

pDS+ CUPL Fitter

The pDS+ CUPL Fitter for ispLSI and pLSI devices is completely integrated within the CUPL Software environment. The pDS+ CUPL Fitter provides hands-off design implementation through intelligent design optimization, logic partitioning, automatic place and route and fusemap generation with optional test vectors, in standard JEDEC format. Extensive top level design control is provided to optimize design implementation for speed and/or high device resource utilization.

Design Optimization & Logic Minimization

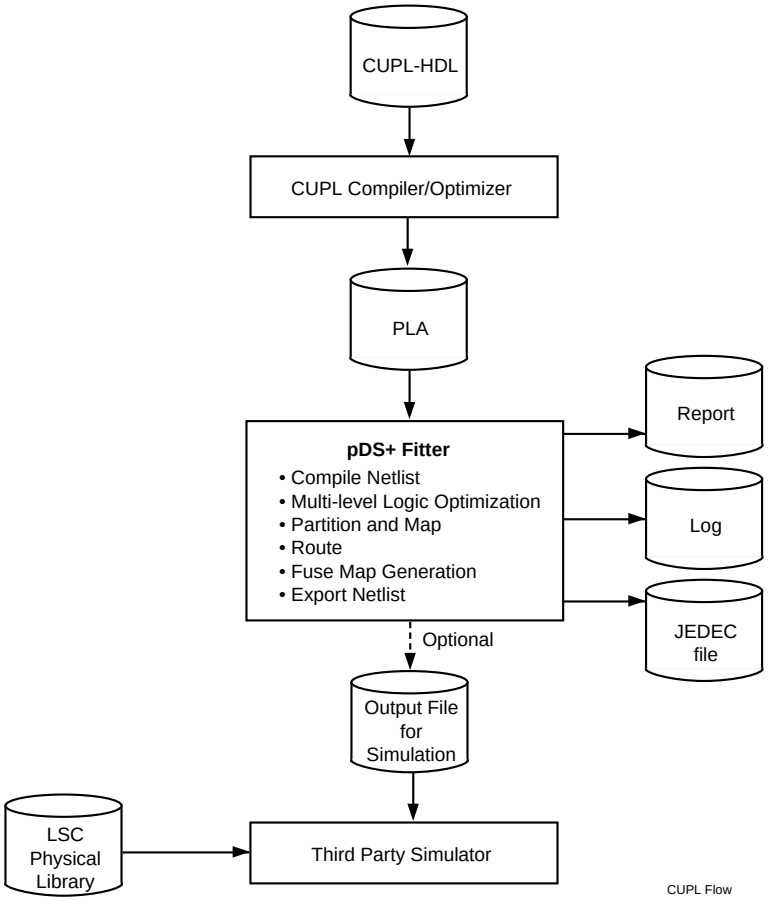
The pDS+ CUPL Fitter uses proprietary algorithms targeted for device specific features. The Fitter optimizes the design thoroughly, utilizing logic minimization, product term sharing and XOR functions whenever possible. In addition, the pDS+ CUPL Fitter supports multiple fitting strategies to obtain the best device utilization and performance.

Automatic Partitioning

The pDS+ CUPL Fitter incorporates a powerful Automatic Partitioner for hands-free synthesis of a design into Generic Logic Blocks (GLBs). The partitioner takes full advantage of the device's powerful features such as the hard XOR function and product term sharing. The internal XOR can be utilized for Arithmetic functions, T-Type flip-flops, and on & off set optimization functions. The partitioner also makes extensive use of product term sharing. Product term sharing allows the fitter to efficiently use device resources by sharing product terms across multiple logic functions. These features combine to maximize device resource utilization and increase design performance.

LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037; http://www.latticesemi.com

Figure 1. pDS+ CUPL Fully Integrated Design Environment



Automatic Place and Route

Automatic place and route eliminates the need for manual editing and accelerates the design cycle. The Router automatically generates pinouts based on the optimal design implementation or user assigned pinouts.

The Router optimally interconnects signals between I/O cells and GLBs through the Global Routing Pool (GRP) and Output Routing Pool (ORP). It also performs GLB splitting and GLB output duplication to enhance routing.

The Extended Route option performs a comprehensive route to maximize device resource utilization and ensure efficient design implementation. The result is that small design changes won't cause expensive PC board re-work.

Design Parameter Control

Extensive design parameter control at the design entry level is possible with the pDS+ CUPL Fitter giving the user the option to optimize the design for maximum utilization and speed. Controls are specified using "Property" statements in the CUPL design file. These controls fall into two categories:

- — Fitter Controls
- — Design Implementation Controls
  - — Net Attributes
  - — Pin Attributes
  - — Path Attributes
  - — Symbol Attributes

Fitter Controls

Special properties can be passed to the pDS+ CUPL Fitter providing complete control over critical design considerations. Fitter control over design partitioning and routing optimizes the design for speed and/or device utilization. Here are a few of the powerful features:

Feature	Description
PART	Determines device type to be used.
PARAM_FILE	Allows user to specify attributes in a text file.
STRATEGY	Choice of AREA (default), DELAY or NO_OPTIMIZE. AREA optimizes device space, DELAY keeps GLB levels to a minimum and NO_OPTIMIZE does not reduce equations.
USE_GLOBAL_RESET	Causes global reset to use dedicated routing for reset.
MAX_GLB_OUT	Specifies maximum number of outputs from a GLB. Default is 4.
MAX_GLB_IN	Controls maximum number of inputs to a GLB. Default is 16 for 1K and 2K devices and 24 for 3K devices.
EFFORT	Controls optimization of partitioner.
EXTENDED_ROUTE	Choice of OFF (fixed) or ON (extended, default).
PIN_FILE	Specifies locked pin assignments.

Design Implementation Controls

Device controls are used for changing design parameters such as security. Some of these implementation controls are:

Feature	Description
ISP	Instructs Router to reserve in-system programming pins.
ISP_EXCEPT_Y2	Reserves all ISP pins except Y2 (ispLSI and pLSI 1016/E and 2032 only).
Y1_AS_RESET	Uses Y1 clock pin on ispLSI and pLSI 1016/E and 2032 as a global reset pin.
SECURITY	Sets the device security cell to prevent unauthorized fuse map read back.

Net Attributes

These properties control how the design is mapped into the specified features of the target device:

Feature	Description
CLK0-CLK2	Assigns a CLK signal to a dedicated CLK line.
IOCLK0-IOCLK1	Assigns a CLK signal to a dedicated IOCLK line if single fanout input pin.
FASTCLK	Fitter assigns CLK signal to CLK0-CLK2 or IOCLK0-IOCLK1.
SLOWCLK	Assigns the CLK signal to a GLB product term CLK.
PRESERVE	Prevents logic minimization on specified nets.
GROUP	Suggests grouping of functions in a GLB.

Pin Attributes

Feature	Description
CRIT	Specifies Output Routing Pool Bypass to minimize delay.
SLOWSLEW	Assigns slow slew rate on a specific I/O cell.
LOCK	Assigns device I/O pins to design I/O ports.
PULLUP	Specifies internal pull-up resistors.

Path Attributes

Feature	Description
SAP/EAP	Defines asynchronous paths to prevent signal duplication.
SCP/ECP	Defines critical paths to reduce delays.
SNP/ENP	Defines logic paths for no logic minimization.

Symbol Attributes

Feature	Description
REGTYPE	Determines where a register is to be placed (IOC or GLB).
PROTECT	Prevents removal of a primitive or a macro during minimization.
OPTIMIZE	Selects either hard or soft macros.

Parameter File

The pDS+ CUPL Fitter provides a parameter file feature which helps designers eliminate guesswork and optimizes the design for the right device. It allows the user to try a number of design implementation options using the design implementation controls in batch mode. The parameter file instructs the partitioner and the router on how to maximize both device utilization and performance.

The pDS+ CUPL Fitter also provides post-route equations showing exactly how the design is implemented in the selected device.

Fuse Map Generation

The pDS+ CUPL Fitter supports a device fusemap in standard JEDEC format. A security feature gives protection of proprietary designs from unauthorized duplication. The fitter also appends any design test vectors in JEDEC format to the device fusemap thus facilitating a quick, easy functional verification of a programmed device.

Design Verification

The pDS+ CUPL software supports functional simulation of all ispLSI and pLSI designs using the built-in CUPL functional simulator. The simulation test vectors can be combined into the JEDEC file for device testing in a programmer.

Complete post route design verification can also be performed using optional Viewlogic Viewsim, PROsim, or other third-party timing simulators. The pDS+ CUPL software generates the output file required for third-party simulation. Simulation libraries are available from Lattice Semiconductor for various PC and Sun-based CAE vendor tools. The Viewlogic PROsim simulator and Synario simulator are available from Lattice Semiconductor for the PC platform.

System Requirements (PC Platform)

- 486/Pentium™ IBM Compatible PC
- Operating System
  - MSDOS Version 4.x or Later
  - Windows 3.1
  - Windows NT
  - Windows 95
- 16 MB RAM with 30MB Hard Disk Space
- CUPL 4.4b or Later
- Parallel Printer Port for Software Key

Programmer Support

All devices in the ispLSI device families can be programmed while installed on the target circuit board. In-system programming can be performed using an ispDOWNLOAD™ Cable and PC, by an on-board microprocessor or by ATE systems during final board test.

All ispLSI and pLSI devices can also be programmed using third-party PLD programmers. The devices are currently supported by programmers from the following vendors:

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30A/B
System General	TURPRO-1/FX

High-pin count socket adapters are available from Emulation Technology, EDI Corporation and PROCON.

Product Ordering Information

Product Code	Description
pDS2190-PC1	Fitter for Logical Devices CUPL on PC Platform
pDS2190-3UP/PC1	3000 Family Upgrade for pDS2190-3UP/PC1
pDS1102-PC2	Viewlogic Library and Interface for PC
pDS3302-PC2	PROSim Simulator with Libraries
pDS1120-PC1	Synario Libraries and Interface
pDS1170-PC1	OrCAD Simulator Library and Interface

Maintenance*

pDS2190M-PC1	Maintenance for pDS2190-PC1
pDS1102M-PC2	Maintenance for pDS1102-PC2
pDS3302M-PC2	Maintenance for pDS3302-PC2
pDS1120M-PC1	Maintenance for pDS1120-PC1
pDS1170M-PC1	Maintenance for pDS1170-PC1

*One year of maintenance is provided with every product purchase.

Warranty/Update Service

- 90-day warranty on disk media
- One-year maintenance support included with purchase
- Annual maintenance agreement available

Technical Support Assistance

Hotline:	1-800-LATTICE (Domestic) 1-408-428-6414 (International)
BBS:	1-408-428-6417
FAX:	1-408-944-8450
email:	apps@latticesemi.com

LATTICE SEMICONDUCTOR CORPORATION
5555 Northeast Moore Court
Hillsboro, Oregon 97124 U.S.A.
Tel.: (503) 681-0118
FAX: (503) 681-3037
http://www.latticesemi.com

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