# ispLSI® and pLSI® 1048C

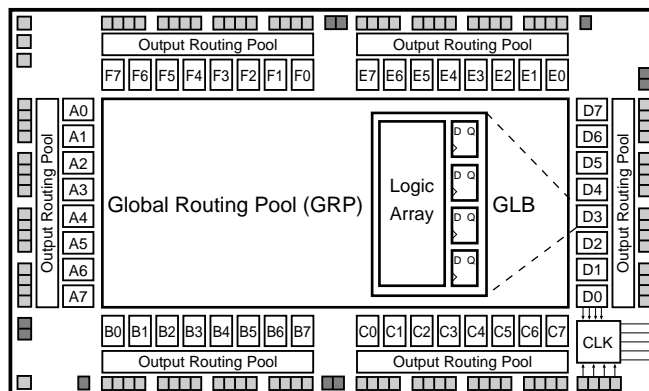## High-Density Programmable Logic

## Features

- **HIGH-DENSITY PROGRAMMABLE LOGIC**
  - **— 8000 PLD Gates**
  - **— 96 I/O Pins, 12 Dedicated Inputs, 2 Global Output Enables**
  - **— 288 Registers**
  - **— High-Speed Global Interconnect**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
  - **— Security Cell Prevents Unauthorized Copying**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— $f$max = 70 MHz Maximum Operating Frequency**
  - **— $f$max = 50 MHz for Industrial and Military/883 Devices**
  - **— $t$pd = 16 ns Propagation Delay**
  - **— TTL Compatible Inputs and Outputs**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile E²CMOS Technology**
  - **— 100% Tested at Time of Manufacture**
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - **— In-System Programmable™ (ISP™) 5-Volt Only**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market, and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Debugging**
- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **— Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **— Four Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispLSI AND pLSI DEVELOPMENT TOOLS**
  - **pDS® Software**
  - **— Easy to Use PC Windows™ Interface**
  - **— Boolean Logic Compiler**
  - **— Manual Partitioning**
  - **— Automatic Place and Route**
  - **— Static Timing Table**
  - **pDS+™ Software**
  - **— Industry Standard, Third-Party Design Environments**
  - **— Schematic Capture, State Machine, VHDL, Verilog**
  - **— Automatic Partitioning and Place and Route**
  - **— Multi-Level Logic Synthesis**
  - **— Comprehensive Logic and Timing Simulation**
  - **— PC and Workstation Platforms**

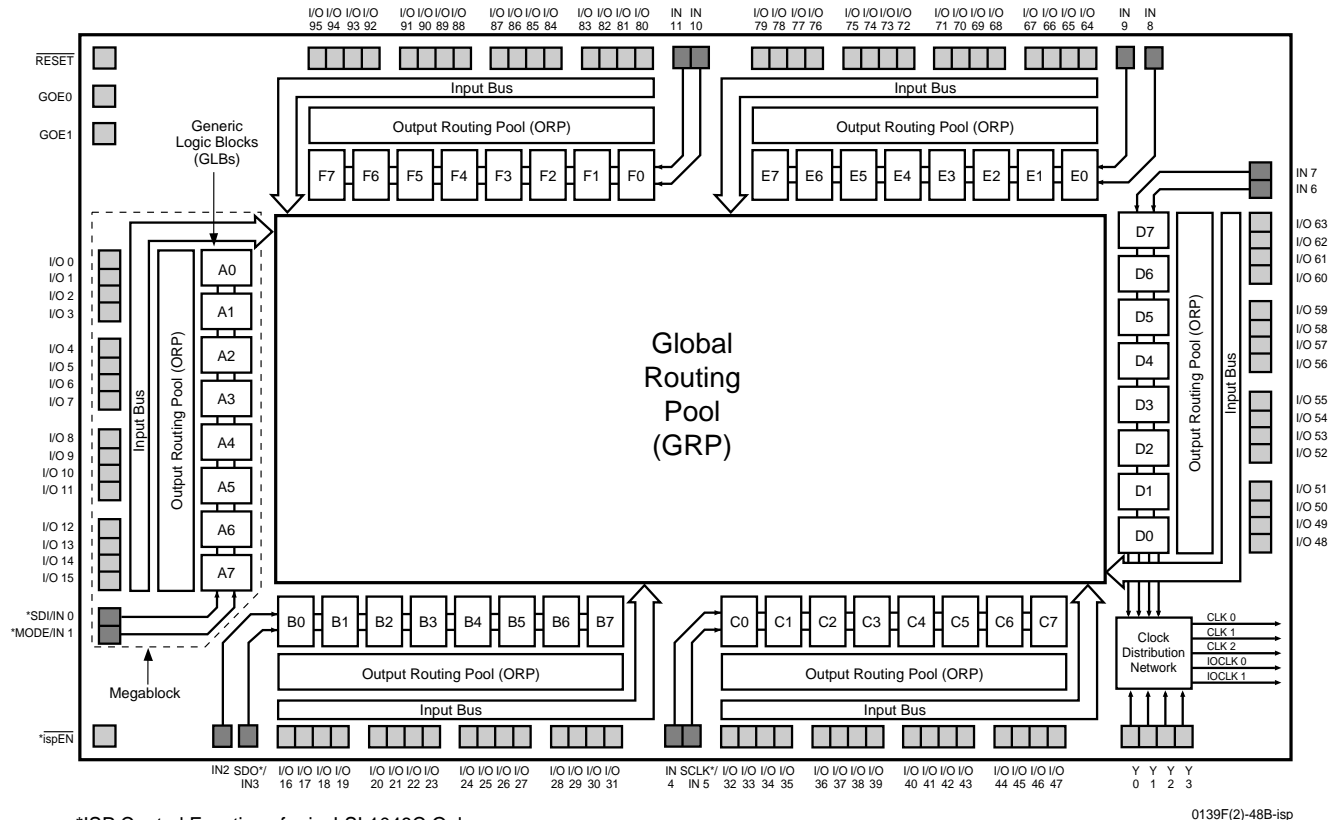## Functional Block Diagram



0139G1A-isp

## Description

The ispLSI and pLSI 1048C are High-Density Programmable Logic Devices containing 288 Registers, 96 Universal I/O pins, 12 Dedicated Input pins, two Global Output Enables (GOE), four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 1048C features 5-Volt in-system programming and in-system diagnostic capabilities. It is the first device which offers non-volatile "on-the-fly" reprogrammability of the logic, and the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 1048C device, but multiplexes four of the dedicated input pins to control in-system programming. Compared to the ispLSI and pLSI 1048, the ispLSI and pLSI 1048C offer two additional dedicated inputs and two new Global Output Enable pins.

The basic unit of logic on the ispLSI and pLSI 1048C devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. F7 in figure 1. There are a total of 48 GLBs in the ispLSI and pLSI 1048C devices. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

## Functional Block Diagram

**Figure 1. ispLSI and pLSI 1048C Functional Block Diagram**



*ISP Control Functions for ispLSI 1048C Only

0139F(2)-48B-isp

The devices also have 96 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. Additionally, all outputs have selectable polarity, active high or active low. The signal voltage levels are TTL-compatible, and the output drivers can source 4 mA or sink 8 mA.

Eight GLBs, 16 I/O cells, two dedicated inputs and one ORP are connected together to make a Megablock as shown in figure 1. The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. The ispLSI and pLSI 1048C devices contain six of these Megablocks.

The GRP has, as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI and pLSI 1048C devices are selected using the Clock Distribution Network. Four dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (D0 on the ispLSI and pLSI 1048C devices). The logic of this GLB allows the user to create an internal clock from a combination of internal signals.

## Absolute Maximum Ratings [1]

Supply Voltage $V_{CC}$ ...................................-0.5 to +7.0V

Input Voltage Applied ........................ -2.5 to $V_{CC}$ +1.0V

Off-State Output Voltage Applied ..... -2.5 to $V_{CC}$ +1.0V

Storage Temperature ................................ -65 to 150°C

Case Temp. with Power Applied .............. -55 to 125°C

Max. Junction Temp. ($T_J$) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

## DC Recommended Operating Conditions

| SYMBOL | PARAMETER | | | MIN. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | Commercial | $T_A = 0°C$ to +70°C | 4.75 | 5.25 | V |
| | | Industrial | $T_A = -40°C$ to +85°C | 4.5 | 5.5 | |
| | | Military/883 | $T_C = -55°C$ to +125°C | 4.5 | 5.5 | |
| $V_{IL}$ | Input Low Voltage | | | 0 | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | | 2.0 | $V_{CC} + 1$ | V |

Table 2- 0005Aisp w/mil.eps

## Capacitance ($T_A$=25°C, f=1.0 MHz)

| SYMBOL | PARAMETER | | MAXIMUM[1] | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|
| $C_1$ | Dedicated Input Capacitance | Commercial/Industrial | 8 | pf | $V_{CC}$=5.0V, $V_{IN}$=2.0V |
| | | Military | 10 | pf | $V_{CC}$=5.0V, $V_{IN}$=2.0V |
| $C_2$ | I/O and Clock Capacitance | | 10 | pf | $V_{CC}$=5.0V, $V_{I/O}$, $V_Y$=2.0V |

1. Guaranteed but not 100% tested.

Table 2- 0006

## Data Retention Specifications

| PARAMETER | MINIMUM | MAXIMUM | UNITS |
|---|---|---|---|
| Data Retention | 20 | – | Years |
| ispLSI Erase/Reprogram Cycles | 10000 | – | Cycles |
| pLSI Erase/Reprogram Cycles | 100 | – | Cycles |

Table 2- 0008B

## Switching Test Conditions

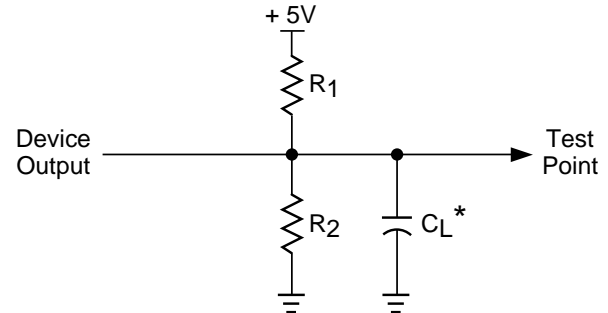| Input Pulse Levels | GND to 3.0V |
|---|---|
| Input Rise and Fall Time | ≤ 3ns 10% to 90% |
| Input Timing Reference Levels | 1.5V |
| Output Timing Reference Levels | 1.5V |
| Output Load | See figure 2 |

3-state levels are measured 0.5V from steady-state active level.

Table 2- 0003

### Figure 2. Test Load



*$C_L$ includes Test Fixture and Probe Capacitance.

### Output Load Conditions (see figure 2)

| Test Condition | | R1 | R2 | CL |
|---|---|---|---|---|
| A | | 470Ω | 390Ω | 35pF |
| B | Active High | ∞ | 390Ω | 35pF |
| | Active Low | 470Ω | 390Ω | 35pF |
| C | Active High to Z at $V_{OH}$ - 0.5V | ∞ | 390Ω | 5pF |
| | Active Low to Z at $V_{OL}$ + 0.5V | 470Ω | 390Ω | 5pF |

Table 2- 0004A

## DC Electrical Characteristics

### Over Recommended Operating Conditions

| SYMBOL | PARAMETER | CONDITION | | MIN. | TYP.[3] | MAX. | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ =8 mA | | – | – | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ =-4 mA | | 2.4 | – | – | V |
| $I_{IL}$ | Input or I/O Low Leakage Current | $0V \leq V_{IN} \leq V_{IL}$ (MAX.) | | – | – | -10 | μA |
| $I_{IH}$ | Input or I/O High Leakage Current | $3.5V \leq V_{IN} \leq V_{CC}$ | | – | – | 10 | μA |
| $I_{IL-isp}$ | $\overline{ispEN}$ Input Low Leakage Current | $0V \leq V_{IN} \leq V_{IL}$ (MAX.) | | – | – | -150 | μA |
| $I_{IL-PU}$ | I/O Active Pull-Up Current | $0V \leq V_{IN} \leq V_{IL}$ | | – | – | -150 | μA |
| $I_{OS}$[1] | Output Short Circuit Current | $V_{CC}$ = 5V, $V_{OUT}$ = 0.5V | | – | – | -200 | mA |
| $I_{CC}$[2,4] | Operating Power Supply Current | $V_{IL}$ = 0.5V, $V_{IH}$ = 3.0V | Commercial | – | 165 | 235 | mA |
| | | $f_{TOGGLE}$ = 1 MHz | Industrial/Military | – | 165 | 260 | mA |

1. One output at a time for a maximum duration of one second. $V_{out}$ = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2. Measured using twelve 16-bit counters.
3. Typical values are at $V_{CC}$ = 5V and $T_A$ = 25°C.
4. Maximum $I_{CC}$ varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this datasheet and Thermal Management section of this Data Book to estimate maximum $I_{CC}$.

Table 2- 0007A-48-isp

## External Timing Parameters

### Over Recommended Operating Conditions

| PARAMETER | TEST[4] COND. | #[2] | DESCRIPTION[1] | -70 MIN. | -70 MAX. | -50 MIN. | -50 MAX. | UNITS |
|---|---|---|---|---|---|---|---|---|
| $t_{pd1}$ | A | 1 | Data Propagation Delay, 4PT bypass, ORP bypass | – | 16.0 | – | 22.0 | ns |
| $t_{pd2}$ | A | 2 | Data Propagation Delay | – | 19.0 | – | 26.0 | ns |
| $f_{max}$ (Int.) | A | 3 | Clock Frequency with Internal Feedback[3] | 70.4 | – | 50.3 | – | MHz |
| $f_{max}$ (Ext.) | – | 4 | Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$ | 47.6 | – | 34.5 | – | MHz |
| $f_{max}$ (Tog.) | – | 5 | Clock Frequency, Max Toggle $\left(\frac{1}{t_{wh} + t_{w1}}\right)$ | 83.3 | – | 58.8 | – | MHz |
| $t_{su1}$ | – | 6 | GLB Reg. Setup Time before Clock, 4PT bypass | 9.5 | – | 13.0 | – | ns |
| $t_{co1}$ | A | 7 | GLB Reg. Clock to Output Delay, ORP bypass | – | 10.0 | – | 14.0 | ns |
| $t_{h1}$ | – | 8 | GLB Reg. Hold Time after Clock, 4 PT bypass | 0 | – | 0 | – | ns |
| $t_{su2}$ | – | 9 | GLB Reg. Setup Time before Clock | 11.0 | – | 15.0 | – | ns |
| $t_{co2}$ | – | 10 | GLB Reg. Clock to Output Delay | – | 11.5 | – | 16.0 | ns |
| $t_{h2}$ | – | 11 | GLB Reg. Hold Time after Clock | 0 | – | 0 | – | ns |
| $t_{r1}$ | A | 12 | Ext. Reset Pin to Output Delay | – | 15.0 | – | 20.5 | ns |
| $t_{rw1}$ | – | 13 | Ext. Reset Pulse Duration | 10.0 | – | 13.5 | – | ns |
| $t_{ptoeen}$ | B | 14 | Input to Output Enable | – | 20.0 | – | 27.5 | ns |
| $t_{ptoedis}$ | C | 15 | Input to Output Disable | – | 20.0 | – | 27.5 | ns |
| $t_{goeen}$ | B | 16 | Global OE Output Enable | – | 15.0 | – | 20.5 | ns |
| $t_{goedis}$ | C | 17 | Global OE Output Disable | – | 15.0 | – | 20.5 | ns |
| $t_{wh}$ | – | 20 | Ext. Sync. Clock Pulse Duration, High | 6.0 | – | 8.5 | – | ns |
| $t_{wl}$ | – | 21 | Ext. Sync. Clock Pulse Duration, Low | 6.0 | – | 8.5 | – | ns |
| $t_{su3}$ | – | 22 | I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3) | 2.0 | – | 3.0 | – | ns |
| $t_{h3}$ | – | 23 | I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3) | 6.5 | – | 9.0 | – | ns |

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

Table 2- 0030-48C/70, 50

## Internal Timing Parameters[1]

| PARAMETER | #[2] | DESCRIPTION | -70 | | -50 | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| **Inputs** | | | | | | | |
| $t_{iobp}$ | 24 | I/O Register Bypass | – | 3.1 | – | 4.3 | ns |
| $t_{iolat}$ | 25 | I/O Latch Delay | – | 4.0 | – | 5.5 | ns |
| $t_{iosu}$ | 26 | I/O Register Setup Time before Clock | 6.5 | – | 9.1 | – | ns |
| $t_{ioh}$ | 27 | I/O Register Hold Time after Clock | 0.1 | – | 0.3 | – | ns |
| $t_{ioco}$ | 28 | I/O Register Clock to Out Delay | – | 3.4 | – | 4.6 | ns |
| $t_{ior}$ | 29 | I/O Register Reset to Out Delay | – | 3.7 | – | 5.1 | ns |
| $t_{din}$ | 30 | Dedicated Input Delay | – | 5.4 | – | 7.4 | ns |
| **GRP** | | | | | | | |
| $t_{grp1}$ | 31 | GRP Delay, 1 GLB Load | – | 4.5 | – | 6.2 | ns |
| $t_{grp4}$ | 32 | GRP Delay, 4 GLB Loads | – | 4.9 | – | 6.7 | ns |
| $t_{grp8}$ | 33 | GRP Delay, 8 GLB Loads | – | 5.8 | – | 8.0 | ns |
| $t_{grp16}$ | 34 | GRP Delay, 16 GLB Loads | – | 7.6 | – | 10.5 | ns |
| $t_{grp48}$ | 35 | GRP Delay, 48 GLB Loads | – | 16.5 | – | 22.7 | ns |
| **GLB** | | | | | | | |
| $t_{4ptbp}$ | 36 | 4 Product Term Bypass Path Delay | – | 4.0 | – | 5.5 | ns |
| $t_{1ptxor}$ | 37 | 1 Product Term/XOR Path Delay | – | 4.9 | – | 6.7 | ns |
| $t_{20ptxor}$ | 38 | 20 Product Term/XOR Path Delay | – | 5.5 | – | 7.5 | ns |
| $t_{xoradj}$ | 39 | XOR Adjacent Path Delay[3] | – | 6.5 | – | 8.9 | ns |
| $t_{gbp}$ | 40 | GLB Register Bypass Delay | – | 0.9 | – | 1.2 | ns |
| $t_{gsu}$ | 41 | GLB Register Setup Time before Clock | 2.9 | – | 3.9 | – | ns |
| $t_{gh}$ | 42 | GLB Register Hold Time after Clock | 5.3 | – | 7.3 | – | ns |
| $t_{gco}$ | 43 | GLB Register Clock to Output Delay | – | 1.5 | – | 2.3 | ns |
| $t_{gro}$ | 44 | GLB Register Reset to Output Delay | – | 2.1 | – | 2.8 | ns |
| $t_{ptre}$ | 45 | GLB Product Term Reset to Register Delay | – | 8.1 | – | 11.1 | ns |
| $t_{ptoe}$ | 46 | GLB Product Term Output Enable to I/O Cell Delay | – | 7.0 | – | 9.6 | ns |
| $t_{ptck}$ | 47 | GLB Product Term Clock Delay | 2.5 | 6.0 | 3.4 | 8.2 | ns |
| **ORP** | | | | | | | |
| $t_{orp}$ | 48 | ORP Delay | – | 2.5 | – | 3.4 | ns |
| $t_{orpbp}$ | 49 | ORP Bypass Delay | – | 1.0 | – | 1.4 | ns |

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
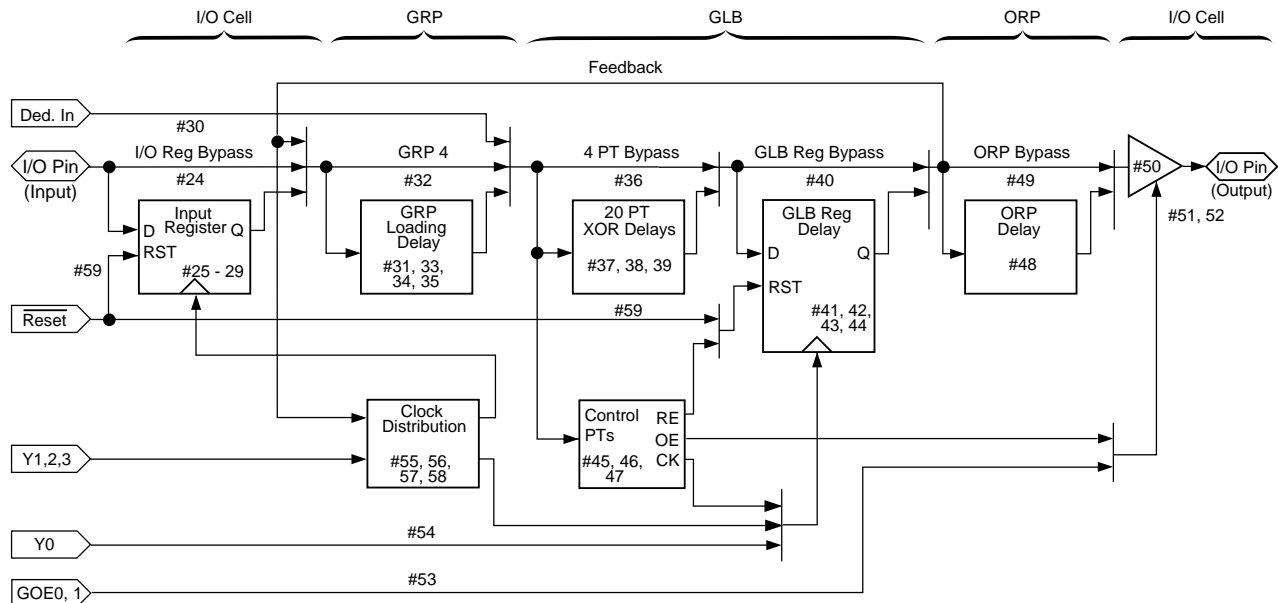3. The XOR adjacent path can only be used by hard macros.

Table 2- 0036-48C/70, 50

## Internal Timing Parameters[1]

| PARAMETER | #[2] | DESCRIPTION | -70 | | -50 | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| **Outputs** | | | | | | | |
| $t_{ob}$ | 50 | Output Buffer Delay | – | 2.1 | – | 2.9 | ns |
| $t_{oen}$ | 51 | I/O Cell OE to Output Enabled | – | 5.0 | – | 6.9 | ns |
| $t_{odis}$ | 52 | I/O Cell OE to Output Disabled | – | 5.0 | – | 6.9 | ns |
| $t_{goe}$ | 53 | Global OE | – | 10.0 | – | 13.6 | ns |
| **Clocks** | | | | | | | |
| $t_{gy0}$ | 54 | Clock Delay, Y0 to Global GLB Clock Line (Ref. clock) | 5.4 | 5.4 | 7.4 | 7.4 | ns |
| $t_{gy1/2}$ | 55 | Clock Delay, Y1 or Y2 to Global GLB Clock Line | 4.5 | 6.4 | 6.1 | 8.7 | ns |
| $t_{gcp}$ | 56 | Clock Delay, Clock GLB to Global GLB Clock Line | 1.9 | 5.5 | 2.6 | 7.6 | ns |
| $t_{ioy2/3}$ | 57 | Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line | 4.5 | 6.4 | 6.1 | 8.7 | ns |
| $t_{iocp}$ | 58 | Clock Delay, Clock GLB to I/O Cell Global Clock Line | 1.9 | 5.5 | 2.6 | 7.6 | ns |
| **Global Reset** | | | | | | | |
| $t_{gr}$ | 59 | Global Reset to GLB and I/O Registers | – | 8.3 | – | 11.4 | ns |

1. Internal Timing Parameters are not tested and are for reference only.

Table 2- 0037-48C/70, 50

## ispLSI and pLSI 1048C Timing Model



0491A/48

### Derivations of tsu, th and tco from the Product Term Clock[1]
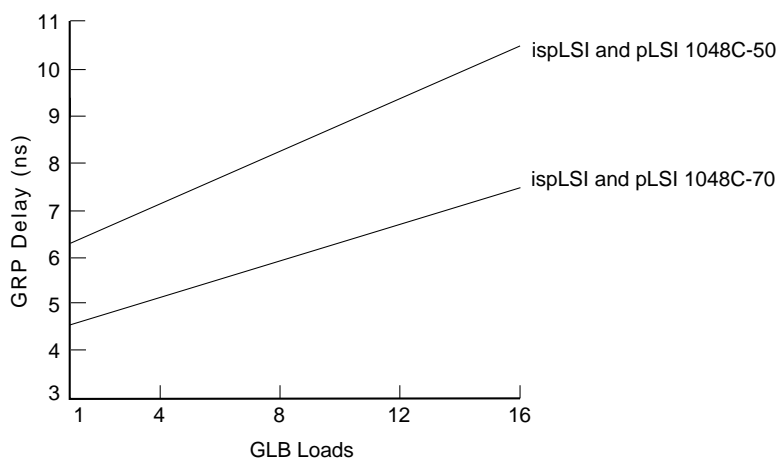
$t$su = Logic + Reg su - Clock (min)
= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck(min)})$
= $(\#24 + \#32 + \#38) + (\#41) - (\#24 + \#32 + \#47)$
5.9 ns = $(3.1 + 4.9 + 5.5) + (2.9) - (3.1 + 4.9 + 2.5)$

$t$h = Clock (max) + Reg h - Logic
= $(t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$
= $(\#24 + \#32 + \#47) + (\#42) - (\#24 + \#32 + \#38)$
5.8 ns = $(3.1 + 4.9 + 6.0) + (5.3) - (3.1 + 4.9 + 5.5)$

$t$co = Clock (max) + Reg co + Output
= $(t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$
= $(\#24 + \#32 + \#47) + (\#43) + (\#48 + \#50)$
20.1 ns = $(3.1 + 4.9 + 6.0) + (1.5) + (2.5 + 2.1)$

### Derivations of tsu, th and tco from the Clock GLB[1]

$t$su = Logic + Reg su - Clock (min)
= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0(min)} + t_{gco} + t_{gcp(min)})$
= $(\#24 + \#32 + \#38) + (\#41) - (\#54 + \#43 + \#56)$
7.6 ns = $(3.1 + 4.9 + 5.5) + (2.9) - (5.4 + 1.5 + 1.9)$

$t$h = Clock (max) + Reg h - Logic
= $(t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$
= $(\#54 + \#43 + \#56) + (\#42) - (\#24 + \#32 + \#38)$
4.2 ns = $(5.4 + 1.5 + 5.5) + (5.3) - (3.1 + 4.9 + 5.5)$

$t$co = Clock (max) + Reg co + Output
= $(t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$
= $(\#54 + \#43 + \#56) + (\#43) + (\#48 + \#50)$
18.5 ns = $(5.4 + 1.5 + 5.5) + (1.5) + (2.5 + 2.1)$

1. Calculations are based upon timing specifications for the ispLSI and pLSI 1048C-70

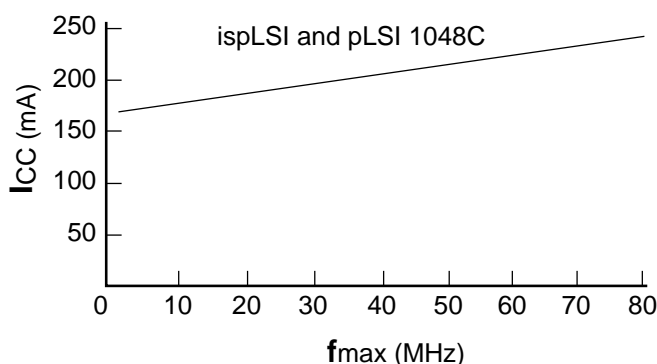Table 2- 0042-48C

## Maximum GRP Delay vs GLB Loads



0126A-48C-80-isp

## Power Consumption

Power consumption in the ispLSI and pLSI 1048C device depends on two primary factors: the speed at which the device is operating, and the number of Product Terms used. Figure 3 shows the relationship between power and operating speed.

**Figure 3. Typical Device Power Consumption vs fmax**



Notes: Configuration of Twelve 16-bit Counters
Typical Current at 5V, 25°C

$I_{CC}$ can be estimated for the ispLSI and pLSI 1048C using the following equation:

$I_{CC}$ = 73 + (# of PTs * 0.23) + (# of nets * Max. freq * 0.010) where:
# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max. freq = Highest Clock Frequency to the device

The $I_{CC}$ estimate is based on typical conditions ($V_{CC}$ = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of $I_{CC}$ is sensitive to operating conditions and the program in the device, the actual $I_{CC}$ should be verified.

0127A-48C-80-isp
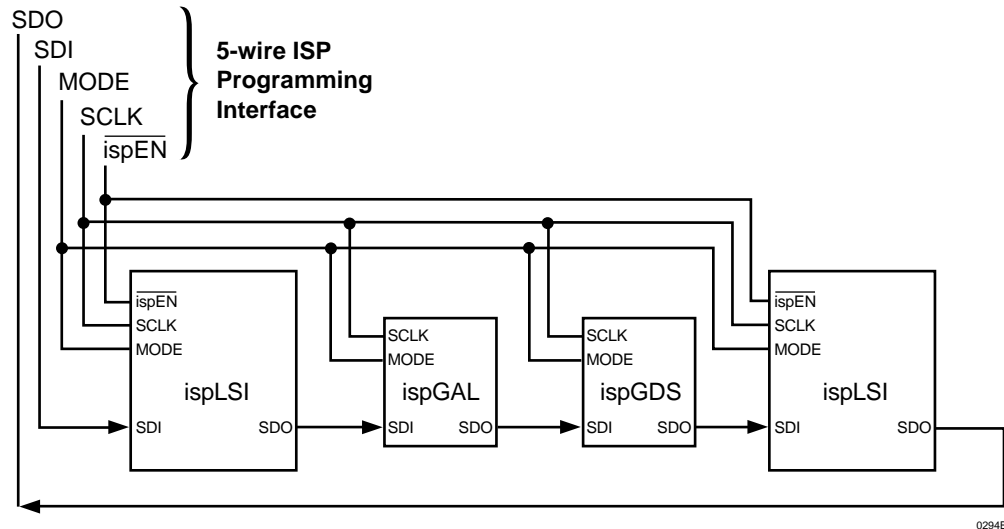
## In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice Semiconductor High-Density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile $E^2$CMOS cells will not lose the pattern even when the power is turned off.

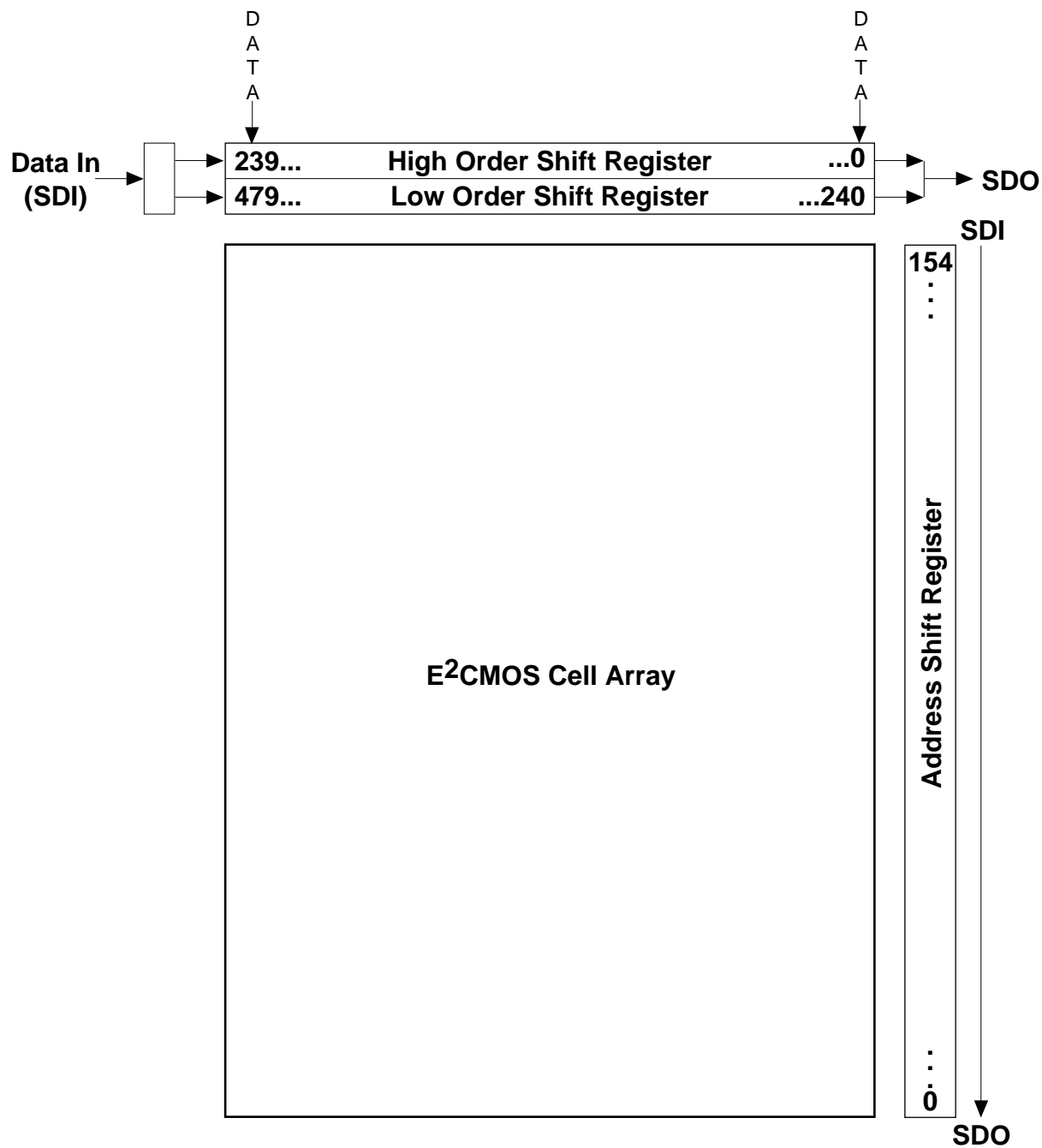All necessary programming is done via five TTL-level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The interface signals are isp Enable ($\overline{\text{ispEN}}$), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 4 illustrates one possible ispLSI device programming scheme. For details on the operation of the internal state machine and programming of the device please refer to the ISP Architecture and Programming section in this Data Book.

The device identifier for the ispLSI 1048C is 0000 0101 (05 hex). This code is the unique device identifier which is generated when a read ID command is performed.

**Figure 4. ISP Programming Interface**

![Lattice Semiconductor Corporation logo]

## ispLSI 1048C Shift Register Layout



DATA

DATA

| | |
|---|---|
| **239...** High Order Shift Register **...0** | |
| **479...** Low Order Shift Register **...240** | |

Data In (SDI)

SDO

SDI

**154**

.
.

**Address Shift Register**

**E²CMOS Cell Array**

.
.
**0**

SDO

Note: A logic "1" in the Address Shift Register bit position enables the row for programming or verification. A logic "0" disables it.

## Pin Description

| NAME | PQFP PIN NUMBERS | DESCRIPTION |
|---|---|---|
| I/O 0 - I/O 5<br>I/O 6 - I/O 11<br>I/O 12 - I/O 17<br>I/O 18 - I/O 23<br>I/O 24 - I/O 29<br>I/O 30 - I/O 35<br>I/O 36 - I/O 41<br>I/O 42 - I/O 47<br>I/O 48 - I/O 53<br>I/O 54 - I/O 59<br>I/O 60 - I/O 65<br>I/O 66 - I/O 71<br>I/O 72 - I/O 77<br>I/O 78 - I/O 83<br>I/O 84 - I/O 89<br>I/O 90 - I/O 95 | 21, 22, 23, 24, 25, 26<br>27, 28, 29, 30, 31, 32<br>34, 35, 36, 37, 38, 39<br>40, 41, 42, 43, 44, 45<br>52, 53, 54, 55, 56, 57<br>58, 59, 60, 61, 62, 63<br>66, 67, 68, 69, 70, 71<br>72, 73, 74, 75, 76, 77<br>85, 86, 87, 88, 89, 90<br>91, 92, 93, 94, 95, 96<br>98, 99,100,101,102, 103<br>104,105,106,107,108, 109<br>117,118,119,120,121, 122<br>123,124,125,126,127, 128<br>2, 3, 4, 5, 6, 7<br>8, 9, 10, 11, 12, 13 | Input/Output Pins - These are the general purpose I/O pins used by the logic array. |
| GOE0, GOE1 | 64, 114 | Global output enables for all I/Os. |
| IN 2, IN 4<br>IN 6 - IN 11 | 47, 51<br>84,110,111, 115,116, 14 | Dedicated input pins to the device. |
| $\overline{ispEN}$*/NC | 18 | Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active. |
| SDI*/IN 0 | 20 | Input – This pin performs two functions. It is a dedicated input pin when $\overline{ispEN}$ is logic high. When $\overline{ispEN}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine. |
| MODE*/IN 1 | 46 | Input – This pin performs two functions. It is a dedicated input pin when $\overline{ispEN}$ is logic high. When $\overline{ispEN}$ is logic low, it functions as a pin to control the operation of the isp state machine. |
| SDO*/IN 3 | 50 | Input/Output – This pin performs two functions. It is a dedicated input pin when $\overline{ispEN}$ is logic high. When $\overline{ispEN}$ is logic low, it functions as an output pin to read serial shift register data. |
| SCLK*/IN 5 | 78 | Input – This pin performs two functions. It is a dedicated input when $\overline{ispEN}$ is logic high. When ispEN is logic low, it functions as a clock pin for the Serial Shift Register. |
| $\overline{RESET}$ | 19 | Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device. |
| Y0 | 15 | Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device. |
| Y1 | 83 | Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device. |
| Y2 | 80 | Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device. |
| Y3 | 79 | Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device. |
| GND | 1, 17, 33, 49, 65, 81<br>97, 112 | Ground (GND) |
| VCC | 16, 48, 82, 113 | $V_{CC}$ |

*For ispLSI 1048C Only

Table 2- 0002C-48C

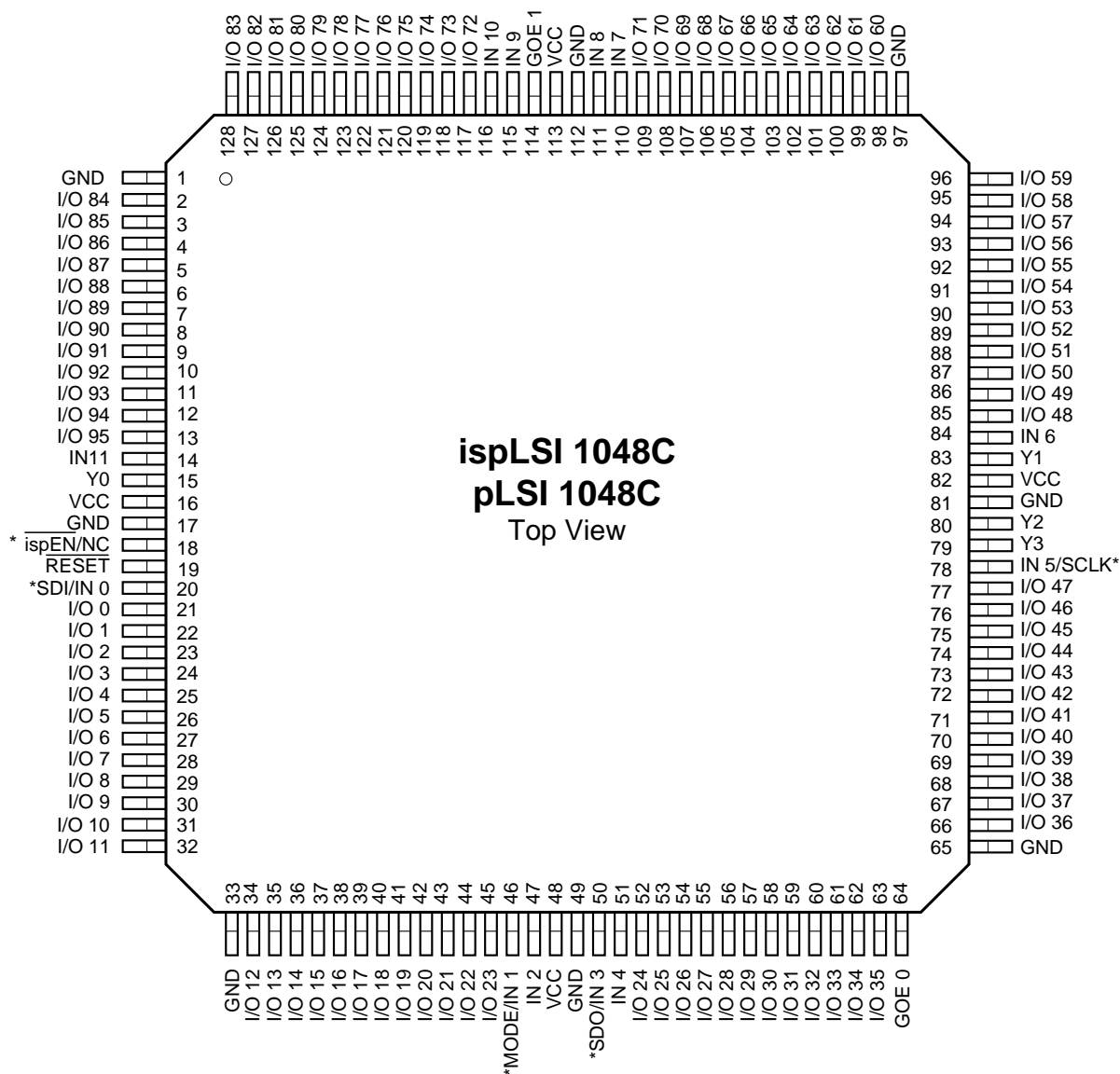## Pin Description

| NAME | CPGA PIN NUMBERS | DESCRIPTION |
|---|---|---|
| I/O 0 - I/O 5<br>I/O 6 - I/O 11<br>I/O 12 - I/O 17<br>I/O 18 - I/O 23<br>I/O 24 - I/O 29<br>I/O 30 - I/O 35<br>I/O 36 - I/O 41<br>I/O 42 - I/O 47<br>I/O 48 - I/O 53<br>I/O 54 - I/O 59<br>I/O 60 - I/O 65<br>I/O 66 - I/O 71<br>I/O 72 - I/O 77<br>I/O 78 - I/O 83<br>I/O 84 - I/O 89<br>I/O 90 - I/O 95 | J2, J3, K1, L1, K2, M1,<br>L2, K3, N1, M2, L3, P1,<br>M3, P2, N3, M4, P3, N4,<br>P4, M5, N5, P5, M6, N6,<br>N9, M9, P10, P11, N10, P12,<br>N11, M10, P13, N12, M11, P14,<br>M12, N14, M13, L12, M14, L13,<br>L14, K12, K13, K14, J12, J13,<br>F13, F12, E14, D14, E13, C14,<br>D13, E12, B14, C13, D12, A14,<br>C12, A13, B12, C11, A12, B11,<br>A11, C10, B10, A10, C9, B9,<br>B6, C6, A5, A4, B5, A3,<br>B4, C5, A2, B3, C4, A1,<br>C3, B1, C2, D3, C1, D2,<br>D1, E3, E2, E1, F3, F2 | Input/Output Pins - These are the general purpose I/O pins used by the logic array. |
| GOE0, GOE1 | N13, B7, | Global output enables for all I/Os. |
| IN 2, IN 4<br>IN 6 - IN 11 | P7, P9<br>F14, A9, A8, A7, A6, F1 | Dedicated input pins to the device. |
| $\overline{\text{ispEN}}$*/NC | H2 | Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active. |
| SDI*/IN 0 | J1 | Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine. |
| MODE*/IN 1 | P6 | Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the isp state machine. |
| SDO*/IN 3 | P8 | Input/Output – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data. |
| SCLK*/IN 5 | J14 | Input – This pin performs two functions. It is a dedicated input when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. |
| $\overline{\text{RESET}}$ | H1 | Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device. |
| Y0 | G1 | Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device. |
| Y1 | G14 | Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device. |
| Y2 | H13 | Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device. |
| Y3 | H14 | Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device. |
| GND | B2, B8, B13, C8, H3, H12,<br>M8, N2, N8 | Ground (GND) |
| VCC | C7, G2, G3, G12, G13, M7,<br>N7 | $V_{CC}$ |

*For ispLSI 1048C Only

Table 2- 0002C-48C/CPGA

Lattice™
Semiconductor
Corporation

## Pin Configuration

**ispLSI and pLSI 1048C 128-Pin PQFP Pinout Diagram**

Top pins (left to right, 128–97):
I/O 83, I/O 82, I/O 81, I/O 80, I/O 79, I/O 78, I/O 77, I/O 76, I/O 75, I/O 74, I/O 73, I/O 72, IN 10, IN 9, GOE 1, VCC, GND, IN 8, IN 7, I/O 71, I/O 70, I/O 69, I/O 68, I/O 67, I/O 66, I/O 65, I/O 64, I/O 63, I/O 62, I/O 61, I/O 60, GND

Left pins (top to bottom, 1–32):
| Pin | Name |
|---|---|
| 1 | GND |
| 2 | I/O 84 |
| 3 | I/O 85 |
| 4 | I/O 86 |
| 5 | I/O 87 |
| 6 | I/O 88 |
| 7 | I/O 89 |
| 8 | I/O 90 |
| 9 | I/O 91 |
| 10 | I/O 92 |
| 11 | I/O 93 |
| 12 | I/O 94 |
| 13 | I/O 95 |
| 14 | IN11 |
| 15 | Y0 |
| 16 | VCC |
| 17 | GND |
| 18 | * ispEN/NC |
| 19 | RESET |
| 20 | *SDI/IN 0 |
| 21 | I/O 0 |
| 22 | I/O 1 |
| 23 | I/O 2 |
| 24 | I/O 3 |
| 25 | I/O 4 |
| 26 | I/O 5 |
| 27 | I/O 6 |
| 28 | I/O 7 |
| 29 | I/O 8 |
| 30 | I/O 9 |
| 31 | I/O 10 |
| 32 | I/O 11 |

Center: **ispLSI 1048C pLSI 1048C** Top View

Right pins (top to bottom, 96–65):
| Pin | Name |
|---|---|
| 96 | I/O 59 |
| 95 | I/O 58 |
| 94 | I/O 57 |
| 93 | I/O 56 |
| 92 | I/O 55 |
| 91 | I/O 54 |
| 90 | I/O 53 |
| 89 | I/O 52 |
| 88 | I/O 51 |
| 87 | I/O 50 |
| 86 | I/O 49 |
| 85 | I/O 48 |
| 84 | IN 6 |
| 83 | Y1 |
| 82 | VCC |
| 81 | GND |
| 80 | Y2 |
| 79 | Y3 |
| 78 | IN 5/SCLK* |
| 77 | I/O 47 |
| 76 | I/O 46 |
| 75 | I/O 45 |
| 74 | I/O 44 |
| 73 | I/O 43 |
| 72 | I/O 42 |
| 71 | I/O 41 |
| 70 | I/O 40 |
| 69 | I/O 39 |
| 68 | I/O 38 |
| 67 | I/O 37 |
| 66 | I/O 36 |
| 65 | GND |

Bottom pins (left to right, 33–64):
GND, I/O 12, I/O 13, I/O 14, I/O 15, I/O 16, I/O 17, I/O 18, I/O 19, I/O 20, I/O 21, I/O 22, I/O 23, *MODE/IN 1, IN 2, VCC, GND, *SDO/IN 3, IN 4, I/O 24, I/O 25, I/O 26, I/O 27, I/O 28, I/O 29, I/O 30, I/O 31, I/O 32, I/O 33, I/O 34, I/O 35, GOE 0

*Pins have dual function capability for ispLSI 1048C only (except pin 18, which is ispEN only).

0124-48C

![Lattice Semiconductor Corporation logo]

## Pin Configuration

**ispLSI and pLSI 1048C 133-Pin CPGA Pinout Diagram**

|  | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |  |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | I/O59 | I/O61 | I/O64 | I/O66 | I/O69 | IN7 | IN8 | IN9 | IN10 | I/O74 | I/O75 | I/O77 | I/O80 | I/O83 |
| B | I/O56 | GND | I/O62 | I/O65 | I/O68 | I/O71 | GND | GOE1 | I/O72 | I/O76 | I/O78 | I/O81 | GND | I/O85 |
| C | I/O53 | I/O57 | I/O60 | I/O63 | I/O67 | I/O70 | GND | Vcc | I/O73 | I/O79 | I/O82 | I/O84 | I/O86 | I/O88 |
| D | I/O51 | I/O54 | I/O58 |  |  |  |  |  | INDEX |  |  | I/O87 | I/O89 | I/O90 |
| E | I/O50 | I/O52 | I/O55 |  |  |  |  |  |  |  |  | I/O91 | I/O92 | I/O93 |
| F | IN6 | I/O48 | I/O49 |  |  |  |  |  |  |  |  | I/O94 | I/O95 | IN11 |
| G | Y1 | Vcc | Vcc |  |  |  |  |  |  |  |  | Vcc | Vcc | Y0 |
| H | Y3 | Y2 | GND |  |  |  |  |  |  |  |  | GND | *ispEN /NC | RESET |
| J | *SCLK/ IN5 | I/O47 | I/O46 |  |  |  |  |  |  |  |  | I/O1 | I/O0 | *SDI/ IN0 |
| K | I/O45 | I/O44 | I/O43 |  |  |  |  |  |  |  |  | I/O7 | I/O4 | I/O2 |
| L | I/O42 | I/O41 | I/O39 |  |  |  |  |  |  |  |  | I/O10 | I/O6 | I/O3 |
| M | I/O40 | I/O38 | I/O36 | I/O34 | I/O31 | I/O25 | GND | Vcc | I/O22 | I/O19 | I/O15 | I/O12 | I/O9 | I/O5 |
| N | I/O37 | GOE0 | I/O33 | I/O30 | I/O28 | I/O24 | GND | Vcc | I/O23 | I/O20 | I/O17 | I/O14 | GND | I/O8 |
| P | I/O35 | I/O32 | I/O29 | I/O27 | I/O26 | IN4 | *SDO/ IN3 | IN2 | *MODE/ IN1 | I/O21 | I/O18 | I/O16 | I/O13 | I/O11 |

**ispLSI 1048C/883**
**pLSI 1048C/883**
Bottom View

PIN A1

*Pins have dual function capability for ispLSI 1048C/883 only (except pin H2, which is ispEN only).

133 CPGA Pinout.eps

## Part Number Description

```
(is)pLSI  1048C − XX  X  X  X
```

Device Family
Device Number
Speed
  70 = 70 MHz **f**max
  50 = 50 MHz **f**max

Grade
  Blank = Commercial
  I = Industrial
  /883 = 883 Military Process

Package
  Q = PQFP
  G = CPGA

Power
  L = Low

0212-80B-isp1048C

## ispLSI and pLSI 1048C Ordering Information

**COMMERCIAL**

| Family | **f**max (MHz) | **t**pd (ns) | Ordering Number | Package |
|---|---|---|---|---|
| ispLSI | 70 | 16 | ispLSI 1048C-70LQ | 128-Pin PQFP |
|  | 50 | 22 | ispLSI 1048C-50LQ | 128-Pin PQFP |
| pLSI | 70 | 16 | pLSI 1048C-70LQ | 128-Pin PQFP |
|  | 50 | 22 | pLSI 1048C-50LQ | 128-Pin PQFP |

**INDUSTRIAL**

| Family | **f**max (MHz) | **t**pd (ns) | Ordering Number | Package |
|---|---|---|---|---|
| ispLSI | 50 | 22 | ispLSI 1048C-50LQI | 128-Pin PQFP |
| pLSI | 50 | 22 | pLSI 1048C-50LQI | 128-Pin PQFP |

**MILITARY**

| Family | **f**max (MHz) | **t**pd (ns) | Ordering Number | SMD Number | Package |
|---|---|---|---|---|---|
| ispLSI | 50 | 22 | ispLSI 1048C-50LG/883 | 5962-9558701MXC | 133-Pin CPGA |
| pLSI | 50 | 22 | pLSI 1048C-50LG/883 | 5962-9558801MXC | 133-Pin CPGA |

Table 2- 0041A-48C-isp

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