Lattice Semiconductor Corporation

pDS+™ LOG/iC Software

Features

- **pLSI® AND ispLSI® DEVELOPMENT SYSTEM**
  - **Supports ispLSI and pLSI 1000/E and 2000**
  - **Upgrade to Support ispLSI and pLSI 3000**
- **DESIGN ENTRY USING ISDATA LOG/iC CLASSIC OR LOG/iC2**
  - **Design Verification Using LOG/iC Functional Simulation**
  - **Lattice Semiconductor Fitter for Design Synthesis**
  - **Optional Timing Simulation**
- **INTEGRATED DEVELOPMENT ENVIRONMENT FOR MIXED-MODE DESIGN ENTRY**
  - **ISDATA LOG/iC Syntax, Including Boolean Equations, Truth Tables and State Machines, Optional VHDL, Schematics or Graphical State Machine Entry**
  - **Graphical, Menu-Driven User Interface**
- **LATTICE SEMICONDUCTOR pDS+ LOG/iC FITTER**
  - **Multi-Level Logic Synthesis**
  - **Efficient Design Optimization and Minimization**
  - **Automatic Mapping and Device Fitting**
  - **Automatic Partitioning with High Utilization**
  - **Predictable Performance**
- **INDUSTRY STANDARD PROGRAMMING FILE GENERATION**
  - **Standard JEDEC Device Fuse Map**
- **IN-SYSTEM PROGRAMMING SUPPORT**
  - **ispCODE™ C Source Routines Included**
  - **ISP Daisy Chain Download**
  - **ispATE™ Board Test Programming Utility**
- **PLATFORMS SUPPORTED**
  - **PC Windows 3.1**

Introduction

The pDS+ LOG/iC software from Lattice Semiconductor Corporation (LSC) offers a powerful solution to fit high density logic designs into ispLSI and pLSI devices.

Design entry is made simple by using LOG/iC Classic or LOG/iC2 software from ISDATA GmbH together with the pDS+ LOG/iC Fitter for design implementation. The pDS+ LOG/iC software combines high-level, device independent design entry with efficient logic compilation, delivering unprecedented performance for the most complex designs.

ISDATA LOG/iC

The easy to use, menu-driven ISDATA software package provides a complete design environment (see figure 1). Using the LOG/iC program, complex designs can be quickly and efficiently described using a combination of Boolean Equations, Truth Tables, State Machine syntax or schematics. The LOG/iC syntax creates designs without regard to any specific device dependencies. The built-in functional simulator allows designs to be fully verified before device fitting. The menu driven environment makes design implementation simple to use.

pDS+ LOG/iC Fitter

The pDS+ LOG/iC Fitter for ispLSI and pLSI devices is completely integrated within the LOG/iC software environment. The Fitter provides hands-off design implementation through intelligent design optimization, logic partitioning, automatic place & route and fusemap generation with optional test vectors in standard JEDEC format. Extensive top level design control is provided to optimize design implementation for speed and/or high device resource utilization.

Design Optimization and Logic Minimization

The pDS+ LOG/iC Fitter uses proprietary algorithms targeted for device specific features. The Fitter optimizes the design thoroughly, compressing multiple level logic into two level logic, and utilizing logic minimization, product term sharing and XOR functions wherever necessary. In addition, the pDS+ LOG/iC Fitter supports multiple fitting strategies to obtain the best device utilization and performance.

Automatic Partitioning

The pDS+ LOG/iC Fitter incorporates a powerful Automatic Partitioner for hands-free synthesis of a design into Generic Logic Blocks (GLBs). The partitioner takes full advantage of the device's powerful features, such as the hard XOR function and product term sharing. The internal XOR can be utilized for arithmetic functions, and T-Type flip-flops. Common sub-expressions are extracted, and unused registers are eliminated. These features combine to maximize device resource utilization and increase design performance.
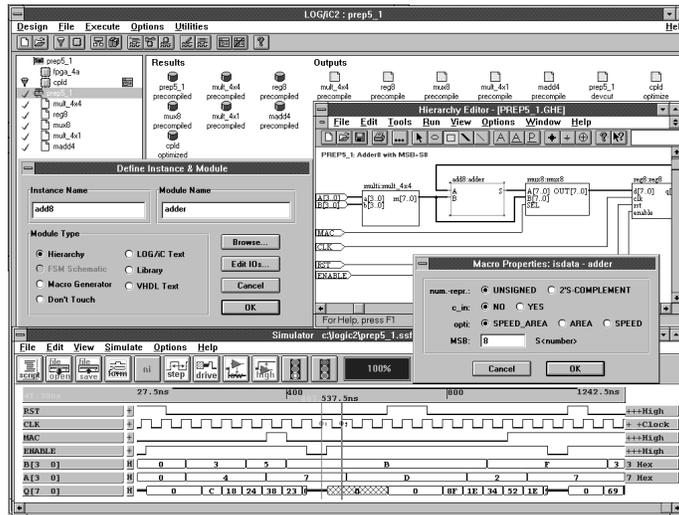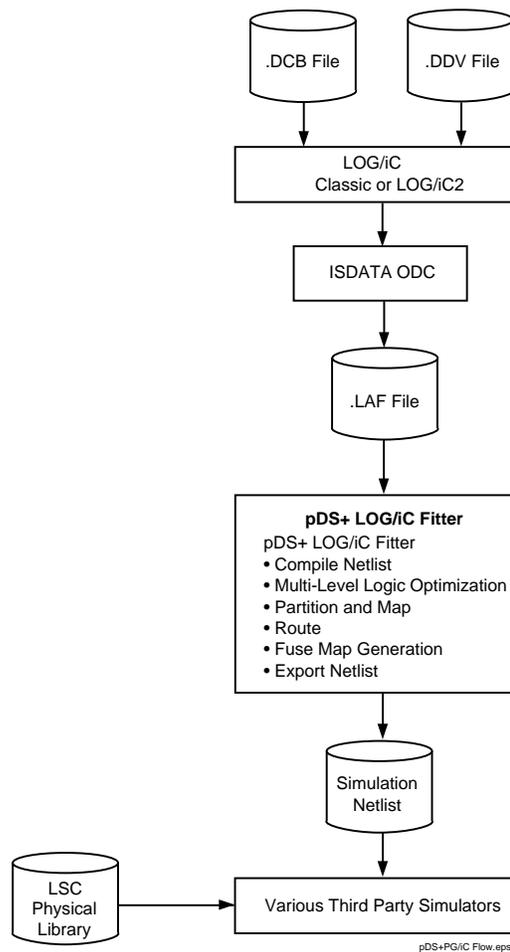
Figure 1. pDS+ LOG/iC Design Interface

Figure 2. pDS+ LOG/iC Fully Integrated Design Environment

.DCB File

.DDV File

LOG/iC
Classic or LOG/iC2

ISDATA ODC

.LAF File

pDS+ LOG/iC Fitter
pDS+ LOG/iC Fitter
• Compile Netlist
• Multi-Level Logic Optimization
• Partition and Map
• Route
• Fuse Map Generation
• Export Netlist

Simulation
Netlist

LSC
Physical
Library

Various Third Party Simulators

pDS+PG/iC Flow.eps

Automatic Place and Route

Automatic place and route eliminates the need for manual editing and accelerates the design cycle. The Router automatically generates pinouts based on the optimal design implementation or incorporates user assigned pinouts.

The Extended Route option performs a comprehensive route to maximize device resource utilization and ensure efficient design implementation. The result is small design changes don't result in expensive PC board rework.

Design Parameter Control

The pDS+ LOG/iC Fitter offers extensive design control at the design entry level, letting the user optimize the design for maximum utilization and/or speed. All of the controls are specified using "attributes" in the design property and parameter files. These controls fall into two categories:

— Fitter Controls
— Design Implementation Controls
    — Net Attributes
    — Pin Attributes
    — Path Attributes
    — Symbol Attributes

Fitter Control Options

Special properties can be passed to the pDS+ LOG/iC Fitter providing complete control over critical design considerations. Fitter control over design partitioning and routing optimizes the design for speed and/or device utilization.

Feature	Description
PART	Determines device type to be used.
PARAM_FILE	Allows user to specify attributes in a text file.
STRATEGY	Choice of AREA (default), DELAY or NO_OPTIMIZE. AREA optimizes device space, DELAY keeps GLB levels to a minimum and NO_OPTIMIZE does not reduce equations.

Feature	Description
USE_GLOBAL_RESET	Causes global reset to use dedicated routing for reset.
MAX_GLB_OUT	Specifies maximum number of outputs from a GLB. Default is 4.
MAX_GLB_IN	Controls maximum number of inputs to a GLB. Default is 16 for 1K and 2K devices and 24 for 3K devices.
EFFORT	Controls optimization of partitioner.
EXTENDED_ROUTE	Choice of OFF (fixed) or ON (extended, default).
PIN_FILE	Specifies locked pin assignments.

Design Implementation Controls

pDS+ LOG/iC Design implementation controls are used for changing such design parameters as security, pull-ups etc. Some of the implementation controls are:

Feature	Description
ISP	Instructs Router to reserve in-system programming pins.
ISP_EXCEPT_Y2	Reserves all ISP pins except Y2 (ispLSI and pLSI 1016/E and 2032 only).
Y1_AS_RESET	Uses Y1 clock pin on ispLSI and pLSI 1016/E and 2032 as a global reset pin.
SECURITY	Sets the device security cell to prevent unauthorized fuse map read back.

Net Attributes

These attributes control how the design is mapped into the specified features of the target device:

Feature	Description
CLK0-CLK2	Assigns a CLK signal to a dedicated CLK line.
IOCLK0-IOCLK1	Assigns a CLK signal to a dedicated IOCLK line if single fanout input pin.
FASTCLK	Fitter assigns CLK signal to CLK0-CLK2 or IOCLK0-IOCLK1.
SLOWCLK	Assigns the CLK signal to a GLB product term CLK.
PRESERVE	Prevents logic minimization on specified nets.
GROUP	Suggests grouping of functions in a GLB.

Pin Attributes

Feature	Description
CRIT	Specifies Output Routing Pool Bypass to minimize delay.
SLOWSLEW	Assigns slow slew rate on a specific I/O cell.
LOCK	Assigns device I/O pins to design I/O ports.
PULLUP	Specifies internal pull-up resistors.

Path Attributes

The following attributes specify paths in the design that have special fitting requirements:

Feature	Description
SAP/EAP	Defines asynchronous paths to prevent signal duplication.
SCP/ECP	Defines critical paths to reduce delays.
SNP/ENP	Defines logic paths for no logic minimization.

Symbol Attributes

Feature	Description
REGTYPE	Determines where a register is to be placed (IOC or GLB).
PROTECT	Prevents removal of a primitive or a macro during minimization.
OPTIMIZE	Selects either hard or soft macros.

Parameter File

The pDS+ LOG/iC Fitter uses a parameter file (.PAR file) feature, which is created by the entries in the .DDV file to help designers optimize the design for the right device. The parameter file instructs the partitioner and the router on how to maximize both device utilization and performance.

Property File

The pDS+ LOG/iC Fitter also accepts a property file (design.prp) which allows the designer to assign specific features to signals and nets using all of the design attributes available. The property file helps guide the fitter in implementing the design in the best way.

The pDS+ LOG/iC Fitter provides post route equations showing exactly how the design is implemented in the selected device. Optional functional simulation is also available for detailed preroute simulation of designs using the VERIFIER section of the LOG/iC menu.

Design Verification

The pDS+ LOG/iC software provides functional simulation of ispLSI and pLSI designs using the optional LOG/iC Functional Design Verifier (FDV).

Complete post route timing simulation is also available using simulators such as OrCAD's VST 386+ and Viewlogic. Timing libraries, sold separately, are required.

Fuse Map Generation

The pDS+ LOG/iC Fitter generates a device fuse map in standard JEDEC format. The fuse map is automatically produced and inserted in the JEDEC file after a successful route. A security feature gives protection of proprietary designs from unauthorized duplication.

System Requirements

486/Pentium IBM Compatible PC
— Windows 3.1
— 16 MB RAM with 20MB Hard Disk Space
— 3 1/2" Floppy Disk Drive
— ISDATA's LOG/iC Classic or LOG/iC2
— Parallel Printer Port for Software Key
— EGA Graphics Monitor or higher

Programmer Support

All devices in the ispLSI device families can be programmed while installed on the target circuit board. In-system programming can be performed using an ispDOWNLOAD™ Cable and PC, by an on-board microprocessor or by ATE systems during final board test.

All ispLSI and pLSI devices can also be programmed using third-party PLD programmers. The devices are currently supported by programmers from the following vendors:

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128

Programmer Vendor	Model
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30A/B
System General	TURPRO-1/FX

High pin-count socket adapters are available from Emulation Technology, EDI Corporation and PROCON.

Product Ordering Information

Product Code	Description
pDS2103-PC1	pDS+ Logic Fitter
pDS2103-3UP/PC1	3000 Family Upgrade
pDS3302-PC2	Viewlogic PROsim Simulator
pDS1102-PC2	Viewsim Library
pDS1170-PC1	OrCAD Library
pDS1131-PC1	Verilog and VHDL Sim Library

Annual Maintenance*

pDS1102M-PC2	Maintenance for pDS1102-PC2
pDS1170M-PC1	Maintenance for pDS1170-PC1
pDS1131M-PC1	Maintenance for pDS1131-PC1
pDS2103M-PC1	Maintenance for pDS2103-PC1
pDS3302M-PC2	Maintenance for pDS3302-PC2

*One year of maintenance is provided with every product purchase.

Warranty/Update Service

• 90-day warranty on disk media
• One-year maintenance support included with purchase
• Annual maintenance agreement available

Technical Support Assistance

Hotline:	1-800-LATTICE (Domestic)
	1-408-428-6414 (International)
BBS:	1-408-428-6417
FAX:	1-408-944-8450
email:	apps@latticesemi.com

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