ISP™ Synario System

Complete Development System: Design Entry, Functional Simulation, Hardware and Device Samples

Includes

- **SOFTWARE**
  - **— Data I/O's Synario Entry and Functional Simulation Software**
  - **— pDS+™ Synario Fitter for ispLSI® and pLSI® Devices**
  - **— ispGDS™ (Generic Digital Switch) Compiler Software**
  - **— ISP™ Programming Software**
- **SAMPLES**
  - **— ispLSI 2032 Device in 44-Pin PLCC Package**
  - **— ispGAL22V10 Device in 28-Pin PLCC Package**
  - **— ispGDS14 Device in 20-pin PLCC Package**
- **HARDWARE**
  - **— ispDOWNLOAD™ Cable**
- **WINDOWS 3.1x AND WINDOWS 95 COMPATIBLE**

Features

- **Easy-to-Use Kit Contains Everything Needed for In-System Programmable™ Device Design-in**
- **Data I/O's Synario Software — Schematic Entry, ABEL HDL Entry, Functional Simulator with Waveform Viewer, Synario Project Navigator**
- **Supports LSC's ispLSI 1000, 1000E, 2000 and 2000V/LV Devices — the Industry's Fastest High Density Programmable Devices at up to 180 MHz**
- **Supports All Lattice Semiconductor GAL Architectures including the ispGAL22V10**
- **Supports ISP Generic Digital Switch for Applications such as Software Driven Hardware Configuration and Multiple DIP Switch Replacement**
- **Keyless for Easy Portability**

Introduction

The Lattice Semiconductor ISP Synario System contains everything needed to design and program with Lattice Semiconductor ispLSI and GAL devices. The full version of Data I/O's Synario-Entry tools for schematic capture and ABEL-HDL language logic design, a functional simulator and Data I/O's Project Navigator for easy design and logic debugging are included. The ISP Synario System supports high density design for Lattice Semiconductor's ispLSI and pLSI 1000, 1000E, 2000 and 2000V/LV devices. The tools included also support the full range of Lattice Semiconductor's industry standard ispGAL and GAL devices, including the ispGAL22V10, GAL16V8, GAL20V8 and GAL6001 devices, and others. In addition, the ISP Synario System includes device samples of the ispLSI 2032, isp GAL22V10 and ispGDS™, as well as an ispDOWNLOAD™ Cable to download designs to the PC board.

In-System Programmability (ISP)

ISP is a LSC innovation that enables device programming and reprogramming on the printer circuit board at 5 volts. There are several advantages to in-system programmability: 1) It accelerates board- and system-level debug and enables you to define your board layout earlier in the design process; 2) ISP eliminates bent leads caused by extra handling and socket insertions made during the device programming process; 3) Systems incorporating ISP are reconfigurable with the devices already soldered to the printed circuit board, minimizing board rework expense; and 4) Field upgrades become easy by downloading a new configuration file to the end equipment via floppy disk or modem.

Synario Entry and pDS+ Fitter

The ISP Synario System contains a full featured version of Data I/O's Synario Entry tools for schematic capture and ABEL-HDL language logic design. The Synario Entry tool also includes a functional simulator with waveform viewer and Data I/O's powerful Project Navigator for easy design and logic debugging. Mixed-mode design entry is made easy with this system using schematics and powerful high level equations, truth tables, and state machine syntax in a single device design. Synario's powerful design features and versatile libraries are all presented in a user friendly Windows™ based environment that makes design even easier. The Synario Project Navigator is a design manager that organizes source files and presents an easy to follow processing checklist.

Tightly integrated with Synario, Lattice's pDS+ Synario Fitter features multi-level logic synthesis, automatic partitioning and mapping, design optimization for higher performance and better device utilization, and programming file creation.

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ispLSI and pLSI Device Support

Available in speed grades from 5.0ns to 20ns t_{PD} and 180MHz to 60MHz Fmax, the ispLSI 1000/E and 2000/V/LV family devices supported by this system represent the fastest and most innovative architectures in the CPLD industry. And best of all, they offer Lattice ISP technology.

ispGAL, GAL and ispGDS Device Support

The ispGAL22V10 is the industry's only in-system programmable 22V10 device and offers speeds up to 7.5ns maximum propagation delay. The logic functionality, fuse map, and AC and DC parameters of the ispGAL22V10 are fully compatible with standard bipolar and CMOS 22V10 devices. The 28-pin PLCC package provides the same functional pinout as the standard 22V10 by using the four no-connect pins on the 28-pin PLCC package for the ISP interface signals. The Lattice GAL device architectures supported include the 16V8, 16V8Z, 16LV8, 16LV8Z, 16VP8, 18V10, 20V8, 20LV8Z, 20RA10, 20VP8, 20XV10, 22LV10, 22V10, 26CV12, 6001, and 6002. Lattice's ispGDS family is a unique in-system programmable switch device with dual banks of I/O switches where any I/O switch in one bank can be driven by any I/O switch in the other bank. Lattice's ispGDS family consists of the ispGDS14, ispGDS18 and ispGDS22 devices.

ISP Daisy Chain Download and ispCODE

ISP Daisy Chain Download software is a comprehensive design download package for the LSC ISP device families. The ISP Daisy Chain software provides an efficient method of programming LSC devices using JEDEC files generated from any compatible software tool. This complete device programming tool helps you to quickly and easily program devices with your designs, supporting both the Microsoft Windows and DOS environments.

The ISP Daisy Chain Download software includes:

- — Support for Microsoft Windows 3.1x and Windows 95 design environments
- — Support for the DOS environment
- — JEDEC file conversion to the ispSTREAM™ for download directly from your system to a device
- — Detection and identification of as many as 60 devices in a daisy chain
- — Single ISP device programming
- — Multiple ISP device daisy chain programming
- — Easy set-up menus for multiple ports
- — Simple device configuration menus

ispCODE software includes ANSI C source routines for In-System Programming. ispCODE makes it easier to implement ISP technology programming using an embedded system microprocessor or ATE final test equipment.

Product Ordering Information

Product Code	Description
ISP-SYN2	ISP Synario System

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