3000 Family Architectural Description
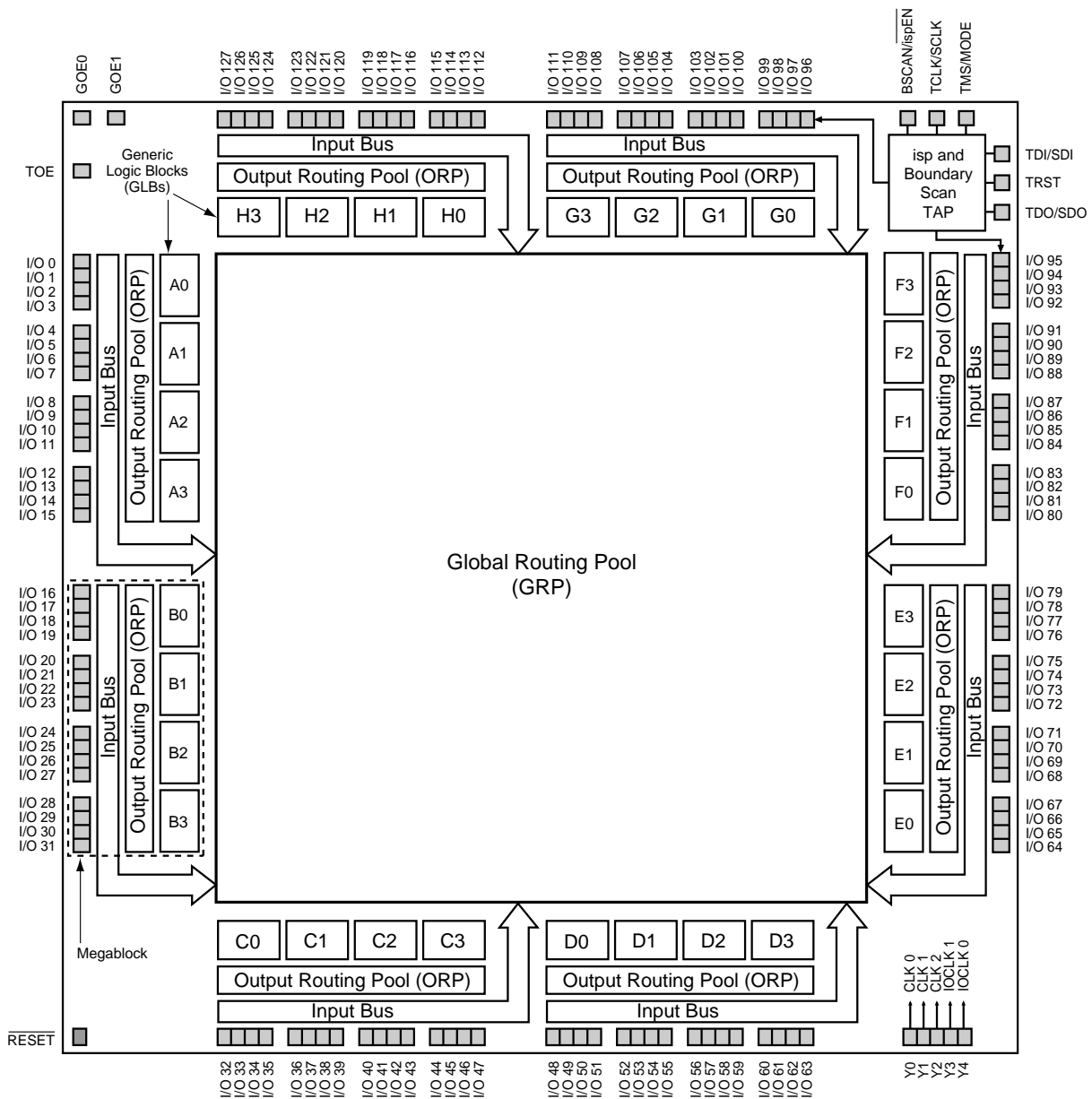
ispLSI and pLSI 3000 Family Introduction

The basic unit of logic of the ispLSI® and pLSI® 3000 family is closely related to that of the ispLSI and pLSI 1000/E family. However, there are some notable archi-tectural differences: Boundary Scan, Megablock and GLB structure, Global clock structure, and I/O cell struc-ture. A functional block diagram of the ispLSI 3256 device is shown in Figure 1. The architectural differences are described in the following sections.

Figure 1. ispLSI 3256 Functional Block Diagram

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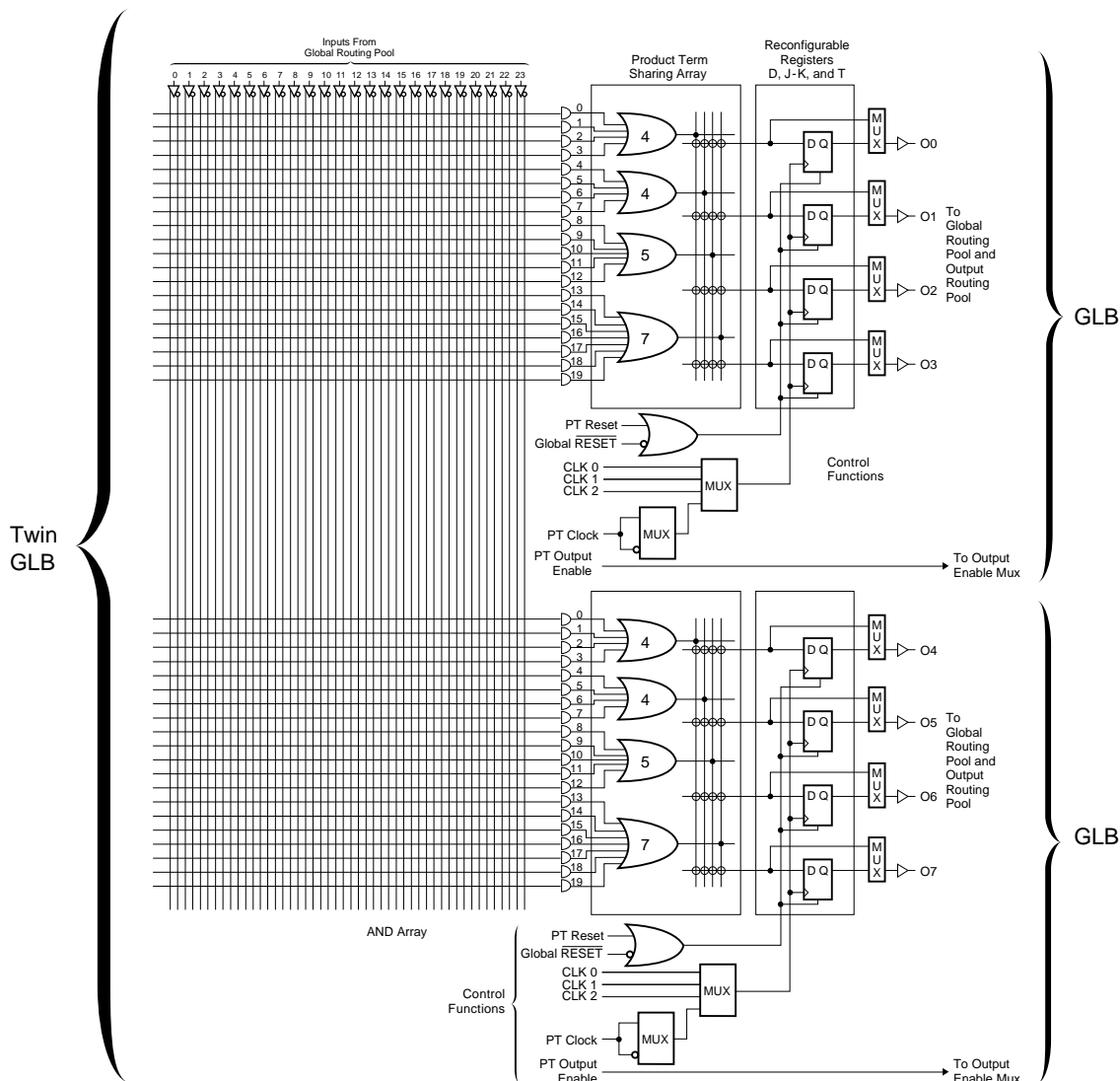# 3000 Family Architectural Description

Generic Logic Block

The Twin GLB™ is the standard logic block of the Lattice Semiconductor ispLSI and pLSI 3000 Family. This Twin GLB has 24 inputs, eight outputs and the logic necessary to implement most standard logic functions. The internal logic of the Twin GLB is divided into four separate sections: The AND Array, the Product Term Sharing Array, the Reconfigurable Registers, and the Control section.

The AND array consists of two 20 Product Term Sharing Arrays which can produce the logical sum of any of the 24 Twin GLB inputs. These inputs all come from the GRP, and are either feedback signals from any of the 32 Twin GLBs or inputs from the external I/O Cells. All Twin GLB input signals are available to the Product Terms in both the logical true and complemented forms which makes Boolean logic reduction easier.

The two Product Term Sharing Arrays (PTSA) take the 20 Product Terms each and allocate them to four Twin GLB outputs. There are four OR gates, with four, four, five and seven inputs respectively. The output of any of these gates can be routed to any of the four Twin GLB outputs, and if more Product Terms are needed, the PTSA can combine them as necessary. If the user's main concern is speed, the PTSA can use a bypass circuit with four Product Terms to increase the performance of the cell. This can be done to any or all of the eight outputs of the Twin GLB.

Figure 2. Twin GLB: Product Term Sharing Array

Megablock Structure

Four Twin GLBs make up a Megablock. Each GLB has a maximum fan-in of 24 inputs, and no dedicated inputs associated with any Megablock. A GLB has eight associated outputs. A total of 32 GLB outputs are fed to the ORP of "single I/O" 3000 family devices (i.e., those with one I/O pin for every two GLB outputs, such as the 3256).

However, only 16 out of the 32 outputs feed to 16 I/O cells. For "double I/O" 3000 family devices (those with one I/O pin for each GLB output, such as the 3192), 16 GLB outputs are fed to each ORP which drives 16 I/O cells. "Double I/O" devices, therefore, employ two ORP's per Megablock.The Megablock structure for single and double I/O devices is shown in Figures 3 and 4.

Figure 3. ispLSI and pLSI 3000 Family Single I/O Megablock Block Diagram
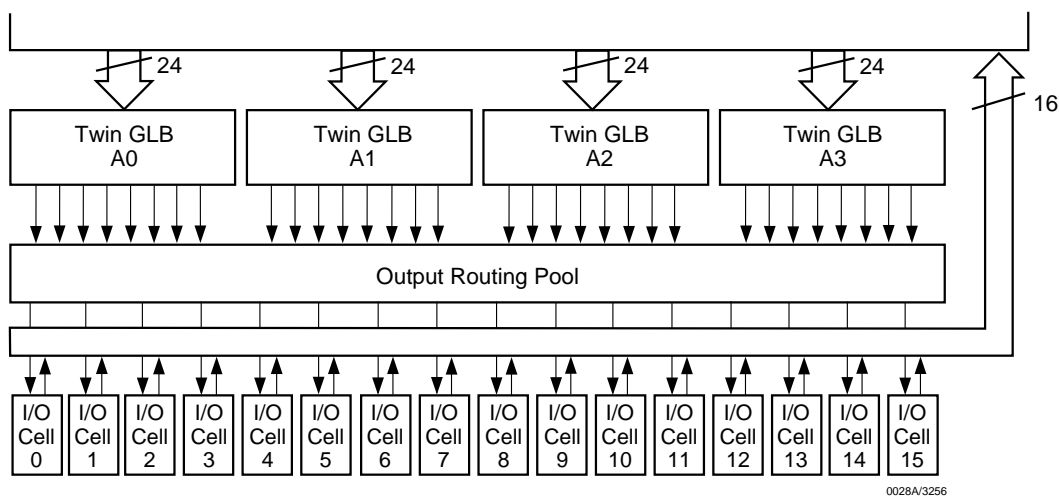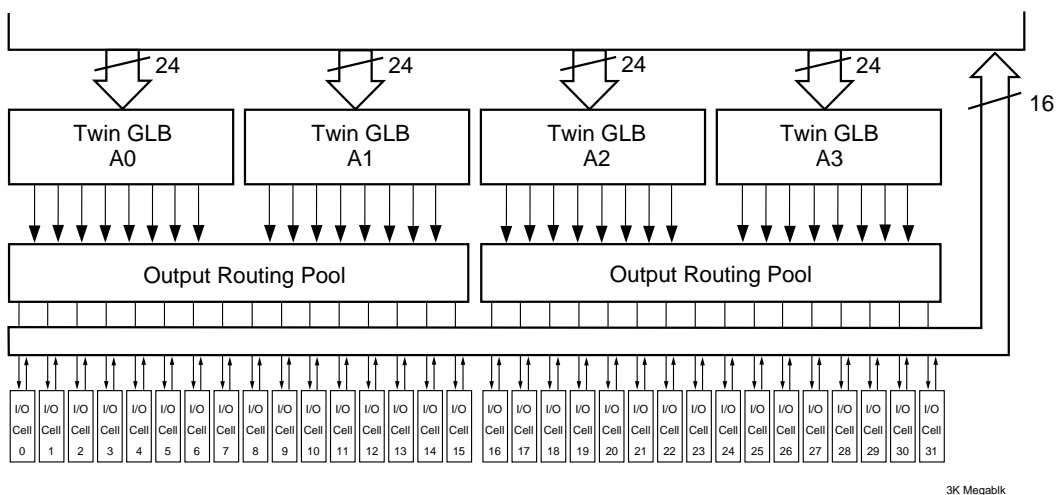

Figure 4. ispLSI and pLSI 3000 Family Double I/O Megablock Block Diagram

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Global Clock Structure

The global clock structure is made up of five global clock input pins, Y0, Y1, Y2, Y3, and Y4. This is shown in Figure 5. Three of the clock pins are dedicated for GLB clocks and the remaining two clock pins are dedicated for I/O register clocks. The clock GLB generation network which is designed into the 1000/E device family has been removed so all input clock signals are fed directly to the GLB clock input via a clock multiplexer. The GLB global clocks do not have inversion capability, but the product term clock does have inversion capability before it reaches the clock multiplexer.
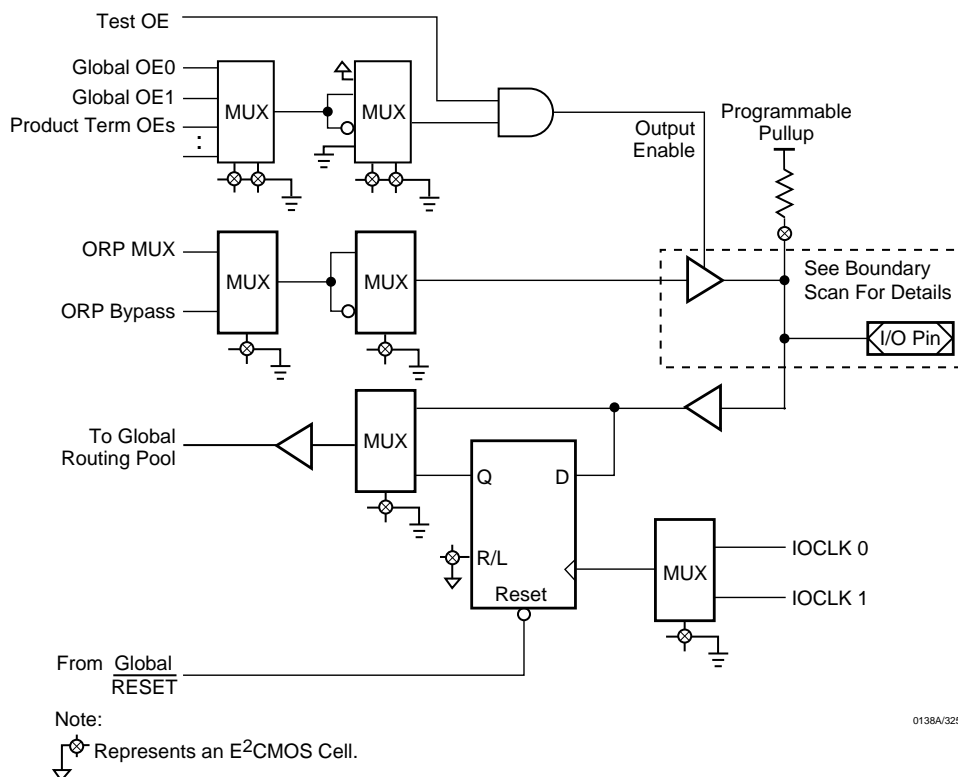
I/O Cells

The I/O cell structure architecture remains nearly the same as the 1000/E Family as illustrated in Figure 6. Each I/O cell now contains Boundary Scan Registers, shown in Figure 9 and discussed in detail in the next section. An input pin has only one scan register as shown in Figure 10. A global test OE signal is hardwired to all I/O cells and is useful to perform static testing of all the 3-state output buffers within the device. In addition to the test OE signal, two global OEs are connected to all I/O

Figure 5. ispLSI and pLSI 3000 Family Global Clock Structure
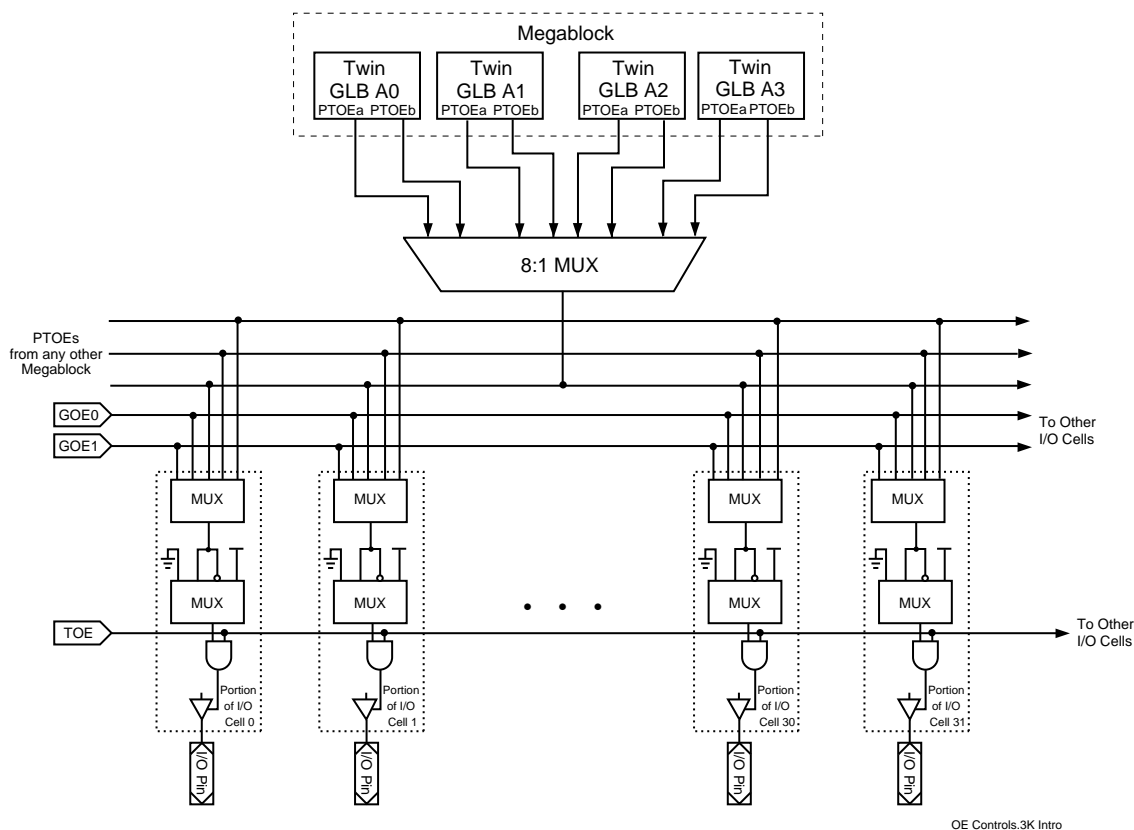

pins. The product term OE signal and global OE signals are fed to an OE multiplexer. The OE signals, with the exception of the test OE, have inversion capability after going through the OE multiplexer as shown in Figure 7.

Figure 6. ispLSI and pLSI 3000 Family I/O Cell Architecture

Note:

⌐⬦ Represents an E^{2}CMOS Cell.

Figure 7. ispLSI and pLSI 3000 Family Output Enable Controls
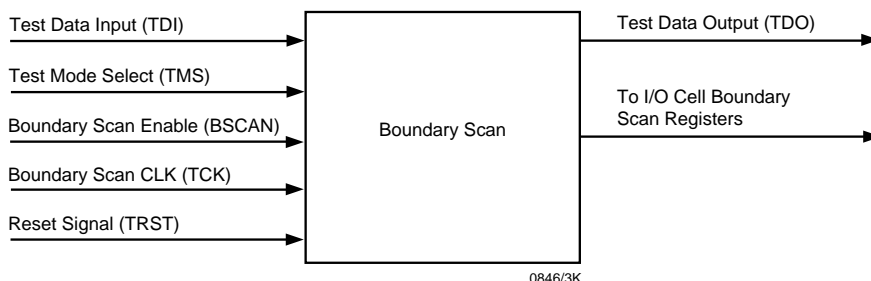

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Boundary Scan

Boundary Scan (IEEE 1149.1 compatible) is a test feature incorporated within the device to provide on-chip test capabilities during PCB testing. Five input signal pins, BSCAN, TDI, TCK, TMS, $\overline{TRST}$, and one output signal pin, TDO, are associated with the boundary scan logic cells. These signal pins occupy the same dedicated signal pins used for ISP programming. The signal BSCAN is associated with the ispEN pin, TDI corresponds to the SDI pin, TCK corresponds to the SCLK pin, TMS corresponds to the MODE pin, and TDO corresponds to the SDO pin. When ispEN is asserted low, the MODE, SDI, SDO, and SCLK options become active for ISP programming. Otherwise, BSCAN, TDI, TCK, TMS, TDO, and $\overline{TRST}$ options become active for boundary scan testing of the device. The boundary scan block diagram is shown in Figure 8. TDI is the test data serial input, TCK is the boundary scan clock associated with the serial shift register, TMS is the test mode select input, TDO is the test data output and $\overline{TRST}$ is the reset signal.

Figure 8. Boundary Scan Block Diagram

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The user interfaces to the boundary scan circuitry through the Test Access Port (TAP). The TAP consists of a control state machine, instruction decoder and instruction register.

The TAP is controlled using the test control lines: Test Data IN (TDI), Test Data Out (TDO), Test Mode Select (TMS), Test Reset (TRST) and Test Clock (TCK).

The TAP controls the operation of the Boundary Scan Registers after decoding the instruction code sent to the instruction register (see Table 1).

The Boundary Scan Registers for the I/O cells are shown in Figure 9. As illustrated in the figure, each I/O cell contains three registers, two latches and five multiplexers to implement the ability to capture the state of the

I/O cell or to set the state of the output path of the cell or to function as a conventional I/O cell.

The Boundary Scan Registers required for an input only cell are shown in Figure 10. An input only cell can only have its state captured, which only requires one MUX and one register.

All of the input cells and I/O cells are serially connected together in a long chain. The scan out of one cell is connected to the scan in of the next cell. The cells for the 3256 are connected in the following order: TDI to IO63 through IO32 to Y4, Y3, Y2, Y1, RESET, TOE, GOE1, GOE0, Y0, IO31 through IO0 to IO64 through IO127 to TDO. The cells for the 3192 are connected in the following order: TDI to GOE0, GOE1, Y0, Y1, Y2, Y3, Y4, RESET, I/O95 through I/O0 to I/O96 through I/O191 to TDO.

Figure 9. Boundary Scan Registers for I/O Cells

Figure 10. Boundary Scan Registers for an Input Only Cell

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Table 1. Boundary Scan Instruction Codes

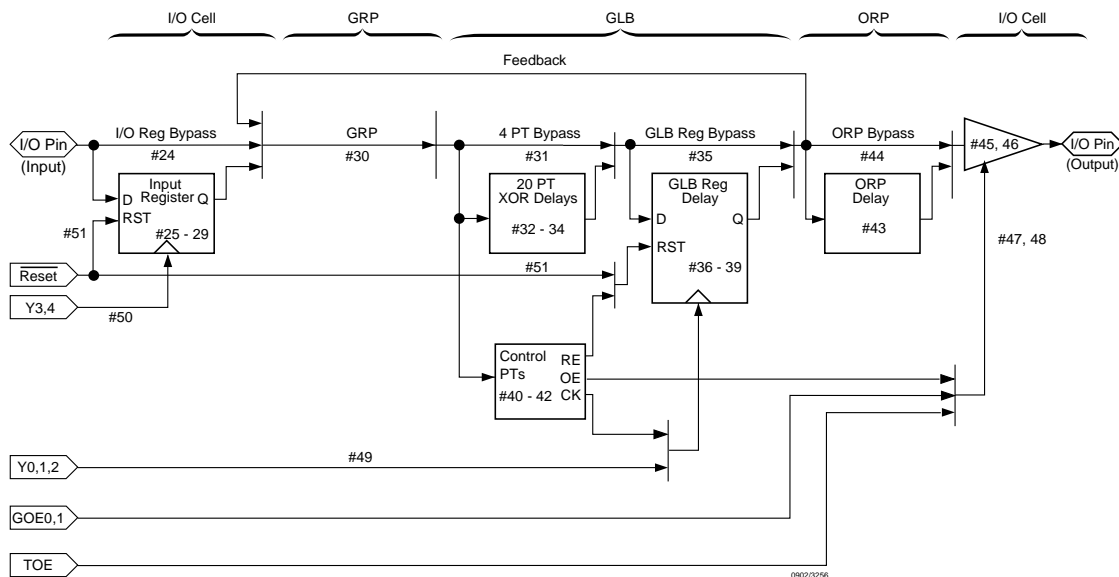| Instruction Name	Code		Description
SAMPLE/PRELOAD	10*	11100	Loads and shifts data into BSCAN registers
EXTEST	00*	00000	Drives external I/O with BSCAN registers
BYPASS	11*	11111	Bypasses registers of selected device(s)

Note: LSB shifts in 1st
*3256 only

Table 10-0006/3K

Timing Model

The task of determining the timing through the device is simple and straightforward. A device timing model is shown in Figure 11. To determine the time that it takes for data to propagate through the device, simply determine the path the data is expected to follow, and add the various delays together (Figure 12). Critical timing paths are shown in Figure 11, using data sheet parameters. Note that the Internal timing parameters are given for reference only, and are not tested. External timing parameters are tested and guaranteed on every device.

Figure 11. ispLSI and pLSI 3256 Timing Model

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Figure 12. Timing Calculation Example

Derivations of tsu, th and tco from the Product Term Clock[1]

tsu   = Logic + Reg su - Clock (min)
           = (**t**iobp + **t**grp + **t**20ptxor) + (**t**gsu) - (**t**iobp + **t**grp + **t**ptck(min))
           = (#24+ #30+ #33) + (#36) - (#24+ #30+ #42)
  8.0 ns = (2.4 + 3.0 + 9.4) + (1.8) - (2.4 + 3.0 + 3.2)

th   = Clock (max) + Reg h - Logic
           = (**t**iobp + **t**grp + **t**ptck(max)) + (**t**gh) - (**t**iobp + **t**grp + **t**20ptxor)
           = (#24+ #30+ #42) + (#37) - (#24+ #30+ #33)
  2.9 ns = (2.4 + 3.0 + 6.3) + (6.0) - (2.4 + 3.0 + 9.4)

tco   = Clock (max) + Reg co + Output
           = (**t**iobp + **t**grp + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
           = (#24 + #30 + #42) + (#38) + (#43 + #45)
  2.9 ns = (2.4 + 3.0 + 6.3) + (1.8) + (2.7 + 2.4)

Table 2- 0042-16/3256

1. Calculations are based upon timing specifications for the ispLSI and pLSI 3256-70L.

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LATTICE SEMICONDUCTOR CORPORATION
5555 Northeast Moore Court
Hillsboro, Oregon 97124 U.S.A.
Tel.: (503) 681-0118
FAX: (503) 681-3037
http://www.latticesemi.com   November 1996