

Key Technology Corp.

FC1306T(GP)

Single Chip Controller for PC ATA Card Adapters

User's Programming Manual

(KTC Confidential)

Revision Logs:

Features:

1. Host Interface:

- 1) Support PC Card ATA, Compact Flash and true IDE interface.
- 2) Fully compatible with PC Card Standard.
- 3) Fully compatible with CFA(Compact Flash Association) Standard.
- 4) Four PC Card ATA Modes:
Common Memory Mapped.
Contiguous I/O Mapped.
Primary I/O(1Fx) Mapped.
Secondary I/O(17x) Mapped.
- 5) Compatible with all PC Card Services and Socket Service.
- 6) Automatic sensing of PC Card ATA or true IDE host interface.
- 7) PIO, Multi-word DMA and Ultra DMA Host Data transfer Support.
- 8) Support 8-bit / 16-bit data transfer on host data bus.
- 9) Integrated PC Card attribute memory of 256 Bytes(CIS).
- 10) 4 PC Card function registers support.
- 11) Automatic wake up from power-down on host reset or command write.
- 12) Sector data transfers without microprocessor intervention.
- 13) ATAPI Interface (SSF-8020i and SFF-8070i)

2. Buffer Management:

- 1) Built-in 1Kx16 SRAM for Data Buffer.
- 2) Auto Data Movement based on the sector (256 words) size.
- 3) Multi-Address Pointer support for different device interface.

3. Error Correction Logic:

- 1) Data Interleave to 2 for each 256 Bytes.
- 2) Error Correction of 1 Byte random error per 128 Bytes of data.
- 3) Automatic on-the-fly, in-buffer error correction.
- 4) Built-in Standard SmartMedia Hardware ECC circuit.

4. Flash Memory Control:

- 1) Flash Sequencer Logic to support all the control signals to execute read/write/erase operation automatically.
- 2) Flash Write Protect control support.
- 3) Support Samsung / Toshiba 16/32/64/128/256/512/1024/2048 Mbits NAND type flash memories.
- 4) Support Hitachi 64/128/256/512 Mbits AND type flash memories.
- 5) Support SmartMedia / SmartMedia 256 Card.
- 6) Support up to 8 devices.
- 7) 8-bit Flash Data I/O.

5. MMC-Port for MMC/SD Card:

- 1) Fully compatible with MMC system specification 2.0.
- 2) Fully compatible with SD Memory Card specification 1.0.
- 3) Standard MMC Mode Interface support.
- 4) Standard SPI(Serial Programming Interface) Interface (option mode of MMC) for MMC(MultiMediaCard) Card.
- 5) Programmable Clock Rate (62.5KHz ~ 24MHz).
- 6) Microprocessor I/O transfer mode (High flexibility) or Automation transfer mode (High speed) Support.
- 7) Auto Command/Response CRC generation/check.
- 8) Auto Data CRC generation/check.
- 9) 2 Clock Lines support for twin-card operation.

6. MS-Port for Memory Stick /Memory Stick Pro Card:

- 1) Fully compatible with Memory Stick Standard -- Format Specification 1.2.
- 2) Programmable Clock Rate (62.5KHz ~ 24MHz).
- 3) Microprocessor I/O transfer mode (High flexibility) or **Automatic** transfer mode (High speed) Support.
- 4) Auto Interface waveform generation.
- 5) Auto Data CRC generation/check.
- 6) 2 Clock Lines support for twin-card operation.
- 7) Support Memory Stick Pro **1-bit / 4-bit** data transfer.

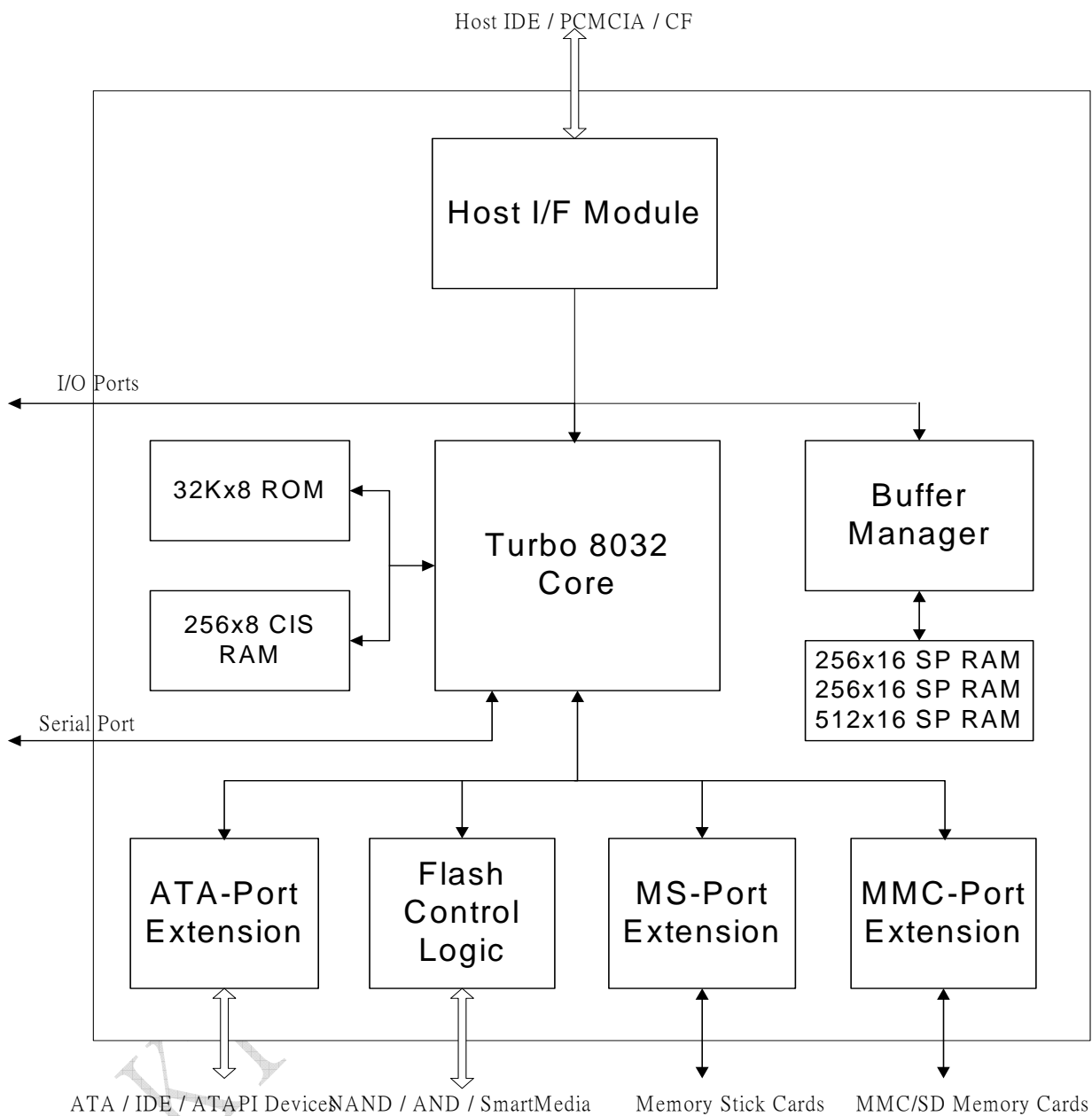
7. ATA-Port for PC ATA Cards / CompactFlash Cards / IDE Devices / ATAPI Devices:

- 1) Support Standard PC Card ATA Host Interface.
- 2) Support Standard True IDE mode Host Interface.
- 3) Support ATAPI Packet Command interface.
- 4) Programmable Register Accessing Cycle Rate (Waveform timing).
- 5) 8-bit/16-bit Data bus selection for Task File Registers Accessing.
- 6) Full Task File Register Set Support.
- 7) Direct Buffer Accessing for Data or Command Packet Transferring.

8. Miscellaneous:

- 1) +5.5V ~ +3.0V wide range power supply.
- 2) Available in 100-lead/128-lead TQFP and QFP package.

Functional Block Diagram:



FC1306 Pins Assignment: total 100/128 pins

Bd.	Pin #		Type	Pin Name	Description
1	1	1	I/O	HD3	Host Data Bus 3
2	2	2	I/O	HD11	Host Data Bus 11
3	3	3	I/O	HD4	Host Data Bus 4
4	4		I/O	A15	Micro-processor Address Bus 15
5	5	4	I/O	HD12	Host Data Bus 12
6	6	5	I/O	HD5	Host Data Bus 5
7	7	6	I/O	HD13	Host Data Bus 13
8	8		I/O	A14	Micro-processor Address Bus 14
9	9	7	I/O	HD6	Host Data Bus 6
10	10	8	I/O	HD14	Host Data Bus 14
11	11	9	I/O	HD7	Host Data Bus 7
12	12		I/O	A13	Micro-processor Address Bus 13
13	13	10	I/O	HD15	Host Data Bus 15
14	14	11	P	VCC5IP	Host voltage: 3.3v/5v
15	14	11	P	VCC5IP	Host voltage: 3.3v/5v
16	15	12	I	CE1#	Card Enable 1. (Pull up 50KΩ)
17	16		I/O	A12	Micro-processor Address Bus 12
18	17	13	I	CE2#	Card Enable 2. (Pull up 50KΩ)
19	18	14	I O	HA10 DA10	Host PCMCIA: PC Card ATA Address 10 Device PCMCIA: PC Card ATA Address 10
20	19	15	I I	HOE# IDE_CS#	Host Output Enable. (Pull up 50KΩ) Host True IDE interface Select
21	20		I/O	A11	Micro-processor Address Bus 11
22	21	16	P	GND	I/O Ground
23	21	16	P	GND	I/O Ground
25	22	17	I	ENCLK	ENCLK='1', ExtCLK . ENCLK='0', IntCLK
26	23	18	I	HIOR#	Host I/O Read. (Pull up 50KΩ)
27	24	19	I	HIOW#	Host I/O Write. (Pull up 50KΩ)
28	25	20	I O	HA9 DA9	Host PCMCIA: PC Card ATA Address 9 Device PCMCIA: PC Card ATA Address 9
29	26		I/O	A10	Micro-processor Address Bus 10
30	27	21	I O	HA8 DA8	Host PCMCIA: PC Card ATA Address 8 Device PCMCIA: PC Card ATA Address 8
31	28	22	I O	HWE# DOE#	Host Write Enable. (Pull up 50KΩ) Device Output Enable
32	29		I/O	A9	Micro-processor Address Bus 9
33	30	23	P	VDD	I/O VDD
34	30	23	P	VDD	I/O VDD
35	31	24	O I O T	HRDY Mas/Sla HIRQ# HIRQ	Memory: PC Card is Ready Select Mas/Sla PC Card I/O: Host Interrupt Request. True IDE: Host Interrupt Request.
36	32	25	I O	HA7 DA7	Host PCMCIA: PC Card ATA Address 7 Device PCMCIA: PC Card ATA Address 7
37	33	26	I O	HA6 DA6	Host PCMCIA: PC Card ATA Address 6 Device PCMCIA: PC Card ATA Address 6
38	34	27	I	HRST	Host Reset.(Schmit)
39	35		I/O	A8	Micro-processor Address Bus 8
40	36	28	I O	HA5 DA5	Host PCMCIA: PC Card ATA Address 5 Device PCMCIA: PC Card ATA Address 5
41	37	29	O	WAIT#	Host Wait. (Pull up 50KΩ)
42	38		I/O	A7	Micro-processor Address Bus 7
43	39	30	I O	HA4 DA4	Host PCMCIA: PC Card ATA Address 4 Device PCMCIA: PC Card ATA Address 4

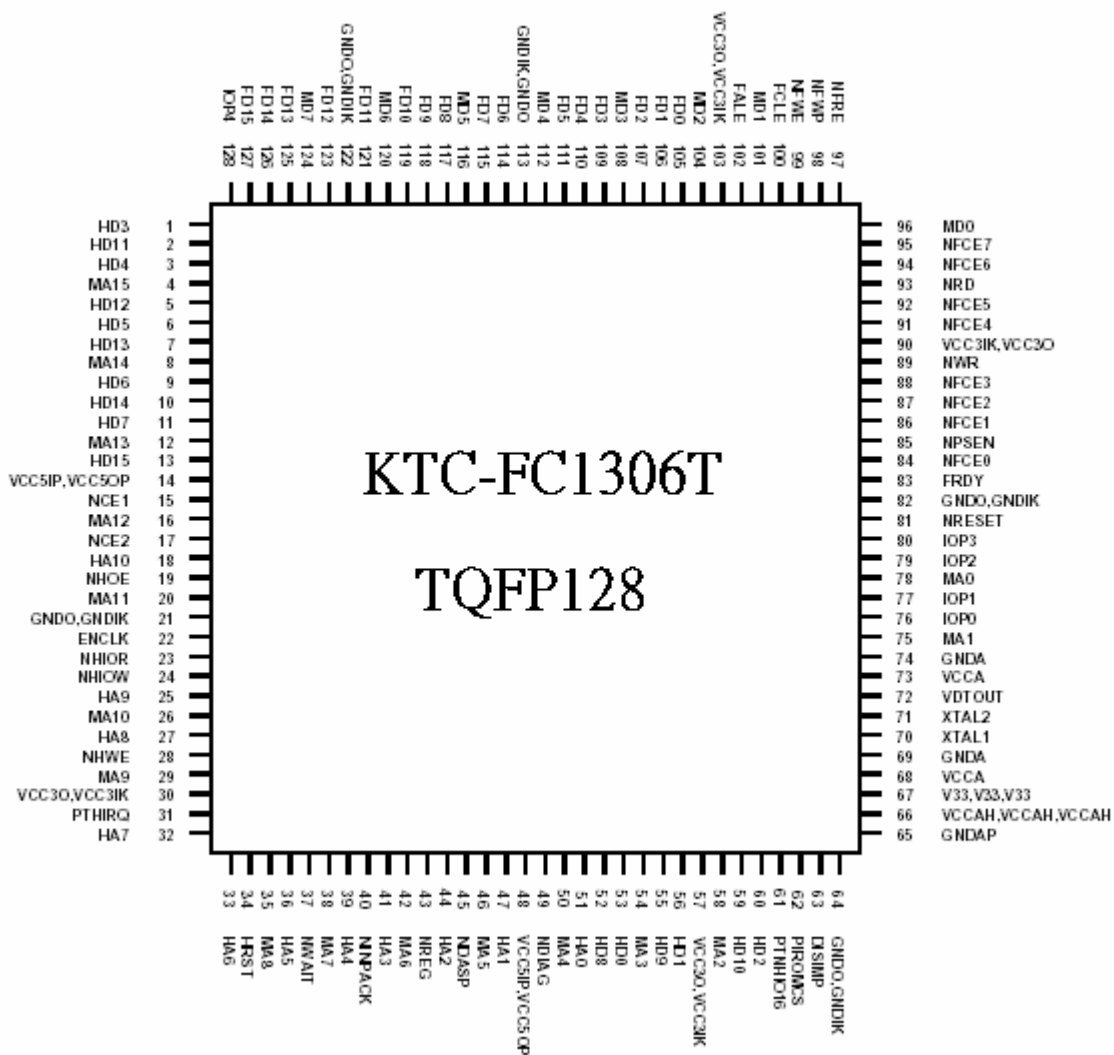
44	40	31	O T	INPACK# DMARQ	PC Card: Input Acknowledge DMA Acknowledge as ATA DMA
45	41	32	I O	HA3 DA3	Host PCMCIA: PC Card ATA Address 3 Device PCMCIA: PC Card ATA Address 3
46	42		I/O	A6	Micro-processor Address Bus 6
47	43	33	I I	REG# DMACK#	Attribute Memory Access (Pull up 50KΩ) Host IDE: DMA Acknowledge
48	44	34	I	HA2	Host Address Bus 2
49	45	35	O O I/O	BVD2 SPKR# DASP#	Memory: Battery Voltage Detect 2. PC Card I/O: Audio Speaker Drive Active/Slave Present. (Pull up 50KΩ)
50	46		I/O	A5	Micro-processor Address Bus 5
51	47	36	I	HA1	Host Address Bus 1
52	48		P	VCC5IP	Host voltage: 3.3v/5v
52	48		P	VCC5IP	Host voltage: 3.3v/5v
53	49	37	O O I/O	BVD1 STSCHG# PDIAG#	Memory: Battery Voltage Detect 1. PC Card I/O: Status Changed. Drive Passed Diagnostics. (Pull up 50KΩ)
54	50		I/O	A4	Micro-processor Address Bus 4
55	51	38	I	HA0	Host Address Bus 0
56	52	39	I/O	HD8	Host Data Bus 8
57	53	40	I/O	HD0	Host Data Bus 0
58	54		I/O	A3	Micro-processor Address Bus 3
59	55	41	I/O	HD9	Host Data Bus 9
60	56	42	I/O	HD1	Host Data Bus 1
61	57	43	P	VDD	I/O VDD
62	57	43	P	VDD	I/O VDD
63	58		I/O	A2	Micro-processor Address Bus 2
64	59	44	I/O	HD10	Host Data Bus 10
65	60	45	I/O	HD2	Host Data Bus 2
66	61	46	O O T	WP IOIS16# IOIS16#	Memory: Card is Write Protected PC Card I/O: Host Data I/O is 16-bit. Host IDE: Host Data I/O is 16-bit.
67	62	47	I	IROMCS#	Internal ROM Chip Select (Pull down 50KΩ)
68	63	48	I	DIS_IMP	Disable Internal 8032 (Pull down 50KΩ)
69	64	49	P	GND	I/O Ground
70	64	49	P	GND	I/O Ground
71				TC2	Oscillator trimming pad
72				TB2	Oscillator trimming pad
73				TA2	Oscillator trimming pad
74				VREF2	
75	65	50	P	GND	Analog Ground
76	66	51	A	VHV	Analog VCC for 3.3V Regulator
77	66	51	A	VHV	Analog VCC for 3.3V Regulator
78	66	51	A	VHV	Analog VCC for 3.3V Regulator
79	67	52	A	V33_OUT	3.3V Regulation Output
80	67	52	A	V33_OUT	3.3V Regulation Output
81	67	52	A	V33_OUT	3.3V Regulation Output
82	68	53	P	AVDD	Analog OSC VDD.
83	69	54	A	AGND	Analog Ground
84				TA3	Regulator trimming pad
85				TB3	Regulator trimming pad
86				TC3	Regulator trimming pad
87	70	55	I	XTAL1	Crystal Port 1, Clock input
88	71	56	O	XTAL2	Crystal Port 2
89	72	57	P	VDTOUT	
90	73	58	P	VDT Power	
91	74	59	P	GND	I/O Ground

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92				TA1	VDT trimming pad
93				TB1	VDT trimming pad
94				TC1	VDT trimming pad
95				VREF1	
96	75		I/O	A1	Micro-processor Address Bus 1
97	76	60	I/O	IOP0	Internal 8032 P1.0 (Pull up 50KΩ)
98	77	61	I/O	IOP1	Internal 8032 P1.1
99	78		I/O	A0	Micro-processor Address Bus 0
100	79	62	I/O	IOP2	Internal 8032 P1.2
101	80	63	I/O	IOP3	Internal 8032 P1.3
102	81	64	I	RESET#	Chip Reset. (Schmidt)
103	82	65	P	GND	I/O Ground
104	82	65	P	GND	I/O Ground
105	83	66	I	FARDY	Flash A-Port Ready/Busy- (Schmit, Pull up 50KΩ)
106	84	67	O	FCE0#	Flash Device Select 0
107	85		I O	PSEN# PSEN#	ROM Output Enable (Pull up 50KΩ), External uP (Input) / Internal uP (output)
108	86	68	O O	FCE1# NDREG	Flash Device Select 1 ATA-Port NDREG
109	87	69	O O O	FCE2# MSCLK1 DA1	Flash Device Select 2 Memory Stick: Synchronous Clock 1 Device PCMCIA: PC Card ATA Address 1
110	88	70	O O O	FCE3# MCLK1 DA2	Flash Device Select 3 MMC/SD: Synchronous Clock 1 Device PCMCIA: PC Card ATA Address 2
111	89		I O	MWR# MWR#	Micro-processor Write (Pull up 50KΩ), External (Input) / Internal (output)
112	90	71	P	VDD	I/O VDD
113	90	71	P	VDD	I/O VDD
114	91	72	O O	FCE4# MSCLK0	Flash Device Select 4 Memory Stick: Synchronous Clock 0
115	92	73	O O	FCE5# MCLK0	Flash Device Select 5 MMC/SD: Synchronous Clock 0
116	93		I O	MRD# MRD#	Micro-processor Read (Pull up 50KΩ), External (Input) / Internal (output)
117	94	74	O O	FCE6# AT_CE1#	Flash Device Select 6 ATA-Port: Card Enable 1
118	95	75	O O	FCE7# AT_CE2#	Flash Device Select 7 ATA-Port: Card Enable 2
119	96		I/O	MD0	Micro-processor Data Bus 0
120	97	76	O O O	FARE# FAOE# AT_IOR#	NAND: Flash A-Port Read Enable AND: Flash A-Port Output Enable ATA-Port: IO read strobe
121	98	77	O O O	FWP# DWE# FRES#	NAND: Flash Write Protect Device Write Enable AND: Flash Reset
122	99	78	O O	FAWE# AT_IOW#	Flash A-Port Write Enable Strobe ATA-Port: IO write strobe.
123	100	79	O O	FCLE FCDE#	NAND: Flash Command Latch Enable AND: Flash Command Data Enable
124	101		I/O	MD1	Micro-processor Data Bus 1
125	102	80	O O O	FAALE FASC DA0	NAND: Flash A-Port Address Latch Enable AND: Flash A-Port Serial Clock Device PCMCIA: PC Card ATA Address 0
126	103	81	P	VDD	I/O VDD.
127	103	81	P	VDD	I/O VDD.
128	104		I/O	MD2	Micro-processor Data Bus 2
129	105	82	I/O I/O	FAD0 ATD0	Flash A-Port Data Bus 0 (Pull up 50KΩ) ATA-Port: Data Bus 0

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130	106	83	I/O I/O	FAD1 ATD1	Flash A-Port Data Bus 1 (Pull up 50KΩ) ATA-Port: Data Bus 1
131	107	84	I/O I/O O	FAD2 ATD2 MS_BS	Flash A-Port Data Bus 2 (Pull up 50KΩ) ATA-Port: Data Bus 2 MS-Port: Bus State
132	108		I/O	MD3	Micro-processor Data Bus 3
133	109	85	I/O I/O I/O	FAD3 ATD3 MS_SD0	Flash A-Port Data Bus 3 (Pull up 50KΩ) ATA-Port: Data Bus 3 MS-Port: SDIO of Memory Stick Cards
134	110	86	I/O I/O I/O	FAD4 ATD4 MS_SD1	Flash A-Port Data Bus 4 (Pull up 50KΩ) ATA-Port: Data Bus 4 MS-Port: SDIO of Memory Stick Cards
135	111	87	I/O I/O I/O	FAD5 ATD5 MS_SD2	Flash A-Port Data Bus 5 (Pull up 50KΩ) ATA-Port: Data Bus 5 MS-Port: SDIO of Memory Stick Cards
136	112		I/O	MD4	Micro-processor Data Bus 4
137	113	88	P	CGND	Core Ground
138	113	88	P	CGND	Core Ground
139	114	89	I/O I/O I/O	FAD6 ATD6 MS_SD3	Flash A-Port Data Bus 6 (Pull up 50KΩ) ATA-Port: Data Bus 6 MS-Port: SDIO of Memory Stick Cards
140	115	90	I/O I/O	FAD7 ATD7	Flash A-Port Data Bus 7 (Pull up 50KΩ) ATA-Port: Data Bus 7
141	116		I/O	MD5	Micro-processor Data Bus 5
142	117	91	I/O	ATD8	ATA-Port: Data Bus 8
143	118	92	I/O	ATD9	ATA-Port: Data Bus 9
144	119	93	I/O I/O	ATD10 MMC_DAT3	ATA-Port: Data Bus 10 MMC mode: MMC Data 3 Line.
145	120		I/O	MD6	Micro-processor Data Bus 6
146	121	94	I/O I/O	ATD11 MMC_DAT2	ATA-Port: Data Bus 11 MMC mode: MMC Data 2 Line.
147	122	95	P	GND	I/O Ground
148	122	95	P	GND	I/O Ground
149	123	96	I/O I/O	ATD12 MMC_DAT1	ATA-Port: Data Bus 12 MMC mode: MMC Data 1 Line.
150	124		I/O	MD7	Micro-processor Data Bus 7
151	125	97	I/O	ATD13	ATA-Port: Data Bus 13
152	126	98	I/O I/O O	ATD14 MMC_CMD SPI_DO	ATA-Port: Data Bus 14 MMC Mode: MMC Command Line. SPI-Port: SPI Data output
153	127	99	I/O I/O I	ATD15 MMC_DAT0 SPI_DI	ATA-Port: Data Bus 15 MMC mode: MMC Data Line. SPI-Port: SPI Data input
154	128	100	I/O O O	IOP4 HINT SDIO	Internal 8032 P1.4 External 32 mode :HINT Memory Stick SDIO



Electrical Specifications:

1. DC Characteristics:

Absolute Maximum Rating

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Core power supply	-0.3 to 3.9	V
V _{CC5}	Power supply of 5V I/O	-0.3 to 6.0	V
V _{IN3}	Input voltage of 3.3V I/O	-0.3 to V _{CC} +0.3	V
	Input voltage of 3.3V I/O with 5V tolerance	-0.3 to V _{CC5} +0.3	V
V _{IN5}	Input voltage of 5V I/O	-0.3 to V _{CC5} +0.3	V
V _{OUT3}	Output voltage of 3.3V I/O	-0.3 to V _{CC} +0.3	V
V _{OUT5}	Output voltage of 5V I/O	-0.3 to V _{CC5} +0.3	V
T _{STG}	Storage temperature	-40 to 150	°C

Note: Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the optional sections of this datasheet. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

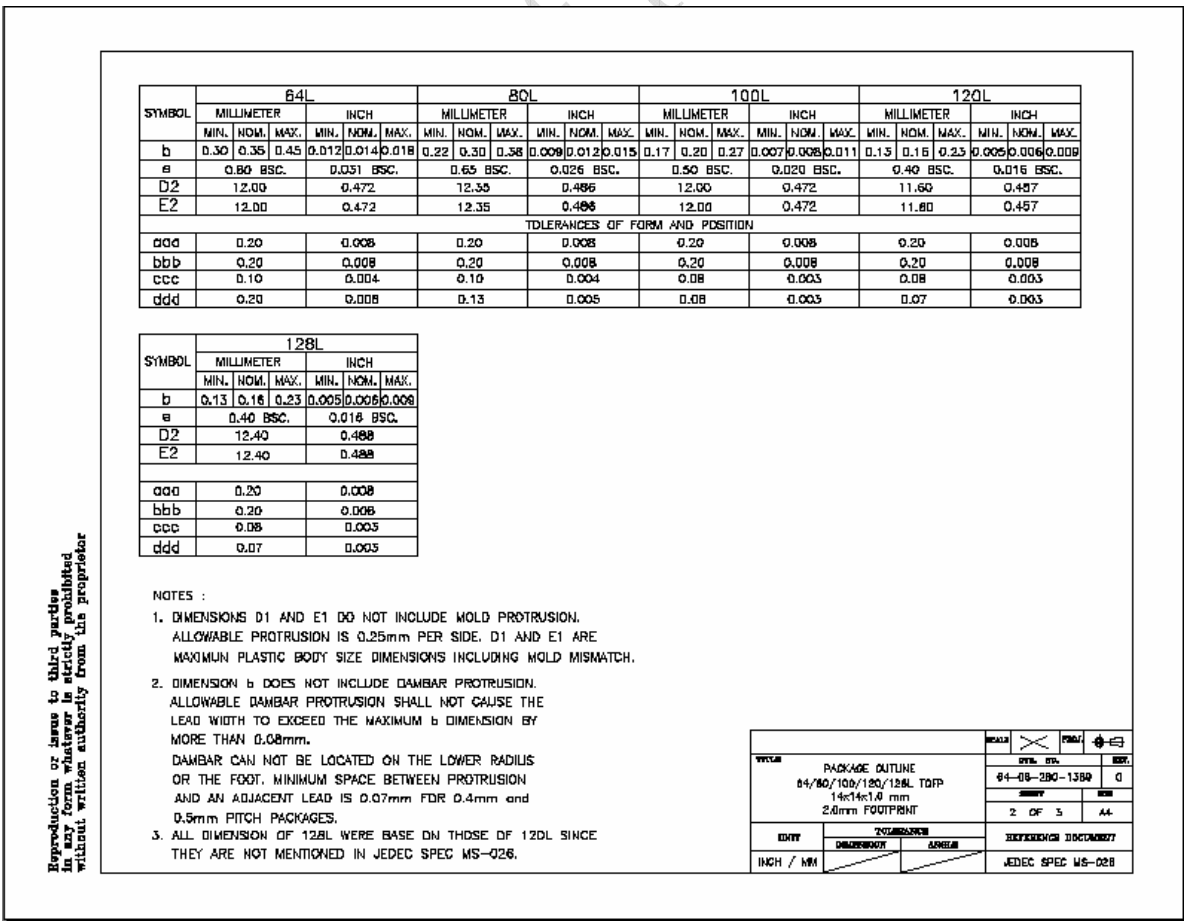
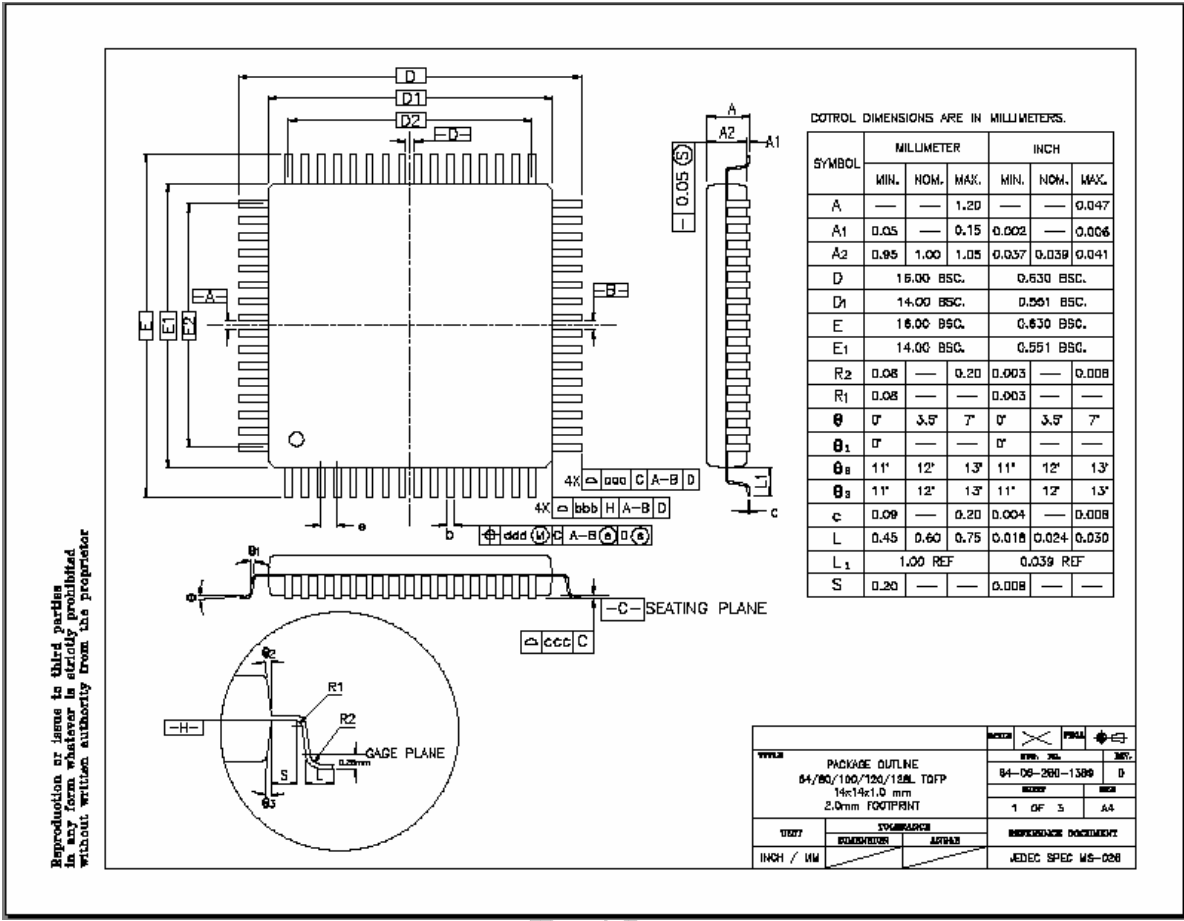
SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	
V _{CC}	Core power supply	3.0	3.3	3.6	V	
V _{CC5}	Power supply of 5V I/O	Commercial	4.75	5.0	5.25	V
		Industrial	4.5	5.0	5.5	V
V _{IN3}	Input voltage of 3.3V I/O	0	3.3	3.6	V	
	Input voltage of 3.3V I/O with 5V tolerance	0	3.3	5.25	V	
V _{IN5}	Input voltage of 5V I/O	0	5	5.25	V	
T _j	Junction operating temperature	Commercial	0	25	115	°C
		Industrial	-40	25	125	°C

Leakage Current and Capacitance

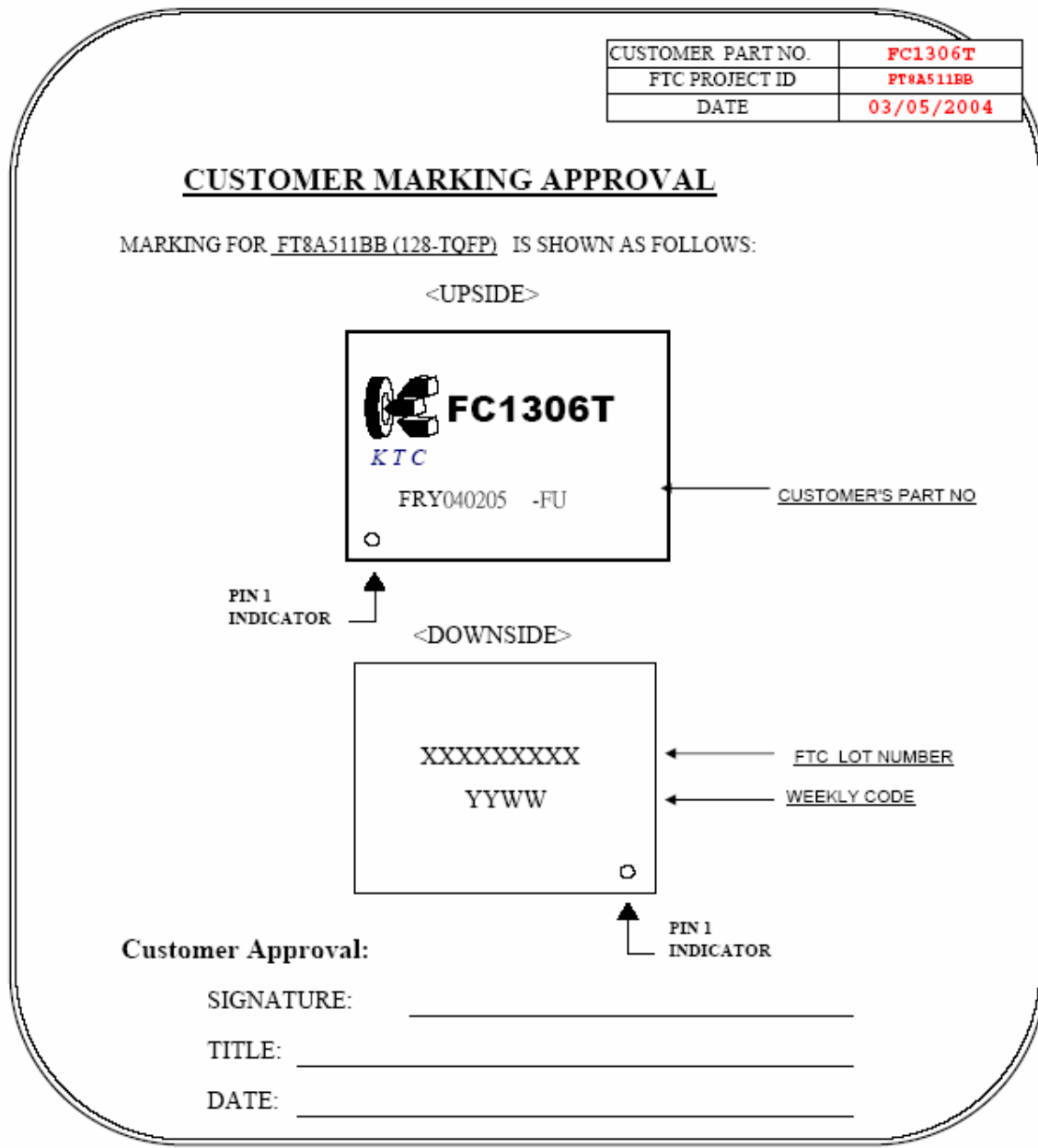
SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
I _{IN}	Input leakage current	No pull-up or pull-down	-10	±1	10	μA
I _{OZ}	Tri-state leakage current		-10	±1	10	μA
C _{IN3}	3.3V input capacitance			2.8		pF
C _{OUT3}	3.3V output capacitance			3.3		pF
C _{BID3}	3.3V bi-directional capacitance			4		pF
C _{IN5}	5V input capacitance			4		pF
C _{OUT5}	5V output capacitance			4.4		pF
C _{BID5}	5V bi-directional capacitance			4.4		pF

DC Characteristics of 3.3V I/O Cells

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V _{CK}	Core power supply	Core area	3.0	3.3	3.6	V
V _{CC3I}	Power supply	3.3V I/O	3.0	3.3	3.6	V
V _{CC3O}	Power supply		3.0	3.3	3.6	V
V _{il}	Input low voltage	CMOS			0.3*V _{CC}	V
V _{ih}	Input high voltage		0.7*V _{CC}			V
V _{il}	Input low voltage	LVTTTL			0.8	V
V _{ih}	Input high voltage		2.0			V
V _{t-}	Schmitt trigger negative going threshold voltage	CMOS	0.9	1.2		V
V _{t+}	Schmitt trigger positive going threshold voltage			2.1	2.5	V
V _{t-}	Schmitt trigger negative going threshold voltage	LVTTTL	0.9	1.1		V
V _{t+}	Schmitt trigger positive going threshold voltage			1.6	1.9	V
V _{ol}	Output low voltage	I _{ol} = 2 ~ 24 mA			0.44 ⁽²⁾	V
V _{oh}	Output high voltage	I _{oh} = -2 ~ -24 mA	2.4			V
R _{pu}	Input pull-up resistance	V _{in} = 0	40	75	190	KΩ
R _{pd}	Input pull-down resistance	V _{in} = V _{CC3I}	40	75	190	KΩ



3.2 Normal Package Logo

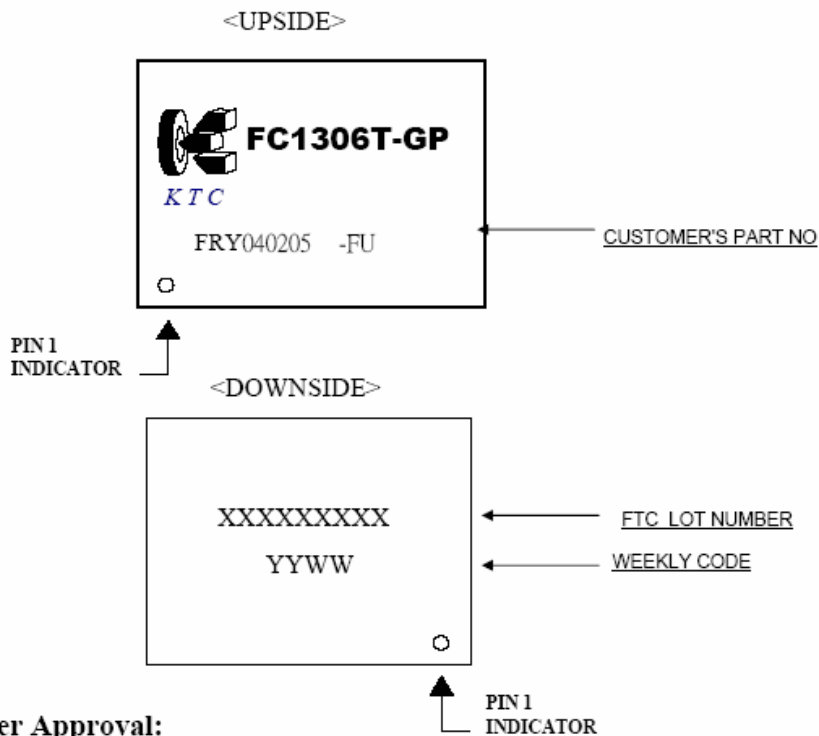


3.3 Green Package Logo

CUSTOMER PART NO.	FC1306T
FTC PROJECT ID	FT8A511BC
DATE	03/05/2004

CUSTOMER MARKING APPROVAL

MARKING FOR FT8A511BB (128-TQFP) IS SHOWN AS FOLLOWS:



Customer Approval:

SIGNATURE:

TITLE:

DATE:

KTC

4. Green Package Report

4.1 Test Report of Compound (G700)



Chemical Laboratory - KAO.,SGS Taiwan Ltd.

TEST REPORT

REPORT NO.KA/2004/C0492/A-1
 DATE: 2004/12/14
 PAGE: 1 OF 1

THE FOLLOWING MERCHANDISE WAS(WERE) SUBMITTED AND IDENTIFIED BY THE CLIENT AS :

CLIENT : SUMITOMO BAKELITE CO.,LTD.
PRODUCT DESCRIPTION : PART (1) (KA/2004/C0268 2004/12/8 TO 2004/12/14).
 : EPOXY MOLDING COMPOUND .
 : EME-G700
 : PART (2) (KA/2004/B0376 2004/11/20 TO 2004/11/26).
 : EPOXY RESIN EME-G700
SAMPLE RECEIVED : (1)2004/12/8 (2)2004/11/19

WE HAVE TESTED THE SAMPLE(S) SUBMITTED AS REQUESTED AND THE FOLLOWING RESULTS WERE OBTAINED.

PART (1) (KA/2004/C0268 2004/12/8 TO 2004/12/14)
 EPOXY MOLDING COMPOUND
 EME-G700

TEST ITEM(S)	UNIT	METHOD	DET. LMT	RESULT
CADMIUM	ppm	ANALYSIS BY ICP-AES WITH ADVANCE TREATMENT EN1122, METHOD B:2001.	2	n.d.

PART (2) (KA/2004/B0376 2004/11/20 TO 2004/11/26).
 EPOXY RESIN EME-G700

TEST ITEM(S)	UNIT	METHOD	DET. LMT	RESULT
CHROMIUM VI	ppm	ANALYSIS BY US EPA 7196A WITH ADVANCE TREATMENT US EPA 3060A.	2	n.d.
MERCURY	ppm	ANALYSIS BY ICP-AES WITH ADVANCE TREATMENT US EPA 3052	2	n.d.
LEAD	ppm	ANALYSIS BY ICP-AES WITH ADVANCE TREATMENT US EPA 3050B	2	n.d.
PBBs	%	WITH REFERENCE TO 83/264/EEC, ANALYSIS WAS PERFORMED BY GC/ECDCMS OR HPLC/DAD/MS.	0.0005	n.d.
PBDEs	%	WITH REFERENCE TO 83/264/EEC, ANALYSIS WAS PERFORMED BY GC/ECDCMS OR HPLC/DAD/MS.	0.0005	n.d.

NOTE : n.d. = not detected.

<END>



George Huang
 George Huang / Supervisor
 Sign for and on behalf of
 SGS Taiwan Limited

4.2 Test Report of Ink (TPC410)



Test Report

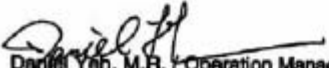
TAI-EE MANUFACTURING CO., LTD.
NO. 8-17, PING-AN ROAD, HOULI TAICHUNG, TAIWAN

Report No. : CE/2005/21944
Date : 2005/02/25
Page : 1 of 3

The following merchandise was (were) submitted and identified by the client as :

Type of Product : TECA-PRINT PAD PRINTING INK
Style/Item No : TPC 410 INK
Sample Received : 2005/02/18
Testing Date : 2005/02/18 TO 2005/02/25

=====
Test Result : - Please see the next page -


Daniel Yeh, M.R. / Operation Manager
Signed for and on behalf of
SGS TAIWAN LTD.



Test Report

TAI-EE MANUFACTURING CO., LTD.
NO. 8-17, PING-AN ROAD, HOULI TAICHUNG, TAIWAN

Report No. : CE/2005/21944
Date : 2005/02/25
Page : 2 of 3

Test Result

PART NAME NO.1 : WHITE INK (PLEASE REFER TO THE PHOTO ATTACHED)

Test Item (s):	Unit	Method	MDL	Result
				No.1
PBBs(Polybrominated biphenyls)(CAS NO:059536-65-1)	%	With reference to USEPA3540C or USEPA3550C. Analysis was performed by HPLC/DAD, LC/MS or GC/MS. (prohibited by 2002/95/EC (RoHS), 83/264/EEC, and 76/769/EEC)	0.0005	N.D.
PBEBs(PBDEs)(Polybrominated biphenyl ethers)	%	With reference to USEPA3540C or USEPA3550C. Analysis was performed by HPLC/DAD, LC/MS or GC/MS. (prohibited by 2002/95/EC (RoHS), 83/264/EEC, and 76/769/EEC)	0.0005	N.D.

Test Item (s):	Unit	Method	MDL	Result
				No.1
Chromium VI (Cr+6)	ppm	As per US EPA 7196A and US EPA 3060A.	2	N.D.
Cadmium (Cd)	ppm	ICP-AES after as per EN 1122, method B:2001 or other acid digestion.	2	N.D.
Mercury (Hg)	ppm	ICP-AES after as per US EPA 3052 or other acid digestion.	2	N.D.
Lead (Pb)	ppm	ICP-AES after as per US EPA 3050B or other acid digestion.	2	N.D.

NOTE: (1) N.D. = Not detected (<MDL)
(2) ppm = mg/kg
(3) MDL = Method Detection Limit

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SGS
Test Report

TAI-EE MANUFACTURING CO., LTD.
NO. 8-17, PING-AN ROAD, HOULI TAICHUNG, TAIWAN

Report No. : CE/2005/21944
Date : 2005/02/25
Page : 3 of 3



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88688-21 270526333 #888-21 27160-11917

4.3 Test Report of Lead frame (Shinko-C7025)



ENVIRONMENTAL MANAGEMENT DIV.

Analysis result report

Report#EE-04-309

Date:Aug 25,2004

SHINKO ELECTRIC INDUSTRIES CO., LTD.

Approval	Design
NOMOTO	NAKAZAWA

Title Quantitative analysis of Cadmium, Lead,Chromium,Mercury,Hexavalent Chromium

1. PURPOSE Confirmation of Cadmium,Lead,Chromium,Mercury,Hexavalent Chromium

2. DETAIL

Product Name	Type
CDA7025+Ag plating	-

3. MEASUREMENT METHOD

1)Pre-conditioning

Measurement Item	Pre-conditioning
Cadmium, Lead,Chromium	A wet decomposition method by sulfuric acid, nitric acid, and hydrogen peroxide (i.e. "plastics-determination of cadmium-wet decomposition method", BS EN 1122:2001)
Hexavalent Chromium	Eluting method
Mercury	Microwave decomposition method

2)Measurement equipment

Measurement Item	Measurement equipment
Cadmium, Lead,Chromium	AAS(Atomic Absorption Spectroscopy) Z-5010
Hexavalent Chromium	UV(Ultraviolet & Visible spectrophotometer)U-2000
Mercury	Vapor Hydride Generation System AAS HG-310

4. MEASUREMENT DATE Jun 23,2004

5. Result of analysis

Cd	N. D. (< 4ppm)
Pb	N. D. (< 10ppm)
T-Cr	N. D. (< 4ppm)
Cr ⁶⁺	N. D. (< 4ppm)
Hg	N. D. (< 5ppm)

Company Certification

Prepared by : MICHIKO NAKAZAWA

Approved by : MASA AKI NOMOTO
Title : ENVIRONMENTAL ENGINEERING DEPT. MANAGER

Signature : M. Nomoto

4.4 Test Report of Silver epoxy (2200S-(PBB+PBDE))



ABLESTIK LABORATORIES
 SUSANA ROAD, RANCHO DOMINGUEZ, CA 90221,
 U. S. A.

Report No. : CE/2004/C1099
 Date : 2004/12/14
 Page : 1 of 2

The following merchandise was (were) submitted and identified by the client as :

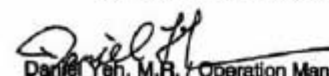
Type of Product : ABLEBOND
Style/Item No : 2200-S
Sample Received : 2004/12/07
Testing Date : 2004/12/07 TO 2004/12/14

Test Result

PART NAME NO.1 : GRAY PASTE(PLEASE REFER TO THE PHOTO ATTACHED)

Test Item (s):	Unit	Method	MDL	Result			
				No. 1			
PBBs(Polybrominated biphenyls)(CAS NO:059536-65-1)	%	With reference to USEPA3540 or USEPA3550. Analysis was performed by HPLC/DAD, LC/MS or GC/MS. (prohibited by 2002/95/EC (RoHS), 83/264/EEC, and 76/769/EEC)	0.0005	N.D.			
PBBEs(PBDEs)(Polybrominated biphenyl ethers)	%	With reference to USEPA3540 or USEPA3550. Analysis was performed by HPLC/DAD, LC/MS or GC/MS. (prohibited by 2002/95/EC (RoHS), 83/264/EEC, and 76/769/EEC)	0.0005	N.D.			

NOTE: (1) N.D. = Not detected (<MDL)
 (2) MDL = Method Detection Limit


 Daniel Yeh, M.R. / Operation Manager
 Signed for and on behalf of
 SGS TAIWAN LTD.

SGS
Test Report

ABLESTIK LABORATORIES
SUSANA ROAD, RANCHO DOMINGUEZ, CA 90221,
U. S. A.

Report No. : CE/2004/C1099
Date : 2004/12/14
Page : 2 of 2



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4.5 Test Report of Silver epoxy (2200S)



Test Report

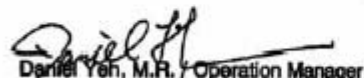
ABLESTIK LABORATORIES
SUSANA ROAD, RANCHO DOMINGUEZ, CA 90221, U.S.A.

Report No. : CE/2005/13498D
Date : 2005/01/26
Page : 1 of 3

The following merchandise was (were) submitted and identified by the client as :

Type of Product : ABLEBOND
Style/Item No : ABLEBOND 2200-S
Sample Received : 2005/01/19
Testing Date : 2005/01/19 TO 2005/01/26

=====
Test Result : - Please see the next page -


Daniel Yeh, M.P., Operation Manager
Signed for and on behalf of
SGS TAIWAN LTD.

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Test Report

ABLESTIK LABORATORIES

SUSANA ROAD, RANCHO DOMINGUEZ, CA 90221, U.S.A.

Report No. : CE/2005/13498D

Date : 2005/01/26

Page : 2 of 3

Test Result

PART NAME NO.1 : GRAY PASTE (PLEASE REFER TO THE PHOTO ATTACHED)

PASS

Test Item (s):	Unit	Method	MDL	Result	Spec.
				No.1	
EN 71 PART 3 Heavy metal content		As per EN 71 PART 3 : 1994 (A1 : 2000) (EN 71 & BS 5665 are identical)			
Soluble Lead (Pb)	ppm	ICP-AES	5	< 5.0	90
Soluble Antimony (Sb)	ppm	ICP-AES	5	< 5.0	60
Soluble Arsenic (As)	ppm	ICP-AES	2.5	< 2.5	25
Soluble Barium (Ba)	ppm	ICP-AES	10	< 10.0	1000
Soluble Cadmium (Cd)	ppm	ICP-AES	5	< 5.0	75
Soluble Chromium (Cr)	ppm	ICP-AES	5	< 5.0	60
Soluble Mercury (Hg)	ppm	ICP-AES	5	< 5.0	60
Soluble Selenium (Se)	ppm	ICP-AES	5	< 5.0	500

Test Item (s):	Unit	Method	MDL	Result	Spec.
				No.1	
Chromium VI (Cr+6)	ppm	As per US EPA 7196A and US EPA 3060A.	2	N.D.	-

NOTE; (1) N.D. = Not detected (<MDL)
 (2) ppm = mg/kg
 (3) MDL = Method Detection Limit
 (4) " - " = No Regulation

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Test Report

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Report No. : CE/2005/13498D
Date : 2005/01/26
Page : 3 of 3



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4.6 Test Report of Solder plating (Sn-Bi)



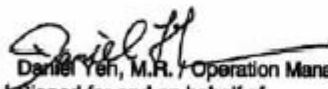
揚博科技股份有限公司
110台北市松德路171號17樓

報告號碼 : CE/2004/63464
日期 : 2004/07/05
頁數 : 1 of 3

以下測試樣品乃供應廠商所提供及確認 :

樣品名稱 : PF-Bi 15
收件日期 : 2004/06/28
測試日期 : 2004/06/28 TO 2004/07/05

=====
測試結果 : - 請見下一頁 -


Daniel Yen, M.R. / Operation Manager
Signed for and on behalf of
SGS TAIWAN LTD.

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揚博科技股份有限公司
110台北市松德路171號17樓

報告號碼：CE/2004/63464
日期：2004/07/05
頁數：2 of 3

測試結果

測試部位 NO.1：透明液體

測試項目：	單位	測試方法	偵測極 限值	結果				
				NO.1				
砷	ppm	依照 US EPA 3052 方法或 其他酸消化方法,用感應藕 合電漿原子發射光譜儀 (ICP-AES)做分析	2	N.D.				
鎳	ppm	依照 US EPA 3050B 方法或 其他酸消化方法,用感應藕 合電漿原子發射光譜儀 (ICP-AES)做分析	2	N.D.				
鎘	ppm	依照 EN1122 方法B:2001或 其他酸消化方法,用感應藕 合電漿原子發射光譜儀 (ICP-AES)做分析	2	N.D.				
鎘	ppm	依照 US EPA 3050B 方法或 其他酸消化方法,用感應藕 合電漿原子發射光譜儀 (ICP-AES)做分析	2	N.D.				
汞	ppm	依照 US EPA 3052 方法或 其他酸消化方法,用感應藕 合電漿原子發射光譜儀 (ICP-AES)做分析	2	N.D.				
鉛	ppm	依照 US EPA 3050B 方法或 其他酸消化方法,用感應藕 合電漿原子發射光譜儀 (ICP-AES)做分析	2	N.D.				
錫	ppm	依照 US EPA 3050B 方法或 其他酸消化方法,用感應藕 合電漿原子發射光譜儀 (ICP-AES)做分析	2	N.D.				

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揚博科技股份有限公司
110台北市松德路171號17樓

報告號碼 : CE/2004/63464
日期 : 2004/07/05
頁數 : 3 of 3

測試項目:	單位	測試方法	偵測極 限值	結果				
				NO. 1				
錳	ppm	依照 US EPA 3052 方法或 其他酸消化方法,用感應藕 合電漿原子發射光譜儀 (ICP-AES)做分析	2	N.D.				

備註 : (1) N.D. = Not detected. (<MDL) / 未檢出(低於偵測極限值)
(2) ppm = µg/kg / 百萬分之一
(3) MDL= Method Detection Limit(偵測極限值)

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