1986

- Discretes
- Analog Switches & Multiplexers
- Amplifiers
- Analog Functions
- Timer/Counter Circuits
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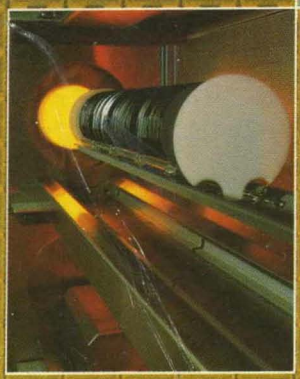

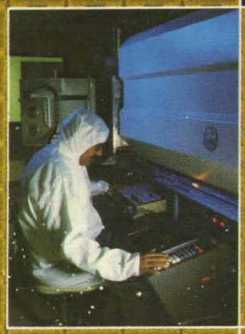

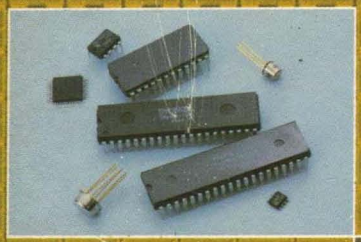

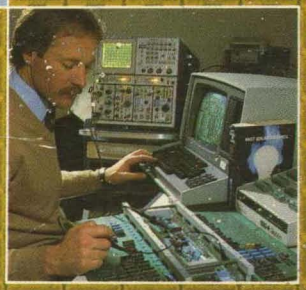

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INTERSIL
10600 Ridgeview Court, Cupertino, CA 95014
408-996-5000
TWX: 910-338-2014

ALPHANUMERIC CROSS REFERENCE

ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
100S	2N5458	2N2606	2N2607	2N3331	2N5270	2N3814	IT132
100U	2N3684	2N2607	2N2607	2N3332	2N5268	2N3815	IT132
102M	2N5686	2N2608	2N2608	2N3333	IT132	2N3816	IT130
102S	2N5457	2N2609	2N2609	2N3334	IT132	2N3816A	IT130A
103M	2N5457	2N2609JAN	2N2609JAN	2N3335	IT132	2N3817	IT130
103S	2N5459	2N2639	IT120	2N3336	IT132	2N3817A	IT130A
104M	2N5458	2N2640	IT122	2N3347	IT137	2N3819	2N5484
105M	2N5459	2N2641	IT122	2N3348	IT138	2N3820	2N2608
105U	2N4340	2N2642	IT120	2N3349	IT139	2N3821	2N3821
106M	2N5485	2N2643	IT122	2N3350	IT137	2N3822	2N3822
107M	2N5485	2N2644	IT122	2N3351	IT138	2N3823	2N3823
110U	2N3685	2N2652	IT120	2N3352	IT139	2N3824	2N3824
120U	2N3686	2N2652A	IT120	2N3365	2N4340	2N3907	IT120
125U	2N4339	2N2720	IT120	2N3366	2N4338	2N3908	IT120
1277A	2N3822	2N2721	IT122	2N3367	2N4338	2N3909	2N2609
1278A	2N3821	2N2722	IT120	2N3368	2N4341	2N3909A	2N2609
1279A	2N3821	2N2802	IT139	2N3369	2N4339	2N3921	2N3921
1280A	2N4224	2N2803	IT139	2N3370	2N4338	2N3922	2N3922
1281A	2N3822	2N2804	IT139	2N3376	2N2608	2N3949	IT132
1282A	2N4341	2N2805	IT139	2N3378	2N2608	2N3950	IT132
1283A	2N4340	2N2806	IT139	2N3380	2N2609	2N3954	2N3954
1284A	2N4222	2N2807	IT139	2N3382	2N3994	2N3954A	2N3954A
1285A	2N3821	2N2841	2N2607	2N3384	2N3993	2N3955	2N3955
1286A	2N4220	2N2842	2N2607	2N3386	2N5114	2N3955A	2N3955A
130U	2N3687	2N2843	2N2607	2N3409	IT122	2N3956	2N3956
1325A	2N4222	2N2844	2N2607	2N3410	IT122	2N3957	2N3957
135U	2N4339	2N2903	IT122	2N3411	IT122	2N3966	2N4416
14T	2N4224	2N2903A	IT120	2N3423	IT122	2N3967	2N4221
155U	2N4416	2N2910	IT122	2N3424	IT122	2N3967A	2N4221
1714A	2N4340	2N2913	IT122	2N3425	IT122	2N3968	2N3685
182S	2N4391	2N2914	IT120	2N3436	2N4341	2N3968A	2N3685
183S	2N3823	2N2915	IT120	2N3437	2N4340	2N3969	2N3686
197S	2N4338	2N2915A	IT120	2N3438	2N4338	2N3969A	2N3686
198S	2N4340	2N2916	IT120	2N3452	2N4220	2N3970	2N3970
199S	2N4341	2N2916A	IT120	2N3453	2N4338	2N3971	2N3971
2000M	2N3823	2N2917	IT122	2N3454	2N4338	2N3972	2N3972
2001M	2N3823	2N2918	IT122	2N3455	2N4340	2N3993	2N3993
200S	2N4392	2N2919	IT120	2N3456	2N4338	2N3993A	2N3993
200U	2N3824	2N2919A	IT120	2N3457	2N4338	2N3994	2N3994
201S	2N4391	2N2920	2N2920	2N3458	2N4341	2N3994A	2N3994
202S	2N4392	2N2920A	2N2920	2N3459	2N4339	2N4009	IT132
203S	2N3821	2N2936	IT120	2N3460	2N4338	2N4010	IT132
204S	2N3821	2N2937	IT120	2N3513	IT122	2N4011	IT132
2078A	2N3955	2N2972	IT122	2N3514	IT122	2N4015	IT139
2079A	2N3955	2N2973	IT122	2N3515	IT122	2N4016	IT137
2080A	2N3955A	2N2974	IT120	2N3516	IT122	2N4017	IT139
2081A	2N3955A	2N2975	IT120	2N3517	IT122	2N4018	IT139
2093M	2N3687	2N2976	IT120	2N3521	IT122	2N4019	IT139
2094M	2N3686	2N2977	IT120	2N3522	IT122	2N4020	IT139
2095M	2N3686	2N2978	IT120	2N3574	2N2607	2N4021	IT139
2098A	2N3954	2N2979	IT120	2N3575	2N2607	2N4022	IT139
2099A	2N3955A	2N2980	IT121	2N3578	2N2608	2N4023	IT137
210U	2N4416	2N2981	IT122	2N3587	IT122	2N4024	IT137
2130U	2N5452	2N2982	IT122	2N3608	3N172	2N4025	IT137
2132U	2N3955	2N3043	IT121	2N3680	IT120	2N4026	3N163
2134U	2N3956	2N3044	IT122	2N3684	2N3684	2N4038	2N4351
2136U	2N3957	2N3045	IT122	2N3684A	2N3684	2N4039	2N4351
2138U	2N3958	2N3046	IT121	2N3685	2N3685	2N4065	3N163
2139U	2N3958	2N3047	IT122	2N3685A	2N3685	2N4066	3N166
2147U	2N3958	2N3048	IT122	2N3686	2N3686	2N4067	3N166
2148U	2N3958	2N3049	IT139	2N3686A	2N3686	2N4082	2N3954
2149U	2N3958	2N3050	IT139	2N3687	2N3687	2N4083	2N3955
231S	2N3954	2N3051	IT139	2N3687A	2N3687	2N4084	2N3954
232S	2N3955	2N3052	IT129	2N3726	IT131	2N4085	2N3955
233S	2N3956	2N3059	IT139	2N3727	IT130	2N4091	2N4091
234S	2N3957	2N3066	2N4340	2N3728	IT122	2N4091A	2N4091
235S	2N3958	2N3067	2N4338	2N3729	IT121	2N4091JAN	2N4091JAN
241U	2N4869	2N3068	2N4338	2N3800	IT132	2N4091JANTX	2N4091JANTX
250U	2N4091	2N3069	2N4341	2N3801	IT132	2N4091JANTXV	2N4091JANTXV
251U	2N4392	2N3070	2N4339	2N3802	IT132	2N4092	2N4092
2N2060	IT120	2N3071	2N4338	2N3803	IT132	2N4092A	2N4092
2N2060A	IT121	2N3084	2N4339	2N3804	IT130	2N4092JAN	2N4092JAN
2N2060B	IT121	2N3085	2N4339	2N3804A	IT130A	2N4092JANTX	2N4092JANTX
2N2223	IT122	2N3086	2N4339	2N3805	IT130	2N4092JANTXV	2N4092JANTXV
2N2223A	IT121	2N3087	2N4339	2N3805A	IT130A	2N4093	2N4093
2N2386	2N2608	2N3088	2N4339	2N3806	IT122	2N4093A	2N4093
2N2386A	2N2608	2N3088A	2N4339	2N3807	IT122	2N4093JAN	2N4093JAN
2N2453	IT122	2N3089	2N4339	2N3808	IT122	2N4093JANTX	2N4093JANTX
2N2453A	IT121	2N3089A	2N4339	2N3809	IT122	2N4093JANTXV	2N4093JANTXV
2N2480	IT122	2N3113	2N2607	2N3810	2N3810	2N4100	2N4100
2N2480A	IT121	2N3277	2N2606	2N3810A	2N3810A	2N4117	2N4117
2N2497	2N2608	2N3278	2N2607	2N3811	2N3811	2N4117A	2N4117A
2N2498	2N2608	2N3328	2N5265	2N3811A	2N3811A	2N4118	2N4118
2N2499	2N2609	2N3329	2N5267	2N3812	IT132	2N4118A	2N4118A
2N2500	2N2608	2N3330	2N5268	2N3813	IT132	2N4119	2N4119

**CONSULT FACTORY

ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
2N4119A	2N4119A	2N5045	2N5453	2N5484	2N5484	2N6484	2N6484
2N4120	3N163	2N5046	2N5454	2N5485	2N5485	2N6485	2N6485
2N4139	2N3822	2N5047	2N5454	2N5486	2N5486	2N6502	IT122
2N4220	2N4220	2N5078	2N5397	2N5515	2N5515	2N6503	IT122
2N4220A	2N4220	2N5090	IT122	2N5516	2N5516	2N6550	2N4868A
2N4221	2N4221	2N5103	2N4416	2N5517	2N5517	2N6568	2N5432
2N4221A	2N4221	2N5104	2N4416	2N5518	2N5518	2SC294	IT122
2N4222	2N4222	2N5105	2N4416	2N5519	2N5519	2SJ11	2N2607
2N4222A	2N4222	2N5114	2N5114	2N5520	2N5520	2SJ12	2N2607
2N4223	2N4223	2N5114JAN	2N5114JAN	2N5521	2N5521	2SJ13	2N5270
2N4224	2N4224	2N5114JANTX	2N5114JANTX	2N5522	2N5522	2SJ15	2N2607
2N4267	3N163	2N5114JANTXV	2N5114JANTXV	2N5523	2N5523	2SJ16	2N2607
2N4268	3N161	2N5115	2N5115	2N5524	2N5524	2SJ47	**
2N4302	2N4302	2N5115JAN	2N5115JAN	2N5545	2N3954	2SJ48	**
2N4303	2N5459	2N5115JANTX	2N5115JANTX	2N5546	2N3955A	2SJ49	**
2N4304	2N5458	2N5115JANTXV	2N5115JANTXV	2N5547	2N3955	2SJ50	**
2N4338	2N4338	2N5116	2N5116	2N5549	2N4093	2SJ78	**
2N4339	2N4339	2N5116JAN	2N5116JAN	2N5555	J310	2SJ79	**
2N4340	2N4340	2N5116JANTX	2N5116JANTX	2N5556	2N3685	2SJ80	**
2N4341	2N4341	2N5116JANTXV	2N5116JANTXV	2N5557	2N3684	2SK11	2N5457
2N4342	2N5461	2N5117	2N5117	2N5558	2N3684	2SK12	2N5457
2N4343	2N5462	2N5118	2N5118	2N5561	U401	2SK13	2N5457
2N4351	2N4351	2N5119	2N5119	2N5562	U402	2SK132	**
2N4352	3N163	2N5120	IT131	2N5563	U404	2SK133	**
2N4353	3N172	2N5121	IT132	2N5564	IT550	2SK134	**
2N4360	2N5460	2N5122	IT132	2N5565	IT550	2SK135	**
2N4381	2N2609	2N5123	IT131	2N5566	IT550	2SK15	2N4868
2N4382	2N5115	2N5124	IT132	2N5592	2N3822	2SK17	2N5484
2N4391	2N4391	2N5125	IT132	2N5593	2N3822	2SK178	**
2N4392	2N4392	2N5158	2N5434	2N5594	2N3822	2SK179	**
2N4393	2N4393	2N5159	2N5433	2N5638	2N5638	2SK18	2N3821
2N4416	2N4416	2N5163	2N3822	2N5639	2N5639	2SK180	**
2N4416A	2N4416A	2N5196	2N5196	2N5640	2N5640	2SK19	ITE4416
2N4417	2N4416	2N5197	2N5197	2N5647	2N4117A	2SK23	2N5459
2N4445	2N5432	2N5198	2N5198	2N5648	2N4117A	2SK30	2N5458
2N4446	2N5434	2N5199	2N5199	2N5649	2N4117A	2SK32	2N3822
2N4447	2N5432	2N5245	ITE4416	2N5653	2N5638	2SK33	2N5397
2N4448	2N5434	2N5246	2N5484	2N5654	2N5639	2SK34	2N3822
2N4856	2N4856	2N5247	2N5486	2N5668	2N5484	2SK37	2N5484
2N4856A	2N4856	2N5248	2N5486	2N5669	2N5485	2SK41	2N5459
2N4856JAN	2N4856JAN	2N5254	IT132	2N5670	2N5486	2SK42	2N3822
2N4856JANTX	2N4856JANTX	2N5255	IT132	2N5793	IT129	2SK43	ITE4092
2N4856JANTXV	2N4856JANTXV	2N5256	IT130	2N5794	IT129	2SK44	ITE4416
2N4857	2N4857	2N5257	2N5457	2N5795	IT139	2SK46	2N5459
2N4857A	2N4857	2N5258	2N5458	2N5796	IT139	2SK48	2N3821
2N4857JAN	2N4857JAN	2N5259	2N5459	2N5797	2N2608	2SK49	2N5484
2N4857JANTX	2N4857JANTX	2N5265	2N2607	2N5798	2N2608	2SK50	ITE4416
2N4857JANTXV	2N4857JANTXV	2N5266	2N2607	2N5799	2N2608	2SK54	2N3822
2N4858	2N4858	2N5267	2N2608	2N5800	2N2608	2SK55	2N3822
2N4858A	2N4858	2N5268	2N2608	2N5801	2N4393	2SK56	2N5459
2N4858JAN	2N4858JAN	2N5269	2N2609	2N5802	2N4393	2SK61	2N5397
2N4858JANTX	2N4858JANTX	2N5270	2N2609	2N5803	2N4392	2SK65	J201
2N4858JANTXV	2N4858JANTXV	2N5277	2N4341	2N5843	IT130	2SK66	2N3821
2N4859	2N4859	2N5278	2N4341	2N5844	IT130	2SK68	2N3822
2N4859A	2N4859	2N5358	2N4220	2N5902	2N5902	2SK72	2N5196
2N4859JAN	2N4856JAN	2N5359	2N4220	2N5903	2N5903	3GS	2N3821
2N4859JANTX	2N4856JANTX	2N5360	2N4221	2N5904	2N5904	3N145	3N163
2N4860	2N4860	2N5361	2N4221	2N5905	2N5905	3N146	3N163
2N4860A	2N4860	2N5362	2N4222	2N5906	2N5906	3N147	3N189
2N4860JAN	2N4857JAN	2N5363	2N4222	2N5907	2N5907	3N148	3N189
2N4860JANTX	2N4857JANTX	2N5364	2N4222	2N5908	2N5908	3N149	3N161
2N4861	2N4861	2N5391	2N4867A	2N5909	2N5909	3N150	3N163
2N4861A	2N4861	2N5392	2N4868A	2N5911	2N5911	3N151	3N190
2N4861JAN	2N4858JAN	2N5393	2N4869A	2N5912	2N5912	3N155	3N163
2N4861JANTX	2N4858JANTX	2N5394	2N4869A	2N5949	2N5486	3N155A	3N163
2N4867	2N4867	2N5395	2N4869A	2N5950	2N5486	3N156	3N163
2N4867A	2N4867A	2N5396	2N4869A	2N5951	2N5486	3N156A	3N163
2N4868	2N4868	2N5397	2N5397	2N5952	2N5484	3N157	3N163
2N4868A	2N4868A	2N5398	2N5398	2N5953	2N5484	3N157A	3N163
2N4869	2N4869	2N5432	2N5432	2N6085	IT122	3N158	3N163
2N4869A	2N4869A	2N5433	2N5433	2N6086	IT122	3N158A	3N163
2N4878	2N4878	2N5434	2N5434	2N6087	IT121	3N160	3N161
2N4879	2N4879	2N5452	2N5452	2N6088	IT121	3N161	3N161
2N4880	2N4880	2N5453	2N5453	2N6089	IT122	3N163	3N163
2N4937	IT131	2N5454	2N5454	2N6090	IT121	3N164	3N164
2N4938	IT132	2N5457	2N5457	2N6091	IT121	3N165	3N165
2N4939	IT132	2N5458	2N5458	2N6092	IT121	3N166	3N166
2N4940	IT132	2N5459	2N5459	2N6441	IT122	3N167	3N161
2N4941	IT131	2N5460	2N5460	2N6442	IT122	3N168	3N161
2N4942	IT132	2N5461	2N5461	2N6443	IT122	3N169	3N170
2N4955	IT122	2N5462	2N5462	2N6444	IT122	3N170	3N170
2N4956	IT122	2N5463	2N5463	2N6445	IT121	3N171	3N171
2N4977	2N5433	2N5464	2N5464	2N6446	IT121	3N172	3N172
2N4978	2N5433	2N5465	2N5465	2N6447	IT121	3N173	3N173
2N4979	2N4859	2N5471	2N5265	2N6448	IT121	3N174	3N163
2N5018	2N5018	2N5472	2N5265	2N6451	U310	3N175	3N170
2N5019	2N5019	2N5473	2N5265	2N6452	U310	3N176	3N170
2N5020	2N2843	2N5474	2N5265	2N6453	U310	3N177	3N171
2N5021	2N2607	2N5475	2N5265	2N6454	U310	3N178	3N172
2N5033	2N5460	2N5476	2N5266	2N6483	2N6483	3N179	3N172

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ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
3N180	3N172	AD7520KD	AD7520KD	AH0139D/883	DG139AK/883B	BF801	2N4867
3N181	3N161	AD7520KN	AD7520KN	AH0140CD	DG140BK	BF802	2N4338
3N182	3N161	AD7520LD	AD7520LD	AH0140D	DG140AK	BF804	2N4338
3N183	3N161	AD7520LN	AD7520LN	AH0140D/883	DG140AK/883B	BF805	2N4869
3N188	3N188	AD7520SD	AD7520SD	AH0141CD	DG141BK	BF806	2N4869
3N189	3N189	AD7520TD	AD7520TD	AH0141D	DG141AK	BF808	2N4868
3N190	3N190	AD7520UD	AD7520UD	AH0141D/883	DG141AK/883B	BF810	2N4858
3N191	3N191	AD7521JD	AD7521JD	AH0142CD	DG142BK	BF811	2N4858
3N207	3N190	AD7521JN	AD7521JN	AH0142D	DG142AK	BF815	2N4858
3N208	3N188	AD7521KD	AD7521KD	AH0142D/883	DG142AK/883B	BF816	2N4858
3SK22	2N5486	AD7521KN	AD7521KN	AH0143CD	DG143BK	BF817	2N4858
3SK23	2N5397	AD7521LD	AD7521LD	AH0143D	DG143AK	BF818	2N4858
3SK28	2N5397	AD7521LN	AD7521LN	AH0143D/883	DG143AK/883B	BFQ10	U401
42T	2N4392	AD7521SD	AD7521SD	AH0144CD	DG144BK	BFQ11	U401
4360TP	2N5462	AD7521TD	AD7521TD	AH0144D	DG144AK	BFQ12	U402
5033TP	2N5460	AD7521UD	AD7521UD	AH0144D/883	DG144AK/883B	BFQ13	U403
588U	2N4416	AD7523AD	AD7523AD	AH0145CD	DG145BK	BFQ14	U404
58T	2N5457	AD7523BD	AD7523BD	AH0145D	DG145AK	BFQ15	U405
59T	2N4416	AD7523CD	AD7523CD	AH0145D/883	DG145AK/883B	BFQ16	U406
703U	2N4220	AD7523JN	AD7523JN	AH0146CD	DG145BK	BFQ23	IT5912
704U	2N4220	AD7523KN	AD7523KN	AH0146D	DG146AK	BFQ26	U403
705U	2N4224	AD7523LN	AD7523LN	AH0146D/883	DG146AK/883B	BFQ44	IT5912
707U	2N4860	AD7523SD	AD7523SD	AH0151CD	DG151BK	BFQ45	IT5912
714U	2N3822	AD7523TD	AD7523TD	AH0151D/883	DG151AK/883B	BFQ49A	2N3055
734EU	2N4416	AD7523UD	AD7523UD	AH0152CD	DG152BK	BFQ49B	2N3958
734U	2N5516	AD7530JD	AD7530JD	AH0152D	DG152AK	BFQ49C	2N3958
751U	2N4340	AD7530JN	AD7530JN	AH0152D/883	DG152AK/883B	BFS21	2N5199
752U	2N4340	AD7530KD	AD7530KD	AH0153CD	DG153BK	BFS21A	2N5199
753U	2N4341	AD7530KN	AD7530KN	AH0153D	DG153AK	BFS67	2N3821
754U	2N4340	AD7530LD	AD7530LD	AH0153D/883	DG153AK/883B	BFS67P	2N5459
755U	2N4341	AD7530LN	AD7530LN	AH0154CD	DG154BK	BFS68	2N3823
756U	2N4340	AD7531JD	AD7531JD	AH0154D	DG154AK	BFS68P	2N4416
A190	ITE4416	AD7531JN	AD7531JN	AH0154D/883	DG143AK/883B	BFS70	2N3821
A191	ITE4416	AD7531KD	AD7531KD	AH0155D	DG151AK	BFS71	2N3822
A192	2N4416	AD7531KN	AD7531KN	AH0161CD	DG161BK	BFS72	2N3823
A193	2N5484	AD7531LD	AD7531LD	AH0161D	DG161AK	BFS73	2N3821
A194	2N5484	AD7531LN	AD7531LN	AH0161D/883	DG161AK/883B	BFS74	2N4856
A195	2N5484	AD7533AD	AD7533AD	AH0162CD	DG162BK	BFS75	2N4857
A196	ITE4416	AD7533BD	AD7533BD	AH0162D	DG162AK	BFS76	2N4858
A197	ITE4391	AD7533CD	AD7533CD	AH0162D/883B	DG162AK/883B	BFS77	2N4859
A198	ITE4392	AD7533JN	AD7533JN	AH0163CD	DG163BK	BFS78	2N4860
A199	ITE4393	AD7533KN	AD7533KN	AH0163D	DG163AK	BFS79	2N4861
A5T3821	2N5484	AD7533LN	AD7533LN	AH0163D/883	DG163AK/883B	BFS80	2N4416A
A5T3822	2N5484	AD7533SD	AD7533SD	AH0164CD	DG164BK	BFT10	2N5397
A5T3823	2N4416	AD7533TD	AD7533TD	AH0164D	DG164AK	BFT11	2N5019
A5T3824	2N4341	AD7533UD	AD7533UD	AH0164D/883	DG164AK/883B	BFW10	2N3823
A5T5460	2N5460	AD7541AD	AD7541AD	AH5009CN	IH5009CPD	BFW11	2N3822
A5T5461	2N5461	AD7541BD	AD7541BD	AH5010CN	IH5010CPD	BFW12	2N4416
A5T5462	2N5462	AD7541JN	AD7541JN	AH5012CN	IH5012CPE	BFW13	2N4867
AD108	LM108	AD7541KN	AD7541KN	AH5013CN	IH5013CPD	BFW39	IT129
AD308	LM308	AD7541SD	AD7541SD	AH5014CN	IH5014CPD	BFW39A	IT120
AD3954	2N3954	AD7541TD	AD7541TD	AH5015CN	IH5015CPE	BFW54	2N3822
AD3954A	2N3954A	AD810	2N4878	AH5016CN	IH5016CPE	BFW55	2N3822
AD3955	2N3955	AD811	2N4878	AM5011CN	IH5011CPE	BFW56	2N4860
AD3956	2N3956	AD812	2N4878	BC264	2N5458	BFW61	2N4224
AD3958	2N3958	AD813	2N4878	BC264A	2N5457	BFX11	IT132
AD503	AD503	AD814	IT124	BC264B	2N5458	BFX15	IT122
AD589	ICL8069	AD815	IT124	BC264C	2N5458	BFX36	IT131
AD590	AD590	AD816	IT120A	BC264D	2N4416	BFX70	IT122
AD5905	2N5905	AD818	IT140	BCY87	IT121	BFX71	IT122
AD5906	2N5906	AD820	IT132	BCY88	IT122	BFX72	IT122
AD5907	2N5907	AD821	IT130A	BCY89	IT122	BFX78	2N5397
AD5908	2N5908	AD822	IT130A	BF244	2N5486	BFX82	2N5019
AD5909	2N5909	AD830	2N5520	BF244A	2N5484	BFX83	2N5019
AD7506/COM/CHIPS	IH6116C/D	AD831	2N5521	BF244B	2N5485	BFX99	IT120A
AD7506/MIL/CHIPS	IH6116M/D	AD832	2N5522	BF244C	2N5486	BFY20	IT122
AD7506JD	IH6116CJI	AD833	2N5523	BF245	2N5486	BFY81	IT122
AD7506JD/883B	IH6116CJI/883B	AD833A	2N5524	BF245A	2N4416	BFY82	IT122
AD7506JN	IH6116CPI	AD835	2N3954	BF245B	2N4416	BFY83	IT122
AD7506KD	IH6116CJI	AD836	2N3955	BF245C	2N4416	BFY84	IT122
AD7506KD/883B	IH6116CJI/883B	AD837	2N3955	BF246	2N5485	BFY85	IT122
AD7506KN	IH6116CPI	AD838	2N3956	BF246A	2N5639	BFY86	IT122
AD7506SD	IH6116MJI	AD839	2N3957	BF246B	2N5638	BFY91	IT122
AD7506SD/883B	IH6116MJI/883B	AD840	2N5520	BF246C	2N5638	BFY92	IT122
AD7506TD	IH6116MJI	AD841	2N5521	BF247	2N4091	BN209	IT122
AD7506TD/883B	IH6116MJI/883B	AD842	2N5523	BF247A	2N4091	BSV22	2N4416
AD7507/COM/CHIPS	IH6216C/D	AH0126CD	DG126BK	BF247B	2N4091	BSV78	2N4856A
AD7507/MIL/CHIPS	IH6216M/D	AH0126D	DG126AK	BF247C	2N4091	BSV79	2N4857A
AD7507JD	IH6216CJI	AH0126D/883	DG126AK/883B	BF256	2N5484	BSV80	2N4858A
AD7507JD/883B	IH6216CJI/883B	AH0129CD	DG129BK	BF256A	2N5484	BSX82	2N3822
AD7507JN	IH6216CPI	AH0129D	DG129AK	BF256B	2N4416	C21	2N3821
AD7507KD	IH6216CJI	AH0129D/883	DG129AK/883B	BF256C	2N4416	C2306	2N5196
AD7507KD/883B	IH6216CJI/883B	AH0133CD	DG133BK	BF320	2N5461	C38	2N4338
AD7507KN	IH6216CPI	AH0133D	DG133AK	BF320A	2N5460	C413N	2N5434
AD7507SD	IH6216M/D	AH0133D/883	DG133AK/883B	BF320B	2N5461	C610	2N4392
AD7507SD/883B	IH6216MJI/883B	AH0134CD	DG134BK	BF320C	2N5462	C611	2N4221
AD7507TD	IH6216MJI	AH0134D	DG134AK	BF346	ITE4392	C612	2N4221
AD7507TD/883B	IH6216MJI/883B	AH0134D/883	DG134AK/883B	BF347	J201	C613	2N4221
AD7520JD	AD7520JD	AH0139CD	DG139BK	BF348	J310	C614	2N4220
AD7520JN	AD7520JN	AH0139D	DG139AK	BF800	2N4867	C615	2N4221

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ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
C620	2N4220	D1202	2N3821	DG151BP	DG151BK	DG188BP	DG188BK
C621	2N4220	D1203	2N4220	DG152AL	DG152AL	DG189AL	DG189AL
C622	2N4220	D123AL	D123AL	DG152AP	DG152AK	DG189AP	DG189AK
C623	2N4220	D123AP	D123AK	DG152BP	DG152BK	DG189BP	DG189BK
C624	2N4220	D123BP	D123BK	DG153AL	DG153AL	DG190AL	DGM190AL
C625	2N4220	D123BP	D123BJ	DG153AP	DG153AK	DG190AL	DG190AL
C650	2N4220	D125AL	D125AL	DG153BP	DG153BK	DG190AP	DGM190AK
C651	2N4220	D125AP	D125AP	DG154AL	DG154AL	DG190AP	DG190AK
C652	2N4220	D125BP	D125BK	DG154AP	DG154AK	DG190BP	DGM190CJ
C653	2N4220	D129AL	D129AL	DG154BP	DG154BK	DG190BP	DGM190BK
C6690	2N4341	D129AP	D129AK	DG161AL	DG161AL	DG190BP	DG190BK
C6691	2N4341	D129BP	D129BK	DG161AP	DG161AK	DG191AL	DGM191AL
C6692	2N4339	D1301	2N4222	DG161BP	DG161BK	DG191AL	DG191AL
C673	2N4341	D1302	2N4220	DG162AL	DG162AL	DG191AP	DGM191AK
C674	2N4341	D1303	2N4220	DG162AP	DG162AK	DG191AP	DG191AK
C680	2N4338	D1420	2N4868	DG162BP	DG162BK	DG191BP	DGM191CJ
C680A	2N4338	D1421	2N3822	DG163AL	DG163AL	DG191BP	DGM191BK
C681	2N4338	D1422	2N4869	DG163AP	DG163AK	DG191BP	DG191BK
C681A	2N4338	D2T2218	IT129	DG163BP	DG163BK	DG200AA	DG200AA
C682	2N4339	D2T2218A	IT129	DG164AL	DG164AL	DG200AK	DG200AK
C682A	2N4339	D2T2219	IT129	DG164AP	DG164AK	DG200AL	DG200AL
C683	2N4339	D2T2219A	IT129	DG164BP	DG164BK	DG200AP	DG200AK
C683A	2N4339	D2T2904	IT139	DG180AA	DG180AA	DG200BA	DG200BA
C684	2N4220	D2T2904A	IT139	DG180AL	DG180AL	DG200BK	DG200BK
C684A	2N4220	D2T2905	IT139	DG180AP	DG180AK	DG200BP	DG200BK
C685	2N4220	D2T2905A	IT139	DG180BA	DG180BA	DG200CJ	DG200CJ
C685A	2N4220	D2T918	IT129	DG180BP	DG180BK	DG201AK	DG201AK
C80	2N4338	DA102	2N5196	DG181AA	DGM181AA	DG201AP	DG201AK
C81	2N4338	DA402	2N5196	DG181AA	DG181AA	DG201BK	DG201BK
C84	2N4338	DAC1020LCD	AD7520LD	DG181AL	DGM181AL	DG201CJ	DG201CJ
C85	2N4338	DAC1020LD	AD7520UD	DG181AL	DG181AL	DG210BP	DG201BK
C91	2N4858	DAC1021LCD	AD7520KD	DG181AP	DGM181AK	DG281AA	IH182MTW
C92	2N4091	DAC1021LD	AD7520TD	DG181AP	DG181AK	DG281AP	IH182MJD
C93	2N4393	DAC1022LCD	AD7520JD	DG181BA	DGM181BA	DG281BA	IH182CTW
C94	2N5457	DAC1022LD	AD7520SD	DG181BA	DG181BA	DG281BP	IH182CJD
C94E	2N5457	DAC1218LCD	AD7541BD	DG181BP	DGM181CJ	DG284AP	IH185MJE
C95	2N5457	DAC1218LCN	AD7541LN	DG181BP	DGM181BK	DG284BP	IH185CJE
C95E	2N5459	DAC1218LCN	AD7541KN	DG181BP	DG181BK	DG287AA	IH188MTW
C96E	2N5484	DAC1219LCD	AD7541AD	DG182AA	DGM182AA	DG287AP	IH188MJD
C97E	2N3822	DAC1219LCN	AD7541JN	DG182AA	DG182AA	DG287BA	IH188CTW
C98E	2N3822	DAC1220LCD	AD7521LD	DG182AL	DGM182AL	DG287BP	IH188CJD
CA308	LM308	DAC1220LD	AD7521UD	DG182AL	DG182AL	DG290AP	IH191MJE
CC4445	2N5432	DAC1221LCD	AD7521KD	DG182AP	DGM182AK	DG290BP	IH191CJE
CC4446	2N5434	DAC1221LD	AD7521TD	DG182AP	DG182AK	DG381AA	DGM182AA
CC697	2N4856	DAC1222LCD	AD7521JD	DG182BA	DGM182BA	DG381AK	DGM182AK
CD22001H	ICM1424C	DAC1222LD	AD7521SD	DG182BA	DG182BA	DG381AP	DGM182AK
CD22015E	ICM7051A	DG123AL	DG123AL	DG182BP	DGM182CJ	DG381BA	DGM181BA
CF2386	2N5458	DG123AP	DG123AK	DG182BP	DGM182BK	DG381BK	DGM181BK
CF24	2N3824	DG123BP	DG123BK	DG182BP	DG182BK	DG381BP	DGM181BK
CFM13026	2N4858	DG125AL	DG125AL	DG183AL	DG183AL	DG381CJ	DGM181CJ
CM600	2N4092	DG125AP	DG125AK	DG183AP	DG183AK	DG384AK	DGM185AK
CM601	2N4091	DG125BP	DG125BK	DG183BP	DG183BK	DG384AP	DGM185AK
CM602	2N4091	DG126AK	DG126AK	DG184AL	DGM184AL	DG384BK	DGM184BK
CM603	2N4091	DG126AL	DG126AL	DG184AL	DG184AL	DG384BP	DGM184BK
CM640	2N4093	DG126BP	DG126BK	DG184AP	DGM184AK	DG384CJ	DGM184CJ
CM641	2N4093	DG129AL	DG129AL	DG184AP	DG184AK	DG387AA	DGM188AA
CM642	2N4093	DG129AP	DG129AK	DG184BP	DGM184CJ	DG387AK	DGM188AK
CM643	2N4092	DG129BP	DG129BK	DG184BP	DGM184BK	DG387AP	DGM188AK
CM644	2N4092	DG133AL	DG133AL	DG184BP	DG184BK	DG387BA	DGM187BA
CM645	2N4092	DG133AP	DG133AK	DG185AL	DGM185AL	DG387BK	DGM187BK
CM646	2N4092	DG133BP	DG133BK	DG185AL	DG185AL	DG387BP	DGM187BK
CM647	2N4091	DG134AL	DG134AL	DG185AP	DGM185AK	DG390AK	DGM191AK
CM650	2N5432	DG134AP	DG134AK	DG185AP	DG185AK	DG390AP	DGM191AK
CM651	2N5433	DG134BP	DG134BK	DG185BP	DGM185CJ	DG390BK	DGM190BK
CM652	2N5432	DG139AL	DG139AL	DG185BP	DGM185BK	DG390BP	DGM190BK
CM653	2N5433	DG139AP	DG139AK	DG185BP	DG185BK	DG390CJ	DGM190CJ
CM697	2N5433	DG139BP	DG139BK	DG186AA	DG186AA	DG503	AD503
CM800	2N5433	DG140AL	DG140AL	DG186AL	DG186AL	DG5040AK	IH5040MJE
CM856	2N5433	DG140AP	DG140AK	DG186AP	DG186AK	DG5040AL	IH5040MFD
CM860	2N4868A	DG140BP	DG140BK	DG186BA	DG186BA	DG5040CJ	IH5040CPE
CMX740	2N5432	DG141AL	DG141AL	DG186BP	DG186BK	DG5040CK	IH5040CJE
CP640	2N4091	DG141AP	DG141AK	DG187AA	DGM187AA	DG5041AA	IH5041MTW
CP643	2N5434	DG141BP	DG141BK	DG187AA	DG187AA	DG5041AK	IH5041MJE
CP650	2N5432	DG142AL	DG142AL	DG187AL	DGM187AL	DG5041AL	IH5041MFD
CP651	2N5433	DG142AP	DG142AK	DG187AL	DG187AL	DG5041CJ	IH5041CPE
CP652	2N5433	DG142BP	DG142BK	DG187AP	DGM187AK	DG5041CK	IH5041CJE
CP653	2N5433	DG143AL	DG143AL	DG187AP	DG187AK	DG5042AA	IH5042MTW
D1101	2N3821	DG143AP	DG143AK	DG187BA	DGM187BA	DG5042AK	IH5042MJE
D1102	2N3821	DG143BP	DG143BK	DG187BA	DG187BA	DG5042AL	IH5042MFD
D1103	2N4338	DG144AL	DG144AL	DG187BP	DGM187BK	DG5042CJ	IH5042CPE
D1177	2N3821	DG144AP	DG144AK	DG187BP	DG187BK	DG5042CK	IH5042CJE
D1178	2N3821	DG144BP	DG144BK	DG188AA	DGM188AA	DG5043AK	IH5043MJE
D1179	2N4338	DG145AL	DG145AL	DG188AA	DG188AA	DG5043AL	IH5043MFD
D1180	2N3822	DG145AP	DG145AK	DG188AL	DGM188AL	DG5043CJ	IH5043CPE
D1181	2N4338	DG145BP	DG145BK	DG188AL	DG188AL	DG5043CK	IH5043CJE
D1182	2N4338	DG146AL	DG146AL	DG188AP	DGM188BK	DG5044AA	IH5044MTW
D1183	2N4341	DG146AP	DG146AK	DG188AP	DGM188AK	DG5044AK	IH5044MJE
D1184	2N4340	DG146BP	DG146BK	DG188AP	DG188AK	DG5044AL	IH5044MFD
D1185	2N4339	DG151AL	DG151AL	DG188BA	DGM188BA	DG5044CJ	IH5044CPE
D1201	2N4224	DG151AP	DG151AK	DG188BA	DG188BA	DG5044CK	IH5044CJE

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ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
DG5045AK	IH5045MJE	E211	2N5397	FM1111	2N3957	HI1-0200-8	DG200AK/883B
DG5045AL	IH5045MFD	E212	2N5397	FM1111A	2N5909	HI1-0201-2	DG201AK
DG5045CJ	IH5045CPE	E230	2N4867	FM1112	2N5196	HI1-0201-4	DG201BK
DG5045CK	IH5045CJE	E231	2N4868	FM1200	2N3954	HI1-0201-5	DG201BK
DG506AR	IH6116MJI	E232	2N4869	FM1201	2N3954	HI1-0201-8	DG201AK/883B
DG506BR	IH6116CJI	E270	J270	FM1202	2N3954	HI1-0381-2	DGM182AK
DG506CJ	IH6116CPI	E271	J271	FM1203	2N3955A	HI1-0381-5	DGM181BK
DG507AR	IH6216MJI	E300	2N5397	FM1204	2N3955	HI1-0381-8	DGM182AK/883B
DG507BR	IH6216CJI	E304	2N5486	FM1205	2N3954	HI1-0384-2	DGM185AK
DG507CJ	IH6216CPI	E305	2N5484	FM1206	2N3954	HI1-0384-5	DGM184BK
DG508AP	IH6108MJE	E308	J308	FM1207	2N3954	HI1-0384-8	DGM185AK/883B
DG508BP	IH6108CJE	E309	J309	FM1208	2N3955A	HI1-0387-2	DGM188AK
DG508CJ	IH6108CPE	E310	J310	FM1209	2N3955	HI1-0387-5	DGM187BK
DG509AP	IH5208MJE	E311	J310	FM1210	2N3955A	HI1-0387-8	DGM188AK/883B
DG509BP	IH6208CJE	E312	2N5397	FM1211	IT5911	HI1-0390-2	DGM191AK
DG509CJ	IH6208CPE	E400	2N3955	FM3954	2N3954	HI1-0390-5	DGM190BK
DGM111AL	DG111AL	E401	2N3955	FM3954A	2N3954A	HI1-0390-8	DGM191AK/883B
DGM111AP	DG111AK	E402	2N3957	FM3955	2N3955	HI1-0506-2	IH6116MJI
DGM111BP	DG111BK	E410	2N3955	FM3955A	2N3955A	HI1-0506-5	IH6116CJI
DN3066A	2N3821	E411	IT5911	FM3956	2N3956	HI1-0506-8	IH6116MJI/883B
DN3067A	2N4338	E412	IT5911	FM3957	2N3957	HI1-0506A-2	IH5116MJI
DN3068A	2N4338	E413	2N5454	FM3958	IT5911	HI1-0506A-5	IH5116IJI
DN3069A	2N3822	E414	2N3956	FP4339	2N4339	HI1-0506A-8	IH5116MJI/883B
DN3070A	2N3821	E415	2N3957	FP4340	2N4340	HI1-0507-2	IH6216MJI
DN3071A	2N4338	E420	IT5911	FT0654A	2N5486	HI1-0507-5	IH6216CJI
DN3365A	2N4220	E421	IT5912	FT0654B	2N5486	HI1-0507-8	IH6216MJI/883B
DN3365B	2N4091	E430	J309(X2)	FT0654C	2N4221	HI1-0507A-2	IH5216MJI
DN3366A	2N3686	E431	J310(X2)	FT0654D	2N4221	HI1-0507A-5	IH5216IJI
DN3366B	2N4091	ESM25	U401	FT3820	2N5460	HI1-0507A-8	IH5216MJI/883B
DN3367A	2N3687	ESM25A	U401	FT3820	2N5019	HI1-0508-2	IH6108MJE
DN3367B	2N4091	ESM4091	2N4091	FT3909	2N5019	HI1-0508-5	IH6108CJE
DN3368A	2N4341	ESM4092	2N4092	FT703	3N161	HI1-0508-8	IH6108MJE/883B
DN3368B	2N4221	ESM4093	2N4093	FT704	3N163	HI1-0508A-2	IH5108MJE
DN3369A	2N4339	ESM4302	2N5457	G115AP	G115AK	HI1-0508A-5	IH5108IJE
DN3369B	2N4220	ESM4303	2N5459	G115BP	G115BK	HI1-0508A-8	IH5108MJE/883B
DN3370A	2N4338	ESM4304	2N5458	G115BP	G115BJ	HI1-0509-2	IH6208MJE
DN3370B	2N4338	ESM4445	2N5432	G116AL	G116AL	HI1-0509-5	IH6208CJE
DN3436A	2N4341	ESM4446	2N5434	G116AP	G116AK	HI1-0509-8	IH6208MJE/883B
DN3436B	2N4222	ESM4447	2N5432	G116BP	G116BK	HI1-0509A-2	IH5208MJE
DN3437A	2N4340	ESM4448	2N5434	G116BP	G116BJ	HI1-0509A-5	IH5208IJE
DN3437B	2N4220	FE0654A	2N4386	G117AL	G117AL	HI1-0509A-8	IH5208MJE/883B
DN3438A	2N4338	FE0654B	2N5485	G118AL	G118AL	HI1-5040-2	IH5040MJE
DN3438B	2N4339	FE100	2N3821	G118AP	G118AK	HI1-5040-5	IH5040CJE
DN3458A	2N4341	FE100A	2N3821	G119AL	G119AL	HI1-5040-8	IH5040MJE/883B
DN3458B	2N4222	FE102	2N4119	G123AL	G123AL	HI1-5041-2	IH5041MJE
DN3459A	2N4339	FE102A	2N4119	G123AP	G123AK	HI1-5041-5	IH5041CJE
DN3459B	2N4220	FE104	2N4118	GET5457	2N5457	HI1-5041-8	IH5041MJE/883B
DN3460A	2N4338	FE104A	2N4118	GET5458	2N5458	HI1-5042-2	IH5042MJE
DN3460B	2N4220	FE1600	2N4092	GET5459	2N5459	HI1-5042-5	IH5042CJE
DNX1	2N4338	FE200	2N3821	HA2720	ICL8021	HI1-5042-8	IH5142MJE/883B
DNX2	2N4338	FE202	2N3821	HA7807	IT132	HI1-5043-2	IH5143MJE
DNX3	2N4338	FE204	2N3821	HA7809	IT132	HI1-5043-5	IH5143CJE
DNX4	2N4869	FE300	2N3822	HD43871	ICM7050H	HI1-5043-8	IH5143MJE/883B
DNX5	2N4868	FE302	2N3821	HD43871	ICM7050G	HI1-5044-2	IH5144MJE
DNX6	2N4338	FE304	2N3821	HDIG1030	3N163	HI1-5044-5	IH5144CJE
DNX7	2N4416	FE3819	2N5484	HEP801	2N3822	HI1-5044-8	IH5144MJE/883B
DNX8	2N4416	FE4302	2N5457	HEP802	2N5484	HI1-5045-2	IH5145MJE
DNX9	2N4339	FE4303	2N5459	HEP803	2N5019	HI1-5045-5	IH5145CJE
DS0026	ICL7667	FE4304	2N5458	HEPF0021	2N5484	HI1-5045-8	IH5145MJE/883B
DU4339	2N5397	FE5245	2N4416	HEPF1035	J176	HI1-5046-2	IH5046MJE
DU4340	2N5398	FE5246	2N5484	HEPF2004	2N5484	HI1-5046-5	IH5046CJE
E100	2N5458	FE5247	2N5486	HEPF2005	2N5459	HI1-5046-8	IH5046MJE/883B
E101	J204	FE5457	2N5457	HI0-0201-6	DG201C/D	HI1-5047-2	IH5047MJE
E102	2N5457	FE5458	2N5458	HI0-0381-6	DGM181C/D	HI1-5047-5	IH5047CJE
E103	2N5459	FE5459	2N5459	HI0-0384-6	DGM184C/D	HI1-5047-8	IH5047MJE/883B
E105	J105	FE5484	2N5484	HI0-0387-6	DGM187C/D	HI1-5049-2	IH5149MJE
E106	J106	FE5485	2N5485	HI0-0390-6	DGM190C/D	HI1-5049-5	IH5149CJE
E107	J107	FE5486	2N5486	HI0-0506-6	IH6116C/D	HI1-5049-8	IH5149MJE/883B
E108	J105	FF400	2N5457	HI0-0506A-6	IH5116C/D	HI1-5050-2	IH5150MJE
E109	J106	FM1100	2N3954A	HI0-0507-6	IH6216C/D	HI1-5050-5	IH5150CJE
E110	J107	FM1100A	2N5906	HI0-0507A-6	IH5216C/D	HI1-5050-8	IH5150MJE/883B
E111	J111	FM1101A	2N5906	HI0-0508-6	IH6108C/D	HI1-5051-2	IH5151MJE
E1115	ICM1115A	FM1102	2N3954	HI0-0508A-6	IH5108C/D	HI1-5051-5	IH5151CJE
E111A	J111	FM1102A	2N5906	HI0-0509-6	IH6208C/D	HI1-5051-8	IH5151MJE/883B
E112	J112	FM1103	2N3955	HI0-0509A-6	IH5208C/D	HI2-0200-2	DG200AA
E112A	J112	FM1103A	2N5908	HI0-5040-6	IH5140C/D	HI2-0200-4	DG200BA
E113	J113	FM1104	2N3957	HI0-5041-6	IH5141C/D	HI2-0200-5	DG200BA
E113A	J113	FM1104A	2N5909	HI0-5042-6	IH5142C/D	HI2-0200-8	DG200AA/883B
E114	J204	FM1105	2N3954A	HI0-5043-6	IH5143C/D	HI2-0381-2	DGM182AA
E1151	ICM1115B	FM1105A	IT500	HI0-5044-6	IH5144C/D	HI2-0381-5	DGM181BA
E1426	ICM7050U	FM1106	2N3954A	HI0-5045-6	IH5145C/D	HI2-0381-8	DGM181AA/883B
E174	J174	FM1106A	IT500	HI0-5046-6	IH5046C/D	HI2-0387-2	DGM188AA
E175	J175	FM1107	2N3954	HI0-5047-6	IH5047C/D	HI2-0387-5	DGM187BA
E176	J176	FM1107A	IT500	HI0-5049-6	IH5149C/D	HI2-0387-8	DGM188AA/883B
E177	J177	FM1108	2N3955	HI0-5050-6	IH5150C/D	HI3-0200-5	DG200CJ
E201	J201	FM1108A	IT502	HI0-5051-6	IH5051C/D	HI3-0201-5	DG201CJ
E202	J202	FM1109	2N3957	HI1-0200-2	DG200AK	HI3-0381-5	DGM181CJ
E203	J203	FM1109A	IT503	HI1-0200-4	DG200BK	HI3-0384-5	DGM184CJ
E204	J204	FM1110	2N3955	HI1-0200-5	DG200BK	HI3-0390-5	DGM190CJ
E210	2N5397	FM1110A	2N5908	HI1-0200-6	DG200C/D	HI3-0506-5	IH6116CPI

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ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
HI3-0506A-5	IH5116CPI	ITC4023	IT137	J109	J106	J4393	ITE4393
HI3-0507-5	IH6216CPI	ITC4024	IT137	J109-18	J106	J4416	ITE4416
HI3-0507A-5	IH5216CPI	ITC4025	IT137	J110	J107	J4856	ITE4856
HI3-0508-5	IH6108CPE	ITE2453	IT120	J110-18	J107	J4857	ITE4857
HI3-0508A-5	IH5108CPE	ITE2639	IT120	J111	J111	J4858	ITE4858
HI3-0509-5	IH6208CPE	ITE2640	IT122	J111-18	J111	J4859	ITE4859
HI3-0509A-5	IH5208CPE	ITE2641	IT122	J111A	J111	J4860	ITE4860
ID100	ID100	ITE2642	IT120	J111A-18	J111	J4861	ITE4861
ID101	ID101	ITE2643	IT122	J112	J112	J4867	2N4867
IMF3954	2N3954	ITE2644	IT122	J112-18	J112	J4867A	2N4867A
IMF3954A	2N3954A	ITE2720	IT120	J112A	J112	J4867RR	2N4867
IMF3955	2N3955	ITE2721	IT122	J112A-18	J112	J4868	2N4868
IMF3955A	2N3955A	ITE2722	IT120	J113	J113	J4868A	2N4868A
IMF3956	2N3956	ITE2903	IT122	J113-18	J113	J4868RR	2N4868
IMF3957	2N3957	ITE2913	IT122	J113A	J113	J4869	2N4869
IMF3958	2N3958	ITE2914	IT122	J113A-18	J113	J4869A	2N4869A
IMF5911	IMF5911	ITE2915	IT120	J114	2N5555	J4869RR	2N4869
IMF5912	IMF5912	ITE2916	IT120	J1401	IT501	J5103	2N5484
IMF6485	IMF6485	ITE2917	IT122	J1402	IT502	J5104	2N5485
IT100	IT100	ITE2918	IT122	J1403	IT503	J5105	2N5486
IT101	IT101	ITE2919	IT120	J1404	IT503	J5163	2N5486
IT108	ITE4416	ITE2920	IT120	J1405	IT504	K114-18	2N5555
IT109	ITE4416	ITE2936	IT120	J1406	IT505	K210-18	2N5397
IT120	IT120	ITE2937	IT120	J174	J174	K211-18	2N5397
IT120A	IT120A	ITE2972	IT122	J174-18	J174	K212-18	2N5397
IT121	IT121	ITE2973	IT122	J175	J175	K300-18	2N5397
IT122	IT122	ITE2974	IT120	J175-18	J175	K304-18	2N5486
IT124	IT124	ITE2975	IT120	J176	J176	K305-18	2N5484
IT126	IT126	ITE2976	IT120	J176-18	J176	K308-18	J308
IT127	IT127	ITE2977	IT120	J177	J177	K309-18	J309
IT128	IT128	ITE2978	IT120	J177-18	J177	K310-18	J310
IT129	IT129	ITE2979	IT120	J201	J201	KE3684	2N3684
IT130	IT130	ITE3066	2N3685	J201-18	J201	KE3685	2N3685
IT130A	IT130A	ITE3067	2N3686	J202	J202	KE3686	2N3686
IT131	IT131	ITE3068	2N3687	J202-18	J202	KE3687	2N3687
IT132	IT132	ITE3347	IT137	J203	J203	KE3823	2N3823
IT136	IT136	ITE3348	IT138	J203-18	J203	KE3970	ITE4391
IT137	IT137	ITE3349	IT139	J204	J204	KE3971	ITE4392
IT138	IT138	ITE3350	IT137	J204-18	J204	KE3972	ITE4393
IT139	IT139	ITE3351	IT138	J210	2N5397	KE4091	ITE4091
IT140	IT140	ITE3680	IT120	J211	2N5397	KE4092	ITE4092
IT1700	IT1700	ITE3800	IT132	J212	2N5397	KE4093	ITE4093
IT1701	3N172	ITE3802	IT132	J230	2N4867	KE4220	2N5457
IT1702	3N163	ITE3804	IT130	J231	2N4868	KE4221	2N5459
IT1750	IT1750	ITE3806	IT132	J232	2N4869	KE4222	2N5459
IT2700	3N165	ITE3807	IT132	J270	J270	KE4223	J204
IT2701	3N165	ITE3808	IT132	J270-18	J270	KE4391	ITE4391
IT400	2N4392	ITE3809	IT132	J271	J271	KE4392	ITE4392
IT500	IT500	ITE3810	IT130	J271-18	J271	KE4393	ITE4393
IT500P	IT500	ITE3811	IT130	J300	2N5397	KE4416	ITE4416
IT501	IT501	ITE3907	IT120	J304	2N5486	KE4856	ITE4391
IT501P	IT501	ITE3908	IT120	J305	2N5484	KE4857	ITE4392
IT502	IT502	ITE4017	IT139	J308	J308	KE4858	ITE4393
IT502P	IT502	ITE4018	IT139	J309	J309	KE4859	ITE4391
IT503	IT503	ITE4019	IT139	J310	J310	KE4860	ITE4392
IT503P	IT503	ITE4020	IT139	J315	2N5397	KE4861	ITE4393
IT504	IT504	ITE4021	IT139	J316	U309	KE510	ITE4393
IT505	IT505	ITE4022	IT139	J317	U310	KE5103	J204
IT550	IT550	ITE4023	IT137	J3970	ITE4391	KE5104	ITE4416
IT5911	IT5911	ITE4024	IT137	J3971	ITE4392	KE5105	ITE4416
IT5912	IT5912	ITE4025	IT137	J3972	ITE4393	KE511	ITE4392
ITC2972	IT122	ITE4091	ITE4091	J401	IT501	KH5196	2N5196
ITC2973	IT122	ITE4092	ITE4092	J402	IT502	KH5197	2N5197
ITC2974	IT120	ITE4093	ITE4093	J403	IT503	KH5198	2N5198
ITC2975	IT120	ITE4117	2N4117	J404	IT503	KH5199	2N5199
ITC2976	IT120	ITE4118	2N4118	J405	IT504	KS5183	ICM7269
ITC2977	IT120	ITE4119	2N4119	J406	IT505	KS5240B01H	ICM7245B
ITC2978	IT120	ITE4338	2N4338	J4091	ITE4091	KS5240B01J	ICM7245A
ITC2979	IT120	ITE4339	2N4339	J4092	ITE4092	KS5240B10H	ICM7245D
ITC3347	IT137	ITE4340	2N4340	J4093	ITE4093	KS5240B12H	ICM7245E
ITC3348	IT138	ITE4341	2N4341	J410	IT502	KS5240B20H	ICM7245F
ITC3349	IT139	ITE4391	ITE4391	J411	IT503	KS5240U01E	ICM7245U
ITC3350	IT137	ITE4392	ITE4392	J412	IT503	LDF603	2N4221
ITC3351	IT138	ITE4393	ITE4393	J420	IT5911	LDF604	2N4221
ITC3352	IT139	ITE4416	ITE4416	J421	IT5912	LDF605	2N4221
ITC3800	IT132	ITE4867	2N4867	J4220	J204	LF11201D	DG201AK
ITC3802	IT132	ITE4868	2N4868	J4221	J202	LF11201D/883	DG201AK/883B
ITC3804	IT130	ITE4869	2N4869	J4222	J203	LF11202D	IH202MJE
ITC3806	IT132	J100	2N5458	J4223	J202	LF11202D/883	IH202MJE/883B
ITC3807	IT132	J101	2N4338	J4224	J202	LF11508D	IH6108MJE
ITC3808	IT132	J102	2N5457	J430	J309(X2)	LF11508D/883	IH6108MJE/883B
ITC3809	IT132	J103	2N5459	J4302	2N4302	LF11509D	IH6208MJE
ITC3810	IT130	J105	J105	J4303	2N5459	LF11509D/883	IH6208MJE/883B
ITC3811	IT130	J105-18	J105	J4304	2N5458	LF13201D	DG201BK
ITC4017	IT139	J106	J106	J431	J310(X2)	LF13201N	DG201CJ
ITC4018	IT139	J106-18	J106	J433	2N5457	LF13202D	IH202CJE
ITC4019	IT139	J107	J107	J4338	2N5457	LF13508D	IH6108CJE
ITC4020	IT139	J107-18	J107	J4339	2N5457	LF13508N	IH6108CPE
ITC4021	IT139	J108	J105	J4391	ITE4391	LF13509D	IH6208CJE
ITC4022	IT139	J108-18	J105	J4392	ITE4392	LF13509N	IH6208CPE

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ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
LH0042	LH0042	LTC1044	ICL7660	MD7003A	IT132	MEM807A	3N172
LH2108	LH2108	LTC1052	ICL7650	MD7003B	IT132	MEM814	3N161
LH2308	LH2308	LTC7652	ICL7652	MD7004	IT129	MEM816	3N172
LM105	LM105	M103	3N161	MD7007	IT129	MEM817	3N172
LM108	LM108	M104	3N161	MD7007A	IT129	MEM823	MFE823
LM113	ICL8069	M106	3N166	MD7007B	IT129	MEM954	3N188
LM114	IT120	M107	3N189	MD708	IT129	MEM954A	3N188
LM114A	IT120A	M108	3N191	MD708A	IT129	MEM954B	3N188
LM114AH	IT120A	M113	3N161	MD708B	IT129	MEM955	3N190
LM114H	IT120	M114	3N161	MD8001	IT120	MEM955A	3N190
LM115	IT120	M116	M116	MD8002	IT120	MEM955B	3N190
LM115A	IT120A	M117	2N4351	MD8003	IT122	MF510	2N4092
LM115AH	IT120A	M119	3N161	MD918	IT122	MF803	2N4338
LM115H	IT120	M163	3N163	MD918A	IT122	MF818	2N4858
LM194	IT120A	M164	3N164	MD918B	IT122	MFE2000	2N4416
LM305	LM305	M5001	ICM7269	MD982	IT139	MFE2001	2N4416
LM308	LM308	M511	3N172	MD984	IT139	MFE2004	2N4093
LM394	IT120A	M511A	3N172	MEF103	2N5457	MFE2005	2N4092
LM4250	LM4250	M517	3N163	MEF104	2N5459	MFE2006	2N4091
LS3069	2N5458	M58434P	ICM7038D	MEF3069	2N4341	MFE2007	2N4860
LS3070	2N5458	M58435P	ICM1115B	MEF3070	2N4339	MFE2008	2N4859
LS3071	2N5458	M58436-001P	ICM7050G	MEF3458	2N4341	MFE2009	2N4859
LS3458	J204	M58437-001P	ICM7070L	MEF3459	2N4339	MFE2010	2N4859
LS3459	J204	MA7807	IT132	MEF3460	2N4338	MFE2011	2N5433
LS3460	J204	MA7809	IT132	MEF3684	2N3684	MFE2012	2N5434
LS3684	2N3684	MAT-01AH	IT140	MEF3685	2N3685	MFE2012	2N5433
LS3685	2N3685	MAT-01FH	IT140	MEF3686	2N3686	MFE2093	2N4338
LS3686	2N3686	MAT-01GH	IT140	MEF3687	2N3687	MFE2094	2N4339
LS3687	2N3687	MAT-01H	IT140	MEF3821	2N3821	MFE2095	2N4340
LS3819	2N5484	MB101	ICM7245B	MEF3822	2N3822	MFE2133	2N4860
LS3821	2N5457	MB103	ICM7245E	MEF3823	2N3823	MFE2912	2N5433
LS3822	2N5458	MB105	ICM7245U	MEF3954	2N3954	MFE3002	3N170
LS3823	2N5458	MB107	ICM7245D	MEF3955	2N3955	MFE3003	3N164
LS3921	2N3921	MB108	ICM7245E	MEF3956	2N3956	MFE3020	3N166
LS3922	2N3922	MB143	ICM7245A	MEF3957	2N3957	MFE3021	3N166
LS3966	ITE4416	MB144	ICM7245F	MEF3958	2N3958	MFE4007	2N3686
LS3967	ITE4416	MB510	ICM1115B	MEF4223	2N4223	MFE4008	2N3686
LS3968	ITE4416	MB511	ICM7050H	MEF4224	2N4224	MFE4009	2N3685
LS3969	ITE4416	MB512	ICM7050H	MEF4391	ITE4391	MFE4010	2N2608
LS4220	J204	MB513	ICM7050G	MEF4392	ITE4392	MFE4011	2N2608
LS4221	J202	MB521	ITS9068	MEF4393	ITE4393	MFE4012	2N2609
LS4222	J203	MB522	ITS9068	MEF4416	ITE4416	MFE823	IT1700
LS4223	J202	MB531	ICM7050H	MEF4856	2N4856	MHW590	AD590
LS4224	J202	MB533	ICM7050H	MEF4857	2N4857	MJ41	ICM1424C
LS4338	2N5457	MB541	ICM7052	MEF4858	2N4858	MJ6	ICM7220
LS4339	2N5457	MB542	ICM7052	MEF4859	2N4859	MK10	2N4416
LS4340	2N5457	MB7B	ICM7245U	MEF4860	2N4860	MM450H	MM450H
LS4341	2N5458	MCC14440	ICM1424C	MEF4861	2N4861	MM451H	MM451H
LS4391	ITE4391	MCC14483	ICM7210	MEF5103	ITE4416	MM452D	MM452J
LS4392	ITE4392	MD1120	IT122	MEF5104	ITE4416	MM452F	MM452F
LS4393	ITE4393	MD1121	IT122	MEF5105	ITE4416	MM455H	MM455H
LS4416	ITE4416	MD1122	IT122	MEF5245	ITE4416	MM550H	MM550H
LS4856	ITE4091	MD1123	IT139	MEF5246	2N5484	MM551H	MM551H
LS4857	ITE4092	MD1129	IT129	MEF5247	2N5486	MM552D	MM552J
LS4858	ITE4093	MD1130	IT139	MEF5248	2N5486	MM552F	MM552F
LS4859	ITE4091	MD2218	IT129	MEF5284	2N5484	MM555H	MM555H
LS4860	ITE4092	MD2218A	IT129	MEF5285	2N5485	MMF1	2N5197
LS4861	ITE4093	MD2219	IT129	MEF5286	2N5486	MMF2	2N3921
LS5103	2N5484	MD2219A	IT129	MEF5561	U401	MMF3	2N5198
LS5104	2N5485	MD2369	IT129	MEF5562	U402	MMF4	2N3922
LS5105	2N5486	MD2369A	IT129	MEF5563	U403	MMF5	2N5199
LS5245	ITE4416	MD2369B	IT122	MEM511	3N172	MMF6	2N3955A
LS5246	2N5484	MD2904	IT139	MEM511A	3N172	MMT3823	2N3823
LS5247	2N5486	MD2904A	IT139	MEM511C	3N172	MN6091	ICM7038B
LS5248	2N5486	MD2905	IT139	MEM517	3N172	MN6092A	ICM7038E
LS5358	J204	MD2905A	IT139	MEM517A	3N172	MN6093	ICM7051A
LS5359	J204	MD2974	IT120	MEM517B	3N172	MN6252	ICM7050G
LS5360	J202	MD2975	IT120	MEM517C	3N172	MP301	IT124
LS5361	J202	MD2978	IT120	MEM550	3N189	MP302	IT124
LS5362	J203	MD2979	IT120	MEM550C	3N189	MP303	IT124
LS5363	J203	MD3008	IT120	MEM550F	3N189	MP310	2N4045
LS5364	J203	MD3250	IT132	MEM551	3N190	MP311	2N4045
LS5391	2N4867A	MD3250A	IT131	MEM551C	3N189	MP312	2N4044
LS5392	2N4868A	MD3251	IT132	MEM556	3N172	MP313	IT124
LS5393	2N4869A	MD3251A	IT131	MEM556C	3N172	MP318	IT120A
LS5394	2N4869A	MD3409	IT129	MEM560	3N161	MP350	IT132
LS5395	2N4869A	MD3410	IT129	MEM560C	3N161	MP351	IT130
LS5396	2N4869A	MD3467	IT139	MEM561	3N163	MP352	IT130
LS5457	2N5457	MD3725	IT129	MEM561C	3N163	MP358	IT130A
LS5458	2N5458	MD3762	IT139	MEM562	2N4351	MP360	IT132
LS5459	2N5459	MD4957	IT132	MEM562C	2N4351	MP361	IT130A
LS5484	2N5484	MD5000	IT132	MEM563	2N4351	MP362	IT130A
LS5485	2N5485	MD5000A	IT132	MEM563C	2N4351	MP3954	2N3954
LS5486	2N5486	MD5000B	IT132	MEM711	M116	MP3954A	2N3954A
LS5556	2N3685	MD7000	IT129	MEM712	M116	MP3955	2N3955
LS5557	2N3684	MD7001	IT139	MEM712A	M116	MP3956	2N3956
LS5558	2N3684	MD7002	IT122	MEM713	3N170	MP3957	2N3957
LS5638	2N5638	MD7002A	IT122	MEM806	3N163	MP3958	2N3958
LS5639	2N5639	MD7002B	IT122	MEM806A	3N163	MP5905	2N5905
LS5640	2N5640	MD7003	IT132	MEM807	3N172	MP5906	2N5906

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ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
MP5907	2N5907	NF4303	2N5459	PF511	2N5114	SG305	LM305
MP5908	2N5908	NF4304	2N5458	PF5301	2N4118A	SG308	LM308
MP5909	2N5909	NF4445	2N5432	PF5301-1	2N4117A	SG4250	LM4250
MP5911	2N5911	NF4446	2N5433	PF5301-2	2N4118A	SG733	UA733
MP5912	2N5912	NF4447	2N5433	PF5301-3	2N4118A	SI7135CPI	ICL7135CPI
MP7520JD	AD7520JD	NF4448	2N5433	PL1091	2N3823	SI7660	ICL7660
MP7520JN	AD7520JN	NF500	2N4224	PL1092	2N3823	SI7661	ICL7662
MP7520KD	AD7520KD	NF501	2N4224	PL1093	2N3823	SJM181BCC	JM38510/11101BCC
MP7520KN	AD7520KN	NF506	2N4416	PL1094	2N3823	SJM181BIC	JM38510/11101BIC
MP7520LD	AD7520LD	NF5101	2N4867	PM308	LM308	SJM182BCC	JM38510/11102BCC
MP7520LN	AD7520LN	NF5102	2N4867	PN3684	2N3684	SJM182BIC	JM38510/11102BIC
MP7520SD	AD7520SD	NF5103	2N4867	PN3685	2N3685	SJM184BEC	JM38510/11103BEC
MP7520TD	AD7520TD	NF511	2N4860	PN3686	2N3686	SJM185BEC	JM38510/11104BEC
MP7520UD	AD7520UD	NF5163	2N4341	PN3687	2N3687	SJM187BCC	JM38510/11105BCC
MP7521JD	AD7521JD	NF520	2N3684	PN4091	ITE4091	SJM187BIC	JM38510/11105BIC
MP7521JN	AD7521JN	NF521	2N3685	PN4092	ITE4092	SJM188BCC	JM38510/11106BCC
MP7521KD	AD7521KD	NF522	2N3686	PN4093	ITE4093	SJM188BIC	JM38510/11106BIC
MP7521KN	AD7521KN	NF523	2N3865	PN4220	J204	SJM190BEC	JM38510/11107BEC
MP7521LD	AD7521LD	NF530	2N4341	PN4221	J202	SJM191BEC	JM38510/11108BEC
MP7521LN	AD7521LN	NF5301	2N4118A	PN4222	J203	SL301AT	IT129
MP7521SD	AD7521SD	NF5301-1	2N4117A	PN4223	J204	SL301BT	IT129
MP7521TD	AD7521TD	NF5301-2	2N4118A	PN4224	J202	SL301CT	IT129
MP7521UD	AD7521UD	NF5301-3	2N4118A	PN4342	2N5461	SL301ET	IT129
MP7523JN	AD7523JN	NF531	2N4339	PN4360	2N5460	SL360C	IT129
MP7523KN	AD7523KN	NF532	2N4341	PN4391	ITE4391	SL362C	IT129
MP7523LN	AD7523LN	NF533	2N4339	PN4392	ITE4392	SM5011	ICM7050G
MP7621AD	AD7541AD	NF5457	2N5457	PN4416	ITE4416	SM5510	ICM1115B
MP7621BD	AD7541BD	NF5458	2N5458	PN4856	2N4856	SM5530B	ICM7070P
MP7621JN	AD7541JN	NF5459	2N5459	PN4857	2N4857	SU2000	2N4340
MP7621KN	AD7541KN	NF5484	2N5484	PN4858	2N4858	SU2020	2N3954
MP7621SD	AD7541SD	NF5485	2N5485	PN4859	2N4859	SU2021	2N3954
MP7621TD	AD7541TD	NF5486	2N5486	PN4860	2N4860	SU2022	2N3954
MP804	2N5520	NF5555	2N5484	PN4861	2N4861	SU2023	2N3954
MP830	2N5520	NF5638	2N5638	PN5033	2N5460	SU2024	2N3954
MP831	2N5521	NF5639	2N5639	PTC151	2N5484	SU2025	2N3954
MP832	2N5522	NF5640	2N5640	PTC152	2N5485	SU2026	2N3954
MP833	2N5523	NF5653	2N4860	S1424	ICM1424C	SU2027	2N3954
MP835	2N3954	NF5654	2N4861	SA2253	IT122	SU2028	2N3954
MP836	2N3955	NF580	2N5432	SA2254	IT122	SU2029	2N5197
MP837	2N3955	NF581	2N5432	SA2255	IT122	SU2029	2N3954
MP838	2N3956	NF582	2N5433	SA2644	IT120	SU2030	2N3955
MP839	2N3957	NF583	2N5434	SA2648	IT120	SU2030	2N3954
MP840	2N5520	NF584	2N5433	SA2710	IT120	SU2031	2N5198
MP841	2N5521	NF585	2N4859	SA2711	IT120	SU2031	2N3954
MP842	2N5523	NF6451	U310	SA2712	IT121	SU2032	2N3954
MPF102	2N5486	NF6452	U310	SA2713	IT121	SU2033	2N3954
MPF103	2N5457	NF6453	U310	SA2714	IT122	SU2034	2N3955
MPF104	2N5458	NF6454	U310	SA2715	IT120	SU2034	2N3954
MPF105	2N5459	NKT80111	2N4220	SA2716	IT120	SU2035	2N3955
MPF106	2N5485	NKT80112	2N4220	SA2717	IT121	SU2035	2N3954
MPF107	2N5486	NKT80113	2N3821	SA2718	IT122	SU2074	2N3954
MPF108	2N5486	NKT80211	2N4339	SA2719	IT120	SU2075	2N3954
MPF109	2N5484	NKT80212	2N4339	SA2720	IT121	SU2076	2N3954
MPF111	2N5458	NKT80213	2N4339	SA2721	IT122	SU2077	2N3955
MPF112	2N5458	NKT80214	2N4339	SA2722	IT120	SU2077	2N3954
MPF161	2N5398	NKT80215	2N4339	SA2723	IT121	SU2078	2N3955
MPF208	2N3821	NKT80216	2N4339	SA2724	IT122	SU2079	2N3955
MPF209	2N3821	NKT80421	2N4220	SA2726	IT122	SU2080	U404
MPF256	ITE4416	NKT80422	2N4220	SA2727	IT122	SU2081	U404
MPF4391	ITE4391	NKT80423	2N4220	SA2738	IT120A	SU2098	2N5197
MPF4392	ITE4392	NKT80424	2N4220	SA2739	IT120	SU2098A	2N5197
MPF4393	ITE4393	NPC108	2N5484	SCL54301	ICM1424C	SU2098B	2N5196
MPF820	J310	NPC211N	2N4338	SCL5478	ICM7269	SU2099	2N5197
MPF970	J175	NPC212N	2N4338	SDF1001	2N5432	SU2099A	2N5197
MPF971	J175	NPC213N	2N4338	SDF1002	2N5433	SU2365	2N3954
MPS5010	ICL8069	NPC214N	2N4339	SDF1003	2N5434	SU2365A	2N3954
MSM5001	ICM7269	NPC215N	2N4339	SDF500	2N5520	SU2366	2N3955
MSM5011	ICM1424C	NPC216N	2N4339	SDF501	2N5520	SU2366A	2N3955
MSM5977	ICM1424C	NPD5564	IT550	SDF502	2N5520	SU2367	2N3955
MTF101	2N5484	NPD5565	IT550	SDF503	2N5520	SU2367A	2N3955
MTF102	2N5484	NPD5566	IT550	SDF504	2N5520	SU2368	2N3956
MTF103	2N5457	NPD8301	2N3954	SDF505	2N5520	SU2368A	2N3956
MTF104	2N5459	NPD8302	2N3955	SDF506	2N5520	SU2369	2N3957
ND5700	IT120A	NPD8303	2N3956	SDF507	2N5520	SU2369A	2N3957
ND5701	IT120A	OT3	2N4338	SDF508	2N5520	SU2410	2N5907
ND5702	IT120	P1004	2N5116	SDF509	2N5520	SU2411	2N5908
NDF9401	IT500	P1005	2N5115	SDF510	2N3954	SU2412	2N5909
NDF9402	IT501	P1027	2N5267	SDF512	2N3954	SU2652	U401
NDF9403	IT502	P1028	2N5270	SDF513	2N3954	SU2652M	U401
NDF9404	IT503	P1029	2N5270	SDF514	2N3954	SU2653	U401
NDF9405	IT504	P1069E	2N2609	SDF661	IT122	SU2653M	U401
NDF9406	IT500	P1086E	2N5115	SDF662	IT122	SU2654	U401
NDF9407	IT501	P1087E	2N5516	SDF663	IT122	SU2654M	U401
NDF9408	IT502	P1117E	2N5640	SES3819	2N5484	SU2655	U402
NDF9409	IT503	P1118E	2N5641	SFT601	2N4338	SU2655M	U402
NDF9410	IT504	P1119E	2N5640	SFT602	2N4338	SU2656	U404
NE590	AD590	PF510	2N5115	SFT603	2N4339	SU2656M	U404
NE592	NE592	PF5101	2N4867	SFT604	2N4339	SX3819	2N5484
NF3819	2N5484	PF5102	2N4867	SG105	LM105	SX3820	2N2608
NF4302	2N5457	PF5103	2N4867	SG108	LM108	TC8031P	ICM7038A

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ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
TC8032P	ICM7038F	TD710	IT122	U112	2N2608	U285	2N5454
TC8051P	ICM7038B	TD711	IT122	U113	2N2608	U290	2N5432
TC8052P	ICM7038E	TD713	IT122	U114	2N2608	U291	2N5434
TC8056PA	ICM1115B	TIS14	2N4340	U1177	2N4220	U295	2N5432
TC8057P	ICM7038D	TIS25	2N3954	U1178	2N3821	U296	2N5434
TD100	IT129	TIS26	2N3954	U1179	2N3821	U300	2N5114
TD101	IT129	TIS27	2N3955	U1180	2N4221	U3000	2N4341
TD102	IT129	TIS34	2N5486	U1181	2N4220	U3001	2N4339
TD200	IT129	TIS41	2N4859	U1182	2N3821	U3002	2N4338
TD201	IT129	TIS42	2N4393	U1277	2N3684	U301	2N5115
TD202	IT129	TIS58	2N5484	U1278	2N3685	U3010	2N4341
TD2219	IT129	TIS59	2N5486	U1279	2N3686	U3011	2N4340
TD224	IT122	TIS68	2N3955A	U1280	2N3684	U3012	2N4338
TD225	IT122	TIS69	2N3955A	U1281	2N3822	U304	U304
TD226	IT122	TIS70	2N3956	U1282	2N4341	U305	U305
TD227	IT122	TIS73	ITE4391	U1283	2N4340	U306	U306
TD228	IT122	TIS74	ITE4392	U1284	2N4341	U308	U308
TD229	IT122	TIS75	ITE4393	U1285	2N4220	U309	U309
TD230	IT121	TIS88	2N4416	U1286	2N4341	U310	U310
TD231	IT121	TIS88A	2N4416	U1287	2N4092	U311	U310
TD232	IT122	TIXS33	2N4392	U1321	2N4860	U312	2N5397
TD233	IT122	TIXS35	2N4857	U1322	2N3822	U314	2N5555
TD234	IT122	TIXS36	2N4391	U1323	2N3822	U315	2N5397
TD235	IT122	TIXS41	2N4859	U1324	2N3687	U316	U309
TD236	IT122	TIXS42	2N5639	U1325	2N3686	U317	U310
TD237	IT122	TIXS59	2N5459	U133	2N2608	U320	2N5433
TD238	IT122	TIXS78	2N4341	U1420	2N3821	U321	2N5434
TD239	IT122	TIXS79	2N4341	U1421	2N3822	U322	2N5433
TD240	IT121	TL182CL	DGM182BA	U1422	2N3822	U328	**
TD241	IT121	TL182CN	DGM182CJ	U146	2N2608	U329	**
TD242	IT120A	TL182IL	DGM182BA	U147	2N2608	U330	**
TD243	IT120A	TL182IN	DGM182CJ	U148	2N2608	U331	**
TD244	IT129	TL182ML	DGM182AA	U149	2N2609	U350	**
TD245	IT129	TL185CJ	IH5045CJE	U168	2N2609	U401	U401
TD246	IT129	TL185CN	IH5045CPE	U1714	2N4340	U402	U402
TD247	IT129	TL185IJ	IH5045CJE	U1715	2N4340	U403	U403
TD248	IT129	TL185IN	IH5045CPE	U182	2N4857	U404	U404
TD250	IT120A	TL185MJ	IH5045MJE	U183	2N3824	U405	U405
TD2905	IT139	TL188CL	IH5042CTW	U1837E	2N5486	U406	U406
TD400	IT139	TL188CN	IH5042CPE	U184	2N5397	U410	2N3955
TD401	IT139	TL188IL	IH5042CTW	U1897E	U1897	U411	2N3956
TD402	IT139	TL188IN	IH5042CPE	U1898E	U1898	U412	2N3958
TD500	IT139	TL188ML	IH5042MTW	U1899E	U1899	U421	2N5908
TD501	IT139	TL191CJ	IH5043CJE	U197	2N4338	U422	2N5908
TD502	IT139	TL191CN	IH5043CPE	U198	2N4340	U423	2N5909
TD509	IT132	TL191IJ	IH5043CJE	U199	2N4341	U424	2N5908
TD510	IT132	TL191IN	IH5043CPE	U1994E	2N4416	U425	2N5908
TD511	IT132	TL191MJ	IH5043MJE	U200	2N4861	U426	2N5909
TD512	IT132	TL503	AD503	U201	2N4860	U430	J309(X2)
TD513	IT132	TL592	NE592	U202	2N4859	U431	J310(X2)
TD514	IT132	TLC555	ICM7555	U2047E	2N4416	U440	IT5911
TD517	IT132	TN4117	2N4117	U221	2N4391	U441	IT5912
TD518	IT132	TN4117A	2N4117A	U222	2N4391	UA105	LM105
TD519	IT132	TN4118	2N4118	U231	U231	UA108	LM108
TD520	IT139	TN4118A	2N4118A	U232	U232	UA305	LM305
TD521	IT139	TN4119	2N4119	U233	U233	UA308	LM308
TD522	IT139	TN4119A	2N4119A	U234	U234	UA733	UA733
TD523	IT139	TN4338	2N4338	U235	U235	UC100	2N3684
TD524	IT139	TN4339	2N4339	U240	2N5432	UC110	2N3685
TD525	IT132	TN4340	2N4340	U241	2N5433	UC115	2N4340
TD526	IT132	TN4341	2N4341	U242	2N5432	UC120	2N3686
TD527	IT131	TN5277	2N4341	U243	2N5433	UC130	2N3687
TD528	IT131	TN5278	2N4341	U244	2N5433	UC155	2N4416
TD5432	2N5432	TP5114	2N5114	U248	2N5902	UC1700	3N163
TD5433	2N5433	TP5115	2N5115	U248A	2N5906	UC1764	3N163
TD5434	2N5434	TP5116	2N5116	U249	2N5903	UC20	2N3686
TD550	IT129	TSC426	ICL7667	U249A	2N5907	UC200	2N3824
TD5902	2N5902	TSC7106CJL	ICL7106CJL	U250	2N5904	UC201	2N3824
TD5902A	2N5902	TSC7106CPL	ICL7106CPL	U250A	2N5908	UC21	2N3687
TD5903	2N5903	TSC7106RCPL	ICL7106RCPL	U251	2N5905	UC210	2N4416
TD5903A	2N5903	TSC7107CJL	ICL7107CJL	U251A	2N5909	UC2130	2N5452
TD5904	2N5904	TSC7107CPL	ICL7107CPL	U252	IT5911	UC2132	2N5453
TD5904A	2N5904	TSC7107RCPL	ICL7107RCPL	U253	IT5912	UC2134	2N5454
TD5905	2N5905	TSC7109CPL	ICL7109CPL	U254	2N4859	UC2136	2N5454
TD5905A	2N5905	TSC7109IJL	ICL7109IJL	U255	2N4860	UC2138	2N5454
TD5906	2N5906	TSC7109MJL	ICL7109MJL	U256	2N4861	UC2139	2N3958
TD5906A	2N5906	TSC7116CJL	ICL7116CJL	U257	U257	UC2147	2N3958
TD5907	2N5907	TSC7116CPL	ICL7116CPL	U257/TO-71	U257/TO-71	UC2148	2N3958
TD5907A	2N5907	TSC7117CJL	ICL7117CJL	U266	2N4856	UC2149	2N3958
TD5908	2N5908	TSC7117CPL	ICL7117CPL	U273	2N4118A	UC220	2N3822
TD5908A	2N5908	TSC7126CJL	ICL7126CJL	U273A	2N4118A	UC240	2N4869
TD5909	2N5909	TSC7126RCPL	ICL7126RCPL	U274	2N4119A	UC241	2N4869
TD5909A	2N5909	TSC7135CJI	ICL7135CJI	U274A	2N4119A	UC250	2N4091
TD5911	IT5911	TSC7135CPI	ICL7135CPI	U275	2N4119A	UC251	2N4392
TD5911A	IT5911	TSC7650	ICL7650	U275A	2N4119A	UC2766	3N166
TD5912	IT5912	TSC7660	ICL7660	U280	2N5452	UC300	2N2608
TD5912A	IT5912	TSC9491	ICL8069	U281	2N5453	UC310	2N2607
TD700	IT122	TT-590	AD590	U282	2N5453	UC320	2N2607
TD701	IT122	U110	2N2608	U283	2N5453	UC330	2N2607
TD709	IT122	U111	2N2608	U284	2N5454	UC340	2N2607

**CONSULT FACTORY

ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
UC40	2N2608						
UC400	2N5270						
UC401	2N5116						
UC41	2N2608						
UC410	2N5268						
UC420	2N5267						
UC450	2N5114						
UC451	2N5116						
UC588	2N4416						
UC703	2N4220						
UC704	2N4220						
UC705	2N4224						
UC707	2N4860						
UC714	2N3822						
UC714E	2N4341						
UC734	2N4416						
UC734E	2N4416						
UC751	2N4340						
UC752	2N4340						
UC753	2N4341						
UC754	2N4340						
UC755	2N4341						
UC756	2N4340						
UC805	2N5270						
UC807	2N5115						
UC814	2N5270						
UC851	2N2608						
UC853	2N2608						
UC854	2N2608						
UC855	2N2609						
UCN-4111M	ICM7038C						
UCN-4112M	ICM7051A						
UCN-4113M	ICM7038B						
UHP-503	AD503						
UPD1952P	ICM7220MFA						
UPD1962C	ICM7050G						
UPD1963C	ICM7050						
UPD815C	ICM7038E						
UPD816C	ICM7038B						
UPD820C	ICM1115B						
UPD833G	ICM7223						
UT100	2N5397						
UT101	2N5397						
UXC2910	IT126						
VCR10N	2N4869						
VCR11N	VNR11N						
VCR12N	2N3958						
VCR13N	2N3958						
VCR20N	2N4341						
VCR2N	VCR2N						
VCR3P	VCR2P						
VCR4N	VCR4N						
VCR5P	VCR5P						
VCR6P	VCR6P						
VCR7N	VCR7N						
VF28	2N4392						
VF811	2N4858						
VF815	2N4858						
VFW40	IT122						
VFW40A	IT120						
VR-8069	ICL8069						
W245A	ITE4416						
W245B	ITE4416						
W245C	ITE4416						
W300	2N5398						
W300A	2N5397						
W300B	2N5397						
W300C	2N5397						
W300D	2N5398						
WG-8038	ICL8038						
WK5457	2N5457						
WK5458	2N5458						
WK5459	2N5459						
XR8038	ICL8038						
ZDT40	IT129						
ZDT41	IT129						
ZDT42	IT129						
ZDT44	IT129						
ZDT45	IT129						

**CONSULT FACTORY

Section 1 — Selector Guides

Switches—Junction FET
N Channel

PART NUMBER	PACKAGE	$r_{DS(ON)}$ Ω Max	V_P V Min	Max	I_{GSS} pA Max	BV_{GSS} V Min	$I_{D(OFF)}$ pA Max	I_{DSS} mA Min	Max	t_{ap} ns Max	C_{rss} pF Max	C_{iss} pF Max	COMMENTS
2N3824	TO-72	250		8.0	−100	−50					3	6	High Isolation
2N3970	TO-18	30	−4.0	−10.0	−250	−40	250	50	150	50	6	25	High Isolation
2N3971	TO-18	60	−2.0	−5.0	−250	−40	250	25	75	90	6	25	High Isolation
2N3972	TO-18	100	−0.5	−3.0	−250	−40	250	5	30	180	6	25	High Isolation
* 2N4091	TO-18	30	−5.0	−10.0	−200	−40	200	30		65	5	16	High Isolation
2N4091A	TO-18	30	−5.0	−10.0	−40	−50	200	30		65	5	16	High Isolation
* 2N4092	TO-18	50	−2.0	−7.0	−200	−40	200	15		95	5	16	High Isolation
2N4092A	TO-18	50	−2.0	−7.0	40	−50	200	15		95	5	16	High Isolation
* 2N4093	TO-18	80	−1.0	−5.0	−200	−40	200	8		140	5	16	High Isolation
2N4093A	TO-18	80	−1.0	−5.0	40	−50	200	8		140	5	16	High Isolation
2N4391	TO-18	30	−4.0	−10.0	−100	−40	100	50	150	55	3.5	14	High Isolation
2N4392	TO-18	60	−2.0	−5.0	−100	−40	100	25	75	75	3.5	14	High Isolation
2N4393	TO-18	100	−0.5	−3.0	−100	−40	100	5	30	100	3.5	14	High Isolation
* 2N4856	TO-18	25	−4.0	−10.0	−250	−40	250	50		34	8	18	High Isolation
* 2N4857	TO-18	40	−2.0	−6.0	−250	−40	250	20	100	60	8	18	High Isolation
* 2N4858	TO-18	60	−0.8	−4.0	−250	−40	250	8	80	120	8	18	High Isolation
* 2N4859	TO-18	25	−4.0	−10.0	−250	−30	250	50		34	8	18	High Isolation
* 2N4860	TO-18	40	−2.0	−6.0	−250	−30	250	20	100	60	8	18	High Isolation
* 2N4861	TO-18	60	−0.8	−4.0	−250	−30	250	8	80	120	8	18	High Isolation
2N4978	TO-18	20	−2.0	−8.0	−500	−30	500	15		55	8	35	Low $r_{DS(ON)}$
2N5432	TO-52	5	−4.0	−10.0	−200	−25	200	150		41	15	30	Low $r_{DS(ON)}$
2N5433	TO-52	7	−3.0	−9.0	−200	−25	200	100		41	15	30	Low $r_{DS(ON)}$
2N5434	TO-52	10	−1.0	−4.0	−200	−25	200	30		41	15	30	Low $r_{DS(ON)}$
2N5555	TO-92	150		−10.0	−1nA	−25	10nA	15		35	1.2	5	Low Cost
2N5638	TO-92	30		−12.0	−1nA	−30	1nA	50		24	4	10	Low Cost
2N5639	TO-92	60		−8.0	−1nA	−30	1nA	25		44	4	10	Low Cost
2N5640	TO-92	100		−6.0	−1nA	−30	1nA	5		63	4	10	Low Cost
2N5653	TO-92	50		−12.0	−1nA	−30	1nA	40		24	3.5	10	Low Cost
2N5654	TO-92	100		−8.0	−1nA	−30	1nA	15		44	3.5	10	Low Cost
ITE4091	TO-92	30	−5.0	−10.0	−200	−40	200	30		65	5	16	Low Cost
ITE4092	TO-92	50	−2.0	−7.0	−200	−40	200	15		95	5	16	Low Cost
ITE4093	TO-92	80	−1.0	−5.0	−200	−40	200	8		140	5	16	Low Cost
ITE4391	TO-92	30	−4.0	−10.0	−100	−40	100	50	150	55	3.5	14	Low Cost
ITE4392	TO-92	60	−2.0	−5.0	−100	−40	100	25	75	75	3.5	14	Low Cost
ITE4393	TO-92	100	−0.5	−3.0	−100	−40	100	5	30	100	3.5	14	Low Cost
J105	TO-92	3	−4.5	−10.0	−3nA	−25	3nA	500		20			Lowest $r_{DS(ON)}$
J106	TO-92	6	−2.0	−6.0	−3nA	−25	3nA	200		20			Lowest $r_{DS(ON)}$
J107	TO-92	8	−0.5	−4.5	−3nA	−25	3nA	100		20			Lowest $r_{DS(ON)}$
J108	TO-92	8	−3.0	−10.0	−3nA	−25	3nA	80		41			Low Cost
J109	TO-92	12	−2.0	−6.0	−3nA	−25	3nA	40		41			Low Cost
J110	TO-92	18	−0.5	−4.0	−3nA	−25	3nA	10		41			Low Cost
J111	TO-92	30	−3.0	−10.0	−1nA	−35	1nA	20		48			Lowest Cost
J112	TO-92	50	−1.0	−5.0	−1nA	−35	1nA	5		48			Lowest Cost
J113	TO-92	100	−0.5	−3.0	−1nA	−35	1nA	2		48			Lowest Cost
J114	TO-92	150		−10.0	−1nA	−25	1nA	15		26			Low Cost

*Also available as JAN/JANTX & JANTXV

**Most TO-92's are available lead formed to a TO-18 or TO-5 configuration

Switches—Junction FET
N Channel

PART NUMBER	PACKAGE	$r_{DS(ON)}$ Ω Max	V_P V Min	Max	I_{GSS} pA Max	BV_{GSS} V Min	$I_{D(OFF)}$ pA Max	I_{DSS} mA Min	Max	t_{ap} ns Max	C_{rss} pF Max	C_{iss} pF Max	COMMENTS
PN4091	TO-92	30	−5.0	−10.0	−200	−40	200	30		65	5	16	Low Cost
PN4092	TO-92	50	−2.0	−7.0	−200	−40	200	15		95	5	16	Low Cost
PN4093	TO-92	80	−1.0	−5.0	−200	−40	200	8		140	5	16	Low Cost
PN5432	TO-92	5	−4.0	−10.0	−200	−25	200	150		41	15	30	Lowest $r_{DS(ON)}$
PN5433	TO-92	7	−3.0	−9.0	−200	−25	200	100		41	15	30	Lowest $r_{DS(ON)}$
PN5434	TO-92	10	−1.0	−4.0	−200	−25	200	30		41	15	30	Lowest $r_{DS(ON)}$
U200	TO-18	150	−0.5	−3.0	−1nA	−30	1nA	3	25		8	30	Low Cost
U201	TO-18	75	−1.5	−5.0	−1nA	−30	1nA	15	75		8	30	Low Cost
U202	TO-18	50	−3.5	−10.0	−1nA	−30	1nA	30	150		8	30	Low Cost
U1897	TO-92	30	−5.0	−10.0	−400	−40	200	30		65	5	16	Low Cost
U1898	TO-92	50	−2.0	−7.0	−400	−40	200	15		95	5	16	Low Cost
U1899	TO-92	80	−1.0	−5.0	−400	−40	200	8		140	5	16	Low Cost

*Also available as JAN/JANTX & JANTXV

**Most TO-92's are available lead formed to a TO-18 or TO-5 configuration

Switches—Junction FET
P Channel

PART NUMBER	PACKAGE	$r_{DS(ON)}$ Ω Max	V_P V Min	Max	I_{GSS} pA Max	BV_{GSS} V Min	$I_{D(OFF)}$ pA Max	I_{DSS} mA Min	Max	t_{ap} ns Max	C_{rss} pF Max	C_{iss} Max	COMMENTS
2N3382	TO-72	300	1.0	5.0	15nA	30	−2nA	−3	−30			16 typ	Low $r_{DS(ON)}$
2N3384	TO-72	180	4.0	5.0	15nA	30	−2nA	−15	−30			16 typ	Low $r_{DS(ON)}$
2N3386	TO-72	150	4.0	9.5	15nA	30	−2.5nA	−15	−50			16 typ	Low $r_{DS(ON)}$
2N3993	TO-72	150	4.0	9.5	1.2nA	25	−1.2nA	−10			4.5	16	
2N3994	TO-72	300	1.0	5.5	1.2nA	25	−1.2nA	−2			4.5	16	
2N5018	TO-18	75		12.0	2nA	30	−10nA	−10		100	10	45	Low $r_{DS(ON)}$
2N5019	TO-18	150		7.0	2nA	30	−10nA	−5		215	10	45	Low $r_{DS(ON)}$
* 2N5114	TO-18	75	5.0	10.0	500	30	−500	−30	−90	37	7	25	Low $r_{DS(ON)}$
* 2N5115	TO-18	100	3.0	6.0	500	30	−500	−15	−60	66	7	25	Low $r_{DS(ON)}$
* 2N5116	TO-18	150	1.0	4.0	500	30	−500	−5	−25	102	7	25	Low $r_{DS(ON)}$
IT100	TO-18	75	2.0	4.5	200	35	−100	−10			12	35	TTL Compatible
IT101	TO-18	60	4.0	10.0	200	35	−100	−20			12	35	TTL Compatible
J174	TO-92	85	5.0	10.0	1nA	30	−1nA	−20	−100	22			Low Cost
J175	TO-92	125	3.0	6.0	1nA	30	−1nA	−7	−60	45			Low Cost
J176	TO-92	250	1.0	4.0	1nA	30	−1nA	−2	−25	70			Low Cost
J177	TO-92	300	0.8	2.25	1nA	30	−1nA	−1.5	−20	90			TTL Compatible
PN5114	TO-92	75	5.0	10.0	500	30	−500	−30	−90	37	7	25	Low Cost
PN5115	TO-92	100	3.0	6.0	500	30	−500	−15	−60	68	7	25	Low Cost
PN5116	TO-92	150	1.0	4.0	500	30	−500	−5	−25	102	7	25	Low Cost
U304	TO-18	85	5.0	10.0	500	30	−500	−30	−90	70	7	27	High Off Isolation
U305	TO-18	110	3.0	6.0	500	30	−500	−15	−60	105	7	27	High Off Isolation
U306	TO-18	175	1.0	4.0	500	30	−500	−5	−25	140	7	27	High Off Isolation

*Also available as JAN/JANTX & JANTXV

**Most TO-92's are available lead formed to a TO-18 or TO-5 configuration

Switches and Amplifiers — MOSFET

N-Channel

PART NUMBER	PACKAGE	$V_{GS(TH)}$ V Min	Max	BV_{DSS} V Min	I_{DSS} pA Max	I_{GSS} pA Max	g_{fs} μmho Min	$r_{DS(ON)}$ Ω Max	$I_{D(ON)}$ mA Min	$I_{D(ON)}$ mA Max	COMMENTS
2N4351	TO-72	1.0	5.0	25	10nA	10	1000	300	3		High Input Z
3N170	TO-72	1.0	2.0	25	10nA	10	1000	200	10		High Input Z
3N171	TO-72	1.5	3.0	25	10nA	10	1000	200	10		High Input Z
IT1750	TO-72	0.5	3.0	25	10nA	10	3000	50	10		Low $r_{DS(ON)}$
M116	TO-72	1.0	5.0	30	10nA	100		100			Diode Protected
M117	TO-72	1.0	5.0	30	10nA	1		100			High Input Z

P-Channel

Generally used where max. isolation between signal source and logic drive is required: switch "On" resistance varies with signal amplitude.

PART NUMBER	PACKAGE	$V_{GS(TH)}$ V Min	Max	BV_{DSS} V Min	I_{DSS} pA Max	I_{GSS} pA Max	g_{fs} μmho Min	$r_{DS(ON)}$ Ω Max	$I_{D(ON)}$ mA Min	$I_{D(ON)}$ mA Max	COMMENTS
2N4352	TO-72	−1.0	−5.0	−25	−10nA	10	1000	600	−3		High Input Z
3N155	TO-72	−1.5	−3.2	−35	−1nA	10	1000	600	−5		High Input Z
3N155A	TO-72	−1.5	−3.2	−35	−250	10	1000	300	−5		High Input Z
3N157	TO-72	−1.5	−3.2	−35	−1nA	10	1000		−5		High Input Z
3N157A	TO-72	−1.5	−3.2	−50	−250	10	1000		−5		High Input Z
3N161	TO-72	−1.5	−5.0	−25	−10nA	−100	3500		−40	−120	Diode Protected
3N163	TO-72	−2.0	−5.0	−40	−200	−10	2000	250	−5	−30	High Input Z
3N164	TO-72	−2.0	−5.0	−30	400	10	1000	300	−3	−30	High Input Z
3N172	TO-72	−2.0	−5.0	−40	−400	−200		250	−5	−30	Diode Protected
3N173	TO-72	−2.0	−5.0	−30	−10nA	−500		350	−5	−30	Diode Protected
IT1700	TO-72	−2.0	−5.0	−40	200		2000	400	−2		High Input Z
IT1701	TO-72	−2.0	−5.0	−40	200	100	2000	400	−2		Diode Protected

Low Leakage Diodes

PART NUMBER	PACKAGE	i_R @ 1V (pA) Typ	I_R @ 10 V, 125°C (nA) Max	BV_R @ 1μA (V) Min	V_F @ 10mA (V) Min	(V) Max	COMMENTS
ID100	TO-78	0.1	10	30	0.8	1.1	(Note 1)
ID101	TO-71	0.1	10	30	0.8	1.1	(Note 1)

Note 1. Used to protect the inputs of MOSFETs such as 3N163, while maintaining input leakage < 0.1pA.

*Also available as JAN/JANTX & JANTXV.

**Most TO-92's are available lead formed to a TO-18 or TO-5 configuration.

Amplifiers — Junction FET

N Channel

PART NUMBER	PACKAGE	g_{fs} μmho Min	I_{DSS} mA Min	Max	V_P V Min	Max	I_{GSS} pA Max	BV_{GSS} V Min	C_{iss} pF Max	C_{rss} pF Max	e_n nV/√Hz Max	COMMENTS
N-Channel:												
2N3684	TO-72	2000	2.5	7.5	−2.0	−5.0	−100	−50	4	1.2	150 @ 20Hz	Low Noise
2N3685	TO-72	1500	1.0	3.0	−1.0	−3.5	−100	−50	4	1.2	150 @ 20Hz	Low Noise
2N3686	TO-72	1000	0.4	1.2	−0.6	−2.0	−100	−50	4	1.2	150 @ 20Hz	Low Noise
2N3687	TO-72	500	0.1	0.5	−0.3	−1.2	−100	−50	4	1.2	150 @ 20Hz	Low Noise
* 2N3821	TO-72	1500	0.5	2.5		−4.0	−100	−50	6	3	200 @ 10Hz	GPA
2N3822	TO-72	3000	2.0	10.0		−6.0	−100	−50	6	3	200 @ 10Hz	GPA
2N3823	TO-72	3500	4.0	20.0	−1.0	−7.5	−500	−30	6	2	2.5dB @ 100MHz	VHF Amp
2N4117	TO-72	70	0.03	0.09	−0.6	−1.8	−10	−40	3	1.5		Low Leakage
2N4117A	TO-72	70	0.03	0.09	−0.6	−1.8	−1	−40	3	1.5		Low Leakage
2N4118	TO-72	80	0.08	0.24	−1.0	−3.0	−10	−40	3	1.5		Low Leakage
2N4118A	TO-72	80	0.06	0.24	−1.0	−3.0	−1	−40	3	1.5		Low Leakage
2N4119	TO-72	100	0.2	0.6	−2.0	−6.0	−10	−40	3	1.5		Low Leakage
2N4119A	TO-72	100	0.2	0.6	−2.0	−6.0	−1	−40	3	1.5		Low Leakage
2N4220	TO-72	1000	0.5	3.0		−4.0	−100	−30	6	2		Low Cost
2N4220A	TO-72	1000	0.5	3.0		−4.0	−100	−30	6	2	2.5dB @ 100Hz	GPA
2N4221	TO-72	2000	2.0	6.0		−6.0	−100	−30	6	2		Low Cost
2N4221A	TO-72	2000	2.0	6.0		−6.0	−100	−30	6	2	2.5dB @ 100Hz	GPA
2N4222	TO-72	2500	5.0	15.0		−8.0	−100	−30	6	2		Low Cost
2N4222A	TO-72	2500	5.0	15.0		−8.0	−100	−30	6	2	2.5dB @ 100Hz	GPA
2N4223	TO-72	3000	3.0	18.0	−0.1	−8.0	−250	−30	6	2		Low Cost
2N4224	TO-72	2000	2.0	20.0	−0.1	−0.8	−150	−30	6	2		Low Cost
2N4338	TO-18	600	0.2	0.6	−0.3	−1.0	−100	−50	7	3	65 @ 1kHz	General Purpose Amp
2N4339	TO-18	800	0.5	1.5	−0.6	−1.8	−100	−50	7	3	65 @ 1kHz	General Purpose Amp
2N4340	TO-18	1300	1.2	3.6	−1.0	−3.0	−100	−50	7	3	65 @ 1kHz	General Purpose Amp
2N4341	TO-18	2000	3.0	9.0	−2.0	−6.0	−100	−50	7	3	65 @ 1kHz	General Purpose Amp
2N4416	TO-72	4500	5.0	15.0		−6.0	−100	−30	4	2		High Gain
2N4867	TO-72	700	0.4	1.2	−0.7	−2.0	−250	−40	25	5	10 @ 1kHz	Audio Amp
2N4867A	TO-72	700	0.4	1.2	−0.7	−2.0	−250	−40	25	5	5 @ 1kHz	Low Noise/GPA
2N4868	TO-72	1000	1.0	3.0	−1.0	−3.0	−250	−40	25	5	10 @ 1kHz	Audio Amp
2N4868A	TO-72	1000	1.0	3.0	−1.0	−3.0	−250	−40	25	5	5 @ 1kHz	Low Noise/GPA
2N4869	TO-72	1300	2.5	7.5	−1.8	−5.0	−250	−40	25	5	10 @ 1kHz	Audio Amp
2N4869A	TO-72	1300	2.5	7.5	−1.8	−5.0	−250	−40	25	5	5 @ 1kHz	Low Noise/GPA
2N5397	TO-72	6000	10.0	30.0	−1.0	−6.0	−100	−25	5.0	1.2	3.5dB @ 450MHz	VHF Amp
2N5398	TO-72	5500	5.0	40.0	−1.0	−6.0	−100	−25	5.5	1.3		VHF Amp
2N5457	TO-92	1000	1.0	5.0	−0.5	−6.0	−1nA	−25	7	3	3dB @ 1kHz	Low Cost/GPA
2N5458	TO-92	1500	2.0	9.0	−1.0	−7.0	−1nA	−25	7	3	3dB @ 1kHz	Low Cost/GPA
2N5459	TO-92	2000	4.0	16.0	−2.0	−8.0	−1nA	−25	7	3	3dB @ 1kHz	Low Cost/GPA
2N5484	TO-92	3000	1.0	5.0	−0.3	−0.3	−1nA	−25	5	1	120 @ 1kHz	Low Cost RF Amp
2N5485	TO-92	3500	4.0	10.0	−0.5	−4.0	−1nA	−25	5	1	120 @ 1kHz	Low Cost RF Amp
2N5486	TO-92	4000	8.0	20.0	−2.0	−6.0	−1nA	−25	5	1	120 @ 1kHz	Low Cost RF Amp
ITE4416	TO-92	4500	5.0	15.0		−6.0	100	−30	4	2		Low Cost RF Amp
J201	TO-92	500	0.2	1.0	−0.3	−1.5	−100	−40	4typ.	1typ.	5typ. @ 1kHz	GPA/Low Cost
J202	TO-92	1000	0.9	4.5	−0.8	−4.0	−100	−40	4typ.	1typ.	5typ. @ 1kHz	GPA/Low Cost
J203	TO-92	1500	4.0	20.0	−2.0	−10.0	−100	−40	4typ.	1typ.	5typ. @ 1kHz	GPA/Low Cost
J204	TO-92				−0.5	−2.0	−100	−25	4typ.	1typ.	10typ.@ 1kHz	GPA/Low Cost
J210	TO-92	4000	2.0	15.0	−1.0	−3.0	−100	−25	4typ.	1typ.	10typ. @ 1kHz	GPA/Low Cost
J211	TO-92	7000	7.0	20.0	−2.5	−4.5	−100	−25	4typ.	1typ.	10typ. @ 1kHz	GPA/Low Cost
J212	TO-92	7000	15.0	40.0	−4.0	−6.0	−100	−25	4typ.	1typ.	10typ. @ 1kHz	GPA/Low Cost

*Available as JAN/TX/TXV.

**Most TO-92's are available lead formed to a TO-18 or TO-5 configuration.

Amplifiers — Junction FET
N Channel

PART NUMBER	PACKAGE	g_{fs} μmho Min	I_{DSS} mA Min	Max	V_P V Min	Max	I_{GSS} pA Max	BV_{GSS} V Min	C_{iss} pF Max	C_{rss} pF Max	e_n nV/√Hz Max	COMMENTS
J300	TO-92	4500	4.0	45.0	−1.5	−7.0	−500	−25	5.5	1.7		VHF AMP/Low Cost
J308	TO-92	8000	12.0	60.0	−1.0	−6.5	−1nA	−25			2.7dB @ 450MHz	VHF Amp/Low Cost
J309	TO-92	10,000	12.0	30.0	−1.0	−4.0	−1nA	−25			2.7dB @ 450MHz	VHF Amp/Low Cost
J310	TO-92	8000	24.0	60.0	−2.0	−6.5	−1nA	−25			2.7dB @ 450MHz	VHF Amp/Low Cost
PN4302	TO-92	1000	0.5	5.0		−4.0	−1nA	−30	6	2	2dB @	PA/Low Cost
PN4303	TO-92	2000	4.0	10.0		−6.0	−1nA	−30	6	2	2dB @ 1kHz	PA/Low Cost
PN4304	TO-92	1000	0.5	15.0		−10.0	−1nA	−30	6	2	3dB @ 1kHz	GPA/Low Cost
PN4338	TO-92	600	0.2	0.6	−0.3	−1.0	−100	−50	7	3	1dB @ 1kHz	GPA/VCR
PN4339	TO-92	800	0.5	1.5	−0.6	−1.8	−100	−50	7	3	1db @ 1kHz	GPA/VCR
PN4340	TO-92	1300	1.2	3.6	−1.0	−3.0	−100	−50	7	3	1db @ 1kHz	GPA/VCR
PN4341	TO-92	2000	3.0	9.0	−2.0	−6.0	−100	−50	7	3	1db @ 1kHZ	GPA/VCR
PN4416	TO-92	4500	5.0	15.0		−6.0	−100	−30	4	2		High Gain/Low Cost
PN5163	TO-92	2000	1.0	40.0	−0.4	−8.0	−10nA	−25	20	5	50 @ 1kHz	Low Cost
U308	TO-52	10,000	12.0	60.0	−1.0	−6.0	−150	−25	7typ.	4.0typ.	2.7dB @ 450MHz	VHF Amp
U309	TO-52	10,000	12.0	30.0	−1.0	−4.0	−150	−25	7typ.	4.0typ.	2.7dB @ 450MHz	VHF Amp
U310	TO-52	10,000	24.0	60.0	−2.5	−6.0	−150	−25	7typ.	4.0typ.	2.7dB @ 450MHz	VHF Amp

*Available as JAN/TX/TXV.

**Most TO-92's are available lead formed to a TO-18 or TO-5 configuration.

Amplifiers — Junction FET
P-Channel

PART NUMBER	PACKAGE	g_{fs} μmho Min	I_{DSS} mA Min	Max	V_P V Min	Max	I_{GSS} nA Max	BV_{GSS} V Min	C_{iss} pF Max	C_{rss} pF Max	e_n nV/√Hz Max	COMMENTS
2N2606	TO-18	110	0.1	−0.5	0.5	4.0	1nA	30	6		3dB@1kHz	VP Min Waiver
2N2607	TO-18	330	−0.3	−1.5	1.0	4.0	3nA	30	10		400@1kHz	Low Noise/GPA
2N2608	TO-18	1000	−0.9	−4.5	1.0	4.0	10nA	30	17		180@1kHz	Low Noise/GPA
2N2609	TO-18	2500	−2.0	−10.0	1.0	4.0	30nA	30	30		180@1kHz	Low Noise/GPA
2N2609JAN	TO-18	2500	−2.0	−10.0	1.0	4.0	30nA	30	30		3dB@1kHz	Low Noise/GPA
2N3328	TO-72	100		−1.0		6.0	1nA	20	4		400@1kHZ	GPA
2N3329	TO-72	1000	−1.0	−3.0		5.0	10nA	20	20		3db@1kHz	GPA
2N3330	TO-72	1500	−2.0	−6.0		6.0	10nA	20	20		3db@1kHz	GPA
2N3331	TO-72	2000	−5.0	−15.0		8.0	10nA	20	20		4db@1kHz	GPA
2N3332	TO-72	1000	−1.0	−6.0		6.0	10nA	20	20		1db@1kHz	GPA
2N5265	TO-72	900	−0.5	−1.0	0.3	1.5	2nA	60	7	2	115@100Hz	Low Noise/GPA
2N5266	TO-72	1000	−0.8	−1.6	0.4	2.0	2nA	60	7	2	115@100Hz	Low Noise/GPA
2N5267	TO-72	1500	−1.5	−3.0	1.0	4.0	2nA	60	7	2	115@100Hz	Low Noise/GPA
2N5268	TO-72	2000	−2.5	−5.0	1.0	4.0	2nA	60	7	2	115@100Hz	Low Noise/GPA
2N5269	TO-72	2200	−4.0	−8.0	2.0	6.0	2nA	60	7	2	115@100Hz	Low Noise/GPA
2N5270	TO-72	2500	−7.0	−14.0	2.0	6.0	2nA	60	7	2	115@100Hz	Low Noise/GPA
2N5460	TO-92	1000	−1.0	−5.0	0.75	6.0	5nA	40	7	2	115@100Hz	Low Noise/Low Cost
2N5461	TO-92	1500	−2.0	−9.0	1.0	7.5	5nA	40	7	2	115@100Hz	Low Noise/Low Cost
2N5462	TO-92	2500	−4.0	−16.0	1.8	9.0	5nA	40	7	2	115@100Hz	Low Noise/Low Cost
2N5463	TO-92	1000	−1.0	−5.0	0.75	6.0	5nA	60	7	2	115@100Hz	Low Noise/Low Cost
2N5464	TO-92	1500	−2.0	−9.0	1.0	7.5	5nA	60	7	2	115 100Hz	Low Noise/Low Cost
2N5465	TO-92	2500	−4.0	−16.0	1.8	9.0	5nA	60	7	2	115@100Hz	Low Noise/Low Cost
J270	TO-92	6000	−2.0	−15.0	0.5	2.0	0.200	30	32typ	4typ	6typ@1kHZ	Low Noise/Low Cost
J271	TO-92	8000	−6.0	−50.0	1.5	4.5	0.200	30	31typ	4typ	6typ@1kHz	Low Noise/Low Cost
PN4342	TO-92	2000	−4.0	−12.0	0.7	5.0	10nA	25	20	5	80@100Hz	Low Noise/Low Cost
PN4343	TO-92	3000	−10.0	−30.0	1.8	9.0	10nA	25	20	5	80@100Hz	Low Noise/Low Cost

*Available as JAN/TX/TXV.

**Most TO-92's are available lead formed to a TO-18 or TO-5 configuration.

Differential Amplifiers — Dual Monolithic N-Channel Junction FETs

PART NUMBER	PACKAGE	V_{GS1-2} mV Max	ΔV_{GS} µV/°C Max	I_G pA Max	BV_{GSS} V Min	V_P V Min	g_{fs} mmho* Max	g_{fs} mmho* Min	I_{DSS} mA Min	I_{DSS} mA Max	e_n nV/√Hz Max	COMMENTS
2N3921	TO-71	5	10	250	−50		−3.0	1.5	1	10.0	2dB @ 1kHz	GP Diff Amp
2N3922	TO-71	5	25	250	−50		−3.0	1.5	1	10.0	2dB @ 1kHz	GP Diff Amp
2N3954	TO-71	5	10	−50	−50	−1.0	−4.5	1	0.5	5.0	160 @ 100Hz	General Purpose
2N3954A	TO-71	5	5	−50	−50	−1.0	−4.5	1	0.5	5.0	160 @ 100Hz	General Purpose
2N3955	TO-71	10	25	−50	−50	−1.0	−4.5	1	0.5	5.0	160 @ 100Hz	General Purpose
2N3955A	TO-71	5	15	−50	−50	−1.0	−4.5	1	0.5	5.0	160 @ 100Hz	General Purpose
2N3956	TO-71	15	50	−50	−50	−1.0	−4.5	1	0.5	5.0	160 @ 100Hz	General Purpose
2N3957	TO-71	20	75	−50	−50	−1.0	−4.5	1	0.5	5.0	160 @ 100Hz	General Purpose
2N3958	TO-71	25	100	−50	−50	−1.0	−4.5	1	0.5	5.0	160 @ 100Hz	General Purpose
2N5045	TO-71	5	65		−50	−0.5	−4.5	1.5	6.0	0.5	8.0	200 @ 10Hz	GP Diff Amp
2N5046	TO-71	10	133		−50	−0.5	−4.5	1.5	6.0	0.5	8.0	200 @ 10Hz	GP Diff Amp
2N5047	TO-71	15	200		−50	−0.5	−4.5	1.5	6.0	0.5	8.0		GP Diff Amp
2N5196	TO-71	5	5	−15	−50	−0.7	−4.0	0.7 @ 200µA		0.7	7.0	20 @ 1kHz	Low Noise, GPA
2N5197	TO-71	5	10	−15	−50	−0.7	−4.0	0.7 @ 200µA		0.7	7.0	20 @ 1kHz	Low Noise, GPA
2N5198	TO-71	10	20	−15	−50	−0.7	−4.0	0.7 @ 200µA		0.7	7.0	20 @ 1kHz	Low Noise, GPA
2N5199	TO-71	15	40	−15	−50	−0.7	−4.0	0.7 @ 200µA		0.7	7.0	20 @ 1kHz	Low Noise, GPA
2N5515	TO-71	5	5	−100	−40	−0.7	−4.0	1	4	0.5	7.5	30 @ 10Hz	GP Diff Amp
2N5516	TO-71	5	10	−100	−40	−0.7	−4.0	1	4	0.5	7.5	30 @ 10Hz	GP Diff Amp
2N5517	TO-71	10	20	−100	−40	−0.7	−4.0	1	4	0.5	7.5	30 @ 10Hz	GP Diff Amp
2N5518	TO-71	15	40	−100	−40	−0.7	−4.0	1	4	0.5	7.5	30 @ 10Hz	GP Diff Amp
2N5519	TO-71	15	80	−100	−40	−0.7	−4.0	1	4	0.5	7.5	30 @ 10Hz	GP Diff Amp
2N5520	TO-71	5	5	−100	−40	−0.7	−4.0	1	4	0.5	7.5	15 @ 10Hz	Lowest Noise
2N5521	TO-71	5	10	−100	−40	−0.7	−4.0	1	4	0.5	7.5	15 @ 10Hz	Lowest Noise
2N5522	TO-71	10	20	−100	−40	−0.7	−4.0	1	4	0.5	7.5	15 @ 10Hz	Lowest Noise
2N5523	TO-71	15	40	−100	−40	−0.7	−4.0	1	4	0.5	7.5	15 @ 10Hz	Lowest Noise
2N5524	TO-71	15	80	−100	−40	−0.7	−4.0	1	4	0.5	7.5	15 @ 10Hz	Lowest Noise
2N5545	TO-71	5	10	−50	−50	−0.5	−4.5	1.5	6	0.5	8.0	180 @ 10Hz	GP Diff Amp
2N5546	TO-71	10	20	−50	−50	−0.5	−4.5	1.5	6	0.5	8.0	200 @ 10Hz	GP Diff Amp
2N5547	TO-71	15	40	−50	−50	−0.5	−4.5	1.5	6	0.5	8.0		GP Diff Amp
2N5902	TO-78	5	5	−3	−40	−0.6	−4.5	0.07	.250	0.03	0.50	100 @ 1kHz	Low Leakage
2N5903	TO-78	5	10	−3	−40	−0.6	−4.5	0.07	.250	0.03	0.50	100 @ 1kHz	Low Leakage
2N5904	TO-78	10	20	−3	−40	−0.6	−4.5	0.07	.250	0.03	0.50	100 @ 1kHz	Low Leakage
2N5905	TO-78	15	40	−3	−40	−0.6	−4.5	0.07	.250	0.03	0.50	100 @ 1kHz	Low Leakage
2N5906	TO-99	5	5	−1	−40	−0.6	−4.5	0.07	0.25	0.03	0.50	100 @ 1kHz	Low Leakage
2N5907	TO-99	5	10	−1	−40	−0.6	−4.5	0.07	0.25	0.03	0.50	100 @ 1kHz	Low Leakage
2N5908	TO-99	10	20	−1	−40	−0.6	−4.5	0.07	0.25	0.03	0.50	100 @ 1kHz	Low Leakage
2N5909	TO-99	15	40	−1	−40	−0.6	−4.5	0.07	0.25	0.03	0.50	100 @ 1kHz	Low Leakage
2N5911	TO-99	10	20	−100	−25	−1.0	−5.0	5/10 @ 5mA		7.0	40.0	20 @ 10kHz	RF Amplifier
2N5912	TO-99	15	40	−100	−25	−1.0	−5.0	5/10 @ 5mA		7.0	40.0	20 @ 10kHz	RF Amplifier
2N6483	TO-71	5	5	−100	−50	−0.7	−4.0	1	4	0.5	7.5	10 @ 10Hz	Low Noise
2N6484	TO-71	10	10	−100	−50	−0.7	−4.0	1	4	0.5	7.5	10 @ 10Hz	Low Noise
2N6485	TO-71	15	25	−100	−50	−0.7	−4.0	1	4	0.5	7.5	10 @ 10Hz	Low Noise
IT500	TO-52	5	5	−5	−50	−0.7	−4.0	0.7/1.6 @ 200µA		0.7	7.0	35 @ 10Hz	Cascode RF Amp
IT501	TO-52	5	10	−5	−50	−0.7	−4.0	0.7/1.6 @ 200µA		0.7	7.0	35 @ 10Hz	Cascode RF Amp
IT502	TO-52	10	20	−5	−50	−0.7	−4.0	0.7/1.6 @ 200µA		0.7	7.0	35 @ 10Hz	Cascode RF Amp
IT503	TO-52	15	40	−5	−50	−0.7	−4.0	0.7/1.6 @ 200µA		0.7	7.0	35 @ 10Hz	Cascode RF Amp
IT504	TO-52	25	100	−5	−25	−0.7	−4.0	0.7/1.6 @ 200µA		0.7	7.0	35 @ 10Hz	Cascode RF Amp
IT505	TO-52	50	200	−5	−25	−0.7	−4.0	0.7/1.6 @ 200µA		0.7	7.0	35 @ 10Hz	Cascode RF Amp

*@I_{DSS}

Differential Amplifiers — continued
Dual Monolithic N-Channel Junction FETs

PART NUMBER	PACKAGE	V_{GS1-2} mV Max	ΔV_{GS} µV/°C Max	I_G pA Max	BV_{GSS} V Min	V_P V Min	Max	g_{fs} mmho* Min	Max	I_{DSS} mA Min	Max	e_n nV/√Hz Max	COMMENTS
IT550	TO-71	50	100		−40	−0.5	−3.0	7.5/12.5 @ 2mA		5.0	30.0	50 @ 10Hz	Cascode RF Amp
IT5911	TO-71	10	20	−100	−25	−1.0	−5.0	5/10 @ 5mA		7.0	40.0	20 @ 10kHz	RF Amplifier
IT5912	TO-71	15	40	−100	−25	−1.0	−5.0	5/10 @ 5mA		7.0	40.0	20 @ 10kHz	RF Amplifier
ITC5911	TO-99	10	20	−100	−25	−1.0	−5.0	5/10 @ 5mA		7.0	40.0	20 @ 10kHz	RF Amplifier
ITC5912	TO-99	15	40	−100	−25	−1.0	−5.0	5/10 @ 5mA		7.0	40.0	20 @ 10kHz	RF Amplifier
U231	TO-71	5	10	−50	−50	−0.5	−4.5	1	5	0.5	5.0	80 @ 100Hz	GP Diff Amp
U232	TO-71	10	25	−50	−50	−0.5	−4.5	1	5	0.5	5.0	80 @ 100Hz	GP Diff Amp
U233	TO-71	15	50	−50	−50	−0.5	−4.5	1	5	0.5	5.0	80 @ 100Hz	GP Diff Amp
U234	TO-71	20	75	−50	−50	−0.5	−4.5	1	5	0.5	5.0	80 @ 100Hz	GP Diff Amp
U235	TO-71	25	100	−50	−50	−0.5	−4.5	1	5	0.5	5.0	80 @ 100Hz	GP Diff Amp
U257	TO-78	100			−25	−1.0	−5.0	4.5	10	5.0	40.0	30 @ 10kHz	Low Cost
U426	TO-78	25	40	−0.5	−40	−0.4	−3.0	0.3	1.5	.06	1.8	70 @ 10Hz	Low Cost
U440	TO-71	10			−25	−1.0	−6.0	4.5/9 @ 5µA		6	30		High Gain
U441	TO-71	20			−25	−1.0	−6.0	4.5/9 @ 5µA		6	30		High Gain

Dual Monolithic P-Channel MOSFETs (Enhancement)

PART NUMBER	PACKAGE	$V_{GS(TH)}$ V Min	Max	BV_{DDS} V Min/Max	I_{DSS} pA Max	I_{GSS} pA Max	g_{fs} µmho Min	$I_{D(ON)}$ mA Min	Max	$r_{DS(ON)}$ Ω Max	$V_{GS\ 1-2}$ mV Max	COMMENTS
3N165	TO-99	−2	−5	−40	−200	−10	1500	−5.0	−30	300	100	Low Leakage
3N166	TO-99	−2	−5	−40	−200	−10	1500	−5.0	−30	300		Low Leakage
3N188	TO-99	−2	−5	−40	−200	−200	1500	−5.0	−30	300	100	Diode Protected
3N189	TO-99	−2	−5	−40	−200	−200	1500	−5.0	−30	300		Diode Protected
3N190	TO-99	−2	−5	−40	−200	−10	1500	−5.0	−30	300	100	High Input Z
3N191	TO-99	−2	−5	−40	−200	−10	1500	−5.0	−30	300		High Input Z

*@I_{DSS}

Differential Amplifiers — Dual NPN Bipolar Transistors

PART NUMBER	PACKAGE	$V_{BE\ 1\text{-}2}$ mV Max	ΔV_{BE} μV/°C Max	h_{FE} (Note 1) Min	$I_{B1\text{-}2}$ (Note 1) nA Max	BV_{CEO} V Min	I_{CBO} nA Max	NF dB Max	f_t MHz @ I_C Min	C_{obo} pF Max	COMMENTS
2N2453	TO-78	3	10	80		30	5	7 typ.			Audio Amp
2N2453A	TO-78	3	5	80		60	5	4 typ.			Audio Amp
2N2920	TO-78	3	10	150		60	2	3 typ.	60 @ 0.5mA	6	High Gain, Low Noise
2N2920A	TO-78	1.5	5	150		60	2	3 typ.	60 @ 0.5mA	6	High Gain, Low Noise
2N4044	TO-78	3	3	200	5	60	0.1	2	200 @ 1mA	0.8	Low Capacitance
2N4045	TO-78	5	10	80	25	45	0.1	3	150 @ 1mA	0.8	Low Capacitance
2N4100	TO-78	5	5	150	10	55	0.1	3	150 @ 1mA	0.8	Low Capacitance
2N4878	TO-71	3	3	200	5	60	0.1	2 typ.	200 @ 1mA	0.8	Low Capacitance
2N4879	TO-71	5	5	150	10	55	0.1	3 typ.	150 @ 1mA	0.8	Low Capacitance
2N4880	TO-71	5	10	80	25	45	0.1	3 typ.	150 @ 1mA	0.8	Low Capacitance
IT120	TO-78 TO-71	2	5	200	5	45	1.0	2 typ.	150 @ 1mA	2	Low Cost, Low V_{OS}
IT120A	TO-78 TO-71	1	3	200	2.5	45	1.0	2 typ.	150 @ 1mA	2	Low Cost, Low V_{OS}
IT121	TO-78 TO-71	3	10	80	25	45	1.0	2 typ.	180 @ 1mA	2	Low Cost
IT122	TO-78 TO-71	5	20	80	25	45	1.0	2 typ.	180 @ 1mA	2	Low Cost
IT124	TO-78	5	15	1500	0.6A	2	0.1	3	100 @ 100μA	0.8	Super β for Log Amps
IT126	TO-78 TO-71	1	3	150	2.5	60	0.1	1 typ.	250 @ 10mA	3	Low V_{OS}
IT127	TO-78 TO-71	2	5	150	5	60	0.1	1 typ.	250 @ 10mA	3	Low V_{OS}
IT128	TO-78 TO-71	3	10	100	10	55	0.1	1 typ.	250 @ 10mA	3	Low V_{OS}
IT129	TO-78 TO-71	10	20	70	20	45	0.1	1 typ.	250 @ 10mA	3	Low V_{OS}
LM114	TO-71	2.0	10	250	10	45	0.050				Low V_{OS}
LM114A	TO-71	0.5	2	500	2	45	0.010				Low V_{OS}
LM114AH	TO-78	0.5	2	500	2	45	0.010				Low V_{OS}
LM114B	TO-71	1.0	5	250	10	45	0.050				Low V_{OS}
LM114BH	TO-78	1.0	5	250	10	45	0.050				Low V_{OS}
LM114H	TO-78	2.0	10	250	10	45	0.050				Low V_{OS}

NOTE:

1. I_C = 10μA

Differential Amplifiers — Dual PNP Bipolar Transistors

PART NUMBER	PACKAGE	$V_{BE\ 1\text{-}2}$ mV Max	ΔV_{BE} µV/°C Max	h_{FE} (Note 1) Min	$I_{B1\text{-}2}$ (Note 1) nA Max	BV_{CEO} V Min	I_{CBO} nA Max	NF dB Max	f_t MHz @ I_C Min	C_{obo} pF Max	COMMENTS
2N3810	TO-78	3	10	100		−60	10	3 typ.	100 @ 1mA	4	Low V_{OS}
2N3810A	TO-78	1.5	5	100		−60	10	3 typ.	100 @ 1mA	4	Low V_{OS}
2N3811	TO-78	3	10	225		−60	10	3 typ.	100 @ 1mA	4	Low V_{OS}
2N3811A	TO-78	1.5	5	225		−60	10	3 typ.	100 @ 1mA	4	Low V_{OS}
2N5117	TO-78	3	3	100	10	−45	0.1	4 typ.	100 @ 0.5mA	0.8	Low V_{OS}
2N5118	TO-78	5	5	100	15	−45	0.1	4 typ.	100 @ 0.5mA	0.8	Low Cost
2N5119	TO-78	5	10	50	40	−45	0.1	4 typ.	100 @ 0.5mA	0.8	Low Cost
IT130	TO-78 TO-71	2	5	200	5	−45	1.0	2 typ.	150 @ 1mA	2	Low V_{OS}
IT130A	TO-78 TO-71	1	3	200	2.5	−45	1.0	2 typ.	150 @ 1mA	2	Low V_{OS}
IT131	TO-78 TO-71	3	10	80	25	−45	1.0	2 typ.	150 @ 1mA	2	Low Cost
IT132	TO-78 TO-71	5	20	80	25	−45	1.0	2 typ.	150 @ 1mA	2	Low Cost
IT136	TO-78 TO-71	1	3	150	2.5	−60	0.1	2 typ.	250 @ 10mA	4	Low V_{OS}
IT137	TO-78 TO-71	2	5	150	5	−60	0.1	2 typ.	250 @ 10mA	4	Low V_{OS}
IT138	TO-78 TO-71	3	10	100	10	−55	0.1	2 typ.	250 @ 10mA	4	Low V_{OS}
IT139	TO-78 TO-71	5	20	70	20	−45	0.1	2 typ.	250 @ 10mA	4	Low V_{OS}

Note:

1. $I_C = 10\mu A$, $V_{CE} = 5V$

General Purpose Analog Switch Selector Guide

SWITCH FAMILY	SPECIAL FEATURES	SWITCH TYPE	SWITCH PARAMETERS				
			$R_{DS(ON)}$ (Ω Max)	$I_{D(OFF)}$ (nA Max)	t_{ON} (ns Max)	t_{OFF} (ns Max)	ANALOG VOLTAGE RANGE (V_{SUPPLY} = ±15V)
DG118-125	Inverting/non-inverting logic inputs	PMOS	600 600	4 4	300 300	1000 1000	—
DG126-54 DG139-164	SPST/DPST SPDT/DPDT switch capability, low $R_{DS(ON)}$ TTL compatible	N-JFET	10 15 30 50 80	10 10 1 1 1	1000 1000 600 600 600	2500 2500 1600 1600 1600	—
DG180-191	Mature, industry-standard switch, low $R_{DS(ON)}$	N-JFET	10 30 75	10 1 1	300 150 250	250 130 130	−7.5 to +15 −7.5 to +15 −10 to +15
DGM181-191	Monolithic replacement for DG180 family	CMOS	50 75	2.0 0.5	250 450	200 250	−15 to +15 −15 to +15
DG200/201 IH5200/5201	Industry-standard low cost	CMOS	70/80 70/80	2.0 0.05	1000 700	500 250	−15 to +15 −15 to +15
DG211 * DG212 *	Low leakage, inverting logic inputs	CMOS	175	5.0	1000	500	−15 to +15
IH5025-38	Low cost, low leakage. O.C. TTL compatible	P-JFET	100 150 100 150	0.5 0.5 0.5 0.5	200 200 200 200	200 200 200 200	0 to +20 0 to +20 0 to +20 0 to +20
IH5040-53	Low quiescent current Low $R_{DS(ON)}$	CMOS	35 75	1.0 1.0	250 500	150 250	−15 to +15 −15 to +15
IH5140-45	High speed, low power, low leakage	CMOS	50	0.05	100-200	75-125	−15 to +14
IH5148-51 *	Low $R_{DS(ON)}$, high speed, low power	CMOS	25	0.05	250-500	200-250	−14 to +14
IH6201/ IH401/A	TTL level translator/low charge injection switch	N-JFET	30-50	0.05	456		—

*New Product

General Purpose Analog Switch Selector Guide. (Continued)

SWITCH CONFIGURATION										
SPST	DUAL SPST	TRIPLE SPST	QUAD SPST	FIVE SPST	SPDT	DUAL SPDT	DPST	DUAL DPST	DPDT	4PST
			DG118	DG123 DG125						
	DG141 DG151 DG133 DG152 DG134				DG146 DG161 DG144 DG162 DG143			DG140 DG153 DG129 DG154 DG126	DG145 DG163 DG139 DG164 DG142	
	DG180 DG181 DG182				DG186 DG187 DG188	DG189 DG190 DG191		DG183 DG184 DG185		
	DGM182				DGM187 DGM188	DGM190 DGM191		DGM184 DGM185		
	DG200 IH5200		DG201 IH5201							
			DG211 DG212							
IH5037 IH5038	IH5033 IH5034 IH5035 IH5036	IH5029 IH5030 IH5031 IH5032	IH5025 IH5026 IH5027 IH5028							
IH5040	IH5048 IH5041		IH5052 IH5053		IH5042	IH5051 IH5043	IH5044	IH5049 IH5045	IH5046	IH5047
IH5140	IH5141				IH5142	IH5143	IH5144	IH5145		
	IH5148				IH5150	IH5151		IH5149		
			IH401 IH401A							

Special Purpose Analog Switch

SWITCH FAMILY	SPECIAL FEATURES	SWITCH TYPE	$r_{DS(ON)}$ (Ω Max)	$I_{D(OFF)}$ (nA Max)	t_{ON} (ns Max)	t_{OFF} (ns Max)	ANALOG VOLTAGE RANGE (V_{SUPPLY} = ±15V)	SWITCH CONFIGURATION			
								SPST	DUAL SPST	TRIPLE SPST	QUAD SPST
IH5009-24	Lowest cost; virtual ground switch	P-JFET	100	0.2	500	500	−0.2 to +0.2	IH5021	IH5017	IH5013	IH5009
			150	0.2	500	500	−0.2 to +0.2	IH5022	IH5018	IH5014	IH5010
			100	0.2	500	500	−0.2 to +0.2	IH5023	IH5019	IH5015	IH5011
			150	0.2	500	500	−0.2 to +0.2	IH5024	IH5020	IH5016	IH5012
IH5341/52*	Video Switch, off-isolation 60 dB (10 MHz)	CMOS	75	1.0	300	150	−15 to +15		IH5341		*IH5352

* New Product

Multiplexers

SWITCH FAMILY	SPECIAL FEATURES	$r_{DS(ON)}$ (Ω Max)	$I_{D(OFF)}$ (nA Max)	t_{ON} (ns Max)	t_{OFF} (ns Max)	ANALOG VOLTAGE RANGE V_{SUPPLY} = (±15V)	CONFIGURATION			
							8-CHANNEL SINGLE-ENDED	4-CHANNEL DIFFER-ENTIAL	16-CHANNEL SINGLE-ENDED	8-CHANNEL DIFFER-ENITAL
IH5108	Industry standard pinouts, fault protection up to ±25V input, low leakage, low input current	900	1.0	1500	1000	−25 to +25 (Input)	IH5108	IH5208		
		1000	1.0	1500	1000	−25 to +25 (Input)			*IH5116	*IH5216
IH6108	Industrial standard pinouts, low leakage, low $R_{DS(ON)}$ break before make switching	300	1.0	1500	1000	−14 to +14	IH6108	IH6208		
		600	1.0	1500	1000	−14 to +14			IH6116	IH6216

Drivers for JFET Switches

TYPE	NUMBER OF CHANNELS	OUTPUT SWING		t_{ON} (ns Max)	t_{OFF} (ns Max)	I_{INL} (μA Max)	I_{INH} (μA Max)	LOGIC INPUT LEVEL	POWER CONSUM-(mW)
		POSITIVE (V Max)	NEGATIVE (V Max)						
D123	6	V_{SUPPLY}	−19.7	250	400-800	1.0	1.0	TTL/DTL	20
D125	6	V_{SUPPLY}	−19.7	250	400-800	700	1.0	TTL	50
D129	4	V_{SUPPLY}	−19.3	250	1000	200	0.25	TTL/DTL	55
IH6201	2	+14.0	−14.0	200	300	1.0	1.0	TTL	350

Operational Amplifiers: Low Power

	TYPE	DESCRIPTION	$I_{QUIESCENT}$ (Per Channel) (μA Typ)	V_{SUPPLY} (V Max)	V_{OS} (mV Max)	I_{BIAS} (nA Max)	GBW (MHz)	COMPEN-SATION	TEMPERATURE RANGE (°C)
SINGLES	ICL7611	CMOS, Selectable I_Q	10	±9	2, 5, 15	0.05	0.044	INT	0 to +70 & −55 to +125
	ICL7612	CMOS, Extended CMVR	10	±9	2, 5, 15	0.05	0.044	INT	
	ICL7613	CMOS, Input Protected	10	±9	2, 5, 15	0.05	0.044	INT	
	ICL8021M	Bipolar, Selectable IQ	30	±18	3	20	0.27	INT	−55 to +125
	ICL8021C	Bipolar, Selectable I_Q	30	±18	6	30	0.27	INT	0 to +70
DUALS	ICL8022M	Dual 8021M	30	±18	3	20	0.27	INT	−55 to +125
	ICL8022C	Dual 8021C	30	±18	6	30	0.27	INT	0 to +70
TRIPLES	ICL7631	CMOS, Selectable I_Q	10	±9	5, 10, 20	0.05	0.044	INT	0 to +70 & −55 to +125
	ICL7632	CMOS, Selectable I_Q	10	±9	5, 10, 20	0.05	0.044	NONE	
	ICL8023M	Triple 8021M	30	±18	3	20	0.27	INT	−55 to +125
	ICL8023C	Triple 8021C	30	±18	6	30	0.27	INT	0 to +70
QUADS	ICL7642	CMOS, Fixed I_Q	10	±9	5, 10, 20	0.05	0.044	INT	0 to +70 & −55 to +125

Operational Amplifiers: General Purpose

	TYPE	DESCRIPTION	V_{OS} (mV Max)	I_{BIAS} (pA Max)	SLEW RATE (V/μs)	GBW (MHz)	COMPEN-SATION	V_{SUPPLY} (V Max)	TEMPERATURE RANGE (°C)
SINGLES	LM108	Bipolar, Super-Beta	2.0	2000	—	1.0	EXT	±20	−55 to +125
	LM308	Bipolar, Super-Beta	7.5	7000	—	1.0	EXT	±18	0 to +70
	ICL7611	CMOS, Selectable I_Q	2, 5, 15	50	1.6	1.4	INT	±9	0 to +70 & −55 to +125
	ICL8007M	JFET Input Op-Amp	20	20	6	1.0	INT	±18	−55 to +125
	ICL8007C	JFET Input Op-Amp	50	50	6	1.0	INT	±18	0 to +70
DUALS	LH2108	Bipolar, Super-Beta	2.0	2000	—	1.0	EXT	±20	−55 to +125
	LH2308	Bipolar, Super-Beta	7.5	7000	—	1.0	EXT	±18	0 to +70
	ICL7621	CMOS, Fixed I_Q	2, 5, 15	50	0.16	0.48	INT	±9	0 to +70 & −55 to +125
	ICL8043M	JFET Input Op-Amp	20	20	6	1.0	INT	±18	−55 to +125
	ICL8043C	JFET Input Op-Amp	50	50	6	1.0	INT	±18	0 to +70
TRIPLES	ICL7631	CMOS, Selectable I_Q	5, 10, 20	50	1.6	1.4	INT	±9	0 to +70 & −55 to +125
QUADS	ICL7641	CMOS, Fixed I_Q	5, 10, 20	50	1.6	1.4	INT	±9	0 to +70 & −55 to +125

Operational Amplifiers: High Output Current

	TYPE	DESCRIPTION	I_{OUT} (A Min)	V_{OUT} (V Min)	V_{SUPPLY} (V Max)	V_{OS} (mV Max)	I_{BIAS} (nA Max)	A_{VOL} (dB Typ)	TEMPRATURE RANGE (°C)
SINGLES	ICH8510M	Hybrid Amplifier	1.0	±26	±32	3.0	250	100	−55 to +125
	ICH8510I	Hybrid Amplifier	1.0	±26	±32	6.0	250	100	−25 to +85
	ICH8515M	Hybrid Amplifier	1.5	±12	±18	3.0	250	100	−55 to +125
	ICH8515I	Hybrid Amplifier	1.25	±12	±18	6.0	50	100	−25 to +85
	ICH8520M	Hybrid Amplifier	2.0	±26	±32	3.0	250	100	−55 to +125
	ICH8502I	Hybrid Amplifier	2.0	±26	±32	6.0	500	100	−25 to +85
	ICH8530M	Hybrid Amplifier	2.7	±25	±32	3.0	250	100	−55 to +125
	ICH8530I	Hybrid Amplifier	2.7	±25	±32	6.0	500	100	−25 to +85

Operational Amplifiers: Low/Ultra-low Input Offset Voltage

	TYPE	DESCRIPTION	V_{OS} (μV Max)	$\Delta Vos/\Delta T$ (μV/°C) (Max)	$\Delta Vos/\Delta t$ (nV/month) (Typ)	I_{BIAS} (pA Max)	GBW (MHz)	V_{SUPPLY} (V Max)	TEMPERATURE RANGE (°C)
SINGLES	ICL7650C	CMOS, Chopper-stabilized	±5	±0.05	100	10	2.0	±9	0 to +70
	ICL7650I		±5	±0.05	100	10	2.0	±9	−25 to +85
	ICL7650M	CMOS, Chopper-stabilized	±5	±0.05	100	10	2.0	±9	−55 to +125
	ICL7652C	Low-noise 7650C	±5	±0.05	100	30	2.0	±9	0 to +70
	ICL7652I	Low-noise 7650I	±5	±0.05	100	30	2.0	±9	−25 to +85
	LM108A	Bipolar, Super-Beta	500	5.0	—	2000	1.0	±20	−55 to +125
	LM308A	Bipolar, Super-Beta	500	5.0	—	7000	1.0	±18	0 to +70
DUALS	LH2108A	Bipolar, Super-Beta	500	5.0	—	2000	1.0	±20	−55 to +125
	LH2308A	Bipolar, Super-Beta	500	5.0	—	7000	1.0	±20	0 to +70

Operational Amplifiers: Low Input Bias Current

	TYPE	DESCRIPTION	I_{BIAS} (pA Max)	I_{OS} (pA Typ)	V_{OS} (mV Max)	GBW (MHz)	COMPEN-SATION	V_{SUPPLY} (V Max)	TEMPERATURE RANGE (°C)
SINGLES	ICL7611	CMOS, Selectable I_Q	50	0.5	2, 5, 15	1.4	INT	±9	0 to +70 & −55 to +125
	ICL7612	CMOS, Extended CMVR	50	0.5	2, 5, 15	1.4	INT	±9	
	ICL7613	CMOS, Input Protected	50	0.5	2, 5, 15	1.4	INT	±9	
	ICL7614	CMOS, Fixed I_Q	50	0.5	2, 5, 15	0.48	EXT	±9	
	ICL7615	CMOS, Input Protected	50	0.5	2, 5, 15	0.48	EXT	±9	
	ICL8007M	JFET Input Op-Amp	20	0.5	20	1.0	INT	±18	−55 to +125
	ICL8007AM	JFET Input, Low Bias	4.0	0.2	30	1.0	INT	±18	−55 to +125
	ICL8007C	JFET Input Op-Amp	50	0.5	50	1.0	INT	±18	0 to +70
	ICL8007AC	JFET Input, Low Bias	4.0	0.2	30	1.0	INT	±18	0 to +70
	ICH8500	PMOS Input	0.1	—	50	0.7	INT	±18	−25 to +85
	ICH8500A	PMOS Input, Low Bias	0.01	—	50	0.7	INT	±18	−25 to +85
DUALS	ICL7621	CMOS, Fixed I_Q	50	0.5	2, 5, 15	0.48	INT	±9	0 to +70 & −55 to +125
	ICL7622	CMOS, Offset Null Pins	50	0.5	2, 5, 15	0.48	INT	±9	
	ICL8043M	JFET Input Op-Amp	20	0.5	20	1.0	INT	±18	−55 to +125
	ICL8043C	JFET Input Op-Amp	50	0.5	50	1.0	INT	±18	0 to +70
TRIPLES	ICL7631	CMOS, Selectable I_Q	50	0.5	5, 10, 20	1.4	INT	±9	0 to +70 & −55 to +125
	ICL7632	CMOS, Selectable I_Q	50	0.5	5, 10, 20	1.4	NONE	±9	
QUADS	ICL7641	CMOS, Fixed I_Q	50	0.5	5, 10, 20	1.4	INT	±9	0 to +70 & −55 to +125
	ICL7642	CMOS, Fixed I_Q	50	0.5	5, 10, 20	0.044	INT	±9	

Commutating Auto-Zero (CAZ) Instrumentation Amplifiers

TYPE	DESCRIPTION	V_{OS} (μV Max)	$\Delta Vos/\Delta T$ (μV/°C) (Max)	$\Delta Vos/\Delta t$ (nV/month) (Typ)	I_{BIAS} (pA Max)	SIGNAL BANDWIDTH (Hz Max)	A_{VOL} (dB Typ)	TEMPERATURE RANGE (°C)
ICL7605C	CMOS, Compensated	5.0	0.2	40	1500	10	105	0 to +70
ICL7605I	CMOS, Compensated	5.0	0.2	40	1500	10	105	−25 to +85
ICL7605M	CMOS, Compensated	5.0	0.2	40	1500	10	105	−55 to +125
ICL7606C	CMOS, Uncompensated	5.0	0.2	40	1500	10	105	0 to +70
ICL7606I	CMOS, Uncompensated	5.0	0.2	40	1500	10	105	−25 to +85
ICL7606M	CMOS, Uncompensated	5.0	0.2	40	1500	10	105	−55 to +125

Log/Antilog Amplifiers

TYPE	DESCRIPTION	ABSOLUTE ERROR (mV Max)	V_{OS} (mV Max)	$\Delta Vout/\Delta T$ (mV/°C) (Typ)	DYNAMIC RANGE (dB)	OUTPUT SWING (V Typ)	V_{SUPPLY} (V Max)	TEMPERATURE RANGE (°C)
ICL8048BC	Logarithmic Amplifier,	30	25	0.8	120	±14	±18	0 to +70
ICL8048CC	1V/Decade Output	60	50	0.8	120	±14	±18	0 to +70
ICL8049BC	Antilog Amplifier	10	25	0.38	60	±14	±18	0 to +70
ICL8049CC	1V/Decade Input	25	50	0.55	60	±14	±18	0 to +70

Power Transistor Drive Amplifiers

TYPE	DESCRIPTION	I_{OUT} (mA Min)	V_{OUT} (V Min)	V_{OS} (mV Max)	A_{VOL} (V/V)	SUPPLY CURRENT (mA Max)	V_{SUPPLY} (V Max)	TEMPERATURE RANGE (°C)
ICL8063M	Bipolar Monolithic	+50/−25	±27V	50	6	6	±35	−55 to +125
ICL8063C	Driver Amplifier	+40/−20	±27V	75	6	7	±35	0 to +70

Video Amplifiers

TYPE	DESCRIPTION	A_V (V/V)	SIGNAL BANDWIDTH (MHz)	V_{oo} (V Max)	I_{BIAS} (μA Max)	$\overline{e}_n$ (μV RMS)	V_{SUPPLY} (V Max)	TEMPERATURE RANGE (°C)
NE592	Bipolar, Programmable	100/400	90/40	0.75	30	12	±8	0 to +70
SE592	gain amplifier	100/400	90/40	0.75	20	12	±8	−55 to +125

Power Supply Circuits (CMOS)

TYPE	FUNCTION	DESCRIPTION	TEMPERATURE RANGE (°C)
ICL7660	Voltage Converter	The ICL7660 performs supply voltage conversion from positive to negative. Input range is +1.5V to +10V resulting in complementary output voltages of −1.5V to −10V.	0 to +70 −55 to +125
ICL7662*	Voltage Converter	This device is similar to the ICL7660 in its operation, except the input voltage range extends from +4.5V to +20.0V.	0 to +70 −55 to +125
ICL7663	Positive Voltage Regulator	The ICL7663 is a low-power, high-efficiency device ($I_Q = 4\mu A$ max) that accepts an input of 1 to 10V, and provides an adjustable output of 1 to 10V at up to 40mA load.	0 to +70
ICL7664	Negative Voltage Regulator	The ICL7664 is similar in operation to the ICL7663, except that it accepts an input of −1 to −10V and provides an adjustable output of −1 to −10V at up to −40mA load.	0 to +70
ICL7673*	Automatic Battery-Backup Switch	The ICL7673 automatically switches between a main power supply (eg. +5V) and a battery backup supply, when the main supply is removed. Load current is 0 to 38mA.	0 to +70 −25 to +85

*New Product

Sample and Hold Circuits

TYPE	DESCRIPTION	V_{INPUT} (V Max)	ACQUISITION TIME (μs)	CHARGE INJECTION ERROR (mV)	V_{OS} (mV)	DRIFT RATE (mV/sec)	V_{SUPPLY} (V Max)	TEMPERATURE RANGE (°C)
IH5110	General purpose	±7.5	6	5	40	5	±16V	−25 to +85 & −55 to +125
IH5111	Sample/Hold Circuit,	±10.5	6	5	40	5	±16V	
IH5112	TTL Compatible	±7.5	6	5	10	5	±16V	
IH5113	Hold Input	±10.0	6	5	10	5	±16V	
IH5114		±7.5	6	5	5	5	±16V	
IH5115		±10.0	6	5	5	5	±16V	

Temperature Transducers

TYPE	DESCRIPTION	ACCURACY (°C)	V_{SUPPLY} (V)	TEMPERATURE RANGE (°C)
AD590I	The AD590 is a 2-wire,	±10	4 to 30	−55 to +150
AD590J	current-output	±5.0	4 to 30	−55 to +150
AD590K	temperature transducer.	±2.5	4 to 30	−55 to +150
AD590L	Output current	±1.0	4 to 30	−55 to +150
AD590M	varies linearly at 1μA/°K.	±0.5	4 to 30	−55 to +150

Voltage References and Detectors

TYPE	FUNCTION	DESCRIPTION	TEMPERATURE RANGE (°C)
ICL7665	Programmable Micropower Voltage Detector	Contains two individually programmable voltage comparators, and requires only 3μA supply current. Intended for battery operated systems that require low or high voltage warnings etc. Open drain outputs for interfacing.	0 to +70
ICL8069	Low Voltage Reference	A 1.20V temperature compensated bandgap voltage reference. It achieves excellent stability and low noise at currents as low as 50μA.	0 to +70 −55 to +125
ICL8211	Programmable Voltage Detector	The ICL8211 is a micropower voltage detector. It contains a 1.15V reference, a comparator, a hysteresis output and a non-inverting main-output.	0 to +70 −55 to +125
ICL8212	Programmable Voltage Detector	The ICL8212 is similar in operation to the ICL8211 except that its main output is inverting as opposed to non-inverting.	0 to +70 −55 to +125

Miscellaneous Circuits

TYPE	FUNCTION	DESCRIPTION	TEMPERATURE RANGE (°C)
ICM7206	CMOS Touch Tone* Encoder	The ICM7206 is a 2-of-8 sine wave DTMF generator for use in telephone dialing systems. Requires a 3.58 MHz crystal & will work with 3 x 4 or 4 x 4 keypads.	−40 to +85
ICL7667	Dual Power MOSFET Driver	The ICL7667 is a TTL-compatible high-speed CMOS driver designed to provide high output current (1.5A) and voltage (up to +15V) for driving the gates of power MOSFETs.	0 to +70 −55 to +125
ICL8013	4-Quadrant Analog Multiplier	The ICL8013 is a bipolar 4-quadrant multiplier. The output is proportional to the product of two input voltages. An internal op-amp is included for level shifting.	0 to +70 −55 to +125
ICL8038	Precision Waveform Generator	The ICL8038 is a bipolar function generator and is capable of producing high accuracy sine, square and triangular waveforms. Frequency range is 0.001 Hz to 300 kHz.	0 to +70 −55 to +125

*New Product

Integrating Analog-to-Digital Converters with Display Drivers (CMOS)

	TYPE	ACCURACY SPECIAL FEATURES	DISPLAY TYPE	CONVERSIONS/SEC	INPUT VOLTAGE RANGES	NON LINEARITY	ROLLOVER ERROR	STABILITY ZERO INPUT DRIFT	SUPPLY V_{SUPPLY}/ I_{SUPPLY}	TEMP RANGE (°C)
3-½ DIGIT	ICL7106	Low Cost	LCD, 7-Segment Direct Drive	0.1 to 15	0 to ±0.2V 0 to ±2.0V	±1 Count	±1 Count	1μV/°C	+9V (Typ) 1.8 mA (Max)	0 to +70
	ICL7107	Low Cost	LED, 7-Segment Common Anode	0.1 to 15	0 to ±0.2V 0 to ±2.0V	±1 Count	±1 Count	1μV/°C	±5V (Typ) 1.8 mA (Max)	0 to +70
	ICL7116	Display Hold Input	LCD, 7-Segment Direct Drive	0.1 to 15	0 to ±0.2V 0 to ±2.0V	±1 Count	±1 Count	1μV/°C	+9V (Typ) 1.8 mA (Max)	0 to +70
	ICL7117	Display Hold Input	LED, 7-Segment Common Anode	0.1 to 15	0 to ±0.2V 0 to ±2.0V	±1 Count	±1 Count	1μV/°C	±5V (Typ) 1.8 mA (Max	0 to +70
	ICL7126	Low Power Operation	LCD, 7-Segment Direct Drive	0.1 to 4	0 to ±0.2V 0 to ±2.0V	±1 Count	±1 Count	1μV/°C	+9V (Typ) 100 μA (Max)	0 to +70
	ICL7136	Improved '7126, Low Power Operation	LCD 7-Segment Direct Drive	0.1 to 4	0 to ±0.2V 0 to ±2.0V	±1 Count	±1 Count	1μV/°C	+9V (Typ) 100 μA (Max)	0 to +70
	ICL7137	Improved '7107, Low Power Operation	LED 7-Segment Common Anode	0.1 to 4	0 to ±0.2V 0 to ±2.0V	±1 Count	±1 Count	1μV/°C	±5V (Typ) 200 μA max	0 to +70
4-½ DIGIT	ICL7129	Range, Display-Hold & Decimal Point Inputs	LCD, 7-Segment Triplexed	2	0 to ±0.2V 0 to +2.0V	±1 Count	0.5 Count (typ)	±0.5μV/°C (typ)	+9V (Typ) 1.4 mA (Max)	0 to +70

Integrating Analog-to-Digital Converters (CMOS)

	TYPE	SPECIAL FEATURES	DIGITAL OUTPUT FORMAT	CONVERSIONS PER SECOND	INPUT VOLTAGE RANGES	NON LINEARITY	ROLLOVER ERROR	STABILITY ZERO INPUT DRIFT	SUPPLY V_{SUPPLY} I_{SUPPLY}	TEMP RANGE (°C)
4-½ DIGIT	ICL7135	Under & over range outputs, polarity output	Multiplexed BCD with strobes	0.1 to 7.5	0 to ±0.2V 0 to ±2.0V	±1 Count	±1 Count	2μV/°C	±5V (Typ) 3.0 mA (Max)	0 to +70
12-BIT	ICL7109	μP-Compatible, run/hold input, UART Handshake	8/4 Bits, Separate Enables	30 (Max)	0 to ±4.0V 0 to ±3.5V	±1 Count	±1 Count	1μV/°C	±5V (Typ) 1.5 mA (Max)	0 to +70 −25 to +85 −55 to +125
12-BIT	ICL7104-12 ICL8052	μP-Compatible, 2-Chip Set, Low Input Leakage	8/4 Bits, Separate Enables	48.8 (Max)	±10V	+1 LSB	+1 LSB	5μV/°C	+5V and ±15V (Typ) 1.0 mA (Max)	0 to +70
12-BIT	ICL7104-12 ICL8068	μP-Compatible, 2-Chip Set, Low Input Noise	8/4 Bits, Separate Enables	48.8 (Max)	±10V	+1 LSB	+1 LSB	5μV/°C	+5V and ±15V (Typ) 1.0 mA (Max)	0 to +70
14-BIT	ICL7104-14 ICL8052	μP-Compatible, 2-Chip Set, Low Input Leakage	8/4 Bits, Separate Enables	12.2 (Max)	±10V	+1 LSB	+1 LSB	2μV/°C	+5V and ±15V (Typ) 1.0 mA (Max)	0 to +70
14-BIT	ICL7104-14 ICL8068	μP-Compatible, 2-Chip Set, Low Input Noise	8/4 Bits, Separate Enables	12.2 (Max)	±10V	+1 LSB	+1 LSB	2μV/°C	+5V and ±15V (Typ) 1.0 mA (Max)	0 to +70
16-BIT	ICL7104-16 ICL8052	μP-Compatible, 2-Chip Set, Low Input Leakage	8/8 Bits, Separate Enables	3 (Max)	±10V	+1 LSB	+1 LSB	2μV/°C	+5V and ±15V (Typ) 1.0 mA (Max)	0 to +70
16-BIT	ICL7104-16 ICL8068	μP-Compatible, 2-Chip Set, Low Input Noise	8/8 Bits, Separate Enables	3 (Max)	±10V	+1 LSB	+1 LSB	2μV/°C	+5V and ±15V (Typ) 1.0 mA (Max)	0 to +70

Successive Approximation Analog-to-Digital Converters (CMOS)

	TYPE	SPECIAL FEATURES	DIGITAL OUTPUT FORMAT	CONVERSION SPEED (μs)	INPUT VOLTAGE RANGE	OVERALL ACCURACY	TOTAL ERROR	GAIN TEMP. COEFF.	SUPPLY V_{SUPPLY}/ I_{SUPPLY}	TEMP RANGE (°C)
8-BIT	ADC0802	μP-Compatible, Differential Inputs	8-Bit Binary	114 (Max)	0 to +5.0V	—	±½ LSB (Unadjusted)	—	+5V (Typ) 2.5 mA (Max)	0 to +70 −40 to +85 −55 to +125
8-BIT	ADC0803	μP-Compatible, Differential Inputs	8-Bit Binary	114 (Max)	0 to +5.0V	—	±½ LSB (Adjusted)	—	+5V (Typ) 2.5 mA (Max)	0 to +70 −40 to +85 −55 to +125
8-BIT	ADC0804	μP-Compatible, Differential Inputs	8-Bit Binary	114 (Max)	0 to +5.0V	—	±1 LSB (Unadjusted)	—	+5V (Typ) 2.5 mA (Max)	0 to +70 −40 to +85 −55 to +125
14-BIT	ICL7115-J/K	μP-Compatible, High Speed Converter	8/6 Bits A_0 Byte Enable	40 (Max)	0 to +5.0V 0 to −5.0V	0.01% (J) 0.006% (K)	+1 LSB	4 ppm/°C	+5V (Typ) 5 mA (Typ)	0 to +70

Digital-to-Analog Converters (CMOS)

	TYPE	SPECIAL FEATURES	DIGITAL INPUT FORMAT	SETTLING TIME (TO 0.05% FS)	OUTPUT VOLTAGE CURRENT	NON LIN-EARITY	GAIN ERROR	STABILITY GAIN LINERITY	SUPPLY V_{SUPPLY} I_{SUPPLY}	TEMP RANGE (°C)
8-BIT	AD7523	µP-Compatible, Low Power Multiplying DAC	Binary/ Offset Binary	200 ns (Max)	± V_{REF} A 10KΩ (Max)	0.2% (J,A,S) 0.1% (K,B,T) 0.05% (L,C,U)	1.5% (Max)	10 ppm/°C 2 ppm/°C	+15V (Typ) 100µA (Max)	0 to +70 −25 to +85 −55 to +125
10-BIT	AD7520	µP-Compatible, 8, 9, 10 Bit Lin. Multiplying DAC	Binary/ Offset Binary	500 ns (Typ)	± V_{REF} A 10KΩ (Max)	0.2% (J,A,S) 0.1% (K,B,T) 0.05% (L,C,U)	0.3% (Typ)	10 ppm/°C 2 ppm/°C	+15V (Typ) 2 mA (Max)	0 to +70 −25 to +85 −55 to +125
10-BIT	AD7530	Same as '7520 But no leakage /feed thru specs	Binary/ Offset Binary	500 ns (Typ)	± V_{REF} A 10KΩ (Max)	0.2% (J,A,S) 0.1% (K,B,T) 0.05% (L,C,U)	0.3% (Typ)	10 ppm/°C 2 ppm/°C	+15V (Typ) 2 mA (Max)	0 to +70 −25 to +85 −55 to +125
10-BIT	AD7533	µP-Compatible, Lowest Cost 10-bit DAC	Binary/ Offset Binary	600 ns (Typ)	± V_{REF} A 10KΩ (Max)	0.2% (J,A,S) 0.1% (K,B,T) 0.05% (L,C,U)	1.4% (Max)	10 ppm/°C 2 ppm/°C	+15V (Typ) 2 mA (Max)	0 to +70 −25 to +85 −55 to +125
12-BIT	AD7521	µP-Compatible, 8, 9, 10 Bit Lin. Multiplying DAC	Binary/ Offset Binary	500 ns (Typ)	± V_{REF} A 10KΩ (Max)	0.2% (J,A,S) 0.1% (K,B,T) 0.05% (L,C,U)	0.3% (Typ)	10 ppm/°C 2 ppm/°C	+15V (Typ) 2 mA (Max)	0 to +70 −25 to +85 −55 to +125
12-BIT	AD7531	Same as '7521 But no leakage /feed thru specs	Binary/ Offset Binary	500 ns (Typ)	± V_{REF} A 10KΩ (Max)	0.2% (J,A,S) 0.1% (K,B,T) 0.05% (L,C,U)	0.3% (Typ)	10 ppm/°C 2 ppm/°C	+15V (Typ) 2 mA (Max)	0 to +70 −25 to +85 −55 to +125
12-BIT	AD7541	µP-Compatible, High perform-ance DAC	Binary/ Offset Binary	1 µs (Max)	± V_{REF} A 10KΩ (Max)	0.02% (J,A,S) 0.01% (K,B,T) 0.01% (L,C,U)	0.3% (Max)	— 2 ppm/°C	+15V (Typ) 2 mA (Max)	0 to +70 −25 to +85 −55 to +125
14-BIT	AD7134	µP-Compatible, Low power Multiplying DAC	Binary/ 2's Complement	3 µs (Max)	± V_{REF} A 7KΩ (Max)	0.1% (J,A,S) 0.006% (K,B,T) 0.003% (L,C,U)	0.02% (J) 0.012% (K) 0.006% (L)	5 ppm/°C 1 ppm/°C	+5V (Typ) 0.5 mA (Max)	0 to +70 −25 to +85 −55 to +125

Quad Current Switches For D/A Conversion (Singles or Matched Pairs)

TYPE	DESCRIPTION	ABSOLUTE ERROR (% Max)	ERROR TEMPCO. (PPM/°C Max)	V_{SUPPLY} (V Max)	I_{SUPPLY} (mA Max)	TEMPERATURE RANGE (°C)
ICL8018A	High precision current	±0.01	±5	±20	10	0 to +70
ICL8019A	switches for use in	±0.10	±25	±25	±20	−55 to +125
ICL8020A	summing D/A converters	±1.00	±50	±20	10	

Timer/Counters With Display Drivers

NUMBER OF DIGITS	TYPE	DISPLAY: LED: Common Anode, Non-MUX	DISPLAY: LED: Common Cathode, MUX	DISPLAY: LED: Common Anode, MUX	DISPLAY: LCD: Direct Drive, Non-MUX	DISPLAY: VF: Non-MUX	FUNCTIONS: UNIT COUNT: Up/Down	FUNCTIONS: UNIT COUNT: Up only	FUNCTIONS: UNIT COUNT: Decade	FUNCTIONS: UNIT COUNT: Modulo 60 (Hr/Min/Sec)	FUNCTIONS: UNIVERSAL COUNTERS: Frequency	FUNCTIONS: UNIVERSAL COUNTERS: Period	FUNCTIONS: UNIVERSAL COUNTERS: Frequency Ratio	FUNCTIONS: UNIVERSAL COUNTERS: Time interval	FUNCTIONS: MUX BCD Outputs	FUNCTIONS: Display Latch	FUNCTIONS: Display Blanking	FUNCTIONS: Count Enable	FUNCTIONS: Leading Zero Blanking	FUNCTIONS: Preset Count	FUNCTIONS: Comparison Register	FUNCTIONS: Equal and Zero Output	MAX COUNT SPEED (MHz)	Evaluation Kit Available	TYPICAL APPLICATIONS AND COMMENTS
4 DIGIT	ICM7217			●			●		●		■				●	●	●		●	●	●	●	2		Industrial control: preset/predetermining counters, sequencers, on/off delay timers, batch counters. Presets and loads compare register from thumbwheel switches
	ICM7217A		●				●		●		■				●	●	●		●	●	●	●	2		
	ICM7217B			●			●			●					●	●	●		●	●	●	●	2		
	ICM7217C		●				●			●					●	●	●		●	●	●	●	2		
	ICM7227			●			●		●						●	●	●		●	●	●	●	2		Microprocessor compatible interface. Industrial control: preset/predetermining counters, sequencers, on/off delay timers, batch counters. Presets and loads compare register from a microprocessor
	ICM7227A		●				●		●						●	●	●		●	●	●	●	2		
	ICM7227B			●			●			●					●	●	●		●	●	●	●	2		
	ICM7227C		●				●			●					●	●	●		●	●	●	●	2		
4-½ DIGIT	ICM7224				●			●	●		■					●		●	●				15	●	10 μA operating current. Can be cascaded for more digits
	ICM7224A				●			●		●						●		●	●				15		
	ICM7225	●						●	●		■					●	●	●	●				15	●	Has brightness adjustment, 10 μA current with display blanked, cascadable
	ICM7225A	●						●		●						●	●	●	●				15		
	ICM7236					●		●	●		■					●	●	●	●				15	●	Up to 30 V output drive for Vacuum Fluorescent
	ICM7236A					●		●		●						●	●	●	●				15		
5-½ DIGIT	ICM7249				●			●	●						●					●					Event timer/counter, hour meter. 14 programmable modes. Selectable input filtering
8 DIGIT	ICM7215		●					●		●					●			●	●						4 functions: start/stop/reset, split, taylor, time out. 1/100's seconds and low battery
7 DIGIT	ICM7208		●					●	●		■					●	●	●	●				2.5		Use with ICM7207/A for a 7-digit frequency counter
8 DIGIT	ICM7216A			●				●	●		●	●	●	●		●	●			●				10		Universal frequency counter with display drivers. 4 internal gate times, auto decimal point, leading zero blanking, overflow indication. Display off, hold, and reset inputs.
	ICM7216B		●					●	●		●	●	●	●		●	●			●				10		
	ICM7216C			●				●	●		●					●	●			●				10		
	ICM7216D		●					●	●		●					●	●			●				10		
	ICM7226A			●				●	●		●	●	●	●	●	●	●	●	●	●				10	●	Same as ICM7216 plus period and time interval averaging, BCD outputs, μP PIA compatible.
	ICM7226B		●					●	●		●	●	●	●	●	●	●	●	●	●				10		

■ These counters will measure frequency when used with the ICM7207 (0.01 and 0.1 second timebase) or the ICM7207A (0.1 and 1.0 second timebase)

Timers/Counters Without Display Drivers

TYPE	SPECIAL FEATURES	DESCRIPTION
ICM7555		Low power CMOS equivalent of industry standard 555 timer—only 80μA supply current. ICM7555 does not have the large supply current transients of the bipolar 555 and does not require the large bypassing capacitors needed by the 555. Low leakage threshold and trigger inputs allow use of higher impedance RC timing components for extra long time delays.
ICM7556		An ICM7556 is a dual ICM7555, a CMOS, low power equivalent of the Bipolar 556 Timer.
ICM7240 ICM7250 ICM7260	Binary 0-225 BCD 0-99 Time 0-59	Programmable CMOS counter/timer. Uses on-board RC oscillator or an external clock. The count is programmed by wire-AND connection of the outputs. Excellent for ON/OFF delay timers, ÷ N counters, and long period delays.
ICM7242	Fixed 128/255	RC oscillator + 8-bit counter, similar to ICM7240 but with fixed 256 count. Used for extremely long time delays. Cascadable.

Oscillator/Divider Selector Guide

TYPE	OUTPUT FREQUENCY	SUPPLY VOLTAGE (V)	TYPICAL CURRENT (μA)	PULSE WIDTH (ms)	CRYSTAL FREQUENCY	OTHER OUTPUTS/COMMENTS
ICM7213	1 Pulse/Min	2-4	100	125, 1000	4.19 MHz	1 Pulse/Sec, 2048, 1024, 34.133, 16 Hz
ICM7207A	0.5 Hz	4-5.5	260	1000, 0.391	5.24288 MHz	5 Hz, 1600 Hz (Note 1)
ICM7213	1 Hz	2-4	100	7.8	4.19 MHz	1 Pulse/Min, 2048, 1024, 34.133, 16 Hz
ICM7207A	5 Hz	4-5.5	260	100, 0.391	5.24288 MHz	0.5, 1600 Hz
ICM7207	5 Hz	4-5.5	260	100, 0.312	6.5536 MHz	50 Hz, 1280 Hz
ICM7213	16 Hz	2-4	100	Sq. Wave	4.19 MHz	1 Pulse/Min, 2048, 1024, 34.133, 1 Hz
ICM7207	50 Hz	4-5.5	260	20, 0.312	6.5536 MHz	5 Hz, 1280 Hz
ICM7213 ICM7213 ICM7207A ICM7207	1000 Hz 1024 Hz 1280 Hz 1600 Hz	2-4 2-4 4-5.5 4-5.5	100 100 260 260	Sq. Wave Sq. Wave Sq. Wave Sq. Wave	4.096 MHz 4.19 MHz 5.24288 MHz 6.5536 Mhz	2000, 2000 Pulses/Min 1 Pulse/Min, 2048, 34.133, 16, 1 Hz 0.5, 5 Hz 5, 50 Hz
ICM7213	2048 Hz	2-4	100	Sq. Wave	4.19 MHz	1 Pulse/Min, 1024, 34.133, 16, 1 Hz
ICM7209	250 kHz-10 MHZ	4.5-5.5	11,000	Sq. Wave	1-10 MHz	(Note 2)

Notes:

1. Oscillator/controller for frequency counter.
2. Two buffered outputs—Crystal Frequency and ÷ 8 output. Drives up to 5 TTL loads.

INTERSIL

TYPE	# OF CHARACTERS OR DIGITS						DISPLAY TYPE						FONT			INTERFACE					FEATURES AND COMMENTS
	# of 7-Segment Digits	# of Decimal Points or Annunciators	# of Alphanumeric 14 Segments + D.P.	# of Alphanumeric 16 Segments + D.P.	# of Alphanumeric 18 Segments	# of Dot Matrix	LED, Common Anode Non-MUX	LED, Common Cathode MUX	LED, Common Anode MUX	LCD, Direct Drive	LCD, # of Ways MUX'D	Vacuum Fluorescent	Hexadecimal (0-9, A-F)	Code B (0-9, H, E, L, P, -, and Blank)	ASCII	MUX BCD (BCD + Digit Select Strobes)	Random Access (Data + Address + WR)	Bit Parallel, Digit Serial	Bit Serial	Cycle Time (ns)	
ICM7211	4									●			●			●				1000	Drives Conventional LCD Displays. Includes RC Oscillator, Divider Chain, Latches, Interface and LCD Drivers. Evaluation Kit Available
ICM7211A	4									●				●		●				1000	
ICM7211M	4									●			●				●			200	
ICM7211AM	4									●				●			●			200	
ICM7212	4						●						●			●				1000	Drives Common Anode LED Displays. 28 Current Controlled Outputs. Includes Latches, Interface and Brightness Control. Evaluation Kit Available.
ICM7212A	4						●							●		●				1000	
ICM7212M	4						●						●				●			200	
ICM7212AM	4						●							●			●			200	
ICM7218A	8	8							●				●	●				●		550	3 Decode Formats Drives UP to 64 Independent LED's. Includes 8x8 Memory, Multiplexed LED Drivers, Decoders, Interface and control. Applications Include Bar Graphs.
ICM7218B	8	8						●					●	●				●		550	
ICM7218C	8	8							●				●	●			●			500	
ICM7218D	8	8						●					●	●			●			500	
ICM7218E	8	8							●				●	●			●			500	
ICM7231A	8	16									3		●				●			500	8 Digits, 16 Annunciators on COM 3, Hexadecimal
ICM7231B	8	16									3			●			●			500	8 Digits, 16 Annunciators on COM 3, Code B
ICM7231C	8	16									3			●			●			500	8 Digits, 16 Annunicators on COM 1 + 3, Code B
ICM7232A	10	20									3		●						●	350	10 Digits, 20 Annunciators on COM 3, Hexadecimal
ICM7232B	10	20									3			●					●	350	10 Digits, 20 Annunciators on COM 3, Code B
ICM7232C	10	20									3			●					●	350	10 Digits, 20 Annunciators on COM 1 + 3, Code B
ICM7233A					4						3				●	●				500	4 Alphanumeric Characters. Evaluation Kit Available
ICM7233B					4						3				●	●				500	4 Alphanumeric Characters. Full-Width Numbers
ICM7234A					5						3				●				●	350	5 Alphanumeric Characters. Half-Width Numbers
ICM7234B					5						3				●				●	350	5 Alphanumeric Characters. Full-Width Numbers
ICM7235	4											●	●			●				1000	Drives 30 Volt Vacuum Fluorescent Displays Directly. Includes Latch/Decoder μP Interface or 4-Bit Input. Hexadecimal or Code B Format Available.
ICM7235A	4											●		●		●				1000	
ICM7235M	4											●	●				●			200	
ICM7235AM	4											●		●			●			200	
ICM7243A				8				●							●		●			250	8 Alphanumeric Characters + Decimal Pt. can be Daisy Chained or Cascaded. Evaluation Kit Available.
ICM7243B			8					●							●		●			250	
ICM7280*		14				80					7& 10				●		●			400	1x80 Ch. Dot Matrix LCD Controller and Row Driver. Use with ICM7281.
ICM7283*		14				80					16				●		●			400	2x40 Ch. Dot Matrix LCD Controller and Row Driver. Use with ICM7281.
ICM7281*						—					—										Column Driver for use with ICM7280 or ICM7283.

*New Product

Microcontrollers, Microperipherals, Memory

Microcontrollers

BASIC PART NUMBER	DESCRIPTION	f_c MHz	INTERNAL MEMORY		PACKAGE	TEMPERATURE RANGE (°C)
			ROM	RAM		
IM80C48*	8048/80C48 Family Compatible	6	1K x 8	64 x 8	PL, JL	0 — +70
IM80C49*	2X the memory of IM80C48	6	2K x 8	128 x 8	PL, JL	
IM80C35*	Same as IM80C48 without ROM	6	None	64 x 8	PL, JL	−40 — +85
IM80C39*	Same as IM80C49 without ROM	6	None	128 x 8	PL, JL	

Microprocessor Peripherals — See also Display Drivers, Counters, A/D, and D/A Converters.

TYPE	DESCRIPTION	f_C (MHz) Max	PACKAGE	TEMPERATURE RANGE (°C)
ICM7170*	μP-Compatible Real-Time Clock, Binary Time Format, Micropower Standby Operation (2μA @ 2.8V)	4.19	PG, JG	−40 — +85
IM6402	CMOS Industry Standard Compatible UART	1.0	PL	−40 — +85
IM6402-1	High-Speed Version of IM6402	2.0	PL, JL	
IM6402A	10V Operating Version of IM6402	4.0	PL, JL	−55 — +125
IM6403	Like Corresponding IM6402	2.46	PL	−40 — +85
IM6403-1	Device but with On-board Crystal	3.58	PL, JL	
IM6403A	Oscillator and Baud Rate Generator	6.0	PL, JL	−55 — +125
IM82C43*	CMOS I/O Expander for 80C48/49 Microcomputers		PG, JG	0 — +70
				−40 — +85
IM4702/12	Baud Rate Generator	3.58	PE, JE	−40 — +85

CMOS EPROMs

ORGANIZATION/ TYPE	MAX ACCESS TIME (ns)	V_{CC} (V)	I_{CC} MAX (mA) OPERATING	I_{CC} MAX (μA) STANDBY	PACKAGE	TEMPERATURE RANGE (°C)
1024 x 4						
IM6653I	550	5	6	140	JG	−40 — +85
IM6653M	600	5	6	140	JG	−55 — +125
IM6653-1I	450	5	6	140	JG	−40 — +85
IM6653AI	300	10	12	140	JG	−40 — +85
IM6653AM	350	10	12	140	JG	−55 — +125
512 x 8						
IM6654I	550	5	6	140	JG	−40 — +85
IM6654M	600	5	6	140	JG	−55 — +125
IM6654-1I	450	5	6	140	JG	−40 — +85
IM6654AI	300	10	12	140	JG	−40 — +85
IM6654AM	350	10	12	140	JG	−55 — +125

*New Product

Section 2 — Discretes

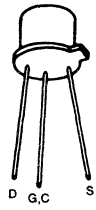
2N2607-2N2609
2N2609JAN
P-Channel JFET
General Purpose Amplifier

APPLICATIONS

- Low-Level Choppers
- Data Switches
- Commutators

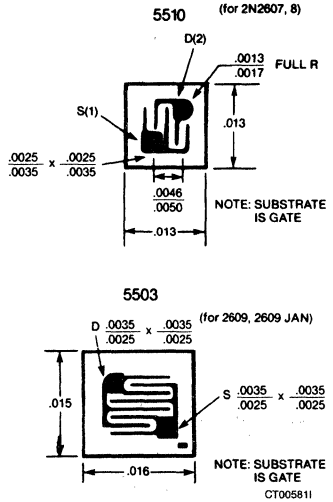
PIN CONFIGURATION

TO-18



PC000111

CHIP TOPOGRAPHY



CT005811

ORDERING INFORMATION*

TO-18	WAFER	DICE
2N2607	2N2607/W	2N2607/D
2N2608	2N2608/W	2N2608/D
2N2609	2N2609/W	2N2609/D
2N2609JAN	—	—

*When ordering wafer/dice refer to Section 10, page 10-1.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source Voltage 30V
Gate-Drain Voltage 30V
Gate Current 50mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +175°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 300mW
Derate above 25°C ..... 2mW/°C

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		2N2607		2N2608		2N2609		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
I_{GSSR}	Gate Reverse Current	V_{GS} = 30V, V_{DS} = 0			3		10		30	nA
		V_{GS} = 5V, V_{DS} = 0, T_A = 150°C			3		10		30	μA
BV_{GSS}	Gate-Drain Breakdown Voltage	1_G = 1μA, V_{DS} = 0		30		30		30		V
V_P	Gate-Source Pinch-Off Voltage	V_{DS} = -5V, I_D = -1μA		1	4	1	4	1	4	V
I_{DSS}	Drain Current at Zero Gate Voltage	V_{DS} = -5V, V_{GS} = 0		-0.30	-1.50	-0.90	-4.50	-2	-10	mA
g_{fs}	Small-Signal Common-Source Forward Transconductance	V_{DS} = -5V, V_{GS} = 0, f = 1kHz		330		1000		2500		μs
C_{iss}	Common-Source Input Capacitance	V_{DS} = -5V, V_{GS} = 1V, f = 1MHz (Note 1)			10		17		30	pF
NF	Noise Figure (Note 1)	V_{DS} = -5V, V_{GS} = 0, f = 1kHz	R_G = 10MΩ		3					dB
			R_G = 1MΩ				3		3	

NOTE 1: For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

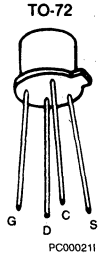
2N3684-2N3687
N-Channel JFET
Low Noise Amplifier

INTERSIL

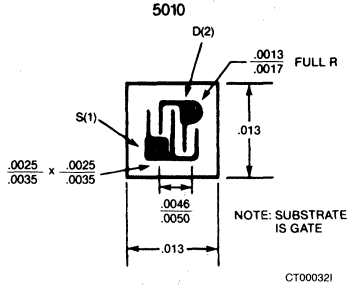
FEATURES
- Low Noise
- High Input Impedance
- Low Capacitance

APPLICATIONS
- Low Level Choppers
- Data Switches
- Multiplexers
- Low Noise Amplifiers

PIN CONFIGURATION



CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-72	WAFER	DICE
2N3684	2N3684/W	2N3684/D
2N3685	2N3685/W	2N3685/D
2N3686	2N3686/W	2N3686/D
2N3687	2N3687/W	2N3687/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage ..... -50V
Gate Current 50mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +175°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 300mW
Derate above 25°C ..... 2.0mW/°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	2N3684		2N3685		2N3686		2N3687		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
BV_{GSS}	Gate to Source Breakdown Voltage	V_{DS} = 0, I_G = 1.0μA	-50		-50		-50		-50		V
V_P	Pinch-Off Voltage	V_{DS} = 20V, I_D = 0.001μA	-2.0	-5.0	-1.0	-3.5	-0.6	-2.0	-0.3	-1.2	
I_{GSS}	Total Gate Leakage Current	V_{GS} = -30V, V_{DS} = 0		-0.1		-0.1		-0.1		-0.1	nA
	T_A = 150°C			-0.5		-0.5		-0.5		-0.5	μA
I_{DSS}	Saturation Current, Drain-to-Source	V_{GS} = 0, V_{DS} = 20V	2.5	7.5	1.0	3.0	0.4	1.2	0.1	0.5	mA
$\|Y_{fs}\|$	Forward Transadmittance	V_{DS} = 20V, V_{GS} = 0 f = 1kHz	2000	3000	1500	2500	1000	2000	500	1500	μs
G_{os}	Common Source Output Conductance			50		25		10		5	μs
C_{iss}	Common Source Input Capacitance	V_{DS} = 20V, V_{GS} = 0 f=1MHz (Note 1)		4.0		4.0		4.0		4.0	pF
C_{rss}	Common Source Short Circuit Reverse Transfer Capacitance			1.2		1.2		1.2		1.2	pF
$r_{DS(on)}$	On Resistance	V_{DS} = 0, V_{GS} = 0		600		800		1200		2400	ohms
NF	Noise Figure (Note 1)	f = 100Hz, R_G = 10MΩ NBW = 6Hz, V_{DS} = 10V, V_{GS} = 0V		0.5		0.5		0.5		0.5	dB

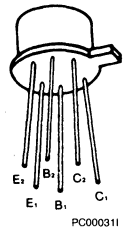
NOTE 1: For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

2N3810/A, 2N3811/A
Dual Matched PNP General Purpose Amplifier

PIN CONFIGURATION

TO-78



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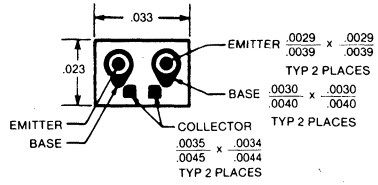
CHIP TOPOGRAPHY

4501



CT000411

ORDERING INFORMATION*

TO-78	WAFER	DICE
2N3810	2N3810/W	2N3810/D
2N3810A		
2N3811	2N3811/W	2N3811/D
2N3811A		

*When ordering wafer/dice refer to Section 10, page 10–1.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Emitter-Base Voltage (Note 1) ..... -5V
Collector-Base or Collector-Emitter Voltage (Note 1) ..... -60V
Collector Current (Note 1) 50mA
Storage Temperature Range ..... -65°C to +175°C
Operating Temperature Range ..... -55°C to +175°C
Lead Temperature (Soldering, 10sec) ..... +300°C

	ONE SIDE	BOTH SIDES
Power Dissipation	500mW	600mW
Derate above 25°C	3.3mW/°C	4.0mW/°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C Ambient Temperature unless otherwise noted

SYMBOL	PARAMETER	TEST CONDITIONS		2N3810/A MIN	2N3810/A MAX	2N3811/A MIN	2N3811/A MAX	UNIT
BV_{CBO}	Collector-Base Breakdown Voltage	I_C = -10μA, I_E = 0		-60		-60		V
BV_{CEO}	Collector-Emitter Breakdown Voltage (Note 2)	I_C = -10mA, I_B = 0		-60		-60		V
BV_{EBO}	Emitter-Base Breakdown Voltage	I_E = -10μA, I_C = 0		-5		-5		V
$I_{C(off)}$	Collector Cutoff Current	V_{CB} = -50V, I_E = 0			-10		-10	nA
	T_A = +150°C				-10		-10	μA
$I_{E(off)}$	Emitter Cutoff Current	V_{BE} = 4V, I_C = 0			-20		-20	nA
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = -5V	I_C = -10μA	100		225		
			I_C = -100μA to -1mA	150	450	300	900	
			I_C = 10mA (Note 2)	125		250		
	T_A = -55°C		I_C = 100μA	75		150		
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	V_{CE} = -5V, I_C = -100μA	I_B = -10μA		-0.7		-0.7	V
			I_B = -100μA		-0.8		-0.8	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage (Note 2)	I_B = -10μA, I_C = -100μA			-0.2		-0.2	V
		I_B = -100μA, I_C = -1mA			-0.25		-0.25	
h_{ie}	Input Impedance (Note 4)	V_{CE} = -10V		3	30	10	40	kΩ
h_{fe}	Forward Current Transfer Ratio (Note 4)	I_C = -1mA		150	600	300	900	
h_{re}	Reverse Voltage Transfer Ratio (Note 4)	f = 1kHz			0.25		0.25	
h_{oe}	Output Admittance (Note 4)			5	60	5	60	μs

Note: All typical values have been guaranteed by characterization and are not tested.

2N3810/A, 2N3811/A

INTERSIL

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER		TEST CONDITIONS		2N3810/A MIN	2N3810/A MAX	2N3811/A MIN	2N3811/A MAX	UNIT
$\|h_{fe}\|$	Magnitude of small signal current gain (Note 4)		$V_{CE} = -5V$	$I_C = -1mA$, f = 100MHz	1	5	1	5	
				$I_C = -500\mu A$, f = 30MHz	1		1		
C_{obo}	Output Capacitance (Note 4)		$V_{CB} = -5V$, $I_E = 0$, f = 1MHz			4		4	pF
C_{ibo}	Input Capacitance (Note 4)		$V_{CB} = -0.5V$, $I_C = 0$, f = 1MHz			8		8	
h_{FE_1}/h_{FE_2}	DC Current Gain Ratio		$V_{CE} = -5V$, $I_C = 100\mu A$		0.9	1.0	0.9	1.0	
		A devices			0.95	1.0	0.95	1.0	
$\|V_{BE_1}-V_{BE_2}\|$	Base-Emitter Voltage Differential		$V_{CE} = -5V$	$I_C = 10\mu A$ to 10mA		-5		-5	mV
		A devices				-2.5		-2.5	
				$I_C = 100\mu A$		-3		-3	
		A devices				-1.5		-1.5	
$\frac{\Delta V_{BE_1}-V_{BE_2}}{\Delta T}$	Base-Emitter Voltage Differential Gradient		$V_{CE} = -5$, $I_C = 100\mu A$			10		10	$\mu V/°C$
		A devices				5		5	
NF	Spot Noise Figure		$V_{CE} = -10V$, $I_C = -100\mu A$, $R_G = 3k\Omega$, f = 100Hz, Noise Bandwidth = 20Hz			7		4	dB
			$V_{CE} = -10V$, $I_C = -100\mu A$, $R_G = 3K\Omega$, f = 1kHz, Noise Bandwidth = 200kHz			3		1.5	
			$V_{CE} = -10V$, $I_C = -100\mu A$, $R_G = 3k\Omega$ f = 10kHz, Noise Bandwidth = 2kHz			2.5		1.5	
	(Note 4)		$V_{CE} = -10V$, $I_C = -100\mu A$, $R_G = 3k\Omega$, Noise Bandwidth = 15.7kHz (Note 3)			3.5		2.5	

NOTES: 1. Per transistor.
2. Pulse width ≤ 300μs, duty cycle ≤ 2.0%.
3. 3dB down at 10Hz and 10kHz.
4. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

2N3821, 2N3822, JAN, JTX, JTXV

N-Channel JFET High Frequency Amplifier

FEATURES

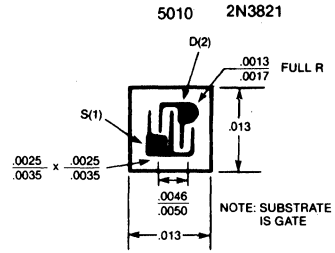
- **Low Capacitance**
- **Up to 6500μs Transconductance**

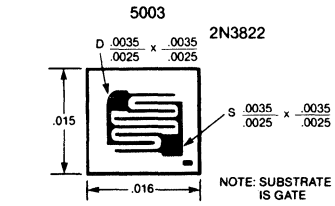
PIN CONFIGURATION

TO-72

CT00650I

CHIP TOPOGRAPHY





CT00052I

ORDERING INFORMATION*

TO-72	WAFER	DICE
2N3821	2N3821/W	2N3821/D
2N3822	2N3822/W	2N3822/D

*When ordering wafer/dice refer to Section 10, page 10-1.

†add JAN, JTX, JTXV to basic part number to specify these devices.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source Voltage ..... -50V
Gate-Drain Voltage ..... -50V
Gate Current 10mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +175°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 300mW
Derate above 25°C ..... 2.0mW/°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	2N3821		2N3822		UNIT
			MIN	MAX	MIN	MAX	
I_{GSS}	Gate Reverse Current	V_{GS} = -30V, V_{DS} = 0		-0.1		-0.1	nA
	T_A = 150°C			-0.1		-0.1	μA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = -1μA, V_{DS} = 0	-50		-50		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 15V, I_D = 0.5nA		-4		-6	
V_{GS}	Gate-Source Voltage	V_{DS} = 15V, I_D = 50μA	-0.5	-2			
		V_{DS} = 15V, I_D = 200μA			-1	-4	
I_{DSS}	Saturation Drain Current (Note 1)	V_{DS} = 15V, V_{GS} = 0	0.5	2.5	2	10	mA

Note: All typical values have been guaranteed by characterization and are not tested.

2N3821, 2N3822, JAN, JTX, JTXV

INTERSIL

SYMBOL	PARAMETER	TEST CONDITIONS		2N3821		2N3822		UNIT
				MIN	MAX	MIN	MAX	
g_{fs}	Common-Source Forward Transconductance (Note 1)	V_{DS} = 15V, V_{GS} = 0	f = 1kHz	1500	4500	3000	6500	μs
$\lvert y_{fs} \rvert$	Common-Source Forward Transadmittance (Note 2)		f = 100MHz	1500		3000		
g_{os}	Common-Source Output Conductance (Note 1)		f = 1kHz		10		20	
C_{iss}	Common-Source Input Capacitance (Note 2)		f = 1MHz		6		6	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)				3		3	
NF	Noise Figure (Note 2)	V_{DS} = 15V, V_{GS} = 0, R_{gen} = 1meg, BW = 5Hz	f = 10Hz		5		5	dB
$\bar{e}_n$	Equivalent Input Noise Voltage (Note 2)	V_{DS} = 15V, V_{GS} = 0, BW = 5Hz			200		200	$\frac{nV}{\sqrt{Hz}}$

NOTES: 1. These parameters are measured during a 2ms interval 100ms after DC power is applied.
2. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

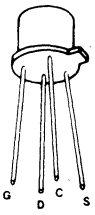
2N3823, JAN, JTX, JTXV
N-Channel JFET
High Frequency Amplifier

INTERSIL

FEATURES
- **Low Noise**
- **Low Capacitance**
- **Transductance Up to 6500μs**

PIN CONFIGURATION

TO-72



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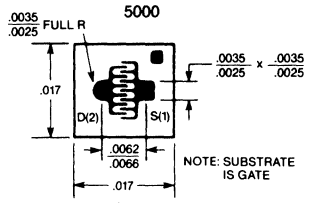
CHIP TOPOGRAPHY



CT00061I

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage ..... -30V
Gate Current 10mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +175°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 300mW
Derate above 25°C ..... 2.0mW/°C

ORDERING INFORMATION*

TO-72	WAFER	DICE
2N3823	2N3823/W	2N3823/D

*When ordering wafer/dice refer to Section 10, page 10-1.
†add JAN,JTX,JTXV to basic part number to specify these devices

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
I_{GSS}	Gate Reverse Current	V_{GS} = -20V, V_{DS} = 0			-0.5	nA
	T_A = 150°C				-0.5	μA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = 1μA, V_{DS} = 0		-30		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 15V, I_D = 0.5nA			-8	
V_{GS}	Gate-Source Voltage	V_{DS} = 15V, I_D = 400μA		-1.0	-7.5	
I_{DSS}	Saturation Drain Current	V_{DS} = 15V, V_{GS} = 0		4	20	mA
g_{fs}	Common-Source Forward Transconductance (Note 1)	V_{DS} = 15V, V_{GS} = 0	f = 1kHz	3,500	6,500	μs
$\|Y_{fs}\|$	Common-Source Forward Transadmittance (Note 2)		f = 100MHz	3,200		
g_{os}	Common-Source Output Transconductance (Note 1)		f = 1kHz		35	
g_{iss}	Common-Source Input Conductance (Note 2)		f = 200MHz		800	
g_{oss}	Common-Source Output Conductance (Note 2)				200	
C_{iss}	Common-Source Input Capacitance (Note 2)		f = 1MHz		6	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)				2	
NF	Noise Figure (Note 2)	V_{DS} = 15V, V_{GS} = 0, R_G = 1kΩ	f = 100MHz		2.5	dB

NOTES: 1. These parameters are measured during a 2ms interval 100ms after DC power is applied.
2. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

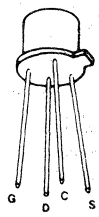
2N3824
N-Channel JFET Switch

INTERSIL

FEATURES
- $r_{ds} < 250$ Ohms
- $I_{D(off)} < 0.1$nA

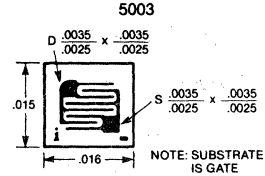
PIN CONFIGURATION

TO-72



PC00020I

CHIP TOPOGRAPHY



CT00051I

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage ..... −50V
Gate Current 10mA
Storage Temperature Range ..... −65°C to +200°C
Operating Temperature Range ..... −55°C to +175°C
Load Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 300mW
Derate above 25°C ..... 2.0mW/°C

ORDERING INFORMATION*

TO-72	WAFER	DICE
2N3824	2N3824/W	2N3824/D

*When ordering wafer/dice refer to Section 10, page 10–1.

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS MIN	LIMITS MAX	UNIT
I_{GSS}	Gate Reverse Current	V_{GS} = −30V, V_{DS} = 0			−0.1	nA
	T_A = 150°C				−0.1	μA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = 1μA, V_{DS} = 0		−50		V
$I_{D(off)}$	Drain Cutoff Current	V_{DS} = 15V, V_{GS} = −8V			0.1	nA
	T_A = 150°C				0.1	μA
$r_{ds(on)}$	Drain-Source ON Resistance	V_{GS} = 0V, I_D = 0	f = 1kHz		250	Ω
C_{iss}	Common-Source Input Capacitance (Note 1)	V_{DS} = 15V, V_{GS} = 0	f = 1MHz		6	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 1)	V_{GS} = −8V, V_{DS} = 0	f = 1MHz		3	pF

NOTE 1: For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

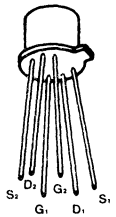
2N3921, 2N3922
Dual N-Channel JFET General Purpose Amplifier

INTERSIL

FEATURES
- Low Drain Current
- High Output Impedance
- Matched V_{GS}, ΔV_{GS}, and g_{fs}

PIN CONFIGURATION

TO-71



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CHIP TOPOGRAPHY

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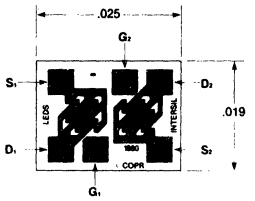


ALL BOND PADS ARE 4 x 4 MIL.

CT000711

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage (Note 1) ..... −50V
Gate Current (Note 1) 50mA
Storage Temperature Range ..... −65°C to +200°C
Operating Temperature Range ..... −55°C to +200°C
Load Temperature (Soldering, 10sec) ..... +300°C
Total Power Dissipation 300mW
Derate above 25°C ..... 1.7mW/°C

ORDERING INFORMATION*

TO-71	WAFER	DICE
2N3921	2N3921/W	2N3921/D
2N3922	2N3922/W	2N3922/D

*When ordering wafer/dice refer to Section 10, page 10–1.

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
I_{GSS}	Gate Reverse Current	V_{GS} = −30V, V_{DS} = 0			−1	nA
	T_A = 100°C				−1	μA
BV_{DGO}	Drain-Gate Breakdown Voltage	I_D = 1μA, I_S = 0		50		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 10V, I_D = 1nA			−3	
V_{GS}	Gate-Source Voltage	V_{DS} = 10V, I_D = 100μA		−0.2	−2.7	
I_G	Gate Operating Current	V_{DG} = 10V, I_D = 700μA			−250	pA
	T_A = 100°C				−25	nA
I_{DSS}	Saturation Drain Current (Note 1)	V_{DS} = 10V, V_{GS} = 0		1	10	mA
g_{fs}	Common-Source Forward Transconductance (Note 2)	V_{DS} = 10V, V_{GS} = 0	f=1kHz	1500	7500	μs
g_{os}	Common-Source Output Conductance				35	
C_{iss}	Common-Source Input Capacitance (Note 3)		f=1MHz		18	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 3)				6	
g_{fs}	Common-Source Forward Transconductance	V_{DG} = 10V, I_D = 700μA	f = 1kHz	1500		μs
g_{oss}	Common-Source Output Conductance				20	
NF	Spot Noise Figure (Note 3)	V_{DS} = 10V, V_{GS} = 0	f = 1kHz, R_G = 1meg		2	dB

Note: All typical values have been guaranteed by characterization and are not tested.

2N3921, 2N3922

MATCHING CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		2N3921		2N3922		UNIT
				MIN	MAX	MIN	MAX	
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage	V_{DG} = 10V, I_D = 700μA			5		5	mV
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Differential Voltage Change with Temperature		T_A = 0°C T_B = 100°C		10		25	μV/°C
g_{fs1}/g_{fs2}	Transconductance Ratio		f = 1kHz	0.95	1.0	0.95	1.0	

NOTES: 1. Per transistor.
2. Pulse test duration = 2 ms.
3. For design reference only, not 100% tested.

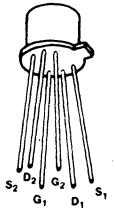
Note: All typical values have been guaranteed by characterization and are not tested.

2N3954-2N3958
2N3954A/2N3955A
Dual N-Channel JFET
General Purpose Amplifier

FEATURES
- Low Offset and Drift
- Low Capacitance
- Low Noise
- Superior Tracking Ability
- Low Output Conductance

PIN CONFIGURATION

TO-71



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CHIP TOPOGRAPHY

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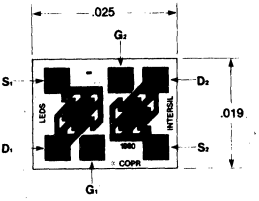


ALL BOND PADS ARE 4 x 4 MIL.

CT000811

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage ..... −50V
Gate-to-Gate Voltage..... ±50V
Gate Current 50mA
Total Device Dissipation 85°C (Each Side) 250mW
Case Temperature (Both Sides)..... 500mW
Power Derating (Each Side)..... 2.86mW/°C
(Both Sides)..... 4.3mW/°C
Storage Temperature Range ..... −65°C to +200°C
Lead Temperature (1/16" from case for 10 seconds) ..... 300°C

ORDERING INFORMATION*

TO-71	WAFER	DICE
2N3954	2N3954/W	2N3954/D
2N3954A	2N3954A/W	2N3954A/D
2N3955	2N3955/W	2N3955/D
2N3955A	2N3955A/W	2N3955A/D
2N3956	2N3956/W	2N3956/D
2N3957	2N3957/W	2N3957/D
2N3958	2N3958/W	2N3958/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	2N3954		2N3954A		2N3955		2N3955A		2N3956		2N3957		2N3958		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{GSS}	Gate Reverse Current	V_{GS} = −30V,		−100		−100		−100		−100		−100		−100		−100	pA
	T_A = 125°C	V_{DS} = 0		−500		−500		−500		−500		−500		−500		−500	nA
BV_{GSS}	Gate-Source Breakdown Voltage	V_{DS} = 0 I_G = −1μA	−50		−50		−50		−50		−50		−50		−50		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 20V, I_D = 1nA	−1.0	−4.5	−1.0	−4.5	−1.0	−4.5	−1.0	−4.5	−1.0	−4.5	−1.0	−4.5	−1.0	−4.5	V
$V_{GS(f)}$	Gate-Source Forward Voltage	V_{DS} = 0 I_G = 1mA		2.0		2.0		2.0		2.0		2.0		2.0		2.0	V
V_{GS}	Gate-Source Voltage	V_{DS} = 20V, I_D = 50μA		−4.2		−4.2		−4.2		−4.2		−4.2		−4.2		−4.2	V
		V_{DS} = 20V, I_D = 200μA	−0.5	−4.0	−0.5	−4.0	−0.5	−4.0	−0.4	−4.0	−0.5	−4.0	−0.5	−4.0	−0.5	−4.0	V
I_G	Gate Operating Current	V_{DS} = 20V,		−50		−50		−50		−50		−50		−50		−50	pA
	T_A = 125°C	I_D = 200μA		−250		−250		−250		−250		−250		−250		−250	nA
I_{DSS}	Saturation Drain Current	V_{DS} = 20V, V_{GS} = 0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	mA

Note: All typical values have been guaranteed by characterization and are not tested.

2N3954-2N3958 2N3954A/2N3955A

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS		2N3954		2N3954A		2N3955		2N3955A		2N3956		2N3957		2N3958		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
g_{fs}	Common-Source Forward Transconductance		f = 1kHz	1000	3000	1000	3000	1000	3000	1000	3000	1000	3000	1000	3000	1000	3000	μs
		(Note 2)	f = 200MHz	1000		1000		1000		1000		1000		1000		1000		
g_{os}	Common-Source Output Conductance	V_{DS} = 20V, V_{GS} = 0	f = 1kHz		35		35		35		35		35		35		35	
C_{iss}	Common-Source Input Capacitance (Note 2)		f = 1MHz		4.0		4.0		4.0		4.0		4.0		4.0		4.0	pF
C_{rss}	Common Source Reverse Transfer Capacitance (Note 2)				1.2		1.2		1.2		1.2		1.2		1.2		1.2	
C_{dgo}	Drain-Gate Capacitance (Note 2)	V_{DG} = 10V, I_S = 0			1.5		1.5		1.5		1.5		1.5		1.5		1.5	
NF	Common-Source Spot Noise Figure (Note 2)	V_{DS} = 20V V_{GS} = 0 R_G = 10MΩ	f = 100Hz		0.5		0.5		0.5		0.5		0.5		0.5		0.5	dB
$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Current	V_{DS} = 20V, I_D = 200μA	T = 125°C		10		10		10		10		10		10		10	nA
I_{DSS1}/I_{DSS2}	Drain Saturation Current Ratio	V_{DS} = 20V V_{GS} = 0		0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	0.90	1.0	0.85	1.0	
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage	V_{DS} = 20V, I_D = 200μA			5.0		5.0		10.0		5.0		15		20		25	mV
$\frac{\Delta\lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Differential Voltage Change With Temperature		T = 25°C to -55°C		0.8		0.4		2.0		1.2		4.0		6.0		8.0	
			T = 25°C to 125°C		1.0		0.5		2.5		1.5		5.0		7.5		10.0	
g_{fs1}/g_{fs2}	Transconductance Ratio		f = 1kHz	0.97	1.0	0.97	1.0	0.97	1.0	0.95	1.0	0.95	1.0	0.90	1.0	0.85	1.0	

NOTES: 1. Per Transistor.
2. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

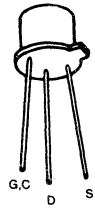
2N3970-2N3972
N-Channel JFET Switch

FEATURES

- Low $r_{DS(on)}$
- $I_{D(OFF)} < 250pA$
- Fast Switching

PIN CONFIGURATION

TO-18



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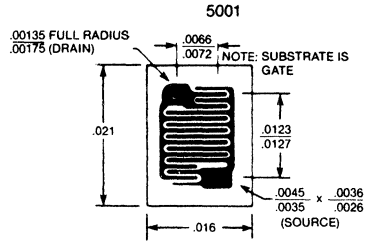
CHIP TOPOGRAPHY



ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage ..... -40V
Gate Current 50mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +200°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 1.8W
Derate above 25°C ..... 10mW/°C

ORDERING INFORMATION*

TO-18	WAFER	DICE
2N3970	2N3970/W	2N3970/D
2N3971	2N3971/W	2N3971/D
2N3972	2N3972/W	2N3972/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

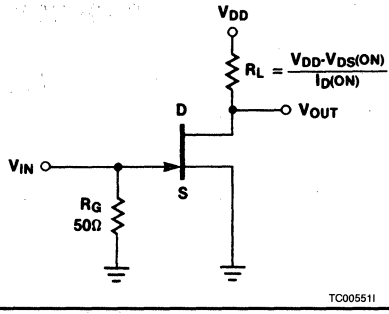
SYMBOL	PARAMETER	TEST CONDITIONS	2N3970		2N3971		2N3972		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
BV_{GSS}	Gate Reverse Breakdown Voltage	$I_G = -1\mu A$, $V_{DS} = 0$	-40		-40		-40		V
I_{DGO}	Drain Reverse Current	$V_{DG} = 20V$, $I_S = 0$		250		250		250	pA
	T_A = 150°C			500		500		500	nA
$I_{D(off)}$	Drain Cutoff Current	$V_{DG} = 20V$, $V_{GS} = -12V$		250		250		250	pA
	T_A = 150°C			500		500		500	nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 20V$, $I_D = 1nA$	-4	-10	-2	-5	-0.5	-3	V
I_{DSS}	Saturation Drain Current (Pulse width 300μs, duty cycle ≤ 3%)	$V_{DS} = 20V$, $V_{GS} = 0$	50	150	25	75	5	30	mA
$V_{DS(on)}$	Drain-Source ON Voltage	$V_{GS} = 0$, I_D = 5mA						2	V
		$V_{GS} = 0$, I_D = 10mA				1.5			
		$V_{GS} = 0$, I_D = 20mA		1					
$r_{DS(on)}$	Static Drain-Source ON Resistance	$V_{GS} = 0$, $I_D = 1mA$		30		60		100	Ω
$r_{ds(on)}$	Drain-Source ON Resistance	$V_{GS} = 0$, $I_D = 0$, f = 1kHz		30		60		100	
C_{iss}	Common-Source Input Capacitance	$V_{DS} = 20V$, $V_{GS} = 0$ (Note 1), f = 1MHz		25		25		25	pF
C_{rss}	Common-Source Reverse Transfer Capacitance	$V_{DS} = 0$, $V_{GS} = -12V$ (Note 1), f = 1MHz		6		6		6	
t_d	Turn-On Delay Time (Note 1)	V_{DD} = 10V, $V_{GS(on)}$ = 0, $I_{D(on)}$, $V_{GS(off)}$, R_L		10		15		40	ns
t_r	Rise Time (Note 1)	2N3970 20mA -10V 450Ω		10		15		40	
t_{off}	Turn-Off Time (Note 1)	2N3971 10mA -5V 850Ω; 2N3972 5mA -3V 1.6KΩ		30		60		100	

NOTE 1: For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

2N3970-2N3972

ELECTRICAL CHARACTERISTICS (CONT.)



Note: All typical values have been guaranteed by characterization and are not tested.

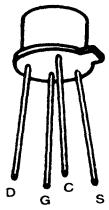
2N3993, 2N3994
P-Channel JFET
General Purpose Amplifier/Switch

INTERSIL

FEATURES
- Low $r_{DS(on)}$
- High Y_{fs}/C_{iss} Ratio (High-Frequency Figure-of-Merit)

APPLICATIONS
Used in high-speed commutator and chopper applications. Also ideal for "Virtual Gnd" switching; needs no ext. translator circuit to switch ±10 VAC. Can be driven direct from TTL or CMOS logic.

PIN CONFIGURATION
TO-72



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CHIP TOPOGRAPHY
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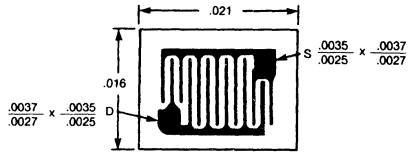


NOTE: SUBSTRATE IS GATE

CT00101I

ORDERING INFORMATION*

TO-72	WAFER	DICE
2N3993	2N3993/W	2N3993/D
2N3994	2N3994/W	2N3994/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Drain-Gate Voltage ..... -25V
Drain-Source Voltage ..... -25V
Continuous Forward Gate Current ..... -10mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +175°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 300mW
Derate above 25°C ..... 2.0mW/°C

2

ELECTRICAL CHARACTERISTICS @ 25°C free-air temperature (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS (Note 3)		2N3993		2N3994		UNIT
				MIN	MAX	MIN	MAX	
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = 1μA,	V_{DS} = 0	25		25		V
I_{DGO}	Drain Reverse Current	V_{DG} = -15V,	I_S = 0		-1.2		-1.2	nA
		V_{DG} = -15V,	I_S = 0, T_A = 150°C		-1.2		-1.2	μA
I_{DSS}	Zero-Gate-Voltage Drain Current	V_{DS} = -10V,	V_{GS} = 0, (See Note 1)	-10		-2		mA
$I_{D(off)}$	Drain Cutoff Current	V_{DS} = -10V,	V_{GS} = 6V				-1.2	nA
		V_{DS} = -10V,	V_{GS} = 6V, T_A = 150°C				-1	μA
		V_{DS} = -10V,	V_{GS} = 10V		-1.2			nA
		V_{DS} = -10V,	V_{GS} = 10V, T_A = 150°C		-1			μA
$V_{GS(off)}$	Gate-Source Voltage	V_{DS} = -10V,	I_D = -1μA	4	9.5	1	5.5	V
$r_{ds(on)}$	Small-Signal Drain-Source On-State Resistance	V_{GS} = 0, f = 1kHz	I_D = 0,		150		300	Ω
$\|y_{fs}\|$	Small-Signal Common-Source Forward Transfer Admittance	V_{DS} = -10V, f = 1kHz,	V_{GS} = 0, (See Note 1)	6	12	4	10	μs
C_{iss}	Common-Source Short-Circuit Input Capacitance (Note 4)	V_{DS} = -10V, f = 1MHz,	V_{GS} = 0, (See Note 2)		16		16	pF

Note: All typical values have been guaranteed by characterization and are not tested.

2N3993, 2N3994

INTERSIL

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS (Note 3)	2N3993		2N3994		UNIT
			MIN	MAX	MIN	MAX	
C_{rss}	Common-Source Short-Circuit Reverse Transfer Capacitance (Note 4)	V_{DS} = 0, V_{GS} = 6V, f = 1MHz				5	pF
		V_{DS} = 0, V_{GS} = 10V, f = 1MHz		4.5			pF

NOTES: 1. These parameters must be measured using pulse techniques, t_p = 100ms, duty cycle ≤ 10%.
2. This parameter must be measured with bias voltage applied for less than 5 seconds to avoid overheating.
3. The case should be connected to the source for all measurements.
4. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

2N4044, 2N4045, 2N4100, 2N4878, 2N4879, 2N4880

Dielectrically Isolated Dual NPN General Purpose Amplifier

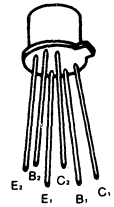
INTERSIL

FEATURES

- High Gain at Low Current
- Low Output Capacitance
- Good h_{FE} Match
- Tight V_{BE} Tracking
- Dielectrically Isolated Matched Pairs for Differential Amplifiers

PIN CONFIGURATION

TO-71
TO-78



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CHIP TOPOGRAPHY

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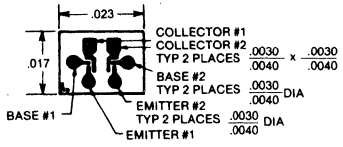

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ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Collector-Base or Collector-Emitter Voltage (Note 1)
- 2N4044, 2N4878 ..... 60V
- 2N4100, 2N4879 ..... 55V
- 2N4045, 2N4880 ..... 45V

Collector-Collector Voltage 100V
Emitter Base Voltage (Note 2) 7V
Collector Current (Note 1) 10mA
Storage Temperature Range ..... −65°C to +175°C
Operating Temperature Range ..... −55°C to +175°C
Lead Temperature (Soldering, 10sec) ..... +300°C

	TO-71		TO-78	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Power Dissipation	200mW	400mW	250mW	500mW
Derate above 25°C (mW/°C)	1.3	2.7	1.7	3.3

ORDERING INFORMATION*

TO-78	TO-71	WAFER	DICE
2N4044	2N4878	2N4044/W	2N4044/D
2N4045	2N4879	2N4045/W	2N4045/D
2N4100	2N4880	2N4100/W	2N4100/D

*When ordering wafer/dice refer to Section 10, page 10–1.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	2N4044 2N4878		2N4100 2N4879		2N4045 2N4880		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
h_{FE}	DC Current Gain	I_C = 10μA, V_{CE} = 5V	200	600	150	600	80	800	
		I_C = 1.0mA, V_{CE} = 5V	225		175		100		
	T_A = −55°C	I_C = 10μA, V_{CE} = 5V	75		50		30		
$V_{BE(on)}$	Emitter-Base On Voltage			0.7		0.7		0.7	V
$V_{CE(sat)}$	Collector Saturation Voltage	I_C = 1.0mA, I_B = 0.1mA		0.35		0.35		0.35	
I_{CBO}	Collector Cutoff Current	I_E = 0, V_{CB} = 45V, 30V*		0.1		0.1		0.1*	nA
	T_A = 150°C			0.1		0.1		0.1*	μA
I_{EBO}	Emitter Cutoff Current	I_C = 0, V_{EB} = 5V		0.1		0.1		0.1	nA
C_{obo}	Output Capacitance (Note 4)	I_E = 0, V_{CB} = 5V, f = 1MHz		0.8		0.8		0.8	pF

Note: All typical values have been guaranteed by characterization and are not tested.

2N4044, 2N4045, 2N4100, 2N4878, 2N4879, 2N4880

INTERSIL

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	2N4044 2N4878		2N4100 2N4879		2N4045 2N4880		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
C_{te}	Emitter Transition Capacitance (Note 4)	$I_C = 0$, $V_{EB} = 0.5V$, f = 1MHz		1		1		1	pF
C_{C_1, C_2}	Collector to Collector Capacitance (Note 4)	$V_{CC} = 0$, f = 1MHz		0.8		0.8		0.8	pF
I_{C_1, C_2}	Collector to Collector Leakage Current	$V_{CC} = \pm 100V$		5		5		5	pA
$V_{CEO(sust)}$	Collector to Emitter Sustaining Voltage	$I_C = 1mA$, $I_B = 0$	60		55		45		V
f_t	Current Gain Bandwidth Product (Note 4)	$I_C = 1mA$, $V_{CE} = 10V$	200		150		150		MHz
f_t	Current Gain Bandwidth Product (Note 4)	$I_C = 10\mu A$, $V_{CE} = 10V$	20		15		15		MHz
NF	Narrow Band Noise Figure (Note 4)	$I_C = 10\mu A$, $V_{CE} = 5V$, $R_G = 10k\Omega$, f = 1kHz, BW = 200Hz		2		3		3	dB
BV_{CBO}	Collector Base Breakdown Voltage	$I_C = 10\mu A$, $I_E = 0$	60		55		45		V
BV_{EBO}	Emitter Base Breakdown Voltage	$I_E = 10\mu A$, $I_C = 0$	7		7		7		V

MATCHING CHARACTERISTICS (25°C unless otherwise noted)

h_{FE_1}/h_{FE_2}	DC Current Gain Ratio (Note 3)	$I_C = 10\mu A$ to 1mA, $V_{CE} = 5V$	0.9	1	0.85	1	0.8	1	
$\lvert V_{BE_1} - V_{BE_2} \rvert$	Base Emitter Voltage Differential	$I_C = 10\mu A$, $V_{CE} = 5V$		3		5		5	mV
$\lvert I_{B_1} - I_{B_2} \rvert$	Base Current Differential	$I_C = 10\mu A$, $V_{CE} = 5V$		5		10		25	nA
$\lvert \Delta(V_{BE_1} - V_{BE_2}) \rvert / \Delta T$	Base Emitter Voltage Differential Change with Temperature	$I_C = 10\mu A$, $V_{CE} = 5V$, $T_A = -55°C$ to $+125°C$		3		5		10	$\mu V/°C$
$\lvert \Delta(I_{B_1} - I_{B_2}) \rvert / \Delta T$	Base Current Differential Change with Temperature			0.3		0.5		1	nA/°C

SMALL SIGNAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	TYPICAL VALUE	UNIT
h_{ib}	Input Resistance	$I_C = -1mA$, $V_{CB} = 5V$ (Note 4)	28	Ω
h_{rb}	Voltage Feedback Ratio		43	$\times 10^{-3}$
h_{fe}	Small Signal Current Gain	$I_C = 1mA$, $V_{CE} = 5V$ (Note 4)	250	
h_{ob}	Output Conductance		60	μS
h_{ie}	Input Resistance		9.6	$k\Omega$
h_{re}	Voltage Feedback Ratio		42	$\times 10^{-3}$
h_{oe}	Output Conductance		12	μS

NOTES:
1. Per transistor.
2. The reverse base-emitter voltage must never exceed 7.0 volts and the reverse base-emitter current must never exceed $10\mu A$.
3. The lowest of two h_{FE} readings is taken as h_{FE_1} for purposes of this ratio.
4. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

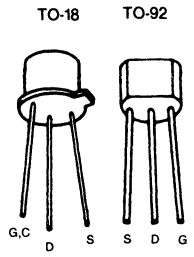
ITE4091-ITE4093
2N4091-2N4093
JAN, JTXV, JANTX*
N-Channel JFET Switch

INTERSIL

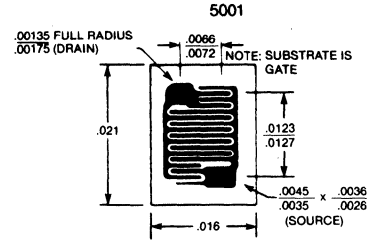
FEATURES

- Low $r_{DS(on)}$
- $I_{D(OFF)} < 100pA$ (JAN TX Types)
- Fast Switching

PIN CONFIGURATIONS



CHIP TOPOGRAPHY



ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage ..... -40V
Gate Current 10mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +200°C
Lead Temperature (Soldering, 10sec) ..... +300°C

	TO-18	TO-92
Power Dissipation	1.8W	360mW
Derate above 25°C	10mW/°C	3.3mW/°C

Plastic
Storage ..... -55°C to +150°C
Operating ..... -55°C to +135°C

ORDERING INFORMATION*

TO-92	TO-18†	WAFER	DICE
ITE 4091	2N4091	2N4091/W	2N4091/D
ITE 4092	2N4092	2N4092/W	2N4092/D
ITE 4093	2N4093	2N4093/W	2N4093/D

†add JANTX to these part numbers if JANTX processing is desired.
*When ordering wafer/dice refer to Section 10, page 10-1.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	2N/ITE 4091		2N/ITE 4092		2N/ITE 4093		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = -1\mu A$, $V_{DS} = 0$	-40		-40		-40		V
I_{DGO}	Drain Reverse Current			200		200		200	pA
	(Not JANTX Specified) T_A = 150°C	V_{DG} = 20V, I_S = 0		400		400		400	nA
I_{GSS}	Gate Reverse Current			-100		-100		-100	pA
	(JANTX, ITE devices only) T_A = 150°C	$V_{GS} = -20V$, $V_{DS} = 0$		-200		-200		-200	nA
$I_{D(OFF)}$	JANTX JAN, JTXV; T_A = 25°C	V_{DS} = 20V, $V_{GS} = -12V$(4091)		100		100		100	pA
		$V_{GS} = -8V$(4092)		200		200		200	
		$V_{GS} = -6V$(4093)							
	Drain Cutoff Current JANTX			200		200		200	
	JAN, JTXV, T_A = 150°C			400		400		400	nA
V_P	Gate-Source Pinch-Off Voltage	V_{DS} = 20V, I_D = 1nA	-5	-10	-2	-7	-1	-5	V
I_{DSS}	Drain Current at Zero Gate Voltage	V_{DS} = 20V, V_{GS} = 0, Pulse Test Duraton = 2ms	30		15		8		mA
$V_{DS(ON)}$	Drain-Source ON Voltage	V_{GS} = 0, I_D = 2.5mA						0.2	V
		I_D = 4mA				0.2			
		I_D = 6.6mA		0.2					

Note: All typical values have been guaranteed by characterization and are not tested.

ITE4091-ITE4093
2N4091-2N4093 JAN, JTXV, JANTX*

INTERSIL

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	2N/ITE 4091		2N/ITE 4092		2N/ITE 4093		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$r_{DS(on)}$	Static Drain-Source ON Resistance	V_{GS} = 0, I_D = 1mA		30		50		80	Ω
$r_{ds(on)}$	Static Drain Source ON Resistance	V_{GS} = 0, I_D = 0, f = 1kHz		30		50		80	Ω
C_{iss}	Common-Source Input Capacitance	V_{DS} = 20V, V_{GS} = 0, f = 1MHz		16		16		16	pF
C_{rss}	JANTX Only	(Note 1)		5		5		5	pF
	Common-Source Reverse Transfer Capacitance	V_{DS} = 0, V_{GS} = −20V, f = 1MHz (Note 1)		5		5		5	pF
$t_{d(ON)}$	Turn-ON Delay Time (Note 1)	V_{DD} = 3V, $V_{GD(ON)}$ = 0		15		15		20	ns
t_r	Rise Time (Note 1)	4091: $I_{D(on)}$ 6.6mA, $V_{GS(off)}$ −12V, R_1 425Ω 4092: 4mA, −8V, 700Ω 4093: 2.5mA, −6V, 1120Ω		10		20		40	ns
t_{off}	Turn-OFF Time (Note 1)			40		60		80	ns

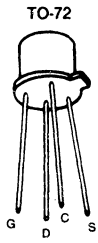
NOTE 1. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

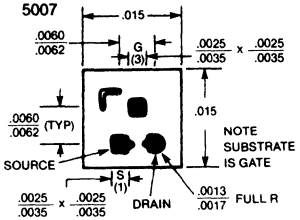
2N4117-19, 2N4117A-19A
N-Channel JFET
General Purpose Amplifier

FEATURES
- **Low Leakage**
- **Low Capacitance**

PIN CONFIGURATION



CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-72	WAFER	CHIP
2N4117	2N4117/W	2N4117/D
2N4117A	—	—
2N4118	2N4118/W	2N4118/D
2N4118A	—	—
2N4119	2N4119/W	2N4119/D
2N4119A	—	—

*When ordering wafer/dice refer to Section 10, page 10-1.

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage ..... -40V
Gate Current 50mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +175°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 300mW
Derate above 25°C ..... 2.0mW/°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	2N4117 2N4117A MIN	2N4117 2N4117A MAX	2N4118 2N4118A MIN	2N4118 2N4118A MAX	2N4119 2N4119A MIN	2N4119 2N4119A MAX	UNIT
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = -1μA, V_{DS} = 0	-40		-40		-40		V
I_{GSS}	Gate Reverse Current	V_{GS} = -20V, V_{DS} = 0		-10		-10		-10	pA
	A devices			-1		-1		-1	
	T_A = +100°C			-25		-25		-25	nA
	A devices			-2.5		-2.5		-2.5	
$V_{GS(off)}$	Gate-Source Pinch-Off Voltage	V_{DS} = 10V, I_D = 1nA	-0.6	-1.8	-1	-3	-2	-6	V
I_{DSS}	Drain Current at Zero Gate Voltage (Note 1)	V_{DS} = 10V, V_{GS} = 0	0.02	0.09	0.08	0.24	0.20	0.60	mA
g_{fs}	Common-Source Forward Transconductance (Note 1)	V_{DS} = 10V, f = 1kHz	70	210	80	250	100	330	μs
g_{fs}	Common-Source Forward Transconductance (Note 2)	V_{GS} = 0, f = 30MHz	60		70		90		μs
g_{os}	Common-Source Output Conductance	V_{DS} = 10V, V_{GS} = 0, f = 1kHz		3		5		10	μs
C_{iss}	Common-Source Input Capacitance (Note 2)	V_{DS} = 10V, V_{GS} = 0, f = 1MHz		3		3		3	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)	V_{DS} = 10V, V_{GS} = 0, f = 1MHz		1.5		1.5		1.5	pF

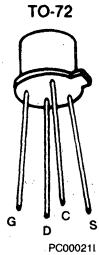
NOTES: 1. Pulse test: Pulse duration of 2ms used during test.
2. For design reference only, not 100% tested.

2N4220-2N4222
N-Channel JFET
General Purpose Amplifier/Switch

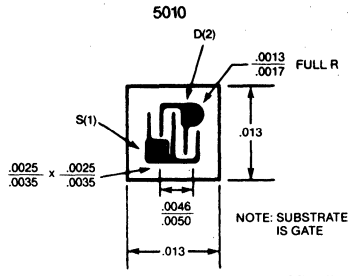
INTERSIL

FEATURES
- C_{rss} < 2pF
- Moderately High Forward Transconductance

PIN CONFIGURATION



CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-72	WAFER	DICE
2N4220	2N4220/W	2N4220/D
2N4221	2N4221/W	2N4221/D
2N4222	2N4222/W	2N4222/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage ..... -30V
Gate Current 10mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +175°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 300mW
Derate above 25°C ..... 2.0mW/°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		2N4220		2N4221		2N4222		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
I_{GSS}	Gate Reverse Current				-0.1		-0.1		-0.1	nA
		T_A = 150°C	V_{GS} = -15V, V_{DS} = 0		-0.1		-0.1		-0.1	μA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = -10μA, V_{DS} = 0		-30		-30		-30		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 15V, I_D = 0.1nA			-4		-6		-8	V
V_{GS}	Gate-Source Voltage	V_{DS} = 15V	I_D = 50μA (2N4220) I_D = 200μA (2N4221) I_D = 500μA (2N4222)	-0.5	-2.5	-1	-5	-2	-6	V
I_{DSS}	Saturation Drain Current (Note 1)	V_{DS} = 15V, V_{GS} = 0		0.5	3	2	6	5	15	mA
g_{fs}	Common-Source Forward Transconductance (Note 1)	V_{DS} = 15V, V_{GS} = 0	f = 1kHz	1000	4000	2000	5000	2500	6000	μs
$\|y_{fs}\|$	Common-Source Forward Transadmittance (Note 2)		f = 100MHz	750		750		750		
g_{os}	Common-Source Output Conductance (Note 1)		f = 1kHz		10		20		40	
C_{iss}	Common-Source Input Capacitance (Note 2)		f = 1MHz		6		6		6	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)				2		2		2	

NOTES: 1. Pulse test duration 2ms.
2. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

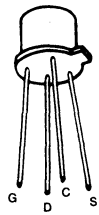
2N4223, 2N4224
N-Channel JFET
High Frequency Amplifier

INTERSIL

FEATURES
- NF = 3dB Typical at 200MHz
- C_{rss} < 2pF

PIN CONFIGURATION

TO-72



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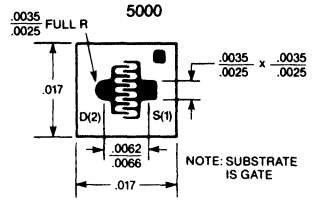
CHIP TOPOGRAPHY



CT00061I

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage ..... -30V
Gate Current 10mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +175°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 300mW
Derate above 25°C ..... 2.0mW/°C

ORDERING INFORMATION*

TO-72	WAFER	DICE
2N4223	2N4223/W	2N4223/D
2N4224	2N4224/W	2N4224/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		2N4223		2N4224		UNIT
				MIN	MAX	MIN	MAX	
I_{GSS}	Gate Reverse Current	V_{GS} = -20V, V_{DS} = 0			-0.25		-0.5	nA
	T_A = +150°C				-0.25		-0.5	μA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = -10μA, V_{DS} = 0		-30		-30		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 15V	I_D = 0.25nA (2N4223) I_D = 0.5nA (2N4224)	-0.1	-8	-0.1	-8	V
V_{GS}	Gate-Source Voltage	V_{DS} = 15V	I_D = 0.3mA (2N4223) I_D = 0.2mA (2N4224)	-1.0	-7.0	-1.0	-7.5	V
I_{DSS}	Saturation Drain Current (Note 1)	V_{DS} = 15V, V_{GS} = 0		3	18	2	20	mA
g_{fs}	Common-Source Forward Transconductance (Note 1)	V_{DS} = 15V, V_{GS} = 0	f = 1kHz	3000	7000	2000	7500	μs
C_{iss}	Common-Source Input Capacitance (Output Shorted)	V_{DS} = 15V, V_{GS} = 0	f = 1MHz		6		6	pF
C_{rss}	Common-Source Reverse Transfer Capacitance	(Note 2)			2		2	pF
$\|y_{fs}\|$	Common-Source Forward Transadmittance	V_{DS} = 15V, V_{GS} = 0 (Note 2)	f = 200MHz	2700		1700		μS
g_{iss}	Common-Source Input Conductance (Output Shorted)				800		800	μS
g_{oss}	Common-Source Output Conductance (Input Shorted)				200		200	μS
G_{ps}	Small Signal Power Gain			10				dB
NF	Noise Figure (Note 2)	V_{DS} = 15V, V_{GS} = 0, R_{gen} = 1kΩ			5			dB

NOTES: 1. Pulse test, duration 2ms.
2. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

2N4338-2N4341
N-Channel JFET
Low Noise Amplifier

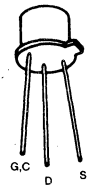
INTERSIL

FEATURES
- Exceptionally High Figure of Merit
- Radiation Immunity
- Extremely Low Noise and Capacitance
- High Input Impedance

APPLICATIONS
- Low-level Choppers
- Data Switches
- Multiplexers and Low Noise Amplifiers

PIN CONFIGURATION

TO-18



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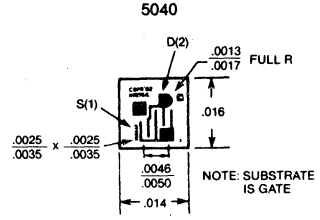
CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-18	WAFER	DICE
2N4338	2N4338/W	2N4338/D
2N4339	2N4339/W	2N4339/D
2N4340	2N4340/W	2N4340/D
2N4341	2N4341/W	2N4341/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage ..... -50V
Gate Current 50mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +175°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 300mW
Derate above 25°C ..... 2.0mW/°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		2N4338		2N4339		2N4340		2N4341		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{GSS}	Gate Reverse Current	V_{GS} = -30V, V_{DS} = 0			-0.1		-0.1		-0.1		-0.1	nA
	T_A = 150°C				-0.1		-0.1		-0.1		-0.1	μA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = -1μA, V_{DS} = 0		-50		-50		-50		-50		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 15V, I_D = 0.1μA		-0.3	-1	-0.6	-1.8	-1	-3	-2	-6	
$I_{D(off)}$	Drain Cutoff Current	V_{DS}=15V, V_{GS} = ( )			0.05 (-5)		0.05 (-5)		0.05 (-5)		0.07 (-10)	nA (V)
I_{DSS}	Saturation Drain Current	V_{DS} = 15V, V_{GS} = 0		0.2	0.6	0.5	1.5	1.2	3.6	3	9	mA
g_{fs}	Common-Source Forward Transconductance	V_{DS} = 15V, V_{GS} = 0	f = 1kHz	600	1800	800	2400	1300	3000	2000	4000	μs
g_{os}	Common-Source Output Conductance				5		15		30		60	
$r_{DS(on)}$	Drain-Source ON Resistance	V_{DS} = 0, I_{DS} = 0			2500		1700		1500		800	ohm
C_{iss}	Common-Source Input Capacitance	V_{DS} = 15V, V_{GS} = 0 (Note 1)	f = 1MHz		7		7		7		7	pF
C_{rss}	Common-Source Reverse Transfer Capacitance				3		3		3		3	
NF	Noise Figure (Note 1)	V_{DS} = 15V, V_{GS} = 0 R_{gen} = 1meg, BW = 200Hz	f = 1kHz		1		1		1		1	dB

NOTE 1: For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

2N4351

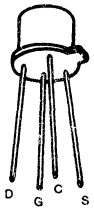
N-Channel Enhancement Mode MOSFET General Purpose Amplifier/Switch

FEATURES

- Low ON Resistance
- Low Capacitance
- High Gain
- High Gate Breakdown Voltage
- Low Threshold Voltage

PIN CONFIGURATION

TO-72



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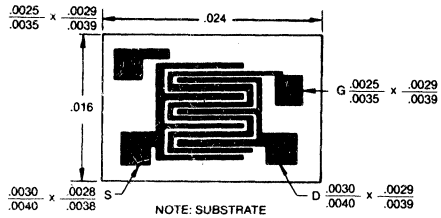
CHIP TOPOGRAPHY

1003



CT00141I

ORDERING INFORMATION*

TO-72	WAFER	DICE
2N4351	2N4351/W	2N4351/D

*When ordering wafer/dice refer to Section 10, page 10–1.

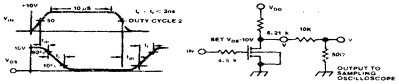
ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Drain-Source Voltage or Drain-Body Voltage 25V
Peak Gate-Source Voltage (Note 1) ..... ±125V
Drain Current 100mA
Storage Temperature Range ..... −65°C to +200°C
Operating Temperature Range ..... −55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 375mW
Derate above 25°C ..... 3mW/°C

2

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted) Substrate connected to source.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage	I_D = 10μA, V_{GS} = 0	25		V
I_{GSS}	Gate Leakage Current	V_{GS} = ±30V, V_{DS} = 0		10	pA
I_{DSS}	Zero-Gate-Voltage Drain Current	V_{DS} = 10V, V_{GS} = 0		10	nA
$V_{GS(th)}$	Gate-Source Threshold Voltage	V_{DS} = 10V, I_D = 10μA	1	5	V
$I_{D(on)}$	'ON' Drain Current	V_{GS} = 10V, V_{DS} = 10V	3		mA
$V_{DS(on)}$	Drain-Source "ON" Voltage	I_D = 2mA, V_{GS} = 10V		1	V
$r_{DS(on)}$	Drain-Source Resistance	V_{GS} = 10V, I_D = 0, f = 1kHz		300	ohms
$\|y_{fs}\|$	Forward Transfer Admittance	V_{DS} = 10V, I_D = 2mA, f = 1kHz	1000		μs
C_{rss}	Reverse Transfer Capacitance (Note 2)	V_{DS} = 0, V_{GS} = 0, f = 1MHz		1.3	pF
C_{iss}	Input Capacitance (Note 2)	V_{DS} = 10V, V_{GS} = 0, f = 1MHz		5.0	
$C_{d(sub)}$	Drain-Substrate Capacitance (Note 2)	$V_{D(SUB)}$ = 10V, f = 1MHz		5.0	
$t_{d(on)}$	Turn-On Delay (Note 2)			45	ns
t_r	Rise Time (Note 2)			65	
$t_{d(off)}$	Turn-Off Delay (Note 2)			60	
t_f	Fall Time (Note 2)			100	

NOTES: 1. Device must not be tested at ±125V more than once or longer than 300ms.
2. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

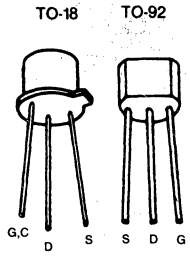
ITE4391-ITE4393
2N4391-2N4393
N-Channel JFET Switch

INTERSIL

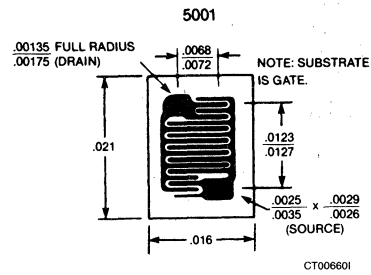
FEATURES

- $r_{ds(on)}$ < 300 Ohms (2N4391)
- $I_{D(OFF)}$ < 100pA
- Switches ±10VAC With ±15V Supplies (2N4392, 2N4393)

PIN CONFIGURATION



CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-92	TO-18	WAFER	DICE
ITE 4391	2N4391	2N4391/W	2N4391/D
ITE 4392	2N4392	2N4392/W	2N4392/D
ITE 4393	2N4393	2N4393/W	2N4393/D

*When ordering wafer/dice refer to Section 10, page 10–1.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage ..... -40V
Gate Current 10mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +200°C
Lead Temperature (Soldering, 10sec) ..... +300°C

	TO-18	TO-92
Power Dissipation	1.8W	360mW
Derate above 25°C	10mW/°C	3.3mW/°C

Plastic
Storage ..... -55°C to +150°C
Operating ..... -55°C to +135°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	4391		4392		4393		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
I_{GSS}	Gate Reverse Current	V_{GS} = -20V, V_{DS} = 0		-100		-100		-100	pA
	T_A = 150°C			-200		-200		-200	nA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = -1μA, V_{DS} = 0	-40		-40		-40		V
$I_{D(off)}$	Drain Cutoff Current	V_{DS} = 20V, V_{GS} = -5V (4393)		100		100		100	pA
	T_A = 150°C	V_{GS} = -7V (4392), V_{GS} = -12V (4391)		200		200		200	nA
$V_{GS(f)}$	Gate-Source Forward Voltage	I_G = 1mA, V_{DS} = 0		1		1		1	V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 20V, I_D = 1nA	-4	-10	-2	-5	-0.5	-3	
I_{DSS}	Saturation Drain Current (Note 1)	V_{DS} = 20V, V_{GS} = 0	50	150	25	75	5	30	mA
$V_{DS(on)}$	Drain-Source ON Voltage	V_{GS} = 0, I_D = 3mA (4393), I_D = 6mA (4392), I_D = 12mA (4391)		0.4		0.4		0.4	V
$r_{DS(on)}$	Static Drain-Source ON Resistance	V_{GS} = 0, I_D = 1mA		30		60		100	Ω
$r_{ds(on)}$	Drain-Source ON Resistance	V_{GS} = 0, I_D = 0, f = 1kHz		30		60		100	Ω

Note: All typical values have been guaranteed by characterization and are not tested.

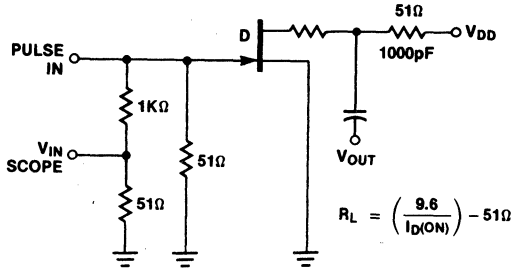
ITE4391-ITE4393 2N4391-2N4393

INTERSIL

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS			4391		4392		4393		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	
C_{iss}	Common-Source Input Capacitance (Note 2)	V_{DS} = 20V, V_{GS} = 0		f = 1MHz		14		14		14	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)	V_{DS} = 0	V_{GS} = −5V							3.5	
			V_{GS} = −7V					3.5			
			V_{GS} = −12V			3.5					
t_d	Turn-ON Delay Time (Note 2)	V_{DD} = 10V, $V_{GS(on)}$ = 0				15		15		15	ns
t_r	Rise Time (Note 2)		$I_{D(on)}$	$V_{GS(off)}$		5		5		5	
t_{off}	Turn-OFF Delay Time (Note 2)	4391	12mA	−12V		20		35		50	
		4392	6	−7							
t_f	Fall Time (Note 2)	4393	3	−5		15		20		30	

NOTES: 1. Pulse test required, pulse width = 300μs, duty cycle ≤ 3%.
2. For design reference only, not 100% tested.



Note: All typical values have been guaranteed by characterization and are not tested.

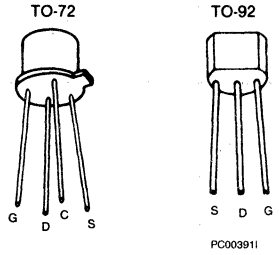
ITE4416, 2N4416/A
N-Channel JFET
High Frequency Amplifier

INTERSIL

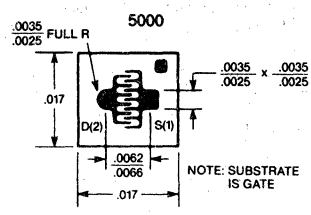
FEATURES

- **Low Noise**
- **Low Feedback Capacitance**
- **Low Output Capacitance**
- **High Transconductance**
- **High Power Gain**

PIN CONFIGURATIONS



CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-92	TO-72	WAFER	DICE
ITE 4416	2N4416	2N4416/W	2N4416/D
—	2N4416A	2N4416A/W	2N4416A/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage
- 2N4416, ITE4416 ..... -30V
- 2N4416A ..... -35V

Gate Current 10mA

Storage Temperature Range
- 2N4416/2N4416A ..... -65°C to +200°C
- ITE4416 ..... -55°C +150°C

Operating Temperature Range
- 2N4416/2N4416A ..... -65°C to +200°C
- ITE4416 ..... -55°C to +135°C

Lead Temperature (Soldering, 10sec) ..... +300°C

Power Dissipation 300mW
- Derate above 25°C .....
- 2N4416/2N4416A ..... 1.7mW/°C
- ITE4416 ..... 2.7mW/°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$V_{GS(f)}$	Gate-Source Forward Voltage		I_G = 1mA, V_{DS} = 0			1	V
I_{GSS}	Gate Reverse Current		V_{GS} = -20V, V_{DS} = 0			-0.1	nA
		T_A = 150°C				-0.1	μA
BV_{GSS}	Gate-Source Breakdown Voltage	2N4416/ITE4416	I_G = -1μA, V_{DS} = 0		-30		V
		2N4416A			-35		
$V_{GS(off)}$	Gate-Source Cutoff Voltage	2N4416/ITE4416	V_{DS} = 15V, I_D = 1nA			-6	
		2N4416A			-2.5	-6	
I_{DSS}	Drain Current at Zero Gate Voltage		V_{DS} = 15V, V_{GS} = 0		5	15	mA
g_{fs}	Common-Source Forward Transconductance			f = 1kHz	4500	7500	μS
g_{os}	Common-Source Output Conductance					50	μs
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 1)			f = 1MHz		0.8	pF
C_{iss}	Common-Source Input Capacitance (Note 1)					4	pF
C_{oss}	Common-Source Output Capacitance (Note 1)					2	

Note: All typical values have been guaranteed by characterization and are not tested.

ITE4416, 2N4416/A

INTERSIL

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	100MHz		400MHz		UNIT
			MIN	MAX	MIN	MAX	
g_{iss}	Common-Source Input Conductance	V_{DS} = 15V, V_{GS} = 0 (Note 1)		100		1000	μS
b_{iss}	Common-Source Input Susceptance			2500		10,000	
g_{oss}	Common-Source Output Conductance			75		100	
b_{oss}	Common-Source Output Susceptance			1000		4000	
g_{fs}	Common-Source Forward Transconductance				4000		
G_{ps}	Common-Source Power Gain	V_{DS} = 15V, I_D = 5mA (Note 1)	18		10		dB
NF	Noise Figure (Note 1)	V_{DS} = 15V, I_D = 5mA, R_G = 1kΩ		2		4	

NOTE 1: For design reference only, not 100% tested.

2

Note: All typical values have been guaranteed by characterization and are not tested.

2N4856-2N4861 2N4856-2N4858 JAN, JTX, JTXV*

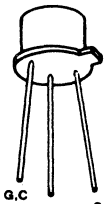
N-Channel JFET Switch

FEATURES

- Low $r_{DS(on)}$
- $I_{D(off)} < 250pA$
- Switches ±10V Signals With ±15V Supplies (2N4858, 2N4861)

PIN CONFIGURATION

TO-18



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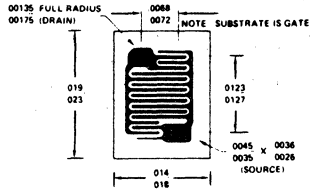
CHIP TOPOGRAPHY

5001



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ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage
- 2N4856–58 ..... −40V
- 2N4859–61 ..... −30V

Gate Current 50mA
Storage Temperature Range ..... −65°C to +200°C
Operating Temperature Range ..... −55°C to +200°C
Led Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 1.8W
Derate above 25°C ..... 10mW/°C

ORDERING INFORMATION*

TO-18	WAFER	DICE
2N4856†	2N4856/W	2N4856/D
2N4857†	2N4857/W	2N4857/D
2N4858†	2N4858/W	2N4858/D
2N4859	2N4859/W	2N4859/D
2N4860	2N4860/W	2N4860/D
2N4861	2N4861/W	2N4861/D

†add JAN, JTX, JTXV, to basic part number to specify these devices.
*When ordering wafer/dice refer to Section 10, page 10-1.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS		2N4856,59		2N4857,60		2N4858,61		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	
BV_{GSS}	Gate-Source Breakdown Voltage	2N4856-58	$I_G = -1\mu A$, $V_{DS} = 0$		−40		−40		−40		V
		2N4859-61			−30		−30		−30		
I_{GSS}	Gate Reverse Current		$V_{GS} = -20V$, $V_{DS} = 0$			−250		−250		−250	pA
		T_A = 150°C	$V_{GS} = -15V$, $V_{DS} = 0$			−500		−500		−500	nA
$I_{D(off)}$	Drain Cutoff Current		$V_{DS} = 15V$, $V_{GS} = -10V$			250		250		250	pA
		T_A = 150°C				500		500		500	nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage		$V_{DS} = 15V$, $I_D = 0.5nA$		−4	−10	−2	−6	−0.8	−4	V
I_{DSS}	Saturation Drain Current (Note 1)		$V_{DS} = 15V$, $V_{GS} = 0$		50		20	100	8	80	mA
$V_{DS(on)}$	Drain-Source ON Voltage		$V_{GS} = 0$, $I_D = (\ )$			0.75 (20)		0.50 (10)		0.50 (5)	V (mA)
$r_{ds(on)}$	Drain-Source ON Resistance		$V_{GS} = 0$, $I_D = 0$	f = 1kHz		25		40		60	ohm

Note: All typical values have been guaranteed by characterization and are not tested.

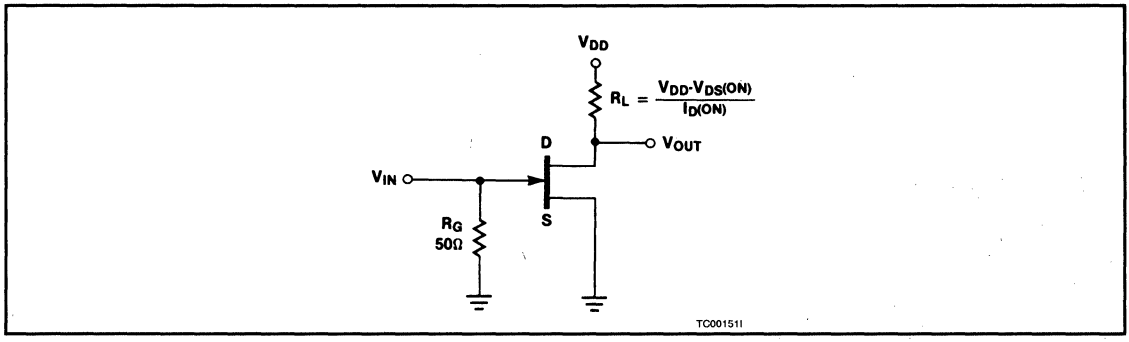
2N4856-2N4861 2N4856-2N4858 JAN, JTX, JTXV*

INTERSIL

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS		2N4856,59		2N4857,60		2N4858,61		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
C_{iss}	Common-Source Input Capacitance	$V_{DS} = 0$, $V_{GS} = -10V$ (Note 2)	f = 1MHz		18		18		18	pF
C_{rss}	Common-Source Reverse Transfer Capacitance				8		8		8	
t_d	Turn-ON Delay Time (Note 2)	$V_{DD} = 10V$, $R_L =$ 464Ω (2N4856,59) 953Ω (2N4857,60) 1910Ω (2N4858,61) $V_{GS(on)} = 0$ $V_{GS(off)} = -10V$, $I_D = 20$ mA (2N4856,9) $V_{GS(off)} = -6V$, $I_D = 10$mA (2N4857,60) $V_{GS(off)} = -4V$, $I_D = 5$mA (2N4858,61)			6		6		10	ns
t_r	Rise Time (Note 2)				3		4		10	
t_{off}	Turn-OFF Time (Note 2)				25		50		100	

NOTES: 1. Pulse test required, pulse width = 100μs, duty cycle ≤ 10%.
2. For design reference only, not 100% tested.



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Note: All typical values have been guaranteed by characterization and are not tested.

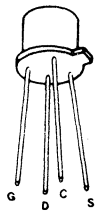
2N4867/A-2N4869/A
N-Channel JFET
Low Noise Amplifier

INTERSIL

FEATURES
- Low Noise Voltage
- Low Leakage
- High Gain

PIN CONFIGURATION

TO-72



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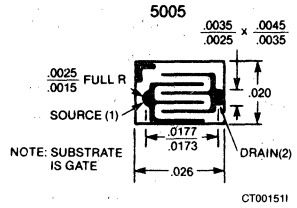
CHIP TOPOGRAPHY



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ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage ..... −40V
Gate Current 50mA
Storage Temperature Range ..... −65°C to +200°C
Operating Temperature Range ..... −55°C to +200°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 300mW
Derate above 25°C ..... 1.7mW/°C

ORDERING INFORMATION*

TO-72	WAFER	DICE
2N4867	2N4867/W	2N4867/D
2N4867A	2N4867A/W	2N4867A/D
2N4868	2N4868/W	2N4868/D
2N4868A	2N4868A/W	2N4868A/D
2N4869	2N4869/W	2N4869/D
2N4869A	2N4869A/W	2N4869A/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		2N4867 2N4867A		2N4868 2N4868A		2N4869 2N4869A		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
I_{GSS}	Gate Reverse Current	V_{GS} = −30V, V_{DS} = 0			−0.25		−0.25		−0.25	nA
	T_A = 150°C				−0.25		−0.25		−0.25	μA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1μA, V_{DS} = 0		−40		−40		−40		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 20V, I_D = 1μA		−0.7	−2	−1	−3	−1.8	−5	
I_{DSS}	Saturation Drain Current (Note 1)	V_{DS} = 20V, V_{GS} = 0		0.4	1.2	1	3	2.5	7.5	mA
g_{fs}	Common-Source Forward Transconductance (Note 1)	V_{DS} = 20V, V_{GS} = 0	f = 1kHz	700	2000	1000	3000	1300	4000	μS
g_{os}	Common-Source Output Conductance				1.5		4		10	
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)		f = 1MHz		5		5		5	pF
C_{iss}	Common-Source Input Capacitance (Note 2)				25		25		25	

Note: All typical values have been guaranteed by characterization and are not tested.

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER		TEST CONDITIONS		2N4867 2N4867A		2N4868 2N4868A		2N4869 2N4869A		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	
$\bar{e}_n$	Short Circuit Equivalent Input Noise Voltage (Note 2)	A devices	V_{DS} = 10V, V_{GS} = 0	f = 10Hz		20		20		20	$\frac{nV}{\sqrt{Hz}}$
				f = 1kHz		10		10		10	
				f = 10Hz		10		10		10	
				f = 1kHz		5		5		5	
NF	Spot Noise Figure (Note 2)		V_{DS} = 10V, V_{GS} = 0 R_{gen} = 20K, (2N4867 Series) R_{gen} = 5K, (2N4867A Series)	f = 1kHz		1		1		1	dB

NOTES: 1. Pulse test duration = 2ms.
2. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

2N5018, 2N5019
P-Channel JFET Switch

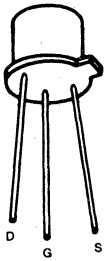
INTERSIL

FEATURES
- Low Insertion Loss
- No Offset or Error Voltages Generated By Closed Switch
- Purely Resistive

APPLICATIONS
- Analog Switches
- Commutators
- Choppers

PIN CONFIGURATION

TO-18



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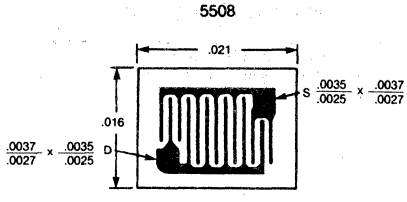
CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-18	WAFER	DICE
2N5018	2N5018/W	2N5018/D
2N5019	2N5019/W	2N5019/D

*When ordering wafer/dice refer to Section 10, page 10–1.

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage 30V
Gate Current 50mA
Storage Temperature Range ..... −65°C to +200°C
Operating Temperature Range ..... −55°C to +200°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 500mW
Derate above 25°C ..... 3mW/°C

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		2N5018		2N5019		UNIT
				MIN	MAX	MIN	MAX	
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = 1μA, V_{DS} = 0		30		30		V
I_{GSSR}	Gate Reverse Current	V_{GS} = 15V, V_{DS} = 0			2		2	nA
$I_{D(off)}$	Drain Cutoff Current	V_{DS} = −15V,	V_{GS} = 12V (2N5018)		−10		−10	nA
	T_A = 150°C		V_{GS} = 7V (2N5019)		−10		−10	μA
I_{DGO}	Drain Reverse Current	V_{DG} = −15V, I_S = 0			−2		−2	nA
	T_A = 150°C				−3		−3	μA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = −15V, I_D = −1μA			10		5	V
I_{DSS}	Saturation Drain Current	V_{DS} = −20V, V_{GS} = 0		−10		−5		mA
$V_{DS(on)}$	Drain-Source ON Voltage	V_{GS} = 0, I_D = −6mA (2N5018), I_D = −3mA (2N5019)			−0.5		−0.5	V
$r_{ds(on)}$	Static Drain-Source ON Resistance	I_D = −1mA, V_{GS} = 0			75		150	Ω
$r_{ds(on)}$	Drain-Source ON Resistance	I_D = 0, V_{GS} = 0	f = 1kHz		75		150	
C_{iss}	Common-Source Input Capacitance (Note 1)	V_{DS} = −15V, V_{GS} = 0	f = 1MHz		45		45	pF
C_{rss}	Common-Source Reserve Transfer Capacitance (Note 1)	V_{DS} = 0, V_{GS} = 12V (2N5018), V_{GS} = 7V (2N5019)	f = 1MHz		10		10	pF

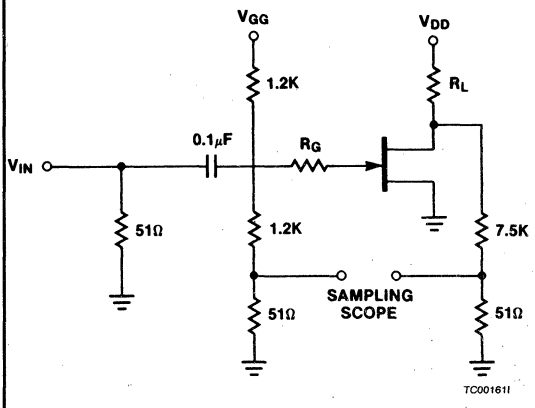
Note: All typical values have been guaranteed by characterization and are not tested.

2N5018, 2N5019

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS				2N5018		2N5019		UNIT
						MIN	MAX	MIN	MAX	
$t_{d(on)}$	Turn-ON Delay Time (Note 1)	V_{DD} = −6V, $V_{GS(on)}$ = 0					15		15	ns
t_r	Rise Time (Note 1)						20		75	
			$V_{GS(off)}$	$I_{D(on)}$	R_L					
$t_{d(off)}$	Turn-off Delay Time (Note 1)	2N5018	12V	−6mA	910Ω		15		25	
t_f	Fall Time (Note 1)	2N5019	7V	−3mA	1.8kΩ		50		100	

NOTES: 1. For design reference only, not 100% tested.



INPUT PULSE
RISE TIME < 1ns
FALL TIME < 1ns
PULSE WIDTH 100ns
REPLETION RATE 1MHz

SAMPLING SCOPE
RISE TIME 0.4ns
INPUT RESISTANCE 10MΩ
INPUT CAPACITANCE 1.5pF

Note: All typical values have been guaranteed by characterization and are not tested.

2N5114-2N5116, JAN, JTX, JTXV
P-Channel JFET Switch

INTERSIL

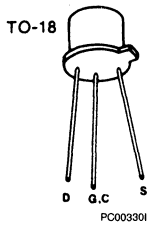
GENERAL DESCRIPTION

Ideal for inverting switching or "Virtual Gnd" switching into inverting input of Op. Amp. No driver is required and ±10VAC signals can be handled using only +5V logic (TTL or CMOS).

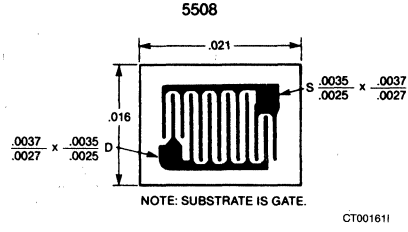
FEATURES

- **Low ON Resistance**
- **$I_{D(off)}$ < 500pA**
- **Switches directly from TTL Logic**

PIN CONFIGURATION



CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO18†	WAFER	DICE
2N5114	2N5114/W	2N5114/D
2N5115	2N5115/W	2N5115/D
2N5116	2N5116/W	2N5116/D

*When ordering wafer/dice refer to Section 10, page 10-1.

†add JAN, JTX, JTXV to basic part number to specify these devices.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage 30V
Gate Current 50mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +200°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 500mW
Derate above 25°C ..... 3mW/°C

SWITCHING CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER	2N5114	2N5115	2N5116	JAN TX 2N5114	JAN TX 2N55115	JAN TX 2N5116	UNIT
	MAX	MAX	MAX	MAX	MAX	MAX	
t_d Turn-ON Delay Time	6	10	12	6	10	25	ns
t_r Rise Time (Note 2)	10	20	30	10	20	35	
t_{off} Turn-OFF Delay Time (Note 2)	6	8	10	6	8	20	
t_f Fall Time (Note 2)	15	30	50	15	30	60	

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	2N5114		2N5115		2N5116		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = 1μA, V_{DS} = 0	30		30		30		V
I_{GSS}	Gate Reverse Current	V_{GS} = 20V, V_{DS} = 0		500		500		500	pA
	T_A = 150°C			1.0		1.0		1.0	μA
$I_{D(off)}$	Drain Cutoff Current	V_{DS} = -15V, V_{GS} = 2N5114 = 12V, 2N5115 = 7V, 2N5116 = 5V		-500		-500		-500	pA
	T_A = 150°C			-1.0		-1.0		-1.0	μA
V_P	Gate-Source Pinch-Off Voltage	V_{DS} = -15V, I_D = -1nA	5	10	3	6	1	4	V

Note: All typical values have been guaranteed by characterization and are not tested.

2N5114-2N5116, JAN, JTX, JTXV

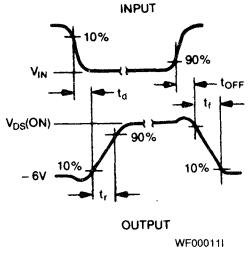
INTERSIL

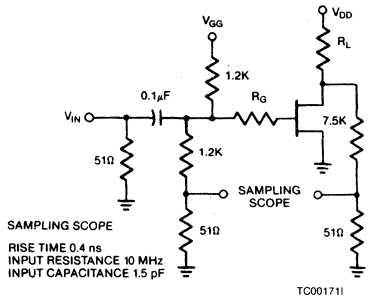
ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	2N5114		2N5115		2N5116		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
I_{DSS}	Drain Current at Zero Gate Voltage (Note 1)	V_{GS} = 0, V_{DS} = 2N5114 = −18V, 2N5115 = −15V, 2N5116 = −15V	−30	−90	−15	−60	−5	−25	mA
$V_{GS(f)}$	Forward Gate-Source Voltage	I_G = −1mA, V_{DS} = 0		−1		−1		−1	V
$V_{DS(on)}$	Drain-Source ON Voltage	V_{GS} = 0, I_D = 2N5114 = −15mA, 2N5115 = −7mA, 2N5116 = −3mA		−1.3		−0.8		−0.6	V
$r_{DS(on)}$	Static Drain-Source ON Resistance	V_{GS} = 0, I_D = −1mA		75		100		150	Ω
$r_{ds(on)}$	Small-Signal Drain-Source ON Resistance	V_{GS} = 0, I_D = 0, f = 1kHz		75		100		150	Ω
	Jan TX only			75		100		175	Ω
C_{iss}	Common-Source Input Capacitance (Note 2)	V_{DS} = −15 V, V_{GS} = 0, f = 1MHz		25		25		25	pF
	Jan TX only			25		25		27	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)	V_{DS} = 0, V_{GS} = 2N5114 = 12V, 2N5115 = 7V, 21N5116 = 5V, f = 1MHz		7		7		7	pF

NOTES: 1. Pulse test; duration = 2ms.
2. For design reference only, not 100% tested.

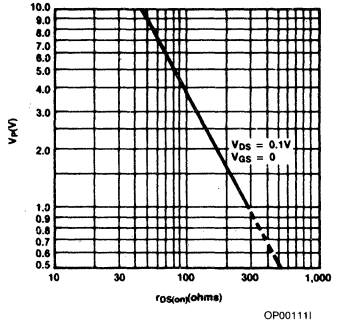
TEST CONDITIONS			
	2N5114	2N5115	2N5116
V_{DD}	−10V	−6V	−6V
V_{GG}	20V	12V	8V
R_L	430Ω	910Ω	2KΩ
R_G	100Ω	220Ω	390Ω
$I_{D(ON)}$	−15mA	−7mA	−3mA
V_{IN}	−12V	−7V	−5V



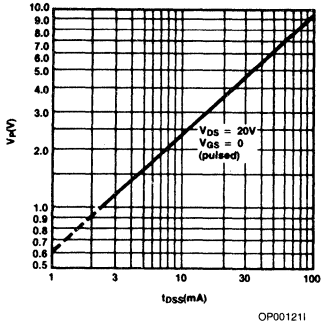


TYPICAL PERFORMANCE CHARACTERISTICS

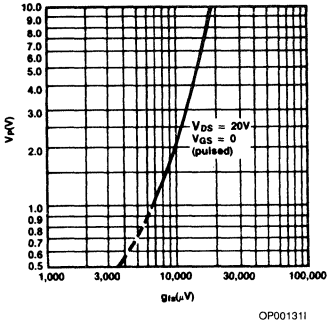
V_p vs $r_{DS(ON)}$



V_p vs I_{DSS}



V_p vs g_{fs}



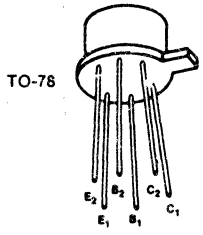
Note: All typical values have been guaranteed by characterization and are not tested.

2N5117-2N5119
Dielectrically Isolated Dual PNP General Purpose Amplifier

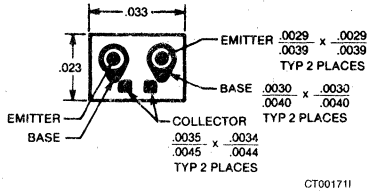
INTERSIL

FEATURES
- High Gain at Low Current
- Low Output Capacitance
- Good h_{FE} Match
- Tight V_{BE} Tracking
- Dielectrically Isolated Matched Pairs for Differential Amplifiers

PIN CONFIGURATION



CHIP TOPOGRAPHY



ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Collector-Base or Collector-Emitter Voltage (Note 1)	-45V
Emitter-Base Voltage (Notes 1 and 2)	-7V
Collector-Collector Voltage	100V
Collector Current (Note 1)	10mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +200°C
Lead Temperature (Soldering, 10sec)	+300°C

	ONE SIDE	BOTH SIDES
Power Dissipation	400mW	750mW
Derate above 25°C	2.3mW/°C	4.3mW/°C

ORDERING INFORMATION*

TO-78	WAFER	DICE
2N5117	2N5117/W	2N5117/D
2N5118	2N5118/W	2N5118/D
2N5119	2N5119/W	2N5119/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	2N5117 2N5118		2N5119		UNIT
			MIN	MAX	MIN	MAX	
h_{FE}	DC Current Gain	I_C = 10μA, V_{CE} = 5.0V	100	300	50		
		I_C = 500μA, V_{CE} = 5.0V	100		50		
	T_A = -55°C	I_C = 10μA, V_{CE} = 5.0V	30		20		
I_{CBO}	Collector Cutoff-Current	I_E = 0, V_{CB} = 30V		0.1		0.1	nA
	T_A = 150°C			0.1		0.1	μA
I_{EBO}	Emitter Cutoff Current	I_C = 0, V_{EB} = 5.0V		0.1		0.1	nA
$I_{C_1-C_2}$	Collector-Collector Leakage	V_{CC} = 100V		5.0		5.0	pA
GBW	Current Gain Bandwith Product (Note 4)	I_C = 500μA, V_{CE} = 10V	100		100		MHz
C_{ob}	Output Capacitance (Note 4)	I_E = 0, V_{CB} = 5.0V, f = 1MHz		0.8		0.8	pF
C_{te}	Emitter Transition Capacitance (Note 4)	I_C = 0, V_{EB} = 0.5V, f = 1MHz		1.0		1.0	
$C_{C_1-C_2}$	Collector-Collector Capacitance (Note 4)	V_{CC} = 0, f = 1MHz		0.8		0.8	
$V_{CEO(sust)}$	Collector-Emitter Sustaining Voltage	I_C = 1.0mA, I_B = 0	45		45		V
NF	Narrow Band Noise Figure (Note 4)	I_C = 10μA, V_{CE} = 5.0V, BW = 200Hz; f = 1kHz, R_G = 10kΩ		4.0		4.0	dB
BV_{CBO}	Collector Base Breakdown Voltage	I_C = 10μA, I_E = 0	45		45		V
BV_{EBO}	Emitter Base Breakdown Voltage	I_E = 10μA, I_C = 0	7.0		7.0		V

Note: All typical values have been guaranteed by characterization and are not tested.

2N5117-2N5119

INTERSIL

MATCHING CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		2N5117		2N5118		2N5119		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
h_{FE_1}/h_{FE_2}	DC Current Gain Ratio (Note 3)	I_C = 10μA to 500μA, V_{CE} = 5V		0.9	1.0					
		I_C = 10μA, V_{CE} = 5.0V				0.85	1.0	0.8	1.0	
V_{BE_1}-V_{BE_2}	Base-Emitter Voltage Differential	I_C = 10μA to 500μA, V_{CE} = 5V			3.0					mV
		I_C = 10μA, V_{CE} = 5.0V					5.0		5.0	
I_{B_1}-I_{B_2}	Base Current Differential				10.0		15		40	nA
$\triangle(V_{BE_1}-V_{BE_2})/\triangle T$	Base Voltage Differential Change with Temperature	I_C = 10μA, V_{CE} = 5.0V	T_A = −55°C to +125°C		3.0		5.0		10	μV/°C
$\triangle(I_{B_1}-I_{B_2})/\triangle T$	Base-Current Differential Change with Temperature		T_A = −55°C to +125°C		0.3		0.5		1.0	nA/°C

NOTES: 1. Per transistor.
2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10μA.
3. Lower of two h_{FE} readings is defined as h_{FE_1}.
4. For design reference only, not 100% tested.

2

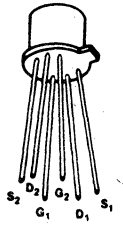
Note: All typical values have been guaranteed by characterization and are not tested.

2N5196-2N5199
Dual N-Channel JFET General Purpose Amplifier

INTERSIL

PIN CONFIGURATION

TO-71



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CHIP TOPOGRAPHY

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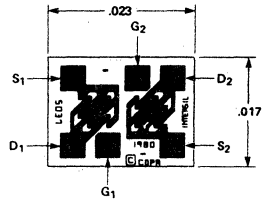


ALL BOND PADS ARE 4 x 4 MIL.

CT000701

ORDERING INFORMATION*

TO-71	WAFER	DICE
2N5196	2N5196/W	2N5196/D
2N5197	2N5197/W	2N5197/D
2N5198	2N5198/W	2N5198/D
2N5199	2N5199/W	2N5199/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage (Note 1) ..... -50V
Gate Current (Note 1) 50mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C

	ONE SIDE	BOTH SIDES
Power Dissipation (T_A = 85°C)	250mW	500mW
Derate above 25°C.....	2.6mW/°C	4.3mW/°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
I_{GSS}	Gate Reverse Current	V_{GS} = -30V, V_{DS} = 0			-25	pA
	T_A = 150°C				-50	nA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = -1μA, V_{DS} = 0		-50		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 20V, I_D = 1nA		-0.7	-4	
V_{GS}	Gate-Source Voltage	V_{DG} = 20V, I_D = 200μA		-0.2	-3.8	
I_G	Gate Operating Current				-15	pA
	T_A = 125°C				-15	nA
I_{DSS}	Saturation Drain Current (Note 2)	V_{DS} = 20V, V_{GS} = 0		0.7	7	mA
g_{fs}	Common-Source Forward Transconductance (Note 2)	V_{DS} = 20V, V_{GS} = 0	f = 1kHz	1000	4000	μs
g_{fs}	Common-Source Forward Transconductance (Note 2)	V_{DG} = 20V, I_D = 200μA		700	1600	
g_{os}	Common-Source Output Conductance (Note 2)	V_{DS} = 20V, V_{GS} = 0			50	
g_{os}	Common-Source Output Conductance (Note 2)	V_{DG} = 20V, I_D = 200μA			4	
C_{iss}	Common-Source Input Capacitance (Note 4)	V_{DS} = 20V, V_{GS} = 0	f = 1MHz		6	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 4)				2	
NF	Spot Noise Figure (Note 4)		f = 100Hz, R_G = 10MΩ		0.5	dB
$\bar{e}_n$	Equivalent Input Noise Voltage (Note 4)		f = 1kHz		20	$\frac{\mu nV}{\sqrt{Hz}}$

Note: All typical values have been guaranteed by characterization and are not tested.

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS		2N5196		2N5197		2N5198		2N5199		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current	V_{DG} = 20V, I_D = 200μA	125°C		5		5		5		5	nA
I_{DSS1}/I_{DSS2}	Saturation Drain Current Ratio (Note 2)	V_{DS} = 20V, V_{GS} = 0V		0.95	1	0.95	1	0.95	1	0.95	1	
g_{fs1}/g_{fs2}	Transconductance Ratio (Note 2)	V_{DG} = 20V, I_D = 200μA	f = 1kHz	0.97	1	0.97	1	0.95	1	0.95	1	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage				5		5		10		15	mV
$\frac{\triangle\lvert V_{GS1}-V_{GS2}\rvert}{\triangle T}$	Gate-Source Differential Voltage		T_A = 25°C, T_B = 125°C		5		10		20		40	μV/°C
	Change with Temperature (Note 3)		T_A = −55°C, T_B = 25°C		5		10		20		40	
$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		f = 1kHz		1		1		1		1	μs

NOTES: 1. Per transistor.
2. Pulse test required, pulsewidth = 300μs, duty cycle < 3%.
3. Measured at endpoints T_A and T_B.
4. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

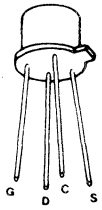
2N5397, 2N5398
N-Channel JFET
High Frequency Amplifier

INTERSIL

FEATURES
- G_{ps} = 15dB Minimum (Common Gate) at 450MHz
- Low Noise
- Low Capacitance

PIN CONFIGURATION

TO-72



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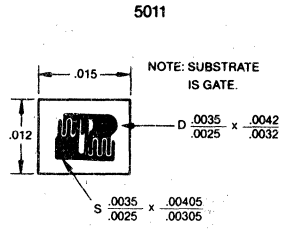
CHIP TOPOGRAPHY



ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Drain-Gate Voltage 25V
Drain-Source Voltage 25V
Continuous Forward Gate Current 10mA
Storage Temperature Range ..... −65°C to +200°C
Operating Temperature Range ..... −55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 300mW
Derate above 25°C ..... 2.4mW/°C

ORDERING INFORMATION*

TO-72	WAFER	DICE
2N5397	2N5397/W	2N5397/D
2N5398	2N5398/W	2N5398/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		2N5397		2N5398		UNIT
				MIN	MAX	MIN	MAX	
I_{GSS}	Gate Reverse Current	V_{GS} = −15V, V_{DS} = 0			−0.1		0.1	nA
	T_A = +150°C		150°C		−0.1		−0.1	μA
BV_{GSS}	Gate-Source Breakdown Voltage	V_{DS} = 0, I_G = −1μA		−25		−25		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 10V, I_D = 1nA		−1.0	−6.0	−1.0	−6.0	
I_{DSS}	Saturation Drain Current (Note 1)	V_{DS} = 10V, V_{DS} = 0		10.	30	5	40	mA
$V_{GS(f)}$	Gate-Source Forward Voltage	V_{DS} = 0, I_G = 1mA			1		1	V
g_{fs}	Common-Source Forward Transconductance (Note 1)	V_{DS} = 10V, I_D = 10mA	f = 1kHz	6000	10,000			μs
		V_{DS} = 10V, V_{GS} = 0				5500	10,000	
g_{oss}	Common-Source Output Conductance	V_{DS} = 10V, I_D = 10mA			200			
		V_{DS} = 10V, V_{GS} = 0					400	
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)	V_{DS} = 10V, I_D = 10mA	f = 1MHz		1.2			pF
		V_{DS} = 10V, V_{GS} = 0					1.3	
C_{iss}	Common-Source Input Capacitance (Note 2)	V_{DG} = 10V, I_D = 10mA			5.0			
		V_{DS} = 10V, V_{GS} = 0					5.5	

Note: All typical values have been guaranteed by characterization and are not tested.

2N5397, 2N5398

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS		2N5397		2N5398		UNIT
				MIN	MAX	MIN	MAX	
g_{iss}	Common-Source Input Conductance (Note 2)	V_{DG} = 10V, I_D = 10mA	f = 450MHz		2000			μs
		V_{DG} = 10V, V_{GS} = 0					3000	
g_{oss}	Common-Source Output Conductance (Note 2)	V_{DG} = 10V, I_D = 10mA			400			
		V_{DS} = 10V, V_{GS} = 0					500	
g_{fs}	Common-Source Forward Transconductance (Note 1, 2)	V_{DG} = 10V, I_D = 10mA		5500	9000			
		V_{DS} = 10V, V_{GS} = 0				5000	10,000	
G_{ps}	Common-Source Power Gain (neutralized)	V_{DG} = 10V, I_D = 10mA (Note 2)		15				dB
NF	Common-Source, Spot Noise Figure (neutralized)				3.5			

NOTES: 1. Pulse test duration = 2ms
2. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

2N5432-2N5434
N-Channel JFET Switch

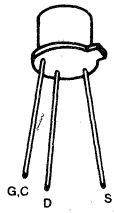
INTERSIL

FEATURES

- Low $r_{ds(on)}$
- Excellent Switching
- Low Cutoff Current

PIN CONFIGURATION

TO-52



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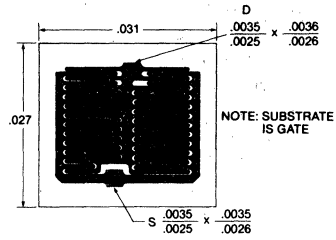
CHIP TOPOGRAPHY

5018



CT00201I

ORDERING INFORMATION*

TO-52	WAFER	DICE
2N5432	2N5432/W	2N5432/D
2N5433	2N5433/W	2N5433/D
2N5434	2N5434/W	2N5434/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source Voltage ..... -25V
Gate-Drain Voltage ..... -25V
Gate Current 100mA
Drain Current 400mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 300mW
Derate above 25°C ..... 2.3mW/°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

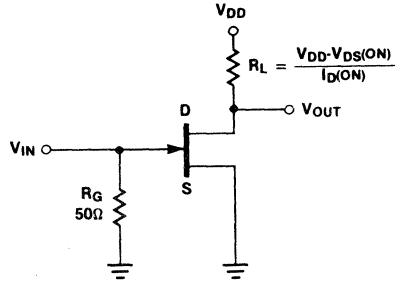
SYMBOL	PARAMETER	TEST CONDITIONS		2N5432		2N5433		2N5434		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
I_{GSS}	Gate Reverse Current	V_{GS} = -15V, V_{DS} = 0			-200		-200		-200	pA
	T_A = 150°C				-200		-200		-200	nA
BV_{GSS}	Gate Source Breakdown Voltage	I_G = -1μA, V_{DS} = 0		-25		-25		-25		V
$I_{D(off)}$	Drain Cutoff Current	V_{DS} = 5V, V_{GS} = -10V			200		200		200	pA
	T_A = 150°C				200		200		200	nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 5V, I_D = 3nA		-4	-10	-3	-9	-1	-4	V
I_{DSS}	Saturation Drain Current (Note 1)	V_{DS} = 15V, V_{GS} = 0		150		100		30		mA
$r_{DS(on)}$	Static Drain-Source ON Resistance	V_{GS} = 0, I_D = 10mA		2	5		7		10	ohm
$V_{DS(on)}$	Drain-Source ON Voltage				50		70		100	mV
$r_{ds(on)}$	Drain-Source ON Resistance	V_{GS} = 0, I_D = 0	f = 1kHz		5		7		10	ohm
C_{iss}	Common-Source Input Capacitance (Note 2)	V_{DS} = 0, V_{GS} = -10V	f = 1MHz		30		30		30	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)				15		15		15	

Note: All typical values have been guaranteed by characterization and are not tested.

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	2N5432		2N5433		2N5434		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_d	Turn-ON Delay Time (Note 2)	V_{DD} = 1.5V,		4		4		4	ns
t_r	Rise Time (Note 2)	$V_{GS(on)}$ = 0,		1		1		1	
t_{off}	Turn-OFF Delay Time (Note 2)	$V_{GS(off)}$ = −12V		6		6		6	
t_f	Fall Time (Note 2)	$I_{D(on)}$ = 10mA		30		30		30	

NOTES: 1. Pulse test required, pulsewidth 300μs, duty cycle ≤ 3%.
2. For design reference only, not 100% tested.



Note: All typical values have been guaranteed by characterization and are not tested.

2N5452-2N5454
Dual N-Channel JFET General Purpose Amplifier

INTERSIL

GENERAL DESCRIPTION

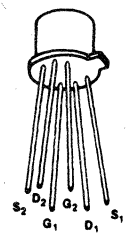
Matched FET pairs for differential amplifiers. This family of general purpose FETs is characterized for low and medium frequency differential amplifier applications requiring low drift and low offset voltage.

FEATURES

- **Low Offset Voltage**
- **Low Drift**
- **Low Capacitance**
- **Low Output Conductance**

PIN CONFIGURATION

TO-71



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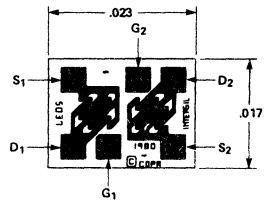
CHIP TOPOGRAPHY

6037



ALL BOND PADS ARE 4 x 4 MIL.

CT00070I

ORDERING INFORMATION*

TO-71	WAFER	DICE
2N5452	2N5452/W	2N5452/D
2N5453	2N5453/W	2N5453/D
2N5454	2N5454/W	2N5454/D

*When ordering wafer/dice refer to Section 10, page 10–1.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source or Gate Drain Voltage (Note 1) ..... −50V
Gate Current (Note 1) 50mA
Storage Temperature Range ..... −65°C to +200°C
Operating Temperature Range ..... −55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C

	ONE SIDE	BOTH SIDES
Power Dissipation (T_C = 85°C)	250mW	500mW
Derate above 25°C.....	2.9mW/°C	4.3mW/°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		2N5452		2N5453		2N5454		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
I_{GSS}	Gate Reverse Current	V_{GS} = −30V, V_{DS} = 0			−100		−100		−100	pA
	T_A = 150°C				−200		−200		−200	nA
BV_{GSS}	Gate-Source Breakdown Voltage	V_{DS} = 0, I_G = −1μA		−50		−50		−50		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 20V, I_D = 1nA		−1	−4.5	−1	−4.5	−1	−4.5	
V_{GS}	Gate-Source Voltage	V_{DS} = 20V, I_D = 50μA		−0.2	−4.2	−0.2	−4.2	−0.2	−4.2	
$V_{GS(f)}$	Gate-Source Forward Voltage	V_{DS} = 0, I_G = 1mA			2		2		2	
I_{DSS}	Saturation Drain Current	V_{DS} = 20V, V_{GS} = 0		0.5	5.0	0.5	5.0	0.5	5.0	mA
g_{fs}	Common-Source Forward Transconductance (Note 2)	V_{DS} = 20V, V_{GS} = 0	f = 1kHz	1000	3000	1000	3000	1000	3000	μs
			f = 100MHz	1000		1000		1000		
g_{os}	Common-Source Output Conductance	V_{DS} = 20V, I_D = 200μA	f = 1kHz		3.0		3.0		3.0	
					1.0		1.0		1.0	
C_{iss}	Common-Source Input Capacitance (Note 2)	V_{DS} = 20V, V_{GS} = 0	f = 1MHz		4.0		4.0		4.0	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)				1.2		1.2		1.2	
C_{dgo}	Drain-Gate Capacitance (Note 2)	V_{DG} = 10V, I_S = 0			1.5		1.5		1.5	

Note: All typical values have been guaranteed by characterization and are not tested.

2N5452-2N5454

INTERSIL

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS		2N5452		2N5453		2N5454		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage	V_{DS} = 20V, V_{GS} = 0	f = 1kHz		20		20		20	$\frac{nV}{\sqrt{Hz}}$
NF	Common-Source Spot Noise Figure (Note 2)	V_{DS} = 20V, V_{GS} = 0 R_G = 10MΩ	f = 100Hz		0.5		0.5		0.5	dB
I_{DSS1}/I_{DSS2}	Drain Saturation Current Ratio	V_{DS} = 20V, V_{GS} = 0		0.95	1.0	0.95	1.0	0.95	1.0	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage	V_{DS} = 20V, I_D = 200μA			5.0		10.0		15.0	mV
$\Delta\lvert V_{GS1}-V_{GS2}\rvert$	Gate-Source Voltage Differential Change with Temperature		T = 25°C to −55°C		0.4		0.8		2.0	
			T = 25°C to +125°C		0.5		1.0		2.5	
g_{fs1}/g_{fs2}	Transconductance Ratio			0.97	1.0	0.97	1.0	0.95	1.0	
$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		f = 1kHz		0.25		0.25		0.25	μS

NOTES: 1. Per transistor.
2. For design reference only, not 100% tested.

2

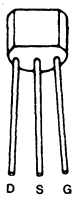
Note: All typical values have been guaranteed by characterization and are not tested.

2N5457-2N5459
N-Channel JFET
General Purpose Amplifier/Switch

INTERSIL

PIN CONFIGURATION

TO-92



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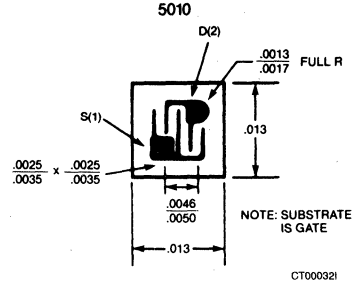
CHIP TOPOGRAPHY



CT000321

ORDERING INFORMATION*

TO-92	WAFER	DICE
2N5457	2N5457/W	2N5457/D
2N5458	2N5458/W	2N5458/D
2N5459	2N5459/W	2N5459/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Drain-Gate Voltage 25V
Drain-Source Voltage 25V
Continuous Forward Gate Current 10mA
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range ..... -55°C to +135°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 310mW
Derate above 25°C ..... 2.82mW/°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{GSS}	Gate-Source Breakdown Voltage		I_G = -10μA, V_{DS} = 0	-25	-60		V
I_{GSS}	Gate Reverse Current		V_{GS} = -15V, V_{DS} = 0		.05	-1.0	nA
			V_{GS} = -15V, V_{DS} = 0, T_A = 100°C			-200	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	2N5457	V_{DS} = 15V, I_D = 10nA	-0.5		-6.0	V
		2N5458		-1.0		-7.0	
		2N5459		-2.0		-8.0	
V_{GS}	Gate-Source Voltage	2N5457	V_{DS} = 15V, I_D = 100μA		-2.5		V
		2N5458	V_{DS} = 15V, I_D = 200μA		-3.5		
		2N5459	V_{DS} = 15V, I_D = 400μA		-4.5		
I_{DSS}	Zero-Gate-Voltage Drain Current (Note 1)	2N5457	V_{DS} = 15V, V_{GS} = 0	1.0	3.0	5.0	mA
		2N5458		2.0	6.0	9.0	
		2N5459		4.0	9.0	16	
$\|y_{fs}\|$	Forward Transfer Admittance	2N5457	V_{DS} = 15V, V_{GS} = 0, f = 1kHz	1000	3000	5000	μs
		2N5458		1500	4000	5500	
		2N5459		2000	4500	6000	
$\|y_{os}\|$	Output Admittance		V_{DS} = 15V, V_{GS} = 0, f = 1kHz		10	50	μs
C_{iss}	Input Capacitance (Note 2)		V_{DS} = 15V, V_{GS} = 0, f = 1MHz		4.5	7.0	pF
C_{rss}	Reverse Transfer Capacitance (Note 2)		V_{DS} = 15V, V_{GS} = 0, f = 1MHz		1.5	3.0	pF
NF	Noise Figure (Note 2)		V_{DS} = 15V, V_{GS} = 0, R_G = 1MHz BW = 1Hz, f = 1kHz			3.0	dB

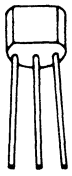
NOTES: 1. Pulse test required. PW ≤ 630ms, duty cycle ≤ 10%
2. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

2N5460-2N5465
P-Channel JFET
Low Noise Amplifier

PIN CONFIGURATION

TO-92



S D G

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CHIP TOPOGRAPHY

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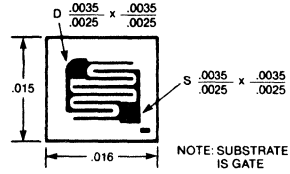


CT00211I

ORDERING INFORMATION*

TO-92	WAFER	DICE
2N5460	2N5460/W	2N5460/D
2N5461	2N5461/W	2N5461/D
2N5462	2N5462/W	2N5462/D
2N5463	2N5463/W	2N5463/D
2N5464	2N5464/W	2N5464/D
2N5465	2N5465/W	2N5465/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Drain-Gate or Source-Gate Voltage
- 2N5460 - 2N5462 ..... -40V
- 2N5463 - 2N5465 ..... -60V

Gate Current 10mA
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range ..... -55°C to +135°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 310mW
Derate above 25°C ..... 2.82mW/°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
BV_{GSS}	Gate-Source Breakdown Voltage	2N5460, 2N5461, 2N5462	I_G = 10μA, V_{DS} = 0		40			V
		2N5463, 2N5464, 2N5465			60			
$V_{GS(off)}$	Gate-Source Cutoff Voltage	2N5460, 2N5463	V_{DS} = -15V, I_D = 1.0μA		0.75		6.0	V
		2N5461, 2N5464			1.0		7.5	
		2N5462, 2N5465			1.8		9.0	
I_{GSS}	Gate Reverse Current	2N5460, 2N5461, 2N5462	V_{DS} = 0	V_{GS} = 20V			5.0	nA
		2N5463, 2N5464, 2N5465		V_{GS} = 30V			5.0	
	T_A = 100°C	2N5460, 2N5461, 2N5462		V_{GS} = 20V			1.0	μA
		2N5463, 2N5464, 2N5465		V_{GS} = 30V			1.0	
I_{DSS}	Zero-Gate Voltage Drain Current	2N5460, 2N5463	V_{DS} = -15V		-1.0		-5.0	mA
		2N5461, 2N5464			-2.0		-9.0	
		2N5462, 2N5465		V_{GS} = 0	-4.0		-16	
V_{GS}	Gate-Source Voltage	2N5460, 2N5463		I_D = 0.1mA	0.5		4.0	V
		2N5461, 2N5464		I_D = -0.2mA	0.8		4.5	
		2N5462, 2N5465		I_D = -0.4mA	1.5		6.0	
g_{fs}	Forward Transadmittance	2N5460, 2N5463	V_{DS} = -15V V_{GS} = 0V	f = 1.0kHz	1000		4000	μs
		2N5461, 2N5464			1500		5000	
		2N5462, 2N5465			2000		6000	
g_{os}	Output Admittance						75	μS
C_{iss}	Input Capacitance (Note 1)					5.0	7	pF
C_{rss}	Reverse Transfer Capacitance (Note 1)			f = 1MHz		1.0	2.0	pF
NF	Common-Source Noise Figure (Note 1)			f = 100Hz		1.0	2.5	DB
$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage (Note 1)			BW = 1.0Hz R_G = 1.0MΩ		60	115	nV/√Hz

NOTE 1: For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

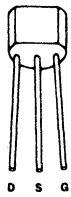
2N5484-2N5486
N-Channel JFET
High Frequency Amplifier

INTERSIL

FEATURES
- Up to 400MHz Operation
- Economy Packaging
- C_{rss} < 1.0pF

PIN CONFIGURATION

TO-92



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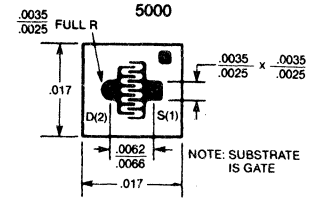
CHIP TOPOGRAPHY



CT002211

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise specified)

Drain-Gate Voltage 25V
Source Gate Voltage 25V
Drain Current 30mA
Forward Gate Current 10mA
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range ..... −55°C to +135°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 310mW
Derate above 25°C ..... 2.82mW/°C

ORDERING INFORMATION*

TO-92	WAFER	DICE
2N5484	2N5484/W	2N5484/D
2N5485	2N5485/W	2N5485/D
2N5486	2N5486/W	2N5486/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		2N5484		2N5485		2N5486		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
I_{GSS}	Gate Reverse Current				−1.0		−1.0		−1.0	nA
		T_A = 100°C	V_{GS} = −20V, V_{DS} = 0		−200		−200		−200	
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1μA, V_{DS} = 0		−25		−25		−25		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 15V, I_D = 10nA		−0.3	−3.0	−0.5	−4.0	−2.0	−6.0	V
I_{DSS}	Saturation Drain Current	V_{DS} = 15V, V_{GS} = 0 (Note 1)		1.0	5.0	4.0	10	8.0	20	mA
g_{fs}	Common-Source Forward Transconductance	V_{DS} = 15V, V_{GS} = 0	f = 1kHz	3000	6000	3500	7000	4000	8000	μs
g_{os}	Common-Source Output Conductance				50		60		75	
$Re_{(yfs)}$	Common-Source Forward Transconductance (Note 2)		f = 100MHz	2500						
			f = 400MHz			3000		3500		
$Re_{(yos)}$	Common-Source Output Conductance (Note 2)		f = 100MHz		75					
			f = 400MHz				100		100	
$Re_{(yis)}$	Common-Source Input Conductance (Note 2)		f = 100MHz		100					
			f = 400MHz				1000		1000	
C_{iss}	Common-Source Input Capacitance (Note 2)		f = 1MHz		5.0		5.0		5.0	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)				1.0		1.0		1.0	
C_{oss}	Common-Source Output Capacitance (Note 2)				2.0		2.0		2.0	

Note: All typical values have been guaranteed by characterization and are not tested.

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS		2N5484		2N5485		2N5486		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
NF	Noise Figure (Note 2)	V_{DS} = 15V, V_{GS} = 0, R_G = 1MΩ	f = 1kHz		2.5		2.5		2.5	dB
		V_{DS} = 15V, V_D = 1mA, R_G = 1kΩ	f = 100MHz		3.0					
							2.0		2.0	
		V_{DS} = 15V, I_D = 4mA, R_G = 1kΩ	f = 400MHz				4.0		4.0	
G_{ps}	Common-Source Power Gain (Note 2)	V_{DS} = 15V, I_D = 1mA	f = 100MHz	16	25					
		V_{DS} = 15V, I_D = 4mA	f = 100MHz			18	30	18	30	
			f = 400MHz			10	20	10	20	

NOTES: 1. Pulse test required. Pulse width = 300μs, duty cycle ≤ 3%.
2. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

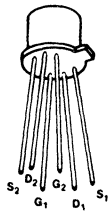
2N5515-2N5524
Dual N-Channel JFET Low Noise Amplifier

INTERSIL

FEATURES
- Tight Temperature Tracking
- Tight Matching
- High Common Mode Rejection
- Low Noise

PIN CONFIGURATION

TO-71



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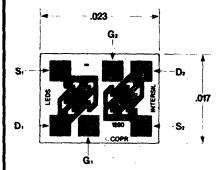
6037



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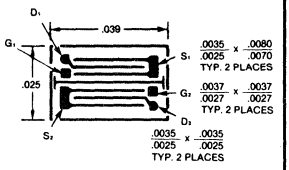
6019



ALL BOND PADS ARE 4 x 4 MIL.

CT005711

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise specified)

Gate-Source or Gate-Drain Voltage ..... −40V
Gate Current (Note 1) 50mA
Storage Temperature Range ..... −65°C to +200°C
Operating Temperature Range ..... −55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C

	ONE SIDE	BOTH SIDES
Power Dissipation (T_A = 85°C)	250mW	375mW
Derate above 25°C.....	2.0mW/°C	3.0mW/°C

NOTE: Per transistor.

ORDERING INFORMATION*

TO-72	WAFER	DICE
2N5515	2N5515/W	2N5515/D
2N5516	2N5516/W	2N5516/D
2N5517	2N5517/W	2N5517/D
2N5518	2N5518/W	2N5518/D
2N5519	2N5519/W	2N5519/D
2N5520		
2N5521		
2N5522		
2N5523		
2N5524		

*When ordering wafer/dice refer to Section 10, page 10-1.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
I_{GSS}	Gate Reverse Current	V_{GS} = −30V, V_{DS} = 0			−250	pA
	T_A = 150°C				−250	nA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1μA, V_{DS} = 0		−40		V
V_P	Gate-Source Pinch-Off Voltage	V_{DS} = 20V, I_D = 1nA		−0.7	−4	V
I_{DSS}	Drain Current at Zero Gate Voltage (Note 1)	V_{DS} = 20V, V_{GS} = 0		0.5	7.5	mA
g_{fs}	Common-Source Forward Transconductance (Note 1)		f = 1kHz	1000	4000	μs
g_{oss}	Common-Source Output Conductance				10	
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 3)		f = 1MHz		5	pF
C_{iss}	Common-Source Input Capacitance (Note 3)				25	

Note: All typical values have been guaranteed by characterization and are not tested.

2N5515-2N5524

INTERSIL

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$\bar{e}_n$	Equivalent Input Noise Voltage (Note 3)	2N5515-19	V_{DG} = 20V, I_D = 200μA	f = 10Hz		30	nV/√Hz
		2N5520-24				15	
		2N5515-24		f = 1kHz		10	
I_G	Gate Current					-100	pA
		T_A = 125°C				-100	nA
V_{GS}	Gate Source Voltage				-0.2	-3.8	V
g_{fs}	Common-Source Forward Transconductance (Note 1)			f = 1kHz	500	1000	μs
g_{oss}	Common-Source Output Conductance					1	μs

MATCHING CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	2N5515,20		2N5516,21		2N5517,22		2N5518,23		2N5519,24		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{DSS1}/I_{DSS2}	Drain Current Ratio at Zero Gate Voltage (Note 1)	V_{DS} = 20V, V_{GS} = 0	0.95	1	0.95	1	0.95	1	0.95	1	0.90	1	
$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Current (+125°C)	V_{DG} = 20V, I_D = 200μA		10		10		10		10		10	nA
g_{fs1}/g_{fs2}	Transconductance Ratio (Note 1)	V_{DG} = 20V, I_D = 200μA f = 1kHz	0.97	1	0.97	1	0.95	1	0.95	1	0.90	1	
$\lvert g_{oss1} - g_{oss2} \rvert$	Differential Output Conductance	V_{DG} = 20V, I_D = 200μA f = 1kHz		0.1		0.1		0.1		0.1		0.1	μs
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage	V_{DG} = 20V, I_D = 200μA		5		5		10		15		15	mV
$\frac{\Delta\lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (T_A = -55°C to +125°C)	V_{DG} = 20V, I_D = 200μA		5		10		20		40		80	μV/°C
CMRR	Common Mode Rejection Ratio (Note 2, 3)	V_{DD} = 10 to 20V, I_D = 200μA	100		100		90						dB

NOTES: 1. Pulse duration of 28ms used during test.
2. CMRR = 20 $\log_{10}\Delta V_{DD}/\Delta\lvert V_{GS1} - V_{GS2}\rvert$, ($\Delta V_{DD}$ = 10V)
3. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

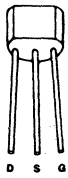
2N5638-2N5640
N-Channel JFET Switch

INTERSIL

FEATURES
- Economy Packaging
- Fast Switching
- Low Drain-Source 'ON' Resistance

PIN CONFIGURATION

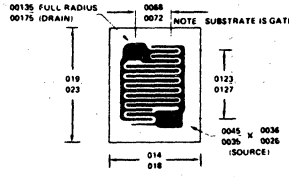
TO-92



PC00340I

CHIP TOPOGRAPHY

5001



CT00090I

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise specified)

Drain-Source Voltage 30V
Drain-Gate Voltage 30V
Source-Gate Voltage 30V
Forward Gate Current 10mA
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range ..... −55°C to +135°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 310mW
Derate above 25°C ..... 2.82mW/°C

ORDERING INFORMATION*

TO-92	WAFER	DICE
2N5638	2N5638/W	2N5638/D
2N5639	2N5639/W	2N5639/D
2N5640	2N5640/W	2N5640/D

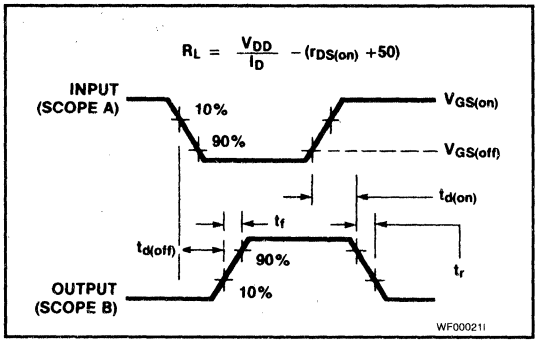
*When ordering wafer/dice refer to Section 10, page 10–1.

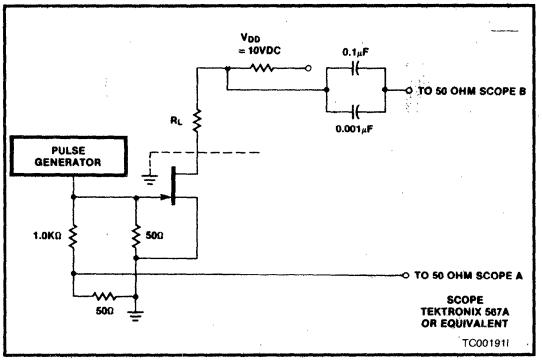
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	2N5638		2N5639		2N5640		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
BV_{GSS}	Gate Reverse Breakdown Voltage	I_G = −10μA, V_{DS} = 0	−30		−30		−30		V
I_{GSS}	Gate Reverse Current	V_{GS} = −15V, V_{DS} = 0		−1.0		−1.0		−1.0	nA
		T_A = 100°C		−1.0		−1.0		−1.0	μA
$I_{D(off)}$	Drain Cutoff Current	V_{DS} = 15V, V_{GS} = −12V (2N5638) V_{GS} = −8V (2N5639), V_{GS} = −6V (2N5640)		1.0		1.0		1.0	nA
		T_A = 100°C		1.0		1.0		1.0	μA
I_{DSS}	Saturation Drain Current	V_{DS} = 20V, V_{GS} = 0 (Note 1)	50		25		5.0		mA
$V_{DS(on)}$	Drain-Source ON Voltage	V_{GS} = 0, I_D = 12mA (2N5638), I_D = 6mA (2N5639), I_D = 3mA (2N5640)		0.5		0.5		0.5	V
$r_{DS(on)}$	Static Drain-Source ON Resistance	I_D = 1mA, V_{GS} = 0		30		60		100	Ω
$r_{ds(on)}$	Drain-Source ON Resistance	V_{GS} = 0, I_D = 0, f = 1kHz		30		60		100	Ω
C_{iss}	Common-Source Input Capacitance (Note 2)	V_{GS} = −12V, V_{DS} = 0, f = 1MHz		10		10		10	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)			4.0		4.0		4.0	pF
$t_{d(on)}$	Turn-On Delay Time (Note 2)	V_{DD} = 10V, $I_{D(on)}$ = 12mA (2N5638) $V_{GS(on)}$ = 0, $I_{D(on)}$ = 6mA (2N5639) $V_{GS(off)}$ = −10V, $I_{D(on)}$ = 3mA (2N5640) R_G = 50Ω (Note 2)		4.0		6.0		8.0	ns
t_r	Rise Time (Note 2)			5.0		8.0		10	ns
t_d	Turn-OFF Delay Time (Note 2)			5.0		10		15	ns
t_f	Fall Time (Note 2)			10		20		30	ns

NOTES: 1. Pulse test; PW ≤ 300μs, duty cycle ≤ 3.0%.
2. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.





2

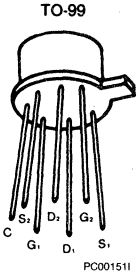
Note: All typical values have been guaranteed by characterization and are not tested.

2N5902-2N5909
Dual N-Channel JFET General Purpose Amplifier

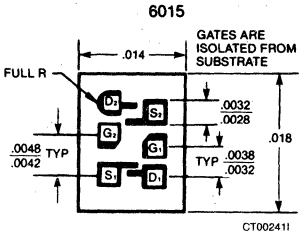
INTERSIL

FEATURES
- Tight Tracking
- Good Matching

PIN CONFIGURATION



CHIP TOPOGRAPHY



ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise specified)

Gate-Drain or Gate-Source Voltage (Note 1) ..... −40V
Gate Current (Note 1) 10mA
Storage Temperature Range ..... −65°C to +200°C
Operating Temperature Range ..... −55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C

	ONE SIDE	BOTH SIDES
Power Dissipation	367mW	500mW
Derate above 25°C	3mW/°C	4mW/°C

ORDERING INFORMATION*

TO-99	WAFER	DICE
2N5902	2N5902/W	2N5902/D
2N5903	2N5903/W	2N5903/D
2N5904	2N5904/W	2N5904/D
2N5905	2N5905/W	2N5905/D
2N5906	2N5906/W	2N5906/D
2N5907	2N5907/W	2N5907/D
2N5908	2N5908/W	2N5908/D
2N5909	2N5909/W	2N5909/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		2N5902-6		2N5903-7		2N5904-8		2N5905-9		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$\lvert I_{G1}-I_{G2} \rvert$	Differential Gate Current	V_{DG} = 10V, I_D = 30μA, T_A = 125°C	2N5902-5		2.0		2.0		2.0		2.0	nA
			2N5906-9		0.2		0.2		0.2		0.2	
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	V_{DS} = 10V, V_{GS} = 0		0.95	1	0.95	1	0.95	1	0.95	1	
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	V_{DG} = 10V, I_D = 30μA	f = 1kHz	0.97	1	0.97	1	0.95	1	0.95	1	
$\lvert V_{GS1}-V_{GS2} \rvert$	Differential Gate-Source Voltage				5		5		10		15	mV
$\frac{\Delta \lvert V_{BS1}-V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Measured at end points T_A and T_B)		T_A = 25°C, T_B = 125°C		5		10		20		40	μV/°C
			T_A = −55°C, T_B = 25°C		5		10		20		40	
$\lvert g_{os1}-g_{os2} \rvert$	Differential Output Conductance		f = 1kHz		0.2		0.2		0.2		0.2	μs

Note: All typical values have been guaranteed by characterization and are not tested.

2N5902-2N5909

INTERSIL

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		2N5902-5		2N5906-9		UNIT
				MIN	MAX	MIN	MAX	
I_{GSS}	Gate Reverse Current	$V_{GS} = -20V$, $V_{DS} = 0$			-5		-2	pA
	$T_A = 125°C$				-10		-5	nA
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = -1\mu A$, $V_{DS} = 0$		-40		-40		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 10V$, $I_D = 1nA$		-0.6	-4.5	-0.6	-4.5	V
V_{GS}	Gate Source Voltage	$V_{DG} = 10V$, $I_D = 30\mu A$			-4		-4	V
I_G	Gate Operating Current				-3		-1	pA
	$T_A = 125°C$				-3		-1	nA
I_{DSS}	Saturation Drain Current	$V_{DS} = 10V$, $V_{GS} = 0$	f = 1kHz	30	500	30	500	μA
g_{fs}	Common-Source Forward Transconductance			70	250	70	250	μs
g_{os}	Common-Source Output Conductance				5		5	μs
C_{iss}	Common-Source Input Capacitance	$V_{DS} = 10V$, $V_{GS} = 0$	f = 1MHz		3		3	pF
C_{rss}	Common-Source Reverse Transfer Capacitance	(Note 1)			1.5		1.5	pF
g_{fs}	Common-Source Forward Transconductance	$V_{DG} = 10V$, $I_D = 30\mu A$	f = 1kHz	50	150	50	150	μs
g_{os}	Common-Source Output Conductance				1		1	μs
$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage (Note 1)	$V_{DS} = 10V$, $V_{GS} = 0$			0.2		0.1	$\frac{\mu V}{\sqrt{Hz}}$
NF	Spot Noise Figure (Note 1)		f = 100Hz, $R_G = 10M\Omega$		3		1	dB

NOTE 1: For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

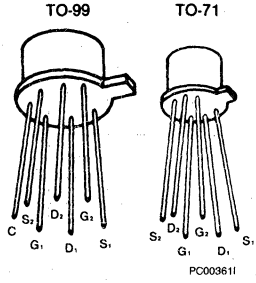
2N5911, 2N5912
IT5911, IT5912
Dual N-Channel JFET High Frequency Amplifier

INTERSIL

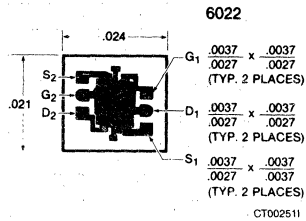
FEATURES

- Tight Tracking
- Low Insertion Loss
- Good Matching

PIN CONFIGURATION



CHIP TOPOGRAPHY



ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage ..... −25V
Gate Current 50mA
Storage Temperature Range ..... −65°C to +200°C
Operating Temperature Range ..... −55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C

	TO-71		TO-99	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Power Dissipation.....	200mW	400mW	367mW	500mW
Derate above 25°C	1.6mW/°C	3.2mW/°C	3.0mW/°C	4.0mW/°C

ORDERING INFORMATION*

TO-71	TO-99	WAFER	DICE
IT5911	2N5911	2N5911/W	2N5911/D
IT5912	2N5912	2N5912/W	2N5912/D

*When ordering wafer/dice refer to Section 10, page 10–1.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
I_{GSS}	Gate Reverse Current	V_{GS} = −15V, V_{DS} = 0			−100	pA
	T_A = 150°C				−250	nA
BV_{GSS}	Gate Reverse Breakdown Voltage	I_G = −1μA, V_{DS} = 0		−25		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 10V, I_D = 1nA		−1	−5	V
V_{GS}	Gate-Source Voltage	V_{DG} = 10V, I_D = 5mA		−0.3	−4	V
I_G	Gate Operating Current				−100	pA
	T_A = 125°C				−100	nA
I_{DSS}	Saturation Drain Current (Pulsewidth 300μs, duty cycle ≤ 3%)	V_{DS} = 10V, V_{GS} = 0V		7	40	mA
gf_s	Common-Source Forward Transconductance	V_{DG} = 10V, I_D = 5mA	f = 1kHz	5000	10,000	μs
gf_s	Common-Source Forward Transconductance (Note 1)		f = 100MHz	5000	10,000	
g_{os}	Common-Source Output Conductance		f = 1kHz		100	
g_{oss}	Common-Source Output Conductance (Note 1)		f = 100MHz		150	
C_{iss}	Common-Source Input Capacitance (Note 1)		f = 1MHz		5	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 1)				1.2	
$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage (Note 1)		f = 10kHz		20	$\frac{nV}{\sqrt{Hz}}$
NF	Spot Noise Figure (Note 1)		f = 10kHz R_G = 100kΩ		1	dB

Note: All typical values have been guaranteed by characterization and are not tested.

2N5911, 2N5912 IT5911, IT5912

INTERSIL

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS		IT, 2N5911		IT, 2N5912		UNIT
				MIN	MAX	MIN	MAX	
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current	V_{DG} = 10V, I_D = 5mA	125°C		20		20	nA
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	V_{DS} = 10V, V_{GS} = 0 (Pulsewidth 300μs, duty cycle ≤ 3%)		0.95	1	0.95	1	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage	V_{DG} = 10V, I_D = 5mA			10		15	mV
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Measured at end points, T_A and T_B)		T_A = 25°C T_B = 125°C		20		40	μV/°C
			T_A = −55°C T_B = 25°C		20		40	
$\frac{g_{fs}1}{g_{fs}2}$	Transconductance Ratio		f = 1kHz	0.95	1	0.95	1	

NOTE 1: For design reference only, not 100% tested.

2

Note: All typical values have been guaranteed by characterization and are not tested.

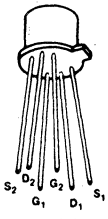
2N6483-2N6485
Dual N-Channel JFET Low Noise Amplifier

INTERSIL

FEATURES
- Ultra Low Noise
- High CMRR
- Low Offset
- Tight Tracking

PIN CONFIGURATION

TO-71



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CHIP TOPOGRAPHY

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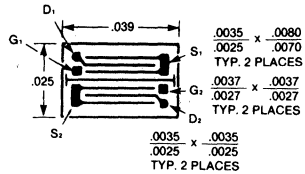


CT00261I

ORDERING INFORMATION*

TO-71	WAFER	DICE
2N6483	2N6483/W	2N6483/D
2N6484	2N6484/W	2N6484/D
2N6485	2N6485/W	2N6485/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage (Note 1) ..... -50V
Gate-Gate Voltage ..... ±50V
Gate Current (Note 1) 50mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +175°C
Lead Temperature (Soldering, 10sec) ..... +300°C

	ONE SIDE	BOTH SIDES
Power Dissipation	250mW	400mW
Derate above 25°C	1.7mW/°C	2.7mW/°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{GSS}	Gate Reverse Current	V_{GS} = -30V, V_{DS} = 0		-200	pA
	T_A = 150°C			-200	nA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = -1μA, V_{DS} = 0	-50		V
V_p	Gate-Source Pinch Off Voltage	V_{DS} = 20V, I_D = 1nA	-0.7	-4.0	
I_{DSS}	Drain Current at Zero Gate Voltage (Note 2)	V_{DS} = 20V, V_{GS} = 0	0.5	7.5	mA
g_{fs}	Common-Source Forward Transconductance (Note 2)	V_{DS} = 20V, V_{GS} = 0, f = 1kHz (Note 6)	1000	4000	μs
g_{oss}	Common-Source Output Conductance				
C_{iss}	Common-Source Input Capacitance	V_{DS} = 20V, V_{GS} = 0, f = 1MHz (Note 6)		20	pF
C_{rss}	Common-Source Reverse Transfer Capacitance			3.5	
I_G	Gate Current	V_{GD} = 20V, I_D = 200μA (Note 6)		100	pA
	T_A = 150°C			100	nA
V_{GS}	Gate Source Voltage	V_{DG} = 20V, I_D = 200μA	0.2	3.8	V
g_{fs}	Common-Source Forward Transconductance	V_{DG} = 20V, I_D = 200μA, f = 1kHz	500	1500	μs
g_{os}	Common-Source Output Conductance	V_{DG} = 20V, I_D = 200μA		1	
$\bar{e}_n$	Equivalent Input Noise Voltage (Note 6)	V_{DS} = 20V, I_D = 200μA, f = 10Hz		10	nV/√Hz
		V_{DS} = 20V, I_D = 200μA, f = 1kHz		5	

NOTES: 1. Per transistor.
2. Pulse test required; pulse width = 2ms.

Note: All typical values have been guaranteed by characterization and are not tested.

2N6483-2N6485

INTERSIL

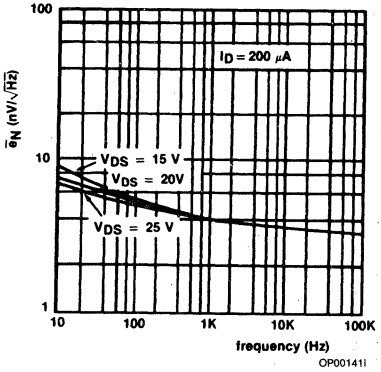
MATCHING CHARACTERISTICS (@ 25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	2N6483		2N6484		2N6485		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$\frac{I_{DSS1}}{I_{DSS2}}$	Drain Current Ratio at Zero Gate Voltage	V_{DS} = 20V, V_{GS} = 0 (Note 4)	0.95	1	0.95	1	0.95	1	
$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Current	V_{DG} = 20V, I_D = 200μA T_A = +125°C		10		10		10	nA
$\frac{g_{fs1}}{g_{gs2}}$	Transconductance Ratio	V_{DG}=20V, I_D = 200μA, f = 1kHz (Note 4)	0.97	1	0.97	1	0.95	1	
$\lvert g_{os1} - g_{os2} \rvert$	Differential Output Conductance (Note 6)	V_{DG} = 20 V, I_D = 200μA, f = 1kHz		0.1		0.1		0.1	μs
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage	V_{DG} = 20V, I_D = 200μA		5		10		15	mV
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift	V_{DG} = 20V, I_D = 200μA T_A = −55°C to +125°C		5		10		25	μV/°C
CMRR	Common Mode Rejection Ratio (Note 6)	V_{DD} = 10 to 20V, I_D = 200μA (Note 5)	100		100		90		dB

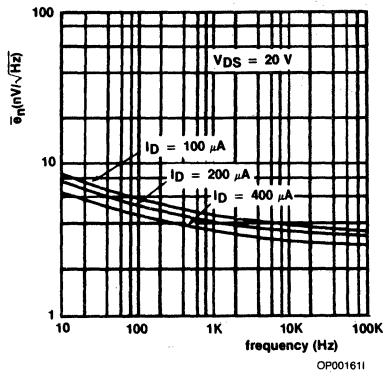
NOTES: 3. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
4. Pulse duration of 2ms used during test.
5. CMRR = $20Log_{10}\Delta V_{DD}/\Delta \lvert V_{GS1}-V_{GS2} \rvert$, ($\Delta V_{DD}$ = 10V), not included in JEDEC registration.
6. For design reference only, not 100% tested.

TYPICAL PERFORMANCE CHARACTERISTICS

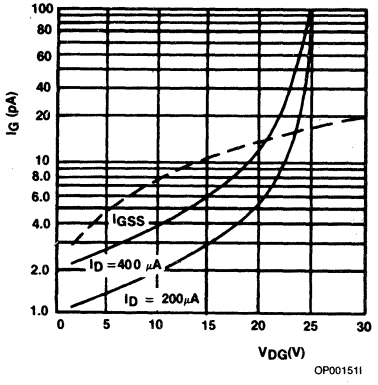
$\bar{e}_n$ vs. FREQUENCY



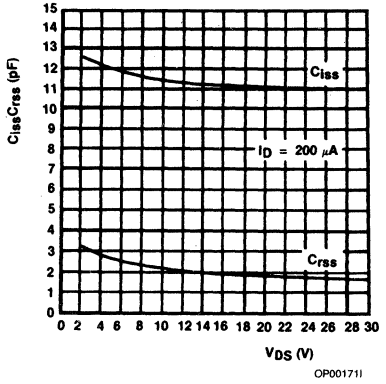
$\bar{e}_n$ vs. FREQUENCY



GATE CURRENT vs. V_{DG}



TYPICAL CAPACITANCE vs. V_{DS}



Note: All typical values have been guaranteed by characterization and are not tested.

IMF6485
Dual N-Channel JFET Low Noise Amplifier

INTERSIL

GENERAL DESCRIPTION

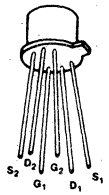
This N-Channel Junction FET is characterized for ultra low noise applications requiring tightly controlled and specified noise parameters at 10Hz and 1000Hz. Tight matching specifications make this device ideal as the input stage for low frequency differential instrumentation amplifiers.

FEATURES

- **Ultra Low Noise**
- **High CMRR**
- **Low Offset**
- **Tight Tracking**

PIN CONFIGURATION

TO-71



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CHIP TOPOGRAPHY

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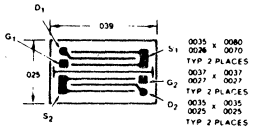


CT002601

ORDERING INFORMATION*

TO-71	WAFER	DICE
IMF6485	IMF6485/W	IMF6485/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage (Note 1) ..... -50V
Gate-Gate Voltage ..... ±50V
Gate Current (Note 1) 50mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +175°C
Lead Temperature (Soldering, 10sec) ..... +300°C

	ONE SIDE	BOTH SIDES
Power Dissipation	250mW	400mW
Derate above 25°C	1.7mW/°C	2.7mW/°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{GSS}	Gate Reverse Current	V_{GS} = -30V, V_{DS} = 0		-200	pA
	T_A = 150°C			-200	nA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = -1μA, V_{DS} = 0	-50		V
V_p	Gate-Source Pinch-Off Voltage	V_{DS} = 20V, I_D = 1nA	-0.7	-4.0	V
I_{DSS}	Drain Current at Zero Gate Voltage (Note 2)	V_{DS} = 20V, V_{GS} = 0	0.5	7.5	mA
g_{fs}	Common-Source Forward Transconductance (Note 2, 3)	V_{DS} = 20V, V_{GS} = 0, f = 1kHz	1000	4000	μs
g_{oss}	Common-Source Output Conductance	V_{DS} = 20V, V_{GS} = 0, f = 1kHz		10	μs
C_{iss}	Common-Source Input Capacitance (Note 4)	V_{DS} = 20V, V_{GS} = 0, f = 1MHz		20	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 4)			3.5	pF
I_G	Gate Current	V_{GD} = 20V, I_D = 200μA		-100	pA
	T_A = 150°C			-100	nA
V_{GS}	Gate-Source Voltage	V_{DG} = 20V, I_D = 200μA	0.2	-3.8	V
g_{fs}	Common-Source Forward Transconductance	V_{DG} = 20V, I_D = 200μA, f = 1kHz	500	1500	μs
g_{os}	Common Source Output Conductance	V_{DG} = 20V, I_D = 200μA		1	μs
$\bar{e}_n$	Equivalent Input Noise Voltage (Note 4)	V_{DS} = 20V, I_D = 200μA, f = 10Hz		15	$nV/\sqrt{Hz}$
		V_{DS} = 20V, I_D = 200μA, f = 1kHz		10	$nV/\sqrt{Hz}$

NOTES: 1. Per transistor.
2. Pulse test required; pulse width = 2ms.
3. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

IMF6485

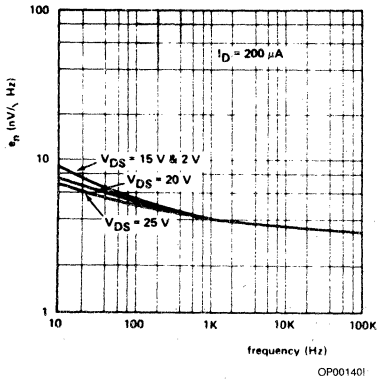
MATCHING CHARACTERISTICS (@ 25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$\frac{I_{DSS1}}{I_{DSS2}}$	Drain Current Ratio at Zero Gate Voltage	V_{DS} = 20V, V_{GS} = 0 (Note 2)	0.95	1	
$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Current	V_{DG} = 20V, I_D = 200μA T_A = +125°C		10	nA
$\frac{g_{fs1}}{g_{gs2}}$	Transconductance Ratio	V_{DG} = 20V, I_D = 200μA, f = 1kHz (Note 2)	0.95	1	
$\lvert g_{os1} - g_{os2} \rvert$	Differential Output Conductance (Note 4)	V_{DG} = 20V, I_D = 200μA, f = 1kHz		0.1	μs
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage	V_{DG} = 20V, I_D = 200μA		25	mV
$\frac{\Delta\lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift	V_{CG} = 20V, I_D = 200μA T_A = −55°C to +125°C		40	μV/°C
CMRR	Common Mode Rejection Ratio (Note 3, 4)	V_{DD} = 10 to 20V, I_D = 200μA	90		dB

NOTES: 1. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
2. Pulse duration of 2ms used during test.
3. CMRR = $20\text{Log}_{10}\Delta V_{DD} / \Delta \lvert V_{GS1} - V_{GS2} \rvert$, ($\Delta V_{DD}$ = 10V)
4. For design reference only, not 100% tested.

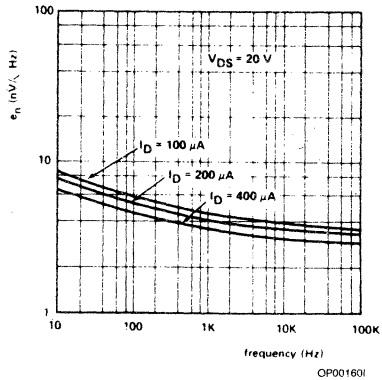
TYPICAL PERFORMANCE CHARACTERISTICS

$\bar{e}_n$ vs. FREQUENCY



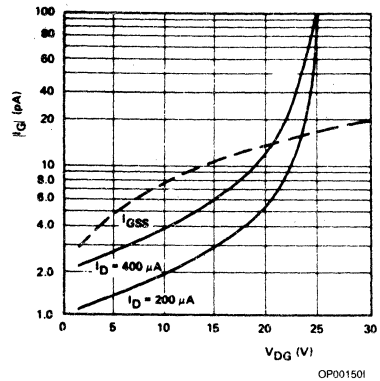
OP00140I

$\bar{e}_n$ vs. FREQUENCY



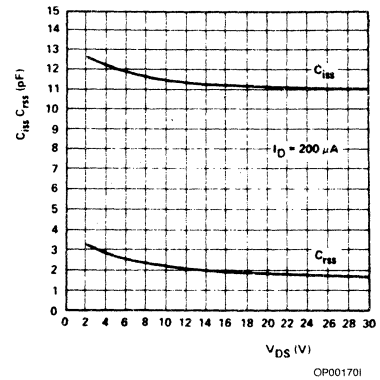
OP00160I

GATE CURRENT vs. V_{DG}



OP00150I

TYPICAL CAPACITANCE vs. V_{DS}



OP00170I

Note: All typical values have been guaranteed by characterization and are not tested.

3N161
Diode Protected P-Channel Enhancement Mode MOSFET General Purpose Amplifier/Switch

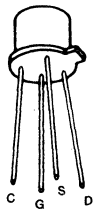
INTERSIL

FEATURES

- **Channel Cut Off With Zero Gate Voltage**
- **Square-Law Transfer Characteristic Reduces Distortion**
- **Independent Substrate Connection Provides Flexibility in Biasing**
- **Internally Connected Diode Protects Gate From Damage Due to Overvoltage**

PIN CONFIGURATION

TO-72



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CHIP TOPOGRAPHY

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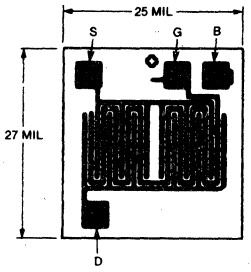


CT002721

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Drain-Source or Drain-Gate Voltage 40V
Drain Current 50mA
Gate Forward Current 10μA
Gate Reverse Current 1mA
Storage Temperature ..... −65°C to +200°C
Operating Temperature ..... −55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 375mW
Derate above 25°C ..... 3.0mW/°C

ORDERING INFORMATION*

TO-72	WAFER	DICE
3N161	3N161/W	3N161/D

*When ordering wafer/dice refer to Section 10, page 10–1.

ELECTRICAL CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{GSSF}	Forward Gate-Terminal Current	V_{GS} = −25V, V_{DS} = 0			−100		pA
	T_A = +100°C					−1	nA
BV_{GSS}	Forward Gate-Source Breakdown Voltage	I_G = −0.1mA, V_{DS} = 0		−25			V
I_{DSS}	Zero-Gate-Voltage Drain Current	V_{DS} = −15V, V_{GS} = 0				−10	nA
		V_{DS} = −25V, V_{GS} = 0				−10	μA
$V_{GS(th)}$	Gate-Source Threshold Voltage	V_{DS} = −15V, I_D = −10μA		−1.5		−5	V
V_{GS}	Gate-Source Voltage	V_{DS} = −15V, I_D = −8mA		−4.5		−8	
$I_{D(on)}$	On-State Drain Current	V_{DS} = −15V, V_{GS} = −15V		−40		−120	mA
$\lvert y_{fs} \rvert$	Small-Signal Common-Source Forward Transfer Admittance	V_{DS} = −15V, I_D = −8mA	f = 1kHz	3500		6500	μs
$\lvert y_{os} \rvert$	Small-Signal Common-Source Output Admittance					250	
C_{iss}	Common-Source Short-Circuit Input Capacitance (Note 1)		f = 1MHz			10	pF
C_{rss}	Common-Source Short Circuit Reverse Transfer Capacitance (Note 1)					4	

NOTE 1: For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

3N163, 3N164

P-Channel Enhancement Mode MOSFET General Purpose Amplifier Switch

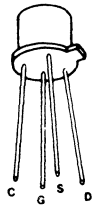
INTERSIL

FEATURES

- Very High Input Impedance
- High Gate Breakdown
- Fast Switching
- Low Capacitance

PIN CONFIGURATION

TO-72



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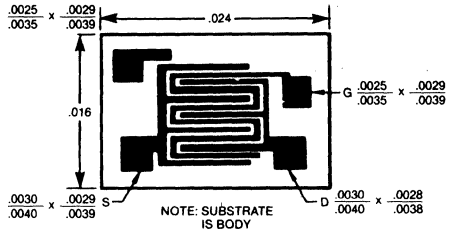
CHIP TOPOGRAPHY

1503



CT002811

ORDERING INFORMATION*

TO-72	WAFER	DICE
3N163	3N163/W	3N163/D
3N164	3N164/W	3N164/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ABSOLUTE MAXIMUM RATINGS (Note 1)

(T_A = 25°C unless otherwise noted)

Drain-Source or Drain-Gate Voltage
- 3N163 ..... -40V
- 3N164 ..... -30V

Static Gate-Source Voltage
- 3N163 ..... ±40V
- 3N164 ..... ±30V

Transient Gate-Source Voltage (Note 2) ..... ±125V
Drain Current 50mA
Storage Temperature ..... -65°C to +200°C
Operating Temperature ..... -55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 375mW
- Derate above +25°C ..... 3.0mW/°C

NOTES:
1. See handling precautions on 3N170 data sheet.
2. Devices must not be tested at ±125V more than once, nor for longer than 300ms.

ELECTRICAL CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless noted)

SYMBOL	PARAMETER	TEST CONDITIONS	3N163		3N164		UNIT
			MIN	MAX	MIN	MAX	
I_{GSSR}	Gate Reverse Leakage Current	V_{GS} = -40V (3N163) V_{GS} = -30V (3N164)		10		10	pA
I_{GSSF}	Gate Forward Current			-10		-10	
	T_A = +125°C			-25		-25	
BV_{DSS}	Drain-Source Breakdown Voltage	I_D = -10μA, V_{GS} = 0	-40		-30		V
BV_{SDS}	Source-Drain Breakdown Voltage	I_S = -10μA, V_{GD} = 0, V_{DS} = 0	-40		-30		
$V_{GS(th)}$	Threshold Voltage	V_{DS} = V_{GS}, I_D = -10μA	-2.0	-5.0	-2.0	-5.0	
$V_{GS(th)}$	Threshold Voltage	V_{DS} = -15V, I_D = -10μA	-2.0	-5.0	-2.0	-5.0	
V_{GS}	Gate Source Voltage	V_{DS} = -15V, I_D = -0.5mA	-3.0	-6.5	-3.0	-6.5	
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -15V, V_{GS} = 0		200		400	pA
I_{SDS}	Source Drain Current	V_{SD} = 15V, V_{GS} = V_{DB} = 0		400		800	
$r_{DS(on)}$	Drain-Source on Resistance	V_{GS} = -20V, I_D = -100μA		250		300	ohms
$I_{D(on)}$	On Drain Current	V_{DS} = -15V, V_{GS} = -10V	-5.0	-30.0	-3.0	-30.0	mA
g_{fs}	Forward Transconductance	V_{DS} = -15V, I_D = -10mA, f = 1kHz	2000	4000	1000	4000	μs
g_{os}	Output Admittance			250		250	

Note: All typical values have been guaranteed by characterization and are not tested.

3N163, 3N164

INTERSIL

ELECTRICAL CHARACTERISTICS (CONT.)

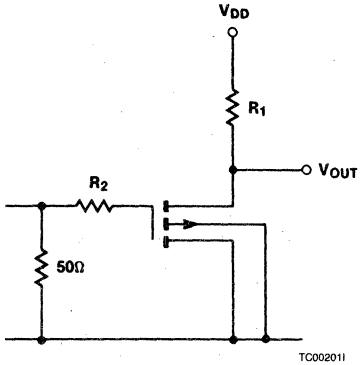
SYMBOL	PARAMETER	TEST CONDITIONS	3N163		3N164		UNIT
			MIN	MAX	MIN	MAX	
C_{iss}	Input Capacitance—Output Shorted	$V_{DS} = -15V$, $I_D = -10mA$, f = 1MHz (Note 1)		2.5		2.5	pF
C_{rss}	Reverse Transfer Capacitance			0.7		0.7	
C_{oss}	Output Capacitance Input Shorted			3.0		3.0	

NOTE 1: For design reference only, not 100% tested.

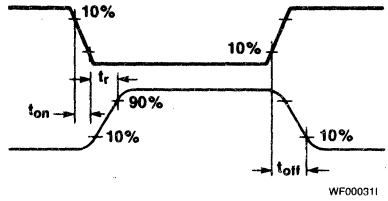
SWITCHING CHARACTERISTICS (@ 25°C and $V_{BS} = 0$)

SYMBOL	PARAMETER	TEST CONDITIONS	3N163		3N164		UNIT
			MIN	MAX	MIN	MAX	
t_{on}	Turn-On Delay Time	$V_{DD} = -15V$		12		12	ns
t_r	Rise Time	$I_{D(on)} = -10mA$ (Note 1)		24		24	
t_{off}	Turn-Off Time	$R_G = R_L = 1.4k\Omega$		50		50	

SWITCHING TIME CIRCUIT



SWITCHING WAVEFORM



Note: All typical values have been guaranteed by characterization and are not tested.

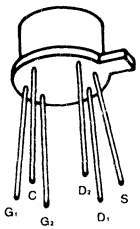
3N165, 3N166
Dual P-Channel Enhancement Mode MOSFET General Purpose Amplifier

INTERSIL

FEATURES
- Very High Impedance
- High Gate Breakdown
- Low Capacitance

PIN CONFIGURATION

TO-99



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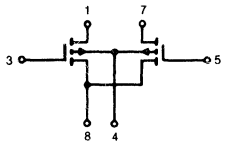
DEVICE SCHEMATIC



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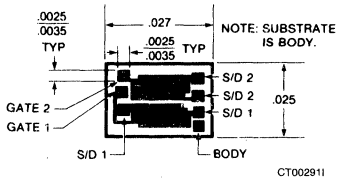
CHIP TOPOGRAPHY

2506



CT00291I

ABSOLUTE MAXIMUM RATINGS (Note 1)

(T_A = 25°C unless otherwise specified)

Drain-Source or Drain-Gate Voltage (Note 2)
- 3N165 ..... 40V
- 3N166 ..... 30V

Transient Gate-Source Voltage (Note 3) ..... ±125
Gate-Gate Voltage ..... ±80V
Drain Current (Note 2) 50mA
Storage Temperature ..... −65°C to +200°C
Operating Temperature ..... −55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation
- One Side 300mW
- Both Sides 525mW
- Total Derating above 25°C ..... 4.2mW/°C

ORDERING INFORMATION*

TO-99	WAFER	DICE
3N165	3N165/W	3N165/D
3N166	3N166/W	3N166/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ELECTRICAL CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless noted)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNIT
I_{GSSR}	Gate Reverse Leakage Current	V_{GS} = 40V		10	pA
I_{GSSF}	Gate Forward Leakage Current	V_{GS} = −40V		−10	pA
	T_A = +125°C	V_{GS} = −40V		−25	pA
I_{DSS}	Drain to Source Leakage Current	V_{DS} = −20V		−200	pA
I_{SDS}	Source to Drain Leakage Current	V_{SD} = −20, V_{DB} = 0		−400	pA
$I_{D(on)}$	On Drain Current	V_{DS} = −15V, V_{GS} = −10V	−5	−30	mA
$V_{GS(th)}$	Gate Source Threshold Voltage	V_{DS} = −15V, I_D = −10μA	−2	−5	V
$V_{GS(th)}$	Gate Source Threshold Voltage	V_{DS} = V_{GS}, I_D = −10μA	−2	−5	V
$r_{DS(on)}$	Drain Source ON Resistance	V_{GS} = −20V, I_D = −100μA		300	ohms
g_{fs}	Forward Transconductance	V_{DS} = −15V, I_D = −10mA, f = 1kHz	1500	3000	μs
g_{os}	Output Admittance	V_{DS} = −15V, I_D = −10mA, f = 1kHz		300	μs

Note: All typical values have been guaranteed by characterization and are not tested.

3N165, 3N166

INTERSIL

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
C_{iss}	Input Capacitance	$V_{DS} = -15V$, $I_D = -10mA$, f = 1MHz (Note 4)		3.0	pF
C_{rss}	Reverse Transfer Capacitance			0.7	
C_{oss}	Output Capacitance			3.0	
$R_E(Y_{fs})$	Common Source Forward Transconductance	$V_{DS} = -15V$, $I_D = -10mA$, f = 100MHz (Note 4)	1200		μs

MATCHING CHARACTERISTICS 3N165

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
Y_{fs1}/Y_{fs2}	Forward Transconductance Ratio	$V_{DS} = -15V$, $I_D = -1500\mu A$, f = 1kHz	0.90	1.0	
V_{GS1-2}	Gate Source Threshold Voltage Differential	$V_{DS} = -15V$, $I_D = -500\mu A$		100	mV
$\frac{\Delta V_{GS1-2}}{\Delta T}$	Gate Source Threshold Voltage Differential Change with Temperature	$V_{DS} = -15V$, $I_A = -500\mu A$ $T_A = -55°C$ to $+25°C$		100	$\mu V/°C$

NOTES
1. See handling precautions on 3N170 data sheet.
2. Per transistor.
3. Devices must not be tested at ±125V more than once, nor for longer than 300ms.
4. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

3N170, 3N171
N-Channel Enhancement Mode MOSFET Switch

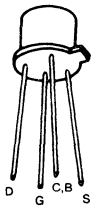
FEATURES
- **Low Switching Voltages**
- **Fast Switching Times**
- **Low Drain-Source Resistance**
- **Low Reverse Transfer Capacitance**

HANDLING PRECAUTIONS
MOS field-effect transistors have extremely high input resistance and can be damaged by the accumulation of excess static charge. To avoid possible damage to the device while wiring, testing, or in actual operation, follow the procedures outlined below.

1. To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used.
2. Avoid unnecessary handling. Pick up devices by the case instead of the leads.
3. Do not insert or remove devices from circuits with the power on as transient voltages may cause permanent damage to the devices.

PIN CONFIGURATION

TO-72



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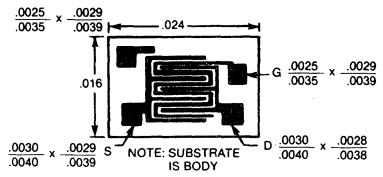
CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-72	WAFER	DICE
3N170	3N170/W	3N170/D
3N171	3N171/W	3N171/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Drain-Gate Voltage ..... ±35V
Drain-Source Voltage 25V
Gate-Source Voltage ..... ±35V
Drain Current 30mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 300mW
Derate above 25°C ..... 2.4mW/°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted) Substrate connected to source.

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage		I_D = 10μA, V_{GS} = 0	25		V
I_{GSS}	Gate Leakage Current		V_{GS} = -35V, V_{DS} = 0		10	pA
		T_A = 125°C			100	
I_{DSS}	Zero-Gate-Voltage Drain Current		V_{DS} = 10V, V_{GS} = 0		10	nA
		T_A = 125°C			1.0	μA
$V_{GS(th)}$	Gate-Source Threshold Voltage	3N170	V_{DS} = 10V, I_D = 10μA	1.0	2.0	V
		3N171		1.5	3.0	
$I_{D(on)}$	"ON" Drain Current		V_{GS} = 10V, V_{DS} = 10V	10		mA
$V_{DS(on)}$	Drain-Source "ON" Voltage		I_D = 10mA, V_{GS} = 10V		2.0	V
$r_{ds(on)}$	Drain-Source ON Resistance		V_{GS} = 10V, I_D = 0, f = 1.0kHz		200	Ω
$\|Y_{fs}\|$	Forward Transfer Admittance		V_{DS} = 10V, I_D = 2.0mA, f = 1.0kHz	1000		μs

Note: All typical values have been guaranteed by characterization and are not tested.

3N170, 3N171

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
C_{rss}	Reverse Transfer Capacitance (Note 1)	V_{DS} = 0, V_{GS} = 0, f = 1.0MHz		1.3	pF
C_{iss}	Input Capacitance (Note 1)	V_{DS} = 10V, V_{GS} = 0, f = 1.0MHz		5.0	
$C_{d(sub)}$	Drain-Substrate Capacitance (Note 1)	$V_{D(SUB)}$ = 10V, f = 1.0MHz		5.0	
$t_{d(on)}$	Turn-On Delay Time (Note 1)	V_{DD} = 10V, $I_{D(on)}$ = 10mA, $V_{GS(on)}$ = 10V, $V_{GS(off)}$ = 0, R_G = 50Ω		3.0	ns
t_r	Rise Time (Note 1)			10	
$t_{d(off)}$	Turn-Off Delay Time (Note 1)			3.0	
t_f	Fall Time (Note 1)			15	

NOTE 1: For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

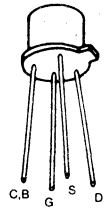
3N172, 3N173
Diode Protected P-Channel Enhancement Mode MOSFET General Purpose Amplifier/Switch

INTERSIL

FEATURES
- High Input Impedance
- Diode Protected Gate

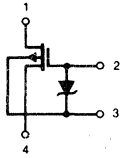
PIN CONFIGURATION

TO-72



PC00191I

DEVICE SCHEMATIC



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CHIP TOPOGRAPHY

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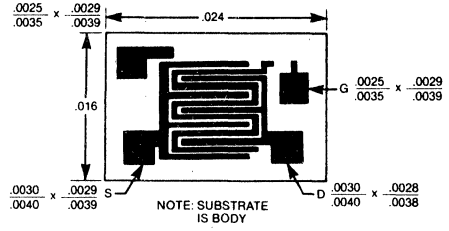

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ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Drain-Source or Drain-Gate Voltage
- 3N172 ..... 40V
- 3N173 ..... 30V

Drain Current 50mA
Gate Forward Current 10μA
Gate Reverse Current 1mA
Storage Temperature ..... −65°C to +200°C
Operating Temperature ..... −55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 375mW
Derate above 25°C ..... 3.0mW/°C

ORDERING INFORMATION*

TO-72	WAFER	DICE
3N172	3N172/W	3N172/D
3N173	3N173/W	3N173/D

*When ordering wafer/dice refer to Section 10, page 10–1.

ELECTRICAL CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless noted)

SYMBOL	PARAMETER	TEST CONDITIONS	3N172		3N173		UNIT
			MIN	MAX	MIN	MAX	
I_{GSS}	Gate Reverse Current	V_{GS} = −20V		−200		−500	pA
	T_A = +125°C			−0.5		−1.0	μA
BV_{GSS}	Gate Breakdown Voltage	I_D = −10μA	−40	−125	−30	−125	V
BV_{DSS}	Drain-Source Breakdown Voltage	I_D = −10μA	−40		−30		
BV_{SDS}	Source-Drain Breakdown Voltage	I_S = −10μA, V_{DB} = 0	−40		−30		
$V_{GS(th)}$	Threshold Voltage	V_{DS} = V_{GS}, I_D = −10μA	−2.0	−5.0	−2.0	−5.0	
		V_{DS} = −15V, I_D = −10μA	−2.0	−5.0	−2.0	−5.0	
V_{GS}	Gate Source Voltage	V_{DS} = −15V, I_D = −500μA	−3.0	−6.5	−2.5	−6.5	
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −15V, V_{GS} = 0		−0.4		−10	nA
I_{SDS}	Zero Gate Voltage Source Current	V_{SD} = −15V, V_{DB} = 0, V_{GD} = 0		−0.4		−10	
$r_{DS(on)}$	Drain Source On Resistance	V_{GS} = −20V, I_D = −100μA		250		350	ohms
$I_{D(on)}$	On Drain Current	V_{DS} = −15V, V_{GS} = −10V	−5.0	−30	−5.0	−30	mA

Note: All typical values have been guaranteed by characterization and are not tested.

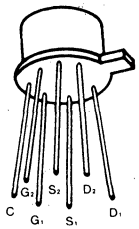
3N188–3N191
Dual P-Channel Enhancement Mode MOSFET General Purpose Amplifier

INTERSIL

FEATURES
- Very High Input Impedance
- High Gate Breakdown 3N190–3N191
- Zener Protected Gate 3N188–3N189
- Low Capacitance

PIN CONFIGURATION

TO-99



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CHIP TOPOGRAPHY

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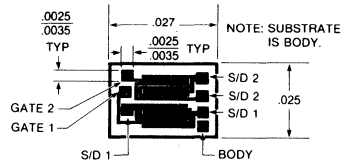


3N190, 3N191 ONLY

CT00321I

ORDERING INFORMATION*

TO-99	WAFER	DICE
3N188	—	—
3N189	—	—
3N190	3N190/W	3N190/D
3N191	3N191/W	3N191/D

*When ordering wafer/dice refer to Section 10, page 10–1.

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Drain-Source or Drain-Gate Voltage (Note 1)
- 3N188, 3N189 ..... 40V
- 3N190, 3N191 ..... 30V

Transient Gate-Source Voltage (Notes 1 and 2) .. ±125V
Gate-Gate Voltage ..... ±80V
Drain Current (Note 1) 50mA
Storage Temperature ..... −65°C to +200°C
Operating Temperature ..... −55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation
- One Side 300mW
- Both Sides 525mW
- Total Derating above 25°C ..... 4.2mW/°C

ELECTRICAL CHARACTERISTICS (25°C and V_{BS} = 0 unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	3N188 3N189		3N190 3N191		UNIT
			MIN	MAX	MIN	MAX	
I_{GSSR}	Gate Reverse Current	V_{GS} = 40V				10	pA
I_{GSSF}	Gate Forward Current	V_{GS} = −40V		−200		−10	pA
	T_A = 125°C			−200		−25	
BV_{DSS}	Drain-Source Breakdown Voltage	I_D = −10μA	−40		−40		V
BV_{SDS}	Source-Drain Breakdown Voltage	I_S = −10μA, V_{BD} = 0	−40		−40		V
$V_{GS(th)}$	Threshold Voltage	V_{DS} = −15V, I_D = −10μA	−2.0	−5.0	−2.0	−5.0	V
		V_{DS} = V_{GS}, I_D = −10μA	−2.0	−5.0	−2.0	−5.0	V
V_{GS}	Gate Source Voltage	V_{DS} = −15V, I_D = −500μA	−3.0	−6.5	−3.0	−6.5	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −15V		−200		−200	pA
I_{SDS}	Source Drain Current	V_{SD} = −15V, V_{DB} = 0		−400		−400	pA
$r_{DS(on)}$	Drain-Source on Resistance	V_{DS} = −20V, I_D = −100μA		300		300	ohms
$I_{D(on)}$	On Drain Current	V_{DS} = −15V, V_{GS} = −10V	−5.0	−30.0	−5.0	−30.0	mA

Note: All typical values have been guaranteed by characterization and are not tested.

3N188-3N191

INTERSIL

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS		3N188 3N189		3N190 3N191		UNIT
				MIN	MAX	MIN	MAX	
g_{fs}	Forward Transconductance (Note 3)	$V_{DS} = -15V$, $I_D = -10mA$	f = 1kHz	1500	4000	1500	4000	μs
Y_{os}	Output Admittance				300		300	
C_{iss}	Input Capacitance Output Shorted (Note 5)		f = 1MHz		4.5		4.5	pF
C_{rss}	Reverse Transfer Capacitance (Note 5)				1.5		1.0	
C_{oss}	Output Capacitance Input Shorted (Note 5)				3.0		3.0	

SWITCHING CHARACTERISTICS (@ 25°C and $V_{BS} = 0$ unless noted)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
$t_{d(on)}$	Turn On Delay Time	$V_{DD} = -15V$, $I_D = -10mA$		15	ns
t_r	Rise Time	$R_G = R_L = 1.4k\Omega$ (Note 5)		30	
t_{off}	Turn Off Time			50	

MATCHING CHARACTERISTICS (@ 25°C and $V_{BS} = 0$ unless noted) 3N188 and 3N190

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
Y_{fs1}/Y_{fs2}	Forward Transconductance Ratio	$V_{DS} = -15V$, $I_D = -500\mu A$, f = 1kHz	0.85	1.0	
V_{GS1-2}	Gate Source Threshold Voltage Differential	$V_{DS} = -15V$, $I_D = -500\mu A$		100	mV
$\frac{\Delta V_{GS1-2}}{\Delta T}$	Gate Source Threshold Voltage Differential Change with Temperature (Note 4)	$V_{DS} = -15V$, $I_D = -500\mu A$, T = −55°C to +25°C		100	μV/°C
$\frac{\Delta V_{GS1-2}}{\Delta T}$	Gate Source Threshold Voltage Differential Change with Temperature (Note 4)	$V_{DS} = -15V$, $I_D = -500\mu A$ T = +25°C to +125°C		100	μV/°C

NOTES:
1. Per transistor.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 300μs; duty cycle ≤ 3%.
4. Measured at end points, T_A and T_B.
5. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

ID100, ID101
Dual Low Leakage Diode

INTERSIL

GENERAL DESCRIPTION

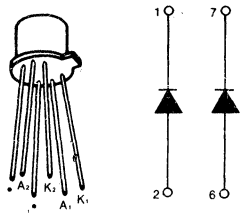
The ID100 and ID101 are monolithic dual diodes intended for use in applications requiring extremely low leakage currents. Applications include interstage coupling with reverse isolation, signal clipping and clamping and protection of ultra low leakage FET differential dual and operational amplifiers.

FEATURES

- I_R = 0.1pA (Typical)
- BV_R > 30V
- C_{rss} = 0.75pF (Typical)

PIN CONFIGURATIONS

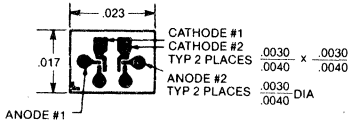
TO-71
TO-78



PC00211I

CHIP TOPOGRAPHY

4000



CT00331I

ORDERING INFORMATION*

TO78	TO71	WAFER	CHIP
ID100	ID101	iD100/W	ID100/D

*When ordering wafer/dice refer to Section 10, page 10–1.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Diode Reverse Voltage 30V
Diode to Diode Voltage ..... ±50V
Forward Current 20mA
Reverse Current 100μA
Storage Temperature Range ..... −65°C to +200°C
Operating Temperature Range ..... −55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 300mW
Derate above 25°C ..... 2.4mW/°C

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	ID100, ID101			UNIT
			MIN	TYP	MAX	
V_F	Forward Voltage Drop	I_F = 10mA	0.8		1.1	V
BV_R	Reverse Breakdown Voltage	I_R = 1μA	30			V
I_R	Reverse Leakage Current	V_R = 1V		0.1		pA
		V_R = 10V		2.0	10	pA
	T_A = 125°C	V_R = 10V			10	nA
$\lvert I_{R_1} - I_{R_2} \rvert$	Differential Leakage Current				3	pA
C_{rss}	Total Reverse Capacitance	V_R = 10V, f = 1MHz (Note 1)		0.75	1	pF

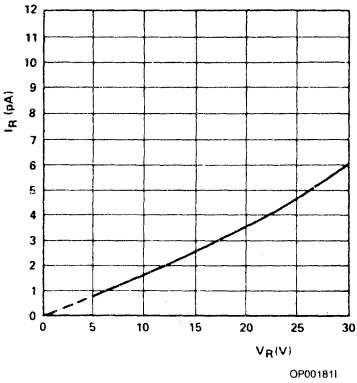
NOTE 1: For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

ID100, ID101

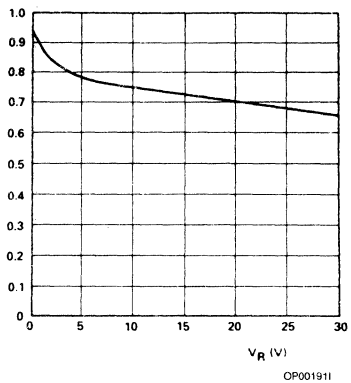
TYPICAL PERFORMANCE CHARACTERISTICS

REVERSE CURRENT vs. VOLTAGE



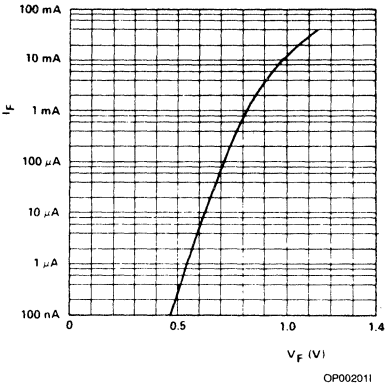
OP00181I

CAPACITANCE vs. VOLTAGE



OP00191I

FORWARD CURRENT vs. VOLTAGE



OP00201I

2

Note: All typical values have been guaranteed by characterization and are not tested.

IT100, IT101
P-Channel JFET Switch

INTERSIL

GENERAL DESCRIPTION

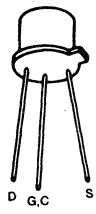
This P-channel JFET has been designed to directly interface with TTL logic, thus eliminating the need for costly drivers, in analog gate circuitry. Bipolar inputs of ±15V can be switched. The FET is OFF for hi level inputs (+5V or +15V) and ON for low level inputs (< 0.5 V for IT100, < 1.5V for IT101).

FEATURES

- **Interfaces Directly w/TTL Logic Elements**
- **$r_{DS(on)}$ < 75Ω for 5V Logic Drive**
- **$I_{D(off)}$ < 100pA**

PIN CONFIGURATION

TO-18



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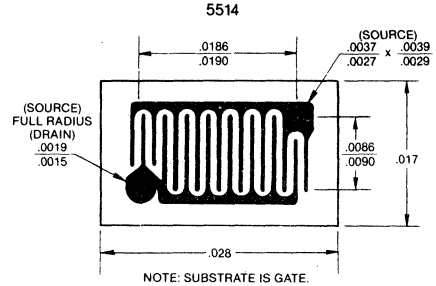
CHIP TOPOGRAPHY



CT00341I

ORDERING INFORMATION*

TO-18	WAFER	DICE
IT100	IT100/W	IT100/D
IT101	IT101/W	IT101/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source Voltage 35V
Gate-Drain Voltage 35V
Gate Current 50mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 300mW
Derate above 25°C ..... 2.4mW/°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	IT100		IT101		UNIT
			MIN	MAX	MIN	MAX	
I_{DSS}	Drain Current	V_{GS} = 0, V_{DS} = -15V	-10		-20		mA
V_P	Pinch Off Voltage	I_D = 1nA, V_{DS} = -15V	2	4.5	4	10	V
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = 1μA, V_{DS} = 0	35		35		V
I_{GSS}	Gate Reverse Current	V_{GS} = 20V, V_{DS} = 0		200		200	pA
g_{fs}	Transconductance	V_{GS} = 0, V_{DS} = -15V	8		8		mS
g_{os}	Output Conductance			1		1	mS
$I_{D(off)}$	Drain (OFF) Leakage	V_{DS} = -10V, V_{GS} = 15V		-100		-100	pA
$r_{DS(on)}$	Drain-Source "ON" Resistance	V_{GS} = 0, V_{DS} = -0.1V		75		60	Ω
C_{iss}	Input Capacitance	V_{DG} = -20V, V_{GS} = 0 (Note 1)		35		35	pF
C_{rss}	Reverse Transfer Capacitance	V_{DG} = -10V, I_S = 0 (Note 1)		12		12	pF

NOTE 1: For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

IT120, IT122
Dual NPN General Purpose Amplifier

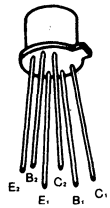
INTERSIL

FEATURES

- High h_{FE} at Low Current
- Low Output Capacitance
- Good Matching
- Tight V_{BE} Tracking

PIN CONFIGURATION

TO-71
TO-78



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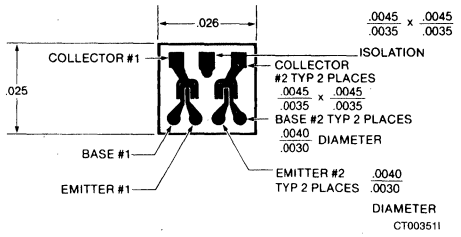
CHIP TOPOGRAPHY



ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Collector-Base Voltage (Note 1) 45V
Collector-Emitter Voltage (Note 1) 45V
Emitter Base Voltage (Notes 1 and 2) 7V
Collector Current (Note 1) 50mA
Collector-Collector Voltage 60V
Storage Temperature Range ..... −65°C to +200°C
Operating Temperature Range ..... −55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C

	TO-78		TO-71	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Power Dissipation	250mW	500mW	200mW	400mW
Derate Above 25°C	1.7mW/°C	3.3mW/°C	1.3mW/°C	2.7mW/°C

ORDERING INFORMATION*

TO-78	TO-71	WAFER	DICE
IT120	IT120-TO71	IT120/W	IT120/D
IT121	IT121-TO71	IT121/W	IT121/D
IT122	IT122-TO71	IT122/W	IT122/D

*When ordering wafer/dice refer to Section 10, page 10–1.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	IT120A		IT120		IT121		IT122		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
h_{FE}	DC Current Gain	I_C = 10μA, V_{CE} = 5.0V	200		200		80		80		
		I_C = 1.0mA, V_{CE} = 5.0V	225		225		100		100		
		T_A = −55°C; I_C = 10μA, V_{CE} = 5.0V	75		75		30		30		
V_{BE}(ON)	Emitter-Base On Voltage	I_C = 10μA, V_{CE} = 5.0V		0.7		0.7		0.7		0.7	V
V_{CE}(SAT)	Collector Saturation Voltage	I_C = 0.5mA, I_B = 0.05mA		0.5		0.5		0.5		0.5	V
I_{CBO}	Collector Cutoff Current	I_E = 0, V_{CB} = 45V		1.0		1.0		1.0		1.0	nA
		T_A = +150°C; I_E = 0, V_{CB} = 45V		10		10		10		10	μA
I_{EBO}	Emitter Cutoff Current	I_C = 0, V_{EB} = 5.0V		1.0		1.0		1.0		1.0	nA
C_{obo}	Output Capacitance	I_E = 0, V_{CB} = 5.0V, f = 1MHz (Note 3)		2.0		2.0		2.0		2.0	pF
C_{te}	Emitter Transition Capacitance	I_C = 0, V_{EB} = 0.5V, f = 1MHz (Note 3)		2.5		2.5		2.5		2.5	pF
C_{C_1,C_2}	Collector to Collector Capacitance	V_{CC} = 0, f = 1MHz (Note 3)		4.0		4.0		4.0		4.0	pF
I_{C_1,C_2}	Collector to Collector Leakage Current	V_{CC} = ±60V (Note 3)		10		10		10		10	nA

Note: All typical values have been guaranteed by characterization and are not tested.

IT120, IT122

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	IT120A		IT120		IT121		IT122		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{CEO}(SUST)$	Collector to Emitter Sustaining Voltage	I_C = 1.0mA, I_B = 0	45		45		45		45		V
GBW	Current Gain Bandwidth Product (Note 3)	I_C = 10μA, V_{CE} = 5V I_C = 1mA, V_{CE} = 5V	10 220		10 220		7 180		7 180		MHz
$\lvert V_{BE_1} - V_{BE_2} \rvert$	Base Emitter Voltage Differential	I_C = 10μA, V_{CE} = 5.0V		1		2		3		5	mV
$\lvert I_{B_1} - I_{B_2} \rvert$	Base Current Differential			2.5		5		25		25	nA
$\frac{\Delta(V_{BE_1} - V_{BE_2})}{\Delta T}$	Base-Emitter Voltage Differential Change with Temperature	(Note 3) T_A = −55°C to +125°C I_C = 10μA, V_{CE} = 5.0V		3		5		10		20	μV/°C

NOTES: 1. Per transistor.
2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10μA.
3. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

IT124
Dual Super-Beta NPN General Purpose Amplifier

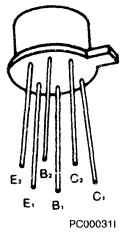
INTERSIL

FEATURES

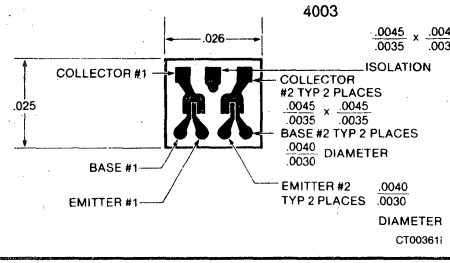
- Very High Gain
- Low Output Capacitance
- Tight V_{BE} Matching
- High GBW

PIN CONFIGURATION

TO-78



CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-78	WAFER	DICE
IT124	IT124/W	IT124/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Collector-Base Voltage (Note 1) 2V
Collector-Emitter Voltage (Note 1) 2V
Emitter-Base Voltage (Notes 1 and 2) 7V
Collector-Current (Note 1) 10mA
Collector-Collector Voltage 100V
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C

	TO-78	
	ONE SIDE	BOTH SIDES
Power Dissipation	300mW	500mW
Derate above 25°C	2.4mW/°C	4.0mW/°C

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNIT
h_{FE}	DC Current Gain	I_C = 1μA, V_{CE} = 1V	1500		
		I_C = 10μA, V_{CE} = 1V	1500		
	T_A = -55°C	I_C = 10μA, V_{CE} = 1V	600		
V_{BE}(ON)	Emitter-Base "ON" Voltage			0.7	V
V_{CE}(SAT)	Collector Saturation Voltage	I_C = 1mA, I_B = 0.1mA		0.5	V
I_{CBO}	Collector Cutoff Current	I_E = 0, V_{CB} = 1V		100	pA
	T_A = +150°C	I_E = 0, V_{CB} = 1V		100	nA
I_{EBO}	Emitter Cutoff Current	I_C = 0, V_{EB} = 5V		100	pA
C_{obo}	Output Capacitance (Note 3)	I_E = 0, V_{CB} = 1V, f = 1MHz		0.8	pF
C_{te}	Emitter Transition Capacitance (Note 3)	I_C = 0, V_{EB} = 0.5V, f = 1MHz		1.0	pF
$C_{C_1C_2}$	Collector to Collector Capacitance (Note 3)	V_{CC} = 0		0.8	pF
$I_{C_1C_2}$	Collector to Collector Leakage Current	V_{CC} = ±50V		250	pA
GBW	Current Gain Bandwidth Product (Note 3)	I_C = 10μA, V_{CE} = 1V	10		MHz
		I_C = 100μA, V_{CE} = 1V	100		MHz
NF	Narrow Band Noise Figure (Note 3)	I_C = 10μA, V_{CE} = 3V, f = 1kHz, R_G = 10kΩ, BW = 200Hz		3	dB
BV_{CBO}	Collector-Base Breakdown Voltage	I_C = 10μA, I_E = 0	2		V
BV_{EBO} (Note 2)	Emitter-Base Breakdown Voltage	I_E = 10μA, I_C = 0	7		V
V_{CEO}(SUST)	Collector-Emitter Sustaining Voltage	I_C = 1mA, I_B = 0	2		V

Note: All typical values have been guaranteed by characterization and are not tested.

IT124

INTERSIL

MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			TYP	MAX	
$\lvert V_{BE1}-V_{BE2}\rvert$	Base Emitter Voltage Differential	$I_C = 10\mu A$, $V_{CE} = 1V$	2	5	mV
$\Delta\lvert(V_{BE1}-V_{BE2})\rvert/\Delta T$	Base Emitter Voltage Differential Change with Temperature (Note 3)	$I_C = 10\mu A$, $V_{CE} = 1V$ $T = -55°C$ to $+125°C$	5	15	$\mu V/°C$
$\lvert I_{B1}-I_{B2}\rvert$	Base Current Differential	$T_C = 10\mu A$, $V_{CE} = 1V$		.6	nA

NOTES: 1. Per transistor.
2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10μA.
3. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

IT126-IT129
Dual NPN General Purpose Amplifier

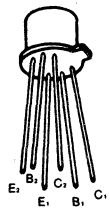
INTERSIL

FEATURES

- High Gain at Low Current
- Low Output Capacitance
- Tight I_B Match
- Tight V_{BE} Tracking
- Dielectrically Isolated Matched Pairs for Differential Amplifiers

PIN CONFIGURATION

TO-71
TO-78



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CHIP TOPOGRAPHY

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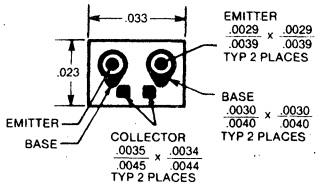


CT003711

ORDERING INFORMATION*

TO78	TO-71	WAFER	DICE
IT126	IT126-TO71	IT126/W	IT126/D
IT127	IT127-TO71	IT127/W	IT127/D
IT128	IT128-TO71	IT128/W	IT128/D
IT129	IT129-TO71	IT129/W	IT129/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise specified)

Collector-Base Voltage (Note 1)
- IT126, IT127 ..... 60V
- IT128 ..... 55V
- IT129 ..... 45V

Collector-Emitter Voltage (Note 1)
- IT126, IT127 ..... 60V
- IT128 ..... 55V
- IT129 ..... 45V

Emitter-Base Voltage (Notes 1 and 2) 7.0V
Collector Current (Note 1) 100mA
Collector-Collector Voltage 70V
Storage Temperature Range ..... -65°C to +175°C
Operating Temperature Range ..... -55°C to +175°C
Lead Temperature (Soldering, 10sec) ..... +300°C

	TO71		TO78	
Power Dissipation	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Total Dissipation at 25°C	200mW	400mW	250mW	500mW
Derating Factor	1.3 mW/°C	2.7 mW/°C	1.7 mW/°C	3.3 mW/°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	IT126		IT127		IT128		IT129		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
h_{FE}	DC Current Gain	I_C = 10μA, V_{CE} = 5V	150		150		100		70		
		I_C = 1.0mA, V_{CE} = 5V	200	800	200	800	150	800	100		
		I_C = 10mA, V_{CE} = 5V	230		230		170		115		
		I_C = 50mA, V_{CE} = 5V	100		100		75		50		
	T_A = -55°C	I_C = 1mA, V_{CE} = 5V	75		75		60		40		
$V_{BE(on)}$	Emitter-Base On Voltage	I_C = 10mA, V_{CE} = 5V		0.9		0.9		0.9		0.9	
		I_C = 50mA, V_{CE} = 5V		1.0		1.0		1.0		1.0	V
$V_{CE(sat)}$	Collector Saturation Voltage	I_C = 10mA, I_B = 1mA		0.3		0.3		0.3		0.3	
		I_C = 50mA, I_B = 5mA		1.0		1.0		1.0		1.0	
I_{CBO}	Collector Cutoff Current	I_E = 0, V_{CB} = 45V, 30V*		0.1		0.1		0.1		0.1*	nA
	T_A = +150°C			0.1		0.1		0.1		0.1*	μA
I_{EBO}	Emitter Cutoff Current	I_C = 0, V_{EB} = 5V		0.1		0.1		0.1		0.1	nA

Note: All typical values have been guaranteed by characterization and are not tested.

IT126-IT129

INTERSIL

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	IT126		IT127		IT128		IT129		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
C_{obo}	Output Capacitance (Note 3)	$I_E = 0$, $V_{CB} = 20V$		3		3		3		3	pF
$BV_{C_1\ C_2}$	Collector to Collector Breakdown Voltage	$I_C = \pm 1\mu A$	±100		±100		±100		±100		V
$V_{CEO(sust)}$	Collector to Emitter Sustaining Voltage	$I_C = 1mA$, $I_B = 0$	60		60		55		45		
BV_{CBO}	Collector Base Breakdown Voltage	$I_C = 10\mu A$, $I_E = 0$	60		60		55		45		
BV_{EBO}	Emitter Base Breakdown Voltage	$I_E = 10\mu A$, $I_C = 0$	7		7		7		7		

MATCHING CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	IT126		IT127		IT128		IT129		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$\lvert V_{BE_1} - V_{BE_2} \rvert$	Base Emitter Voltage Differential	$I_C = 1mA$, $V_{CE} = 5V$		1		2		3		5	mV
$\frac{\Delta(\lvert V_{BE_1} - V_{BE_2} \rvert)}{\Delta T}$	Base Emitter Voltage Differential Change with Temperature (Note 3)	$I_C = 1mA$, $V_{CE} = 5V$ $T_A = -55°C$ to $+125°C$		3		5		10		20	µV/°C
$\lvert I_{B_1} - I_{B_2} \rvert$	Base Current Differential	$I_C = 10\mu A$, $V_{CE} = 5V$		2.5		5		10		20	nA
		$I_C = 1mA$, $V_{CE} = 5V$		0.25		0.5		1.0		2.0	µA

NOTES: 1. Per transistor.
2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10µA.
3. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

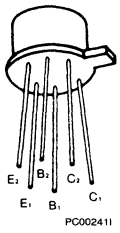
IT130–IT132
Dual PNP
General Purpose Amplifier

INTERSIL

FEATURES
- High h_{FE} at Low Current
- Low Output Capacitance
- Tight I_B Match
- Tight V_{BE} Tracking

PIN CONFIGURATIONS

TO-71
TO-78



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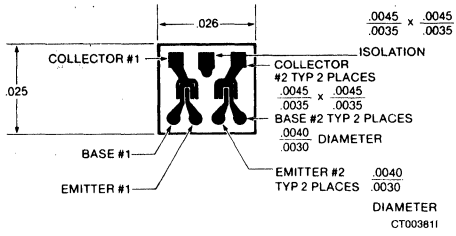
CHIP TOPOGRAPHY



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ORDERING INFORMATION*

TO-78	TO-71	WAFER	DICE
IT130A	IT130A-TO71	IT130A/W	IT130A/D
IT130	IT130-TO71	IT130/W	IT130/D
IT131	IT131-TO71	IT131/W	IT131/D
IT132	IT132-TO71	IT132/W	IT132/D

*When ordering wafer/dice refer to Section 10, page 10–1.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise specified)

Collector-Base Voltage (Note 1) 45V
Collector-Emitter Voltage (Note 1) 45V
Emitter Base Voltage (Notes 1 and 2) 7V
Collector Current (Note 1) 50mA
Collector-Collector Voltage 60V
Storage Temperature Range ..... −65°C to +175°C
Operating Temperature Range ..... −55°C to +175°C
Lead Temperature (Soldering, 10sec) ..... +300°C

	TO-71		TO-78	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Power Dissipation	200mW 1.3mW/°C	400mW 2.7mW/°C	250mW 1.7mW/°C	500mW 3.3mW/°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	IT130A		IT130		IT131		IT132		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
h_{FE}	DC Current Gain	I_C = 10μA, V_{CE} = 5.0V	200		200		80		80		
		I_C = 1.0mA, V_{CE} = 5.0V	225		225		100		100		
	T_A = −55°C	I_C = 10μA, V_{CE} = 5.0V	75		75		30		30		
V_{BE}(ON)	Emitter-Base On Voltage	I_C = 10μA, V_{CE} = 5.0V		0.7		0.7		0.7		0.7	V
V_{CE}(SAT)	Collector Saturation Voltage	I_C = 0.5mA, I_B = 0.05mA		0.5		0.5		0.5		0.5	
I_{CBO}	Collector Cutoff Current	I_E = 0, V_{CB} = 45V		−1.0		−1.0		−1.0		−1.0	nA
	T_A = +150°C			−10		−10		−10		−10	μA
I_{EBO}	Emitter Cutoff Current	I_C = 0, V_{EB} = 5.0V		−1.0		−1.0		−1.0		−1.0	nA
C_{ob} (Note 3)	Output Capacitance	I_E = 0, V_{CB} = 5.0V		2.0		2.0		2.0		2.0	
C_{te} (Note 3)	Emitter Transition Capacitance	I_C = 0, V_{EB} = 0.5V		2.5		2.5		2.5		2.5	pF
$C_{C_1-C_2}$ (Note 3)	Collector to Collector Capacitance	V_{CC} = 0		4.0		4.0		4.0		4.0	
$I_{C_1-C_2}$	Collector to Collector Leakage Current	V_{CC} = ±60V		10		10		10		10	nA
V_{CEO}(SUST)	Collector to Emitter Sustaining Voltage	I_C = 1.0mA, I_B = 0	−45		−45		−45		−45		V
GBW	Current Gain Bandwidth Product (Note 3)	I_C = 10μA, V_{CE} = 5V	5		5		4		4		MHz
		I_C = 1mA, V_{CE} = 5V	110		110		90		90		
$\lvert V_{BE_1}-V_{BE_2}\rvert$	Base Emitter Voltage Differential	I_C = 10μA, V_{CE} = 5.0V		1		2		3		5	mV

Note: All typical values have been guaranteed by characterization and are not tested.

IT130–IT132

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	IT130A		IT130		IT131		IT132		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$\lvert I_{B_1}-I_{B_2}\rvert$	Base Current Differential	$I_C = 10\mu A$, $V_{CE} = 5.0V$		2.5		5		25		25	nA
$\Delta(V_{BE_1}-V_{BE_2})/\Delta T$	Base-Emitter Voltage Differential Change with Temperature (Note 3)	$T_A = -55°C$ to $+125°C$ $I_C = 10\mu A$, $V_{CE} = 5.0V$		3		5		10		20	$\mu V/°C$

NOTES: 1. Per transistor.
2. The reverse base-to-emitter voltage must never exceed 7.0V, and the reverse base-to-emitter current must never exceed 10μA.
3. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

IT136–IT139
Dual PNP General Purpose Amplifier

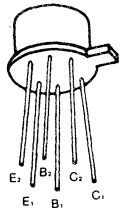
INTERSIL

FEATURES

- High Gain at Low Current
- Low Output Capacitance
- Tight I_B Match
- Tight V_{BE} Tracking
- Dielectrically Isolated Matched Pairs for Differential Amplifiers

PIN CONFIGURATION

TO-71
TO-78



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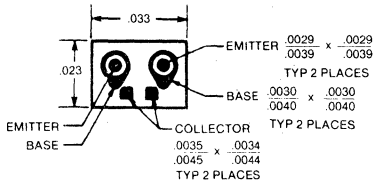

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ORDERING INFORMATION*

TO-78	TO-71	WAFER	DICE
IT136	IT136-TO71	IT136/W	IT136/D
IT137	IT137-TO71	IT137/W	IT137/D
IT138	IT138-TO71	IT138/W	IT138/D
IT139	IT139-TO71	IT139/W	IT139/D

*When ordering wafer/dice refer to Section 10, page 10–1.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Collector-Base Voltage (Note 1)
- IT136, IT137 ..... 60V
- IT138 ..... 55V
- IT139 ..... 45V

Collector-Emitter Voltage (Note 1)
- IT136, IT137 ..... 60V
- IT 138 ..... 55V
- IT139 ..... 45V

Emitter Base Voltage (Notes 1 and 2) 7V
Collector Current (Note 1) 100mA
Collector-Collector Voltage 70V
Storage Temperature Range ..... −65°C to +175°C
Operating Temperature Range ..... −55°C to +175°C
Lead Temperature (Soldering, 10sec) ..... +300°C

	TO-71		TO-78	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Power Dissipation	200mW	400mW	250mW	500mW
Derate above 25°C ...	1.3mW/°C	2.7mW/°C	1.7mW/°C	3.3mW/°C

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	IT136		IT137		IT138		IT139		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
h_{FE}	DC Current Gain	I_C = 10μA, V_{CE} = 5V	150		150		100		70		
		I_C = 1.0mA, V_{CE} = 5V	150	800	150	800	100	800	70	800	
		I_C = 10mA, V_{CE} = 5V	125		125		80		50		
		I_C = 50mA, V_{CE} = 5V	65		60		40		25		
	T_A = 55°C	I_C = 1mA, V_{CE} = 5V	75		75		60		40		
$V_{BE(on)}$	Emitter-Base On Voltage	I_C = 10mA, V_{CE} = 5V		.9		.9		.9		.9	V
		I_C = 50mA, V_{CE} = 5V		1.0		1.0		1.0		1.0	
$V_{CE(sat)}$	Collector Saturation Voltage	I_C = 1mA, I_B = .1mA		.3		.3		.3		.3	
		I_C = 10mA, I_B = 1mA		.6		.6		.6		.6	

Note: All typical values have been guaranteed by characterization and are not tested.

IT136-IT139

INTERSIL

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	IT136		IT137		IT138		IT139		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{CBO}	Collector Cutoff Current	$I_E = 0$, $V_{CB} = 45V$, 30V*		0.1		0.1		0.1		0.1*	nA
	$T_A = +150°C$			0.1		0.1		0.1		0.1*	μA
I_{EBO}	Emitter Cutoff Current	$I_C = 0$, $V_{EB} = 5V$		0.1		0.1		0.1		0.1	nA
C_{obo}	Output Capacitance (Note 3)	$I_E = 0$, $V_{CB} = 20V$, f = 1MHz		3		3		3		3	pF
$BV_{C_1C_2}$	Collector to Collector Breakdown Voltage	$I_C = \pm 1\mu A$	±100		±100		±100		±100		V
$V_{CEO(sust)}$	Collector to Emitter Sustaining Voltage	$I_C = 1mA$, $I_B = 0$	60		60		55		45		
BV_{CBO}	Collector Base Breakdown Voltage	$I_C = 10\mu A$, $I_E = 0$	60		60		55		45		
BV_{EBO}	Emitter Base Breakdown Voltage	$I_E = 10\mu A$, $I_C = 0$	7		7		7		7		
$\lvert V_{BE_1} - V_{BE_2} \rvert$	Base Emitter Voltage Differential	$I_C = 1mA$, $V_{CE} = 5V$		1		2		3		5	mV
$\Delta\lvert(V_{BE_1} - V_{BE_2})\rvert / \Delta T$	Base Emitter Voltage Differential Change with Temperature (Note 3)	$I_C = 1mA$, $V_{CE} = 5V$ $T_A = -55°C$ to $+125°C$		3		5		10		20	μV/°C
$\lvert I_{B_1} - I_{B_2} \rvert$	Base Current Differential	$I_C = 10\mu A$, $V_{CE} = 5V$		2.5		5		10		20	nA
		$I_C = 1mA$, $V_{CE} = 5V$		.25		.5		1.0		2.0	μA

NOTES: 1. Per transistor.
2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10μA.
3. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

IT500–IT505
Dual Cascoded N-Channel JFET General Purpose Amplifier

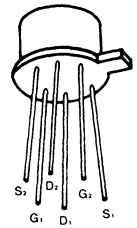
INTERSIL

GENERAL DESCRIPTION

A low noise, low leakage FET that employs a cascode structure to accomplish very low I_G at high voltage levels, while giving high transconductance and very high common, mode rejection ratio.

PIN CONFIGURATION

TO-71
low profile



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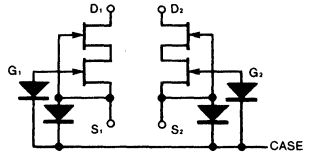
SCHEMATIC DIAGRAM



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ORDERING INFORMATION*

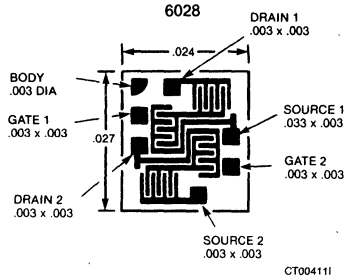
TO-71	WAFER	DICE
IT500	IT500/W	IT500/D
IT501	IT501/W	IT501/D
IT502	IT502/W	IT502/D
IT503	IT503/W	IT503/D
IT504	IT504/W	IT504/D
IT505	IT505/W	IT505/D

*When ordering wafer/dice refer to Section 10, page 10–1.

FEATURES

- C_{MRR} > 120dB
- I_G < 5pA @ 50V_{DG}
- C_{rss} < 0.5pF
- g_{os} > .025μs

CHIP TOPOGRAPHY



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ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise specified)

Drain-Source and Drain-Gate Voltages (Note 1) 60V
Drain Current (Note 1) 50mA
Gate-Gate Voltage ..... ±60V
Storage Temperature ..... -65°C to +200°C
Operating Temperature ..... -55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C

	ONE SIDE	BOTH SIDES
Power Dissipation (Note 3)	250mW	500mW
Derate above 25°C.....	3.8mW/°C	7.7mW/°C

NOTE 1. Per transistor.

NOTE 2. Due to the non-symmetrical structure of these devices, the drain and source ARE NOT interchangeable.

NOTE 3. @ 85°C free air temp.

Note: All typical values have been guaranteed by characterization and are not tested.

IT500-IT505

INTERSIL

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise specified)

SYMBOL	CHARACTERISTICS	TEST CONDITIONS		LIMITS MIN	LIMITS MAX	UNIT
I_{GSS}	Gate Reverse Current	$V_{GS} = -20V$, $V_{DS} = 0$			-100	pA
	$T_A = 125°C$				-5	nA
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = -1\mu A$, $V_{DS} = 0$		-60		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 20V$, $I_D = 1nA$		-0.7	-4	V
V_{GS}	Gate-Source Voltage	$V_{DG} = 50V$, $I_D = 200\mu A$		-0.2	-3.8	V
I_G	Gate Operating Current				-5	pA
	$T_A = 125°C$				-5	nA
I_{DSS}	Saturation Drain Current (Note 1)	$V_{DS} = 20V$, $V_{GS} = 0$		0.7	7	mA
g_{fs}	Common-Source Forward Transconductance (Note 1)	$V_{DS} = 20V$, $V_{GS} = 0$	f = 1kHz	1000	4000	μs
g_{fs}	Common-Source Forward Transconductance (Note 1)	$V_{DG} = 20V$, $I_D = 200\mu A$		700	1600	
g_{os}	Common-Source Output Conductance	$V_{DS} = 20V$, $V_{GS} = 0$			1	
g_{os}	Common-Source Output Conductance	$V_{DS} = 20V$, $I_D = 200\mu A$			0.025	
C_{g1g2}	Gate to Gate Capacitance (Note 4)	$V_{G1} = V_{G2} = 10V$	f = 1MHz		3.5	pF
C_{iss}	Common-Source Input Capacitance (Note 4)	$V_{DS} = 20V$, $V_{GS} = 0$			7	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 3, 4)				0.5	
NF	Spot Noise Figure (Note 4)		f = 100Hz, $R_G = 10M\Omega$		0.5	dB
$\bar{e}_n$	Equivalent Input Noise Voltage (Note 4)		f = 10Hz		0.035	$\frac{\mu V}{\sqrt{Hz}}$
			f = 1kHz		0.010	

SYMBOL	CHARACTERISTICS	TEST CONDITIONS		IT500 MIN	IT500 MAX	IT501 MIN	IT501 MAX	IT502 MIN	IT502 MAX	IT503 MIN	IT503 MAX	IT504 MIN	IT504 MAX	IT505 MIN	IT505 MAX	UNIT
$I_{G1}-I_{G2}$	Differential Gate Current	$V_{DG} = 20V$, $I_D = 200\mu A$	+125°C		5		5		5		5		10		15	nA
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 1)	$V_{DS} = 20V$, $V_{GS} = 0V$		0.95	1	0.95	1	0.95	1	0.95	1	0.9	1	0.85	1	
g_{fs1}/g_{fs2}	Transconductance Ratio (Note 1)		f = 1kHz	0.97	1	0.97	1	0.95	1	0.95	1	0.90	1	0.85	1	
$V_{GS1}-V_{GS2}$	Differential Gate-Source Voltage				5		5		10		15		25		50	mV
$\frac{\Delta V_{GS1}-V_{GS2}}{\Delta T}$	Gate-Source Differential Voltage	$V_{DG} = 20V$ $I_D = 200\mu A$	$T_A = 25°C$ $T_B = 125°C$		5		10		20		40		100		200	μV/°C
	Change with Temp. (Note 2, 4)		$T_A = -55°C$ $T_B = 25°C$		5		10		20		40		100		200	
C_{MRR}**	Common Mode Rejection Ratio (Note 4)	$\Delta V_{DD} = 10V$, $I_D = 200\mu A$		120		120		120		120		120		120		dB

** $C_{MRR} = 20 \log_{10} \Delta V_{DD} / \Delta [V_{gs1} - V_{gs2}]$, $\Delta V_{DD} = 10/-20V$

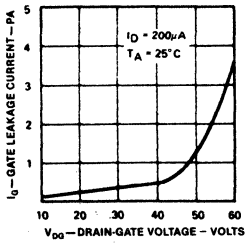
NOTES: 1. Pulse test required, pulsewidth = 300μs, duty cycle ≤ 3%.
2. Measured at end points, T_A and T_B.
3. With case guarded C_{rss} is typically < 0.15pF.
4. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

IT500-IT505

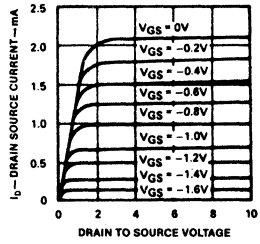
TYPICAL PERFORMANCE CHARACTERISTICS

GATE LEAKAGE



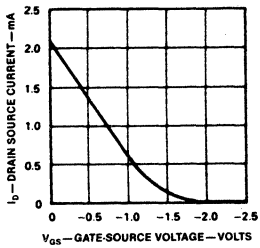
OP00211I

OUTPUT CHARACTERISTICS



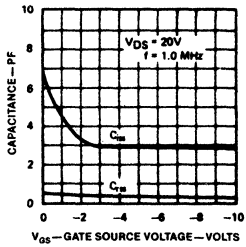
OP00221I

OUTPUT CHARACTERISTICS



OP00231I

TYPICAL CAPACITANCE VS. GATE-SOURCE VOLTAGE



OP00241I

Note: All typical values have been guaranteed by characterization and are not tested.

IT550
Dual N-Channel JFET Switch

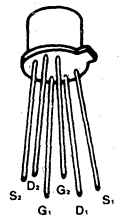
INTERSIL

FEATURES

- **Specified Matching Characteristics**
- **High Gain**
- **Low "ON" Resistance**

PIN CONFIGURATION

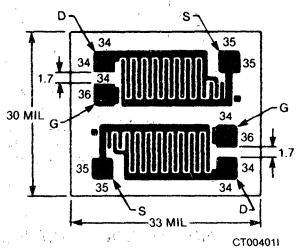
TO-71



PC000511

CHIP TOPOGRAPHY

6033



CT004011

ORDERING INFORMATION*

TO-71	WAFER	DICE
IT550	IT550/W	IT550/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ABSOLUTE MAXIMUM RATINGS

(25°C Unless otherwise noted)

Gate-Drain or Gate-Source Voltage ..... -40V
Gate Current 50mA
Gate-Gate Voltage ..... ±80V
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +175°C
Lead Temperature (Soldering, 10sec) ..... +300°C

	ONE SIDE	BOTH SIDES
Power Dissipation	325mW	650mW
Derate above 25°C	2.2mW/°C	4.3mW/°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS MIN	LIMITS MAX	UNIT
I_{GSSR}	Gate-Reverse Current	V_{GS} = -20V, V_{DS} = 0			-100	pA
	T_A = 150°C				-200	mA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = -1μA, V_{DS} = 0		-40		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 15V, I_D = 1nA		-0.5	-3	
$V_{GS(f)}$	Gate-Source Voltage	V_{DS} = 0V, I_G = 2mA			1.0	
I_{DSS}	Saturation Drain Current (Note 1)	V_{DS} = 15V, V_{GS} = 0		5	30	mA
$r_{DS(on)}$	Static Drain Source ON Resistance	I_D = 1mA, V_{GS} = 0			100	Ω
g_{fs}	Common-Source Forward Transconductance (Note 1)	V_{DG} = 15V, I_D = 2mA	f = 1kHz	7500	12,500	μs
			f = 100MHz (Note 4)	7000		
g_{os}	Common-Source Output Conductance		f = 1kHz		45	
C_{rss}	Common-Source Reverse Transfer Capacitance		f = 1MHz (Note 4)		3	pF
C_{iss}	Common-Source Input Capacitance				12	
NF	Spot Noise Figure (Note 4)		f = 10Hz, R_g = 1M		1.0	dB
e_n	Equivalent Short Circuit Input Noise Voltage (Note 4)		f = 10Hz		50	$\frac{nV}{\sqrt{Hz}}$
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1, 2)	V_{DS} = 15V, V_{GS} = 0		0.95	1	—

Note: All typical values have been guaranteed by characterization and are not tested.

IT550

INTERSIL

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage	V_{DS} = 15V, I_D = 2mA		50	mV
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 3)	(T_A = −55°C to +125°C)		100	µV/°C
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Notes 1, 2)	V_{DS} = 15V, I_D = 2mA f = 1kHz	0.90	1	—

NOTES: 1. Pulse test required; pulse width 300µs, duty cycle ≤ 3%.
2. Assumes smaller value in numerator.
3. Measured at end points T_A and T_B.
4. For design reference only, not 100% tested.

2

Note: All typical values have been guaranteed by characterization and are not tested.

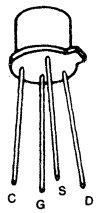
IT1700
P-Channel Enhancement Mode MOSFET General Purpose Amplifier

INTERSIL

FEATURES
- Low ON-Resistance
- High Gain
- Low Noise Voltage
- High Input Impedance
- Low Leakage

PIN CONFIGURATION

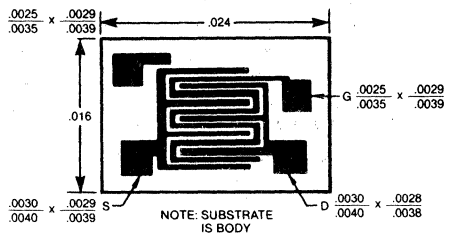
TO-72



PC002711

CHIP TOPOGRAPHY

1503



CT00421I

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Drain-Source and Gate-Source Voltage ..... −40V
Peak Gate-Source Voltage (Note 1) ..... ±125V
Drain Current 50mA
Storage Temperature ..... −65°C to +200°C
Operating Temperature Range ..... −55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 375mW
Derate above 25°C ..... 3mW/°C

ORDERING INFORMATION*

TO-72	WAFER	DICE
IT1700	IT1700/W	IT1700/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted), V_{BS} = 0 unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNIT
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0, I_D = −10μA	−40		V
BV_{SDS}	Source to Drain Breakdown Voltage	V_{GS} = 0, I_D = −10μA	−40		V
I_{GSS}	Gate Leakage Current		(See note 2)		
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0, V_{DS} = −20V		200	pA
I_{DSS} (150°C)	Drain to Source Leakage Current			0.4	μA
I_{SDS}	Source to Drain Leakage Current			400	pA
I_{SDS} (150°C)	Source to Drain Leakage Current			0.8	μA
$V_{GS}(th)$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = −10μA	−2	−5	V
$r_{DS(on)}$	Static Drain to Source "on" Resistance	V_{GS} = −10V, V_{DS} = 0		400	ohms
$I_{DS(on)}$	Drain to Source "on" Current	V_{GS} = −10V, V_{DS} = −15V	2		mA
g_{fs}	Forward Transconductance Common Source	V_{DS} = −15V, I_D = −10mA f = 1kHz	2000	4000	μs
C_{iss}	Small Signal, Short Circuit, Common Source, Input Capacitance	V_{DS} = −15V, I_D = −10mA f = 1MHz (Note 3)		5	pF
C_{rss}	Small Signal, Short Circuit, Common Source, Reverse Transfer Capacitance	V_{DG} = −15V, I_D = 0 f = 1MHz (Note 3)		1.2	pF
C_{oss}	Small Signal, Short Circuit, Common Source, Output Capacitance	V_{DS} = −15V, I_D = −10mA f = 1MHz (Note 3)		3.5	pF

NOTES:
1. Device must not be tested at ±125V more than once nor longer than 300ms.
2. Actual gate current is immeasurable. Package suppliers are required to guarantee a package leakage of < 10pA. External package leakage is the dominant mode which is sensitive to both transient and storage environment, which cannot be guaranteed.
3. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

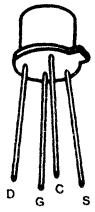
IT1750
N-Channel Enhancement Mode MOSFET General Purpose Amplifier Switch

INTERSIL

FEATURES
- Low ON Resistance
- Low C_{dg}
- High Gain
- Low Threshold Voltage

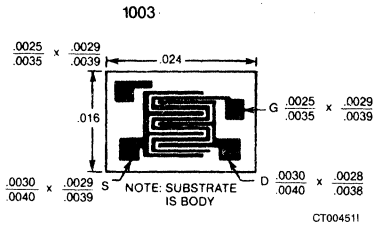
PIN CONFIGURATION

TO-72



PC000711

CHIP TOPOGRAPHY



CT004511

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Drain-Source and Gate-Source Voltage 25V
Peak Gate-Source Voltage (Note 1) ..... ±125V
Drain Current 100mA
Storage Temperature Range ..... −65°C to +200°C
Operating Temperature Range ..... −55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 375mW
Derate above 25°C ..... 3mW/°C

ORDERING INFORMATION*

TO-72	WAFER	DICE
IT1750	IT1750/W	IT1750/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ELECTRICAL CHARACTERISTICS
(T_A = 25°C, Body connected to Source and V_{BS} = 0 unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 10μA	0.50	1.5	3.0	V
I_{DSS}	Drain Leakage Current	V_{DS} = 10V, V_{GS} = 0		0.1	10	nA
I_{GSS}	Gate Leakage Current		See note 2.			
BV_{DSS}	Drain Breakdown Voltage	I_D = 10μA, V_{GS} = 0	25			V
$r_{DS(on)}$	Drain To Source on Resistance	V_{GS} = 20V		25	50	ohms
$I_{D(on)}$	Drain Current	V_{DS} = V_{GS} = 10V	10	50		mA
Y_{fs}	Forward Transadmittance	V_{DS} = 10V, I_D = 10mA, f = 1kHz	3,000			μs
C_{iss}	Total Gate Input Capacitance	I_D = 10mA, V_{DS} = 10V, f = 1MHz (Note 3)		5.0	6.0	pF
C_{dg}	Gate to Drain Capacitance	V_{DG} = 10V, f = 1MHz (Note 3)		1.3	1.6	pF

NOTES:
1. Devices must not be tested at ±125V more than once nor longer than 300ms.
2. Actual gate current is immeasurable. Package suppliers are required to guarantee a package leakage of < 10pA. External package leakage is the dominant mode which is sensitive to both transient and storage environment, which cannot be guaranteed.
3. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

J105–J107
N-Channel JFET Switch

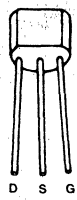
INTERSIL

FEATURES
- Low $r_{DS(on)}$

APPLICATIONS
- Analog Switches
- Choppers
- Commutators

PIN CONFIGURATION

TO-92



PC00131I

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage ..... −25V
Gate Current 50mA
Storage Temperature Range ..... −55°C to +150°C
Operating Temperature Range ..... −55°C to +135°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 360mW
Derate above 25°C ..... 3.3mW/°C

ORDERING INFORMATION*

J105	TO-92 only
J106	TO-92 only
J107	TO-92 only

*When ordering wafer/dice refer to Section 10, page 10–1.

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

SYMBOL	PARAMETER	TEST CONDITIONS	J105			J106			J107			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{GSS}	Gate-Reverse Current (Note 1)	V_{DS} = 0V, V_{GS} = −15V			−3			−3			−3	nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 5V, I_D = 1μA	−4.5		−10	−2		−6	−0.5		−4.5	V
BV_{GSS}	Gate-Source Breakdown Voltage	V_{DS} = 0V, I_G = −1μA	−25			−25			−25			
I_{DSS}	Drain Saturation Current (Note 2)	V_{DS} = 15V, V_{GS} = 0V	500			200			100			mA
$I_{D(off)}$	Drain Cutoff Current (Note 1)	V_{DS} = 5V, V_{GS} = −10V			3			3			3	nA
$r_{DS(on)}$	Drain source ON Resistance	V_{DS} ≤ 0.1V, V_{GS} = 0V			3			6			8	Ω
$C_{dg(off)}$	Drain Gate OFF Capacitance	V_{DS} = 0V, V_{GS} = −10V (Note 3), f = 1MHz			35			35			35	pF
$C_{sg(off)}$	Source Gate OFF Capacitance				35			35			35	
$C_{dg(on)}$ + $C_{sg(on)}$	Drain Gate plus Source Gate ON Capacitance	(Note 3) V_{DS} = V_{GS} = 0V, f = 1MHz			160			160			160	
$t_{d(on)}$	Turn On Delay Time	Switching Time-Test Conditions (Note 3)		15			15			15		ns
t_r	Rise Time			20			20			20		
$t_{d(off)}$	Turn Off Delay Time			15			15			15		
t_f	Fall Time			20			20			20		

Switching Time-Test Conditions (Note 3)	J105	J106	J107
V_{DD}	1.5V	1.5V	1.5V
$V_{GS(off)}$	−12V	−7V	−5V
R_L	50Ω	50Ω	50Ω

NOTES: 1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300μs; duty cycle ≤ 3%.
3. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

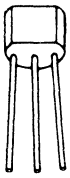
J111–J113
N-Channel JFET Switch

FEATURES
- Low Cost
- Automated Insertion Package
- Low Insertion Loss
- No Offset or Error Voltage Generated By Closed Switch
  - Purely Resistive
  - High Isolation Resistance From Driver
- Fast Switching
- Short Sample and Hold Aperture Time

APPLICATIONS
- Analog Switches
- Choppers
- Commutators

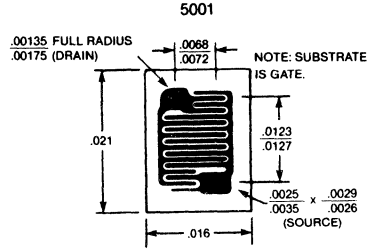
PIN CONFIGURATION

TO-92



PC001311

CHIP TOPOGRAPHY



CT00660I

ORDERING INFORMATION*

TO-92	WAFER	DICE
J111	J111/W	J111/D
J112	J112/W	J112/D
J113	J113/W	J113/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage ..... -35V
Gate Current 50mA
Storage Temperature Range ..... -55°C to +150°C
Operating Temperature Range ..... -55°C to +135°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 360mW
Derate Above 25°C ..... 3.3mW/°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

SYMBOL	PARAMETER	TEST CONDITIONS		J111			J112			J113			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{GSSR}	Gate Reverse Current (Note 1)	V_{DS} = 0V, V_{GS} = -15V				-1			-1			-1	nA
$V_{GS(off)}$	Gate Source Cutoff Voltage	V_{DS} = 5V, I_D = 1μA		-3		-10	-1		-5	-0.5		-3	V
BV_{GSS}	Gate Source Breakdown Voltage	V_{DS} = 0V, I_G = -1μA		-35			-35			-35			V
I_{DSS}	Drain Saturation Current (Note 2)	V_{DS} = 15V, V_{GS} = 0V		20			5			2			mA
$I_{D(off)}$	Drain Cutoff Current (Note 1)	V_{DS} = 5V, V_{GS} = -10V				1			1			1	nA
$r_{DS(on)}$	Drain Source ON Resistance	V_{DS} = 0.1V, V_{GS} = 0V				30			50			100	Ω
$C_{dg(off)}$	Drain Gate OFF Capacitance	V_{DS} = 0V, V_{GS} = -10V (Note 3)	f = 1MHz			5			5			5	pF
$C_{sg(off)}$	Source Gate OFF Capacitance					5			5			5	
$C_{dg(on)}$ + $C_{sg(on)}$	Drain Gate Plus Source Gate ON Capacitance	V_{DS} = V_{GS} = 0 (Note 3)				28			28			28	

Note: All typical values have been guaranteed by characterization and are not tested.

J111–J113

INTERSIL

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	J111			J112			J113			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{d(on)}$	Turn On Delay Time	Switching Time Test Conditions (Note 3)		7			7			7		ns
t_r	Rise Time	J111 J112 J113		6			6			6		
$t_{d(off)}$	Turn Off Delay Time	V_{DD} 10V 10V 10V		20			20			20		
t_f	Fall Time	$V_{GS(off)}$ −12V −7V −5V R_L 0.8kΩ 1.6kΩ 3.2kΩ		15			15			15		

NOTES: 1. Approximately doubles for every 10°C increase in T_A.
2. Pulse Test duration 300μs; duty cycle ≤ 3%.
3. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

J174–J177
P–Channel JFET Switch

INTERSIL

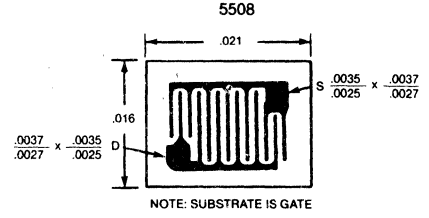
FEATURES
- Low Insertion Loss
- No Offset or Error Generated By Closed Switch
  - Purely Resistive
  - High Isolation Resistance From Driver
- Short Sample and Hold Aperture Time
- Fast Switching

APPLICATIONS
- Analog Switches
- Choppers
- Commutators

PIN CONFIGURATION

TO-92

CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-92	WAFER	DICE
J17X	J17X/W	J17X/D

*When ordering wafer/dice refer to Section 10, page 10–1.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage 30V
Gate Current 50mA
Storage Temperature Range ..... −55°C to +150°C
Operating Temperature Range ..... −55°C to +135°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Power Dissipation 350mW
Derate above 25°C ..... 3.3mW/°C

2

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

SYMBOL	PARAMETER	TEST CONDITIONS		J174			J175			J176			J177			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{GSS}	Gate Reverse Current (Note 1)	V_{DS} = 0, V_{GS} = 20V				1			1			1			1	nA
$V_{GS(off)}$	Gate Source Cutoff Voltage	V_{DS} = −15V, I_D = −10nA		5		10	3		6	1		4	0.8		2.25	V
BV_{GSS}	Gate Source Breakdown Voltage	V_{DS} = 0, I_G = 1μA		30			30			30			30			
I_{DSS}	Drain Saturation Current (Note 2)	V_{DS} = −15V, V_{GS} = 0		−20		−100	−7		−60	−2		−25	−1.5		−20	mA
$I_{D(off)}$	Drain Cutoff Current (Note 1)	V_{DS} = −15V, V_{GS} = 10V				−1			−1			−1			−1	nA
$r_{DS(on)}$	Drain-Source ON Resistance	V_{GS} = 0, V_{DS} = −0.1V				85			125			250			300	Ω
$C_{dg(off)}$	Drain-Gate OFF Capacitance	V_{DS} = 0, V_{GS} = 10V	f = 1MHz (Note 3)		5.5			5.5			5.5			5.5		pF
$C_{sg(off)}$	Source-Gate OFF Capacitance				5.5			5.5			5.5			5.5		
$C_{dg(on)}$ + $C_{sg(on)}$	Drain-Gate Plus Source Gate ON Capacitance	V_{DS} = V_{GS} = 0			40			40			40			40		

Note: All typical values have been guaranteed by characterization and are not tested.

J174–J177

INTERSIL

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	J174			J175			J176			J177			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{d(on)}$	Turn On Delay Time	Switching Time Test Conditions (Note 3) J174 / J175 / J176 / J177		2			5			15			20		ns
t_r	Rise Time	V_{DD} −10V / −6V / −6V / −6V		5			10			20			25		
$t_{d(off)}$	Turn Off Delay Time	$V_{GS(off)}$ 12V / 8V / 3V / 3V		5			10			15			20		
t_f	Fall Time	R_L 560Ω / 12kΩ / 5.6kΩ / 10kΩ $V_{GS(on)}$ 0V / 0V / 0V / 0V		10			20			20			25		

NOTES: 1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration −300μs; duty cycle ≤ 3%.
3. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

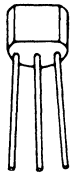
J201–J204
N-Channel JFET
General Purpose Amplifier

INTERSIL

FEATURES
- High Input Impedance
- Low I_{GSS}

PIN CONFIGURATION

TO-92



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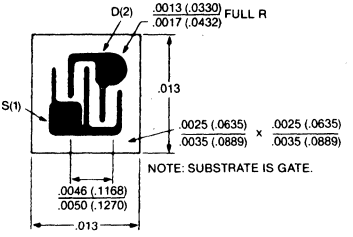
CHIP TOPOGRAPHY



CT004311

ORDERING INFORMATION*

TO-92	WAFER	DICE
J201	J201/W	J201/D
J202	J202/W	J202/D
J203	J203/W	J203/D
J204	J204/W	J204/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage ..... −40V
Gate Current 50mA
Storage Temperature Range ..... −55°C to +150°C
Operating Temperature Range ..... −55°C to +135°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 360mW
Derate above 25°C ..... 3.3mW/°C

2

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

SYMBOL	PARAMETER	TEST CONDITIONS		J201			J202			J203			J204			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{GSS}	Gate Reverse Current (Note 1)	V_{DS} = 0, V_{GS} = −20V				−100			−100			−100			−100	pA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 20V, I_D = 10nA		−0.3		−1.5	−0.8		−4.0	−2.0		−10.0	−0.3		−2.0	V
BV_{GSS}	Gate-Source Breakdown Voltage	V_{DS} = 0, I_G = 1μA		−40			−40			−40			−25			
I_{DSS}	Saturation Drain Current (Note 2)	V_{DS} = 20V, V_{GS} = 0		0.2		1.0	0.9		4.5	4.0		20	0.2	1.2	3.0	mA
I_G	Gate Current (Note 1)	V_{DG} = 20V, I_D = 200μA			−3.5			−3.5			−3.5			−3.5		pA
g_{fs}	Common-Source Forward Transconductance (Note 2)	V_{DS} = 20V, V_{GS} = 0	f = 1kHz	500			1,000			1,500			500	1,500		μs
g_{os}	Common Source Output Conductance				1			3.5			10			2.5		
C_{iss}	Common-Source Input Capacitance		f = 1MHz (Note 3)		4			4			4			4		pF
C_{rss}	Common-Source Reverse Transfer Capacitance				1			1			1			1		
$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage	V_{DS} = 10V, V_{GS} = 0	f = 1kHz (Note 3)		5			5			5			10		$\frac{nV}{\sqrt{Hz}}$

NOTES: 1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 2ms.
3. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

J308–J310
N-Channel JFET
High Frequency Amplifier

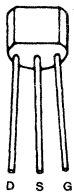
INTERSIL

FEATURES
- Industry Standard Part in Low Cost Plastic Package
- High Power Gain
- Low Noise
- Dynamic Range Greater Than 100dB
- Easily Matched to 75Ω Input

APPLICATIONS
- VHF/UHF Amplifiers
- Oscillators
- Mixers

PIN CONFIGURATION

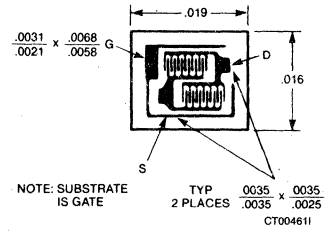
TO-92



PC00131I

CHIP TOPOGRAPHY

5021



CT00461I

ORDERING INFORMATION*

TO-92	WAFER	DICE
J30X	J30X/W	J30X/D

*When ordering wafer/dice refer to Section 10, page 10–1.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Drain-Gate Voltage ..... −25V
Drain-Source Voltage ..... −25V
Continuous Forward Gate Current ..... −10mA
Storage Temperature Range ..... −55°C to +150°C
Operating Temperature Range ..... −55°C to +135°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 360mW
Derate above 25°C ..... 3.27mW/°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

SYMBOL	PARAMETER	TEST CONDITIONS		J308			J309			J310			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1μA, V_{DS} = 0		−25			−25			−25			V
I_{GSS}	Gate Reverse Current	V_{GS} = −15V, V_{DS} = 0				−1.0			−1.0			−1.0	nA
	T_A = 125°C					−1.0			−1.0			−1.0	μA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 10V, I_D = 1nA		−1.0		−6.5	−1.0		−4.0	−2.0		−6.5	V
I_{DSS}	Saturation Drain Current (Note 1)	V_{DS} = 10V, V_{GS} = 0		12		60	12		30	24		60	mA
$V_{GS(f)}$	Gate-Source Forward Voltage	V_{DS} = 0, I_G = 1mA				1.0			1.0			1.0	V
g_{fs}	Common-Source Forward Transconductance	V_{DS} = 10V, I_D = 10mA, (Note 2)	f = 1kHz	8,000		20,000	10,000		20,000	8,000		18,000	μs
g_{os}	Common-Source Output Conductance					200			200			200	
g_{fg}	Common-Gate Forward Transconductance				13,000			13,000			12,000		
g_{og}	Common Gate Output Conductance				150			150			150		

Note: All typical values have been guaranteed by characterization and are not tested.

J308–J310

INTERSIL

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS		J308			J309			J310			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
C_{gd}	Gate-Drain Capacitance	V_{DS} = 10V,	f = 1MHz		1.8	2.5		1.8	2.5		1.8	2.5	pF
C_{gs}	Gate-Source Capacitance	V_{GS} = −10V	(Note 2)		4.3	5.0		4.3	5.0		4.3	5.0	
e_n	Equivalent Short-Circuit Input Noise Voltage	V_{DS} = 10V, I_D = 10mA	f = 100Hz (Note 2)		10			10			10		$\frac{nV}{\sqrt{Hz}}$
$Re_{(Vfs)}$	Common-Source Forward Transconductance	V_{DS} = 10V, I_D = 10mA (Note 2)	f = 105MHz		12			12			12		μs
$Re_{(Vfg)}$	Common-Gate Input Conductance				14			14			14		
$Re_{(Vis)}$	Common-Source Input Conductance				0.4			0.4			0.4		
$Re_{(Vos)}$	Common-Source Output Conductance				0.15			0.15			0.15		
G_{pg}	Common-Gate Power Gain at Noise Match				16			16			16		dB
NF	Noise Figure				1.5			1.5			1.5		
G_{pg}	Common-Gate Power Gain at Noise Match		f = 450MHz		11			11			11		
NF	Noise Figure				2.7			2.7			2.7		

NOTES: 1. Pulse test PW 300μs, duty cycle ≤ 3%.
2. For design reference only, not 100% tested.

2

Note: All typical values have been guaranteed by characterization and are not tested.

LM114/H, LM114A/AH
Dual NPN General Purpose Amplifier

GENERAL DESCRIPTION

These devices contain a pair of junction-isolated NPN transistors fabricated on a single silicon substrate. This monolithic structure makes possible extremely tight parameter matching at low cost. Further, advanced processing techniques yield exceptionally high current gains at low collector currents, virtual elimination of "popcorn noise," low leakages and improved long-term stability.

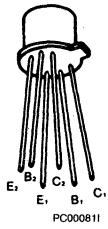
Although designed primarily for high breakdown voltage and exceptional DC characteristics, these transistors have surprisingly good high-frequency performance. The gain-bandwidth product is 300MHz with 1mA collector current and 5V collector-base voltage and 22MHz with 10μA collector current. Typical collector-base capacitance is only 1.6 pF at 5V.

FEATURES

- **Low Offset Voltage**
- **Low Drift**
- **High Current Gain**
- **Tight Beta Match**
- **High Breakdown Voltage**
- **Matching Guaranteed Over A 0V to 45V Collector-Base Voltage Range**
- **CMRR > 100dB**

PIN CONFIGURATION

TO-71
TO-78



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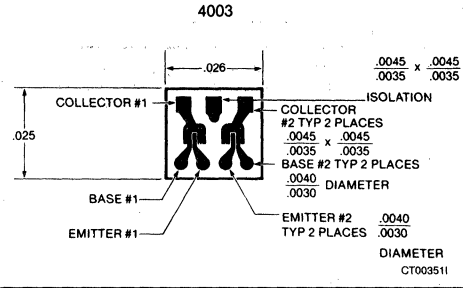
CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-71	TO-78	WAFER	DICE
LM114	LM114H	LM114/W	LM114/D
LM114A	LM114AH		

*When ordering wafer/dice refer to Section 10, page 10–1.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Collector-Base Voltage (1) 45V
Collector-Emitter Voltage (1) 45V
Collector-Collector Voltage 45V
Emitter-Base Voltage (1) 6V
Collector Current (1) 20mA
Storage Temperature Range ..... −65°C to +200°C
Operating Temperature Range ..... −55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation (T_C = 25°C) 800mW
Derate above 25°C ..... 14mW/°C

ELECTRICAL CHARACTERISTICS (NOTE 2)

SYMBOL	PARAMETER	TEST CONDITIONS	MAXIMUM LIMITS		UNIT
			LM114A, AH	LM114, H	
V_{BE1-2}	Offset Voltage	1μA ≤ I_C ≤ 100μA	0.5	2.0	mV
I_{B-2}	Offset Current	I_C = 10μA	2.0	10	nA
	Bias Current	I_C = 1μA	0.5		
		I_C = 10μA	20	40	nA
		I_C = 1μA	3.0		
$\Delta V_{BE}/V$	Offset Voltage Change	0V ≤ V_{CB} ≤ V_{MAX}, I_C = 10μA	0.2	1.5	mV
$\Delta V_{BE}/V$	Offset Current Change		1.0	4.0	nA

Note: All typical values have been guaranteed by characterization and are not tested.

LM114/H, LM114A/AH

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	MAXIMUM LIMITS		UNIT
			LM114A, AH	LM114, H	
$\Delta V_{BE}/\Delta T$	Offset Voltage Drift	$-55°C \le T_A \le +125°C$, $I_C = 10\mu A$	2.0	10	$\mu V/°C$
$\Delta I_{B1-2}/\Delta T$	Offset Current		12	50	
$\Delta I_B/\Delta T$	Bias Current		60	150	nA
I_{CBO}	Collector-Base Leakage Current	$V_{CB} = V_{MAX}$	10	50	pA
	$T_A = 125°C$ (Note 3)		10	50	nA
I_{CEO}	Collector-Emitter Leakage Current	$V_{CE} = V_{MAX}$, $V_{EB} = 0V$	50	200	pA
	$T_A = 125°C$ (Note 3)		50	200	nA
I_{C1-C2}	Collector-Collector Leakage Current	$V_{CC} = V_{MAX}$	100	300	pA
	$T_A = 125°C$ (Note 3)		100	300	nA

NOTES: 1: Per transistor.
2: These specifications apply for $T_A = +25°C$ and $0V \le V_{CB} \le V_{MAX}$, unless otherwise specified. For the LM114 and LM114A, $V_{MAX} = 30V$.
3. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

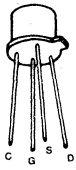
M116
Diode Protected N-Channel Enhancement Mode MOSFET General Purpose Amplifier

INTERSIL

FEATURES
- Log I_{GSS}
- Integrated Zener Clamp for Gate Protection

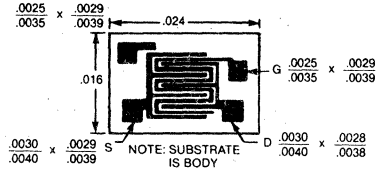
PIN CONFIGURATION

TO-72



PC00271I

CHIP TOPOGRAPHY



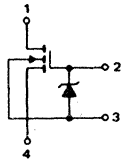
CT00451I

ORDERING INFORMATION*

TO-72	WAFER	DICE
M116	M116/W	M116/D

*When ordering wafer/dice refer to Section 10, page 10-1.

DEVICE SCHEMATIC



DS00041I

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Drain to Source Voltage	30V
Gate to Drain Voltage	30V
Drain Current	50mA
Gate Zener Current	±0.1mA
Storage Temperature Range	−65°C to +200°C
Operating Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	225mW
Derate above 25°C	2.2mW/°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted, V_{BS} = 0)

SYMBOL	PARAMETER	TEST CONDITIONS	M116 MIN	M116 MAX	UNIT
$r_{DS(on)}$	Drain Source ON Resistance	V_{GS} = 20V, I_D = 100μA, V_{BS} = 0		100	Ω
		V_{GS} = 10V, I_D = 100μA, V_{BS} = 0		200	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 10μA, V_{BS} = 0	1	5	V
BV_{DSS}	Drain-Source Breakdown Voltage	I_D = 1μA, V_{GS} = V_{BS} = 0	30		
BV_{SDS}	Source-Drain Breakdown Voltage	I_S = 1μA, V_{GD} = V_{BD} = 0	30		
BV_{GBS}	Gate-Body Breakdown Voltage	I_G = 10μA, V_{SB} = V_{DB} = 0	30	60	
$I_{D(OFF)}$	Drain Cutoff Current	V_{DS} = 20V, V_{GS} = V_{BS} = 0		10	nA
$I_{S(OFF)}$	Source Cutoff Current	V_{SD} = 20V, V_{GD} = V_{BD} = 0		10	
I_{GSS}	Gate-Body Leakage	V_{GS} = 20V, V_{DS} = V_{BS} = 0		100	pA
C_{gs}	Gate-Source (Note 1)	V_{GB} = V_{DB} = V_{SB} = 0, f = 1MHz		2.5	pF
C_{gd}	Gate-Drain Capacitance (Note 1)	Body Guarded		2.5	
C_{db}	Drain-Body Capacitance (Note 1)	V_{GB} = 0, V_{DB} = 10V, f = 1MHz		7	
C_{iss}	Input Capacitance (Note 1)	V_{GB} = 0, V_{DB} = 10V, V_{BS} = 0, f = 1MHz		10	

NOTE 1: For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

U200–U202
N-Channel JFET Switch

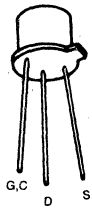
INTERSIL

FEATURES
- Low Insertion Loss
- Good OFF Isolation

APPLICATIONS
- Analog Switches
- Commutators
- Choppers

PIN CONFIGURATION

TO-18



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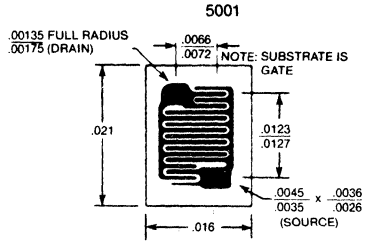
CHIP TOPOGRAPHY



CT000911

ORDERING INFORMATION*

TO-18	WAFER	DICE
U200	U200/W	U200/D
U201	U201/W	U201/D
U202	U202/W	U202/D

*When ordering wafer/dice refer to Section 10, page 10–1.

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage ..... −30V
Gate Current 50mA
Storage Temperature Range ..... −65°C to +200°C
Operating Temperature Range ..... −55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Total Device Dissipation (T_C = 25°C) 1.8W
Derate above 25°C ..... 10mW/°C

2

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		U200		U201		U202		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
I_{GSS}	Gate Reverse Current	V_{GSS} = 20V, V_{DS} = 0			−1		−1		−1	nA
	T_A = 150°C				−1		−1		−1	μA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1μA, V_{DS} = 0		−30		−30		−30		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 20V, I_D = 10nA		−0.5	−3	−1.5	−5	−3.5	−10	V
$I_{D(off)}$	Drain Cutoff Current	V_{DS} = 10V, V_{GS} = −12V			1		1		1	nA
	T_A = 150°C				1		1		1	μA
I_{DSS}	Saturation Drain Current (Note 1)	V_{DS} = 20V, V_{GS} = 0		3	25	15	75	30	150	mA
$r_{ds(on)}$	Drain-Source ON Resistance	V_{GS} = 0, I_D = 0	f = 1kHz		150		75		50	ohm
C_{iss}	Common-Source Input Capacitance (Note 2)	V_{DS} = 20V, V_{GS} = 0	f = 1MHz		30		30		30	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)	V_{DS} = 0, V_{GS} = −12V	f = 1MHz		8		8		8	pF

NOTES: 1: Pulse test required, pulsewidth = 300μs, duty cycle ≤ 3%.
2. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

U231-U235
Dual N-Channel JFET General Purpose Amplifier

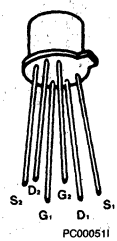
INTERSIL

FEATURES
- Good Matching Characteristics

APPLICATIONS
- Differential Amplifiers
- Low and Medium Frequency Amplifiers

PIN CONFIGURATION

TO-71



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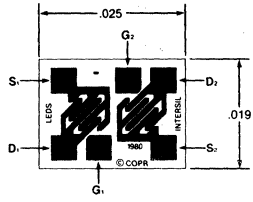
CHIP TOPOGRAPHY

6037



ALL BOND PADS ARE 4 x 4 MIL.

CT00481I

ORDERING INFORMATION*

TO-71	WAFER	DICE
U23X	U23X/W	U23X/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage (Note 1) ..... -50V
Gate Current (Note 1) 50mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +200°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 300mW
Derate above 25°C ..... 1.7mW/°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS MIN	LIMITS MAX	UNIT
I_{GSS}	Gate Reverse Current	V_{GS} = -30V, V_{DS} = 0			-100	pA
	T_A = 150°C				-500	nA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = 1μA, V_{DS} = 0		-50		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 20V, I_D = 1nA		-0.5	-4.5	
V_{GS}	Gate-Source Voltage			-0.3	-4.0	
I_G	Gate Operating Current	V_{DG} = 20V, I_D = 200μA			-50	pA
	T_A = 125°C				-250	nA
I_{DSS}	Saturation Drain Current (Note 2)	V_{DS} = 20V, V_{GS} = 0		0.5	5.0	mA
g_{fs}	Common-Source Forward Transconductance (Note 1)	V_{DS} = 20V, V_{GS} = 0	f = 1kHz	1000	3000	μs
			f = 100MHz (Note 4)	1000		
g_{fs}	Common-Source Forward Transconductance (Note 1)	V_{DG} = 20V, I_D = 200μA	f = 1kHz	600	1600	
g_{os}	Common-Source Output Capacitance	V_{DS}=20V, V_{GS} = 0			35	
g_{os}	Common-Source Output Conductance	V_{DG} = 20V, I_D = 200μA			10	
C_{iss}	Common-Source Input Capacitance	V_{DS} = 20V, V_{GS} = 0 (Note 4)	f = 1MHz		6	pF
C_{rss}	Common-Source Reverse Transfer Capacitance				2	
$\overline{e_n}$	Equivalent Short Circuit Input Noise Voltage		f = 100Hz		80	$\frac{nV}{\sqrt{Hz}}$

Note: All typical values have been guaranteed by characterization and are not tested.

U231-U235

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	MATCHING CHARACTERISTICS	TEST CONDITIONS		U231 MAX	U232 MAX	U233 MAX	U234 MAX	U235 MAX	UNIT
$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Current (Note 4)	V_{DG} = 20V, I_D = 200μA	125°C	10	10	10	10	10	nA
$\frac{(I_{DSS1} - I_{DSS2})}{I_{DSS1}}$	Saturation Drain Current Match (Note 2, 4)	V_{DS} = 20V, V_{GS} = 0		5	5	5	10	15	%
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage	V_{DG} = 20V, I_D = 200μA	T_A = 25°C	5	10	15	20	25	mV
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 3)		T_A = 25°C T_B = 125°C	10	25	50	75	100	μV/°C
			T_A = −55°C T_B = 25°C	10	25	50	75	100	
$\frac{(g_{fs1} - g_{fs2})}{g_{fs1}}$	Transconductance Match (Note 2)		f = 1kHz	3	5	5	10	15	%
$\lvert g_{os1} - g_{os2} \rvert$	Differential Output Conductance			5	5	5	5	5	μs

NOTES: 1. Per transistor.
2. Pulse test required, pulse width = 300μs, duty cycle ≤ 3%.
3. Measured at end points, T_A and T_B
4. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

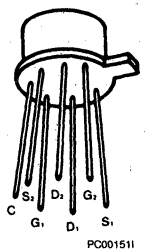
U257
Dual N-Channel JFET High Frequency Amplifier

INTERSIL

FEATURES
- g_{fs} > 5000μs From DC to 100MHz
- Matched V_{GS}, g_{fs} and g_{os}

PIN CONFIGURATION

TO-99



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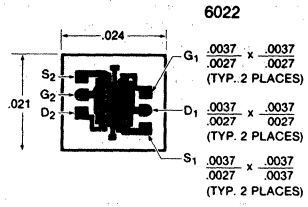


CT005611

ORDERING INFORMATION*

TO-99	WAFER	DICE
U257	U257/W	U257/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage (Note 1) ..... -25V
Gate Current (Note 1) 50mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C

	ONE SIDE	BOTH SIDES
Power Dissipation (T_A = 85°C)	250mW	500mW
Derate above 25°C	3.8mW/°C	7.7mW/°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
I_{GSSR}	Gate Reverse Current	V_{GS} = 15V, V_{DS} = 0			-100	pA
	T_A = 150°C				-250	nA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = -1μA, V_{DS} = 0		-25		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 10V, I_D = 1nA		-1	-5	V
I_{DSS}	Saturation Drain Current (Note 2)	V_{DS} = 10V, V_{GS} = 0		5	40	mA
g_{fs}	Common-Source Forward Transconductance	V_{DS} = 10V, I_D = 5mA	f = 1kHz	5000	10,000	μs
g_{fs}	Common-Source Forward Transconductance	V_{DG} = 10V, I_D = 5mA	f = 100MHz (Note 3)	5000	10,000	μs
g_{os}	Common-Source Output Conductance	V_{DS} = 10V, I_D = 5mA	f = 1kHz		150	μs
g_{oss}	Common-Source Output Conductance	V_{DG} = 10V, I_D = 5mA	f = 100MHz		150	μs
C_{iss}	Common-Source Input Capacitance	V_{DG} = 10V, I_D = 5mA	f = 1MHz		5	pF
C_{rss}	Common-Source Reverse Transfer Capacitance	V_{DG} = 10V, I_D = 5mA	f = 1MHz		1.2	pF
$\overline{e_n}$	Equivalent Input Noise Voltage	(Note 3)	f = 10kHz		30	$\frac{nV}{\sqrt{Hz}}$
$\frac{I_{DSS1}}{I_{DSS2}}$	Drain Current Ratio at Zero Gate Voltage (Note 2)	V_{DS} = 10V, V_{GS} = 0		0.85	1	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage	V_{DG} = 10V, I_D = 5mA			100	mV
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	V_{DG} = 10V, I_D = 5mA		0.85	1	
$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance	V_{DG} = 10V, I_D = 5mA	f = 1kHz		20	μs

NOTES: 1. Per transistor.
2. Pulse test required, pulse width = 300μs, duty cycle ≤ 3%.
3. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

U304–U306
P-Channel JFET Switch

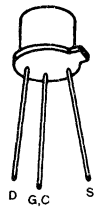
INTERSIL

FEATURES
- Low ON Resistance
- $I_{D(off)} < 500pA$
- Switches directly from TTL Logic (U306)

APPLICATIONS
- Analog Switches
- Commutators
- Choppers

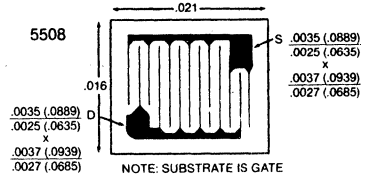
PIN CONFIGURATION

TO-18



PC000111

CHIP TOPOGRAPHY



CT004911

ORDERING INFORMATION*

TO-18	WAFER	DICE
U304	U304/W	U304/D
U305	U305/W	U305/D
U306	U306/W	U306/D

*When ordering wafer/dice refer to Section 10, page 10–1.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage (Note 1) 30V
Gate Current 50mA
Storage Temperature Range ..... −65°C to +200°C
Operating Temperature Range ..... −55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Power Dissipation 350mW
Derate above 25°C ..... 2.8mW/°C

2

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS		U304 MIN	U304 MAX	U305 MIN	U305 MAX	U306 MIN	U306 MAX	UNIT
I_{GSSR}	Gate Reverse Current	V_{GS} = 20V, V_{DS} = 0			500		500		500	pA
	T_A = 150°C				1.0		1.0		1.0	μA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = 1μA, V_{DS} = 0		30		30		30		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = −15V, I_D = −1μA		5	10	3	6	1	4	V
$V_{DS(on)}$	Drain-Source ON Voltage	V_{GS} = 0, I_D = −15mA (U304), I_D = −7mA (U305), I_D = −3mA (U306)			−1.3		−0.8		−0.6	V
I_{DSS}	Saturation Drain Current (Note 1)	V_{DS} = −15V, V_{GS} = 0		−30	−90	−15	−60	−5	−25	mA
$I_{D(off)}$	Drain Cutoff Current	V_{DS} = −15V, V_{GS} = 12V (U304) V_{GS} = 7V (U305) V_{GS} = 5V (U306)			−500		−500		−500	pA
	T_A = 150°C				−1.0		−1.0		−1.0	μA
$r_{DS(on)}$	Static Drain-Source ON Resistance	V_{GS} = 0V, I_D = −1mA			85		110		175	Ω
$r_{ds(on)}$	Drain-Source ON Resistance	V_{GS} = 0V, I_D = 0	f = 1kHz		85		110		175	Ω
C_{iss}	Common-Source Input Capacitance (Note 2)	V_{DS} = −15V, V_{GS} = 0	f = 1MHz		27		27		27	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)	V_{DS} = 0, V_{GS} = 12V (U304) V_{GS} = 7V (U305), V_{GS} = 5V (U306)	f = 1MHz		7		7		7	pF

Note: All typical values have been guaranteed by characterization and are not tested.

U304-U306

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS				U304		U305		U306		UNIT
						MIN	MAX	MIN	MAX	MIN	MAX	
			U304	U305	U306							
$t_{d(on)}$	Turn-ON Delay Time (Note 2)	V_{DD}	−10V	−6V	−6V		20		25		25	
t_r	Rise Time (Note 2)	$V_{GS(off)}$	12V	7V	5V		15		25		35	ns
$t_{d(off)}$	Turn-OFF Delay Time (Note 2)	R_L	580Ω	743Ω	1800Ω		10		15		20	
t_f	Fall Time (Note 2)	$V_{GS(on)}$	0	0	0		25		40		60	
		$I_{D(on)}$	−15mA	−7mA	−3mA							

NOTES: 1. Pulse test pulsewidth = 300μs, duty cycle ≤ 3%.
2. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

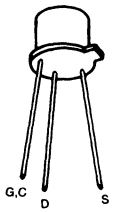
U308–U310
N-Channel JFET
High Frequency Amplifier

INTERSIL

FEATURES
- High Power Gain
- Low Noise
- Dynamic Range Greater Than 100dB
- Easily Matched to 75Ω Input

PIN CONFIGURATIONS

TO-52



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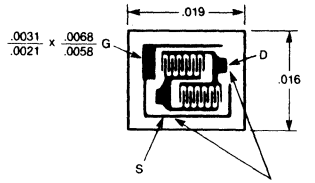

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ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage ..... −25V
Gate Current 20mA
Storage Temperature ..... −65°C to +200°C
Operating Temperature Range ..... −55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 500mW
Derate above 25°C ..... 4mW/°C

ORDERING INFORMATION*

TO-52	WAFER	DICE
U308	U308/W	U308/D
U309	U309/W	U309/D
U310	U310/W	U310/D

*When ordering wafer/dice refer to Section 10, page 10–1.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		U308			U309			U310			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{GSS}	Gate Reverse Current	V_{GS} = −15V				−150			−150			−150	pA
	T_A = 125°C	V_{GS} = 0				−150			−150			−150	nA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1μA, V_{DS} = 0		−25			−25			−25			V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 10V, I_D = 1nA		−1.0		−6.0	−1.0		−4.0	−2.5		−6.0	
I_{DSS}	Saturation Drain Current (Note 1)	V_{DS} = 10V, V_{GS} = 0		12		60	12		30	24		60	mA
$V_{GS(f)}$	Gate-Source Forward Voltage	I_G = 10mA, V_{DS} = 0				1.0			1.0			1.0	V
g_{fg}	Common-Gate Forward Transconductance (Note 1)	V_{DS} = 10V, I_D = 10mA	f = 1kHz	10	17		10	17		10	17		μs
g_{ogs}	Common Gate Output Conductance					250			250			250	μs
C_{gd}	Drain-Gate Capacitance	V_{GS} = −10V,	f = 1MHz (Note 2)			2.5			2.5			2.5	pF
C_{gs}	Gate-Source Capacitance	V_{DS} = 10V				5.0			5.0			5.0	
$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage	V_{DS} = 10V, I_D = 10mA	f = 100Hz (Note 2)		10			10			10		$\frac{nV}{\sqrt{Hz}}$

Note: All typical values have been guaranteed by characterization and are not tested.

U308-U310

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS		U308			U309			U310			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
g_{fg}	Common-Gate Forward Transconductance	V_{DS} = 10V, I_D = 10mA (Note 2)	f = 100MHz		15			15			15		μs
			f = 450MHz		14			14			14		
g_{ogs}	Common-Gate Output Conductance		f = 100MHz		0.18			0.18			0.18		
			f = 450MHz		0.32			0.32			0.32		
G_{pg}	Common-Gate Power Gain		f = 100MHz	14	16		14	16		14	16		dB
			f = 450MHz	10	11		10	11		10	11		
NF	Noise Figure		f = 100MHz		1.5	2.0		1.5	2.0		1.5	2.0	
			f = 450MHz		2.7	3.5		2.7	3.5		2.7	3.5	

NOTES: 1. Pulse test duration = 2ms.
2. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

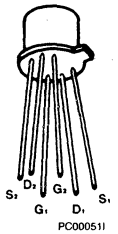
U401-U406
Dual N-Channel JFET Switch

INTERSIL

FEATURES
- **Minimum System Error and Calibration**
- **Low Drift With Temperature**
- **Operates From Low Power Supply Voltages**
- **High Output Impedance**

PIN CONFIGURATION

TO-71



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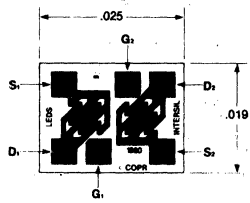


ALL BOND PADS ARE 4 x 4 MIL.

CT000711

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage 50V
Gate Current (Note 1) 10mA
Storage Temperature Range ..... −65°C to +200°C
Operating Temperature Range ..... −55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C

	ONE SIDE	BOTH SIDES
Power Dissipation (T_A = 85°C)	300mW	500mW
Derate above 25°C.....	2.6mW/°C	5mW/°C

ORDERING INFORMATION*

TO-71	WAFER	DICE
U40X	U40X/W	U40X/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS		U401		U402		U403		U404		U405		U406		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
BV_{GSS}	Gate-Source Breakdown Voltage	V_{DS} = 0, I_G = −1μA		−50		−50		−50		−50		−50		−50		V
I_{GSS}	Gate Reverse Current (Note 2)	V_{DS} = 0, V_{GS} = −30V			−25		−25		−25		−25		−25		−25	pA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 15V, I_D = 1nA		−.5	−2.5	−.5	−2.5	−.5	−2.5	−.5	−2.5	−.5	−2.5	−.5	−2.5	V
$V_{GS(on)}$	Gate-Source Voltage (on)	V_{DG} = 15V, I_D = 200μA			−2.3		−2.3		−2.3		−2.3		−2.3		−2.3	
I_{DSS}	Saturation Drain Current (Note 3)	V_{DS} = 10V, V_{GS} = 0		0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	mA
I_G	Operating Gate Current	V_{DG} = 15V, I_D = 200μA			−15		−15		−15		−15		−15		−15	pA
	(Note 2) T_A = 125°C				−10		−10		−10		−10		−10		−10	nA
BV_{G1-G2}	Gate-Gate Breakdown Voltage	V_{DS} = 0, V_{GS} = 0, I_G = ±1μA		±50		±50		±50		±50		±50		±50		V
g_{fs}	Common-Source Forward Transconductance (Note 3)	V_{DS} = 10V, V_{GS} = 0	f = 1kHz	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	μs
g_{os}	Common-Source Output Conductance				20		20		20		20		20		20	
g_{fs}	Common-Source Forward Transconductance	V_{DG} = 15V, I_D = 200μA	f = 1kHz	1000	1600	1000	1600	1000	1600	1000	1600	1000	1600	1000	1600	
g_{os}	Common-Source Output Conductance				2.0		2.0		2.0		2.0		2.0		2.0	
C_{iss}	Common-Source Input Capacitance (Note 6)		f = 1MHz		8.0		8.0		8.0		8.0		8.0		8.0	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 6)				3.0		3.0		3.0		3.0		3.0		3.0	

Note: All typical values have been guaranteed by characterization and are not tested.

U401-U406

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS		U401		U402		U403		U404		U405		U406		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
e_n	Equivalent Short-Circuit Input Noise Voltage	V_{DS} = 15V, V_{GS} = 0	f = 10Hz (Note 6)		20		20		20		20		20		20	$\frac{nV}{\sqrt{Hz}}$
CMRR	Common-Mode Rejection Ratio	V_{DG} = 10 to 20V, I_D = 200μA (Note 5, 6)		95		95		95		95		90				dB
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage	V_{DG} = 10V, I_D = 200μA			5		10		10		15		20		40	mV
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 4)	V_{DG} = 10V, I_D = 200μA	T_A = −55°C, T_B = +25°C, T_C = +125°C		10		10		25		25		40		80	μV/°C

NOTES: 1. Per transistor.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 300μs; duty cycle ≤ 3%.
4. Measured at end points, T_A, T_B, T_C.
5. $\text{CMRR} = 20 \log_{10} \left[\frac{\Delta V_{DD}}{\Delta \lvert V_{GS1} - V_{GS2} \rvert} \right]$, ΔV_{DD} = 10V.
6. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

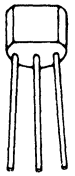
U1897-U1899
N-Channel JFET Switch

FEATURES
- Low Insertion Loss
- No Error or Offset Voltage Generated By Closed Switch

APPLICATIONS
- Analog Switches, Choppers

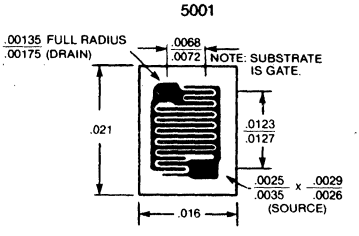
PIN CONFIGURATION

TO-92



PC001311

CHIP TOPOGRAPHY



CT00511I

ORDERING INFORMATION*

TO-92	TO-92-18	WAFER	DICE
U1897	U1897-18	U1897/W	U1897/D
U1898	U1898-18	U1898/W	U1898/D
U1899	U1899-18	U1899/W	U1899/D

*When ordering wafer/dice refer to Section 10, page 10-1.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage ..... -40V
Forward Gate Current 10mA
Storage Temperature Range ..... -55°C to +150°C
Operating Temperature Range ..... -55°C to +135°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 350mW
Derate above 25°C ..... 3.2mW/°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

SYMBOL	PARAMETER	TEST CONDITIONS		U1897		U1898		U1899		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = -1μA, V_{DS} = 0		-40		-40		-40		V
I_{GSS}	Gate Reverse Current	V_{GS} = -20V, V_{DS} = 0			-400		-400		-400	pA
I_{DGO}	Drain-Gate Leakage Current	V_{DG} = 20V, I_S = 0			200		200		200	
I_{SGO}	Source-Gate Leakage Current	V_{SG} = 20V, I_D = 0			200		200		200	
$I_{D(off)}$	Drain Cutoff Current	V_{DS} = 20V, V_{GS} = -12V (U1897)			200		200		200	
	T_A = 85°C	V_{GS} = -8V (U1898) V_{GS} = -6V (U1899)			10		10		10	nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 20V, I_D = 1nA		-5.0	-10	-2.0	-7.0-	-1.0	-5.0	V
I_{DSS}	Saturation Drain Current (Note 1)	V_{DS} = 20V, V_{GS} = 0		30		15		8.0		mA
$V_{DS(on)}$	Drain-Source ON Voltage	V_{GS} = 0, I_D = 6.6mA (U1897) I_D = 4.0mA (U1898) I_D = 2.5mA (U1899)			0.2		0.2		0.2	V
$r_{DS(on)}$	Static Drain-Source ON Resistance	I_D = 1mA, V_{GS} = 0			30		50		80	Ω
C_{dg}	Drain-Gate Capacitance	V_{DG} = 20V, I_S = 0	f = 1MHz		5		5		5	pF
C_{sg}	Source-Gate Capacitance	V_{SG} = 20V, I_D = 0			5		5		5	
C_{iss}	Common-Source Input Capacitance	V_{DS} = 20V, V_{GS} = 0			16		16		16	
C_{rss}	Common-Source Reverse Transfer Capacitance		(Note 2)		3.5		3.5		3.5	

Note: All typical values have been guaranteed by characterization and are not tested.

U1897-U1899

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	U1897		U1898		U1899		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{d(on)}$	Turn ON Delay Time (Note 2)	Switching Time Test Conditions		15		15		20	ns
t_r	Rise Time (Note 2)	U1897 U1898 U1899		10		20		40	
t_{off}	Turn OFF Time (Note 2)	V_{DD} 3V 3V 3V $V_{GS(on)}$ 0 0 0 $V_{GS(off)}$ −12V −8V −6V R_L 425Ω 770Ω 1120Ω $I_{D(on)}$ 6.6mA 4mA 2.5mA		40		60		80	

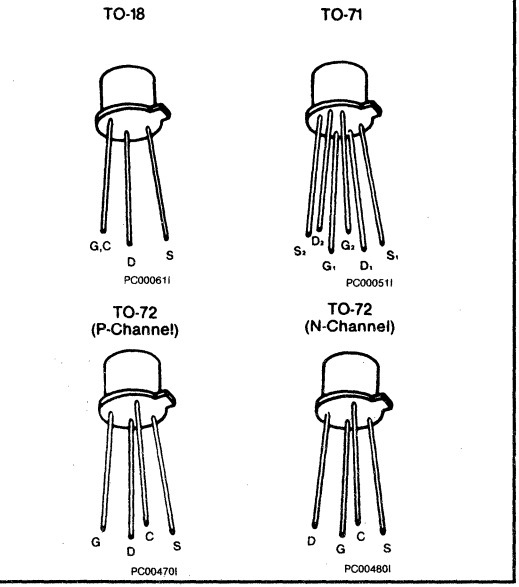
NOTES: 1. Pulse test pulsewidth = 300μs; duty cycle < 3%.
2. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

VCR2N/3P/4N/7N
Voltage Controlled Resistors

APPLICATIONS
- Small Signal Attenuators
- Filters
- Amplifier Gain Control
- Oscillator Amplitude Control

PIN CONFIGURATIONS



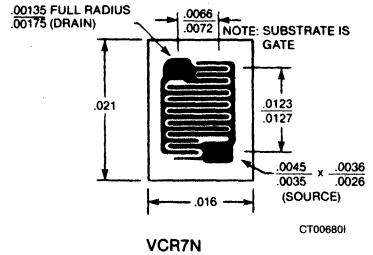
ORDERING INFORMATION*

TO-18	TO-72	WAFER	DICE
VCR2N	—	VCR2N/W	VCR2N/D
VCR4N	—	VCR4N/W	VCR4N/D
—	VCR3P	VCR3P/W	VCR3P/D
—	VCR7N	VCR7N/W	VCR7N/D

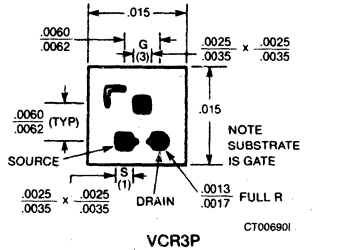
*When ordering wafer/dice refer to Section 10, page 10–1.

CHIP TOPOGRAPHY

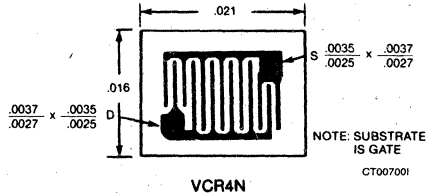
VCR2N
5001



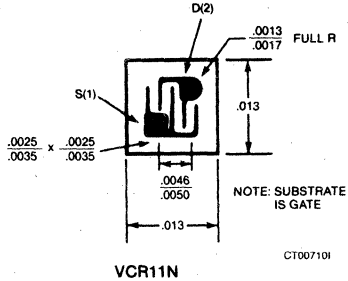
VCR7N
5007



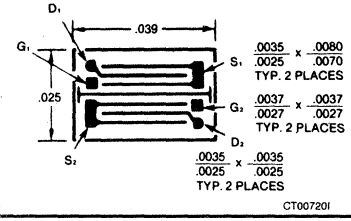
VCR3P
5508



VCR4N
5010 (4N)



VCR11N
6019



Note: All typical values have been guaranteed by characterization and are not tested.

VCR2N/3P/4N/7N

INTERSIL

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage 15V
Gate Current 10mA
Storage Temperature Range ..... −65°C to +200°C
Operating Temperature Range ..... −55°C to +175°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 300mW
Derate above 25°C ..... 2mW/°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

N Channel VCR FETs

SYMBOL	PARAMETER	TEST CONDITIONS		VCR2N		VCR4N		VCR7N		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
STATIC										
I_{GSS}	Gate Reverse Current	V_{GS} = −15V, V_{DS} = 0			−5		−0.2		−0.1	nA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1μA, V_{DS} = 0		−15		−15		−15		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	I_D = 1μA, V_{DS} = 10V		−3.5	−7	−3.5	−7	−2.5	−5	
$r_{ds(on)}$	Drain source ON Resistance	V_{GS} = 0, I_D = 0	f = 1kHz	20	60	200	600	4,000	8,000	Ω
DYNAMIC (Note 1)										
C_{dgo}	Drain-Gate Capacitance	V_{GD} = −10V, I_S = 0	f = 1MHz		7.5		3		1.5	pF
C_{sgo}	Source-Gate Capacitance	V_{GS} = −10V, I_D = 0			7.5		3		1.5	

NOTE 1: For design reference only, not 100% tested.

P Channel VCR FETS

SYMBOL	PARAMETER	TEST CONDITIONS		VCR3P		UNIT
				MIN	MAX	
STATIC						
I_{GSS}	Gate Reverse Current	V_{GS} = 15V, V_{DS} = 0			20	nA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = 1μA, V_{DS} = 0		15		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	I_D = −1μA, V_{DS} = −10V		3.5	7	
$r_{ds(on)}$	Drain-Source ON Resistance	V_{GS} = 0, I_D = 0	f = 1kHz	70	200	Ω
DYNAMIC (Note 1)						
C_{dgo}	Drain-Gate Capacitance	V_{GD} = 10V, I_S = 0	f = 1MHz		6	pF
C_{sgo}	Source-Gate Capacitance	V_{GS} = 10V, I_D = 0	(Note 1)		6	

NOTE 1: For design reference only, not 100% tested.

JFETS AS VOLTAGE REGULATORS

The voltage controlled resistor is a junction field effect transistor whose drain to source ON resistance is controlled by gate to source voltage.

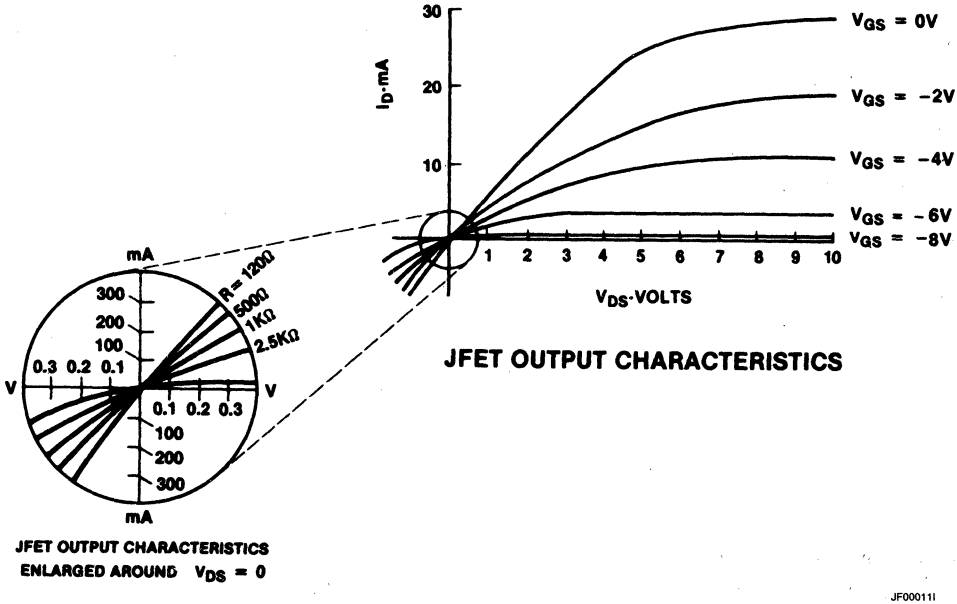
The gate control terminal is high impedance thereby allowing negligible control current. The gate voltage is zero for minimum resistance, and increases as the gate voltage approaches the pinch-off voltage.

This VCR is intended for use on applications using low level AC signals. Figure 1 shows the output characteristics, with an enlarged graph of VDS = 0 for AC signals with no DC component. Operation is in the first and third quadrants; the device will operate in the first quadrant only if a constant current is applied to the drain and the input signal level is kept low.

Figure 1 also shows that certain combinations of gate control voltage and signal levels will cause resistance modulation. This distortion may be improved by introducing local feedback as shown in figure 2 for best frequency response and impedance levels; eliminating the feedback capacitor will require the gate control voltage to be double for the same ON resistance. The resistor values should be equal, and about 100Ω.

Best gate control voltage for best linearity is up to about $0.8V_{PK}$; ON resistance increases rapidly beyond this point.

Note: All typical values have been guaranteed by characterization and are not tested.



JFET OUTPUT CHARACTERISTICS

Figure 1

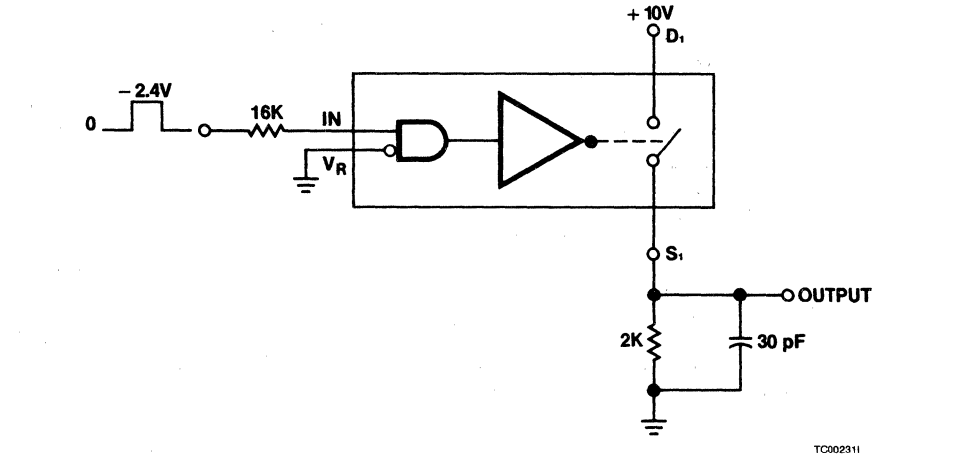


Figure 2

Note: All typical values have been guaranteed by characterization and are not tested.

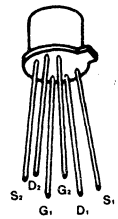
VCR11N
Voltage Controlled Resistors

INTERSIL

APPLICATIONS
- Small Signal Attenuators
- Filters
- Amplifier Gain Control
- Oscillator Amplitude Control

PIN CONFIGURATION

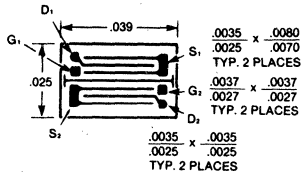
TO-71



PC000511

CHIP TOPOGRAPHY

6019



CT00261I

ORDERING INFORMATION*

TO-71	WAFER	DICE
VCR11N	VCR11N/W	VCR11N/D

*When ordering wafer/dice refer to Section 10, page 10–1.

ABSOLUTE MAXIMUM RATINGS
(= 25°C)

Gate-Drain or Gate-Source Voltage 25V
Gate Current 10mA
Total Device Dissipation at T_A = 25°C
(Derate at 2.0mW/°C to 175°C) 300mW
Storage Temperature Range ..... −55°C to +175°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	CHARACTERISTIC	TEST CONDITIONS		VCR11N MIN	VCR11N MAX	UNIT
I_{GSS}	Gate Reverse Current	V_{GS} = −15V, V_{DS} = 0			−0.2	nA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1μA, V_{DS} = 0		−25		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	I_D = 1μA, V_{DS} = 10V		−8	−12	V
$r_{ds(on)}$	Drain Source ON Resistance	V_{GS} = 0, I_D = 0	f = 1kHz	100	200	Ω
C_{dgo}	Drain-Gate Capacitance (Note 2)	V_{GD} = −10V, I_S = 0	f = 1MHz		8	pF
C_{sgo}	Source-Gate Capacitance (Note 2)	V_{GS} = −10V, I_D = 0	f = 1MHz		8	pF
$\frac{r_{DS}min}{r_{DS}max}$		V_{DS} = 100mV	r_{DS1} = 200μ	.95	1	Ω
		$V_{GS1} = V_{GS2}$	r_{DS1} = 2kμ	.95	1	Ω

NOTES: 1. V_{GS1} + Control Voltage necessary to force r_{DS} to 200Ω or 2kΩ.
2. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

Section 3 — Analog Switches and Multiplexers

D123/D125
SPST 6-Channel JFET Switch Driver

GENERAL DESCRIPTION

The D123 and D125 monolithic bipolar drivers convert low-level positive logic signals (0 & +5V) to the high level positive and negative voltages necessary to drive FET switches. One lead can be used to provide an enabling capability.

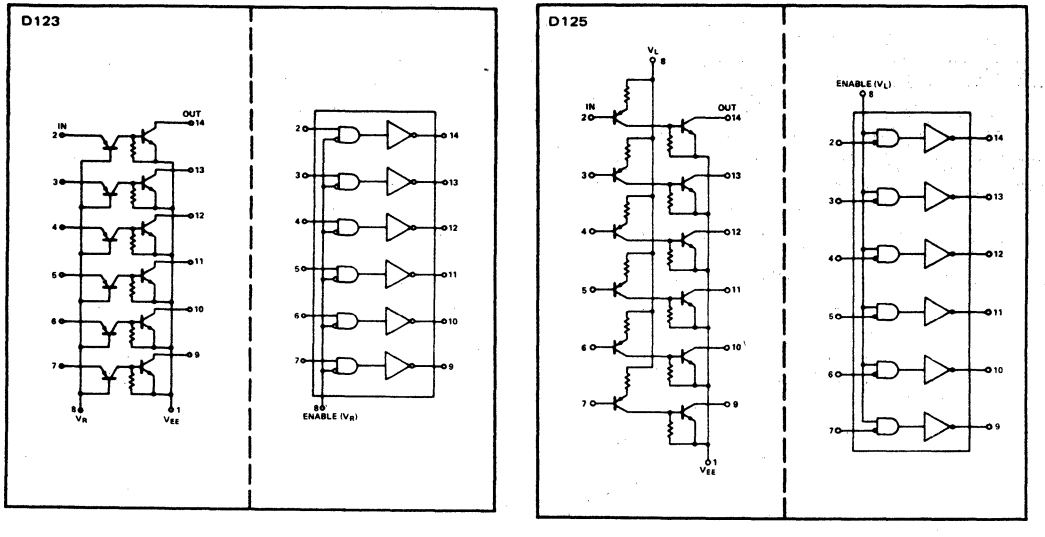
FEATURES

- **Provides DC Level Shifting Between Low-Level Logic and MOSFET or JFET Switches**
- **External Collector Pull-Ups Required**
- **Direct Interface With G116, G117, G119, G115, and G123 MOSFET Switches**

ORDERING INFORMATION

DG123 A K

- Package
  - K – 14-pin CERDIP
  - L – 14-pin Flat Package
  - P – 14-pin Hermetic DIP (Special Order Only)
- Temperature Range
  - A – Military (–55°C to +125°C)
  - B – Industrial (–20°C to +85°C)
- Device Chip Type



LD00040I LD00050I

Figure 1: Functional Diagram (Outline Dwgs DD, FD-2, JD)

3

Note: All typical values have been guaranteed by characterization and are not tested.

D123/D125

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Input-to-Emitter Voltage ($V_{IN} - V_{EE}$) 33V
Output-to-Emitter Voltage ($V_O - V_{EE}$) 33V
Logic Supply-to-Emitter Voltage ($V_L - V_{EE}$) 27V
Input-to-Reference Voltage ($V_{IN} - V_R$) 2V
Input-to-Logic Supply Voltage ($V_{IN} - V_L$) ..... +6V
Reference-to-Emitter Voltage ($V_R - V_{EE}$) 31V

Maximum Dissipation (Note) 750mW
Current (any pin) 30mA
Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature of 70°C. Derate 10mW/°C for higher ambient temperature.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

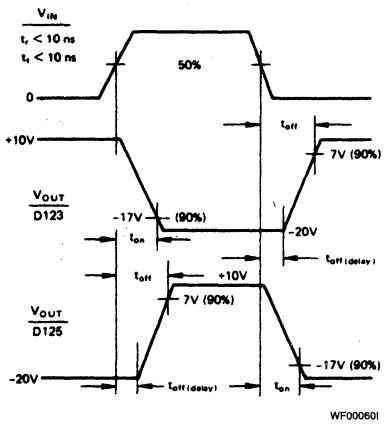
ELECTRICAL CHARACTERISTICS

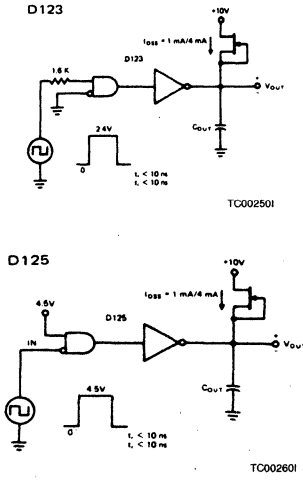
Test conditions unless otherwise specified are as follows: $V_{EE} = -20V$, $V_L = 4.5V$, $I_{OUT} = 0$, $V_R = 0$. Output and power supply measurements based on specified input conditions.

DEVICE NO.	PARAMETER	TEST CONDITIONS	MAX LIMIT			UNIT
			-55°C	25°C	125°C	
INPUT						
D123	$I_{IN(OFF)}$	$V_{IN} = 0.4V$	1	1	100	µA
	$V_{IN(ON)}$	$I_{IN} = 1mA$	1.3	1	0.8	V
D125	$I_{IN(OFF)}$	$V_{IN} = 4.1V$	1	1	20	µA
	$I_{IN(ON)}$	$V_{IN} = 0.5V$	-0.7	-0.7	-0.7	mA
OUTPUT						
D125 & D123	$I_{OUT(OFF)}$	$V_{OUT} = +10V$	0.1	0.1	10	µA
	$V_{OUT(ON)}$	$I_{OUT} = 1mA$	-19.7	-19.7	-19.5	V
	$V_{OUT(ON)}$	$I_{OUT} = 4mA$	-19.2	-19.2	-19.0	V
POWER SUPPLY						
D123	$I_{R(ON)}$(1)	$I_{OUT} = 0$ for ON measurements. $V_{OUT} = +10V$ for OFF measurements.	0.5	0.5	0.5	mA
	$I_{R(OFF)}$(2)		1	1	150	µA
	$I_{EE(ON)}$(1)		1	1	1	mA
	$I_{EE(OFF)}$(2)		2	2	200	µA
D125	$I_{L(ON)}$(1)		2	2	1.9	mA
	$I_{L(OFF)}$(1)		1	1	100	µA
	$I_{EE(ON)}$(1)		2	2	1.9	mA
	$I_{EE(OFF)}$(2)		2	2	200	µA
SWITCHING TIMES						
D125 & D123	$t_{(ON)}$	$I_{OUT} = 1mA$, C_{OUT}(3) = 10pF (See Switching Times) (4)		250		ns
	$t_{(OFF)}$(4)			800		ns
	$t_{(on)}$	$I_{OUT} = 4mA$, C_{OUT}(3) = 10pF (See Switching Times)		250		ns
	$t_{(off)}$(5)			600		ns

NOTES: 1. One channel ON, 5 channels OFF.
2. All channels OFF.
3. Add 30ns per pF for 1mA and add 8ns per pF for 4mA for additional capacitive loading.
4. For Dual-In-Line package add 120ns to $t_{(off)}$.
5. For Dual-In-Line package add 30ns to $t_{(off)}$.

Note: All typical values have been guaranteed by characterization and are not tested.



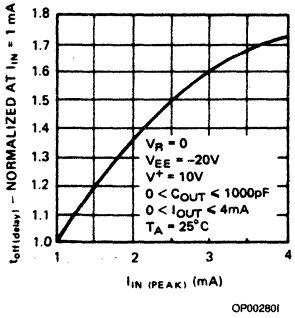


Circuit Diagrams

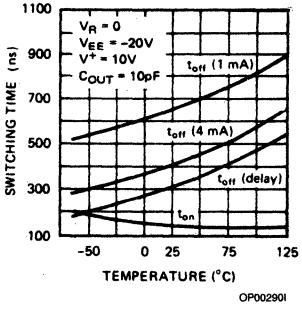
Figure 2: Switching Times

TYPICAL PERFORMANCE CHARACTERISTICS

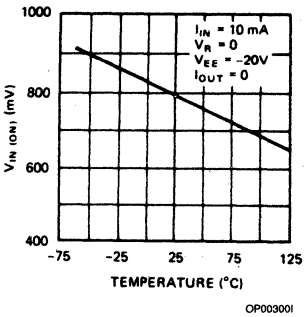
$t_{off(delay)}$ VS $I_{IN(PEAK)}$ D123



SWITCHING TIMES VS TEMPERATURE D123 AND D125 (SEE NOTES 4 AND 5)



$V_{IN(ON)}$ VS TEMPERATURE D123

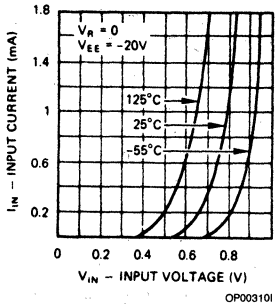


Note: All typical values have been guaranteed by characterization and are not tested.

D123/D125

TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

I_{IN} VS V_{IN} D123



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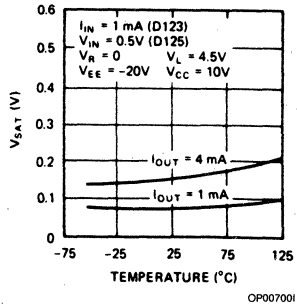
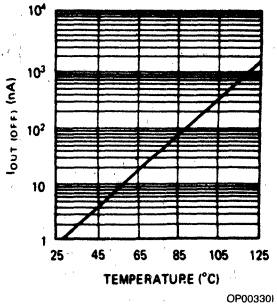
V_{SAT} VS TEMPERATURE D123 AND D125



OP00700I

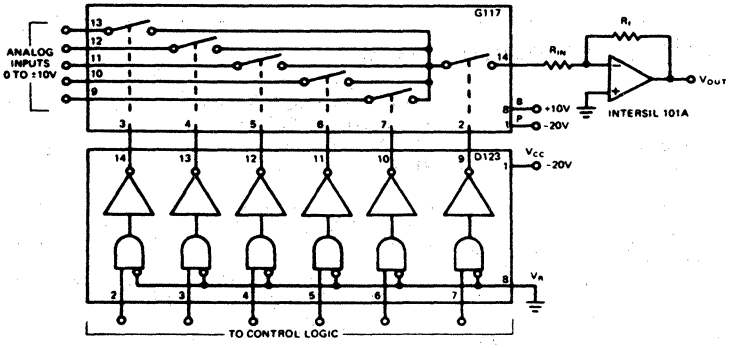
$I_{OUT(OFF)}$ VS TEMPERATURE D123 AND D125



OP00330I

APPLICATIONS

Using INTERSIL'S MOSFET SWITCH, G117, with either the D123 or D125 drivers provides a convenient means of designing a 5 channel analog multiplexer with a series on/off switch.



AF00050I

Figure 3: 5-Channel Multiplexer

Note: All typical values have been guaranteed by characterization and are not tested.

D123/D125

APPLICATION TIPS

Interfacing the D123 and D125

In order to meet all the specifications on this data sheet, certain requirements must be met by the drive circuitry.

The D125 can be turned ON easily, but care must be exercised to insure turn-off. Keeping $V_L - V_{IN} \leq 0.4V$ is a must to insure turn-off. To accomplish this, a shunt resistor must be added to supply the leakage current (I_{CES}) for DTL devices. Since $I_{CES} = 50\mu A$, a $0.4V/0.05mA = 8k\Omega$ or less resistor should be used. For TTL devices using a $2k\Omega$ resistor will insure turn-off with up to $200\mu A$ of leakage current.

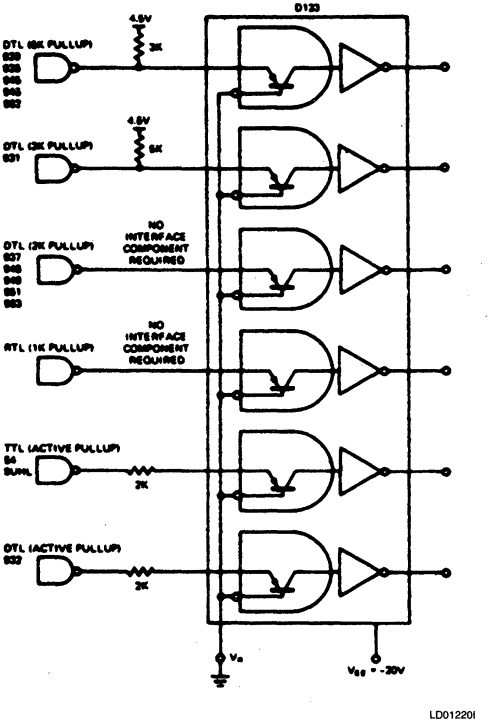


Figure 4: D123 Interface

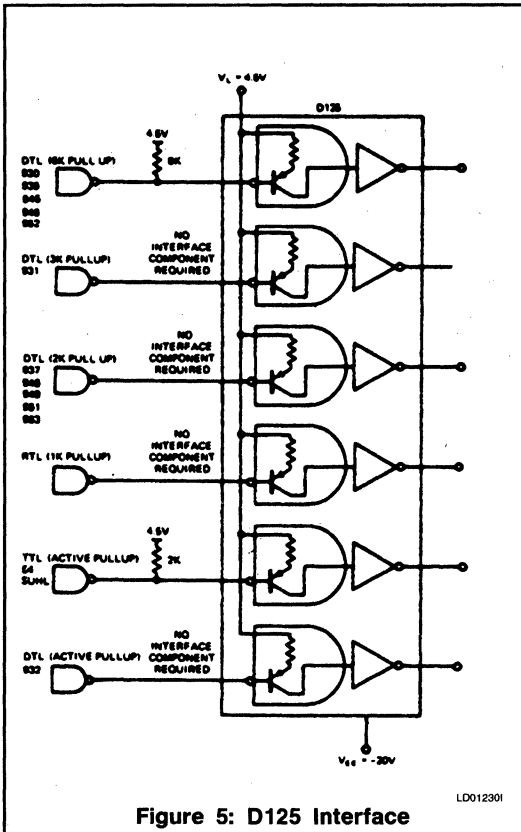


Figure 5: D125 Interface

Using the ENABLE Control

Device pins V_R or V_L, can be used to enable the D123 or D125 drivers. For the D123, the enabling driver must sink $I_{R(ON)}$ X no. of channels used. For the D125, $I_{L(ON)}$ X no. of channels used must be sourced with a voltage at least +4V greater than V_{IN}.

Note: All typical values have been guaranteed by characterization and are not tested.

D129
4-Channel Decoded JFET Switch Driver

GENERAL DESCRIPTION

The D129 is a 4-channel driver with binary decode input. It was designed to provide the DC level-shifting required to interface low-level logic outputs (0.7 to 2.2V) to field-effect transistor inputs (up to 50V peak-to-peak). For a 5V input logic supply, the V^- terminal can be set at any voltage between −5V and −30V. The output transistor is capable of sinking 10mA and will stand-off up to 50V above V^- in the off-state.

The ON state of the driver is controlled by a logic "1" (open) on all three input logic lines, while the OFF state of the driver is achieved by pulling any one of the three inputs to a logic "0" (ground).

The 4-channel driver is internally connected such that each one can be controlled independently or decoded from a binary counter.

FEATURES

- **Quad Three-Input Gates Decode Binary Counter to Four Lines**
- **Inputs Compatible With Low Power TTL and DTL, I_F = 200μA Max**
- **Output Current Sinking Capability 10mA**
- **External Pull-Up Elements Required**
- **Compatible With G115 and G123 Series Multichannel MOSFET Switches Which Include Current-Limiter Pull-Up FETs**

ORDERING INFORMATION

D129 A K

- Package
  - K – 14-pin CERDIP
  - L – 14-pin Flat Pak
  - P – 14-pin Ceramic DIP (Special Order Only)
- Temperature Range
  - A – Military (−55°C to +125°C)
  - B – Commercial (−20°C to +85°C)
- Device Chip Type

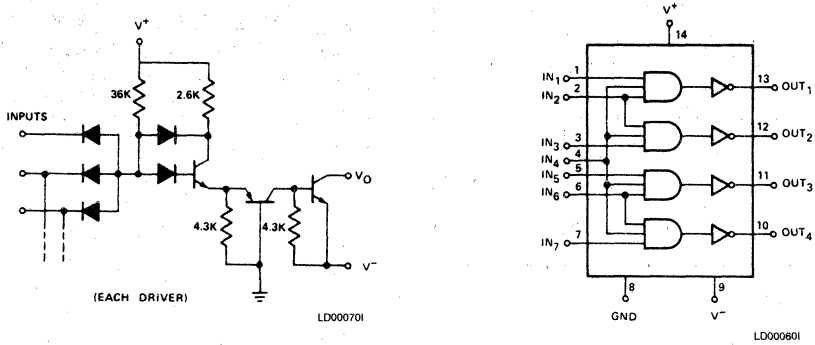


Figure 1: Functional Diagrams (Outline Dwgs DD, FD-2, JD)

Note: All typical values have been guaranteed by characterization and are not tested.

D129

ABSOLUTE MAXIMUM RATINGS

$V_O - V^-$ 50V
GND – V^- 33V
V^+ – GND 8V
V_{IN} – GND ..... ±6V
Current (any terminal) 30mA

Storage Temperature ..... –65°C to +150°C
Operating Temperature ..... –55°C to +125°C
Power Dissipation (note) 750mW
Lead Temperature (Soldering, 10sec) ..... 300°C

Note: Dissipation rating assumes device mounted with all leads welded or soldered to pc board in ambient temperature of 70°C. Derate 10mW/°C for higher ambient temperatures.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS Test conditions unless otherwise specified $V^- = -20V$, $V^+ = 5V$

SYMBOL	PARAMETER	TEST CONDITIONS		MAXIMUM LIMIT						UNIT
				D129M			D129I			
				-55°C	25°C	125°C	-20°C	25°C	85°C	
OUT										
V_{OL}	Output Voltage, Low	I_O = 10mA	V_{IN} = 2.2V, V^+ = 4.5V	-19.3	-19.3	-19	-19.25	-19.25	-19	V
V_{OL}	Output Voltage, Low	I_O = 1mA	V_{IN} = 2.2V, V^+ = 4.5V	-19.8	-19.8	-19.75				V
I_{OH}	Output Current, High	V_O = 10V, V_{IN} = 0.7V		0.1	0.1	20	0.2	0.2	10	µA
INPUT										
I_{INH} *	Input Current Input Voltage High	V_{IN} = 5V Input Under Test, V_{IN} = 0 All Other Inputs		0.25	0.25	5	1	1	5	µA
I_{INL} *	Input Current Input Voltage Low	V_{IN} = 0, V^+ = 5.5V		-250	-200	-160	-250	-225	-200	µA
TIME										
t_{on}	Turn-ON Time	See Switching Time Test Circuit			0.25			0.3		µs
t_{off}	Turn-OFF Time	See Switching Time Test Circuit			1.0			1.5		µs
SUPPLY										
I_{EE}	Negative Supply Current	V^- = -20V, V^+ = 5.5V	One Channel "ON"		-2			-2.25		mA
I_L	Logic Supply Current	V^- = -20V, V^+ = 5.5V	One Channel "ON"		3			3.3		mA
I_{EE}	Negative Supply Current	V^- = -20V, V^+ = 5.5V	All V_{IN} = 0, All Channels "OFF"		-10			-25		µA
I_L	Logic Supply Current	V^- = -20V, V^+ = 5.5V	All V_{IN} = 0, All Channels "OFF"		0.75			1		mA

*Per gate Input

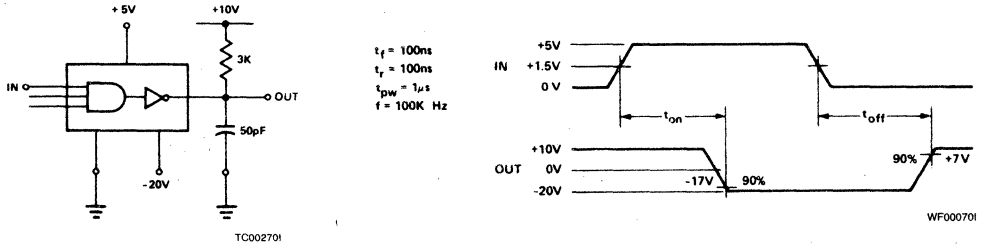


Figure 2: Switching Time and Test Circuit

Note: All typical values have been guaranteed by characterization and are not tested.

DG118/DG123/DG125
4 & 5-Channel SPST Driver With Switch

INTERSIL

GENERAL DESCRIPTION

This series includes devices with four and five channel switching capability. Each channel is composed of a driver and a MOSFET switch. Two driver versions are supplied for inverting and noninverting applications. A MOSFET, used as a current source provides an active pull-up for faster switching.

An external biasing connection is brought out for biasing, the current source, for optimization of speed and power.

FEATURES

- **Available With and Without Programmable Constant Current Pull-up**
- **Zener Protection on All Gates**
- **P-Channel Enhancement-Type MOSFET Switches**
- **Each Switch Summed to One Common Point**

ORDERING INFORMATION

DG118 A K

- Package
  - K – 14-pin CERDIP
  - L – 14-pin Flat Package
  - P – 14-pin Ceramic DIP (Special Order Only)
- Temperature Range
  - A – Military (–55°C to +125°C)
  - B – Commercial (–20°C to +85°C)
- Device Chip Type

TRUTH TABLE

DG123		DG118, DG125		Switch Cond.
V_{IN}	V_R	V_{IN}	V_L	
L	L	L	L	OFF
H	L	L	H	ON
L	H	H	L	OFF
H	H	H	H	OFF

L = 0V, H = +V

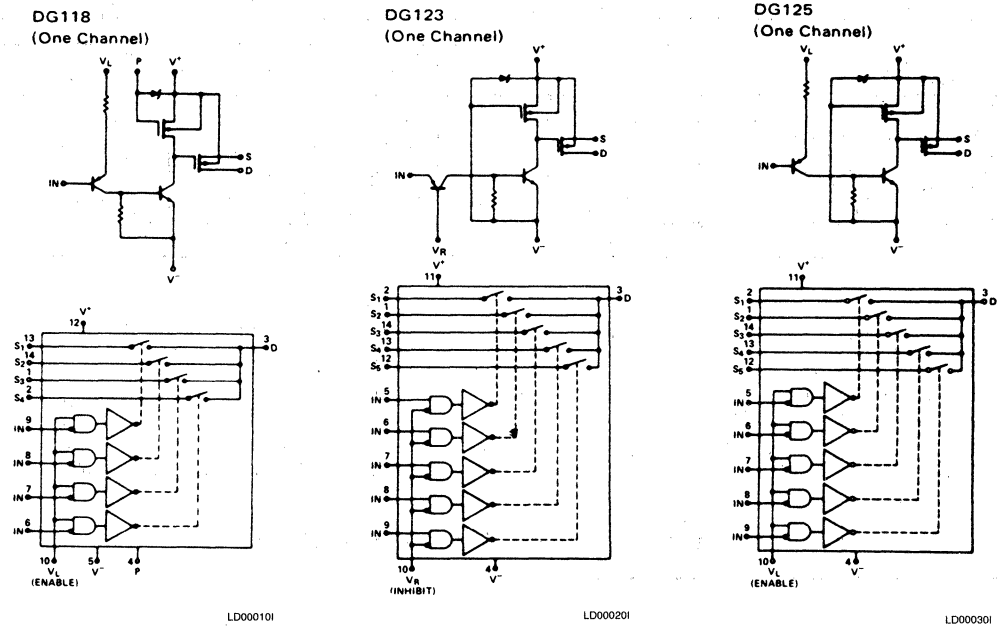


Figure 1: Schematic & Logic Diagrams (Outline Dwgs DD, FD-2, JD)

Note: All typical values have been guaranteed by characterization and are not tested.

ABSOLUTE MAXIMUM RATINGS

Collector to Emitter ($V^+ - V^-$) 33V
Collector to Pull-up ($V^+ - V_P$) 33V
Drain to Emitter ($V_D - V^-$) 32V
Source to Emitter ($V_S - V^-$) 32V
Drain to Source ($V_D - V_S$) 28V
Source to Drain ($V_S - V_D$) 28V
Logic to Emitter ($V_L - V^-$) 33V
Reference to Emitter ($V_R - V^-$) 31V
Reference to Input ($V_R - V_{IN}$) 6V

Logic to Input ($V_L - V_{IN}$) ..... ±6V
Input to Emitter ($V_{IN} - V^-$) 33V
Current (any terminal) 30mA
Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Dissipation (Note) 750mW
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature of 70°C. Derate 10mW/°C for higher ambient temperature.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

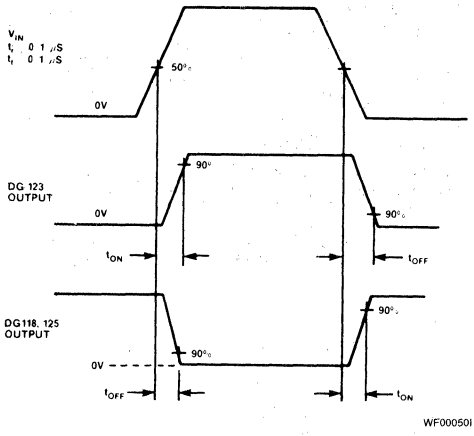
ELECTRICAL CHARACTERISTICS

Test conditions unless specified otherwise are as follows: $V_L = 4.5V$, $V_R = 0$, $V^- = -20V$, and $P = -20V$. Input ON and OFF test conditions used for output and power supply specifications.

DEVICE NO.	PARAMETER (NOTE)	TEST CONDITIONS	MAX LIMITS			UNIT
			-55°C	+25°C	+125°C	
INPUT						
DG123	$I_{IN(OFF)}$	$V_{IN} = 0.4V$	1	1	100	µA
	$V_{IN(ON)}$	$I_{IN} = 1mA$	1.3	1.0	0.8	V
DG118	$I_{IN(OFF)}$	$V_{IN} = 4.1V$	1	1	20	µA
DG125	$I_{IN(ON)}$	$V_{IN} = 0.5V$	-0.7	-0.7	-0.7	mA
OUTPUT						
All circuits	$r_{DS(ON)}$	$V_D = 10V$, $I_S = -1mA$	100	100	125	Ω
		$V_D = 0$, $I_S = -100µA$	200	200	250	Ω
		$V_D = -10V$, $I_S = -100µA$	450	450	600	Ω
	$I_{D(ON)}$	$V_D = 10V$, $I_{S(all)} = 0$		4	4000	nA
	$I_{D(OFF)}$	$V_{S(all)} = 10V$, $V_D = -10V$		-4	-4000	nA
	$I_{S(OFF)}$	$V_D = 10V$, $V_S = -10V$		-1	-1000	nA
POWER SUPPLY						
All circuits	$I_{CC(ON)}$	One Channel (ON)		3		mA
	$I_{L(ON)}$			3		mA
	$I_{R(ON)}$			-0.5		mA
	$I_{EE(ON)}$			-6		mA
All circuits	$I_{CC(OFF)}$	All Channels (OFF)		10		µA
	$I_{L(OFF)}$			10		µA
	$I_{R(OFF)}$			-15		µA
	$I_{EE(OFF)}$			-20		µA
SWITCHING TIMES						
All circuits	$t_{(ON)}$	See Switching Times		0.3		µs
	$t_{(OFF)}$			1		µs

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the MOSFET switch for the given test condition.

Note: All typical values have been guaranteed by characterization and are not tested.



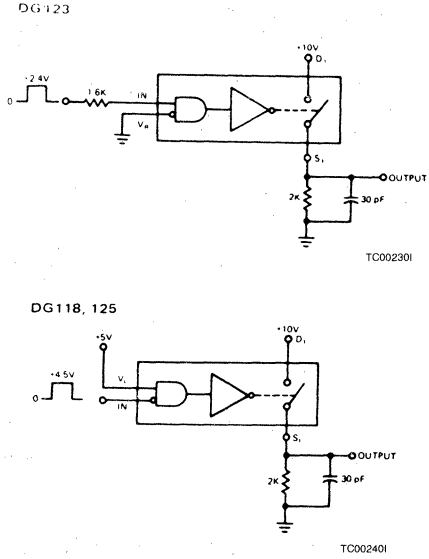
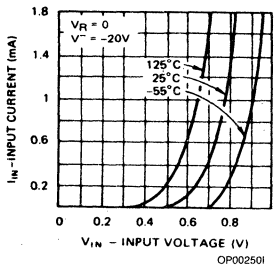


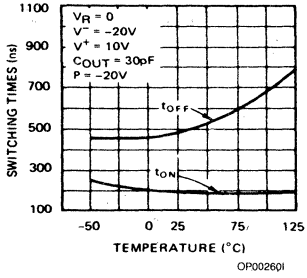
Figure 2: Switching Times

TYPICAL PERFORMANCE CHARACTERISTICS

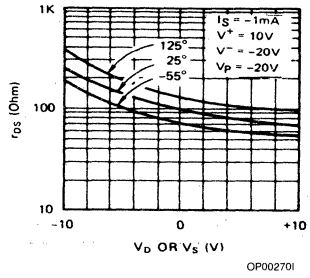
I_{IN} vs V_{IN} DG123



SWITCHING TIMES vs TEMPERATURE



$r_{DS(ON)}$ vs V_D or V_S



Note: All typical values have been guaranteed by characterization and are not tested.

APPLICATION TIPS

The recommended resistor values for interfacing RTL, DTL, and TTL Logic are shown in Figures 3 and 4.

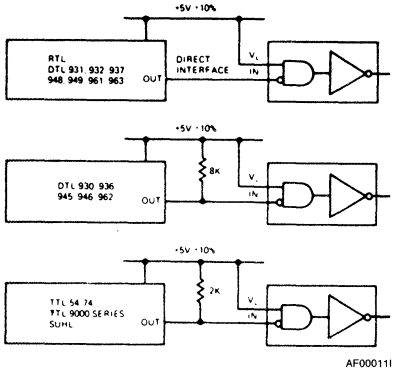


Figure 3: DG118 and DG125 Interface

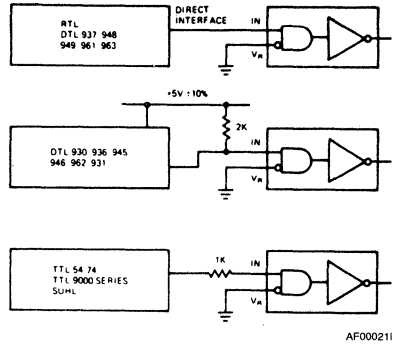


Figure 4: DG123 Interface

Enable Control

The V_R and V_L terminals can be used as either a Strobe or an Enable control. The requirements for sinking current at V_R or sourcing current at V_L are: $I_{L(ON)}$ x No. of channels used, for DG118 and DG125, and $I_{R(ON)}$ x No. of channels used for the DG123 devices. The voltage at V_L must be greater than the voltage at V_{IN} by at least +4V.

Note: All typical values have been guaranteed by characterization and are not tested.

DG126, DG129, DG133, DG134, DG140, DG141, DG151, DG152, DG153, DG154

DUAL JFET Analog Switch

INTERSIL

GENERAL DESCRIPTION

These switching circuits contain two channels in one package, each channel consisting of a driver circuit controlling a SPST or DPST junction FET switch. The driver interfaces DTL, TTL or RTL logic signals for multiplexing, commutating, and D/A converter applications, which permits logic design directly with the switch function. Logic "1" at the input turns the FET switch ON, and logic "0" turns it off.

FEATURES

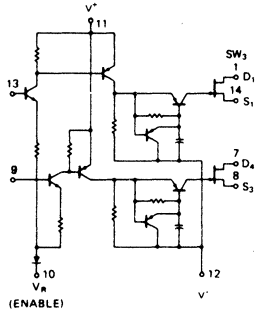
- **Each Channel Complete–Interfaces With Most Integrated Logic**
- **Low OFF Power Dissipation, 1mW**
- **Switches Analog Signals Up to 20 Volts Peak-to-Peak**
- **Low $r_{DS(ON)}$, 10 Ohms Max on DG140/A and DG141/A**
- **Switching Times Improved 100%–'A' Versions**

ORDERING INFORMATION

D126 A K

- Package
  - K – 14-pin CERDIP
  - L – 14-pin Flat Pack
  - P – 14-pin Ceramic DIP (Special Order Only)
- Temperature Range
  - A – Military (–55°C to +125°C)
  - B – Industrial (–20°C to +80°C)
- Device Chip Type

DUAL SPST
DG133 ($r_{DS(ON)}$ = 30Ω)
DG134 ($r_{DS(ON)}$ = 80Ω)
DG141 ($r_{DS(ON)}$ = 10Ω)
DG151 ($r_{DS(ON)}$ = 15Ω)
DG152 ($r_{DS(ON)}$ = 50Ω)



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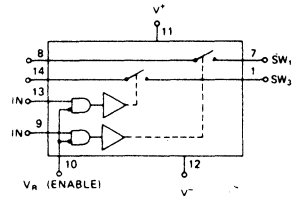

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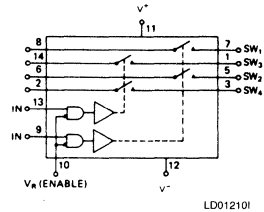
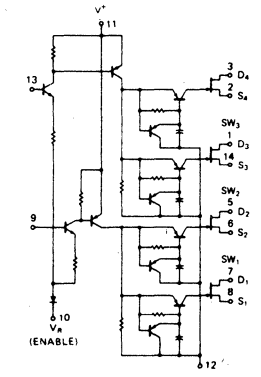
DUAL DPST
DG126 ($r_{DS(ON)}$ = 80Ω)
DG129 ($r_{DS(ON)}$ = 30Ω)
DG140 ($r_{DS(ON)}$ = 10Ω)
DG153 ($r_{DS(ON)}$ = 15Ω)
DG154 ($r_{DS(ON)}$ = 50Ω)



LD01210I



DS02750I

Figure 1: Functional Diagrams (Outline Dwgs DD, FD-2, JD)

Note: All typical values have been guaranteed by characterization and are not tested.

DG126, DG129, DG133, DG134, DG140, DG141, DG151, DG152, DG153, DG154

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Analog Signal Voltage ($V_A - V^-$ or $V^+ - V_A$) 30V
Total Supply Voltage ($V^+ - V^-$) 36V
Positive Supply Voltage to Ref. Voltage ($V^+ - V_R$).. 25V
Ref. Voltage to Neg. Supply Voltage ($V_R - V^-$) 22V
Power Dissipation (Note) 750mW

Current (any terminal) 30mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C. For higher temperature, derate at rate of 10mW/°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Per Channel)

Applied voltages for all test: DG126, DG129, DG133, DG134, DG140, DG141 ($V^+ = +12V$, $V^- = -18V$, $V_R = 0$), and DG151, DG152, DG153, DG154 ($V^+ = +15V$, $V^- = -15V$, $V_R = 0$). Input test condition which guarantees FET switch ON or OFF as specified is used for output and power supply specifications.

SYMBOL (NOTE)	CHARACTERISTIC	TYPE	TEST CONDITIONS	ABSOLUTE MAX LIMIT			UNIT
				−55°C	25°C	125°C	
INPUT							
$V_{IN(ON)}$	Input Voltage-On	All Circuits	$V_2 = -12V$	2.9 min	2.5 min	2.0 min	Volts
$V_{IN(OFF)}$	Input Voltage-Off		$V_2 = -12V$	1.4	1.0	0.6	Volts
$I_{IN(ON)}$	Input Current		$V_{IN} = 2.5V$	120	60	60	μA
$I_{IN(OFF)}$	Input Leakage Current		$V_{IN} = 0.8V$	0.1	0.1	2	μA
SWITCH OUTPUT							
$r_{DS(ON)}$	Drain-Source On Resistance	DG126, DG134	V_{IN} = (See Note), $V_D = 10V$, $I_S = 10mA$	80	80	150	Ω
		DG129, DG133		30	30	50	Ω
		DG140, DG141		10	10	20	Ω
		DG151, DG153	$V_D = 7.5V$, $I_S = 10mA$, V_{IN} = (See Note)	15	15	30	Ω
		DG152, DG154		50	50	100	Ω
$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG126, DG129, DG133, DG134	$V_D = V_S = -10V$		±2	100	nA
$I_{S(OFF)}$	Source Leakage Current		$V_S = 10V$, $V_D = -10V$		±1	100	nA
$I_{D(OFF)}$	Drain Leakage Current		$V_D = 10V$, $V_S = -10V$		±1	100	nA
$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG140, DG141	$V_D = V_S = -10V$		±2	100	nA
$I_{S(OFF)}$	Source Leakage Current		$V_S = 10V$, $V_D = -10V$		±10	1000	nA
$I_{D(OFF)}$	Drain Leakage Current		$V_D = 10V$, $V_S = -10V$		±10	1000	nA
$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG151, DG153	$V_D = V_S = -7.5V$		±2	500	nA
$I_{S(OFF)}$	Source Leakage Current		$V_S = 7.5V$, $V_D = -7.5V$		±10	1000	nA
$I_{D(OFF)}$	Drain Leakage Current		$V_D = 7.5V$, $V_S = -7.5V$		±10	1000	nA
$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG152, DG154	$V_D = V_S = -7.5V$		±2	500	nA
$I_{S(OFF)}$	Source Leakage Current		$V_S = 7.5V$, $V_D = -7.5V$		±2	200	nA
$I_{D(OFF)}$	Drain Leakage Current		$V_D = 7.5V$, $V_S = -7.5V$		±2	200	nA

NOTE: V_{IN} must be a step function with a minimum slew-rate of 1V/μs.

Note: All typical values have been guaranteed by characterization and are not tested.

DG126, DG129, DG133, DG134, DG140, DG141, DG151, DG152, DG153, DG154

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL (NOTE)	CHARACTERISTIC	TYPE	TEST CONDITIONS	ABSOLUTE MAX LIMIT			UNIT
				-55°C	25°C	125°C	
POWER SUPPLY							
$I_{1(ON)}$	Positive Power Supply Drain Current	All Circuits	One Driver ON, V_{IN} = 2.5V		3		mA
$I_{2(ON)}$	Negative Power Supply Drain Current				-1.8		mA
$I_{R(ON)}$	Reference Power Supply Drain Current				-1.4		mA
$I_{1(OFF)}$	Positive Power Supply Leakage Current		Both Drivers OFF, V_{IN} = 0.8V		25		µA
$I_{2(OFF)}$	Negative Power Supply Leakage Current				-25		µA
$I_{R(OFF)}$	Reference Power Supply Leakage Current				-25		µA
SWITCHING							
t_{ON}	Turn-On Time	See Below	DG126, DG129, DG133, DG134, DG152, DG154		600		ns
t_{OFF}	Turn-Off Time	See Below	DG126, DG129, DG133, DG134, DG152, DG154		1.6		µs
t_{ON}	Turn-On Time	See Below	DG140, DG141, DG151, DG153		1.0		µs
t_{OFF}	Turn-On Time	See Below	DG140, DG141, DG151, DG153		2.5		µs
POWER							
P_{ON}	ON Driver Power	All Circuits	Both Inputs V_{IN} = 2.5V		175		mW
P_{OFF}	OFF Driver Power		Both Inputs V_{IN} = 1V		1		mW

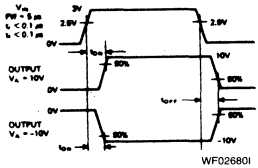
NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

Note: All typical values have been guaranteed by characterization and are not tested.

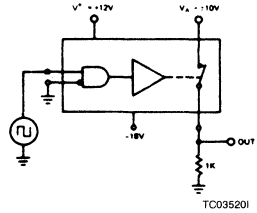
DG126, DG129, DG133, DG134, DG140, DG141, DG151, DG152, DG153, DG154

ELECTRICAL CHARACTERISTICS (CONT.)

DG126, 129, 133, 134, 140, 141

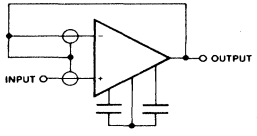


WF02680I



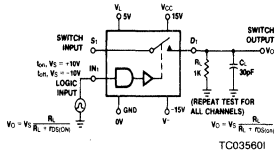
TC03520I

OFF MODEL



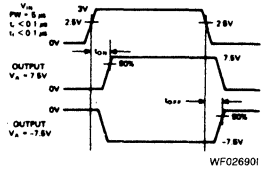
TC03540I

ON MODEL

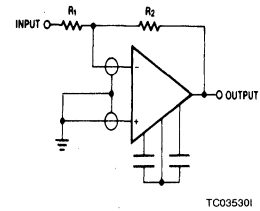


TC03560I

DG151, 152, 153, 154

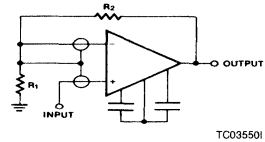


WF02690I



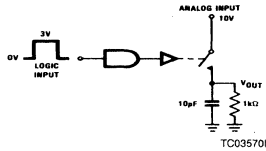
TC03530I

OFF MODEL



TC03550I

ON MODEL



TC03570I

Figure 2: Switching Times (at 25°C)

Note: All typical values have been guaranteed by characterization and are not tested.

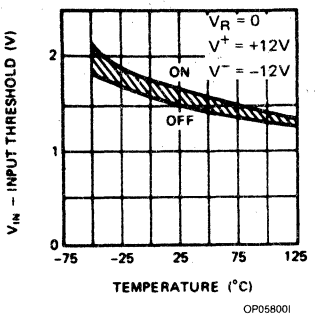
DG126, DG129, DG133, DG134, DG140, DG141, DG151, DG152, DG153, DG154

INTERSIL

TYPICAL PERFORMANCE CHARACTERISTICS (per channel)

DG126, 129, 133, 134, 140, 141

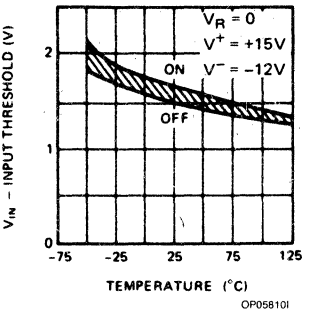
V_{IN} THRESHOLD vs TEMPERATURE



OP05800I

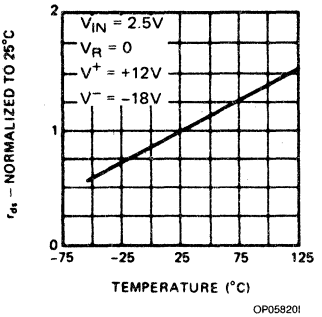
DG151, 152, 153, 154

V_{IN} THRESHOLD vs TEMPERATURE



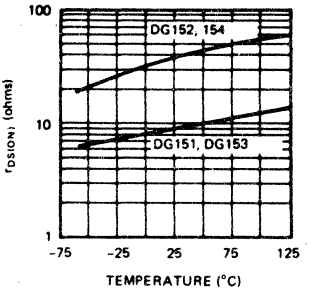
OP05810I

$r_{DS(ON)}$ vs TEMPERATURE (Normalized to 25°C Value)



OP05820I

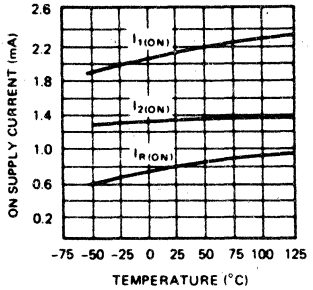
$r_{DS(ON)}$ vs TEMPERATURE



OP05830I

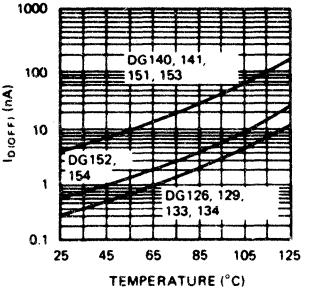
ALL CIRCUITS

ON SUPPLY CURRENT vs TEMPERATURE



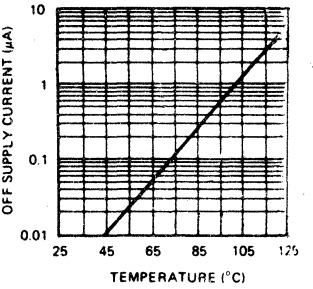
OP05840I

$I_{D(OFF)}$ vs TEMPERATURE



OP05850I

OFF SUPPLY CURRENT vs TEMPERATURE



OP05860I

Note: All typical values have been guaranteed by characterization and are not tested.

DG139, DG142-DG146, DG161-DG164
DUAL JFET Analog Switch

GENERAL DESCRIPTION

Each package contains a monolithic driver with differential input and 2 or 4 discrete FET switches. The driver may be treated as a special purpose differential amplifier which controls the conduction state of the FET switches. The differential output of the driver sets the switches in opposition, one pair open and the other pair closed. All switches may be opened by applying a positive control signal to the V_R terminal.

FEATURES

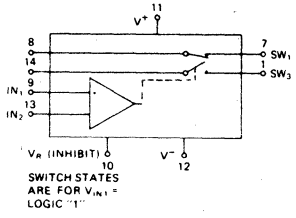
- **Each Channel Complete – Interfaces With Most Integrated Logic**
- **Low OFF Power Dissipation, 1mW**
- **Switches Analog Signals Up to 20 Volts Peak-to-Peak**
- **Low $r_{DS(ON)}$, 10 Ohms Max on DG145 and DG146**

ORDERING INFORMATION

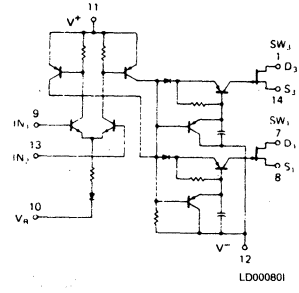
D139 A K

- Package
  - K – 14-pin CERDIP
  - L – 14-pin Flat Pack
  - P – 14-pin Ceramic DIP (Special Order Only)
- Temperature Range
  - A – Military (–55°C to +125°C)
  - B – Industrial (–20°C to +85°C)
- Device Type

SPDT
DG143 ($r_{DS(ON)}$ = 80Ω)
DG144 ($r_{DS(ON)}$ = 30Ω)
DG146 ($r_{DS(ON)}$ = 10Ω)
DG161 ($r_{DS(ON)}$ = 15Ω)
DG162 ($r_{DS(ON)}$ = 50Ω)

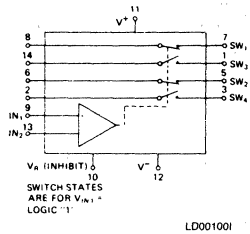


LD00090I

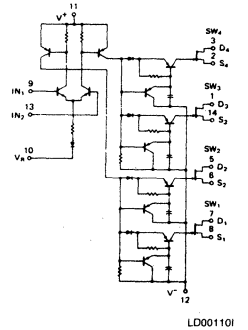


LD00080I

DPDT
DG139 ($r_{DS(ON)}$ = 30Ω)
DG142 ($r_{DS(ON)}$ = 80Ω)
DG145 ($r_{DS(ON)}$ = 10Ω)
DG163 ($r_{DS(ON)}$ = 15Ω)
DG164 ($r_{DS(ON)}$ = 50Ω)



LD00100I



LD00110I

Figure 1: Functional Diagrams (Outline Dwgs DD, FD-2, JD)

Note: All typical values have been guaranteed by characterization and are not tested.

DG139, DG142-DG146, DG161-DG164

ABSOLUTE MAXIMUM RATINGS

$V^+ - V^-$ 36V
$V_S - V^-$ 30V
$V^+ - V_S$ 30V
$V_S - V_D$ ..... ±22V
$V_R - V^-$ 21V
$V^+ - V_R$ 17V
$V^+ - V_{IN1}$ or V_{IN2} 14V
$V_{IN1} - V_{IN2}$ ..... ±6V
$V_{IN1} - V_R$ ..... ±6V
$V_{IN2} - V_R$ ..... ±6V
Power Dissipation (Note) 750mW
Current (any terminal) 30mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C. For higher temperature, derate at rate of 10mW/°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Applied voltages for all tests: DG139, DG142, DG143, DG144, DG145, DG146 (V^+ = 12V, V^- = −18V, V_R = 0, V_{IN2} = 2.5V) and DG161, DG162, DG163, DG164 (V^+ = 15V, V^- = −15V, V_R = 0, V_{IN2} = 2.5V). Input test condition that guarantees FET switch ON or OFF as specified is used for output specifications.

SYMBOL (NOTE)	PARAMETER	TYPE	TEST CONDITIONS	ABSOLUTE MAX LIMIT			UNIT
				−55°C	25°C	125°C	
INPUT							
$I_{IN1(ON)}$	Input Current	All Circuits	V_{IN1} = 3.0V	120	60	60	µA
$I_{IN2(ON)}$			V_{IN2} = 2.0V	120	60	60	µA
$I_{IN1(OFF)}$	Input Leakage Current		V_{IN1} = 2.0V	0.1	0.1	2	µA
$I_{IN2(OFF)}$			V_{IN2} = 3.0V	0.1	0.1	2	µA
SWITCH OUTPUT							
$r_{DS(ON)}$	Drain-Source On Resistance	DG142 DG143	V_D = 10V, I_S = −10mA V_{IN} (See Note)	80	80	150	Ω
		DG139 DG144		30	30	60	Ω
		DG145 DG146	V_D = 10V, I_S = −10mA V_{IN} (See Note)	10	10	20	Ω
		DG161 DG163	V_D = 7.5V, I_S = −10mA V_{IN} (See Note)	15	15	30	Ω
		DG162 DG164		50	50	100	Ω
$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG139 DG142 DG143 DG144	$V_D = V_S$, = −10V		2	100	nA
$I_{S(OFF)}$	Source Leakage Current		V_S = 10V, V_D = −10V		1	100	nA
$I_{D(OFF)}$	Drain Leakage Current		V_D = 10V, V_S = −10V		1	100	nA
$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG145 DG146	$V_D = V_S$ = −10V		2	100	nA
$I_{S(OFF)}$	Source Leakage Current		V_S = 10V, V_D = −10V		10	1000	nA
$I_{D(OFF)}$	Drain Leakage Current		V_D = 10V, V_S = −10V		10	1000	nA
$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG161 DG163	$V_D = V_S$ = −7.5V		2	500	nA
$I_{S(OFF)}$	Source Leakage Current		V_S = 7.5V, V_D = −7.5V		10	1000	nA
$I_{D(OFF)}$	Drain Leakage Current		V_D = 7.5V, V_S = −7.5V		10	1000	nA
$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG162 DG164	$V_D = V_S$ = −7.5V		2	500	nA
$I_{S(OFF)}$	Source Leakage Current		V_S = 7.5V, V_D = −7.5V		2	200	nA
$I_{D(OFF)}$	Drain Leakage Current		V_D = 7.5V, V_S = −7.5V		2	200	nA

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test. V_{IN} must be a step function with a minimum slew-rate of 1V/µs.

Note: All typical values have been guaranteed by characterization and are not tested.

DG139, DG142-DG146, DG161-DG164

INTERSIL

ELECTRICAL CHARACTERISTICS (CONT.)

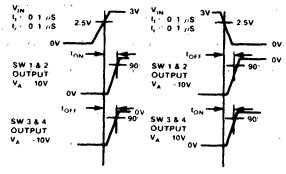
SYMBOL (NOTE)	PARAMETER	TYPE	TEST CONDITIONS	ABSOLUTE MAX LIMIT			UNIT
				-55°C	25°C	125°C	
POWER SUPPLY							
$I_{1(ON)}$	Positive Power Supply Drain Current	All Circuits	V_{IN1} = 3V or V_{IN1} = 2V		4.0		mA
$I_{2(ON)}$	Negative Power Supply Drain Current				-2.0		mA
$I_{R(ON)}$	Reference Power Supply Drain Current				-2.0		mA
$I_{1(OFF)}$	Positive Power Supply Leakage Current		V_{IN1} = V_{IN2}, = 0.8V		25		µA
$I_{2(OFF)}$	Negative Power Supply Leakage Current				-25		µA
$I_{R(OFF)}$	Reference Power Supply Leakage Current				-25		µA
SWITCHING							
t_{ON}	Turn-On Time	DG139, DG142 DG143, DG144 DG162, DG164	See Switching Times		0.8		µs
t_{OFF}	Turn-Off Time	DG139, DG142 DG143, DG144 DG162, DG164	See Switching Times		1.6		µs
t_{ON}	Turn-On Time	DG145, DG146 DG161, DG163	See Switching Times		1.0		µs
t_{OFF}	Turn-Off Time	DG145, DG146 DG161, DG163	See Switching Times		2.5		µs

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

3

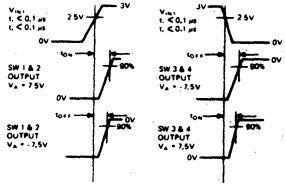
Note: All typical values have been guaranteed by characterization and are not tested.

DG139, 142, 143, 144, 145, 146

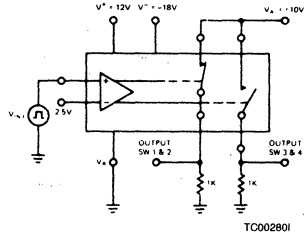


WF00080I

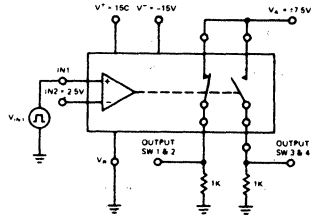
DG161, 162, 163, 164



WF00090I



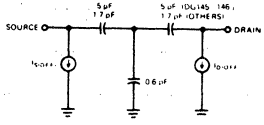
TC00280I



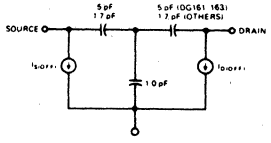
TC00290I

OFF MODEL

OFF MODEL



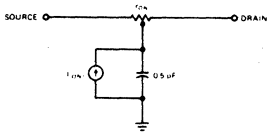
TC00300I



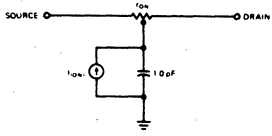
TC00310I

ON MODEL

ON MODEL



TC00320I



TC00330I

Figure 2: Switching Times Test Circuits

Note: All typical values have been guaranteed by characterization and are not tested.

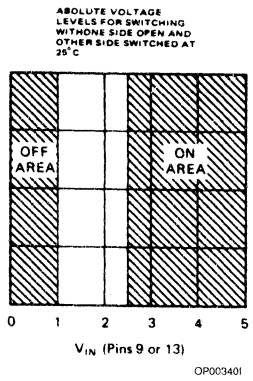


Figure 3

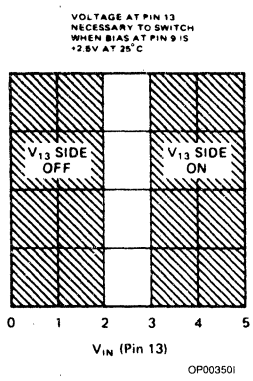


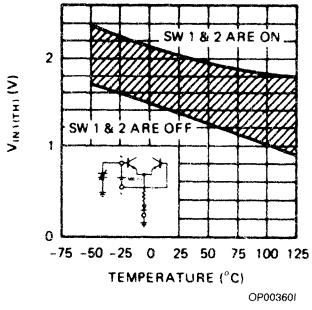
Figure 4

NOTE 1: An example of Absolute Minimum Differential Voltage, $|V_9-V_{13}|$, is when V_9 = 3V and V_{13} = 2.5V, the V_9 side of the switch is ON and the V_{13} side of the switch is OFF at 25°C. Conversely, when V_9 = 2V and V_{13} = 2.5V, the V_9 side of the switch is OFF and the V_{13} side of the switch is ON at 25°C.

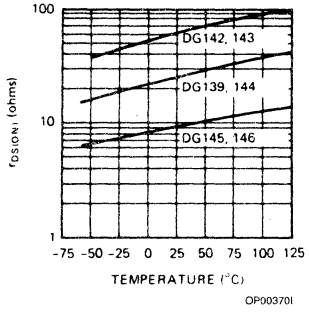
TYPICAL PERFORMANCE CHARACTERISTICS (per channel)

DG139, 142, 144, 145, 146

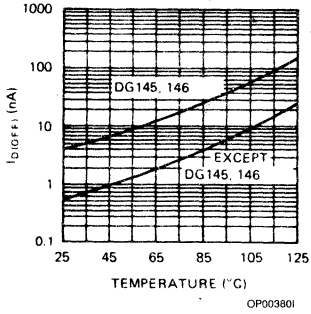
V_{IN1} THRESHOLD vs TEMPERATURE



$r_{DS(ON)}$ vs TEMPERATURE

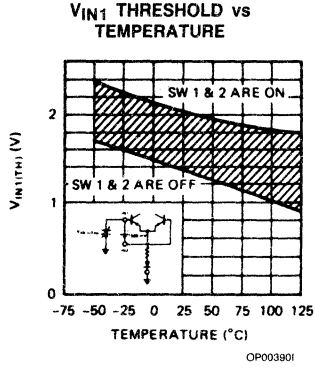


$I_{D(OFF)}$ vs TEMPERATURE

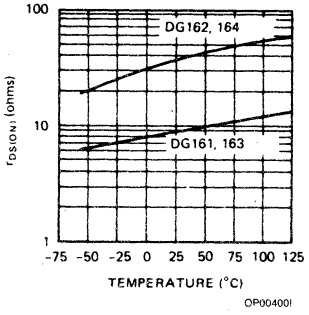


DG161, 162, 163, 164

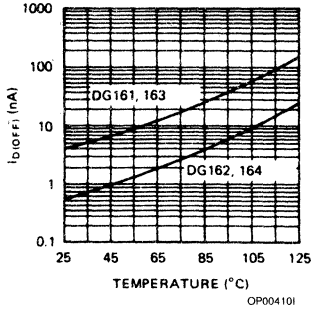
V_{IN1} THRESHOLD vs TEMPERATURE



$R_{DS(ON)}$ vs TEMPERATURE



$I_{S(OFF)}$ vs TEMPERATURE



Note: All typical values have been guaranteed by characterization and are not tested.

DG180-191
High-Speed Driver With JFET Switch

INTERSIL

GENERAL DESCRIPTION

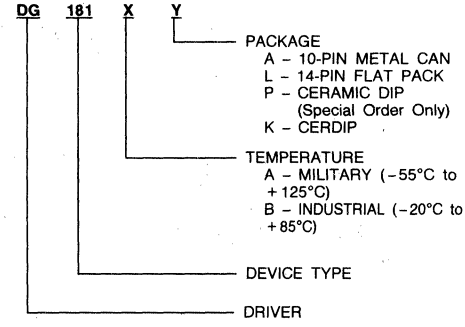
The DG180 thru DG191 series of analog gates consist of 2 or 4 N-channel junction-type field-effect transistors (JFET) designed to function as electronic switches. Level-shifting drivers enable low-level inputs (0.8 to 2V) to control the ON-OFF state of each switch. The driver is designed to provide a turn-off speed which is faster than turn-on speed, so that break-before-make action is achieved when switching from one channel to another. In the ON state, each switch conducts current equally well in both directions. In the OFF condition, the switches will block voltages up to 20V peak-to-peak. Switch-OFF input-output isolation is 50dB at 10MHz, due to the low output impedance of the FET-gate driving circuit.

FEATURES

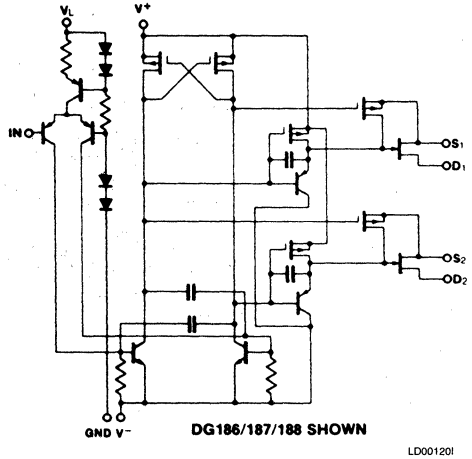
- **Constant ON-Resistance for Signals to ±10V (DG182, 185, 188, 191), to ±7.5V (All Devices)**
- **±15V Power Supplies**
- **< 2nA Leakage From Signal Channel in Both ON and OFF States**
- **TTL, DTL, RTL Direct Drive Compatibility**
- **t_{on}, t_{off} < 150ns, Break-Before-Make Action**
- **Cross-talk and Open Switch Isolation > 50dB at 10MHz (75Ω Load)**
- **JAN 38510 Approved**

ORDERING INFORMATION

PART NUMBER	TYPE	$r_{DS(on)}$ (MAX)
DG180	Dual SPST	10
DG181	Dual SPST	30
DG182	Dual SPST	75
DG183	Dual DPST	10
DG184	Dual DPST	30
DG185	Dual DPST	75
DG186	SPDT	10
DG187	SPDT	30
DG188	SPDT	75
DG189	Dual SPDT	10
DG190	Dual SPDT	30
DG191	Dual SPDT	75



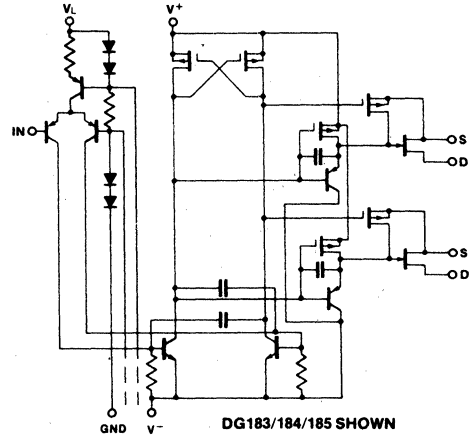
ONE AND TWO CHANNEL SPDT AND SPST CIRCUIT CONFIGURATION



DG186/187/188 SHOWN

LD00120I

TWO CHANNEL DPST CIRCUIT CONFIGURATION



DG183/184/185 SHOWN

LD00130I

Figure 1: Functional Diagram (Typical Channel)

Note: All typical values have been guaranteed by characterization and are not tested.

ABSOLUTE MAXIMUM RATINGS

V^+-V^- 36V
V^+-V_D 33V
V_D-V^- 33V
V_D-V_S ..... ±22V
V_L-V^- 36V
V_L-V_{IN} 8V
V_L-GND 8V
V_{IN}-GND 8V

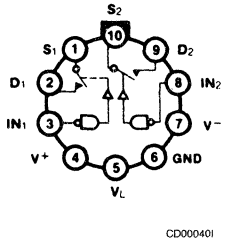
GND-V^- 27V
GND-V_{IN} 20V
Current (S or D) See Note 3 ..... 200mA
Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Power Dissipation* ..... 450 (TW), 750 (FLAT), 825(DIP)mW
Lead Temperature (Soldering, 10sec) ..... 300°C

*Device mounted with all leads welded or soldered to PC board. Derate 6mW/°C (TW); 10mW/°C (FLAT); 11mW/°C (DIP) above 75°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DUAL SPST (DG180, 181, 182)

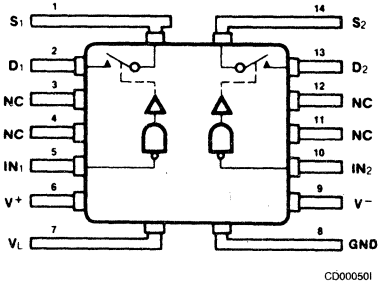
Metal Can Package



CD00040I

(OUTLINE DWG TO-100)

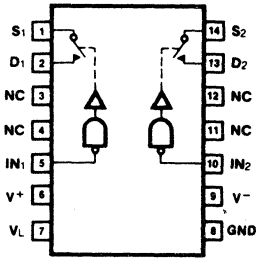
Flat Package



CD00050I

(OUTLINE DWG FD-2)

CERDIP*

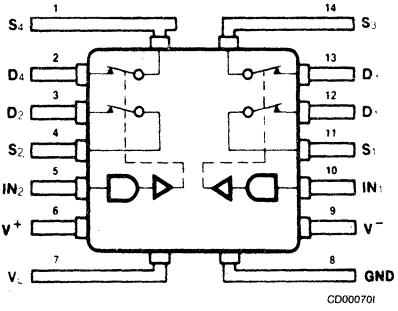


CD00060I

(OUTLINE DWG JD)

DUAL DPST (DG183, 184, 185)

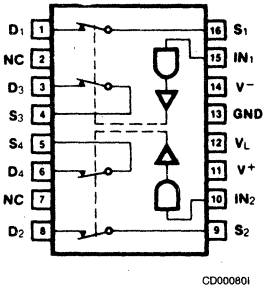
Flat Package



CD00070I

(OUTLINE DWG FD-2)

CERDIP*



CD00080I

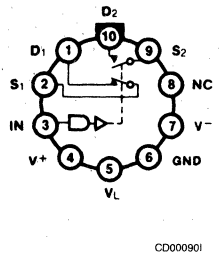
(OUTLINE DWG JE)

Figure 2: Pin Configurations and Switching State Diagram

Note: All typical values have been guaranteed by characterization and are not tested.

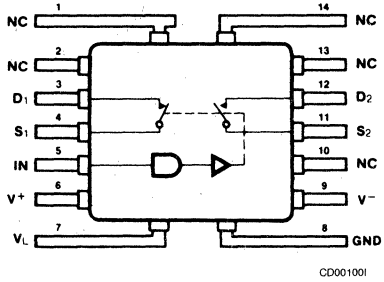
SPDT (DG186, 187, 188)

Metal Can Package



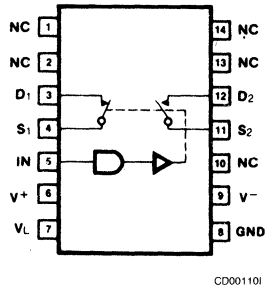
(OUTLINE DWG TO-100)

Flat Package



(OUTLINE DWG FD-2)

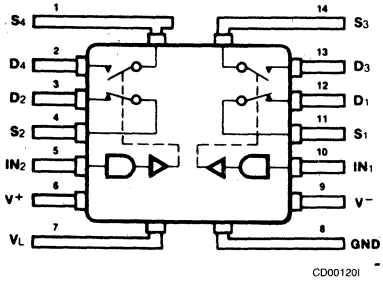
CERDIP*



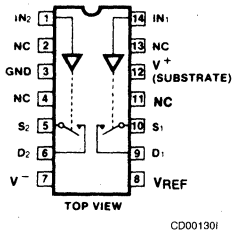
(OUTLINE DWG JD)

DUAL SPDT (DG189, 190, 191)

Flat Package



CERDIP*



*Side braze ceramic package available as special order only. Consult factory.

(OUTLINE DWG FD-2)

(OUTLINE DWG JE)

Figure 2: Pin Configurations and Switching State Diagram (Cont.)

ELECTRICAL CHARACTERISTICS ($V^+ = +15V$, $V^- = -15V$, $V_L = 5V$, Unless Noted)

PARAMETER	DEVICE NO.	TEST CONDITIONS (NOTE 1)	A SERIES			B SERIES			UNIT
			−55°C	+25°C	+125°C	−20°C	+25°C	+85°C	
SWITCH									
$I_{S(off)}$	DG181, 182, 184, 185 187, 188, 190, 191 (DG180, 183, 186, 189)	$V_S = 10V$, $V_D = -10V$, $V^+ = 10V$ $V^- = -20V$, $V_{IN} =$ "OFF"		±1 ±(10)	100 (1000)		±5 (15)	100 (300)	nA
	DG181, 184, 187, 190 (DG180, 183, 186, 189)	$V_S = 7.5V$, $V_D = -7.5V$ $V_{IN} =$ "OFF"		±1 ±(10)	100 (1000)		±5 (15)	100 (300)	nA
	DG182, 185, 188, 191	$V_S = 10V$, $V_D = -10V$ $V_{IN} =$ "OFF"		±1	100		±5	100	nA
$I_{D(off)}$	DG181, 182, 184, 185 187, 188, 190, 191 (DG180, 183, 186, 189)	$V_S = 10V$, $V_D = -10V$, $V^+ = 10V$ $V^- = -20V$, $V_{IN} =$ "OFF"		±1 ±(10)	100 (1000)		±5 (15)	100 (300)	nA
	DG181, 184, 187, 190 (DG180, 183, 186, 189)	$V_S = 7.5V$, $V_D = -7.5V$ $V_{IN} =$ "OFF"		±1 ±(10)	100 (1000)		±5 (15)	100 (300)	nA
	DG182, 185, 188, 191	$V_S = 10V$, $V_D = -10V$ $V_{IN} =$ "OFF"		±1	100		±5	100	nA
$I_{D(on)} + I_{S(on)}$	DG180, 181, 183, 184 186, 187, 189, 190	$V_D = V_S = -7.5V$, $V_{IN} =$ "ON"		±2	−200		−10	−200	nA
	DG182, 185, 188, 191	$V_D = V_S = -10V$, $V_{IN} =$ "ON"		±2	−200		−10	−200	nA

Note: All typical values have been guaranteed by characterization and are not tested.

DG180-191

ELECTRICAL CHARACTERISTICS (CONT.)

PARAMETER	DEVICE NO.	TEST CONDITIONS (NOTE 1)	A SERIES			B SERIES			UNIT
			-55°C	+25°C	+125°C	-20°C	+25°C	+85°C	
INPUT									
I_{INL}	ALL	V_{IN} = 0V	-250	-250	-250	-250	-250	-250	µA
I_{INH}	ALL	V_{IN} = 5V		10	20		10	20	µA
DYNAMIC									
t_{on}	10Ω Switches	See switching time test circuit		300			350		ns
	30Ω Switches			150			180		
	75Ω Switches			250			300		
t_{off}	10Ω Switches			250			300		
	30Ω and 75Ω Switches			130			150		
$C_{S(off)}$	DG181, 182, 184, 185, 187, 188, 190, 191 (DG180, 183, 186 189)	V_S = -5V, I_D = 0, f = 1MHz	9 typical (21 typical)						pF
$C_{D(off)}$		V_D = +5V, I_S = 0, f = 1MHz	6 typical (17 typical)						
$C_{D(on)} + C_{S(on)}$		V_D = V_S = 0, f = 1MHz	14 typical (17 typical)						
OFF Isolation		R_L = 75Ω, C_L = 3pF	Typically > 50dB at 10MHz (See Note 2)						
SUPPLY									
I^+	DG180, 181, 182, 189 190, 191	V_{IN} = 5V		1.5			1.5		mA
	DG183, 184, 185			0.1			0.1		
	DG186, 187, 188			0.8			0.8		
I^-	DG180, 181, 182, 189 190, 191			-5.0			-5.0		
	DG183, 184, 185			-4.0			-4.0		
	DG186, 187, 188			-3.0			-3.0		
I_L	DG180, 181, 182, 183 184, 185, 189, 190, 191			4.5			4.5		
	DG186, 187, 188			3.2			3.2		
I_{GND}	ALL			-2.0			-2.0		
I^+	DG180, 181, 182, 189 190, 191	V_{IN} = 0V		1.5			1.5		
	DG183, 184, 185			3.0			3.0		
	DG186, 187, 188			0.8			0.8		
I^-	DG180, 181, 182, 189 190, 191			-5.0			-5.0		
	DG183, 184, 185			-5.5			-5.5		
	DG186, 187, 188			-3.0			-3.0		
I_L	DG180, 181, 182, 183 184, 185, 189, 190, 191			4.5			4.5		
	DG186, 187, 188			3.2			3.2		
I_{GND}	ALL			-2.0			-2.0		

NOTES 1. See Switching State Diagrams for V_{IN} "ON" and V_{IN} "OFF" Test Conditions.
2. Off Isolation typically > 55dB at 1MHz for DG180, 183, 186, 189.
3. Saturation Drain Current for DG180, 183, 186, 189 only, typically 300mA (2ms Pulse Duration). Maximum Current on all other devices (any terminal) 30mA.

Note: All typical values have been guaranteed by characterization and are not tested.

DG180-191

ELECTRICAL CHARACTERISTICS (CONT.) MAXIMUM RESISTANCES ($r_{DS(ON)}$ MAX)

DEVICE NUMBER	CONDITIONS (Note 1) $V^+ = 15V$, $V^- = -15V$, $V_L = 5V$		MILITARY TEMPERATURE			INDUSTRIAL TEMPERATURE			UNIT
			−55°C	+25°C	+125°C	−20°C	+25°C	+85°C	
DG180	$V_D = -7.5V$		10	10	20	15	15	25	Ω
DG181	$V_D = -7.5V$		30	30	60	50	50	75	Ω
DG182	$V_D = -10V$		75	75	100	100	100	150	Ω
DG183	$V_D = -7.5V$		10	10	20	15	15	25	Ω
DG184	$V_D = -7.5V$		30	30	60	50	50	75	Ω
DG185	$V_D = -10V$	$I_S = -10mA$	75	75	150	100	100	150	Ω
DG186	$V_D = -7.5V$		10	10	20	15	15	25	Ω
DG187	$V_D = -7.5V$	V_{IN} = "ON"	30	30	60	50	50	75	Ω
DG188	$V_D = -10V$		75	75	150	100	100	150	Ω
DG189	$V_D = -7.5V$		10	10	20	15	15	25	Ω
DG190	$V_D = -7.5V$		30	30	60	50	50	50	Ω
DG191	$V_D = -10V$		75	75	150	100	100	150	Ω

APPLICATION HINT (for design only): Normally the minimum signal handling capability of the DG180 through DG191 family is 20V peak-to-peak for the 75Ω switches and 15V peak-to-peak for the 10Ω and 30Ω (refer I_D and I_S tests above). For other Analog Signals, the following guidelines can be used: proper switch turn-off requires that $V^- \leq V_{ANALOG}(peak) - V_p$ where $V_p = 7.5V$ for the 10Ω and 30Ω switches and $V_p = 5.0V$ for 75Ω switches e.g., −10V minimum (−peak) analog signal and a 75Ω switch ($V_P = 5V$), requires that $V^- \leq -10V - 5V = -15V$.

Logic Input for "OFF" to "ON" Condition (DG180/181/182 Shown)

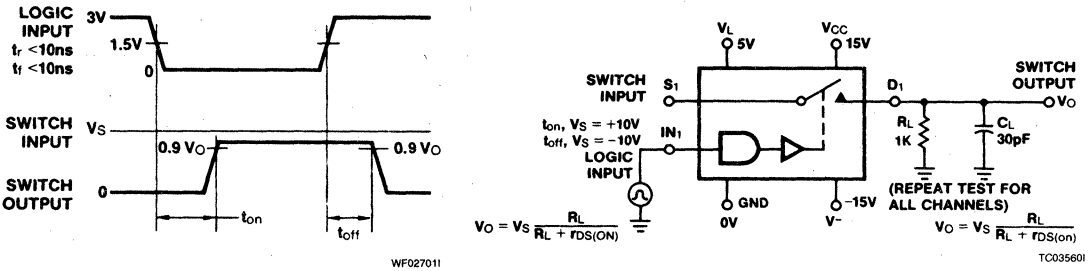


Figure 3: Switching Time Test Circuits

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

DUAL SPST-DG180/181/182

TEST CONDITIONS

DG180/181/182	
V_{IN} "ON" = 0.8V	All Channels
V_{IN} "OFF" = 2.0V	All Channels

SWITCH STATES ARE
FOR LOGIC "1" INPUT = 2.0V

DUAL DPST-DG183/184/185

TEST CONDITIONS

DG183/184/185	
V_{IN} "ON" = 2.0V	All Channels
V_{IN} "OFF" = 0.8V	All Channels

SWITCH STATES ARE
FOR LOGIC "1" INPUT = 2.0V

SPDT-DG186/187/188

TEST CONDITIONS

DG186/187/188	
V_{IN} "ON" = 2.0V	Channel 1
V_{IN} "ON" = 0.8V	Channel 2
V_{IN} "OFF" = 2.0V	Channel 2
V_{IN} "OFF" = 0.8V	Channel 1

SWITCH STATES ARE
FOR LOGIC "1" INPUT = 2.0V

DUAL SPDT-DG189/190/191

TEST CONDITIONS

DG189/190/191	
V_{IN} "ON" = 2.0V	Channels 1 & 2
V_{IN} "ON" = 0.8V	Channels 3 & 4
V_{IN} "OFF" = 2.0V	Channels 3 & 4
V_{IN} "OFF" = 0.8V	Channels 1 & 2

SWITCH STATES ARE
FOR LOGIC "1" INPUT = 2.0V

Note: All typical values have been guaranteed by characterization and are not tested.

DG200/IH5200
CMOS Dual SPST Analog Switches

GENERAL DESCRIPTION

The DG200/IH5200 solid state analog gates are designed using an improved, high voltage CMOS monolithic technology. They provide ease-of-use and performance advantages not previously available from solid state switches. Destructive latch-up of solid state analog gates has been eliminated by INTERSIL's CMOS technology.

The DG200 is completely spec and pin-out compatible with the industry standard device, while the IH5200 offers significantly enhanced specifications with respect to ON and OFF leakage currents, switching times, and supply current.

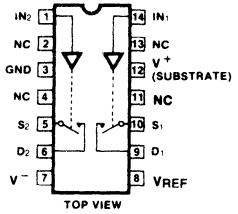
FEATURES

- **Switches Greater Than 28Vpp Signals With ±15V Supplies**
- **Break-Before-Make Switching t_{off} 250ns, t_{on} 700ns Typical**
- **TTL, DTL, CMOS, PMOS Compatible**
- **Non-Latching With Supply Turn-Off**
- **Complete Monolithic Construction**
- **Industry Standard (DG200)**
- **Improved Performance Version (IH5200)**

ORDERING INFORMATION

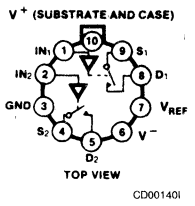
INDUSTRY STANDARD PART	IMPROVED SPEC DEVICE	PACKAGE	TEMPERATURE RANGE
DG200AA	IH5200MTW	10-Pin Metal Can	−55°C to +125°C
DG200AK	IH5200MJD	14-Pin CERDIP	−55°C to +125°C
DG200AL	IH5200MFD	14-Pin Flat Pak	−55°C to +125°C
DG200BA	IH5200ITW	10-Pin Metal Can	−25°C to +85°C
DG200BK	IH5200IJD	14-Pin CERDIP	−25°C to +85°C
DG200BL	IH5200IFD	14-Pin Flat Pak	−25°C to +85°C
DG200CJ	IH5200CPD	14-Pin Epoxy Dip	0°C to +70°C

CERDIP & EPOXY DUAL-IN-LINE PACKAGE (outline dwgs JD, PD)



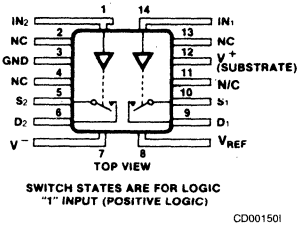
CD00130I

METAL CAN PACKAGE (outline dwg TO-100)



CD00140I

FLAT PACKAGE (outline dwg FD-2)



CD00150I

Figure 1: Pin Configurations

Note: All typical values have been guaranteed by characterization and are not tested.

DG200/IH5200

INTERSIL

ABSOLUTE MAXIMUM RATINGS

V^+-V^- ..... < 33V
V^+-V_D ..... < 30V
V_D-V^- ..... < 30V
V_D-V_S ..... < ±22V
V_{IN}-GND ..... < 20V
Current (Any Terminal) ..... > 30mA

Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Power Dissipation 450mW

(All Leads Soldered to a P.C. Board.) Derate 6mW/°C Above 75°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

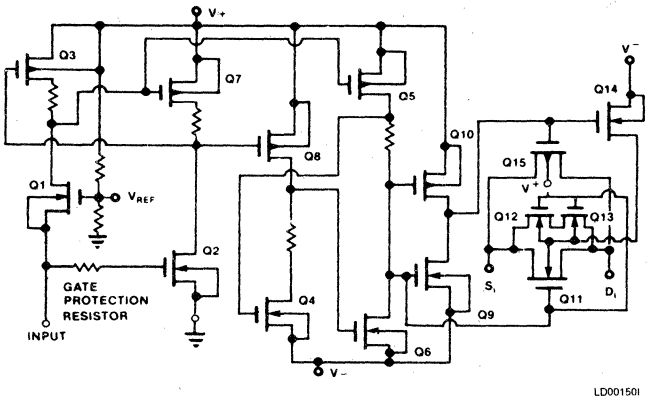


Figure 2: Functional Diagram (1/2 DG200/IH5200)

DG200 ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = +15V, V^- = -15V)

PER CHANNEL		TEST CONDITIONS	MIN/MAX LIMITS						UNIT
			MILITARY			COM'L/INDUSTRIAL			
SYMBOL	CHARACTERISTIC		-55°C	+25°C	+125°C	0/ -25°C	+25°C	+70°C/ +85°C	
$I_{IN(ON)}$	Input Logic Current	V_{IN} = 0.8V See Note 1	±10	±1	±10		±10	±10	µA
$I_{IN(OFF)}$	Input Logic Current	V_{IN} = 2.4V See Note 1	±10	±1	±10		±10	±10	µA
$r_{DS(ON)}$	Drain-Source On Resistance	I_S = 10mA V_{ANALOG} = ±10V	70	70	100	80	80	100	Ω
$r_{DS(ON)}$	Channel-to-Channel $r_{DS(ON)}$ Match			25 (typ)			30 (typ)		Ω
V_{ANALOG}	Min. Analog Signal Handling Capability			±15			±15		V
$I_{D(OFF)}$	Switch OFF Leakage Current	V_{ANALOG} = -14V to +14V		±2	100		±5	100	nA
$I_{S(OFF)}$	Switch OFF Leakage Current	V_{ANALOG} = -14V to +14V		±2	100		±5	100	nA
$I_{D(ON)}$ + $I_{S(ON)}$	Switch ON Leakage Current	V_D = V_S = -14V to +14V		±2	200		±10	200	nA
t_{on}	Switch "ON" Time See Note 1	R_L = 1kΩ, V_{ANALOG} = -10V to +10V See Fig. 3		1.0			1.0		µs
t_{off}	Switch "OFF" Time	R_L = 1kΩ, V_{ANALOG} = -10V to +10V See Fig. 3		0.5			0.5		µs
$Q_{(INJ.)}$	Charge Injection	See Fig. 4		15 (typ)			20 (typ)		mV

Note: All typical values have been guaranteed by characterization and are not tested.

DG200/IH5200

INTERSIL

PER CHANNEL SYMBOL	PER CHANNEL CHARACTERISTIC	TEST CONDITIONS	MIN/MAX LIMITS MILITARY −55°C	MILITARY +25°C	MILITARY +125°C	COM'L/INDUSTRIAL 0/−25°C	COM'L/INDUSTRIAL +25°C	COM'L/INDUSTRIAL +70°C/+85°C	UNIT
OIRR	Min. Off Isolation Rejection Ratio	f = 1MHz, R_L = 100Ω, C_L ≤ 5pF See Fig. 5 (Note 1)		54 (typ)			50 (typ)		dB
I_{V1}	+ Power Supply Quiescent Current	V_{IN} = 0V or V_{IN} = 5V	1000	1000	2000	1000	1000	2000	μA
I_{V2}	−Power Supply Quiescent Current		1000	1000	2000	1000	1000	2000	μA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off		54 (typ)			50 (typ)		dB

NOTE 1: Pull Down Resistor must be ≤ 2kΩ
NOTE 2: Typical values are for design aid only, not guaranteed and not subject to production testing.

IH5200 ELECTRICAL CHARACTERISTICS (@ 25°C, V^+ = +15V, V^- = −15V$_{REF}$ open)

PER CHANNEL SYMBOL	PER CHANNEL CHARACTERISTIC	TEST CONDITIONS	MIN/MAX LIMITS MILITARY −55°C	MILITARY +25°C	MILITARY +125°C	COM'L/INDUSTRIAL 0/−25°C	COM'L/INDUSTRIAL +25°C	COM'L/INDUSTRIAL +70°C/+85°C	UNIT
$I_{IN(ON)}$	Input Logic Current	V_{IN} = 0.8V	±10	±1	±10		±10	±10	μA
$I_{IN(OFF)}$	Input Logic Current	V_{IN} = 2.4V	±10	±1	10		±10	±10	μA
$r_{DS(ON)}$	Drain-Source On Resistance	I_S = 10mA V_{ANALOG} = ±10V	70	70	100	80	80	100	Ω
$r_{DS(ON)}$	Channel-to-Channel $r_{DS(ON)}$ Match			25 (typ)			30 (typ)		Ω
V_{ANALOG}	Min. Analog Signal Handling Capability			±15 (typ)			±15 (typ)		V
$I_{D(OFF)}$	Switch OFF Leakage Current	V_{ANALOG} = −14V to +14V		±1	50	1	±2	50	nA
$I_{S(OFF)}$	Switch OFF Leakage Current	V_{ANALOG} = −14V to +14V		±1	50	1	±2	50	nA
$I_{D(ON)}$ + $I_{S(ON)}$	Switch ON Leakage Current	V_D = V_S = −14V to +14V		±1	100	1	±2	100	nA
t_{on}	Switch "ON" Time See Note 3	R_L = 1kΩ, V_{ANALOG} = −10V to +10V See Fig. 3		0.7			0.8		μs
t_{off}	Switch "OFF" Time	R_L = 1kΩ, V_{ANALOG} = −10V to +10V See Fig. 3		0.25			0.4		μs
$Q_{(INJ.)}$	Charge Injection	See Fig. 4		5 (typ)			10 (typ)		mV
OIRR	Min. Off Isolation Rejection Ratio	f = 1MHz, R_L = 100Ω, C_L ≤ 5pF See Fig. 5		54 (typ)			50 (typ)		dB
I_{V1}	+ Power Supply Quiescent Current	V_{IN} = 0V or V_{IN} = 5V	250	200	150	300	250	200	μA
I_{V2}	−Power Supply Quiescent Current		10	10	100	10	10	100	μA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off		54 (typ)			50 (typ)		dB

Note: All typical values have been guaranteed by characterization and are not tested.

DG200/IH5200

INTERSIL

TEST CIRCUITS

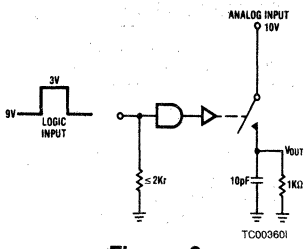


Figure 3

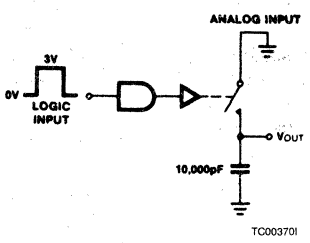


Figure 4

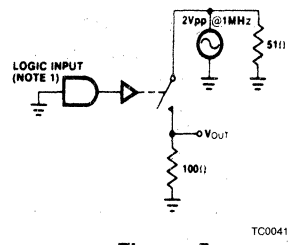
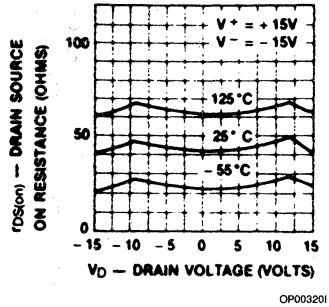


Figure 5

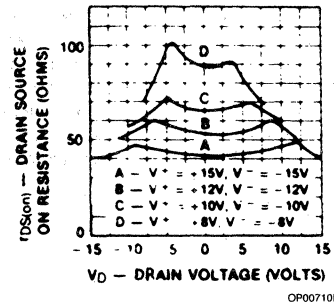
NOTE 3: All channels are turned off by high "1" logic inputs and all channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Peak input current required for transition is typically −120μA.

TYPICAL PERFORMANCE CHARACTERISTICS

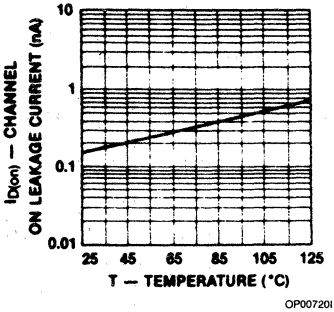
$r_{DS(on)}$ vs V_D and Temperature



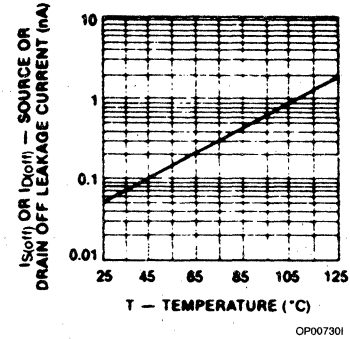
$r_{DS(on)}$ vs V_D and Power Supply Voltage



$I_{D(on)}$ vs Temperature*



$I_{S(off)}$ or $I_{D(off)}$ vs Temperature*



Note: All typical values have been guaranteed by characterization and are not tested.

APPLICATIONS

Using the V_{REF} Terminal

The DG200 has an internal voltage divider setting the TTL threshold on the input control lines for V^+ equal to +15V. The schematic shown here with nominal resistor values, gives approximately 2.4V on the V_{REF} pin. As the TTL input signal goes from +0.8V to +2.4V, Q1 and Q2 switch states to turn the switch ON and OFF.

If the power supply voltage is less than +15V, then a resistor must be added between V^+ and the V_{REF} pin, to restore +2.4V at V_{REF}. The table shows the value of this resistor for various supply voltages, to maintain TTL compatibility. If CMOS logic levels on a +5V supply are being used, the threshold shifts are less critical, but a separate column of suitable values is given in the table. For logic swings of −5V to +5V, no resistor is needed.

In general, the "low" logic level should be < 0.8V to prevent Q1 and Q2 from both being ON together (this will cause incorrect switch function). With open collector logic, and a low value of pull-up resistor, the logic "low" level can be above 0.8V. In this case, INTERSIL can supply parts with thresholds > 1.5V, allowing the user to define the "low" as < 1.5V (consult factory). The V_{REF} point should be set at least 2.6V above this "low" state, or to > 4.1V. An external resistor of 27kΩ between V^+ and V_{REF} is required, for a +15V supply.

V^+ Supply (V)	TTL Resistor (kΩ)	CMOS Resistor (kΩ)
+15	–	–
+12	100	–
+10	51	–
+9	(34)	34
+8	(27)	27
+7	18	18

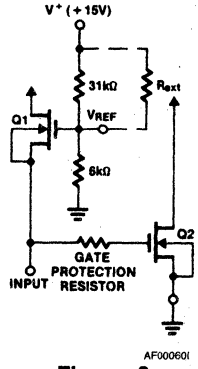


Figure 6.

Note: All typical values have been guaranteed by characterization and are not tested.

DG201/IH5201
Quad SPST CMOS Analog Switch

INTERSIL

GENERAL DESCRIPTION

The DG201/IH5201 solid-state analog switches are designed using an improved, high-voltage CMOS monolithic technology. They provide performance advantages not previously available from solid-state switches. Destructive latch-up of solid-state analog gates has been eliminated by INTERSIL's CMOS technology.

The DG201 is completely specification and pin-out compatible with the industry standard device, while the IH5201 offers significantly enhanced specifications with respect to ON and OFF leakage currents, switching times, and supply current.

FEATURES

- **Switches Greater Than $28V_{p-p}$ Signals With ±15V Supplies**
- **Break-Before-Make Switching t_{off} = 250ns, t_{on} = Typically 500ns**
- **TTL, DTL, CMOS, PMOS Compatible**
- **Non-Latching With Supply Turn-Off**
- **Complete Monolithic Construction**
- **Industry Standard (DG201)**
- **Improved Performance Version IH5201**

ORDERING INFORMATION

INDUSTRY STANDARD PART NUMBER	IMPROVED SPEC PART NUMBER	TEMPERATURE RANGE	PACKAGE
DG201AK	IH5201MJE	-55°C to +125°C	16-Pin CERDIP
DG201BK	IH5201IJE	-25°C to +85°C	16-Pin CERDIP
DG201CJ	IH5201CPE	0°C to +70°C	16-Pin Plastic DIP

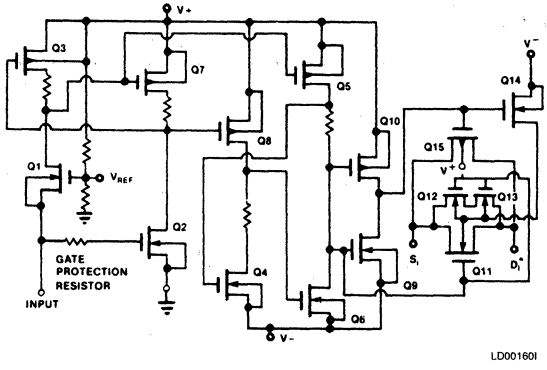


Figure 1: Functional Diagram (1/4 DG201/IH5201)

Switch Open For Logic "1" Input

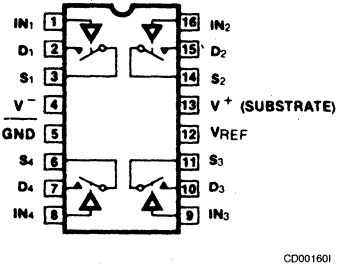


Figure 2: Pin Configuration (Outline dwgs JE, PE) DUAL-IN-LINE PACKAGE

Note: All typical values have been guaranteed by characterization and are not tested.

DG201/IH5201

INTERSIL

ABSOLUTE MAXIMUM RATINGS

V^+ to V^- ..... < 33V
V^+ to V_D ..... < 30V
V_D to V^- ..... < 30V
V_D to V_S ..... < ±22V
V_{REF} to V^- ..... < 33V
V_{REF} to V_{IN} ..... < 30V
V_{REF} to GND ..... < 20V

V_{IN} to GND ..... < 20V
Current (Any Terminal) ..... < 30mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) .....300°C
Power Dissipation 450mW
Derate 6mW/°C Above 70°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DG201 ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = +15V, V^- = −15V)

PER CHANNEL		TEST CONDITIONS	MIN/MAX LIMITS						UNIT
			MILITARY			COMMERCIAL			
SYMBOL	CHARACTERISTIC		−55°C	+25°C	+125°C	0°C	+25°C	+70°C/ +85°C	
$I_{IN(ON)}$	Input Logic Current	V_{IN} = 0.8V See Note 1	10	±1	10	±1	±1	10	µA
$I_{IN(OFF)}$	Input Logic Current	V_{IN} = 2.4V See Note 1	10	±1	10	±1	±1	10	µA
$R_{DS(ON)}$	Drain-Source On Resistance	I_S = 10mA V_{ANALOG} = ±10V	80	80	125	100	100	125	Ω
$R_{DS(ON)}$	Channel to Channel $R_{DS(ON)}$ Match			25 (typ)			30 (typ)		Ω
V_{ANALOG}	Analog Signal Handling Capability			±15 (typ)			±15 (typ)		V
$I_{D(OFF)}$	Switch OFF Leakage Current	V_{ANALOG} = −14V to +14V		±1	100		±5	100	nA
$I_{S(OFF)}$	Switch OFF Leakage Current	V_{ANALOG} = −14V to +14V		±1	100		±5	100	nA
$I_{D(ON)}$ + $I_{S(ON)}$	Switch ON Leakage Current	V_D = V_S = ±14V		±2	200		±5	200	nA
t_{on}	Switch "ON" Time See Note 2	R_L = 1kΩ, V_{ANALOG} = −10V to +10V See Figure 3		1.0			1.0		µs
t_{off}	Switch "OFF" Time See Note 2	R_L = 1kΩ, V_{ANALOG} = −10V to +10V See Figure 3		0.5			0.5		µs
$Q_{(INJ.)}$	Charge Injection	See Figure 4		15 (typ)			20 (typ)		mV
OIRR	Min. Off Isolation Rejection Ratio	f = 1MHz, R_L = 100Ω, C_L ≤ 5pF See Figure 5		54 (typ)			50 (typ)		dB
$I_{\bar{Q}}^{+}$	+ Power Supply Quiescent Current	V_{IN} = 0V to 5V	2000	1000	2000	2000	1000	2000	µA
$I_{\bar{Q}}$	−Power Supply Quiescent Current		2000	1000	2000	2000	1000	2000	µA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off		54 (typ)			50 (typ)		dB

NOTE 1: Typical values are for design aid only, not guaranteed and not subject to production testing.

Note: All typical values have been guaranteed by characterization and are not tested.

DG201/IH5201

INTERSIL

TEST CIRCUITS

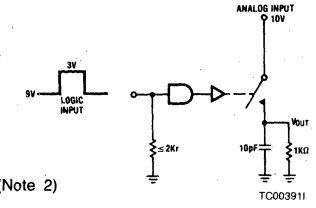


Figure 3

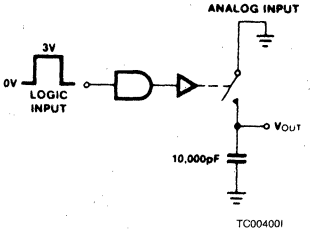


Figure 4

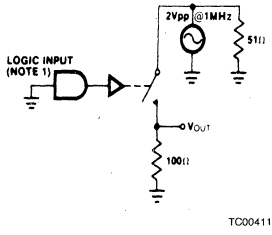


Figure 5

NOTE 2: All channels are turned off by high "1" logic inputs and all channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Peak input current required for transition is typically $-120\mu A$.

IH5201 ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = +15V$, $V^- = -15V$)

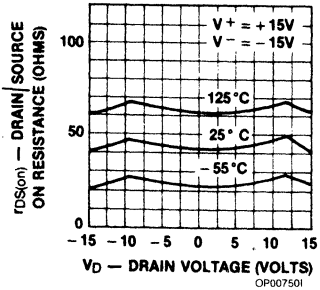
PER CHANNEL		TEST CONDITIONS	MIN/MAX LIMITS						UNIT
			MILITARY			COMMERCIAL			
SYMBOL	CHARACTERISTIC		-55°C	+25°C	+125°C	0°C	+25°C	+70°C/ +85°C	
$I_{IN(ON)}$	Input Logic Current	$V_{IN} = 0.8V$	1	1	10	1	1	10	μA
$I_{IN(OFF)}$	Input Logic Current	$V_{IN} = 2.4V$	1	1	10	1	1	10	μA
$R_{DS(ON)}$	Drain-Source On Resistance	$I_S = 10mA$ $V_{ANALOG} = \pm 10V$	75	75	100	100	100	125	Ω
$R_{DS(ON)}$	Channel to Channel $R_{DS(ON)}$ Match			25 (typ)			30 (typ)		Ω
V_{ANALOG}	Analog Signal Handling Capability			±15 (typ)			±15 (typ)		V
$I_{D(OFF)}$/ $I_{S(OFF)}$	Switch OFF Leakage Current	$V_{ANALOG} = -14V$ to $+14V$		±0.5	50		±2	50	nA
$I_{D(ON)}$ + $I_{S(ON)}$	Switch ON Leakage Current	$V_D = V_S = \pm 14V$		±0.5	100		±2	100	nA
t_{on}	Switch "ON" Time See Note 2	$R_L = 1k\Omega$, V_{ANALOG} $= -10V$ to $+10V$ See Figure 3		0.7			0.8		μs
t_{off}	Switch "OFF" Time See Note 2	$R_L = 1k\Omega$, V_{ANALOG} $= -10V$ to $+10V$ See Figure 3		0.35			0.4		μs
$Q_{(INJ.)}$	Charge Injection	See Fig. 4		5 (typ)			10 (typ)		mV
OIRR	Min. Off Isolation Rejection Ratio	$f = 1MHz$, $R_L = 100\Omega$, $C_L \leq 5pF$ See Figure 5, (Note 1)		54 (typ)			50 (typ)		dB
I_Q^+	+ Power Supply Quiescent Current	$V_{IN} = 0V$ to $5V$	1000	750	600	1500	1000	1000	μA
I_Q^-	-Power Supply Quiescent Current		10	10	100	20	20	200	μA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off (Note 1)		54 (typ)			50 (typ)		dB

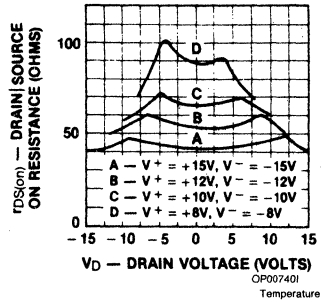
NOTE: Pull Down resistor must be $\leq 2k\Omega$
NOTE: Typical values are for design aid only, not guaranteed and not subject to production testing.

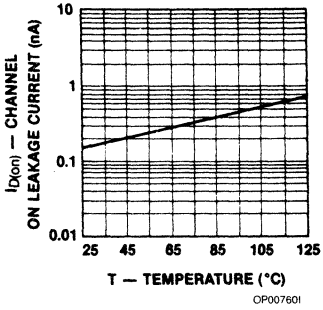
Note: All typical values have been guaranteed by characterization and are not tested.

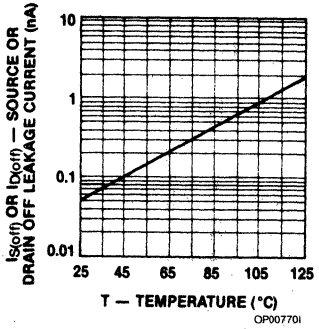
DG201/IH5201

TYPICAL PERFORMANCE CHARACTERISTICS









APPLICATIONS

Using the V_{REF} Terminal

The DG201 has an internal voltage divider that sets the TTL threshold on the input control lines for $V^+ = 15V$. The schematic is shown here, with nominal resistor values, giving approximately 2.4V on the V_{REF} pin. As the TTL input signal goes from +0.8V to +2.4V, Q1 and Q2 switch states to turn the switch ON and OFF.

If the power supply voltage is less than +15V, then a resistor needs to be added between V^+ and V_{REF} pin, to restore +2.4V at V_{REF}. The table shows the value of this resistor for various supply voltages, to maintain TTL compatibility. If CMOS logic levels with a +5V supply are being used, the threshold shifts are less critical, but a separate column of suitable values is given in the table. For logic swings of −5V to +5V, no resistor is needed.

In general, the "low" logic level should be < 0.8V to prevent Q1 and Q2 from both being ON together (this will cause incorrect switch function). With open collector logic, and a low value of pull-up resistor, the logic 'low' level can be above 0.8V. In this case, INTERSIL can supply parts with thresholds > 1.5V(consult factory). The V_{REF} point should be set at least 2.6V above this "low" state, or to > 4.1V. An external resistor of 27kΩ and V_{REF} is required, for a +15V supply.

V^+ Supply (V)	TTL Resistor (kΩ)	CMOS Resistor (kΩ)
+15	–	–
+12	100	–
+10	51	–
+9	(34)	34
+8	(27)	27
+7	18	18

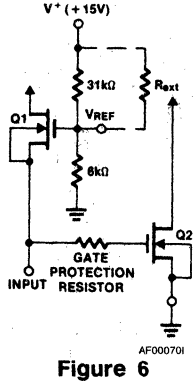


Figure 6

Note: All typical values have been guaranteed by characterization and are not tested.

DG211/DG212
SPST 4-Channel Analog Switch

INTERSIL

GENERAL DESCRIPTION

The DG211 and DG212 are low cost, CMOS monolithic, QUAD SPST analog switches. These can be used in general purpose switching applications for communications, instrumentation, process control and computer peripheral equipment. Both devices provide true bidirectional performance in the ON condition and will block signals to 30V peak-to-peak in the OFF condition. The DG211 and DG212 differ only in that the digital control logic is inverted, as shown in the truth table.

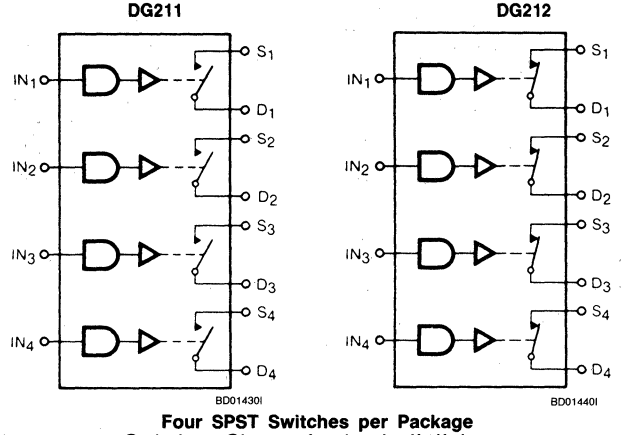
DG211 and DG212 are available in a 16-pin Dual-In-Line plastic package and are rated for operation over 0°C to 70°C.

FEATURES

- **Switches ±15V Analog Signals**
- **TTL Compatibility**
- **Logic Inputs Accept Negative Voltages**
- **$R_{ON} \leq 175$ Ohm**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
DG211CJ	0°C to +70°C	16-Pin Plastic DIP
DG212CJ	0°C to +70°C	16-Pin Plastic DIP



Four SPST Switches per Package
Switches Shown for Logic "1" Input

Truth Table

LOGIC	DG211	DG212
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8V
Logic "1" ≥ 2.4V

Figure 1: Functional Diagrams

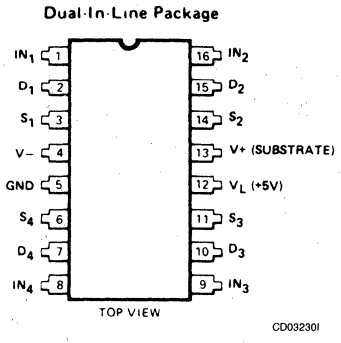


Figure 2. Pin Configuration

307020-001

Note: All typical values have been guaranteed by characterization and are not tested.

DG211/DG212

INTERSIL

ABSOLUTE MAXIMUM RATINGS

V^+ to V^- 36V
V_{IN} to Ground ..... V^-, V^+
V_L to Ground ..... −0.3V, 25V
V_S or V_D to V^+ ..... 0, −36V
V_S or V_D to V^- 0, 36V
V^+ to Ground 25V
V^- to Ground ..... −25V
Current, Any Terminal Except S or D 30mA
Continuous Current, S or D 20mA
Peak Current, S or D
(Pulsed at 1msec, 10% duty cycle max) 70mA
Storage Temperature ..... −65°C to +125°C
Operating Temperature ..... 0°C to +70°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Power Dissipation (Package)*
16 Pin Plastic DIP** 470mW

*Device mounted with all leads soldered or welded to PC board.
**Derate 6.5mW/°C above 25°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	TEST CONDITIONS V_1 = +15V, V_2 = −15V, V_L = +5V, GND		LIMITS MIN[1]	LIMITS TYP[2]	LIMITS MAX	UNIT
SWITCH							
V_{ANALOG}	Analog Signal Range	V^- = −15V, V_L = +5V		−15		15	V
$R_{DS(ON)}$	Drain-Source On Resistance	V_D = ±10V, V_{IN} = 2.4V — DG212 I_S = 1mA, V_{IN} = 0.8V — DG211			115	175	Ω
$I_{S(off)}$	Source OFF Leakage Current	V_{IN} = 2.4V DG211 V_{IN} = 0.8V DG212	V_S = 14V, V_D = −14V		0.01	5.0	nA
			V_S = −14V, V_D = 14V	−5.0	−0.02		
$I_{D(off)}$	Drain OFF Leakage Current		V_D = 14V, V_S = −14V		0.01	5.0	
			V_D = −14V, V_S = 14V	−5.0	−0.02		
$I_{D(ON)}$	Drain ON Leakage Current[3]	V_S = V_D = −14V, V_{IN} = 0.8V, DG211 V_{IN} = 2.4V, DG212			0.1	5.0	
				−5.0	−0.15		
INPUT							
I_{INH}	Input Current With Input Voltage High	V_{IN} = 2.4V		−10	−0.0004		μA
		V_{IN} = 15V			0.003	1.0	
I_{INL}	Input Current With Input Voltage Low	V_{IN} = 0V		−1.0	−0.0004		
DYNAMIC							
t_{on}	Turn-ON Time	See Switching Time Test Circuit[5] V_S = 10V, R_L = 1kΩ, C_L = 35pF			460	1000	ns
t_{off1}	Turn-OFF Time				360	500	
t_{off2}					450		
$C_{S(off)}$	Source OFF Capacitance	V_S = 0V, V_{IN} = 5V, f = 1MHz[2]			5		pF
$C_{D(off)}$	Drain OFF Capacitance	V_D = 0V, V_{IN} = 5V, f = 1MHz[2]			5		
$C_{D+S(on)}$	Channel ON Capacitance	V_D = V_S = 0V, V_{IN} = 0V, f = 1MHz[2]			16		
OIRR	OFF Isolation[4]	V_{IN} = 5V, R_L = 1kΩ, C_L = 15pF, V_S = 1VRMS, f = 100kHz[2]			70		dB
CCRR	Crosstalk (Channel to Channel)				90		
SUPPLY							
I^+	Positive Supply Current	V_{IN} = 0 and 2.4V			.1	10	μA
I^-	Negative Supply Current				.1	10	
I_L	Logic Supply Current				.1	10	

NOTES:
1. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
2. For design reference only, not 100% tested.
3. $I_{D(on)}$ is leakage from driver into "ON" switch.
4. OFF Isolation = $20\log\frac{V_S}{V_D}$, V_S = input to OFF switch, V_D = output.
5. Switching times only sampled.

Note: All typical values have been guaranteed by characterization and are not tested.

DG211/DG212

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note the V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

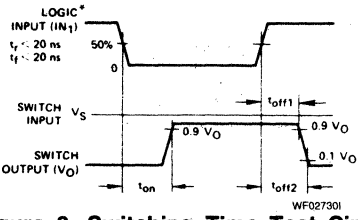


Figure 3: Switching Time Test Circuit
Logic shown for DG211. Invert for DG212.

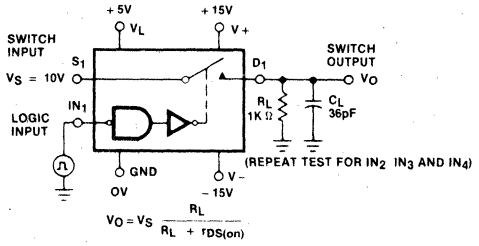


Figure 4: Switching Time Test Circuit

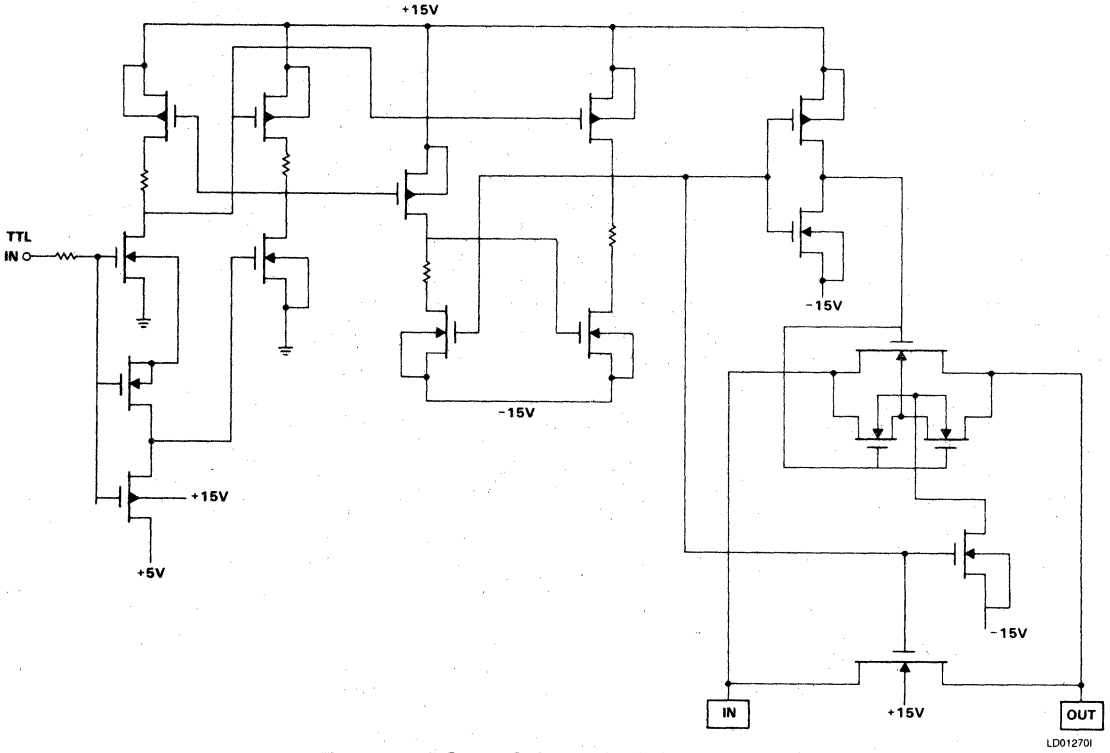


Figure 5: DG212 Schematic (1/4 as shown)

Note: All typical values have been guaranteed by characterization and are not tested.

DGM181-191
High-Speed CMOS Analog Switch

GENERAL DESCRIPTION

The DGM181 family of CMOS monolithic switches utilizes intersil's latch-free junction isolated processing to combine the speed of the hybrid DG181 family with the reliability and low power consumption of a monolithic CMOS construction. These devices, therefore, are a cost effective replacement for the DG181 family.

The DGM181 family has a high state threshold of 2.4V; and a low state of +0.8V.

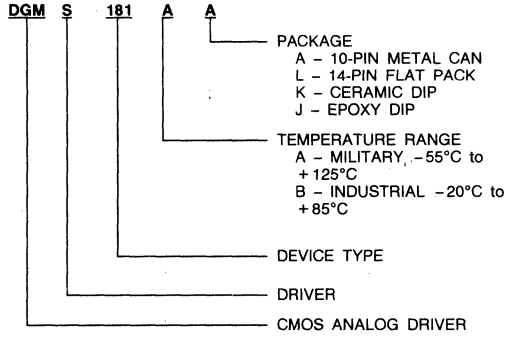
Very low quiescent power is dissipated in either the ON or OFF state of the switch. Maximum power supply current is 10μA from any supply, and typical quiescent currents are in the 10nA range. OFF leakages are typically less than 200pA at 25°C.

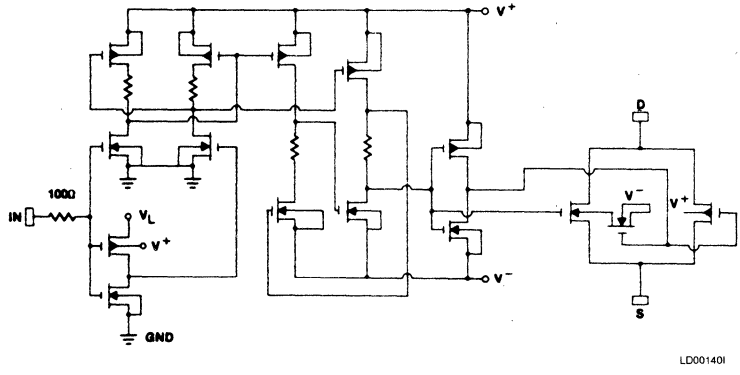
FEATURES

- **Pin and Function Replacement for DG181 Family**
- **Meets or Exceeds All DG181 Family Specifications With Monolithic Reliability**
- **Low Power Consumption**
- **1nA Leakage From Signal Channel in Both ON and OFF States**
- **TTL, DTL, RTL Direct Drive Capability**
- **t_{on}, t_{off} < 150ns, Break-Before-Make Action**
- **Crosstalk and Open Load Switch Isolation > 50dB at 10MHz (75Ω Load)**

ORDERING INFORMATION

TYPE	STANDARD PART NUMBER	STANDARD PART NUMBER	$r_{DS(on)}$ MAX AT 25°C
Dual SPST	DGM181BX	DGMS181BX	50
	DGM182AX	DGMS182AX	50
	DGM182BX	DGMS182BX	75
Dual DPST	DGM184BX	DGMS181BX	50
	DGM185AX	DGMS185AX	50
	DGM185BX	DGMS185BX	75
SPDT	DGM187BX	DGMS187BX	50
	DGM188AX	DGMS188AX	50
	DGM188BX	DGMS188BX	75
Dual SPDT	DGM190BX	DGMS190BX	50
	DGM191AX	DGMS191AX	50
	DGM191BX	DGMS191BX	75





NOTE: 1/2 of DGM182

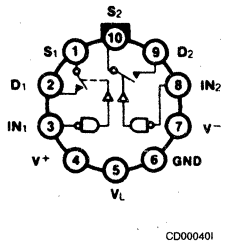
Figure 1: Functional Diagram (Typical Channel)

Note: All typical values have been guaranteed by characterization and are not tested.

DGM181-191

DUAL SPST (DGM181, 182)

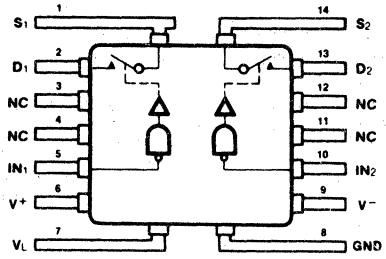
Metal Can Package



CD00040I

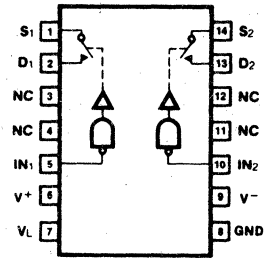
(OUTLINE DWG TO-100)

Flat Package (FD-2)



CD00050I

Dual-In-Line Package



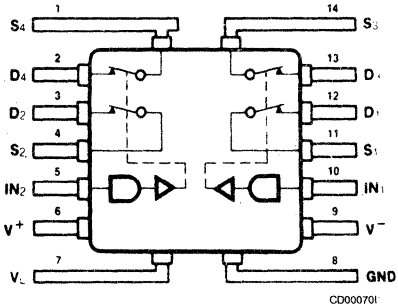
CD00060I

(OUTLINE DWGS DD, PD)

SWITCH STATES ARE FOR LOGIC "1" INPUT

DUAL DPST (DGM184, 185)

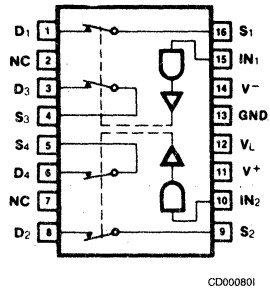
Flat Package



CD00070I

(OUTLINE DWG FD-2)

Dual-In-Line Package



CD00080I

(OUTLINE DWGS DE, PE)

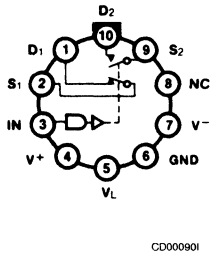
SWITCH STATES ARE FOR LOGIC "1" INPUT

Figure 2: Pin Configuration and Switching State Diagram

Note: All typical values have been guaranteed by characterization and are not tested.

SPDT (DGM187, 188)

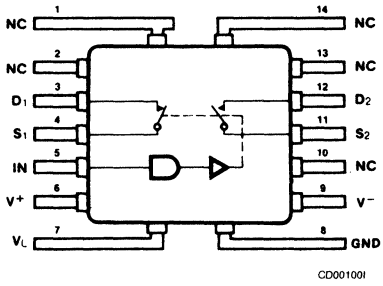
Metal Can Package



CD00090I

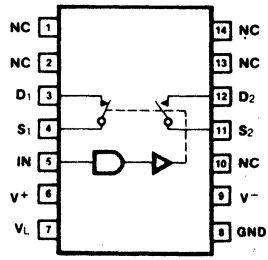
(OUTLINE DWG TO-100)

Flat Package (FD-2)



CD00100I

Dual-In-Line Package



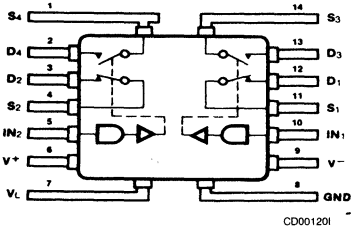
CD00110I

(OUTLINE DWGS DD, PD)

SWITCH STATES ARE FOR LOGIC "1" INPUT

DUAL SPDT (DGM190, 191)

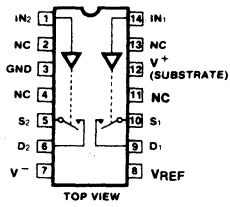
Flat Package



CD00120I

(OUTLINE DWG FD-2)

Dual-In-line Package



CD00130I

(OUTLINE DWGS DE, PE)

SWITCH STATES ARE FOR LOGIC "1" INPUT

Figure 2: Pin Configuration and Switching State Diagram (Cont.)

Note: All typical values have been guaranteed by characterization and are not tested.

DGM181-191

ABSOLUTE MAXIMUM RATINGS

V^+–V^- 36V
V^-–V_D 33V
V_D–V^- 33V
V_D–V_S ..... ±22V
V_L–V^- 36V
V_L–V_{IN} 30V
V_L–V_{GND} 20V
V_{IN}–V_{GND} 20V
GND–V^- 27V
GND–V_{IN} 20V
Current (Any Terminal) 30mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Power Dissipation* ..... 450 (TW), 750 (FLAT), 825(DIP)mW

*Device mounted with all leads welded or soldered to PC board. Derate 6mW/°C (TW); 10mW/°C (FLAT); 11mW/°C (DIP) above 75°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS ($V^+ = +15V$, $V^- = -15V$, $V_L = 5V$, unless noted)

PARAMETER	DEVICE NO.	TEST CONDITIONS (Note 1)	A SERIES			B SERIES			UNIT
			−55°C	+25°C	+125°C	−20°C	+25°C	+85°C	
SWITCH									
$I_{S(off)}$	DGM181, 184, 187, 190	$V_S = 7.5V$, $V_D = -7.5V$, V_{IN} = "OFF"		±1	100		±2.0	200	nA
	DGM182, 185, 188, 191	$V_S = 10V$, $V_D = -10V$, V_{IN} = "OFF"		±1	100		±2	200	nA
$I_{D(off)}$	DGM181, 184, 187, 190	$V_S = 7.5V$, $V_D = -7.5V$, V_{IN} = "OFF"		±1	100		±2	200	nA
	DGM182, 185, 188, 191	$V_S = 10V$, $V_D = -10V$, V_{IN} = "OFF"		±1	100		±2	200	nA
$I_{D(on)} + I_{S(on)}$	DGM181, 184, 187, 190	$V_D = V_S = -7.5V$, V_{IN} = "ON"		±2	±200		±5	500	nA
	DGM182, 185, 188, 191	$V_D = V_S = -10V$, V_{IN} = "ON"		±2	±200		±5	500	nA
INPUT									
I_{INL}	ALL	$V_{IN} = 0V$		±1.0	20		10	20	µA
I_{INH}	ALL	$V_{IN} = 5V$		±1.0	20		10	20	µA
DYNAMIC									
t_{on}	DGM181, 184, 187, 190 DGM182, 185, 188, 191	See switching time test circuit		450			500		ns
t_{off}	ALL			250			275		
$C_{S(off)}$	DGM181, 182, 184, 185, 187, 188, 190, 191	$V_S = -5V$, $I_D = 0$, f = 1MHz	5pF typical						pF
$C_{D(off)}$		$V_D = +5V$, $I_S = 0$, f = 1MHz	6pF typical						
$C_{D(on)} + C_{S(on)}$		$V_D = V_S = 0$, f = 1MHz	11pF typical						
OFF Isolation		$R_L = 75\Omega$, $C_L = 3pF$	Typically > 50dB at 10MHz						
SUPPLY									
I^+	ALL	$V_{IN} = 5V$	10	10	100		100		µA
I^-	ALL		10	10	100		100		
I_L	ALL		10	10	100		100		
I_{GND}	ALL		10	10	100		100		
I^+	ALL	$V_{IN} = 0V$	10	10	100		100		
I^-	ALL		10	10	100		100		
I_L	ALL		10	10	100		100		
I_{GND}	ALL		10	10	100		100		

Note 1: See Switching State Diagrams for V_{IN} and V_{IN} "OFF" Test Conditions.

Note: All typical values have been guaranteed by characterization and are not tested.

DGM181-191

ELECTRICAL CHARACTERISTICS MAXIMUM RESISTANCES $r_{DS(ON)}$

DEVICE NUMBER	CONDITIONS (Note 1) $V^+ = 15V, V^- = -15V, V_L = 5V$		MILITARY TEMPERATURE			INDUSTRIAL TEMPERATURE			UNIT
			−55°C	+25°C	+125°C	−20°C	+25°C	+85°C	
DGM181	$V_D = -7.5V$		–	–	–	50	50	75	Ω
DGM182	$V_D = -10V$		50	50	75	75	75	100	Ω
DGM184	$V_D = -7.5V$		30	30	60	50	50	75	Ω
DGM185	$V_D = -10V$	$I_S = -10mA$	50	50	75	75	75	100	Ω
DGM187	$V_D = -7.5V$	V_{IN} = "ON"	30	30	60	50	50	75	Ω
DGM188	$V_D = -10V$		50	50	75	75	75	100	Ω
DGM190	$V_D = -7.5V$		30	30	60	50	50	75	Ω
DGM191	$V_D = -10V$		50	50	75	75	75	100	Ω

APPLICATION COMMENT: The charge injection in these switches is of opposite polarity to that of the standard DG180 family, but considerably smaller.

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

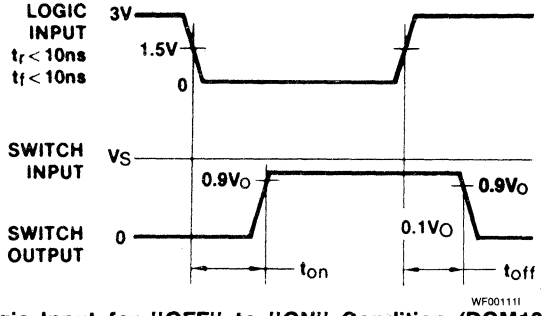


Figure 3: Logic Input for "OFF" to "ON" Condition (DGM181/182 Shown)

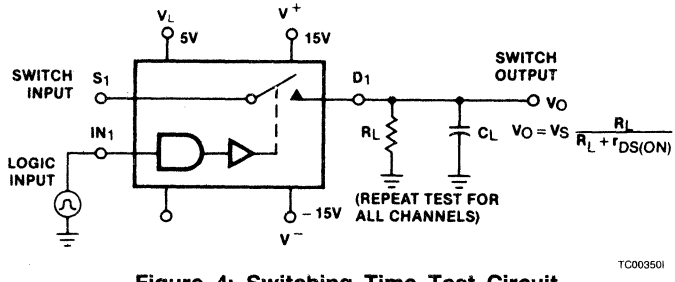


Figure 4: Switching Time Test Circuit

Note: All typical values have been guaranteed by characterization and are not tested.

DGM181-191

SWITCH STATES

DUAL SPST DGM181/182

TEST CONDITIONS

DGM181/182	
V_{IN} "ON" = 0.8V	All Channels
V_{IN} "OFF" = 2.4V	All Channels

SPDT DGM187/188

TEST CONDITIONS

DGM187/188	
V_{IN} "ON" = 2.4V	Channel 1
V_{IN} "ON" = 0.8V	Channel 2
V_{IN} "OFF" = 2.4V	Channel 2
V_{IN} "OFF" = 0.8V	Channel 1

DUAL DPST DGM184/185

TEST CONDITIONS

DGM184/185	
V_{IN} "ON" = 2.4V	All Channels
V_{IN} "OFF" = 0.8V	All Channels

DUAL SPDT DGM190/191

TEST CONDITIONS

DGM190/191	
V_{IN} "ON" = 2.4V	Channels 1 & 2
V_{IN} "ON" = 0.8V	Channels 3 & 4
V_{IN} "OFF" = 2.4V	Channels 3 & 4
V_{IN} "OFF" = 0.8V	Channels 1 & 2

Note: All typical values have been guaranteed by characterization and are not tested.

G115/G123
4 and 6-Channel MOSFET Switch

GENERAL DESCRIPTION

These switches may be connected directly to the INTERSIL switch-driver D123 series without the need of any interfacing components, and are internally protected by a Zener diode integrated on the silicon chip. A MOSFET used as a current source provides an active pull-up for faster switching capability. The active pull-up FET can be disabled without sacrificing the Zener protection of the gates.

FEATURES

- **Integrated MOSFET Constant-Current Sources for Open Collector Driver Pull-up**
- **Integrated Zener Diode Protection for Both Positive and Negative Spike Protection**
- **P-Channel Enhancement-Type Switches**

ORDERING INFORMATION

G115 A K

Package
- J — Plastic DIP
- K — CERDIP
- L — Flat Package
- P — Ceramic DIP (Special Order Only)

Temperature Range
- A — Military (−55°C to +125°C)
- B — Industrial (−20°C to +85°C)
- C — Commercial (0°C to +70°C)

Device Chip Type

NOTE: Plastic package available in commercial and industrial temperature ranges only.

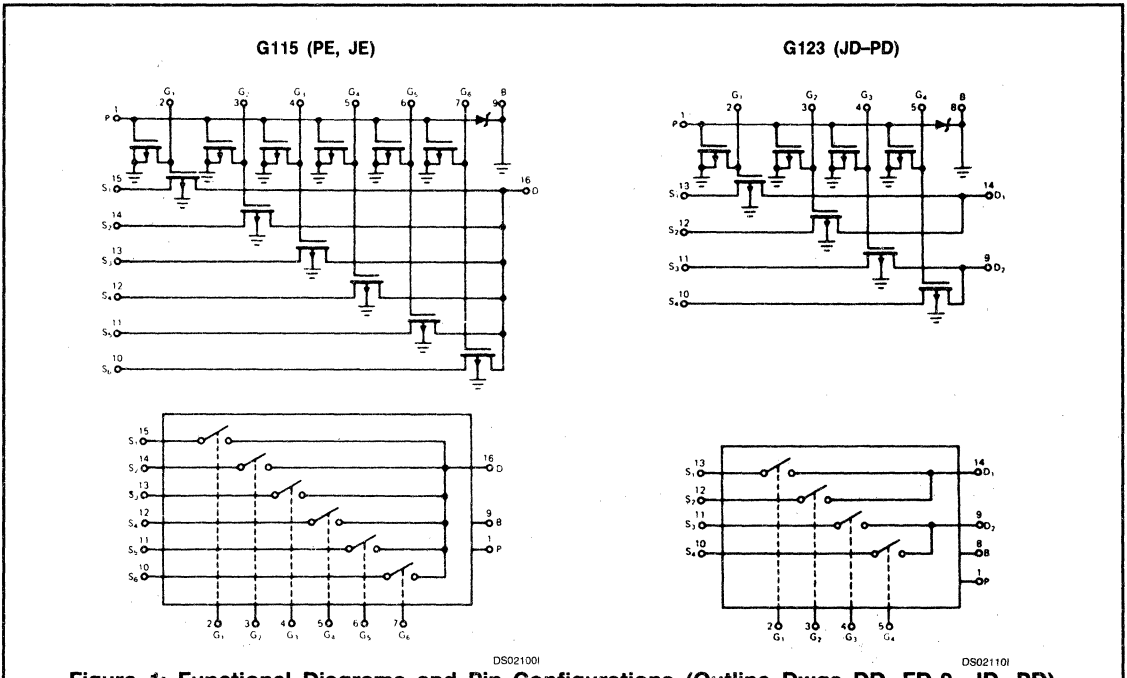


Figure 1: Functional Diagrams and Pin Configurations (Outline Dwgs DD, FD-2, JD, PD)

NOTE: G115 Built-in 16-Pin DIP Only.

Note: All typical values have been guaranteed by characterization and are not tested.

G115/G123

INTERSIL

ABSOLUTE MAXIMUM RATINGS (25°C)

Source Current (I_S) 100mA
Drain Current (I_D) 100mA
Gate Current (I_G) 5mA
Pull-up Control Current (I_P) 100μA
Body to Source ($V_B - V_S$) ..... -2V to +25V
Body to Drain ($V_B - V_D$) ..... -2V to +25V
Body to Gate ($V_B - V_G$) ..... +35V
Body to Pull-up ($V_B - V_P$) ..... +35V
Power Dissipation
(derate 10mW/°C above 70°C) 750mW
Lead Temperature (Soldering, 10sec) ..... 300°C

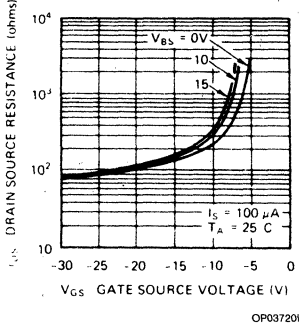
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (per channel unless noted)

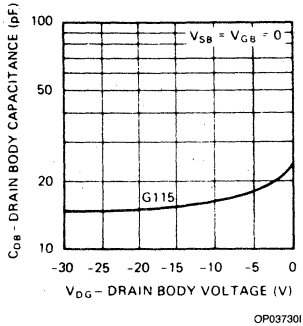
DEVICE	PARAMETER	TEST CONDITIONS		LIMITS -20°C	LIMITS 25°C	LIMITS 85°C	MIN/MAX	UNIT
G115 and G123	$R_{DS(ON)}$	V_{BD} = 0, V_{GD} = -30V	I_S =	125	125	150	Max	Ω
		V_{BD} = +10V, V_{GD} = -20V	1mA	250	250	300		
		V_{BD} = +20V, V_{GD} = -10V		500	500	600		
	$I_{D(OFF)}$	V_{DS} = -20V, V_{BS} = V_{GS} = V_{PS} = 0			-10	-500	Max	nA
	$I_{S(OFF)}$	V_{SD} = -20V, V_{BD} = V_{GD} = V_{PD} = 0			-5	-100	Max	nA
	I_{GBS}	V_{GB} = -20V, V_{DB} = V_{SB} = V_{PB} = 0			-5	-100	Max	nA
	$I_{G(ON)}$	V_{GB} = -30V, V_{PB} = -30V, V_{DB} = 0			-0.8		Min	mA
					-2.4		Max	
	$V_{GS(th)}$	I_S = -10μA, V_{DG} = 0,		-1.5	-1.5	-1.5	Min	V
		V_{BS} = V_{PS} = 0		-4	-4	-4	Max	
	BV_{DSS}	I_D = -10μA, V_{GB} = V_{BS} = V_{PS} = 0		-25	-25	-25	Min	V
	BV_{SDS}	I_S = -10μA, V_{GD} = V_{BD} = V_{PD} = 0		-25	-25	-25	Min	V
	BV_{GBS}	I_G = -10μA, V_{DB} = V_{SB} = V_{PB} = 0		-35	-35	-35	Min	V
				-110	-110	-110	Max	V
	BV_{PBS}	I_P = -10μA, V_{DB} = V_{SB} = V_{GB} = 0		-35	-35	-35	Min	V
				-110	-110	-110	Max	V
	C_{GS}, C_{GD}	V_{GB} = 0, V_{SB} = 0, V_{DB} = 0, V_{PB} = 0			3*		Typ	pF
	C_{DS}	f = 1MHz, Body Guarded			0.4*		Typ	pF
G115	G_{DB}	V_{DB} = -5V, V_{SB} = V_{GB} = V_{PB} = 0 f = 1MHz			18*		Typ	pF
G123					9*		Typ	pF
Both	C_{SB}	V_{SB} = -5V, V_{DB} = 0, V_{GB} = V_{PB} = 0 f = 1MHz			3.5*		Typ	pF

*Typical values not garanteed or tested in production

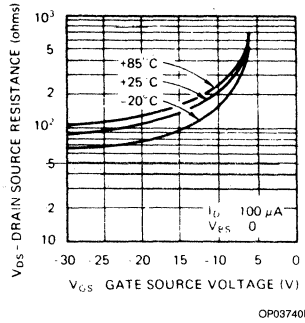
TYPICAL PERFORMANCE CHARACTERISTICS



OP03720I



OP03730I



OP03740I

Note: All typical values have been guaranteed by characterization and are not tested.

G115/G123

APPLICATION TIPS

Description of Analog Switch

Single Channel

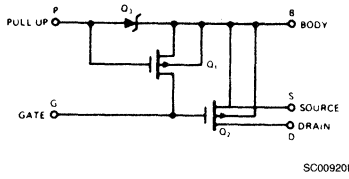


Figure 3

G-Terminal — This is the control terminal of the switch. The voltage at this terminal determines the conduction state of Q_2. To insure conduction of Q_2 when voltages between ±10V are switched, the gate voltage (V_G) should be at least 10V more negative than the most negative voltage to be switched (−10V). Therefore, V_G should go to −20V. To insure turn-off V_G should not be less than the most positive voltage to be switched, +10V. For convenience the same potential as the body could be used.

B-Terminal — This terminal is connected to the body (substrate) of the chip and must be maintained at a voltage that is equal to or greater than the most positive voltage to be switched. This is to ensure that the drain-to-body or the source-to-body junctions do not become forward biased.

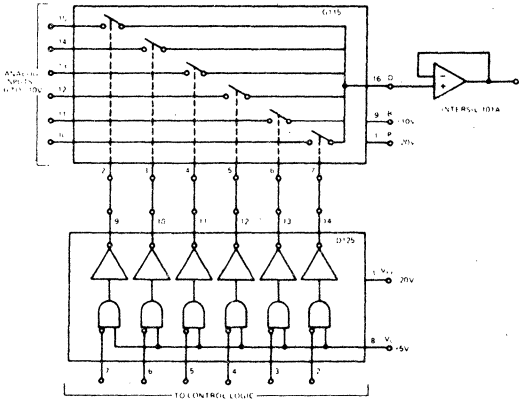
P-Terminal — The potential, with respect to the body, at this terminal determines the gate-to-source voltage of Q_1 which determines the amount of drain current available for driver-collector pull-up. Shorting terminal P to B prevents Q_1 and Q_3 from conducting, but still allows the body-to-drain junction of Q_1 to act as a forward biased diode for positive gate voltages, and to act as a Zener diode for negative voltages which exceed BV_{DSS} (−30 to −90V) for protecting the gate of Q_2.

D-Terminal — The common point of the MOSFET switches (summing point).

S-Terminal — This is the normally-open terminal of the MOSFET switch and is normally used as the input.

APPLICATIONS

Channel Multiplexer



Dual Current-to-Voltage Converter With Range Programming

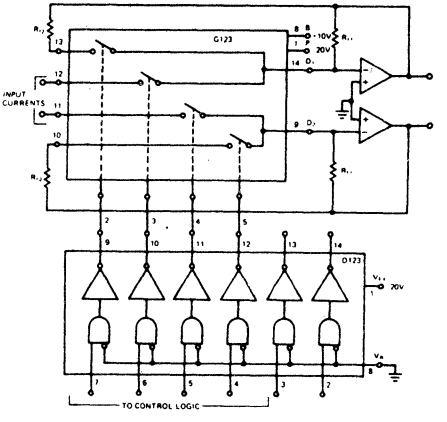


Figure 4

Note: All typical values have been guaranteed by characterization and are not tested.

G116, G118, G119
Monolithic MOSFET Switch

GENERAL DESCRIPTION

These switches may be connected directly to the INTERSIL switch-driver D123 series without need of any interfacing components. These MOSFET switches are internally protected by a Zener diode integrated on the silicon chip. A MOSFET used as a current source provides an active pull-up for faster switching. The active pull-up FET can be disabled without sacrificing the Zener protection of the gates.

FEATURES

- **P-Channel Enhancement-Type MOSFET Switches**
- **Zener Protection on All Gates**
- **With and Without Constant Current Source Pull-Up**

ORDERING INFORMATION

G116 M J

- Package
  - J – 14-pin Plastic DIP
  - K – 14-pin CERDIP
  - L – 14-pin Flat Package
  - P – 14-pin Hermetic DIP (Special Order Only)
- Temperature Range
  - A – Military (–55°C to +125°C)
  - B – Industrial (–20°C to +85°C)
- Device Chip Type

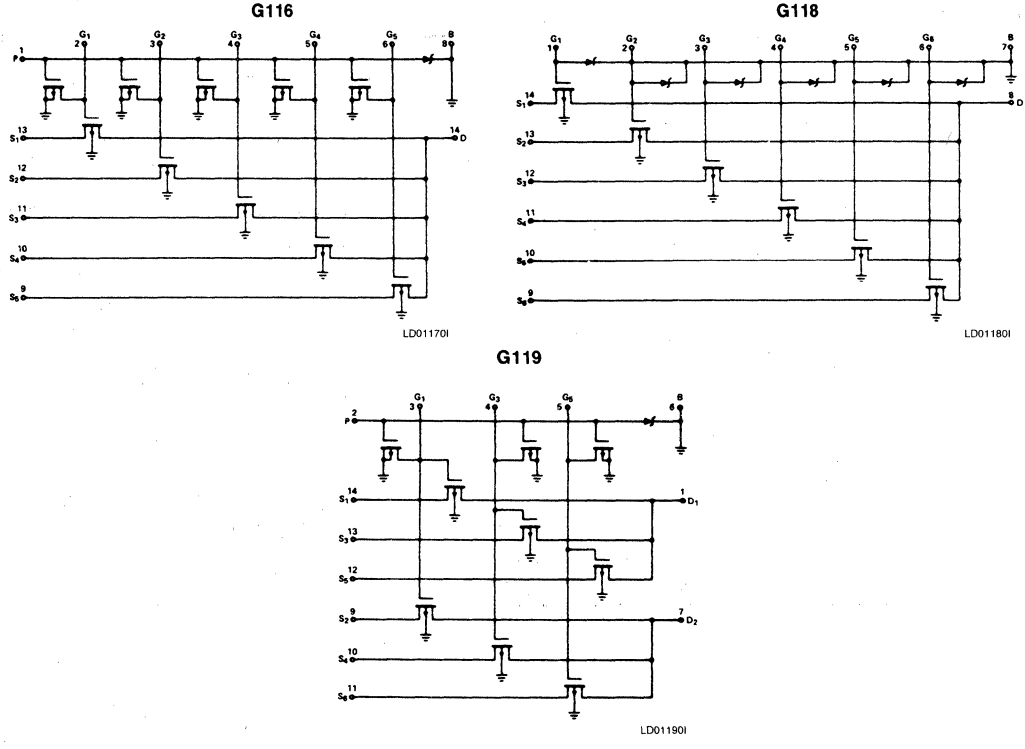


Figure 1: Functional Diagrams (Outline Dwgs PD, JD, FD-2, DD)

Note: All typical values have been guaranteed by characterization and are not tested.

G116, G118, G119

INTERSIL

ABSOLUTE MAXIMUM RATINGS (25°C)

Source Current (I_S) 100mA
Drain Current (I_D) 100mA
Control Gate Current I_G 5mA
Pull-Up Gate Current I_P 100μA
Body Voltage (V_B) to Any Terminal ..... −2 to +30V

Power Dissipation (Note) 750mW
Storage Temperature ..... −55°C to +150°C
Operating Temperature ..... −50°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70°C. For higher temperatures, derate 10mW/°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Per Channel Unless Noted)

References to pull-up gate P do not apply to G118.

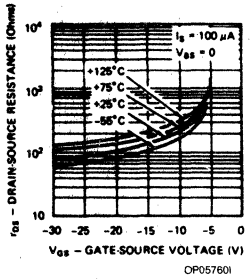
PARAMETER	TEST CONDITIONS		LIMITS					
			G116M Series		G116C Series		MIN/MAX	UNIT
			25°C	125°C	25°C	125°C		
$r_{DS(ON)}$ (Note 1)	V_{BD} = 0, V_{GD} = −30V, V_{PB} = 0	I_S = −1mA	100	125	125		Max	Ω
	V_{BD} = +10V, V_{GD} = −20V, V_{PB} = 0		200	250	250			
	V_{BD} = +20V, V_{GD} = −10V, V_{PB} = 0		450	600	600			
$I_{S(OFF)}$	V_{SD} = −20V, V_{BD} = V_{GD} = V_{PD} = 0		−0.5	−500	−1		Max	nA
$I_{D(OFF)}$	V_{DS} = −20V	G116	−2.5	−2500	−5		Max	nA
	V_{BD} = V_{GD} = V_{PD} = 0	G118	−3.0	−3000	−6			
		G119	−1.5	−1500	−3			
	V_{G1B} to V_{G5B} = 0, V_{G6B} = −30V, V_{DB} = −20V, V_{SB} = V_{PB} = 0	G117	−0.5	−500	−1		Max	nA
BV_{DSS}	I_D = −10μA, V_{GS} = V_{BS} = V_{PS} = 0		−30		−30		Min	V
BV_{SDS}	I_S = −10μA, V_{GD} = V_{BD} = V_{PD} = 0		−30		−30		Min	
BV_{GBS}	I_G = −10μA, V_{PB} = V_{SB} = V_{DB} = 0		−30		−30		Min	
			−110		−110		Max	
BV_{PBS}	I_P = −10μA, V_{GB} = V_{SB} = V_{DB} = 0		−30		−30		Min	
			−110		−110		Max	
$V_{GD(th)}$	I_S = −10μA, V_{DS} = −10V, V_{SB} = 0		−1.5		−1.5		Min	
			−4		−4		Max	
$I_{GS(ON)}$ (Note 2)	V_{GB} = −30V, V_{PB} = −30V, V_{SB} = V_{DB} = 0		−0.5		−0.3		Min	mA
			−2		−2.5		Max	
I_{GSS}	V_{GB} = −20V, V_{DS} = V_{BS} = V_{PS} = 0		−0.5	−500	−1		Max	nA
C_{GD} or C_{GS}	V_{PB} = 0, V_{BS} = 0, or V_{BD} = 0		3		3		Typ	pF
C_{SD} (Note 3)	Body Guarded, f = 1MHz		0.4		0.4		Typ	pF
C_{SB} (Note 3)	V_{PB} = V_{GB} = V_{DB} = 0, V_{SB} = −5V, f = 1MHz		−3.5		−3.5		Typ	pF
C_{DG} (Note 3)	V_{PB} = V_{GB} = V_{SB} = 0 V_{DB} = −5V, f = 1MHz	G116	18		18		Typ	pF
		G118	18		18			
		G119	10		10			
	V_{G6B} = −30V, V_{PB} = V_{SB} = 0, V_{G1B} to V_{G5B} = 0, V_{DB} = −5V, f=1MHz	G117	20		20		Typ	pF

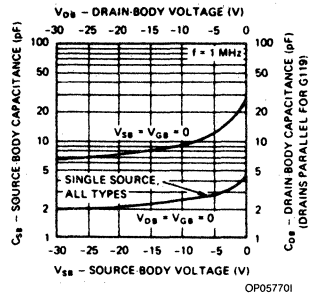
NOTES:
1. For the G117 this is the resistance from each of the source terminals (5 terminals) and the one drain terminal to the internal junction of the output MOSFETs.
2. Not applicable to G118.
3. Typical values not guaranteed or tested in production.

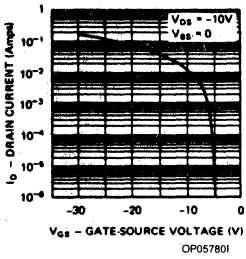
Note: All typical values have been guaranteed by characterization and are not tested.

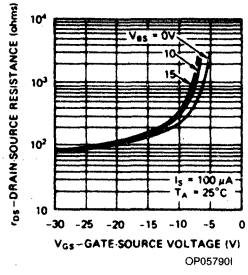
G116, G118, G119

TYPICAL PERFORMANCE CHARACTERISTICS









APPLICATION TIPS

Description of Analog Switch

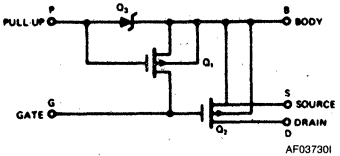


Figure 2: Single Channel

G–Terminal — This is the control terminal of the switch; the voltage at this terminal determines the conduction state of Q_2. To insure conduction of Q_2 when voltages between ±10V are switched, the gate voltage (V_G) should be at least 10V more negative than the most negative voltage to be switched (–10V). Therefore, V_G should go to –20V. To insure turn-off V_G should not be less than the most positive voltage to be switched, + 10V. For convenience the same potential as the body could be used.

B–Terminal — This terminal is connected to the body (substrate) of the chip and must be maintained at a voltage that is equal to or greater than the most positive voltage to be switched. This is to insure that the drain-to-body or the source-to-body junctions do not become forward biased.

P–Terminal — The potential, with respect to the body, at this terminal determines the gate-to-source voltage of Q_1 which determines the amount of drain current available for driver-collector pull-up. Shorting terminal P to B prevents Q_1 and Q_3 from conducting, but still allows the body-to-drain junction of Q_1 to act as a forward biased diode for positive gate voltages, and to act as a Zener diode for negative voltages which exceed BV_{DSS} (–30 to –110V) for protecting the gate of Q_2.

D–Terminal — The common point of the MOSFET switches (summing point).

S–Terminal — This is the normally-open terminal of the MOSFET switch and is normally used as the input.

Note: All typical values have been guaranteed by characterization and are not tested.

G116, G118, G119

APPLICATIONS

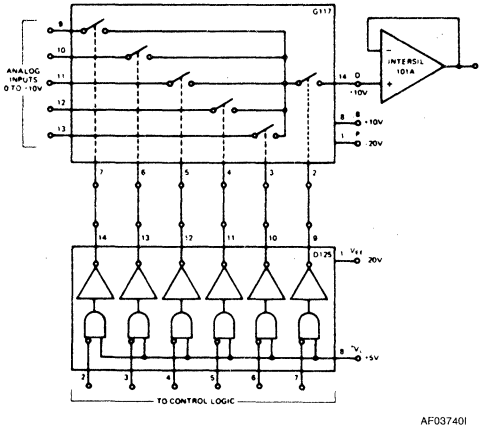


Figure 3: 5–Channel Multiplexer With Series Switch

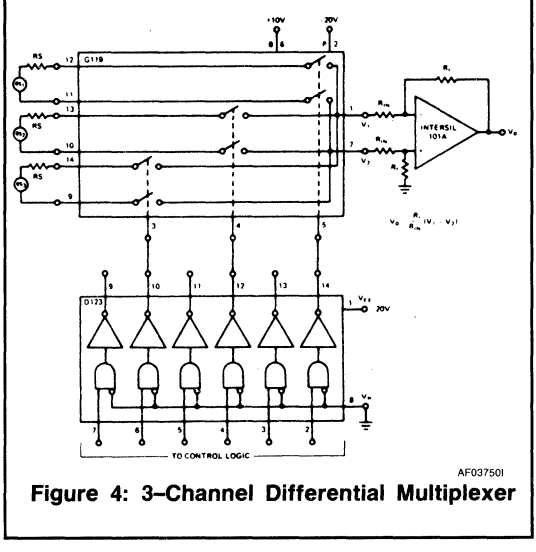


Figure 4: 3–Channel Differential Multiplexer

3

Note: All typical values have been guaranteed by characterization and are not tested.

IH311/IH312
High Speed SPST 4-Channel Analog Switch

INTERSIL

GENERAL DESCRIPTION

The IH311 and IH312 are CMOS, monolithic, QUAD, SPST analog switches for use in high-speed switching applications for communications, instrumentation, process control and computer peripherals. Both devices provide true bi-directional performance in the ON condition and will block signals to 30V peak-to-peak in the OFF condition. The IH311 and IH312 differ only in that the digital control logic is inverted, as shown in the truth table.

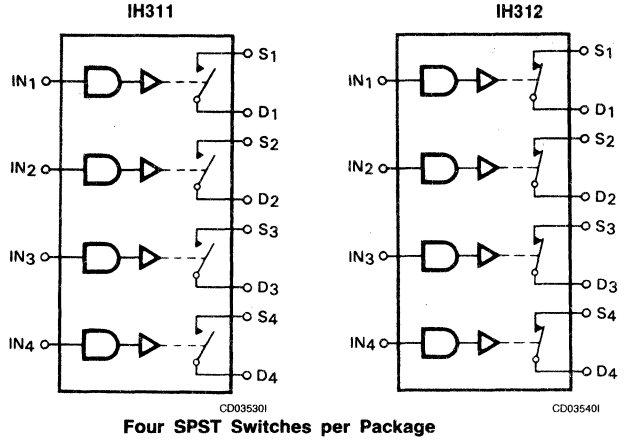
IH311 and IH312 are available in 16-pin Dual-In-Line packages and are offered in both military and commercial temperature ranges.

FEATURES

- **Switches ±15V Analog Signals**
- **TTL Compatibility**
- **Logic Inputs Accept Negative Voltages**
- **$R_{ON} \leq 175$ Ohm**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH311MJE	−55°C to +125°C	16 Pin CERDIP
IH311CJE	0°C to +70°C	16 Pin CERDIP
IH311CPE	0°C to +70°C	16 Pin Plastic DIP
IH312MJE	−55°C to +125°C	16 Pin CERDIP
IH312CJE	0°C to +70°C	16 Pin CERDIP
IH312CPE	0°C to +70°C	16 Pin Plastic DIP



Four SPST Switches per Package

Switches Shown for Logic "1" Input

Truth Table

LOGIC	IH311	IH312
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8V
Logic "1" ≥ 2.4V

Figure 1: Functional Diagram

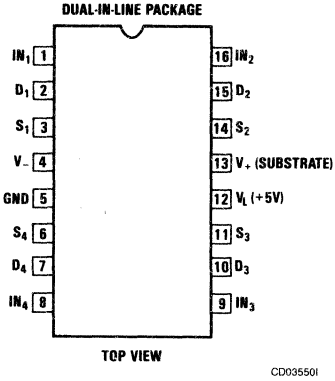


Figure 2: Pin Configuration (Outline dwgs DE, PE)

307040-001

Note: All typical values have been guaranteed by characterization and are not tested.

IH311/IH312

INTERSIL

ABSOLUTE MAXIMUM RATINGS

V^+ to V^- 36V
V_{IN} to Ground ..... V^+, V^+
V_L to Ground ..... -0.3V, 25V
V_S or V_D to V^+ ..... 0, -36V
V_S or V_D to V^- 0, 40V
V^+ to Ground 25V
V^- to Ground ..... -25V
Current, Any Terminal Except S or D 30mA
Continuous Current, S or D 20mA
Peak Current, S or D
(Pulsed at 1msec, 10% duty cycle max) 70mA
Storage Temperature ..... -65°C to +125°C
Operating Temperature ..... -55°C to +125°C
Power Dissipation (Package)*
16 Pin Plastic DIP** 470mW

*Device mounted with all leads soldered or welded to PC board.
**Derate 6.5mW/°C above 25°C

ELECTRICAL CHARACTERISTICS — MILITARY TEMPERATURE RANGE

SYMBOL	PARAMETER	TEST CONDITIONS $V_1 = +15V$, $V_2 = -15V$, $V_L = 5V$, GND		LIMITS -55°C	LIMITS +25°C	LIMITS +125°C	UNIT
SWITCH							
V_{ANALOG}	Analog Signal Range	$V^- = -15V$, $V_L = +5V$			±15		V
$R_{DS(ON)}$	Drain-Source On Resistance	$V_D = \pm 10V$, $V_{IN} = 2.4V$ — IH312 $I_S = 1mA$, $V_{IN} = 0.8V$ — IH311		125	125	150	Ω
$I_{S(off)}$	Source OFF Leakage Current	$V_{IN} = 2.4V$ IH311	$V_S = 14V$, $V_D = -14V$		±1	100	nA
			$V_S = -14V$, $V_D = 14V$		±1	100	
$I_{D(off)}$	Drain OFF Leakage Current	$V_{IN} = 0.8V$ IH312	$V_D = 14V$, $V_S = -14V$		±1	100	
			$V_D = -14V$, $V_S = 14V$		±1	100	
$I_{D(ON)}$	Drain ON Leakage Current[3]	$V_S = V_D = -14V$, $V_{IN} = 0.8V$, IH311 $V_{IN} = 2.4V$, IH312			±2	200	
					±2	200	
INPUT							
I_{INH}	Input Current With Input Voltage High	$V_{IN} = 2.4V$		10	±1	10	µA
		$V_{IN} = 15V$		10	±1	10	
I_{INL}	Input Current With Input Voltage Low	$V_{IN} = 0V$		10	10	10	

Note: All typical values have been guaranteed by characterization and are not tested.

IH311/IH312

INTERSIL

DYNAMIC

t_{on}	Turn-ON Time	See Switching Time Test Circuit V_S = 10V, R_L = 1kΩ, C_L = 35pF		200		ns
t_{off1}	Turn-OFF Time			80		
t_{off2}						
$C_{S(off)}$	Source OFF Capacitance	V_S = 0V, V_{IN} = 5V, f = 1MHz		5		pF
$C_{D(off)}$	Drain OFF Capacitance	V_D = 0V, V_{IN} = 5V, f = 1MHz[2]		5		
$C_{D+S(on)}$	Channel ON Capacitance	V_D = V_S = 0V, V_{IN} = 0V, f = 1MHz		16		
OIRR	OFF Isolation[4]	V_{IN} = 5V, R_L = 1kΩ, C_L = 15pF, V_S = 1VRMS, f = 100kHz[2]		70		dB[4]
CCRR	Crosstalk (Channel to Channel)			90		
SUPPLY						
I^+	Positive Supply Current	V_{IN} = 0 and 2.4V	10	1	10	μA
I^-	Negative Supply Current		10	1	10	
I_L	Logic Supply Current		10	1	10	

NOTES: 1. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
2. For design reference only, not 100% tested.
3. $I_{D(on)}$ is leakage from driver into "ON" switch.
4. OFF Isolation = $20\log\frac{V_S}{V_D}$, V_S = input to OFF switch, V_D = output.

Note: All typical values have been guaranteed by characterization and are not tested.

IH311/IH312

INTERSIL

ABSOLUTE MAXIMUM RATINGS

V^+ to V^- 36V
V_{IN} to Ground ..... V^+, V^+
V_L to Ground ..... −0.3V, 25V
V_S or V_D to V^+ .....0, −36V
V_S or V_D to V^-.....0, 40V
V^+ to Ground 25V
V^- to Ground..... −25V
Current, Any Terminal Except S or D.....30mA
Continuous Current, S or D 20mA

Peak Current, S or D
(Pulsed at 1msec, 10% duty cycle max) 70mA
Storage Temperature..... −65°C to +125°C
Operating Temperature ..... 0°C to +70°C
Power Dissipation (Package)*
16 Pin Plastic DIP** 470mW

*Device mounted with all leads soldered or welded to PC board.
**Derate 6.5mW/°C above 25°C

ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE

SYMBOL	PARAMETER	TEST CONDITIONS $V_1 = +15V$, $V_2 = -15V$, $V_L = 5V$, GND		LIMITS +25°C	LIMITS +70°C	UNIT
SWITCH						
V_{ANALOG}	Analog Signal Range	$V^- = -15V$, $V_L = +5V$		±15		V
$R_{DS(ON)}$	Drain-Source On Resistance	$V_D = \pm 10V$, $V_{IN} = 2.4V$ — IH212 $I_S = 1mA$, $V_{IN} = 0.8V$ — IH211		150	175	Ω
$I_{S(off)}$	Source OFF Leakage Current	$V_{IN} = 2.4V$ IH311 $V_{IN} = 0.8V$ IH312	$V_S = 14V$, $V_D = -14V$	±5	100	nA
			$V_S = -14V$, $V_D = 14V$	±5	100	
$I_{D(off)}$	Drain OFF Leakage Current		$V_D = 14V$, $V_S = -14V$	±5	100	
			$V_D = -14V$, $V_S = 14V$	±5	100	
$I_{D(ON)}$	Drain ON Leakage Current[3]	$V_S = V_D = -14V$, $V_{IN} = 0.8V$, IH211 $V_{IN} = 2.4V$, IH212		±5	200	
				±5	200	
INPUT						
I_{INH}	Input Current With Input Voltage High	$V_{IN} = 2.4V$		±1	−10	μA
		$V_{IN} = 15V$		±1	10	
I_{INL}	Input Current With Input Voltage Low	$V_{IN} = 0V$		±1	−10	
DYNAMIC						
t_{on}	Turn-ON Time	See Switching Time Test Circuit[5] $V_S = 10V$, $R_L = 1k\Omega$, $C_L = 35pF$		300		ns
t_{off1}	Turn-OFF Time			150		
t_{off2}						
$C_{S(off)}$	Source OFF Capacitance	$V_S = 0V$, $V_{IN} = 5V$, f = 1MHz		5		pF
$C_{D(off)}$	Drain OFF Capacitance	$V_D = 0V$, $V_{IN} = 5V$, f = 1MHz[2]		5		
$C_{D+S(on)}$	Channel ON Capacitance	$V_D = V_S = 0V$, $V_{IN} = 0V$, f = 1MHz		16		
OIRR	OFF Isolation[4]	$V_{IN} = 5V$, $R_L = 1k\Omega$, $C_L = 15pF$, $V_S = 1VRMS$, f = 100kHz[2]		70		dB
CCRR	Crosstalk (Channel to Channel)			90		
SUPPLY						
I^+	Positive Supply Current	$V_{IN} = 0$ and 2.4V		±1	10	μA
I^-	Negative Supply Current			±1	−10	
I_L	Logic Supply Current			±1	10	

NOTES: 1. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
2. For design reference only, not 100% tested.
3. $I_{D(on)}$ is leakage from driver into "ON" switch.
4. OFF Isolation = $20\log\frac{V_S}{V_D}$, V_S = input to OFF switch, V_D = output.
5. Switching times only sampled.

3

Note: All typical values have been guaranteed by characterization and are not tested.

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note the V_S may be + or – as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

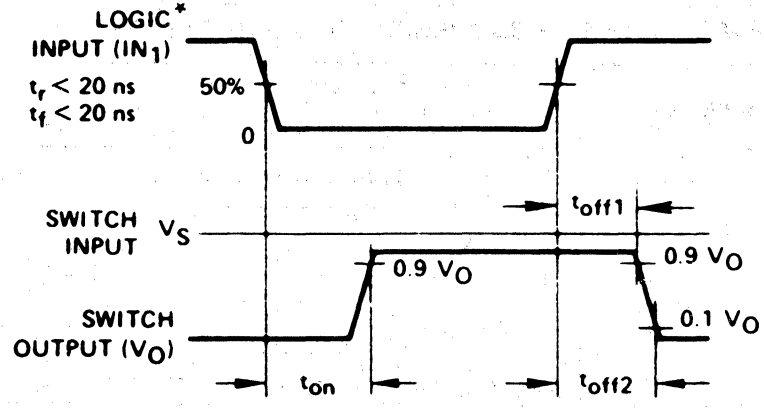


Figure 3: Switching Time Test Circuit
Logic shown for IH311. Invert for IH312.

Note: All typical values have been guaranteed by characterization and are not tested.

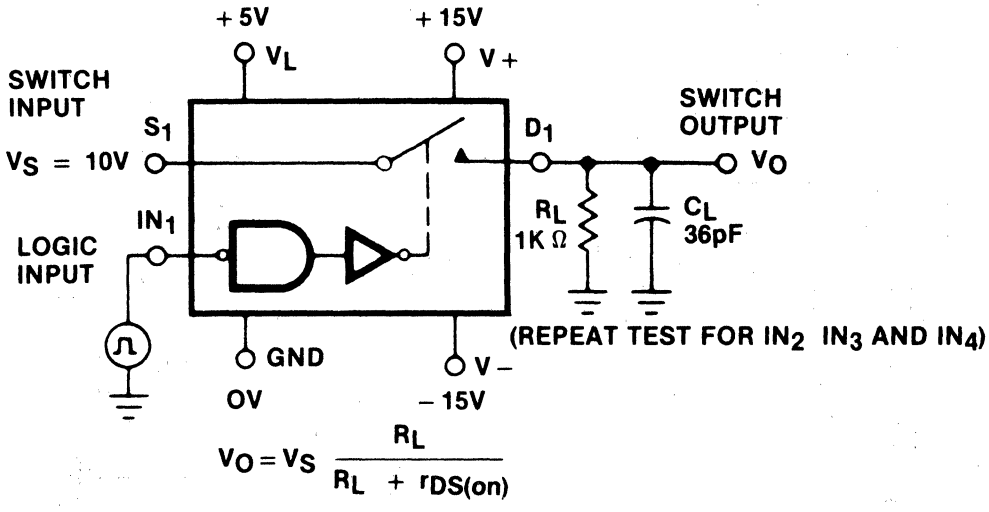


Figure 4: Switching Time Test Circuit

Note: All typical values have been guaranteed by characterization and are not tested.

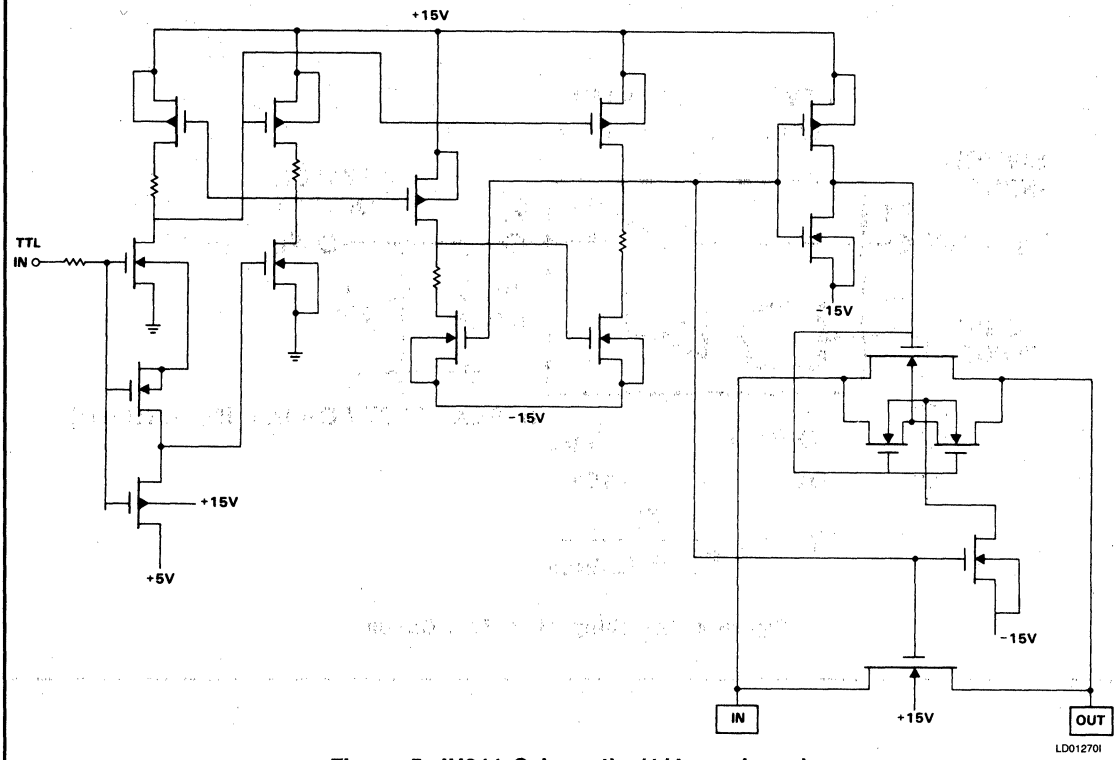


Figure 5: IH311 Schematic (1/4 as shown)

Note: All typical values have been guaranteed by characterization and are not tested.

IH401/IH401A
QUAD Varafet Analog Switch

GENERAL DESCRIPTION

The IH401 is made up of 4 monolithically constructed combinations of a varactor type diode and an N-channel JFET. The JFET itself is very similar to the popular 2N4391, and the driver diode is specially designed, such that its capacitance is a strong function of the voltage across it. The driver diode is electrically in series with the gate of the N-channel FET and simulates a back-to-back diode structure. This structure is needed to prevent forward biasing the source-to-gate or drain-to-gate junctions of the JFET when used in switching applications.

Previous applications of JFETs required the addition of diodes, in series with the gate, and then perhaps a gate-to-source referral resistor or a capacitor in parallel with the diode; therefore, at least 3 components were required to perform the switch function. The IH401 does this same job in one component (with a great deal better performance characteristics).

Like a standard JFET, to practically perform a solid state switch function a translator should be added to drive the diode. This translator takes the TTL levels and converts them to voltages required to drive the diode/FET system (typically a 0V to −15V translation and a 3V to +15V shift). With ±15V power supplies, the IH401 will typically switch $18V_{p\text{-}p}$ at any frequency from DC to 20MHz, with less than 30Ω $R_{DS(on)}$. The IH401A will typically switch $22V_{p\text{-}p}$ with less than 50Ω $R_{DS(on)}$.

FEATURES

- **$R_{DS(on)}$ = 25Ω Typical (IH401)**
- **$I_{D(off)}$ of 10pA Typical**
- **Switching Times of 25ns for t_{on} and 75ns for t_{off} (R_L = 1kΩ)**
- **Built-In Overvoltage Protection (±25V)**
- **Charge Injection Error of 3mV Typical Into 0.01μF Capacitor**
- **C_{iss} < 1pF Typical**
- **Can Be Used for Hybrid Construction**

ORDERING INFORMATION

PART NUMBER	PACKAGE
IH401	CERDIP
IH401A	CERDIP
IH401/D	DICE

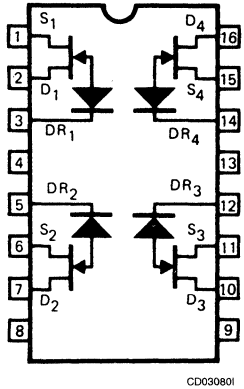


Figure 1: Pin Configuration (Outline Dwg JE)

Note: All typical values have been guaranteed by characterization and are not tested.

IH401/IH401A

INTERSIL

ABSOLUTE MAXIMUM RATINGS

V_S to V_D 35V
V_G to V_S, V_D 35V
Operating Temperature ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS AT 25°C/125°C

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	IH401			UNIT
			MIN	TYP	MAX	
$R_{DS(on)}$	Switch "on" Resistance	V_{DRIVE} = 15V, V_{DRAIN} = −7.5V I_D = 10mA		20	30	Ω
V_P	Pinch-Off Voltage	I_D = 1nA, V_{DS} = 10V	3	6	7.5	V
$I_{D(off)}$	Switch "off" Current or "off" Leakage	V_{DRIVE} = −15V, V_{SOURCE} = −7.5V, V_{DRAIN} = +7.5V		10	±500	pA
$I_{D(off)}$	Switch "off" Leakage at 125°C	V_{DRIVE} = −15V, V_{SOURCE} = −7.5V, V_{DRAIN} = +7.5V		0.25	50	nA
$I_{S(off)}$	Switch "off" Current	V_{DRIVE} = −15V, V_{DRAIN} = −7.5V, V_{SOURCE} = +7.5V		10	±500	pA
$I_{S(off)}$	Switch "off" Leakage at 125°C	V_{DRIVE} = −15V, V_{SOURCE} = −7.5V, V_{DRAIN} = +7.5V		0.3	50	nA
$I_{D(on)}$ + $I_{S(on)}$	Switch Leakage when Turned "on"	V_D = V_S = −7.5V, V_{DRIVE} = +15V		0.02	±2	nA
V_{analog}	AC Input Voltage Range without Distortion	See Figure 3	15	18		V_{p-p}
V_{inject}	Charge Injection Error Voltage	See Figure 4		3		mV_{p-p}
BV_{diode}	Diode Reverse Breakdown Voltage. This Correlates to Overvoltage Protection	V_D = V_S = −V, I_{DRIVE} = 1μA, V_{DRIVE} = 0V	−30	−45		V
BV_{GSS}	Gate to Source or Gate to Drain Reverse Breakdown Voltage	V_{DRIVE} = −V, V_D = V_S = 0V, I_{DRIVE} = 1μA	30	41		V
I_{DSS}	Maximum Current Switch can Deliver (Pulsed)	V_{DRIVE} = 15V, V_S = 0V, V_D = +10V	45	70		mA
t_{on}	Switch "on" time (Note 1)	See Figure 2		50		ns
t_{off}	Switch "off" time (Note 1)	See Figure 2		150		ns

NOTE 1: Driving waveform must be > 100ns rise and fall time.

Note: All typical values have been guaranteed by characterization and are not tested.

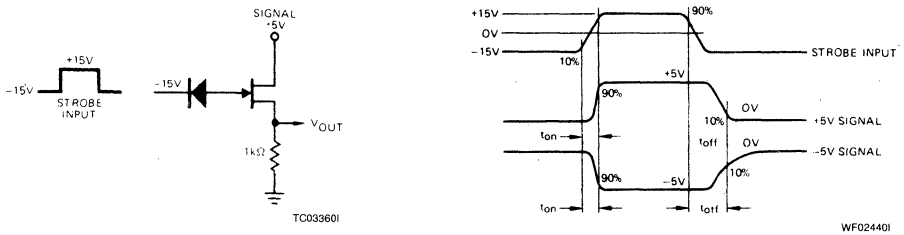


Figure 2: Switching Time Test Circuit and Waveforms

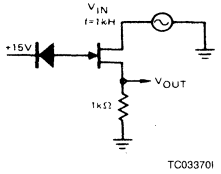


Figure 3: Analog Input Voltage Range Test Circuit

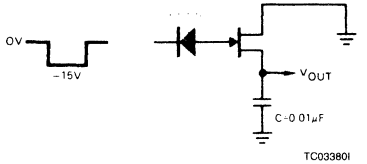


Figure 4: Charge Injection Test Circuit

ELECTRICAL CHARACTERISTICS AT 25°C/125°C

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	IH401A			UNIT
			MIN	TYP	MAX	
$R_{DS(on)}$	Switch "on" Resistance	V_{DRIVE} = 15V, V_{DRAIN} = −10V, I_D = 10mA		35	50	Ω
V_P	Pinch-Off Voltage	I_D = 1nA, V_{DS} = 10V	2	4	5	V
$I_{D(off)}$	Switch "off" Current or "off" Leakage	V_{DRIVE} = −15V, V_{SOURCE} = −10V, V_{DRAIN} = +10V		10	±500	pA
$I_{D(off)}$	Switch "off" Leakage at 125°C	V_{DRIVE} = −15V, V_{SOURCE} = −10V, V_{DRAIN} = +10V		0.25	50	nA
$I_{S(off)}$	Switch "off" Current	V_{DRIVE} = −15V, V_{DRAIN} = −10V, V_{SOURCE} = +10V		10	±500	pA
$I_{S(off)}$	Switch "off" Leakage at 125°C	V_{DRIVE} = −15V, V_{SOURCE} = −10V, V_{DRAIN} = +10V		0.3	50	nA
$I_{D(on)}$ + $I_{S(on)}$	Switch Leakage when Turned "on"	V_D = V_S = −10V, V_{DRIVE} = +15V		0.02	±2	nA
V_{analog}	AC Input Voltage Range without Distortion	See Figure 3	20	22		V_{p-p}
V_{inject}	Charge Injection Amplitude	See Figure 4		3		mV_{p-p}
BV_{diode}	Diode Reverse Breakdown Voltage. This Correlates to Overvoltage Protection	V_D = V_S = −V, I_{DRIVE} = 1μA, V_{DRIVE} = 0V	−30	−45		V

Note: All typical values have been guaranteed by characterization and are not tested.

IH401/IH401A

INTERSIL

ELECTRICAL CHARACTERISTICS AT 25°C/125°C (CONT.)

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	IH401A			UNIT
			MIN	TYP	MAX	
BV_{GSS}	Gate to Source or Gate to Drain Reverse Breakdown Voltage	$V_{DRIVE} = -V$, $V_D = V_S = 0V$, $I_{DRIVE} = 1\mu A$	30	41		V
I_{DSS}	Maximum Current Switch can Deliver (Pulsed)	$V_{DRIVE} = 15V$, $V_S = 0V$, $V_D = +10V$	35	55		mA
t_{on}	Switch "on" time (Note 1)	See Figure 2		50		ns
t_{off}	Switch "off" time (Note 1)	See Figure 2		150		ns

NOTE: Driving waveform must be > 100ns rise and fall time.

APPLICATIONS

IH401 Family

In general, the IH401 family can be used in any application formally using a JFET/isolation diode combination (2N4391 or similar). Like standard FET circuits, the IH401 requires a translator for normal analog switch function. The translator is used to boost the TTL input signals to the ±15V analog supply levels which allow the IH401 to handle ±7.5V analog signals (or IH401A to handle ±10V analog signals). A typical simple PNP translator is shown in Figure 5.

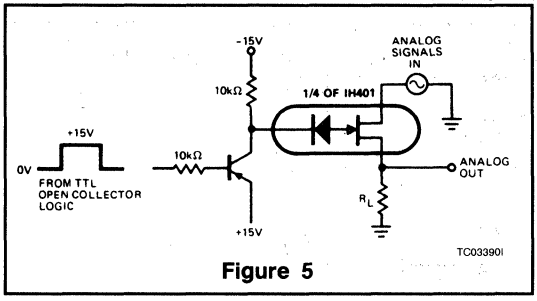
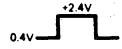


Figure 5

Although this simple PNP circuit represents a minimum of components, it requires open collector TTL input and $t_{(off)}$ is limited by the collector load resistor (approximately 1.5μs for 10kΩ). Improved switching speed can be obtained by increasing the complexity of the translator stage.

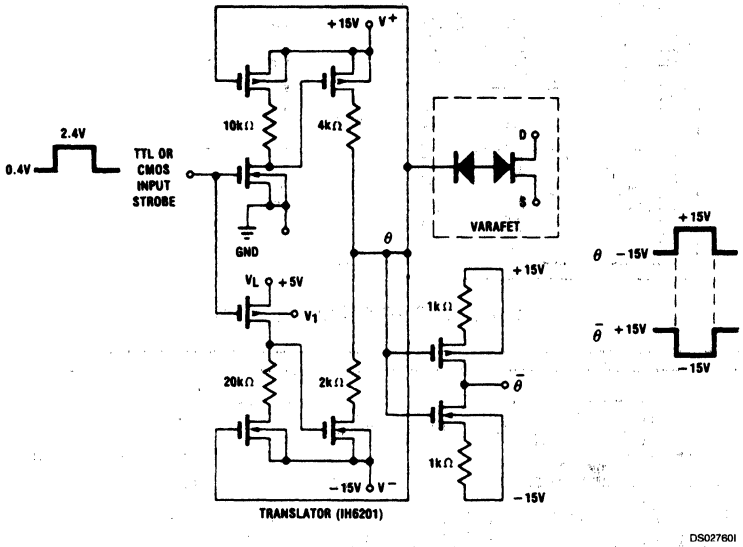
A translator which overcomes the problems of the simple PNP stage is the Intersil IH6201.* This translator driving an IH401 varafet produces the following typical features:

- t_{on} time of approx. 200ns } break before
- t_{off} time of approx. 80ns } make switch
- TTL compatible strobing levels of 

- $I_{D(on)}$ + $I_{S(on)}$ typically 20pA up to ±10V analog signals
- $I_{D(off)}$ or $I_{S(off)}$ typically 20pA
- Quiescent current drain of approx. 100nA in either "on" or "off" case

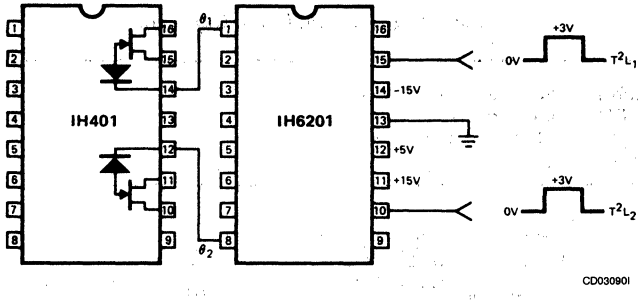
*The IH6201 is a dual translator (two independent translators per package) constructed from monolithic CMOS technology. The schematic of one-half IH6201, driving one-fourth of an IH401, is shown in Figure 6.

Note: All typical values have been guaranteed by characterization and are not tested.



NOTE: Each translator output has a θ and $\bar{\theta}$ output. $\bar{\theta}$ is just the inverse of θ i.e., ($\bar{\theta}$ output is 180° out of phase with respect to θ output).

Figure 6: IH6201 Driving An IH401



NOTE: Either switch is turned on when strobe input goes high.

Figure 7: Dual SPST Analog Switch

Note: All typical values have been guaranteed by characterization and are not tested.

IH401/IH401A

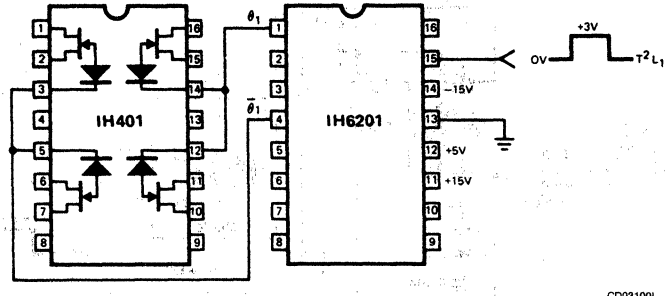


Figure 8: DPDT Analog Switch

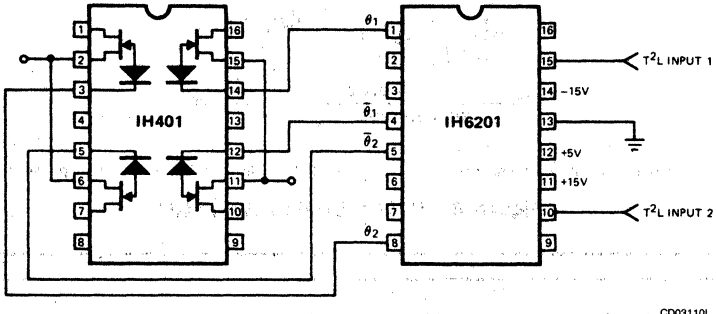


Figure 9: Dual SPDT Analog Switch

A very useful feature of this system is that one-half of an IH6201 and one-half of an IH401 can combine to make a SPDT switch, or an IH6201 plus an IH401 can make a dual SPDT analog switch. (See Figure 9)

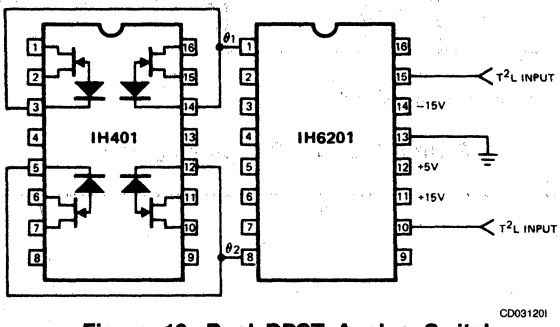


Figure 10: Dual DPST Analog Switch

Note: All typical values have been guaranteed by characterization and are not tested.

IH5009-IH5024
Virtual Ground Analog Switch

GENERAL DESCRIPTION

The IH5009 series of analog switches were designed to fill the need for an easy-to-use, inexpensive switch for both industrial and military applications. Although low cost is a primary design objective, performance and versatility have not been sacrificed.

Each package contains up to four channels of analog gating and is designed to eliminate the need for an external driver. The odd numbered devices are designed to be driven directly from TTL open collector logic (15 volts) while the even numbered devices are driven directly from low level TTL logic (5 volts). Each channel simulates a SPDT switch. SPDT switch action is obtained by leaving the diode cathode unconnected; for SPDT action, the cathode should be grounded (0V). The parts are intended for high performance multiplexing and commutating usage. A logic "0" turns the channel ON and a logic "1" turns the channel OFF.

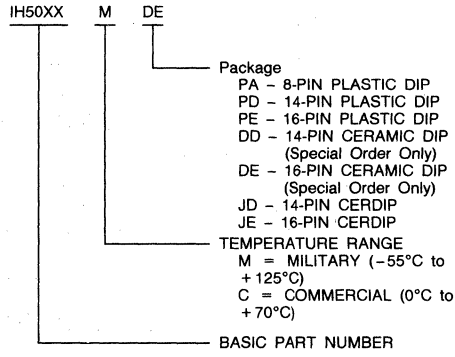
FEATURES

- **Switches Analog Signals Up to 20 Volts Peak-to-Peak**
- **Each Channel Complete – Interfaces With Most Integrated Logic**
- **Switching Speeds Less Than 0.5μs**
- **$I_{D(OFF)}$ Less Than 500pA Typical at 70°C**
- **Effective $r_{ds(ON)}$ – 5Ω to 50Ω**
- **Commercial and Military Temperature Range Operation**

ORDERING INFORMATION

BASIC PART NUMBER	CHANNELS	LOGIC LEVEL	PACKAGES
IH5009	4	+15	JD,DD,PD
IH5010	4	+5	JD,DD,PD
IH5011	4	+15	JE,DE,PE
IH5012	4	+5	JE,DE,PE
IH5013	3	+15	JD,DD,PD
IH5014	3	+5	JD,DD,PD
IH5015	3	+15	JE,DE,PE
IH5016	3	+5	JE,DE,PE
IH5017	2	+15	JD,DD,PA
IH5018	2	+5	JD,DD,PA
IH5019	2	+15	JE,DE,PA
IH5020	2	+5	JE,DE,PA
IH5021	1	+15	JD,DD,PA
IH5022	1	+5	JD,DD,PA
IH5023	1	+15	JE,DE,PA
IH5024	1	+5	JE,DE,PA

NOTE: Mil-Temperature range (−55°C to +125°C) available in ceramic packages only.



Note: All typical values have been guaranteed by characterization and are not tested.

IH5009-IH5024

ABSOLUTE MAXIMUM RATINGS

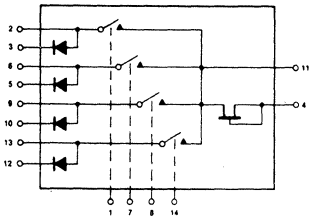
Positive Analog Signal Voltage 30V
Negative Analog Signal Voltage..... -15V
Diode Current 10mA
Power Dissipation (Note).....500mW
Storage Temperature..... -65°C to +150°C

Lead Temperature (Soldering, 10sec) .....300°C
Operating Temperature
5009C Series..... 0°C to +70°C
5009M Series ..... -55°C to +125°C
Lead Temperature (Soldering, 10sec) .....300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 75°C. For higher temperature, derate at rate of 5m/W°C.

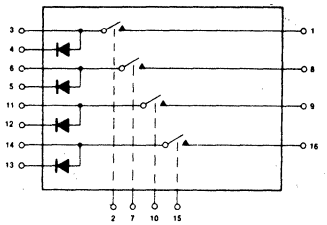
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

IH5009 ($r_{DS(ON)} \leq 100\Omega$) IH5010 ($r_{DS(ON)} \leq 150\Omega$) 14 PIN DIP (OUTLINE DWGS DD, PD, JD)



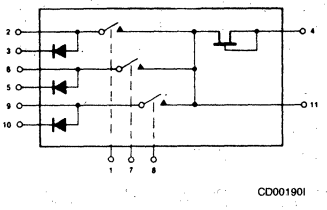
CD00170I

IH5011 ($r_{DS(ON)} \leq 100\Omega$) IH5012 ($r_{DS(ON)} \leq 150\Omega$) 16 PIN DIP (OUTLINE DWGS DE, PE, JE)



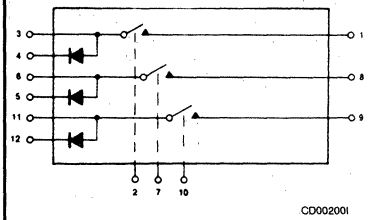
CD00180I

IH5013 ($r_{DS(ON)} \leq 100\Omega$) IH5014 ($r_{DS(ON)} \leq 150\Omega$) 14 PIN DIP (OUTLINE DWGS DD, PE, JE)



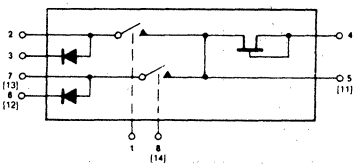
CD00190I

IH5015 ($r_{DS(ON)} \leq 100\Omega$) IH5016 ($r_{DS(ON)} \leq 150\Omega$) 16 PIN DIP (OUTLINE DWGS DE, PE, JE)



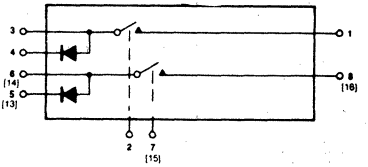
CD00200I

IH5017 ($r_{DS(ON)} \leq 100\Omega$) IH5018 ($r_{DS(ON)} \leq 150\Omega$) 8 PIN DIP (OUTLINE DWGS DD, PA, JD)



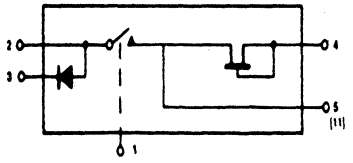
CD00210I

IH5019 ($r_{DS(ON)} \leq 100\Omega$) IH5020 ($r_{DS(ON)} \leq 150\Omega$) 8 PIN DIP (OUTLINE DWGS DE, PA, JE)



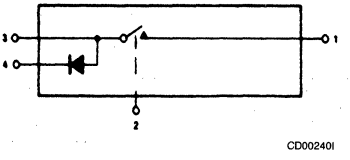
CD00220I

IH5021 ($r_{DS(ON)} \leq 100\Omega$) IH5022 ($r_{DS(ON)} \leq 150\Omega$) 8 PIN DIP (OUTLINE DWGS DD, PA, JD)



CD00230I

IH5023 ($r_{DS(ON)} \leq 100\Omega$) IH5024 ($r_{DS(ON)} \leq 150\Omega$) 8 PIN DIP (OUTLINE DWGS DE, PA)



CD00240I

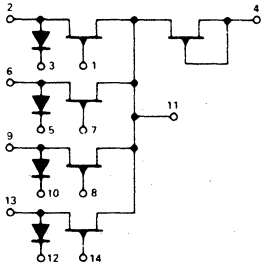
(Note: Numbers in brackets refer to CERDIP packages.)

Figure 1: Pin Connections

Note: All typical values have been guaranteed by characterization and are not tested.

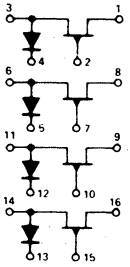
FOUR CHANNEL

IH5009 ($r_{DS(ON)} \leq 100\Omega$)
IH5010 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP



DS01670I

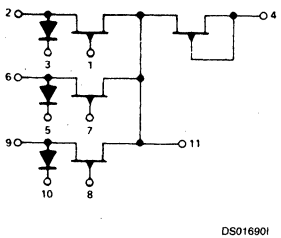
IH5011 ($r_{DS(ON)} \leq 100\Omega$)
IH5012 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP



DS01680I

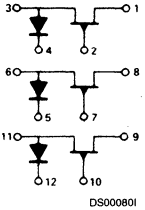
THREE CHANNEL

IH5013 ($r_{DS(ON)} \leq 100\Omega$)
IH5014 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP



DS01690I

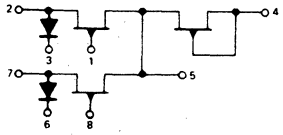
IH5015 ($r_{DS(ON)} \leq 100\Omega$)
IH5016 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP



DS00080I

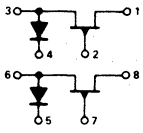
TWO CHANNEL

IH5017 ($r_{DS(ON)} \leq 100\Omega$)
IH5018 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



DS00090I

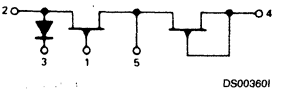
IH5019 ($r_{DS(ON)} \leq 100\Omega$)
IH5020 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



DS00100I

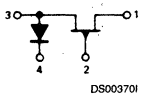
SINGLE CHANNEL

IH5021 ($r_{DS(ON)} \leq 100\Omega$)
IH5022 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



DS00360I

IH5023 ($r_{DS(ON)} \leq 100\Omega$)
IH5024 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



DS00370I

Figure 2: Device Schematics and Pin Connections

ELECTRICAL CHARACTERISTICS (per channel)

SYMBOL (Note 1)	CHARACTERISTIC	TYPE (Note 4)	TEST CONDITIONS (Note 2)	SPECIFICATION LIMIT				UNIT
				-55°C (M) 0°C (C) MIN/MAX	25°C TYP	25°C MIN/MAX	+125°C (M) +70°C (C) MIN/MAX	
$I_{IN(ON)}$	Input Current-ON	ALL	V_{IN} = 0V, I_D = 2mA		0.01	±0.5	100	μA
$I_{IN(OFF)}$	Input Current-OFF	5V Logic Ckts	V_{IN} = +4.5V, V_A = ±10V		0.04	±0.5	20	nA
$I_{IN(OFF)}$	Input Current-OFF	15V Logic Ckts	V_{IN} = +11V, V_A = ±10V		0.04	±0.5	20	nA
$V_{IN(ON)}$	Channel Control Voltage-ON	5V Logic Ckts	See Figure 7, Note 3	0.5		0.5	0.5	V
$V_{IN(ON)}$	Channel Control Voltage-ON	15V Logic Ckts	See Figure 8, Note 3	1.5		1.5	1.5	V
$V_{IN(OFF)}$	Channel Control Voltage-OFF	5V Logic Ckts	See Figure 6, Note 3			4.5	4.5	V
$V_{IN(OFF)}$	Channel Control Voltage-OFF	15V Logic Ckts	See Figure 8, Note 3			11.0	11.0	V
$I_{D(OFF)}$	Leakage Current-OFF	5V Logic Ckts	V_{IN} = +4.5V, V_A = ±10V		0.02	±0.5	20	nA
$I_{D(OFF)}$	Leakage Current-OFF	15V Logic Ckts	V_{IN} = +11V, V_A = ±10V		0.02	±0.5	20	nA
$I_{D(ON)}$	Leakage Current-ON	5V Logic Ckts	V_{IN} = 0V, I_S = 1mA		0.30	±1.0	1000 (M) 200 (C)	nA
$I_{D(ON)}$	Leakage Current-ON	15V Logic Ckts	V_{IN} = 0V, I_S = 1mA		0.10	±0.5	500 (M) 100 (C)	nA
$I_{D(ON)}$	Leakage Current-ON	5V Logic Ckts	V_{IN} = 0V, I_S = 2mA			1.0	10	μA
$I_{D(ON)}$	Leakage Current-ON	15V Logic Ckts	V_{IN} = 0V, I_S = 2mA			2.0	100	μA
$r_{DS(ON)}$	Drain-Source ON-Resistance	5V Logic Ckts	I_D = 2mA, V_{IN} = 0.5V	150	90	150	385 (M) 240 (C)	Ω
$r_{DS(ON)}$	Drain-Source ON-Resistance	15V Logic Ckts	I_D = 2mA, V_{IN} = 1.5V	100	80	100	250 (M) 160 (C)	Ω
$t_{(on)}$	Turn-ON Time	All	See Figures 5 & 6		150	500		ns

Note: All typical values have been guaranteed by characterization and are not tested.

IH5009-IH5024

INTERSIL

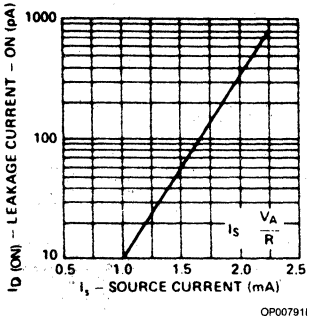
ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL (Note 1)	CHARACTERISTIC	TYPE (Note 4)	TEST CONDITIONS (Note 2)	SPECIFICATION LIMIT				UNIT
				-55°C (M) 0°C (C) MIN/MAX	25°C TYP	25°C MIN/MAX	+125°C (M) +70°C (C) MIN/MAX	
$t_{(off)}$	Turn-OFF Time	All	See Figures 5 & 6		300	500		ns
CT	Cross Talk	All	f = 100Hz		120			dB

NOTES 1: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.
2: Refer to Figure 2 for definition of terms.
3: $V_{IN(ON)}$ and $V_{IN(OFF)}$ are test conditions guaranteed by the tests of $r_{DS(ON)}$ and $I_{D(OFF)}$ respectively.
4: "5V Logic CKTS" applies to even-numbered devices. "15V Logic CKTS" applies to odd-numbered devices.

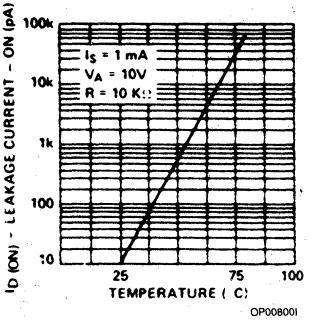
TYPICAL PERFORMANCE CHARACTERISTICS (per channel)

$I_{D(ON)}$ vs. I_S AT 25°C



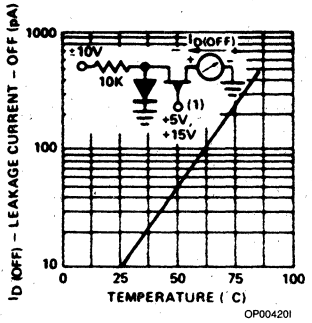
OP00791I

$I_{D(ON)}$ vs. TEMPERATURE



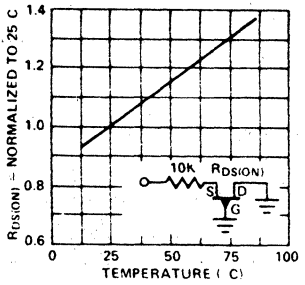
OP00800I

$I_{D(OFF)}$ vs. TEMPERATURE



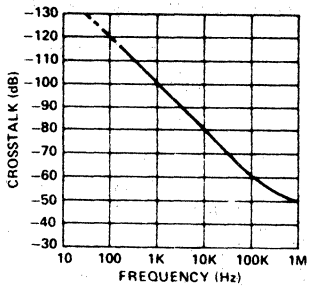
OP00420I

$R_{DS(ON)}$ vs. TEMPERATURE (NORMALIZED TO 25°C VALUE)



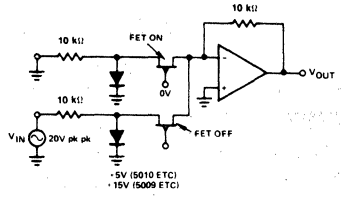
OP00431I

CROSSTALK AS A FUNCTION OF FREQUENCY



OP00440I

CROSSTALK MEASUREMENT CIRCUIT



TC00420I

DETAILED DESCRIPTION

The signals seen at the drain of a junction FET type analog switch can be arbitrarily divided into two categories; those which are less than ±200mV, and those which are greater than ±200mV. The former category includes all those circuits where switching is performed at the virtual ground point of an op-amp, and it is primarily towards these applications that the IH5009 family of circuits is directed.

By limiting the analog signal at the switching point to ±200mV, no external driver is required and the need for additional power supplies is eliminated.

Devices are available with both common drains and with uncommitted drains.

Those devices which feature common drains have another FET in addition to the channel switches. This FET, which has gate and source connected such that $V_{GS} = 0$, is intended to compensate for the on-resistance of the switch. When placed in series with the feedback resistor (Figure 3) the gain is given by:

$$GAIN = \frac{10k\Omega + r_{DS(ON)}(compensator)}{10k\Omega + r_{DS(switch)}}.$$

Note: All typical values have been guaranteed by characterization and are not tested.

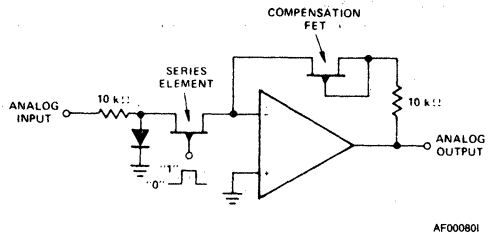


Figure 3: Use of Compensation FET

Clearly, the gain error caused by the switch is dependent on the match between the FETs rather than the absolute value of the FET on-resistance. For the standard product, all the FETs in a given package are guaranteed to match within 50Ω. Selections down to 5Ω are available however. Contact factory for details. Since the absolute value of $r_{DS(ON)}$ is guaranteed only to be less than 100Ω or 150Ω, a substantial improvement in gain accuracy can be obtained by using the compensating FET.

DEFINITION OF TERMS

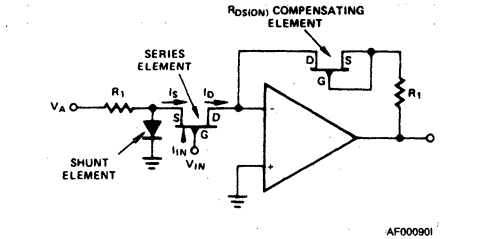


Figure 4.

NOISE IMMUNITY

The advantage of SPDT switching is high noise immunity when the series elements is OFF. For example, if a ±10V analog input is being switched by TTL open collector logic, the series switch is OFF when the logic level is at +15 volts. At this time, the diode conducts and holds the source at approximately +0.7 volts with an AC impedance to ground of 25 ohms. Thus random noise superimposed on the +10 volt analog input will not falsely trigger the FET since the noise voltage will be shunted to ground.

When switching a negative voltage, the input further increases the OFF voltage beyond pinch-off, so there is no danger of the FET turning on.

SWITCHING CHARACTERISTICS

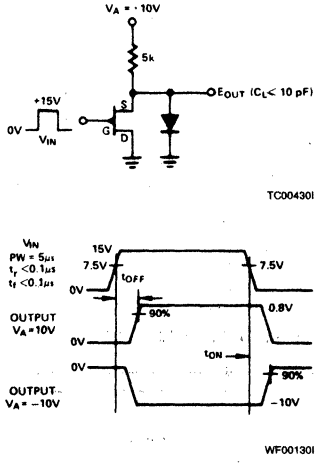


Figure 5: High Level Logic

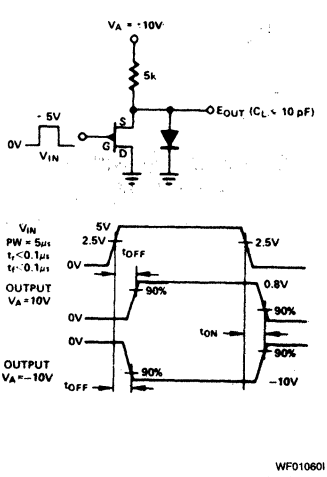


Figure 6: Standard DTL, TTL, RTL

Note: All typical values have been guaranteed by characterization and are not tested.

LOGIC INTERFACE CIRCUITS

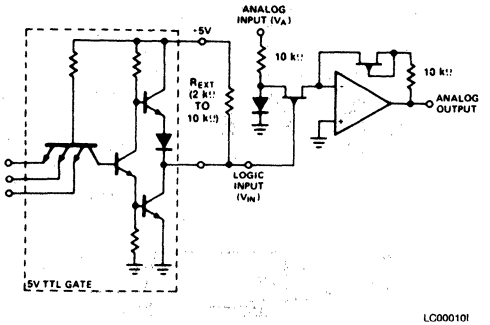


Figure 7: Interfacing with +5V Logic

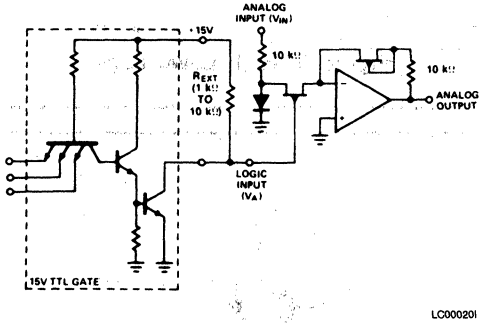


Figure 8: Interfacing with +15V Open Collector Logic

APPLICATIONS (Note)

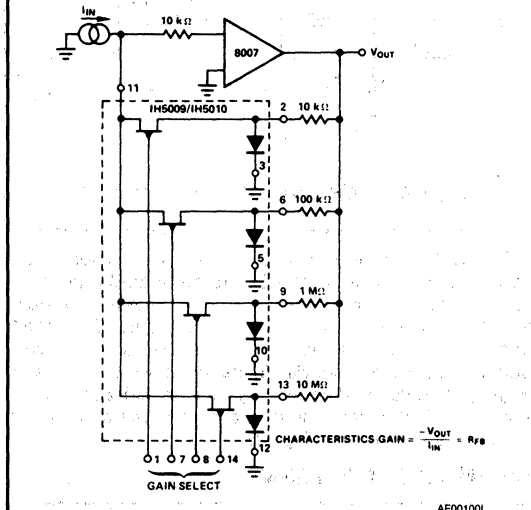


Figure 9

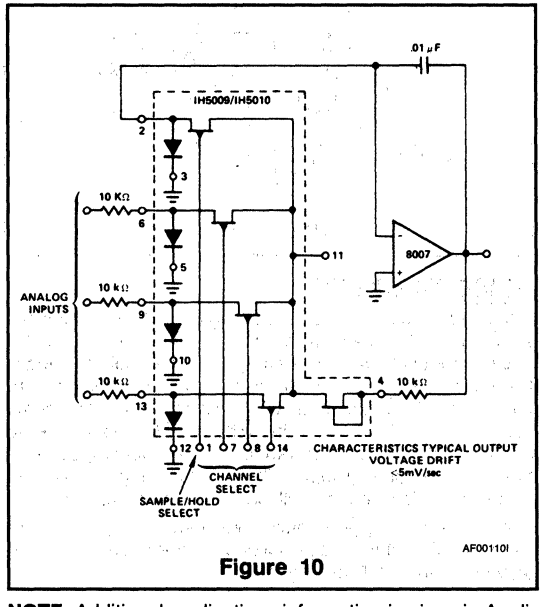


Figure 10

NOTE: Additional applications information is given in Application Bulletins A003 "Understanding and Applying the Analog Switch" and A004 "The 5009 Series of Low Cost Analog Switches".

Note: All typical values have been guaranteed by characterization and are not tested.

IH5025-IH5038
Positive Signal Analog Switch

GENERAL DESCRIPTION

The IH5025 series of analog switches was designed to fill the need for an easy-to-use, inexpensive switch for both industrial and military applications. Although low cost is a primary design objective, performance and versatility have not been sacrificed.

Each package contains up to four channels of analog gating and is designed to eliminate the need for an external driver.

The entire family is designed to be driven from TTL open collector logic (15V), but can be driven from 5V logic if signal input is less than 1V. Alternatively, 20V switching is readily obtainable if TTL supply voltage is +25V. Normally, only positive signals can be switched; however, up to ±10V can be handled by the addition of a PNP stage (Figure 14) or by capacitor isolation (Figure 13). Each channel is a SPST switch. A logic "0" turns the channel ON and a logic "1" turns the channel OFF.

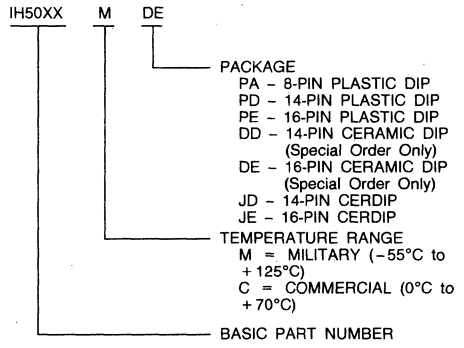
FEATURES

- **Switches Up to +20V Into High Impedance Loads (i.e. Non-Inverting Input of Operational Amp.)**
- **Driven From TTL Open Collector Logic**
- **$I_{D(OFF)}$ < 50pA**
- **$r_{DS(ON)}$ < 150Ω**
- **$r_{DS(ON)}$ Match < 50Ω Channel to Channel**
- **Switching Speeds < 100ns**

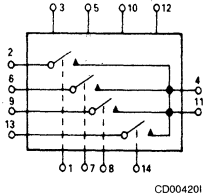
ORDERING INFORMATION

BASIC PART NUMBER	CHANNELS	LOGIC LEVEL	PACKAGES
IH5025	4	+15	JD,DD,PD
IH5026	4	+5	JD,DD,PD
IH5027	4	+15	JE,DE,PE
IH5028	4	+5	JE,DE,PE
IH5029	3	+15	JD,DD,PD
IH5030	3	+5	JD,DD,PD
IH5031	3	+15	JE,DE,PE
IH5032	3	+5	JE,DE,PE
IH5033	2	+15	JD,DD,PA
IH5034	2	+5	JD,DD,PA
IH5035	2	+15	JE,DE,PA
IH5036	2	+5	JE,DE,PA
IH5037	1	+15	JD,DD,PA
IH5038	1	+5	JD,DD,PA

NOTE: Mil-Temperature range (−55°C to +125°C) available in ceramic packages only.

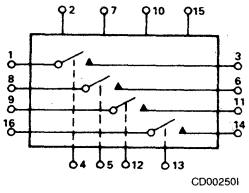


IH5025 ($r_{DS(ON)}$ ≤ 100Ω)
IH5026 ($r_{DS(ON)}$ ≤ 150Ω)
14 PIN DIP



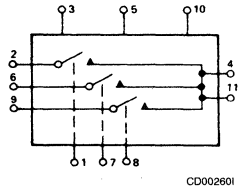
CD00420I

IH5027 ($r_{DS(ON)}$ ≤ 100Ω)
IH5028 ($r_{DS(ON)}$ ≤ 150Ω)
16 PIN DIP



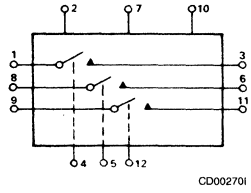
CD00250I

IH5029 ($r_{DS(ON)}$ ≤ 100Ω)
IH5030 ($r_{DS(ON)}$ ≤ 150Ω)
14 PIN DIP



CD00260I

IH5031 ($r_{DS(ON)}$ ≤ 100Ω)
IH5032 ($r_{DS(ON)}$ ≤ 150Ω)
16 PIN DIP



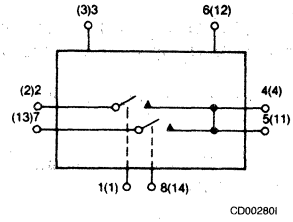
CD00270I

Figure 1: Pin Connections

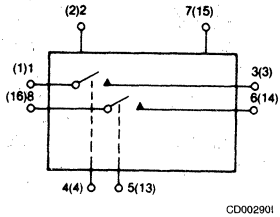
Note: All typical values have been guaranteed by characterization and are not tested.

IH5025-IH5038

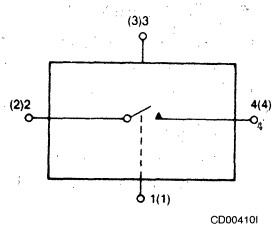
IH5033 ($r_{DS(ON)} \leq 100\Omega$)
IH5034 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



IH5035 ($r_{DS(ON)} \leq 100\Omega$)
IH5036 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



IH5037 ($r_{DS(ON)} \leq 100\Omega$)
IH5038 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP

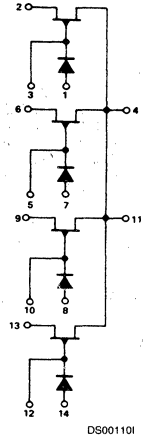


NUMBERS IN PARENTHESES INDICATE CERAMIC PACKAGE PIN-OUT

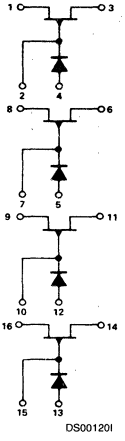
Figure 1: Pin Connections (Cont.)

FOUR CHANNEL

IH5025 ($r_{DS(ON)} \leq 100\Omega$)
IH5026 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP

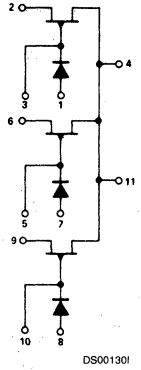


IH5027 ($r_{DS(ON)} \leq 100\Omega$)
IH5028 ($r_{DS(ON)} \leq 150\Omega$)
14PIN DIP

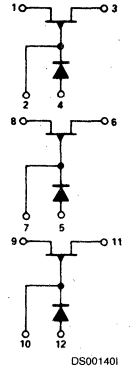


THREE CHANNEL

IH5029 ($r_{DS(ON)} \leq 100\Omega$)
IH5030 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP

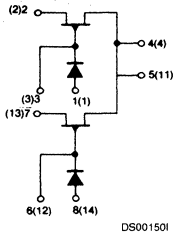


IH5031 ($r_{DS(ON)} \leq 100\Omega$)
IH5032 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP



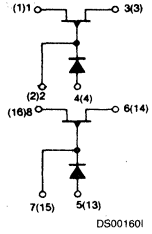
TWO CHANNEL

IH5033 ($r_{DS(ON)} \leq 100\Omega$) IH5034 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP

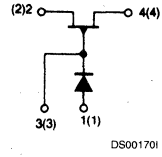


SINGLE CHANNEL

IH5035 ($r_{DS(ON)} \leq 100\Omega$) IH5036 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



IH5037 ($r_{DS(ON)} \leq 100\Omega$) IH5038 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



Numbers in parentheses indicate CERAMIC PACKAGE LAYOUT

Figure 2: Device Schematics

Note: All typical values have been guaranteed by characterization and are not tested.

IH5025-IH5038

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Positive Analog Signal Voltage 25V
Negative Analog Signal Voltage ..... -0.5VDC
Drain Current 25mA
Power Dissipation (Note) 500mW
Storage Temperature ..... -65°C to +150°C

Operating Temperature
5025C Series ..... 0°C to +70°C
5025M Series ..... -55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

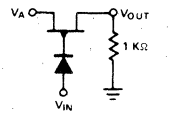
NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 75°C. For higher temperature, derate at rate of 5m/W°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (per channel)

SYMBOL (Note 1)	CHARACTERISTIC	TYPE	TEST CONDITIONS	SPECIFICATION LIMIT				UNIT MIN/MAX
				-55°C (M) 0°C (C)	25°C		+125°C (M) +70°C (C)	
					TYP	MIN/MAX		
$I_{IN(ON)}$	Input Current-ON	All	V_{IN} = 0V		0.30	1.0	100 (M) 25 (C)	nA (max)
$I_{IN(OFF)}$	Input Current-OFF	All	V_{IN} = 15V		0.20	1.0	50 (M) 50 (C)	nA (max)
$V_{IN(ON)}$	Channel Control Voltage-ON	All	See Figure 3	1.5		1.5	1.5	V (max)
$V_{IN(OFF)}$	Channel Control Voltage-OFF	All	See Figure 3	14.0		14.0	14.0	V (min)
$I_{D(OFF)}$	Leakage Current-OFF	All	See Figure 5		0.06	0.5	100 (M) 50 (C)	nA (max)
$I_{D(ON)}$	Leakage Current-ON	Odd Nos.	See Figure 6		1.00	10.0	5000 (M) 250 (C)	nA (max)
$I_{D(ON)}$	Leakage Current-ON	Even Nos.	See Figure 6		0.10	1.0	500 (M) 25 (C)	nA (max)
$r_{DS(ON)}$	Drain-Source ON-Resistance	Odd Nos.	V_{IN} = 0.5V, I_D = 1mA	100	60.00	100.0	250 (M) 150 (C)	Ω (max)
$r_{DS(ON)}$	Drain-Source ON-Resistance	Even Nos.	V_{IN} = 0.5V, I_D = 1mA	150	90.00	150.0	385 (M) 240 (C)	Ω (max)
$r_{DS(ON)}$	Drain-Source ON-Resistance	Odd Nos.	V_{IN} = 1.0V, I_D = 1mA	160	85.00	160.0	420 (M) 250 (C)	Ω (max)
$r_{DS(ON)}$	Drain-Source ON-Resistance	Even Nos.	V_{IN} = 1.0V, I_D = 1mA		110.00	200.0	400 (M) 250 (C)	Ω (max)
$t_{(on)}$	Turn-ON Time	All	See Figure 4		0.10	0.2	0.4	μs (max)
$t_{(off)}$	Turn-OFF Time	All	See Figure 4		0.10	0.2	0.4	μs (max)
$Q_{(INJ)}$	Charge Injection	All	See Figure 5		7.0	20.0		mV_{p-p} (max)
$V_{A(OFF)}$	Cross Coupling Rejection	All	See Figure 6		0.10	1.0		mV_{p-p} (max)
$\Delta r_{DS(ON)}$	Channel to Channel $r_{DS(ON)}$ Match	All	V_{IN} = 0.5V, I_D = 1mA		25.00			Ω (max)

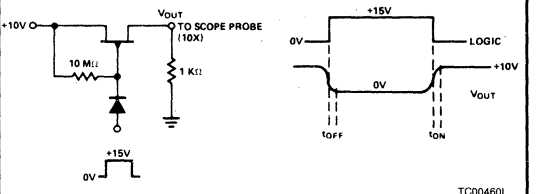
Note 1: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.



FET "ON" FOR $V_{IN} \leq$ 1.5V
FET "OFF" FOR $V_{IN} \geq$ 14.0V

TC00450I

Figure 3: Test Circuits



TC00460I

Figure 4: Test Circuits

Note: All typical values have been guaranteed by characterization and are not tested.

IH5025-IH5038

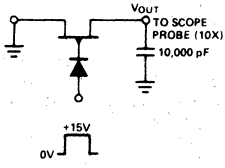


Figure 5: Test Circuits

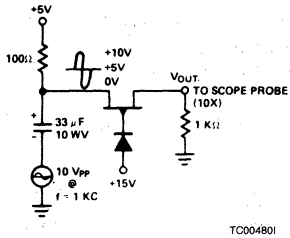
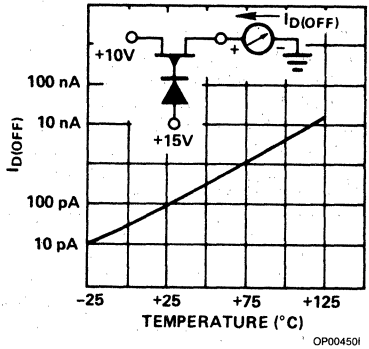


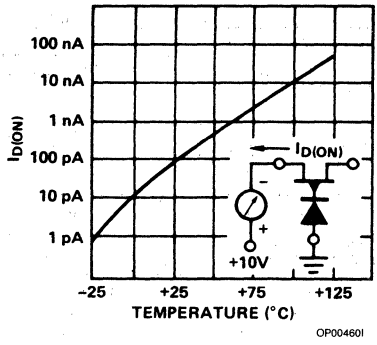
Figure 6: Test Circuits

TYPICAL PERFORMANCE CHARACTERISTICS (per channel)

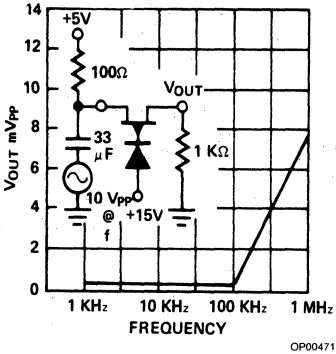
$I_{D(OFF)}$ VS. TEMPERATURE



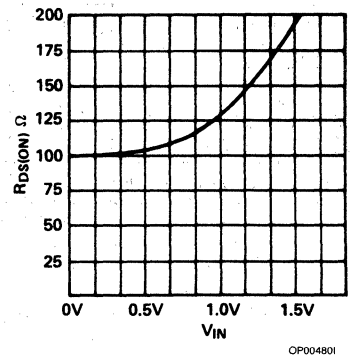
$I_{D(ON)}$ VS. TEMPERATURE



CROSS COUPLING REJECTION VS. FREQUENCY



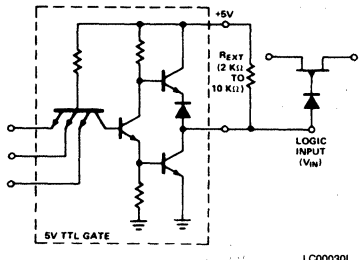
$R_{DS(ON)}$ VS. V_{IN}



Note: All typical values have been guaranteed by characterization and are not tested.

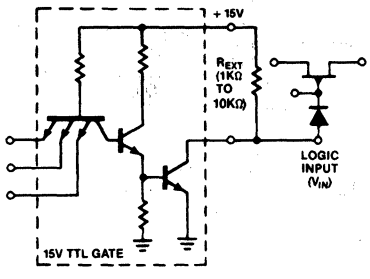
LOGIC INTERFACE CIRCUITS

When operating with TTL logic it is necessary to use pull-up resistors as shown in Figures 6 and 7. This ensures the necessary positive voltages for proper gating action.



LC00030I

Figure 7: Interfacing with +5V Logic



LC00041I

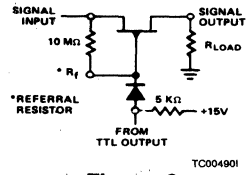
Figure 8: Interfacing with +15V Open Collector Logic

THEORY OF OPERATION

The IH5025 series differs from the IH5009 series in that they may be driven by floating outputs. This family is generally used when operating into the non-inverting input of an operational amplifier, while the IH5009 series is used in operations where the output feeds into the inverting (virtual ground) input.

The IH5025 model is a basic charge area switching device, in that proper gating action depends upon the capacitance vs. voltage relationship for the diode junctions. This C vs. V, when integrated, produces total charge Q. It is Q total which is switched between the series diode and the gate to source and gate to drain junctions. The charge area (C vs. V) for the diode has been chosen to be a minimum of four (4) times the area of the gate to source junction, thus providing adequate safety margins to insure proper switching action.

If normal logical voltage levels of ground to +15V (open collector TTL) are used, only signals which are between 0V and +10V can be switched. The pinch-off range of the P-Channel FET has been selected between 2.0V and 3.9V; thus with +15V at the logical input, and a +10V signal input, 1.1V of margin exists for turn-off. When the IH5025 is used with 5V TTL logic, a maximum of +1V can be switched. The gate of each FET has been brought out so that a "referral resistor" can be placed between gate and source. This is used to minimize charge injection effects. The connection is shown below:

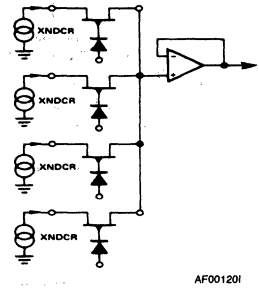


TC00490I

Figure 9

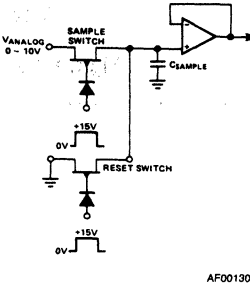
For switching levels > +10V, the +15V power supply must be increased so that there is a minimum of 5V of difference between supply and signal. For example, to switch +15V level, +20V TTL supply is required. Up to +20V levels can be gated.

APPLICATIONS



AF00120I

Figure 10: Multiplexer from Positive Output Transducers



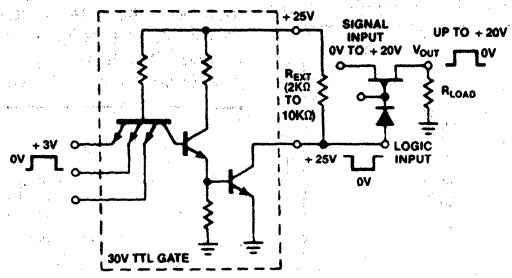
AF00130I

Figure 11: Sample and Hold Switch

Note: All typical values have been guaranteed by characterization and are not tested.

IH5025-IH5038

APPLICATIONS (CONT.)



AF00141I

Figure 12: Switching up to +20V Signals with TTL Logic

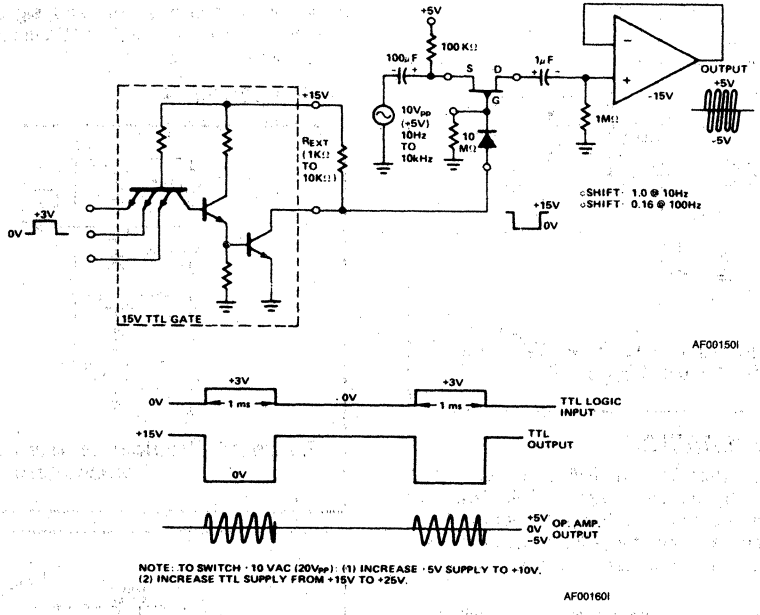
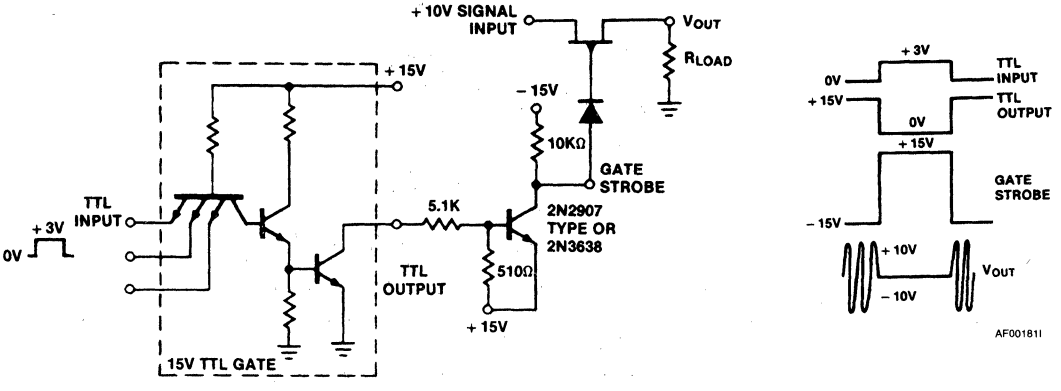


Figure 13: Switching Bipolar Signals with TTL Logic

Note: All typical values have been guaranteed by characterization and are not tested.

APPLICATIONS (CONT.)



ADVANTAGES OVER FIGURE NO. 10 METHOD

A. DC LEVELS OF UP TO ±10V CAN BE SWITCHED, AS WELL AS AC SIGNALS UP TO 100kHz; NO. 10 METHOD SWITCHES ONLY AC RANGE OF 10MHz TO 10kHz.

B. CKT IS NOW BREAK BEFORE MAKE

DISADVANTAGES

A. PNP CKT DRAWS 3mA, WHEN ON; THUS ADDS 3mA x 30V = 90mW POWER DISS.

B. t_{ON} TIME WILL BE CONSIDERABLY SLOWED DOWN FROM 100ns (BEFORE IN FIGURE NO. 13 TO) 1–2μs NOW.

Figure 14: Switching Bipolar Signals with TTL Logic (Alternate Method)

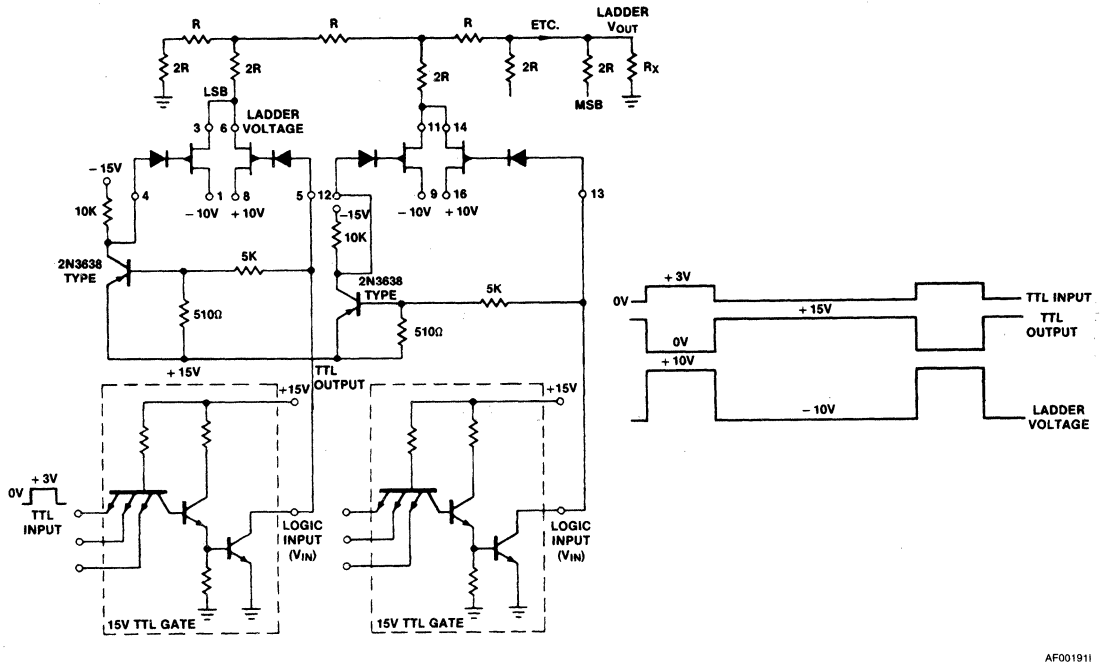


Figure 15: Using the IH5028 as a Dual SPDT Switch to Drive Ladder Networks for Bipolar Switching (up to ±10V)

Note: All typical values have been guaranteed by characterization and are not tested.

IH5025-IH5038

APPLICATIONS (CONT.)

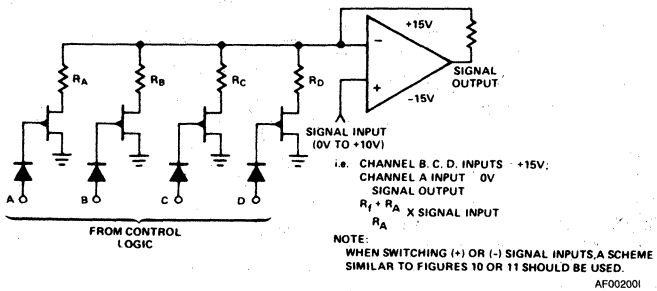


Figure 16: Gain Control with High Input Impedance

Note: All typical values have been guaranteed by characterization and are not tested.

IH5040-IH5047
High-Level CMOS Analog Switch

GENERAL DESCRIPTION

The IH5040 family of solid state analog switches use an improved, high voltage CMOS monolithic technology. These devices provide ease-of-use and performance advantages not previously available from solid state switches. This improved CMOS technology provides input overvoltage capability to ±25 volts without damage to the device, and destructive latch-up has been eliminated. Early CMOS switches were destroyed when power supplies were removed with an input signal present. The IH5040 CMOS technology has eliminated this serious problem.

Key performance advantages of the 5040 series are TTL compatibility and ultra low-power operation. The quiescent current requirement is less than 1μA. Also, the 5040 guarantees Break-Before-Make switching, accomplished by extending the t_{on} time (300ns TYP.) so that it exceeds t_{off} time (200ns TYP.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. The need for external logic required to avoid channel to channel shorting during switching is eliminated.

Many of the 5040 series improve upon and are pin-for-pin and electrical replacements for other solid state switches.

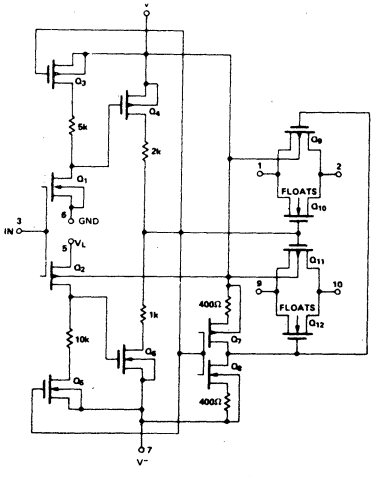
FEATURES

- **Switches Greater Than 20Vpp Signals With ±15V Supplies**
- **Quiescent Current Less Than 1μA**
- **Overvoltage Protection to ±25V**
- **Break-Before-Make Switching t_{off} 200ns, t_{on} 300ns Typical**
- **TTL, DTL, CMOS, PMOS Compatible**
- **Non-Latching With Supply Turn-Off**
- **New DPDT & 4PST Configurations**
- **Complete Monolithic Construction**

ORDERING INFORMATION

IH5040 M JE

- JE — Package
  - DE –16-Pin Ceramic DIP (Special Order Only)
  - FD-2 – 14-Pin Flatpak
  - JE – 16-Pin CERDIP
  - PE – 16-Pin Plastic DIP
  - TW – TO-100 Metal Can (IH5041/2, IH5044)
- M — Temperature Range
  - M – Military (–55°C to +125°C)
  - C – Commercial (0°C to +70°C)
- IH5040 — Basic Part Number



LD00170I

Figure 1: Functional Driver, Typical Driver, Gate — IH5042

FUNCTIONAL DESCRIPTION

INTERSIL PART NO.	TYPE	$r_{DS(on)}$	PIN FOR PIN COMPATIBLE
IH5040	SPST	75Ω	HI5040/DG5040
IH5041	Dual SPST	75Ω	HI5041/DG5041
IH5042	SPDT	75Ω	HI5042/DG5042
IH5043	Dual SPDT	75Ω	HI5043/DG5043
IH5044	DPST	75Ω	HI5044/DG5044
IH5045	Dual DPST	75Ω	HI5045/DG5045
IH5046	DPDT	75Ω	HI5046
IH5047	4PST	75Ω	HI5047

NOTE 1. See Switching State diagrams for applicable package equivalency.

3

Note: All typical values have been guaranteed by characterization and are not tested.

IH5040-IH5047

INTERSIL

ABSOLUTE MAXIMUM RATINGS

V^+-V^- ..... < 33V
V^+-V_D ..... < 30V
V_D-V^- ..... < 30V
V_D-V_S ..... < ±22V
V_L-V^- ..... < 33V
V_L-V_{IN} ..... < 30V
V_L-GND ..... < 20V
V_{IN}-GND ..... < 20V

Current (Any Terminal) ..... < 30mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Power Dissipation 450mW
(All Leads Soldered to a P.C. Board)
Derate 6mW/°C Above 70°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (@ 25°C, V^+ = +15V, V^- = −15V, V_L = +5V)

PER CHANNEL		TEST CONDITIONS	MIN/MAX LIMITS						UNIT
			MILITARY			COMMERCIAL			
SYMBOL	CHARACTERISTIC		−55°C	+25°C	+125°C	0	+25°C	+70°C	
$I_{IN(ON)}$	Input Logic Current	V_{IN} = 2.4V Note 1	±1	±1	10	±1	±1	10	μA
$I_{IN(OFF)}$	Input Logic Current	V_{IN} = 0.8V Note 1	±1	±1	10	±1	±1	10	μA
$r_{DS(on)}$	Drain-Source On Resistance	I_S = 10mA V_{ANALOG} = −10V to +10V	75	75	150	80	80	130	Ω
$\Delta r_{DS(ON)}$	Channel to Channel $r_{DS(ON)}$ Match			25 (typ)			30 (typ)		Ω
V_{ANALOG}	Min. Analog Signal Handling Capability			±11 (typ)			±10 (typ)		V
$I_{D(OFF)}$/ $I_{S(OFF)}$	Switch OFF Leakage Current	V_{ANALOG} = −10V to +10V		±1	100		±5	100	nA
$I_{D(ON)}$ + $I_{S(ON)}$	Switch On Leakage Current	V_D = V_S = −10V to +10V		±2	200		±10	100	nA
t_{on}	Switch "ON" Time	R_L = 1kΩ, V_{ANALOG} = −10V to +10V See Fig. 3		750			1000		ns
t_{off}	Switch "OFF" Time	R_L = 1kΩ, V_{ANALOG} = −10V to +10V See Fig. 3		350			500		ns
$Q_{(INJ.)}$	Charge Injection	See Fig. 3		15 (typ)			20 (typ)		mV
OIRR	Min. Off Isolation Rejection Ratio	f = 1MHz, R_L = 100Ω, C_L ≤ 5pF See Fig. 5		54 (typ)			50 (typ)		dB
I^+_Q	V^+ Power Supply Quiescent Current		1	1	10	10	10	100	μA
I^-_Q	V^- Power Supply Quiescent Current	V^+ = +15V, V = −15V, V_L = +5V V_L = +5V	1	1	10	10	10	100	μA
I^-_{LQ}	+5V Supply Quiescent Current		1	1	10	10	10	100	μA
I_{GND}	Gnd Supply Quiescent Current		1	1	10	10	10	100	μA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off; Any Other Channel Switches as per Fig. 6		54 (typ)			50 (typ)		dB

Note 1: Typical values are for design aid only, not guaranteed and not subject to production testing.

Note: All typical values have been guaranteed by characterization and are not tested.

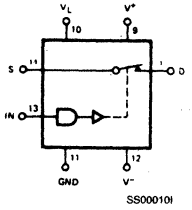
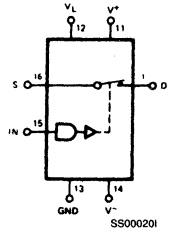
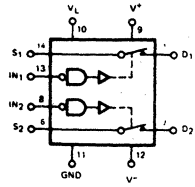
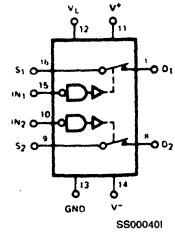
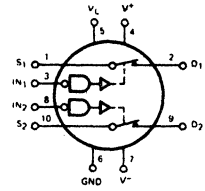
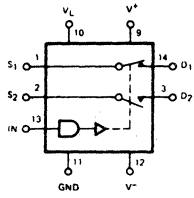
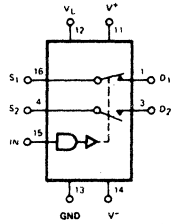
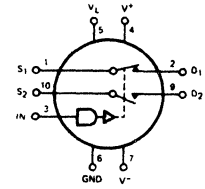
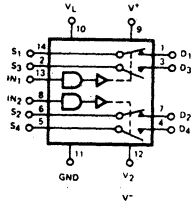
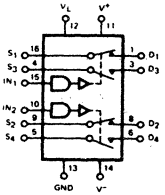
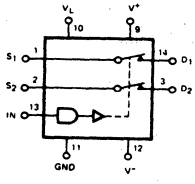
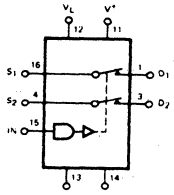
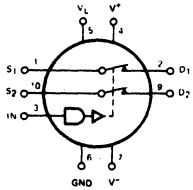
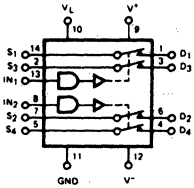
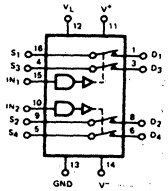
SWITCH STATES ARE FOR LOGIC "1" INPUT	(OUTLINE DWG FD-2)	(OUTLINE DWGS DE, JE, PE)	(OUTLINE DWG TO-100)
SPST IH5040 ($r_{DS(on)} < 75\Omega$)	 SS000101	 SS000201	
DUAL SPST IH5041 ($r_{DS(on)} < 75\Omega$)	 SS000301	 SS000401	 SS000501
SPDT IH5042 ($r_{DS(on)} < 75\Omega$)	 SS000601	 SS000701	(DG188 EQUIVALENT)  SS000801
DUAL SPDT IH5043 ($r_{DS(on)} < 75\Omega$)	 SS000901	(DG191 EQUIVALENT)  SS001001	

Figure 2: Switching State Diagrams

Note: All typical values have been guaranteed by characterization and are not tested.

IH5040-IH5047

INTERSIL

SWITCH STATES ARE FOR LOGIC "1" INPUT	(OUTLINE DWG FD-2)	(OUTLINE DWGS DE, JE, PE)	(OUTLINE DWG TO-100)
DPST IH5044 ($r_{DS(on)} < 75\Omega$)	 SS00110I	 SS00120I	 SS00130I
DUAL DPST IH5045 ($r_{DS(on)} < 75\Omega$)	(DG185 EQUIVALENT)  SS00140I	 SS00150I	

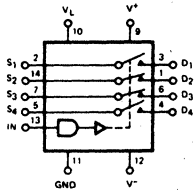
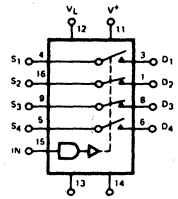
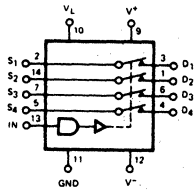
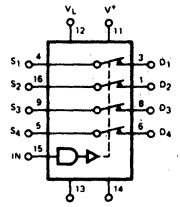
SWITCH STATES ARE FOR LOGIC "1" INPUT	FLAT PACKAGE FD-2)	DIP (DE) PACKAGE	TO-100
DPDT IH5046 ($r_{DS(ON)} < 75\Omega$)	 SS00160I	 SS00170I	
4PST IH5047 ($r_{DS\ (ON)} < 75\Omega$)	 SS00180I	 SS00190I	

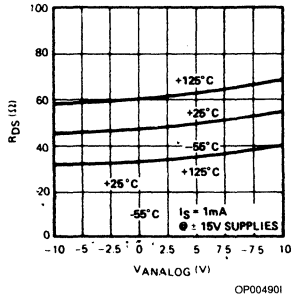
Figure 2: Switching State Diagrams (Cont.)

Note: All typical values have been guaranteed by characterization and are not tested.

IH5040-IH5047

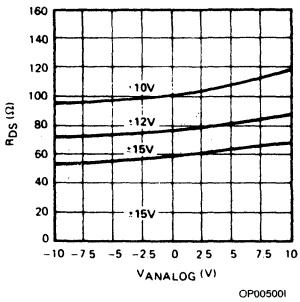
TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel)

$r_{DS(on)}$ vs V_{ANALOG} SIGNAL



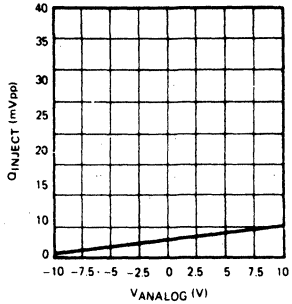
OP00490I

$r_{DS(on)}$ vs POWER SUPPLY VOLTAGE

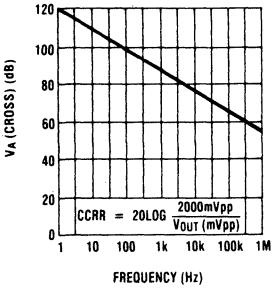


OP00500I

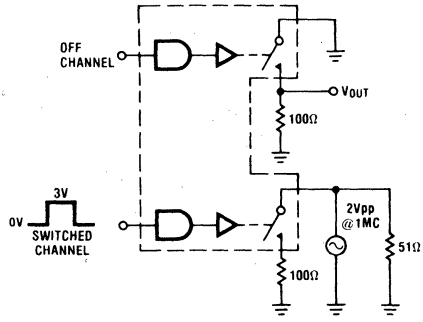
CHARGE INJECTION vs V_{ANALOG} (SEE FIG. B) C_L = 10,000pF



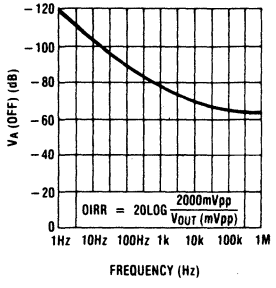
OP00510I



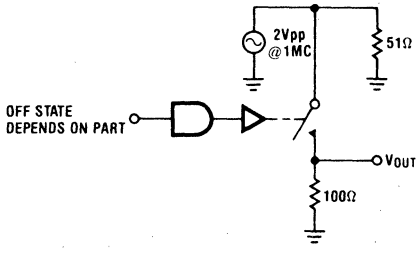
OP00520I



TC00530I



OP00530I



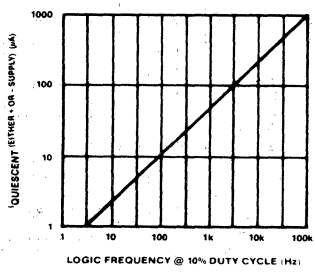
TC00540I

Note: All typical values have been guaranteed by characterization and are not tested.

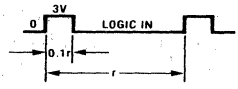
IH5040-IH5047

TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

POWER SUPPLY QUIESCENT CURRENT vs LOGIC FREQUENCY RATE

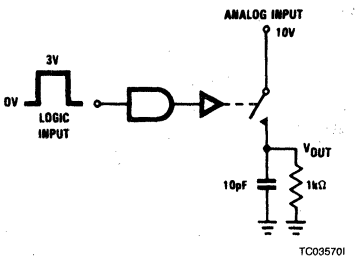


OP005401



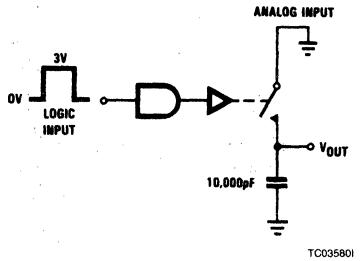
WF001601

TEST CIRCUITS



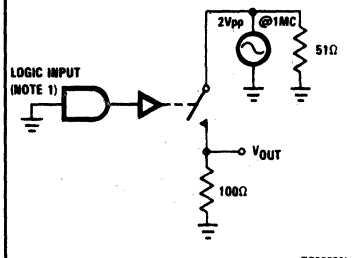
TC035701

Figure 3



TC035801

Figure 4

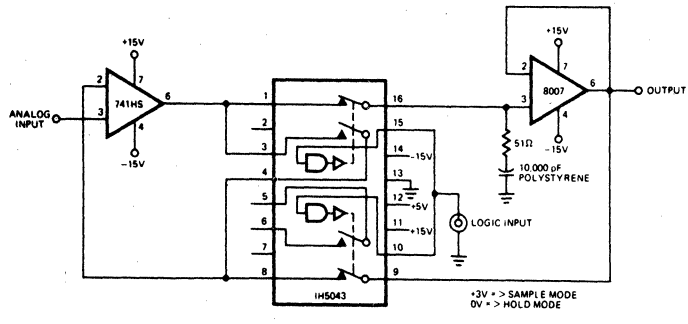


TC035901

Figure 5

NOTE 1: Some channels are turned on by high "1" logic inputs and other channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to see absolute value of logic input required to produce "ON" or "OFF" state.

APPLICATIONS



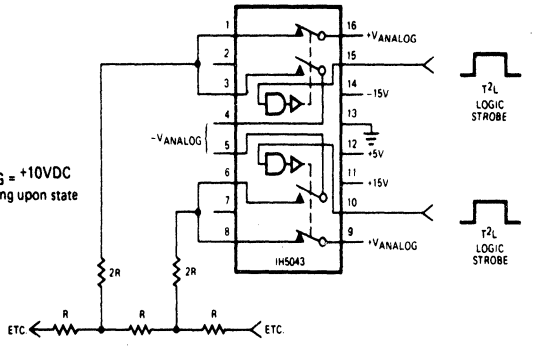
AF005801

Figure 6: Improved Sample & Hold Using IH5043

Note: All typical values have been guaranteed by characterization and are not tested.

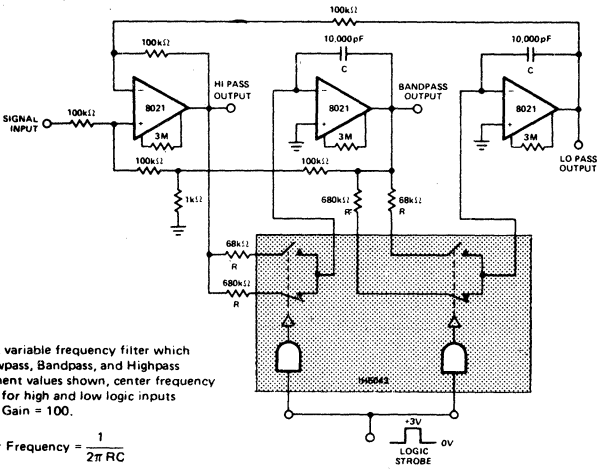
APPLICATIONS (CONT.)

EXAMPLE: If $-V_{ANALOG} = -10VDC$ and $+V_{ANALOG} = +10VDC$ then Ladder Legs are switched between ±10VDC, depending upon state of Logic Strobe.



AF00210I

Figure 7: Using the CMOS Switch to Drive an R/2R Ladder Network (2 Legs)



Constant gain, constant Q, variable frequency filter which provides simultaneous Lowpass, Bandpass, and Highpass outputs. With the component values shown, center frequency will be 235Hz and 23.5Hz for high and low logic inputs respectively, Q = 100, and Gain = 100.

$$f_n = \text{Center Frequency} = \frac{1}{2\pi RC}$$

AF00220I

Figure 8: Digitally Tuned Low Power Active Filter

Note: All typical values have been guaranteed by characterization and are not tested.

APPLICATIONS (CONT.)

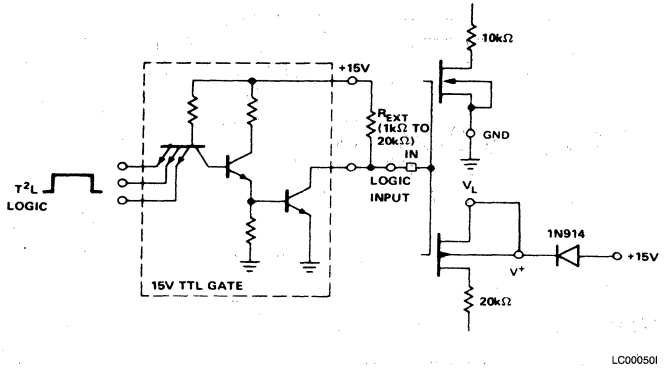


Figure 9: Interfacing with TTL Open Collector Logic (Typ. Example for +15V Case Shown)

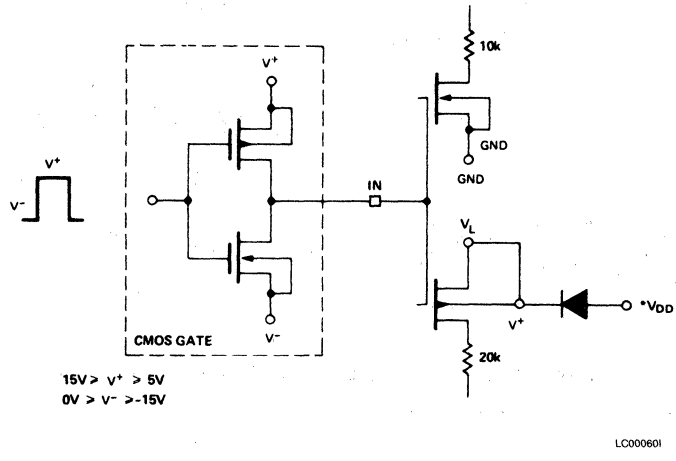


Figure 10: Interfacing with CMOS Logic

Note: All typical values have been guaranteed by characterization and are not tested.

APPLICATIONS (CONT.)

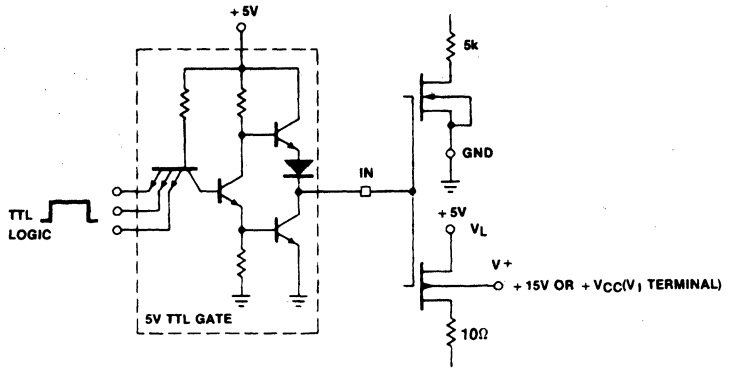


Figure 11: TTL Logic Interface

Note: All typical values have been guaranteed by characterization and are not tested.

IH5048-IH5051
Low Charge Injection CMOS Analog Switches

INTERSIL

GENERAL DESCRIPTION

The IH5048 family of analog switches is especially made for low charge injection and low leakage. Construction includes our CMOS high level driver circuitry combined with unique "VARAFET" switches.

FEATURES

- **Low Charge Injection—5mV (Typ.)**
- **Quiescent Current Less Than 1μA**
- **TTL, DTL, CMOS, PMOS Compatible**
- **Non-Latching With Supply Turn-Off**
- **Low $r_{DS(on)}$ – 35Ω (Typ.)**
- **Pin-Out Compatible With IH5040 Family**

ORDERING INFORMATION

IH5048 M JE

Package
- DE –16-Pin Ceramic DIP (Special Order Only)
- FD-2 – 14-Pin Flatpak
- JE – 16-Pin CERDIP
- PE – 16-Pin Plastic DIP
- TW – TO-100 Metal Can (IH5048, IH5050 Only)

Temperature Range
- M – Military (–55°C to +125°C)
- C – Commercial (0°C to +70°C)

Basic Part Number

ORDERING INFORMATION

INTERSIL PART NO.	TYPE	$r_{DS(on)}$
IH5048 Dual	SPST	35Ω
IH5049 Dual	DPST	35Ω
IH5050	SPDT	35Ω
IH5051 Dual	SPDT	35Ω

NOTE 1. See Switching State diagrams for applicable package equivalency.

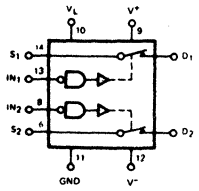
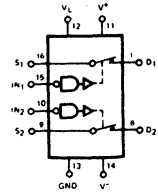
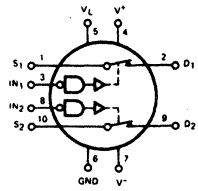
SWITCH STATES ARE FOR LOGIC '1' INPUT	FLAT PACKAGE (FD-2)	DIP (DE) PACKAGE	TO-100
DUAL SPST IH5048 (r_{DS} (ON) < 35Ω)	 SS00200I	 SS00210I	 SS00220I

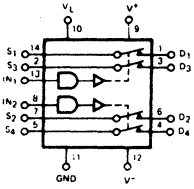
Figure 1: Switching State Diagrams

Note: All typical values have been guaranteed by characterization and are not tested.

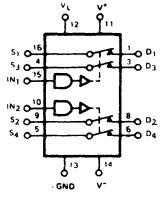
SWITCH STATES ARE FOR LOGIC '1" INPUT	FLAT PACKAGE (FD-2)	DIP (DE) PACKAGE	TO-100

DUAL DPST IH5049
(r_{DS} (ON) < 35Ω)

(DG184 EQUIVALENT)

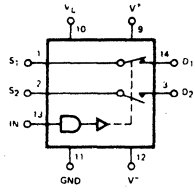


SS00230I

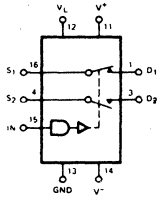


SS00240I

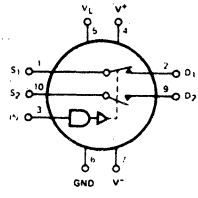
SPDT IH5050
(r_{DS} (ON) < 35Ω)



SS00250I



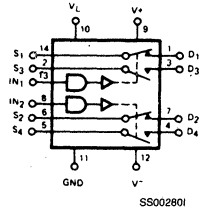
SS00260I



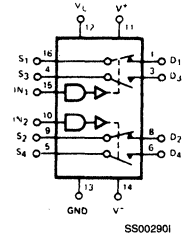
SS00270I

DUAL SPDT IH5051
(r_{DS} (ON) < 35Ω)

(DG190 EQUIVALENT)



SS00280I



SS00290I

Figure 1: Switching State Diagrams (Cont.)

Note: All typical values have been guaranteed by characterization and are not tested.

IH5048-IH5051

ABSOLUTE MAXIMUM RATINGS

$V^+ - V^-$ ..... < 33V
$V^+ - V_D$ ..... < 30V
$V_D - V^-$ ..... < 30V
$V_D - V_S$ ..... < ±22V
$V_L - V^-$ ..... < 33V
$V_L - V_{IN}$ ..... < 30V
$V_L - GND$ ..... < 20V
$V_{IN} - GND$ ..... < 20V

Current (Any Terminal) ..... < 30mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Power Dissipation 450mW
(All Leads Soldered to a P.C. Board)
Derate 6mW/°C Above 70°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (@ 25°C, V^+ = +15V, V^- = −15V, V_L = +5V)

PER CHANNEL		TEST CONDITIONS	MIN/MAX LIMITS						UNIT
			MILITARY			COMMERCIAL			
SYMBOL	CHARACTERISTIC		−55°C	+25°C	+125°C	0	+25°C	+70°C	
$I_{IN(ON)}$	Input Logic Current	V_{IN} = 2.4V Note 1	±1	±1	10	±1	±1	10	µA
$I_{IN(OFF)}$	Input Logic Current	V_{IN} = 0.8V Note 1	±1	±1	10	±1	±1	10	µA
$r_{DS(on)}$	Drain-Source On Resistance	I_S = −10mA V_{ANALOG} = −10V		40	60		45	75	Ω
$\Delta r_{DS(ON)}$	Channel to Channel $r_{DS(ON)}$ Match			15 (Typ)			15 (Typ)		Ω
V_{ANALOG}	Min. Analog Signal Handling Capability			±10			±10		V
$I_{D(OFF)}$/ $I_{S(OFF)}$	Switch OFF Leakage Current	V_{ANALOG} = −10V to +10V		±1	100		±5	100	nA
$I_{D(ON)}$ + $I_{S(ON)}$	Switch On Leakage Current	V_D = V_S = −10V to +10V		±2	200		±10	200	nA
t_{on}	Switch "ON" Time	R_L = 1kΩ, V_{ANALOG} = −10V to +10V See Fig. 2		500			1000		ns
t_{off}	Switch "OFF" Time	R_L = 1kΩ, V_{ANALOG} = −10V to +10V See Fig. 2		250			500		ns
$Q_{(INJ.)}$	Charge Injection	See Fig. 3		1 (Typ)			2 (Typ)		mV
OIRR	Min. Off Isolation Rejection Ratio	f = 1MHz, R_L = 100Ω, C_L ≤ 5pF See Fig. 4, (Note 1)		54 (Typ)			50 (Typ)		dB
I^+_Q	V+ Power Supply Quiescent Current		1	1	10	10	10	100	µA
I^-_Q	V− Power Supply Quiescent Current	V^+ = +15V, V = −15V, V_L = +5V V_L = +5V	1	1	10	10	10	100	µA
I^-_{LQ}	+5V Supply Quiescent Current		1	1	10	10	10	100	µA
I_{GND}	Gnd Supply Quiescent Current		1	1	10	10	10	100	µA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off; Any Other Channel Switches as per Performance Characteristics (Note 1)		54 (Typ)			50 (Typ)		dB

Note 1: Not tested in production.

TEST CIRCUITS

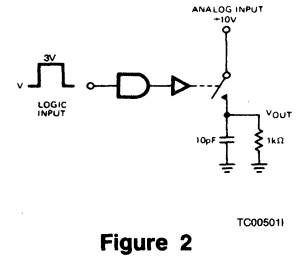


Figure 2

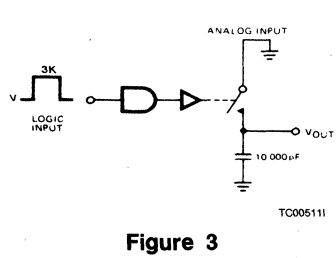


Figure 3

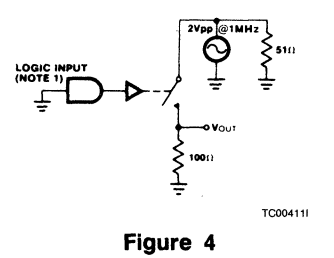


Figure 4

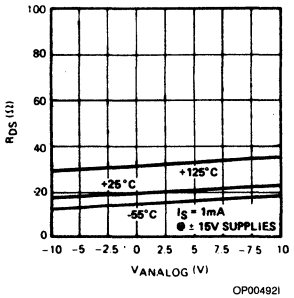
NOTE 1: Some channels are turned on by high "1" logic inputs and other channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to see absolute value of logic input required to produce "ON" or "OFF" state.

Note: All typical values have been guaranteed by characterization and are not tested.

IH5048–IH5051

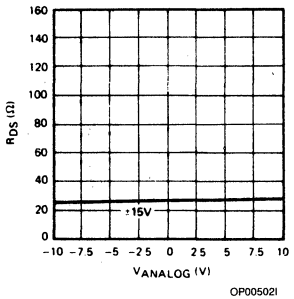
TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel)

$r_{DS(on)}$ vs V_{ANALOG} SIGNAL



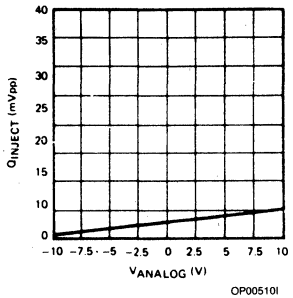
OP00492I

$r_{DS(on)}$ vs POWER SUPPLY VOLTAGE

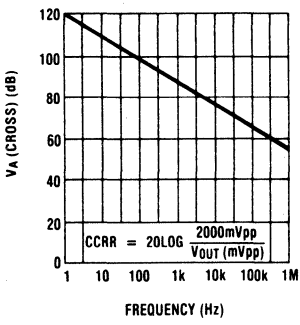


OP00502I

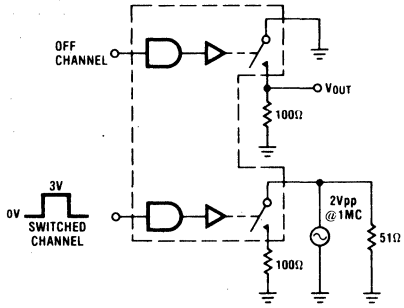
CHARGE INJECTION vs V_{ANALOG} (SEE FIG. 3) C_L = 10,000pF



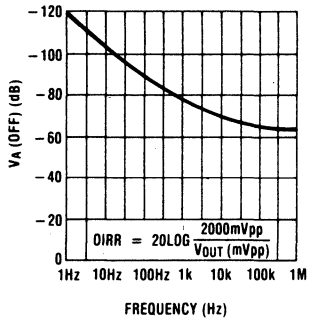
OP00510I



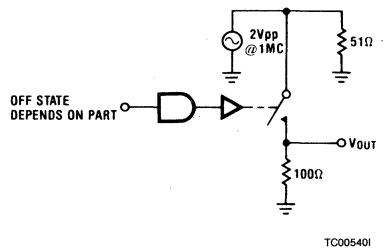
OP00520I



TC00530I



OP00530I



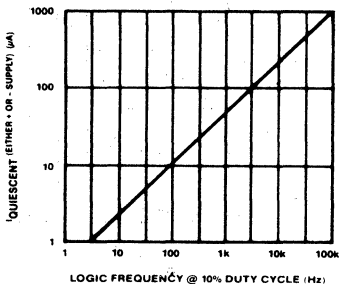
TC00540I

Note: All typical values have been guaranteed by characterization and are not tested.

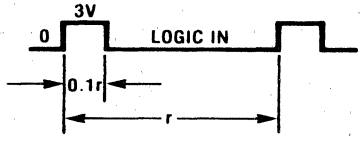
IH5048-IH5051

TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

POWER SUPPLY QUIESCENT CURRENT vs LOGIC FREQUENCY RATE



OP00540I



WF00160I

Note: All typical values have been guaranteed by characterization and are not tested.

IH5052/IH5053
QUAD CMOS Analog Switch

GENERAL DESCRIPTION

The IH5052/3 analog switches use an improved, high voltage CMOS technology, which provides performance advantages not previously available from solid state switches. Early CMOS switches were destroyed when power supplies were removed with an input signal present. The INTERSIL CMOS technology has eliminated this serious systems problem. Key performance advantages are TTL compatibility and ultra low-power operation — the quiescent current requirement is less than 10μA.

The IH5052/3 also guarantees Break-Before-Make switching. This is accomplished by extending the t_{ON} time (400ns TYP.) such that it exceeds t_{OFF} time (200ns TYP.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON, and eliminates the need for external logic required to avoid channel to channel shorting during switching. With a logical "0" (0.8V or less) at its control inputs, the IH5052 switches are closed, while the IH5053 switches are closed with a logical "1" (2.4V or more) at its control inputs.

FEATURES

- **Switches Greater Than 20Vpp Signals With ±15V Supplies**
- **Quiescent Current Less Than 10μA**
- **Overvoltage Protection to ±25V**
- **Break-Before-Make Switching t_{off} 100ns, t_{on} 250ns Typical**
- **TTL, CMOS Compatible**
- **Non-Latching With Supply Turn-Off**
- **IH5052 4 Normally Closed Switches**
- **IH5053 4 Normally Open Switches**

ORDERING INFORMATION

IH505X C JE

- JE — Package: JE = 16-Pin CERDIP; DE = 16-Pin Ceramic DIP (Special Order Only)
- C — Temperature Range: M = Military; C = Commercial
- IH505X — Basic Part Number

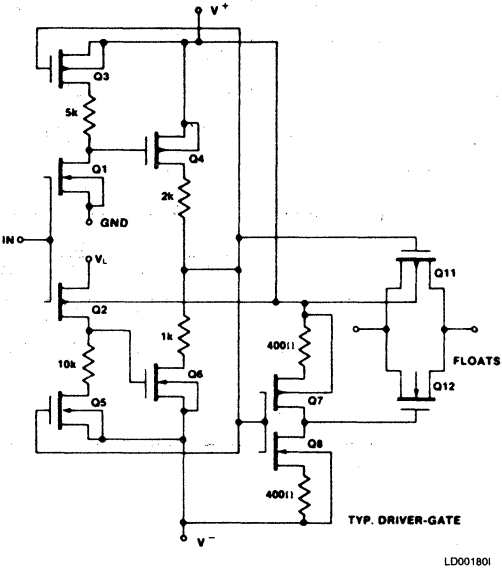


Figure 1: Functional Diagram

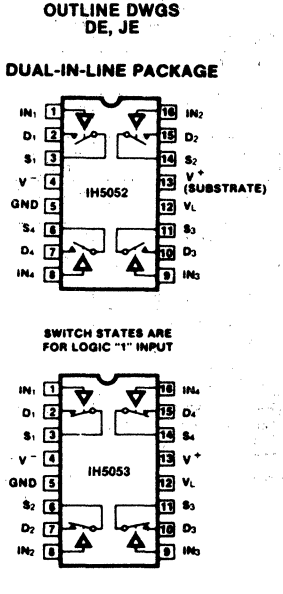


Figure 2: Pin Configurations

Note: All typical values have been guaranteed by characterization and are not tested.

IH5052/IH5053

ABSOLUTE MAXIMUM RATINGS

V^+–V^- ..... < 33V
V^+–V_D ..... < 30V
V_D–V^- ..... < 30V
V_D–V_S ..... < ±22V
V_L–V^- ..... < 33V
V_L–V_{IN} ..... < 30V
V_L–GND ..... < 20V
V_{IN}–GND ..... < 20V

Current (Any Terminal) ..... < 30mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Power Dissipation 450mW
(All Leads Soldered to a P.C. Board)
Derate 6mW/°C Above 70°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = +15V, V^- = −15V, V_L = +5V)

PER CHANNEL		TEST CONDITIONS	MIN/MAX LIMITS						
			MILITARY			COMMERCIAL			
SYMBOL	CHARACTERISTIC		−55°C	+25°C	+125°C	0	+25°C	+70°C	UNIT
$I_{IN(ON)}$	Input Logic Current	V_{IN} = 2.4V (IH5053) = 0.8V (IH5052)	10	±1	10		±10		μA
$I_{IN(OFF)}$	Input Logic Current	V_{IN} = 0.8V (IH5053) = 2.4V (IH5052)	10	±1	10		±10		μA
$r_{DS(ON)}$	Drain-Source On Resistance	I_S = 10mA, V_{analog} = −10V to +10V	75	75	100	80	80	100	Ω
$\Delta r_{DS(ON)}$	Channel to Channel $r_{DS(ON)}$ Match			25 (typ)			30 (typ)		Ω
V_{ANALOG}	Min. Analog Signal Handling Capability			±11 (typ)			±10 (typ)		V
$I_{D(OFF)}$ / $I_{S(OFF)}$	Switch OFF Leakage Current	V_{ANALOG} = −10V to +10V		±1	100		±5	100	nA
$I_{D(ON)}$ + $I_{S(ON)}$	Switch On Leakage Current	V_D = V_S = −10V to +10V		±2	200		±10	100	nA
t_{ON}	Switch "ON" Time	R_L = 1kΩ, V_{analog} = −10V to +10V See Fig. 3		500			1000		ns
t_{OFF}	Switch "OFF" Time	R_L = 1kΩ, V_{analog} = −10V to +10V See Fig. 3		250			500		ns
$Q_{(INJ.)}$	Charge Injection	See Fig. 4		15 (typ)			20 (typ)		mV
OIRR	Min. Off Isolation Rejection Ratio	f = 1MHz, R_L = 100Ω, C_L ≤ 5pF See Fig. 5		54 (typ)			50 (typ)		dB
I^+	+ Power Supply Quiescent Current	V^+ = +15V, V^- = −15V, V_L = +5V with GND	10	10	100	10	10	100	μA
I^-	− Power Supply Quiescent Current		10	10	100	10	10	100	μA
I_{VL}	+5V Supply Quiescent Current		10	10	100	10	10	100	μA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off		54 (typ)			50 (typ)		dB

NOTE 1: Typical values are for design aid only, not guaranteed and not subject to production testing.

Note: All typical values have been guaranteed by characterization and are not tested.

TEST CIRCUITS

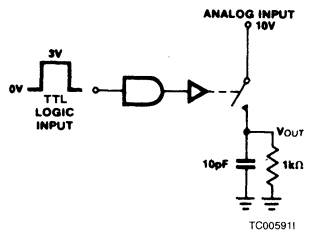


Figure 3

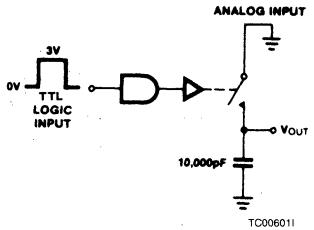


Figure 4

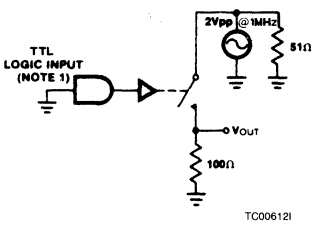
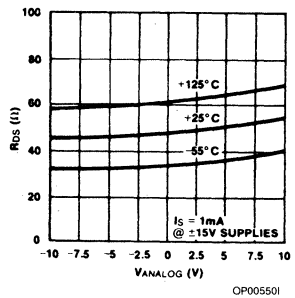


Figure 5

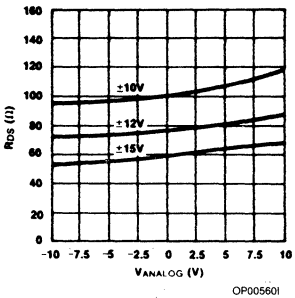
NOTE 1: The 5053 is turned on by high "1" logic inputs and the 5052 is turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to see absolute value of logic input required to produce "ON" or "OFF" state.

TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel)

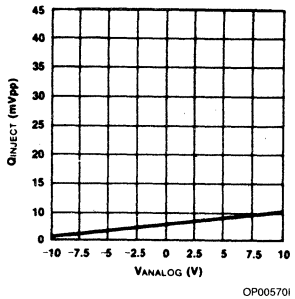
$r_{DS(ON)}$ vs V_{ANALOG} SIGNAL



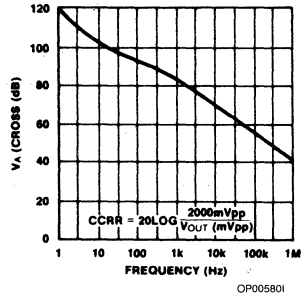
$r_{DS(ON)}$ vs POWER SUPPLY VOLTAGE

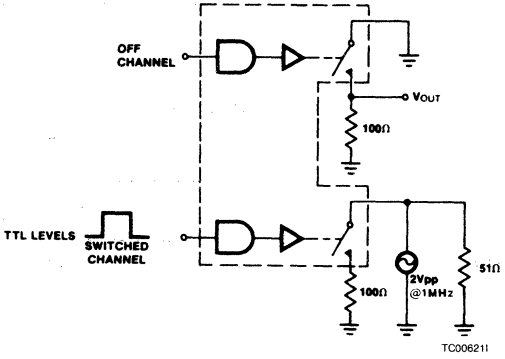


CHARGE INJECTION vs V_{ANALOG} (SEE Figure B) C_L = 10,000pF



CROSS COUPLING REJECTION vs FREQUENCY





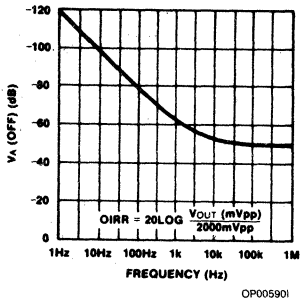
Cross Coupling Rejection Test Circuit

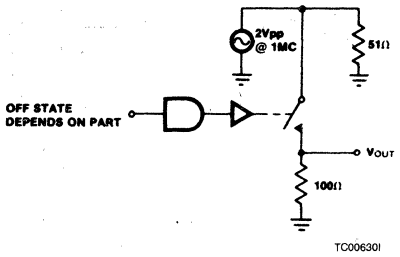
Note: All typical values have been guaranteed by characterization and are not tested.

IH5052/IH5053

TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

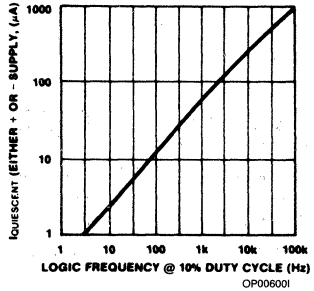
OFF ISOLATION vs FREQUENCY

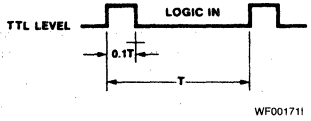




Off Isolation Test Circuit

POWER SUPPLY QUIESCENT CURRENT vs LOGIC FREQUENCY RATE





Logic Input Waveform

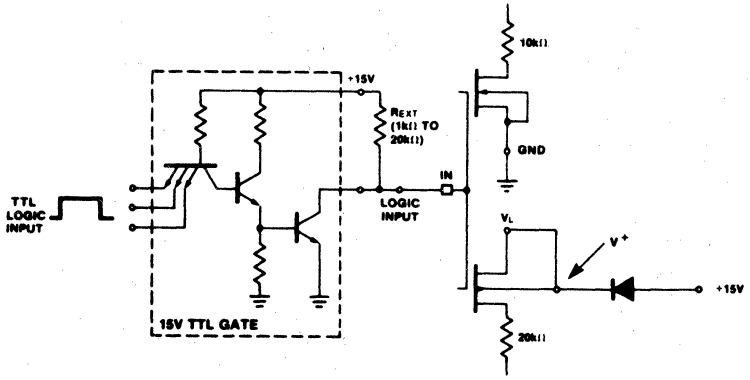


Figure 6: +15V Open Collector TTL Interface to IH5052/5053

Note: All typical values have been guaranteed by characterization and are not tested.

APPLICATIONS

PROGRAMMABLE GAIN NON-INVERTING AMPLIFIER WITH SELECTABLE INPUTS

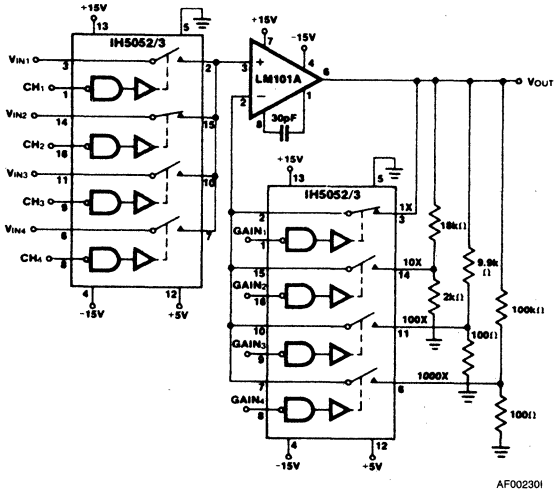
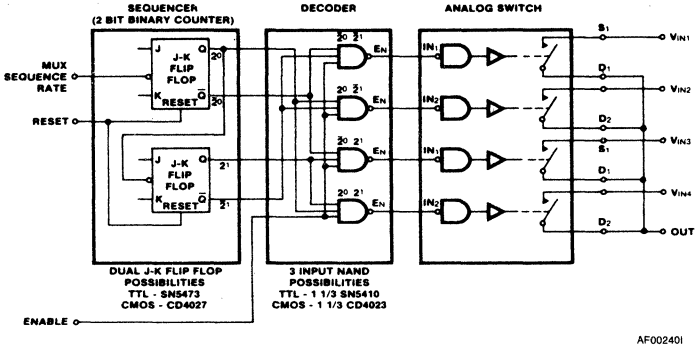


Figure 7: Active Low Pass Filter with Digitally Selected Break Frequency



TRUTH TABLE (IH5052)

ENABLE	MUX SEQUENCE RATE	SEQUENCER OUTPUT		SWITCH STATES (–DENOTES OFF)			
		2^0	2^1	SW1	SW2	SW3	SW4
0	0	0	0	—	—	—	—
1	0	0	0	ON	—	—	—
1	1 pulse	1	0	—	ON	—	—
1	2 pulses	0	1	—	—	—	—
1	3 pulses	1	1	—	—	—	ON
1	4 pulses	0	0	ON	—	—	—

Figure 8: 4-Channel Sequencing MUX

Note: All typical values have been guaranteed by characterization and are not tested.

IH5052/IH5053

A LATCHING DPDT SWITCH

The latch feature insures positive switching action in response to non-repetitive or erratic commands. The A_1 and A_2 inputs are normally low. A HIGH input to A_2 turns S_1 and S_2 ON, a HIGH to A_1 turns S_3 and S_4 ON. Desirable for use with limit detectors, peak detectors, or mechanical contact closures.

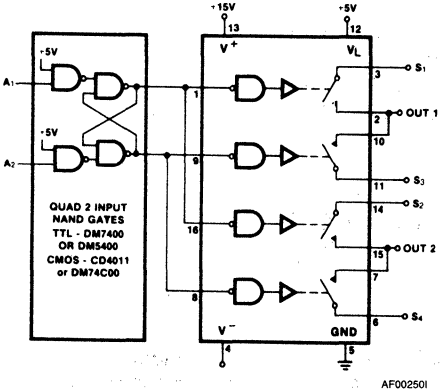


Figure 9: A Latching DPDT

TRUTH TABLE (IH5052)

COMMAND		STATE OF SWITCHES AFTER COMMAND	
A_2	A_1	S_3 & S_4	S_1 & S_2
0	0	same	same
0	1	on	off
1	0	off	on
1	1	INDETERMINATE	

Note: All typical values have been guaranteed by characterization and are not tested.

IH5108
8-Channel Fault Protected CMOS Analog Multiplexer

GENERAL DESCRIPTION

The IH5108 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the HI508A and similar devices, but adds fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to ±25V, even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc.

A binary 3-bit address code together with the ENable input allows selection of any one channel, or none at all. These 4 inputs are all TTL compatible for easy logic interface; the ENable input also facilitates MUX expansion and cascading.

FEATURES

- **All Channels OFF When Power OFF, for Analog Signals up to ±25V**
- **Power Supply Quiescent Current Less Than 1mA**
- **±13V Analog Signal Range**
- **No SCR Latchup**
- **Break-Before-Make Switching**
- **Pin Compatible With HI-508A**
- **Any Channel Turns OFF if Input Exceeds Supply Rails by Up to ±25V**
- **TTL and CMOS Compatible Binary Address and ENable Inputs**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5108MJE	−55°C to +125°C	16 pin CERDIP
IH5108IJE	−20°C to +85°C	16 pin CERDIP
IH5108CPE	0°C to 70°C	16 pin plastic DIP

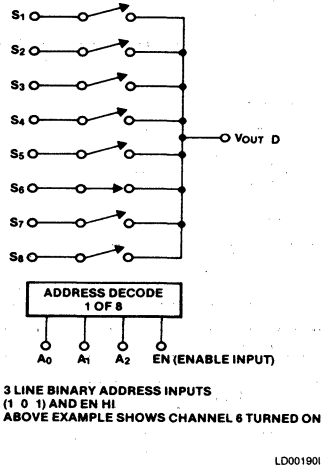


Figure 1: Functional Diagram

DECODE TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

A_0, A_1, A_2, EN
Logic "1" = $V_{AH} \geq 2.4V$
Logic "0" = $V_{AL} \leq 0.8V$

(outline dwg JE, PE)

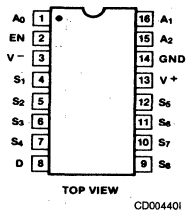


Figure 2: Pin Configuration

Note: All typical values have been guaranteed by characterization and are not tested.

IH5108

INTERSIL

ABSOLUTE MAXIMUM RATINGS

V_{IN}(A, EN) ..... V^- to (V^+ −0.05)
V_{IN}(A, EN) to Ground ..... −15V to 15V
V_S or V_D to V^+ ..... +25V, −40V
V_S or V_D to V^- ..... −25V, +40V
V^+ to Ground 16V
V^- to Ground ..... −16V

Current (Any Terminal) 20mA
Operating Temperature ..... −55 to 125°C
Storage Temperature ..... −65 to 150°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Power Dissipation* 1200mW

*All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V^+ = 15V, V^- = −15V, V_{EN} = 2.4V, unless otherwise specified.)

CHARACTERISTIC	MEASURED TERMINAL	NO TESTS PER TEMP	TEST CONDITIONS		TYP 25°C	MAX LIMITS						UNIT
						M SUFFIX			C SUFFIX			
						−55°C	25°C	125°C	−20°C/ 0°C	25°C	85°C/ 70°C	
SWITCH												
$r_{DS(on)}$	S to D	8	V_D = 10V, I_S = −1.0mA	Sequence each switch on	700	1000	1000	1500	1200	1200	1800	Ω
		8	V_D = −10V I_S = −1.0mA	V_{AL} = 0.8V, V_{AH} = 2.4V	500	1000	1000	1500	1200	1200	1800	
$\Delta r_{DS(on)}$			$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg.}}$ V_S = ±10V		5							%
$I_{S(off)}$	S	8	V_S = 10V, V_D = −10V		0.02		±0.5	50		±1.0	50	nA
		8	V_S = −10V, V_D = 10V		0.02		±0.5	50		±1.0	50	
$I_{D(off)}$	D	1	V_D = 10V, V_S = −10V	V_{EN} = 0.8V	0.02		±1.0	100		±2.0	100	
		1	V_D = −10V, V_S = 10V		0.05		±1.0	100		±2.0	100	
$I_{D(on)}$	D	8	$V_{S(All)}$ = V_D = 10V	Sequence each switch on	0.1		±2.0	100		±5	100	
		8	$V_{S(All)}$ = V_D = −10V	V_{AL} = 0.8V, V_{AH} = 2.4V, V_{EN} = 2.4V	0.1		±2.0	100		±5	100	
FAULT												
I_S with Power OFF	S	8	V_{SUPP} = 0V, V_{IN} = ±25V, V_{EN} = V_O = 0V, A_0, A_1, A_2 = 0V		1.0		2.0			5.0		µA
$I_{S(off)}$ with Overvoltage	S	8	V_{IN} = ±25V, V_O = ±10V		1.0		5.0			10		
INPUT												
$I_{EN(on)}$ $I_{A(on)}$ or $I_{EN(off)}$ $I_{A(off)}$	A_0, A_1, A_2 or EN		V_A = 2.4V or 0V		0.01		±1.0	−30		−10	−30	µA
		4	V_A = 15V or 0V		0.01		±1.0	30		10	30	
DYNAMIC												
$t_{transition}$	D		See Figure 3		0.3		1					µs
t_{open}	D		See Figure 4		0.2							
$t_{on(EN)}$	D		See Figure 5		0.6		1.5					
$t_{off(EN)}$	D				0.4		1					
t_{on}-t_{off} Break-Before-Make Delay Settling Time	D	8	V_{EN} = +5V, A_0, A_1, A_2 Strobed V_{IN} = ±10V, Figure 6		10							
"OFF" Isolation	D		V_{EN} = 0, R_L = 200Ω, C_L = 3pF, V_S = 3 VRMS, f = 500kHz		60							dB
$C_{S(off)}$	S		V_S = 0	V_{EN} = 0V,	5							pF
$C_{D(off)}$	D		V_D = 0	f = 140kHz	25							
$C_{DS(off)}$	D to S		V_S = 0, V_D = 0	to 1 MHz	1							

Note: All typical values have been guaranteed by characterization and are not tested.

CHARACTERISTIC	MEASURED TERMINAL	NO TESTS PER TEMP	TEST CONDITIONS	TYP 25°C	MAX LIMITS						UNIT
					M SUFFIX			C SUFFIX			
					-55°C	25°C	125°C	-20°C/ 0°C	25°C	85°C/ 70°C	
SUPPLY											
Supply Current	I^+	1	V_{EN} = 5V	0.5	0.7	0.6	0.5		1.0		mA
	I^-	1	All V_{ADD} = 0V/5V	0.02	0.7	0.6	0.5		1.0		

Note 1. Readings taken 400ms after the overvoltage occurs.

SWITCHING TIME TEST CIRCUITS

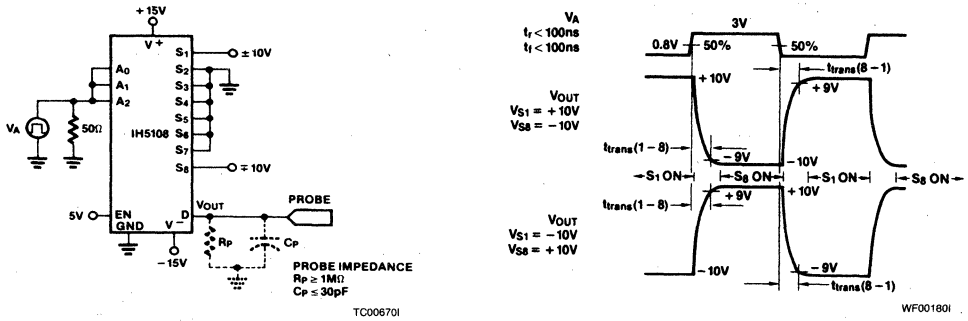


Figure 3: $t_{transition}$ Switching Test Circuit and Waveforms

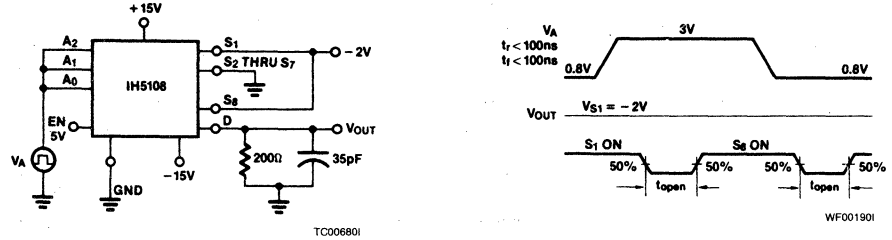


Figure 4: t_{open} (Break-Before-Make) Switching Test Circuit and Waveforms

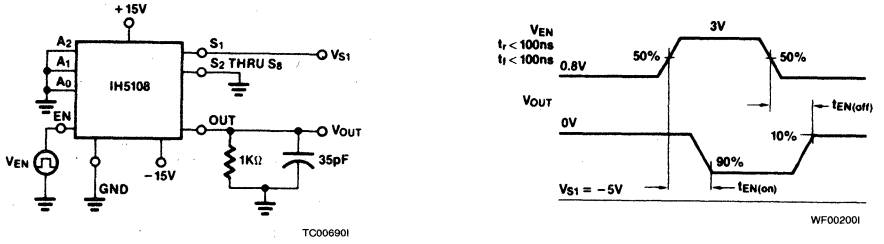


Figure 5: t_{on} and t_{off} Switching Test Circuit and Waveforms

Note: All typical values have been guaranteed by characterization and are not tested.

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SWITCHING TIME TEST CIRCUITS (CONT.)

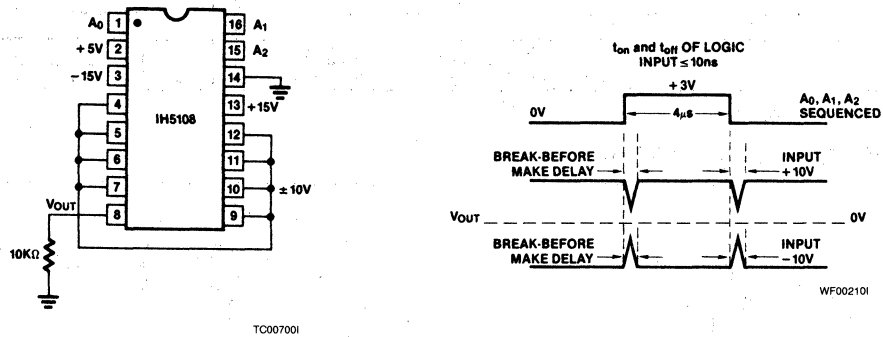


Figure 6: Break-Before-Make Delay Test Circuit and Waveforms

DETAILED DESCRIPTION

The IH5108, like all Intersil's multiplexers, contains a set of CMOS switches that form the channels, and driver and decoder circuitry to control which channel turns ON, if any. In addition, the IH5108 contains an internal regulator which provides a fully TTL compatible ENable input that is identical in operation to the Address inputs. This does away with the special conditions that many multiplexer enable inputs require for proper logic swings. The identical circuit conditions of the ENable and Address lines also helps ensure the extension of break-before-make switching to wider multiplexer systems (see applications section).

Another, and more important difference lies in the switching channel. Previous devices have used parallel n- and p-channel MOSFET switches. While this scheme yields reasonably good ON resistance characteristics and allows the switching of rail-to-rail input signals, it also has a number of drawbacks. The sources and drains of the switch transistors will conduct to the substrate if the input goes outside the supply rails, and even careful use of diodes cannot avoid channel-to-output and channel-to-channel coupling in cases of input overrange. The IH5108 uses a novel series arrangement of the p- and n-channel switches (Figure 7) combined with a dielectrically isolated process to eliminate these problems.

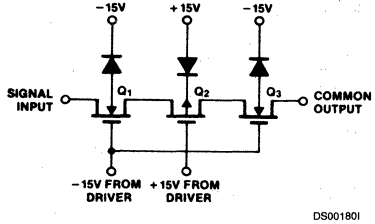
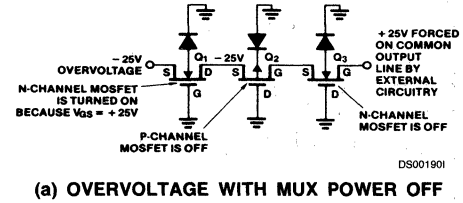
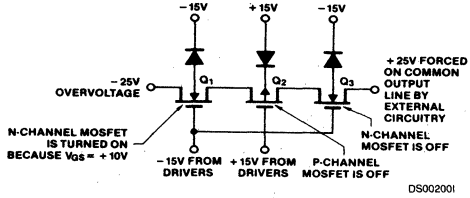


Figure 7: Series Connection of Channel Switches

Within the normal analog signal range, the inherent variation of switch ON resistance will balance out almost as well as the customary parallel configuration, but as the analog signal approaches either supply rail, even for an ON channel, either the p- or the n-channel will become a source follower, disconnecting the channel (Figure 8). Thus protection is provided for any input or output channel against overvoltage, even in the absence of multiplexer supply voltages. This applies up to the breakdown voltage of the respective switches. Figure 9 shows a more detailed schematic of the channel switches, including the back-gate driver devices which ensure optimum channel ON resistances and breakdown voltage under the various conditions.



(a) OVERVOLTAGE WITH MUX POWER OFF



(b) OVERVOLTAGE WITH MUX POWER ON

Figure 8: Overvoltage Protection

Under some circumstances, if the logic inputs are present but the multiplexer supplies are not, the circuit will use the logic inputs as a sort of phantom supply; this could result in an output up to that logic level. To prevent this from

Note: All typical values have been guaranteed by characterization and are not tested.

DETAILED DESCRIPTION (CONT.)

occurring, simply ensure that the ENable pin is LOW any time the multiplexer supply voltages are missing (Figure 10).

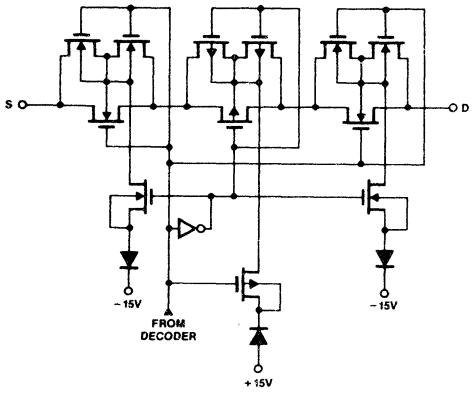


Figure 9: Detailed Channel Switch Schematic

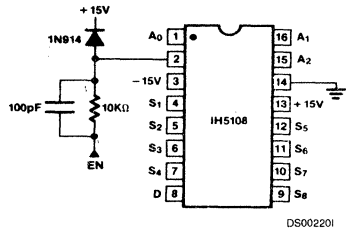


Figure 10: Protection Against Logic Input

MAXIMUM SIGNAL HANDLING CAPABILITY

The IH5108 is designed to handle signals in the ±10V range, with a typical $r_{DS(on)}$ of 600Ω; it can successfully handle signals up to ±13V, however, $r_{DS(on)}$ will increase to about 1.8kΩ. Beyond ±13V the device approaches an open circuit, and thus ±12V is about the practical limit, see Figure 11.

Figure 12 shows the input/output characteristics of an ON channel, illustrating the inherent limiting action of the series switch connection (see Detailed Description), while Figure 13 gives the ON resistance variation with temperature.

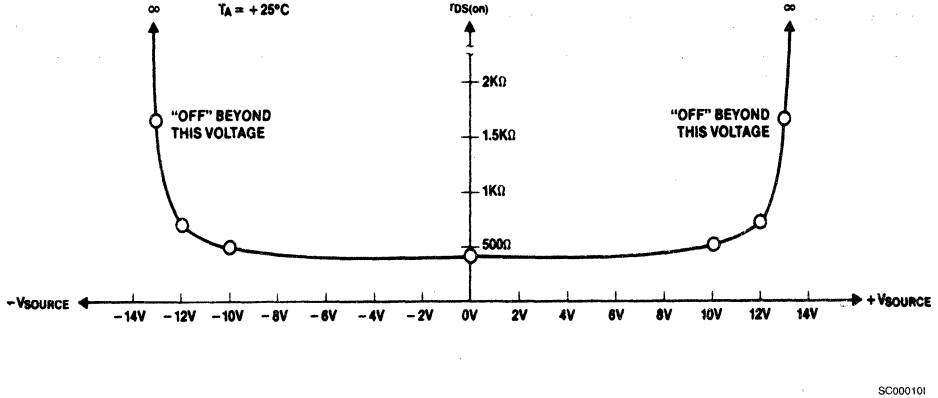


Figure 11: $r_{DS(on)}$ vs Signal Output Voltage @ T_A = +25°C

Note: All typical values have been guaranteed by characterization and are not tested.

IH5108

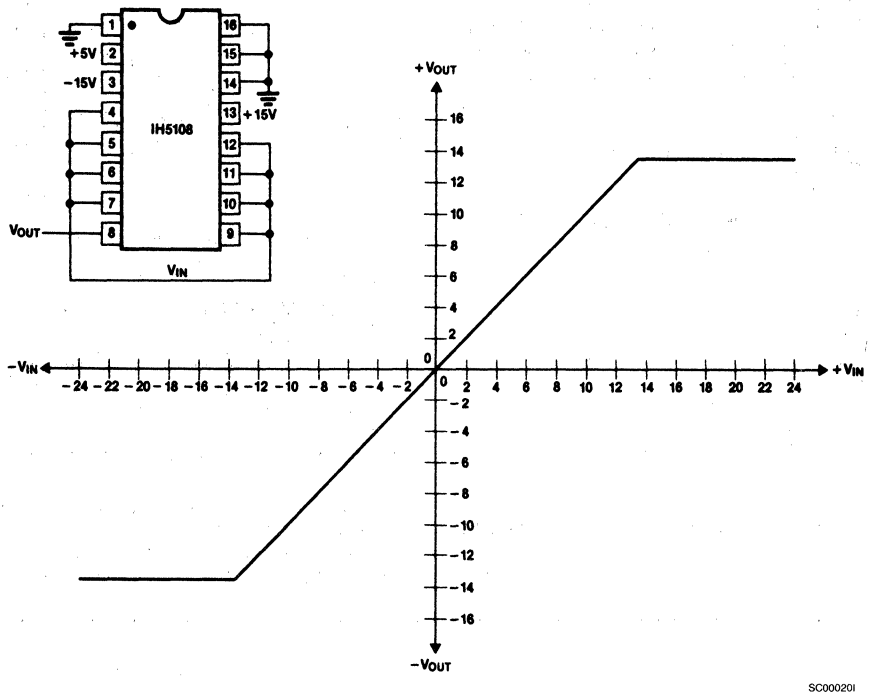


Figure 12: MUX Output Voltage vs Input Voltage (Channel 1 Shown; All Channels Similar)

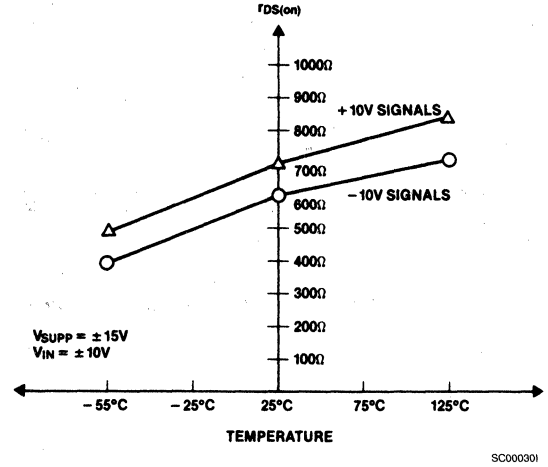


Figure 13: Typical $r_{DS(on)}$ Variation With Temperature

Note: All typical values have been guaranteed by characterization and are not tested.

USING THE IH5108 WITH SUPPLIES OTHER THAN ±15V

The IH5108 will operate successfully with supply voltages from ±5V to ±15V, however $r_{DS(on)}$ increases as supply voltage decreases, as shown in Figure 14. Leakage currents, on the other hand, decrease with a lowering of supply voltage, and therefore the error term product of $r_{DS(on)}$ and leakage current remains reasonably constant. $r_{DS(on)}$ also decreases as signal levels decrease. For high system accuracy [acceptable levels of $r_{DS(on)}$] the maximum input signal should be 3V less than the supply voltages. The logic levels remain TTL compatible.

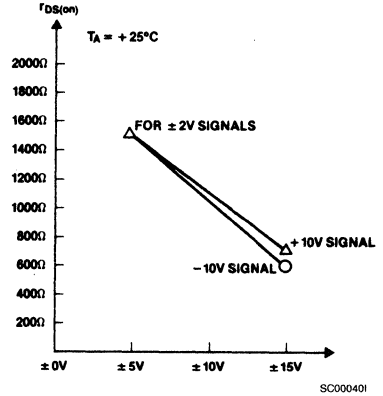


Figure 14: Typical $r_{DS(on)}$ Variation With Supply Voltages

APPLICATION NOTES

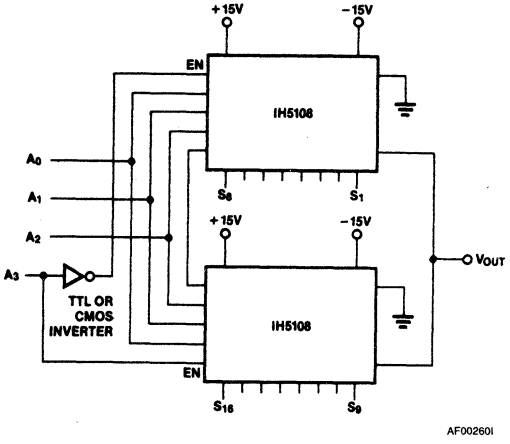
Further information may be found in:

A003 "Understanding and Applying the Analog Switch," by Dave Fullagar

A006 "A New CMOS Analog Gate Technology," by Dave Fullagar

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Slieger

IH5108 APPLICATIONS INFORMATION



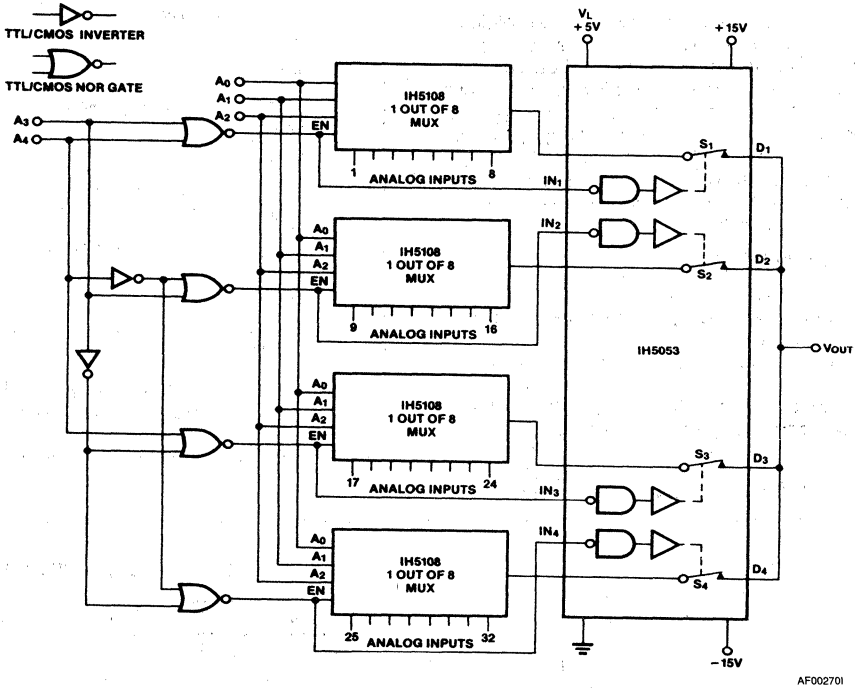
DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	ON SWITCH
0	0	0	0	S1
0	0	0	1	S2
0	0	1	0	S3
0	0	1	1	S4
0	1	0	0	S5
0	1	0	1	S6
0	1	1	0	S7
0	1	1	1	S8
1	0	0	0	S9
1	0	0	1	S10
1	0	1	0	S11
1	0	1	1	S12
1	1	0	0	S13
1	1	0	1	S14
1	1	1	0	S15
1	1	1	1	S16

Figure 15: 1 of 16 Channel Multiplexer Using Two IH5108s. Overvoltage Protection Is Maintained Between All Channels, As Is Break-Before-Make Switching.

Note: All typical values have been guaranteed by characterization and are not tested.

IH5108 APPLICATIONS INFORMATION (CONT.)



DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16

DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
1	0	0	0	0	S17
1	0	0	0	1	S18
1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

Figure 16: 1 Of 32 Multiplexer Using 4 IH5108s and An IH5053 As A Submultiplexer. Note That The IH5053 Is Protected Against Overvoltages By The IH5108s. Submultiplexing Reduces Output Leakage and Capacitance.

Note: All typical values have been guaranteed by characterization and are not tested.

IH5116
16-Channel Fault Protected CMOS Analog Multiplexer

INTERSIL

GENERAL DESCRIPTION

The IH5116 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the HI506A and similar devices, but adding fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to ±25V, even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc. Cross talk onto "good" channels is also prevented.

A binary 2-bit address code together with the ENable input allows selection of any channel pair or none at all. These 3 inputs are all TTL compatible for easy logic interface. The ENable input also facilitates MUX expansion and cascading.

FEATURES

- **All Channels OFF When Power OFF, for Analog Signals Up to ±25V**
- **Power Supply Quiescent Current Less Than 1mA**
- **±13V Analog Signal Range**
- **No SCR Latchup**
- **Break-Before-Make Switching**
- **TTL and CMOS Compatible Strobe Control**
- **Pin Compatible With HI506A**
- **Any Channel Turns OFF If Input Exceeds Supply Rails By Up to ±25V**
- **TTL and CMOS Compatible Binary Address and ENable Inputs**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5116MJI	−55°C to +125°C	28 pin CERDIP
IH5116CJI	0°C to +70°C	28 pin CERDIP
IH5116CPI	0°C to +70°C	28 pin Plastic DIP

Ceramic package available as special order only (IH5116MDI/CDI)

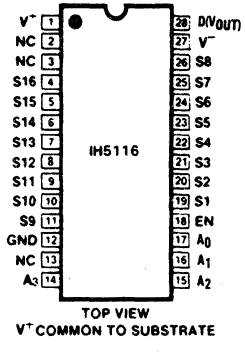


Figure 1: Pin Configuration (Outline dwg JE, PE)

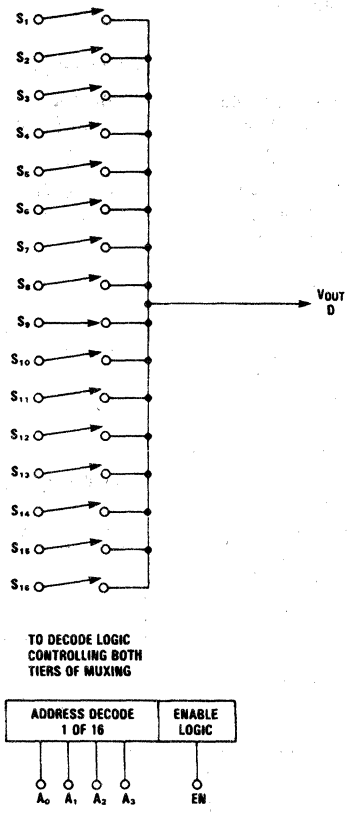
DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	EN	ON SWITCH
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

Logic "1" = $V_{AH} \geq 2.4V$ $V_{ENH} \geq 2.4V$
Logic "0" = $V_{AL} \leq 0.8V$

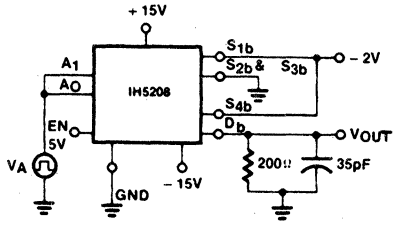
Note: All typical values have been guaranteed by characterization and are not tested.

IH5116

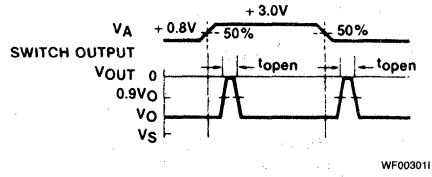


LD011311

Figure 2: Functional Diagram



TC038501



WF003011

Figure 3: t_{open} (Break-Before-Make) Switching Test

Note: All typical values have been guaranteed by characterization and are not tested.

IH5116

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V to +15V
V_S or V_D to V^+ ..... +25V to −40V
V_S or V_D to V^- ..... −25V to +40V
V^+ to Ground 16V
V^- to Ground ..... −16V

Current (Any Terminal) 20mA
Operating Temperature ..... −55 to +125°C
Storage Temperature ..... −65 to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Power Dissipation* 1200mW

*All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V^+ = 15V, V^- = −15V, V_{EN} = 2.4V, unless otherwise specified.)

CHARACTERISTIC		MEASURED TERMINAL	NO TESTS PER TEMP	TEST CONDITIONS		TYP 25°C	MAX LIMITS M SUFFIX −55°C	M SUFFIX 25°C	M SUFFIX 125°C	C SUFFIX 0°C	C SUFFIX 25°C	C SUFFIX 70°C	UNIT
SWITCH													
$R_{DS(on)}$		S to D	16	V_D = 10V, I_S = −1.0mA	Sequence each switch on	700	1000	1000	1500	1200	1200	1800	Ω
			16	V_D = −10V I_S = −1.0mA	V_{AL} = 0.8V, V_{AH} = 2.4V	500	1000	1000	1500	1200	1200	1800	
$\Delta R_{DS(on)}$				$\Delta R_{DS(on)} = \frac{R_{DS(on)max} - R_{DS(on)min}}{R_{DS(on)avg.}}$ V_S = ±10V		5							%
$I_{S(off)}$		S	16	V_S = 10V, V_D = −10V	V_{EN} = 0.8V	0.02		±0.5	50		±1.0	50	nA
			16	V_S = −10V, V_D = 10V		0.02		±0.5	50		±1.0	50	
$I_{D(off)}$		D	1	V_D = 10V, V_S = −10V		0.05		±1.0	100		±2.0	100	
			1	V_D = −10V, V_S = 10V		0.05		±1.0	100		±2.0	100	
$I_{D(on)}$		D	16	$V_{S(All)}$ = V_D = 10V	Sequence each switch on	0.1		±2.0	100		±4.0	100	
			16	$V_{S(All)}$ = V_D = −10V	V_{AL} = 0.8V, V_{AH} = 2.4V	0.1		±2.0	100		±4.0	100	
FAULT													
I_S with Power OFF		S	16	V_{SUPP} = 0V, V_{IN} = ±25V, V_{EN} = V_O = 0V, A_0, A_1, A_2 = 0V or 5V		1.0		2.0			5.0		μA
$I_{S(off)}$ with Overvoltage		S	16	V_{IN} = ±25V, V_0 = ±10V		1.0		2.0			5.0		
INPUT													
$I_{EN(on)}$ $I_{A(on)}$ or $I_{EN(off)}$ $I_{A(off)}$		A_0, A_1, A_2, A_3 or EN	4	V_A = 2.4V or 0V		0.01		−10	−30		−10	−30	μA
			4	V_A = 15V		0.01		10	30		10	30	
DYNAMIC													
$t_{transition}$		D				0.3		1					μs
t_{open}		D				0.2							
$t_{on(EN)}$		D				0.6		1.5					
$t_{off(EN)}$		D				0.4		1					
t_{on}-t_{off} Break-Before-Make Delay Settling Time		D	16	V_{EN} = +5V, A_0, A_1, A_2 Strobed V_{IN} = ±10V.		25							ns
"OFF" Isolation		D		V_{EN} = 0, R_L = 200Ω, C_L = 3pF, V_S = 3VRMS, f = 500kHz		60							dB
$C_{S(off)}$		S		V_S = 0	V_{EN} = 0V,	5							pF
$C_{D(off)}$		D		V_D = 0	f = 140kHz	25							
$C_{DS(off)}$		D to S		V_S = 0, V_D = 0	to 1 MHz	1							
SUPPLY													
Supply	+	I^+	1	All V_A = 0V/5V		0.5		0.6			1.0		mA
Current	−	I^-	1	V_{EN} = 5V		0.02		0.6			1.0		

Note: All typical values have been guaranteed by characterization and are not tested.

IH5140-IH5145 Family
High-Level CMOS Analog Switch

INTERSIL

GENERAL DESCRIPTION

The IH5140 Family of CMOS monolithic switches utilizes Intersil's latch-free junction isolated processing to build the fastest switches currently available. These switches can be toggled at a rate of greater than 1MHz with super fast t_{on} times (80ns typical) and faster t_{off} times (50ns typical), guaranteeing break before make switching. This family of switches combines the speed of the hybrid FET DG180 family with the reliability and low power consumption of a monolithic CMOS construction.

OFF leakages are guaranteed to be less than 200pA at 25°C. Very low quiescent power is dissipated in either the ON or the OFF state of the switch. Maximum power supply current is 1μA from any supply and typical quiescent currents are in the 10nA range which makes these devices ideal for portable equipment and military applications.

The IH5140 Family is completely compatible with TTL (5V) logic, TTL open collector logic and CMOS logic. It is pin compatible with Intersil's IH5040 family and part of the DG180/190 family as shown in the switching state diagrams.

FEATURES

- **Super Fast Break-Before-Make Switching**
- **t_{on} 80ns Typ, t_{off} 50ns Typ (SPST Switches)**
- **Power Supply Currents Less Than 1μA**
- **OFF Leakages Less Than 100pA @ 25°C Guaranteed**
- **Non-latching With Supply Turn-off**
- **Single Monolithic CMOS Chip**
- **Plug-in Replacements for IH5040 Family and Part of the DG180 Family to Upgrade Speed and Leakage**
- **Greater Than 1MHz Toggle Rate**
- **Switches Greater Than 20Vp-p Signals With ±15V Supplies**
- **TTL, CMOS Direct Compatibility**

ORDERING INFORMATION

Order Part Number	Function	Package	Temperature Range
IH5140 MJE	SPST	16 Pin CERDIP	-55°C to 125°C
IH5140 CJE	SPST	16 Pin CERDIP	0°C to 70°C
IH5140 CPE	SPST	16 Pin Plastic DIP	0°C to 70°C
IH5140 MFD	SPST	14 Pin Flat Pack	-55°C to 125°C
IH5141 MJE	Dual SPST	16 Pin CERDIP	-55°C to 125°C
IH5141 CJE	Dual SPST	16 Pin CERDIP	0°C to 70°C
IH5141 CPE	Dual SPST	16 Pin Plastic DIP	0°C to 70°C
IH5141 MFD	Dual SPST	14 Pin Flat Pack	-55°C to 125°C
IH5141 CTW	Dual SPST	TO-100	0°C to 70°C
IH5141 MTW	Dual SPST	TO-100	-55°C to 125°C
IH5142 MJE	SPDT	16 Pin CERDIP	-55°C to 125°C
IH5142 CJE	SPDT	16 Pin CERDIP	0°C to 70°C
IH5142 CPE	SPDT	16 Pin Plastic DIP	0°C to 70°C
IH5142 MFD	SPDT	14 Pin Flat Pack	-55°C to 125°C
IH5142 CTW	SPDT	TO-100	0°C to 70°C
IH5142 MTW	SPDT	TO-100	-55°C to 125°C
IH5143 MJE	Dual SPDT	16 Pin CERDIP	-55°C to 125°C
IH5143 CJE	Dual SPDT	16 Pin CERDIP	0°C to 70°C
IH5143 CPE	Dual SPDT	16 Pin Plastic DIP	0°C to 70°C
IH5143 MFD	dual SPDT	14 Pin Flat Pack	-55°C to 125°C
IH5144 MJE	DPST	16 Pin CERDIP	-55°C to 125°C
IH5144 CJE	DPST	16 Pin CERDIP	0°C to 70°C
IH5144 CPE	DPST	16 Pin Plastic DIP	0°C to 70°C
IH5144 MFD	DPST	14 Pin Flat Pack	-55°C to 125°C
IH5144 CTW	DPST	TO-100	0°C to 70°C
IH5144 MTW	DPST	TO-100	-55°C to 125°C
IH5145 MJE	Dual DPST	16 Pin CERDIP	-55°C to 125°C
IH5145 CJE	Dual DPST	16 Pin CERDIP	0°C to 70°C
IH5145 CPE	Dual DPST	16 Pin Plastic DIP	0°C to 70°C
IH5145 MFD	Dual DPST	14 Pin Flat Pack	-55°C to 125°C

Note: 1. Ceramic (side braze) devices also available; consult factory.
2. MIL temp range parts also available with MIL-STD-883 processing.

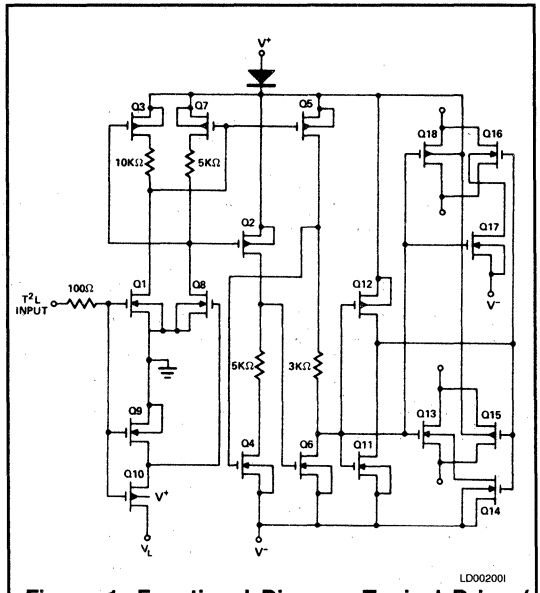


Figure 1: Functional Diagram Typical Driver/ Gate - IH5142

Note: All typical values have been guaranteed by characterization and are not tested.

IH5140-IH5145

INTERSIL

ABSOLUTE MAXIMUM RATINGS

$V^+ - V^-$ ..... < 33V
$V^+ - V_D$ ..... < 30V
$V_D - V^-$ ..... < 30V
$V_D - V_S$ ..... < ±22V
$V_L - V^-$ ..... < 33V
$V_L - V_{IN}$ ..... < 30V
V_L ..... < 20V
V_{IN} ..... < 20V

Current (Any Terminal) ..... < 30mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −55°C to +125°C
Lead Temperature (Soldering 10sec) .....300°C
Power Dissipation 450mW
(All Leads Soldered to a P.C. Board)
Derate 6 mW/°C Above 70°C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (@ 25°C, V^+ = +15V, V^- = −15V, V_L = +5V)

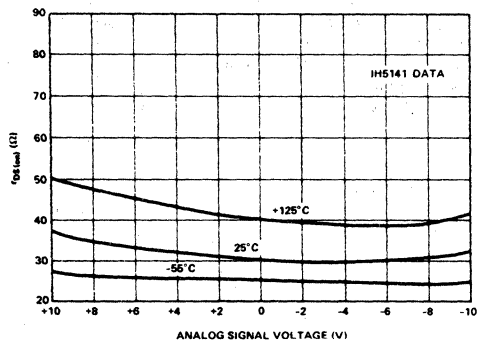
PER CHANNEL		TEST CONDITIONS	MIN/MAX LIMITS						UNIT
			MILITARY			COMMERCIAL			
SYMBOL	CHARACTERISTIC		−55°C	+25°C	+125°C	0	+25°C	+70°C	
LOGIC INPUT									
I_{INH}	Input Logic Current	V_{IN} = 2.4V Note 1	±1	±1	10		±10	10	μA
I_{INL}	Input Logic Current	V_{IN} = 0.8V Note 1	±1	±1	10		±10	10	μA
SWITCH									
$r_{DS(on)}$	Drain–Source On Resistance	I_S = −10mA V_{ANALOG} = −10V to +10V	50	50	75	75	75	100	Ω
$\Delta r_{DS(on)}$	Channel to Channel $r_{DS(on)}$ Match			25 (typ)			30 (typ)		Ω
V_{ANALOG}	Min. Analog Signal Handling Capability			±11 (typ)			±10 (typ)		V
$I_{D(off)}$ + $I_{S(off)}$	Switch OFF Leakage Current	V_D = +10V, V_S = −10V V_D = −10V, V_S = +10V		±.5 ±.5	100 100		±5 ±5	100 100	nA
$I_{D(on)}$ + $I_{S(on)}$	Switch On Leakage Current	$V_D = V_S$ = −10V to +10V		±1	200		±2	200	nA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off; Any Other Channel Switches See Performance Characteristics		54 (typ)			50 (typ)		dB
t_{on} t_{off}	Switch "ON" Time Switch "OFF" Time	See switching time specifications and timing diagrams.							
$Q_{(INJ.)}$	Charge Injection	See Performance Characteristics		10 (typ)			15 (typ)		pC
OIRR	Min. Off Isolation Rejection Ratio	f = 1MHz, R_L = 100Ω, $C_L \leq$ 5pF See Performance Characteristics		54 (typ)			50 (typ)		dB
SUPPLY									
I^+	+ Power Supply Quiescent Current	V^+ = +15V, V^- = −15V, V_L = +5V See Performance Characteristics	1.0	1.0	10.0	10	10	100	μA
I^-	− Power Supply Quiescent Current		1.0	1.0	10.0	10	10	100	μA
I_L	+5V Supply Quiescent Current		1.0	1.0	10.0	10	10	100	μA
I_{GND}	Gnd Supply Quiescent Current		1.0	1.0	10.0	10	10	100	μA

NOTES: 1. Some channels are turned on by high (1) logic inputs and other channels are turned on by low (0) inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to find logical value of logic input required to produce ON or OFF state.
2. Typical values are for design aid only, not guaranteed and not subject to production testing.

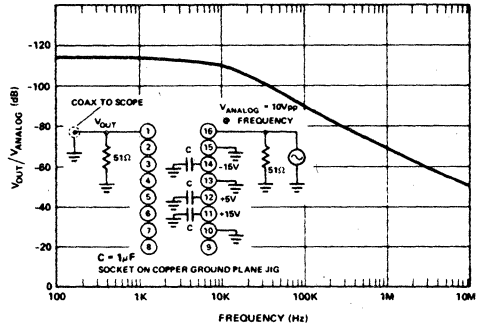
Note: All typical values have been guaranteed by characterization and are not tested.

IH5140-IH5145

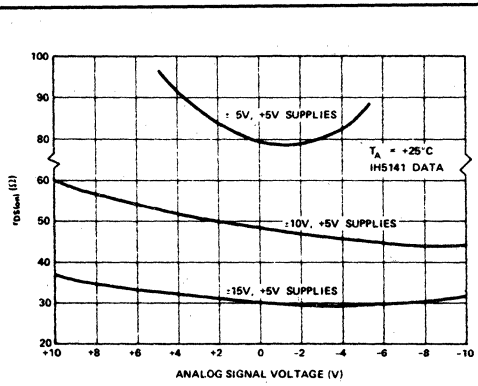
TYPICAL PERFORMANCE CHARACTERISTICS



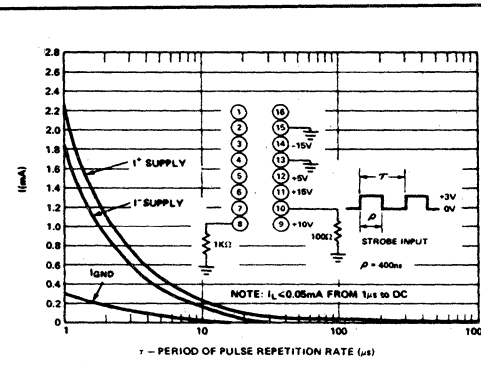
$r_{DS(on)}$ vs. Temp., @ ±15V, +5V Supplies



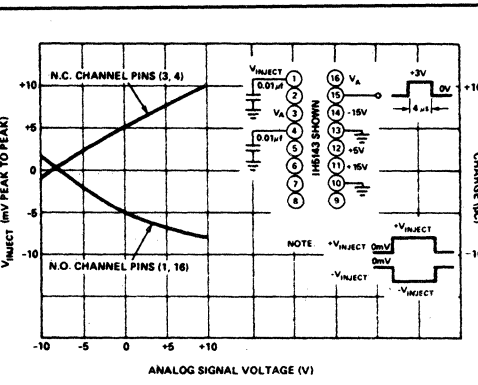
"OFF" Isolation vs. Frequency



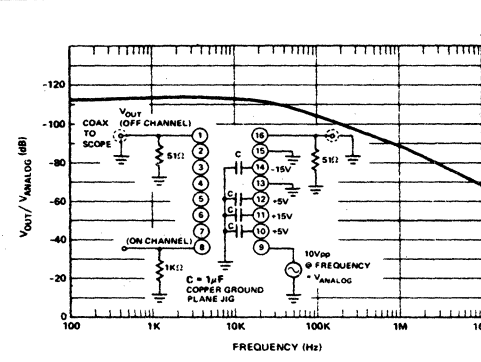
$r_{DS(on)}$ vs. Power Supplies



Power Supply Currents vs. Logic Strobe Rate



Charge Injection vs. Analog Signal



Channel to Channel Cross Coupling Rejection vs. Frequency

Note: All typical values have been guaranteed by characterization and are not tested.

IH5140-IH5145

INTERSIL

SWITCHING TIME SPECIFICATIONS

(t_{on}, t_{off} are maximum specifications and t_{on}-t_{off} is minimum specifications)

PART NUMBER	SYMBOL	CHARACTERISTIC	TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
				-55°C	+25°C	+125°C	0	+25°C	+70°C	
IH5140-5141	t_{on}	Switch "ON" time	Figure 2*		100			150		ns
	t_{off}	Switch "OFF" time			75			125		
	t_{on}-t_{off}	Break-before-make			10			5		
	t_{on}	Switch "ON" time	Figure 3		150			175		ns
	t_{off}	Switch "OFF" time			125			150		
	t_{on}-t_{off}	Break-before-make			*10 (typ)			5		
IH5142-5143	t_{on}	Switch "ON" time	Figure 2*		175			250		ns
	t_{off}	Switch 'OFF" time			125			150		
	t_{on}-t_{off}	Break-before-make			10			5		
	t_{on}	Switch "ON" time	Figure 3		200			300		ns
	t_{off}	Switch "OFF" time			125			150		
	t_{on}-t_{off}	Break-before-make			*10 (typ)			5		
	t_{on}	Switch "ON" time	Figure 4*		175			250		ns
	t_{off}	Switch "OFF" time			125			150		
	t_{on}-t_{off}	Break-before-make			10			5		
	t_{on}	Switch "ON" time	Figure 5*		200			300		ns
	t_{off}	Switch "OFF" time			125			150		
	t_{on}-t_{off}	Break-before-make			10			5		
IH5144-5145	t_{on}	Switch "ON" time	Figure 2*		175			250		ns
	t_{off}	Switch "OFF" time			125			150		
	t_{on}-t_{off}	Break-before-make			10			5		
	t_{on}	Switch "ON" time	Figure 3		200			300		ns
	t_{off}	Switch "OFF" time			125			150		
	t_{on}-t_{off}	Break-before-make			*10			5		

NOTE: SWITCHING TIMES ARE MEASURED @ 90% PTS. * Typical values for design aid only, not guaranteed nor subject to production testing.

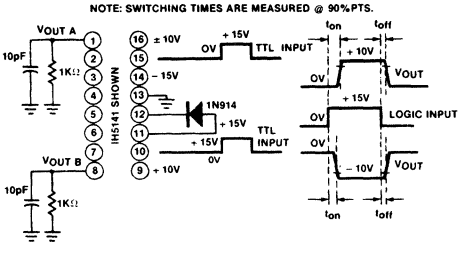


Figure 2.

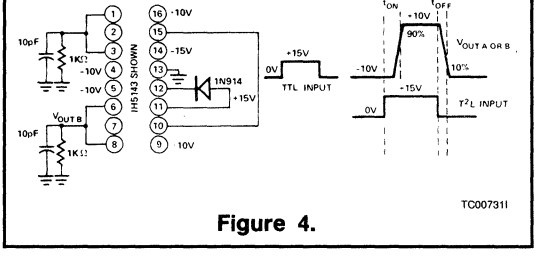


Figure 4.

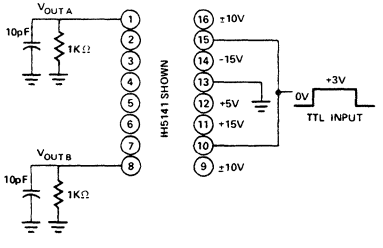


Figure 3.

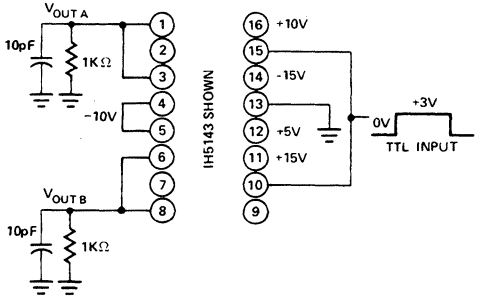


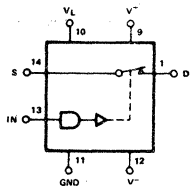
Figure 5.

Note: All typical values have been guaranteed by characterization and are not tested.

IH5140-IH5145

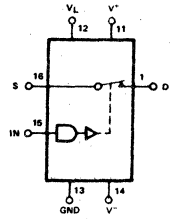
INTERSIL

FLATPACK (FD-2)



SS00350I

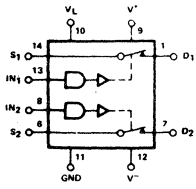
DIP (JE, PE)



SS00360I

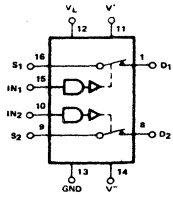
SPST
IH5140 ($r_{DS(on)} < 75\Omega$)

FLATPACK (FD-2)



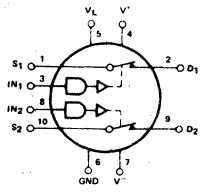
SS00370I

DIP (JE, PE)



SS00380I

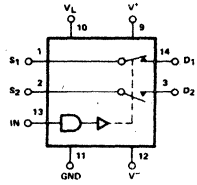
TO-100



SS00390I

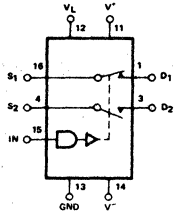
DUAL SPST
IH5141 ($r_{DS(on)} < 75\Omega$)

FLATPACK (FD-2)



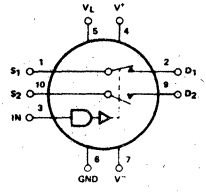
SS00400I

DIP (JE, PE)



SS00410I

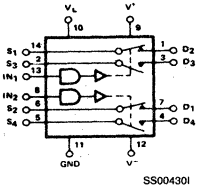
TO-100 (DG188 EQUIVALENT)



SS00420I

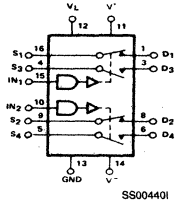
SPDT
IH5142 ($r_{DS(on)} < 75\ \Omega$)

FLATPACK (FD-2)



SS00430I

DIP (JE, PE) (DG191 EQUIVALENT)



SS00440I

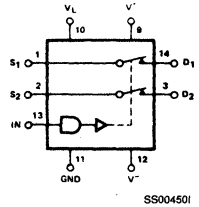
DUAL SPDT
IH5143 ($r_{DS(on)} < 75\Omega$)

SWITCH STATES ARE FOR LOGIC "1" INPUT

Figure 6: Switching State Diagrams

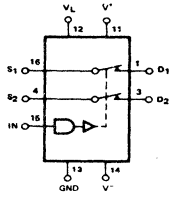
Note: All typical values have been guaranteed by characterization and are not tested.

FLATPACK (FD-2)



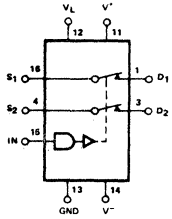
SS00450I

DIP (JE, PE)



SS00460I

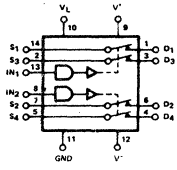
TO-100



SS00460I

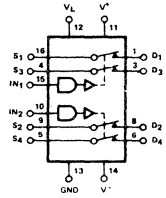
DPST
IH5144 ($r_{DS(on)} < 75\Omega$)

FLATPACK (FD-2)



SS00480I

DIP (JE, PE) (DG185 EQUIVALENT)



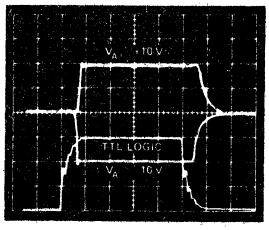
SS00490I

DUAL DPST
IH5145 ($r_{DS(on)} < 75\Omega$)

Figure 6: Switching State Diagrams (Cont.)

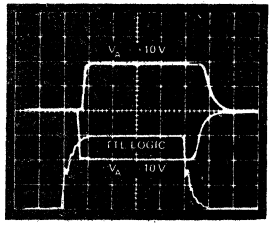
TYPICAL SWITCHING WAVEFORMS SCALE: VERT. = 5V/DIV. HORIZ. = 100ns/DIV.

TTL OPEN COLLECTOR LOGIC DRIVE (Corresponds to Figure 8)



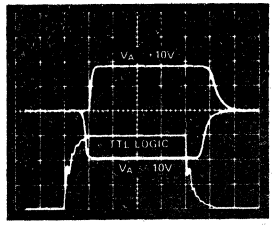
-55°C

WF00470I



+25°C

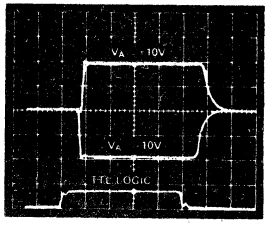
WF00220I



+125°C

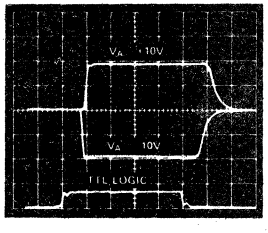
WF00230I

TTL OPEN COLLECTOR LOGIC DRIVE (Corresponds to Figure 9)



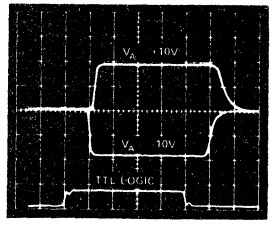
-55°C

WF00240I



+25°C

WF00250I



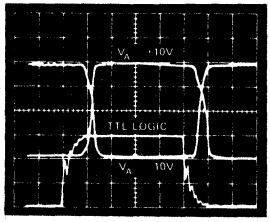
+125°C

WF00260I

Note: All typical values have been guaranteed by characterization and are not tested.

TYPICAL SWITCHING WAVEFORMS (CONT.)

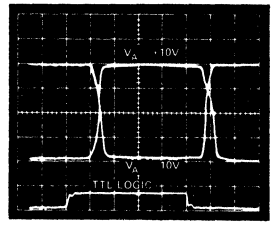
TTL OPEN COLLECTOR LOGIC DRIVE
(Corresponds to Figure 10)



+25°C

WF00270I

TTL OPEN COLLECTOR LOGIC DRIVE
(Corresponds to Figure 11)



+25°C

WF00280I

APPLICATION NOTE

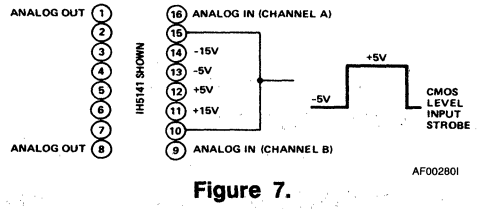
To maximize switching speed on the IH5140 family, TTL open collector logic (15V with a 1kΩ or less collector resistor) should be used. This configuration will result in (SPST) t_{on} and t_{off} times of 80ns and 50ns, for signals between −10V and +10V. The SPDT and DPST switches are approximately 30ns slower in both t_{on} and t_{off} with the same drive configuration. 15V CMOS logic levels can be used (0V to +15V), but propagation delays in the CMOS logic will slow down the switching (typical 50ns → 100ns delays).

When driving the IH5140 Family from either +5V TTL or CMOS logic, switching times run 20ns slower than if they were driven from +15V logic levels. Thus t_{on} is about 105ns, and t_{off} 75ns for SPST switches, and 135ns and 105ns (t_{on}, t_{off}) for SPDT or DPST switches. The low level drive can be made as fast as the high level drive if ±5V strobe levels are used instead of the usual 0V→ +3.0V drive. Pin 13 is taken to −5V instead of the usual GND and strobe input is taken from +5V to −5V levels as shown in Figure 7.

The typical channel of the IH5140 family consists of both P and N-channel MOSFETs. The N-channel MOSFET uses a "Body Puller" FET to drive the body to −15V (±15V supplies) to get good breakdown voltages when the switch is in the off state (See Fig. 8). This "Body Puller" FET also allows the N-channel body to electrically float when the switch is in the on state producing a fairly constant $R_{DS}(ON)$ with different signal voltages. While this "Body Puller" FET improves switch performance, it can cause a problem when analog input signals are present (negative signals only) and power supplies are off. This fault condition is shown in Figure 9.

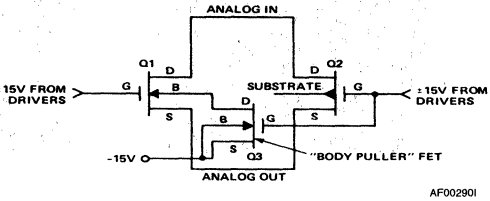
Current will flow from −10V analog voltage through the drain to body junction of Q1, then through the drain to body junction of Q3 to GND. This means that there is 10V across two forward-biased silicon diodes and current will go to whatever value the input signal source is capable of supplying. If the analog input signal is derived from the same supplies as the switch this fault condition cannot occur. Turning off the supplies would turn off the analog signal at the same time.

This fault situation can also be eliminated by placing a diode in series with the negative supply line (pin 14) as shown in Figure 10. Now when the power supplies are off and a negative input signal is present this diode is reverse biased and no current can flow.



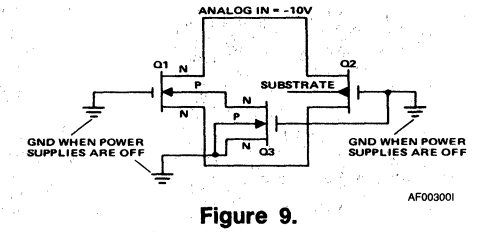
AF00280I

Figure 7.



AF00290I

Figure 8.



AF00300I

Figure 9.

Note: All typical values have been guaranteed by characterization and are not tested.

APPLICATION NOTE (CONT.)

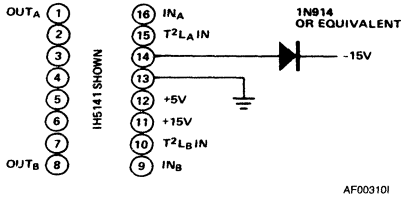


Figure 10.

APPLICATIONS

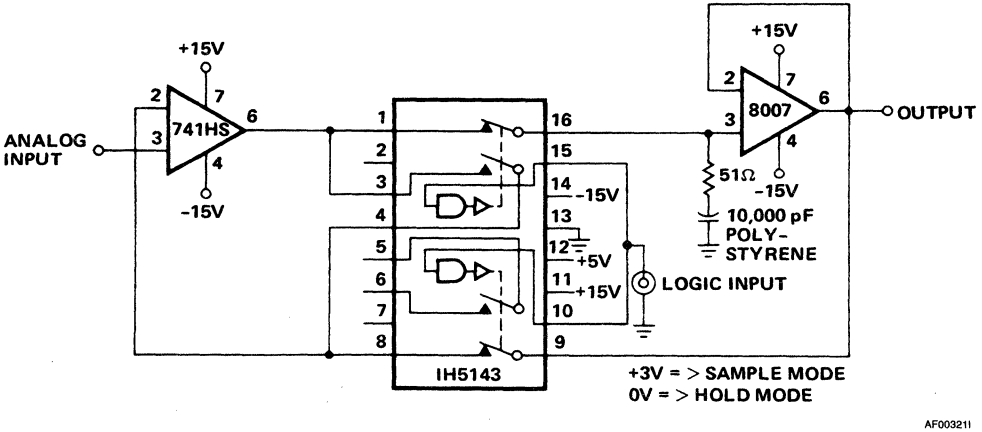
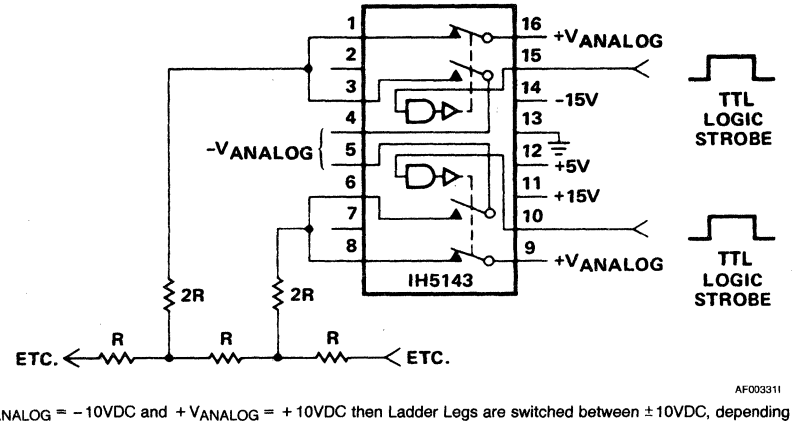


Figure 11: Improved Sample and Hold Using IH5143

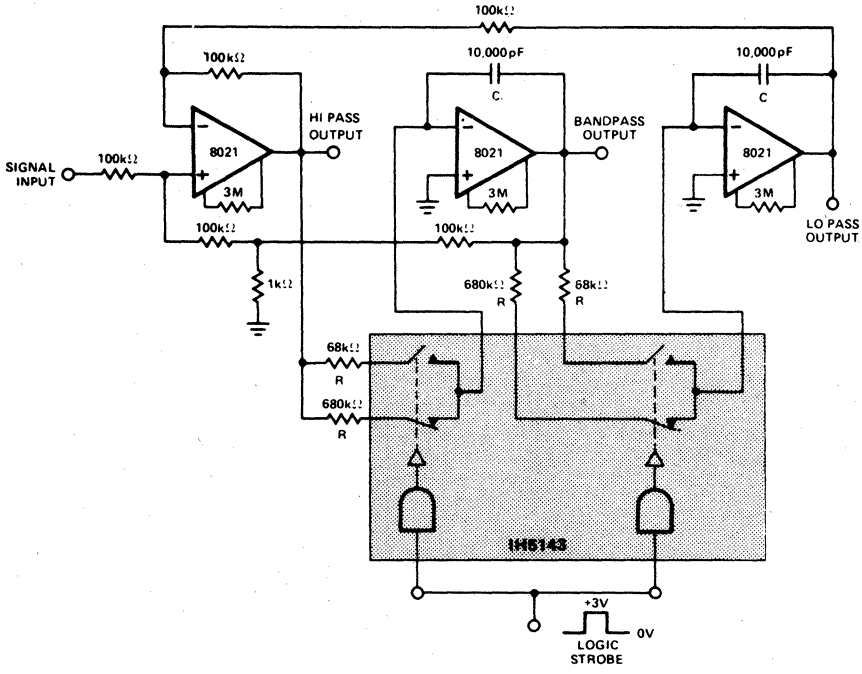


EXAMPLE: If $-V_{ANALOG} = -10VDC$ and $+V_{ANALOG} = +10VDC$ then Ladder Legs are switched between $\pm 10VDC$, depending upon state of Logic Strobe.

Figure 12: Using the CMOS Switch to Drive an R/2R Ladder Network (2 Legs)

Note: All typical values have been guaranteed by characterization and are not tested.

APPLICATIONS (CONT.)



AF00340I

CONSTANT GAIN, CONSTANT Q, VARIABLE FREQUENCY FILTER WHICH PROVIDES SIMULTANEOUS LOWPASS, BANDPASS, AND HIGHPASS OUTPUTS. WITH THE COMPONENT VALUES SHOWN, CENTER FREQUENCY WILL BE 235Hz AND 23.5Hz FOR HIGH AND LOW LOGIC INPUTS RESPECTIVELY, Q = 100, AND GAIN = 100.

$$f_n = \text{CENTER FREQUENCY} = \frac{1}{2\pi RC}$$

Figure 13: Digitally Tuned Low Power Active Filter

Note: All typical values have been guaranteed by characterization and are not tested.

IH5148-IH5151
High-Level CMOS Analog Switches

GENERAL DESCRIPTION

The IH5148 family of solid state analog switches are designed using an improved, high voltage CMOS technology. Destructive latchup has been eliminated. Early CMOS switches were destroyed when power supplies were removed with an input signal present; the IH5148 CMOS technology has eliminated this problem.

Key performance advantages of the 5148 series are TTL compatibility and ultra low-power operation. $R_{DS(on)}$ Switch resistance is typically in the 14Ω To 18Ω Area, for Signals in the −10V to +10V range. Quiescent current is less than 10μA. The 5148 also guarantees Break-Before-Make switching which is logically accomplished by extending the t_{ON} time (200nsec typ.) such that it exceeds t_{OFF} time 120nsec typ.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. The need for external logic required to avoid channel to channel shorting during switching is thus eliminated.

Many of the devices in the 5148 series are pin-for-pin compatible with other analog switches, and offer improved electrical characteristics.

FEATURES

- **Low $R_{DS(ON)}$ — 25Ω**
- **Switches Greater Than 20Vpp Signals With ±15V Supplies**
- **Quiescent Current Less Than 100μA**
- **Break-Before-Make Switching t_{OFF} 120nsec, Typ. t_{ON} 200nsec Typical**
- **TTL, CMOS Compatible**
- **Non-Latching With Supply Turn-Off**
- **Complete Monolithic Construction**
- **±5V to ±15V Supply Range**

CMOS ANALOG SWITCH PRODUCT CONDITIONING

- **The Following Processes Are Performed 100% in Accordance With MIL-STD-883**
- **Precap Visual — Method 2010, Cond. B**
- **Stabilization Bake — Method 1008**
- **Temperature Cycle — Method 1010**
- **Centrifuge — Method 2001, Cond. E**
- **Hermeticity — Method 1014, Cond. A, C**
- **(Leak Rate < 5×10^{-7} atm cc/s)**

ORDERING INFORMATION

ORDER PART NUMBER	FUNCTION	PACKAGE	TEMPERATURE RANGE	HARRIS EQUIVALENT
IH5148MJE	Dual SPST	16 Pin CERDIP	−55°C to 125°C	HI-5048
IH5148CJE	Dual SPST	16 Pin CERDIP	0°C to 70°C	HI-5048
IH5148CPE	Dual SPST	16 Pin Plastic DIP	0°C to 70°C	HI-5048
IH5148MFD	Dual SPST	14 Pin Flat Pack	−50°C to 125°C	HI-5048
IH5148CTW	Dual SPST	TO-100	0°C to 70°C	HI-5048
IH5148MTW	Dual SPST	TO-100	−55°C to 125°C	HI-5048
IH5149MJE	Dual DPST	16 Pin CERDIP	−55°C to 125°C	HI-5049
IH5149CJE	Dual DPST	16 Pin CERDIP	0°C to 70°C	HI-5049
IH5149CPE	Dual DPST	16 Pin Plastic DIP	0°C to 70°C	HI-5049
IH5149MFD	Dual DPST	14 Pin Flat Pack	−50°C to 125°C	HI-5049
IH5150MJE	SPDT	16 Pin CERDIP	−55°C to 125°C	HI-5050
IH5150CJE	SPDT	16 Pin CERDIP	0°C to 70°C	HI-5050
IH5150CPE	SPDT	16 Pin Plastic DIP	0°C to 70°C	HI-5050
IH5150MFD	SPDT	14 Pin Flat Pack	−50°C to 125°C	HI-5050
IH5150CTW	SPDT	TO-100	0°C to 70°C	HI-5050
IH5150MTW	SPDT	TO-100	−55°C to 125°C	HI-5050
IH5151MJE	Dual SPDT	16 Pin CERDIP	−55°C to 125°C	HI-5051
IH5151CJE	Dual SPDT	16 Pin CERDIP	0°C to 70°C	HI-5051
IH5151CPE	Dual SPDT	16 Pin Plastic DIP	0°C to 70°C	HI-5051
IH5151MFD	Dual SPDT	14 Pin Flat Pack	−50°C to 125°C	HI-5051

NOTES: 1. Ceramic (side braze) devices also available; consult factory.
2. MIL temp range parts also available with MIL-STD-883 processing.

304300-002

Note: All typical values have been guaranteed by characterization and are not tested.

IH5148-IH5151

INTERSIL

ABSOLUTE MAXIMUM RATINGS

V^+, V^-	< 36V
V^+, V_D	< 30V
V_D, V^-	< 30V
V_D, V_S	< ±22V
V_L, V^-	< 33V
V_L, V_{IN}	< 30V
V_L	< 20V
V_{IN}	< 20V

Current (Any Terminal)	< 50mA
Storage Temperature	-65°C to +150°C
Operating Temperature	-55°C to +125°C
Lead Temperature (Soldering, 10sec)	300°C
Power Dissipation	450mW
(All Leads Soldered to a P.C. Board)	
Derate 6mW/°C Above 70°C	

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

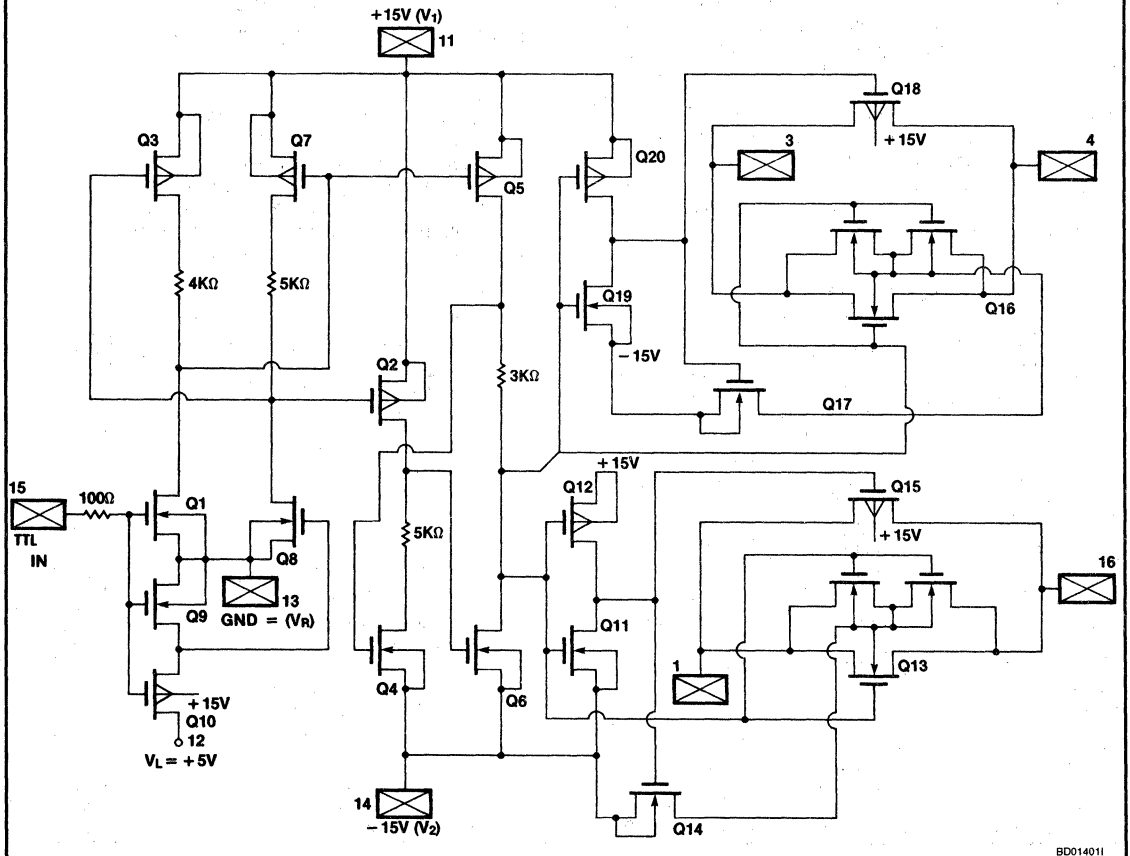


Figure 1: Functional Diagram (Typical Switch Schematic-IH5150 in 16 pin DIP PKG.)

Note: All typical values have been guaranteed by characterization and are not tested.

IH5148-IH5151

INTERSIL

ELECTRICAL CHARACTERISTICS (T_A @ 25°C, $V^+ = +15V$, $V^- = -15V$, $V_L = +5V$)

PER CHANNEL		TEST CONDITIONS	MIN/MAX LIMITS						UNIT
			MILITARY			COMMERCIAL			
SYMBOL	CHARACTERISTIC		-55°C	+25°C	+125°C	0	+25°C	+70°C	
$I_{IN(ON)}$	Input Logic Current	$V_{IN} = 2.4V$ (Note 1)	±1	±1	±10		±1	±10	μA
$I_{IN(OFF)}$	Input Logic Current	$V_{IN} = 0.8V$ (Note 1)	±1	±1	±10		±1	±10	μA
$R_{DS(ON)}$	Drain-Source On Resistance	$V_D = ±10V$, $I_S = -10mA$	25	25	50		30		Ω
$\Delta R_{DS(ON)}$	Channel to Channel $R_{DS(ON)}$ Match			10 (Typ)			15 (Typ)		Ω
V_{ANALOG}	Min. Analog Signal Handling Capability			±14 (Typ)			±14 (Typ)		V
$I_{D(OFF)}$ $I_{S(OFF)}$	Switch OFF Leakage Current	$V_{ANALOG} = -10V$ to $+10V$		±0.5	50		±1.0	100	nA
$I_{D(ON)} + I_{S(ON)}$	Switch On Leakage Current	$V_D = V_S = -10V$ to $+10V$		±1.0	100		±2.0	100	nA
$Q_{(INJ)}$	Charge Injection	See Figure 4		(10) (Typ)			(10) (Typ)		mV
OIRR	Min. Off Isolation Rejection Ratio	$f = 1MHz$, $R_L = 100Ω$, $C_L \leq 5pF$ See Figure 5		54 (Typ)			50 (Typ)		dB
SUPPLY									
I^+	+ Power Supply Quiescent Current	$V_1 = +15V$, $V_2 = -15V$. $V_L = +5V$, $V_R = 0$	10	10	100		10		μA
I^-	- Power Supply Quiescent Current		10	10	100		10		μA
I_L	+ 5V Supply Quiescent Current		10	10	100		10		μA
I_{GND}	Gnd Supply Quiescent Current		10	10	100		10		μA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off; Any Other Channel Switches as per Figure 8		54 (Typ)			50		dB

NOTE 1: Some channels are turned on by high "1" logic inputs and other channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to find logical value of logic input required to produce "ON" or "OFF" state.

SWITCHING TIME SPECIFICATION
IH5148 SPST SWITCH

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{on}	Switch "on" time	$R_L = 1KΩ$, $V_{ANALOG} = -10V$		250	ns
t_{off}	Switch "off" time	$T_O + 10V$; See Figures 3 and 6		200	ns

IH5149 DPST SWITCH

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{on}	Switch "on" time	$R_L = 1KΩ$, $V_{ANALOG} = -10V$		350	ns
t_{off}	Switch "off" time	$T_O + 10V$; See Figures 3 and 6		250	ns

IH5150 & IH5151 SPDT SWITCH

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{on}	Switch "on" time	$R_L = 1KΩ$, $V_{ANALOG} = -10V$		500	ns
t_{off}	Switch "off" time	$T_O + 10V$; See Figures 3 and 6		250	ns

NOTE 2: For IH5150 & IH5151 devices, channels which are off for logic input ≥ 2.4V (Pins 3 & 4 on 5150, & Pins 3 & 4, 5 & 6 on 5151) have slower t_{on} time, than channels on Pins 1, 16, & 8, 9. This is done so switch will maintain break-before-make action when connected in DT configuration, i.e. Pin 1 connected in Pin 3.

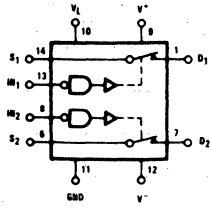
Note: All typical values have been guaranteed by characterization and are not tested.

IH5148-IH5151

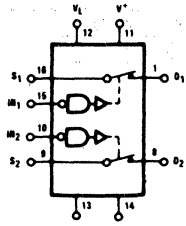
INTERSIL

SWITCH STATES ARE FOR LOGIC "1" INPUT	FLAT PACKAGE	DIP (DE) PACKAGE	(TW) PACKAGE

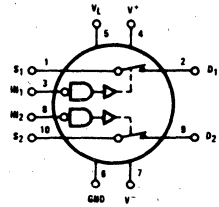
DUAL SPST IH5148



SS00740I

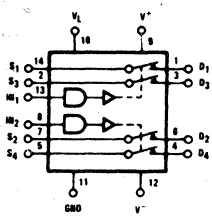


SS00750I



SS00760I

DUAL DPST IH5149



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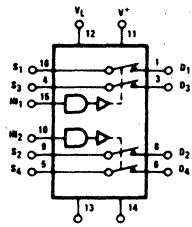
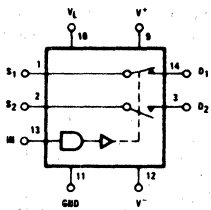
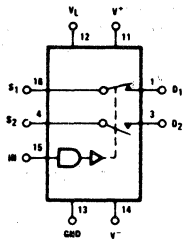


SS00780I

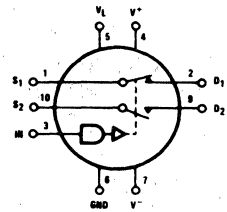
SPDT IH5150



SS00790I

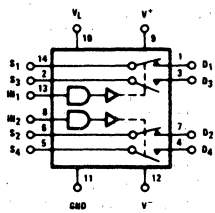


SS00800I



SS00810I

DUAL SPDT IH5151



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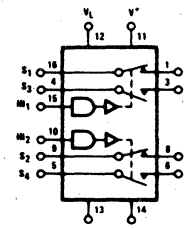


SS00830I

Figure 2: Switching State Diagrams

Note: All typical values have been guaranteed by characterization and are not tested.

TEST CIRCUITS

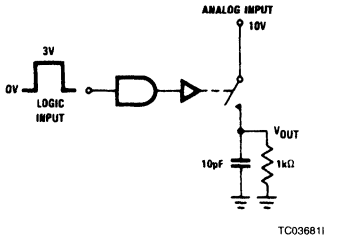


Figure 3

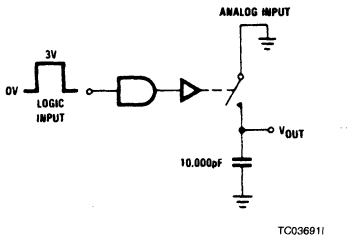


Figure 4

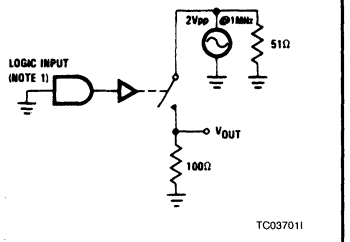
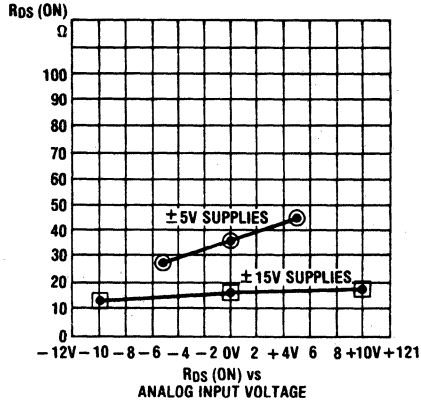
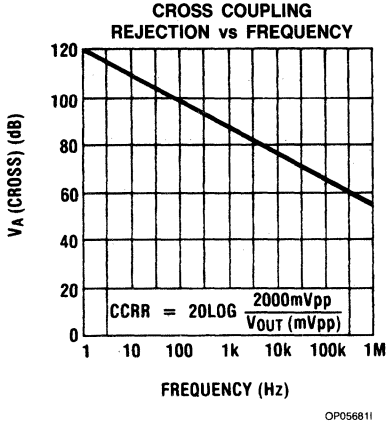


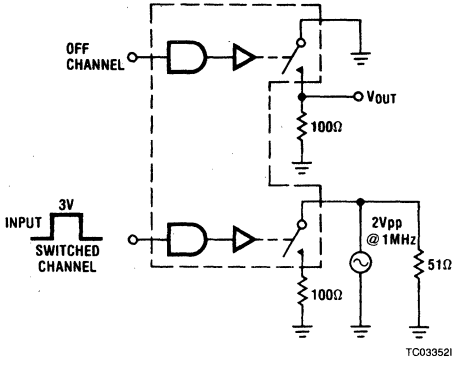
Figure 5

TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel)

$R_{DS(ON)}$ @ ±15V, ±5V SUPPLIES







CROSS COUPLING
REJECTION TEST CIRCUIT

Note: All typical values have been guaranteed by characterization and are not tested.

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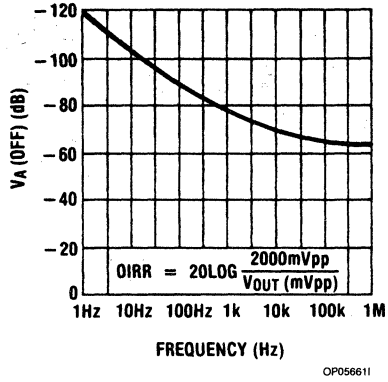
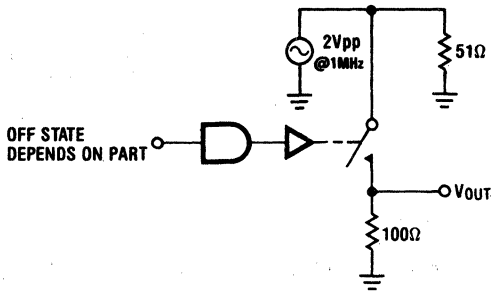
TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

OFF ISOLATION vs FREQUENCY



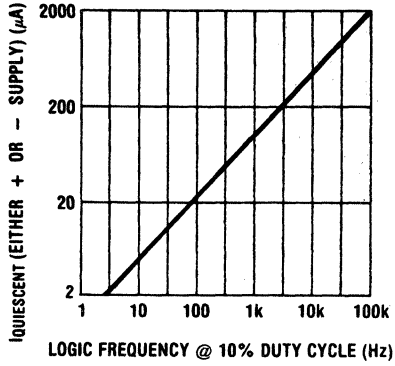
OP05661I



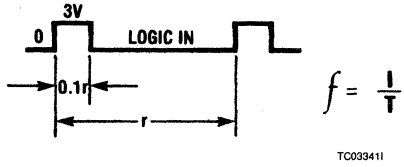
TC03311I

OFF ISOLATION TEST CIRCUIT

POWER SUPPLY QUIESCENT CURRENT vs LOGIC FREQUENCY RATE

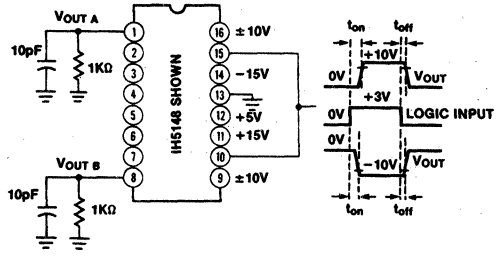


OP05671I



TC03341I

LOGIC INPUT WAVEFORM



TC03670I

Figure 6: Switching Time Test Circuit

Note: All typical values have been guaranteed by characterization and are not tested.

Nulling Out Charge Injection:

Charge injection (Qinv. on spec. sheet) is caused by gate to drain, or gate to source capacitance of the output switch MOSFET. The gates of these MOSFETs typically swing from −15V to +15V as a rapidly changing pulse; thus this 30Vpp pulse is coupled through gate capacitance to output load capacitance, and the output "step" is a voltage divider from this combination. For example:

$$Qinject\ (Vpp) \cong \frac{C_{gate}}{C_{Load}} \times 30V\ step.$$

i.e.

C_{gate} = 1.5pF, C_{Load} = 1000pF, then

$$Qinject(Vpp) = \frac{1.5pF}{1000pF} \times 30V\ step = 45mVpp$$

Thus if you are using switch in a Sample & Hold application with C_{sample} = 1000pF, a 45mVpp "Sample to Hold error step" will occur.

To null this error step out to zero the following circuit can be used:

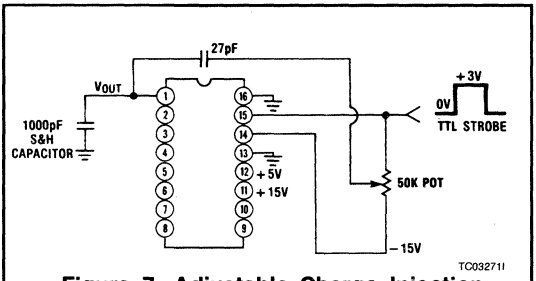


Figure 7: Adjustable Charge Injection Compensation Circuit

The circuit shown above nulls out charge injection effects on switch pins 1 and 16; a similar circuit would be required on switch pins 8 and 9.

Simply adjust the pot until V_{OUT} = 0mVpp pulse, with V_{ANALOG} = 0V.

If you do not desire to do any adjusting, but wish the least amount of charge injection possible, then the following circuit should be used:

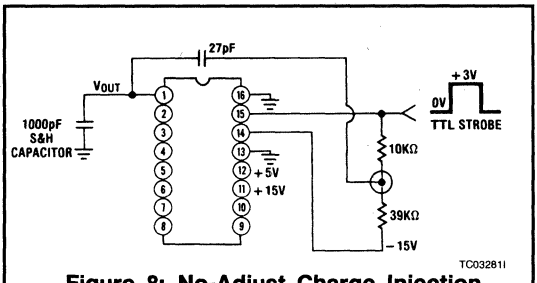


Figure 8: No-Adjust Charge Injection Compensation Circuit

This configuration will produce a typical charge injection of $V_{OUT} \leq$ 10mVpp into the 1000pF S & H capacitor shown.

Fault Condition Protection

If your system has analog voltage levels which are independent of the ±15V (Power Supplies), and these analog levels can be present when supplies are shut off, you should add fault protection diodes as shown below:

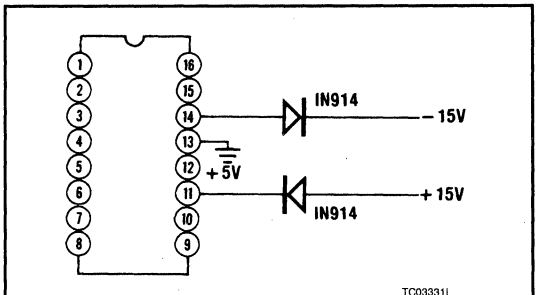


Figure 9: Adding Diodes Protects Switch

If the analog input levels are below ±15V, the pn junctions of Q13 & Q15 are reversed biased. However if the ±15V supplies are shut off and analog levels are still present, the configuration becomes:

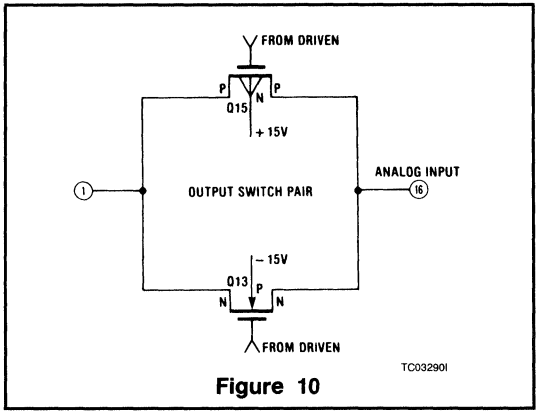


Figure 10

Note: All typical values have been guaranteed by characterization and are not tested.

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The need for these diodes, in this circumstance, is shown below:

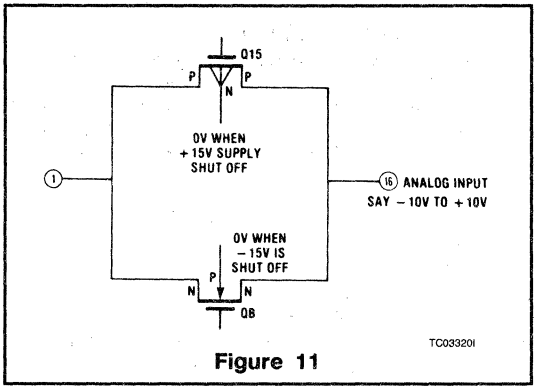


Figure 11

If ANALOG in is greater than $1V_{pn}$, then pn junction of Q15 is forward biased and excessive current will be drawn. The addition of IN914 diodes prevents the fault currents from destroying the switch. A similar event would occur if ANALOG in was less than or equal to −1V, wherein Q13 would become forward biased. The IN914 diodes form a "back to back" diode arrangement with Q13 & Q15 bodies.

This structure provides a degree of overvoltage protection when supplies are on normally, and analog input level exceeds supplies.

This circuit will switch up to about ±18V ANALOG overvoltages. Beyond this drain(N) to P(body) breakdown VOLTAGE of Q13 limits overvoltage protection.

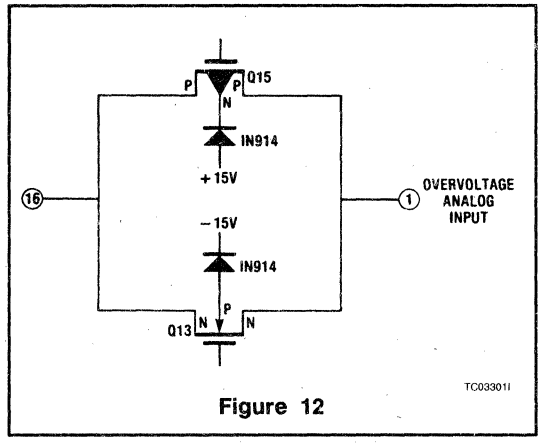


Figure 12

Note: All typical values have been guaranteed by characterization and are not tested.

IH5208
4-Channel Differential Fault Protected CMOS Analog Multiplexer

GENERAL DESCRIPTION

The IH5208 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the HI509A and similar devices, but adds fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to ±25V, even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc.

A binary 2-bit address code together with the ENable input allows selection of any channel pair or none at all. These 3 inputs are all TTL compatible for easy logic interface; the ENable input also facilitates MUX expansion and cascading.

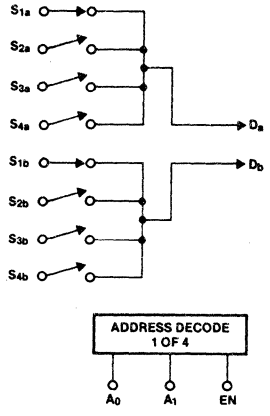
FEATURES

- **All Channels OFF When Power OFF, for Analog Signals Up to ±25V**
- **Power Supply Quiescent Current Less Than 1μA**
- **±13V Analog Signal Range**
- **No SCR Latchup**
- **Break-Before-Make Switching**
- **TTL and CMOS Compatible Strobe Control**
- **Pin Compatible With HI-509A**
- **Any Channel Turns OFF If Input Exceeds Supply Rails by Up to ±25V**
- **TTL and CMOS Compatible Binary Address and ENable Inputs**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5208MJE	-55°C to +125°C	16 pin CERDIP
IH5208IJE	-20°C to +85°C	16 pin CERDIP
IH5208CPE	0°C to 70°C	16 pin plastic DIP

3



2 LINE BINARY ADDRESS INPUTS
(0 0) AND EN = 1
ABOVE EXAMPLE SHOWS CHANNELS 1a AND 1b ON

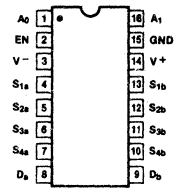
LD00210I

Figure 1: Functional Diagram

DECODE TRUTH TABLE

A_1	A_0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1a, 1b
0	1	1	2a, 2b
1	0	1	3a, 3b
1	1	1	4a, 4b

A_0, A_1, EN
Logic "1" = $V_{AH} \geq 2.4V$
Logic "0" = $V_{AL} \leq 0.8V$



CD00320I

Figure 2: Pin Configuration (Outline dwg JE, PE)

Note: All typical values have been guaranteed by characterization and are not tested.

IH5208

INTERSIL

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V, +15V
V_S or V_D to V^+ ..... +25V, −40V
V_S or V_D to V^- ..... −25V, +40V
V^+ to Ground 16V
V^- to Ground ..... −16V
Current (Any Terminal) 20mA

Operating Temperature ..... −55 to 125°C
Storage Temperature ..... −65 to 150°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Power Dissipation (Package)* 1200mW

*All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

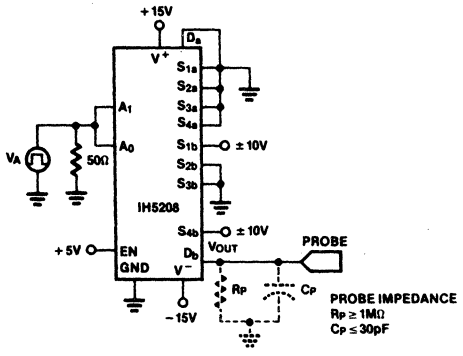
ELECTRICAL CHARACTERISTICS $V^+ = 15V$, $V^- = -15V$, $V_{EN} = 2.4V$, unless otherwise specified.

CHARACTERISTIC	MEASURED TERMINAL	NO TESTS PER TEMP	TEST CONDITIONS		TYP 25°C	MAX LIMITS M SUFFIX −55°C	MAX LIMITS M SUFFIX 25°C	MAX LIMITS M SUFFIX 125°C	MAX LIMITS C SUFFIX −20°C/0°C	MAX LIMITS C SUFFIX 25°C	MAX LIMITS C SUFFIX 85°C/70°C	UNIT
SWITCH												
$r_{DS(on)}$	S to D	8	$V_D = 10V$, $I_S = 1.0mA$	Sequence each switch on	700	1000	1000	1500	1200	1200	1800	Ω
		8	$V_D = -10V$, $I_S = -1.0mA$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$	500	1000	1000	1500	1200	1200	1800	
$\Delta r_{DS(on)}$			$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg.}}$, $V_S = \pm 10V$		5							%
$I_{S(off)}$	S	8	$V_S = 10V$, $V_D = -10V$	$V_{EN} = 0.8V$	0.02		±0.5	50		±1.0	50	nA
		8	$V_S = -10V$, $V_D = 10V$		0.02		±0.5	50		±1.0	50	
$I_{D(off)}$	D	1	$V_D = 10V$, $V_S = -10V$		0.02		±1.0	100		±2.0	100	
		1	$V_D = -10V$, $V_S = 10V$		0.05			100			100	
$I_{D(on)}$	D	8	$V_{S(All)} = V_D = 10V$	Sequence each switch on	0.1		±2.0	100		±5.0	100	
		8	$V_{S(All)} = V_D = -10V$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$	0.1		±2.0	100		±5.0	100	
FAULT												
I_S with Power OFF	S	8	$V_{SUPP} = 0V$, $V_{IN} = \pm 25V$, $V_{EN} = V_O = 0V$, $A_0, A_1, A_2 = 0V$		1.0		2			5		µA
$I_{S(off)}$ with Overvoltage	S	8	$V_{IN} = \pm 25V$, $V_0 = \pm 10V$		1.0		5			10		
INPUT												
$I_{EN(on)}$ $I_{A(on)}$ or $I_{EN(off)}$ $I_{A(off)}$	A_0, A_1, A_2 or EN	4	$V_A = 2.4V$ or 0V		0.01		−10	−30		−10	−30	µA
		4	$V_A = 15V$ or 0V		0.01		10	30		10	30	
DYNAMIC												
$t_{transition}$	D		See Figure 3		0.3							µs
t_{open}	D		See Figure 4		0.2							
$t_{on(EN)}$	D		See Figure 5		0.6		1.5					
$t_{off(EN)}$	D				0.4		1					
t_{on}-t_{off} Break-Before-Make Delay Settling Time	D	8	$V_{EN} = +5V$, A_0, A_1, A_2 Strobed $V_{IN} = \pm 10V$, Figure 6		10							ns
"OFF" Isolation	D		$V_{EN} = 0$, $R_L = 200\Omega$, $C_L = 3pF$, $V_S = 3VRMS$, $f = 500kHz$		60							dB
$C_{s(off)}$	S		$V_S = 0$	$V_{EN} = 0V$, $f = 140kHz$ to 1 MHz	5							pF
$C_{D(off)}$	D		$V_D = 0$		25							
$C_{DS(off)}$	D to S		$V_S = 0$, $V_D = 0$		1							
SUPPLY												
Supply +	I^+	1	All V_A, $V_{EN} = 5V$		0.5	0.7	0.6	0.5		1.0		mA
Current −	I^-	1	All $V_{ADD} = 0V/5V$		0.02	0.7	0.6	0.5		1.0		

Note 1. Readings taken 400ms after the overvoltage occurs.

Note: All typical values have been guaranteed by characterization and are not tested.

SWITCHING INFORMATION



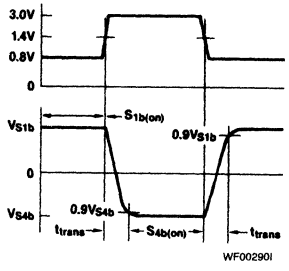
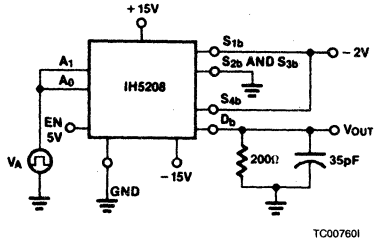


Figure 3: t_{trans} Switching Test



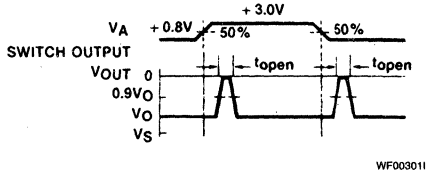
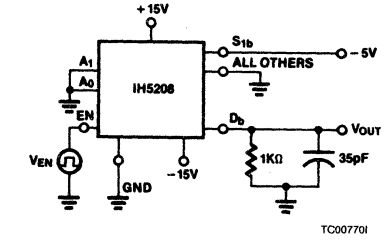


Figure 4: t_{open} (Break-Before-Make) Switching Test



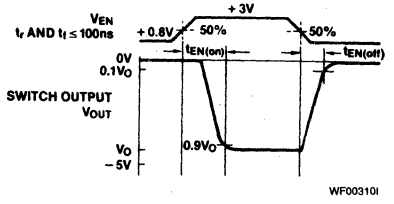


Figure 5: t_{on} and t_{off} Switching Test

Note: All typical values have been guaranteed by characterization and are not tested.

IH5208

SWITCHING INFORMATION (CONT.)

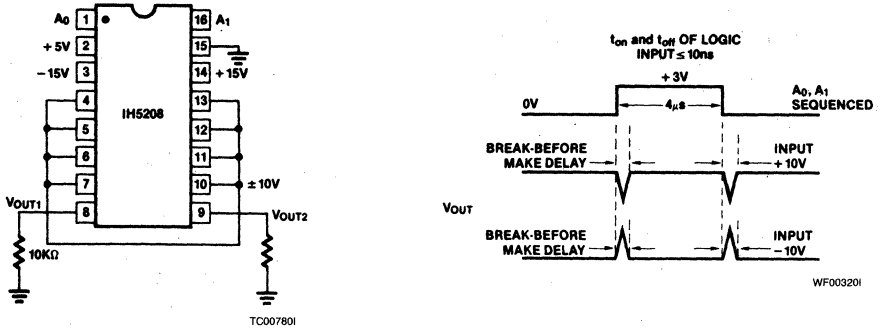


Figure 6: Break-Before-Make Delay Test

DETAILED DESCRIPTION

The IH5208, like all Intersil's multiplexers, contains a set of CMOS switches that form the channels, and driver and decoder circuitry to control which channel turns ON, if any. In addition, the IH5208 contains an internal regulator which provides a fully TTL compatible ENable input that is identical in operation to the Address inputs. This does away with the special conditions that many multiplexer enable inputs require for proper logic swings. The identical circuit conditions of the ENable and Address lines also helps ensure the extension of break-before-make switching to wider multiplexer systems (see applications section).

Another, and more important difference lies in the switching channel. Previous devices have used parallel n- and p-channel MOSFET switches. While this scheme yields reasonably good ON resistance characteristics and allows the switching of rail-to-rail input signals, it also has a number of drawbacks. The sources and drains of the switch transistors will conduct to the substrate if the input goes outside the supply rails, and even careful use of diodes cannot avoid channel-to-output and channel-to-channel coupling in cases of input overrange. The IH5208 uses a novel series arrangement of the p- and n-channel switches (Figure 7) combined with the dielectrically isolated process to eliminate these problems.

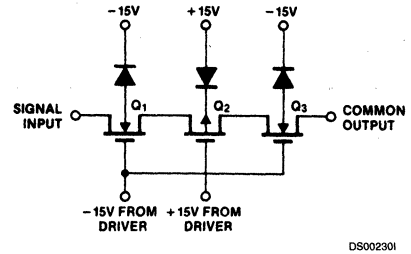
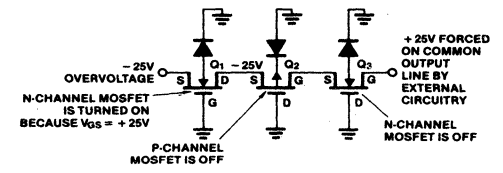
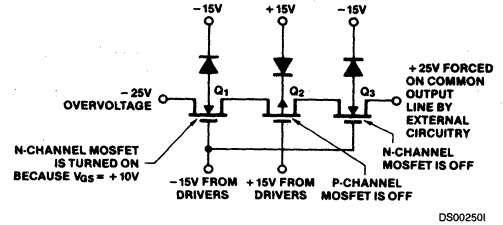


Figure 7: Series Connection of Channel Switches

Within the normal analog signal range, the inherent variation of switch ON resistance will balance out almost as well as the customary parallel configuration, but as the analog signal approaches either supply rail, even for an ON channel, either the p- or the n-channel will become a source follower, disconnecting the channel (Figure 8). Thus protection is provided for any input or output channel against overvoltage, even in the absence of multiplexer supply voltages. This applies up to the breakdown voltage of the respective switches. Figure 9 shows a more detailed schematic of the channel switches, including the back-gate driver devices which ensure optimum channel ON resistances and breakdown voltage under the various conditions.



(a) OVERVOLTAGE WITH MUX POWER OFF



(b) OVERVOLTAGE WITH MUX POWER ON

Figure 8: Overvoltage Protection

Note: All typical values have been guaranteed by characterization and are not tested.

DETAILED DESCRIPTION (CONT.)

Under some circumstances, if the logic inputs are present but the multiplexer supplies are not, the circuit will use the logic inputs as a sort of phantom supply; this could result in an output up to that logic level. To prevent this from occurring, simply ensure that the ENable pin is LOW any time the multiplexer supply voltages are missing (Figure 10).

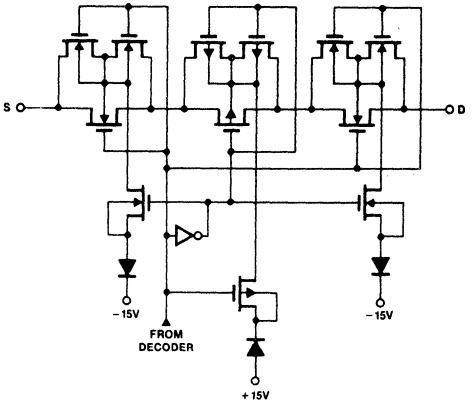


Figure 9: Detailed Channel Switch Schematic

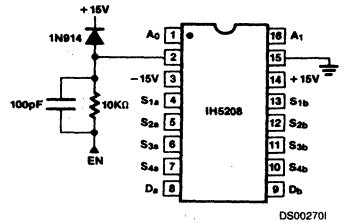


Figure 10: Protection Against Logic Input

MAXIMUM SIGNAL HANDLING CAPABILITY

The IH5208 is designed to handle signals in the ±10V range, with a typical $r_{DS(on)}$ of 600Ω; it can successfully handle signals up to ±13V, however, $r_{DS(on)}$ will increase to about 1.8kΩ. Beyond ±13V the device approaches an open circuit, and thus ±12V is about the practical limit, see Figure 11.

Figure 12 shows the input/output characteristics of an ON channel, illustrating the inherent limiting action of the series switch connection (see Detailed Description), while Figure 13 gives the ON resistance variation with temperature.

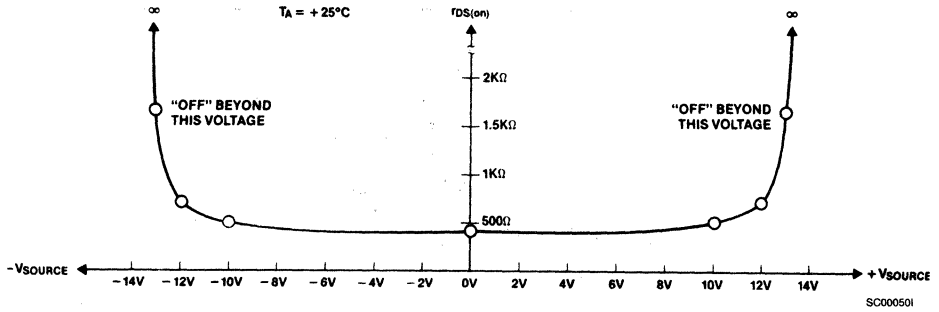


Figure 11: $r_{DS(on)}$ vs Signal Input Voltage @ T_A = +25°C

Note: All typical values have been guaranteed by characterization and are not tested.

IH5208

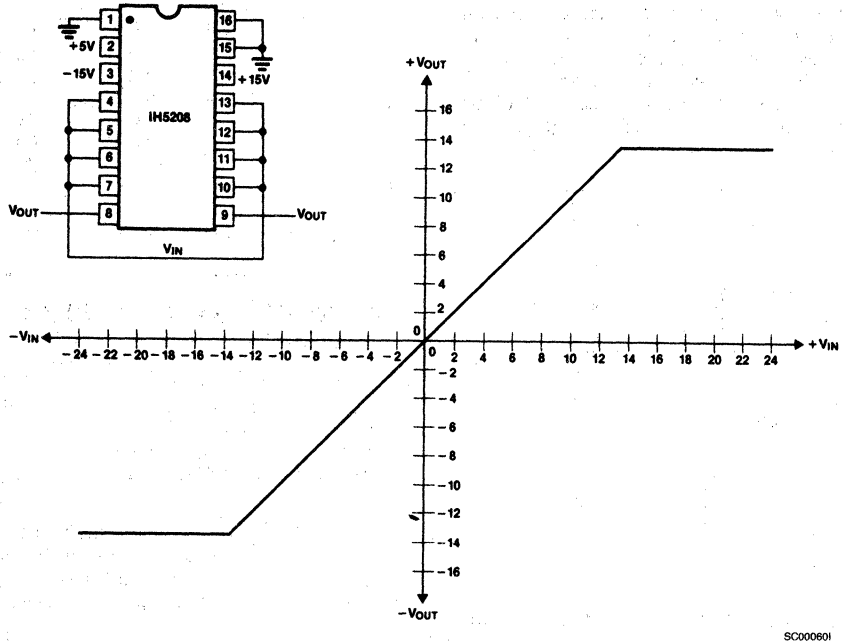


Figure 12: MUX Output Voltage vs Input Voltage Channel 1 Shown; All Channels Similar

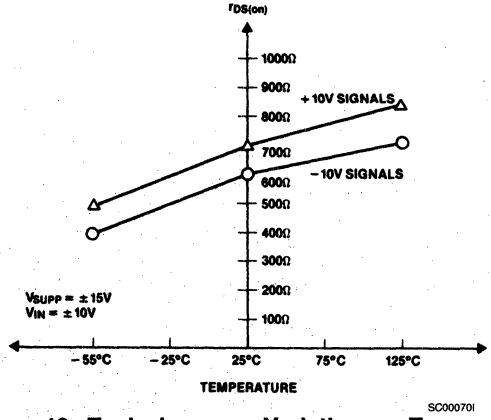


Figure 13: Typical $r_{DS(on)}$ Variation vs Temperature

Note: All typical values have been guaranteed by characterization and are not tested.

USING THE IH5208 WITH SUPPLIES OTHER THAN ±15V

The IH5208 will operate successfully with supply voltages from ±5V to ±15V, however $r_{DS(on)}$ increases as supply voltage decreases, as shown in Figure 14. Leakage currents, on the other hand, decrease with a lowering of supply voltage, and therefore the error term product of $r_{DS(on)}$ and leakage current remains reasonably constant. $r_{DS(on)}$ also decreases as signal levels decrease. For high system accuracy [acceptable levels of $r_{DS(on)}$] the maximum input signal should be 3V less than the supply voltages. The logic thresholds remain TTL compatible.

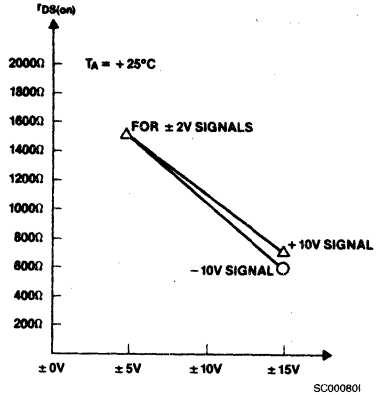


Figure 14: $r_{DS(on)}$ vs Supply Voltages

APPLICATION NOTES

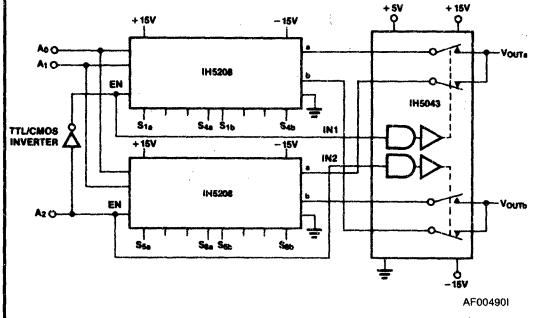
Further information may be found in:

A003 "Understanding and Applying the Analog Switch," by Dave Fullagar

A006 "A New CMOS Analog Gate Technology," by Dave Fullagar

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Slieger

IH5208 APPLICATIONS INFORMATION



DECODE TRUTH TABLE

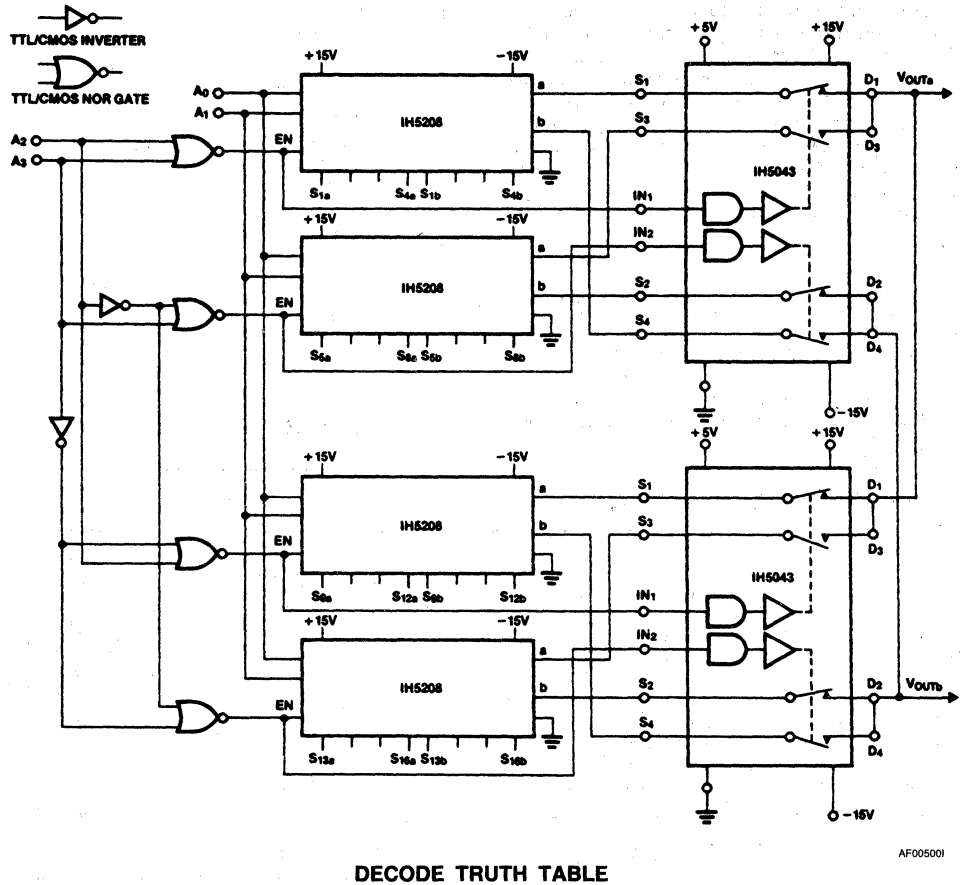
A_2	A_1	A_0	ON SWITCH PAIR
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

Figure 15: 2 of 16 Channel Multiplexer Using Two IH5208s. Overvoltage Protection and Break-Before-Make Switching Are Extended to All Channels.

Note: All typical values have been guaranteed by characterization and are not tested.

IH5208

IH5208 APPLICATIONS INFORMATION (CONT.)



DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	ON SWITCH		ON SWITCH	
0	0	0	0	S1a		S1b	
0	0	0	1	S2a		S2b	
0	0	1	0	S3a		S3b	
0	0	1	1	S4a		S4b	
0	1	0	0	S5a		S5b	
0	1	0	1	S6a		S6b	
0	1	1	0	S7a		S7b	
0	1	1	1	S8a	V_{OUTa}	S8b	V_{OUTb}
1	0	0	0	S9a		S9b	
1	0	0	1	S10a		S10b	
1	0	1	0	S11a		S11b	
1	0	1	1	S12a		S12b	
1	1	0	0	S13a		S13b	
1	1	0	1	S14a		S14b	
1	1	1	0	S15a		S15b	
1	1	1	1	S16a		S16b	

Figure 16: Submultiplexed 2 of 32 System. The Two IH5043s Are Overvoltage Protected By The IH5208s. Submultiplexing Reduces Output Capacitance and Leakage Currents.

Note: All typical values have been guaranteed by characterization and are not tested.

IH5216
8-Channel Differential Fault Protected CMOS Analog Multiplexer

GENERAL DESCRIPTION

The IH5216 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the HI507A and similar devices, but adding fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to ±25V, even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc. Cross talk onto "good" channels is also prevented.

A binary 2-bit address code together with the ENable input allows selection of any channel pair or none at all. These 3 inputs are all TTL compatible for easy logic interface. The ENable input also facilitates MUX expansion and cascading.

FEATURES

- **All Channels OFF When Power OFF, for Analog Signals Up to ±25V**
- **Power Supply Quiescent Current Less Than 1mA**
- **±13V Analog Signal Range**
- **No SCR Latchup**
- **Break-Before-Make Switching**
- **TTL and CMOS Compatible Strobe Control**
- **Pin Compatible With HI507A**
- **Any Channel Turns OFF If Input Exceeds Supply Rails By Up to ±25V**
- **TTL and CMOS Compatible Binary Address and ENable Inputs**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5216MJI	−55°C to +125°C	28 pin CERDIP
IH5216CJI	0°C to +70°C	28 pin CERDIP
IH5216CPI	0°C to +70°C	28 pin Plastic DIP

Ceramic package available as special order only (IH5216MDI/CDI)

DECODE TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "1" = $V_{AH} > 2.4V$ $V_{ENH} > 2.4V$
Logic "0" = $V_{AL} < 0.8V$

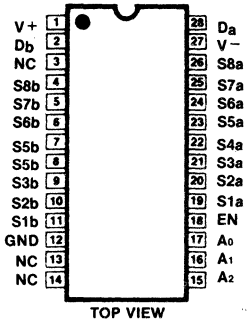


Figure 1: Pin Configuration (Outline dwgs JE, PE)

Note: All typical values have been guaranteed by characterization and are not tested.

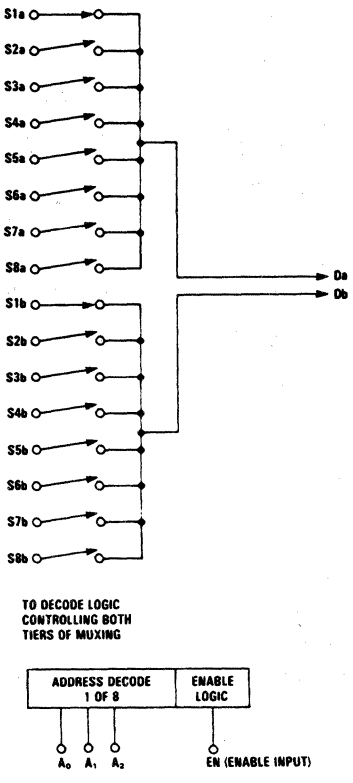


Figure 2: Functional Diagram

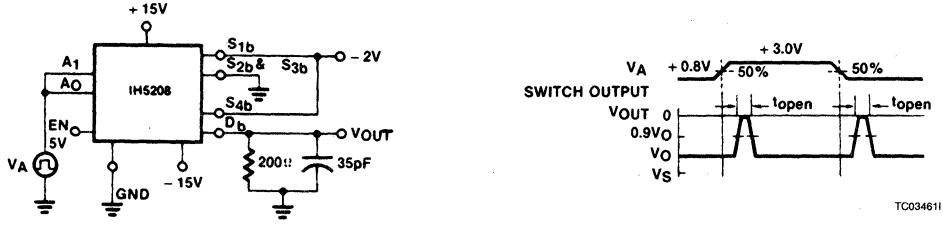


Figure 3: t_{open} (Break-Before-Make) Switching Test

Note: All typical values have been guaranteed by characterization and are not tested.

IH5216

INTERSIL

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V to +15V
V_S or V_D to V^+ ..... +25V to −40V
V_S or V_D to V^- ..... −25V to +40V
V^+ to Ground 16V
V^- to Ground ..... −16V

Current (Any Terminal) 20mA
Operating Temperature ..... −55 to +125°C
Storage Temperature ..... −65 to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Power Dissipation* 1200mW

*All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V^+ = 15V, V^- = −15V, V_{EN} = 2.4V, unless otherwise specified.)

CHARACTERISTIC	MEASURED TERMINAL	NO TESTS PER TEMP	TEST CONDITIONS		TYP 25°C	MAX LIMITS						UNIT
						M SUFFIX			C SUFFIX			
						−55°C	25°C	125°C	0°C	25°C	70°C	
SWITCH												
$R_{DS(on)}$	S to D	16	V_D = 10V, I_S = −1.0mA	Sequence each switch on	700	1000	1000	1500	1200	1200	1800	Ω
		16	V_D = −10V I_S = −1.0mA	V_{AL} = 0.8V, V_{AH} = 2.4V	500	1000	1000	1500	1200	1200	1800	
$\Delta R_{DS(on)}$			$\Delta R_{DS(on)} = \frac{R_{DS(on)max} - R_{DS(on)min}}{R_{DS(on)avg.}}$ V_S = ±10V		5							%
$I_{S(off)}$	S	16	V_S = 10V, V_D = −10V		0.02		±0.5	50		±1.0	50	nA
		16	V_S = −10V, V_D = 10V		0.02		±0.5	50		±1.0	50	
$I_{D(off)}$	D	1	V_D = 10V, V_S = −10V	V_{EN} = 0.8V	0.05		±1.0	100		±2.0	100	
		1	V_D = −10V, V_S = 10V		0.05		±1.0	100		±2.0	100	
$I_{D(on)}$	D	16	$V_{S(All)} = V_D$ = 10V	Sequence each switch on	0.1		±2.0	100		±4.0	100	
		16	$V_{S(All)} = V_D$ = −10V	V_{AL} = 0.8V, V_{AH} = 2.4V	0.1		±2.0	100		±4.0	100	
FAULT												
I_S with Power OFF	S	16	V_{SUPP} = 0V, V_{IN} = ±25V, $V_{EN} = V_O$ = 0V, A_0, A_1, A_2 = 0V or 5V		1.0		2.0			5.0		μA
$I_{S(off)}$ with Overvoltage	S	16	V_{IN} = ±25V, V_O = ±10V		1.0		2.0			5.0		
INPUT												
$I_{EN(on)}$ $I_{A(on)}$ or $I_{EN(off)}$ $I_{A(off)}$	A_0, A_1, A_2 or EN	4	V_A = 2.4V or 0V		0.01		−10	−30		−10	−30	μA
		4	V_A = 15V		0.01		10	30		10	30	
DYNAMIC												
$t_{transition}$	D				0.3		1					μs
t_{open}	D				0.2							
$t_{on(EN)}$	D				0.6		1.5					
$t_{off(EN)}$	D				0.4		1					
t_{on}-t_{off} Break-Before-Make Delay Settling Time	D	16	V_{EN} = +5V, A_0, A_1, A_2 Strobed V_{IN} = ±10V.		25							ns
"OFF" Isolation	D		V_{EN} = 0, R_L = 200Ω, C_L = 3pF, V_S = 3VRMS, f = 500kHz		60							dB
$C_{S(off)}$	S		V_S = 0	V_{EN} = 0V,	5							pF
$C_{D(off)}$	D		V_D = 0	f = 140kHz	25							
$C_{DS(off)}$	D to S		V_S = 0, V_D = 0	to 1 MHz	1							
SUPPLY												
Supply Current +	I^+	1	All V_A = 0V/5V		0.5		0.6			1.0		mA
Supply Current −	I^-	1	V_{EN} = 5V		0.02		0.6			1.0		

Note: All typical values have been guaranteed by characterization and are not tested.

IH5341
Dual SPST CMOS RF/Video Switch

INTERSIL

GENERAL DESCRIPTION

The IH5341 is a dual SPST, CMOS monolithic switch which uses a "Series/Shunt" ("T" switch) configuration to obtain high "OFF" isolation while maintaining good frequency response in the "ON" condition.

Construction of remote and portable video equipment with extended battery life is facilitated by the extremely low current requirements. Switching speeds are typically t_{on} = 150ns and t_{off} = 80ns, and "Break-Before-Make" switching is guaranteed.

Switch "ON" resistance is typically 40Ω–50Ω with ±15V power supplies, increasing to typically 175Ω for ±5V supplies. The devices are available in TO-100 and 14-pin epoxy DIP packages.

FEATURES

- **$R_{DS(on)}$ < 75Ω**
- **Switch Attenuation Varies Less Than 3dB From DC to 100MHz**
- **"OFF" Isolation > 60dB @ 10MHz**
- **Cross Coupling Isolation > 60dB @ 10MHz**
- **Compatible With TTL, CMOS Logic**
- **Wide Operating Power Supply Range**
- **Power Supply Current < 1μA**
- **"Break-Before-Make" Switching**
- **Fast Switching (80ns/150ns Typ)**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5341CPD	0 to +70°C	14-pin PLASTIC DIP
IH5341ITW	−20°C to +85°C	10-pin TO–100
IH5341MTW	−55°C to +125°C	10-pin TO–100

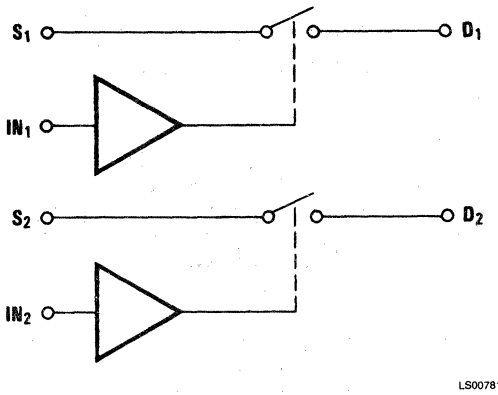
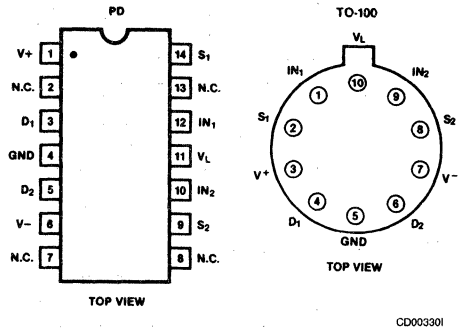


Figure 1: Functional Diagram (Switches are open for a logical "0" control input, and closed for a logical "1" control input.)



Outline dwg: PD Outline dwg: TW

Figure 2: Pin Configurations

Note: All typical values have been guaranteed by characterization and are not tested.

ABSOLUTE MAXIMUM RATINGS

V^+ to Ground ..... +17V
V^- to Ground ..... -17V
V_L to Ground ..... V^+ to V^-
Logic Control Voltage ..... V^+ to V^-
Analog Input Voltage ..... V^+ to V^-
Current (any Terminal) 50mA

Operating Temperature:
(M Version) ..... -55°C to +125°C
(I Version) ..... -25°C to +85°C
(C Version) ..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Power Dissipation 250mW
Derate above 25°C @ ..... 7.5mW/°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

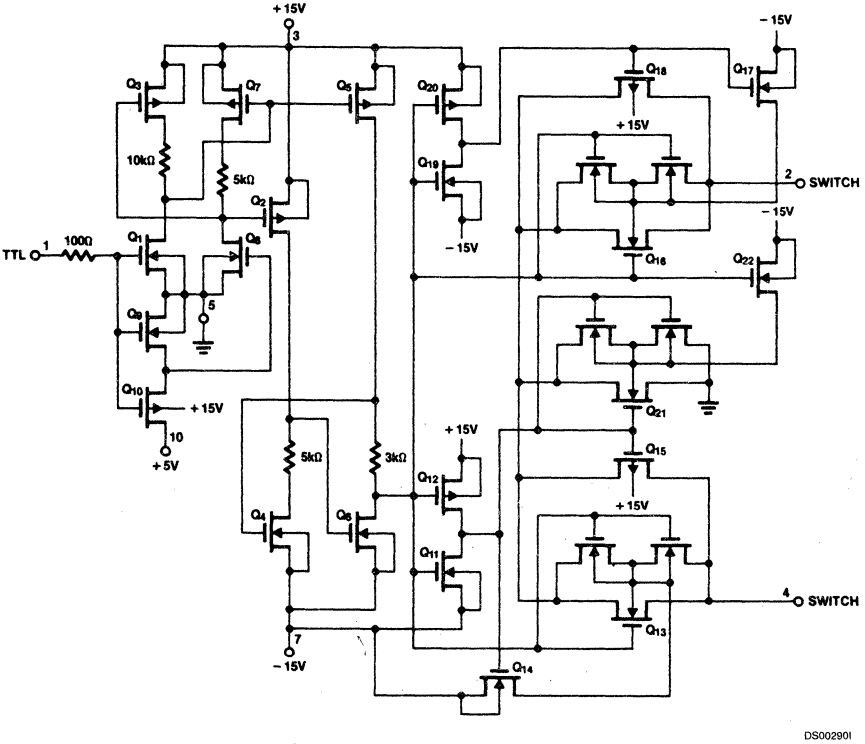


Figure 3: Equivalent Schematic Diagram IH5341ITW (1/2 of actual circuit on chip shown)

Note: All typical values have been guaranteed by characterization and are not tested.

IH5341

INTERSIL

DC ELECTRICAL CHARACTERISTICS

$V^+ = +15V$, $V_L = +5V$, $V^- = -15V$, $T_A = 25°C$ unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	TYP	M GRADE DEVICE			I/C GRADE DEVICE			UNIT
				-55°C	+25°C	+125°C	-25/ 0°C	+25°C	+85/ +70°C	
V^+ V_L V^-	Supply Voltage Ranges Positive Supply Logic Supply Negative Supply	(Note 3)	 4.5 > 16 4.5 > V^+ -4 > -16							V
$R_{DS(on)}$	Switch "ON" Resistance (Note 4)	$V_D = \pm 5V$ $I_S = 10mA$, $V_{IN} \geq 2.4V$ $V_D = \pm 10V$		75 125	75 125	100 175	75 150	75 150	100 175	Ω
$R_{DS(on)}$	Switch "ON" Resistance	$V^+ = V_L = +5V$, $V_{IN} = 3V$ $V^- = -5V$, $V_D = \pm 3V$ $I_S = 10mA$		250	250	350	300	300	350	
$\Delta R_{DS(on)}$	On Resistance Match Between Channels	$I_S = 10mA$, $V_D = \pm 5V$	5							
V_{IH} V_{IL}	Logical "1" Input Voltage Logical "0" Input Voltage		> 2.4 < 0.8							V
$I_{D(off)}$ or $I_{S(off)}$	Switch "OFF" Leakage (Notes 2 and 4)	$V_{S/D} = \pm 5V$ $V_{IN} \leq 0.8V$ $V_{S/D} = \pm 14V$			±0.5 ±0.5	50 50		±1.0 ±1.0	100 100	nA
$I_{D(on)}$ + $I_{S(on)}$	Switch "ON" Leakage	$V_{S/D} = \pm 5V$ $V_{IN} \geq 2.4V$ $V_{S/D} = \pm 14V$			±1 ±1	50 100		±2 ±2	100 100	
I_{IN}	Input Logic Current	$V_{IN} \geq 2.4V$ or $< 0V$	0.1	±1	±1	10	±1	±1	10	µA
I^+	Positive Supply Quiescent Current	$V_{IN} = 0V$ or $+5V$	0.1	1	1	10	1	1	10	
I^-	Negative Supply Quiescent Current	$V_{IN} = 0V$ or $+5V$	0.1	1	1	10	1	1	10	
I_L	Logic Supply Quiescent Current	$V_{IN} = 0V$ or $+5V$	0.1	1	1	10	1	1	10	

NOTES:
1. Typical values are not tested in production. They are given as a design aid only.
2. Positive and negative voltages applied to opposite sides of switch, in both directions successively.
3. These are the operating voltages at which the other parameters are tested, and are not directly tested.
4. The logic inputs are either greater than or equal to 2.4V or less than or equal to 0.8V, as required, for this test.

AC ELECTRICAL CHARACTERISTICS

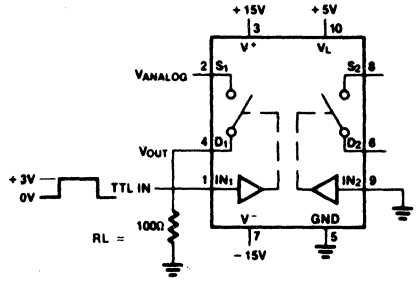
$V^+ = +15V$, $V_L = +5V$, $V^- = 0V$, $T_A = 25°C$ unless otherwise specified (Note 5).

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{on}	Switch "ON" Time	See Figure 4		150	300	ns
t_{off}	Switch "OFF" Time	See Figure 4		80	150	
OIRR	"OFF" Isolation Rejection Ratio	See Figure 5 (Note 6)		60		dB
CCRR	Cross Coupling Rejection Ratio	See Figure 6 (Note 6)		60		
f_{3dB}	Switch Attenuation 3dB Frequency	See Figure 7 (Note 6)		100		

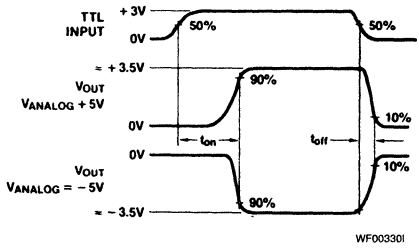
NOTES:
5. All AC parameters are sample tested only.
6. Test circuit should be built on copper clad ground plane board, with correctly terminated coax leads, etc.

Note: All typical values have been guaranteed by characterization and are not tested.

TEST CIRCUITS



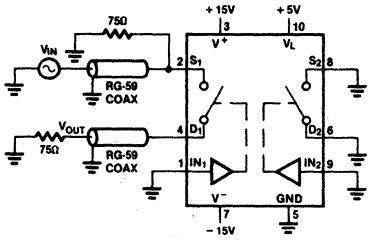
TC00791I



WF00330I

Note: Only one channel shown. Other acts identically.

Figure 4: Switching Time Test Circuit and Waveforms



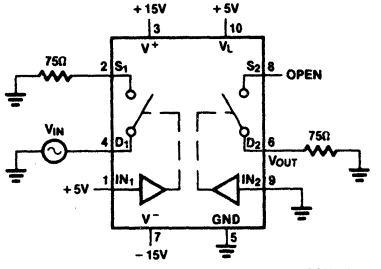
TC00800I

$V_{IN} = \pm 5V\ (10V_{p\text{-}p})\ @\ f = 10MHz$

$$OIRR = 20\log \frac{V_{IN}}{V_{OUT}}$$

Note: Only one channel shown. Other acts identically.

Figure 5: OFF Isolation Test Circuit

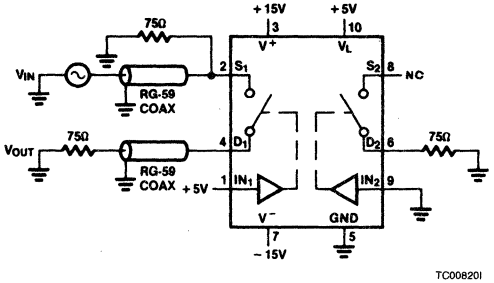


TC00810I

$V_{IN} = 225mVrms\ @\ f = 10MHz$

$$CCRR = 20\log \frac{V_{IN}}{V_{OUT}}$$

Figure 6: Cross-Coupling Rejection Test Circuit



TC00820I

$$ATTN: = 20\ \log_{10} \frac{R_L}{R_{DS(on)} + R_L}$$

Nominally, at DC, this ratio is equal to -4dB. When the attenuation reaches -1dB, the frequency at which this occurs is f_{3dB}.

Note: Only one channel shown. Other acts identically.

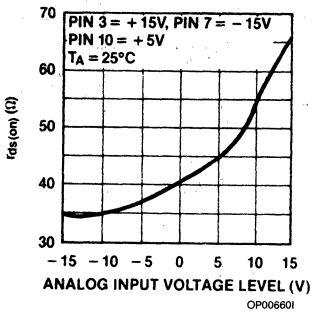
Figure 7: Switch Attenuation Versus Frequency, Test Circuit

Note: All typical values have been guaranteed by characterization and are not tested.

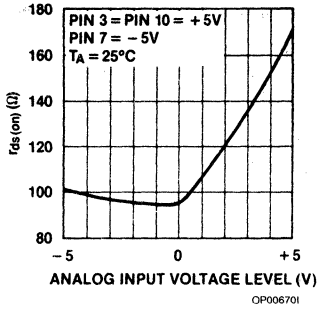
IH5341

TYPICAL PERFORMANCES CHARACTERISTICS

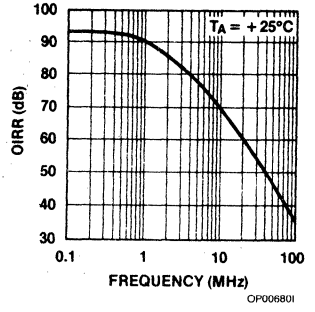
$R_{DS(on)}$ Versus Analog Input Voltage with ±15V Power Supplies



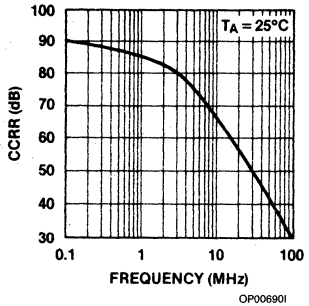
$R_{DS(on)}$ Versus Analog Input Level with ±5V Power Supplies



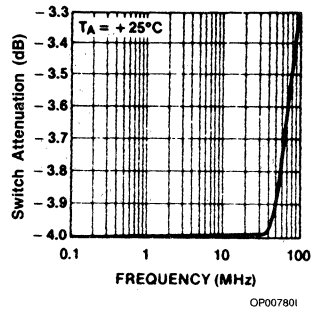
OIRR (OFF Isolation Rejection) Versus Frequency (See Figure 5)



CCRR (Cross Coupling Rejection) Versus Frequency (See Figure 6)



Typical Switch Attenuation Versus Frequency (R_L = 75Ω, See Figure 7)



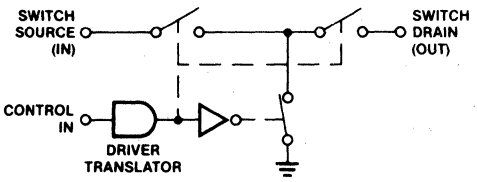
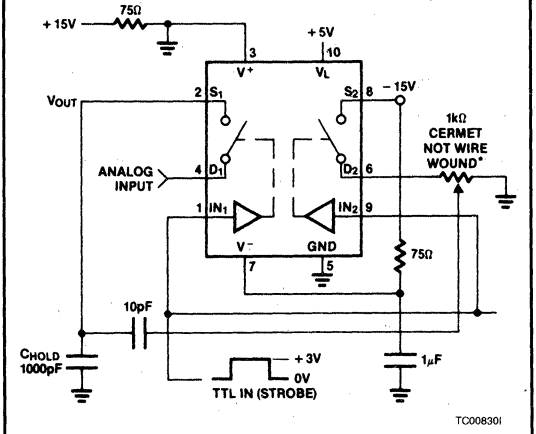


Figure 8: Internal Switch Configuration



*Adjust pot for 0mV$_{p-p}$ step @ V_{OUT} with no analog (AC) signal present

Figure 9: Charge Injection Compensation

DETAILED DESCRIPTION

As can be seen in Figure 8, the switch circuitry is of the so-called "T" configuration, where a shunt switch is closed when the switch is open. This provides much better isolation between the input and the output than single series switch does, especially at high frequencies. The result is excellent performance in the Video and RF region compared to conventional Analog Switches.

The input level shifting circuit is similar to that of the IH5140 Series of Analog Switches, giving very high speed and guaranteed "Break-before-Make" action, with negligible static power consumption and TTL compatibility.

Note: All typical values have been guaranteed by characterization and are not tested.

DETAILED DESCRIPTION (CONT.)

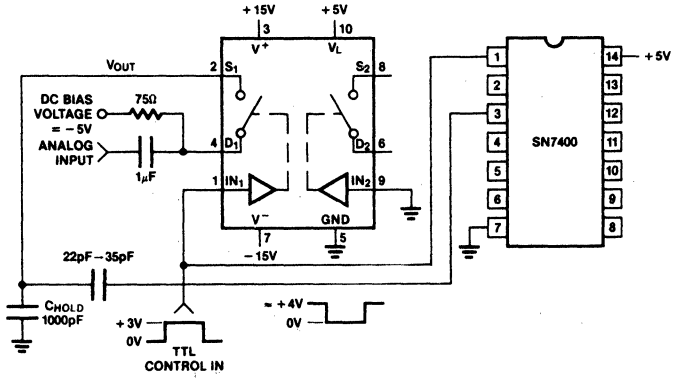


Figure 10: Alternative Compensation Circuit

APPLICATIONS

Charge Compensation Techniques

Charge injection results from the signals out of the level translation circuit being coupled through the gate-channel and gate-source/drain capacitances to the switch inputs and outputs. This feedthrough is particularly troublesome in Sample-and-Hold or Track-and-Hold applications, as it causes a Sample (Track) to Hold offset. The IH5341 devices have a typical injected charge of 30pC-50pC (corresponding to 30mV-50mV in a 1000pF capacitor), at $V_{S/D}$ of about 0V.

This Sample (Track) to Hold offset can be compensated by bringing in a signal equal in magnitude but of the opposite polarity. The circuit of Figure 9 accomplishes this charge injection compensation by using one side of the device as a S & H (T & H) switch, and the other side as a generator of a compensating signal. The 1kΩ potentiometer allows the user to adjust the net injected charge to exactly zero for any analog voltage in the −5V to +5V range.

Since individual parts are very consistent in their charge injection, it is possible to replace the potentiometer with a pair of fixed resistors, and achieve less than 5mV error for all devices without adjustment.

An alternative arrangement, using a standard TTL inverter to generate the required inversion, is shown in Figure 10. The capacitor needs to be increased, and becomes the only method of adjustment. A fixed value of 22pF is good for analog values referred to ground, while 35pF is optimum for AC coupled signals referred to −5V as shown in the figure. The choice of −5V is based on the virtual disappearance at this analog level of the transient component of switching charge injection. This combination will lead to a virtually "glitch-free" switch.

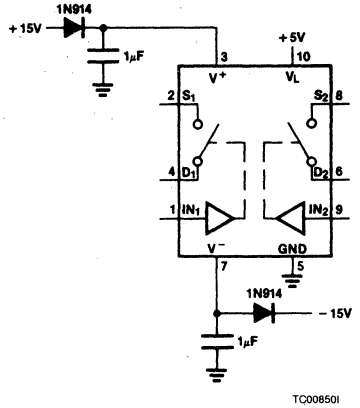


Figure 11: Overvoltage Protection Circuit

Overvoltage Spike Protection

If sustained operation with no supplies but with analog signals applied is possible, it is recommended that diodes (such as 1N914) be inserted in series with the supply lines to the IH5341. Such conditions can occur if these signals come from a separate power supply or another location, for example. The diodes will be reverse biased under this type of operation, preventing heavy currents from flowing from the analog source through the IH5341.

The same method of protection will provide over ±25V overvoltage protection on the analog inputs when the supplies are present. The schematic for this connection is shown in Figure 11.

Note: All typical values have been guaranteed by characterization and are not tested.

IH5352
QUAD SPST CMOS RF/Video Switch

INTERSIL

GENERAL DESCRIPTION

The IH5352 is a QUAD SPST, CMOS monolithic video switch which uses a "Series/Shunt" ("T" switch) configuration to obtain high "OFF" isolation while maintaining good frequency response in the "ON" condition.

Construction of remote and portable video equipment with extended battery life is facilitated by the extremely low current requirements. Switching speeds are typically t_{on} = 150ns and t_{off} = 80ns, and "Break-Before-Make" switching is guaranteed.

Switch "ON" resistance is typically 40Ω-50Ω with ±15V power supplies, increasing to typically 175Ω for ±5V supplies.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5352CPE	0°C to +70°C	16-PIN PLASTIC DIP
IH5352IJE	-25°C to +85°C	16-PIN CERDIP
IH5352MJE	-55°C to +125°C	16-PIN CERDIP

FEATURES

- **$R_{DS(on)}$ < 75Ω**
- **Switch Attenuation Varies Less Than 3dB From DC to 100MHz**
- **"OFF" Isolation > 60dB @ 10MHz**
- **Cross Coupling Isolation > 60dB @ 10MHz**
- **Directly Compatible with TTL, CMOS Logic**
- **Wide Operating Power Supply Range**
- **Power Supply Current < 1μA**
- **"Break-Before-Make" Switching**
- **Fast Switching (80ns/150ns Typ)**

APPLICATIONS

- **Video Switch**
- **Communications Equipment**
- **Disk Drives**
- **Instrumentation**
- **CATV**

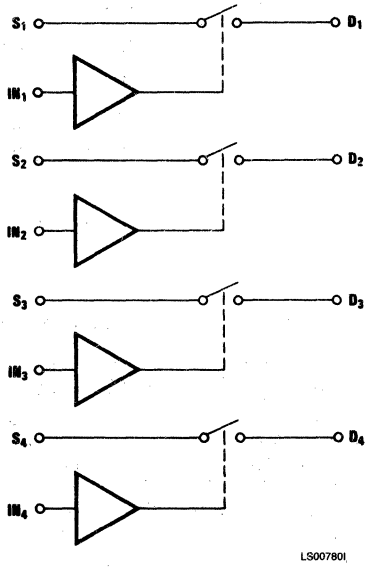


Figure 1: Functional Diagram (Switches are open for a logic "0" control input, and closed for a logic "1" control input.)

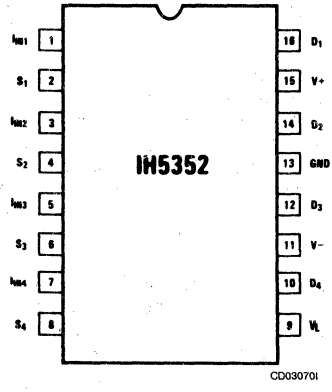


Figure 2: Pin Configurations Package Outline Drawing: PE, JE

305529-003

Note: All typical values have been guaranteed by characterization and are not tested.

IH5352

INTERSIL

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

V^+ to Ground ..... +17V
V^- to Ground ..... −17V
V_L to Ground ..... V^+ to V^-
Logic Control Voltage ..... V^+ to V^-
Analog Input Voltage ..... V^+ to V^-
Current (any terminal) ..... < 50mA
Operating Temperature:
(M Version) ..... −55°C to +125°C
(I Version) ..... −20°C to +85°C
(C Version) ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature
(Soldering, 10sec) ..... 300°C
Power Dissipation:
CERDIP 450mW
derate 4mW/°C above 25°C
Plastic 350mW
derate 3mW/°C above 25°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

V^+ = +15V, V^- = −15V, V_L = +5V, T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS		TYP @25°C	MAXIMUM RATINGS						UNIT
					M GRADE DEVICE			I/C GRADE DEVICE			
					−55°C	+25°C	+125°C	−25/0°C	+25°C	+85/ +70°C	
V^+	Supply Voltage Ranges: Positive Supply	(Note 3)		5 to 15							V
V_L	Logic Supply			5 to 15							
V^-	Negative Supply			−5 to −15							
$R_{DS(on)}$	Switch "ON" Resistance (Note 4)	I_S = 10mA	V_D = ±5V	50	75	75	100	75	75	100	Ω
		$V_{IN} \geq$ 2.4V	V_D = ±10V	100	125	125	175	150	150	175	
$R_{DS(on)}$	Switch "ON" Resistance	I_S = 10mA, $V^+ = V_L$ = +5V V^- = −5V, V_D = ±3V, V_{IN} = 3V		175	250	250	350	300	300	350	
$\Delta R_{DS(on)}$	On Resistance Match Between Channels	I_S = 10mA, V_D = ±5V		5							
V_{IH}	Logical "1" Input Voltage			> 2.4							V
V_{IL}	Logical "0" Input Voltage			< 0.8							
$I_{D(off)}$ or $I_{S(off)}$	Switch 'OFF' Leakage (Note 2 and 4)	$V_{S/D}$ = ±5V, $V_{S/D}$ = ±14V, $V_{IN} \leq$ 0.8V				±1.0	50		±2.0	100	nA
						±1.0	50		±2.0	100	
$I_{D(on)}$ + $I_{S(on)}$	Switch 'ON' Leakage	$V_{S/D}$ = ±5V, $V_{S/D}$ = ±14V, $V_{IN} \geq$ 2.4V				±1.0	100		±2.0	100	
						±1.0	100		±2.0	100	
I_{IN}	Logic Control Input Current	$V_{IN} \geq$ 2.4V or < 0V		0.1	±1	±1	10	±1	±1	10	μA
I^+	Positive Supply Quiescent Current	V_{IN} = 0V or +5V		0.1	1	1	10	1	1	10	
I^-	Negative Supply Quiescent Current	V_{IN} = 0V or +5V		0.1	1	1	10	1	1	10	
I_L	Logic Supply Quiescent Current	V_{IN} = 0V or +5V		0.1	1	1	10	1	1	10	

Note: All typical values have been guaranteed by characterization and are not tested.

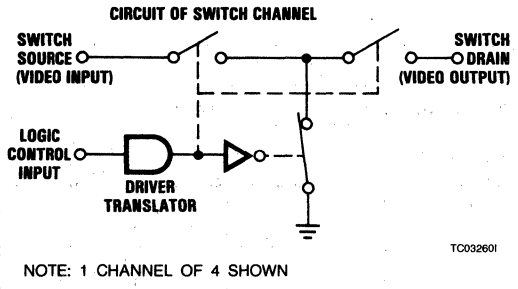
IH5352

AC ELECTRICAL CHARACTERISTICS

$V^+ = +15V$, $V_L = +15V$, $V^- = -15V$, $T_A = 25°C$ unless otherwise specified (Note 5).

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{on}	Switch "ON" Time		150	300	ns
t_{off}	Switch "OFF" Time		80	150	
OIRR	"OFF" Isolation Rejection Ratio		60		dB
CCRR	Cross Coupling Rejection Ratio		60		
f_{3dB}	Switch Attenuation 3dB Frequency		100		MHz

Notes:
1. Typical values are not tested in production. They are given as a design aid only.
2. Positive and negative voltages applied to opposite sides of switch, in both directions successively.
3. These are the operating voltages at which the other parameters are tested, and are not directly tested.
4. The logic inputs are either greater than or equal to 2.4V or less than or equal to 0.8V, as required, for this test.
5. All AC parameters are sample tested only.



NOTE: 1 CHANNEL OF 4 SHOWN

Figure 3: Internal Switch Configuration

DETAILED DESCRIPTION

Figure 3 shows the internal circuit of one channel of the IH5352. This is identical to the IH5341 "T-Switch" configuration. Here, a shunt switch is closed, and the two series switches are open when the video switch channel is open or off. This provides much better isolation between the input and output terminals than a simple series switch does, especially at high frequencies. The result is excellent off-isolation in the Video and RF frequency ranges when compared to conventional analog switches.

The control input level shifting circuitry is very similar to that of the IH5140 series of Analog Switches, and gives very high speed, guaranteed "Break-Before-Make" action, low static power consumption and TTL compatibility.

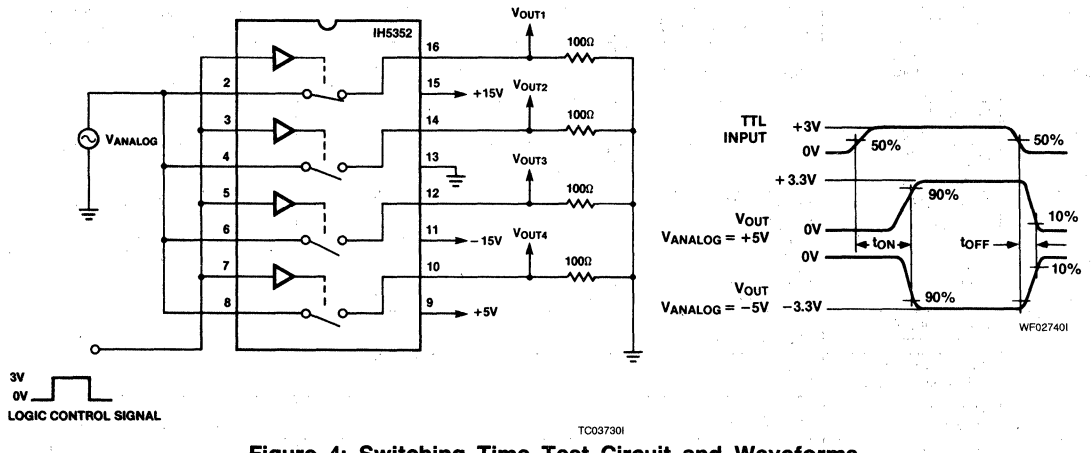
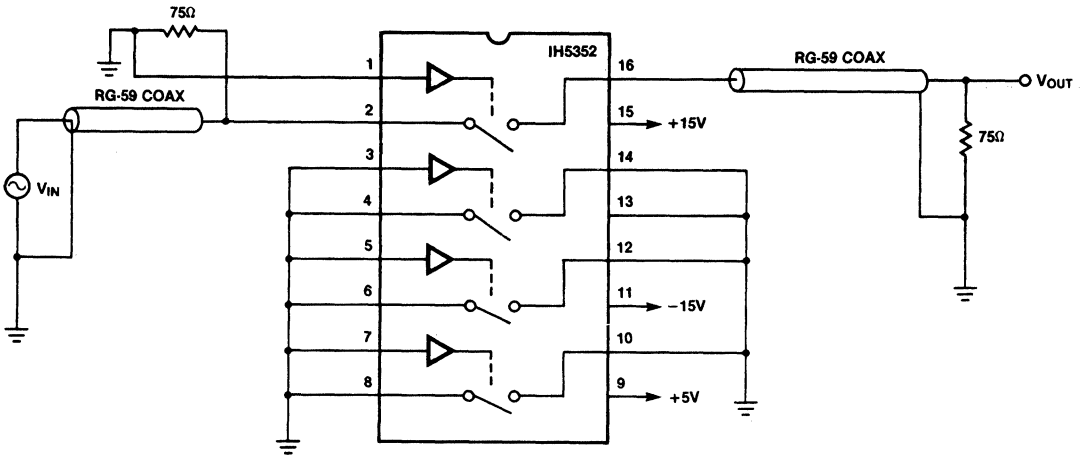


Figure 4: Switching Time Test Circuit and Waveforms

Note: All typical values have been guaranteed by characterization and are not tested.

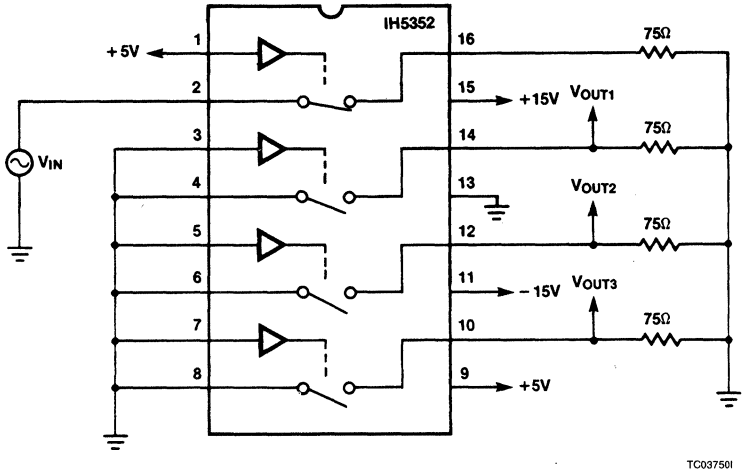


TC03741I

$$OIRR = 20 \text{ LOG } \frac{V_{IN}}{V_{OUT}}$$

V_{IN} = 5V pn SINEWAVE @ 10MHz

Figure 5: Off Isolation Test Circuit



TC03750I

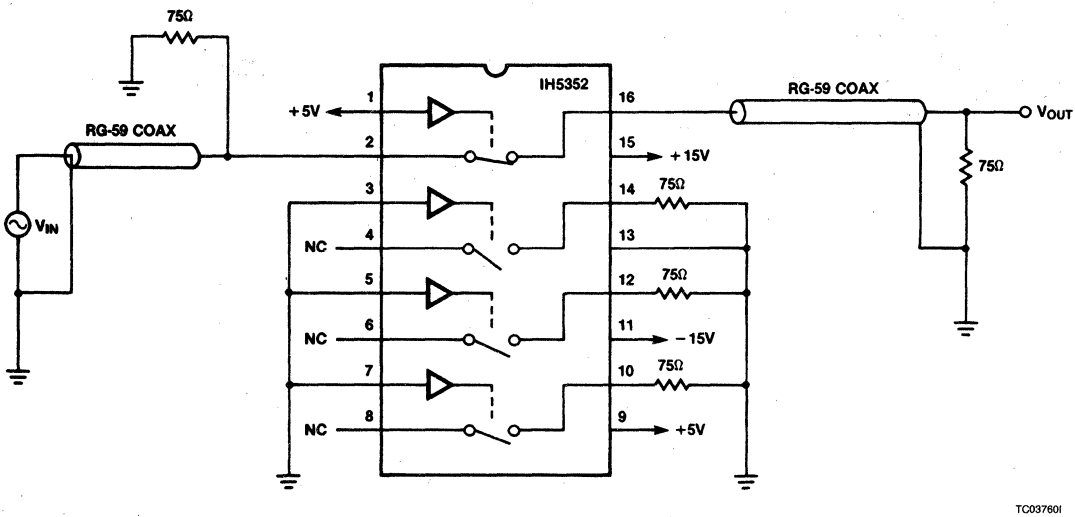
$$CCRR = 20 \text{ LOG } \frac{V_{IN}}{V_{OUT}}$$

V_{IN} = 225mV RMS SINEWAVE @ 10MHz

Figure 6: Cross-Coupling Rejection Test Circuit

Note: All typical values have been guaranteed by characterization and are not tested.

IH5352



f − 3dB = FREQUENCY WHERE DC SWITCH ATTENUATION IS DOWN 3dB

V_{IN} = 225mV RMS @ 10–100MHz

Figure 7: Switch Attenuation −3dB Frequency Test Circuit

Note: All typical values have been guaranteed by characterization and are not tested.

IH6108
8-Channel CMOS Analog Multiplexer

GENERAL DESCRIPTION

The IH6108 is a CMOS monolithic, one of 8 multiplexer. The part is a plug-in replacement for the DG508. Three line decoding is used so that the 8 channels can be controlled by 3 Address inputs; additionally a fourth input is provided for use as a system enable. When the ENable input is high (5V), a channel is selected by the three Address inputs, and when low (0V) all channels are off. The 3 Address inputs are TTL and CMOS logic compatible, with a "1" corresponding to any voltage greater than 2.4V.

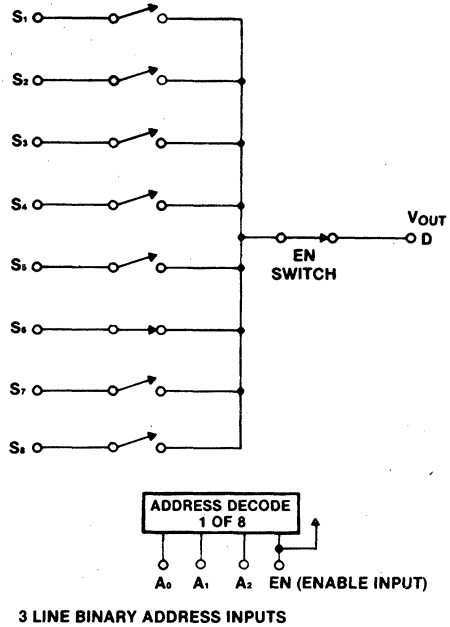
FEATURES

- **Ultra Low Leakage — $I_{D(off)} \leq 100pA$**
- **$r_{DS(on)} < 400$ Ohms Over Full Signal and Temperature Range**
- **Power Supply Quiescent Current Less Than 100μA**
- **$\pm$14V Analog Signal Range**
- **No SCR Latchup**
- **Break-Before-Make Switching**
- **Binary Address Control (3 Address Inputs Control 8 Channels)**
- **TTL and CMOS Compatible Strobe Control**
- **Pin Compatible With DG508, HI-508 & AD7508**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH6108MJE	−55°C to +125°C	16 pin CERDIP
IH6108CJE	0°C to 70°C	16 pin CERDIP
IH6108CPE	0°C to 70°C	16 pin plastic DIP

Ceramic package available as special order only (IH6108MDE/CDE)



3 LINE BINARY ADDRESS INPUTS
(1 0 1) AND EN @ 5V
ABOVE EXAMPLE SHOWS CHANNEL 6 TURNED ON

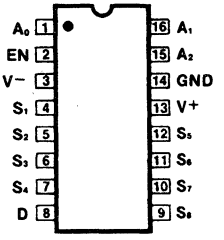
LD002311

Figure 1: Functional Diagram

DECODE TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH
x	x	x	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

A_0, A_1, A_2
Logic "1" = $V_{AH} \geq 2.4V$ $V_{ENH} \geq 4.5V$
Logic "0" = $V_{AL} \leq 0.8V$



CD003411

Figure 2: Pin Configuration

305530-002

Note: All typical values have been guaranteed by characterization and are not tested.

IH6108

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V to 15V
V_S or V_D to V+ ..... 0, −32V
V_S or V_D to V− 0, 32V
V+ to Ground 16V
V− to Ground ..... −16V
Current (Any Terminal) 30mA
Current (Analog Source or Drain) 20mA
Operating Temperature ..... −55 to 125°C
Storage Temperature ..... −65 to 150°C
Lead Temp (Soldering, 10sec) ..... 300°C
Power Dissipation (Package)* 1200mW

*All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

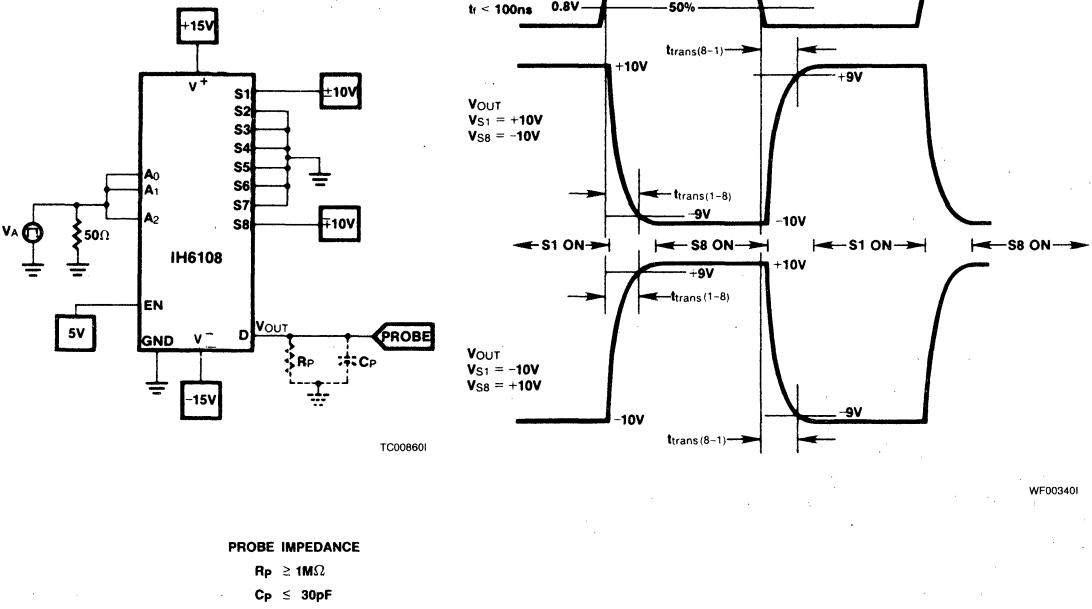
V+ = 15V, V− = −15V, V_{EN} = +5V (Note 1), Ground = 0V, unless otherwise specified.

CHARACTERISTIC		MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	TEST CONDITIONS		MAX LIMITS M SUFFIX −55°C	M SUFFIX 25°C	M SUFFIX 125°C	C SUFFIX 0°C	C SUFFIX 25°C	C SUFFIX 70°C	UNIT
SWITCH													
$r_{DS(ON)}$		S to D	8	180	V_D = 10V, I_S = −1.0mA	Sequence each switch on	300	300	400	350	350	450	Ω
			8	150	V_D = −10V, I_S = −1.0mA	V_{AL} = 0.8V, V_{AH} = 2.4V	300	300	400	350	350	450	
$\Delta r_{DS(ON)}$				20	$\Delta r_{DS(on)} = \frac{\Delta r_{DS(on)}^{min}}{r_{DS(on)}^{avg.}}$ V_S = ±10V								%
$I_{S(OFF)}$		S	8	0.002	V_S = 10V, V_D = −10V			±.5	50		±1	50	nA
			8	0.002	V_S = −10V, V_D = 10V			±.5	50		±1	50	
$I_{D(OFF)}$		D	1	0.03	V_D = 10V, V_S = −10V	V_{EN} = 0.8V		±2	100		±5	100	
			1	0.03	V_D = −10V, V_S = 10V			±2	100		±5	100	
$I_{D(ON)}$		D	8	0.1	$V_{S(ALL)}$ = V_D = 10V	Sequence each switch on		±2	100		±5	100	
			8	0.1	$V_{S(ALL)}$ = V_D = −10V	V_{AL} = 0.8V, V_{AH} = 2.4V		±2	100		±5	100	
INPUT													
$I_{AN(ON)}$ or $I_{A(on)}$		A_0, A_1 or A_2	3	0.01	V_A = 2.4V or 0V			−10	−30		−10	−30	μA
$I_{AN(OFF)}$ $I_{A(off)}$		Inputs	3	0.01	V_A = 15V or 0V			10	30		10	30	
I_A		A_0, A_1 A_2	3		V_{EN} = 5V	All V_A = 0 (Address pins)		−10	−30		−10	−30	
		EN	1		V_{EN} = 0			−10	−30		−10	−30	
DYNAMIC													
$t_{transition}$		D		0.3	See Fig. 1			1					μs
t_{open}		D		0.2	See Fig. 2								
$t_{on(EN)}$		D		0.6	See Fig. 3			1.5					
$t_{off(EN)}$		D		0.4				1					
"OFF" Isolation		D		60	V_{EN} = 0, R_L = 200Ω, C_L = 3pF, V_S = 3VRMS, f = 500kHz								dB
$C_{s(off)}$		S		5	V_S = 0	V_{EN} = 0V, f = 140kHz to 1MHz							pF
$C_{d(off)}$		D		25	V_D = 0								
$C_{DS(off)}$		D to S		1	V_S = 0, V_D = 0								
SUPPLY													
Supply	+	V^+	1	40	V_{EN} = 5V	All V_A = 0 or 5V		200			1000		μA
Current	−	V^-	1	2				100			1000		
Standby	+	V^+	1	1	V_{EN} = 0			100			1000		
Current	−	V^-	1	1				100			1000		

NOTE 1: See Enable Input Strobing Levels, in Application Section.

Note: All typical values have been guaranteed by characterization and are not tested.

SWITCHING INFORMATION



PROBE IMPEDANCE

$R_P \geq 1M\Omega$

$C_P \leq 30pF$

Figure 3: $t_{transition}$ Switching Test

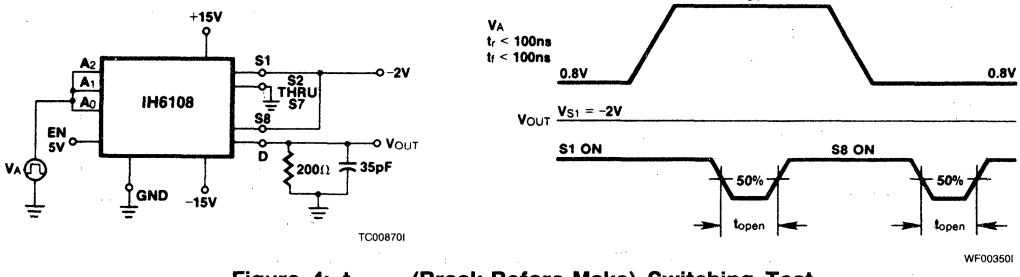


Figure 4: t_{open} (Break-Before-Make) Switching Test

Note: All typical values have been guaranteed by characterization and are not tested.

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SWITCHING INFORMATION (CONT.)

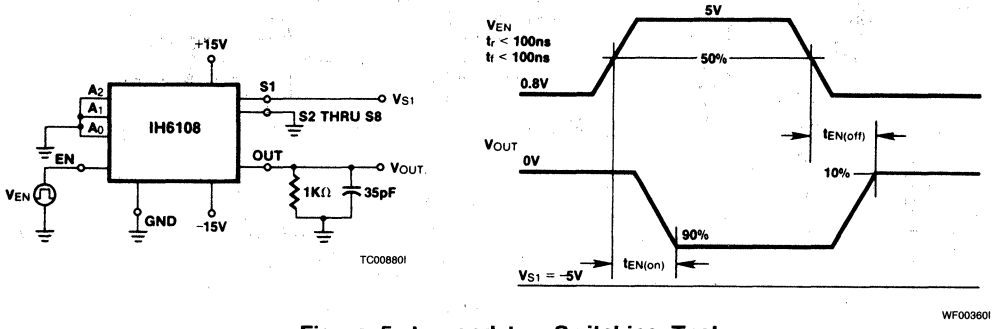

Figure 5: t_{on} and t_{off} Switching Test

IH6108 APPLICATION INFORMATION

ENable Input Strobing Levels

The ENable input on the IH6108 requires a minimum of +4.5V to trigger to the "1" state and a maximum of +0.8V to trigger to the "0" state. If the ENable input is being driven from TTL logic, a pull-up resistor of 1k to 3kΩ is required from the gate output to +5V supply. (See Figure 6)

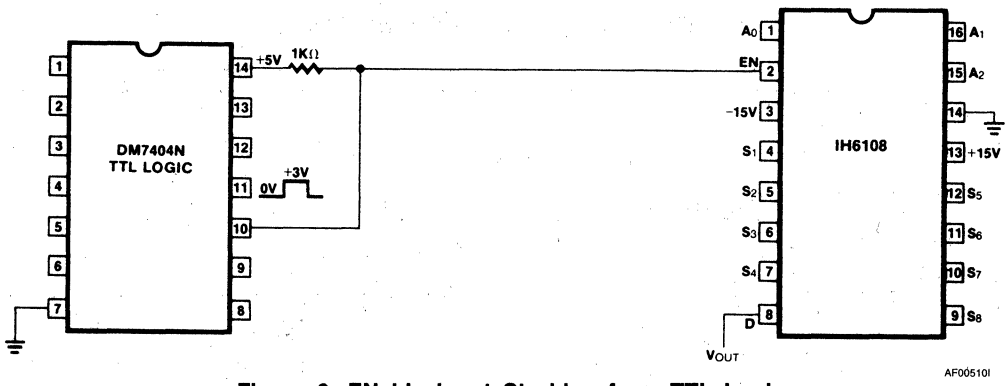

Figure 6: ENable Input Strobing from TTL Logic

When the EN input is driven from CMOS logic, no pullup is necessary, see Fig. 7.

Note: All typical values have been guaranteed by characterization and are not tested.

IH6108 APPLICATION INFORMATION (CONT.)

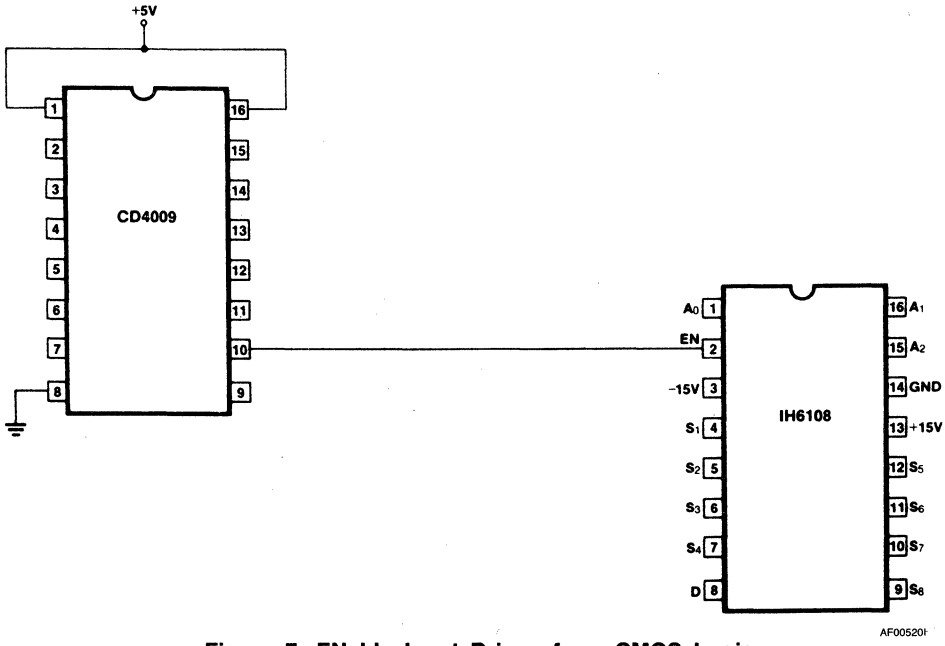

Figure 7: ENable Input Driven from CMOS Logic

The supply voltage of the CD4009 affects the switching speed of the IH6108; the same is true for TTL supply voltage levels. The following chart shows the effect, on t_{trans} for a supply varying from +4.5V to +5.5V.

CMOS OR TTL SUPPLY VOLTAGE	TYPICAL t_{trans} @ 25°C
+4.5V	400ns
+4.75V	300ns
+5.00V	250ns
+5.25V	200ns
+5.50V	175ns

The throughput rate can therefore be maximized by using a +5V to +5.5V supply for the ENable Strobe Logic.

The examples shown in Figures 6 and 7 deal with ENable strobing when expansion to more than eight channels is required. In these cases the EN terminal acts as a fourth address input. If eight channels or less are being multiplexed, the EN terminal can be directly connected to +5V logic supply to enable the IH6108 at all times.

Using the IH6108 with supplies other than ±15V

The IH6108 can be used with power supplies ranging from ±6V to ±16V. The switch $r_{DS(on)}$ will increase as the supply voltages decrease, however, the multiplexer error term (the product of leakage times $r_{DS(on)}$) will remain approximately constant since leakage decreases as the supply voltages are reduced.

Caution must be taken to ensure that the enable (EN) voltage is at least 0.7V below V+ at all times. If this is not done, the Address input strobing levels will not function properly. This may be achieved quite simply by connecting EN (pin 2) to V+ (pin 13) via a silicon diode as shown in Figure 8. When using this type of configuration, a further requirement must be met: the strobe levels of A0 and A1 must be within 2.5V of the EN voltage in order to define a binary "1" state. For the case shown in Figure 8 the EN voltage is 11.3V which means that logic high at A0 and A1 is = +8.8V (logic low continues to be = 0.8V). In this configuration the IH6108 cannot be driven by TTL (+5V) or CMOS (+5V) logic. It can be driven by TTL open collector logic or CMOS logic with +12V supplies.

If the logic and the IH6108 have common supplies, the EN pin should again be connected to the supply through a silicon diode. In this case, tying EN to the logic supply directly will not work since it violates the 0.7V differential voltage required between V+ and EN, (See Figure 9). A 1μF capacitor can be placed across the diode to minimize switching glitches.

Note: All typical values have been guaranteed by characterization and are not tested.

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IH6108 APPLICATION INFORMATION (CONT.)

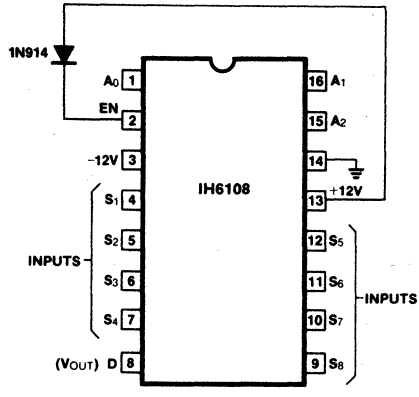


Figure 8: IH6108 Connection Diagram for less than ±15V Supply Operation

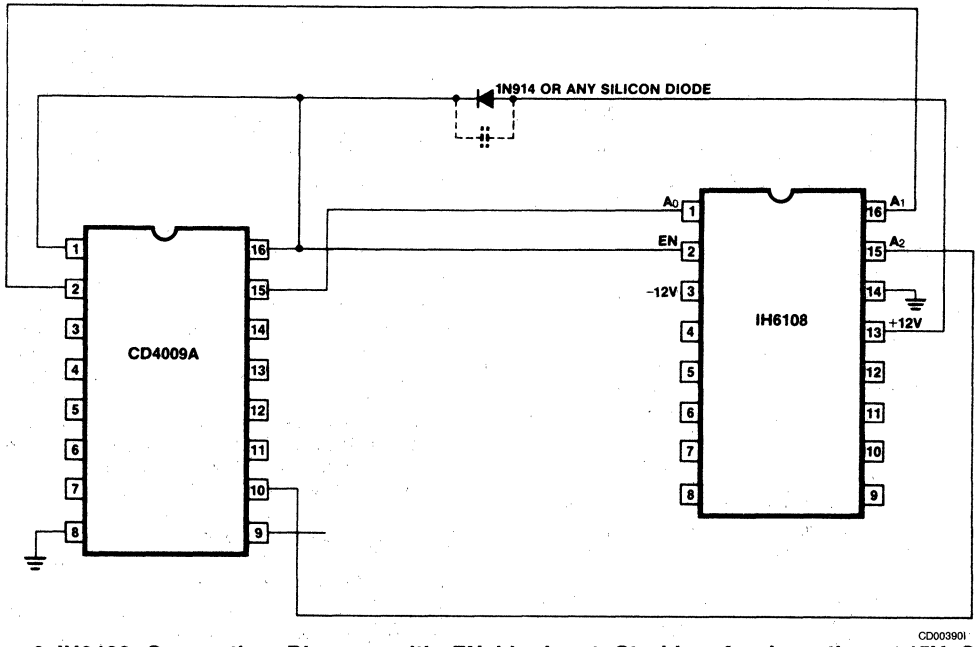


Figure 9: IH6108 Connection Diagram with ENable Input Strobing for less than ±15V Supply Operation

Peak-to-Peak Signal Handling Capability

The IH6108 can handle input signals up to ±14V (actually −15V to +14.3V because of the input protection diode) when using ±15V supplies.

The electrical specifications of the IH6108 are guaranteed for ±10V signals, but the specifications have very minor changes for ±14V signals. The notable changes are slightly lower $r_{DS(on)}$ and slightly higher leakages.

Note: All typical values have been guaranteed by characterization and are not tested.

IH6116
16-Channel CMOS Analog Multiplexer

INTERSIL

GENERAL DESCRIPTION

The IH6116 is a CMOS monolithic, one of 16 multiplexer. The part is a plug-in replacement for the DG506. Four line binary decoding is used so that the 16 channels can be controlled by 4 Address inputs; additionally a fifth input is provided to be used as a system enable. When the ENable input is high (5V) the channels are sequenced by the 4 line Address inputs, and when low (0V), all channels are off. The 4 Address inputs are controlled by TTL logic or CMOS logic elements with a "0" corresponding to any voltage less than 0.8V and a "1" corresponding to any voltage greater than 2.4V. Note that the ENable input must be taken to 5V to enable the system and less than 0.8V to disable the system.

FEATURES

- **Pin Compatible With DG506, HI-506 & AD7506**
- **Ultra Low Leakage — $I_{D(off)} \leq 100pA$**
- **±11 Analog Signal Range**
- **$r_{DS(on)} < 700$ Ohms Over Full Signal and Temperature Range**
- **Break-Before-Make Switching**
- **TTL and CMOS Compatible Address Control**
- **Binary Address Control (4 Address Inputs Control 16 Channels)**
- **Two Tier Submultiplexing to Facilitate Expandability**
- **Power Supply Quiescent Current Less Than 100μA**
- **No SCR Latchup**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH6116MJI	−55°C to +125°C	28 pin CERDIP
IH6116CJI	0°C to 70°C	28 pin CERDIP
IH6116CPI	0°C to 70°C	28 pin Plastic DIP

Ceramic package available as special order only (IH6116MDI/CDI)

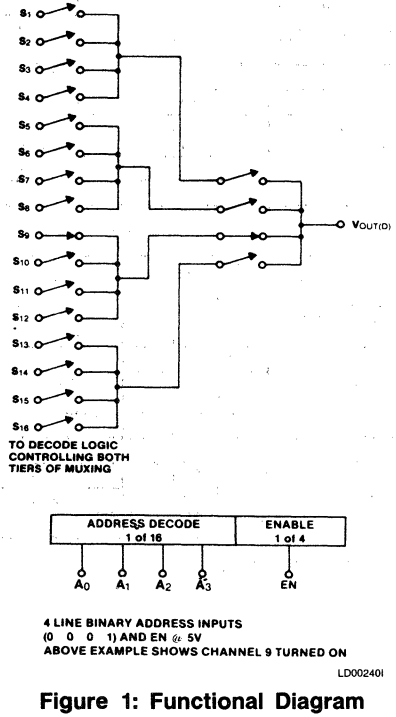


Figure 1: Functional Diagram

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	EN	ON SWITCH
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

Logic "1" = $V_{AH} \geq 2.4V$ $V_{ENH} \geq 4.5V$
Logic "0" = $V_{AL} \leq 0.8V$

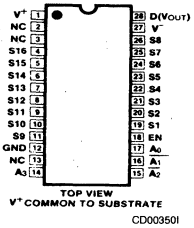


Figure 2: Pin Configuration

305534-002

Note: All typical values have been guaranteed by characterization and are not tested.

IH6116

INTERSIL

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V to 15V
V_S or V_D to V+ ..... 0, −32V
V_S or V_D to V− 0, 32V
V+ to Ground 16V
V− to Ground ..... −16V
Current (Any Terminal) 30mA
Current (Analog Source or Drain) 20mA
Operating Temperature ..... −55 to 125°C
Storage Temperature ..... −65 to 150°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Power Dissipation (Package)* 1200mW

*All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V+ = 15V, V− = −15V, V_{EN} = +5V (Note 1), Ground = 0V, unless otherwise specified.

CHARACTERISTIC		MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	TEST CONDITIONS		MAX LIMITS M SUFFIX −55°C	M SUFFIX 25°C	M SUFFIX 125°C	C SUFFIX 0°C	C SUFFIX 25°C	C SUFFIX 70°C	UNIT
SWITCH													
$r_{DS(ON)}$		S to D	16	480	V_D = 10V, I_S = −1mA	Sequence each switch on	600	600	700	650	650	750	Ω
			16	300	V_D = −10V, I_S = 1mA	V_{AL} = 0.8V, V_{AH} = 3V	600	600	700	650	650	750	
$\Delta r_{DS(ON)}$				20	$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg.}}$ V_S = ±10V								%
$I_{S(OFF)}$		S	16	0.01	V_S = 10V, V_D = −10V			±.5	50		±1	50	nA
			16	0.01	V_S = −10V, V_D = 10V			±.5	50		±1	50	
$I_{D(OFF)}$		D	1	0.1	V_D = 10V, V_S = −10V	V_{EN} = 0.8V		±1	100		±5	100	
			1	0.1	V_D = −10V, V_S = 10V			±2	100		±5	100	
$I_{D(ON)}$		D	16	0.1	$V_{S(ALL)}$ = V_D = 10V	Sequence each switch on		±2	100		±5	100	
			16	0.1	$V_{S(ALL)}$ = V_D = −10V	V_{AL} = 0.8V, V_{AH} = 3V		±2	100		±5	100	
INPUT													
$I_{A(on)}$ or $I_{A(off)}$			4	0.01	V_A = 2.4V			−10	−30		−10	−30	μA
			4	0.01	V_A = 15V			10	30		10	30	
I_A		A_0 A_1 A_2 A_3	4		V_{EN} = 5V	All V_A = 0		−10	−30		−10	−30	
		EN	1		V_{EN} = 0			−10	−30		−10	−30	
DYNAMIC													
t_{trans}		D		0.6	See Fig. 3								μs
t_{open}		D		0.2	See Fig. 4								
$t_{EN(on)}$		D		0.8	See Fig. 5			1.5					
$t_{EN(off)}$		D		0.3				1					
"OFF" Isolation		D		60	V_{EN} = 0, R_L = 200Ω, C_L = 3pF, V_S = 3VRMS, f = 500kHz								dB
$C_{s(OFF)}$		S		5	V_S = 0								pF
$C_{d(OFF)}$		D		40	V_D = 0	V_{EN} = 0, f = 140kHz to 1MHz							
$C_{ds(OFF)}$		D to S		1	V_S = 0, V_D = 0								
SUPPLY													
Supply Current	+	V^+	1	55	V_{EN} = 5V	All V_A = 0 or 5V		200			1000		μA
	−	V^-	1	2				100			1000		
Standby Current	+	V^+	1	1	V_{EN} = 0			100			1000		
	−	V^-	1	1				100			1000		

NOTE 1: See Section V. Enable Input Strobing Levels.

Note: All typical values have been guaranteed by characterization and are not tested.

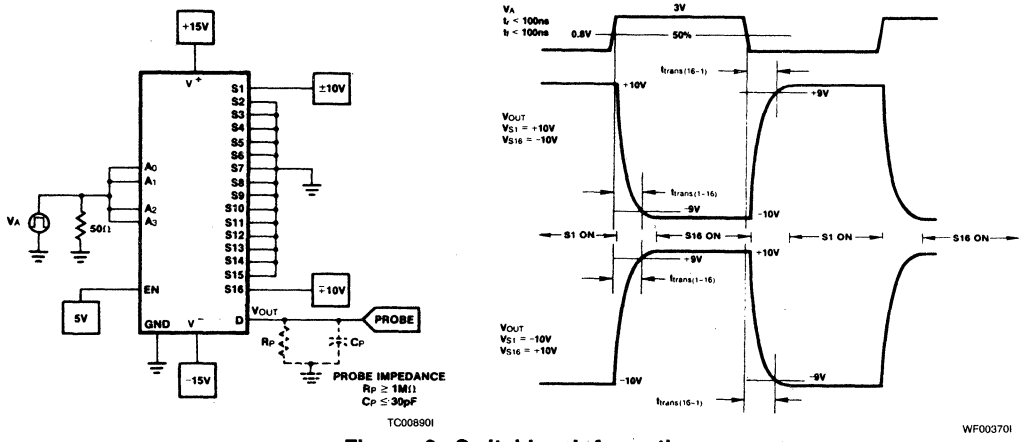


Figure 3: Switching Information

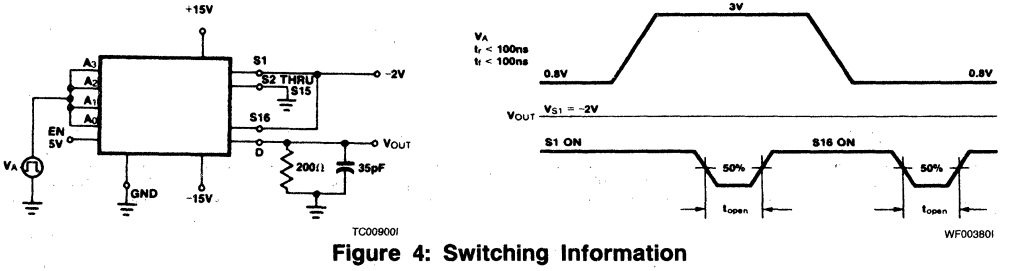


Figure 4: Switching Information

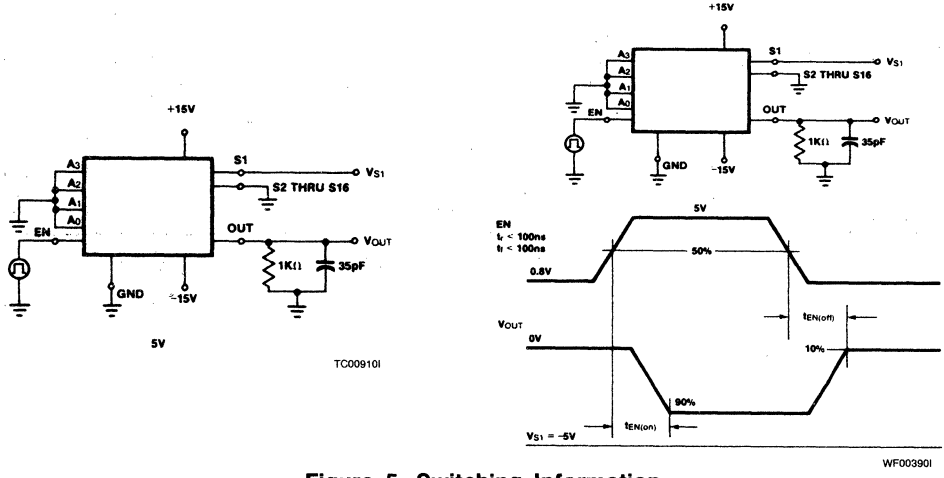
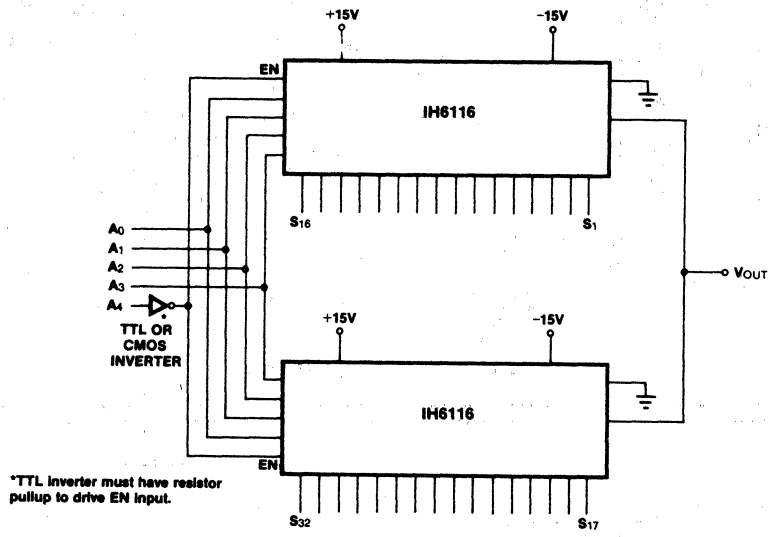


Figure 5: Switching Information

Note: All typical values have been guaranteed by characterization and are not tested.

IH6116

IH6116 APPLICATIONS



DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16

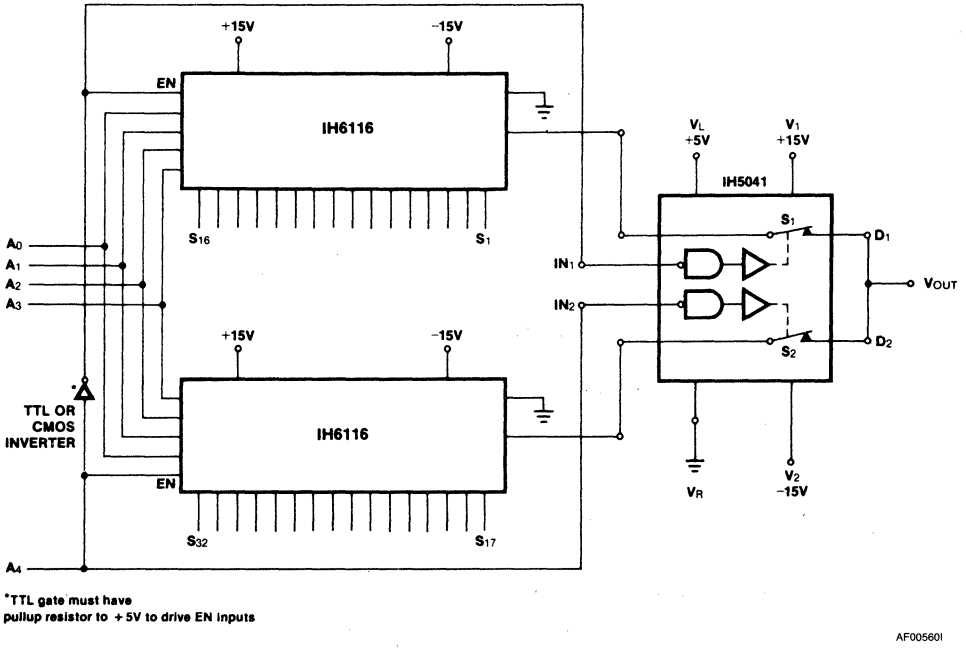
DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
1	0	0	0	0	S17
1	0	0	0	1	S18
1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

Figure 6: 1 Out of 32 Channel Multiplexer Using 2 IH6116s

Note: All typical values have been guaranteed by characterization and are not tested.

IH6116 APPLICATIONS (CONT.)



*TTL gate must have pullup resistor to +5V to drive EN inputs

AF00560I

DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16

DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
1	0	0	0	0	S17
1	0	0	0	1	S18
1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

Figure 7: 1 Out of 32 Channel Multiplexer Using 2 IH6116s; Using An IH5041 for Submultiplexing

Note: All typical values have been guaranteed by characterization and are not tested.

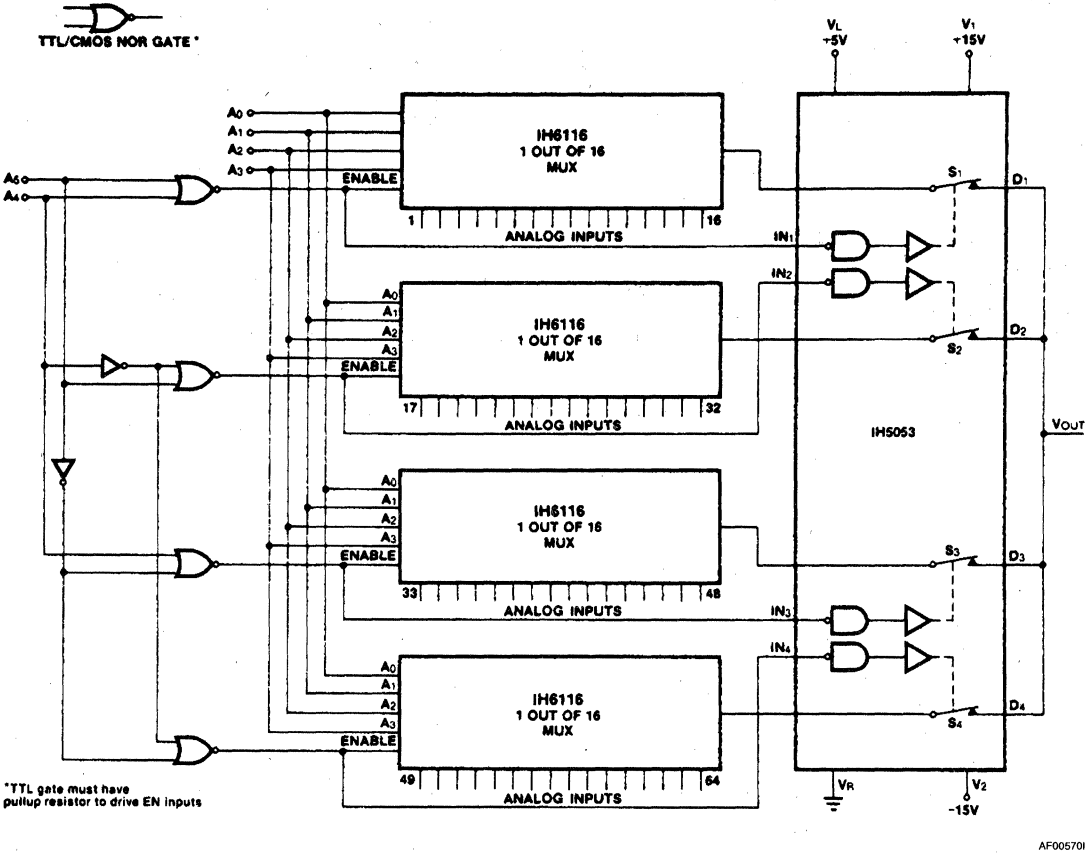


Figure 8: 1 Out of 64 Multiplexer Using 4 1/16s and IH5053 As Submultiplexer

General note on expandability of IH6116

The IH6116 is a two tier multiplexer, where sixteen input channels are routed to a common output in blocks of 4. Each block of 4 input channels is routed to one common output channel, and thus the submultiplexed system looks like 4 blocks of 4 inputs routed to 4 different outputs with the 4 outputs tied together. Thus 20 switches are needed to handle the 16 channels of information. The advantage of this is lower output capacitance and leakage than would be possible with a system using all 16 channels tied to one common output. Also the expandability into 32, 64, 128, channels etc. is facilitated. Figures 6, 7, and 8 show how the IH6116 can be expanded.

Figure 6 shows a 1 of 32 multiplexer, using 2 IH6116s. Since the 6116 is itself a 2 tier MUX, the system as shown is basically a 2 tier system. The four output channels of each 6116 are tied together so that 8 channels are tied to the V_{OUT} common point. Since only one channel of information is on at a time, the common output will consist of 7 OFF channels and 1 ON channel. Thus the output leakage will correspond to 7 $I_{D(offs)}$ and 1 $I_{D(on)}$, or about 1.0nA of typical leakage at room temperature. Throughput speed will be typically 0.8μs for t_{on} and 0.3μs for t_{off}. Throughput channel resistance will be in the 500Ω area.

Figure 7 shows the 1 of 32 MUX of Figure 6, with a third tier of submultiplexing added to further reduce leakage and output capacitance. The IH5041 has typical ON resistances of 50Ω (max. is 75Ω) so it only increases thruput channel resistance from the 500 ohms of Figure 6 to about 550 ohms for Figure 7. Throughput channel speed is a little slower by about 0.5μs for both ON and OFF time, and output leakage is about 0.2nA.

Note: All typical values have been guaranteed by characterization and are not tested.

Figure 8 shows a 1 of 64 MUX using 3 tier MUXing (similar to Figure 7). The Intersil IH5053 is used to get the third tier of MUXing. The V_{OUT} point will see 3 OFF channels and 1 ON channel at any one time, so that the typical leakages will be about 0.4 nA. Throughput channel resistance will be in the 550 ohm area with throughput switching speeds about 1.3μs for ON time and 0.8μs for OFF time.

The IH5053 was chosen as the third tier of the MUX because it will switch the same AC signals as the IH6116 (typically plus and minus 15V) and uses break before make switching. Also power supply quiescent currents are on the order of 1-2μA, so that no excessive system power is dissipated. Note that the logic of the 5053 is such that it can be tied directly to the ENable input (as shown in the figures) with no extra circuitry being required.

Enable input strobing levels

The enable input (EN) acts as an enabling or disabling pin for the IH6116 when used as a 16 channel MUX. However, when expanding the MUX to more than 16 channels, the EN pin acts as another address input. Figures 6 and 7 show the EN pin used as the A4 input.

For the system to function properly the EN input (pin 18) must go to 5V ±5% for the high state and less than 0.8V for the low state. When using TTL logic, a pull-up resistor of 1kΩ or less should be used to pull the output voltage up to 5V. When using CMOS logic, the high state goes to the power supply so no pull-up is required.

If used on high voltage logic supplies, EN should be at least 0.7V below V+ at all times. See IH6108 data sheet for details.

APPLICATION NOTES

Further information may be found in:

A003 "Understanding and Applying the Analog Switch," by Dave Fullagar

A006 "A New CMOS Analog Gate Technology," by Dave Fullagar

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Slieger

R009 "Reduce CMOS Multiplexer Troubles Through Proper Device Selection," by Dick Wilenken

NOTE: This multiplexer does not require external resistors and/or diodes to eliminate what is commonly known as a latch up or SCR action. Because of this fact, the $r_{DS(ON)}$ of the switch is maintained at specified values.

Note: All typical values have been guaranteed by characterization and are not tested.

IH6201
Dual CMOS Driver/Voltage Translator

GENERAL DESCRIPTION

The IH6201 is a CMOS, Monolithic, Dual Voltage Translator; it takes low level TTL or CMOS logic signals and converts them to higher levels (i.e. to ±15V swings). This translator is typically used in making solid state switches, or analog gates.

When used in conjunction with the Intersil IH401 family of Varafets, the combination makes a complete solid state switch capable of switching signals up to 22Vpp and up to 20MHz in frequency. This switch is a "break-before-make" type (i.e. t_{off} time < t_{on} time). The combination has typical $t_{off} \approx 80ns$ and typ. $t_{on} \approx 200ns$ for signals up to 20Vpp in amplitude.

A TTL "1" input strobe will force the θ driver output up to V^+ level; the $\bar{\theta}$ output will be driven down to the V^- level. When the TTL input goes to "0", the θ output goes to V^- and $\bar{\theta}$ goes to V^+; thus θ and $\bar{\theta}$ are 180° out of phase with each other. These complementary outputs can be used to create a wide variety of functions such as SPDT and DPDT switches, etc.; alternatively the complementary outputs can be used to drive N and P channel MOSFETs, to make a complete CMOS analog gate.

The driver typically uses +5V and ±15V power supplies, however a wide range of V^+ and V^- is also possible. It is necessary that $V^+ > 5V$ for the driver to work properly, however.

FEATURES

- **Driven Direct From TTL or CMOS Logic**
- **Translates Logic Levels Up to 30V Levels**
- **Switches $20V_{ACPP}$ Signals When Used in Conjunction With Intersil IH401A Varafet (As An Analog Gate)**
- **$t_{ON} \leq 300ns$ & $t_{OFF} \leq 200ns$ for 30V Level Shifts**
- **Quiescent Supply Current ≤ 100μA for Any State (D.C.)**
- **Provides Both Normal & Inverted Outputs**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE
*IH6201CDE	0°C to 70°C
*IH6201MDE	−55°C → +125°C
IH6201CJE	0°C to 70°C
IH6201MJE	−55°C to 125°C
IH6201CPE	0°C to 70°C

*Special Order Only

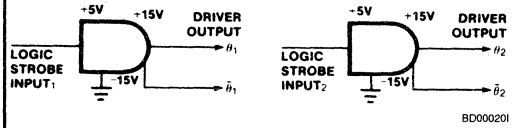
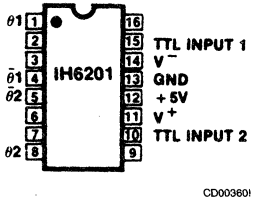


Figure 1: Functional Diagram



(Outline dwgs DE,JE,PE)

Figure 2: Pin Configuration

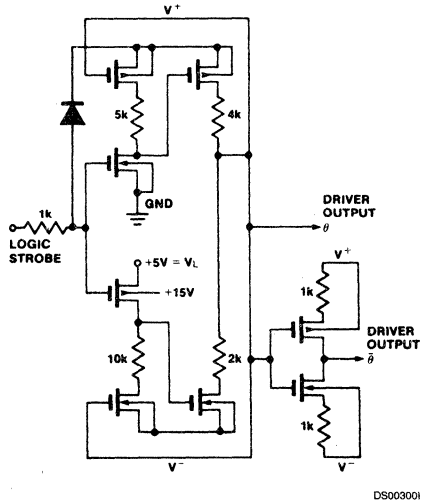


Figure 3: Schematic Diagram (One Channel)

Note: All typical values have been guaranteed by characterization and are not tested.

ABSOLUTE MAXIMUM RATINGS

V^+ to V^- 35V
V^+ 35V
V^- 35V
V^+ to V_{IN} 40V

Operating Temperature ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL SPECIFICATIONS $V^+ = +15V$, $V^- = -15V$, $V_L = +5V$

ITEM	TEST CONDITIONS	IH6201CDE			IH6201MDE			UNIT
		−25°C	+25°C	+85°C	−55°C	+25°C	+125°C	
θ or $\bar{\theta}$ driver output swing	V_{IN} = 0V ⊓⊔ +3V Fig. 5B		28			28		V_{pp}
V_{IN} strobe level ("1")for proper translation	$\theta \geq 14V$ $\bar{\theta} \geq -14V$	3.0	3.0	3.0		2.4		$V_{D.C.}$
V_{IN} strobe level ("0")for proper translation	$\theta \geq -14V$ $\bar{\theta} \geq 14V$	0.4	0.4	0.4		0.8		$V_{D.C.}$
I_{IN} input strobe current draw (for 0V − 5V range)	V_{IN} = 0V or +5V	±1	±1	10	±1	±1	10	μA
t_{on} time	V_{IN} = 0V ⊓⊔ C_L = 30pF switching turn-on time fig. 5B		400			300		ns
t_{off} time	V_{IN} = 0V ⊓⊔ C_L = 30pF switching turn-off time fig. 5B		300			200		ns
I^+ (V^+) power supply quiescent current	V_{IN} = 0V or +5V	100	100	100	100	100	100	μA
I^- (V^-) power supply quiescent current	V_{IN} = 0V or +5V	100	100	100	100	100	100	μA
I_L (V_L) power supply quiescent current	V_{IN} = 0V or +5V	100	100	100	100	100	100	μA

APPLICATIONS

Input Drive Capability

The strobe input lines are designed to be driven from TTL logic levels; this means 0.8V to 2.4V levels max. and min. respectively. For those users who require 0.8V to 2.0V operation, a pull-up resistor is recommended from the TTL output to +5V line. This resistor is not critical and can be in the 1kΩ to 10kΩ range.

When using 4000 series CMOS logic, the input strobe is connected direct to the 4000 series gate output and no pull up resistors, or any other interface, is necessary.

When the input strobe voltage level goes below Gnd (i.e. to −15V) the circuit is unaffected as long as V^+ to V_{IN} does not exceed absolute maximum rating.

Output Drive Capability

The translator output is designed to drive the Intersil IH401 family of Varafets; these are N-channel JFETS with built-in driver diodes. Driver diodes are necessary to isolate the signal source from the driver/translator output; this prevents a forward bias condition between the signal input and the $+V_{CC}$ supply. The IH6201 will drive any JFET provided some sort of isolation is added i.e.

You will notice in Figure 4 that a "referral" resistor has been added from 2N4391 gate to its source. This resistor is needed to compensate for the inadequate charge area curve for isolation diode (i.e. if C vs. V plot for diode ≤ 2 [C vs. V plot for output JFET] switch won't function; then adding this resistor overcomes this condition. The "referral" resistor is normally in the 100kΩ to 1MΩ range and is not too critical.

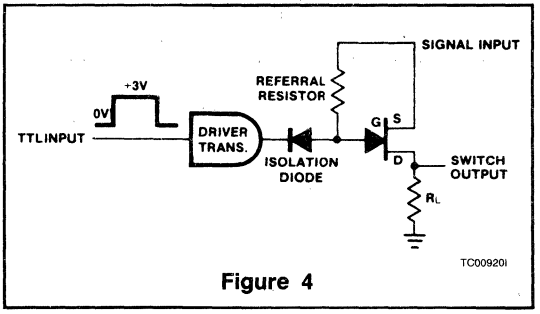


Figure 4

Making a Complete Solid State Switch That Can Handle 20Vpp Signals

The limitation on signal handling capability comes from the output gating device. When a JFET is used, the pinch-off of the JFET acting with the V^- supply does the limiting. In fact max. signal handling capability = 2 (Vp + (V^-)) Vpp where Vp = pinch-off voltage of JFET chosen. i.e. Vp = 7V, V^- = −15V ∴ max. signal handling = 2 (7V + (−15V)) Vpp = 2(7V−15)pp = 2(−8Vpp) = 16Vpp. Obviously to get ≥ 20Vpp, Vp ≥ 5V with V^- = −15V. Another simple way to get 20Vpp with Vp = 7V, is to increase V^- to −17V. In fact using V^+ = +12V or +15V and setting V^- = −18V

Note: All typical values have been guaranteed by characterization and are not tested.

IH6201

APPLICATIONS (CONT.)

allows one to switch 20Vpp with any member of IH401 family. The advantage of using the Vp = 7V pinch-off (along with unsymmetrical supplies), over the Vp = 5V pinch-off (and ±15V supplies), is that you will have a much lower $R_{DS(ON)}$ for the Vp = 7 JFET (i.e. for the 2N4391).

$r_{DS(ON)} \approx 22\Omega$, $V_p = 7V$ $\quad$ $r_{DS(ON)} \approx 35\Omega$, $V_p = 5V$

The IH6201 is a dual translator, each containing 4 CMOS FETs pairs. The schematic of one-half IH6201, driving one-quarter of an IH401, is shown in Figure 5A.

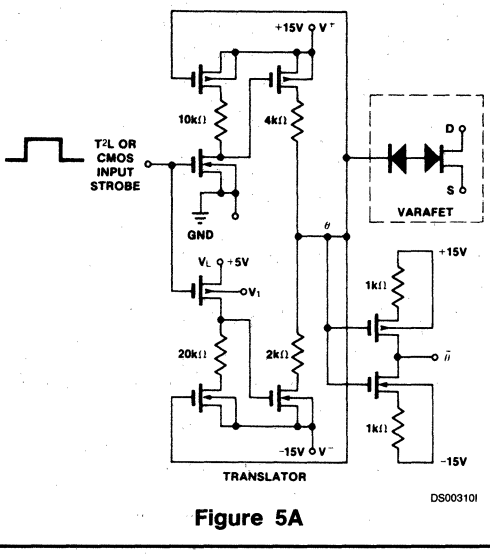


Figure 5A

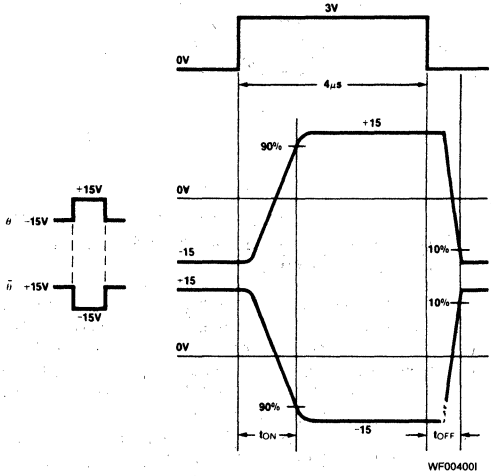


Figure 5B

NOTE: Each translator output has a θ and $\bar{\theta}$ output. θ is just the inverse of $\bar{\theta}$.

A very useful feature of this system is that one-half of an IH6201 and one-half of an IH401 can combine to make a SPDT switch, or an IH6201 plus an IH401 can make a dual SPDT analog switch. (See Figure 8)

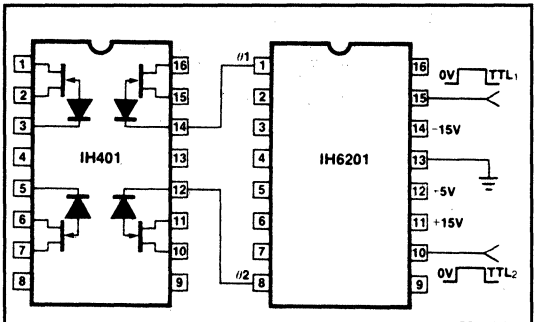


Figure 6: Dual SPST Analog Switch

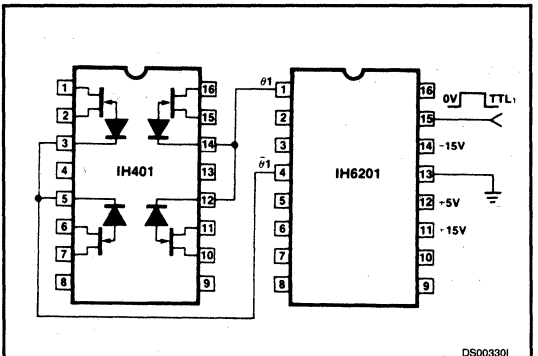


Figure 7: DPDT Analog Switch

NOTE: Either switch is turned on when strobe input goes high.

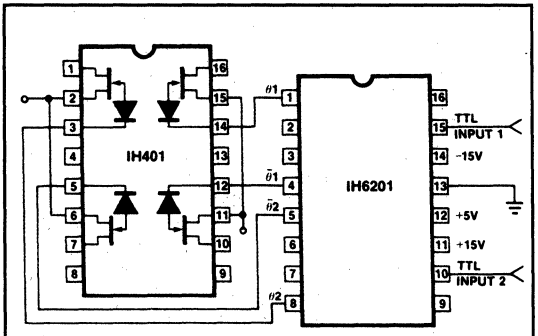


Figure 8: Dual SPDT

Note: All typical values have been guaranteed by characterization and are not tested.

APPLICATIONS (CONT.)

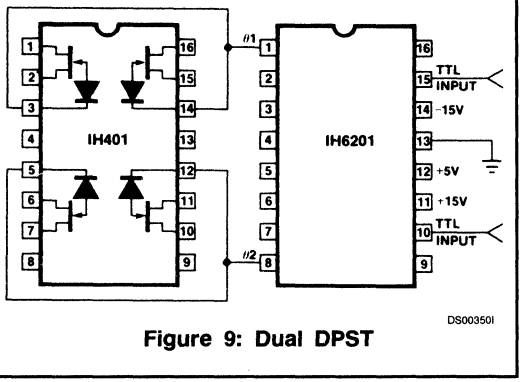


Figure 9: Dual DPST

Note: All typical values have been guaranteed by characterization and are not tested.

IH6208
4-Channel Differential CMOS Analog Multiplexer

INTERSIL

GENERAL DESCRIPTION

The IH6208 is a monolithic 2 of 8 CMOS multiplexer. The part is a plug-in replacement for the DG509. Two line binary decoding is used so that the 8 channels can be controlled in pairs by the binary inputs; additionally a third input is provided to use as a system enable. When the ENable input is high (5V) the channels are sequenced by the 2 line binary inputs, and when low (0V) all channels are off. The 2 Address inputs are controlled by TTL logic or CMOS logic elements with a "0" corresponding to any voltage less than 0.8V and a "1" corresponding to any voltage greater than 2.4V. Note that the ENable input must be taken to 5V to enable the system, and less than 0.8V to disable the system.

FEATURES

- **Ultra Low Leakage — $I_{D(off)} \leq 100pA$**
- **$r_{DS(on)} < 400$ Ohms Over Full Signal and Temperature Range**
- **Power Supply Quiescent Current Less Than 100μA**
- **$\pm 14V$ Analog Signal Range**
- **No SCR Latchup**
- **Break-Before-Make Switching**
- **Binary Address Control (2 Address Inputs Control 2 Out of 8 Channels)**
- **TTL and CMOS Compatible Address Control**
- **Pin Compatible With HI509, DG509 & AD7509**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH6208MJE	−55°C to +125°C	16 pin CERDIP
IH6208CJE	0°C to 70°C	16 pin CERDIP
IH6208CPE	0°C to 70°C	16 pin Plastic DIP

Ceramic package available as special order only (IH6208MDE/CDE)

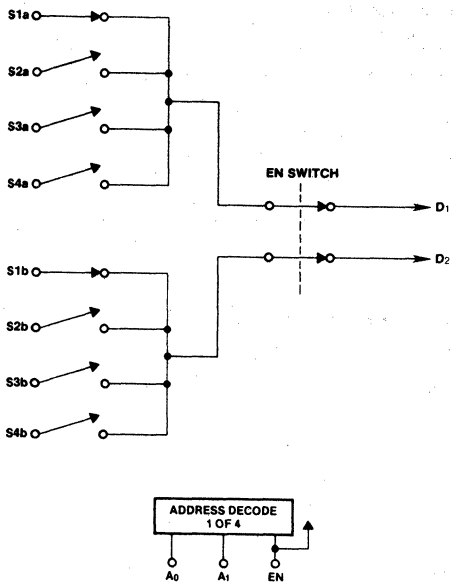


Figure 1: Functional Diagram

DECODE TRUTH TABLE

A_1	A_0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1a, 1b
0	1	1	2a, 2b
1	0	1	3a, 3b
1	1	1	4a, 4b

A_0, A_1
LOGIC "1" = $V_{AH} \geq 2.4V$ $V_{ENH} \geq 4.5V$
LOGIC "0" = $V_{AL} \leq 0.8V$

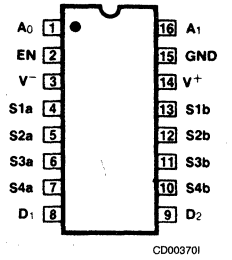


Figure 2: Pin Configuration

Note: All typical values have been guaranteed by characterization and are not tested.

IH6208

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V, V_1
V_S or V_D to V^+ ..... 0, −32V
V_S or V_D to V^- 0, 32V
V^+ to Ground 16V
V^- to Ground ..... −16V
Current (Any Terminal) 30mA
Current (Analog Source or Drain) 20mA
Operating Temperature ..... −55 to 125°C
Storage Temperature ..... −65 to 150°C
Lead Temp (Soldering, 10sec) ..... 300°C
Power Dissipation (Package)* 1200mW

*All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

$V^+ = 15V$, $V^- = -15V$, $V_{EN} = +5V$ (Note 1), Ground = 0V, unless otherwise specified.

CHARACTERISTIC		MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	TEST CONDITIONS		MAX LIMITS M SUFFIX −55°C	M SUFFIX 25°C	M SUFFIX 125°C	C SUFFIX 0°C	C SUFFIX 25°C	C SUFFIX 70°C	UNIT
SWITCH													
$r_{DS(ON)}$		S to D	8	180	$V_D = 10V$, $I_S = -1.0mA$	Sequence each switch on	300	300	400	350	350	450	Ω
			8	150	$V_D = -10V$, $I_S = -1.0mA$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$	300	300	400	350	350	450	
$\Delta r_{DS(ON)}$				20	$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg.}}$ $V_S = \pm 10V$								%
$I_{S(OFF)}$		S	8	0.002	$V_S = 10V$, $V_D = -10V$	$V_{EN} = 0.8V$		±.5	50		±1	50	nA
			8	0.002	$V_S = -10V$, $V_D = 10V$			±.5	50		±1	50	
$I_{D(OFF)}$		D	2	0.03	$V_D = 10V$, $V_S = -10V$			±2	50		±5	100	
			2	0.03	$V_D = -10V$, $V_S = 10V$			±2	50		±5	100	
$I_{D(ON)}$		D	8	0.1	$V_{S(ALL)} = V_D = 10V$	Sequence each switch on		±2	50		±5	100	
			8	0.1	$V_{S(ALL)} = -10V$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$		±2	50		±5	100	
INPUT													
$I_{A(on)}$			2	0.01	$V_A = 2.4V$ or 0V			−10	−30		−10	−30	μA
$I_{A(off)}$			2	0.01	$V_A = 15V$ or 0V			10	30		10	30	
I_A		A_0, A_1	2		$V_{EN} = 5V$	All $V_A = 0$ (Address Pins)		−10	−30		−10	−30	
		EN	1		$V_{EN} = 0$			−10	−30		−10	−30	
DYNAMIC													
$t_{transition}$		D		0.3	See Fig. 3			1					μs
t_{open}		D		0.2	See Fig. 4								
$t_{EN(on)}$		D		0.6	See Fig. 5			1.5					
$t_{EN(off)}$		D		0.4				1					
"OFF" Isolation		D		60	$V_{EN} = 0$, $R_L = 200\Omega$, $C_L = 3pF$, $V_S = 3VRMS$, f = 500kHz								dB
$C_{s(off)}$		S		5	$V_S = 0$								pF
$C_{d(off)}$		D		12	$V_D = 0$	$V_{EN} = 0V$, f = 140kHz to 1MHz							
$C_{ds(off)}$		D to S		1	$V_S = 0$, $V_D = 0$								
SUPPLY													
Supply	+	V^+	1	40		All $V_A = 0$ or 5V		200			1000		μA
Current	−	V^-	1	2	$V_{EN} = 5V$			100			1000		
Standby	+	V^+	1	1				100			1000		
Current	−	V^-	1	1	$V_{EN} = 0$			100			1000		

NOTE 1: See Section 1 Enable Input Strobing Levels.

Note: All typical values have been guaranteed by characterization and are not tested.

IH6208

SWITCHING INFORMATION

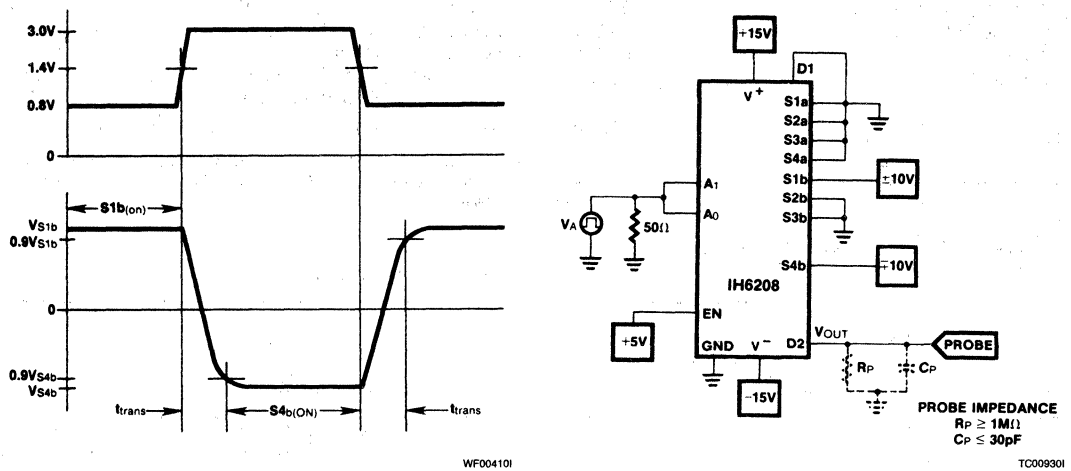


Figure 3: t_{trans} Switching Test

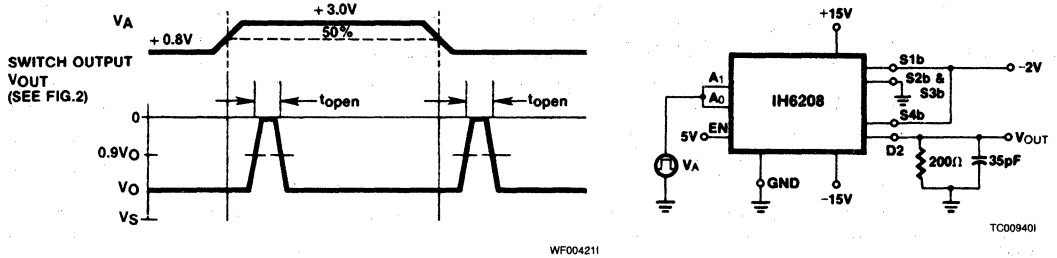


Figure 4: t_{open} (Break-Before-Make) Switching Test

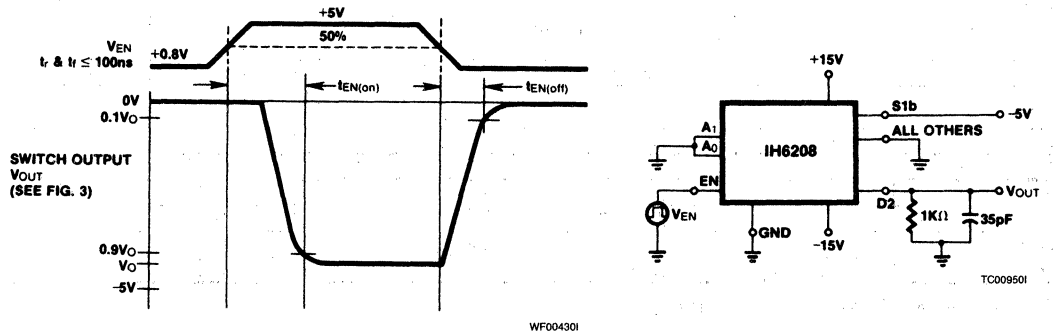


Figure 5: t_{on} and t_{off} Switching Test

Note: All typical values have been guaranteed by characterization and are not tested.

IH6208 APPLICATION INFORMATION

ENable Input Strobing Levels

The ENable input on the IH6208 requires a minimum of +4.5V to trigger it into the "1" state and a maximum of +0.8V to trigger it into the "0" state. If the ENable input is being driven from TTL logic, a pull-up resistor of 1k to 3kΩ is required from the gate output to +5V supply. (See Figure 6).

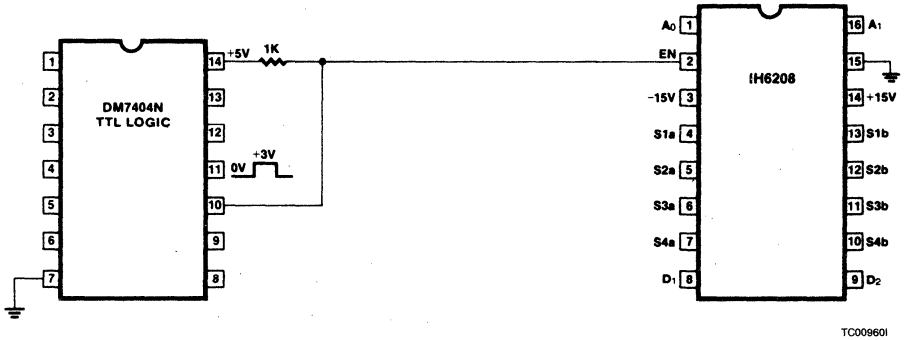


Figure 6: ENable Input Strobing From TTL Logic

When the EN input is driven from CMOS logic, no pullup is necessary. (See Fig. 7)

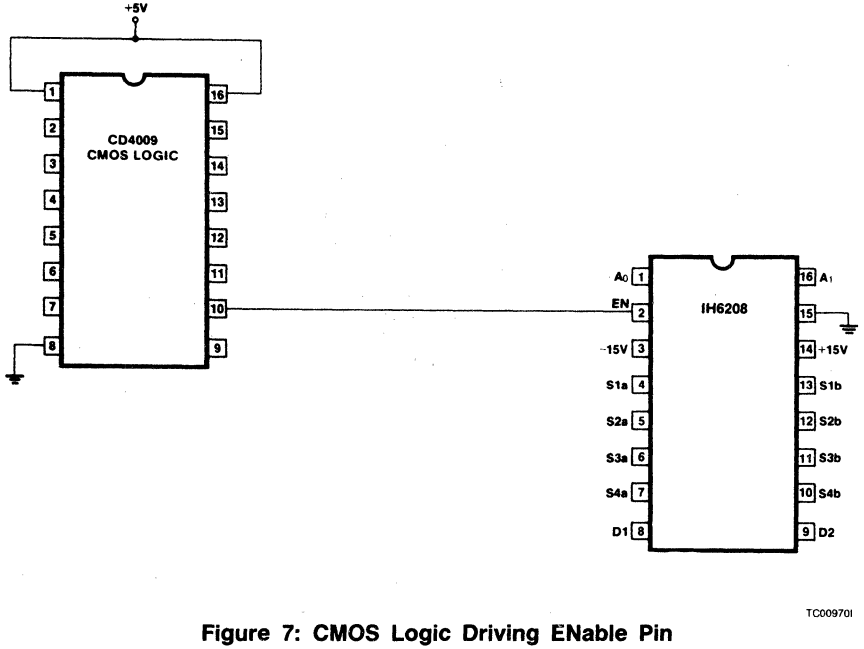


Figure 7: CMOS Logic Driving ENable Pin

Note: All typical values have been guaranteed by characterization and are not tested.

IH6208

IH6208 APPLICATION INFORMATION (CONT.)

The supply voltage of the CD4009 affects the switching speed of the IH6208; the same is true for TTL supply voltage levels. The chart below shows the effect on t_{trans} for a supply varying from +4.5V to +5.5V.

CMOS OR TTL SUPPLY	TYPICAL t_{trans} @ 25°C
+4.5V	400ns
+4.75V	300ns
+5.0V	250ns
+5.25V	200ns
+5.50V	175ns

The throughput rate can therefore be maximized by using a +5V to +5.5V supply for the ENable Strobe Logic.

The examples shown in Figures 6 and 7 deal with ENable strobing when expansion to more than four differential channels is required; in these cases the EN terminal acts as a third address input. If four channel pairs or less are being multiplexed, the EN terminal can be directly connected to +5V to enable the IH6208 at all times.

Using the IH6208 with supplies other than ±15V

The IH6208 can be used with power supplies ranging from ±6V to ±16V. The switch $r_{DS(on)}$ will increase as the supply voltages decrease, however, the multiplexer error term (the product of leakage times $r_{DS(on)}$) will remain approximately constant since leakage decreases as the supply voltages are reduced.

Caution must be taken to ensure that the enable (EN) voltage is at least 0.7V below V^+ at all times. If this is not done the Address Input strobing levels will not function properly. This may be achieved quite simply by connecting EN (pin 2) to V^+ (pin 14) via a silicon diode as shown in Figure 8. A further requirement must be met when using this type of configuration; the strobe levels at A0 and A1 must be within 2.5V of the EN voltage in order to define a binary "1" state. For the case shown in Figure 8 the EN voltage is 11.3V, which means that logic high at A0 and A1 is = +8.8V (logic low continues to be = 0.8V). In this configuration the IH6208 cannot be driven by TTL (+5V) or CMOS (+5V) logic. It can be driven by TTL open collector logic or CMOS logic with +12V supplies.

If the logic and the IH6208 have common supplies, the EN pin should again be connected to the supply through a silicon diode. In this case, tying EN to the logic supply directly will not work since it violates the 0.7V differential voltage required between V^+ and EN (See Figure 9). A 1μF capacitor can be placed across the diode to minimize switching glitches.

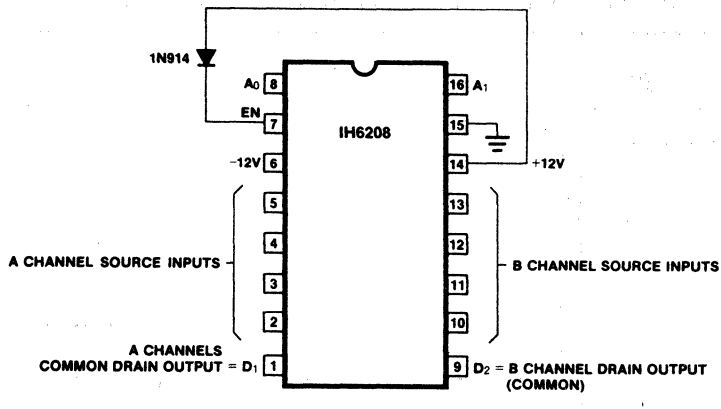


Figure 8: IH6208 Connection Diagram for Less Than ±15V Supply Operation

Note: All typical values have been guaranteed by characterization and are not tested.

IH6208 APPLICATION INFORMATION (CONT.)

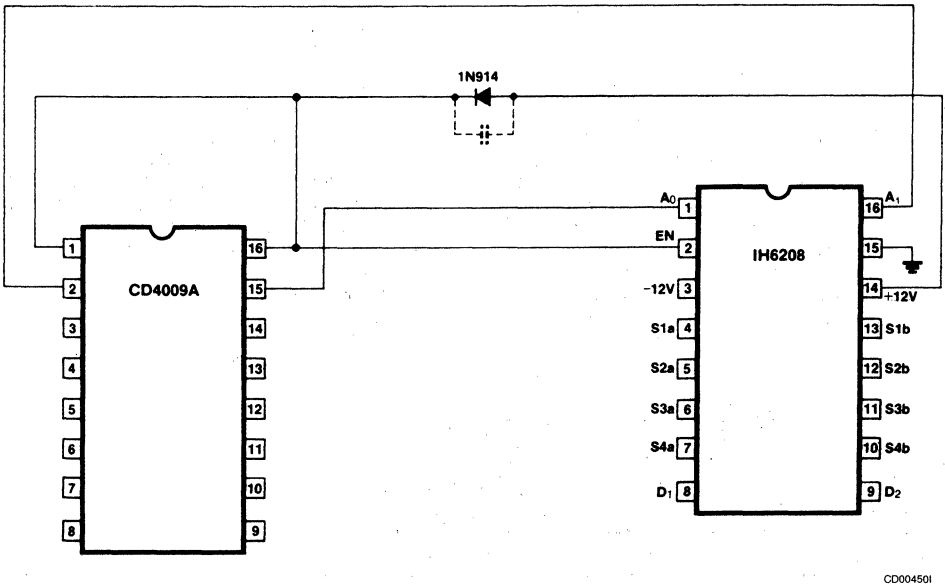


Figure 9: IH6208 Connection Diagram With ENable Input Strobing for Less Than ±15V Supply Operation

Peak-to-Peak Signal Handling Capability

The IH6208 can handle input signals up to ±14V (actually −15V to +14.3V because of the input protection diode) when using ±15V supplies.

The electrical specifications of the IH6208 are guaranteed for ±10V signals, but the specifications have very minor changes for ±14V signals. The notable changes are slightly lower $r_{DS(on)}$ and slightly higher leakages.

Note: All typical values have been guaranteed by characterization and are not tested.

IH6216
8-Channel Differential CMOS Analog Multiplexer

INTERSIL

GENERAL DESCRIPTION

The IH6216 is a CMOS monolithic 2 of 16 multiplexer. The part is a plug-in replacement for the DG507. Three line binary decoding is used so that the 16 channels can be controlled in pairs by the binary inputs; additionally a fourth input is provided to use as a system enable. When the ENable input is high (5V) the channels are sequenced by the 3 line binary inputs, and when low (0V), all channels are off. The 3 Address inputs are controlled by TTL logic or CMOS logic elements with a "0" corresponding to any voltage less than 0.8V and a "1" corresponding to any voltage greater than 3.0V. Note that the ENable input must be taken to 5V to enable the system and less than 0.8V to disable the system.

FEATURES

- **Pin Compatible With HI507, DG507 & AD7507**
- **±11V Analog Signal Range**
- **$r_{DS(on)}$ < 700 Ohms Over Full Signal and Temperature Range**
- **Break-Before-Make Switching**
- **TTL and CMOS Compatible Address Control**
- **Binary Address Control (3 Address Inputs Control 2 Out of 16 Channels)**
- **Two Tier Submultiplexing to Facilitate Expandability**
- **Power Supply Quiescent Current Less Than 100μA**
- **No SCR Latchup**
- **Very Low Leakage $I_{D(OFF)} \leq 100pA$**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH6216MJI	−55°C to +125°C	28 pin CERDIP
IH6216CJI	0°C to 70°C	28 pin CERDIP
IH6216CPI	0°C to 70°C	28 pin Plastic DIP

Ceramic package available as special order only (IH6216MDI/CDI)

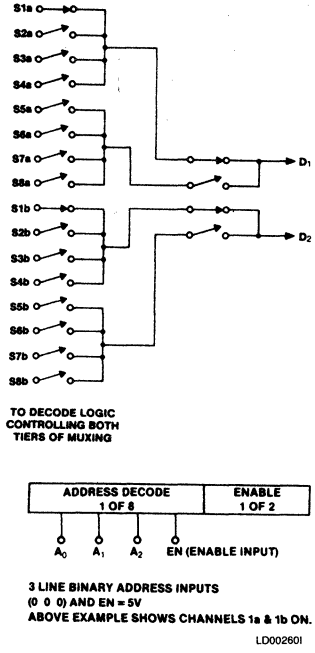


Figure 1: Functional Diagram

DECODE TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

LOGIC "1" = $V_{AH} > 3V$ $V_{ENH} > 4.5V$
LOGIC "0" = $V_{AL} < 0.8V$

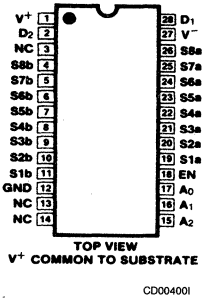


Figure 2: Pin Configuration

Note: All typical values have been guaranteed by characterization and are not tested.

IH6216

INTERSIL

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... $-15V_0$–V_1
V_S or V_D to V+ ..... 0, −32V
V_S or V_D to V− 0, 32V
V+ to Ground 16V
V− to Ground ..... −16V
Current (Any Terminal) 30mA
Current (Analog Source or Drain) 20mA
Operating Temperature ..... −55 to 125°C
Storage Temperature ..... −65 to 150°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Power Dissipation (Package)* 1200mW

*All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

$V^+ = 15V$, $V^- = -15V$, $V_{EN} = +5V$ (Note 1), Ground = 0V, unless otherwise specified.

CHARACTERISTIC		MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	TEST CONDITIONS		MAX LIMITS M SUFFIX −55°C	M SUFFIX 25°C	M SUFFIX 125°C	C SUFFIX 0°C	C SUFFIX 25°C	C SUFFIX 70°C	UNIT
SWITCH													
			16	480	$V_D = 10V$, $I_S = -1mA$	Sequence each switch on	600	600	700	650	650	750	
$r_{DS(ON)}$		S to D	16	300	$V_D = -10V$, $I_S = 1mA$	$V_{AL} = 0.8V$, $V_{AH} = 3V$	600	600	700	650	650	750	Ω
$\Delta r_{DS(ON)}$				20	$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg.}}$	$V_S = \pm 10V$							%
			16	0.01	$V_S = 10V$, $V_D = -10V$			±.5	50		±1	50	
$I_{S(OFF)}$		S	16	0.01	$V_S = -10V$, $V_D = 10V$			±.5	50		±1	50	
			2	0.1	$V_D = 10V$, $V_S = -10V$	$V_{EN} = 0.8V$		±2	100		±5	100	nA
$I_{D(OFF)}$		D	2	0.1	$V_D = -10V$, $V_S = 10V$			±2	100		±5	100	
			16	0.1	$V_{S(ALL)} = V_D = 10V$	Sequence each switch on		±2	100		±5	100	
$I_{D(ON)}$		D	16	0.1	$V_{S(ALL)} = V_D = -10V$	$V_{AL} = 0.8V$, $V_{AH} = 3V$		±2	100		±5	100	
INPUT													
$I_{A(on)}$ or			3	0.01	$V_A = 3.0V$			−10	−30		−10	−30	
$I_{A(off)}$			3	0.01	$V_A = 15V$			10	30		10	30	
I_A		A_0 A_1 A_2 A_3	3		$V_{EN} = 5V$	All $V_A = 0$		−10	−30		−10	−30	µA
		EN	1		$V_{EN} = 0$			−10	−30		−10	−30	
DYNAMIC													
t_{trans}		D		0.6	See Fig. 3			1					
t_{open}		D		0.2	See Fig. 4								
$t_{on(EN)}$		D		0.8	See Fig. 5			1.5					µs
$t_{off(EN)}$		D		0.3				1					
"OFF" Isolation		D		60	$V_{EN} = 0$, $R_L = 200\Omega$, $C_L = 3pF$, $V_S = 3VRMS$, f = 500kHz								dB
C_s		S		5	$V_S = 0$								
$C_{d(off)}$		D		20	$V_D = 0$	$V_{EN} = 0$, f = 140kHz to 1MHz							pF
C_{ds}		D to S		1	$V_S = 0$, $V_D = 0$								
SUPPLY													
Supply	+	V^+	1	55				200			1000		
Current	−	V^-	1	2	$V_{EN} = 5V$			100			1000		
Standby	+	V^+	1	1		All $V_A = 0$ or 5V		100			1000		µA
Current	−	V^-	1	1	$V_{EN} = 0$			100			1000		

NOTE 1: See Enable Input Strobing Levels, Section 1.

3

Note: All typical values have been guaranteed by characterization and are not tested.

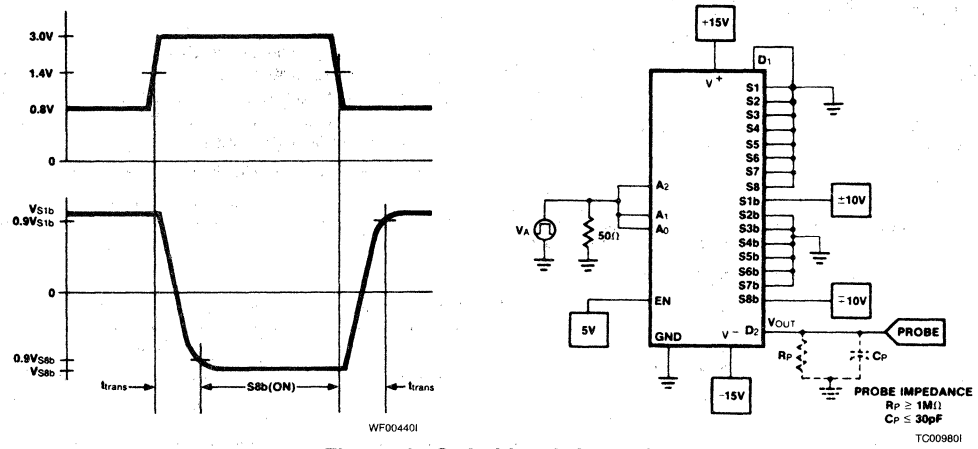


Figure 3: Switching Information

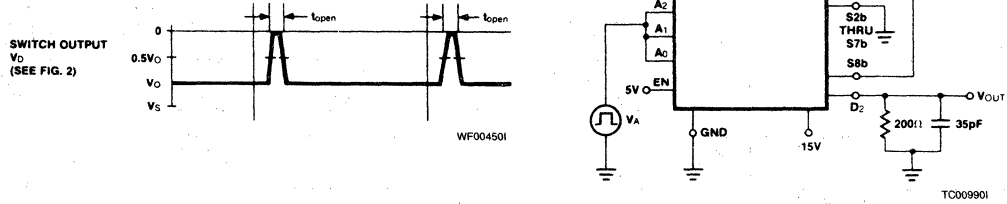


Figure 4: Switching Information

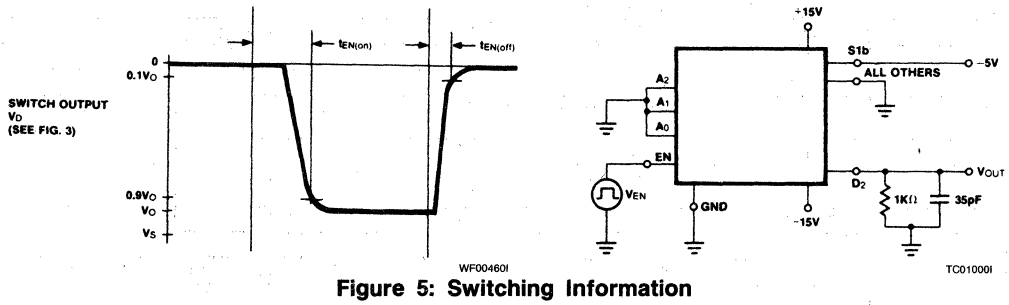
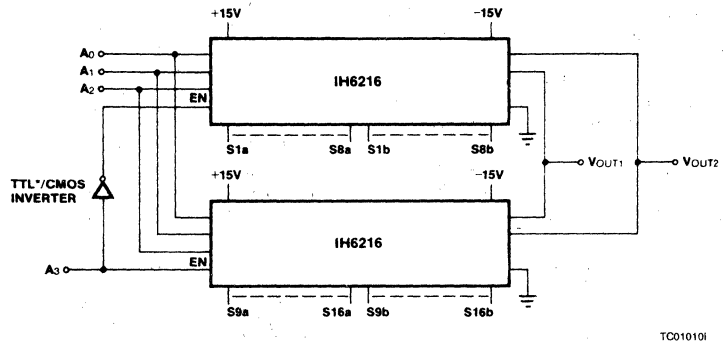


Figure 5: Switching Information

Note: All typical values have been guaranteed by characterization and are not tested.

IH6216 APPLICATIONS



*TTL gate must have pullup to drive EN input

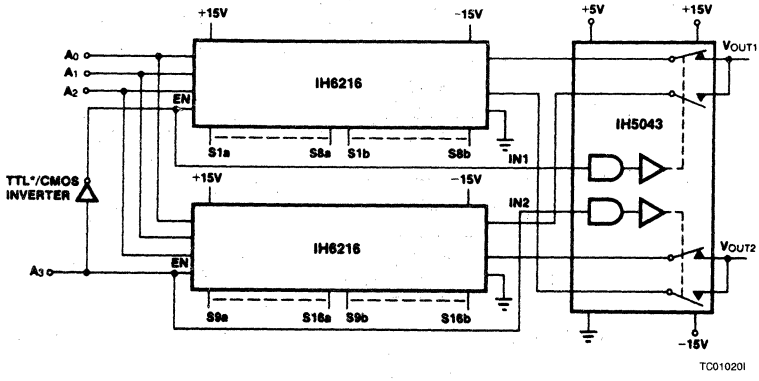
Figure 6: 2 Out of 32 Channel Multiplexer Using 2 IH6216s

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	ON SWITCH	
0	0	0	0	S1a	
0	0	0	1	S2a	
0	0	1	0	S3a	
0	0	1	1	S4a	
0	1	0	0	S5a	
0	1	0	1	S6a	
0	1	1	0	S7a	
0	1	1	1	S8a	V_{OUT1}
1	0	0	0	S9a	
1	0	0	1	S10a	
1	0	1	0	S11a	
1	0	1	1	S12a	
1	1	0	0	S13a	
1	1	0	1	S14a	
1	1	1	0	S15a	
1	1	1	1	S16a	

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	ON SWITCH	
0	0	0	0	S1b	
0	0	0	1	S2b	
0	0	1	0	S3b	
0	0	1	1	S4b	
0	1	0	0	S5b	
0	1	0	1	S6b	
0	1	1	0	S7b	
0	1	1	1	S8b	V_{OUT2}
1	0	0	0	S9b	
1	0	0	1	S10b	
1	0	1	0	S11b	
1	0	1	1	S12b	
1	1	0	0	S13b	
1	1	0	1	S14b	
1	1	1	0	S15b	
1	1	1	1	S16b	



*TTL inverter must have resistor pullup to drive EN input

Figure 7: 2 One of 32 Multiplexer Using Two IH6216s, and An IH5043 for Submultiplexing

Note: All typical values have been guaranteed by characterization and are not tested.

General note on expandability of IH6216

The IH6216 is a two tier multiplexer, where 8 pairs of input channels are routed to a pair of outputs in blocks of 4. Each block of 4 input channels is routed to one common output channel, and thus the submultiplexed system looks like 4 blocks of 4 inputs routed to 4 different outputs with the 4 outputs tied in pairs. Thus 20 switches are needed to handle the 16 channels of information. The advantages of this are lower output capacity and leakage than would be possible using a system with all 8 channels tied to one common output. Also the expandability into 2 out of 32, 64, 128, etc. is facilitated. Figures 6, 7, and 8 show how the IH6216 is expanded.

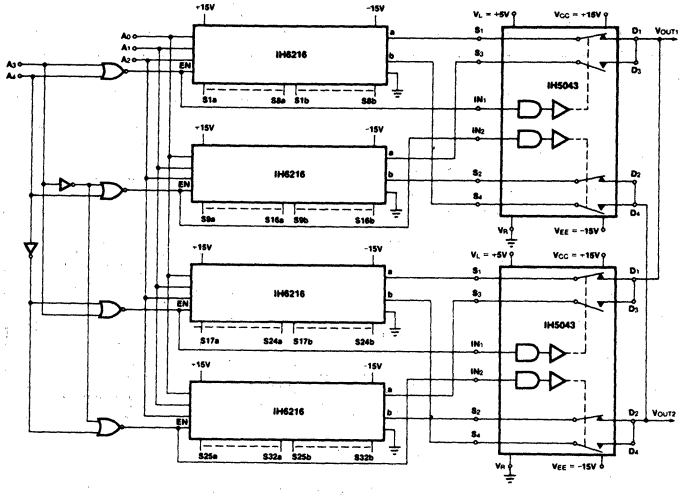
Figure 6 shows a 2 of 32 multiplexer, using 2 IH6216s. Since the 6216 is itself a 2 tier MUX, the system as shown is basically a 2 tier system. Corresponding output points of each of the 6216 are connected together, and the ENable input strobe is used as the A_3 input. Since each output (pins 2 and 28) corresponds to an "ON" FET and an "OFF" FET, the overall system looks like 1 "ON" FET and 3 "OFF" FETs for each of the V_{out1} and V_{out2} outputs. Thus the output leakage will be 1 $I_{D(on)}$ plus 3 $I_{D(off)}$s or about 0.4nA at room temperature. Throughput speed will be typically 0.8μs for t_{on} and 0.3μs for t_{off}, with throughput channel resistance in the 500Ω area.

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	ON SWITCH	
0	0	0	0	S1a	
0	0	0	1	S2a	
0	0	1	0	S3a	
0	0	1	1	S4a	
0	1	0	0	S5a	
0	1	0	1	S6a	
0	1	1	0	S7a	
0	1	1	1	S8a	V_{OUT1}
1	0	0	0	S9a	
1	0	0	1	S10a	
1	0	1	0	S11a	
1	0	1	1	S12a	
1	1	0	0	S13a	
1	1	0	1	S14a	
1	1	1	0	S15a	
1	1	1	1	S16a	

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	ON SWITCH	
0	0	0	0	S1b	
0	0	0	1	S2b	
0	0	1	0	S3b	
0	0	1	1	S4b	
0	1	0	0	S5b	
0	1	0	1	S6b	
0	1	1	0	S7b	
0	1	1	1	S8b	V_{OUT2}
1	0	0	0	S9b	
1	0	0	1	S10b	
1	0	1	0	S11b	
1	0	1	1	S12b	
1	1	0	0	S13b	
1	1	0	1	S14b	
1	1	1	0	S15b	
1	1	1	1	S16b	



TC01030I

Figure 8: 2 One of 64 Multiplexer Using 4 IH6216s and 2 IH5043s as Submultiplexers

Note: All typical values have been guaranteed by characterization and are not tested.

Figure 7 shows the 2 of 32 MUX of Figure 6, with a third tier of submultiplexing added to further reduce leakage and output capacity. The IH5043 has typical ON resistance of 50Ω (max. is 75Ω) so it only increases throughput channel resistance from the 500 ohms of Figure 6 to about 550 ohms for Figure 7. Throughput channel speed is a little slower by about 0.5μs for both ON and OFF time, and output leakage is about 0.2nA.

Figure 8 shows a 2 of 64 MUX using 3 tier MUXing (similar to Figure 7). The Intersil IH5043 is used for the third tier of MUXing. Each V_{out} point will see 3 OFF channels and 1 ON channel at anytime, so that the typical leakages will be about 0.4nA. Throughput channel resistance will be in the 550Ω area and throughput switching speeds about 1.3μs for ON time and 0.8μs for OFF time.

The IH5043 was chosen as the third tier of the MUX because it will switch the same AC signals as the IH6216 (typically plus and minus 15V) and uses break before make switching. Also power supply quiescent currents are typically 1-2μA so that no excessive system power is generated. Note that the logic of the 5043 is such that it can be tied directly to the ENable input (as shown in the figures) with no extra logic being required.

Enable input strobing levels

The ENable input acts as an enabling or disabling pin for the IH6216 when used as a 2 out of 16 channel MUX, however when expanding the MUX to more than 16 channels, the EN pin acts as another address input. Figures 6 and 7 show the EN pin used as the A_3 input.

For the system to function properly the EN input (pin 18) must go to 5V ±5% for the high state and less than 0.8V for the low state. When using TTL logic, a pull-up of 1kΩ or less resistor should be used to pull the output voltage up to 5V. When using CMOS logic, the high state goes to the power supply so no pull-up is required.

If used on high voltage logic supplies, EN should be at least 0.7V below V+ at all times. See IH6208 data sheet for details.

APPLICATION NOTES

Further information may be found in:

A003 "Understanding and Applying the Analog Switch," by Dave Fullagar

A006 "A New CMOS Analog Gate Technology," by Dave Fullagar

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Slieger

R009 "Reduce CMOS Multiplexer Troubles Through Proper Device Selection," by Dick Wilenken

NOTE: This multiplexer does not require external resistors and/or diodes to eliminate what is commonly known as a latch up or SCR action. Because of this fact, the $r_{DS(ON)}$ of the switch is maintained at specified values.

Note: All typical values have been guaranteed by characterization and are not tested.

MM450/451/452/455
MM550/551/552/555
High Voltage Analog Switch

INTERSIL

GENERAL DESCRIPTION

The MM450, and MM550 series each contain p channel MOS enhancement mode transistors. These devices are useful in airborne and ground support systems requiring multiplexing, analog transmission, and numerous signal routing applications. The use of low threshold transistors (V_{TH} = 2 volts) permits operations with large analog input swings (±10 volts) at low gate voltages (−20 volts).

Each gate input is protected from static charge build-up by the incorporation of zener diode protective devices connected between the gate input and device bulk.

FEATURES

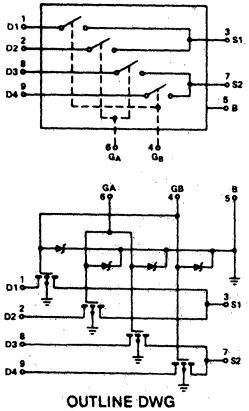
- **Large Analog Input — ±10V**
- **Low Supply Voltage — V_{BULK} = +10V**
  V_{GG} = −20V
- **Typical ON Resistance — V_{IN} = −10V, 150Ω**
  V_{IN} = +10V, 75Ω
- **Low Leakage Current — 200pA @ 25°C**
- **Input Gate Protection**

ORDERING INFORMATION

MM 4 90 F

- F — Package: F — 14 Pin Flatpak; J — 16 Pin CERDIP; H — 10 Pin Metal Can
- 90 — Device Type
- 4 — Temperature Range: 4 — (−55°C to +125°C); 5 — (0°C to 70°C)
- MM — Analog Switch

MM450, MM550 Dual Differential Switch

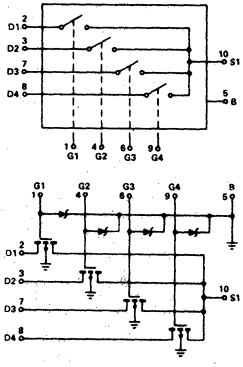


OUTLINE DWG TO-100

DS02130I

OUTLINE DWG TO-100

MM451, MM551 Four Channel 4PST Mux

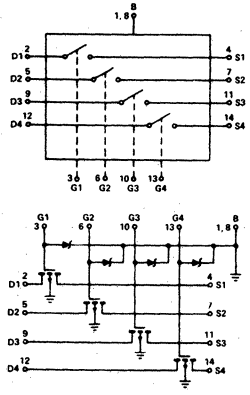


OUTLINE DWG TO-100

DS02140I

OUTLINE DWG TO-100

MM452, MM552 QUAD SPST MOS

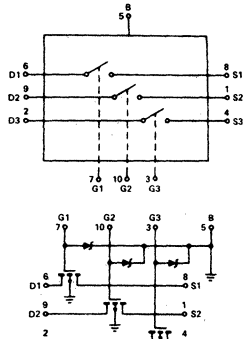


OUTLINE DWGS JE,FD-2

DS02150I

OUTLINE DWGS JE, FD-2

MM455, MM555 Three SPST MOS Transistor Package



OUTLINE DWG TO-100

DS02160I

OUTLINE DWG TO-100

Figure 1: Functional Diagram

Note: All typical values have been guaranteed by characterization and are not tested.

MM450/451/452/455
MM550/551/552/555

INTERSIL

ABSOLUTE MAXIMUM RATINGS (Note 1)

Gate Voltage (V_{GG}) ..... +14.5V to −30V
Bulk Voltage (V_{BULK}) ..... +14V
Analog Input (V_{IN}) ..... +14V to −20V
Power Dissipation 200mW

Operating Temperature
MM450, MM451, MM452, MM455 .. −55°C to +125°C
MM550, MM551, MM552, MM555 ..... 0°C to 70°C
Storage Temperature. ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE 1: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C. For higher temperature, derate at rate of 10mW/°C for FD package and 6.5 mW/°C for TW package.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

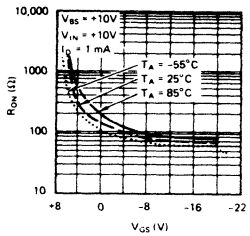
ELECTRICAL CHARACTERISTICS (per channel unless noted)

SYMBOL	CHARACTERISTIC	TYPE	TEST CONDITIONS	LIMITS 25°C	70°C	125°C	MIN / MAX	UNIT
V_{IN}	Analog Input Voltage	All		±10			Max	V
$V_{GS(Th)}$	Threshold Voltage	All	V_{DG} = 0, I_D = 10μA	1.0			Min	V
				3.0			Max	
$R_{DS(ON)}$	Drain-Source On Resistance	All	V_{IN} = −10V; I_D = 10mA, V_B = 10V	600		700	Max	Ω
			V_{IN} = +10V; V_{GS} = −20V	200		250	Max	Ω
I_{GBS}	Gate Leakage Current	All	V_{GS} = −25V, V_{BS} = V_{DS} = 0	±5		100	Max	nA
$I_{D(OFF)}$	Drain Leakage Current	MM450, MM451, MM452, MM455	V_{DB} = −25V, V_{GB} = V_{SB} = 0	±0.5		200	Max	nA
		MM550, MM551, MM552, MM555		20	100		Max	nA
$I_{S(OFF)}$	Source Leakage Current	MM450, MM451, MM452, MM455	V_{SB} = −25V, V_{DB} = V_{GB} = 0	±0.5		400	Max	nA
		MM550, MM551, MM552, MM555			100		Max	nA
C_{DB}	Drain-Body Capacitance	All	V_{DB} = V_{GB} = V_{SB} = 0, f = 1MHz (Note 1)	10			Typ	pF
C_{SB}	Source-Body Capacitance	MM450, MM550		14			Typ	pF
		MM451, MM551		24			Typ	pF
		MM452, MM552		11			Typ	pF
		MM455, MM555		11			Typ	pF
C_{GB}	Gate-Body Capacitance	MM450, MM550		13			Typ	pF
		MM451, MM551		8			Typ	pF
		MM452, MM552		9			Typ	pF
		MM455, MM555		9			Typ	pF
C_{GS}	Gate-Source Capacitance	All		5			Typ	pF

NOTE 1: Typical characteristics not tested in production

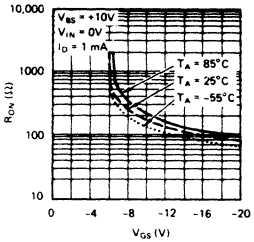
TYPICAL PERFORMANCE CHARACTERISTICS

$R_{DS(on)}$ vs V_{GS}



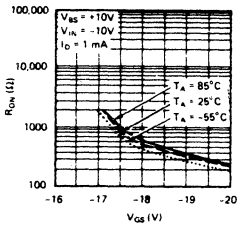
OP03680I

$R_{DS(on)}$ vs V_{GS}



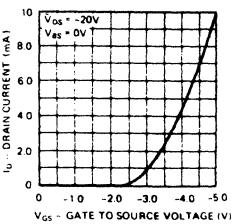
OP03690I

$R_{DS(on)}$ vs V_{GS}



OP03700I

DRAIN CURRENT vs GATE TO SOURCE VOLTAGE



OP03710I

Note: All typical values have been guaranteed by characterization and are not tested.

Section 4 — Amplifiers — Operational and Special Purpose

ICH8500/A
Ultra Low Input-Bias Operational Amplifier

GENERAL DESCRIPTION

The ICM8500 and ICH8500A are hybrid circuits designed for ultra low input bias current operational amplifier applications. They are ideally suited for analog and electrometer applications where high input resistance and low input current are of prime importance.

Functionally, they are pin for pin identical to the popular 741 monolithic amplifier. These amplifiers are unconditionally stable and the input offset voltage can be adjusted to zero with an external 20kΩ potentiometer. The input bias current for the inverting and noninverting inputs is 0.1pA maximum for the ICH8500, and 0.01pA maximum for the ICH8500A and are constant over the operating temperature range of −25°C to +85°C.

Pin 8 is connected to the case. This permits the designer to operate the case at any desired potential. This is the key to achieving the ultra low input currents associated with these two amplifiers. Forcing the case to the same potential as the inputs eliminates current flow between the case and the input pins, and leakage currents that may have otherwise existed between any of the other pins and the inputs are intercepted by the case.

FEATURES

- **Input Diode Protection**
- **Input Bias Current Less Than 0.01pA (8500A) at All Operating Temperatures**
- **No Frequency Compensation Required**
- **Offset Voltage Null Capability**
- **Short Circuit Protection**
- **Low Power Consumption**

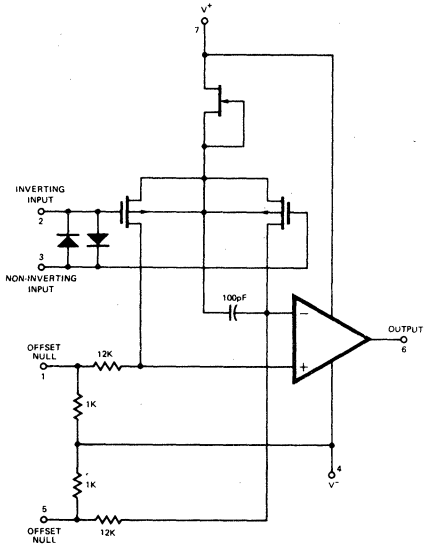
APPLICATIONS

- **Femto Ammeter**
- **Electrometers**
- **Long Time Integrators**
- **Flame Detectors**
- **pH Meters**
- **Proximity Detector**
- **Sample and Hold Circuits**

ORDERING INFORMATION

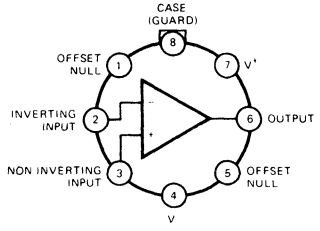
ICH 8500A TV

- TV — PACKAGE
  - TV = TO-99 Metal Can
- 8500A — DEVICE TYPE
- ICH — INTERSIL HYBRID CIRCUIT



DS01990I

Figure 1: Functional Diagram



CD01880I

Figure 2: Pin Configuration (Outline dwg TV)

Note: All typical values have been guaranteed by characterization and are not tested.

ICH8500/A

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Internal Power Dissipation (1) 500mW
Differential Voltage ..... ±0.5V
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −25°C to +85°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Output Short Circuit Duration ..... Indefinite

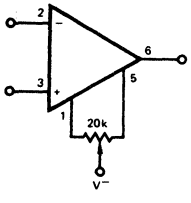
Note: 1. Rating applies for ambient temperature to +70°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified, V_{SUPPLY} = ±15V)

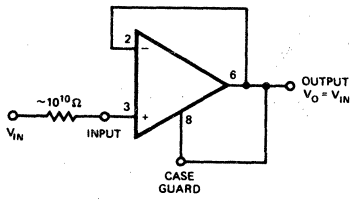
SYMBOL	CHARACTERISTICS	TEST CONDITIONS	ICH8500			ICH8500A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{BIAS}	Input Bias Current (Inverting and Non-Inverting)	Case at same potential as inputs			±0.1			±0.01	pA
V_{OS}	Input Offset Voltage				±75			±50	mV
	Offset Voltage Adjustment Range	20kΩ Potentiometer		±50			±50		mV
$\Delta V_{OS}/\Delta T$	Change in Input Offset Voltage Over Temperature	+25 to +85°C −25 to +25°C		±200			±100		mV
$\Delta V_{OS}/\Delta t$	Long Term Input Offset Voltage Stability	At 25°C		±3.0			±3.0		mV
CMRR	Common Mode Rejection Ratio	±5 volts common mode voltage		75			75		dB
ΔV_O	Output Voltage Swing	$R_L \geq 10k\Omega$	±11			±11			V
CMVR	Common Mode Voltage Range		±10			±10			V
A_{VOL}	Large Signal Voltage Gain		20,000	10^5		20,000	10^5		—
C_{fb}	Feedback Capacitance	Case guarded		0.1			0.1		pF
SR	Slew Rate	$R_L \geq 2k\Omega$		0.5			0.5		V/μs
C_{IN}	Input Capacitance	Case guarded		0.7			0.7		pF
C_{IN}	Input Capacitance	Case grounded		1.5			1.5		pF

VOLTAGE OFFSET NULL CIRCUIT



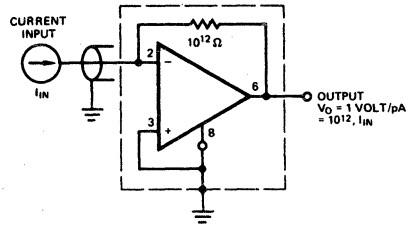
TC02610I

VOLTAGE FOLLOWER



LC01470I

LOW LEVEL CURRENT MEASURING CIRCUIT



LC01480I

NOTE: Adjust input offset voltage to 0V±10μV before measuring leakage.

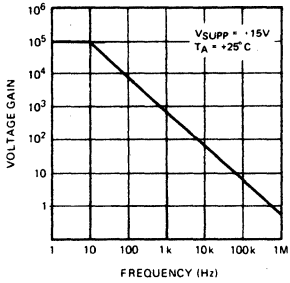
Figure 3: Circuit Notes

Note: All typical values have been guaranteed by characterization and are not tested.

ICH8500/A

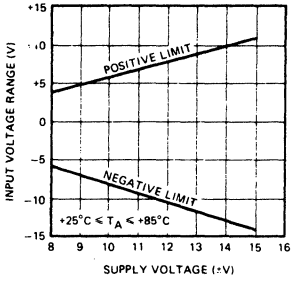
TYPICAL PERFORMANCE CHARACTERISTICS

OPEN LOOP VOLTAGE GAIN vs. FREQUENCY



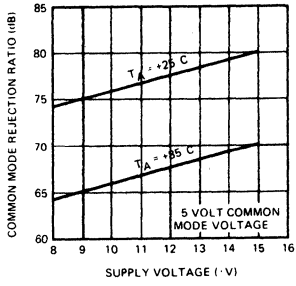
OP03490I

INPUT VOLTAGE RANGE vs. SUPPLY VOLTAGE



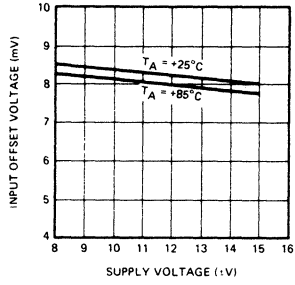
OP03500I

COMMON MODE REJECTION RATIO vs. SUPPLY VOLTAGE



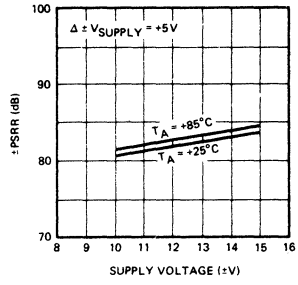
OP03510I

INPUT OFFSET VOLTAGE vs. SUPPLY VOLTAGE



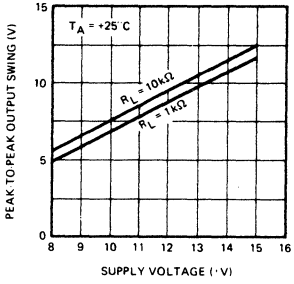
OP03520I

±POWER SUPPLY REJECTION RATIO vs. SUPPLY VOLTAGE



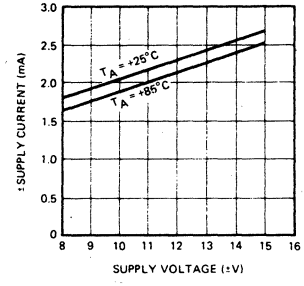
OP03530I

OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE



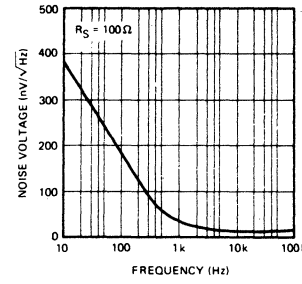
OP03540I

±QUIESCENT SUPPLY CURRENT vs. SUPPLY VOLTAGE



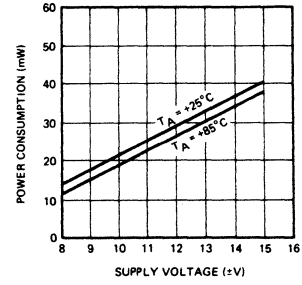
OP03550I

INPUT REFERRED NOISE VOLTAGE



OP03560I

POWER CONSUMPTION vs. SUPPLY VOLTAGE



OP03570I

Note: All typical values have been guaranteed by characterization and are not tested.

ICH8500/A

APPLICATIONS

The Pico Ammeter

A very sensitive pico ammeter can be constructed with the ICH8500. The basic circuit (illustrated in Figure 4) employs the amplifier in the inverting or current summing mode.

Care must be taken to eliminate any stray currents from flowing into the current summing node. This can be accomplished by forcing all points surrounding the input to the same potential as the input. In this case the potential of the input is at virtual ground, or 0V. Therefore, the case of the device is grounded to intercept any stray leakage currents that may otherwise exist between the ±15V input terminals and the inverting input summing junctions. Feedback capacitance* should be kept to a minimum in order to maximize the response time of the circuit to step function input currents. The time constant of the circuit is approximately the product of the feedback capacitance C_{fb} times the feedback resistor R_{fb}. For instance, the time constant of the circuit in Figure 4 is 1 sec if C_{fb} = 1pF. Thus, it takes approximately 5 sec (5 time constants) for the circuit to stabilize to within 1% of its final output voltage after a step function of input current has been applied. C_{fb} of less than 0.2 to 0.3pF can be achieved with proper circuit layout. A practical pico ammeter circuit is illustrated in Figure 5.

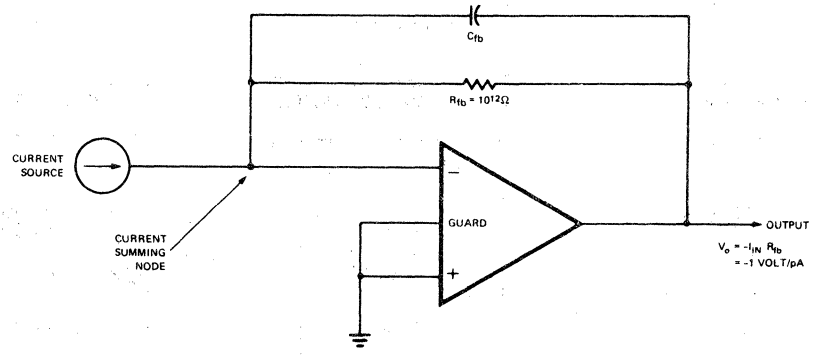


Figure 4: Basic Pico Ammeter Circuit

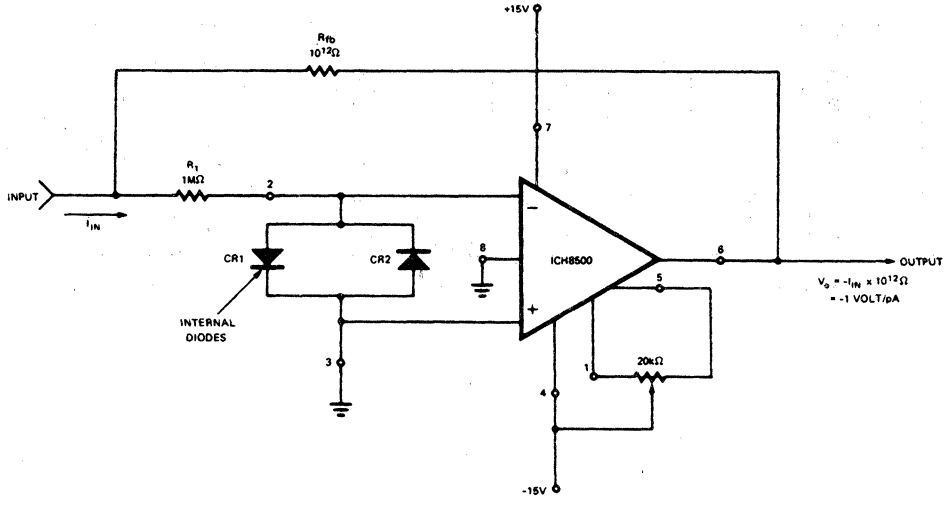


Figure 5: Pico Ammeter Circuit

Note: All typical values have been guaranteed by characterization and are not tested.

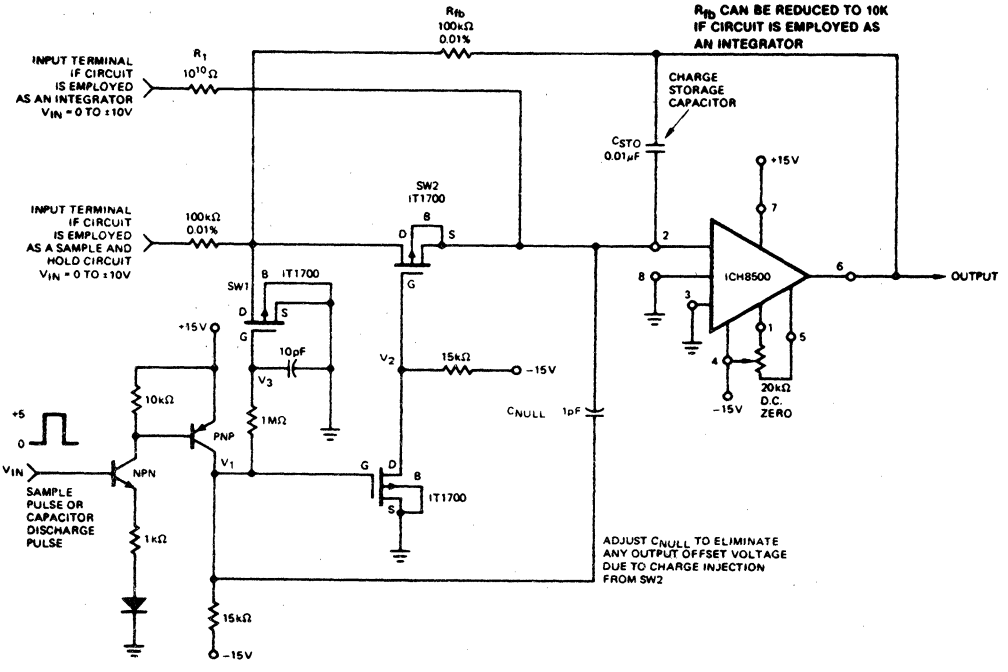


Figure 6: Sample and Hold Circuit or Integrator Circuit

The internal diodes CR1 and CR2 together with external resistor R1 protect the input stage of the amplifier from voltage transients. The two diodes contribute no error currents, since under normal operating conditions there is no voltage across them.

Feedback capacitance is the capacitance between the output and the inverting input terminal of the amplifier.

Sample and Hold Circuit

The basic principle of this circuit (Figure 6) is to rapidly charge a capacitor C_{STO} to a voltage equal to an input signal. The input signal is then electrically disconnected from the capacitor with the charge still remaining on C_{STO}. Since C_{STO} is in the negative feedback loop of the operational amplifier, the output voltage of the amplifier is equal to the voltage across the capacitor. Ideally, the voltage across C_{STO} should remain constant, causing the output of the amplifier to remain constant as well. However, the voltage across C_{STO} will decay at a rate proportional to the current being injected or taken out of the current summing node of the amplifier. This current can come from four sources: leakage resistance of C_{STO}, leakage current due to the solid state switch SW2, currents due to high resistance paths on the circuit fixture, and most important, bias current of the operational amplifier. If the ICH8500A operational amplifier is employed, this bias current is almost non-existant (< 0.01pA). Note that the voltages on the source, drain and gate of switch SW2 are zero or near zero when the circuit is in the hold mode. Careful construction will eliminate stray resistance paths and capacitor resistance can be eliminated if a quality capacitor is selected. The net result is a low drift sample and hold circuit.

As an example, suppose the leakage current due to all sources flowing into the current summing node of the sample and hold circuit is 100pA. The rate of change of the voltage across the 0.01μF storage capacitor is then 10mV/sec. In contrast, if an operational amplifier which exhibited an input bias current of 1nA were employed, the rate of change of the voltage across C_{STO} would be 0.1V/sec. An error build up such as this could not be tolerated in most applications.

Wave forms illustrating the operation of the sample and hold circuit are shown in Figure 7.

The Gated Integrator

The circuit in Figure 6 can double as an integrator. In this application the input voltage is applied to the integrator input terminal. The time constant of the circuit is the product of R1 and C_{STO}. Because of the low leakage current associated with the ICH8500 and ICH8500A, very large values of R1 (Up to 10^{12} ohms) can be employed. This permits the use of small values of integrating capacitor (C_{STO}) in applications that require long time delays. Waveforms for the integrator circuit are illustrated in Figure 8.

Note: All typical values have been guaranteed by characterization and are not tested.

ICH8500/A

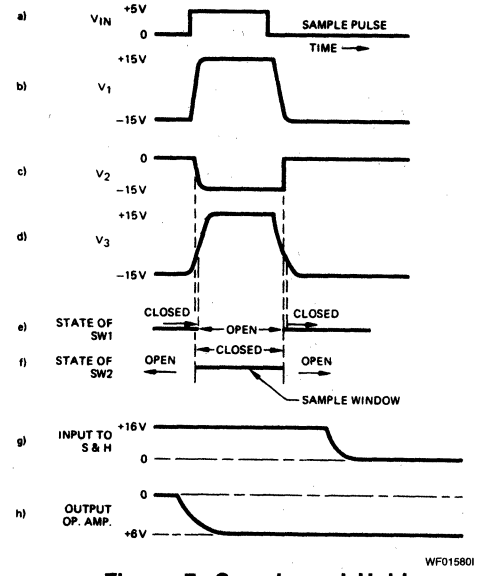


Figure 7: Sample and Hold Circuit Waveforms

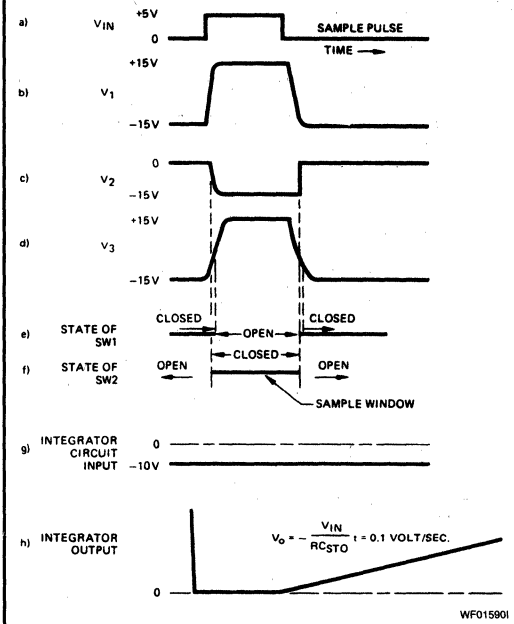


Figure 8: Gated Integrator Waveforms

Note: All typical values have been guaranteed by characterization and are not tested.

ICH8510/8520/8530
Power Operational Amplifier

GENERAL DESCRIPTION

The ICH8510/8520/8530 is a family of hybrid power amplifiers that have been specifically designed to drive linear and rotary actuators, electronic valves, push-pull solenoids, and DC & AC motors.

There are three models available for up to +30V power supply operation: 2.7 amps @ 24 volt output levels, 2 amps @ 24V and 1 amp @ 24V. All amplifiers are protected against shorts to ground by the addition of 2 external protection resistors. For a device operating at lower voltages, see the ICH8515 data sheet.

The design uses a conventional 741 operational amplifier, a special monolithic driver chip (BL8063), NPN & PNP power transistors, and internal frequency compensating capacitors. The chips are mounted on a beryllium oxide substrate for optimum heat transfer to the metal package. This substrate also provides electrical isolation between amplifiers and metal package.

The I.C. power driver chip has built-in regulators that provide the 741 with typically a ±13V supply.

FEATURES

- **Delivers Up to 2.7 Amps @ 24-28V DC (30V Supplies)**
- **Protected Against Inductive Kick Back With Internal Power Limiting**
- **Programmable Current Limiting (Short Circuit Protection)**
- **Package is Electrically Isolated (Allowing Easy Heat Sinking)**
- **Open Loop DC Gain > 100dB**
- **20mA Typical Standy Quiescent Current**
- **Popular 8 Pin TO-3 Package**
- **Internal Frequency Compensation**
- **Can Drive Up to 0.1 Horsepower Motors**

ORDERING INFORMATION

ICH85X0 M KA

- KA — Package: KA = 8 lead TO-3 can
- M — Temperature Range: M = Military −55°C to +125°C; I = Industrial −20°C to +85°C
- ICH85X0 — Basic Part Number: 8510 = 1A output; 8520 = 2A output; 8530 = 2.7A output

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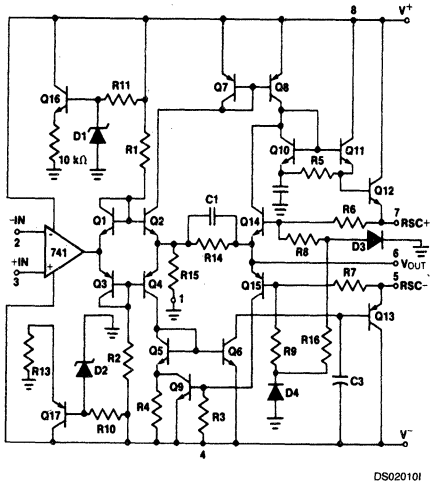

Figure 1: Functional Diagram

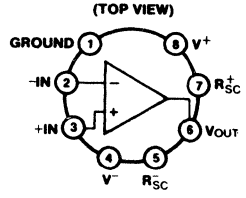

Figure 2: Pin Configuration

Note: All typical values have been guaranteed by characterization and are not tested.

ICH8510/8520/8530

INTERSIL

ABSOLUTE MAXIMUM RATINGS @ T_A = 25°C

Supply Voltage ..... ±32V
Power Dissipation, Safe Operating Area ..... See Curves
Differential Input Voltage ..... ±30V
Input Voltage ..... ±15V (Note 1)
Peak Output Current ..... See Curves (Note 2)
Output Short Circuit Duration
(to ground) ..... Continuous (Note 2)

Operating Temperature Range M ..... −55°C → +125°C
I ..... −20°C → +85°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Max Case Temperature ..... 150°C

Note 1: Rating applies to supply voltages of ±15V. For lower supply voltages, $V_{INMAX} = V_{SUPP}$.

Note 2: Ratings apply as long as package dissipation is not exceeded. Device must be mounted on heat sink, see Figures 12 and 16.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS T_A = +25°C. V_{SUPPLY} = ±30V (unless otherwise stated)

SYMBOL	DESCRIPTION	TEST CONDITIONS	ICH85101		ICH8510M		ICH85201		ICH8520M		ICH65301		ICH8530M		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$\Delta V_{OS}/\Delta Pd$	Input Offset Voltage Change with Power Dissipation	Mtd on Wakefield 403 Heat Sink		4 (Typ.)		2 (Typ.)		4 (Typ.)		2 (Typ.)		4 (Typ.)		2 (Typ.)	mV/W
V_{OS}	Input Offset Voltage	R_S < 10kΩ Pd < 1W	−6	+6	−3	+3	−6	+6	−3	+3	−6	+6	−3	+3	mV
I_{BIAS}	Input Bias Current	R_S < 10kΩ P_d < 1W		500		250		500		250		500		250	nA
I_{OS}	Input Offset Current	R_S < 10kΩ P_d < 1W		200		100		200		100		200		100	nA
A_{VOL}	Large Signal Voltage Gain	R_L = 20Ω V_O > 2/3 V_{SUPP}	100 (Typ.)		100 (Typ.)		100 (Typ.)		100 (Typ.)		100 (Typ.)		100 (Typ.)		dB
V_{CMR}	Input Voltage Range	Typical	−10	+10	−10	+10	−10	+10	−10	+10	−10	+10	−10	+10	V
CMRR	Common Mode Rejction Ratio	R_S = 10kΩ	70 (Typ.)		70 (Typ.)		70 (Typ.)		70 (Typ.)		70 (Typ.)		70 (Typ.)		dB
PSRR	Power Supply Rejection Ratio	R_S = 10kΩ	77 (Typ.)		77 (Typ.)		77 (Typ.)		77 (Typ.)		77 (Typ.)		77 (Typ.)		dB
SR	Slew Rate	C_L = 3 pF, A_V = 1 R_L = 10Ω V_O = 2/3 V_{SUPP}	0.5 (Typ.)		0.5 (Typ.)		0.5 (Typ.)		0.5 (Typ.)		0.5 (Typ.)		0.5 (Typ.)		V/μs
V_{OMAX}	Output Voltage Swing	R_L = 20Ω A_V = 10	(R_L = 30Ω) ±26V		(R_L = 30Ω ±26V		±26V		±26V		±25V		±25V		V
I_{MAX}	Output Current (3)	R_L = 8Ω A_V = 10	1.0		1.0		2.0		2.0		2.7		2.7		A
I_Q	Power Supply Quiescent Current	R_L = ∞ V_{IN} = 0V		125		100		125		100		125		100	mA

NOTE 2: See Figure 7 if Power Suplies are less than ±30V .

ELECTRICAL SPECIFICATIONS T_A = −55°C. to +125°C.(M) or T_A = −20°C. to +85°C (I).

SYMBOL	DESCRIPTION	TEST CONDITIONS	ICH85101		ICH8510M		ICH85201		ICH8520M		ICH65301		ICH8530M		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{0s}	Input Offset Voltage	Pd < 1W	−10	+10	−9	+9	−10	+10	−9	+9	−10	+10	−9	+9	MV
I_{BIAS}	Input Bias Current	Pd < 1W		1500		750		1500		750		1500		750	nA
I_{OS}	Input Offset Current			500		200		500		200		500		200	nA
A_{VOL}	Large Signal Voltage Gain	R_L = 20Ω ΔV_O = 2/3 V_{SUPP}	90 (Typ.)		90 (Typ.)		90 (Typ.)		90 (Typ.)		90 (Typ.)		90 (Typ.)		dB
V_{OMAX}	Output Voltage Swing	R_L = 20Ω, A_V = 10	±24		±24		±24		±24		±24		±24		V
$R_{\theta JA}$	Thermal Resistance Junction to Ambient	Without Heat Sink		40 (Typ.)		40		40		40		40		40	°C/W
$R_{\theta JC}$	Thermal Resistance Junction to Case			2.5 (Typ.)		2.5 (Typ.)		2.5 (Typ.)		2.5 (Typ.)		2.5 (Typ.)		2.5 (Typ.)	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient	Mtd. on Wakefield 403 Heat Sink		(Typ.) 4.0		(Typ.) 4.0		(Typ.) 4.0		(Typ.) 4.0		(Typ.) 4.0		(Typ.) 4.0	°C/W
V_{SUPP}	Supply Voltage Range		±20	±30	±20	±30	±20	±30	±20	±30	±20	±30	±20	±30	V

Note: All typical values have been guaranteed by characterization and are not tested.

How To Set The Externally Programmable, Current Limiting Resistors:

The maximum output current is set by the addition of two external resistors, $R_{SC(+)}$ and $R_{SC(-)}$. Due to the current limiting circuitry, maximum output current is available only when V_O is close to either power supply. As V_O moves away from V_{SUPPLY}, the maximum output current decreases in proportion to output voltage. The curve on the next page shows maximum output current versus output voltage.

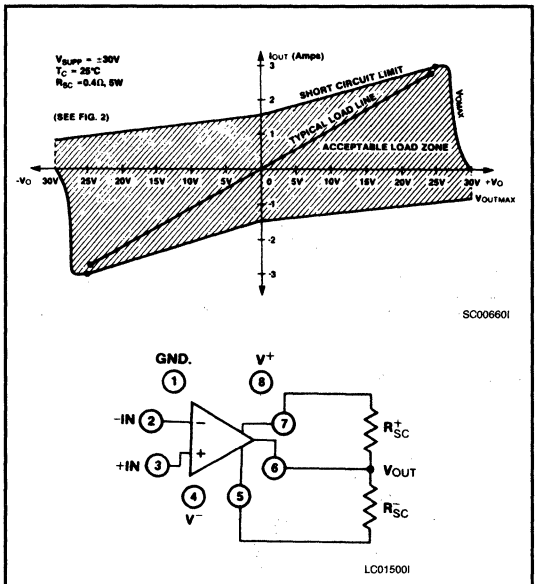

Figure 3: Maximum Output Current for Given R_{SC}

In general, for a given V_O, I_{SC} limit, and case temperature T_C, R_{SC} can be calculated from the equation below for V_O positive, I_{OUT} positive.

$$R_{SC} = \frac{(20.6V_O)^* + 680 - 2.2(T_C - 25°C)}{I_{SC(LIMIT)}}$$

*For V_O negative, replace this term with $10.3\ (V_O - 1.2)$

For example, for $I_O = 1.5A$ @ $V_O = 25V$ and $T_C = 25°C$,

$$R_{SC} = \frac{1195}{1500} = 0.797$$

Therefore for this application, $R_{SC} = 0.82\Omega$ (closest standard value)

When 0.82Ω is used, I_{SC} @ $V_O = 0V$ will be reduced to about 1A. Except for small changes in the "$\pm V_{O(max)}$ Limit" area, the effects of changing R_{SC} on the I_{OUT} vs V_{OUT} characteristics can be determined by merely changing the I_{OUT} scale on Figure 3 to correspond to the new value. Changes in T_C move the limit curve bodily up and down.

This internal current limiting circuitry however does not at all restrict the normal use of the driver. For any normal load, the static load line will be similar to that shown in Figure 3.

Clearly, as V_O decreases, the I_O requirement falls also, more steeply than the I_O available. For reactive loads, the dynamic load lines are more complex. Two typical operating point loci are sketched here:

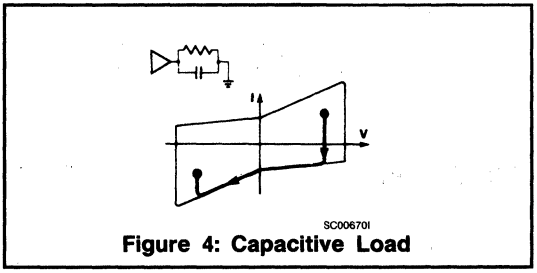

Figure 4: Capacitive Load

Thus the limiting circuitry protects the load and avoids needless damage to the driver during abnormal conditions. For any 24-28VDC motor/actuator, the R_{SC} resistors must be calculated to get proper power delivered to the motor (up to a maximum of 2.7A) and V_{SUPP} set at ±30V. For lower supply and/or output voltages, the maximum output current will follow graphs.

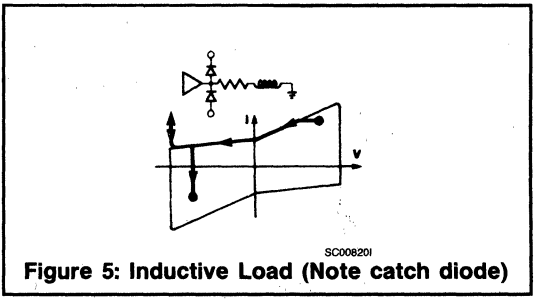

Figure 5: Inductive Load (Note catch diode)

NOTE ON AMPLIFIER POWER DISSIPATION

The steady state power dissipation limit is given by

$$P_D = \frac{T_{J(MAX)} - T_A}{R_{\theta JC} + R_{\theta CH} + R_{\theta HA}}$$

where:

T_J = Maximum junction temperature

T_A = Ambient temperature

$R_{\theta JC}$ = Thermal resistance from transistor junction to case of package

$R_{\theta CH}$ = Thermal resistance from case to heat sink

$R_{\theta HA}$ = Thermal resistance from heat sink to ambient air

And since

T_J = 200°C for silicon transistors

$R_{\theta JC} \cong$ 2.0°C/W for a steel bottom TO-3 package with die attachment to beryllia substrate header

$R_{\theta CH}$ = .045°C/W for 1 mil thickness of Wakefield type 120 thermal joint compound
.09°C/W for 2 mil thickness of type 120
.13°C/W for 3 mil thickness of type 120
.17°C/W for 4 mil thickness for type 120
.21°C/W for 5 mil thickness of type 120
.24°C/W for 6 mil thickness of type 120

Note: All typical values have been guaranteed by characterization and are not tested.

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$R_{\theta HA}$ = The choice of heat sink that a user selects depends upon the amount of room available to mount the heat sink. A sample calculation follows: by choosing a Wakefield 403 heat sink, with free air, natural convection (no fan). $R_{\theta HA} \cong 2.0°C/W$. Using 4 mil joint compound,

$$P_D = \frac{200°C - T_A}{(2.0 + 0.17 + 2.0)°C/W} = \frac{200°C - T_A}{4.17°C/W}$$

or @ $T_A = 25°C$,

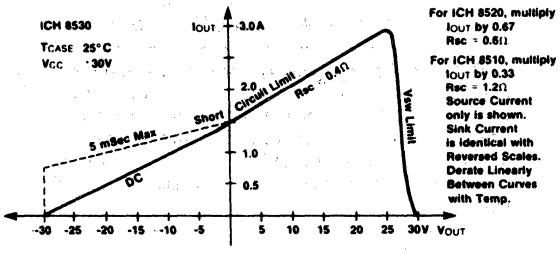
$$\frac{200°C - 25°C}{4.17°C/W} = 42W$$

and @ $T_A = 125°C$,

$$\frac{200°C - 125°C}{4.17°C/W} = 18W$$

From Figure 6 the worst case steady state power dissipation for an IH8520 ($R_{SC} = 0.62\Omega$) is about 30W and 18W respectively. Thus this heat sink is adequate.

TYPICAL PERFORMANCE CHARACTERISTICS



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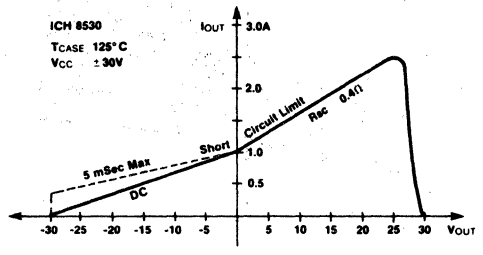

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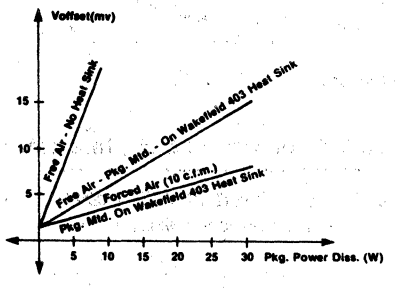
Safe Operating Area; I_{OUT} vs V_{OUT} vs T_C



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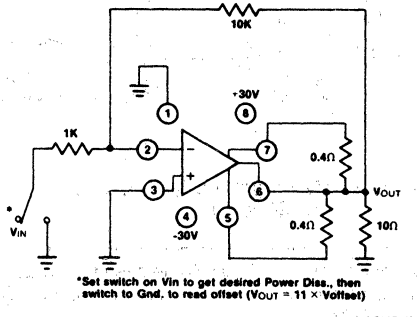

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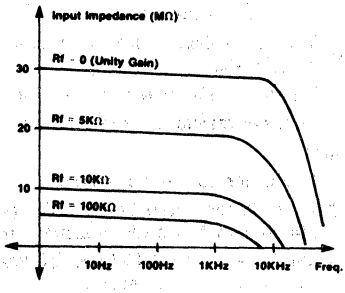
Input Offset Voltage vs Power Dissipation



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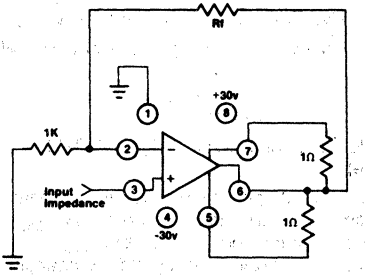

LC01520I

Input Impedance vs Gain vs Frequency

Note: All typical values have been guaranteed by characterization and are not tested.

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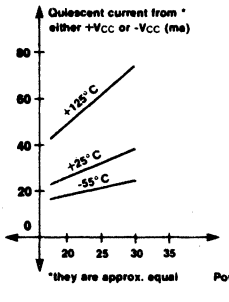
TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)



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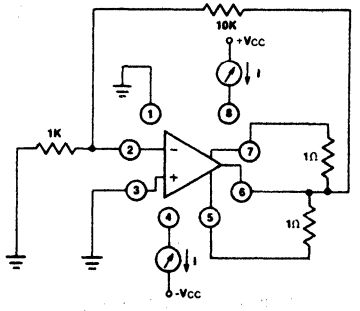

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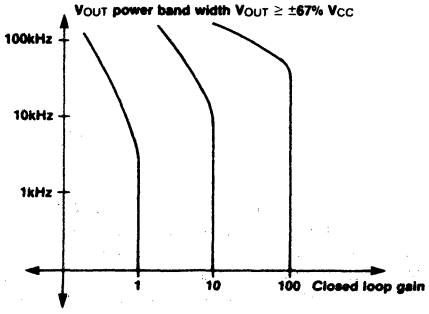
Quiescent Current vs Power Supply Voltage



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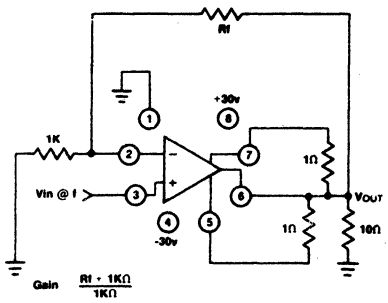

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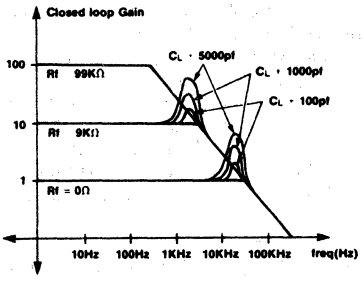
Large Signal Power Bandwidth



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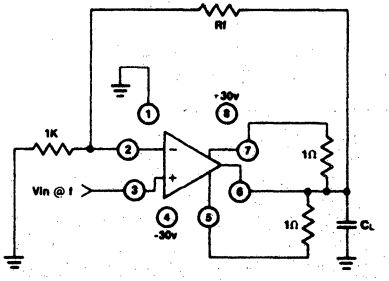

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Small Signal Frequency Response

Note: All typical values have been guaranteed by characterization and are not tested.

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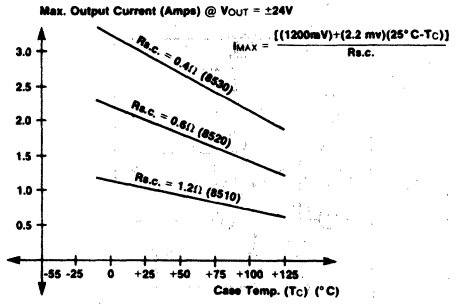

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Figure 6: Maximum Output Current vs. Case Temperature

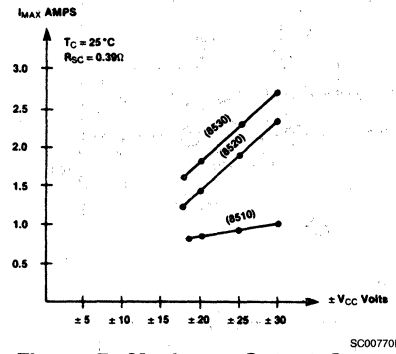

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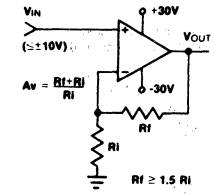
Figure 7: Maximum Output Current vs. V_{SUPPLY}

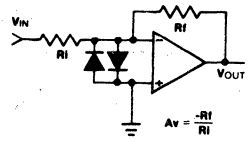
APPLICATION NOTES

The maximum input voltage range, for $V_{SUPPLY} < \pm 15V$, is substantially less than the available output voltage swing. Thus non-inverting amplifiers, as in Figure 8, should always be set up with a gain greater than about 2.5, (with ±30V supplies), so that the full output swing is available without hazard to the input. At first sight, it would seem that no restrictions would apply to inverting amplifiers, since the inputs are virtual ground and ground. However, under fault (output short-circuited) or high slew conditions, the input can be substantially removed from ground. Thus for inverting amplifiers with gains less than about 5, some protection should be provided at this input. A suitable resistor from the input to ground will provide protection, but also increases the effect of input offset voltage at the output. A pair of diodes, as shown in Figure 10, has no effect on normal operation, but gives excellent protection.



DS02020I

Figure 8: Non-Inverting Amplifier



DS02030I

Figure 9: Inverting Amplifier

Power dissipation is another important parameter to consider. The current protection circuit protects the device against short circuits to ground, (but only for transients to the opposite supply) provided the device has adequate heat sinking. A curve of power dissipation vs V_O under short circuit conditions is given in Figure 10. The limiting circuit is more closely dependent on case temperature than (output transistor) junction temperatures. Although these operating conditions are unlikely to be attained in actual use, they do represent the limiting case a heat sink must cope with. For a fully safe design, the anticipated range of V_O values that could occur, (steady state, including faults) should be examined for the highest power dissipation, and the device provided with a heat sink that will keep the junction temperature below 200°C and the case temperature below 150°C with the worst case ambient temperature expected.

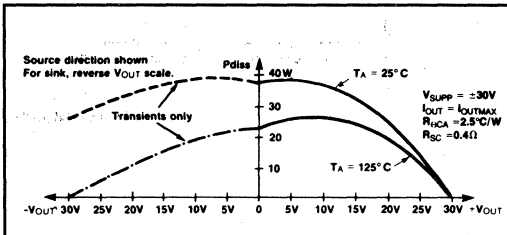


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Figure 10: Power Dissipation under Short Circuit Conditions

Note: All typical values have been guaranteed by characterization and are not tested.

TYPICAL APPLICATIONS

Actuator Driving Circuit (24→28 VDC rated)

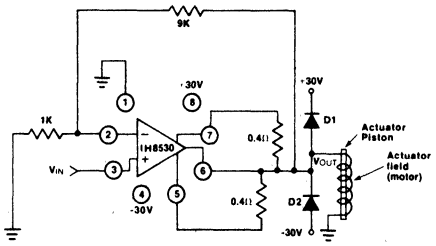


Figure 11: Power Amp Driving Actuator

The gain of the circuit is set to +10, so a V_{IN} = +2.4V will produce a +24V output (and deliver up to 2.7 amps output current). To reverse the piston travel, invert V_{IN} to −2.4V and V_{OUT} will go to −24V. Diodes D1 and D2 absorb the inductive kick of the motor during transients (turn-on or turn-off); their breakdown should exceed 60V.

Obtaining Up To 5 Amps Output Current Capability By Paralleling Amplifiers

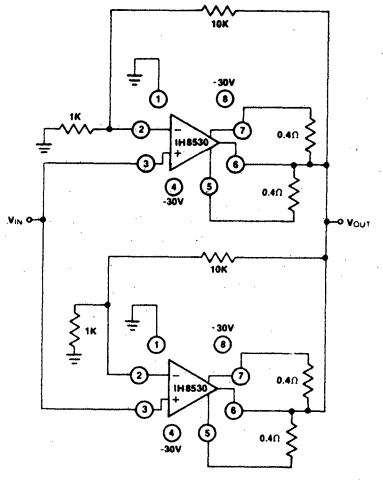


Figure 12: Paralleling Power Amps for Increased Current Capability

This paralleling procedure can be repeated to get any desired output current. However, care must be taken to provide sufficient load to avoid the amplifiers pulling against each other.

Driving A 48VDC Motor

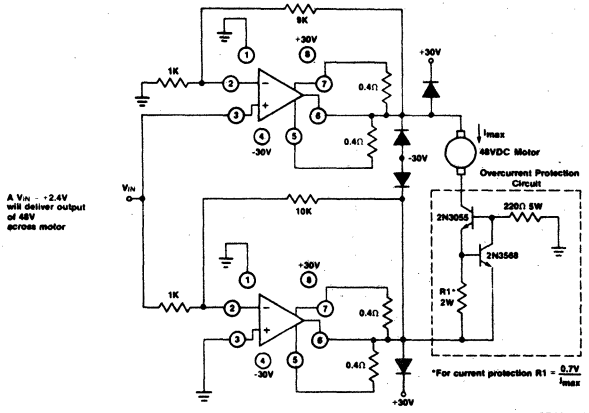


Figure 13: Power Amp Driving 48 VDC Motor

Note: All typical values have been guaranteed by characterization and are not tested.

Precise Rate Control of an Electronic Valve

There are two methods to get very fine control of the opening of an orifice driven by an electronic valve.

1. Keep the voltage constant, i.e., 24VDC or 12VDC, and vary the time the voltage is applied, i.e., if it takes five seconds to completely open an orifice at 24VDC, then applying 24V for only $2\frac{1}{2}$ seconds opens it only 50%.
2. Simply vary the DC driving voltage to valve. Most valves obtain full opening as an inverse of applied voltage, i.e., valves open 100% in five seconds at 24VDC and in 10 seconds at 12VDC.

A circuit to perform the second method is shown below; the advantage of this is that digit switches can precisely set driving voltage to 0.2% accuracy (8-bit DAC), thereby controlling the rate at which the valve opens.

The circuit presented in Figure 14 is also an excellent way to get a precise power supply voltage; in fact, it is possible to build a precision variable power supply using a BCD coded DAC with BCD Thumbwheel switches.

There is great power available in the sub-systems shown in Figures 14 & 15; there the D/A converter is shown being set manually (via digit switches) to get a precise analog output (binary # x full scale voltage), then the driver amplifier multiplies this voltage to produce the final output voltage. It seems obvious that the next logical step is to let a microprocessor control the D/A converter. Then total, pre-programmable, electronic control of an actuator, electronic valve, motor, etc., is obtained. This would be used in conjunction with a transducer/multiplex system for electronic monitoring and control of any electromechanical function.

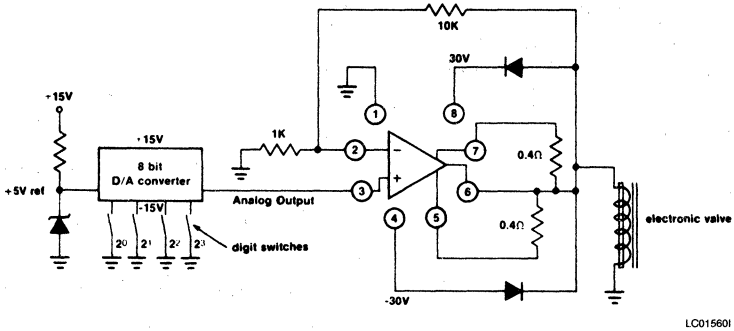
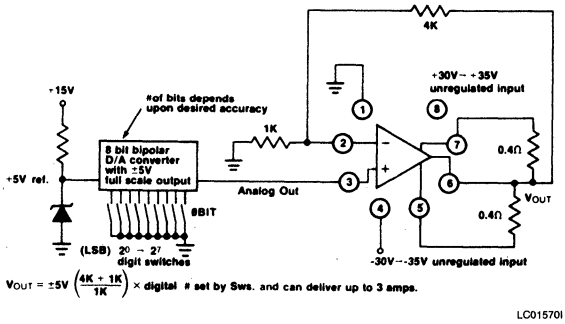


Figure 14: Digitally Controlled Electronic Value

Note: All typical values have been guaranteed by characterization and are not tested.



LC01570I

2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	0 BIT	V_{out}
1	1	1	1	1	1	1	1		+25VDC
1	1	1	1	1	1	1	1	0	−25VDC
0	1	0	1	1	0	0	1	1	+15VDC
0	1	0	1	1	0	0	1	0	−15VDC
1	0	0	0	0	0	0	0	1	+0.098VDC
1	0	0	0	0	0	0	0	0	−0.098VDC

The power supply can be set set to ±0.1VDC.

Figure 15: Digitally Programmable Power Supply

HEAT SINK INFORMATION

Heat sinks are available from Intersil. Order part number 29-0305 ($10.00 ea.) with a $R_{\theta HA}$ = 1.3°C/watt. A convenient mating connector is also available. Order part number 29-0306 ($4.50 ea.).

Note: This product contains Beryllia. If used in an application where the package integrity may be breached and the internal parts crushed or machined, avoid inhalation of the dust.

APPLICATION NOTES

For Further Applications Assistance, See:

A021 "Power D/A Converters Using The ICH8510/20/30," by Dick Wilenken
A026 "DC Servo Motor Systems Using The ICH8510/20/30," by Ken McAllister
A029 "Power Op Amp Heat Sink Kit," by Skip Osgood

Note: All typical values have been guaranteed by characterization and are not tested.

ICH8515
Power Operational Amplifier

GENERAL DESCRIPTION

The ICH8515 is a hybrid power amplifier specifically designed to drive linear and rotary actuators, electronic valves, push-pull solenoids, and DC & AC motors.

The design uses a conventional 741 operational amplifier, a special monolithic driver chip (BL8063), NPN & PNP power transistors, and an internal frequency compensating capacitor. The chips are mounted on a beryllium oxide substrate, for optimum heat transfer to the metal package. This substrate provides electrical isolation between the amplifier and the metal package.

The 8515 has special SOA (safe operating area) circuitry which allows it to withstand a direct short to ground or to either supply indefinitely. It has been designed to operate with ±12 or ±15VDC supplies and will deliver typically 1.5 to 1.8A @ +13V out using ±15V supplies.

Internal frequency compensation provides stability down to unity gain (either inverting or noninverting) even when using inductive loads.

FEATURES

- **Delivers Up to 1.5 Amps @ +12VDC (±15VDC Supplies)**
- **Protected Against Inductive Kick Back By Internal Power Limiting**
- **Programmable Current Limiting (Short Circuit Protection)**
- **Package Is Electrically Isolated (Allowing Easy Heat Sinking)**
- **Open Loop DC Gain > 100dB**
- **Popular 8 Pin TO-3 Package**
- **Internal Frequency Compensation**
- **Can Drive Up to 0.033 Horsepower Motors**
- **Pin Equivalent to ICH8510/20/30 Family**

ORDERING INFORMATION

PART NUMBER	OUTPUT CURRENT	TEMPERATURE	PACKAGE
ICH8515MKA	1.5A	−55°C to +125°C	8-Lead TO-3
ICH8515IKA	1.25A	−25°C to +85°C	8-Lead TO-3

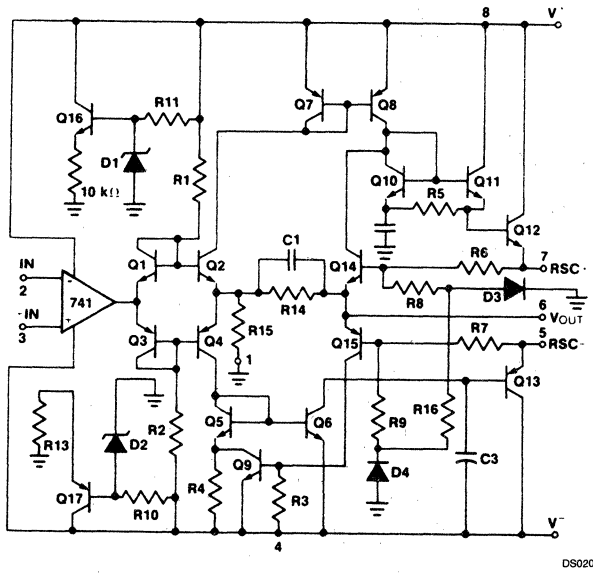


Figure 1: Functional Diagram

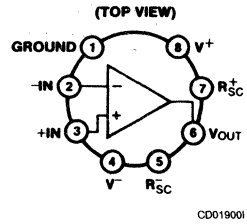


Figure 2: Pin Configuration (Outline dwg KA)

Note: All typical values have been guaranteed by characterization and are not tested.

ICH8515

ABSOLUTE MAXIMUM RATINGS @ $T_A = 25°C$

Supply Voltage ..... ±18V
Power Dissipation, Safe Operating Area ..... See Curves
Differential Input Voltage ..... ±30V
Input Voltage ..... ±15V (Note 1)
Peak Output Current ..... See Curves (Note 2)
Output Short Circuit Duration
(to ground) ..... Continuous (Note 2)

Operating Temperature Range M ..... −55°C to +125°C
I ..... −25°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Max Case Temperature ..... 150°C

Note 1: Rating applies to supply voltages of ±15V. For lower supply voltages, $V_{INMAX} = V_{SUPPLY}$.

Note 2: Rating applies as long as package dissipation is not exceeded for heat sink attached.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS
OPERATING CHARACTERISTICS $T_A = +25°C$. $V_{SUPPLY} = ±15V$ (unless otherwise stated)

SYMBOL	PARAMETER	TEST CONDITIONS	ICH8515I			ICH8515M			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$\Delta V_{OS}/\Delta Pd$	Input Offset Voltage Change with Power Dissipation	Mtd. on Wakefield 403 Heat Sink			4 (Typ.)			2 (Typ.)	mV/W
V_{OS}	Input Offset Voltage	$R_S \leq 10k\Omega$, Pd < 1W	−6	1	6	−3	0.7	3	mV
I_{BIAS}	Input Bias Current	$R_S \leq 10k\Omega$, Pd < 1W			500			250	nA
I_{OS}	Input Offset Current	$R_S \leq 10k\Omega$, Pd < 1W			200			100	nA
A_{VOL}	Large Signal Voltage Gain	$R_L = 10\Omega$, $V_O > 2/3\ V_{SUPPLY}$	100 (Typ.)			100 (Typ.)			dB
V_{CMR}	Input Voltage Range	Typical	−10		+10	−10		+10	V
CMRR	Common Mode Rejection Ratio	$R_S = 10k\Omega$	70 (Typ.)			70 (Typ.)			dB
PSRR	Power Supply Rejection Ratio	$R_S = 10\Omega$	77 (Typ.)			77 (Typ.)			dB
SR	Slew Rate	$C_L = 30pF$, $A_V = 1$, $R_L = 10\Omega$ $V_O \geq 2/3\ V_{SUPP}$	0.5 (Typ.)			0.5 (Typ.)			V/μs
ΔV_O	Output Voltage Swing	$R_L = 10\Omega$, $A_V = 10$	±12			±12			V
I_O	Output Current	$R_L = 5\Omega$, $A_V = 10$	±1.25	1.4		±1.5	1.8		A
I_Q	Power Supply Quiescent Current	$R_L = \infty$, $V_{IN} = 0V$		80	125		70	100	mA
OPERATING CHARACTERISTICS (continued) $T_A = -55°C$ to $+125°C$ (M) or $T_A = -25°C$ to $+85°C$ (I).									
V_{OS}	Input Offset Voltage	Pd < 1W	−10		+10	−9		+9	mV
I_{BIAS}	Input Bias Current	Pd < 1W			1500			750	nA
I_{OS}	Input Offset Current				500			200	nA
A_{VOL}	Large Signal Voltage Gain	$R_L = 10\Omega$, $\Delta V_O = 2/3\ V_{SUPPLY}$	90 (Typ.)			90 (Typ.)			dB
ΔV_O	Output Voltage Swing	$R_L = 10\Omega$, $A_V = 10$	±10			±10			V
$R_{\theta JA}$	Thermal Resistance Junction to Ambient	Without Heat Sink			40 (Typ.)			40 (Typ.)	°C/W
$R_{\theta JC}$	Thermal Resistance Junction to Case				3.0 (Typ.)			3.0 (Typ.)	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient	Mtd. on Wakefield 403 Heat Sink		4.5 (Typ.)			4.5 (Typ.)		°C/W
V_{SUPPLY}	Supply Voltage Range		±11		±17	±11		±17	V

Note: All typical values have been guaranteed by characterization and are not tested.

ICH8515

How To Set The Externally Programmable, Current Limiting Resistors:

The maximum output current is set by the addition of two external resistors. $R_{SC(+)}$ and $R_{SC(-)}$. Because of the internal power limiting circuitry, the maximum output current is available only when V_O is close to either power supply. As V_O moves away from V_{SUPPLY}, the maximum output current decreases in proportion to output voltage. The curve below shows maximum output current versus output voltage.

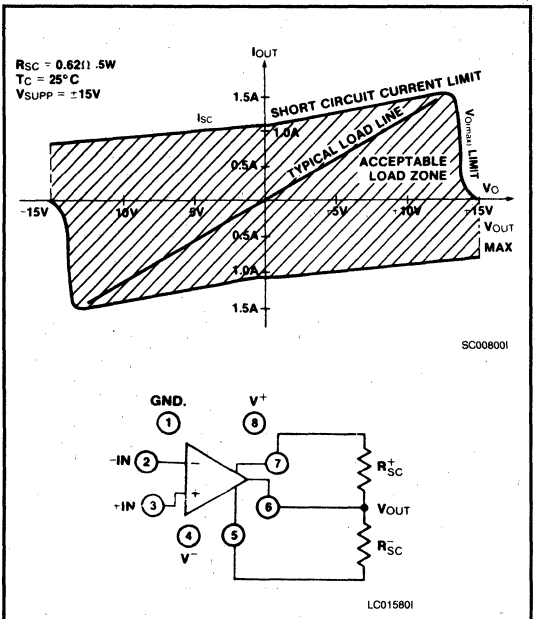


Figure 3: Maximum Output Current for Given R_{SC}

In general, for a given V_O, I_{SC} limit, and case temperature T_C, R_{SC} can be calculated from the equation below for V_O positive, I_{OUT} positive.

$$R_{SC} = \frac{(20.6V_O)^* + 680 - 2.2(T_C - 25°C)}{I_{SC\ (limit)}\ \text{in mA}}$$

*For V_O negative, replace this term with 10.3 $(V_O - 1.2)$

For example, for I_O = 1.5A @ V_O = 12V and T_C = 25°C,

$$R_{SC} = \frac{(20.6)(12) + 680}{1500} = \frac{927.2}{1500} = .618\Omega$$

Therefore for this application, R_{SC} = .62Ω (closest standard value).

When 0.62Ω is used, I_{SC} @ V_O = 0V will be reduced to about 1A. Except for small changes in the "$\pm V_{O(max)}$ Limit" area, the effects of changing R_{SC} on the I_{OUT} vs V_{OUT} characteristics can be determined by merely changing the I_{OUT} scale on Figure 3 to correspond to the new value. Changes in T_C move the limit curve bodily up and down.

This internal power limiting circuitry however does not at all restrict the normal use of the driver. For any normal load, the static load line will be similar to that shown in Figure 3. Clearly, as V_O decreases, the I_O requirement falls also, more steeply than the I_O available. For reactive loads, the dynamic load lines are more complex. Two typical operating point loci are sketched here:

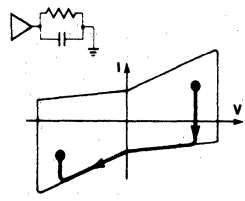


Figure 4: Capacitive Load

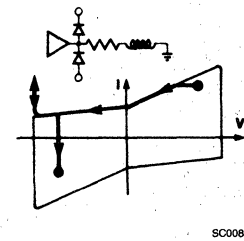


Figure 5: Inductive Load (Note catch diode)

Thus the limiting circuitry protects the load and avoids needless damage to the driver during abnormal conditions. For any 12VDC motor/actuator, the R_{SC} resistors must be calculated to get proper power delivered to the motor (up to a maximum of 1.5 amps) and V_{SUPP} set at ±15V. For lower supply and/or output voltages, the maximum output current will follow graphs of Figures 3 and 13.

NOTE ON AMPLIFIER POWER DISSIPATION

The steady state power dissipation limit is given by

$$P_D = \frac{T_{J(MAX)} - T_A}{R_{\theta JC} + R_{\theta CH} + R_{\theta HA}}$$

where

T_J = Maximum junction temperature

T_A = Ambient temperature

$R_{\theta JC}$ = Thermal resistance from transistor junction to case of package

$R_{\theta CH}$ = Thermal resistance from case to heat sink

$R_{\theta HA}$ = Thermal resistance from heat sink to ambient air

And since

T_J = 150°C for silicon transistors

$R_{\theta JC} \cong$ 2.0C/WATT for a steel bottom TO-3 package with die attachment to beryllia substrate header

Note: All typical values have been guaranteed by characterization and are not tested.

$R_{\theta CH}$ = .045°C/W for 1 mil thickness of Wakefield type 120 thermal joint compound
.09°C/W for 2 mil thickness of type 120
.13°C/W for 3 mil thickness of type 120
.17°C/W for 4 mil thickness for type 120
.21°C/W for 5 mil thickness of type 120
.24°C/W for 6 mil thickness of type 120

$R_{\theta HA}$ = The choice of heat sink that a user selects depends upon the amount of room available to mount the heat sink. A sample calculation follows: by choosing a Wakefield 403 heat sink, with free air, natural convection (no fan). $R_{\theta HA} \cong 2.0°C/W$. Using 4 mil joint compound,

$$P_D = \frac{150°C - T_A}{2.0° + 0.17° + 2.0} = \frac{150°C - T_A}{4.17°C/W}$$

or @ $T_A = 25°C$,

$$\frac{150°C - 25°C}{4.17°C/W} = 30W$$

and @ $T_A = 125°C$,

$$\frac{150°C - 125°C}{4.17°C/W} = 6W$$

From Figure 6 the worst case steady state power dissipation for the IH8515 ($R_{SC} = 0.62\Omega$) is about 15W and 11W respectively. Thus this heat sink is adequate.

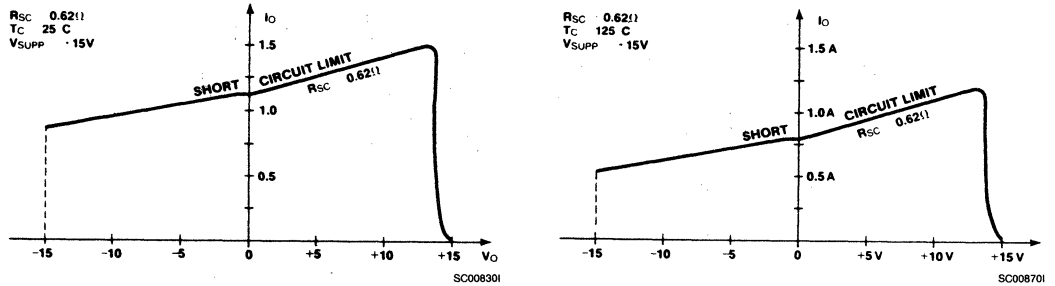
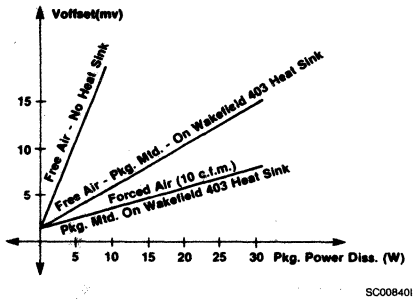
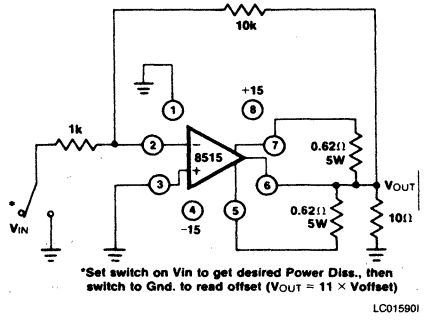


Figure 6: I_{OUT} vs V_{OUT}

TYPICAL PERFORMANCE CHARACTERISTICS



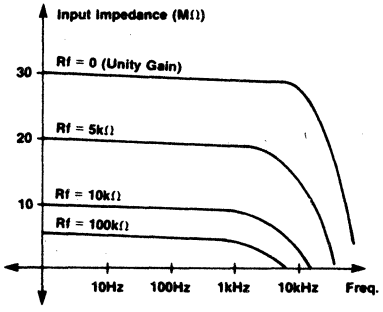


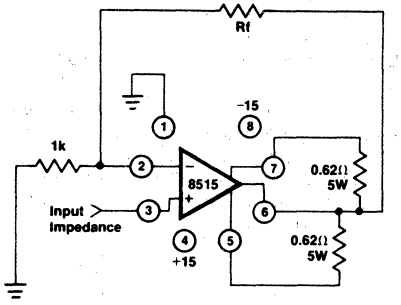
Input Offset Voltage vs Power Dissipation

Note: All typical values have been guaranteed by characterization and are not tested.

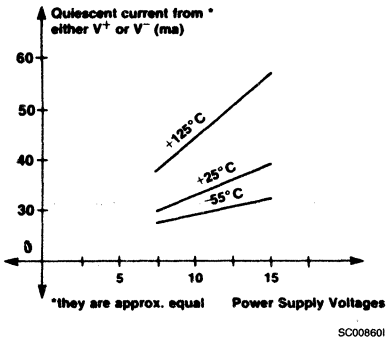
ICH8515

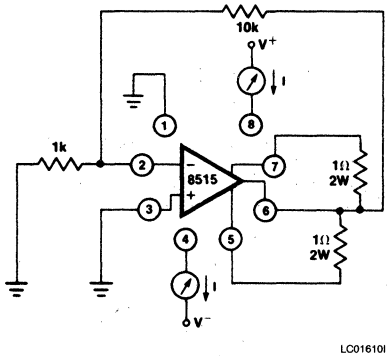
TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)



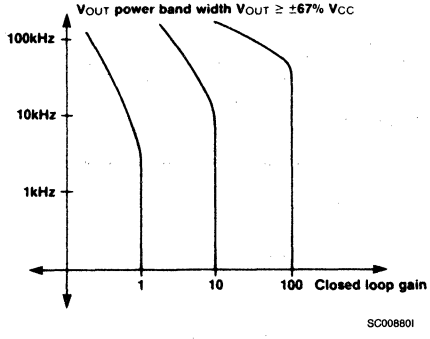


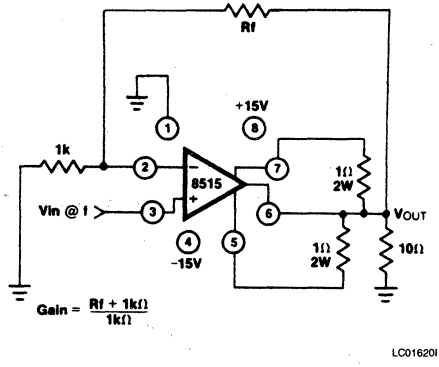
Input Impedance vs Gain vs Frequency





Quiescent Current vs Power Supply Voltage

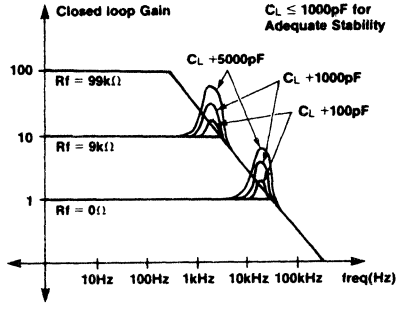


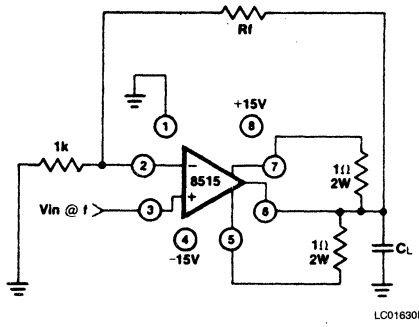


Large Signal Power Band Width

Note: All typical values have been guaranteed by characterization and are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)





Small Signal Frequency Response

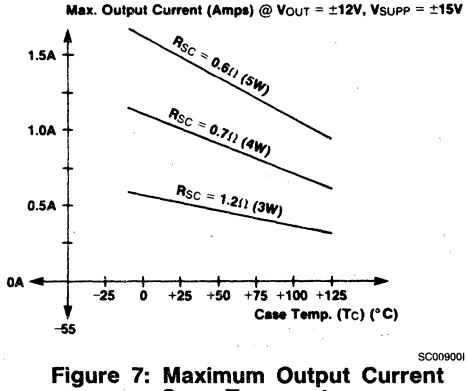


Figure 7: Maximum Output Current vs. Case Temperature

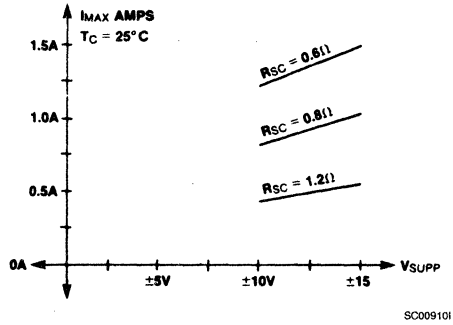


Figure 8: Maximum Output Current vs. V_{SUPPLY}

Note: All typical values have been guaranteed by characterization and are not tested.

ICH8515

TYPICAL APPLICATIONS

Constant Voltage Drive For D.C. Motors

Here $V_{OUT}/V_{IN} = 4$, and if $V_{IN} = -3V$, $V_{OUT} = +12V$, and vice versa for $V_{IN} = +3V$. Diodes D1, D2 should be 1N4001 types: these absorb the inductive kickbacks of the motor. The 2000pF capacitor is used to prevent system oscillation, by providing gain rolloff @ approx. 20kHz (−3dB).

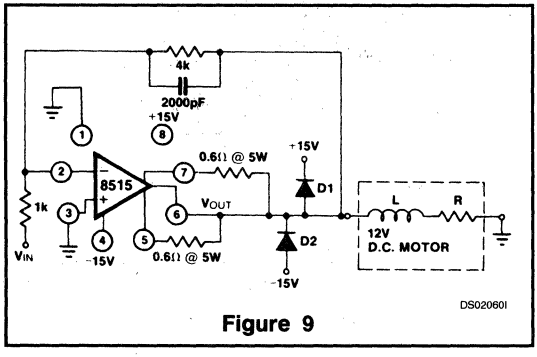


Figure 9

Constant Current Drive For D.C. Motors

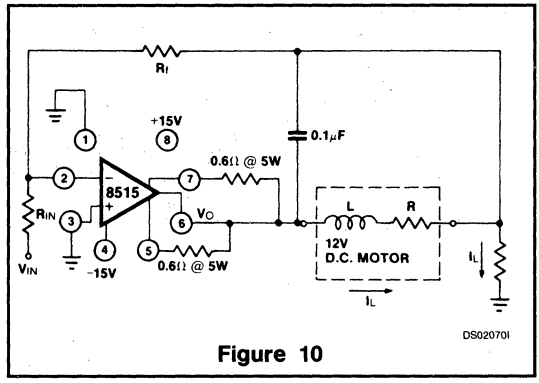


Figure 10

$$\frac{I_L}{V_{IN}} = -\frac{R_f}{R_{IN}} \cdot \frac{1}{R_L}, \text{ assuming } R_f >> R_L.$$

This circuit allows precisely set motor drive current with op. amp. feedback accuracy. If $R_{IN} = R_F = 1k\Omega$, and $R_L = 10\Omega$, then $\frac{I_L}{V_{IN}} = -0.1$ Amps/Volt, and if $R_L = 1\Omega$ (use 4W or more) and $R_F = R_{IN} = 1k\Omega$,

$$\frac{I_L}{V_{IN}} = -1 \times 1 = \frac{1 \text{ Amp}}{\text{Volt}}.$$

thus if $V_{IN} = 1.5V$, 1.5 amps will flow thru the motor. Since one side of the motor will have a 1.5V drop (with respect to GND), the V_O point will go to 13.5V and develop 12V across motor.

HEAT SINK INFORMATION

Heat sinks are available from Intersil. Order part number 29-0305 ($10.00 ea.) with a $R_{\theta HA} = 1.3°C/watt$. A convenient mating connector is also available. Order part number 29-0306 ($4.50 ea.).

NOTE: This product contains Beryllia. If used in an application where the package integrity may be breached and the internal parts crushed or machined, avoid inhalation of the dust.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7605/ICL7606
Commutating Auto-Zero (CAZ) Instrumentation Amplifier

GENERAL DESCRIPTION

The ICL7605/ICL7606 CMOS commutating auto-zero (CAZ) instrumentation amplifiers are designed to replace most of today's hybrid or monolithic instrumentation amplifiers, for low frequency applications from DC to 10Hz. This is made possible by the unique construction of this new Intersil device, which takes an entirely new design approach to low frequency amplifiers.

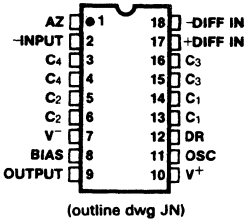
Unlike conventional amplifier designs, which employ three op-amps and require ultra-high accuracy in resistor tracking and matching, the CAZ instrumentation amplifier requires no trimming except for gain. The key features of the CAZ principle involve automatic compensation for long-term drift phenomena and temperature effects, and a flying capacitor input.

The ICL7605/ICL7606 consist of two analog sections — a unity gain differential to single-ended voltage converter and a CAZ op amp. The first section senses the differential input and applies it to the CAZ amp section. This section consists of an operational amplifier circuit which continuously corrects itself for input voltage errors, such as input offset voltage, temperature effects, and long term drift.

The ICL7605/ICL7606 is intended for low-frequency operation in applications such as strain gauge amplifiers which require voltage gains from 1 to 1000 and bandwidths from DC to 10Hz. Since the CAZ amp automatically corrects itself for internal errors, the only periodic adjustment required is that of gain, which is established by two external resistors. This, combined with extremely low offset and temperature coefficient figures, makes the CAZ instrumentation amplifier very desirable for operation in severe environments (temperature, humidity, toxicity, radiation, etc.) where equipment service is difficult.

FEATURES

- **Exceptionally Low Input Offset Voltage — 2μV**
- **Low Long Term Input Offset Voltage Drift — 0.2μV/Year**
- **Low Input Offset Voltage Temperature Coefficient — 0.05μV/°C**
- **Wide Common Mode Input Voltage Range — 0.3V Above Supply Rail**
- **High Common Mode Rejection Ratio — 100 dB**
- **Operates at Supply Voltages As Low As ±2V**
- **Short Circuit Protection On Outputs for ±5V Operation**
- **Static-Protected Inputs — No Special Handling Required**
- **Compensated (ICL7605) or Uncompensated (ICL7606) Versions**



(outline dwg JN)

CD01470I

Figure 1: Pin Configuration

ORDERING INFORMATION

Order parts by the following part numbers:

PART NUMBER	COMPENSATION	TEMPERATURE RANGE	PACKAGE
ICL7605CJN	INTERNAL	0°C to +70°C	18-PIN CERDIP
ICL7605IJN	INTERNAL	-25°C to +85°C	18-PIN CERDIP
ICL7605MJN	INTERNAL	-55°C to +125°C	18-PIN CERDIP
ICL7605/D	INTERNAL	—	DICE**
ICL7606CJN	EXTERNAL	0°C to +70°C	18-PIN CERDIP
ICL7606IJN	EXTERNAL	-25°C to +85°C	18-PIN CERDIP
ICL7606MJN	EXTERNAL	-55°C to +125°C	18-PIN CERDIP
ICL7606/D	EXTERNAL	—	DICE**

**Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.

301681-002

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7605/ICL7606

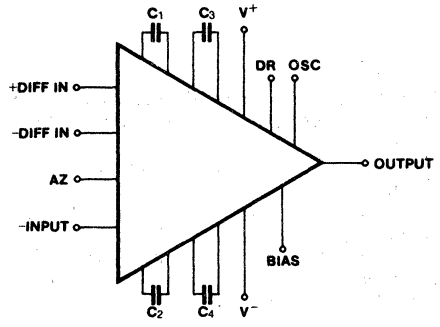


Figure 2: Symbol

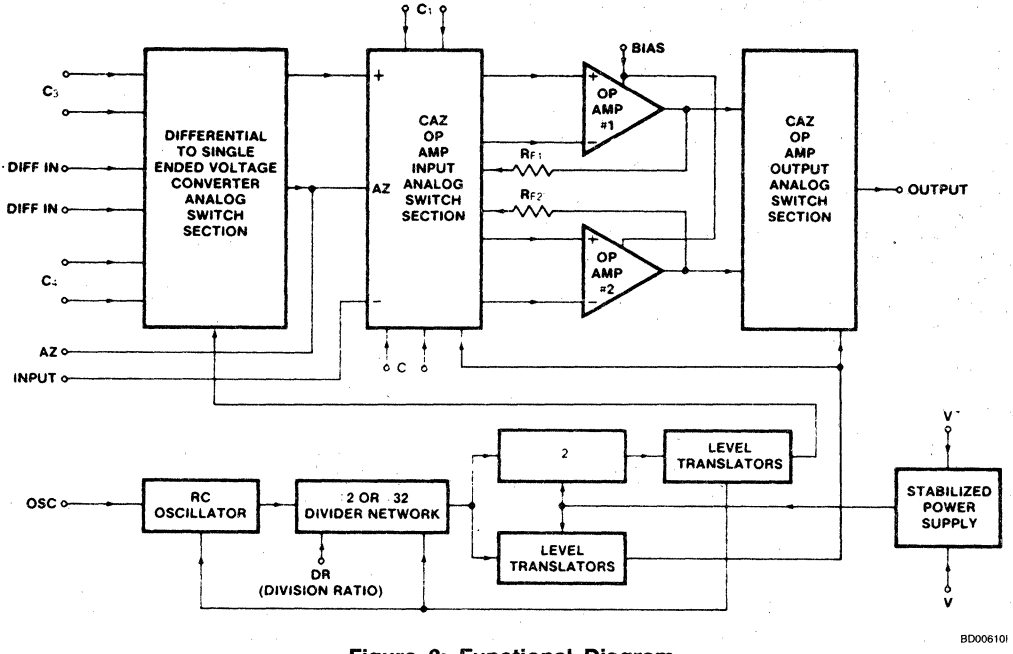


Figure 3: Functional Diagram

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7605/ICL7606

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
DR Input Voltage ..... (V^+ −8) to (V^+ +0.3)V
Input Voltage (C_1, C_2, C_3, C_4 +DIFF IN, −DIFF IN, −INPUT, BIAS, OSC), (Note 1) ..... (V^- −0.3) to (V^+ +0.3)V
Differential Input Voltage (+DIFF IN to −DIFF IN) (Note 2) ..... (V^- −0.3) to (V^+ +0.3)V
Duration of Output Short Circuit (Note 3) ..... Unlimited
Continuous Total Power Dissipation (Note 4) 500mW
Operating Temperature Range:
ICL7605/ICL7606CJN ..... 0 to +70°C
ICL7605/ICL7606IJN ..... −25°C to +85°C
ICL7605/ICL7606MJN ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Due to the SCR structure inherent in all CMOS devices, exceeding these limits may cause destructive latch up. For this reason, it is recommended that no inputs from sources operating on a separate power supply be applied to the 7605/6 before its own power supply is established, and that when using multiple supplies, the supply for the 7605/6 should be turned on first.

Note 2: No restrictions are placed on the differential input voltages on either the +DIFF IN or −DIFF IN inputs so long as these voltages do not exceed the power supply voltages by more than 0.3V.

Note 3: The outputs may be shorted to ground (GND) or to either supply (V^+ or V^-). Temperatures and/or supply voltages must be limited to insure that the dissipation ratings are not exceeded.

Note 4: For operation above 25°C ambient temperature, derate 4mW/°C from 500mW above 25°C.

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +5V$, $V^- = -5V$, $T_A = +25°C$, DR pin connected to V^+ ($f_{COM} \simeq 160Hz$, $f_{COM1} \simeq 80Hz$), $C_1 = C_2 = C_3 = C_4 = 1\mu F$, Test Circuit 1 unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		VALUE MIN	VALUE TYP	VALUE MAX	UNIT
V_{OS}	Input Offset Voltage	$R_S \le 1k\Omega$	Low Bias Setting		±2		μV
			Med Bias Setting		±2	±5	μV
			High Bias Setting		±7		μV
		MIL version over temp.	Med Bias Setting			±20	μV
$\Delta V_{OS}/\Delta T$	Average Input Offset Voltage Temperature Coefficient (Note 5)	Low or Med Bias Settings	−55°C > T_A > +25°C		0.01	0.2	μV/°C
			+25°C > T_A > +85°C		0.01	0.2	μV/°C
			+25°C > T_A > +125°C		0.05	0.2	μV/°C
$\Delta V_{OS}/\Delta t$	Long Term Input Offset Voltage Stability	Low or Med Bias Settings			0.5		μV/Year
CMVR	Common Mode Input Range			−5.3		+5.3	V
CMRR	Common Mode Rejection Ratio	$C_{OSC} = 0$, DR connected to V^+, $C_3 = C_4 = 1\mu F$			94		dB
		$C_{OSC} = 1\mu F$, DR connected to GND, $C_3 = C_4 = 1\mu F$			100		dB
		$C_{OSC} = 1\mu F$, DR connected to GND, $C_3 = C_4 = 10\mu F$			104		dB
PSRR	Power Supply Rejection Ratio				110		dB
$-I_{BIAS}$	−INPUT Bias Current	Any bias setting, $f_c = 160Hz$ (Includes charge injection currents)			0.15	1.5	nA
$\bar{e}_{n(p-p)}$	Equivalent Input Noise Voltage peak-to-peak		Low Bias Mode		4.0		μV
		Band Width 0.1 to 10Hz	Med Bias Mode		4.0		μV
			High Bias Mode		5.0		μV
$\bar{e}_n$	Equivalent Input Noise voltage	Band Width 0.1 to 1.0Hz	All Bias Modes		1.7		μV
A_{VOL}	Open Loop Voltage Gain	$R_L = 10k\Omega$	Low Bias Setting	90	105		dB
			Med Bias Setting	90	105		dB
			High Bias Setting	80	100		dB
$\pm V_O$	Maximum Output Voltage Swing	$R_L = 1M\Omega$			±4.9		V
		$R_L = 100k\Omega$			±4.8		V
		$R_L = 10k\Omega$	Positive Swing	+4.4			V
			Negative Swing			−4.5	V
GBW	Bandwidth of Input Voltage Translator	$C_3 = C_4 = 1\mu F$	All Bias Modes		10		Hz
f_{COM}	Nominal Commutation Frequency	$C_{OSC} = 0$	DR Connected to V^+		160		Hz
			DR Connected to GND		2560		Hz
f_{COM1}	Nominal Input Converter Commutation Frequency	$C_{OSC} = 0$	DR Connected to V^+		80		Hz
			DR Connected to GND		1280		Hz
V_{BH}	Bias Voltage required to set Quiescent Current	Low Bias Setting		$V^+ - 0.3$	V^+	$V^+ + 0.3$	V
V_{BM}		Med Bias Setting		$V^- + 1.4$	GND	$V^+ - 1.4$	V
V_{BL}		High Bias Setting		$V^- - 0.3$	V^-	$V^- + 0.3$	V
I_{BIAS}	Bias (Pin 8) Input Current				±30		pA

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7605/ICL7606

INTERSIL

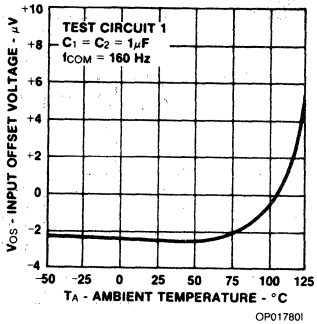
ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	VALUE			UNIT
			MIN	TYP	MAX	
I_{DR}	Division Ratio Input Current	$V^+ - 8.0 \le V_{DR} \le V^+ + 0.3$ volt		±30		pA
V_{DRH} V_{DRL}	DR Voltage required to set Oscillator division ratio	Internal oscillator division ratio 32 Internal oscillator division ratio 2	$V^+ - 0.3$ $V^+ - 8$		$V^+ + 0.3$ $V^+ - 1.4$	V V
R_{AS}	Effective Impedance of Voltage Translator Analog Switches			30		kΩ
I_{SUPP}	Supply Current	High Bias Setting Med Bias Setting Low Bias Setting		7 1.7 0.6	15 5 1.5	mA mA mA
$V^+ - V^-$	Operating Supply Voltage Range	High Bias Setting Med or Low Bias Setting	5 4		10 10	V V

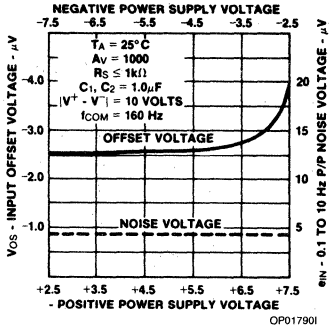
Note 5: For Design only, not 100% tested.

TYPICAL PERFORMANCE CHARACTERISTICS

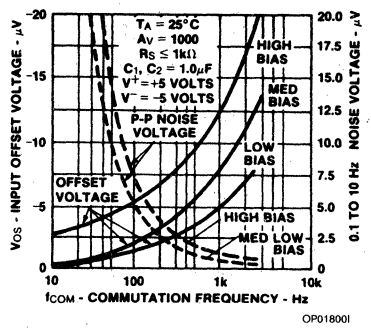
INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



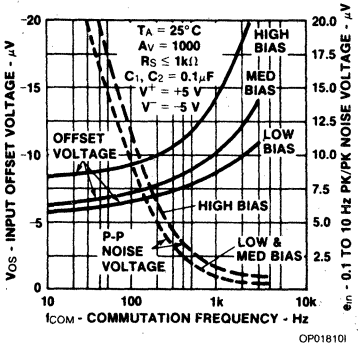
INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGES



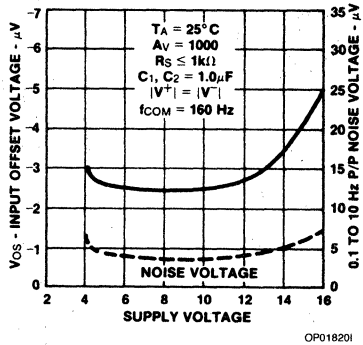
INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A FUNCTION OF COMMUTATION FREQUENCY (C_1, C_2 = 1µF)



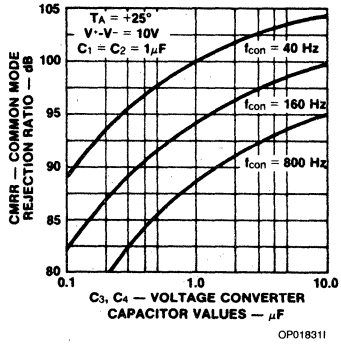
INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A FUNCTION OF COMMUTATION FREQUENCY (C_1, C_2 = 0.1 µF)



INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE AS A FUNCTION OF SUPPLY VOLTAGE (V^+-V^-)



COMMON MODE REJECTION RATIO AS A FUNCTION OF THE INPUT DIFFERENTIAL TO SINGLE ENDED VOLTAGE CONVERTER CAPACITORS

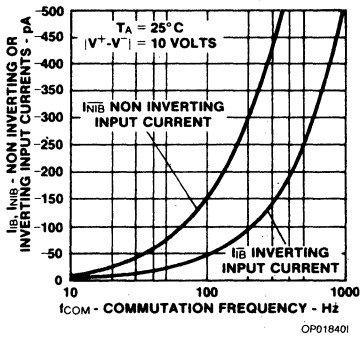


Note: All typical values have been guaranteed by characterization and are not tested.

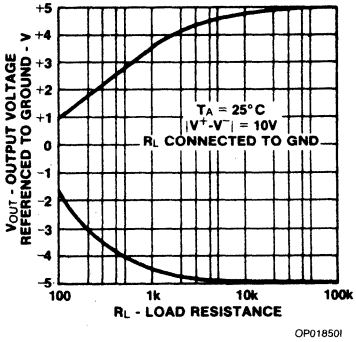
ICL7605/ICL7606

TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

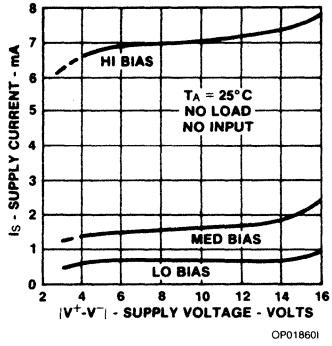
INPUT CURRENT AS A FUNCTION OF COMMUTATION FREQUENCY



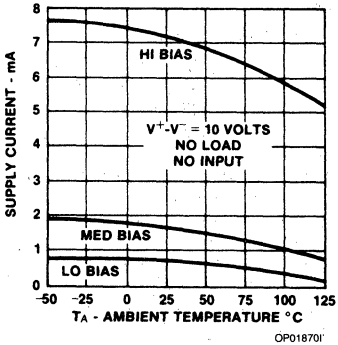
MAXIMUM OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT LOAD RESISTANCE



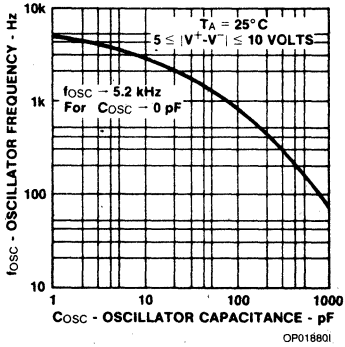
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



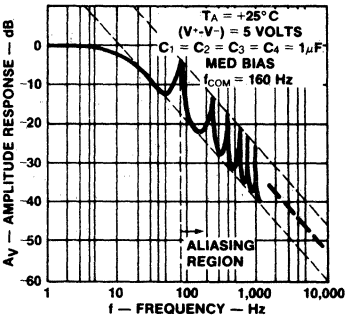
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



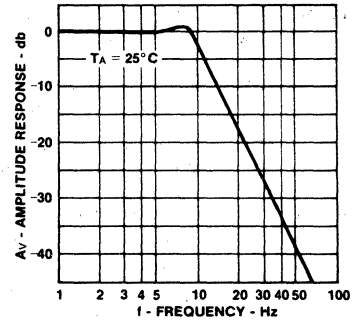
OSCILLATOR FREQUENCY AS A FUNCTION OF EXTERNAL CAPACITIVE LOADING



AMPLITUDE RESPONSE OF THE INPUT DIFFERENTIAL TO SINGLE ENDED VOLTAGE CONVERTER



FREQUENCY RESPONSE OF THE 10Hz LOW PASS FILTER USED TO MEASURE NOISE (TEST CIRCUIT 2).



Note: All typical values have been guaranteed by characterization and are not tested.

ICL7605/ICL7606

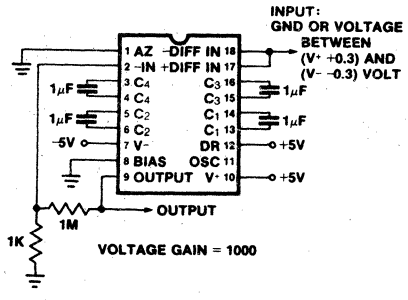


Figure 4: Test Circuit 1

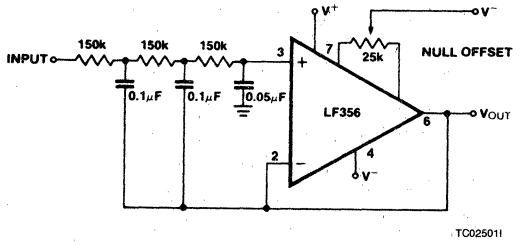


Figure 5: Test Circuit 2
DC to 10Hz Unity Gain Low Pass Filter

DETAILED DESCRIPTION

CAZ Instrumentation Amp Overview

The CAZ instrumentation amplifier operates on principles which are very different from those of the conventional three op-amp designs, which must use ultra-precise trimmed resistor networks in order to achieve acceptable accuracy. An important advantage of the ICL7605/ICL7606 CAZ instrumentation amp is the provision for self-compensation of internal error voltages, whether they are derived from steady-state conditions, such as temperature and supply voltage fluctuations, or are due to long term drift.

The CAZ instrumentation amplifier is constructed with monolithic CMOS technology, and consists of three distinct sections, two analog and one digital. The two analog sections — a differential to single-ended voltage converter, and a CAZ op amp — have on-chip analog switches to steer the input signal. The analog switches are driven from a self-contained digital section which consists of an RC oscillator, a programmable divider, and associated voltage translators. A functional layout of the ICL7605/ICL7606 is shown in Figure 6.

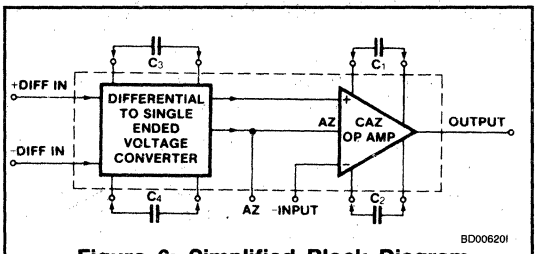


Figure 6: Simplified Block Diagram

The ICL7605/ICL7606 have approximately constant equivalent input noise voltage, CMRR, PSRR, input offset voltage and drift values independent of the gain configuration. By comparison, hybrid-type modules which use the traditional three op amp configuration have relatively poor performance at low gain (1 to 100) with improved performance above a gain of 100.

The only major limitation of the ICL7605/ICL7606 is its low-frequency operation (10 to 20Hz maximum). However in many applications bandwidth is not the most important parameter.

CAZ Op Amp Section

Operation of the CAZ op-amp section of the ICL7605/ICL7606 is best illustrated by referring to Figure 7. The basic amplifier configuration, represented by the large triangles, has one more input than does a regular op amp — the AZ, or auto-zero terminal. The voltage on the AZ input is that level at which each of the internal op amps will be auto-zeroed. In Mode A, op amp #2 is connected in a unity gain mode through on-chip analog switches. It charges external capacitor C_2 to a voltage equal to the DC input offset voltage of the amplifier plus the instantaneous low-frequency noise voltage. A short time later, the analog switches reconnect the on-chip op amps to the configuration shown in Mode B. In this mode, op amp #2 has capacitor C_2 (which is charged to a voltage equal to the offset and noise voltage of op amp #2) connected in series to its non-inverting (+) input in such a manner as to null out the input offset and noise voltages of the amplifier. While one of the on-chip op amps is processing the input signal, the second op amp is in an auto-zero mode, charging a capacitor to a voltage equal to its equivalent DC and low frequency error voltage. The on-chip amplifiers are connected and reconnected at a rate designated as the commutation frequency (f_{COM}), so that at all times one or the other of the on-chip op amps is processing the input signal, while the voltages on capacitors C_1 and C_2 are being updated to compensate for variables such as low frequency noise voltage and input offset voltage changes due to temperature, drift or supply voltages effects.

Note: All typical values have been guaranteed by characterization and are not tested.

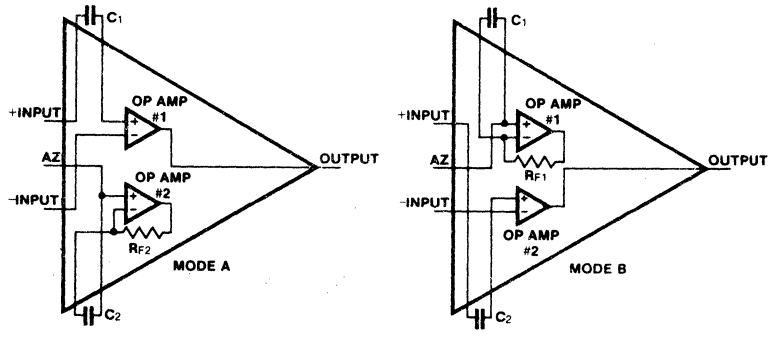


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Figure 7: Diagrammatic representation of the 2 half cycles of operation of the CAZ OP AMP.

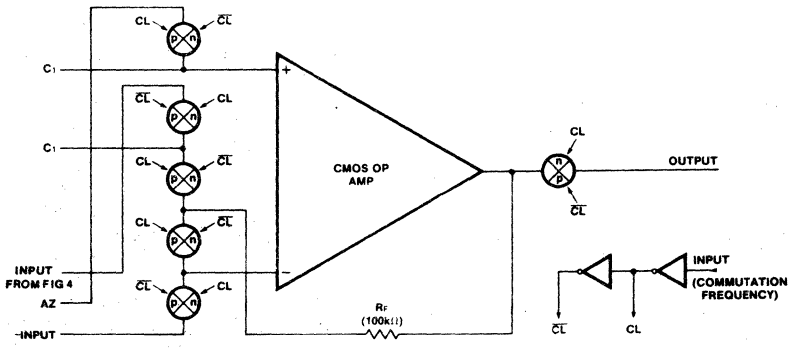

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Figure 8: Schematic of analog switches connecting each internal OP AMP to its inputs and output.

Note: All typical values have been guaranteed by characterization and are not tested.

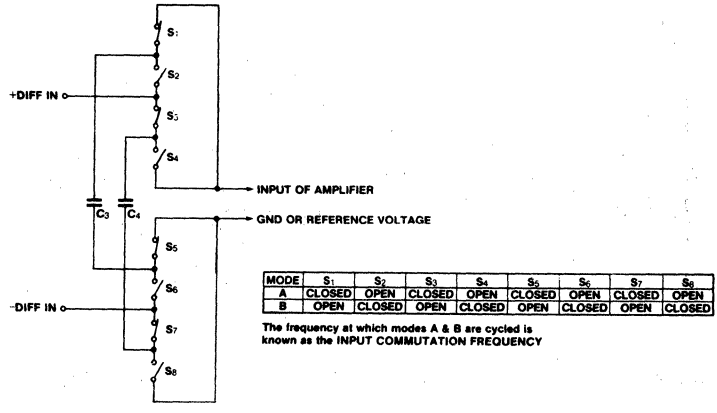


Figure 9: Schematic of the differential to single ended voltage converter

Compared to the standard bipolar or FET input op amps, the CAZ amp scheme demonstrates a number of important advantages:

* Effective input offset voltages can be reduced from 1000 to 10,000 times without trimming.
* Long-term offset voltage drift phenomena can be compensated and dramatically reduced.
* Thermal effects can be compensated for over a wide operating temperature range. Reductions can be as much as 100 times or better.
* Supply voltage sensitivity is reduced.

CMOS processing is ideally suited to implement the CAZ amp structure. The digital section is easily fabricated, and the transmission gates (analog switches) which connect the on-chip op amps can be constructed for minimum charge injection and the widest operating voltage range. The analog section, which includes the on-chip op amps, contributes performance figures which are similar to bipolar or FET input designs. The CMOS structure provides the CAZ op-amp with open-loop gains of greater than 100dB, typical input offset voltages of ±5mV, and ultra-low leakage currents, typically 1pA.

The CMOS transmission gates connect the on-chip op amps to external input and output terminals, as shown in Figure 8. Here, one op amp and its associated analog switches are required to connect each on-chip op amp, so that at any time three switches are open and three switches are closed. Each analog switch consists of a P-channel transistor in parallel with an N-channel transistor.

DIFFERENTIAL-TO-SINGLE-ENDED UNITY GAIN VOLTAGE CONVERTER

An idealized schematic of the voltage converter block is shown in Figure 9. The mode of operation is quite simple, involving two capacitors and eight switches. The switches are arranged so that four are open and four are closed. The four conducting switches connect one of the capacitors across the differential input, and the other from a ground or reference voltage to the input of the CAZ instrumentation amp. The output signal of this configuration is shown in Figure 10, where the voltage steps equal the differential voltage (V_A-V_B) at commutation times a, b, c, etc. The output waveform thus represents all information contained in the input signal from DC up to the commutation frequency, including commutation and noise voltages. Sampling theory states that to preserve the information to be processed, at least two samples must be taken within a period (1/f) of the highest frequency being sampled. Consequently this scheme preserves information up to the commutation frequency. Above the commutation frequency, the input signal is translated to a lower frequency. This phenomenon is known as aliasing. Although the output responds to inputs above the commutation frequency, the frequencies of the output responses will be below the commutation frequency.

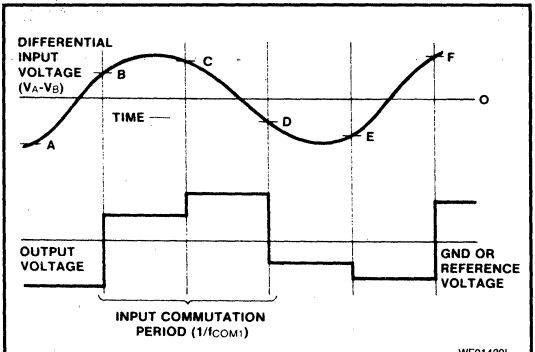


Figure 10: Input to Output Voltage waveforms from the differential to single ended voltage converter. For additional information, see frequency characteristics in Amplitude Response of the Input Differential to single ended voltage converter graph on page 5.

Note: All typical values have been guaranteed by characterization and are not tested.

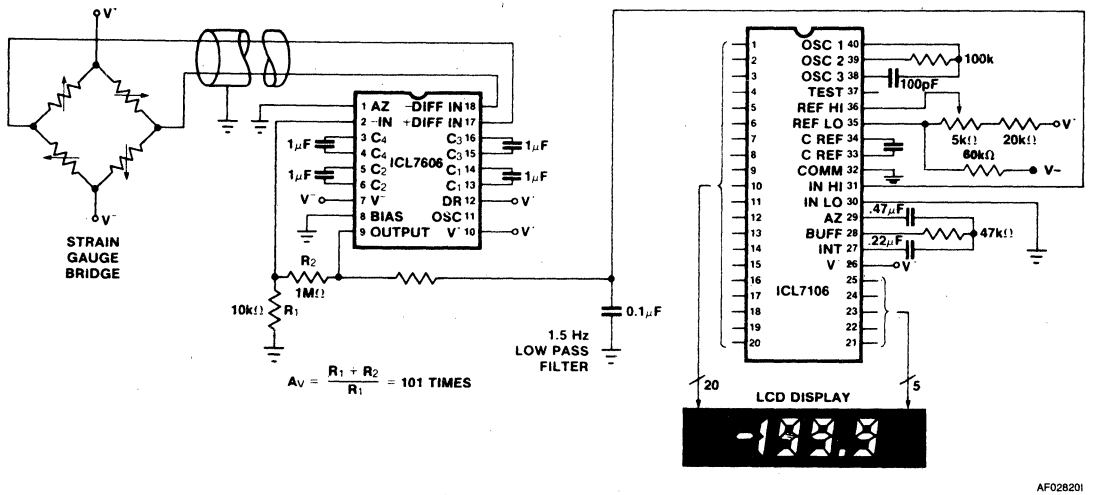


Figure 11: 3-1/2 Digit Digital Readout Torque Wrench

The voltage converter is fabricated with CMOS analog switches, which contain a parallel combination of P-channel and N-channel transistors. The switches have a finite ON impedances of 30kΩ, plus parasitic capacitances to the substrate. Because of the charge injection effects which appear at both the switches and the output of the voltage converter, the values of capacitors C_3 and C_4 must be about 1μF to preserve signal translation accuracies to 0.01%. The 1μF capacitors, coupled with the 30kΩ equivalent impedance of the switches, produce a low-pass filter response from the voltage converter which is down approximately 3dB at 10Hz.

APPLICATIONS

Using the ICL7605/ICL7606 to Build a Digital Readout Torque Wrench

A typical application for the ICL7605/ICL7606 is in a strain gauge system, such as the digital readout torque wrench circuit shown in Figure 6. In this application, the CAZ instrumentation amplifier is used as a preamplifier, taking the differential voltage of the bridge and converting it to a single-ended voltage referenced to ground. The signal is then amplified by the CAZ instrumentation amplifier and applied to the input of a 3-1/2 digit dual-slope A/D converter which drives the LCD panel meter display. The A/D converter device used in this instance is the Intersil ICL7106.

In the digital readout torque wrench circuit, the reference voltage for the ICL7106 is derived from the stimulus applied to the strain gauge, to utilize the ratiometric capabilities of the A/D. In order to set the full-scale reading, a value of gain for the ICL7605/ICL7606 instrumentation CAZ amp must be selected along with an appropriate value for the reference voltage. The gain should be set so that at full scale, the output will swing about 0.5V. The reference voltage required is about one-half the maximum output swing, or approximately 0.25V.

In this type of system, only one adjustment is required. Either the amplifier gain or the reference voltage must be varied for full-scale adjustment. Total current consumption of all circuitry, less the current through the strain gauge bridge, is typically 2mA. The accuracy is limited only by resistor ratios and the transducer.

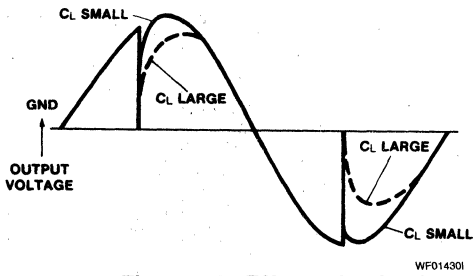
SOME HELPFUL HINTS

Testing the ICL7605/ICL7606 CAZ Instrumentation Amplifier

Figure 4 and 5 (Test Circuits) provide a convenient means of measuring most of the important electrical parameters of the CAZ instrumentation amp. The output signal can be viewed on an oscilloscope after being fed through a low-pass filter. It is recommended that for most applications, a low-pass filter of about 1.0 to 1.5Hz be used to reduce the peak-to-peak noise to about the same level as the input offset voltage.

The output low-pass filter must be a high-input impedance RC type — not simply a capacitor across the feedback resistor R_2. Resistor and capacitor values of about 100kΩ and 1.0μF are necessary so that the output load impedance on the CAZ op-amp is greater than 100kΩ.

Note: All typical values have been guaranteed by characterization and are not tested.



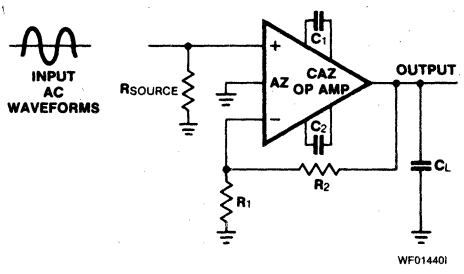


Figure 12: Effect of a load capacitor on output voltage waveforms.

Bias Control

The on-chip op amps consume over 90% of the power required by the ICL7605/ICL7606. For this reason, the internal op amps have externally- programmable bias levels. These levels are set by connecting the BIAS terminal to either V^+, GND, or V^-, for LOW, MED or HIGH BIAS levels, respectively. The difference between each bias setting is about a factor of 3, allowing a 9:1 ratio of quiescent supply current versus bias setting. This current programmability provides the user with a choice of device power dissipation levels, slew rates (the higher the slew rate, the better the recovery from commutation spikes), and offset errors due to "IR" voltage drops and thermoelectric effects (the higher the power dissipation, the higher the input offset error). In most cases, the medium bias (MED BIAS) setting will be found to be the best choice.

Output Loading (Resistive)

With a 10kΩ load, the output voltage swing can vary across nearly the entire supply voltage range, and the device can be used with loads as low as 2kΩ.

However, with loads of less than 50kΩ, the on-chip op amps will begin to exhibit the characteristics of transconductance amplifiers, since their respective output impedances are nearly 50kΩ each. Thus the open-loop gain is 20dB less with a 2kΩ load than it would be with a 20kΩ load. Therefore, for high gain configurations requiring high accuracy, an output load of 100kΩ or more is suggested.

There is another consideration in applying the CAZ instrumentation op amps which must not be overlooked. This is the additional power dissipation of the chip which will result from a large output voltage swing into a low resistance load. This added power dissipation can affect the initial input offset voltages under certain conditions.

Output Loading (Capacitive)

In many applications, it is desirable to include a low-pass filter at the output of the CAZ instrumentation op amp to reduce high-frequency noise outside the desired signal passband. An obvious solution when using a conventional op amp would be to place a capacitor across the external feedback resistor and thus produce a low-pass filter.

However, with the CAZ op amp concept this is not possible because of the nature of the commutation spikes. These voltage spikes exhibit a low-impedance characteristic in the direction of the auto-zero voltage and a high-impedance characteristic on the recovery edge, as shown in Figure 12. It can be seen that the effect of a large load capacitor produces an area error in the output waveform, and hence an effective gain error. The output low-pass filter must be of a high-impedance type to avoid these area errors. For example, a 1.5Hz filter will require a 100kΩ resistor and a 1.0μF capacitor, or a 1MΩ resistor and an 0.1μF capacitor.

Oscillator and Digital Circuitry Considerations

The oscillator has been designed to run free at about 5.2kHz when the OSC terminal is open circuit. If the full divider network is used, this will result in a nominal commutation frequency of approximately 160Hz. The commutation frequency is that frequency at which the on-chip op amps are switched between the signal processing and the auto-zero modes. A 160Hz commutation frequency represents the best compromise between input offset voltage and low frequency noise. Other commutation frequencies may provide optimization of some parameters, but always at the expense of others.

The oscillator has a very high output impedance, so that a load of only a few picofarads on the OSC terminal will cause a significant shift in frequency. It is therefore recommended that if the natural oscillator frequency is desired (5.2kHz) the terminal remains open circuit. In other instances, it may be desirable to synchronize the oscillator with an external clock source, or to run it at another frequency. The ICL7605/ICL7606 CAZ amp provides two degrees of flexibility in this respect. First, the DR (division ratio) terminal allows a choice of either dividing the oscillator by 32 (DR terminal to V^+) or by 2 (DR terminal to GND) to obtain the commutation frequency. Second, the oscillator may have its frequency lowered by the addition of an external capacitor connected between the OSC terminal and the V^+ or system GND terminals. For situations which require that the commutation frequency be synchronized with a master clock, (Figure 13) the OSC terminal may be driven from TTL logic (with resistive pull-up) or by CMOS logic, provided that the V^+ supply is +5V (±10%) and the logic driver also operates from a similar voltage supply. The reason for this requirement is that the logic section (including the oscillator) operates from an internal −5V supply, referenced to V^+ supply, which is not accessible externally.

Thermoelectric Effects

The ultimate limitations to ultra-high-sensitivity DC amplifiers are due to thermoelectric, Peltier, or thermocouple effects in electrical junctions consisting of various metals (alloys, silicon, etc.) Unless all junctions are at precisely the

Note: All typical values have been guaranteed by characterization and are not tested.

same temperature, small thermoelectric voltages will be produced, generally about 0.1μV/°C. However, these voltages can be several tens of microvolts per °C for certain thermocouple materials.

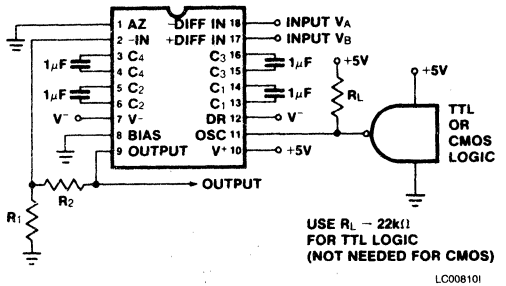


Figure 13: ICL7605 being clocked from external logic into the oscillator terminal.

In order to realize the extremely low offset voltages which the CAZ op amp can produce, it is necessary to take precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement across device surfaces. In addition, the supply voltages and power dissipation should be kept to a minimum by use of the MED BIAS setting. Employ a high impedance load and keep the ICL7605/ICL7606 away from equipment which dissipates heat.

Component Selection

The four capacitors (C_1 thru C_4) should each be about 1.0μF. These are relatively large values for non-electrolytic capacitors, but since the voltages stored on them change significantly, problems of dielectric absorption, charge bleed-off and the like are as significant as they would be for integrating dual-slope A/D converter applications. Polypropylene types are the best for C_3 and C_4, although Mylar may be adequate for C_1 and C_2.

Excellent results have been obtained for commercial temperature ranges using several of the less-expensive, smaller-size capacitors, since the absolute values of the capacitors are not critical. Even polarized electrolytic capacitors rated at 1.0μF and 50V have been used successfully at room temperature, although no recommendations are made concerning the use of such capacitors.

Commutation Voltage Transient Effects

Although in most respects the CAZ instrumentation amplifier resembles a conventional op amp, its principal applications will be in very low level, low-frequency preamplifiers limited to DC through 10Hz. The is due to the finite switching transients which occur at both the input and output terminals because of commutation effects. These transients have a frequency spectrum beginning at the commutation frequency, and including all of the higher harmonics of the commutation frequency. Assuming that the commutation frequency is higher than the highest in-band frequency, then the commutation transients can be filtered out with a low-pass filter.

The input commutation transients arise when each of the on-chip op amps experiences a shift in voltage which is equal to the input offset voltages (about 5-10mV), usually occurring during the transition between the signal processing mode and the auto-zero mode. Since the input capacitances of the on-chip op-amps are typically in the 10pF range, and since it is desirable to reduce the effective input offset voltage about 10,000 times, the offset voltage auto-zero capacitors C_1 and C_2 must have values of at least 10,000 x 10pF, or 0.1μF each.

The charge that is injected into the input of each op amp when being switched into the signal processing mode produces a rapidly-decaying voltage spike at the input, plus an equivalent DC input bias current averaged over a full cycle. This bias current is directly proportional to the commutation frequency, and in most instances will greatly exceed the inherent leakage currents of the input analog switches, which are typically 1.0pA at an ambient temperature of 25°C.

The output waveform in Figure 4 (with no input signal) is shown in Figure 14. Note that the equivalent noise voltage is amplified 1000 times, and that due to the slew rate of the on-chip op amps, the input transients of approximately 7mV are amplified by a factor of less than 1000.

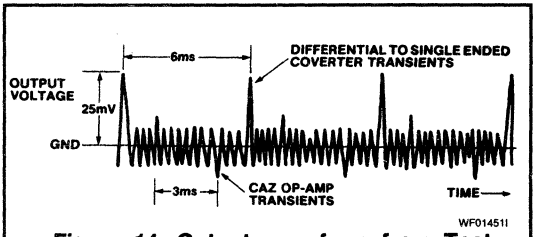


Figure 14: Output waveform from Test Circuit 1.

Layout Considerations

Care should be exercised in positioning components on the PC board particularly the capacitors C_1, C_2, C_3 and C_4, which must all be shielded from the OSC terminal. Also, parasitic PC board leakage capacitances associated with these four capacitors should be kept as low as possible to minimize charge injection effects.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL76XX
ICL76XX Series Low Power CMOS Operational Amplifiers

GENERAL DESCRIPTION

The ICL761X/762X/763X/764X series is a family of monolithic CMOS operational amplifiers. These devices provide the designer with high performance operation at low supply voltages and selectable quiescent currents, and are an ideal design tool when ultra low input current and low power dissipation are desired.

The basic amplifier will operate at supply voltages ranging from ±1.0V to ±8V, and may be operated from a single Lithium cell.

A unique quiescent current programming pin allows setting of standby current to 1mA, 100μA, or 10μA, with no external components. This results in power consumption as low as 20μW. Output swings range to within a few millivolts of the supply voltages.

Of particular significance is the extremely low (1pA) input current, input noise current of .01pA/$\sqrt{Hz}$, and $10^{12}\Omega$ input impedance. These features optimize performance in very high source impedance applications.

The inputs are internally protected and require no special handling procedures. Outputs are fully protected against short circuits to ground or to either supply.

AC performance is excellent, with a slew rate of 1.6V/μs, and unity gain bandwidth of 1MHz at I_Q = 1mA.

Because of the low power dissipation, operating temperatures and drift are quite low. Applications utilizing these features may include stable instruments, extended life designs, or high density packages.

FEATURES

- **Wide Operating Voltage Range ±1.0V to ±8V**
- **High Input Impedance — $10^{12}\Omega$**
- **Programmable Power Consumption — Low As 20μW**
- **Input Current Lower Than BIFETs — Typ 1pA**
- **Available As Singles, Duals, Triples, and Quads**
- **Output Voltage Swings to Within Millivolts Of V^- and V^+**
- **Low Power Replacement for Many Standard Op Amps**
- **Compensated and Uncompensated Versions**
- **Inputs Protected to ±200V (ICL7613/15)**
- **Input Common Mode Voltage Range Greater Than Supply Rails (ICL7612)**

APPLICATIONS

- **Portable Instruments**
- **Telephone Headsets**
- **Hearing Aid/Microphone Amplifiers**
- **Meter Amplifiers**
- **Medical Instruments**
- **High Impedance Buffers**

SELECTION GUIDE

DEVICE NOMENCLATURE

ICL76XX X X XX

- XX — Package Code
  - TV — TO-99, 8 pin
  - PA — Plastic 8 pin Minidip
  - PD — 14 pin Plastic Dip
  - PE — 16 pin Plastic Dip
  - JD — 14 pin CERDIP
  - JE — 16 pin CERDIP
  - ID — Dice
- X — Temperature Range
  - C = 0°C to 70°C
  - M = −55°C to +125°C
- X — V_{OS} Selection
  - A = 2mV
  - B = 5mV
  - C = 10mV
  - D = 15mV
  - E = 20mV

SPECIAL FEATURE CODES

C	=	INTERNALLY COMPENSATED
E	=	EXTERNALLY COMPENSATED
H	=	HIGH QUIESCENT CURRENT (1mA)
I	=	INPUT PROTECTED TO ±200V
L	=	LOW QUIESCENT CURRENT (10μA)
M	=	MEDIUM QUIESCENT CURRENT (100μA)
O	=	OFFSET NULL CAPABILITY
P	=	PROGRAMMABLE QUIESCENT CURRENT
V	=	EXTENDED CMVR

Note: All typical values have been guaranteed by characterization and are not tested.

ICL76XX

INTERSIL

ORDERING INFORMATION

BASIC PART NUMBER	NUMBER OF OP-AMPS IN PACKAGE, AND SPECIAL FEATURES (SEE ABOVE)	PACKAGE TYPE AND SUFFIX							
		8-LEAD TO-99		8-PIN MINIDIP	8-PIN SOIC	PLASTIC DIP (1)	CERAMIC DIP (1)		DICE
		0°C to +70°C	−55°C to +125°C	0°C to +70°C	0°C to +70°C	0°C to +70°C	0°C to +70°C	−55°C to +125°C	
ICL7611 ICL7612 ICL7613 ICL7614 ICL7615	SINGLE OP-AMP: C, O, P C, O, P, V C, I, O, P E, M, O E, I, M, O	ACTV BCTV DCTV	AMTV BMTV	ACPA BCPA DCPA	DCPA DCBA				D/D
ICL7621	DUAL OP-AMP: C, M	ACTV BCTV DCTV	AMTV BMTV	ACPA BCPA DCPA					D/D
ICL7622	DUAL OP-AMP: C, M, O					ACPD BCPD DCPD	ACJD BCJD DCJD	AMJD BMJD	D/D
ICL7631 ICL7632	TRIPLE OP-AMP: C, P P(3)					CCPE ECPE	CCJE ECJE	CMJE	E/D
ICL7641 ICL7642	QUAD OP-AMP: C, H C, L					CCPD ECPD	CCJD ECJD	CMJD	E/D

NOTES: 1. Duals and quads are available in 14 pin DIP package, triples in 16 pin only.
2. Ordering code must consist of basic part number and package suffix, e.g., ICL7611BCPA.
3. ICL7632 is not compensatable. Recommended for use in high gain circuits only.
**Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.

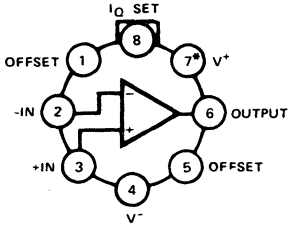
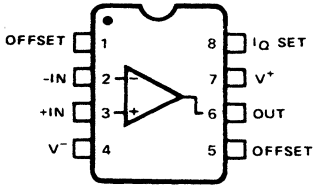
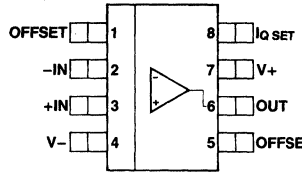
DEVICE	DESCRIPTION	PIN ASSIGNMENTS
ICL7611XCPA ICL7611XCTV ICL7611XMTV ICL7612XCPA ICL7612XCTV ICL7612XMTV ICL7613XCPA ICL7613XCTV ICL7613XMTV	Internal compensation, plus offset null capability and external I_Q control	TO-99 (TOP VIEW) (outline dwg TV)  *Pin 7 connected to case. 8 PIN DIP (TOP VIEW) (outline dwg PA)  8 PIN DIP (TOP VIEW) (outline dwg BA) 

Figure 1: Pin Configurations

Note: All typical values have been guaranteed by characterization and are not tested.

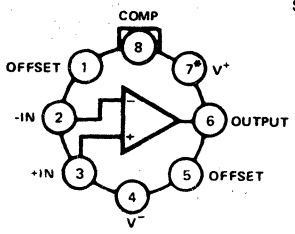
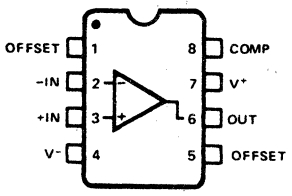
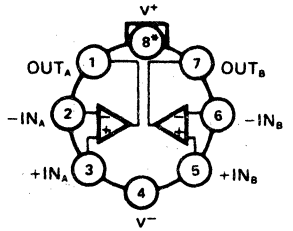
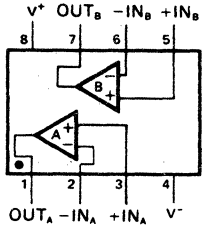
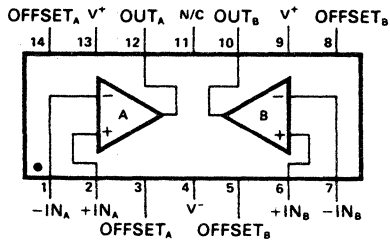
DEVICE	DESCRIPTION	PIN ASSIGNMENTS
ICL7614XCPA ICL7614XCTV ICL7614XMTV ICL7615XCPA ICL7615XCTV ICL7615XMTV	Fixed I_Q (100μA), external compensation, and offset null capability	TO-99 (TOP VIEW) (outline dwg TV)  *Pin 7 connected to case. 8 PIN DIP (TOP VIEW) (outline dwg PA) SOIC-8 
ICL7621XCPA ICL7621XCTV ICL7621XMTV	Dual op amps with internal compensation; I_Q fixed at 100μA Pin compaptible with Texas Inst. TL082 Motorola MC1458 Raytheon RC4558	TO-99 (TOP VIEW) (outline dwg TV)  *Pin 8 connected to case. * PIN DIP (TOP VIEW) (outline dwg PA) 
ICL7622XCPD	Dual op amps with external compensation and offset null capability; I_Q fixed at 100μA Pin compatible with Texas Inst. TL083 Fairchild μA747	14 PIN DIP (TOP VIEW) (outline dwgs JD, PD)  Note: Pins 9 and 13 are internally connected.

Figure 1: Pin Configurations (Cont.)

Note: All typical values have been guaranteed by characterization and are not tested.

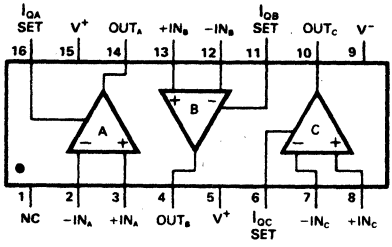
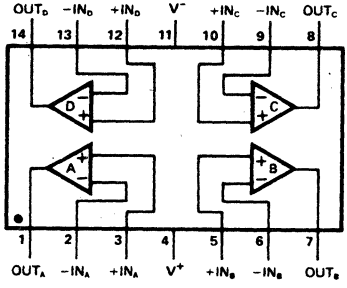
DEVICE	DESCRIPTION	PIN ASSIGNMENTS
ICL7631XCPE ICL7632XCPE	Triple op amps with internal compensation (ICL7631) and no compensation (ICL7632). Adjustable I_Q Same pin configuration as ICL8023.	16 PIN DIP (TOP VIEW) (outline dwgs JE, PE)  Note: pins 5 and 15 are internally connected.
ICL7641XCPD ICL7642XCPD	Quad op amps with internal compensation. I_Q fixed at 1mA (ICL7641) I_Q fixed at 10μA (ICL7642) Pin compatible with Texas Instr. TL084 National LM324 Harris HA4741	14 PIN DIP (TOP VIEW) (outline dwg JD, PD) 

Figure 1: Pin Configurations (Cont.)

Note: All typical values have been guaranteed by characterization and are not tested.

ICL76XX

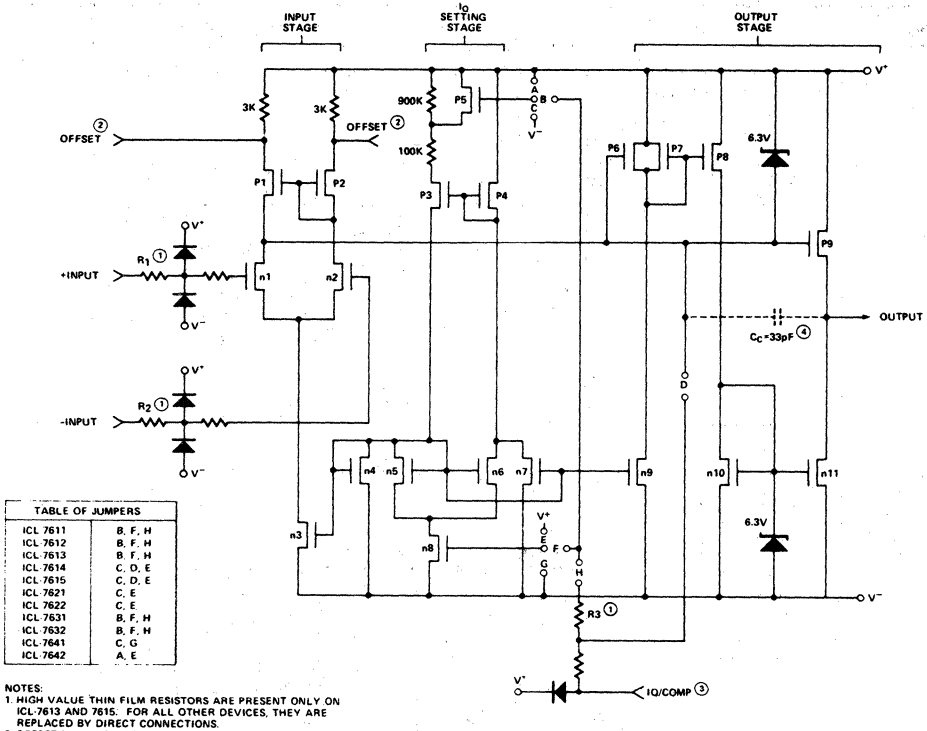


TABLE OF JUMPERS	
ICL 7611	B, F, H
ICL-7612	B, F, H
ICL-7613	B, F, H
ICL-7614	C, D, E
ICL-7615	C, D, E
ICL-7621	C, E
ICL 7622	C, E
ICL-7631	B, F, H
ICL 7632	B, F, H
ICL-7641	C, G
ICL-7642	A, E

NOTES:
1. HIGH VALUE THIN FILM RESISTORS ARE PRESENT ONLY ON ICL-7613 AND 7615. FOR ALL OTHER DEVICES, THEY ARE REPLACED BY DIRECT CONNECTIONS.
2. OFFSET NULLING PINS ARE NOT AVAILABLE ON TRIPLE (ICL-763X) AND QUAD (ICL-764X) VERSIONS.
3. I_Q AND COMP TERMINALS ARE METAL MASK OPTIONS OF THE SAME BONDING PAD; ONLY ONE OF THESE FUNCTIONS IS AVAILABLE IN A GIVEN DEVICE.
4. FOR INTERNALLY COMPENSATED VERSIONS ONLY. THIS CAPACITOR IS ABSENT FOR ALL OTHER DEVICES.

DS017301

Figure 2: Functional Diagram

Note: All typical values have been guaranteed by characterization and are not tested.

ICL76XX

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage V^+ to V^- 18V
Input Voltage .....V^- −0.3 to V^+ +0.3V
Input Voltage ICL7613/15 Only .....
V^- −200V to V^+ +200V
Differential Input Voltage[2] ...±[(V^+ +0.3) − (V^- −0.3)]V
Differential Input Voltage[2] ICL7613/15 Only .....
±[(V^+ +200) − (V^- −200)]V
Duration of Output Short Circuit[3] .....Unlimited

Continuous Power Dissipation

	@25°C	Above 25°C derate as below:
TO-99	250mW	2mW/°C
8 Lead Minidip	250mW	2mW/°C
14 Lead Plastic	375mW	3mW/°C
14 Lead Cerdip	500mW	4mW/°C
16 Lead Plastic	375mW	3mW/°C
16 Lead Cerdip	500mW	4mW/°C

Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range
M Series ..... −55°C to +125°C
C Series ..... 0°C to +70°C
Lead Temperature (Soldering, 10sec) .....300°C

Notes:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Long term offset voltage stability will be degraded if large input differential voltages are applied for long periods of time.
3. The outputs may be shorted to ground or to either supply. for $V_{SUPP} \leq 10V$. Care must be taken to insure that the dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS (761X and 762X ONLY)

($V_{SUPPLY} = \pm 5.0V$, $T_A = 25°C$, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	76XXA			76XXB			76XXD			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$R_S \leq 100k\Omega$, $T_A = 25°C$ $T_{MIN} \leq T_A \leq T_{MAX}$			2 3			5 7			15 20	mV
$\Delta V_{OS}/\Delta T$	Temperature Coefficient of V_{OS}	$R_S \leq 100k\Omega$		10			15			25		µV/°C
I_{OS}	Input Offset Current	$T_A = 25°C$ $\Delta T_A = C_{(2)}$ $\Delta T_A = M_{(2)}$		0.5	30 300 800		0.5	30 300 800		0.5	30 300 800	pA
I_{BIAS}	Input Bias Current	$T_A = 25°C$ $\Delta T_A = C$ $\Delta T_A = M$		1.0	50 400 4000		1.0	50 400 4000		1.0	50 400 4000	pA
V_{CMR}	Common Mode Voltage Range (Except ICL7612)	$I_Q = 10\mu A$(1) $I_Q = 100\mu A$ $I_Q = 1mA$(1)	±4.4 ±4.2 ±3.7			±4.4 ±4.2 ±3.7			±4.4 ±4.2 ±3.7			V
V_{CMR}	Extended Common Mode Voltage Range (!CL7612 Only)	$I_Q = 10\mu A$	±5.3			±5.3			±5.3			V
		$I_Q = 100\mu A$	+5.3 −5.1			+5.3 −5.1			+5.3 −5.1			
		$I_Q = 1mA$	+5.3 −4.5			+5.3 −4.5			+5.3 −4.5			
V_{OUT}	Output Voltage Swing	(1) $I_Q = 10\mu A$, $R_L = 1M\Omega$ $T_A = 25°C$ $\Delta T_A = C$ $\Delta T_A = M$	 ±4.9 ±4.8 ±4.7			 ±4.9 ±4.8 ±4.7			 ±4.9 ±4.8 ±4.7			V
		$I_Q = 100\mu A$, $R_L = 100k\Omega$ $T_A = 25°C$ $\Delta T_A = C$ $\Delta T_A = M$	 ±4.9 ±4.8 ±4.5			 ±4.9 ±4.8 ±4.5			 ±4.9 ±4.8 ±4.5			
		(1) $I_Q = 1mA$, $R_L = 10k\Omega$ $T_A = 25°C$ $\Delta T_A = C$ $\Delta T_A = M$	 ±4.5 ±4.3 ±4.0			 ±4.5 ±4.3 ±4.0			 ±4.5 ±4.3 ±4.0			

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Note: All typical values have been guaranteed by characterization and are not tested.

ICL76XX

ELECTRICAL CHARACTERISTICS (761X and 762X ONLY) (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	76XXA			76XXB			76XXD			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 4.0V$, $R_L = 1M\Omega$										
		$I_Q = 10\mu A^{(1)}$, $T_A = 25°C$	86	104		80	104		80	104		
		ΔT_A = C	80			75			75			
		ΔT_A = M	74			68			68			
		$V_O = \pm 4.0V$, $R_L = 100k\Omega$										
		$I_Q = 100\mu A$, $T_A = 25°C$	86	102		80	102		80	102		
		ΔT_A = C	80			75			75			dB
		ΔT_A = M	74			68			68			
		$V_O = \pm 4.0V$, $R_L = 10k\Omega$										
		$I_Q = 1mA^{(1)}$, $T_A = 25°C$	80	83		76	83		76	83		
		ΔT_A = C	76			72			72			
		ΔT_A = M	72			68			68			
GBW	Unity Gain Bandwidth	$I_Q = 10\mu A^{(1)}$		0.044			0.044			0.044		MHz
		$I_Q = 100\mu A$		0.48			0.48			0.48		
		$I_Q = 1mA^{(1)}$		1.4			1.4			1.4		
R_{IN}	Input Resistance			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common Mode Rejection Ratio	$R_S \leq 100k\Omega$, $I_Q = 10\mu A^{(1)}$	76	96		70	96		70	96		
		$R_S \leq 100k\Omega$, $I_Q = 100\mu A$	76	91		70	91		70	91		dB
		$R_S \leq 100k\Omega$, $I_Q = 1mA^{(1)}$	66	87		60	87		60	87		
PSRR	Power Supply Rejection Ratio	$R_S \leq 100k\Omega$, $I_Q = 10\mu A^{(1)}$	80	94		80	94		80	94		
		$R_S \leq 100k\Omega$, $I_Q = 100\mu A$	80	86		80	86		80	86		dB
		$R_S \leq 100k\Omega$, $I_Q = 1mA^{(1)}$	70	77		70	77		70	77		
e_n	Input Referred Noise Voltage	$R_S = 100\Omega$, f = 1kHz		100			100			100		$nV/\sqrt{Hz}$
i_n	Input Referred Noise Current	$R_S = 100\Omega$, f = 1kHz		0.01			0.01			0.01		$pA/\sqrt{Hz}$
I_{SUPPLY}	Supply Current (Per Amplifier)	No Signal, No Load										
		I_Q SET = +5V$^{(1)}$		0.01	0.02		0.01	0.02		0.01	0.02	
		I_Q SET = 0V		0.1	0.25		0.1	0.25		0.1	0.25	mA
		I_Q SET = −5V$^{(1)}$		1.0	2.5		1.0	2.5		1.0	2.5	
V_{O1}/V_{O2}	Channel Separation	A_{VOL} = 100		120			120			120		dB
SR	Slew Rate$^{(3)}$	A_{VOL} = 1, C_L = 100pF										
		V_{IN} = 8Vp-p										
		$I_Q = 10\mu A^{(1)}$, $R_L = 1M\Omega$		0.016			0.016			0.016		V/μs
		$I_Q = 100\mu A$, $R_L = 100k\Omega$		0.16			0.16			0.16		
		$I_Q = 1mA^{(1)}$, $R_L = 10k\Omega$		1.6			1.6			1.6		
t_r	Rise Time$^{(3)}$	V_{IN} = 50mV, C_L = 100pF										
		$I_Q = 10\mu A^{(1)}$, $R_L = 1M\Omega$		20			20			20		
		$I_Q = 100\mu A$, $R_L = 100k\Omega$		2			2			2		μs
		$I_Q = 1mA^{(1)}$, $R_L = 10k\Omega$		0.9			0.9			0.9		
	Overshoot Factor$^{(3)}$	V_{IN} = 50mV, C_L = 100pF										
		$I_Q = 10\mu A^{1}$, $R_L = 1M\Omega$		5			5			5		
		$I_Q = 100\mu A$, $R_L = 100k\Omega$		10			10			10		%
		$I_Q = 1mA^{1}$, $R_L = 10k\Omega$		40			40			40		

NOTES: 1. ICL7611, 7612, 7613 only. 2. C = Commercial Temperature Range: 0°C to +70°C
M = Military Temperature Range: −55°C to +125°C
3. ICL7614/15; 39pF from pin 6 to pin.

ELECTRICAL CHARACTERISTICS (761X AND 762X ONLY)

($V_{SUPPLY} = \pm 1.0V$, $I_Q = 10\mu A$, $T_A = 25°C$, unless otherwise specified. Specs apply to ICL7611/7612/7613 only.)

SYMBOL	PARAMETER	TEST CONDITIONS	76XXA			76XXB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$R_S \leq 100k\Omega$, $T_A = 25°C$			2			5	mV
		$T_{MIN} \leq T_A \leq T_{MAX}$			3			7	
$\Delta V_{OS}/\Delta T$	Temperature Coefficient of V_{OS}	$R_S \leq 100k\Omega$		10			15		μV/°C

Note: All typical values have been guaranteed by characterization and are not tested.

ELECTRICAL CHARACTERISTICS (761X AND 762X ONLY) (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	76XXA			76XXB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{OS}	Input Offset Current	$T_A = 25°C$ $\Delta T_A = C$		0.5	30 300		0.5	30 300	pA
I_{BIAS}	Input Bias Current	$T_A = 25°C$ $\Delta T_A = C$		1.0	50 500		1.0	50 500	pA
V_{CMR}	Common Mode Voltage Range (Except ICL7612)		±0.6			±0.6			V
V_{CMR}	Extended Common Mode Voltage Range (ICL7612 Only)		+0.6 to −1.1			+0.6 to −1.1			V
V_{OUT}	Output Voltage Swing	$R_L = 1M\Omega$, $T_A = 25°C$ $\Delta T_A = C$		±0.98 ±0.96			±0.98 ±0.96		V
A_{VOL}	Large Signal Voltage Gain	$V_O = ±0.1V$, $R_L = 1M\Omega$ $T_A = 25°C$ $\Delta T_A = C$		90 80			90 80		dB
GBW	Unity Gain Bandwidth			0.044			MHz		
R_{IN}	Input Resistance			10^{12}			10^{12}		
CMRR	Common Mode Rejection Ratio	$R_S \leq 100k\Omega$		80			80		
PSRR	Power Supply Rejection Ratio	$R_S \leq 100k\Omega$		80			80		dB
e_n	Input Referred Noise Voltage	$R_S = 100\Omega$, f = 1kHz		100			100		$nV/\sqrt{Hz}$
i_n	Input Referred Noise Current	$R_S = 100\Omega$, f = 1kHz		0.01			0.01		$pA/\sqrt{Hz}$
I_{SUPPLY}	Supply Current (Per Amplifier)	No Signal, No Load		6	15		6	15	μA
SR	Slew Rate	$A_{VOL} = 1$, $C_L = 100pF$ $V_{IN} = 0.2Vp\text{-}p$ $R_L = 1M\Omega$		0.016			0.016		V/μs
t_r	Rise Time	$V_{IN} = 50mV$, $C_L = 100pF$ $R_L = 1M\Omega$		20			20		μs
	Overshoot Factor	$V_{IN} = 50mV$, $C_L = 100pF$ $R_L = 1M\Omega$		5			5		%

NOTE: C = Commercial Temperature Range (0°C to +70°C) M = Military Temperature Range (−55°C to +125°C).

ELECTRICAL CHARACTERISTICS (763X, 764X ONLY)

($V_{SUPPLY} = ±5.0V$, $T_A = 25°C$, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	76XXC (6)			76XXE (6)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$R_S \leq 100k\Omega$, $T_A = 25°C$ $T_{MIN} \leq T_A \leq T_{MAX}$			10 15			20 25	mV
$\Delta V_{OS}/\Delta T$	Temperature Coefficient of V_{OS}	$R_S \leq 100k\Omega$ (Note 5)		20			30		
I_{OS}	Input Offset Current	$T_A = 25°C$ $\Delta T_A = C$ $\Delta T_A = M$		0.5	30 300 800		0.5	30 300 800	pA
I_{BIAS}	Input Bias Current	$T_A = 25°C$ $\Delta T_A = C$ $\Delta T_A = M$		1.0	50 500 4000		1.0	50 500 4000	pA
V_{CMR}	Common Mode Voltage Range	$I_Q = 10\mu A$(1) $I_Q = 100\mu A$(3) $I_Q = 1mA$(2)	±4.4 ±4.2 ±3.7			±4.4 ±4.2 ±3.7			V

Note: All typical values have been guaranteed by characterization and are not tested.

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ELECTRICAL CHARACTERISTICS (763X, 764X ONLY) (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	76XXC (6)			76XXE (6)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OUT}	Output Voltage Swing	(1) I_Q = 10μA, R_L = 1MΩ							
		T_A = 25°C	±4.9			±4.9			
		ΔT_A = C	±4.8			±4.8			
		ΔT_A = M	±4.7			±4.7			
		I_Q = 100μA, R_L = 100kΩ							
		(3) T_A = 25°C	±4.9			±4.9			V
		ΔT_A = C	±4.8			±4.8			
		ΔT_A = M	±4.5			±4.5			
		(2) I_Q = 1mA, R_L = 10kΩ							
		T_A = 25°C	±4.5			±4.5			
		ΔT_A = C	±4.3			±4.3			
		ΔT_A = M	±4.0			±4.0			
A_{VOL}	Large Signal Voltage Gain	V_O = ±4.0V, R_L = 1MΩ(1)							
		I_Q = 10μA(1), T_A = 25°C	80	104		80	104		
		ΔT_A = C	75			75			
		ΔT_A = M	68			68			
		V_O = ±4.0V, R_L = 100kΩ(3)							
		I_Q = 100μA, T_A = 25°C	80	102		80	102		
		ΔT_A = C	75			75			
		ΔT_A = M	68			68			dB
		V_O = ±4.0V, R_L = 10kΩ(2)							
		I_Q = 1mA(1), T_A = 25°C	80	98		80	98		
		ΔT_A = C	75			75			
		ΔT_A = M	68			68			
GBW	Unity Gain Bandwidth	I_Q = 10μA(1)		0.044			0.044		MHz
		I_Q = 100μA(3)		0.48			0.48		
		I_Q = 1mA(2)		1.4			1.4		
R_{IN}	Input Resistance		10^{12}			10^{12}		Ω	
CMRR	Common Mode Rejection Ratio	R_S ≤ 100kΩ, I_Q = 10μA(1)	70	96		70	96		
		R_S ≤ 100kΩ, I_Q = 100μA	70	91		70	91		dB
		R_S ≤ 100kΩ, I_Q = 1mA(2)	60	87		60	87		
PSRR	Power Supply Rejection Ratio	R_S ≤ 100kΩ, I_Q = 10μA(1)	80	94		80	94		
		R_S ≤ 100kΩ, I_Q = 100μA	80	86		80	86		dB
		R_S ≤ 100kΩ, I_Q = 1mA(2)	70	77		70	77		
e_n	Input Referred Noise Voltage	R_S = 100Ω, f = 1kHz		100			100		nV/√Hz
I_n	Input Referred Noise Current	R_S = 100Ω, f = 1kHz		0.01			0.01		pA/√Hz
I_{SUPPLY}	Supply Current (Per Amplifier)	No Signal, No Load		0.01	0.03		0.01	0.03	
		7642 ONLY							
		I_Q = 10μA(1)		0.01	0.022		0.01	0.022	
		I_Q = 100μA		0.1	0.25		0.1	0.25	mA
		I_Q = 1mA(2)		1.0	2.5		1.0	2.5	
V_{O1}/V_{O2}	Channel Separation	A_{VOL} = 100		120			120		dB
SR	Slew Rate(4)	A_{VOL} = 1, C_L = 100pF							
		V_{IN} = 8Vp-p							
		I_Q = 10μA(1), R_L = 1MΩ		0.016			0.016		V/μs
		I_Q = 100μA, R_L = 100kΩ		0.16			0.16		
		I_Q = 1mA(1), R_L = 10kΩ(2)		1.6			1.6		
t_r	Rise Time(4)	V_{IN} = 50mV, C_L = 100pF							
		I_Q = 10μA(1), R_L = 1MΩ		20			20		μs
		I_Q = 100μA, R_L = 100kΩ		2			2		
		I_Q = 1mA(2), R_L = 10kΩ		0.9			0.9		

Note: All typical values have been guaranteed by characterization and are not tested.

ELECTRICAL CHARACTERISTICS (763X, 764X ONLY) (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	76XXC (6)			76XXE (6)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	Overshoot Factor(4)	V_{IN} = 50mV, C_L = 100pF I_Q = 10μA(1), R_L = 1MΩ I_Q = 100μA, R_L = 100kΩ I_Q = 1mA(2), R_L = 10kΩ		5 10 40			5 10 40		%

NOTES:
1. Does not apply to 7641.
2. Does not apply to 7642.
3. ICL7631/32 only.
4. Does not apply to 7632.

For Test Conditions:
C = Commercial Temperature Range: 0°C to +70°C
M = Military Temperature Range: −55°C to +125°C

ELECTRICAL CHARACTERISTICS (763X AND 764X ONLY)

(V_{SUPPLY} = ±1.0V, I_Q = 10μA, T_A = 25°C, unless otherwise specified. Specs apply to ICL7631/7632/7642 only.)

SYMBOL	PARAMETER	TEST CONDITIONS	76XXC			UNIT
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$R_S \leq 100k\Omega$, T_A = 25°C $T_{MIN} \leq T_A \leq T_{MAX}$			10 12	mV
$\Delta V_{OS}/\Delta T$	Temperature Coefficient of V_{OS}	$R_S \leq 100k\Omega$		20		μV/°C
I_{OS}	Input Offset Current	T_A = 25°C ΔT_A = C		0.5	30 300	pA
I_{BIAS}	Input Bias Current	T_A = 25°C ΔT_A = C		1.0	50 500	pA
V_{CMR}	Common Mode Voltage Range		±0.6			V
V_{OUT}	Output Voltage Swing	R_L = 1MΩ, T_A = 25°C ΔT_A = C		±0.98 ±0.96		V
A_{VOL}	Large Signal Voltage Gain	V_O = ±0.1V, R_L = 1MΩ T_A = 25°C ΔT_A = C		90 80		dB
GBW	Unity Gain Bandwidth		0.044			MHz
R_{IN}	Input Resistance		10^{12}			Ω
CMRR	Common Mode Rejection Ratio	$R_S \leq 100k\Omega$		80		dB
PSRR	Power Supply Rejection Ratio		80			dB
e_n	Input Referred Noise Voltage	R_S = 100Ω, f = 1kHz		100		$nV/\sqrt{Hz}$
i_n	Input Referred Noise Current	R_S = 100Ω, f = 1kHz		0.01		$pA/\sqrt{Hz}$
I_{SUPPLY}	Supply Current (Per Amplifier)	No Signal, No Load		6	15	μA
V_{O1}/V_{O2}	Channel Separation	A_{VOL} = 100		120		dB
SR	Slew Rate	A_{VOL} = 1, C_L = 100pF V_{IN} = 0.2Vp-p R_L = 1MΩ		0.016		V/μs
t_r	Rise Time	V_{IN} = 50mV, C_L = 100pF R_L = 1MΩ		20		μs
	Overshoot Factor	V_{IN} = 50mV, C_L = 100pF R_L = 1MΩ		5		%

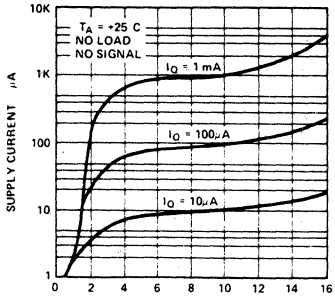
NOTE: C = Commercial Temperature Range (0°C to +70°C)

Note: All typical values have been guaranteed by characterization and are not tested.

ICL76XX

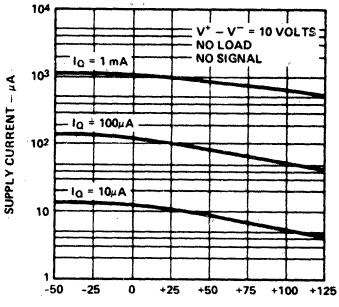
TYPICAL PERFORMANCE CHARACTERISTICS

SUPPLY CURRENT PER AMPLIFIER AS A FUNCTION OF SUPPLY VOLTAGE



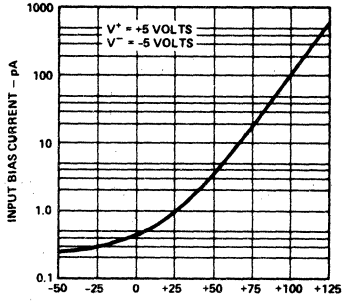
OP01630I

SUPPLY CURRENT PER AMPLIFIER AS A FUNCTION OF FREE-AIR TEMPERATURE



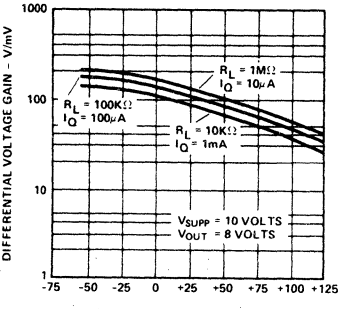
OP01640I

INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE



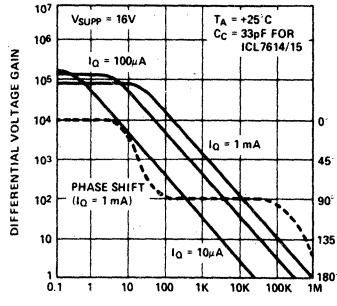
OP01650I

LARGE SIGNAL DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF FREE-AIR TEMPERATURE



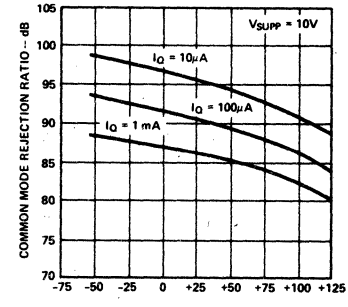
OP01660I

LARGE SIGNAL DIFFERENTIAL VOLTAGE GAIN AND PHASE SHIFT AS A FUNCTION OF FREQUENCY



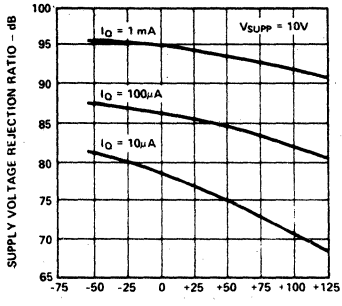
OP01670I

COMMON MODE REJECTION RATIO AS A FUNCTION OF FREE-AIR TEMPERATURE



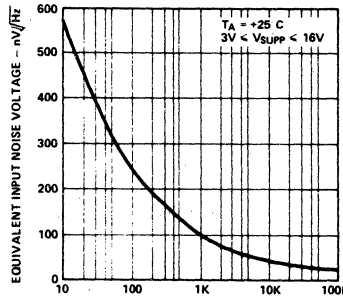
OP01680I

POWER SUPPLY REJECTION RATIO AS A FUNCTION OF FREE-AIR TEMPERATURE



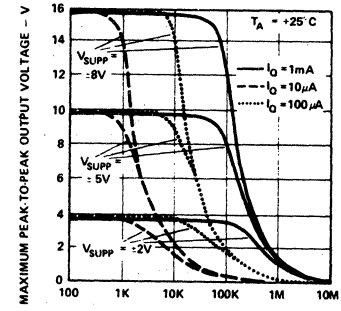
OP01690I

EQUIVALENT INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



OP01700I

PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF FREQUENCY

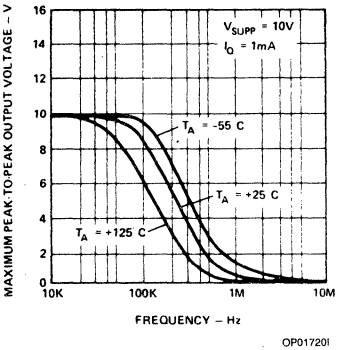


OP01710I

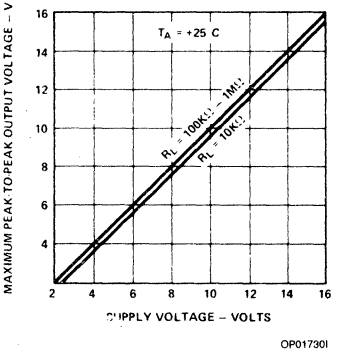
Note: All typical values have been guaranteed by characterization and are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

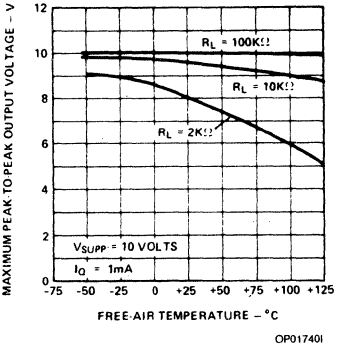
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF FREQUENCY



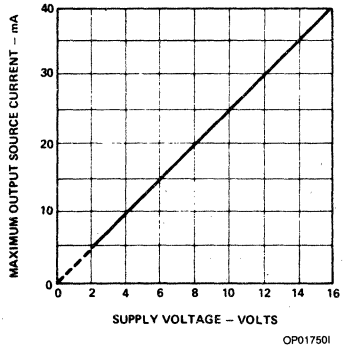
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



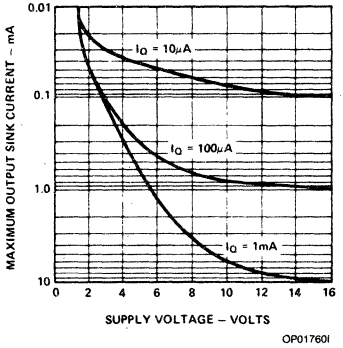
MAXIMUM PEAK-TO-PEAK VOLTAGE AS A FUNCTION OF FREE-AIR TEMPERATURE



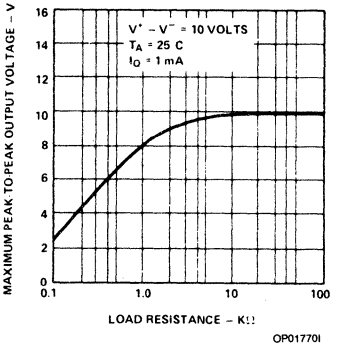
MAXIMUM OUTPUT/SOURCE CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



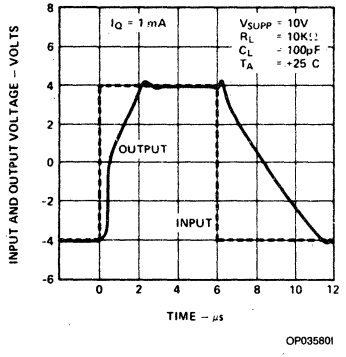
MAXIMUM OUTPUT SINK CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



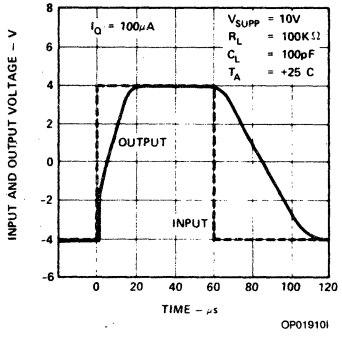
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF LOAD RESISTANCE



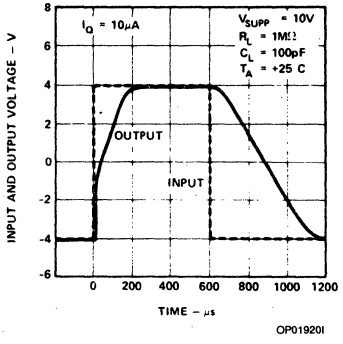
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



Note: All typical values have been guaranteed by characterization and are not tested.

DETAILED DESCRIPTION

Static Protection

All devices are static protected by the use of input diodes. However, strong static fields should be avoided, as it is possible for the strong fields to cause degraded diode junction characteristics, which may result in increased input leakage currents.

Latchup Avoidance

Junction-isolated CMOS circuits employ configurations which produce a parasitic 4-layer (p-n-p-n) structure. The 4-layer structure has characteristics similar to an SCR, and under certain circumstances may be triggered into a low impedance state resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails may be applied to any pin. (An exception to this rule concerns the inputs of the ICL7613 and ICL7615, which are protected to ±200V.) In general, the op-amp supplies must be established simultaneously with, or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to 2mA to prevent latchup.

Choosing the Proper I_Q

Each device in the ICL76XX family has a similar I_Q set-up scheme, which allows the amplifier to be set to nominal quiescent currents to 10μA, 100μA or 1mA. These current settings change only very slightly over the entire supply voltage range. The ICL7611/12/13 and ICL7631/32 have an external I_Q control terminal, permitting user selection of each amplifiers' quiescent current. (The ICL7614/15, 7621/22, and 7641/42 have fixed I_Q settings — refer to selector guide for details.) To set the I_Q of programmable versions, connect the I_Q terminal as follows:

I_Q = 10μA — I_Q pin to V^+

I_Q = 100μA — I_Q pin to ground. If this is not possible, any voltage from V^+ −0.8 to V^- +0.8 can be used.

I_Q = 1mA — I_Q pin to V^-

NOTE: The negative output current available is a function of the quiescent current setting. For maximum p-p output voltage swings into low impedance loads, I_Q of 1mA should be selected.

Output Stage and Load Driving Considerations

Each amplifiers' quiescent current flows primarily in the output stage. This is approximately 70% of the I_Q settings. This allows output swings to almost the supply rails for output loads of 1MΩ, 100kΩ, and 10kΩ, using the output stage in a highly linear class A mode. In this mode, crossover distortion is avoided and the voltage gain is maximized. However, the output stage can also be operated in Class AB for higher output currents. (See graphs under Typical Operating Characteristics). During the transition from Class A to Class B operation, the output transfer characteristic is non-linear and the voltage gain decreases.

A special feature of the output stage is that it approximates a transconductance amplifier, and its gain is directly proportional to load impedance. Approximately the same open loop gains are obtained at each of the I_Q settings if corresponding loads of 10kΩ, 100kΩ, and 1MΩ are used.

Input Offset Nulling

For those models provided with OFFSET NULLING pins, nulling may be achieved by connecting a 25K pot between the OFFSET terminals with the wiper connected to V^+. At quiescent currents of 1mA and 100μA, the nulling range provided is adequate for all V_{OS} selections; however with I_Q = 10μA, nulling may not be possible with higher values of V_{OS}.

Frequency Compensation

The ICL7611/12/13, 7621/22, 7631, 7641/42 are internally compensated, and are stable for closed loop gains as low as unity with capacitive loads up to 100pF

The ICL7614/15 are externally compensated by connecting a capacitor between the COMP and OUT pins. A 39pF capacitor is required for unity gain compensation; for greater than unity gain applications, increased bandwidth and slew rate can be obtained by reducing the value of the compensating capacitor. Since the g_m of the first stage is proportional to $\sqrt{I_Q}$, greatest compensation is required when I_Q=1mA.

The ICL7632 is not compensated internally, nor can it be compensated externally. The device is stable when used as follows:

I_Q of 1mA for gains ≥ 20
I_Q of 100μA for gains ≥ 10
I_Q of 10μA for gains ≥ 5

High Voltage Input Protection

The ICL7613 and 7615 include on-chip thin film resistors and clamping diodes which allow voltages of up to ±200V to be applied to either input for an indefinite time without device failure. These devices will be useful where high common mode voltages, differential mode voltages, or high transients may be experienced. Such conditions may be found when interfacing separate systems with separate supplies. Unity gain stability is somewhat degraded with capacitive loads because of the high value of input resistors.

Extended Common Mode Input Range

The ICL7612 incorporates additional processing which allows the input CMVR to exceed each power supply rail by 0.1 volt for applications where $V_{SUPP} \geq \pm 1.5V$. For those applications where $V_{SUPP} \leq \pm 1.5V$, the input CMVR is limited in the positive direction, but may exceed the negative supply rail by 0.1 volt in the negative direction (eg. for $V_{SUPP} = \pm 1.0V$, the input CMVR would be +0.6 volts to −1.1 volts).

OPERATION AT $V_{SUPP} = \pm 1.0$ VOLTS

Operation at $V_{SUPP} = \pm 1.0V$ is guaranteed at I_Q = 10μA only. This applies to those devices with selectable I_Q, and devices that are set internally to I_Q = 10μA (i.e., ICL7611, 7612, 7613, 7631, 7632, 7642).

Output swings to within a few millivolts of the supply rails are achievable for $R_L \geq 1M\Omega$. Guaranteed input CMVR is ±0.6V minimum and typically +0.9V to −0.7V at $V_{SUPP} = \pm 1.0V$. For applications where greater common mode range is desirable, refer to the description of ICL7612 above.

The user is cautioned that, due to extremely high input impedances, care must be exercised in layout, construction,

Note: All typical values have been guaranteed by characterization and are not tested.

board cleanliness, and supply filtering to avoid hum and noise pickup.

APPLICATIONS

Note that in no case is I_Q shown. The value of I_Q must be chosen by the designer with regard to frequency response and power dissipation.

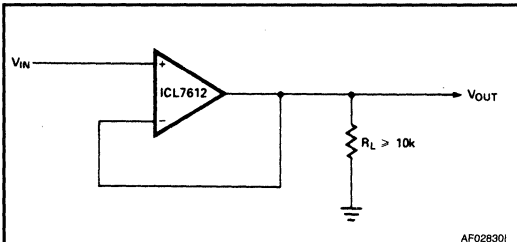
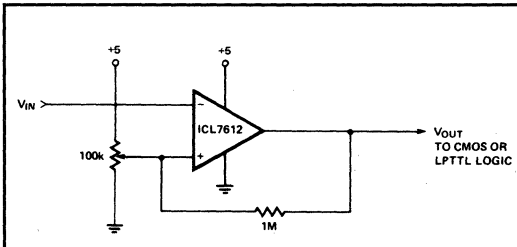
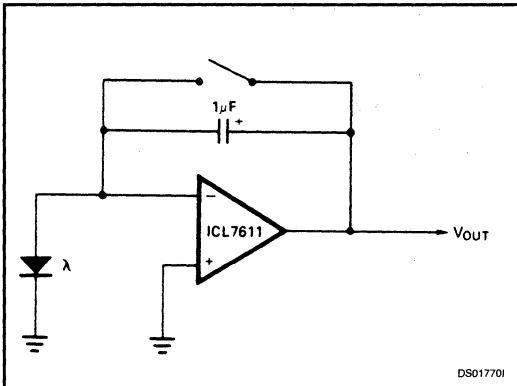


Figure 3: Simple Follower*



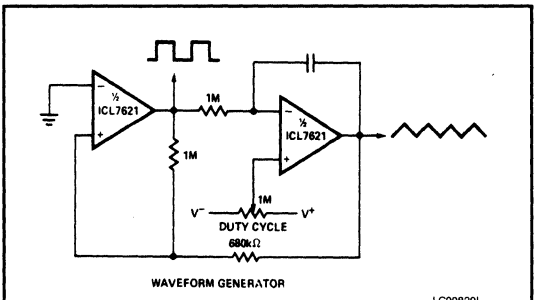
*By using the ICL7612 in these applications, the circuits will follow rail to rail inputs.

Figure 4: Level Detector*



*Low leakage currents allow integration times up to several hours.

Figure 5: Photocurrent Integrator



Since the output range swings exactly from rail to rail, frequently and duty cycle are virtually independent of power supply variations.

Figure 6: Precise Triangle/Square Wave Generator

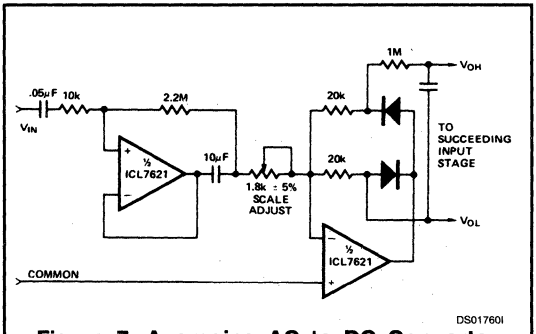
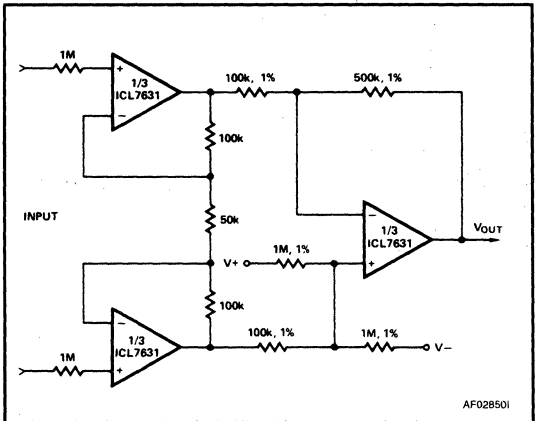


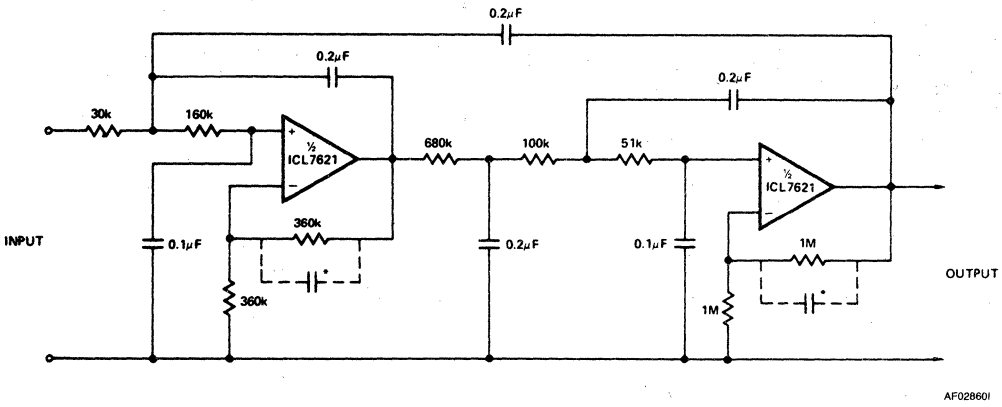
Figure 7: Averaging AC to DC Converter for A/D Converters Such as ICL7106, 7107, 7109, 7116, 7117



Note that A_{VOL} = 25; single Ni-cad battery operation. Input current (from sensors connected to patient) limited to < 5μA under fault conditions.

Figure 8: Medical Instrument Preamp

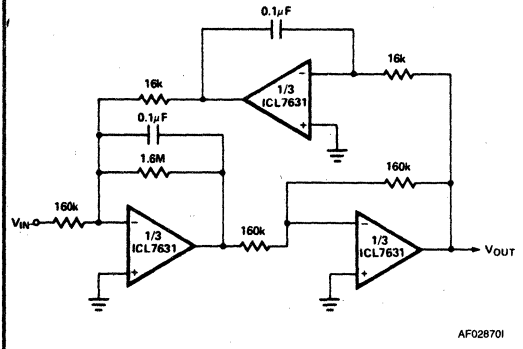
Note: All typical values have been guaranteed by characterization and are not tested.



The low bias currents permit high resistance and low capacitance values to be used to achieve low frequency cutoff. f_C = 10Hz, A_{VCL} = 4, Passband ripple = 0.1dB

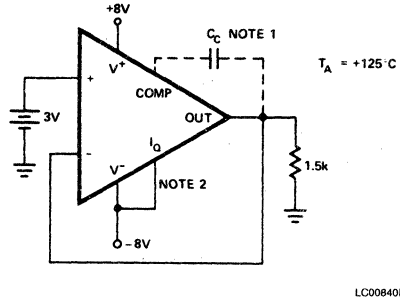
*Note that small capacitors (25–50pF) may be needed for stability in some cases.

Figure 9: Fifth Order Chebyshev Multiple Feedback Low Pass Filter



Note that I_Q on each amplifier may be different. A_{VCL} = 10, Q = 100, f_O = 100Hz.

Figure 10: Second Order Biquad Bandpass Filter

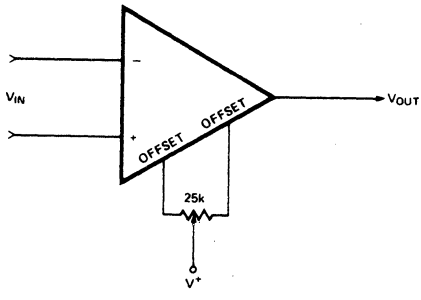


NOTES:

1. For devices with external compensation, use 33pF.
2. For devices with programmable standby current, connect I_Q pin to V^- (I_Q = 1mA mode).

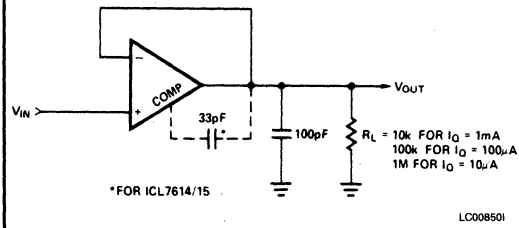
Figure 11: Burn-In and Life Test Circuit

Note: All typical values have been guaranteed by characterization and are not tested.



LC008301

Figure 12: V_{OS} Null Circuit



LC008501

Figure 13: Unity Gain Frequency Compensation

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7650
Chopper-Stabilized Operational Amplifier

GENERAL DESCRIPTION

The ICL7650 chopper-stabilized amplifier is a high-performance device which offers exceptionally low offset voltage and input-bias parameters, combined with excellent bandwidth and speed characteristics. Intersil's unique CMOS approach to chopper-stabilized amplifier design yields a versatile precision component that can replace more expensive hybrid or monolithic devices.

The chopper amplifier achieves its low offset by comparing the inverting and non-inverting input voltages in a nulling amplifier, nulled by alternate clock phases. Two external capacitors are required to store the correcting potentials on the two amplifier nulling inputs; these are the only external components necessary.

The clock oscillator and all the other control circuitry is entirely self-contained, however the 14-pin version includes a provision for the use of an external clock, if required for a particular application. In addition, the ICL7650 is internally compensated for unity-gain operation.

FEATURES

- **Extremely Low Input Offset Voltage — 2μV**
- **Low Long-Term and Temperature Drifts of Input Offset Voltage**
- **Low DC Input Bias Current — 10pA (20pA 7650B)**
- **Extremely High Gain, CMRR and PSRR — Min 120dB**
- **High Slew Rate — 2.5V/μs**
- **Wide Bandwidth — 2MHz**
- **Unity-Gain Compensated**
- **Very Low Intermodulation Effects (Open Loop Phase Shift < 10°C @ Chopper Frequency)**
- **Clamp Circuit to Avoid Overload Recovery Problems and Allow Comparator Use**
- **Extremely Low Chopping Spikes at Input and Output**

ORDERING INFORMATION

PART	TEMPERATURE RANGE	PACKAGE
ICL7650CPA-1	0°C to +70°C	8-PIN Plastic
ICL7650BCPA-1	0°C to +70°C	8-PIN Plastic
ICL7650CPD	0°C to +70°C	14-PIN Plastic
ICL7650BCPD	0°C to +70°C	14-PIN Plastic
ICL7650CTV-1	0°C to +70°C	8-PIN TO-99
ICL7650BCTV-1	0°C to +70°C	8-PIN TO-99
ICL7650IJA-1	−25°C to +85°C	8-PIN CERDIP
ICL7650BIJA-1	−25°C to +85°C	8-PIN CERDIP

PART	TEMPERATURE RANGE	PACKAGE
ICL7650IJD	−25°C to +85°C	14-PIN CERDIP
ICL7650BIJD	−25°C to +85°C	14-PIN CERDIP
ICL7650ITV-1	−25°C to +85°C	8-PIN TO-99
ICL7650BITV-1	−25°C to +85°C	8-PIN TO-99
ICL7650MJD	−55°C to +125°C	14-PIN CERDIP
ICL7650BMJD	−55°C to +125°C	14-PIN CERDIP
ICL7650MTV-1	−55°C to +125°C	8-PIN TO-99
ICL7650BMTV-1	−55°C to +125°C	8-PIN TO-99

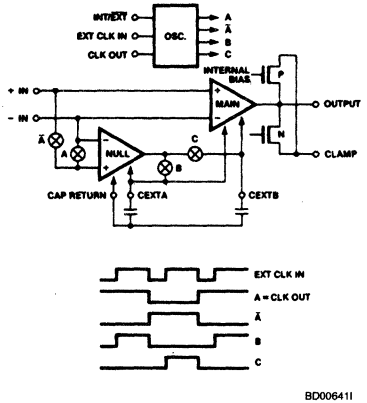


Figure 1: Functional Diagram

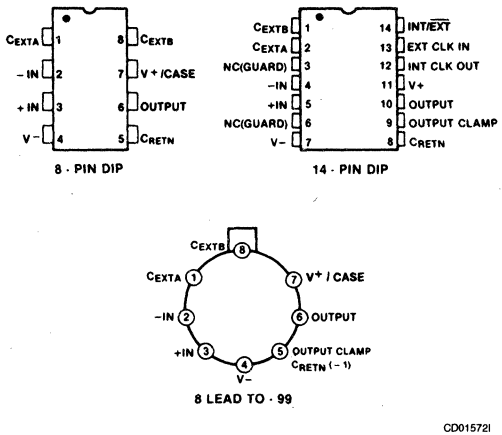


Figure 2: Pin Configuration

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7650

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) ..... 18 Volts
Input Voltage ..... ($V^+ + 0.3$) to ($V^- - 0.3$) Volts
Voltage on oscillator control pins ..... V^+ to V^-
except EXT CLOCK IN: ... ($V^+ + 0.3$) to ($V^+ - 6.0$) Volts
Duration of Output short circuit ..... Indefinite
Current into any pin 10mA
—while operating (Note 4) 100μA

Cont. Total Power Dissipn ($T_A = 25°C$)
CERDIP Package 500mW
Plastic Package 375mW
TO-99 ..... 250mW
Storage Temp. Range ..... −65°C to 150°C
Operating Temp. Range ..... See Note 1
Lead Temperature (Soldering, 10sec) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +5V$, $V^- = -5V$, $T_A = +25°C$, (unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS 7650			LIMITS 7650B			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$T_A = +25°C$ $-25°C < T_A < +85°C$ $-55°C < T_A < +125°C$		±2 ±5	±5 ±50		±2 ±5	±10.0 ±75	μV
$\frac{\Delta V_{OS}}{\Delta T}$	Average Temp. Coefficient of Input Offset Voltage	$-25°C < T_A < +85°C$		0.1			0.1		μV/°C
$\frac{\Delta V_{OS}}{\Delta t}$	Change in Input Offset Voltage With Time			100			100		nV/month
I_{BIAS}	Input Bias Current (doubles every 10°C) Polarity is + or − (Note 5)	$T_A = +25°C$ $0°C < T_A < +70°C$ $-25°C < T_A < +85°C$		±1.5 ±35 ±100	±10		±1.5 ±35 ±100	±20	pA
I_{OS}	Input Offset Current (Note 5)	$T_A = 25°C$		5.0			5.0		pA
R_{IN}	Input Resistance			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$R_L = 10kΩ$	$1x10^6$	$5x10^6$		$1x10^6$	$5x10^6$		V/V
V_{OUT}	Output Voltage Swing (Note 3)	$R_L = 10kΩ$ $R_L = 100kΩ$	±4.7	±4.85 ±4.95		±4.7	±4.85 ±4.95		V
CMVR	Common Mode Voltage Range		−5.0	−5.2 to +2.0	1.5	−5.0	−5.2 to +2.0	1.5	V
CMRR	Common Mode Rejection Ratio	CMVR = −5V to +1.5	110	120		110	120		dB
PSRR	Power Supply Rejection Ratio	±3V to ±8V	120	130		120	130		dB
e_n	Input Noise Voltage	$R_S = 100Ω$ f = 0 to 10Hz		2			2		$μV_{p-p}$
i_n	Input Noise Current	f = 10Hz		0.01			0.01		$pA/\sqrt{Hz}$
GBW	Unity Gain Bandwidth			2.0			2.0		MHz
SR	Slew Rate	$C_L = 50pF$, $R_L = 10kΩ$		2.5			2.5		V/μs
t_r	Rise Time			0.2			0.2		μs
	Overshoot			20			20		%
V+ to V−	Operating Supply Range		4.5		16	4.5		16	V
I_{SUPP}	Supply Current	no load		2.0	3.5		2.0	3.5	mA
f_{ch}	Internal Chopping Frequency	pins 12-14 open (DIP)	120	200	375	120	200	375	Hz
	Clamp ON Current (note 2)	$R_L = 100kΩ$	25	70	150	25	70	150	μA
	Clamp OFF Current (note 2)	$-4.0V < V_{OUT} < +4.0V$		1			1		pA

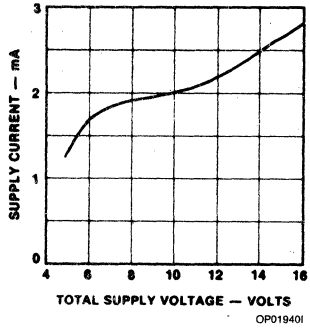
NOTES: 1. Operating temperature range for M series parts is −55°C to +125°C, for I series is −25°C to +85°C, for C series is 0°C to +70°C
2. See OUTPUT CLAMP under detailed description.
3. OUTPUT CLAMP not connected. See typical characteristic curves for output swing vs clamp current characteristics.
4. Limiting input current to 100μA is recommended to avoid latchup problems. Typically 1mA is safe, however this is not guaranteed.
5. $I_{OS} = 2 \bullet I_{BIAS}$

Note: All typical values have been guaranteed by characterization and are not tested.

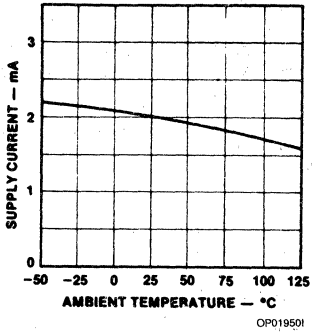
ICL7650

TYPICAL PERFORMANCE CHARACTERISTICS

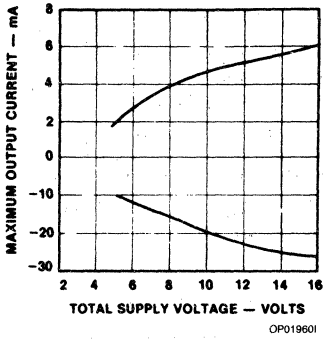
SUPPLY CURRENT vs. SUPPLY VOLTAGE



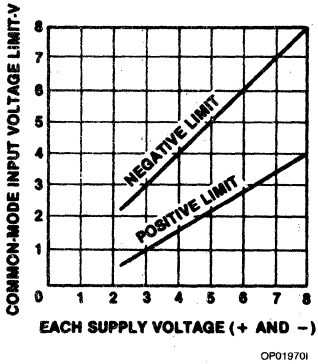
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



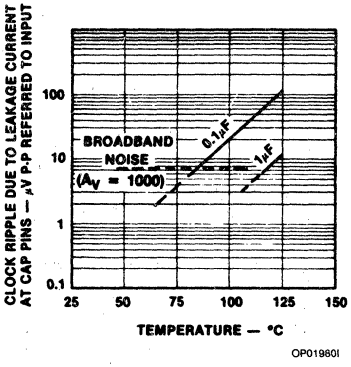
MAXIMUM OUTPUT CURRENT vs. SUPPLY VOLTAGE



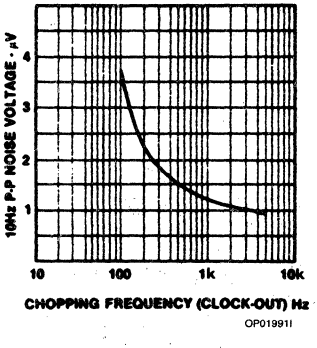
COMMON-MODE INPUT-VOLTAGE RANGE vs SUPPLY VOLTAGE



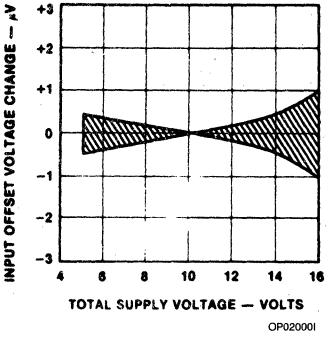
CLOCK RIPPLE REFERRED TO THE INPUT vs. TEMPERATURE



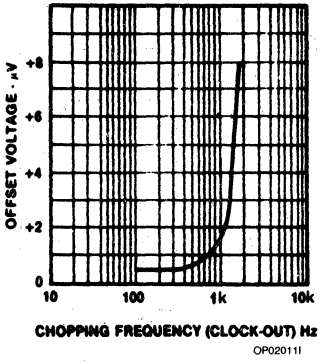
10Hz P-P NOISE VOLTAGE vs. CHOPPING FREQUENCY



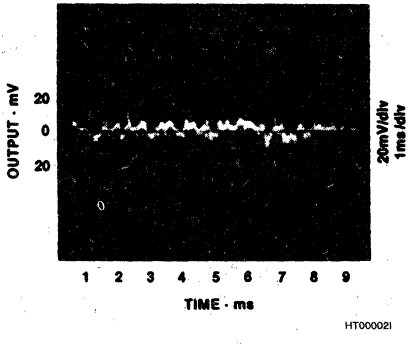
INPUT OFFSET VOLTAGE CHANGE vs. SUPPLY VOLTAGE



INPUT OFFSET VOLTAGE vs. CHOPPING FREQUENCY



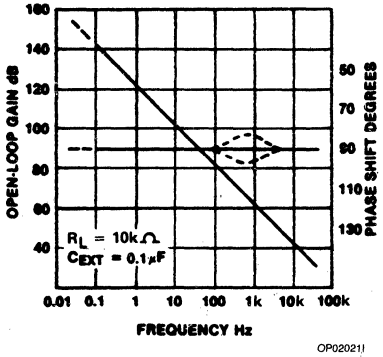
OUTPUT WITH ZERO INPUT; GAIN = 1000; BALANCED SOURCE IMPEDANCE = 10KΩ



Note: All typical values have been guaranteed by characterization and are not tested.

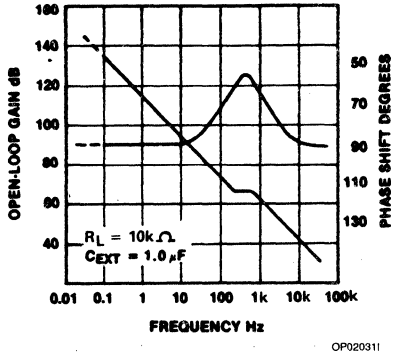
TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

OPEN LOOP GAIN AND PHASE SHIFT vs. FREQUENCY



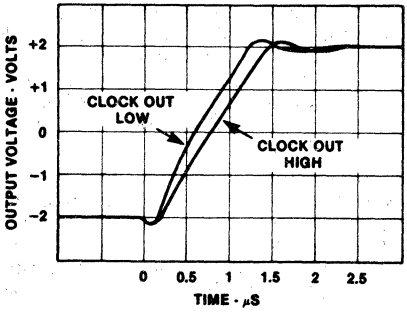
OP02021I

OPEN LOOP GAIN AND PHASE SHIFT vs. FREQUENCY



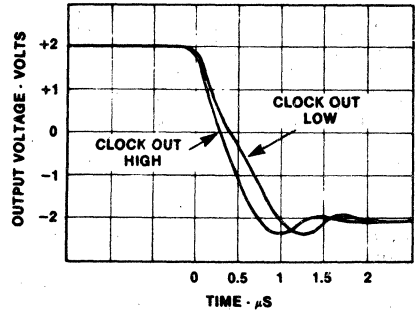
OP02031I

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE*



OP02040I

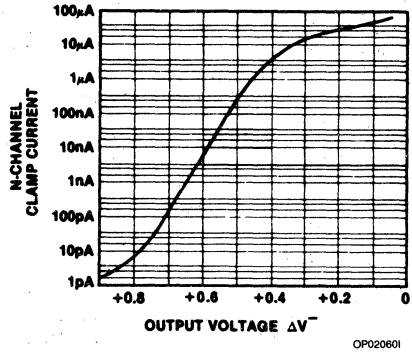
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE*



OP02050I

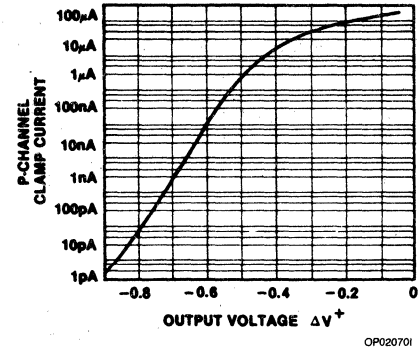
* THE TWO DIFFERENT RESPONSES CORRESPOND TO THE TWO PHASES OF THE CLOCK.

N-CHANNEL CLAMP CURRENT vs. OUTPUT VOLTAGE



OP02060I

P-CHANNEL CLAMP CURRENT vs. OUTPUT VOLTAGE



OP02070I

4

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7650

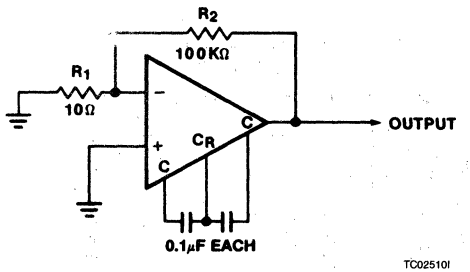


Figure 3: ICL7650/B Test Circuit

DETAILED DESCRIPTION

Amplifier

The functional diagram shows the major elements of the ICL7650. There are two amplifiers, the main amplifier, and the nulling amplifier. Both have offset-null capability. The main amplifier is connected continuously from the input to the output, while the nulling amplifier, under the control of the chopping oscillator and clock circuit, alternately nulls itself and the main amplifier. The nulling connections, which are MOSFET gates, are inherently high impedance, and two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants. The nulling arrangement operates over the full common-mode and power-supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and A_{VOL}.

Careful balancing of the input switches, and the inherent balance of the input circuit, minimizes chopper frequency charge injection at the input terminals, and also the feedforward-type injection into the compensation capacitor, which is the main cause of output spikes in this type of circuit.

Intermodulation

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite AC gain of the amplifier necessitates a small AC signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies and causing disturbances to the gain and phase vs. frequency characteristics near the chopping frequency. These effects are substantially reduced in the ICL7650 by feeding the nulling circuit with a dynamic current, corresponding to the compensation capacitor current, in such a way as to cancel that portion of the input signal due to finite AC gain. Since that is the major error contribution to the ICL7650, the intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

Capacitor Connection

The null/storage capacitors should be connected to the C_{EXTA} and C_{EXTB} pins, with a common connection to the C_{RETN} pin. This connection should be made directly by either a separate wire or PC trace to avoid injecting load current IR drops into the capacitive circuitry. The outside foil, where available, should be connected to C_{RETN}.

Output Clamp

The OUTPUT CLAMP pin allows reduction of the overload recovery time inherent with chopper-stabilized amplifiers. When tied to the inverting input pin, or summing junction, a current path between this point and the OUTPUT pin occurs just before the device output saturates. Thus uncontrolled input differential inputs are avoided, together with the consequent charge build-up on the correction-storage capacitors. The output swing is slightly reduced.

Clock

The ICL7650 has an internal oscillator giving a chopping frequency of 200Hz, available at the CLOCK OUT pin on the 14-pin devices. Provision has also been made for the use of an external clock in these parts. The INT/$\overline{EXT}$ pin has an internal pull-up and may be left open for normal operation, but to utilize an external clock this pin must be tied to V^- to disable the internal clock. The external clock signal may then be applied to the EXT. CLOCK IN pin. At low frequencies, the duty cycle of the external clock is not critical, since an internal divide-by-two provides the desired 50% switching duty cycle. However, since the capacitors are charged only when EXT CLK IN is HIGH, a 50-80% positive duty cycle is favored for frequencies above 500Hz to ensure that any transients have time to settle before the capacitors are turned OFF. The external clock should swing between V^+ and GROUND for power supplies up to ±6V, and between V^+ and V^+ −6V for higher supply voltages. Note that a signal of about 400Hz will be present at the EXT CLK IN pin with INT/$\overline{EXT}$ high or open. This is the internal clock signal before the divider.

In those applications where a strobe signal is available, an alternate approach to avoid capacitor misbalancing during overload can be used. If a strobe signal is connected to EXT CLK IN so that it is low during the time that the overload signal is applied to the amplifier, neither capacitor will be charged. Since the leakage at the capacitor pins is quite low at room temperature, the typical amplifier will drift less than 10μV/sec, and relatively long measurements can be made with little change in offset.

BRIEF APPLICATION NOTES

Component Selection

The two required capacitors, C_{EXTA} and C_{EXTB}, have optimum values depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1μF, and to maintain the same relationship between the chopping frequency and the nulling time constant this value should be scaled approximately in proportion if an external clock is used. A high-quality film-type capacitor such as mylar is preferred, although a ceramic or other lower-grade capacitor may prove suitable in many applications. For quickest settling on initial turn-on, low dielectric absorbtion capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1μV.

Static Protection

All device pins are static-protected by the use of input diodes. However, strong static fields and discharges should be avoided, as they can cause degraded diode junction characteristics, which may result in increased input-leakage currents.

Note: All typical values ve been guaranteed by characterization and are not tested.

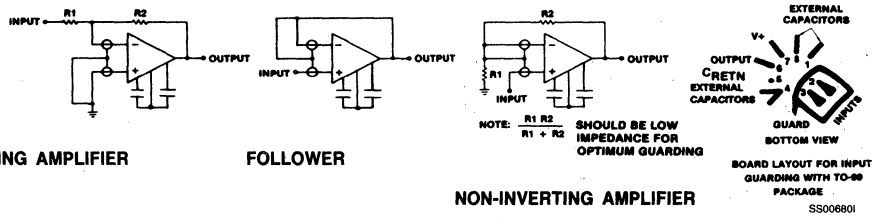


Figure 4: Connection of Input Guards

Latchup Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low-impedance state, resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 1mA to avoid latchup, even under fault conditions.

Output Stage/Load Driving

The output circuit is a high-impedance type (approximately 18kΩ), and therefore with loads less than this value, the chopper amplifier behaves in some ways like a transconductance amplifier whose open-loop gain is proportional to load resistance. For example, the open-loop gain will be 17dB lower with a 1kΩ load than with a 10kΩ load. If the amplifier is used strictly for DC, this lower gain is of little consequence, since the DC gain is typically greater than 120dB even with a 1kΩ load. However, for wideband applications, the best frequency response will be achieved with a load resistor of 10kΩ or higher. This will result in a smooth 6dB/octave response from 0.1Hz to 2MHz, with phase shifts of less than 10° in the transition region where the main amplifier takes over from the null amplifier.

Thermo-Electric Effects

The ultimate limitations to ultra-high precision DC amplifiers are the thermo-electric or Peltier effects arising in thermocouple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermoelectric voltages typically around 0.1μV/°C, but up to tens of μV/°C for some materials, will be generated. In order to realize the extremely low offset voltages that the chopper amplifier can provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially that caused by power-dissipating elements in the system. Low thermoelectric-coefficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and good separation from surrounding heat-dissipating elements is advisable.

Guarding

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the ICL7650. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the 14-pin dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration, but corresponds to that of the LM108).

Pin Compatibility

The basic pinout of the 8-pin device corresponds, where possible, to that of the industry-standard 8-pin devices, the LM741, LM101, etc. The null-storing external capacitors are connected to pins 1 and 8, usually used for offset null or compensation capacitors, or simply not connected. The output-clamp pin (5) is similarly used. In the case of the OP-05 and OP-07 devices, the replacement of the offset-null pot, connected between pins 1 and 8 and V^+, by two capacitors from those pins to V^-, will provide easy compatibility. As for the LM108, replacement of the compensation capacitor between pins 1 and 8 by the two capacitors to V^- is all that is necessary. The same operation, with the removal of any connection to pin 5, will suffice for the LM101, μA748, and similar parts.

The 14-pin device pinout corresponds most closely to that of the LM108 device, owing to the provision of "NC" pins for guarding between the input and all other pins. Since this device does not use any of the extra pins, and has no provision for offset-nulling, but requires a compensation capacitor, some changes will be required in layout to convert it to the ICL7650.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7650

TYPICAL APPLICATIONS

Clearly the applications of the ICL7650 will mirror those of other op. amps. Anywhere that the performance of a circuit can be significantly improved by a reduction of input-offset voltage and bias current, the ICL7650 is the logical choice. Basic non-inverting and inverting amplifier circuits are shown in Figures 5 and 6. Both circuits can use the output clamping circuit to enhance the overload recovery performance. The only limitations on the replacement of other op amps by the ICL7650 are the supply voltage (±8V max.) and the output drive capability (10kΩ load for full swing). Even these limitations can be overcome using a simple booster circuit, as shown in Figure 7, to enable the full output capabilities of the LM741 (or any other standard device) to be combined with the input capabilities of the ICL7650. The pair form a composite device, so loop gain stability, when the feedback network is added, should be watched carefully.

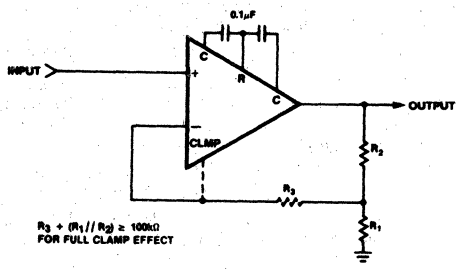


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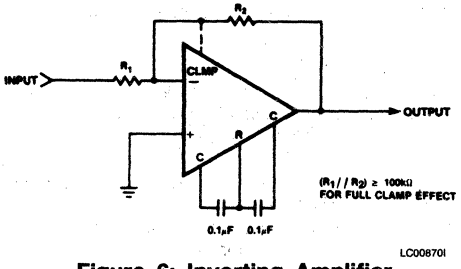
Figure 5: Non Inverting Amplifier With (Optional Clamp)

NOTE: $R_1//R_2$ INDICATES THE PARALLEL COMBINATION OF R_1 AND R_2

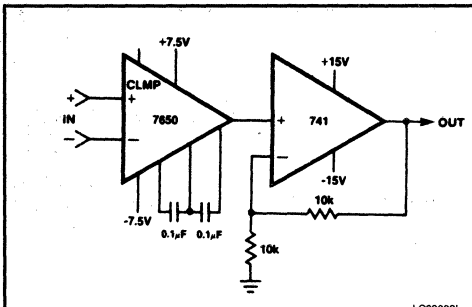


LC00870I

Figure 6: Inverting Amplifier With (Optional) Clamp

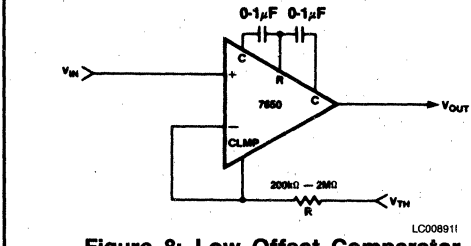
NOTE: $R_1//R_2$ INDICATES THE PARALLEL COMBINATION OF R_1 AND R_2

Figure 8 shows the use of the clamp circuit to advantage in a zero-offset comparator. The usual problems in using a chopper stabilized amplifier in this application are avoided, since the clamp circuit forces the inverting input to follow the input signal. The threshold input must tolerate the output clamp current ≈ V_{IN}/R without disturbing other portions of the system.



LC00880I

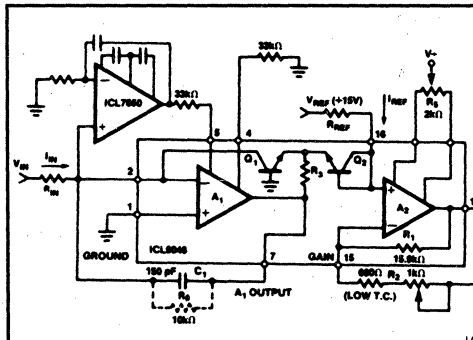
Figure 7: Using 741 to Boost Output Drive Capacity



LC00891I

Figure 8: Low Offset Comparator

Normal logarithmic amplifiers are limited in dynamic range in the voltage-input mode by their input-offset voltage. The built-in temperature compensation and convenience features of the ICL8048 can be extended to a voltage-input dynamic range of close to 6 decades by using the ICL7650 to offset-null the ICL8048, as shown in Figure 8. The same concept can also be used with such devices as the HA2500 or HA2600 families of op amps to add very low offset voltage capability to their very high slew rates and bandwidths. Note that these circuits will also have their DC gains, CMRR, and PSRR enhanced.



LC00900I

Figure 9: ICL8048 Offset Nulled by ICL7650

FOR FURTHER APPLICATIONS ASSISTANCE, SEE A053 AND R017

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7652
Chopper-Stabilized Low-Noise Operational Amplifier

GENERAL DESCRIPTION

The ICL7652 chopper-stabilized amplifier offers exceptionally low input offset voltage and is extremely stable with respect to time and temperature. It is similar to INTERSIL's ICL7650 but offers improved noise performance and a wider common-mode input voltage range. The bandwidth and slew rate are reduced slightly.

INTERSIL's unique CMOS chopper-stabilized amplifier circuitry is user-transparent, virtually eliminating the traditional chopper amplifier problems of intermodulation effects, chopping spikes, and overrange lock-up.

The chopper amplifier achieves its low offset by comparing the inverting and non-inverting input voltages in a nulling amplifier, nulled by alternate clock phases. Two external capacitors are required to store the correcting potentials on the two amplifier nulling inputs; these are the only external components necessary.

The clock oscillator and all the other control circuitry is entirely self-contained, however the 14-pin version includes a provision for the use of an external clock, if required for a particular application. In addition, the ICL7652 is internally compensated for unity-gain operation.

FEATURES

- **Extremely Low Input Offset Voltage — 10μV Over Temperature Range**
- **Ultra Low Long-Term and Temperature Drifts of Input Offset Voltage (150nV/Month, 100nV/°C)**
- **Low DC Input Bias Current — 15pA**
- **Extremely High Gain, CMRR and PSRR — Min 110dB**
- **Low Input Noise Voltage — 0.2μVp-p (DC — 1Hz)**
- **Internally Compensated for Unity-Gain Operation**
- **Very Low Intermodulation Effects (Open-Loop Phase Shift < 2°@ Chopper Frequency)**
- **Clamp Circuit to Avoid Overload Recovery Problems and Allow Comparator Use**
- **Extremely Low Chopping Spikes at Input and Output**

ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ICL7652CPD	0°C to +70°C	14-pin plastic
ICL7652IJD	−25°C to +85°C	14-pin CERDIP
ICL7652CTV	0°C to +70°C	8-pin TO-99
ICL7652ITV	−25°C to +85°C	8-pin TO-99

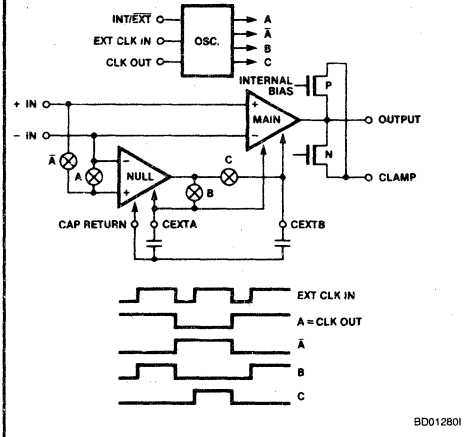


Figure 1: Functional Diagram

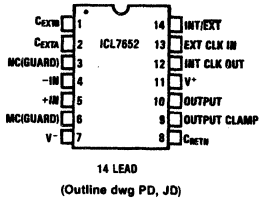


Figure 2: Pin Configuration

302062-002

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7652

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
Input Voltage ..... (V^+ + 0.3) to (V^- – 0.3)V
Voltage on Oscillator Control Pins ..... V^+ to V^-
Duration of Output Short Circuit ..... Indefinite
Current into Any Pin 10mA
— while operating (Note 4) 100μA

Continuous Total Power Dissipation (T_A = 25°C)
CERDIP Package 500mW
Plastic Package 375mW
TO-99 ..... 250mW
Storage Temperature Range ..... –55°C to 150°C
Operating Temperature Range
ICL7652CXX ..... 0°C to +70°C
ICL7652IXX ..... –25°C to +85°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Test Conditions: V^+ = +5V, V^- = –5V, T_A = +25°C, Test Circuit (unless otherwise specified)

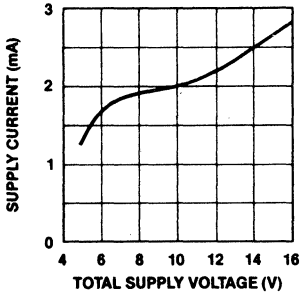
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	T_A = +25°C		±2	±5	μV
		Over Operating Temperature Range (Note 1)		±10		
$\frac{\Delta V_{OS}}{\Delta T}$	Average Temperature Coefficient of Input Offset Voltage	Operating Temperature Range (Note 1)		0.1		μV/°C
$\frac{\Delta V_{OS}}{\Delta T}$	Offset Voltage vs Time			150		nV/month
I_{BIAS}	Input Bias Current	T_A = +25°C		15	30	pA
	(Doubles every 10°C)	0°C < T_A < +70°C		35		
		–25°C < T_A < +85°C		100		
I_{OS}	Input Offset Current	T_A = +25°C		25		pA
R_{IN}	Input Resistance			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	R_L = 10kΩ, V_{OUT} = ±4V	120	150		dB
V_{OUT}	Output Voltage Swing (Note 3)	R_L = 10kΩ	±4.7	±4.85		V
		R_L = 100kΩ		±4.95		
CMVR	Common-Mode Voltage Range		–4.3	–4.8 to +4.0	3.5	V
CMRR	Common-Mode Rejection Radio	CMVR = –4.3V to +3.5V	110	130		dB
PSRR	Power Supply Rejection Ratio	±3V to ±8V	110	130		dB
e_n	Input Noise Voltage	R_S = 100Ω, DC to 1Hz		0.2		μVp-p
		DC to 10Hz		0.7		
i_n	Input Noise Current	f = 10Hz		0.01		pA/$\sqrt{Hz}$
GBW	Unity-Gain Bandwidth			0.4		MHz
SR	Slew Rate	C_L = 50pF, R_L = 10kΩ		0.5		V/μs
	Overshoot			15		%
V^+ to V^-	Operating Supply Range		5.0		16	V
I_{SUPPLY}	Supply Current	No Load		2.0	3.5	mA
f_{ch}	Internal Chopping Frequency	Pins 12-14 Open (DIP)	200	400	600	Hz
	Clamp ON Current (Note 2)	R_L = 100kΩ	25	100	150	μA
	Clamp OFF Current (Note 2)	–4.0V < V_{OUT} < +4.0V		1		pA

NOTES: 1. –25°C to +85°C, or 0°C to +70°C.
2. See OUTPUT CLAMP under detailed description.
3. OUTPUT CLAMP not connected. See typical characteristics curves for output swing vs clamp current characteristics.
4. Limiting input current to 100μA is recommended to avoid latchup problems. Typically 1mA is safe, however this is not guaranteed.

Note: All typical values have been guaranteed by characterization and are not tested.

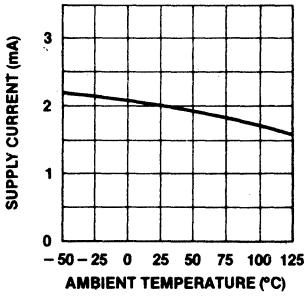
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage



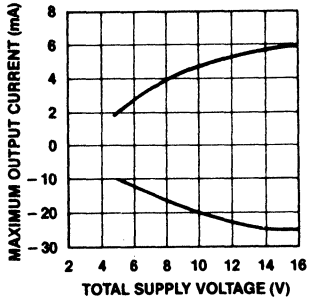
OP03590I

Supply Current vs Ambient Temperature



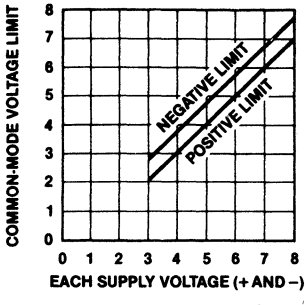
OP03600I

Maximum Output Current vs Supply Voltage



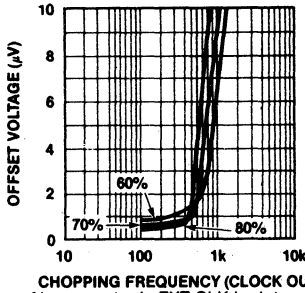
OP03610I

Common-Mode Input Voltage Range vs Supply Voltage



OP03620I

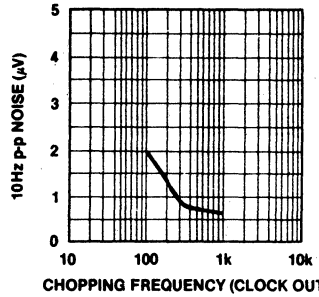
Input Offset Voltage vs Chopping Frequency



% parameter is EXT CLK in duty cycle

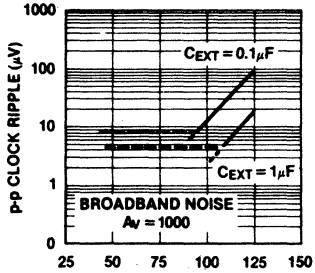
OP03630I

10Hz P-P Noise Voltage Voltage vs Chopping Frequency



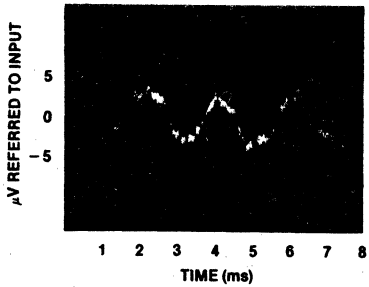
OP03640I

Clock Ripple Referred to the Input vs Temperature



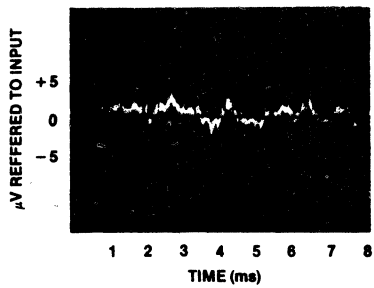
OP03650I

Broadband Noise Balanced Source Impedance = 1kΩ Gain = 1000
C_{EXT} = 0.1µF



OP03660I

Broadband Noise Balanced Source Impedance = 1kΩ Gain = 1000
C_{EXT} = 1.0µF



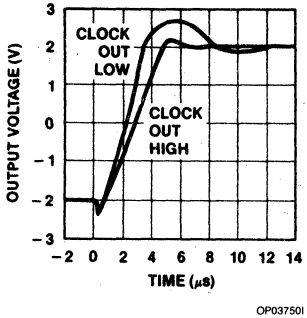
OP03670I

Note: All typical values have been guaranteed by characterization and are not tested.

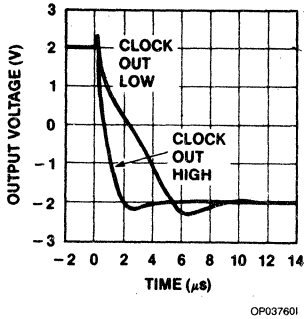
ICL7652

TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

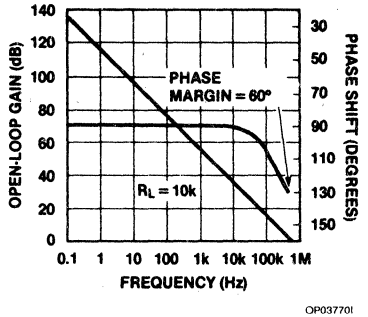
Voltage Follower Large Signal Pulse Response*



Voltage Follower Large Signal Pulse Response*

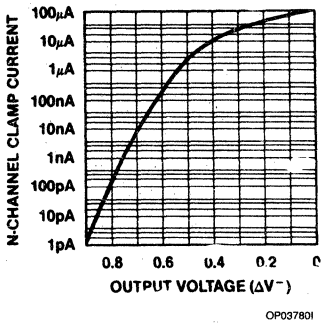


Open-Loop Gain and Phase Shift vs Frequency

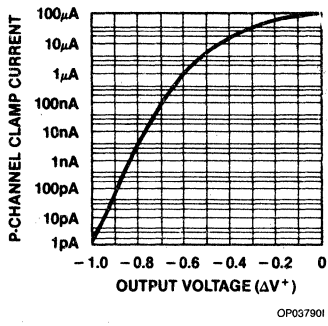


*The two different responses correspond to the two phases of the clock.

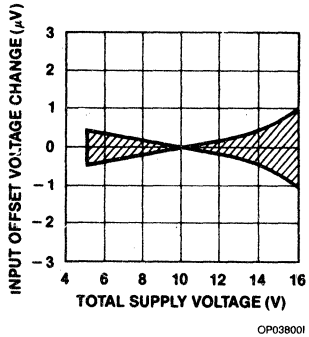
N-Channel Clamp Current vs Output Voltage



P-Channel Clamp Current vs Output Voltage



Input Offset Voltage Change vs Supply Voltage



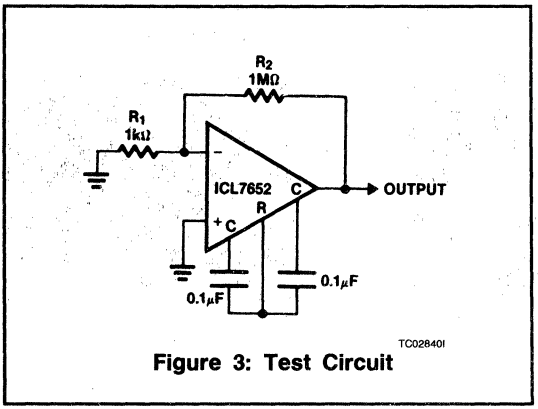


Figure 3: Test Circuit

DETAILED DESCRIPTION

The Functional Diagram (Figure 1) shows the major elements of the ICL7652. There are two amplifiers, the main amplifier, and the nulling amplifier. Both have offset-null capability. The main amplifier is connected continuously from the input to the output. The nulling amplifier, under the control of the chopping frequency oscillator and clock circuit, alternately nulls itself and the main amplifier. The nulling connections, which are MOSFET gates, are inherently high-impedance, and two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants. The nulling arrangement operates over the full common-mode and power supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and A_{VOL}.

Careful balancing of the input switches, together with the inherent balance of the input circuit, minimizes chopper frequency charge injection at the input terminals. Feedforward-type injection into the compensation capacitor is also minimized, which is the main cause of output spikes in this type of circuit.

Intermodulation

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite AC gain of the amplifier necessitates a small AC signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies and causing disturbances to the gain and phase vs frequency characteristics near the chopping

Note: All typical values have been guaranteed by characterization and are not tested.

frequency. These effects are substantially reduced in the ICL7652 by feeding the nulling circuit with a dynamic current, corresponding to the compensation capacitor current, in such a way as to cancel that portion of the input signal due to finite AC gain. Since that is the major error contribution to the ICL7652, the intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

Capacitor Connection

The null-storage capacitors should be connected to the C_{EXTA} and C_{EXTB} pins, with a common connection to the C_{RETN} pin. This connection should be made directly by either a separate wire or PC trace to avoid injecting load current IR drops into the capacitive circuitry. The outside foil, where available, should be connected to C_{RETN}.

Output Clamp

The OUTPUT CLAMP pin allows reduction of the overload recovery time inherent with chopper-stabilized amplifiers. When tied to the inverting input pin, or summing junction, a current path between this point and the OUTPUT pin occurs just before the device output saturates. Thus uncontrolled differential input voltages are avoided, together with the consequent charge build-up on the correction-storage capacitors. The output swing is slightly reduced.

Clock

The ICL7652 has an internal oscillator, giving a chopping frequency of 400Hz, available at the CLOCK OUT pin on the 14-pin devices. Provision has also been made for the use of an external clock in these parts. The INT/$\overline{EXT}$ pin has an internal pull-up and may be left open for normal operation, but to utilize an external clock this pin must be tied to V^- to disable the internal clock. The external clock signal may then be applied to the EXT CLOCK IN pin. An internal divide-by-two provides the desired 50% input switching duty cycle. Since the capacitors are charged only when EXT CLOCK IN is high, a 50%–80% positive duty cycle is recommended, especially for higher frequencies. The external clock can swing between V^+ and V^-. The logic threshold will be at about 2.5V below V^+. Note also that a signal of about 800Hz, with a 70% duty cycle, will be present at the EXT CLOCK IN pin with INT/EXT high or open. This is the internal clock signal before being fed to the divider.

In those applications where a strobe signal is available, an alternate approach to avoid capacitor misbalancing during overload can be used. If a strobe signal is connected to EXT CLK IN so that it is low during the time that the overload signal is applied to the amplifier, neither capacitor will be charged. Since the leakage at the capacitor pins is quite low at room temperature, the typical amplifier will drift less than 10μV/sec, and relatively long measurements can be made with little change in offset.

BRIEF APPLICATION NOTES

Component Selection

The required capacitors, C_{EXTA} and C_{EXTB}, are normally in the range of 0.1μF to 1.0μF. A 1.0μF capacitor should be used in broad bandwidth circuits if minimum clock ripple noise is desired. For limited bandwidth applications where clock ripple is filtered out, using a 0.1μF capacitor results in slightly lower offset voltage. A high-quality film-type capacitor such as mylar is preferred, although a ceramic or other lower-grade capacitor may prove suitable in many applications. For quickest settling on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1μV.

Static Protection

All device pins are static-protected by the use of input diodes. However, strong static fields and discharges should be avoided, as they can cause degraded diode junction characteristics which may result in increased input-leakage currents.

Latchup Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be trigerred into a low-impedance state, resulting in excessive supply current. To avoid this condition no voltage greater than 0.3V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 1mA to avoid latchup, even under fault conditions.

Output Stage/Load Driving

The output circuit is a high-impedance type (approximately 18kΩ), and therefore, with loads less than this the chopper amplifier behaves in some ways like a transconductance amplifier whose open-loop gain is proportional to load resistance. For example, the open-loop gain will be 17dB lower with a 1kΩ load than with a 10kΩ load. If the amplifier is used strictly for DC, this lower gain is of little consequence, since the DC gain is typically greater than 120dB even with a 1kΩ load. However, for wideband applications, the best frequency response will be achieved with a load resistor of 10kΩ or higher. This will result in a smooth 6dB/octave response from 0.1Hz to 2MHz, with phase shifts of less than 2° in the transition region where the main amplifier takes over from the null amplifier.

Thermo-Electric Effects

The ultimate limitations to ultra-high precision DC amplifiers are the thermo-electric or Peltier effects arising in thermo-couple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermo-electric voltages typically around 0.1μV/°C, but up to tens of μV/°C for some materials, will be generated. In order to realize the extremely low offset voltages that the chopper amplifier can provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially that caused by power-dissipating elements in the system. Low thermoelectric-coefficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and good separation from surrounding heat-dissipating elements is advisable.

Guarding

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the ICL7652. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7652

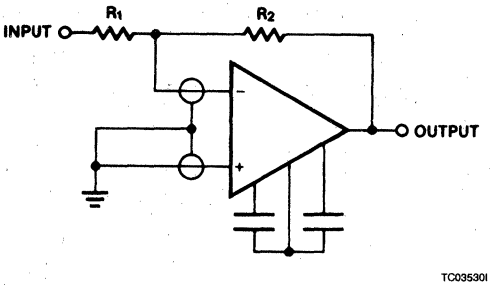
Even with properly cleaned and coated boards, leakage currents may cause trouble, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8 lead TO-99 package is accomplished by using a 10 lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low-impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the 14-pin dual-in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration, but corresponds to that of the LM108).

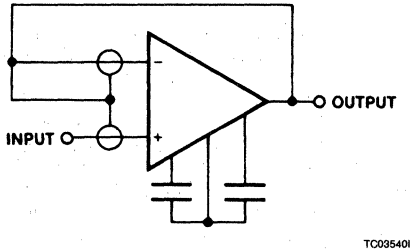
PIN COMPATIBILITY

The basic pinout of the 8-pin device corresponds, where possible, to that of the industry-standard 8-pin devices, the LM741, LM101, etc. The null-storing external capacitors are connected to pins 1 and 8, which are usually used for offset-null or compensation capacitors. The output-clamp pin (5) is similarly used. In the case of the OP-05 and OP-07 devices, the replacement of the offset-null pot, connected between pins 1 and 8 and V^+, by two capacitors from those pins to V^-, will provide easy compatibility. As for the LM108, replacement of the compensation capacitor between pins 1 and 8 by the two capacitors to V^- is all that is necessary. The same operation, with the removal of any connection to pin 5, will suffice for the LM101, μA748, and similar parts.

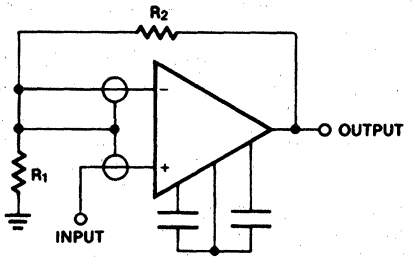
The 14-pin device pinout corresponds most closely to that of the LM108 device, owing to the provision of "NC" pins for guarding between the input and all other pins. Since this device does not use any of the extra pins, and has no provision for offset-nulling, but requires a compensation capacitor, some changes will be required in layout to convert to the ICL7652.



Inverting Amplifier



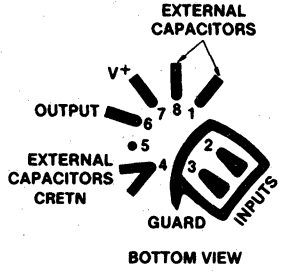
Follower



Note: $\frac{R_1 R_2}{R_1 + r_2}$

Should be low impedance for optimum guarding

Non-Inverting Amplifier



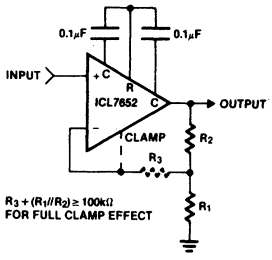
BOTTOM VIEW

Board Layout for Input Guarding With TO-99 Package

Figure 4: Connection of Input Guards

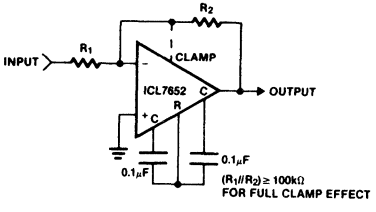
Note: All typical values have been guaranteed by characterization and are not tested.

TYPICAL APPLICATIONS



LC01650I

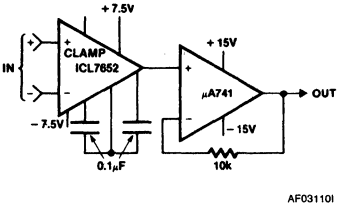
Figure 5: Non-Inverting Amplifier with (Optional) Clamp



LC01770I

Figure 6: Inverting Amplifier with (Optional) Clamp

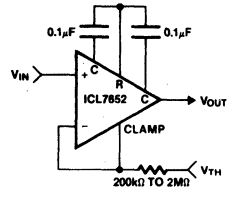
Clearly the applications of the ICL7652 will mirror those of other op-amps. Thus, anywhere that the performance of a circuit can be significantly improved by a reduction of input-offset voltage and bias current, the ICL7652 is the logical choice. Basic non-inverting and inverting amplifier circuits are shown in Figures 5 and 6. Both circuits can use the output clamping circuit to enhance the overload recovery performance. The only limitations on the replacement of other op-amps by the ICL7652 are the supply voltage (±8V max) and the output drive capability (10kΩ load for full swing). Even these limitations can be overcome using a simple booster circuit, as shown in Figure 7, to enable the full output capabilities of the LM741 (or any other standard device) to be combined with the input capabilities of the ICL7652. The pair form a composite device, so loop gain stability, when the feedback network is added, should be watched carefully.



AF03110I

Figure 7: Using 741 to Boost Output Drive Capability

Figure 8 shows the use of the clamp circuit to advantage in a zero-offset comparator. The usual problems in using a chopper-stabilized amplifier in this application are avoided, since the clamp circuit forces the inverting input to follow the input signal. The threshold input must tolerate the output clamp current $\approx V_{IN}/R$ without disturbing other portions of the system.



AF03120I

Figure 8: Low Offset Comparator

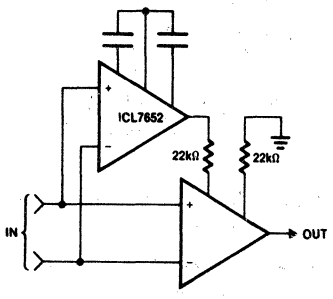
It is possible to use the ICL7652 to offset-null such high slew rate and bandwidth amplifiers as the HA2500 and HA2600 series, as shown in Figure 9. The same basic idea can be used with low-noise bipolar devices, such as the OP-05, and also with the ICL8048 logarithmic amplifier, to achieve a voltage-input dynamic range of close to 6 decades. Note that these circuits will also have their DC gains, CMRR and PSRR enhanced. More details on these and other ideas are explained in application note A053.

Mixing the ICL7652 with circuits operating at ±15V supplies requires the provision of a lower voltage. Although this can be done fairly easily, a highly efficient voltage divider can be built using the ICL7660 voltage converter circuit "backwards". A suitable connection is shown in Figure 10.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7652

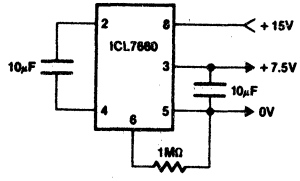
TYPICAL APPLICATIONS (CONT.)



AF03131I

HA2500/10/20
HA2600/20
OR SIMILAR DEVICE

Figure 9: HA2500 or HA2600 Offset-Nulled by ICL7652



AF03080I

Figure 10: Splitting +15V with ICL7660 at >95% efficiency. Same for −15V

For further applications assistance, see A053 and R017

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8007
JFET Input Operational Amplifier

GENERAL DESCRIPTION

The Intersil ICL8007 is a low input current JFET input operational amplifier. The ICL8007A is selected for 4 pA max input current.

The devices are designed for use in very high input impedance applications. Because of their high slew rate, high common mode voltage range and absence of "latch-up", they are ideal for use as a voltage follower.

The Intersil 8007 and 8007A are short circuit protected. They require no external components for frequency compensation because the internal 6 dB/roll-off insures stability in closed loop applications. A unique bootstrap circuit insures unusually good common mode rejection for a JFET input op-amp and prevents large input currents as seen in some amplifiers at high common mode voltage.

FEATURES

- **Ultra Low Input Current**
- **High Slew Rate — 6V/μs**
- **Wide Input Common Mode Voltage**
- **1MHz Band Width**
- **Excellent Stability**
- **Ideal for Unity Gain Applications**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL8007CTY ICL8007ACTV	0°C to +70°C	8 LEAD TO-99 METAL CAN
ICL8007MTY ICL8007AMTV	−55°C to +125°C	
ICL8007/D	—	DICE**

**Parameter Min/Max Limits quaranteed at 25°C only for DICE orders.

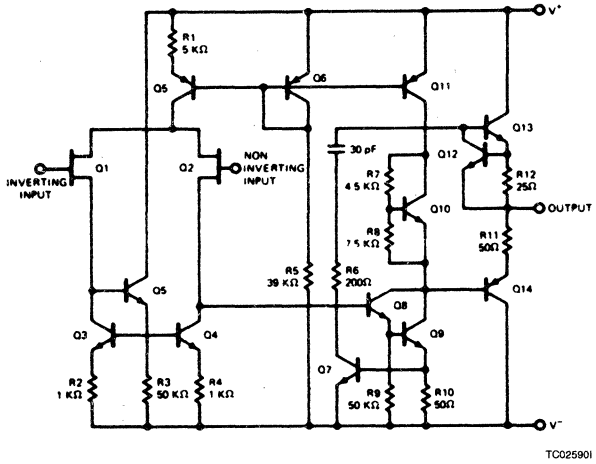
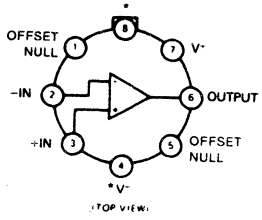


Figure 1: Functional Diagram



ICL8007 pin 4 connected to case (TY package)
ICL8007A pin 8 connected to case (TV package)

Figure 2: Pin Configuration

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8007

ABSOLUTE MAXIMUM RATINGS

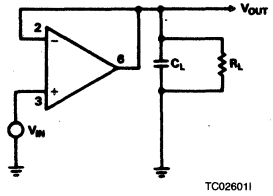
Supply Voltage ..... ±18V
Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±15V
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range
8007M, 8007AM ..... −55°C to +125°C
8007C, 8007AC ..... 0°C to +70°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Output Short-Circuit Duration (Note 3) ..... Indefinite

NOTES:

1. Rating applies for case temperatures to 125°C; derate linearly at 6.5 mW/°C for ambient temperatures above +75°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
4. For Design only, not 100% tested.

ELECTRICAL CHARACTERISTICS (V_S = ±15V unless otherwise specified)

CHARACTERISTICS	TEST CONDITIONS	8007M			8007C			8007AM & 8007AC			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
The following specifications apply for T_A = 25°C:											
Input Offset Voltage	$R_S \leq 100k\Omega$		10	20		20	50		15	30	mV
Input Offset Current			0.5			0.5			0.2		pA
Input Bias Current (either input)			2.0	20		3.0	50		0.5	4.0	pA
Input Resistance			10^6			10^6			10^6		MΩ
Input Capacitance			2.0			2.0			2.0		pF
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	50,000			20,000			20,000			V/V
Output Resistance			75			75			75		Ω
Output Short-Circuit Current			25			25			25		mA
Supply Current			3.4	5.2		3.4	6.0		3.4	6.0	mA
Power Consumption			102	156		102	180		102	180	mW
Slew Rate			6.0			6.0		2.5	6.0		V/μs
Unity Gain Bandwidth			1.0			1.0			1.0		MHz
Risetime	$C_L \leq 100pF$, $R_L = 2k\Omega$		300			300			300		ns
Overshoot	$C_L \leq 100pF$, $R_L = 2k\Omega$		10			10			10		%
The following specifications apply for 0°C ≤ T_A ≤ +70°C (8007C and 8007AC), and −55°C ≤ T_A ≤ +125°C (8007M and 8007AM):											
Input Voltage Range		±10	±12		±10	±12		±10	±12		V
Common Mode Rejection Ratio		70	90		70	90		86	95		dB
Supply Voltage Rejection Ratio			70	300		70	600		70	200	μV/V
Large Signal Voltage Gain		25,000			15,000			15,000			V/V
Output Voltage Swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12 ±10	±14 ±13		±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
Input Bias Current (either input)	T_A = +125°C T_A = +70°C		2.0			50			1.0 30		nA pA
Average Temperature Coefficient of Input Offset Voltage	(Note 4)			75			75			50	μV/°C



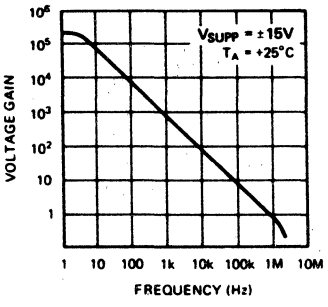
TC02601I

Figure 3: Transient Response Test Circuit

Note: All typical values have been guaranteed by characterization and are not tested.

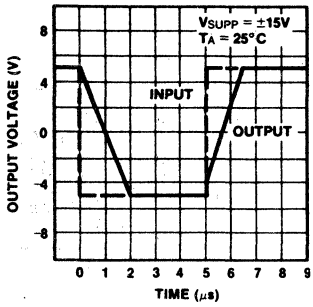
TYPICAL PERFORMANCE CHARACTERISTICS

OPEN LOOP VOLTAGE GAIN



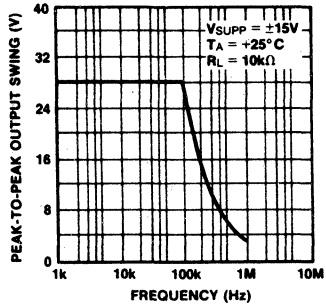
OP02580I

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



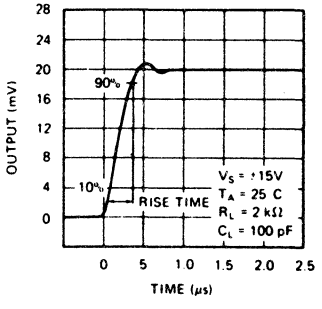
OP02590I

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



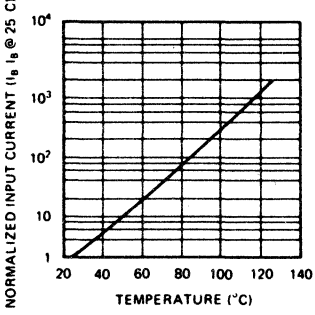
OP02600I

TRANSIENT RESPONSE



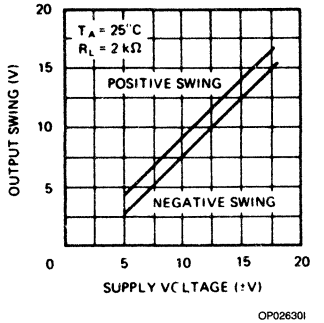
OP02610I

INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE



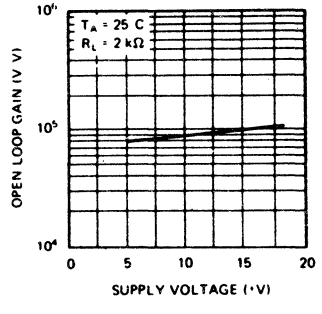
OP02620I

OUTPUT SWING AS A FUNCTION OF SUPPLY VOLTAGE



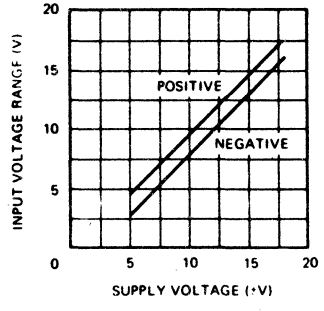
OP02630I

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



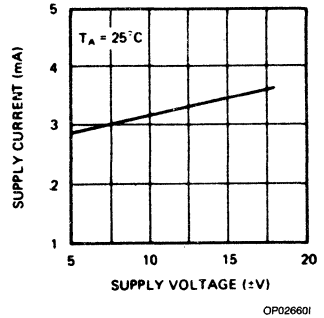
OP02640I

INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



OP02650I

QUIESCENT SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



OP02660I

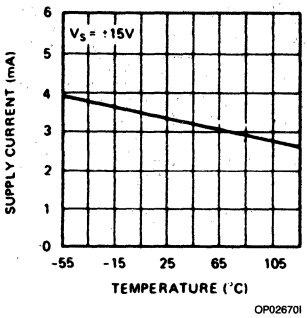
4

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8007

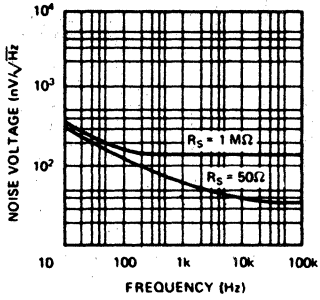
TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

QUIESCENT SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



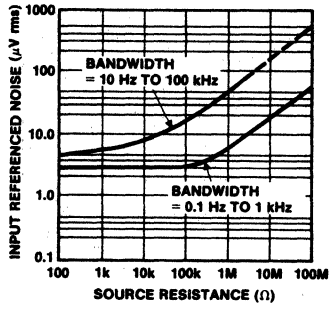
OP02670I

INPUT VOLTAGE NOISE AS A FUNCTION OF FREQUENCY



OP02680I

WIDEBAND NOISE AS A FUNCTION OF SOURCE RESISTANCE



OP02691I

For additional information, see Application Note A005.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8021/ICL8022/ ICL8023

Low Power Bipolar Operational Amplifier

GENERAL DESCRIPTION

The Intersil ICL8021 series are low power operational amplifiers specifically designed for applications requiring very low standby power consumption over a wide range of supply voltages. The electrical characteristics of the 8021 series can be tailored to a particular application by adjusting an external resistor, R_{SET}, which controls the quiescent current. This is advantageous because I_Q can be made independent of the supply voltages: it can be set to an extremely low value where power is critical, or to a larger value for high slew rate or wideband applications.

Other features of the 8021 series include low input current that remains constant with temperature, low noise, high input impedance, internal compensation and pin-for-pin compatibility with the 741.

The Intersil 8022 (8023) consists of two (three) low power operational amplifiers in a single 14(16)-pin DIP. Each amplifier is identical to an 8021 low power op amp, and has separate connections for adjusting its electrical characteristics by means of an external resistor, R_{SET}, which controls the quiescent current of that amplifier.

FEATURES

- **V_{OS} = 3mV Max (Adjustable to Zero)**
- **±1.5V to ±18V Power Supply Operation**
- **Power Consumption — 20μW @ ±1V**
- **Input Bias Current — 30nA Max**
- **Internal Compensation**
- **Pin-For-Pin Compatible With 741**
- **Short Circuit Protected**

ORDERING INFORMATION

ICL8021 C TY

Package
- TY — TO-99 Metal Can
- PA — 8 pin Minidip

8021 only

- JD — 14 pin CERDIP
- PD — 14 pin Plastic DIP

8022 only

- JE — 16 pin CERDIP
- PE — 16 pin Plastic DIP

8023 only

Temperature
- C — Commercial — 0°C to +70°C
- M — Military — −55°C to +125°C

Basic Part Number
- 8021 — Single
- 8022 — Dual
- 8023 — Triple

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL8021/D	—	DICE**
ICL8021CJA	0°C to 70°C	8 Lead CERDIP
ICL8021CBA	0°C to 70°C	8 Lead S.O.I.C
ICL8021CPA	0°C to 70°C	8 Lead MINIDIP
ICL8021CTY	0°C to 70°C	8 Lead Metal Can
ICL8021MJA	−55°C to +125°C	8 Lead CERDIP
ICL8021MJD	−55°C to +125°C	14 Lead CERDIP
ICL8021MTY	−55°C to +125°C	8 Lead Metal Can
ICL8022/D	—	DICE
ICL8022CJD	0°C to 70°C	14 Lead CERDIP
ICL8022CPD	0°C to 70°C	14 Lead MINIDIP
ICL8022MJD	−55°C to +125°C	14 Lead CERDIP
ICL8023/D	—	DICE
ICL8023CJE	0°C to 70°C	16 Lead CERDIP
ICL8023CPE	0°C to 70°C	16 Lead MINIDIP
ICL8023MJE	−55°C to +125°C	16 Lead CERDIP

**Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8021/ICL8022/ICL8023

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Differential Input Voltage (Note 1) ..... ±15V
Common Mode Input Voltage (Note 1) ..... ±15V
Output Short Circuit Duration ..... Indefinite
Power Dissipation (Note 2) 300mW

Operating Temperature Range
8021M ..... −55°C to +125°C
8021C ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C

NOTE 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
NOTE 2: Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +95°C.

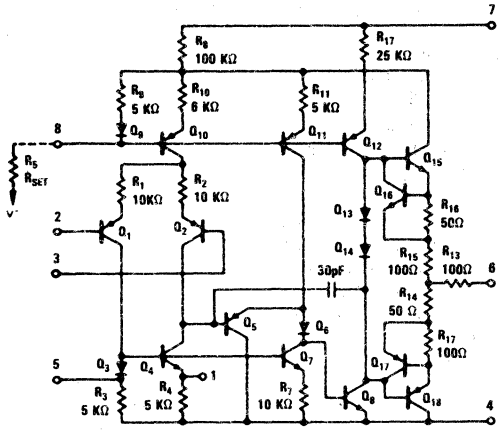
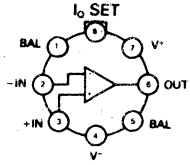
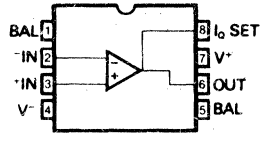


Figure 1: Functional Diagram



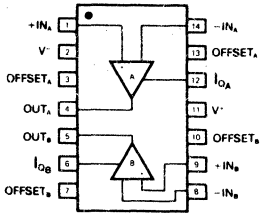
(outline dwg TY)

CD01740I



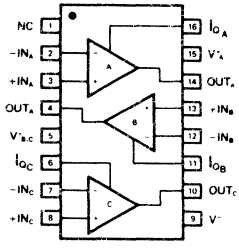
(outline dwg PA)

CD01750I



(outline dwg JD, PD)

CD01760I

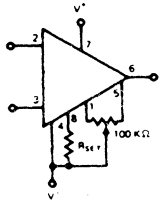


(outline dwg JE, PE)

CD01770I

Figure 2: Pin Configurations

Note: All typical values have been guaranteed by characterization and are not tested.



TC03480I

Figure 3: Voltage Offset Null Circuit

ELECTRICAL CHARACTERISTICS (V_{SUPPLY} = ±6V, I_Q = 30μA, unless otherwise specified.)

CHARACTERISTICS	TEST CONDITIONS	8021M			8021C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
The following specifications apply for T_A = 25°C:								
Input Offset Voltage	$R_S \leq 100k\Omega$		2	3		2	6	mV
Input Offset Current			.5	7.5		.7	10	nA
Input Bias Current			5	20		7	30	nA
Input Resistance		3	10		3	10		MΩ
Input Voltage Range	V_{SUPPLY} = ±15V	±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	80		70	80		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		30	150		30	150	μV/V
Output Resistance	Open Loop		2			2		kΩ
Output Voltage Swing	$R_L \geq 20k\Omega$, V_{SUPPLY} = ±15V	±12	±14		±12	±14		V
	$R_L \geq 10k\Omega$, V_{SUPPLY} = ±15V	±11	±13		±11	±13		V
Output Short-Circuit Current			±13			±13		mA
Power Consumption	V_{OUT} = 0		360	480		360	600	μW
Slew Rate (Unity Gain)			0.16			0.16		V/μs
Unity Gain Bandwidth	R_L = 20kΩ, V_{IN} = 20mV		270			270		kHz
Transient Response (Unity Gain)	R_L = 20kΩ, V_{IN} = 20mV							
Risetime			1.3			1.3		μs
Overshoot			10			10		%
The following specifications apply for 0°C ≤ T_A ≤ +70°C (8021C) and −55°C ≤ T_A ≤ +125°C (8021M)								
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	4.0		2.0	7.5	mV
Input Offset Current			1.0	11		1.5	15	nA
Input Bias Current			10	32		15	50	nA
Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 10k\Omega$		5			5		μV/°C
Average Temperature Coefficient of Input Offset Current			1.7			0.8		pA/°C
Large Signal Voltage Gain	R_L = 10kΩ	50	200		50	200		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±10	±13		±10	±13		V

Note: All typical values have been guaranteed by characterization and are not tested.

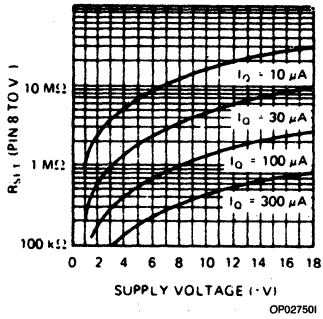
ICL8021/ICL8022/ICL8023

QUIESCENT CURRENT ADJUSTMENT

QUIESCENT CURRENT SETTING RESISTOR
(PIN 8 to V⁻)

	I_Q			
V_S	10μA	30μA	100μA	300μA
±1.5	1.5MΩ	470kΩ	150kΩ	–
±3	3.3MΩ	1.1MΩ	330kΩ	100kΩ
±6	7.5MΩ	2.7MΩ	750kΩ	220kΩ
±9	13MΩ	4MΩ	1.3MΩ	350kΩ
±12	18MΩ	5.6MΩ	1.5MΩ	510kΩ
±15	22MΩ	7.5MΩ	2.2MΩ	620kΩ

QUIESCENT CURRENT SETTING RESISTOR
(PIN 8 to V⁻)

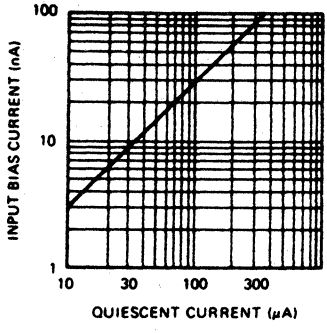


OP02750I

TYPICAL PERFORMANCE CHARACTERISTICS*

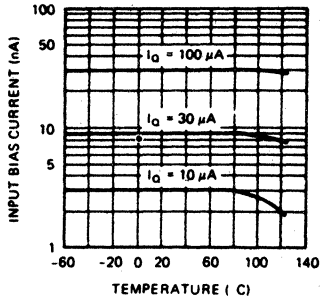
(T_A = +25°C, V_S = ±6V, I_Q = 30μA unless otherwise specified.)

INPUT BIAS CURRENT VS QUIESCENT CURRENT



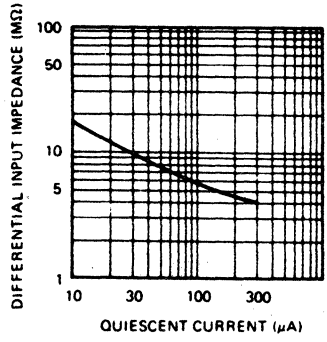
OP02760I

INPUT BIAS CURRENT VS AMBIENT TEMPERATURE



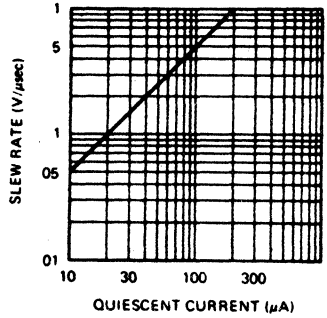
OP02770I

DIFFERENTIAL INPUT IMPEDANCE VS QUIESCENT CURRENT



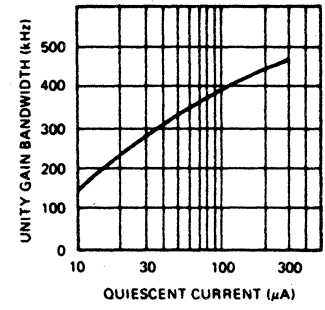
OP02780I

SLEW RATE VS QUIESCENT CURRENT



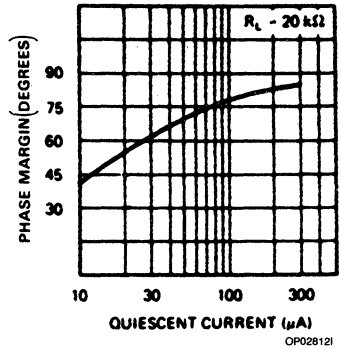
OP02790I

FREQUENCY RESPONSE VS QUIESCENT CURRENT



OP02800I

PHASE MARGIN VS QUIESCENT CURRENT



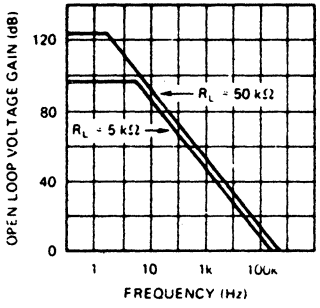
OP02812I

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8021/ICL8022/ICL8023

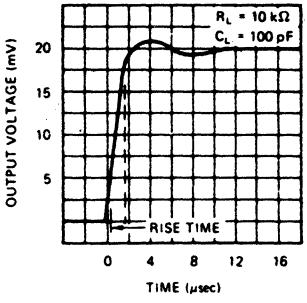
TYPICAL PERFORMANCE CHARACTERISTICS* (CONT.)

OPEN-LOOP FREQUENCY RESPONSE



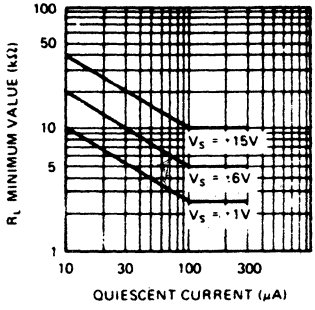
OP02820I

TRANSIENT RESPONSE



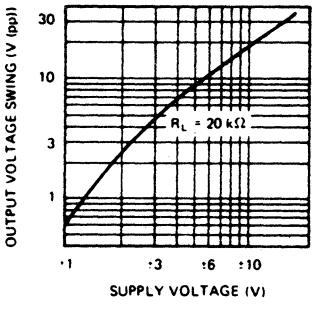
OP02830I

MAXIMUM LOAD VS QUIESCENT CURRENT



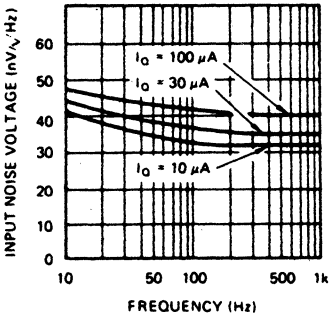
OP02840I

OUTPUT VOLTAGE SWING VS SUPPLY VOLTAGE



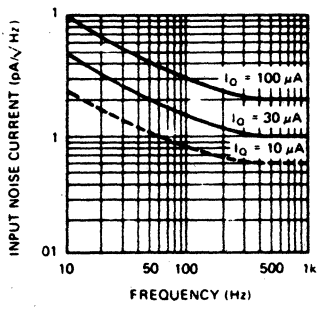
OP02850I

EQUIVALENT INPUT NOISE VOLTAGE VS FREQUENCY



OP02860I

EQUIVALENT INPUT NOISE CURRENT VS FREQUENCY



OP02870I

*ICL8021C guaranteed only for $0°C \leq T_A \leq +70°C$

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8043
Dual JFET Input Operational Amplifier

GENERAL DESCRIPTION

The ICL8043 contains two FET input op amps, each similar in performance to the ICL8007. The inputs and outputs are fully short circuit protected, and no latch-up problems exist. Offset nulling is accomplished by using a single pot (for each amplifier) connected to the positive supply voltage. The devices have excellent common mode rejection.

FEATURES

- **Very Low Input Current — 2pA Typical**
- **High Slew Rate — 6V/μs**
- **Internal Frequency Compensation**
- **Low Power Dissipation — 135mW Typical**
- **Monolithic Construction**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL8043MJE	-55°C to 125°C	CERAMIC 16 Pin DIP
ICL8043CPE	0°C to 70°C	Plastic 16 Pin DIP
ICL8043CJE	0°C to 70°C	CERAMIC 16 Pin DIP

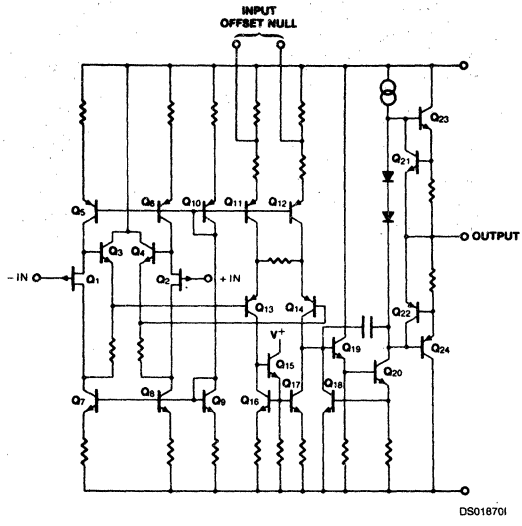


Figure 1: Functional Diagram (One Side)

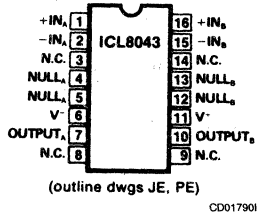


Figure 2: Pin Configuration 16 Pin DIP (Top View)

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8043

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±15V
Voltage between Offset Null and V^+ ..... ±0.5V
Storage Temperature Range ..... −65°C to +150°C

Operating Temperature Range
8043M ..... −55°C to +125°C
8043C ..... 0°C to +70°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Output Short-Circuit Duration ..... Indefinite

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTES: 1. Rating applies for case temperatures to 125°C; derate linearly at 9mW/°C for ambient temperatures above +95°C.

2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS (V_{SUPPLY} = ±15V unless otherwise specified)

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	8043M			8043C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
The following specifications apply for T_A = 25°C:									
V_{OS}	Input Offset Voltage	R_S < 100kΩ		10	20		20	50	mV
I_{OS}	Input Offset Current			0.5			0.5		pA
I_{IN}	Input Current (either input)			2.0	20		3.0	50	pA
R_{IN}	Input Resistance			10^6			10^6		MΩ
C_{IN}	Input Capacitance			2.0			2.0		pF
A_V	Large Signal Voltage Gain	R_L > 2kΩ, V_{out} = ±10V	50,000			20,000			V/V
R_O	Output Resistance			75			75		Ω
I_{SC}	Output Short-Circuit Current			25			25		mA
I_{SUPPLY}	Supply Current (Total)			4.5	6		4.5	6.8	mA
P_{DISS}	Power Consumption			135	180		135	204	mW
SR	Slew Rate			6.0			6.0		V/μs
GBW	Unity Gain Bandwidth			1.0			1.0		MHz
t_r	Transient Response (Unity Gain) Risetime Overshoot	C_L < 100pF, R_L = 2kΩ		300 10			300 10		ns %
The following specifications apply for 0°C < T_A < +70°C (8043C), −55°C < T_A < +125°C (8043M):									
ΔV_{IN}	Input Voltage Range		±10	±12		±10	±12		V
CMRR	Common Mode Rejection Ratio		70	90		70	90		dB
PSRR	Supply Voltage Rejection Ratio			70	300		70	600	μV/V
A_V	Large Signal Voltage Gain		25,000			15,000			V/V
ΔV_O	Output Voltage Swing	R_L > 10kΩ	±12	±14		±12	±14		V
		R_L > 2kΩ	±10	±13		±10	±13		V
V_{OS}	Input Offset Voltage			15	30		30	60	mV
I_{IN}	Input Current (either input)	T_A = +125°C		2.0	15				nA
		T_A = +70°C					50	175	pA
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	(Note 3)		75			75		μV/°C

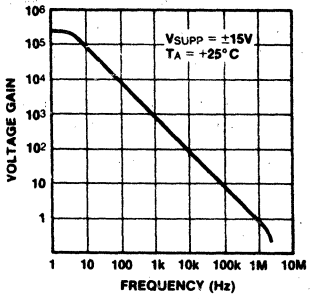
NOTE: 3. For Design only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

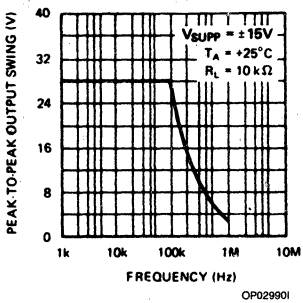
ICL8043

TYPICAL PERFORMANCE CHARACTERISTICS

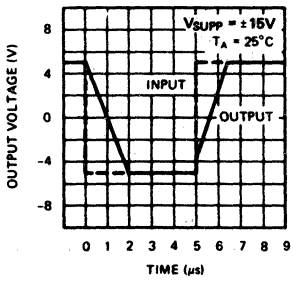
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



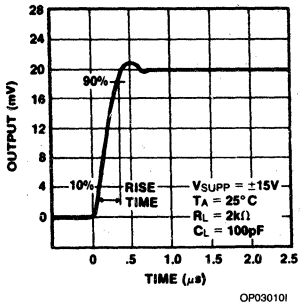
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



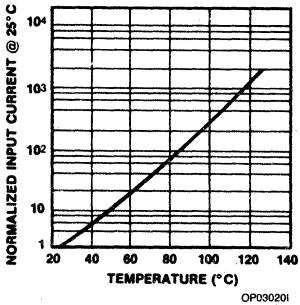
VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE



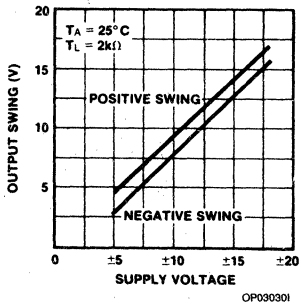
TRANSIENT RESPONSE



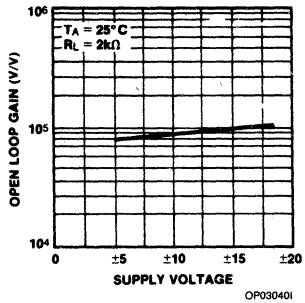
INPUT CURRENT AS A FUNCTION OF TEMPERATURE



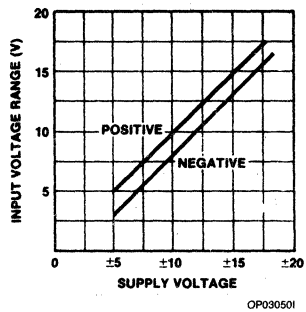
OUTPUT SWING AS A FUNCTION OF SUPPLY VOLTAGE



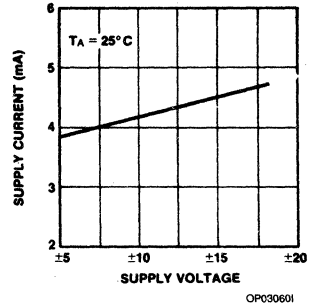
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



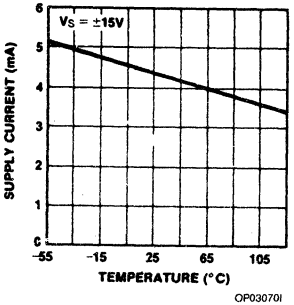
QUIESCENT SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



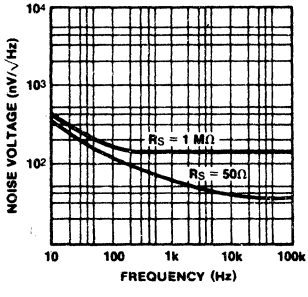
Note: All typical values have been guaranteed by characterization and are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

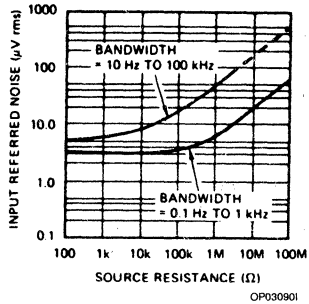
TOTAL QUIESCENT SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



WIDEBAND NOISE AS A FUNCTION OF SOURCE RESISTANCE



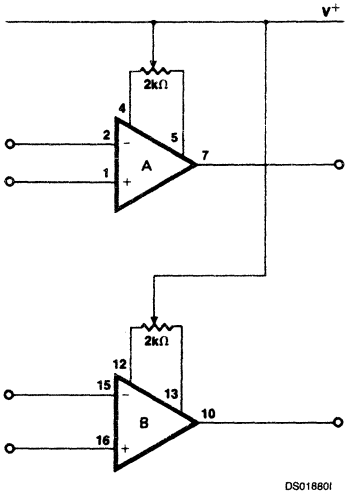


Figure 3: Offset Voltage Null Circuit

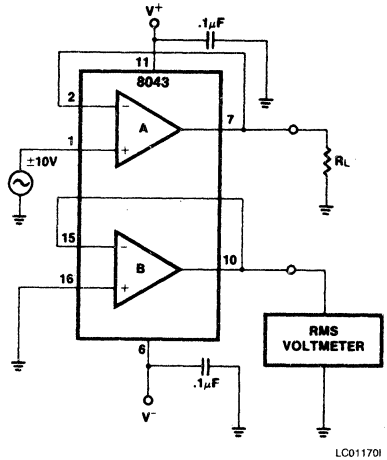


Figure 4: Channel Separation Test Circuit

CHANNEL SEPARATION

Channel separation or crosstalk is measured using the circuit of Figure 4. One amplifier is driven so that its output swings ±10V; the signal amplitude seen in the other amplifier (referred to the input) is then measured. Typical performance is shown in Figure 5.

$$\text{Channel Separation} = 20 \log \left(\frac{V_{OUT\ (A)}}{V_{IN\ (B)}} \right)$$

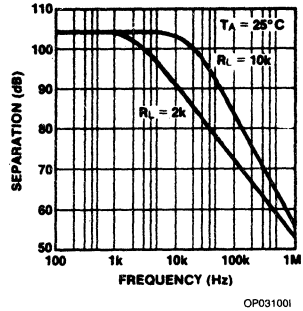


Figure 5: Channel Separation Performance

Note: All typical values have been guaranteed by characterization and are not tested.

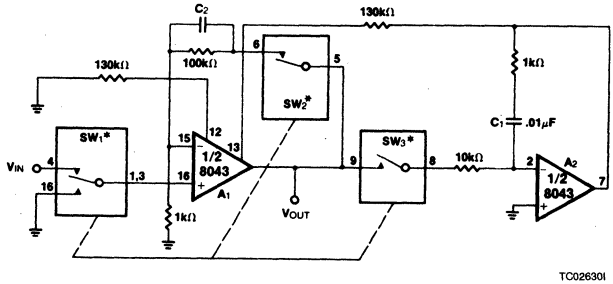
APPLICATIONS

Applications for any dual amplifier fall into two categories. There are those which use the two-in-one package concept simply to save circuit-board space and cost, but more interesting are those circuits where the two sides of the dual are used to complement one another in a subsystem application. The circuits which follow have been selected on this basis.

AUTOMATIC OFFSET SUPPRESSION CIRCUIT

The circuit shown in Figure 6 uses one amplifier (A_1) as a normal gain stage, while the other (A_2) forms part of an offset voltage zeroing loop. There are two modes of operation which occur sequentially. First, an offset null correction mode occurs during which the offset voltage of A_1 is nulled out. Following this nulling operation, A_1 is used as a normal amplifier while the voltage necessary to zero its offset voltage is stored on the integrator comprised of A_2 and C_1.

The advantage of this circuit is that it allows chopper amplifier performance to be achieved at one-tenth the cost. The only limitation is that during the offset nulling mode, A_1 is disconnected from the input. However, in most data acquisition systems, many inputs are scanned sequentially. It is fairly simple to synchronize the offset nulling operation so that it does not occur when that particular amplifier is being "looked at". For the component values shown in Figure 3, and assuming a total leakage of 50pA at the inverting input of A_2, the offset voltage referred to the input of A_1 will drift away from zero at only 40μV/sec. Thus, the offset nulling information stored on C_1 can be "refreshed" relatively infrequently. The measured offset voltage of A_1 during the amplification mode was 11μV; offset voltage drift with temperature was less than 0.1μV/°C.



*SW_1, SW_2, & SW_3 ARE ALL PART OF A SINGLE IH5043 CMOS ANALOG SWITCH CONNECTED AS SHOWN IN FIGURE 6(b)

Figure 6(a): Automatic Offset Null Circuit

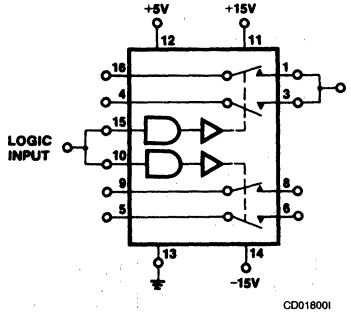


Figure 6(b)

Note: All typical values have been guaranteed by characterization and are not tested.

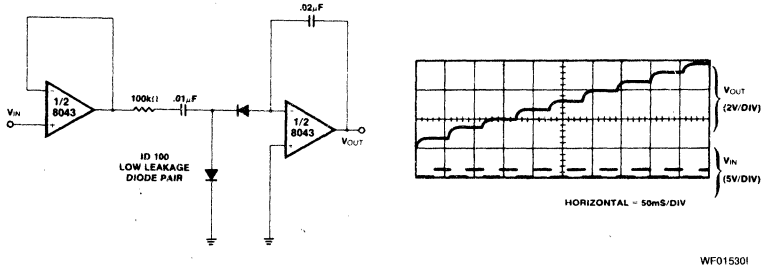


Figure 7: Staircase Generator Circuit

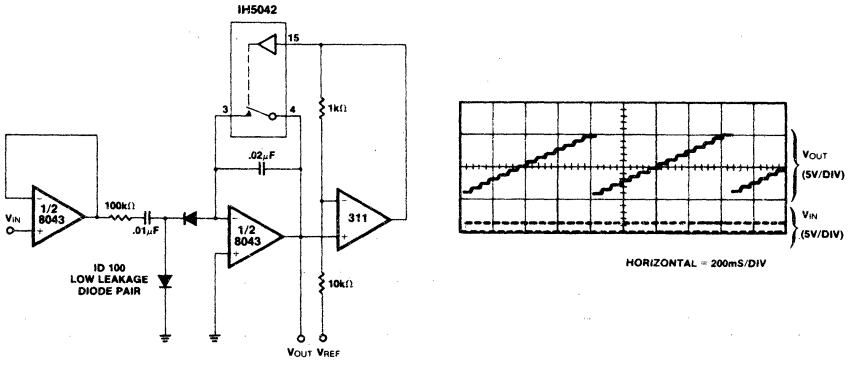


Figure 8: Analog Counter Circuit

STAIRCASE GENERATOR

The circuit shown in Figure 7 is a high input impedance version of the so-called "diode pump" or staircase generator. Note that charge transfer takes place at the negative-going edge of the input-signal.

The most common application for staircase generators is in low cost counters. By resetting the capacitor when the output reaches a predetermined level, the circuit may be made to count reliably up to a maximum of about 10. A straightforward circuit using a LM311 for the level detector, and a CMOS analog gate to discharge the capacitor, is shown in Figure 8. An important property of this type of counter is the ease with which the count can be changed; it is only necessary to change the voltage at which the comparator trips. A low cost A-D converter can also be designed using the same principle since the digital count between reset periods is directly proportional to the analog voltage used as a reference for the comparator.

A considerable amount of hysteresis is used in the comparator shown in Figure 8. This ensures that the capacitor is completely discharged during the reset period. In a more sophisticated circuit, a dual comparator "window detector" could be used, the lower trip point set close to ground to assure complete discharge. The upper trip point could then be adjusted independently to determine the pulse count.

SAMPLE & HOLD CIRCUIT

Two important properties of the 8043 are used to advantage in this circuit. The low input bias currents give rise to slow output decay rates ("droop") in the hold mode, while the high slew rate (6V/μs) improves the tracking speed and the response time of the circuit. See Figure 6.

The ability of the circuit to track fast moving inputs is shown in Figure 10A. The upper waveform is the input (10V/div), the lower waveform the output (5V/div). The logic input is high.

Actual sample and hold waveforms are shown in Figure 10B. The center waveform is the analog input, a ramp moving at about 67V/ms, the lower waveform is the logic input to the sample & hold; a logic "1" initiates the sample mode. The upper waveform is the output, displaced by about 1 scope division (2V) from the input to avoid superimposing traces. The hold mode, during which the output remains constant, is clearly visible. At the beginning of a sample period, the output takes about 8μs to catch up with the input, after which it tracks until the next hold period.

Note: All typical values have been guaranteed by characterization and are not tested.

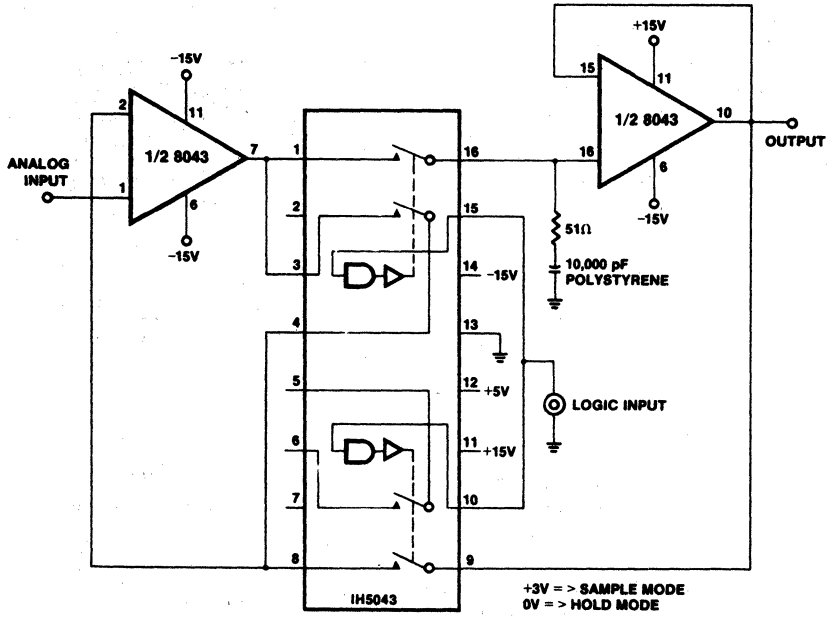
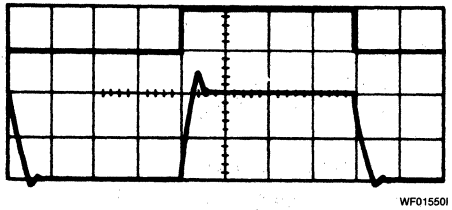
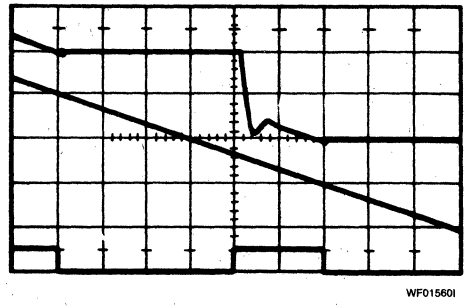


Figure 9: Sample And Hold Circuit



TOP: INPUT (10V/DIV)
BOTTOM: OUTPUT (5V/DIV)
HORIZONTAL: 10μs/DIV

Figure 10A



TOP: 2V/DIV
CENTER: 2V/DIV
BOTTOM: 10V/DIV
HORIZONTAL: 10μs/DIV

Figure 10B

Note: All typical values have been guaranteed by characterization and are not tested.

INSTRUMENTATION AMPLIFIER

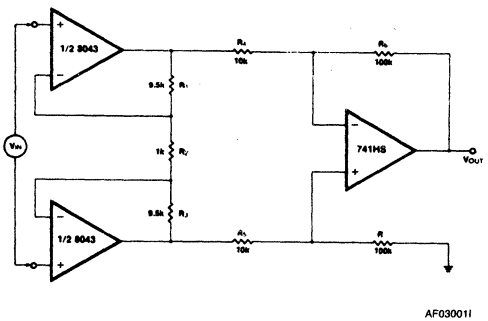
A dual JFET-input operational amplifier is an attractive component around which to build an instrumentation amplifier because of the high input resistance. The circuit shown in Figure 11 uses the popular triple op-amp approach. The output amplifier is a High Speed 741 (741 HS, slew rate guaranteed $\geq 0.7V/\mu s$) so that the high slew rate of the 8043 is utilized to the full extent. Input resistance of the circuit (either input, regardless of gain configuration) is in excess of 10^{12} ohms.

For the component values shown, the overall amplifier gain is 200 (front end gain = $\frac{2R_1 + R_2}{R_2}$, back end gain, = R_6/R_4).

Common mode rejection is largely determined by the matching between R_4 and R_5, and R_6 and R_7. In applications where offset nulling is required, a single potentiometer can be connected as shown in Figure 12.

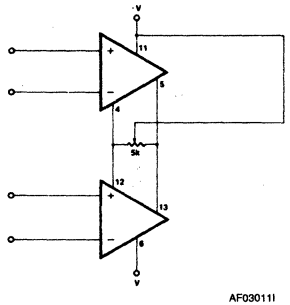
Another popular circuit is given in Figure 13. In this case the gain is $1 + R_1/R_2$, and the CMRR determined by the match between R_1 and R_4, R_2 and R_3.

For more information on FET input operational amplifiers, see Intersil Application Bulletin A005 "The 8007: A High Performance FET-input Operational Amplifier."



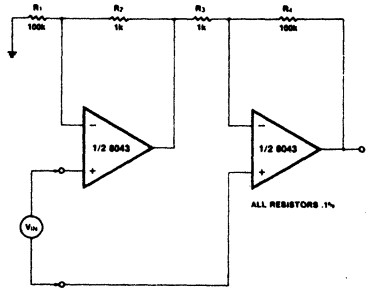
AF03001I

Figure 11: Instrumentation Amplifier



AF03011I

Figure 12: Offset Nulling Both Amplifiers With One Potentiometer



AF03021I

Figure 13: Modified Instrumentation Amplifier

4

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8048/ICL8049
Log/Antilog Amplifier

GENERAL DESCRIPTION

The 8048 is a monolithic logarithmic amplifier capable of handling six decades of current input, or three decades of voltage input. It is fully temperature compensated and is nominally designed to provide 1 volt of output for each decade change of input. For increased flexibility, the scale factor, reference current and offset voltage are externally adjustable.

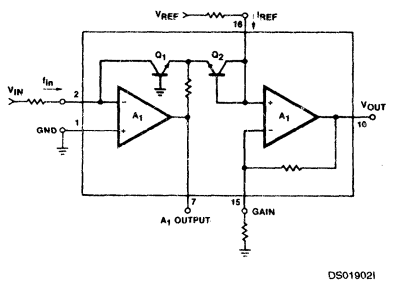
The 8049 is the antilogarithmic counterpart of the 8048; it nominally generates one decade of output voltage for each 1 volt change at the input.

FEATURES

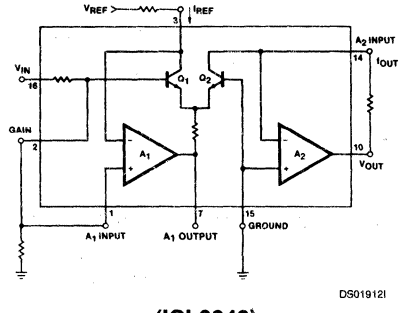
- **1/2% Full Scale Accuracy**
- **Temperature Compensated for 0°C to +70°C Operation**
- **Scale Factor 1V/Decade, Adjustable**
- **120dB Dynamic Current Range (8048)**
- **60dB Dynamic Voltage Range (8048 & 8049)**
- **Dual JFET-Input Op-Amps**

ORDERING INFORMATION

PART NUMBER	ERROR (25°C)	TEMPERATURE RANGE	PACKAGE
ICL8048BCJE	30mV	0°C to +70°C	16 Pin CERDIP
ICL8048BCPE	30mV	0°C to +70°C	16 Pin Plastic DIP
ICL8048CCJE	60mV	0°C to +70°C	16 Pin CERDIP
ICL8048CCPE	60mV	0°C to +70°C	16 Pin Plastic DIP
ICL8049BCJE	10mV	0°C to +70°C	16 Pin CERDIP
ICL8049BCPE	10mV	0°C to +70°C	16 Pin Plastic DIP
ICL8049CCJE	25mV	0°C to +70°C	16 Pin CERDIP
ICL8049CCPE	25mV	0°C to +70°C	16 Pin Plastic DIP

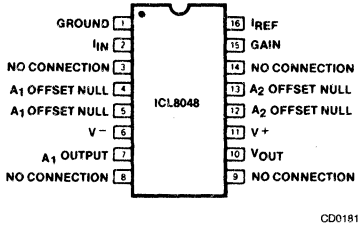


(ICL8048)



(ICL8049)

Figure 1: Functional Diagram



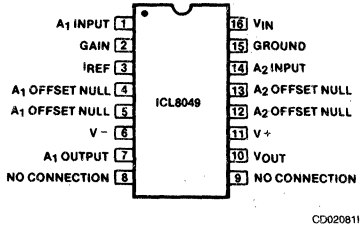


Figure 2: Pin Configurations (Outline Dwgs, JE, PE)

302800-002

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8048/ICL8049

INTERSIL

ABSOLUTE MAXIMUM RATINGS (ICL8048)

Supply Voltage ..... ±18V
I_{IN} (Input Current) 2mA
I_{REF} (Reference Current) 2mA
Voltage between Offset Null and V^+ ..... ±0.5V
Power Dissipation 750mW

Operating Temperature Range ..... 0°C to +70°C
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

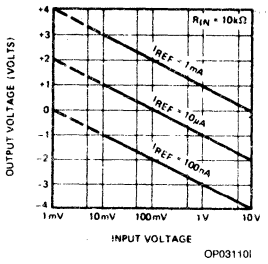
ELECTRICAL CHARACTERISTICS (ICL8048)

$V_S = \pm 15V$, $T_A = 25°C$, $I_{REF} = 1mA$, scale factor adjusted for 1V/decade unless otherwise specified.

PARAMETER	TEST CONDITIONS	8048BC			8048CC			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Dynamic Range I_{IN} (1nA – 1mA) V_{IN} (10mV – 10V)	 $R_{IN} = 10k\Omega$	 120 60			 120 60			 dB dB
Error, % of Full Scale	$T_A = 25°C$, $I_{IN} = 1nA$ to 1mA		.20	0.5		.25	1.0	%
Error, % of Full Scale	$T_A = 0°C$ to +70°C, $I_{IN} = 1nA$ to 1mA		.60	1.25		.80	2.5	%
Error, Absolute Value	$T_A = 25°C$, $I_{IN} = 1nA$ to 1mA		12	30		14	60	mV
Error, Absolute Value	$T_A = 0°C$ to +70°C $I_{IN} = 1nA$ to 1mA		36	75		50	150	mV
Temperature Coefficient of V_{OUT}	$I_{IN} = 1nA$ to 1mA		0.8			0.8		mV/°C
Power Supply Rejection Ratio	Referred to Output		2.5			2.5		mV/V
Offset Voltage (A_1 & A_2)	Before Nulling		15	25		15	50	mV
Wideband Noise	At Output, for $I_{IN} = 100\mu A$		250			250		μV(RMS)
Output Voltage Swing	$R_L = 10k\Omega$	±12	±14		±12	±14		V
	$R_L = 2k\Omega$	±10	±13		±10	±13		V
Power Consumption			150	200		150	200	mW
Supply Current			5	6.7		5	6.7	mA

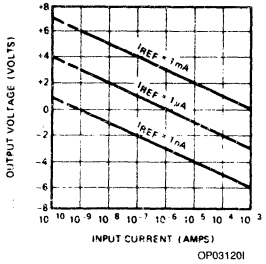
TYPICAL PERFORMANCE CHARACTERISTICS

TRANSFER FUNCTION FOR CURRENT INPUTS



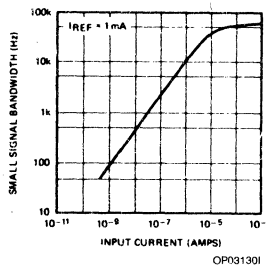
OP03110I

TRANSFER FUNCTION FOR VOLTAGE INPUTS



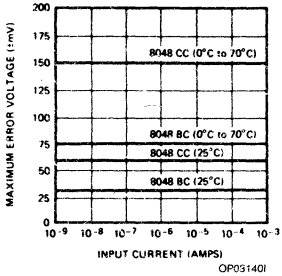
OP03120I

SMALL SIGNAL BANDWIDTH AS A FUNCTION OF INPUT CURRENT



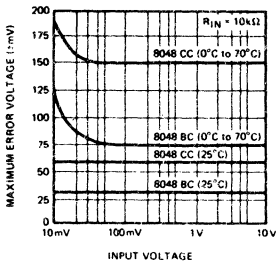
OP03130I

MAXIMUM ERROR VOLTAGE AT THE OUTPUT AS A FUNCTION OF INPUT CURRENT



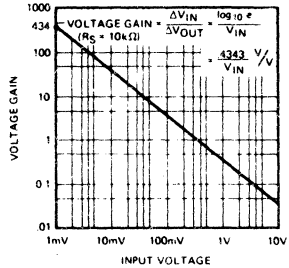
OP03140I

MAXIMUM ERROR VOLTAGE AT THE OUTPUT AS A FUNCTION OF INPUT VOLTAGE



OP03150I

SMALL SIGNAL VOLTAGE GAIN AS A FUNCTION OF INPUT VOLTAGE FOR $R_S = 10k\Omega$



OP03160I

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8048/ICL8049

INTERSIL

ABSOLUTE MAXIMUM RATINGS (ICL8049)

Supply Voltage ..... ±18V
V_{IN} (Input Voltage) ..... ±15V
I_{REF} (Reference Current) 2mA
Voltage between Offset Null and V^+ ..... ±0.5V
Power Dissipation 750mW

Operating Temperature Range ..... 0°C to +70°C
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

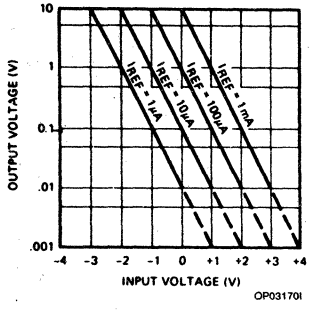
ELECTRICAL CHARACTERISTICS (ICL8049)

$V_S = \pm 15V$, $T_A = 25°C$, $I_{REF} = 1mA$, scale factor adjusted for 1 decade (out) per volt (in), unless otherwise specified.

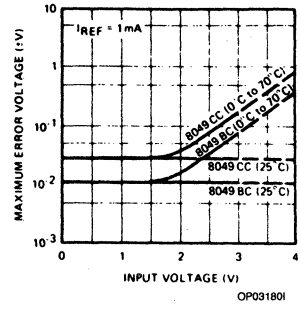
PARAMETER	TEST CONDITIONS	8049BC			8049CC			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Dynamic Range (V_{OUT})	V_{OUT} = 10mV to 10V	60			60			dB
Error, Absolute Value	$T_A = 25°C$, $0V \le V_{IN} \le 3V$		3	10		5	25	mV
Error, Absolute Value	$T_A = 0°C$ to +70°C, $0V \le V_{IN} \le 3V$		20	75		30	150	mV
Temperature Coefficient, Referred to V_{IN}	$V_{IN} = 3V$		0.38			0.55		mV/°C
Power Supply Rejection Ratio	Referred to Input, for $V_N = 0V$		2.0			2.0		μV/V
Offset Voltage (A_1 & A_2)	Before Nulling		15	25		15	50	mV
Wideband Noise	Referred to Input, for $V_{IN} = 0V$		26			26		μV(RMS)
Output Voltage Swing	$R_L = 10k\Omega$	±12	±14		±12	±14		V
	$R_L = 2k\Omega$	±10	±13		±10	±13		V
Power Consumption			150	200		150	200	mW
Supply Current			5	6.7		5	6.7	mA

TYPICAL PERFORMANCE CHARACTERISTICS

TRANSFER FUNCTION (V_{OUT} AS A FUNCTION OF V_{IN})



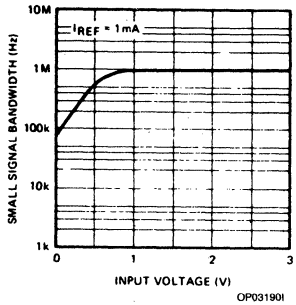
MAXIMUM ERROR VOLTAGE REFERRED TO THE INPUT AS A FUNCTION OF V_{IN}



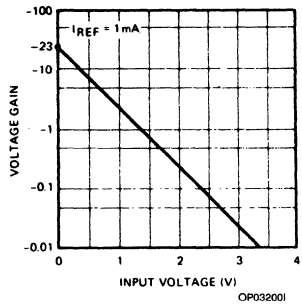
Note: All typical values have been guaranteed by characterization and are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

SMALL SIGNAL BANDWIDTH AS A FUNCTION OF INPUT VOLTAGE



SMALL SIGNAL VOLTAGE GAIN AS A FUNCTION OF INPUT VOLTAGE



ICL8048 DETAILED DESCRIPTION

The ICL8048 relies for its operation on the well-known exponential relationship between the collector current and the base-emitter voltage of a transistor:

$$I_C = I_S\left[e^{\,qV_{BE}/kT} - 1\right] \qquad (1)$$

For base-emitter voltages greater than 100mV, Eq. (1) becomes

$$I_C = I_S e^{qV_{BE}/kT} \qquad (2)$$

From Eq. (2), it can be shown that for two identical transistors operating at different collector currents, the V_{BE} difference (ΔV_{BE}) is given by:

$$\Delta V_{BE} = -2.303 \times \frac{kT}{q} \log_{10}\left[\frac{I_{C1}}{I_{C2}}\right] \qquad (3)$$

Referring to Figure 3, it is clear that the potential at the collector of Q_2 is equal to the ΔV_{BE} between Q_1 and Q_2. The output voltage is ΔV_{BE} multiplied by the gain of A_2:

$$V_{OUT} = -2.303\left(\frac{R_1 + R_2}{R_2}\right)\left(\frac{kT}{q}\right)\log_{10}\left[\frac{I_{IN}}{I_{REF}}\right] \qquad (4)$$

The expression $2.303 \times \frac{kT}{q}$ has a numerical value of 59mV at 25°C; thus in order to generate 1 volt/decade at the output, the ratio $(R_1 + R_2)/R_2$ is chosen to be 16.9 For this scale factor to hold constant as a function of temperature, the $(R_1 + R_2)/R_2$ term must have a 1/T characteristic to compensate for kT/q.

In the ICL8048 this is achieved by making R_1 a thin film resistor, deposited on the monolithic chip. It has a nominal value of 15.9kΩ at 25°C, and its temperature coefficient is carefully designed to provide the necessary compensation. Resistor R_2 is external and should be a low T.C. type; it should have a nominal value of 1kΩ to provide 1 volt/decade, and must have an adjustment range of ±20% to allow for production variations in the absolute value of R_1.

ICL8048 OFFSET AND SCALE FACTOR ADJUSTMENT*

A log amp, unlike an op-amp, cannot be offset adjusted by simply grounding the input. This is because the log of zero approaches minus infinity; reducing the input current to zero starves Q_1 of collector current and opens the feedback loop around A_1. Instead, it is necessary to zero the offset voltage of A_1 and A_2 separately, and then to adjust the scale factor. Referring to Figure 3, this is done as follows:

1) Temporarily connect a 10kΩ resistor (R_0) between pins 2 and 7. With no input voltage, adjust R_4 until the output of A_1 (pin 7) is zero. Remove R_0.
   Note that for a current input, this adjustment is not necessary since the offset voltage of A_1 does not cause any error for current-source inputs.
2) Set $I_{IN} = I_{REF} = 1mA$. Adjust R_5 such that the output of A_2 (pin 10) is zero.
3) Set $I_{IN} = 1\mu A$, $I_{REF} = 1mA$. Adjust R_2 for $V_{OUT} = 3$ volts (for a 1 volt/decade scale factor) or 6 volts (for a 2 volt/decade scale factor).

Step #3 determines the scale factor. Setting $I_{IN} = 1\mu A$ optimizes the scale factor adjustment over a fairly wide dynamic range, from 1mA to 1nA. Clearly, if the 8048 is to be used for inputs which only span the range 100μA to 1mA, it would be better to set $I_{IN} = 100\mu A$ in Step #3. Similarly, adjustment for other scale factors would require different I_{IN} and V_{OUT} values.

*See A053 for an automatic offset nulling circuit.

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Note: All typical values have been guaranteed by characterization and are not tested.

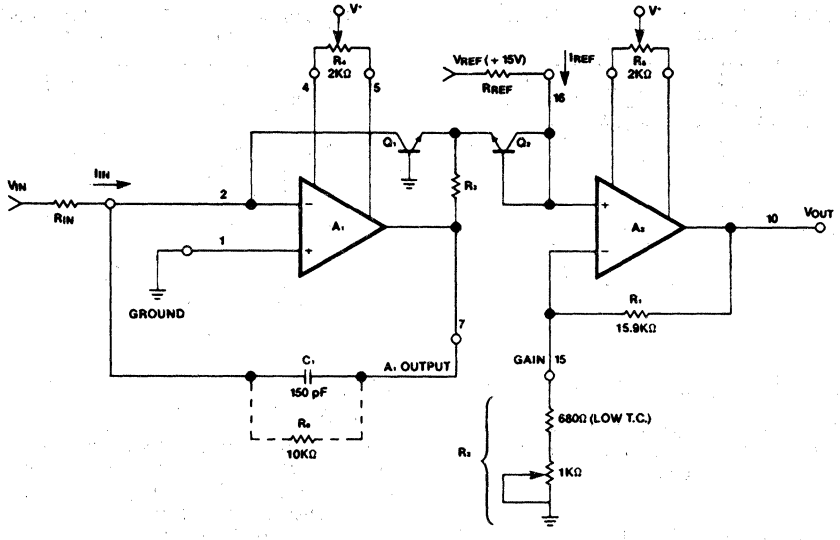

Figure 3: ICL8048 Offset and Scale Factor Adjustment

ICL8049 DETAILED DESCRIPTION

The ICL8049 relies on the same logarithmic properties of the transistor as the ICL8048. The input voltage forces a specific $\triangle V_{BE}$ between Q_1 and Q_2 (Figure 4). This V_{BE} difference is converted into a difference of collector currents by the transistor pair. The equation governing the behavior of the transistor pair is derived from (2) on the previous page and is as follows:

$$\frac{I_{C1}}{I_{C2}} = \exp\left[\frac{q\triangle V_{BE}}{kT}\right]$$

When numerical values for q/kT are put into this equation, it is found that a $\triangle V_{BE}$ of 59mV (at 25°C) is required to change the collector current ratio by a factor of ten. But for ease of application, it is desirable that a 1 volt change at the input generate a tenfold change at the output. The required input attenuation is achieved by the network comprising R_1 and R_2. In order that scale factors other than one decade per volt may be selected, R_2 is external to the chip. It should have a value of 1kΩ, adjustable ±20%, for one decade per volt. R_1 is a thin film resistor deposited on the monolithic chip; its temperature characteristics are chosen to compensate the temperature dependence of equation 5, as explained on the previous page.

The overall transfer function is as follows:

$$\frac{I_{OUT}}{I_{REF}} = \exp\left[\frac{-R_2}{(R_1 + R_2)} \times \frac{qV_{IN}}{kT}\right] \quad (6)$$

Substituting $V_{OUT} = I_{OUT} \times R_{OUT}$ gives:

$$V_{OUT} = R_{OUT}\, I_{REF} \exp\left[\frac{-R_2}{(R_1 + R_2)} \times \frac{qV_{IN}}{kT}\right] \quad (7)$$

For voltage references equation 7 becomes

$$V_{OUT} = V_{REF} \times \frac{R_{OUT}}{R_{REF}} \exp\left[\frac{-R_2}{(R_1 + R_2)} \times \frac{qV_{IN}}{kT}\right] \quad (8)$$

ICL8049 OFFSET AND SCALE FACTOR ADJUSTMENT*

As with the log amplifier, the antilog amplifier requires three adjustments. The first step is to null out the offset voltage of A_2. This is accomplished by reverse biasing the base-emitter of Q_2. A_2 then operates as a unity gain buffer with a grounded input. The second step forces $V_{IN} = 0$; the output is adjusted for $V_{OUT} = 10V$. This step essentially "anchors" one point on the transfer function. The third step applies a specific input and adjusts the output to the correct voltage. This sets the scale factor. Referring to Figure 4, the exact procedure for 1 decade/volt is as follows:

1) Connect the input (pin #16) to +15V. This reverse biases the base-emitter of Q_2. Adjust R_7 for $V_{OUT} = 0V$. Disconnect the input from +15V.
2) Connect the input to Ground. Adjust R_4 for $V_{OUT} = 10V$. Disconnect the input from Ground.
3) Connect the input to a precise 2V supply and adjust R_2 for $V_{OUT} = 100mV$.

The procedure outlined above optimizes the performance over a 3 decade range at the output (i.e., V_{OUT} from 10mV to 10V). For a more limited range of output voltages, for example 1V to 10V, it would be better to use a precise 1 volt supply and adjust for $V_{OUT} = 1V$. For other scale factors and/or starting points, different values for R_2 and R_{REF} will be needed, but the same basic procedure applies.

*See A053 for an automatic offset nulling circuit.

Note: All typical values have been guaranteed by characterization and are not tested.

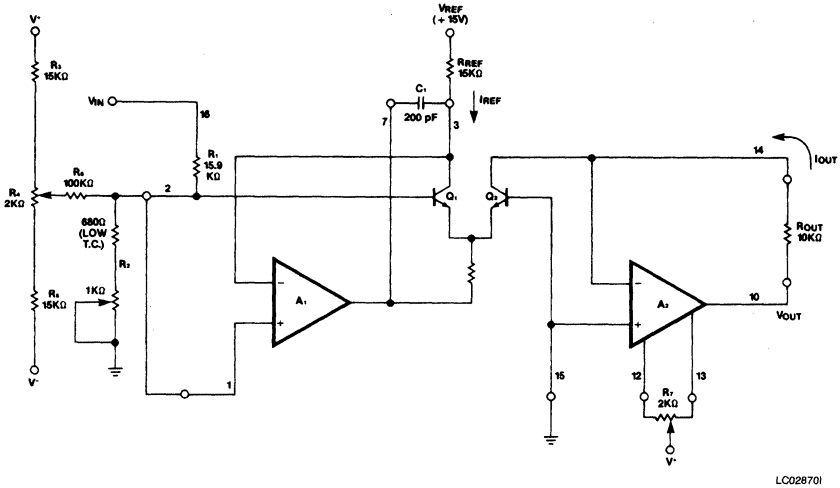

Figure 4: ICL8049 Offset and Scale Factor Adjustment

APPLICATIONS INFORMATION

ICL8048 Scale Factor Adjustment

The scale factor adjustment procedures outlined previously for the ICL8048 and ICL8049, are primarily directed towards setting up 1 volt (ΔV_{OUT}) per decade (ΔI_{IN} or ΔV_{IN}) for the log amp, or one decade (ΔV_{OUT}) per volt (ΔV_{IN}) for the antilog amp.

This corresponds to K = 1 in the respective transfer functions:

$$\text{Log Amp: } V_{OUT} = -K \log_{10}\left[\frac{I_{IN}}{I_{REF}}\right] \quad (9)$$

$$\text{Antilog Amp: } V_{OUT} = R_{OUT}\, I_{REF}\, 10^{\frac{-V_{IN}}{K}} \quad (10)$$

By adjusting R_2 (Figure 3 and Figure 4) the scale factor "K" in equation 9 and 10 can be varied. The effect of changing K is shown graphically in Figure 5 for the log amp, and Figure 6 for the antilog amp. The nominal value of R_2 required to give a specific value of K can be determined from equation 11. It should be remembered that R_1 has a ±20% tolerance in absolute value, so that allowance shall be made for adjusting the nominal value of R_2 by ±20%.

$$R_2 = \frac{941}{(K - .059)}\ \Omega \quad (11)$$

Frequency Compensation

Although the op-amps in both the ICL8048 and the ICL8049 are compensated for unity gain, some additional frequency compensation is required. This is because the log transistors in the feedback loop add to the loop gain. In the 8048, 150 pF should be connected between Pins 2 and 7 (Figure 3). In the 8049, 200 pF between Pins 3 and 7 is recommended (Figure 4).

EFFECT OF VARYING "K" ON THE LOG AMPLIFIER

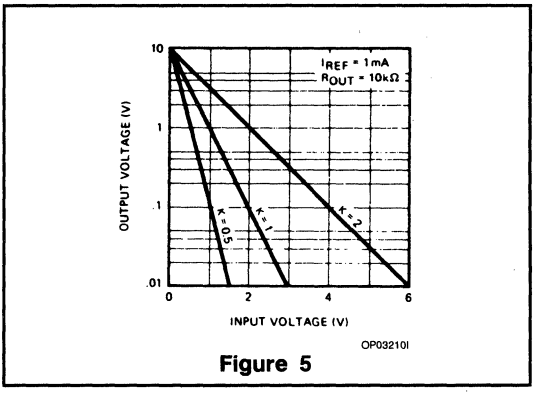

Figure 5

EFFECT OF VARYING "K" ON THE ANTILOG AMPLIFIER

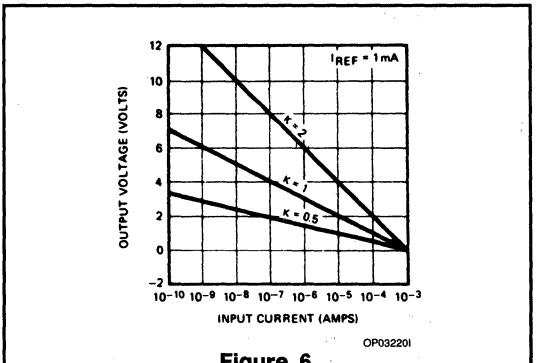

Figure 6

Note: All typical values have been guaranteed by characterization and are not tested.

Error Analysis

Performing a meaningful error analysis of a circuit containing log and antilog amplifiers is more complex than dealing with a similar circuit involving only op-amps. In this data sheet every effort has been made to simplify the analysis task, without in any way compromising the validity of the resultant numbers.

The key difference in making error calculations in log/antilog amps, compared with op-amps, is that the gain of the former is a function of the input signal level. Thus, it is necessary, when referring errors from output to input, or vice versa, to check the input voltage level, then determine the gain of the circuit by referring to the graphs given in the Typical Performance Characteristics section.

The various error terms in the log amplifier, the ICL8048, are Referred To the Output (RTO) of the device. The error terms in the antilog amplifier, the ICL8049, are Referred To the Input (RTI) of the device. The errors are expressed in this way because in the majority of systems a number of log amps interface with an antilog amp, as shown in Figure 7.

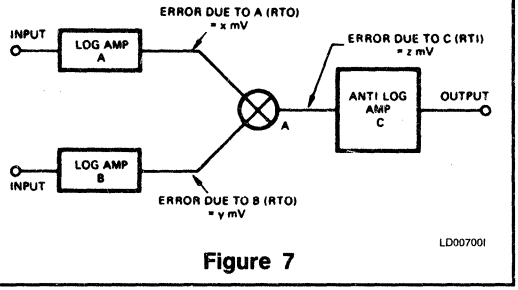

Figure 7

It is very straightforward to estimate the system error at node (A) by taking the square root of the sum-of-the squares of the errors of each contributing block.

$$\text{Total Error} = \sqrt{x^2 + y^2 + z^2} \quad \text{at (A)}$$

If required, this error can be referred to the system output through the voltage gain of the antilog circuit, using the voltage gain versus input voltage plot.

The numerical values of x, y, and z in the above equation are obtained from the maximum error voltage plots. For example, with the ICL8048BC, the maximum error at the output is 30mV at 25°C. This means that the measured output will be within 30mV of the theoretical transfer function, provided the unit has been adjusted per the procedures described previously. Figure 8 illustrates this point.

To determine the maximum error over the operating temperature range, the 0 to 70°C absolute error values given in the table of electrical characteristics should be used. For intermediate temperatures, assume a linear increase in the error between the 25°C value and the 70°C value.

For the antilog amplifier, the only difference is that the error refers to the input, i.e., the horizontal axis. It will be noticed that the maximum error voltage of the ICL8049, over the temperature range, is strongly dependent on the input voltage. This is because the output amplifier, A_2, has an offset voltage drift which is directly transmitted to the output. When this error is referred to the input, it must be divided by the voltage gain, which is input voltage dependent. At $V_{IN} = 3V$, for example, errors at the output are multiplied by 1/.023 (= 43.5) when referred to the input.

TRANSFER FUNCTION FOR CURRENT INPUTS

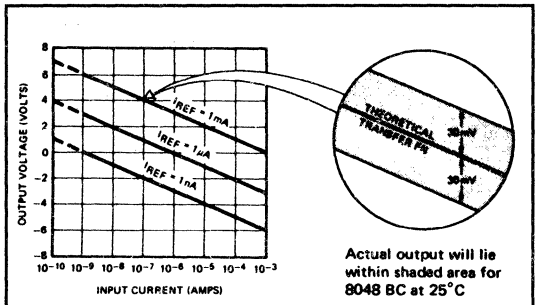

Figure 8

It is important to note that both the ICL8048 and the ICL8049 require positive values of I_{REF}, and the input (ICL8048) or output (ICL8049) currents (or voltages) respectively must also be positive. Application of negative I_{IN} to the ICL8048 or negative I_{REF} to either circuit will cause malfunction, and if maintained for long periods, would lead to device degradation. Some protection can be provided by placing a diode between pin 7 and ground.

SETTING UP THE REFERENCE CURRENT

In both the ICL8048 and the ICL8049 the input current reference pin (I_{REF}) is not a true virtual ground. For the ICL8048, a fraction of the output voltage is seen on Pin 16 (Figure 3). This does not constitute an appreciable error provided V_{REF} is much greater than this voltage. A 10V or 15V reference satisfies this condition. For the ICL8049, a fraction of the input voltage appears on Pin 3 (Figure 4), placing a similar restraint on the value of V_{REF}.

Alternatively, I_{REF} can be provided from a true current source. One method of implementing such a current source is shown in Figure 9.

LOG OF RATIO CIRCUIT, DIVISION

The 8048 may be used to generate the log of a ratio by modulating the I_{REF} input. The transfer function remains the same, as defined by equation 9:

$$V_{OUT} = -K\log_{10}\left[\frac{I_{IN}}{I_{REF}}\right] \qquad (9)$$

Clearly it is possible to perform division using just one ICL8048, followed by an ICL8049. For multiplication, it is generally necessary to use two log amps, summing their outputs into an antilog amp.

To avoid the problems caused by the I_{REF} input not being a true virtual ground (discussed in the previous section), the circuit of Figure 9 is again recommended if the I_{REF} input is to be modulated.

Note: All typical values have been guaranteed by characterization and are not tested.

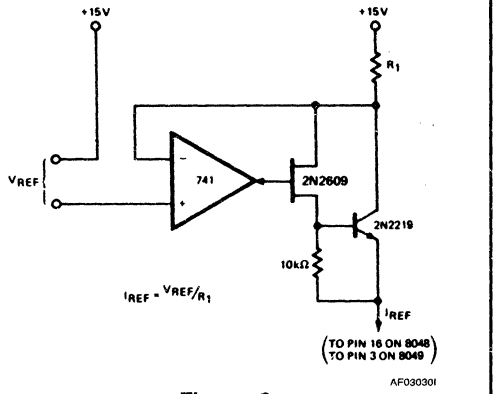

Figure 9

DEFINITION OF TERMS

In the definitions which follow, it will be noted that the various error terms are referred to the output of the log amp, and to the input of the antilog amp. The reason for this is explained on the previous page.

DYNAMIC RANGE The dynamic range of the ICL8048 refers to the range of input voltages or currents over which the device is guaranteed to operate. For the ICL8049 the dynamic range refers to the range of output voltage over which the device is guaranteed to operate.

ERROR, ABSOLUTE VALUE The absolute error is a measure of the deviation from the theoretical transfer function, after performing the offset and scale factor adjustments as outlined, (ICL8048) or (ICL8049). It is expressed in mV and referred to the linear axis of the transfer function plot. Thus, in the case of the ICL8048, it is a measure of the deviation from the theoretical output voltage for a given input current or voltage. For the ICL8049 it is a measure of the deviation from the theoretical input voltage required to generate a specific output voltage.

The absolute error specification is guaranteed over the dynamic range.

ERROR, % OF FULL SCALE The error as a percentage of full scale can be obtained from the following relationship:

$$\text{Error, \% of Full Scale} = \frac{100 \times \text{Error, absolute value}}{\text{FullScale Output Voltage}}$$

TEMPERATURE COEFFICIENT OF V_{OUT} OR V_{IN} For the ICL8048 the temperature coefficient refers to the drift with temperature of V_{OUT} for a constant input current.

For the ICL8049 it is the temperature drift of the input voltage required to hold a constant value of V_{OUT}.

POWER SUPPLY REJECTION RATIO The ratio of the voltage change in the linear axis of the transfer function (V_{OUT} for the ICL8048, V_{IN} for the ICL8049) to the change in the supply voltage, assuming that the log axis is held constant.

WIDEBAND NOISE For the ICL8048, this is the noise occurring at the output under the specified conditions. In the case of the ICL8049, the noise is referred to the input.

SCALE FACTOR For the log amp, the scale factor (K) is the voltage change at the output for a decade (i. e. 10:1) change at the input. For the antilog amp, the scale factor is the voltage change required at the input to cause a one decade change at the output. See equations 9 and 10.

APPLICATION NOTES

For further applications assistance, see

A007 "The ICL8048/8049 Monolithic Log-Antilog Amplifiers", by Ray Hendry

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Note: All typical values have been guaranteed by characterization and are not tested.

ICL8063
Power Transistor Driver/Amplifier

GENERAL DESCRIPTION

The ICL8063 is a unique monolithic power transistor driver and amplifier that allows construction of minimum chip power amplifier systems. It includes built in safe operating area circuitry, short circuit protection and voltage regulators, and is primarily intended for driving complementary output stages.

Designed to operate with all varieties of operational amplifiers and other functions, two external power transistors, and 8 to 10 passive components, the ICL8063 is ideal for use in such applications as linear and rotary actuator drivers, stepper motor drivers, servo motor drivers, power supplies, power DACs and electronically controlled orifices.

The ICL8063 takes the output levels (typically ±11V) from an op amp and boosts them to ±30V to drive power transistors, (e.g. 2N3055 (NPN) and 2N3789 (PNP)). The outputs from the ICL8063 supply up to 100mA to the base leads of the external power transistors.

The amplifier-driver contains internal positive and negative regulators, to power an op amp or other device; thus, only ±30V supplies are needed for a complete power amp.

FEATURES

- **Converts ±12V Outputs From Op Amps and Other Linear Devices to ±30V Levels**
- **When Used in Conjunction With General-Purpose Op Amps and External Complementary Power Transistors, System Can Deliver > 50 Watts to External Loads**
- **Built-in Safe Area Protection and Short-Circuit Protection**
- **Produces 25mA Quiescent Current in Power Output Stage**
- **Built-in ±13V Regulators to Power Op Amps or Other External Functions**
- **500kΩ Input Impedance With R_{BIAS} = 1MΩ**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL8063MJE	−55°C to +125°C	CERDIP
ICL8063CJE	0°C to +70°C	CERDIP
ICL8063CPE	0°C to +70°C	PLASTIC DIP

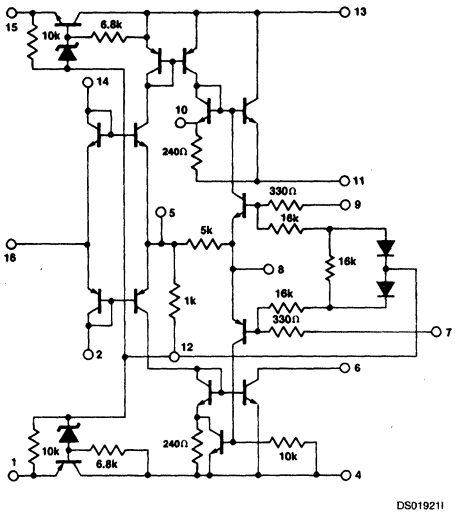


Figure 1: Functional Diagram

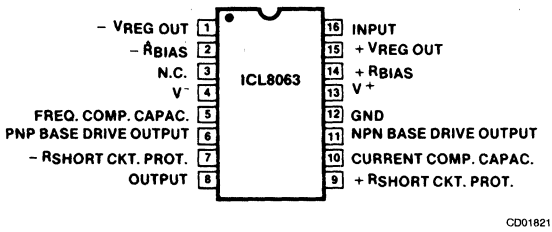


Figure 2: Pin Configuration

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8063

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±35V
Power Dissipation 500mW
Input Voltage (Note 1) ..... ±30V
Regulator Output Currents 10mA

Operating Temperature Range
ICL8063MJE ..... −55°C to +125°C
ICL8063CPE ..... 0°C to +70°C
ICL8063CJE ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{SUPPLY} = ±30V)

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	MIN/MAX LIMITS						UNIT
			ICL8063M			ICL8063C			
			−55°C	+25°C	+125°C	0°C	+25°C	+70°C	
V_{OS}	Max. Offset Voltage	See Figure 3	150	50	50		75		mV
I_{OH}	Min. Positive Drive Current	See Figure 4	50	50	50		40		mA
I_{OQ}	Max. Positive Output Quiescent Current	See Figure 5	500	250	250		300		µA
I_{OL}	Min. Negative Drive Current	See Figure 4	25	25	25		20		mA
I_{QL}	Max. Negative Output Quiescent Current	See Figure 6	500	250	250		300		µA
V_{REG}	Regulator Output Voltages Range		±13.7 ±1.2V	±13.7 ±1.0V	±13.7 ±1.5V	±13.7 ±1.0V	±13.7 ±1.0V	±13.7 ±1.0 V	V
I_{REG}	Regulator Output Current	(See Note 2)	10	10			10		mA
Z_{IN}	A.C. Input Impedance	See Figure 8		400 (Typ)			400 (Typ)		kΩ
V_{SUPPLY}	Power Supply Range		±5 to ±35V						V
I_Q	Power Supply Quiescent Currents		10	6	6		7		mA
A_V	Range of Voltage Gain	See Figure 9 V_{IN} = 8Vp-p	6±2	6±2	6±2		6±2		V/V
$V_{OUT(MIN)}$	Minimum Output Swing	See Figure 9; Increase V_{IN} until V_{OUT} flattens	±27	±27	±27		±27		V
I_{BIAS}	Input Bias Current	See Figure 10	100	100	100		100		µA

NOTES: 1. For supply voltages less than ±30V the absolute maximum input voltage is equal to the supply voltage.
2. Care should be taken to ensure that maximum power dissipation is not exceeded.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8063

TEST CIRCUITS

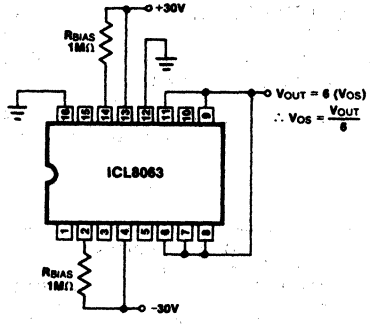
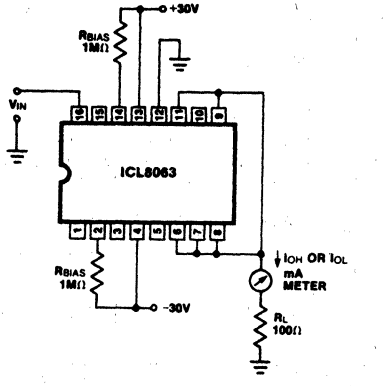


Figure 3: Offset Voltage Measurement



FOR I_{OUT}: V_{IN} IS POSITIVE: INCREASE V_{IN} UNTIL I_{OUT} LIMITS
FOR I_{OUT}: V_{IN} IS NEGATIVE: INCREASE V_{IN} UNTIL I_{OUT} LIMITS

Figure 4: Output Current Measurement

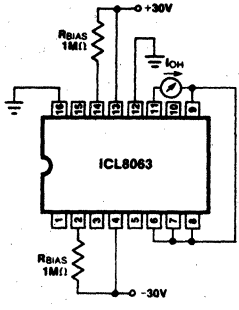


Figure 5: Positive Output Quiescent Current

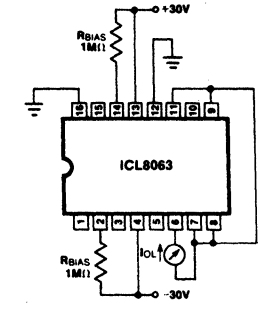


Figure 6: Negative Output Quiescent Current

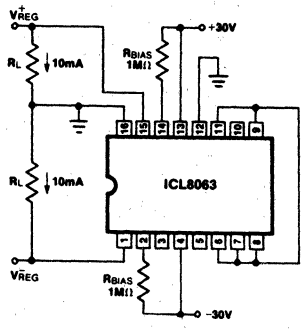


Figure 7: On Chip Regulator Measurement

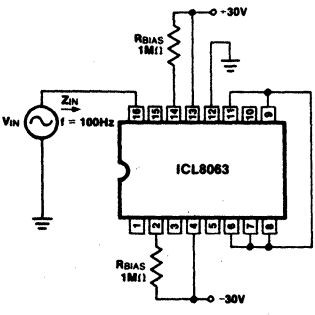


Figure 8: A.C. Input Impedance Measurement

Note: All typical values have been guaranteed by characterization and are not tested.

TEST CIRCUITS (CONT.)

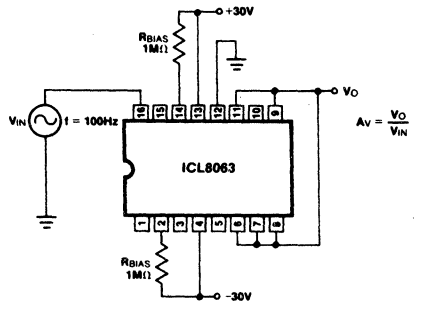


Figure 9: Gain and Output Voltage Swing Measurement

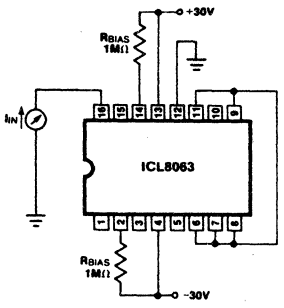


Figure 10: Input Bias Current Measurement

APPLICATIONS INFORMATION

One problem faced almost every day by circuit designers is how to interface the low voltage, low current outputs of linear and digital devices to that of power transistors and darlingtons.

For example, a low level op amp has a typical output voltage range of ±6 to ±12V, and output current usually on the order of about 5 milliamperes. A power transistor with a ±35 volt supply, a collector current of 5 amperes, and a beta, or gain of 100 needs at least 50 milliamperes of drive.

In the past, connecting two transistors with widely dissimilar requirements meant that a rather ornate discrete circuit had to be built to convert the weak output signals from the first into levels large enough to drive the second. However, in addition to converting voltage and current, it was also necessary to include a number of protection circuits to guard against damage from shorts, for example, and all this design work was both tedious and expensive.

The ICL8063 provides a solution to these problems. It's a monolithic power transistor driver and power transistor amplifier circuit on the same chip, has all the necessary safe operating area circuitry and short circuit protection, and has on-chip ±13V voltage regulators to eliminate the need for extra external power supplies.

Using the ICL8063 to make a complete Power Amplifier

As Figure 11 shows, using the ICL8063 allows the circuit designer to build a power amplifier block capable of delivering ±2 amperes at ±25 volts (50 watts) to any load, with only three additional discrete devices and 8 passive components. Moreover, the circuit draws only about ±30 milliamperes of quiescent current from either of the ±30V power supplies. A similar design using discrete components would require anywhere from 50 to 100 components.

Slew rate is about the same as that of a 741 op amp, approximately 1V/μs. Input current, voltage offset, CMRR and PSRR are also the same. Use of 1,000 picofarad compensation capacitors (three in this configuration) allows good stability down to unity gain non-inverting (the worst case). This circuit will drive a 1000pF C_L to Gnd, or in other words, the circuit can drive 30 feet of RG-58 coaxial cable for line driver applications with no problems.

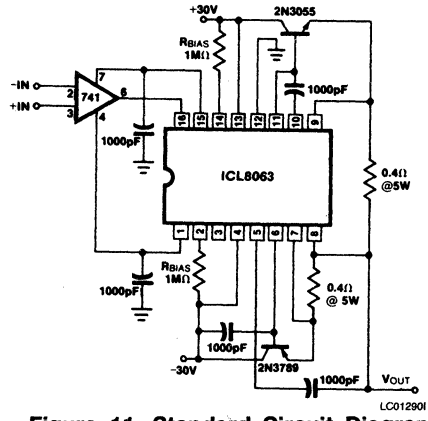


Figure 11: Standard Circuit Diagram

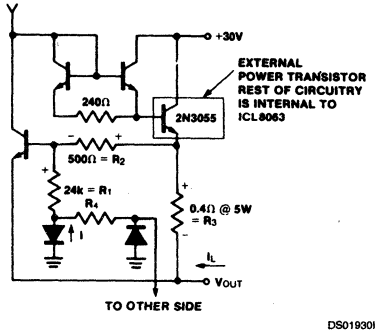


Figure 12: Current Limiting (Safe Area) Protection Circuit (one side shown)

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8063

As Figure 12 indicates, setting up a current limiting (safe area) protection circuit is straightforward. The 0.4 ohm, 5 watt resistors set the maximum current one can get out of the output. The equation this SOA circuit follows is: for V_{OUT} positive,

$$V_{be} = I_L R_3 - \frac{R_2}{R_1 + R_2}(V_{OUT} + I_L R_3 - 0.7V)$$

$$\approx I_L R_3 - \frac{R_2}{R_1 + R_2}(V_{OUT})$$

for V_{OUT} negative,

$$V_{be} = I_L R_3 - \frac{R_2}{R_1 + R_2 + R_4}(V_{OUT} + I_2 R_3 + 0.7)$$

$$\approx I_L R_3 - \frac{R_2}{R_1 + R_2 + R_4}(V_{OUT})$$

Solving these equations we get the following:

V_{OUT}	I	I_L @ 25°C	I_L @ 125°C
24V	1mA	3 amps	2.4 amps
20V	830μA	2.8 amps	
16V	670μA	2.6 amps	
12V	500μA	2.4 amps	1.8 amps
8V	333μA	2.1 amps	
4V	167μA	1.9 amps	
0V	0μA	1.7 amps	1.1 amps

As this table indicates, maximum power delivered to a load is obtained when $V_{OUT} \geq 24V$.

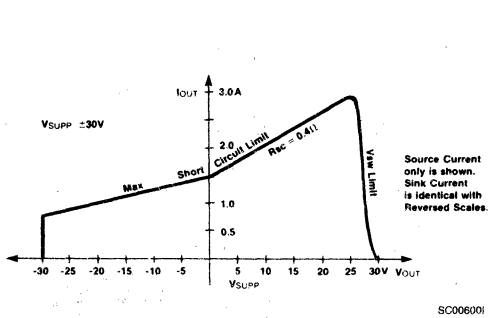
Often design requirements necessitate an unsymmetrical output current capability. In that case, instead of the 0.4 ohm resistors protecting the npn and pnp output stages, as shown in Figure 11, simply substitute any other value. For example, if up to 3 amps are required when $V_{OUT} \geq +24V$ and only 1 amp out when $V_{OUT} \geq -24V$, use a 0.4 ohm resistor between pin 8 and pin 9 on the ICL8063 and a 1 ohm, 2 watt resistor between pin 7 and pin 8. Maximum output current versus V_{OUT} for varying values of protection resistors are as follows:

V_{OUT}	0.4Ω @ 25°C	0.68Ω @ 25°C	1Ω @ 25°C
24V	3 amps	1.7 amps	1.2 amps
12V	2.4 amps	1.4 amps	0.9 amps
0V	1.7 amps	1.0 amps	0.7 amps

The biasing resistors located between pin 13 and pin 14 and between pin 2 and pin 4 are typically 1mΩ for $V_{SUPPLY} = \pm 30V$, which guarantees adequate performance in such applications as DC motor drivers, power DACs, programmable power supplies and line drivers (with ±30 volt supplies). The table that follows shows the proper value for R_{BIAS} for optimum output current capability with supply voltages between ±5V and ±30V.

$\pm V_{CC}$	R_{BIAS}
30V	1 MΩ
25V	680kΩ
20V	500kΩ
15V	300kΩ
10V	150kΩ
5V	62kΩ

If 30V and 1MΩ are used, performance curves appear as shown in Figure 13.



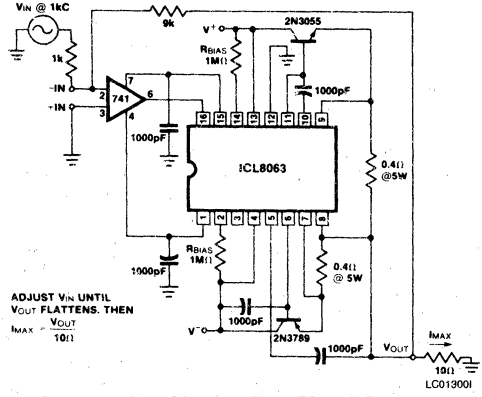
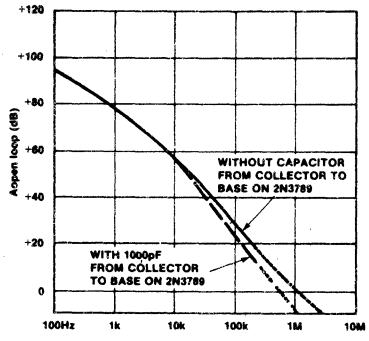


Figure 13: Typical Performance Curve of Max. Output Current Vs. V_{SUPP} For Fixed R_{BIAS} = 1MΩ

Note: All typical values have been guaranteed by characterization and are not tested.



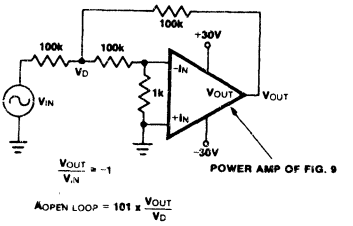
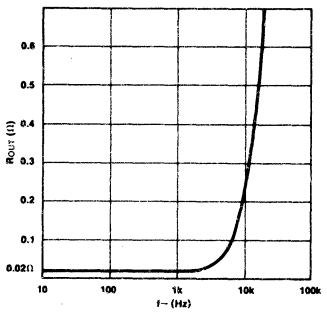


Figure 14: Bode Plot of Open Loop Gain of Above Schematic



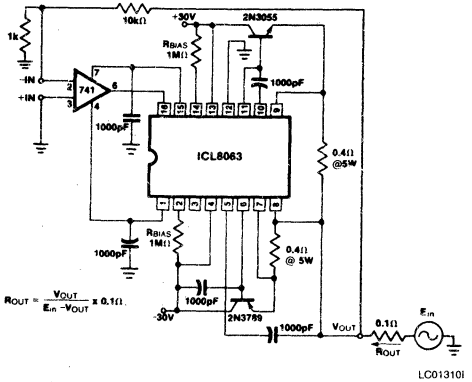


Figure 15: Typical Performance of R_{OUT} vs. Frequency of Power Amplifier System

When buying external power transistors, careful attention should be paid to beta values. For 2N3055 and 2N3789 transistors used in this circuit, beta should be no more than 150 max at I_C = 20mA and V_{CE} = 30V. This beta value sets the quiescent current at less than 30mA when not delivering power to a load.

The design in Figure 11 will tolerate a short circuit to ground indefinitely, provided adequate heat sinking is used.

However if V_{OUT} is shunted to ±30V the output transistors (2N3055 and 2N3789) will be destroyed, but since the safe operating area for these devices is 4 amps at 30 volts, the problem does not occur for V_{SUPP} = ±15V.

A typical bode plot of the power amplifier system open-loop frequency-response is shown in Figure 14. Referring to Figure 8, the schematic for this bode plot is shown in Figure 14.

Designing A Simple Function Generator

Using a variation of the fundamental power amplifier building block described in the previous section, the ICL8063 can be used in the design of a simple, low cost function generator (Figure 16). It will supply sine waves, triangular waves and square waves from 2 hertz to 20 kilohertz. This complete test instrument can be plugged into a standard 110VAC line for power. V_{OUT} will be up to ±25V (50V p-p) across loads as small as 10 ohms (about 2.5 amps maximum output current).

Capacitor working voltages should be greater than 50V DC and all resistors should be 1/2W, unless otherwise indicated. The interconnecting leads from the 741 pins 2 and 3 to their respective resistors should be kept short, less than 2 inches if possible; longer leads may result in oscillation.

Full output swing is possible to about 5kHz; after that the output begins to taper off due to the slew rate of the 741, until at 20kHz the output swing will be about $20V_{pp}$ (±10V). This problem can be remedied by simply using an op amp with a higher slew rate, such as the LF356.

Note: All typical values have been guaranteed by characterization and are not tested.

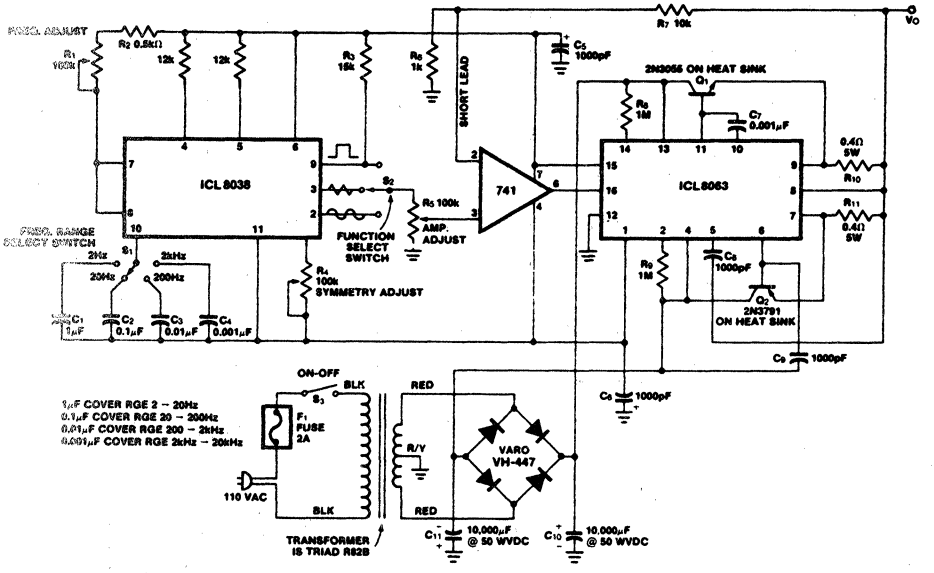


Figure 16: Power Function Generator

Building a Constant Current Motor Drive Circuit

The constant current motor drive configuration shown in Figure 17 is an extremely simple circuit to construct using the ICL8063. This minimum device circuit can be used to drive DC motors where there is some likelihood of stalling or lock up; if the motor locks, the current drive remains constant and the system does not destroy itself. Using this approach two 6V batteries are sufficient for good performance. A 10 volt input will produce one amp of output current to drive the motor, and if the motor is stalled, I_{OUT} remains at 1 amp.

For example, suppose it is necessary to drive a 24V DC motor with 1 amp of drive current. First make V_{SUPPLY} at least 6 volts more than the motor being driven (in this case 30 volts). Next select R_{BIAS} according to V_{SUPPLY} from the data sheet, which indicates $R_{BIAS} = 1M\Omega$. Then choose R_1, R_2, and R_a for optimum sensitivity. That means making $R_a = 1\Omega$ to minimize the voltage drop across R_a (the drop will be 1 amp x 1 ohm or 1 volt). If 1 amp/volt sensitivity is desirable let $R_2 = R_1 = 10k\Omega$ to minimize feedback current error. Then a ±1V input voltage will produce a ±1 amp current through the motor.

Capacitors should be at least 50 volts working voltage and all resistors 1/2W, except for those valued at 0.4 ohms. Power across $R_a = I \times V = 1$ amp x 1 volt = 1 watt, so at least a 2 watt value should be used. Use large heat sinks for the 2N3055 and 2N3791 power transistors. A Delta NC-641 or the equivalent is appropriate. Use a thermal compound when mounting the transistor to the heat sink. (See Intersil ICH8510 data sheet for further information).

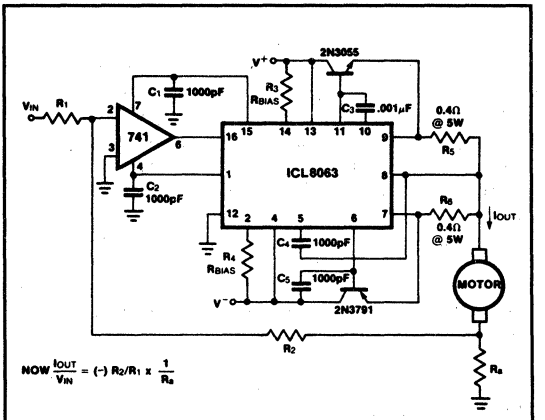


Figure 17: Constant Current Motor Drive

Building A Low Cost 50 Watt per Channel Audio Amplifier

For about $20 per channel, it is possible to build a high fidelity amplifier using the ICL8063 to drive 8 ohm speakers.

Note: All typical values have been guaranteed by characterization and are not tested.

A channel is defined here as all amplification between turntable or tape output and power output. (Figure 18)

The input 741 stage is a preamplifier with R.I.A.A. equalization for records. Following the first 741 stage is a 10kΩ control pot, whose wiper arm feeds into the power amplifier stage consisting of a second 741, the ICL8063 and the power transistors. To achieve good listening results, selection of proper resistance values in the power amplifier stage is important. Best listening is to be found at a gain value of 6 [(5kΩ + 1kΩ/1kΩ = 6)]. 3 is a practical minimum, since the first stage 741 preamp puts out only ±10 volt maximum signals, and if maximum power is necessary this value must be multiplied by 3 to get ±30 volt levels at the output of the power amp stage.

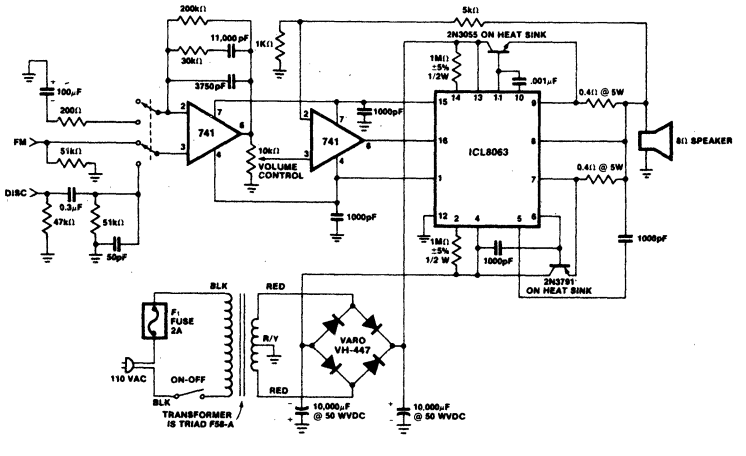
Each channel delivers about 56 volts p-p across an 8 ohm speaker and this converts to 50 watts RMS power. This is derived as follows:

$$\text{Power} = \frac{V_{rms}^2}{8\ \text{ohms}},\quad V_{rms} = \frac{56V_{P\text{-}P}}{2.82} = 20V,\quad (20V)^2 = 400V^2$$

$$\therefore\ \text{Power} = \frac{400V^2}{8\ \text{ohms}} = 50\ \text{watts RMS Power.}$$

Distortion will be < 0.1% up to about 100Hz, and then it increases as the frequency increases, reaching about 1% at 20kHz.

The ganged switch at the input is for either disc playing or FM, either from an FM tuner or a tape amplifier. Assuming DC coupling on the outputs, there is no need for a DC reference to ground (resistor) for FM position. To clear the signal in the FM position, place a 51kΩresistor to ground as shown in Figure 18 (from FM input position to ground).



BD00760I

Figure 18: Hi-Fi Amplifier

Note: All typical values have been guaranteed by characterization and are not tested.

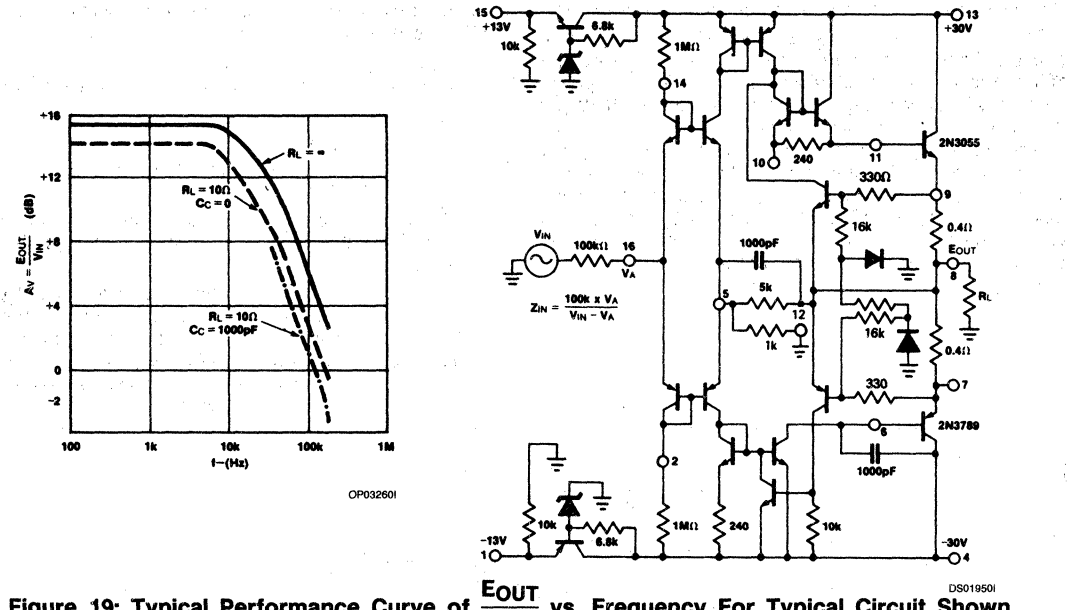


Figure 19: Typical Performance Curve of $\frac{E_{OUT}}{V_{IN}}$ vs. Frequency For Typical Circuit Shown

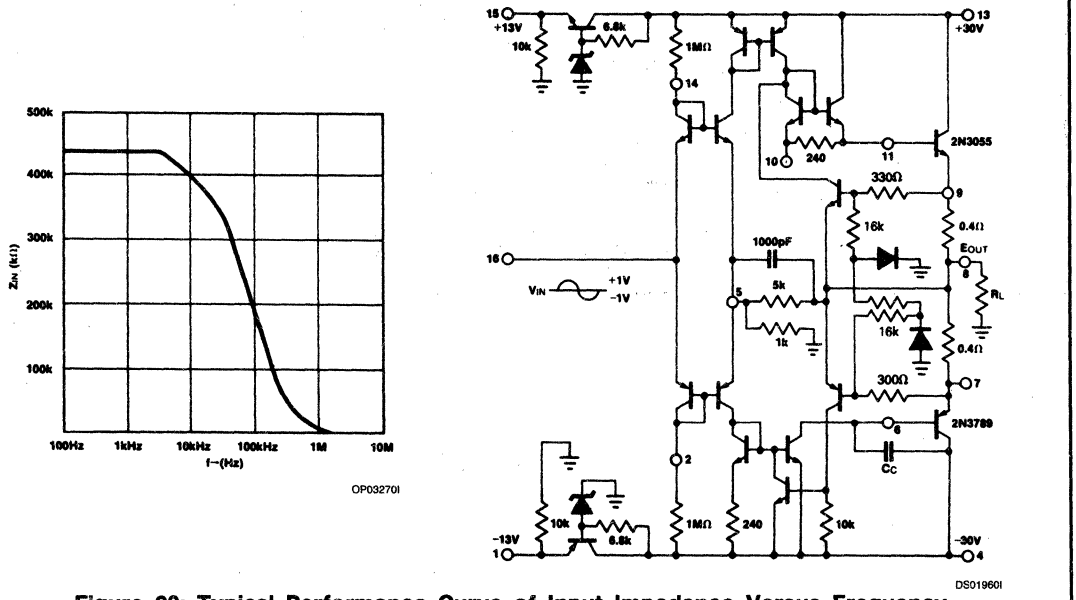


Figure 20: Typical Performance Curve of Input Impedance Versus Frequency for Typical Circuit Shown

Note: Intersil offers a hybrid power amplifier similar to that shown in Figure 11. See ICH8510/8520/8530 data sheet for details.

Note: All typical values have been guaranteed by characterization and are not tested.

LH2108/LH2308
Dual Super-Beta Operational Amplifier

GENERAL DESCRIPTION

The LH2108A/LH2308A and LH2108/LH2308 series of dual operational amplifiers consist of two LM108A or LM108 type op amps in a single hermetic package. Featuring all the same performance characteristics of the single device, these duals also offer closer thermal tracking, lower weight, and reduced insertion cost.

FEATURES

- **Low Offset Current — 50pA**
- **Low Offset Voltage — 0.7mV**
- **Low Offset Voltage**
  LH2108A: 0.3mV
  LH2108: 0.7mV
- **Wide Input Voltage Range — ±15V**
- **Wide Operating Supply Range — ±3V to ±20V**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
LH2108D	−55°C to +125°C	16-PIN CERAMIC
LH2108AD	−55°C to +125°C	
LH2308D	0°C to +70°C	
LH2308AD	0°C to +70°C	

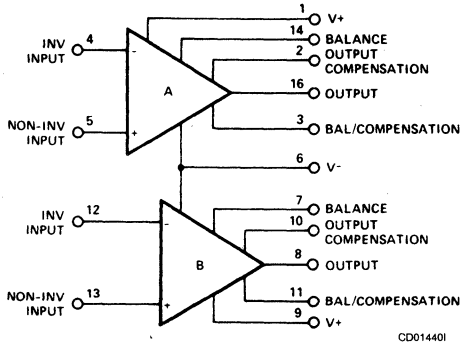


Figure 1: Functional Diagram

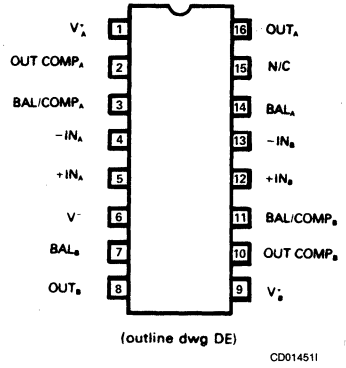


Figure 2: Pin Configuration

Note: All typical values have been guaranteed by characterization and are not tested.

LH2108/LH2308

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Power Dissipation (Note 1) 500mW
Differential Input Current (Note 2) ..... ±10mA
Input Voltage (Note 3) ..... ±15V
Output Short Circuit Duration ..... Continuous

Operating Temperature Range
LH2108A/LH2108 ..... −55°C to +125°C
LH2308A/LH2408 ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

ELECTRICAL CHARACTERISTICS (See Note 4) (LH2108/LH2308)

PARAMETER	TEST CONDITIONS	LIMITS		UNIT
		LH2108	LH2308	
Input Offset Voltage	T_A = 25°C	2.0	7.5	mV Max
Input Offset Current	T_A = 25°C	0.2	1.0	nA Max
Input Bias Current	T_A = 25°C	2.0	7.0	
Input Resistance (Note 5)	T_A = 25°C	30	10	MΩ Min
Supply Current	T_A = 25°C	0.6	0.8	mA Max
Large Signal Voltage Gain	T_A = 25°C V_S = ±15V V_{OUT} = ±10V, $R_L \geq 10k\Omega$	50	25	V/mV Min
Input Offset Voltage		3.0	10	mV Max
Average Temperature Coefficient of Input Offset Voltage (Note 6)		15	30	µV/°C Max
Input Offset Current		0.4	1.5	nA Max
Average Temperature Coefficient of Input Offset Current (Note 6)		2.5	10	pA/°C Max
Input Bias Current		3.0	10	nA Max
Supply Current	T_A = +125°C	0.4	–	mA Max
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V $R_L \geq 10k\Omega$	25	15	V/mV Min
Output Voltage Swing	V_S = ±15V, R_L = 10kΩ	±13	±13	V Min
Input Voltage Range	V_S = ±15V	±13.5	±14	
Common Mode Rejection Ratio	V_S = ±15V, V_{CM} = ±13.5V	85	80	dB Min
Supply Voltage Rejection Ratio	±5V to ±20V	80	80	
ELECTRICAL CHARACTERISTICS — LH2108/LH2308				
Input Offset Voltage	T_A = 25°C	0.5	0.5	mV Max
Input Offset Current	T_A = 25°C	0.2	1.0	nA Max
Input Bias Current	T_A = 25°C	2.0	7.0	
Input Resistance	T_A = 25°C	30	10	MΩ Min
Supply Current	T_A = 25°C	0.6	0.8	mA Max
Large Signal Voltage Gain	T_A = 25°C V_S = ±15V V_{OUT} = ±10V, $R_L \geq 10k\Omega$	80	80	V/mV Min
Input Offset Voltage		1.0	0.73	mV Max
Average Temperature Coefficient of Input Offset Voltage (Note 6)		5	5	µV/°C Max
Input Offset Current		0.4	1.5	nA Max
Average Temperature Coefficient of Input Offset Current (Note 6)		2.5	10	pA/°C Max
Input Bias Current		3.0	10	nA Max
Supply Current	T_A = +125°C	0.4	–	mA Max
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V $R_L \geq 10k\Omega$	40	60	V/mV Min
Output Voltage Swing	V_S = ±15V, R_L = 10kΩ	±13	±13	V Min
Input Voltage Range	V_S = ±15V	±13.5	±14	

Note: All typical values have been guaranteed by characterization and are not tested.

LH2108/LH2308

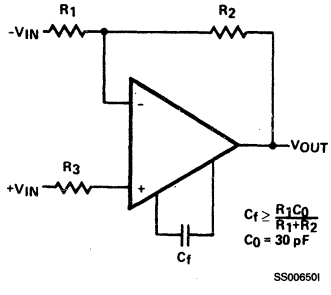
INTERSIL

ELECTRICAL CHARACTERISTICS (CONT.)

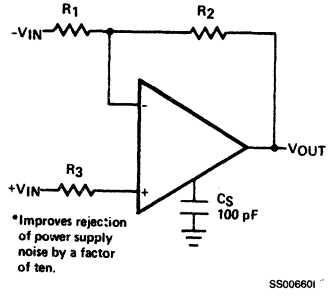
PARAMETER	TEST CONDITIONS	LIMITS		UNIT
		LH2108	LH2308	
Common Mode Rejection Ratio		96	96	dB Min
Supply Voltage Rejection Ratio		96	96	

NOTES:
1. The maximum junction temperature of the LH2108/A is 150°C, and that of the LH2308/A is 85°C. The thermal resistance of the packages is 100°C C/W, junction to ambient.
2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.
3. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
4. These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified, and the LH2308A/LH2308 for $\pm 5V \leq V_S \leq 15V$ and $0°C \leq T_A \leq 70°C$.
5. Input resistance is guaranteed by Input Bias Current test.
6. For Design only, not 100% tested.

STANDARD COMPENSATION CIRCUIT



ALTERNATE* FREQUENCY COMPENSATION



FEEDFORWARD COMPENSATION

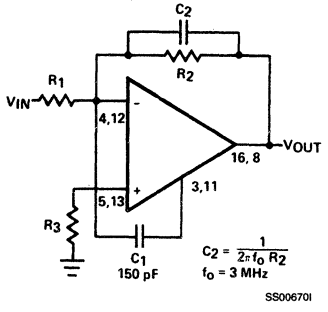


Figure 3: Auxiliary Circuit

Note: All typical values have been guaranteed by characterization and are not tested.

LM108/A, LM308/A
Super-Beta Operational Amplifier

GENERAL DESCRIPTION

These differential input, precision amplifiers provide low input currents and offset voltages comparable to FET and chopper stabilized amplifiers. They feature low power consumption over a supply voltage range of > 2V to ±20V. The amplifiers may be frequency compensated with a single external capacitor. The LM108A and LM308A are high performance selections from the 108/308 amplifier family.

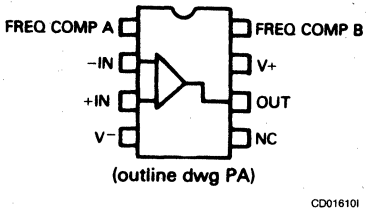
FEATURES

- **Input Bias Current — 2nA Max to 7nA Max**
- **Input Offset Current — 0.2nA Max to 1nA Max**
- **Input Offset Voltage — 0.5mV Max to 7.5mV Max**
- **ΔVos/ΔT — 5μV/°C to 30μV/°C**
- **ΔIos/ΔT — 2.5pA/°C to 10pA/°C**
- **Pin for Pin Replacement for 101A/301A**

ORDERING INFORMATION

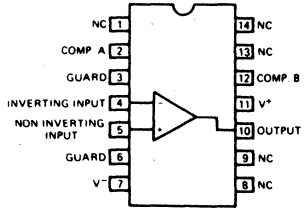
PART NUMBER	TO-99 CAN	8 PIN MINIDIP	14 PIN CERDIP	10 PIN FLATPAK	** DICE
LM108A LM308A	LM108AH* LM308AH	— LM308AN	LM108AJ LM308AJ	LM108AF LM308AF	
LM108 LM308	LM108H* LM308H	— LM308N	LM108J LM308J	LM108F LM308F	LM308/D

*If 883C processing is desired add /883C to part number.
**Parametric Min/Max Limits guaranteed at 25°C only for DICE orders.



(outline dwg PA)

CD01610I



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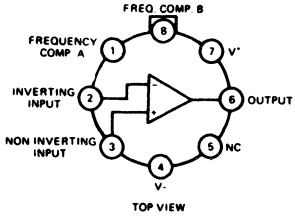
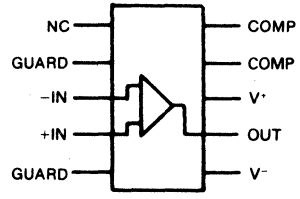


(outline dwg TY)

CD01620I



(outline dwg FB-1)

CD01640I

Figure 1: Pin Configurations

302030-002

Note: All typical values have been guaranteed by characterization and are not tested.

LM108/A, LM308/A

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- 108, 108A ..... ±20V
- 308, 308A ..... ±18V

Internal Power Dissipation (Note 1)
- Metal CAn (TO-99) 500mW
- DIP 500mW

Differential Input Current (Note 2) ..... ±10mA

Input Voltage (Note 3) ..... ±15V
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range
- 108, 108A ..... −55°C to +125°C
- 308, 308A ..... 0°C to +70°C

Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 4)

PARAMETER	TEST CONDITIONS	308			308A			108			108A			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage			2.0	7.5		0.3	0.5		0.7	2.0		0.3	0.5	mV
Input Offset Current			0.2	1.0		0.2	1.0		0.05	0.2		0.05	0.2	nA
Input Bias Current			1.5	7		1.5	7		0.8	2.0		0.8	2.0	nA
Input Resistance	Note 5	10	40		10	40		30	70		30	70		MΩ
Supply Current	V_S = ±20V V_S = ±15V		0.3	0.8		0.3	0.8		0.3	0.6		0.3	0.6	mA mA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V R_L > 10kΩ	25	300		80	300		50	300		80	300		V/mV
THE FOLLOWING SPECIFICATIONS APPLY OVER THE OPERATING TEMPERATURE RANGES														
Input Offset Voltage				10			0.73			3.0			1.0	mV
Input Offset Current				1.5			1.5			0.4			0.4	nA
Average Temperature Coefficient of Input Offset Voltage	Note 6		6.0	30		1.0	5.0		3.0	15		1.0	5.0	µV/°C
Average Temperature Coefficient of Input Offset Current	Note 6		2	10		2.0	10		0.5	2.5		0.5	2.5	pA/°C
Input Bias Current				10			10			3.0			3.0	nA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V R_L ≥ 10kΩ	15			60			25			40			V/mV
Input Voltage Range	V_S = ±15V	±13.5			±13.5			±13.5			±13.5			V
Common Mode Rejection Ratio	V_S = ±15V V_{CM} = ±13.5V	80	100		96	110		85	100		96	110		dB
Supply Voltage Rejection Ratio	±5V to ±20V	80	96		96	110		80	96		96	110		dB
Output Voltage Swing	V_S = ±15V, R_L = 10kΩ	±13	±14		±13	±14		±13	±14		±13	±14		V
Supply Current	T_A = +125°C, V_S = ±20V								0.15	0.4		0.15	0.4	mA

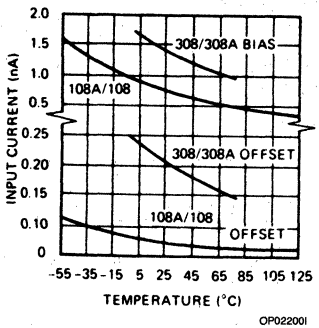
NOTES:
1. Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C and the Dual In-Line package at 9mW/°C for operation at ambient temperatures above 95°C.
2. The inputs are shunted with back-to-back diodes for over-voltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.
3. For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.
4. Unless otherwise specified, these specifications apply for supply voltages from +5V to ±20V for the 108, and 108A and +5V to ±15V for the 308 and 308A.
5. Input resistance is guaranteed by Input Bias Current test.
6. For Design only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

LM108/A, LM308/A

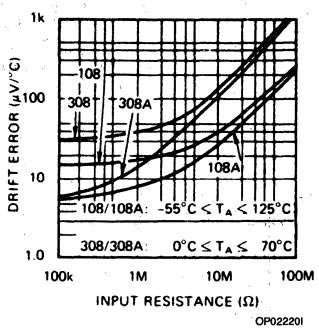
TYPICAL PERFORMANCE CHARACTERISTICS

INPUT CURRENTS



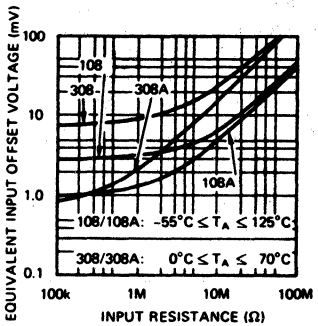
OP02200I

MAXIMUM DRIFT ERROR



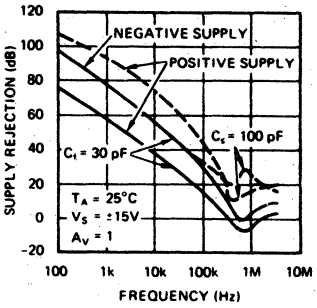
OP02220I

MAXIMUM OFFSET ERROR



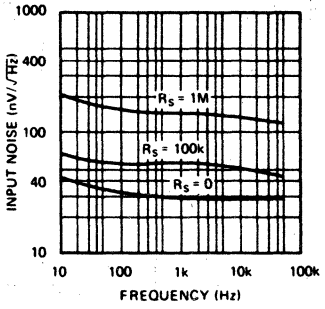
OP02210I

POWER SUPPLY REJECTION



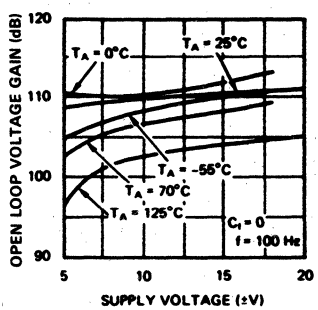
OP02230I

INPUT NOISE VOLTAGE



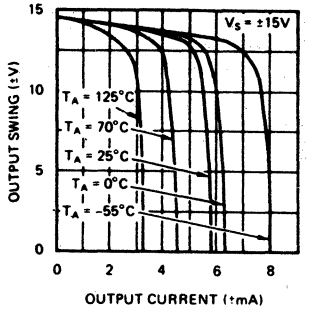
OP02241I

OPEN LOOP VOLTAGE GAIN



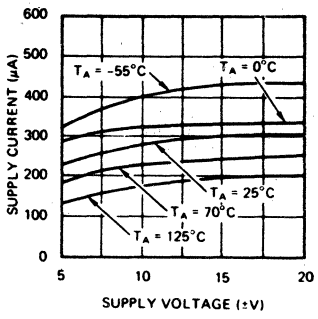
OP02251I

OUTPUT SWING



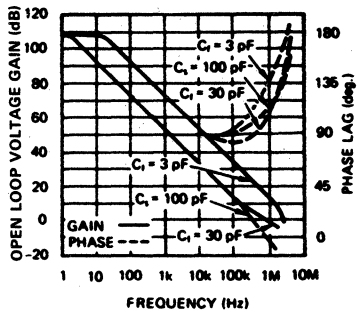
OP02260I

SUPPLY CURRENT



OP02270I

OPEN LOOP FREQUENCY RESPONSE

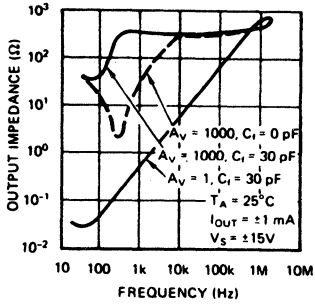


OP02281I

Note: All typical values have been guaranteed by characterization and are not tested.

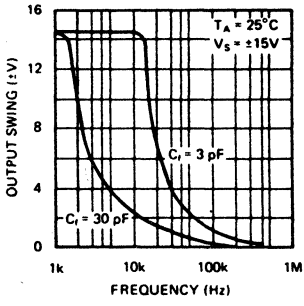
TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

CLOSED LOOP OUTPUT IMPEDANCE



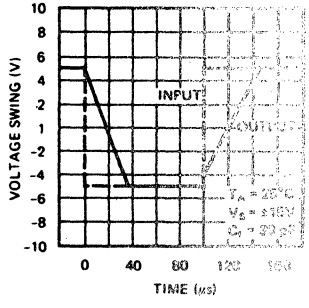
OP022901

LARGE SIGNAL FREQUENCY RESPONSE



OP023001

VOLTAGE FOLLOWER PULSE RESPONSE



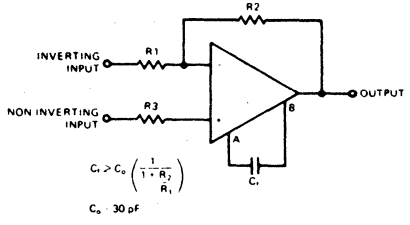
OP023101

GUARDING

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the 108 amplifier. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at 125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage at the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

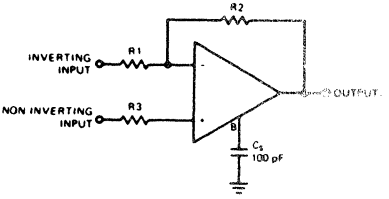
The pin configuration of the dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration).



LC021401

Figure 2: Frequency Compensation Circuit

STANDARD CIRCUIT



LC021501

Figure 3: Frequency Compensation Circuit

ALTERNATE CIRCUIT IMPROVES REJECTION OF POWER SUPPLY NOISE BY A FACTOR OF TEN

Note: All typical values have been guaranteed by characterization and are not tested.

NE/SE592
Video Amplifier

INTERSIL

GENERAL DESCRIPTION

The NE/SE592 is a monolithic, two-stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 0 to 400 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disc head amplifiers. The NE/SE592 is a pin-for-pin replacement for the μA733 in most applications.

FEATURES

- **120MHz Bandwidth**
- **Adjustable Gains From 0 to 400**
- **Adjustable Pass Band**
- **No Frequency Compensation Required**
- **Wave Shaping With Minimal External Components**

ORDERING INFORMATION

BASIC PART NUMBER	TEMP RANGE	PACKAGE			
		14-PIN PLASTIC	14-PIN CERDIP	10-PIN TO-100	8-PIN MINI DIP
SE592	−55°C to +125°C	—	SE592F	SE592H	—
NE592	0°C to +70°C	NE592N	NE592F	NE592H	NE592N-8

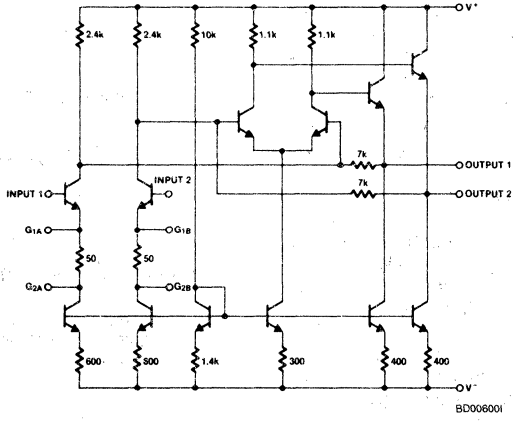
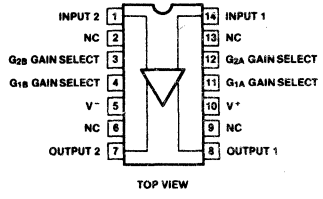
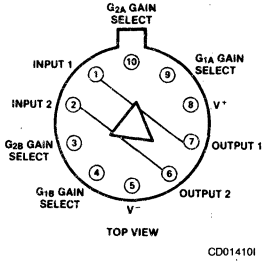


Figure 1: Functional Diagram (Resistor Values Nominal Only)

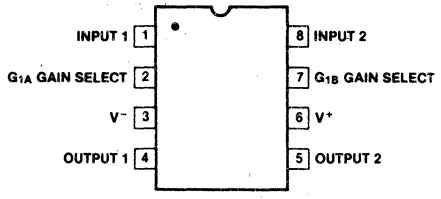
14-Pin DIP Package (JD, PD Package)



10-Pin TO-100 Package (H Package)



8-Pin DIP Package (N-8 Package)



Note: Pin 5 connected to case.

Figure 2: Pin Configurations

Note: All typical values have been guaranteed by characterization and are not tested.

NE/SE592

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±8V
Differential Input Voltage ..... ±5V
Common-Mode Input Voltage ..... ±6V
Output Current 10mA

Operating Temperature Range
SE592 ..... −55°C to +125°C
NE592 ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C
Power Dissipation 500mW
Lead Temperature (Soldering, 10sec) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A = +25°C, V_{SUPPLY} = ±6V, V_{CM} = 0 unless otherwise specified. V_S = ±6.0V

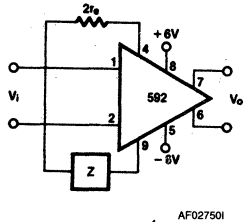
SYMBOL	PARAMETER	TEST CONDITIONS	NE592			SE592			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
A_{VOL}	Differential Voltage Gain Gain 1 (Note 1) Gain 2 (Note 2)	R_L = 2kΩ, V_{OUT} = 3Vp-p	250 80	400 100	600 120	300 90	400 100	500 110	V/V
BW	Bandwidth Gain 1 (Note 1) Gain 2 (Note 2)			40 90			40 90		MHz
t_r	Rise Time Gain 1 (Note 1) Gain 2 (Note 2) (Note 4)	V_{OUT} = 1Vp-p		10.5 4.5	12		10.5 4.5	10	ns
t_d	Propagation Delay Gain 1 (Note 1) Gain 2 (Note 2) (Note 4)	V_{OUT} = 1Vp-p		7.5 6.0	10		7.5 6.0	10	ns
R_{IN}	Input Resistance Gain 1 (Note 1) Gain 2 (Note 2)		 10	4.0 30		 20	4.0 30		kΩ
C_{IN}	Input Capacitance (Note 2) (Note 4)	Gain 2		2.0			2.0		pF
I_{OS}	Input Offset Current			0.4	5.0		0.4	3.0	μA
I_{BIAS}	Input Bias Current			9.0	30		9.0	20	μA
$\bar{e}_n$	Input Noise Voltage	BW = 1kHz to 10MHz		12			12		μV rms
ΔV_{IN}	Input Voltage Range				±1.0			±1.0	V
CMRR	Common-Mode Rejection Ratio Gain 2 (Note 2) Gain 2 (Note 2)	 V_{CM} ±1V, f < 100kHz V_{CM} ±1V, f = 5MHz	 60	 86 60		 60	 86 60		dB
PSRR	Supply Voltage Rejection Ratio Gain 2 (Note 2)	ΔV_S = ±0.5V	50	70		50	70		dB
V_{OO}	Output Offset Voltage Gain 2 (Note 2)	R_L = ∞		0.35	0.75		0.35	0.75	V
V_{OCM}	Output Common-Mode Voltage	R_L = ∞	2.4	2.9	3.4	2.4	2.9	3.4	V
$V_{O(DIFF)}$	Differential Output Voltage Swing	R_L = 2kΩ	3.0	4.0		3.0	4.0		V
R_O	Output Resistance			20			20		Ω
I^+	Power Supply Current (Note 3)	R_L = ∞		18	24		18	24	mA

NOTES: 1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. Recommended supply voltage = ±6V
4. For design reference only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

NE/SE592

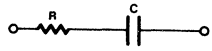
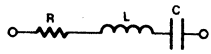
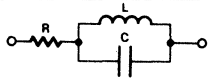
TYPICAL APPLICATIONS



AF02750I

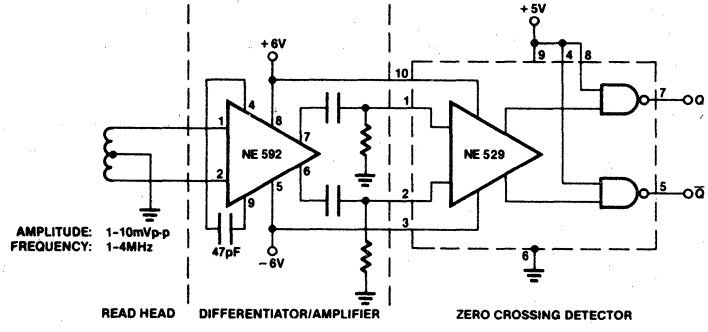
$$\frac{V_o}{V_i}(S) \cong \frac{1.4 \times 10^4}{Z(s) + 2r_e} \cong \frac{1.4 \times 10^4}{Z(s) + 32}$$

Filter Networks

SCHEMATIC	FILTER TYPE	$\frac{V_o}{V_i}(S)$ TRANSFER FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/L\ s + 1/LC}\right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

NOTE: In the networks above, the R value used is assumed to include the internal $2r_e$ of approximately 32Ω.

Figure 3: Basic Configuration



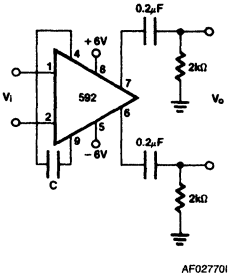
AF02761I

Figure 4: Disc/Tape Modulated Readback Systems

Note: All typical values have been guaranteed by characterization and are not tested.

For frequency $f_1 << 1/2\pi(32)C$

$$V_o \cong 1.4 \times 10^4 C \frac{dV_i}{dt}$$



AF027701

Figure 5: Differentiation with High Common Noise Rejection

Note: All typical values have been guaranteed by characterization and are not tested.

Section 5 — Special Analog Functions

AD590
2-Wire Current Output Temperature Transducer

INTERSIL

GENERAL DESCRIPTION

The AD590 is an integrated-circuit temperature transducer which produces an output current proportional to absolute temperature. The device acts as a high impedance constant current regulator, passing 1μA/°K for supply voltages between +4V and +30V. Laser trimming of the chip's thin film resistors is used to calibrate the device to 298.2μA output at 298.2°K (+25°C).

The AD590 should be used in any temperature-sensing application between −55°C and +150°C (0°C and 70°C for TO-92) in which conventional electrical temperature sensors are currently employed. The inherent low cost of a monolithic integrated circuit combined with the elimination of support circuitry makes the AD590 an attractive alternative for many temperature measurement situations. Linearization circuitry, precision voltage amplifiers, resistance-measuring circuitry and cold-junction compensation are not needed in applying the AD590. In the simplest application, a resistor, a power source and any voltmeter can be used to measure temperature.

In addition to temperature measurement, applications include temperature compensation or correction of discrete components, and biasing proportional to absolute temperature. The AD590 is available in chip form making it suitable for hybrid circuits and fast temperature measurements in protected environments.

The AD590 is particularly useful in remote sensing applications. The device is insensitive to voltage drops over long lines due to its high-impedance current output. Any well-insulated twisted pair is sufficient for operation hundreds of feet from the receiving circuitry. The output characteristics also make the AD590 easy to multiplex: the current can be switched by a CMOS multiplexer or the supply voltage can be switched by a logic gate output.

FEATURES

- **Linear Current Output: 1μA/°K**
- **Wide Range: −55°C to +150°C**
- **Two-Terminal Device: Voltage In/Current Out**
- **Laser Trimmed to ±0.5°C Calibration Accuracy (AD590M)**
- **Excellent Linearity: ±0.5°C Over Full Range (AD590M)**
- **Wide Power Supply Range: +4V to +30V**
- **Sensor Isolation From Case**
- **Low Cost**

ORDERING INFORMATION

NON-LINEARITY (°C)	PART NUMBER/PACKAGE		
	TO-52 PACKAGE	TO-92 PACKAGE	DICE**
±3.0	AD590IH	AD590IZR	AD590/D
±1.5	AD590JH	AD590JZR	
±0.8	AD590KH	—	
±0.4	AD590LH	—	
±0.3	AD590MH	—	
TEMPERATURE RANGE	−55°C to +150°C	0°C to +70°C	DICE

**Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.

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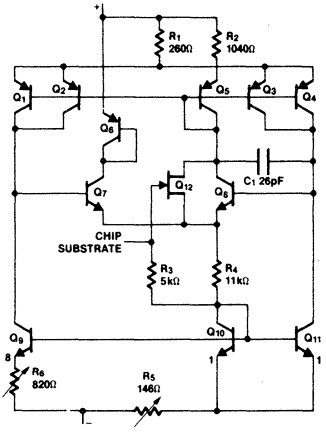


Figure 1: Functional Diagram

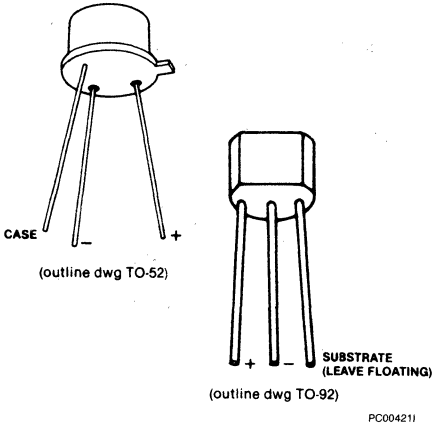


Figure 2: Pin Configurations

300106-002

Note: All typical values have been guaranteed by characterization and are not tested.

AD590

INTERSIL

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Forward Voltage (V^+ to V^-) ..... +44V
Reverse Voltage (V^+ to V^-) ..... -20V
Breakdown Voltage (Case to V^+ or V^-) ..... ±200V
Storage Temperature Range ..... -65°C to +150°C

Rated Performance Temperature Range
TO-92 ..... 0°C to +70°C
TO-52 ..... -55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (Typical values at T_A = +25°C, V^+ = 5V unless otherwise noted)

CHARACTERISTICS	AD590I	AD590J	AD590K	AD590L	AD590M	UNIT
Output Nominal Output Current @ + 125°C(298.2°K)	298.2	298.2	298.2	298.2	298.2	μA
Nominal Temperature Coefficient	1.0	1.0	1.0	1.0	1.0	μA/° K
Calibration Error @ + 25°C (Notes 1, 5)	±10.0 max	±5.0 max	±2.5 max	±1.0 max	±0.5 max	°C
Absolute Error (-55°C to +150°C) (Note 7) Without External Calibration Adjustment With External Calibration Adjustment	 ±20.0 max ±5.8 max	 ±10.0 max ±3.0 max	 ±5.5 max ±2.0 max	 ±3.0 max ±1.6 max	 ±1.7 max ±1.0 max	 °C °C
Non-Linearity (Note 6)	±3.0 max	±1.5 max	±0.8 max	±0.4 max	±0.3 max	°C
Repeatability (Notes 2, 6)	±0.1 max	±0.1 max	±0.1 max	±0.1 max	±0.1 max	°C
Long Term Drift (Notes 3, 6)	±0.1 max	±0.1 max	±0.1 max	±0.1 max	±0.1 max	°C/month
Current Noise	40	40	40	40	40	$pA/\sqrt{Hz}$
Power Supply Rejection: +4V < V^+ < +5V +5V < V^+ < +15V +15V < V^+ < +30V	 0.5 0.2 0.1	 0.5 0.2 0.1	 0.5 0.2 0.1	 0.5 0.2 0.1	 0.5 0.2 0.1	 μA/V μA/V μA/V
Case Isolation to Either Lead	10^{10}	10^{10}	10^{10}	10^{10}	10^{10}	Ω
Effective Shunt Capacitance	100	100	100	100	100	pF
Electrical Turn-On Time (Note 1)	20	20	20	20	20	μs
Reverse Bias Leakage Current (Note 4)	10	10	10	10	10	pA
Power Supply Range	+4 to +30	+4 to +30	+4 to +30	+4 to +30	+4 to +30	V

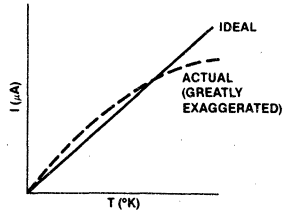
NOTES:
1. Does not include self heating effects.
2. Maximum deviation between +25°C reading after temperature cycling between -55°C and +150°C (0°C and 70°C for TO-92).
3. Conditions: Constant +5V, constant +125°C.
4. Leakage current doubles every +10°C.
5. Mechanical strain on package (especially TO-92) may disturb calibration of device.
6. Guaranteed. But not tested.
7. -55°C Guaranteed by testing @ +25°C and @ +150°C.

TRIMMING OUT ERRORS

The ideal graph of current versus temperature for the AD590 is a straight line, but as Figure 3 shows, the actual shape is slightly different. Since the sensor is limited to the range of -55°C to +150°C (0°C to 70°C for TO-92), it is possible to optimize the accuracy by trimming. Trimming also permits extracting maximum performance from the lower-cost sensors.

The circuit of Figure 4 trims the slope of the AD590 output. The effect of this is shown in Figure 5.

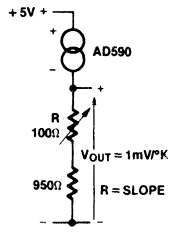
The circuit of Figure 6 trims both the slope and the offset. This is shown in Figure 7. The diagrams are exaggerated to show effects, but it should be clear that these trims can be used to minimize errors over the whole range, or over any selected part of the range. In fact, it is possible to adjust the I-grade device to give less than 0.1°C error over the range 0°C to 90°C and less than 0.05°C error from 25°C to 60°C.



SC005001

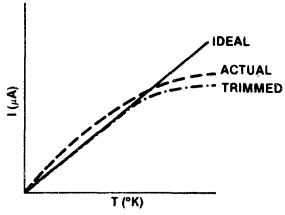
Figure 3: Trimming Out Errors

Note: All typical values have been guaranteed by characterization and are not tested.



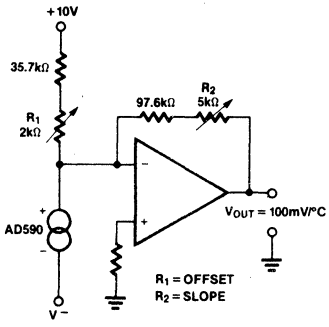
TC02471I

Figure 4: Slope Trimming



SC00510I

Figure 5: Effect of Slope Trim



TC02480I

Figure 6: Slope and Offset Trimming

ACCURACY

Maximum errors over limited temperature spans, with V_S = +5V, are listed by device grade in the following tables. The tables reflect the worst-case linearities, which invariably occur at the extremities of the specified temperature range. The trimming conditions for the data in the tables are shown in Figures 4 and 5.

All errors listed in the tables are ±°C. For example, if ±1°C maximum error is required over the +25°C to +75°C range (i.e., lowest temperature of +25°C and span of 50°C), then the trimming of a J-grade device, using the single-trim circuit (Figure 4), will result in output having the required accuracy over the stated range. An M-grade device with no trims will have less than ±0.9°C error, and an I-grade device with two trims (Figure 5) will have less than ±0.2°C error. If the requirement is for less than ±1.4°C maximum error, from −25°C to +75°C (100° span from −25°C), it can be satisfied by an M-grade device with no trims, a K-grade device with one trim, or an I-grade device with two trims.

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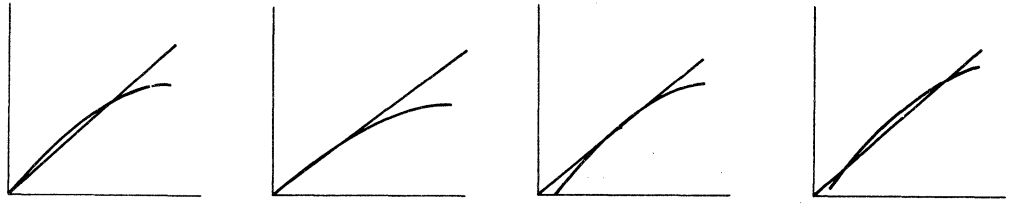


a) Untrimmed — SC00520I

b) Trim One: Offset — SC00530I

c) Trim Two: Slope — SC00540I

d) Trim Three: Offset Again — SC00550I

Figure 7: Effect of Slope and Offset Trimming

Note: All typical values have been guaranteed by characterization and are not tested.

AD590

I GRADE — MAXIMUM ERRORS, °C

NUMBER OF TRIMS	TEMPERATURE SPAN—°C	LOWEST TEMPERATURE IN SPAN—°C							
		−55	−25	0	+25	+50	+75	+100	+125
None	10	8.4	9.2	10.0	10.8	11.6	12.4	13.2	14.4
None	25	10.0	10.4	11.0	11.8	12.0	13.8	15.0	16.0
None	50	13.0	13.0	12.8	13.8	14.6	16.4	18.0	
None	100	15.2	16.0	16.6	17.4	18.8			
None	150	18.4	19.0	19.2					
None	205	20.0							
One	10	0.6	0.4	0.4	0.4	0.4	0.4	0.4	0.6
One	25	1.8	1.2	1.0	1.0	1.0	1.2	1.6	1.8
One	50	3.8	3.0	2.0	2.0	2.0	3.0	3.8	
One	100	4.8	4.5	4.2	4.2	5.0			
One	150	5.5	4.8	5.5					
One	205	5.8							
Two	10	0.3	0.2	0.1	*	*	0.1	0.2	0.3
Two	25	0.5	0.3	0.2	*	0.1	0.2	0.3	0.5
Two	50	1.2	0.6	0.4	0.2	0.2	0.3	0.7	
Two	100	1.8	1.4	1.0	2.0	2.5			
Two	150	2.6	2.0	2.8					
Two	205	3.0							

* Less than 0.05°C.

J GRADE — MAXIMUM ERRORS, °C

NUMBER OF TRIMS	TEMPERATURE SPAN—°C	LOWEST TEMPERATURE IN SPAN—°C							
		−55	−25	0	+25	+50	+75	+100	+125
None	10	4.2	4.6	5.0	5.4	5.8	6.2	6.6	7.2
None	25	5.0	5.2	5.5	5.9	6.0	6.9	7.5	8.0
None	50	6.5	6.5	6.4	6.9	7.3	8.2	9.0	
None	100	7.7	8.0	8.3	8.7	9.4			
None	150	9.2	9.5	9.6					
None	205	10.0							
One	10	0.3	0.2	0.2	0.2	0.2	0.2	0.2	0.3
One	25	0.9	0.6	0.5	0.5	0.5	0.6	0.8	0.9
One	50	1.9	1.5	1.0	1.0	1.0	1.5	1.9	
One	100	2.3	2.2	2.0	2.0	2.3			
One	150	2.5	2.4	2.5					
One	205	3.0							
Two	10	0.1	*	*	*	*	*	*	0.1
Two	25	0.2	0.1	*	*	*	*	0.1	0.2
Two	50	0.4	0.2	0.1	*	*	0.1	0.2	*
Two	100	0.7	0.5	0.3	0.7	1.0			
Two	150	1.0	0.7	1.2					
Two	205	1.6							

* Less than ±0.05°C.

Note: All typical values have been guaranteed by characterization and are not tested.

AD590

K GRADE — MAXIMUM ERRORS, °C

NUMBER OF TRIMS	TEMPERATURE SPAN—°C	LOWEST TEMPERATURE IN SPAN—°C							
		−55	−25	0	+25	+50	+75	+100	+125
None	10	2.1	2.3	2.5	2.7	2.9	3.1	3.3	3.6
None	25	2.6	2.7	2.8	3.0	3.2	3.5	3.8	4.2
None	50	3.8	3.5	3.4	3.6	3.8	4.3	5.1	
None	100	4.2	4.3	4.4	4.6	5.1			
None	150	4.8	4.8	5.3					
None	205	5.5							
One	10	0.2	0.1	0.1	0.1	0.1	0.1	0.1	0.2
One	25	0.6	0.4	0.3	0.3	0.3	0.4	0.5	0.6
One	50	1.2	1.0	0.7	0.7	0.7	1.0	1.2	
One	100	1.5	1.4	1.3	1.3	1.5			
One	150	1.7	1.5	1.7					
One	205	2.0							
Two	10	0.1	*	*	*	*	*	*	0.1
Two	25	0.2	0.1	*	*	*	*	0.1	0.2
Two	50	0.3	0.1	*	*	*	0.1	0.2	
Two	100	0.5	0.3	0.2	0.3	0.7			
Two	150	0.6	0.5	0.7					
Two	205	0.8							

* Less than ±0.05°C.

L GRADE — MAXIMUM ERRORS, °C

NUMBER OF TRIMS	TEMPERATURE SPAN—°C	LOWEST TEMPERATURE IN SPAN—°C							
		−55	−25	0	+25	+50	+75	+100	+125
None	10	1.0	1.0	1.1	1.1	1.2	1.3	1.4	1.6
None	25	1.3	1.3	1.3	1.4	1.5	1.6	1.7	1.9
None	50	1.9	1.8	1.7	1.8	1.9	2.1	2.4	
None	100	2.4	2.4	2.4	2.4	2.7			
None	150	2.7	2.6	2.8					
None	205	3.0							
One	10	0.2	0.1	0.1	0.1	0.1	0.1	0.1	0.2
One	25	0.5	0.4	0.3	0.3	0.3	0.3	0.4	0.5
One	50	1.0	0.8	0.6	0.6	0.6	0.8	1.0	
One	100	1.3	1.2	1.1	1.1	1.3			
One	150	1.4	1.3	1.4					
One	205	1.6							
Two	10	0.1	*	*	*	*	*	*	0.1
Two	25	0.1	*	*	*	*	*	*	0.1
Two	50	0.2	*	*	*	*	*	0.2	
Two	100	0.3	0.2	0.1	0.2	0.3			
Two	150	0.3	0.2	0.3					
Two	205	0.4							

* Less than ±0.05°C.

M GRADE — MAXIMUM ERRORS, °C

NUMBER OF TRIMS	TEMPERATURE SPAN—°C	LOWEST TEMPERATURE IN SPAN—°C							
		−55	−25	0	+25	+50	+75	+100	+125
None	10	0.6	0.5	0.6	0.6	0.7	0.7	0.7	0.9
None	25	0.8	0.8	0.7	0.7	0.8	0.8	1.0	1.1
None	50	1.0	0.9	0.8	0.9	0.9	1.1	1.2	
None	100	1.3	1.4	1.3	1.4	1.5			
None	150	1.5	1.6	1.6					
None	205	1.7							

Note: All typical values have been guaranteed by characterization and are not tested.

AD590

M GRADE — MAXIMUM ERRORS, °C (CONT.)

NUMBER OF TRIMS	TEMPERATURE SPAN—°C	LOWEST TEMPERATURE IN SPAN—°C							
		−55	−25	0	+25	+50	+75	+100	+125
One	10	0.2	0.1	0.1	0.1	0.1	0.1	0.1	0.2
One	25	0.4	0.3	0.2	0.2	0.2	0.2	0.3	0.4
One	50	0.5	0.4	0.3	0.3	0.3	0.4	0.5	
One	100	0.8	0.8	0.7	0.7	0.8			
One	150	0.9	0.9	0.9					
One	205	1.0							
Two	10	0.1	*	*	*	*	*	*	0.1
Two	25	0.1	*	*	*	*	*	*	0.1
Two	50	0.2	*	*	*	*	*	0.2	
Two	100	0.2	0.1	*	0.1	0.2			
Two	150	0.3	0.2	0.3					
Two	205	0.3							

* Less than ±0.05°C.

NOTES

1. Maximum errors over all ranges are guaranteed based on the known behavior characteristic of the AD590.
2. For one-trim accuracy specifications, the 205°C span is assumed to be trimmed at +25°C; for all other spans, it is assumed that the device is trimmed at the midpoint.
3. For the 205°C span, it is assumed that the two-trim temperatures are in the vicinity of 0°C and +140°C; for all other spans, the specified trims are at the endpoints.
4. In precision applications, the actual errors encountered are usually dependent upon sources of error which are often overlooked in error budgets. These typically include:
   a. Trim error in the calibration technique used
   b. Repeatability error
   c. Long-term drift errors

Trim error is usually the largest error source. This error arises from such causes as poor thermal coupling between the device to be calibrated and the reference sensor; reference sensor errors; lack of adequate time for the device being calibrated to settle to the final temperature; radically different thermal resistances between the case and the surroundings ($R_{\theta CA}$) when trimming and when applying the device.

Repeatability errors arise from a strain hysteresis of the package. The magnitude of this error is solely a function of the magnitude of the temperature span over which the device is used. For example, thermal shocks between 0°C and 100°C involve extremely low hysteresis and result in repeatability errors of less than ±0.05°C. When the thermal-shock excursion is widened to −55°C to +150°C, the device will typically exhibit a repeatability error of ±0.05°C (±0.10 guaranteed maximum).

Long-term drift errors are related to the average operating temperature and the magnitude of the thermal shocks experienced by the device. Extended use of the AD590 at temperatures above 100°C typically results in long-term drift of ±0.03°C per month; the guaranteed maximum is ±0.10°C per month. Continuous operation at temperatures below 100°C induces no measurable drifts in the device. Besides the effects of operating temperature, the severity of thermal shocks incurred will also affect absolute stability. For thermal-shock excursions less than 100°C, the drift is difficult to measure (< 0.03°C). However, for 200°C excursions, the device may drift by as much as ±0.10°C after twenty such shocks. If severe, quick shocks are necessary in the application of the device, realistic simulated life tests are recommended for a thorough evaluation of the error introduced by such shocks.

TYPICAL APPLICATIONS

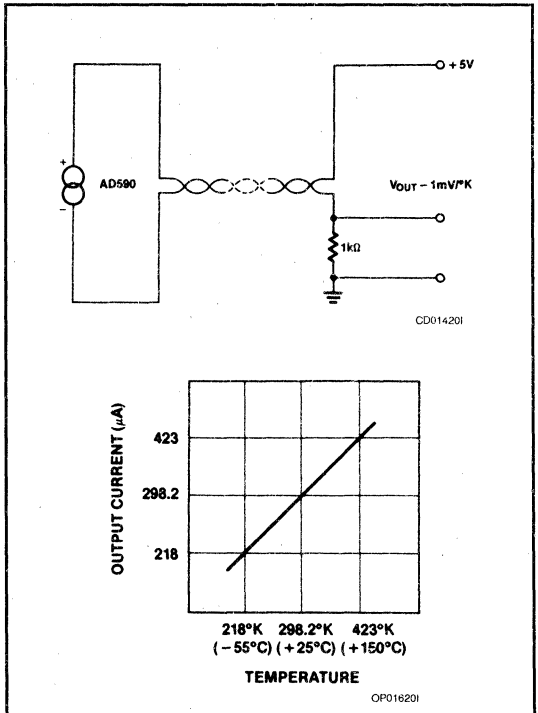
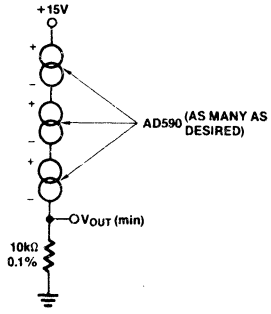


Figure 8: Simple connection. Output is proportional to absolute temperature.

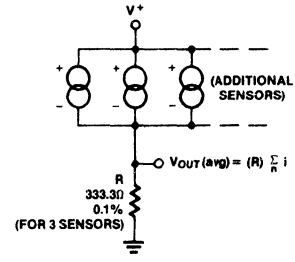
Note: All typical values have been guaranteed by characterization and are not tested.

TYPICAL APPLICATIONS (CONT.)



DS01700I

Figure 9: Lowest-temperature sensing scheme. Available current is that of the "coldest" sensor.

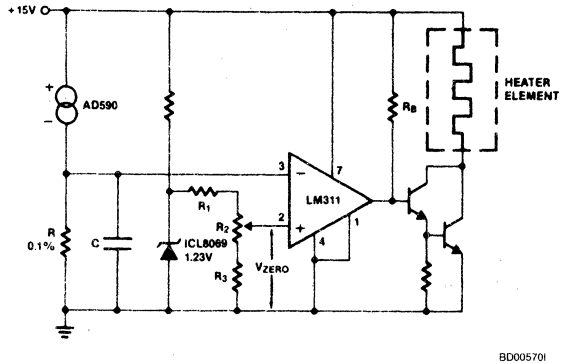


DS01710I

Figure 10: Average-temperature sensing scheme. The sum of the AD590 currents appears across R, which is chosen by the formula:

$$R = \frac{10k\Omega}{n}$$

n being the number of sensors.



BD00570I

Figure 11: Single-setpoint temperature controller. The AD590 produces a temperature-dependent voltage across R (C is for filtering noise). Setting R_2 produces a scale-zero voltage. For the Celsius scale, make R = 1kΩ and V_{ZERO} = 0.273 volts. For Fahrenheit, R = 1.8kΩ and V_{ZERO} = 0.460 volts.

Note: All typical values have been guaranteed by characterization and are not tested.

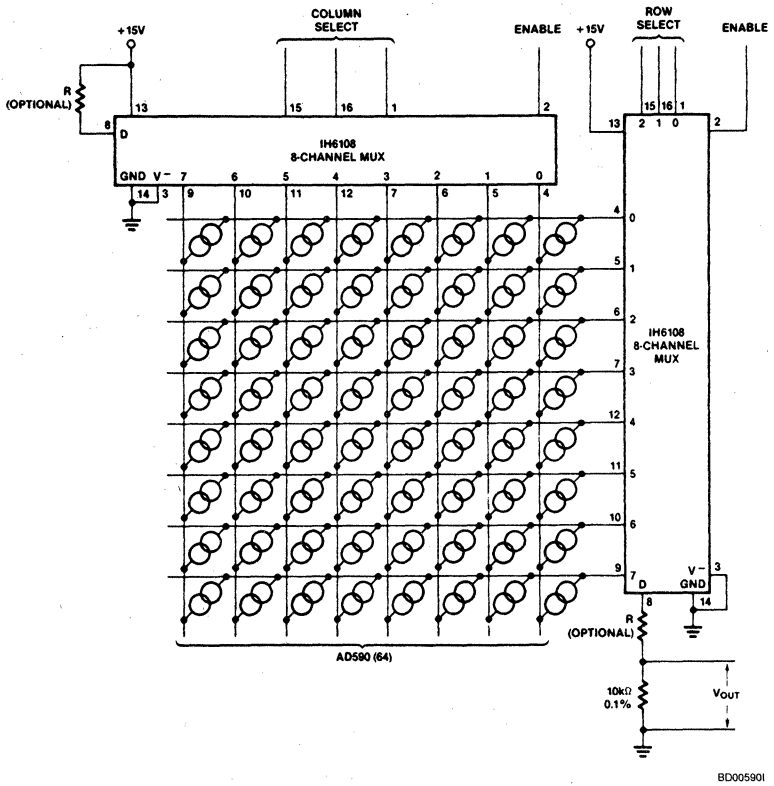


Figure 12: Multiplexing sensors. If shorted sensors are possible, a series resistor in series with the D line will limit the current (shown as R, above: only one is needed). A six-bit digital word will select one of 64 sensors.

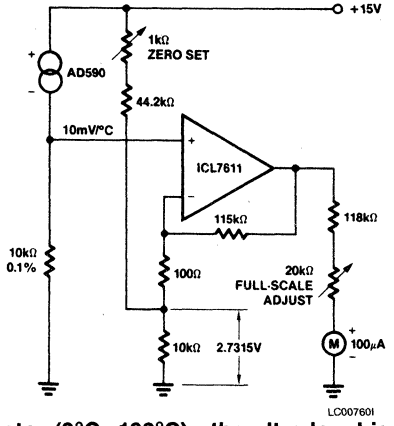


Figure 13: Centigrade thermometer (0°C–100°C) . the ultra-low bias current of the ICL7611 allows the use of large-value gain-resistors, keeping meter-current error under 1/2%, and therefore saving the expense of an extra meter-driving amplifier.

Note: All typical values have been guaranteed by characterization and are not tested.

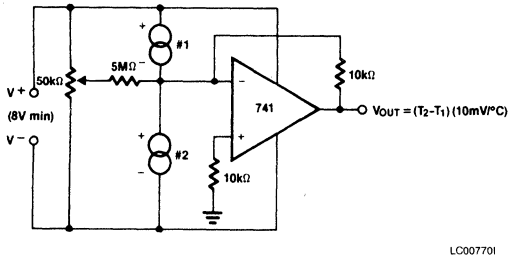


Figure 14: Differential thermometer. The 50kΩ pot trims offsets in the devices whether internal or external, so it can be used to set the size of the difference interval. This also makes it useful for liquid-level detection (where there will be a measurable temperature difference).

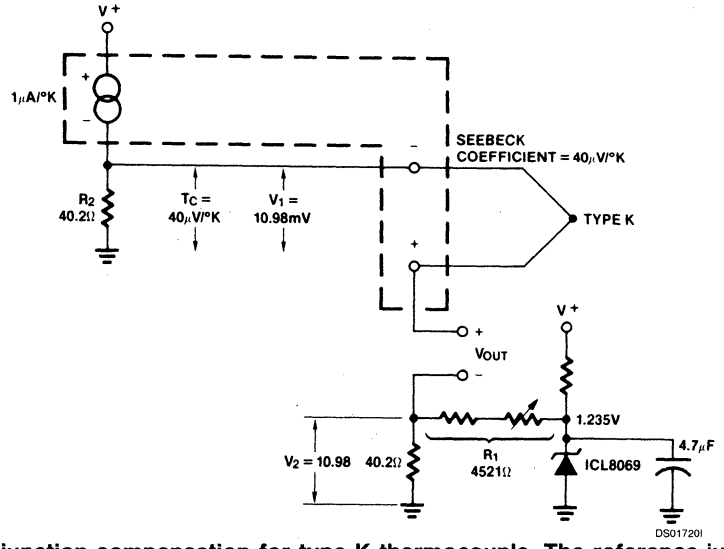


Figure 15: Cold-junction compensation for type K thermocouple. The reference junction(s) should be in close thermal contact with the AD590 case. V^+ must be at least 4V, while ICL8069 current should be set at 1mA – 2mA. Calibration does not require shorting or removal of the thermocouple: set R_1 for V_2 = 10.98mV. If very precise measurements are needed, adjust R_2 to the exact Seebeck coefficient for the thermocouple used (measured or from table) note V_1, and set R_1 to buck out this voltage (i.e., set $V_2 = V_1$). For other thermocouple types, adjust values to the appropriate Seebeck coefficient.

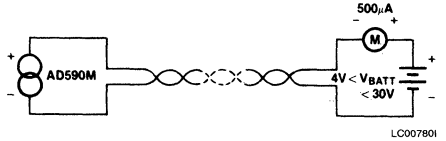
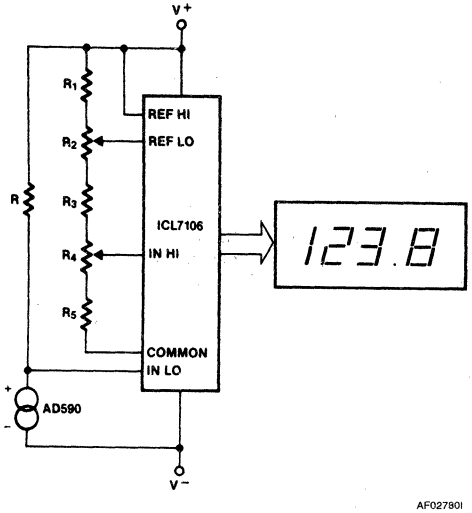


Figure 16: Simplest thermometer. Meter displays current output directly in degrees Kelvin. Using the AD590M, sensor output is within ±1.7 degrees over the entire range, and less than ±1 degree over the greater part of it.

Note: All typical values have been guaranteed by characterization and are not tested.



AF02780I

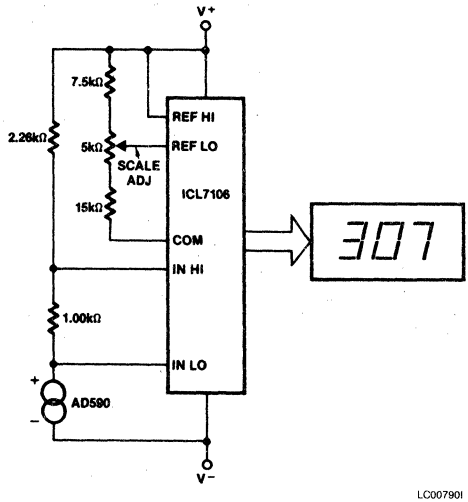
	R	R_1	R_2	R_3	R_4	R_5
°F	9.00	4.02	2.0	12.4	10.0	0
°C	5.00	4.02	2.0	5.11	5.0	11.8

$$\sum_{n=1}^{5} R_n = 28k\Omega \text{ nominal}$$

All values in kΩ

The ICL7106 has a V_{IN} span of ±2.0V, and a V_{CM} range of (V^+ −0.5) Volts to (V^- +1) Volts; R is scaled to bring each range within V_{CM} while not exceeding V_{IN}. V_{REF} for both scales is 500mV. Maximum reading on the Celsius range is 199.9°C, limited by the (short-term) maximum allowable sensor temperature. Maximum reading on the Fahrenheit range is 199.9°F (93.3°C), limited by the number of display digits. See note next page.

Figure 17: Basic digital thermometer, Celsius and Fahrenheit scales



LC00790I

Figure 18: Basic digital thermometer, Kelvin scale. The Kelvin scale version reads from 0 to 1999°K theoretically, and from 223°K to 473°K actually. The 2.26kΩ resistor brings the input within the ICL7106 V_{CM} range: 2 general-purpose silicon diodes or an LED may be substituted.

Note: All typical values have been guaranteed by characterization and are not tested.

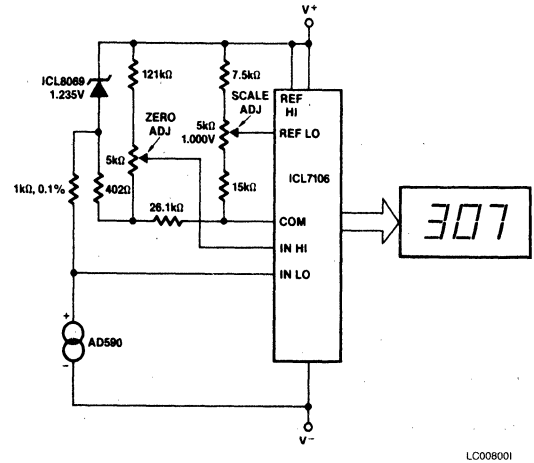


Figure 19: Basic digital thermometer, Kelvin scale with zero adjust. This circuit allows "zero adjustment" as well as slope adjustment. The ICL8069 brings the input within the common-mode range, while the 5kΩ pots trim any offset at 218°K (−55°C), and set the scale factor.

Note on Figure 17, Figure 18 and Figure 19: Since all 3 scales have narrow V_{IN} spans, some optimization of ICL7106 components can be made to lower noise and preserve CMR. The table below shows the suggested values. Similar scaling can be used with the ICL7126/36.

SCALE	V_{IN} RANGE (V)	R_{INT}(kΩ)	C_{AZ}(μF)
K	0.223 to 0.473	220	0.47
C	−0.25 to +1.0	220	0.1
F	−0.29 to +0.996	220	0.1

For all:

$C_{REF} = 0.1\mu F$
$C_{INT} = 0.22\mu F$

$C_{OSC} = 100pF$
$R_{OSC} = 100k\Omega$

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7660
CMOS Voltage Converter

GENERAL DESCRIPTION

The Intersil ICL7660 is a monolithic CMOS power supply circuit which offers unique performance advantages over previously available devices. The ICL7660 performs supply voltage conversion from positive to negative for an input range of +1.5V to +10.0V, resulting in complementary output voltages of −1.5V to −10.0V. Only 2 non-critical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7660 can also be connected to function as a voltage doubler and will generate output voltages up to +18.6V with a +10V input. Note that an additional diode is required for V_{SUPPLY} > 6.5V.

Contained on chip are a series DC power supply regulator, RC oscillator, voltage level translator, and four output power MOS switches. A unique logic element senses the most negative voltage in the device and ensures that the output N-channel switch source-substrate junctions are not forward biased. This assures latchup free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 5.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be overdriven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+3.5 to +10.0 volts), the LV pin is left floating to prevent device latchup.

FEATURES

- **Simple Conversion of +5V Logic Supply to ±5V Supplies**
- **Simple Voltage Multiplication ($V_{OUT} = (-) nV_{IN}$)**
- **99.9% Typical Open Circuit Voltage Conversion Efficiency**
- **98% Typical Power Efficiency**
- **Wide Operating Voltage Range 1.5V to 10.0V**
- **Easy to Use — Requires Only 2 External Non-Critical Passive Components**

APPLICATIONS

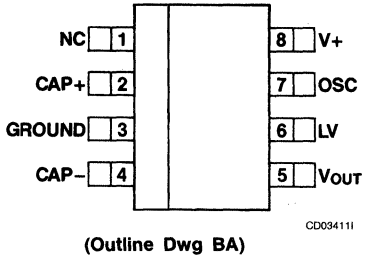
- **On Board Negative Supply for Dynamic RAMs**
- **Localized μ-Processor (8080 Type) Negative Supplies**
- **Inexpensive Negative Supplies**
- **Data Acquisition Systems**

ORDERING INFORMATION

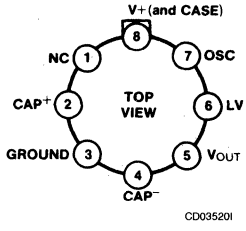
PART NUMBER	TEMP. RANGE	PACKAGE
ICL7660CTV	0° to +70°C	TO-99
ICL7660CBA	0°C to +70°C	8 PIN SOIC
ICL7660CPA	0° to +70°C	8 PIN MINI DIP
ICL7660MTV*	−55° to +125°C	TO-99
ICL7660/D	–	DICE**

*Add /883B to part number if 883B processing is required.

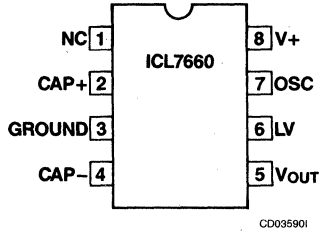
**Parameter min/max limits guaranteed at 25°C only for DICE orders.



(Outline Dwg BA)
8 LEAD MiniDIP



(Outline Dwg TV)
8 LEAD TO-99



(Outline Dwg PA)

Figure 1: Pin Configurations

302063-003

Note: All typical values have been guaranteed by characterization and are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 10.5V
LV and OSC Input Voltage
(Note 1) ..... −0.3V to (V^+ ± +0.3V) for $V^+ < 5.5V$
(V^+ −5.5V) to (V^+ +0.3V) for $V^+ > 5.5V$
Current into LV (Note 1) ..... 20μA for V+ > 3.5V
Output Short Duration ($V_{SUPPLY} \leq 5.5V$) ..... Continuous
Power Dissipation (Note 2)
ICL7660CTV 500mW
ICL7660CPA 300mW
ICL7660MTV 500mW

Operating Temperature Range
ICL7660M ..... −55°C to +125°C
ICL7660C ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature
(Soldering, 10sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

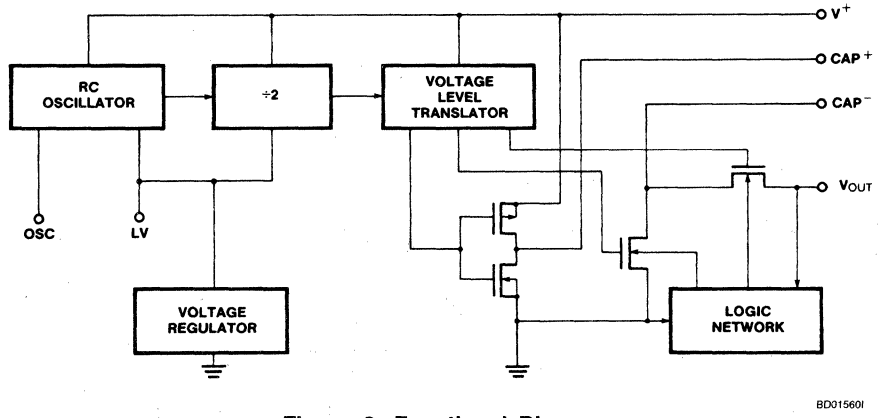


Figure 2: Functional Diagram

OPERATING CHARACTERISTICS

$V^+ = 5V$, $T_A = 25°C$, $C_{OSC} = 0$, Test Circuit Figure 3 (unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I^+	Supply Current	$R_L = \infty$		170	500	μA
V_{H1}^+	Supply Voltage Range – Hi	0°C ≤ T_A ≤ 70°C, R_L = 10kΩ, LV Open	3.0		6.5	V
	(D_X out of circuit) (Note 3)	−55°C ≤ T_A ≤ 125°C, R_L = 10kΩ, LV Open	3.0		5.0	V
V_{L1}^+	Supply Voltage Range – Lo (D_X out of circuit)	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV to GROUND	1.5		3.5	V
V_{H2}^+	Supply Voltage Range – Hi (D_X in circuit)	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV Open	3.0		10.0	V
V_{L2}^+	Supply Voltage Range – Lo (D_X in circuit)	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV to GROUND	1.5		3.5	V

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7660

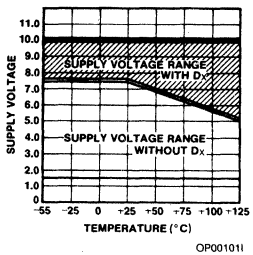
OPERATING CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
R_{OUT}	Output Source Resistance	I_{OUT} = 20mA, T_A = 25°C		55	100	Ω
		I_{OUT} = 20mA, 0°C ≤ T_A ≤ +70°C			120	Ω
		I_{OUT} = 20mA, −55°C ≤ T_A ≤ +125°C (Note 3)			150	Ω
		V^+ = 2V, I_{OUT} = 3mA, LV to GROUND 0°C ≤ T_A ≤ +70°C			300	Ω
		V^+ = 2V, I_{OUT} = 3mA, LV to GROUND, −55°C ≤ T_A ≤ +125°C, D_X in circuit (Note 3)			400	Ω
f_{OSC}	Oscillator Frequency			10		kHz
P_{Ef}	Power Efficiency	R_L = 5kΩ	95	98		%
$V_{OUT\ Ef}$	Voltage Conversion Efficiency	R_L = ∞	97	99.9		%
Z_{OSC}	Oscillator Impedance	V^+ = 2 Volts		1.0		MΩ
		V = 5 Volts		100		kΩ

Notes: 1. Connecting any input terminal to voltages greater than V+ or less than GROUND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the ICL7660.
2. Derate linearly above 50°C by 5.5mW/°C.
3. ICL7660M only.

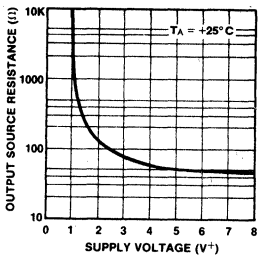
TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 3)

OPERATING VOLTAGE AS A FUNCTION OF TEMPERATURE



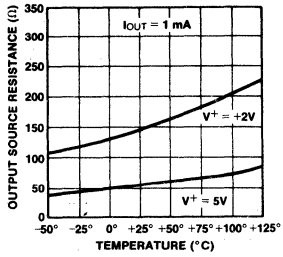
OP00101I

OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE



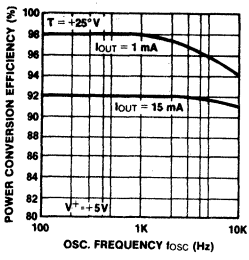
OP00070I

OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE



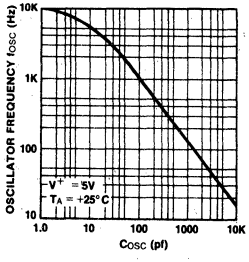
OP00040I

POWER CONVERSION EFFICIENCY AS A FUNCTION OF OSC. FREQUENCY



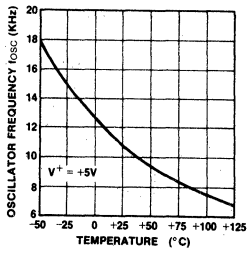
OP00030I

FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSC. CAPACITANCE



OP00080I

UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE

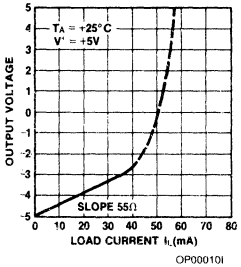


OP00051I

Note: All typical values have been guaranteed by characterization and are not tested.

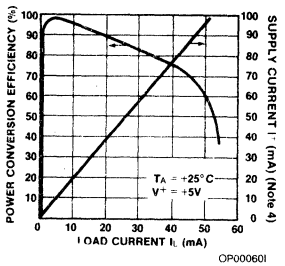
TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



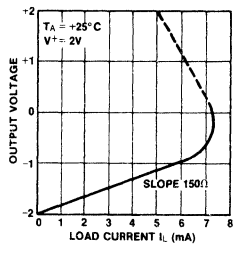
OP00010I

SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



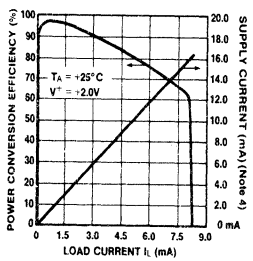
OP00060I

OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



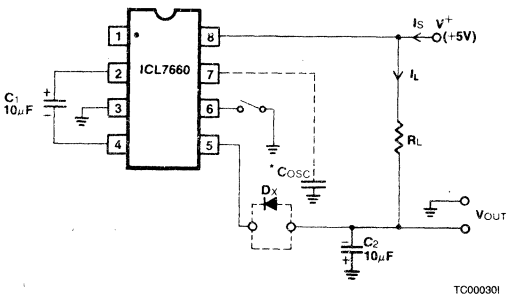
OP00020I

SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



OP00090I

NOTE 4. These curves include in the supply current that current fed directly into the load R_L from V^+ (see Figure 3). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7660, to the negative side of the load. Ideally, $V_{OUT} \cong 2\ V_{IN}$, $I_S \cong 2\ I_L$, so $V_{IN} \cdot I_S \cong V_{OUT} \cdot I_L$.



TC00030I

NOTES:

1. For large values of C_{OSC} (> 1000pF) the values of C_1 and C_2 should be increased to 100μF.
2. D_X is required for supply voltages greater than 6.5V @ −55°C ≤ T_A ≤ +70°C; refer to performance curves for additional information.

Figure 3: ICL7660 Test Circuit

DETAILED DESCRIPTION

The ICL7660 contains all the necessary circuitry to complete a negative voltage converter, with the exception of 2 external capacitors which may be inexpensive 10μF polarized electrolytic types. The mode of operation of the device may be best understood by considering Figure 4, which shows an idealized negative voltage converter. Capacitor C_1 is charged to a voltage, V^+, for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly V^+, assuming ideal switches and no load on C_2. The ICL7660 approaches this ideal situation more closely than existing non-mechanical circuits.

In the ICL7660, the 4 switches of Figure 4 are MOS power switches; S_1 is a P-channel device and S_2, S_3 & S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 & S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit startup, and under output short circuit conditions ($V_{OUT} = V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the ICL7660 by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 & S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the ICL7660 is an integral part of the anti-latchup circuitry, however its inherent voltage drop can degrade operation at low voltages.

Note: All typical values have been guaranteed by characterization and are not tested.

Therefore, to improve low voltage operation the "LV" pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 3.5 volts the LV terminal must be left open to insure latchup proof operation, and prevent device damage.

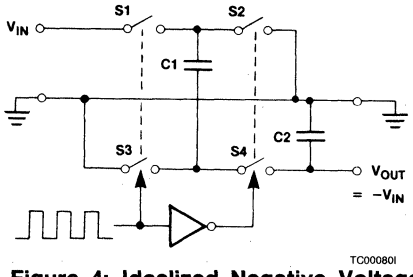


Figure 4: Idealized Negative Voltage Converter

THEORETICAL POWER EFFICIENCY CONSIDERATIONS

In theory a voltage converter can approach 100% efficiency if certain conditions are met:

A The drive circuitry consumes minimal power.

B The output switches have extremely low ON resistance and virtually no offset.

C The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7660 approaches these conditions for negative voltage conversion if large values of C_1 and C_2 are used.

ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS. The energy lost is defined by:

$$E = 1/2\ C_1\ (V_1^2 - V_2^2)$$

where V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 4) compared to the value of R_L, there will be a substantial difference in the voltages V_1 and V_2. Therefore it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

DO'S AND DON'TS

1. Do not exceed maximum supply voltages.
2. Do not connect LV terminal to GROUND for supply voltages greater than 3.5 volts.
3. Do not short circuit the output to V^+ supply for supply voltages above 5.5 volts for extended periods, however, transient conditions including startup are okay.
4. When using polarized capacitors, the + terminal of C_1 must be connected to pin 2 of the ICL7660 and the + terminal of C_2 must be connected to GROUND.
5. Add diode D_X as shown in Figure 3 for high-voltage, elevated temperature applications.
6. Add capacitor ($\sim 0.1\mu F$, disc) from pin 8 to ground to limit rate of rise of input voltage to approximately $2V/\mu s$.

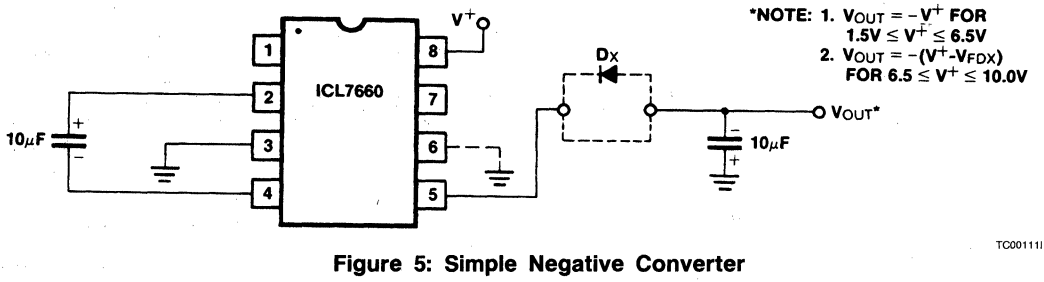


Figure 5: Simple Negative Converter

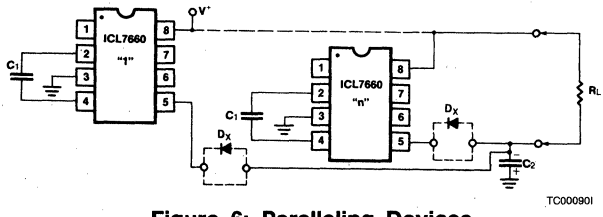


Figure 6: Paralleling Devices

Note: All typical values have been guaranteed by characterization and are not tested.

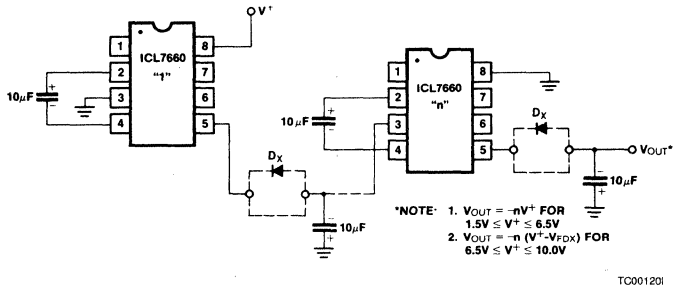


Figure 7: Cascading Devices for Increased Output Voltage

CONSIDERATIONS FOR HIGH VOLTAGE & ELEVATED TEMPERATURE

The ICL7660 will operate efficiently over its specified temperature range with only 2 external passive components (storage & pump capacitors), provided the operating supply voltage does not exceed 6.5 volts at +70°C and 5.0 volts at +125°C. Exceeding these maximums at the temperatures indicated may result in destructive latchup of the ICL7660. (Ref: Graph "Operating Voltage Vs. Temperature")

Operation at supply voltages of up to 10.0 volts over the full temperature range without danger of latchup can be achieved by adding a general purpose diode in series with the ICL7660 output, as shown by "D_X" in the circuit diagrams. The effect of this diode on overall circuit performance is the reduction of output voltage by one diode drop (approximately 0.6 volts).

TYPICAL APPLICATIONS

Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the ICL7660 for generation of negative supply voltages. Figure 5 shows typical connections to provide a negative supply where a positive supply of +1.5V to +10.0 volts is available. Keep in mind that pin 6 (LV) is tied to the supply negative (GND) for supply voltages below 3.5 volts, and that diode D_X must be included for proper operation at higher voltages and/or elevated temperatures.

The output characteristics of the circuit in Figure 5 are those of a nearly ideal voltage source in series with 55 ohms. Thus for a load current of −10mA and a supply voltage of +5 volts, the output voltage will be −4.3 volts. The dynamic output impedance due to the capacitor impedances is approximately $1/\omega C$, where:

$$C = C_1 = C_2$$

$$\text{which gives } \frac{1}{\omega C} = \frac{1}{2\pi\ f_{PUMP} \times 10^{-5}} \cong 3 \text{ ohms}$$

for $C = 10\mu F$ and $f_{PUMP} = 5kHz$ (1/2 of oscillator frequency)

Paralleling Devices

Any number of ICL7660 voltage convertors may be paralleled to reduce output resistance. The reservoir capacitor, C_2, serves all devices while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT}\ \text{(of ICL7660)}}{n\ \text{(number of devices)}}$$

Cascading Devices

The ICL7660 may be cascaded as shown to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n\ (V_{IN}),$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7660 R_{OUT} values.

Changing the ICL7660 Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 8. In order to prevent possible device latchup, a 1kΩ resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10kΩ pullup resistor to V^+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

Note: All typical values have been guaranteed by characterization and are not tested.

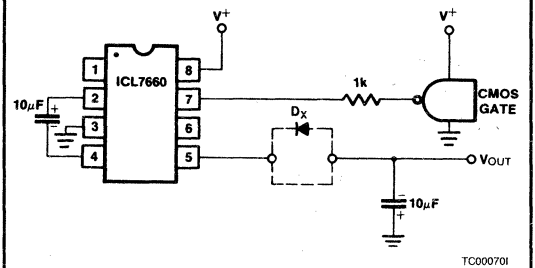


Figure 8: External Clocking

It is also possible to increase the conversion efficiency of the ICL7660 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is shown in Figure 9. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and reservoir (C_2) capacitors; this is overcome by increasing the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (Osc) and V^+ will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of C_1 and C_2 (from 10µF to 100µF).

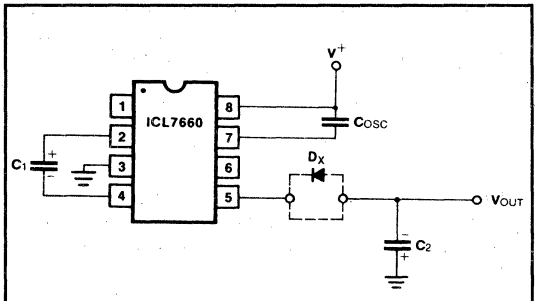


Figure 9: Lowering Oscillator Frequency

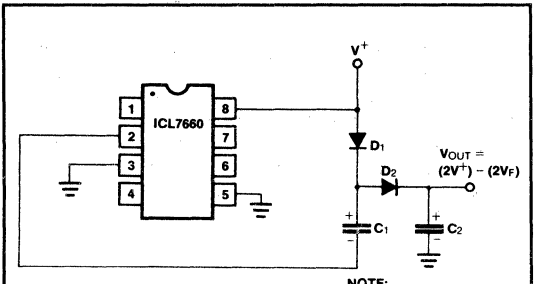


Figure 10: Positive Voltage Doubler

Positive Voltage Doubling

The ICL7660 may be employed to achieve positive voltage doubling using the circuit shown in Figure 10. In this application, the pump inverter switches of the ICL7660 are used to charge C_1 to a voltage level of $V^+ - V_F$ (where V^+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V^+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes $(2V^+) - (2V_F)$ or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for $V^+ = 5$ volts and an output current of 10mA it will be approximately 60 ohms.

Combined Negative Voltage Conversion and Positive Supply Doubling

Figure 11 combines the functions shown in Figures 5 and 10 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9 volts and −5 volts from an existing +5 volt supply. In this instance capacitors C_1 and C_3 perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir respectively for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

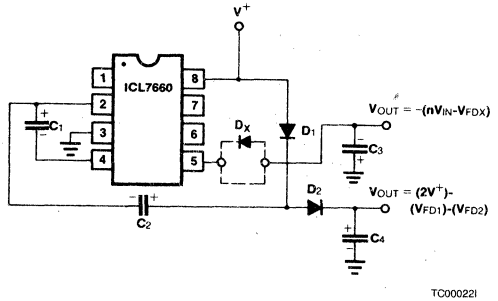


Figure 11: Combined Negative Voltage Converter and Positive Doubler

Voltage Splitting

The bidirectional characteristics can also be used to split a higher supply in half, as shown in Figure 12. The combined load will be evenly shared between the two sides, and a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 7, +15V can be converted (via +7.5, and −7.5) to a nominal −15V, although with rather high series output resistance (~250Ω).

Note: All typical values have been guaranteed by characterization and are not tested.

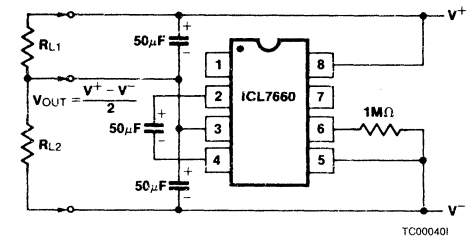


Figure 12: Splitting A Supply in Half

Regulated Negative Voltage Supply

In some cases, the output impedance of the ICL7660 can be a problem, particularly if the load current varies substantially. The circuit of Figure 13 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the ICL7660's output does not respond instantaneously to change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the 7660, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provides an output impedance of less than 5Ω to a load of 10mA.

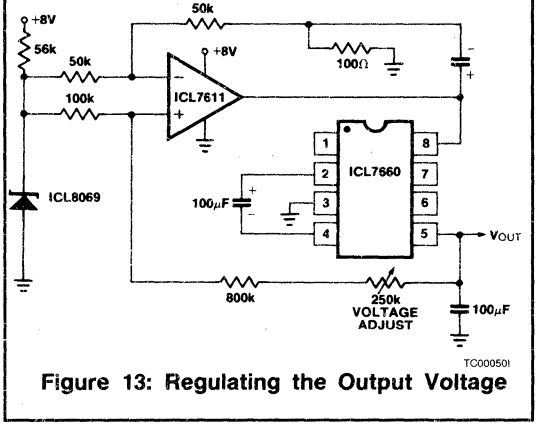


Figure 13: Regulating the Output Voltage

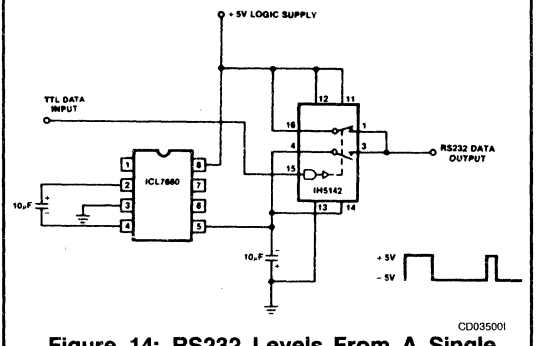


Figure 14: RS232 Levels From A Single 5V Supply

OTHER APPLICATIONS

Further information on the operation and use of the ICL7660 may be found in A051 "Principals and Applications of the ICL7660 CMOS Voltage Converter" by Peter Bradshaw and Dave Bingham.

5

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7662
CMOS Voltage Converter

GENERAL DESCRIPTION

The Intersil ICL7662 is a monolithic high-voltage CMOS power supply circuit which offers unique performance advantages over previously available devices. The ICL7662 performs supply voltage conversion from positive to negative for an input range of +4.5V to +20.0V, resulting in complementary output voltages of −4.5V to −20V. Only 2 non-critical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7662 can also function as a voltage doubler, and will generate output voltages up to +38.6V with a +20V input.

Contained on chip are a series DC power supply regulator, RC oscillator, voltage level translator, four output power MOS switches. A unique logic element senses the most negative voltage in the device and ensures that the output N-channel switch source-substrate junctions are not forward biased. This assures latchup free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 15.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be overdriven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+10 to +20V), the LV pin is left floating to prevent device latchup.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7662CTV	0°C to +70°C	TO-99
ICL7662CPA	0°C to +70°C	8 PIN MINI DIP
ICL7662MTV	−55°C to +125°C	TO-99
ICL7662/D	—	DICE**

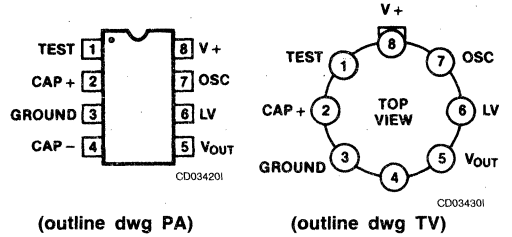
**Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.

FEATURES

- **No External Diode Needed Over Entire Temperature Range**
- **Pin Compatible With ICL7660**
- **Simple Conversion of +15V Supply to −15V Supply**
- **Simple Voltage Multiplication ($V_{OUT} = (-)\ nV_{IN}$)**
- **99.9% Typical Open Circuit Voltage Conversion Efficiency**
- **96% Typical Power Efficiency**
- **Wide Operating Voltage Range 4.5V to 20.0V**
- **Easy to Use — Requires Only 2 External Non-Critical Passive Components**

APPLICATIONS

- **On Board Negative Supply for Dynamic RAMs**
- **Localized μ-Processor (8080 Type) Negative Supplies**
- **Inexpensive Negative Supplies**
- **Data Acquisition Systems**
- **Up to −20V for Op Amps**



(outline dwg PA) (outline dwg TV)

Figure 1: Pin Configurations

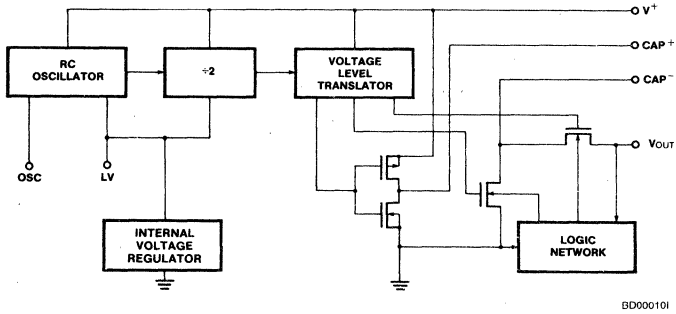


Figure 2: Functional Diagram

302064-003

Note: All typical values have been guaranteed by characterization and are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 22V
Oscillator Input Voltage (Note 1) .....
−0.3V to (V^+ +0.3V) for $V^+ < 10V$
(V^+ − 10V) to (V^+ +0.3V) for $V^+ > 10V$
Current into LV (Note 1) .....20μA for $V^+ > 10V$
Output Short Duration ..... Continuous

Power Dissipation (Note 2)
ICL7662CTY 500mW
ICL7662CPA 300mW
ICL7662MTY 500mW
Lead Temperature (Soldering, 10sec) .....300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS $V^+ = 15V$, $T_A = 25°C$, $C_{OSC} = 0$, unless otherwise stated. Test Circuit Figure 3.

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
V^+L V^+H	Supply Voltage Range–Lo Supply Voltage Range–Hi	$R_L = 10k\Omega$, LV = GND $R_L = 10k\Omega$, LV = Open	Min < T_A < Max Min < T_A < Max	4.5 9		11 20	V V
I^+	Supply Current	$R_L = \infty$, 'LV = Open	$T_A = 25°C$ 0°C < T_A < +70°C −55°C < T_A < +125°C		.25 .30 .40	.60 .85 1.0	μA
R_O	Output Source Resistance	I_O = 20mA, LV = Open	$T_A = 25°C$ 0°C < T_A < +70°C −55°C < T_A < +125°C		60 70 90	100 120 150	Ω
I^+_5	Supply Current	$V^+ = 5V$, $R_L = \infty$, LV = GND	$T_A = 25°C$ 0°C < T_A < +70°C −55°C < T_A < +125°C		20 25 30	150 200 250	μA
R_{O5}	Output Source Resistance	$V^+ = 5V$, I_O = 3mA, LV = GND	$T_A = 25°C$ 0°C < T_A < +70°C −55°C < T_A < +125°C		125 150 200	200 250 350	Ω
F_{OSC}	Oscillator Frequency				10		kHz
P_{eff}	Power Efficiency	$R_L = 2K\Omega$	$T_A = 25°C$ Min < T_A < Max	93 90	96 95		%
V_{OEf}	Voltage Conversion Effic.	$R_L = \infty$	Min < T_A < Max	97	99.9		%
I_{OSC}	Oscillator Sink or Source Current	$V^+ = 5V$ (V_{OSC} = 0V to +5V) $V^+ = 15V$ (V_{OSC} = +5V to +15V)			0.5 4.0		μA

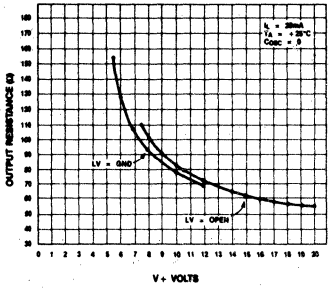
NOTES: 1. Connecting any terminal to voltages greater than V^+ or less than ground may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the ICL7662.
2. Derate linearly above 50°C by 5.5mW/°C.
3. Pin 1 is a Test pin and is not connected in normal use.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7662

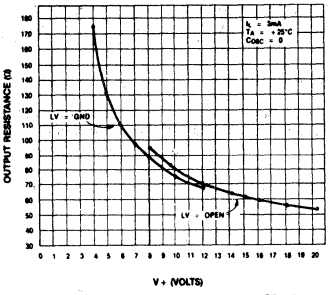
TYPICAL PERFORMANCE CHARACTERISTICS (See Test Circuit of Figure 3)

OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE



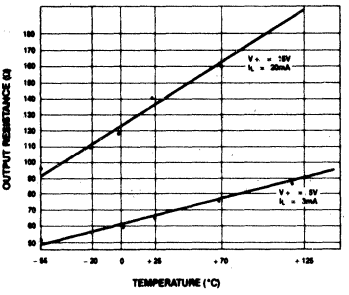
OP04671I

OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE



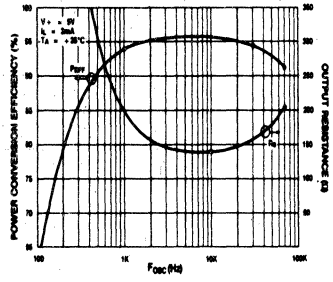
OP04771I

OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE



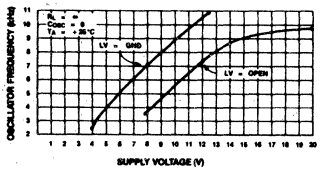
OP04681I

POWER CONVERSION EFFICIENCY AND OUTPUT SOURCE RESISTANCE AS A FUNCTION OF OSCILLATOR FREQUENCY OSC. FREQUENCY



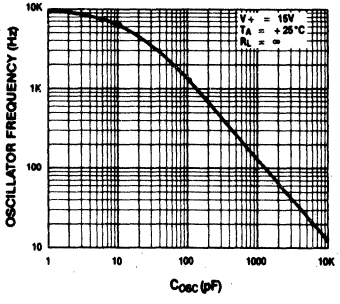
OP04691I

POWER CONVERSION EFFICIENCY AND OUTPUT SOURCE RESISTANCE AS A FUNCTION OF OSC. FREQUENCY



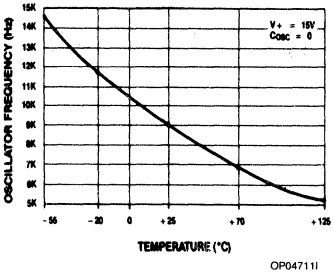
OP04761I

FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSC. CAPACITANCE



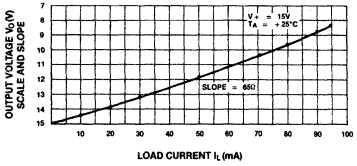
OP04701I

UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE



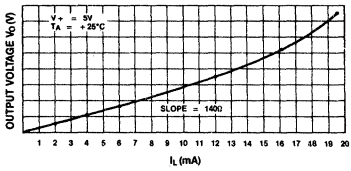
OP04711I

OUTPUT VOLTAGE AS A FUNCTION OF LOAD CURRENT



OP04721I

OUTPUT VOLTAGE AS A FUNCTION OF LOAD CURRENT

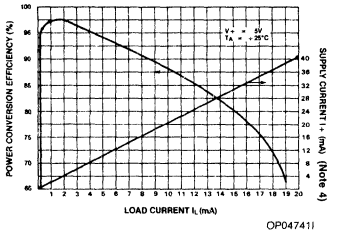


OP04731I

Note: All typical values have been guaranteed by characterization and are not tested.

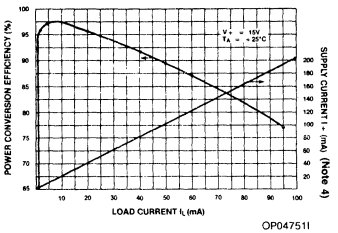
TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



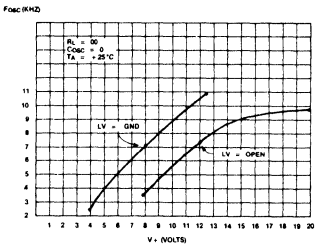
OP04741I

SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



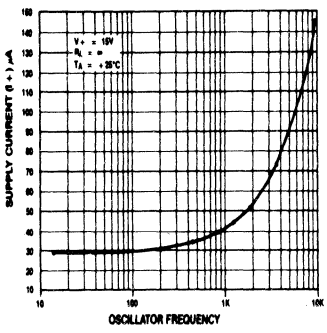
OP04751I

FREQUENCY OF OSCILLATION AS A FUNCTION OF SUPPLY VOLTAGE



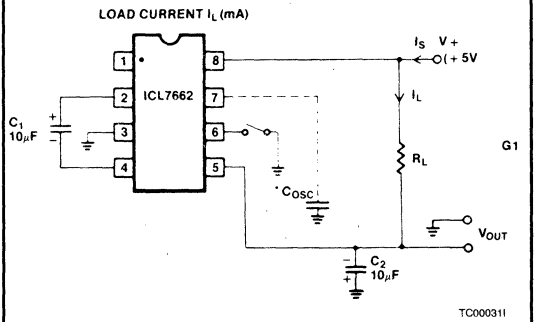
OP04782I

SUPPLY CURRENT AS A FUNCTION OF OSCILLATOR FREQUENCY



OP04791I

NOTE 4.
Note that these curves include in the supply current that current fed directly into the load R_L from V^+ (see Figure 3). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7662, to the negative side of the load.Ideally, $V_{LOAD} \simeq 2V_{IN}$, $I_S \simeq 2\ I_L$, so $V_{IN} \cdot I_S \simeq V_{LOAD} \cdot I_L$



NOTE: 1. For large value of C_{OSC} (> 1000pf) the values of C_1 and C_2 should be increased to 100μF.

Figure 3: ICL7662 Test Circuit

CIRCUIT DESCRIPTION

The ICL7662 contains all the necessary circuitry to complete a negative voltage converter, with the exception of 2 external capacitors which may be inexpensive 10μF polarized electrolytic capacitors. The mode of operation of the device may be best understood by considering Figure 4, which shows an idealized negative voltage converter. Capacitor C_1 is charged to a voltage, V^+, for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly V^+, assuming ideal switches and no load on C_2. The ICL7662 approaches this ideal situation more closely than existing non-mechanical circuits.

In the ICL7662, the 4 switches of Figure 4 are MOS power switches; S_1 is a P-channel device and S_2, S_3 & S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 & S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit startup, and under output short circuit conditions ($V_{OUT} = V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the ICL7662 by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 & S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the ICL7662 is an integral part of the anti-latchup circuitry, however its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the "LV" pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 11 volts the LV terminal must be left open to insure latchup proof operation, and prevent device damage.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7662

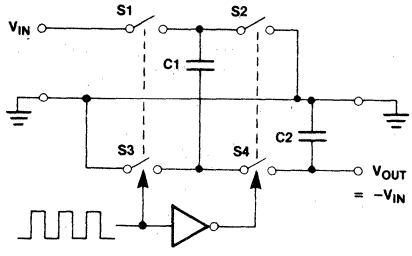


Figure 4: Idealized Negative Converter

THEORETICAL POWER EFFICIENCY CONSIDERATIONS

In theory a voltage multiplier can approach 100% efficiency if certain conditions are met:

A The drive circuitry consumes minimal power

B The output switches have extremely low ON resistance and virtually no offset.

C The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7662 approaches these conditions for negative voltage multiplication if large values of C_1 and C_2 are used. **ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS.** The energy lost is defined by:

$$E = 1/2\ C_1\ (V_1^2 - V_2^2)$$

where V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 4) compared to the value of R_L, there will be a substantial difference in the voltages V_1 and V_2. Therefore it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

DO'S AND DON'TS

1. Do not exceed maximum supply voltages.
2. Do not connect LV terminal to GROUND for supply voltages greater than 11 volts.
3. When using polarized capacitors, the + terminal of C_1 must be connected to pin 2 of the ICL7662 and the + terminal of C_2 must be connected to GROUND.

TYPICAL APPLICATIONS

Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the ICL7662 for generation of negative supply voltages. Figure 5 shows typical connections to provide a negative supply where a positive supply of +4.5V to 20.0V is available. Keep in mind that pin 6 (LV) is tied to the supply negative (GND) for supply voltages below 11 volts.

The output characteristics of the circuit in Figure 5 are those of a nearly ideal voltage source in series with 65 ohms. Thus for a load current of −10mA and a supply voltage of +15 volts, the output voltage will be 14.35 volts. The dynamic output impedance due to the capacitor impedances is approximately $1/\omega C$, where:

$$C = C_1 = C_2$$

$$\text{which gives } \frac{1}{\omega C} = \frac{1}{2\pi\ \text{fpump} \times 10^{-5}} = 3 \text{ ohms}$$

for C = 10μF and fpump = 5kHz (1/2 of oscillator frequency)

Paralleling Devices

Any number of ICL7662 voltage converters may be paralleled to reduce output resistance. The reservoir capacitor, C_2, serves all devices while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately

$$R_{OUT} = \frac{R_{OUT}\ \text{(of ICL7662)}}{n\ \text{(number of devices)}}$$

Cascading Devices

The ICL7662 may be cascaded as shown to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n\ (V_{IN}),$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7662 R_{OUT} values.

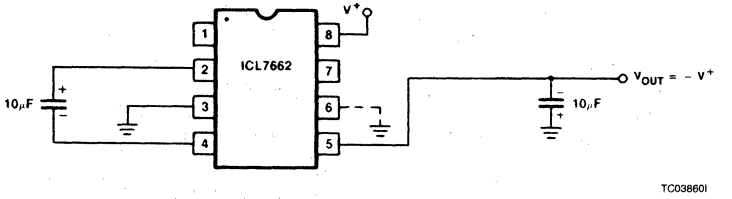


Figure 5: Simple Negative Converter

Note: All typical values have been guaranteed by characterization and are not tested.

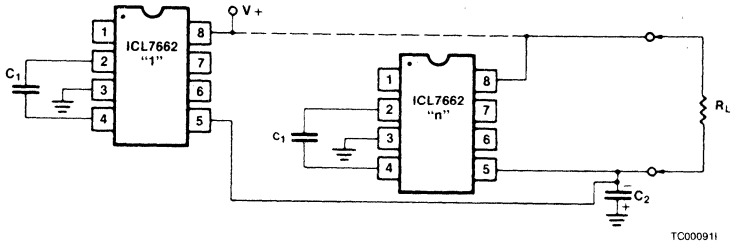


Figure 6: Paralleling Devices

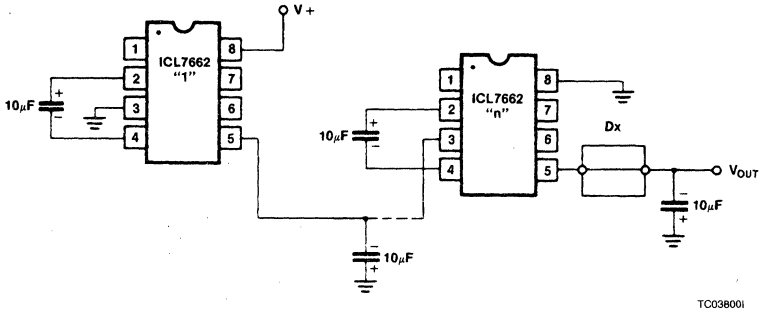


Figure 7: Cascading Devices for Increased Output Voltage

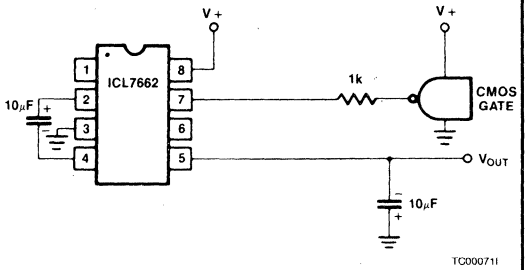


Figure 8: External Clocking

Changing the ICL7662 Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 8. In order to prevent possible device latchup, a 1kΩ resistor must be used in series with the clock output. In the situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10kΩ pullup resistor to V^+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

It is also possible to increase the conversion efficiency of the ICL7662 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is achieved by connecting an additional capacitor, C_{OSC}, as shown in Figure 9. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and reservoir (C_2) capacitors; this is overcome by increasing the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (Osc) and V^+ will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of C_1 and C_2 (from 10µF to 100µF).

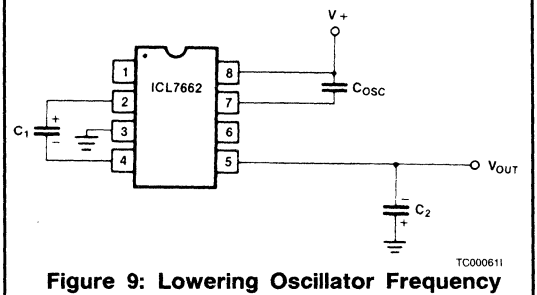


Figure 9: Lowering Oscillator Frequency

Positive Voltage Doubling

The ICL7662 may be employed to achieve positive voltage doubling using the circuit shown in Figure 10. In this

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7662

application, the pump inverter switches of the ICL7662 are used to charge C_1 to a voltage level of $V^+ - V_F$ (where V^+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V^+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes $(2V^+) - (2V_F)$ or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for $V^+ = 15$ volts and an output current of 10mA it will be approximately 70 ohms.

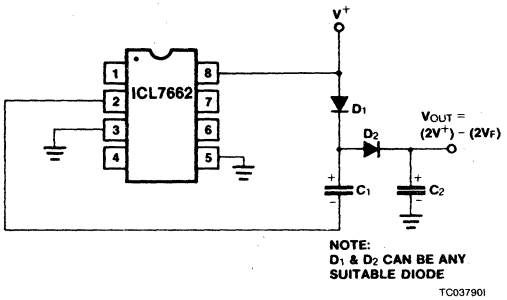


Figure 10: Positive Voltage Doubler

Combined Negative Voltage Conversion and Positive Supply Doubling

Figure 11 combines the functions shown in Figures 5 and 10 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9 volts and −5 volts from an existing +5 volt supply. In this instance capacitors C_1 and C_3 perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir respectively for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

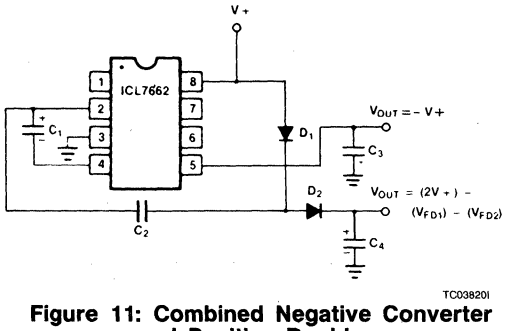


Figure 11: Combined Negative Converter and Positive Doubler

Voltage Splitting

The bidirectional characteristics can also be used to split a higher supply in half, as shown in Figure 12. The combined load will be evenly shared between the two sides and, a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 7, +30V can be converted (via +15V, and −15V) to a nominal −30V, although with rather high series output resistance (~250Ω).

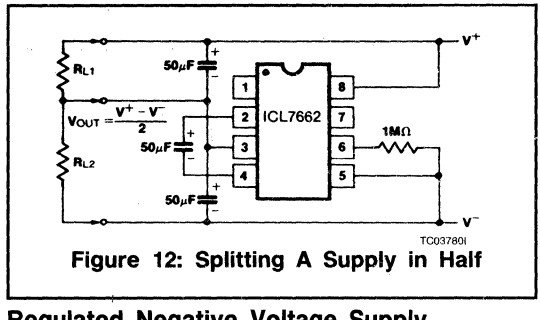


Figure 12: Splitting A Supply in Half

Regulated Negative Voltage Supply

In some cases, the output impedance of the ICL7662 can be a problem, particularly if the load current varies substantially. The circuit of Figure 13 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the ICL7662's output does not respond instantaneously to a change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the 7662, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provides an output impedance of less than 5Ω to a load of 10mA.

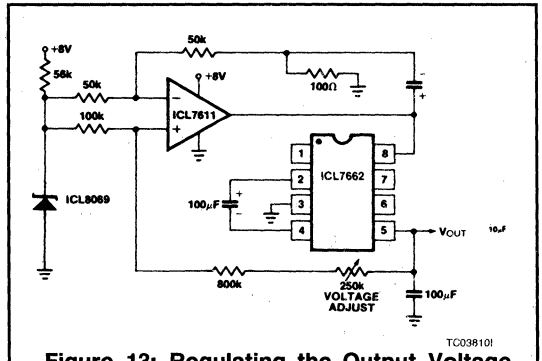


Figure 13: Regulating the Output Voltage

OTHER APPLICATIONS

Further information on the operation and use of the ICL7662 may be found in A051 "Principals and Applications of the ICL7660 CMOS Voltage Converter" by Peter Bradshaw and Dave Bingham.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7663/7664
CMOS Programmable Micropower Voltage Regulators

GENERAL DESCRIPTION

The ICL7663 (positive) and ICL7664 (negative) series regulators are low-power, high-efficiency devices which accept inputs from 1.6V to 10V and provide adjustable outputs over the same range at currents up to 40mA. Operating current is typically less than 4μA, regardless of load.

Output current sensing and remote shutdown are available on both devices, thereby providing protection for the regulators and the circuits they power. A unique feature, on the ICL7663 only, is a negative temperature coefficient output. This can be used, for example, to efficiently tailor the voltage applied to a multiplexed LCD through the driver (e.g., ICM7231/2/3/4) so as to extend the display operating temperature range many times.

The ICL7663 and ICL7664 are available in either an 8-pin plastic, TO-99 can, CERDIP, and SOIC packages.

FEATURES

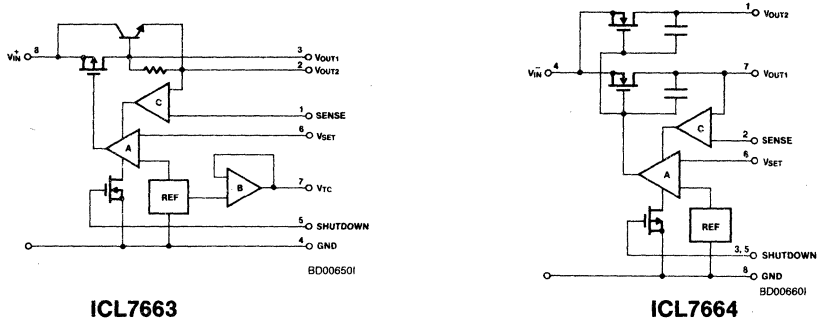
- **Ideal for Battery-Operated Systems: Less Than 4μA Typical Current Drain**
- **Will Handle Input Voltages From 1.6V to 16V**
- **Very Low Input-Output Differential Voltage**
- **1.3V Bandgap Voltage Reference**
- **Up to 40mA Output Current**
- **Output Shutdown Via Current-Limit Sensing or External Logic Signal**
- **Output Voltages Programmable From 1.3V to 16V**
- **Output Voltages With Programmable Negative Temperature Coefficients (ICL7663 Only)**

ORDERING INFORMATION

POSITIVE REGULATOR		
PART NUMBER	**TEMPERATURE RANGE**	**PACKAGE**
ICL7663CBA	0°C to +70°C	8-Lead SOIC
ICL7663CPA	0°C to +70°C	8-Lead MiniDIP
ICL7663CJA	0°C to +70°C	8-Lead CERDIP
ICL7663/D	—	DICE**
ICL7663CTV	0°C to +70°C	8-Lead TO-99

NEGATIVE REGULATOR		
PART NUMBER	**TEMPERATURE RANGE**	**PACKAGE**
ICL7664/D	—	DICE**
ICL7664CBA	0°C to +70°C	8-Lead SOIC
ICL7664CJA	0°C to +70°C	8-Lead CERDIP
ICL7664CPA	0°C to +70°C	8-Lead MiniDIP
ICL7664CTV	0°C to +70°C	8-Lead TO-99

**Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.



ICL7663 ICL7664

Figure 1: Functional Diagram

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7663/7664

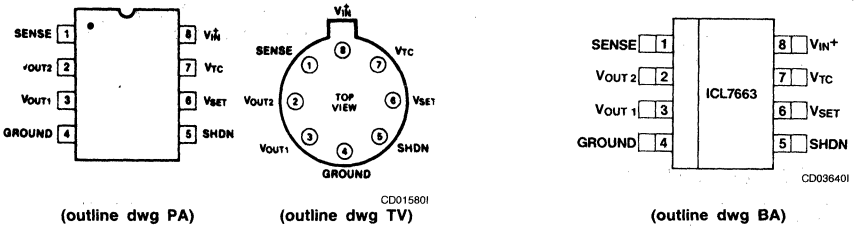
INTERSIL

ABSOLUTE MAXIMUM RATINGS, ICL7663 POSITIVE REGULATOR

Input Supply Voltage ..... +18V
Any Input or Output Voltage (Note 1) (Terminals 1, 2, 3, 5, 6, 7).....(GND −0.3V) to (V_{IN}^{+} +0.3V)
Output Source Current
(Terminal 2) 50mA
(Terminal 3) 25mA
Output Sinking Current (Terminal 7) ..... −10mA
Power Dissipation (Note 2)
MiniDIP 200mW
TO-99 Can.....300mW
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) .....300°C

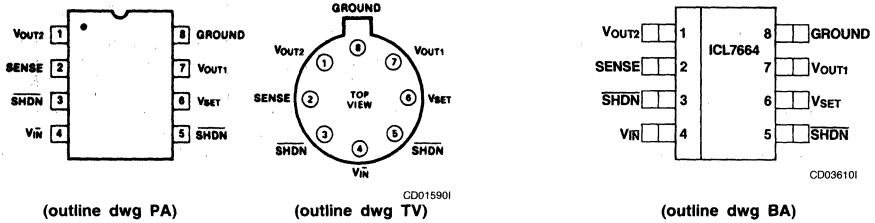
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ICL7663 Positive Regulator



(outline dwg PA) (outline dwg TV) (outline dwg BA)

ICL7664 Negative Regulator



(outline dwg PA) (outline dwg TV) (outline dwg BA)

Figure 2: Pin Configurations

ICL7663 ELECTRICAL CHARACTERISTICS

V_{IN}^{+} = 9V, V_{OUT} = 5V, T_A = +25°C, unless otherwise specified. See Test Circuit Figure 3.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
V_{IN}	Input Voltage	T_A = +25°C 0°C ≤ T_A ≤ +70°C	1.5 1.6		16.0 16.0	V
I_Q	Quiescent Current	R_L = ∞, 1.4V ≤ V_{OUT} ≤ 8.5V; V_{IN} = 16V R_L = ∞, 1.4V ≤ V_{OUT} ≤ 8.5V; V_{IN} = 9V		4.0 3.5	12 10	µA
V_{SET}	Reference Voltage		1.2	1.3	1.4	V
$\frac{\Delta V_{SET}}{\Delta T}$	Temperature Coefficient	8.5V < V_{IN} < 9V		±200		ppm
$\frac{\Delta V_{SET}}{V_{SET}\Delta V_{IN}}$	Line Regulation	2V < V_{IN} < 9V		0.03		%/V
I_{SET}	V_{SET} Input Current			±0.01	10	nA
I_{SHDN}	Shutdown Input Current			±0.01	10	nA
V_{SHDN}	Shutdown Input Voltage	V_{SHDN}HI: Both V_{OUT} Disabled V_{SHDN}LO: Both V_{OUT} Enabled	1.4		0.3	V

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7663 ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I_{SENSE}	Sense Pin Input Current			0.01	10	nA
V_{CL}	Sense Pin Input Threshold Voltage	$V_{CL} = V_{OUT2} - V_{SENSE}$ (Current-Limit Threshold)		0.7		V
R_{SAT}	Input-Output On-Resistance (Note 3)	$V_{IN} = 2V$ $V_{IN} = 9V$ $V_{IN} = 15V$		200 70 50		Ω
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$\Delta I_{OUT1} = 100\mu A$ @ $V_{OUT1} = 5V$ $\Delta I_{OUT2} = 10mA$ @ $V_{OUT2} = 5V$		2.0 1.0		Ω
I_{OUT2}	Available Output Current (V_{OUT2})	$V_{IN} = 3V$ $V_{OUT} = V_{SET}$ $V_{IN} = 9V$ $V_{OUT} = 5V$ $V_{IN} = 15V$ $V_{OUT} = 5V$	10 25 40			mA
V_{TC}	Negative-Tempco Output (Note 4)	Open-Circuit Voltage		0.9		V
I_{TC}		Maximum Sink Current	0	8	2.0	mA
$\frac{\Delta V_{TC}}{\Delta T}$	Temperature Coefficient of V_{TC} Output	Open Circuit		+2.5		mV/°C
$I_{L(min)}$	Minimum Load Current	(Includes V_{SET} Divider)	1.0			μA

NOTES: 1. Connecting any terminal to voltages greater then (V_{IN}^{+} +0.3V) or less than (GND−0.3V) may cause destructive device latchup. It is recommended that no inputs from sources operating on external power supplies be applied prior to ICL7663B power-up.

2. Derate linearly above 50°C at 5mW/°C for minidip and 7.5mW/°C for TO-99 can.

3. This parameter refers to the on-resistance of the MOS pass transistor. The minimum input-output voltage differential at low current (under 5mA), can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.

4. This output has a positive temperature coefficient. Using it in combination with the inverting input of the regulator at V_{SET}, a negative coefficient results in the output voltage. See Figure 4 for details. Pin will not source current.

5

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7663/7664

ABSOLUTE MAXIMUM RATINGS, ICL7664 NEGATIVE REGULATOR

Input Supply Voltage ..... −18V
Any Input or Output Voltage (Note 1) Terminals 1, 2, 3, 4, 5, 6, 7).....(GND +0.3V) to ($V_{\overline{IN}}$ −0.3V)
Output Sink Current
(Terminals 1, 7) 25mA

Power Dissipation (Note 2)
MiniDIP 200mW
TO-99 .....300mW
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) .....300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

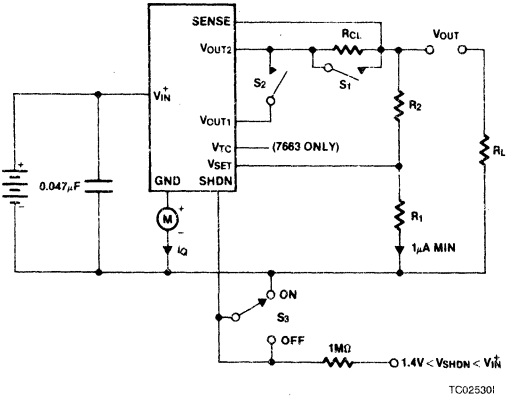
ICL7664 ELECTRICAL CHARACTERISTICS

$V_{\overline{IN}}$ = −9V, V_{OUT} = −5V, T_A = +25°C, unless otherwise specified. See Test Circuit Figure 3.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{IN}	Input Voltage	T_A = +25°C 0°C ≤ T_A ≤ +70°C	−1.5 −1.6		−16.0 −16.0	V
I_Q	Quiescent Current	R_L = ∞, −1.4V ≤ V_{OUT} ≤ −8.5V V_{IN} = 16V V_{IN} = 9V		4.0 3.5	12 10	μA
V_{SET}	Reference Voltage		−1.2	−1.3	−1.4	V
$\frac{\Delta V_{SET}}{\Delta T}$	Temperature Coefficient	−8.5V < V_{IN} < −9V		±200		ppm
$\frac{\Delta V_{SET}}{V_{SET}\Delta V_{IN}}$	Line Regulation	−2V < V_{IN} < −9V		0.03		%/V
I_{SET}	V_{SET} Input Current			±0.01	10	nA
I_{SHDN}	Shutdown Input Current			±0.01	10	nA
V_{SHDN}	Shutdown Input Voltage	V_{SHDN}HI: Both V_{OUT} Disabled V_{SHDN}LO: Both V_{OUT} Enabled	−0.3		−1.6	V
I_{SENSE}	Sense Pin Input Current			0.01	10	nA
V_{CL}	Sense Pin Input Threshold Voltage	V_{CL} = V_{OUT2} − V_{SENSE} (Current-Limit Threshold)		−0.35		V
R_{SAT}	Input-Output On-Resistance (Note 3)	V_{IN} = 2V V_{IN} = 9V V_{IN} = 15V		150 40 30		Ω
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	ΔI_{OUT1} = 100μA @ V_{OUT} = −5V		2.0		Ω
I_{OUT}	Output Current V_{OUT1} or V_{OUT2}	V_{IN} = 3V V_{OUT} = V_{SET} V_{IN} = 9V V_{OUT} = −5V V_{IN} = 15V V_{OUT} = −5V		−2 −20 −40		mA
$I_{L(min)}$	Minimum Load Current (Includes V_{SET} Divider)		1.0			μA

NOTES: 1. Connecting any terminal to voltages greater then (GND +0.3V) or less then ($V_{\overline{IN}}$ −0.3V) may cause destructive device latchup. It is recommended that no inputs from sources operating on external power supplies be applied prior to ICL7664 power-up.
2. Derate linearly above 50°C at 5mW/°C for minidip and 7.5mW/°C for TO-99 can.
3. This parameter refers to the on-resistance of the MOS pass transistor. The minimum input-output voltage differential can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.

Note: All typical values have been guaranteed by characterization and are not tested.



NOTES: 1. S_1 when closed, disables output current limiting.

2. For ICL7664, exchange V_{OUT1} and V_{OUT2}. S_2 action differs, as follows:

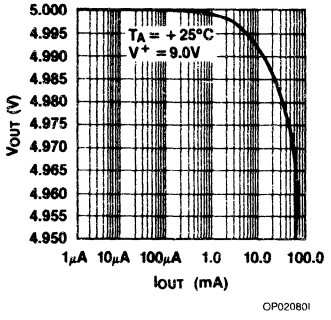
DEVICE	S_2 CLOSED	S_2 OPEN
ICL7663	V_{OUT1}	V_{OUT2}
ICL7664	$V_{OUT1} + V_{OUT2}$	V_{OUT1}

3. $V_{OUT} = \frac{R_2 + R_1}{R_1} V_{SET}$
4. I_Q quiescent current is measured at GND pin by meter M. S_3 when ON, permits normal operation,
5. when OFF, shuts down both V_{OUT1} and V_{OUT2}.

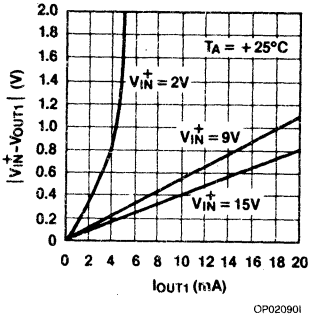
Figure 3: Test Circuit for ICL7663/64 (Polarities shown are for ICL7663. Reverse for ICL7664)

TYPICAL PERFORMANCE CHARACTERISTICS

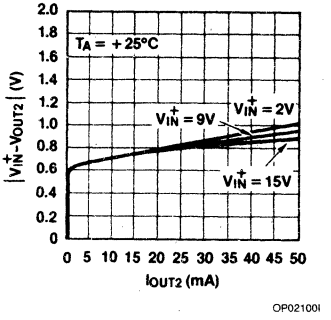
ICL7663 OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



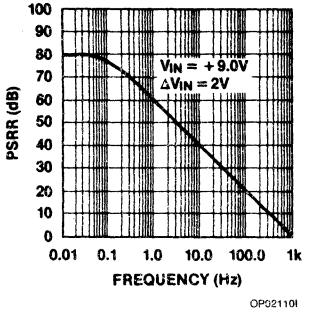
ICL7663 V_{OUT1} INPUT-OUTPUT DIFFERENTIAL VS OUTPUT CURRENT



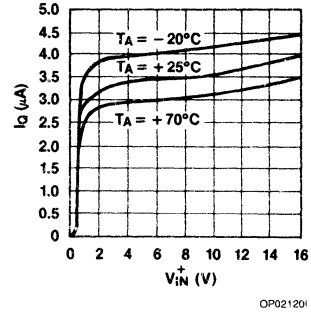
ICL7663 V_{OUT2} INPUT-OUTPUT DIFFERENTIAL VS OUTPUT CURRENT



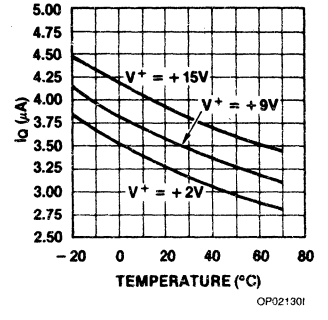
ICL7663 INPUT POWER SUPPLY REJECTION RATIO



ICL7663 QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



ICL7663 QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



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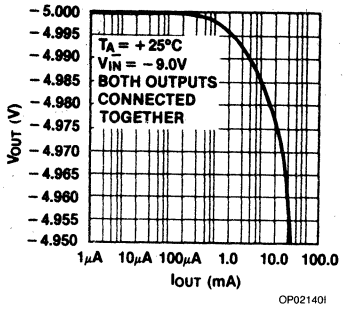
Note: All typical values have been guaranteed by characterization and are not tested.

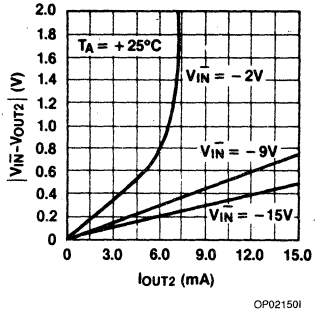
ICL7663/7664

TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

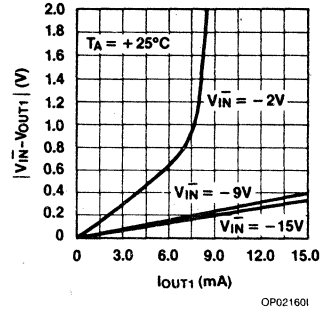
ICL7664 OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



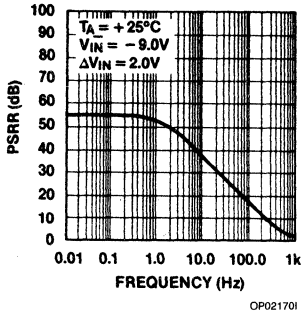
ICL7664 V_{OUT1} INPUT-OUTPUT DIFFERENTIAL VS OUTPUT CURRENT



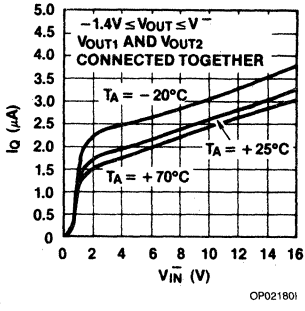
ICL7664 V_{OUT2} INPUT-OUTPUT DIFFERENTIAL VS OUTPUT CURRENT



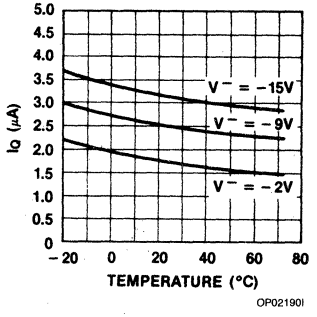
ICL7664 INPUT POWER SUPPLY REJECTION RATIO



ICL7664 QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



ICL7664 QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



DETAILED DESCRIPTION

The ICL7663 and ICL7664 are CMOS integrated circuits which contain all the functions of a voltage regulator plus protection circuitry on a single monolithic chip. Referring to the functional diagrams (Figure 1), it can be seen that each contains a bandgap-type voltage reference of 1.3 Volts. This voltage, therefore, is the lowest output voltage the regulators can control (−1.3V for the ICL7664). Error amplifier A drives either a P-channel (ICL7663) or an N-channel (ICL7664) pass transistor which is sufficient for low (under about 5mA) currents; this transistor is augmented by a duplicate in the ICL7664, which permits higher current outputs. In the ICL7663, the high current output is passed by an NPN bipolar transistor connected as a follower. This configuration gives more gain and lower output impedance.

Logic-controlled shutdown is implemented via an MOS transistor of the appropriate polarity. Current-sensing is achieved with comparator C, which functions with the V_{OUT2} line on each chip. Finally, the positive regulator (ICL7663 only) has an output (V_{TC}) from a buffer amplifier (B), which can be used to generate programmable-temperature-coefficient output voltages.

The amplifiers, reference and comparator circuitry all operate at bias levels well below 1μA to achieve the extremely low quiescent current. This does limit the dynamic response of the circuits, however, and transients are best dealt with outside the regulator loop.

BASIC OPERATION

The ICL7663 and ICL7664 are designed to regulate battery voltages in the 5V to 15V region at maximum load currents of about 5mA to 30mA. Although intended as low power devices, power dissipation limits must be observed. For example, the power dissipation in the case of a 10V supply regulated down to 2V with a load current of 30mA clearly exceeds the power dissipation rating of the minidip: $(10-2)(30)\ (10^{-3}) = 240mW$. The test circuit illustrates proper use of the devices. Although the following discussion refers to the ICL7663, it applies as well to the parallel features of the ICL7664 as long as the appropriate polarities are reversed. Individual features and precautions will be discussed where appropriate.

CMOS devices generally require two precautions: every input pin must go somewhere, and maximum values of applied voltages and current limits must be rigorously observed. Neglecting these precautions may lead to, at the least, incorrect or non-operation, and at worst, destructive device failure. To avoid the problem of latchup, do not apply inputs to any pins before supply voltage is applied.

Note: All typical values have been guaranteed by characterization and are not tested.

Input Voltages — These regulators accept working inputs of 1.4V to 18V. When power is applied, the rate-of-rise of the input may be hundreds of volts per microsecond. This is potentially harmful to the regulators, where internal operating currents are in the nanoampere range. The 0.047μF capacitor on the device side of the switch will limit inputs to a safe level around 2V/μs. Use of this capacitor is suggested in all applications. In severe rate-of-rise cases, it may be advisable to use an RC network on the SHutDowN pin to delay output turn-on. Battery charging surges, transients, and assorted noise signals should be kept from the regulators by RC filtering, zener protection, or even fusing.

Output Voltages — The resistor divider R_2/R_1 is used to scale the reference voltage, V_{SET}, to the desired output using the formula $V_{OUT} = (1 + R_2/R_1)\ V_{SET}$. In the ICL7664, V_{IN} and V_{SET} are negative, so V_{OUT} will also be negative. Suitable arrangements of these resistors, using a potentiometer, enables exact values for V_{OUT} to be obtained. Because of the low leakage current of the V_{SET} terminal, these resistors can be tens of megohms for minimum additional quiescent drain current. However, *some* load current is required for proper operation, so for extremely low-drain applications it is necessary to draw at least 1μA. This can include the current for R_2 and R_1.

Output voltages up to nearly the V_{IN} supply may be obtained at low load currents, while the low limit is the reference voltage. The minimum input-output differential in each regulator is obtained using the V_{OUT1} terminal.

Output Currents — For the ICL7663, low output currents of less than 5mA are obtained with the least input-output differential from the V_{OUT1} terminal (connect V_{OUT2} to V_{OUT1}). Either output may be used on the ICL7664, with the unused output connected to $V_{\overline{IN}}$. Where higher currents are needed, use V_{OUT2} on the ICL7663 (V_{OUT1} should be left open in this case) and parallel V_{OUT1} and V_{OUT2} on the ICL7664.

High output currents can be obtained only as far as package dissipation allows. It is strongly recommended that output current-limit sensing be used in such cases.

Current-Limit Sensing — The on-chip comparator (C in the block diagrams) permits shutdown of the regulator output in the event of excessive current drain. As the test circuits show, a current-limiting resistor, R_{CL}, is placed in series with V_{OUT2}, and the SENSE terminal is connected to the load side of R_{CL}. When the current through R_{CL} is high enough to produce a voltage drop equal to V_{CL} (0.7V for ICL7663, 0.35V for ICL7664) the voltage feedback is bypassed and the regulator output will be limited to this current. Therefore, when the maximum load current (I_{LOAD}) is determined, simply divide V_{CL} by I_{LOAD} to obtain the value for R_{CL}.

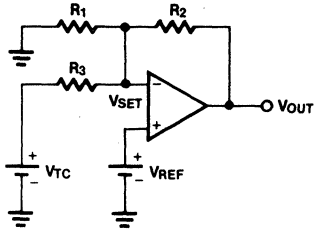
Logic-Controllable Shutdown — When equipment is not needed continuously (e.g., in remote data-acquisition systems), it is desirable to eliminate its drain on the system until it *is* required. This usually means switches, with their unreliable contacts. Instead, the ICL7663 and ICL7664 can be shut down by a logic signal, leaving only I_Q (under 4μA) as a drain on the power source. Since this pin must not be left open, it should be tied to ground if not needed. A voltage of less than 0.3V for the ICL7663, and greater than −0.3V for the ICL7664 will keep the regulator ON, and a voltage level of more than 1.4V but less than $V_{\overline{IN}}^{+}$ for the ICL7663, and less than −1.4V but not less than $V_{\overline{IN}}$ for the ICL7664 control will turn the outputs OFF. If there is a possibility that the control signal could exceed the regulator input ($V_{\overline{IN}}^{+}$ or $V_{\overline{IN}}$), the current from this signal should be limited to 100μA maximum by a high-value (1MΩ) series resistor. This situation may occur when the logic signal originates from a system powered separately from that of the regulator.

Additional Circuit Precautions — These regulators have poor rejection of voltage fluctuations from AC sources above 10Hz or so. To prevent the output from responding (where this might be a problem), a reservoir capacitor across the load is advised. The value of this capacitor is chosen so that the regulated output voltage reaches 90% of its final value in 20ms. From

$$I = C\frac{\Delta V}{\Delta t},\quad C = I_{OUT}\frac{(20 \times 10^{-3})}{0.9V_{OUT}} = 0.022\frac{I_{OUT}}{V_{OUT}}.$$

In addition, where such a capacitor is used, a current-limiting resistor is also suggested (see **"Current-Limit Sensing"**).

Producing Output Voltages With Negative Temperature Coefficients — The ICL7663 has an additional output (not present on the ICL7664) which is 0.9V relative to GND and has a tempco of +2.5mV/°C. By applying this voltage to the inverting input of amplifier A (i.e., the V_{SET} pin), output voltages having negative TC may be produced. The TC of the output voltage is controlled by the R_2/R_3 ratio (see Figure 4 and its design equations).



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EQ.1: $V_{OUT} = V_{SET}(1 + \frac{R_2}{R_1}) + \frac{R_2}{R_3}(V_{SET} - V_{TC})$

EQ.2: TC $V_{OUT} = -\frac{R_2}{R_3}(TCV_{TC})$ in mV/°C

WHERE: $V_{SET} = 1.3V$
$V_{TC} = 0.9V$
$TCV_{TC} = +2.5mV/°C$

Figure 4: Generating Negative Temperature Coefficients

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7663/7664

APPLICATIONS

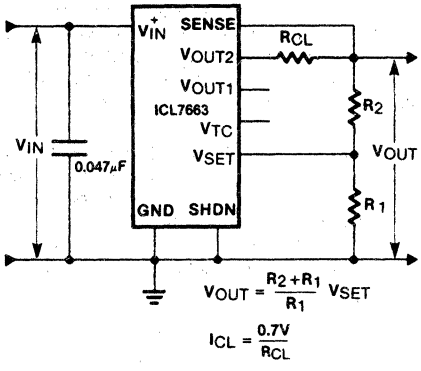


Figure 5: Basic Application of ICL7663 as Positive Regulator with Current Limit

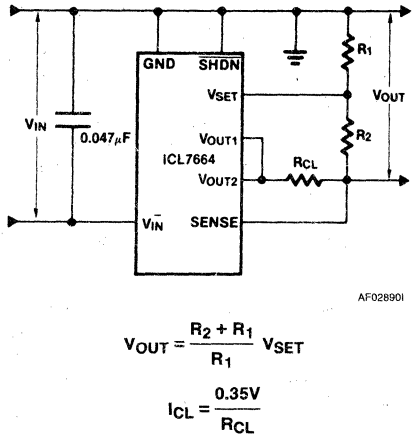
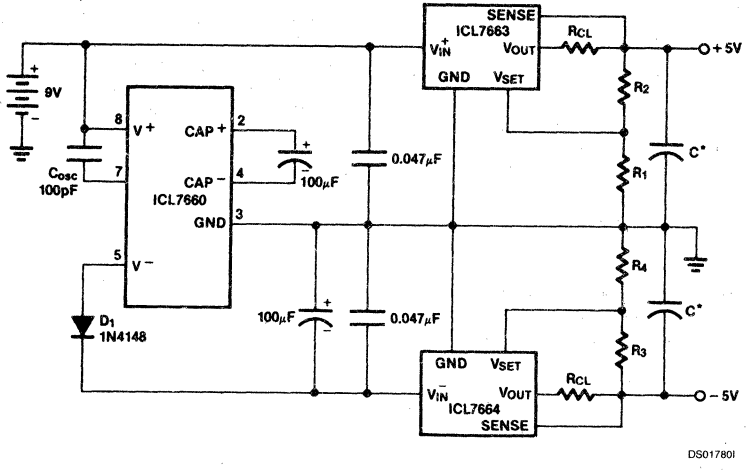


Figure 6: Basic Application of ICL7664 as Negative Regulator with Current Limit



*Values depend on load characteristics

Figure 7: Generating regulated split supplies from a single supply.

The oscillation frequency of the ICL7660 is reduced by the external oscillator capacitor, so that it inverts the battery voltage more efficiently.

Note: All typical values have been guaranteed by characterization and are not tested.

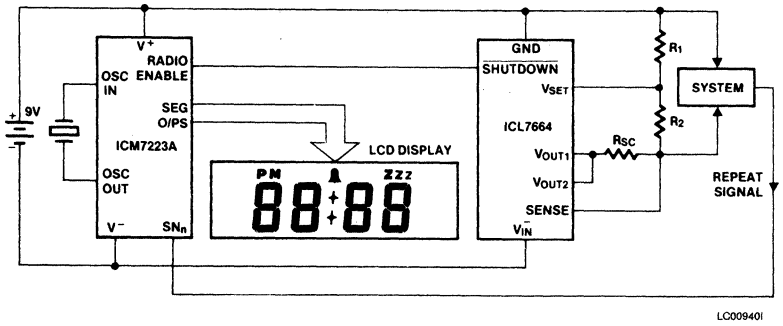


Figure 8: Once a Day System.

This circuit will turn on a regulated supply to a system for one minute every day, via the $\overline{\text{SHUTDOWN}}$ pin on the ICL7664, and under control of the ICM7223A Alarm Clock circuit. If the system decides it needs another one minute activation, pulling the REPEAT line to V^+ (GND) during one activation will trigger a subsequent activation after a snooze interval set by the choice of SN pins (2 mins shown). Alternatively, activation of the Sleep timer, without pause, can be achieved. See ICM7223A data sheet for details.

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Note: All typical values have been guaranteed by characterization and are not tested.

ICL7663/7664

ICL7663B/4B ADDENDUM TO THE ICL7663/4 DATASHEET

This Addendum to the standard ICL7663/4 datasheet describes changes and/or modifications to the DC Operating characteristics applicable to the ICL7663B/ICL7664B devices. The following table indicates those limits to which the ICL7663B/ICL7664B is tested and/or guaranteed operational.

ICL7663B POSITIVE REGULATOR ORDERING INFORMATION

POSITIVE REGULATOR		
ICL7663B/D	—	DICE
ICL7663BCBA	0°C to 70°C	8-pin S.O.I.C.
ICL7663BCJA	0°C to 70°C	8-pin CERDIP
ICL7663BCPA	0°C to 70°C	8-pin MiniDIP
ICL7663BCTV	0°C to 70°C	TO-99

ABSOLUTE MAXIMUM RATINGS ICL7663B

Input Supply Voltage ..... +12V
Any Input or Output Voltage (Note 1) Terminals 1, 2, 3, 4, 5, 6, 7).....(GND −0.3V) to (V_{IN}^+ +0.3V)
Output Source Current
(Terminal 2) 50mA
(Terminal 3) 25mA
Output Sinking Current (Terminal 7) ..... −10mA
Power Dissipation (Note 2)
MiniDIP 200mW
TO-99 Can.....300mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ICL7663B OPERATING CHARACTERISTICS $V_{IN}^+ = 9V$, $V_{OUT} = 5V$, $T_A = +25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{IN}^+	Input Voltage	$T_A = +25°C$ $20°C \le T_A \le +70°C$	1.5 1.6		10 10	V
I_Q	Quiescent Current	$\{R_L = \infty$ $\{1.4V \le V_{OUT} \le 8.5V\}$		3.5	10	µA
V_{SET}	Reference Voltage		1.2	1.3	1.4	V
$\frac{\Delta V_{SET}}{\Delta T}$	Temperature Coefficient	$8.5V < V_{IN}^+ < 9V$		±200		ppm
$\frac{\Delta V_{SET}}{V_{SET}\Delta V_{IN}}$	Line Regulation	$2V < V_{IN}^+ < 9V$		0.03		%/V
I_{SET}	V_{SET} Input Current			±0.01	10	nA
I_{SHDN}	Shutdown Input Current			±0.01	10	nA
V_{SHDN}	Shutdown Input Voltage	V_{SHDN}HI: Both V_{OUT} Disabled V_{SHDN}LO: Both V_{OUT} Enabled	1.4		0.3	V
I_{SENSE}	Sense Pin Input Current			0.01	10	nA
V_{CL}	Sense Pin Input Threshold Voltage	$V_{CL} = V_{OUT2} - V_{SENSE}$ (Current-Limit Threshold)		0.7		V
R_{SAT}	Input-Output Saturation Resistance (Note 3)	$V_{IN}^+ = 2V$ $V_{IN}^+ = 9V$		200 70		Ω
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$\Delta I_{OUT1} = 100µA$ @ $V_{OUT1} = 5V$ $\Delta I_{OUT2} = 10mA$ @ $V_{OUT2} = 5V$		2 1		Ω
I_{OUT2}	Available Output Current (V_{OUT2})	$V_{IN}^+ = 3V$ $V_{OUT} = V_{SET}$ $V_{IN}^+ = 9V$ $V_{OUT} = 5V$	10 25			mA
V_{TC}	Negative-Tempco Output (Note 4)	Open-Circuit Voltage		0.9		V
I_{TC}		Maximum Sink Current	0	8	2	mA

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7663B OPERATING CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
$\frac{\Delta V_{TC}}{\Delta T}$	Temperature Coefficient	Open Circuit		+2.5		mV/°C
$I_{L(min)}$	Minimum Load Current	(Includes V_{SET} Divider)			1	μA

NOTES:
1. Connecting any terminal to voltages greater than (V_{IN} +0.3V) or less than (GND −0.3V) may cause destructive device latchup. It is recommended that no inputs from sources operating on external power supplies be applied prior to ICL7663B power-up.
2. Derate linearly above 50°C at 5mW/°C for minidip and 7.5mW/°C for TO-99 can.
3. This parameter refers to the saturation resistance of the MOS pass transistor. The minimum input-output voltage differential at low current (under 5mA), can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.
4. This output has a positive temperature coefficient. Using it in combination with the inverting input of the regulator at V_{SET}, a negative coefficient results in the output voltage. See Figure 3 for details. Pin will not source current.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7663/7664

ICL7664B NEGATIVE REGULATOR

ORDERING INFORMATION

Negative Regulator		
ICL7664BCPA	0 to +70°C	8-pin MiniDIP
ICL7664BCTV	0 to +70°C	TO-99
ICL7664B/D	—	DICE
ICL7664BCBA	0 to +70°C	8-pin S.O.I.C
ICL7664BCJA	0 to +70°C	8-pin CERDIP

ABSOLUTE MAXIMUM RATINGS ICL7664B

Input Supply Voltage ..... −12V
Any Input or Output Voltage (Note 1)
(Terminals 1,2,3,4,5,6,7,) ..... (GND +0.3V) to ($V_{\overline{IN}}$-0.3V)
Output Source Current
(Terminal 1,7) ..... −25mA
Power Dissipation (Note 2)
MiniDIP 200mW
TO-99 ..... 300mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ICL7664B OPERATING CHARACTERISTICS

$V_{\overline{IN}}$ = 9V, V_{out} = −5V, T_A = +25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
$V_{\overline{IN}}$	Input Voltage	T_A = +25°C 0 ≤ T_A ≤ +70°C	−1.5 −1.6		−10 −10	V
I_Q	Quiescent Current	{R_L = ∞} {−1.4V ≤ V_{OUT} ≤ −8.5V}	3.5	10	μA	
V_{SET}	Reference Voltage		−1.2	−1.3	−1.4	V
$\frac{\Delta V_{SET}}{\Delta T}$	Temperature Coefficient	−8.5V < $V_{\overline{IN}}$ < −9V		±200		ppm
$\frac{\Delta V_{SET}}{V_{SET}\Delta V_{IN}}$	Line Regulation	−2V < $V_{\overline{IN}}$ < −9V		0.03		%/V
I_{SET}	V_{SET} Input Current			±0.01	10	nA
I_{SHDN}	Shutdown Input Current			±0.01	10	nA
V_{SHDN}	Shutdown Input Voltage	V_{SHDN}HI: Both V_{OUT} Disabled V_{SHDN}LO: Both V_{OUT} Enabled	−0.3		−1.4	V
I_{SENSE}	Sense Pin Input Current			0.01	10	nA
V_{CL}	Sense Pin Input Threshold Voltage	V_{CL} = V_{OUT2} − V_{SENSE} (Current-Limit Threshold)		−0.35		V
R_{SAT}	Input-Output Saturation Resistance (Note 3)	$V_{\overline{IN}}$ = 2V $V_{\overline{IN}}$ = 9V		150 40		Ω
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	ΔI_{OUT1} = 100μA @ ΔI_{OUT} = −5V		2		Ω
I_{OUT}	Output Current V_{OUT1} or V_{OUT2}	$V_{\overline{IN}}$ = 3V V_{OUT} = V_{SET} $V_{\overline{IN}}$ = 9V V_{OUT} = −5V		−2 −20		mA
$I_{L(min)}$	Minimum Load Current (Includes V_{SET} Divider)				1	μA

NOTES: 1. Connecting any terminal to voltages greater than (GND +0.3V) or less than ($V_{\overline{IN}}$ −0.3V) may cause destructive device latchup. It is recommended that no inputs from sources operating on external power supplies be applied prior to ICL7664B power-up.
2. Derate linearly above 50°C at 5mW/°C for minidip and 7.5mW/°C for TO-99 can.
3. This parameter refers to the saturation resistance of the MOS pass transistor. The minimum input-output voltage differential can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7665
Micropower Under/Over Voltage Detector

GENERAL DESCRIPTION

The ICL7665 contains two individually programmable voltage detectors on a single chip. Requiring only 3μA typical for operation, the device is intended for battery-operated systems and instruments which require high or low voltage warnings, settable trip points, or fault monitoring and correction. Typical applications are battery-backup computer memories, battery-operated medical devices, radiation dosimeters, pocket pagers, portable calibrators, test instruments, and charging systems.

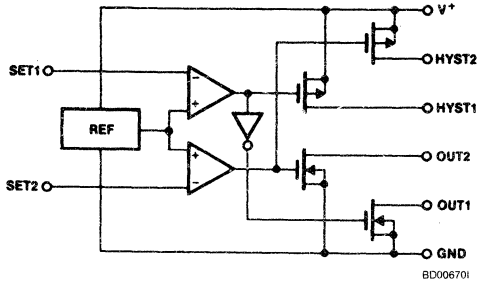
FEATURES

- **Exceptionally Low Supply Current (< 3μA Typ)**
- **Individually Programmable Upper and Lower Trip Voltages and Hysteresis Levels**
- **Accurate On-Chip Bandgap Reference**
- **Up to 20mA Output Current Sinking Ability**
- **Wide Supply Voltage Range**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7665CPA	0°C to +70°C	8 Lead MiniDIP
ICL7665CTV	0°C to +70°C	8 Lead TO-99
ICL7665/D	—	DICE
ICL7665CBA	0°C to 70°C	8 Lead SOIC
ICL7665CJA	0°C to 70°C	8 Lead CERDIP

**Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.



Conditions*

V_{SET1} > 1.3V, OUT1 switch ON	HYST1 switch ON
V_{SET1} < 1.3V, OUT1 switch OFF	HYST1 switch OFF
V_{SET2} > 1.3V, OUT2 switch OFF	HYST2 switch ON
V_{SET2} < 1.3V, OUT2 switch ON	HYST2 switch OFF

*See Operating Characteristics for exact thresholds.

Figure 1: Functional Diagram

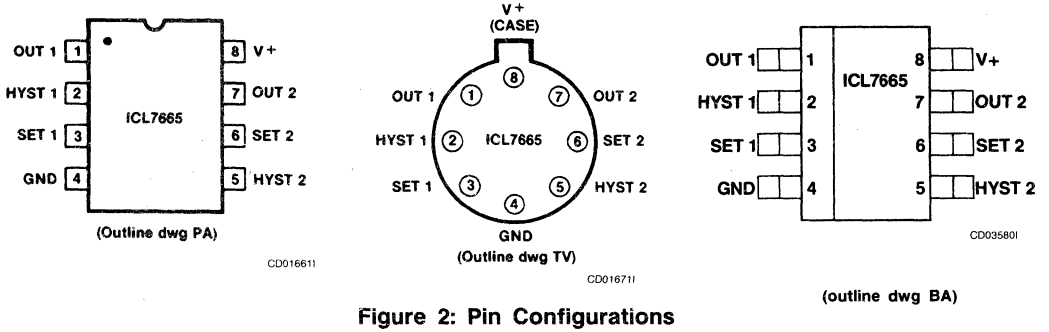


Figure 2: Pin Configurations

302067-002

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7665

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... −0.3V to +18V
Output Voltages OUT1 and OUT2 (with respect to GND) (Note 2) ..... −0.3V to +18V
Output Voltages HYST1 and HYST2 (with respect to V^+) (Note 2) ..... +0.3V to −18V
Input Voltages SET1 and SET2 (Note 2) ..... (GND − 0.3V) to (V^+ + 0.3V)
Maximum Sink Output Current OUT1 and OUT2 ... 25mA
Maximum Source Output Current HYST1 and HYST2 ..... −25mA
Power Dissipation (Note 1) 200mW
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

DC OPERATING CHARACTERISTICS (V^+ = 5V, T_A = +25°C, unless otherwise specified. See Test Circuit Fig. 4)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V^+	Operating Supply Voltage	T_A = +25°C 0°C ≤ T_A ≤ +70°C	1.6 1.8		16 16	V
I^+	Supply Current	GND ≤ V_{SET1}, V_{SET2} ≤ V^+ All Outputs Open Circuit V^+ = 2V V^+ = 9V V^+ = 15V		 2.5 2.6 2.9	 10 10 15	µA
V_{SET1} V_{SET2}	Input Trip Voltage		1.15 1.2	1.3 1.3	1.45 1.4	V
$\frac{\Delta V_{SET}}{\Delta T}$	Temperature Coefficient of V_{SET}			±200		ppm/°C
$\frac{\Delta V_{SET}}{\Delta V_S}$	Supply Voltage Sensitivity of V_{SET1}, V_{SET2}	R_{OUT1}, R_{OUT2}, R_{HYST1}, R_{HYST2} = 1MΩ		0.004		%/V
I_{OLK} I_{HLK}	Output Leakage Currents on OUT and HYST	V_{SET} = 0V or V_{SET} ≥ 2V		10 −10	200 −100	nA
I_{OLK} I_{HLK}		V^+ = 9V, T_A = 70°C V^+ = 9V, T_A = 70°C			2000 −500	
V_{OUT1} V_{OUT1} V_{OUT1}	Output Saturation Voltages	V^+ = 2V, V_{SET1} = 2V, I_{OUT1} = 2mA V^+ = 5V, V_{SET1} = 2V, I_{OUT1} = 2mA V^+ = 9V, V_{SET1} = 2V, I_{OUT1} = 2mA		0.2 0.1 0.06	0.5 0.3 0.2	V
V_{HYST1} V_{HYST1} V_{HYST1}		V^+ = 2V, V_{SET1} = 2V, I_{HYST1} = −0.5mA V^+ = 5V, V_{SET1} = 2V, I_{HYST1} = −0.5mA V^+ = 9V, V_{SET1} = 2V, I_{HYST1} = −0.5mA		−0.15 −0.05 −0.02	−0.3 −0.15 −0.10	
V_{OUT2} V_{OUT2} V_{OUT2}		V^+ = 2V, V_{SET2} = 0V, I_{OUT2} = 2mA V^+ = 5V, V_{SET2} = 0V, I_{OUT2} = 2mA V^+ = 9V, V_{SET2} = 0V, I_{OUT2} = 2mA		0.2 0.15 0.11	0.5 0.3 0.25	
V_{HYST2} V_{HYST2} V_{HYST2}		V^+ = 2V, V_{SET2} = 2V, I_{HYST2} = −0.2mA V^+ = 5V, V_{SET2} = 2V, I_{HYST2} = −0.5mA V^+ = 9V, V_{SET2} = 2V, I_{HYST2} = −0.5mA		−0.25 −0.43 0.35	−0.8 −1.0 −1.0	
I_{SET}	V_{SET} Input Leakage Current	GND ≤ V_{SET} ≤ V^+		0.01	10	nA
ΔV_{SET}	ΔV_{SET} Input for Complete Output Change	R_{OUT} = 4.7kΩ, R_{HYST} = 20kΩ V_{OUT}LO = 1% V^+, V_{OUT}HI = 99% V^+		1		mV
V_{SET1}-V_{SET2}	Difference in Trip Voltages	R_{OUT}, R_{HYST} = 1MΩ		±5	±50	
	Output/Hysteresis Difference	R_{OUT}, R_{HYST} = 1MΩ		±1		

NOTES: 1. Derate above ±25°C ambient temperature at 4mW/°C.
2. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than (V^+ + 0.3V) or less than (GND − 0.3V) may cause destructive device latchup. For these reason, it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICL7665 be turned on first. If this is not possible, currents into inputs and/or outputs must be limited to ±0.5mA and voltages must not exceed those defined above.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7665

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
t_{SO1d} t_{SH1d} t_{SO2d} t_{SH2d}	Output Delay Time Input Going HI	V_{SET} Switched from 1.0V to 1.6V R_{OUT} = 4.7kΩ, C_L = 12pF R_{HYST} = 20kΩ, C_L = 12pF		70 80 120 230		µs
$t_{\overline{SO}1d}$ $t_{\overline{SH}2d}$ $t_{\overline{SO}2d}$ $t_{\overline{SH}2d}$	Output Delay Time Input Going LO	V_{SET} Switched from 1.6V to 1.0V R_{OUT} = 4.7kΩ, C_L = 12pF R_{HYST} = 20kΩ, C_L = 12pF		1040 610 70 30		µs
t_{O1r} t_{O2r} t_{H1r} t_{H2r}	Output Rise Times	V_{SET} Switched between 1.0V and 1.6V R_{OUT} = 4.7kΩ, C_L = 12pF R_{HYST} = 20kΩ, C_L = 12pF		120 80 330 25		µs
t_{O1f} t_{O2f} t_{H1f} t_{H2f}	Output Fall Times	V_{SET} Switched between 1.0V and 1.6V R_{OUT} = 4.7kΩ, C_L = 12pF R_{HYST} = 20kΩ, C_L = 12pF		30 60 180 30		µs

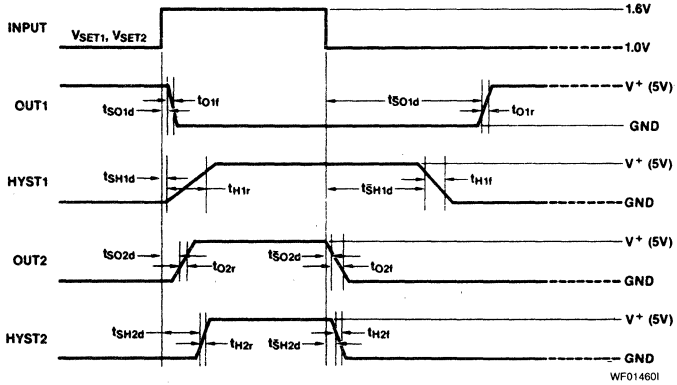


Figure 3: Switching Waveforms

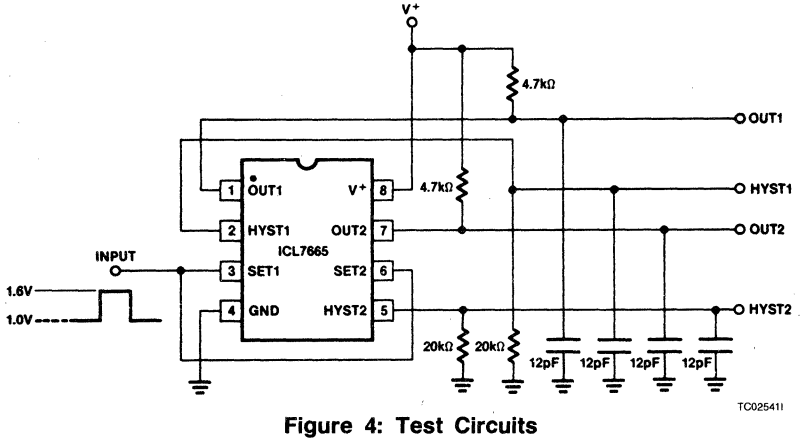


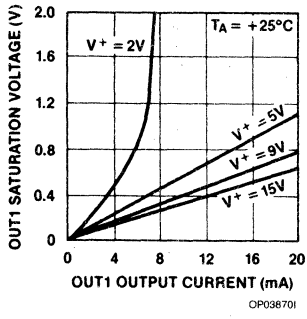
Figure 4: Test Circuits

Note: All typical values have been guaranteed by characterization and are not tested.

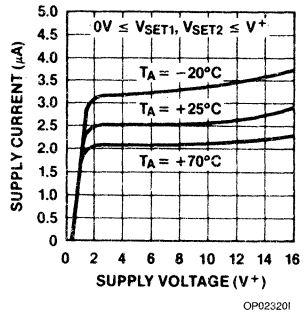
ICL7665

TYPICAL PERFORMANCE CHARACTERISTICS

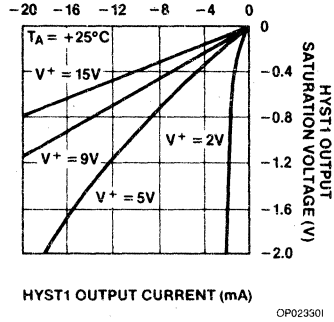
OUT1 SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



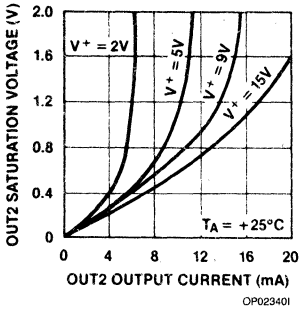
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



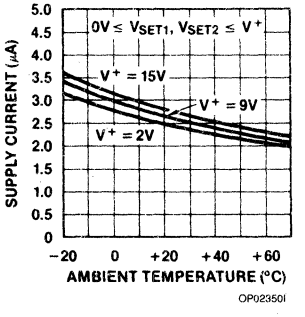
HYST1 OUTPUT SATURATION VOLTAGE VS HYST1 OUTPUT CURRENT



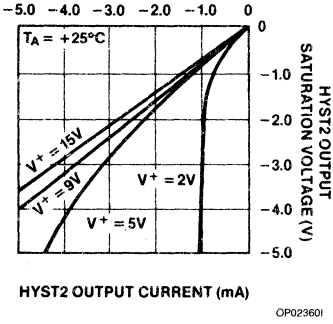
OUT2 SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



HYST2 OUTPUT SATURATION VOLTAGE VS HYST2 OUTPUT CURRENT



DETAILED DESCRIPTION

As shown in the Functional Diagram, the ICL7665 consists of two comparators which compare input voltages on the SET1 and SET2 terminals to an internal 1.3V band-gap reference. The outputs from the two comparators drive open-drain N-channel transistors for OUT1 and OUT2, and open-drain P-channel transistors for HYST1 and HYST2 outputs. Each section, the Under-Voltage Detector and the Over-Voltage Detector, is independent of the other, although both use the internal 1.3V reference. The offset voltages of the two comparators will normally be unequal, so V_{SET1} will generally not quite equal V_{SET2}.

The input impedances of the SET1 and SET2 pins are extremely high, and for most practical applications can be ignored. The four outputs are open-drain MOS transistors, and when ON behave as low resistance switches to their respective supply rails. This minimizes errors in setting-up the hysteresis, and maximizes the output flexibility. The operating currents of the bandgap reference and the comparators are around 100nA each.

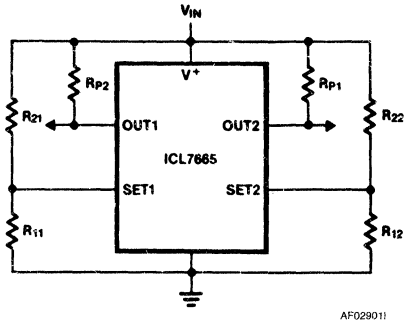
PRECAUTIONS

Junction-isolated CMOS devices like the ICL7665 have an inherent SCR or 4-layer PNPN structure distributed throughout the die. Under certain circumstances, this can be triggered into a potentially destructive high-current mode. This latchup can be triggered by forward-biasing an input or output with respect to the power supply, or by applying excessive supply voltages. In very-low current analog circuits, such as the ICL7665, this SCR can also be triggered by applying the input power supply extremely rapidly ("instantaneously"), e.g. through a low impedance battery and an ON/OFF switch with short lead lengths. The rate-of-rise of the supply voltage can exceed 100V/µs in such a circuit. A low-impedance capacitor (e.g. 0.05µF disc ceramic) between the V^+ and GrouND pins of the ICL7665 can be used to reduce the rate-of-rise of the supply voltage in battery applications. In line-operated systems, the rate-of-rise of the supply is limited by other considerations, and is normally not a problem.

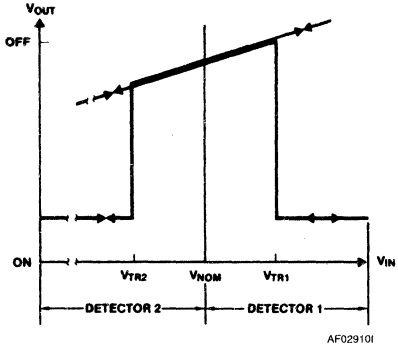
If the SET voltages must be applied before the supply voltage V^+, the input current should be limited to less than 0.5mA by appropriate external resistors, usually required for voltage setting anyway. A similar precaution should be taken with the outputs if it is likely that they will be driven by other circuits to levels outside the supplies at any time. See M011 for some other protection ideas.

Note: All typical values have been guaranteed by characterization and are not tested.

APPLICATIONS



(a) Circuit Configuration



(b) Transfer Characteristics

Figure 5: Simple Threshold Detector

Figure 5 shows the simplest connection of the ICL7665 for threshold detection. From the graph (b), it can be seen that at low input voltages OUT1 is OFF, or high, while OUT2 is ON, or low. As the input rises (e.g. at power-on) toward V_{NOM} (usually the eventual operating voltage), OUT2 goes high on reaching V_{TR2}. If the voltage rises above V_{NOM} as much as V_{TR1}, OUT1 goes low. The equations giving V_{SET1} and V_{SET2} are, from Figure 1(a):

$$V_{SET1} = V_{IN}\frac{R_{11}}{(R_{11} + R_{21})}; \quad V_{SET2} = V_{IN}\frac{R_{12}}{(R_{12} + R_{22})}$$

Since the voltage to trip each comparator is nominally 1.3V, the value of V_{IN} for each trip point can be found from

$$V_{TR1} = V_{SET1}\frac{(R_{11} + R_{21})}{R_{11}} = 1.3\,\frac{(R_{11} + R_{21})}{R_{11}} \text{ for detector 1}$$

and

$$V_{TR2} = V_{SET2}\,\frac{(R_{12} + R_{22})}{R_{12}} = 1.3\,\frac{(R_{12} + R_{22})}{R_{12}} \text{ for detector 2.}$$

Either detector may be used alone, as well as both together, in any of the circuits shown here.

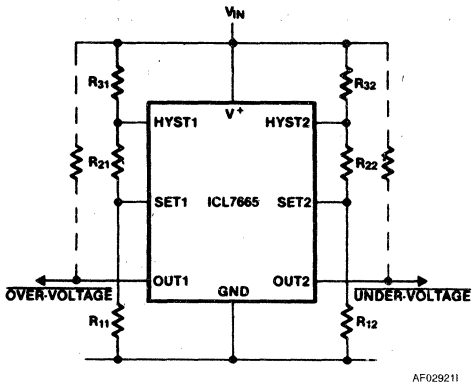
When V_{IN} is very close to one of the trip voltages, normal variations and noise may cause it to wander back and forth across this level, leading to erratic output ON and OFF conditions. The addition of hysteresis, making the trip points slightly different for rising and falling inputs, will avoid this condition.

Figure 6(a) shows how to set up such hysteresis, while Figure 6(b) shows how the hysteresis around each trip point produces switching action at different points depending on whether V_{IN} is rising or falling (the arrows indicate direction of change). The HYST outputs are basically switches which short out R_{31} or R_{32} when V_{IN} is above the respective trip point. Thus if the input voltage rises from a low value, the trip point will be controlled by R_{1n}, R_{2n} and R_{3n}, until the trip point is reached. As this value is passed, the detector changes state, R_{3n} is shorted out, and the trip point becomes controlled by only R_{1n} and R_{2n}, a lower value. The input will then have to fall to this new point to restore the initial comparator state, but as soon as this occurs, the trip point will be raised again.

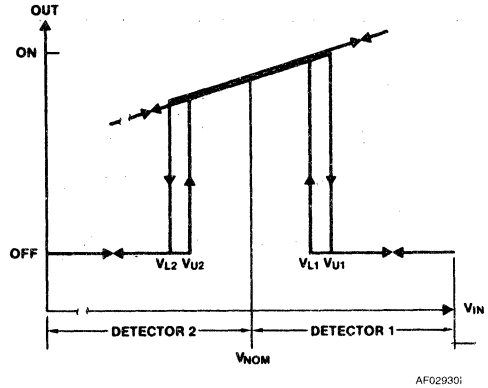
An alternative circuit for obtaining hysteresis is shown in Figure 7. In this configuration, the HYST pins put the extra resistor in parallel with the upper setting resistor. The values of the resistors differ, but the action is essentially the same. The governing equations are given in Table 1. These ignore the effects of the resistance of the HYST outputs, but these can normally be neglected if the resistor values are above about 100kΩ.

5

Note: All typical values have been guaranteed by characterization and are not tested.



(a) Circuit Configuration



(b) Transfer Characteristics

Figure 6: Threshold Detector with Hysteresis

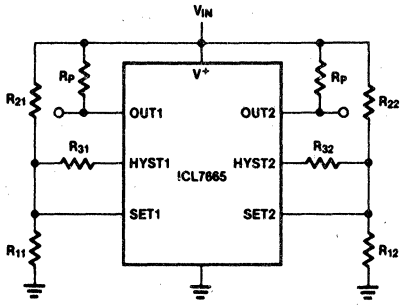


Figure 7: An Alternative Hysteresis Circuit

Table 1. Set-Point Equations

a) NO HYSTERESIS

$$\text{Over-Voltage } V_{TRIP} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$$

$$\text{Under-Voltage } V_{TRIP} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$$

b) HYSTERESIS PER FIGURE 6A

$$\text{Over-Voltage } V_{TRIP} \quad V_{U1} = \frac{R_{11} + R_{21} + R_{31}}{R_{11}} \times V_{SET1}$$

$$V_{L1} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$$

$$\text{Under-Voltage } V_{TRIP} \quad V_{U2} = \frac{R_{12} + R_{22} + R_{32}}{R_{12}} \times V_{SET2}$$

$$V_{L2} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$$

c) HYSTERESIS PER FIGURE 7

$$\text{Over-Voltage } V_{TRIP} \quad V_{U1} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$$

$$V_{L1} = \frac{R_{11} + \dfrac{R_{21}\,R_{31}}{R_{21} + R_{31}}}{R_{11}} \times V_{SET1}$$

$$V_{U2} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$$

$$\text{Under-Voltage } V_{TRIP}$$

$$V_{L2} = \frac{R_{12} + \dfrac{R_{22}\,R_{32}}{R_{22} + R_{32}}}{R_{12}} \times V_{SET2}$$

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7665

INTERSIL

ICL7665B ADDENDUM TO THE ICL7665 DATASHEET

This Addendum to the standard ICL7665B datasheet describes changes and/or modifications to the DC Operating characteristics applicable to the ICL7665B device. The following table indicates those limits to which the ICL7665B is tested and/or guaranteed operational.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7665BCPA	0 to +70°C	8 Lead MiniDIP
ICL7665BCTV	0 to +70°C	8 Lead TO-99
ICL7665B/D	—	DICE Only
ICL7665BCJA	0 to +70°C	8-Lead Cerdip
ICL7665BCBA	0 to +70°C	8-Lead S.O.I.C.

ABSOLUTE MAXIMUM RATINGS, ICL7665B

Supply Voltage ..... −0.3V to +12V
Output Voltages OUT1 and OUT2 (with respect to GND) (Note 2) ..... −0.3V to +12V
Output Voltages HYST1 and HYST2 (with respect to V^+) (Note 2) ..... +0.3V to −12V
Input Voltages SET1 and SET2 (Note 2) ..... (GND −0.3V) to (V^+ +0.3V)
Maximum Sink Output Current OUT1 and OUT2 ... 25mA
Maximum Source Output Current HYST1 and HYST2 ..... −25mA
Power Dissipation (Note 1) 200mW
Operating Temperature Range ..... 0 to +70°C
Storage Temperature Range ..... −55°C to +125°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC OPERATING CHARACTERISTICS $V^+ = 5V$, $T_A = +25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
V^+	Operating Supply Voltage	$T_A = +25°C$ $0 \le T_A \le +70°C$	1.6 1.8		10 10	V
I^+	Supply Current	$GND \le V_{SET1}, V_{SET2} \le V^+$ All Outputs Open Circuit $V^+ = 2V$ $V^+ = 9V$		 2.5 2.6	 10 10	µA
V_{SET1} V_{SET2}	Input Trip Voltage		1.15 1.2	1.3 1.3	1.45 1.4	V
$\frac{\Delta V_{SET}}{\Delta T}$	Temperature Coefficient of V_{SET}			±200		ppm/°C
$\frac{\Delta V_{SET}}{\Delta V_S}$	Supply Voltage Sensitivity of V_{SET1}, V_{SET2}	R_{OUT1}, R_{OUT2}, R_{HYST1}, $R_{HYST2} = 1M\Omega$		0.004		%/V
I_{OLK} I_{HLK}	Output Leakage Currents on OUT and HYST	$V_{SET} = 0V$ or $V_{SET} \ge 2V$		10 −10	200 −100	nA
I_{OLK} I_{HLK}		$V^+ = 9V$, $T_A = 70°C$ $V^+ = 9V$, $T_A = 70°C$			2000 −500	
V_{OUT1} V_{OUT1} V_{OUT1}	Output Saturation Voltages	$V^+ = 2V$, $V_{SET1} = 2V$, $I_{OUT1} = 2mA$ $V^+ = 5V$, $V_{SET1} = 2V$, $I_{OUT1} = 2mA$ $V^+ = 9V$, $V_{SET1} = 2V$, $I_{OUT1} = 2mA$		0.2 0.1 0.06	0.5 0.3 0.25	V
V_{HYST1} V_{HYST1} V_{HYST1}		$V^+ = 2V$, $V_{SET1} = 2V$, $I_{HYST1} = -0.5mA$ $V^+ = 5V$, $V_{SET1} = 2V$, $I_{HYST1} = -0.5mA$ $V^+ = 9V$, $V_{SET1} = 2V$, $I_{HYST1} = -0.5mA$		−0.15 −0.05 −0.02	−0.3 −0.15 0.15	
V_{OUT2} V_{OUT2} V_{OUT2}		$V^+ = 2V$, $V_{SET2} = 0V$, $I_{OUT2} = 2mA$ $V^+ = 5V$, $V_{SET2} = 0V$, $I_{OUT2} = 2mA$ $V^+ = 9V$, $V_{SET2} = 0V$, $I_{OUT2} = 2mA$		0.2 0.15 0.11	0.5 0.3 0.3	
V_{HYST2} V_{HYST2} V_{HYST2}		$V^+ = 2V$, $V_{SET2} = 2V$, $I_{HYST2} = -0.2mA$ $V^+ = 5V$, $V_{SET2} = 2V$, $I_{HYST2} = -0.5mA$ $V^+ = 9V$, $V_{SET2} = 2V$, $I_{HYST2} = -0.5mA$		−0.25 −0.43 0.35	−0.8 −1 −1	

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Note: All typical values have been guaranteed by characterization and are not tested.

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DC OPERATING CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
I_{SET}	V_{SET} Input Leakage Current	$GND \le V_{SET} \le V^+$		0.01	10	nA
ΔV_{SET}	ΔV_{SET} Input for Complete Output Change	$R_{OUT} = 4.7k\Omega$, $R_{HYST} = 20k\Omega$ $V_{OUT}LO = 1\%\ V^+$, $V_{OUT}HI = 99\%\ V^+$		1		mV
V_{SET1}-V_{SET2}	Difference in Trip Voltages	R_{OUT}, $R_{HYST} = 1M\Omega$		±5	±50	
	Output/Hysteresis Difference	R_{OUT}, $R_{HYST} = 1M\Omega$		±1		

NOTES: 1. Derate above ±25°C ambient temperature at 4mW/°C.
2. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than (V^+ + 0.3V) or less than (GND – 0.3V) may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICL7665B be turned on first. If this is not possible, currents into inputs and/or outputs must be limited to ±0.5mA and voltages must not exceed those defined above.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7667
Dual Power MOSFET Driver

INTERSIL

GENERAL DESCRIPTION

The ICL7667 is a dual monolithic high-speed driver designed to convert TTL level signals into high current outputs at voltages up to 15V. Its high speed and 1.5A peak current output enable it to drive large capacitive loads with high slew rates and low propagation delays. With an output voltage swing only millivolts less than the supply voltage and a maximum supply voltage of 15V, the ICL7667 is well suited for driving power MOSFETs in high frequency switched-mode power converters. The ICL7667's high current outputs (1.5A peak) minimize power losses in the power MOSFETs by rapidly charging and discharging the gate capacitance. The ICL7667's inputs are TTL compatible and can be directly driven by common pulse-width modulation control IC's.

FEATURES

- **1.5A Peak Output Current**
- **Fast Rise and Fall Times**
  — 40ns With 1000pF Load
- **Wide Supply Voltage Range**
  — V_{CC} = 4.5 to 15V
- **Low Power Consumption**
  — 4mW With Inputs Low
  — 120mW With Inputs High
- **TTL/CMOS Input Compatible Power Driver**
  — R_{OUT} = 6Ω
- **Direct Interface With Common PWM Control IC's**
- **Pin Equivalent to DS0026/DS0056; TSC426**

TYPICAL APPLICATIONS

- **Switching Power Supplies**
- **DC/DC Converters**
- **Motor Controllers**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7667MTV ICL7667MJA	−55°C to +125°C	TO-99 Can 8-Pin Cerdip
ICL7667CPA ICL7667CJA ICL7667CTV	0°C to +70°C	8-Pin Plastic 8-Pin Cerdip TO-99 Can
ICL7667/D	—	DICE**

**Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.

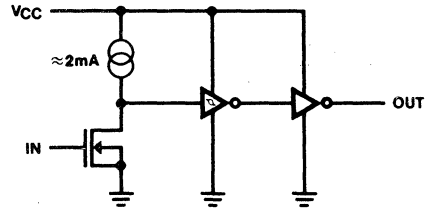
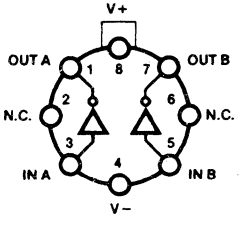


Figure 1: Functional Diagram



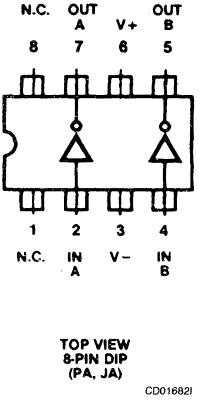


Figure 2: Pin Configurations

302068-002

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7667

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 15V
Input Voltage ..... 15V to (V^- −0.3V)
Peak Output Current 1.5A
Package Dissipation, T_A = 25°C 500mW

Linear Derating Factors

TO-99	Plastic	Cerdip
6.7mW/°C	5.6mW/°C	6.7mW/°C
above 50°C	above 36°C	above50°C

Storage Temperature ..... −65°C to +150°C
Operating Temperature Range
ICL7667C ..... 0°C to +70°C
ICL7667M ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (STATIC)

Test Conditions: V_{CC} = 4.5 to 15V, T_A = +25°C unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{IH}	Logic 1 Input Voltage		2.4			V
V_{IL}	Logic 0 Input Voltage				0.8	V
I_{IN}	Input Current	$0 < V_{IN} < V_{CC}$	−1	0	1	μA
V_{OH}	Output Voltage High	No Load	V_{CC} −0.05	V_{CC}		V
V_{OL}	Output Voltage Low	No Load		0	0.05	V
R_{OUT}	Output Resistance	$V_{IN} = V_{IL}$ I_{OUT} = −10mA V_{CC} = 15V		6	20	Ω
R_{OUT}	Output Resistance	$V_{IN} = V_{IH}$ I_{OUT} = 10mA V_{CC} = 15V		6	20	Ω
I_{CC}	Power Supply Current	V_{IN} = 3V (both inputs)		4	6	mA
I_{CC}	Power Supply Current	V_{IN} = 0V (both inputs)		150	400	μA

ELECTRICAL CHARACTERISTICS (DYNAMIC)

Test Conditions: V_{CC} = 15V, T_A = +25°C, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
T_{D2}	Delay Time	Figure 3		50	75	ns
T_R	Rise Time	Figure 3		35	50	ns
T_F	Fall Time	Figure 3		40	55	ns
T_{D1}	Delay Time	Figure 3		20	35	ns

Note: All typical values have been guaranteed by characterization and are not tested.

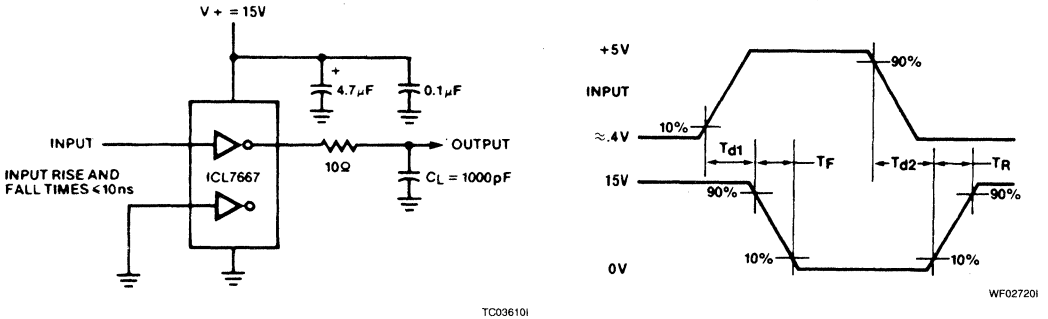
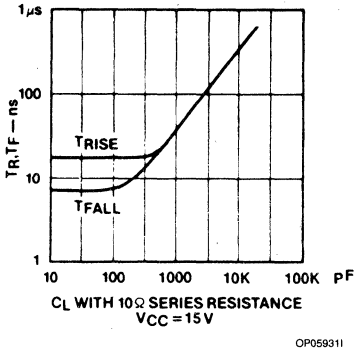


Figure 3: Test Circuit

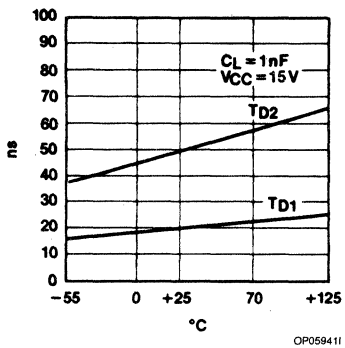
TYPICAL PERFORMANCE CHARACTERISTICS

NOTE: With the 10Ω resistor shorted (or removed), the rise, fall and delay times will be decreased by typically 10%.

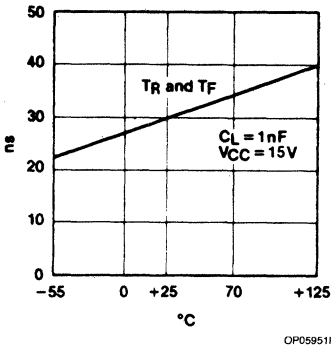
Rise and Fall Times vs C_L



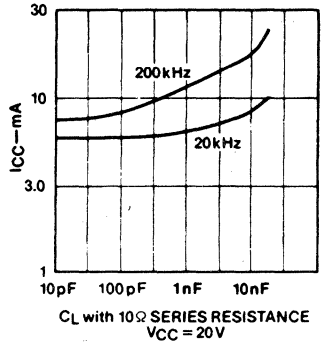
T_{D1}, T_{D2} vs Temperature



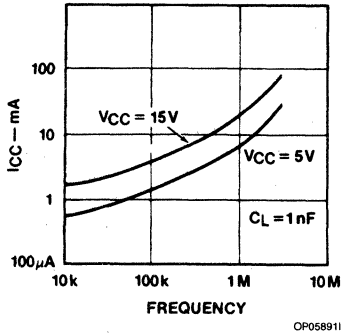
T_R, T_F vs Temperature



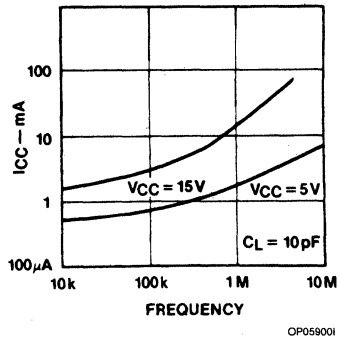
I_{CC} vs C_L



I_{CC} vs Frequency



No Load I_{CC} vs Frequency

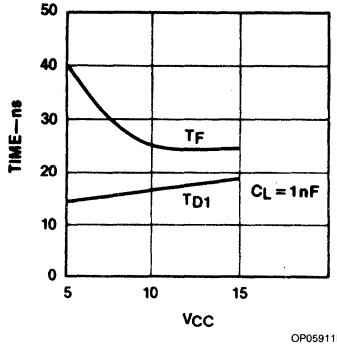


Note: All typical values have been guaranteed by characterization and are not tested.

ICL7667

TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

Delay and Fall Times vs V_{CC}



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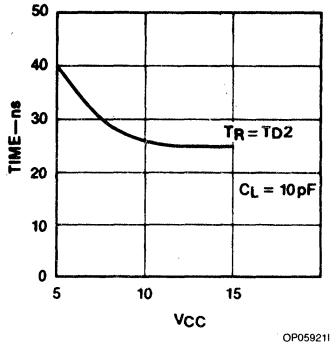
Rise Time vs V_{CC}



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DETAILED DESCRIPTION

The ICL7667 is a dual high-power CMOS inverter whose inputs respond to TTL levels while the outputs can swing as high as 15V. Its 1.5A peak output current enables it to rapidly charge and discharge the gate capacitance of power MOSFETs, minimizing the switching losses in switchmode power supplies. Since the output stage is CMOS, the output will swing to within millivolts of both ground and V_{CC} without any external parts or extra power supplies as required by the DS0026/56 family. Although most specifications are at V_{CC} = 15V, the propagation delays and specifications are almost independent of V_{CC}.

In addition to power MOS drivers, the ICL7667 is well suited for other applications such as bus, control signal, and clock drivers on large memory of microprocessor boards, where the load capacitance is large and low propagation delays are required. Other potential applications include peripheral power drivers and charge-pump voltage inverters.

INPUT STAGE

The input stage is a large N-channel FET with a P-channel constant-current source. This circuit has a threshold of about 1.5V, relatively independent of the V_{CC} voltage. This means that the inputs will be directly compatible with TTL over the entire 4.5–15V V_{CC} range. Being CMOS, the inputs draw less than 1μA of current over the entire input voltage range of ground to V_{CC}. The quiescent current or no load supply current of the ICL7667 is affected by the input voltage, going to nearly zero when the inputs are at the 0 logic level and rising to 6mA maximum when both inputs are the 1 logic level. A small amount of hysteresis, about 50–100mV at the input, is generated by positive feedback around the second stage.

OUTPUT STAGE

The ICL7667 output is a high-power CMOS inverter, swinging between ground and V_{CC}. At V_{CC} = 15V, the output impedance of the inverter is typically 6Ω, with a peak current output of typically 1.5A. It is this high peak current capability that enables the ICL7667 to drive a 1000pF load with a rise time of only 40ns. Because the output stage impedance is very low, up to 300mA will flow through the series N- and P-channel output devices (from V_{CC} to ground) during output transitions. This crossover current is responsible for a significant portion of the internal power dissipation of the ICL7667 at high frequencies. It can be minimized by keeping the rise and fall times of the input to the ICL7667 below 1μs.

APPLICATION NOTES

Although the ICL7667 is simply a dual level-shifting inverter, there are several areas to which careful attention must be paid.

GROUNDING

Since the input and the high current output current paths both include the ground pin, it is very important to minimize any common impedance in the ground return. Since the ICL7667 is an inverter, any common impedance will generate negative feedback, and will degrade the delay, rise and fall times. Use a ground plane if possible, or use separate ground returns for the input and output circuits. To minimize any common inductance in the ground return, separate the input and output circuit ground returns as close to the ICL7667 as is possible.

BYPASSING

The rapid charging and discharging of the load capacitance requires very high current spikes from the power supplies. A parallel combination of capacitors that has a low impedance over a wide frequency range should be used. A 4.7μF tantalum capacitor in parallel with a low inductance 0.1μF capacitor is usually sufficient bypassing.

OUTPUT DAMPING

Ringing is a common problem in any circuit with very fast rise or fall times. Such ringing will be aggravated by long inductive lines with capacitive loads. Techniques to reduce ringing include:

1) Reduce inductance by making printed circuit board traces as short as possible.
2) Reduce inductance by using a ground plane or by closely coupling the output lines to their return paths.
3) Use a 10 to 30Ω resistor in series with the output of the ICL7667. Although this reduces ringing, it will also slightly increase the rise and fall times.
4) Use good bypassing techniques to prevent ringing caused by supply voltage ringing.

Note: All typical values have been guaranteed by characterization and are not tested.

POWER DISSIPATION

The power dissipation of the ICL7667 has three main components:

1) Input inverter current loss
2) Output stage crossover current loss
3) Output stage I^2R power loss

The sum of the above must stay within the specified limits for reliable operation.

As noted above, the input inverter current is input voltage dependent, with an I_{CC} of 0.2mA maximum with a logic 0 input and 6mA maximum with a logic 1 input.

The output stage crowbar current is the current that flows through the series N- and P-channel devices that form the output. This current, about 300mA, occurs only during output transitions. **Caution:** The inputs should never be allowed to remain between V_{IL} and V_{IH} since this could leave the output stage in a high current mode, rapidly leading to destruction of the device. If only one of the drivers is being used, be sure to tie the unused input to a ground. **NEVER** leave an input floating. The average supply current drawn by the output stage is frequency dependent, as can be seen in I_{CC} vs. Frequency graph in the Typical Characteristics Graphs.

The output stage I^2R power dissipation is nothing more than the product of the output current times the voltage drop across the output device. In addition to the current drawn by any resistive load, there will be an output current due to the charging and discharging of the load capacitance. In most high frequency circuits the current used to charge and discharge capacitance dominates, and the power dissipation is approximately

$$P_{AC} = CV_{CC}^2f$$

Where C = Load Capacitance
f = Frequency

In cases where the load is a power MOSFET and the gate drive requirements are described in terms of gate charge, the ICL7667 power dissipation will be

$$P_{AC} = Q_GV_{CC}f$$

Where Q_G = Charge required to switch the gate, in Coulombs.
f = Frequency

POWER MOS DRIVER CIRCUITS

POWER MOS DRIVER REQUIREMENTS

Because it has a very high peak current output, the ICL7667 excels at driving the gate of power MOS devices. The high current output is important since it minimizes the time the power MOS device is in the linear region. Figure 5 is a typical curve of charge vs. gate voltage for a power MOSFET. The flat region is caused by the Miller capacitance, where the drain-to-gate capacitance is multiplied by the voltage gain of the FET. This increase in capacitance occurs while the power MOSFET is in the linear region and is dissipating significant amounts of power. The very high current output of the ICL7667 is able to rapidly overcome this high capacitance and quickly turns the MOSFET fully on or off.

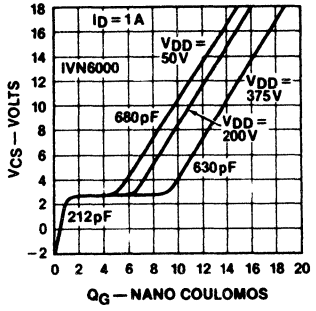

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Figure 5: MOSFET Gate Dynamic Characteristics

DIRECT DRIVE OF MOSFETs

Figure 6 shows interfaces between the ICL7667 and typical switching regulator ICs. Note that unlike the DS0026, the ICL7667 does not need a dropping resistor and speed-up capacitor between it and the regulator IC. The ICL7667, with its high slew rate and high voltage drive can directly drive the gate of the MOSFET. The 1527 IC is the same as the 1525 IC, except that the outputs are inverted. This inversion is needed since ICL7667 is an inverting buffer.

TRANSFORMER COUPLED DRIVE OF MOSFETs

Transformers are often used for isolation between the logic and control section and the power section of a switching regulator. The high output drive capability of the ICL7667 enables it to directly drive such transformers. Figure 7 shows a typical transformer coupled drive circuit. PWM ICs with either active high or active low outputs can be used in this circuit, since any inversion required can be obtained by reversing the windings on the secondaries.

BUFFERED DRIVERS FOR MULTIPLE MOSFETs

In very high power applications which use a group of MOSFETs in parallel, the input capacitance may be very large and it can be difficult to charge and discharge quickly. Figure 8 shows a circuit which works very well with very large capacitance loads. When the input of the driver is zero, Q1 is held in conduction by the lower half of the ICL7667 and Q2 is clamped off by Q1. When the input goes positive, Q1 is turned off and a current pulse is applied to the gate of Q2 by the upper half of the ICL7667 through the transformer, T1. After about 20ns, T1 saturates and Q2 is held on by its own C_{gs} and the bootstrap circuit of C1, D1 and R1. This bootstrap circuit may not be needed at frequencies greater than 10kHz since the input capacitance of Q2 discharges slowly.

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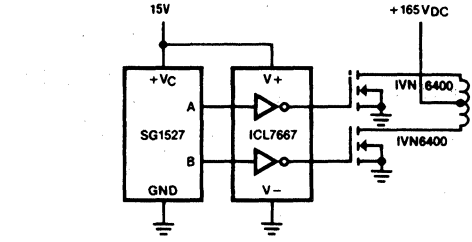
Note: All typical values have been guaranteed by characterization and are not tested.



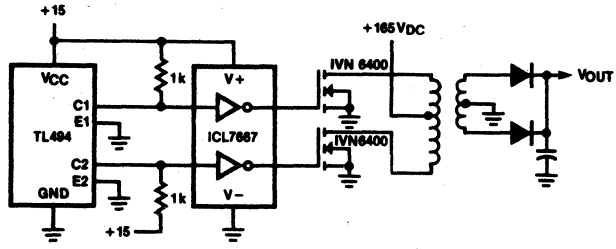


Figure 6: Direct Drive of MOSFET Gates

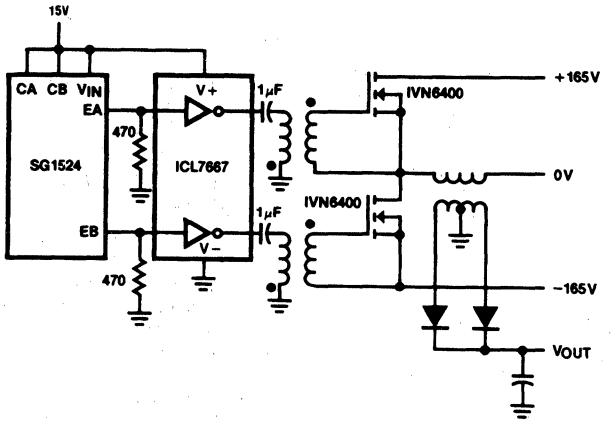
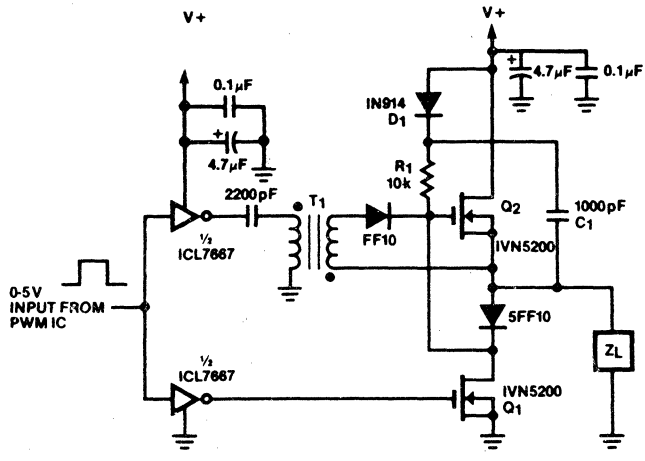


Figure 7: Transformer Coupled Drive Circuit

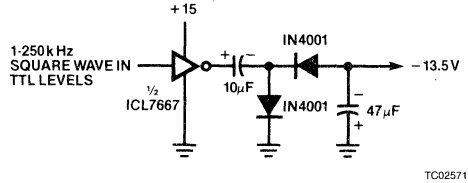
Note: All typical values have been guaranteed by characterization and are not tested.



T_1 — IS THREE TURNS 30 BIFILAR ON A FERRITE BEAD.

DS01821I

Figure 8: Very High-Speed Driver



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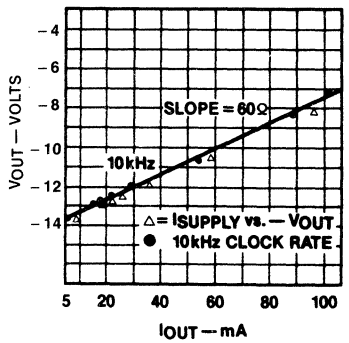


OP02570I

Figure 9: Voltage Inverter

5

Note: All typical values have been guaranteed by characterization and are not tested.

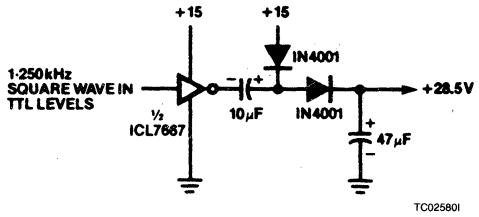


Figure 10: Voltage Doubler

OTHER APPLICATIONS

RELAY AND LAMP DRIVERS

The ICL7667 is suitable for converting low power TTL or CMOS signals into high current, high voltage outputs for relays, lamps and other loads. Unlike many other level translator/driver ICs, the ICL7667 will both source and sink current. The continuous output current is limited to 200mA by the I^2R power dissipation in the output FETs.

CHARGE PUMP OR VOLTAGE INVERTERS AND DOUBLERS

The low output impedance and wide V_{CC} range of the ICL7667 make it well suited for charge pump circuits. Figure 9 shows a typical charge pump voltage inverter circuit and a typical performance curve. A common use of this circuit is to provide a low current negative supply for analog circuitry or RS232 drivers. With an input voltage of +15V, this circuit will deliver 20mA at −12.6V. By increasing the size of the capacitors, the current capability can be increased and the voltage loss decreased. The practical range of the input frequency is 500Hz to 250kHz. As the frequency goes up, the charge pump capacitors can be made smaller, but the internal losses in the ICL7667 will rise, reducing the circuit efficiency.

Figure 10, a voltage doubler, is very similar in both circuitry and performance. A potential use of Figure 8 would be to supply the higher voltage needed for EEPROM or EPROM programming.

CLOCK DRIVER

Some microprocessors (such as the 68XX and 65XX families) use a clock signal to control the various LSI peripherals of the family. The ICL7667's combination of low propagation delay, high current drive capability and wide voltage swing make it attractive for this application. Although the ICL7667 is primarily intended for driving power MOSFET gates at 15V, the ICL7667 also works well as a 5V high-speed buffer. Unlike standard 4000 series CMOS, the ICL7667 uses short channel length FETs and the ICL7667 is only slightly slower at 5V than at 15V.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7673
Automatic Battery Back-up Switch

GENERAL DESCRIPTION

The Intersil ICL7673 is a monolithic CMOS battery backup circuit that offers unique performance advantages over conventional means of switching to a backup supply. The ICL7673 is intended as a low-cost solution for the switching of systems between two power supplies; main and battery backup. The main application is keep-alive-battery power switching for use in volatile CMOS RAM memory systems and real time clocks. In many applications this circuit will represent a low insertion voltage loss between the supplies and load. This circuit features low current consumption, wide operating voltage range, and exceptionally low leakage between inputs. Logic outputs are provided that can be used to indicate which supply is connected and can also be used to increase the power switching capability of the circuit by driving external PNP transistors.

The ICL7673 is available in either an 8-pin plastic minidip package, a TO-99 metal can, or as dice.

FEATURES

- **Automatically Connects Output to The Greater Of Either Input Supply Voltage**
- **If Main Power to External Equipment Is Lost, Circuit Will Automatically Connect Battery Backup**
- **Reconnects Main Power When Restored**
- **Logic Indicator Signaling Status Of Main Power**
- **Low Impedance Connection Switches**
- **Low Internal Power Consumption**
- **Wide Supply Range: 2.5 to 15 Volts**
- **Low Leakage Between Inputs**
- **External Transistors May Be Added If Very Large Currents Need to Be Switched**

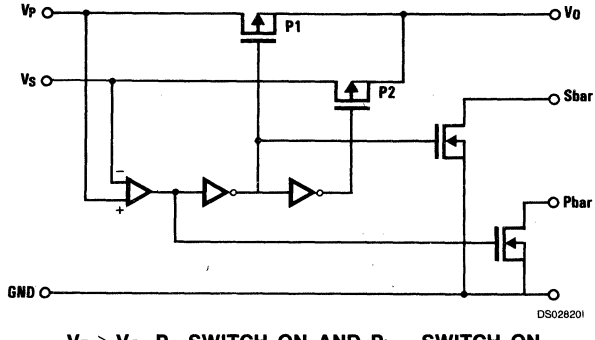
APPLICATIONS

- **On Board Battery Backup for Real-Time Clocks, Timers, or Volatile RAMs**
- **Over/Under Voltage Detector**
- **Peak Voltage Detector**
- **Other Uses:**
  - **Portable Instruments, Portable Telephones, Line Operated Equipment**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7673CPA	0°C to +70°C	8-pin minidip
ICL7673CBA	0°C to +70°C	8-pin SOIC
ICL7673ITV	−25°C to +85°C	8-pin TO-99
ICL7673/D	—	DICE ONLY**

**Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.



$V_P > V_S$, P_1 SWITCH ON AND P_{bar} SWITCH ON
$V_S > V_P$, P_2 SWITCH ON AND S_{bar} SWITCH ON

Figure 1: Functional Diagram

302070-003

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7673

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Input Supply (V_P or V_S) Voltage ..... −0.3 to +18V
Output Voltages P_{bar} and S_{bar} ..... −0.3 to +18V
Peak Current
- Input V_P (@ V_P = 5V) (note 1) 38mA
- Input V_S (@ V_S = 3V) 30mA
- P_{bar} or S_{bar} 150mA

Continuous Current
- Input V_P (@ V_P = 5V) (note 1) 38mA
- Input V_S (@ V_S = 3V) 30mA
- P_{bar} or S_{bar} 50mA

Package Dissipation 300mW

Linear Derating Factors

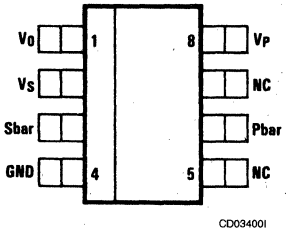
TO-99	PLASTIC
5.7mW/°C	6.1mW/°C
above 50°C	above 36°C

Operating Temperature Range:
- ICL7673CPA/CBA ..... 0°C to +70°C
- ICL7673ITV ..... −25°C to +85°C

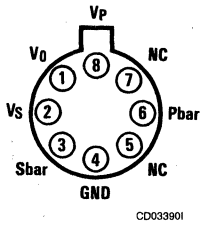
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Note 1. Derate above 25°C by 0.38mA/°C.

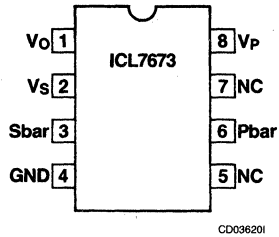
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



(Outline Dwg BA)
8-LEAD SOIC



(Outline Dwg TV)
8-LEAD TO-99



(Outline Dwg PA)
8-LEAD Minidip

Figure 2: Pin Configurations

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_P	INPUT VOLTAGE	V_S = 0 volts I load = 0mA	2.5	–	15	V
V_S		V_P = 0 volts I load = 0mA	2.5	–	15	
I^+	QUIESCENT SUPPLY CURRENT	V_P = 0 volts V_S = 3 volts I load = 0mA	–	1.5	5	μA
$R_{ds(on)P1}$	SWITCH RESISTANCE P1 (NOTE 2)	V_P = 5 volts V_S = 3 volts I load = 15mA	–	8	15	Ω
		@ T_A = 85°C	–	16	–	
		V_P = 9 volts V_S = 3 volts I load = 15mA	–	6	–	Ω
		V_P = 12 volts V_S = 3 volts I load = 15mA	–	5	–	Ω
$T_{C(P1)}$	TEMPERATURE COEFFICIENT OF SWITCH RESISTANCE P1	V_P = 5 volts V_S = 3 volts I load = 15mA	–	2.03	–	%/°C

Note: All typical values have been guaranteed by characterization and are not tested.

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{ds(on)P_2}$	SWITCH RESISTANCE P2 (NOTE 2)	V_P = 0 volts V_S = 3 volts I load = 1mA	–	40	100	Ω
		@ T_A = 85°C	–	60	–	
		V_P = 0 volts V_S = 5 volts I load = 1mA	–	26	–	Ω
		V_P = 0 volts V_S = 9 volts I load = 1mA	–	16	–	Ω
$T_{C(P2)}$	TEMPERATURE COEFFICIENT OF SWITCH RESISTANCE P2	V_P = 0 volts V_S = 3 volts I load = 1mA	–	0.7	–	%/°C
$I_{L(PS)}$	LEAKAGE CURRENT (V_P to V_S)	V_P = 5 volts V_S = 3 volts I load = 10mA	–	0.01	20	nA
		@ T_A = 85°C	–	35	–	
$I_{L(SP)}$	LEAKAGE CURRENT (V_S to V_P)	V_P = 0 volts V_S = 3 volts I load = 1mA	–	0.01	50	nA
		@ T_A = 85°C	–	120	–	
$V_{O\ Pbar}$	OPEN DRAIN OUTPUT SATURATION VOLTAGES	V_P = 5 volts V_S = 3 volts I sink = 3.2mA I load = 0mA	–	85	400	mV
		@ T_A = 85°C	–	120	–	
		V_P = 9 volts V_S = 3 volts I sink = 3.2mA I load = 0mA	–	50	–	mV
		V_P = 12 volts V_S = 3 volts I sink = 3.2mA I load = 0mA	–	40	–	mV
$V_{O\ Sbar}$		V_P = 0 volts V_S = 3 volts I sink = 3.2mA I load = 0mA	–	150	400	mV
		@ T_A = 85°C	–	210	–	
		V_P = 0 volts V_S = 5 volts I sink = 3.2mA I load = 0mA	–	85	–	mV
		V_P = 0 volts V_S = 9 volts I sink = 3.2mA I load = 0mA	–	50	–	mV

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7673

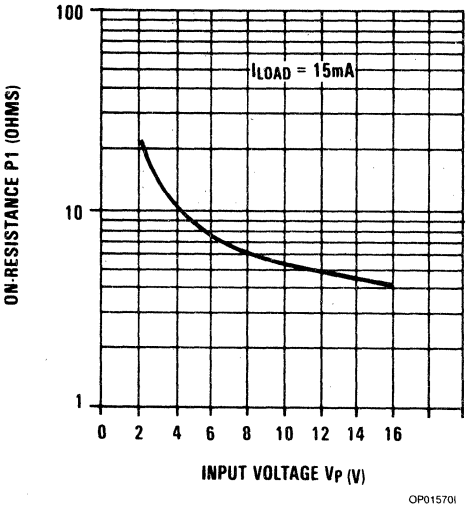
ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{L\ Pbar}$	OUTPUT LEAKAGE CURRENTS OF Pbar AND Sbar	V_P = 0 volts V_S = 15 volts I load = 0mA	–	50	500	nA
		@ T_A = 85°C	–	900	–	
$I_{L\ Sbar}$		V_P = 15 volts V_S = 0 volts I load = 0mA	–	50	500	nA
		@ T_A = 85°C	–	900	–	
$V_P - V_S$	SWITCHOVER UNCERTAINTY FOR COMPLETE SWITCHING OF INPUTS AND OPEN DRAIN OUTPUTS.	V_S = 3 volts I sink = 3.2mA I load = 0mA	–	5	50	mV

NOTE 2. The minimum input to output voltage can be determined by multiplying the load current by the switch resistance.

TYPICAL PERFORMANCE CHARACTERISTICS

ON-RESISTANCE SWITCH P1 AS A FUNCTION OF INPUT VOLTAGE V_P



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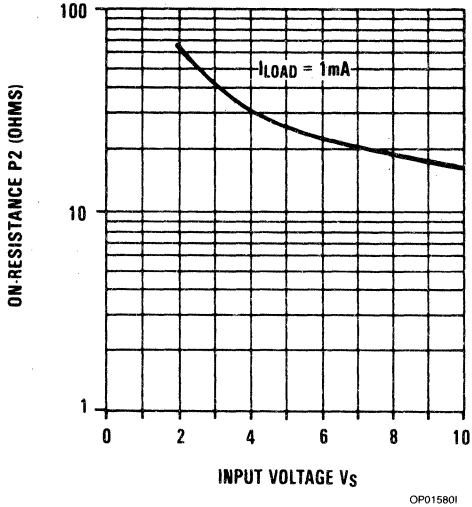
ON-RESISTANCE SWITCH P2 AS A FUNCTION OF INPUT VOLTAGE V_S



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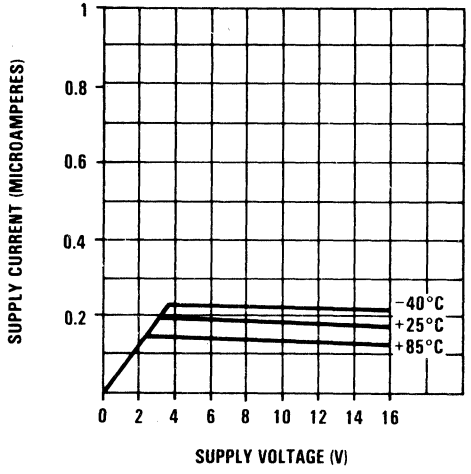
Note: All typical values have been guaranteed by characterization and are not tested.

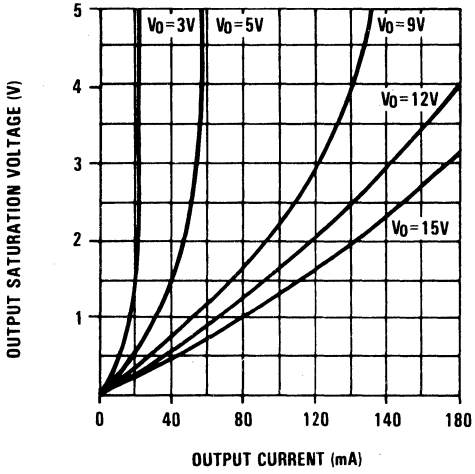
TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



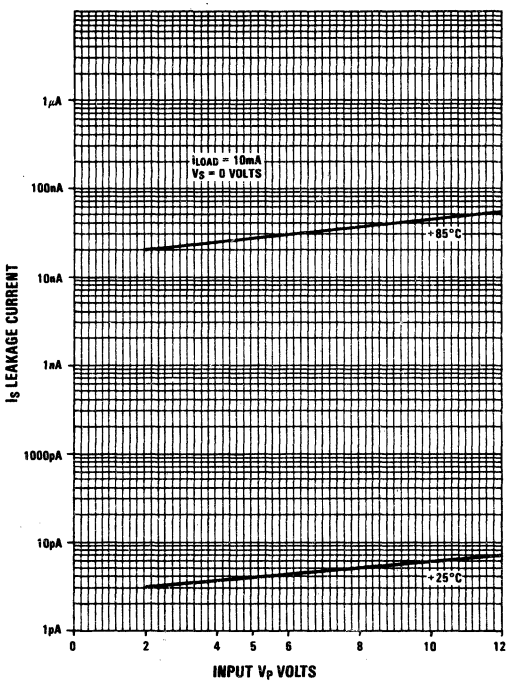
OP01590I

Pbar OR Sbar SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



OP01600I

I_S LEAKAGE CURRENT V_P to V_S AS A FUNCTION OF INPUT VOLTAGE



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DETAILED DESCRIPTION

As shown in the functional diagram (Figure 1), the ICL7673 includes a comparator which senses the input voltages V_P and V_S. The output of the comparator drives the first inverter and the open-drain N-channel transistor P_{bar}. The first inverter drives a large P-channel switch, P1, a second inverter, and another open-drain N-channel transistor, S_{bar}. The second inverter drives another large P-channel switch P2. The ICL7673, connected to a main and a backup power supply, will connect the supply of greater potential to its output. The circuit provides break-before-make switch action as it switches from main to backup power in the event of a main power supply failure. For proper operation, inputs V_P and V_S must not be allowed to float, and, the difference in the two supplies must be greater than 50 millivolts. The leakage current through the reverse biased parasitic diode of switch P2 is very low.

OUTPUT VOLTAGE

The output operating voltage range is 2.5 to 15 volts. The insertion loss between either input and the output is a function of load current, input voltage, and temperature. This is due to the P-channels being operated in their triode region, and, the ON-resistance of the switches is a function of output voltage V_O. The ON-resistance of the P-channels have positive temperature coefficients, and therefore as temperature increases the insertion loss also increases. At low load currents the output voltage is nearly equal to the greater of the two inputs. The maximum voltage drop across switch P1 or P2 is 0.5 volts, since above this voltage the body-drain parasitic diode will become forward biased. Complete switching of the inputs and open-drain outputs typically occurs in 50 microseconds.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7673

INPUT VOLTAGE

The input operating voltage range for V_P or V_S is 2.5 to 15 volts. The input supply voltage (V_P or V_S) slew rate should be limited to 2 volts per microsecond to avoid potential harm to the circuit. In line-operated systems, the rate-of-rise (or fall) of the supply is a function of power supply design. For battery applications it may be necessary to use a capacitor between the input and ground pins to limit the rate-of-rise of the supply voltage. A low-impedance capacitor such as a 0.047μF disc ceramic can be used to reduce the rate-of-rise.

STATUS INDICATOR OUTPUTS

The N-channel open drain output transistors can be used to indicate which supply is connected, or can be used to drive external PNP transistors to increase the power switching capability of the circuit. When using external PNP power transistors, the output current is limited by the beta and thermal characteristics of the power transistors. The application section details the use of external PNP transistors.

APPLICATIONS

A typical discrete battery backup circuit is illustrated in Figure 3. This approach requires several components, substantial printed circuit board space, and high labor cost. It also consumes a fairly high quiescent current. The ICL7673 battery backup circuit, illustrated in Figure 4, will often replace such discrete designs and offer much better performance, higher reliability, and lower system manufacturing cost. A trickle charge system could be implemented with an additional resistor and diode as shown in Figure 5. A complete low power AC to regulated DC system can be implemented using the ICL7673 and ICL7663 micropower voltage regulator as shown in Figure 6.

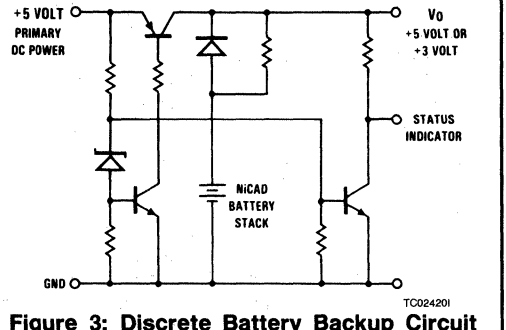


Figure 3: Discrete Battery Backup Circuit

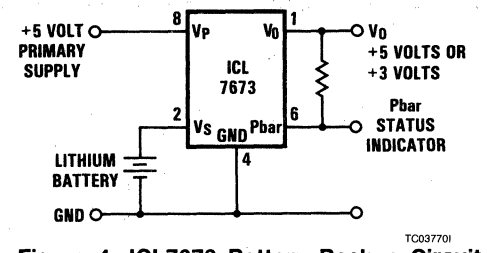


Figure 4: ICL7673 Battery Backup Circuit

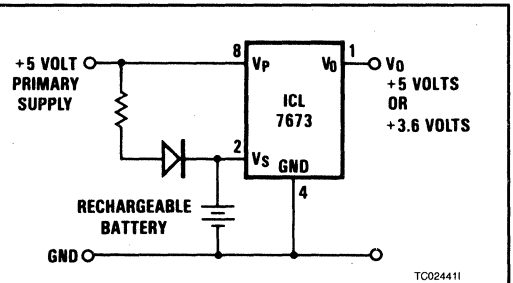


Figure 5: Application Requiring Rechargeable Battery Backup

Applications for the ICL7673 include volatile semiconductor memory storage systems, real-time clocks, timers, alarm systems, and over/under voltage detectors. Other systems requiring DC power when the master AC line supply fails can also use the ICL7673.

A typical application, as illustrated in Figure 7, would be a microprocessor system requiring a 5 volt supply. In the event of primary supply failure, the system is powered down, and a 3 volt battery is employed to maintain clock or volatile memory data. The main and backup supplies are connected to V_P and V_S, with the circuit output V_O supplying power to the clock or volatile memory. The ICL7673 will sense the main supply, when energized, to be of greater potential than V_S and connect, via its internal MOS switches, V_P to output V_O. The backup input, V_S will be disconnected internally. In the event of main supply failure, the circuit will sense that the backup supply is now the greater potential, disconnect V_P from V_O, and connect V_S.

Figure 8 illustrates the use of external PNP power transistors to increase the power switching capability of the circuit. In this application the output current is limited by the beta and thermal characteristics of the power transistors.

If hysteresis is desired for a particular low power application, positive feedback can be applied between the input V_P and open drain output S_{bar} through a resistor as illustrated in Figure 9. For high power applications hysteresis can be applied as shown in Figure 10.

The ICL7673 can also be used as a clipping circuit as illustrated in Figure 11. With high impedance loads the circuit output will be nearly equal to the greater of the two input signals.

Note: All typical values have been guaranteed by characterization and are not tested.

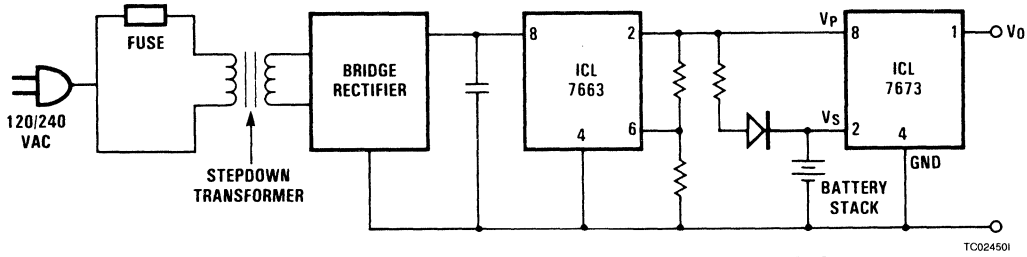


Figure 6: Power Supply for Low Power Portable AC to DC Systems

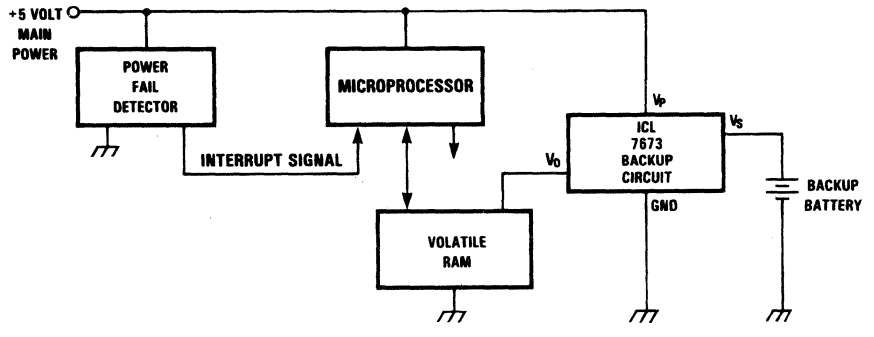


Figure 7: Typical Microprocessor Memory Application

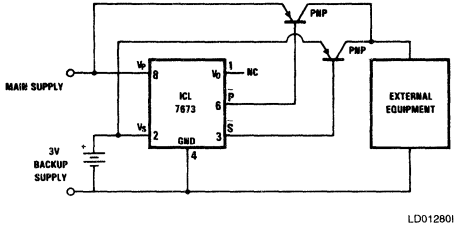


Figure 8: High Current Battery Backup System

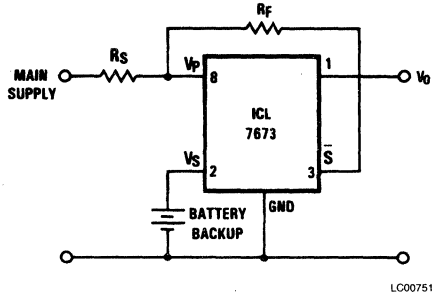


Figure 9: Low Current Battery Backup System With Hysteresis

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7673

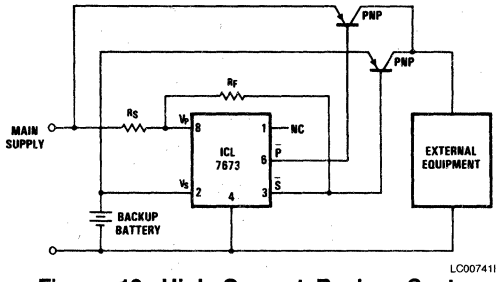


Figure 10: High Current Backup System With Hysteresis

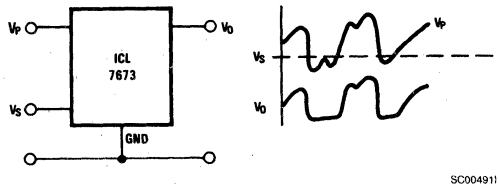


Figure 11: Clipping Circuits

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8013
Four Quadrant Analog Multiplier

GENERAL DESCRIPTION

The ICL8013 is a four quadrant analog multiplier whose output is proportional to the algebraic product of two input signals. Feedback around an internal op-amp provides level shifting and can be used to generate division and square root functions. A simple arrangement of potentiometers may be used to trim gain accuracy, offset voltage and feedthrough performance. The high accuracy, wide bandwidth, and increased versatility of the ICL8013 make it ideal for all multiplier applications in control and instrumentation systems. Applications include RMS measuring equipment, frequency doublers, balanced modulators and demodulators, function generators, and voltage controlled amplifiers.

FEATURES

- **Accuracy of ±0.5% ("A" Version)**
- **Full ±10V Input Voltage Range**
- **1MHz Bandwidth**
- **Uses Standard ±15V Supplies**
- **Built-in Op Amp Provides Level Shifting, Division and Square Root Functions**

ORDERING INFORMATION

PART NUMBER	MULTIPLICATION ERROR	TEMPERATURE RANGE	PACKAGE
ICL8013AM TZ	±0.5%	−55°C to +125°C	
ICL8013BM TZ	±1% MAX	−55°C to +125°C	
ICL8013CM TZ	±2%	−55°C to +125°C	10-LEAD
ICL8013AC TZ	±5%	0°C to +70°C	TO-100
ICL8013BC TZ	±1% MAX	0°C to +70°C	
ICL8013CC TZ	±2%	0°C to +70°C	
ICL8013/D	±2% TYP	—	DICE**

**Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.

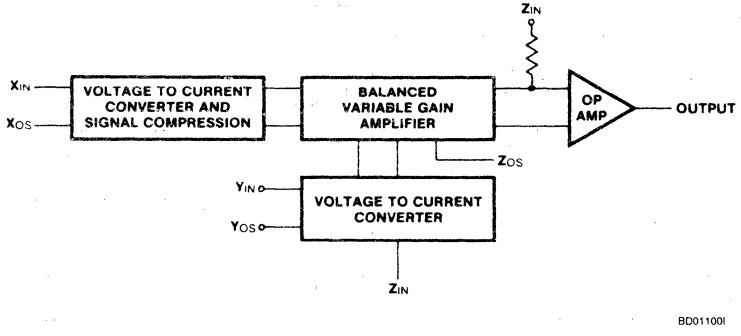


Figure 1: Functional Diagram (Multiplexer)

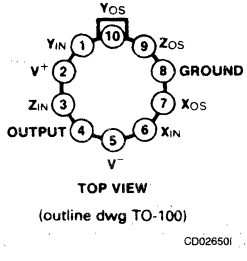


Figure 2: Pin Configuration

5

302085-002

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8013

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Power Dissipation (Note 1) 500mW
Input Voltages
(X_{IN}, Y_{IN}, Z_{IN}, X_{OS}, Y_{OS}, Z_{OS}) ..... V_{SUPPLY}

Operating Temperature Range:
ICL8013XC ..... 0°C to +70°C
ICL8013XM ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE 1: Derate at 6.8mW/°C for operation at ambient temperature above 75°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Unless otherwise specified T_A = 25°C, V_{SUPPLY} = ±15V, Gain and Offset Potentiometers Externally Trimmed)

PARAMETER		TEST CONDITIONS	ICL8013A			ICL8013B			ICL8013C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Multiplier Function				$\frac{XY}{10}$			$\frac{XY}{10}$			$\frac{XY}{10}$		
Multiplication Error		−10 < X < 10 −10 < Y < 10			0.5			1.0		2.0*	2.0	% Full Scale
Divider Function				$\frac{10Z}{X}$			$\frac{10Z}{X}$			$\frac{10Z}{X}$		
Division Error		X = −10 X = −1		0.3 1.5			0.3 1.5			0.3 1.5		% Full Scale % Full Scale
Feedthrough		X = 0 Y = $20V_{p-p}$ f = 50Hz Y = 0 X = $20V_{p-p}$ f = 50Hz			50 50			100 100		200* 150*	200 150	mV_{p-p} mV_{p-p}
Non-Linearity	X Input	X = $20V_{p-p}$ Y = ±10Vdc		±0.5			±0.5			±0.8		%
	Y Input	Y = $20V_{p-p}$ X = ±10Vdc		±0.2			±0.2			±0.3		%
Frequency Response Small Signal Bandwidth (−3dB)				1.0			1.0			1.0		MHz
Full Power Bandwidth				750			750			750		kHz
Slew Rate				45			45			45		V/μs
1% Amplitude Error				75			75			75		kHz
1% Vector Error (0.5° Chase Shift)				5			5			5		kHz
Settling Time (to ±2% of Final Value) Overload Recovery (to ±2% of Final Value)		V_{IN} = ±10V		1 1			1 1			1 1		μs μs
Output Noise		5 Hz to 10 kHz 5 Hz to 5 MHz		0.6 3			0.6 3			0.6 3		mV rms mV rms
Input Resistance	X Input			10			10			10		MΩ
	Y Input			6			6			6		MΩ
	Z Input			36			36			36		kΩ
Input Bias Current	X or Y Input			2	5			7.5			10	μA
	Z Input			25			25			25		μA
Power Supply Variation	Multiplication Error			0.2			0.2			0.2		%/%
	Output Offset				50			75			100	mV/V
	Scale Factor			0.1			0.1			0.1		%/%
Quiescent Current				3.5	6.0		3.5	6.0		3.5	6.0	mA

Note: All typical values have been guaranteed by characterization and are not tested.

ELECTRICAL CHARACTERISTICS (CONT.)

PARAMETER		TEST CONDITIONS	ICL8013A			ICL8013B			ICL8013C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
THE FOLLOWING SPECIFICATIONS APPLY OVER THE OPERATING TEMPERATURE RANGES												
Multiplication Error		$-10V < X_{IN} < 10V$, $-10V < Y_{IN} < 10V$		1.5			2			3		% Full Scale
Average Temperature Coefficients	Accuracy			0.06			0.06			0.06		%/°C
	Output Offset			0.2			0.2			0.2		mV/°C
	Scale Factor			0.04			0.04			0.04		%/°C
Input Bias Current	X or Y Input				5			5			10	μA
	Z Input				25			25			35	μA
Input Voltage (X, Y, or Z)					±10			±10			±10	V
Output Voltage Swing		$R_L \geq 2k\Omega$ $C_L < 1000pF$		±10			±10			±10		V

*Dice only

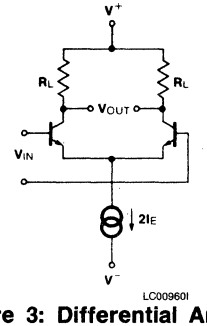


Figure 3: Differential Amplifier

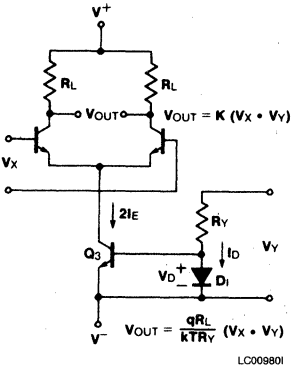


Figure 4: Transconductance Multiplier

DETAILED DESCRIPTION

The fundamental element of the ICL8013 multiplier is the bipolar differential amplifier of Figure 3.

The small signal differential voltage gain of this circuit is given by

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{R_L}{r_e}$$

Substituting $r_e = \frac{1}{g_m} = \frac{kT}{qI_E}$

$$V_{OUT} = V_{IN}\frac{R_L}{r_e} = V_{IN} \cdot \frac{qI_E R_L}{kT}$$

The output voltage is thus proportional to the product of the input voltage V_{IN} and the emitter current I_E. In the simple transconductance multiplier of Figure 4, a current source comprising Q_3, D_1, and R_Y is used. If V_Y is large compared with the drop across D_1, then

$$I_D \simeq \frac{V_Y}{R_Y} = 2I_E \text{ and}$$

$$V_{OUT} = \frac{qR_L}{kTR_Y}(V_X \cdot V_Y)$$

There are several difficulties with this simple modulator:

1: V_Y must be positive and greater than V_D.

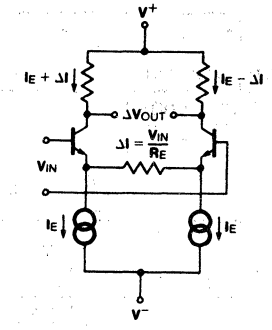
2: Some portion of the signal at V_X will appear at the output unless $I_E = 0$.

3: V_X must be a small signal for the differential pair to be linear.

4: The output voltage is not centered around ground.

The first problem relates to the method of converting the V_Y voltage to a current to vary the gain of the V_X differential pair. A better method, Figure 5, uses another differential pair but with considerable emitter degeneration. In this circuit the differential input voltage appears across the common emitter resistor, producing a current which adds or subtracts from the quiescent current in either collector. This type of voltage to current converter handles signals from 0 volts to ±10 volts with excellent linearity.

Note: All typical values have been guaranteed by characterization and are not tested.

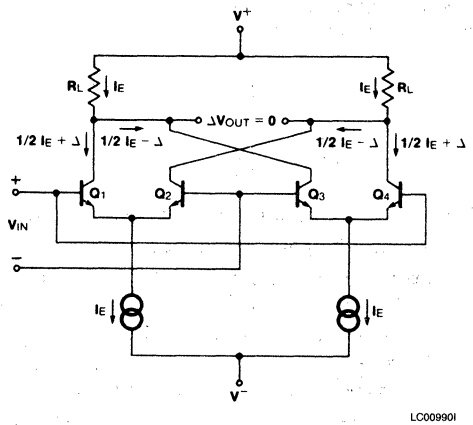


LC00970I

Figure 5: Voltage to Current Converter

The second problem is called feedthrough; i.e. the product of zero and some finite input signal does not produce zero output voltage. The circuit whose operation is illustrated by Figures 6A, B, and C overcomes this problem and forms the heart of many multiplier circuits in use today.

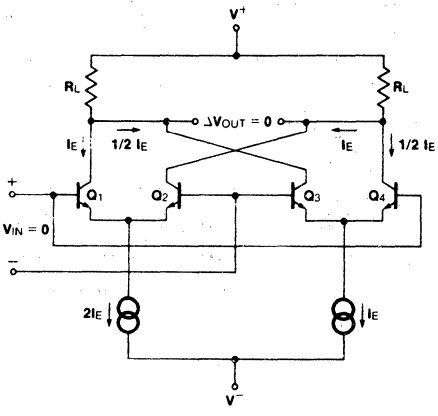
This circuit is basically two matched differential pairs with cross coupled collectors. Consider the case shown in 6A of exactly equal current sources biasing the two pairs. With a small positive signal at V_{IN}, the collector current of Q_1 and Q_4 will increase but the collector currents of Q_2 and Q_3 will decrease by the same amount. Since the collectors are cross coupled the current through the load resistors remains unchanged and independent of the V_{IN} input voltage.



LC00990I

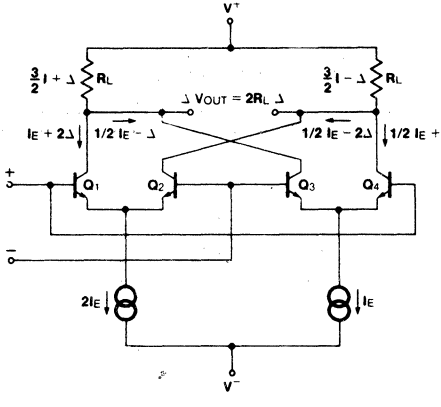
Figure 6A: Input Signal with Balanced Current Sources $\Delta V_{OUT} = 0V$

In Figure 6B, notice that with $V_{IN} = 0$ any variation in the ratio of biasing current sources will produce a common mode voltage across the load resistors. The differential output voltage will remain zero. In Figure 6C we apply a differential input voltage with unbalanced current sources. If I_{E1} is twice I_{E2}, the gain of differential pair Q_1 and Q_2 is twice the gain of pair Q_3 and Q_4. Therefore, the change in cross coupled collector currents will be unequal and a differential output voltage will result. By replacing the separate biasing current sources with the voltage to current converter of Figure 5 we have a balanced multiplier circuit capable of four quadrant operation (Figure 7).



LC01000I

Figure 6B: No Input Signal with Unbalanced Current Sources $\Delta V_{OUT} = 0V$

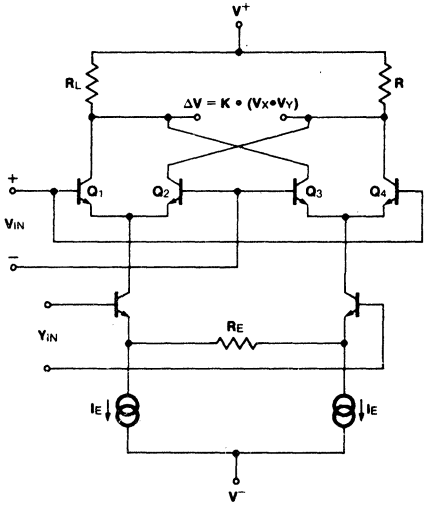


LC01020I

Figure 6C: Input Signal with Unbalanced Current Sources, Differential Output Voltage

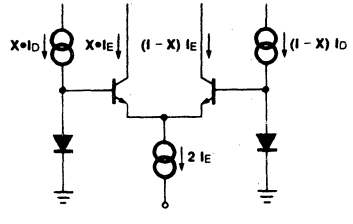
Note: All typical values have been guaranteed by characterization and are not tested.

This circuit of Figure 7 still has the problem that the input voltage V_{IN} must be small to keep the differential amplifier in the linear region. To be able to handle large signals, we need an amplitude compression circuit.



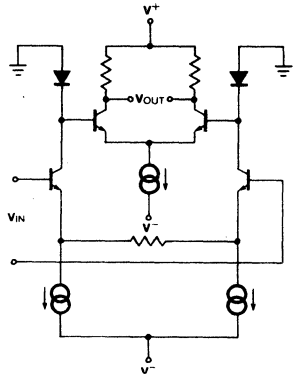
LC01010I

Figure 7: Typical Four Quadrant Multiplier-Modulator



LC01030I

Figure 8A: Current Gain Cell



LC01040I

Figure 8B: Voltage Gain with Signal Compression

Figure 5 showed a current source formed by relying on the matching characteristics of a diode and the emitter base junction of a transistor. Extension of this idea to a differential circuit is shown in Figure 8A. In a differential pair, the input voltage splits the biasing current in a logarithmic ratio. (The usual assumption of linearity is useful only for small signals.) Since the input to the differential pair in Figure 8A is the difference in voltage across the two diodes, which in turn is proportional to the log of the ratio of drive currents, it follows that the ratio of diode currents and the ratio of collector currents are linearly related and independent of amplitude. If we combine this circuit with the voltage to current converter of Figure 5, we have Figure 8B. The output of the differential amplifier is now proportional to the input voltage over a large dynamic range, thereby improving linearity while minimizing drift and noise factors.

The complete schematic is shown in Figure 9. The differential pair Q_3 and Q_4 form a voltage to current converter whose output is compressed in collector diodes Q_1 and Q_2. These diodes drive the balanced cross-coupled differential amplifier Q_7/Q_8 Q_{14}/Q_{15}. The gain of these amplifiers is modulated by the voltage to current converter Q_9 and Q_{10}. Transistors Q_5, Q_6, Q_{11}, and Q_{12} are constant current sources which bias the voltage to current converter. The output amplifier comprises transistors Q_{16} through Q_{27}.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8013

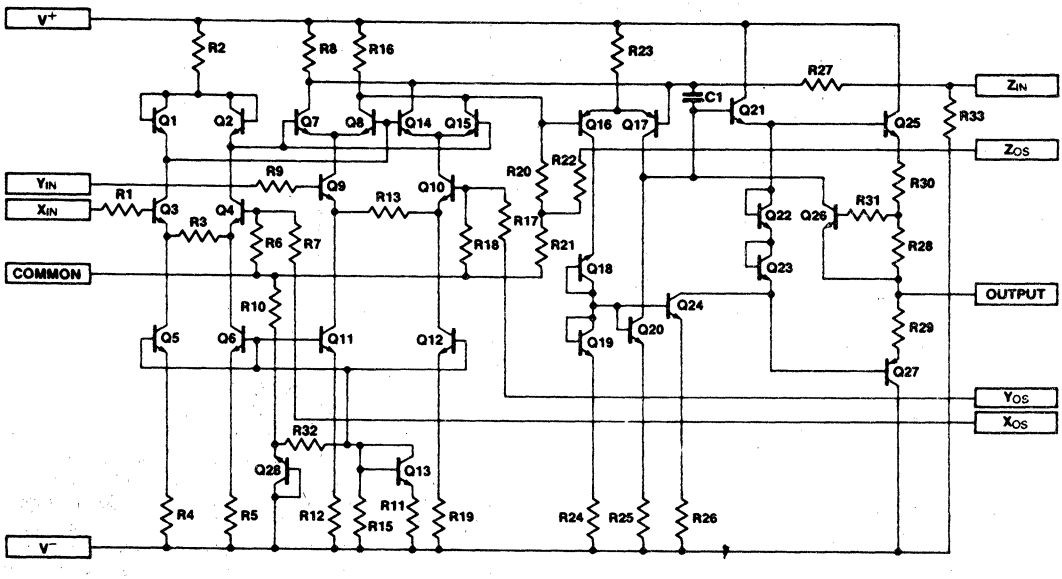


Figure 9: ICL8013 Schematic

MULTIPLICATION

In the standard multiplier connection, the Z terminal is connected to the op amp output. All of the modulator output current thus flows through the feedback resistor R27 and produces a proportional output voltage.

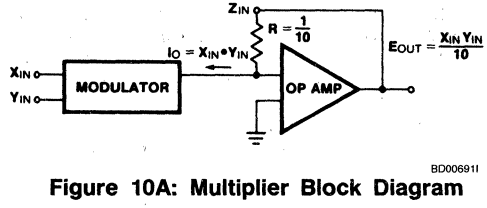


Figure 10A: Multiplier Block Diagram

Multiplier Trimming Procedure

1. Set $X_{IN} = Y_{IN} = 0V$ and adjust Z_{OS} for zero Output.
2. Apply a ±10V low frequency (≤ 100Hz) sweep (sine or triangle) to Y_{IN} with $X_{IN} = 0V$, and adjust X_{OS} for minimum output.
3. Apply the sweep signal of Step 2 to X_{IN} with $Y_{IN} = 0V$ and adjust Y_{OS} for minimum Output.
4. Readjust Z_{OS} as in Step 1, if necessary.
5. With $X_{IN} = 10.0V$ DC and the sweep signal of Step 2 applied to Y_{IN}, adjust the Gain potentiometer for Output = Y_{IN}. This is easily accomplished with a differential scope plug-in (A + B) by inverting one signal and adjusting Gain control for (Output – Y_{IN}) = Zero.

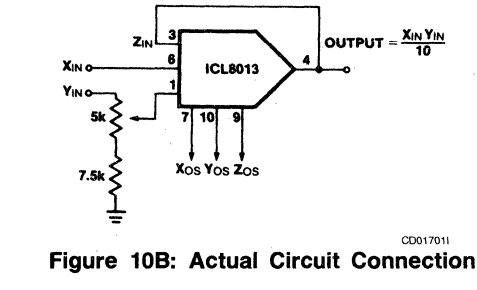


Figure 10B: Actual Circuit Connection

DIVISION

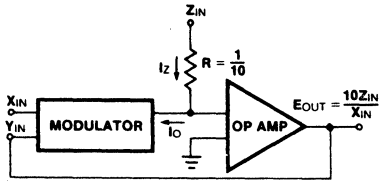
If the Z terminal is used as an input, and the output of the op-amp connected to the Y input, the device functions as a divider. Since the input to the op-amp is at virtual ground, and requires negligible bias current, the overall feedback forces the modulator output current to equal the current produced by Z.

$$\text{Therefore } I_O = X_{IN} \cdot Y_{IN} = \frac{Z_{IN}}{R} = 10Z_{IN}$$

$$\text{Since } Y_{IN} = E_{OUT},\ E_{OUT} = \frac{10Z_{IN}}{X_{IN}}$$

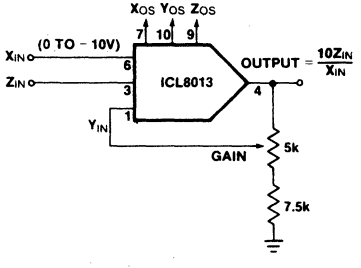
Note: All typical values have been guaranteed by characterization and are not tested.

Note that when connected as a divider, the X input must be a negative voltage to maintain overall negative feedback.



BD007011

Figure 11A: Division Block Diagram



CD017111

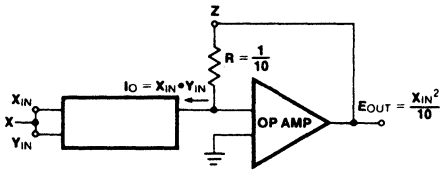
Figure 11B: Actual Circuit Connection

Divider Trimming Procedure

1. Set trimming potentiometers at mid-scale by adjusting voltage on pins 7, 9 and 10 (X_{OS}, Y_{OS}, Z_{OS}) for zero volts.
2. With Z_{IN} = 0V, trim Z_{OS} to hold the Output constant, as X_{IN} is varied from −10V through −1V.
3. With Z_{IN} = 0V and X_{IN} = −10.0V adjust Y_{OS} for zero Output voltage.
4. With $Z_{IN} = X_{IN}$ (and/or $Z_{IN} = -X_{IN}$) adjust X_{OS} for minimum worst-case variation of Output, as X_{IN} is varied from −10V to −1V.
5. Repeat Steps 2 and 3 if Step 4 required a large initial adjustment.
6. With $Z_{IN} = X_{IN}$ (and/or $Z_{IN} = -X_{IN}$) adjust the gain control until the output is the closest average around +10.0V (−10V for $Z_{IN} = -X_{IN}$) as X_{IN} is varied from −10V to −3V.

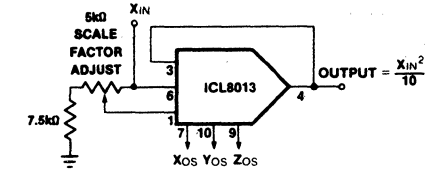
SQUARING

The squaring function is achieved by simply multiplying with the two inputs tied together. The squaring circuit may also be used as the basis for a frequency doubler since $\cos^2\omega t = 1/2\ (\cos 2\omega t + 1)$.



BD007211

Figure 12A: Squarer Block Diagram



CD017211

Figure 12B: Actual Circuit Connection

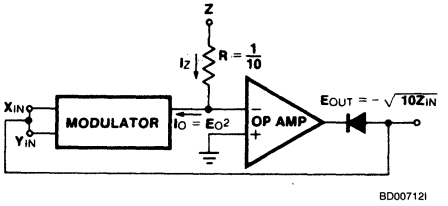
SQUARE ROOT

Tying the X and Y inputs together and using overall feedback from the Op Amp results in the square root function. The output of the modulator is again forced to equal the current produced by the Z input.

$$I_O = X_{IN} \cdot Y_{IN} = (-E_{OUT})^2 = 10Z_{IN}$$

$$E_{OUT} = -\sqrt{10Z_{IN}}$$

The output is a negative voltage which maintains overall negative feedback. A diode in series with the Op Amp output prevents the latchup that would otherwise occur for negative input voltages.



BD007121

Figure 13A: Square Root Block Diagram

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8013

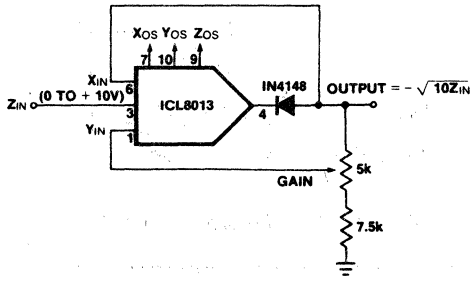


Figure 13B: Actual Circuit Connection

Square Root Trimming Procedure

1. Connect the ICL8013 in the *Divider* configuration.
2. Adjust Z_{OS}, Y_{OS}, X_{OS}, and Gain using Steps 1 through 6 of Divider Trimming Procedure.
3. Convert to the Square Root configuration by connecting X_{IN} to the Output and inserting a diode between Pin 4 and the Output node.
4. With Z_{IN} = 0V adjust Z_{OS} for zero Output voltage.

VARIABLE GAIN AMPLIFIER

Most applications for the ICL8013 are straight forward variations of the simple arithmetic functions described above. Although the circuit description frequently disguises the fact, it has already been shown that the frequency doubler is nothing more than a squaring circuit. Similarly the variable gain amplifier is nothing more than a multiplier, with the input signal applied at the X input and the control voltage applied at the Y input.

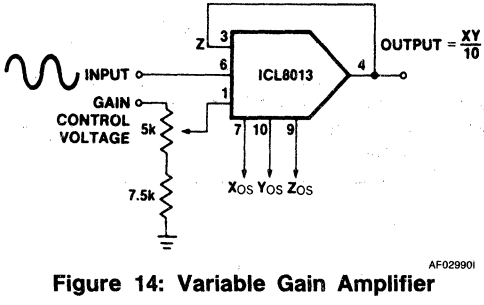


Figure 14: Variable Gain Amplifier

TYPICAL APPLICATIONS

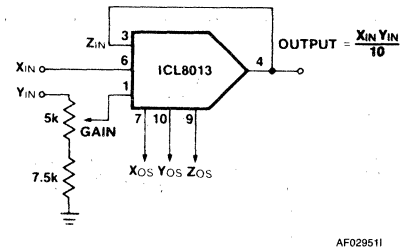


Figure 15: Multiplication

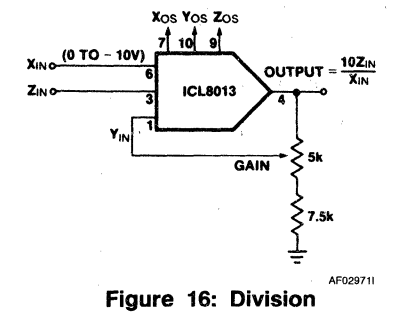


Figure 16: Division

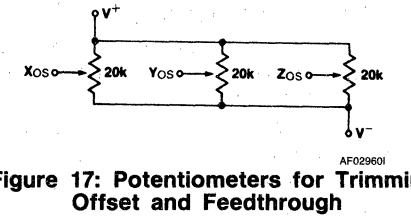


Figure 17: Potentiometers for Trimming Offset and Feedthrough

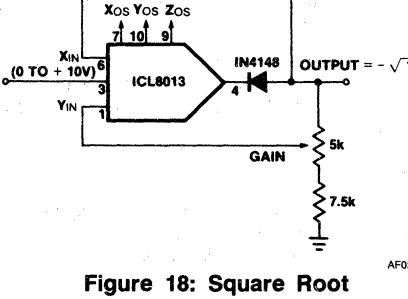


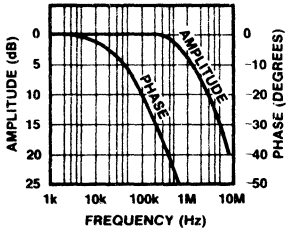
Figure 18: Square Root

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8013

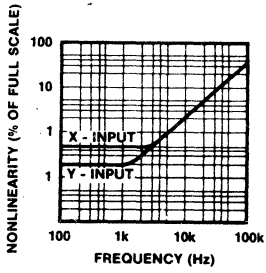
TYPICAL PERFORMANCE CHARACTERISTICS

AMPLITUDE AND PHASE AS A FUNCTION OF FREQUENCY



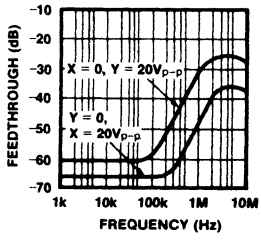
OP02720I

NONLINEARITY AS A FUNCTION OF FREQUENCY



OP02730I

FEEDTHROUGH AS A FUNCTION OF FREQUENCY



OP02740I

DEFINITION OF TERMS

Multiplication/Division Error: This is the basic accuracy specification. It includes terms due to linearity, gain, and offset errors, and is expressed as a percentage of the full scale output.

Feedthrough: With either input at zero, the output of an ideal multiplier should be zero regardless of the signal applied to the other input. The output seen in a non-ideal multiplier is known as the feedthrough.

Nonlinearity: The maximum deviation from the best straight line constructed through the output data, expressed as a percentage of full scale. One input is held constant and the other swept through its nominal range. The nonlinearity is the component of the total multiplication/division error which cannot be trimmed out.

5

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8038
Precision Waveform Generator/Voltage Controlled Oscillator

GENERAL DESCRIPTION

The ICL8038 Waveform Generator is a monolithic integrated circuit capable of producing high accuracy sine, square, triangular, sawtooth and pulse waveforms with a minimum of external components. The frequency (or repetition rate) can be selected externally from .001Hz to more than 300kHz using either resistors or capacitors, and frequency modulation and sweeping can be accomplished with an external voltage. The ICL8038 is fabricated with advanced monolithic technology, using Schottky-barrier diodes and thin film resistors, and the output is stable over a wide range of temperature and supply variations. These devices may be interfaced with phase locked loop circuitry to reduce temperature drift to less than 250ppm/°C.

FEATURES

- **Low Frequency Drift With Temperature — 250ppm/°C**
- **Simultaneous Sine, Square, and Triangle Wave Outputs**
- **Low Distortion — 1% (Sine Wave Output)**
- **High Linearity — 0.1% (Triangle Wave Output)**
- **Wide Operating Frequency Range — 0.001Hz to 300kHz**
- **Variable Duty Cycle — 2% to 98%**
- **High Level Outputs — TTL to 28V**
- **Easy to Use — Just A Handful of External Components Required**

ORDERING INFORMATION

PART NUMBER	STABILITY	TEMP. RANGE	PACKAGE
ICL8038CCJD	250ppm/°C typ	0°C to +70°C	CERDIP
ICL8038BCJD	180ppm/°C typ	0°C to +70°C	CERDIP
ICL8038ACJD	110ppm/°C typ	0°C to +70°C	CERDIP
ICL8038BMJD*	350ppm/°C max	−55°C to +125°C	CERDIP
ICL8038AMJD*	250ppm/°C max	−55°C to +125°C	CERDIP
ICL8038/D	—	—	DICE**

*Add /883B to part number if 883 processing is required.

**Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.

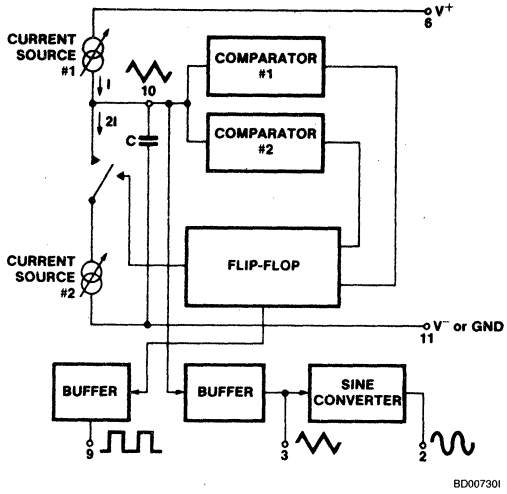


Figure 1: Functional Diagram

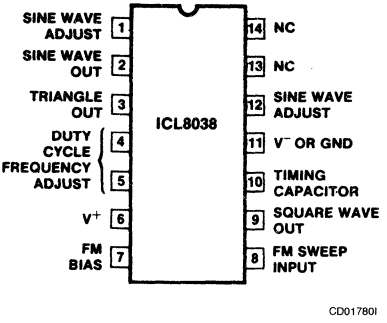


Figure 2: Pin Configuration (Outline dwg JD)

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8038

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^- to V^+) 36V
Power Dissipation[1] 750mW
Input Voltage (any pin) ..... V^- to V^+
Input Current (Pins 4 and 5) 25mA
Output Sink Current (Pins 3 and 9) 25mA

Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range:
8038AM, 8038BM ..... −55°C to +125°C
8038AC, 8038BC, 8038CC ..... 0°C to +70°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: Derate ceramic package at 12.5mW/°C for ambient temperatures above 100°C.

ELECTRICAL CHARACTERISTICS (V_{SUPPLY} = ±10V or +20V, T_A = 25°C, R_L = 10kΩ, Test Circuit Unless Otherwise Specified)

SYMBOL	GENERAL CHARACTERISTICS	8038CC			8038BC(BM)			8038AC(AM)			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{SUPPLY}	Supply Voltage Operating Range										
V^+	Single Supply	+10		+30	+10		30	+10		30	V
V^+, V^-	Dual Supplies	±5		±15	±5		±15	±5		±15	V
I_{SUPPLY}	Supply Current (V_{SUPPLY} = ±10V)[2]										
	8038AM, 8038BM					12	15		12	15	mA
	8038AC, 8038BC, 8038CC		12	20		12	20		12	20	mA
FREQUENCY CHARACTERISTICS (all waveforms)											
f_{max}	Maximum Frequency of Oscillation	100			100			100			kHz
f_{sweep}	Sweep Frequency of FM Input		10			10			10		kHz
	Sweep FM Range[3]		35:1			35:1			35:1		
	FM Linearity 10:1 Ratio		0.5			0.2			0.2		%
Δf/ΔT	Frequency Drift With Temperature[5] 8038 AC, BC, CC 0°C to 70°C		250			180			110		ppm/°C
	8038 AM, BM, −55°C to 125°C						350			250	
Δf/ΔV	Frequency Drift With Supply Voltage (Over Supply Voltage Range)		0.05			0.05			0.05		%/V
OUTPUT CHARACTERISTICS											
I_{OLK}	**Square-Wave** Leakage Current (V_9 = 30V)			1			1			1	μA
V_{SAT}	Saturation Voltage (I_{SINK} = 2mA)		0.2	0.5		0.2	0.4		0.2	0.4	V
t_r	Rise Time (R_L = 4.7kΩ)		180			180			180		ns
t_f	Fall Time (R_L = 4.7kΩ)		40			40			40		ns
ΔD	Typical Duty Cycle Adjust (Note 6)	2		98	2		98	2		98	%
$V_{TRIANGLE}$	**Triangle/Sawtooth/Ramp** Amplitude (R_{TRI} = 100kΩ)	0.30	0.33		0.30	0.33		0.30	0.33		xV_{SUPPLY}
	Linearity		0.1			0.05			0.05		%
Z_{OUT}	Output Impedance (I_{OUT} = 5mA)		200			200			200		Ω
V_{SINE}	**Sine-Wave** Amplitude (R_{SINE} = 100kΩ)	0.2	0.22		0.2	0.22		0.2	0.22		xV_{SUPPLY}
THD	THD (R_S = 1MΩ)[4]		2.0	5		1.5	3		1.0	1.5	%
THD	THD Adjusted (Use Figure 6)		1.5			1.0			0.8		%

NOTES: 2. R_A and R_B currents not included.
3. V_{SUPPLY} = 20V; R_A and R_B = 10kΩ, f ≅ 10kHz nominal; can be extended 1000 to 1. See Figures 7a and 7b.
4. 82kΩ connected between pins 11 and 12, Triangle Duty Cycle set at 50%. (Use R_A and R_B.)
5. Figure 3, pins 7 and 8 connected, V_{SUPPLY} = ±10V. See Typical Curves for T.C. vs V_{SUPPLY}.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8038

TEST CONDITIONS

PARAMETER		R_A	R_B	R_L	C_1	SW_1	MEASURE
Supply Current		10kΩ	10kΩ	10kΩ	3.3nF	Closed	Current into Pin 6
Sweep FM Range(1)		10kΩ	10kΩ	10kΩ	3.3nF	Open	Frequency at Pin 9
Frequency Drift with Temperature		10kΩ	10kΩ	10kΩ	3.3nF	Closed	Frequency at Pin 3
Frequency Drift with Supply Voltage(2)		10kΩ	10kΩ	10kΩ	3.3nF	Closed	Frequency at Pin 9
Output Amplitude:	Sine	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Pk-Pk output at Pin 2
(Note 4)	Triangle	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Pk-Pk output at Pin 3
Leakage Current (off)(3)		10kΩ	10kΩ		3.3nF	Closed	Current into Pin 9
Saturation Voltage (on)(3)		10kΩ	10kΩ		3.3nF	Closed	Output (low) at Pin 9
Rise and Fall Times (Note 5)		10kΩ	10kΩ	4.7kΩ	3.3nF	Closed	Waveform at Pin 9
Duty Cycle Adjust:	MAX	50kΩ	~1.6kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 9
(Note 5)	MIN	~25kΩ	50kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 9
Triangle Waveform Linearity		10kΩ	10kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 3
Total Harmonic Distortion		10kΩ	10kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 2

NOTES: 1. The hi and lo frequencies can be obtained by connecting pin 8 to pin 7 (f_{hi}) and then connecting pin 8 to pin 6 (f_{lo}). Otherwise apply Sweep Voltage at pin 8 $(2/3\ V_{SUPPLY} + 2V) \leq V_{SWEEP} \leq V_{SUPPLY}$ where V_{SUPPLY} is the total supply voltage. In Figure 7b, pin 8 should vary between 5.3V and 10V with respect to ground.

2. $10V \leq V^+ \leq 30V$, or $\pm 5V \leq V_{SUPPLY} \leq \pm 15V$.
3. Oscillation can be halted by forcing pin 10 to +5 volts or −5 volts.
4. Output Amplitude is tested under static conditions by forcing pin 10 to 5.0V then to −5.0V.
5. Not tested; for design purposes only.

DEFINITION OF TERMS:

Supply Voltage (V_{SUPPLY}). The total supply voltage from V^+ to V^-

Supply Current. The supply current required from the power supply to operate the device, excluding load currents and the currents through R_A and R_B.

Frequency Range. The frequency range at the square wave output through which circuit operation is guaranteed.

Sweep FM Range. The ratio of maximum frequency to minimum frequency which can be obtained by applying a sweep voltage to pin 8. For correct operation, the sweep voltage should be within the range

$$(2/3\ V_{SUPPLY} + 2V) < V_{SWEEP} < V_{SUPPLY}$$

FM Linearity. The percentage deviation from the best-fit straight line on the control voltage versus output frequency curve.

Output Amplitude. The peak-to-peak signal amplitude appearing at the outputs.

Saturation Voltage. The output voltage at the collector of Q_{23} when this transistor is turned on. It is measured for a sink current of 2mA.

Rise and Fall Times. The time required for the square wave output to change from 10% to 90%, or 90% to 10%, of its final value.

Triangle Waveform Linearity. The percentage deviation from the best-fit straight line on the rising and falling triangle waveform.

Total Harmonic Distortion. The total harmonic distortion at the sine-wave output.

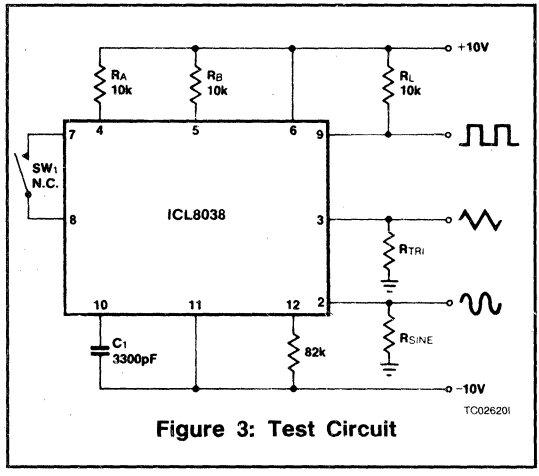
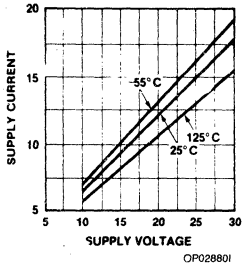


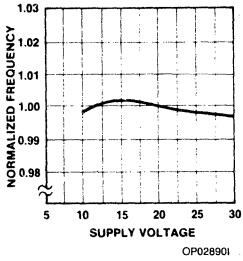
Figure 3: Test Circuit

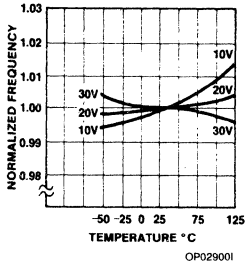
Note: All typical values have been guaranteed by characterization and are not tested.

ICL8038

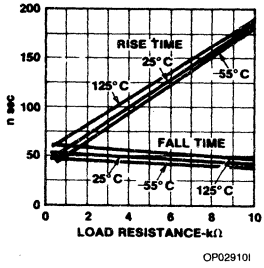
TYPICAL PERFORMANCE CHARACTERISTICS

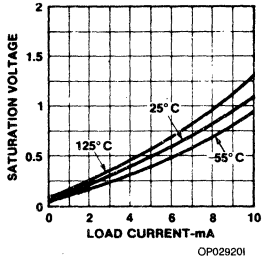




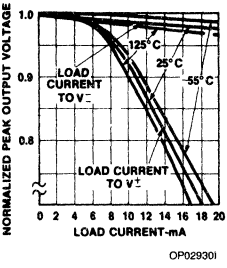


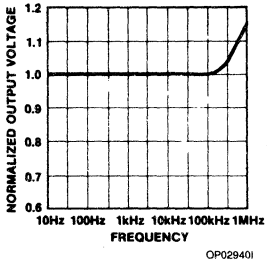
Performance of the Square-Wave Output

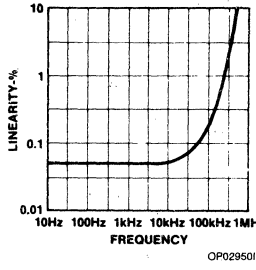




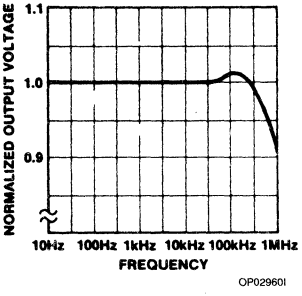
Performance of Triangle-Wave Output

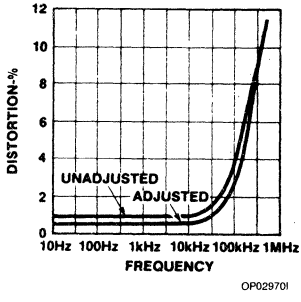




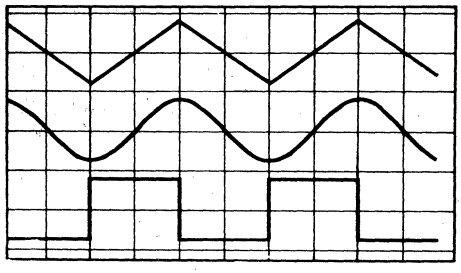


Performance of Sine-Wave Output



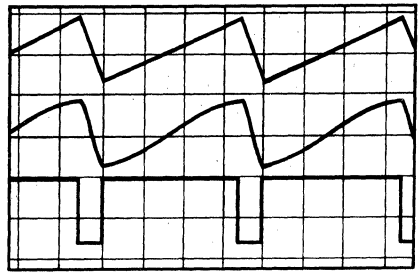


Note: All typical values have been guaranteed by characterization and are not tested.



WF01490I

Square-Wave Duty Cycle—50%



WF01500I

Square-Wave Duty Cycle—80%

Figure 4: Phase Relationship of Waveforms

DETAILED DESCRIPTION (See Figure 1)

An external capacitor C is charged and discharged by two current sources. Current source #2 is switched on and off by a flip-flop, while current source #1 is on continuously. Assuming that the flip-flop is in a state such that current source #2 is off, and the capacitor is charged with a current I, the voltage across the capacitor rises linearily with time. When this voltage reaches the level of comparator #1 (set at 2/3 of the supply voltage), the flip-flop is triggered, changes states, and releases current source #2. This current source normally carries a current 2I, thus the capacitor is discharged with a net-current I and the voltage across it drops linearly with time. When it has reached the level of comparator #2 (set at 1/3 of the supply voltage), the the flip-flop is triggered into its original state and the cycle starts again.

Four waveforms are readily obtainable from this basic generator circuit. With the current sources set at I and 2I respectively, the charge and discharge times are equal. Thus a triangle waveform is created across the capacitor and the flip-flop produces a square-wave. Both waveforms are fed to buffer stages and are available at pins 3 and 9.

The levels of the current sources can, however, be selected over a wide range with two external resistors. Therefore, with the two currents set at values different from I and 2I, an asymmetrical sawtooth appears at terminal 3 and pulses with a duty cycle from less than 1% to greater than 99% are available at terminal 9.

The sine-wave is created by feeding the triangle-wave into a non-linear network (sine-converter). This network provides a decreasing shunt-impedance as the potential of the triangle moves toward the two extremes.

WAVEFORM TIMING

The *symmetry* of all waveforms can be adjusted with the external timing resistors. Two possible ways to accomplish this are shown in Figure 5. Best results are obtained by keeping the timing resistors R_A and R_B separate (a). R_A controls the rising portion of the triangle and sine-wave and the 1 state of the square-wave.

The magnitude of the triangle-waveform is set at 1/3 V_{SUPPLY}; therefore the rising portion of the triangle is,

$$t_1 = \frac{C \times v}{I} = \frac{C \times \frac{1}{3} \times V_{SUPPLY} \times R_A}{\frac{1}{5} \times V_{SUPPLY}} = \frac{5}{3} R_A \times C$$

The falling portion of the triangle and sine-wave and the 0 state of the square-wave is:

$$t_2 = \frac{C \times V}{I} = \frac{C \times 1/3\ V_{SUPPLY}}{\frac{2}{5} \times \frac{V_{SUPPLY}}{R_B} - \frac{1}{5} \times \frac{V_{SUPPLY}}{R_A}} = \frac{5}{3} \times \frac{R_A R_B C}{2R_A - R_B}$$

Thus a 50% duty cycle is achieved when $R_A = R_B$.

If the duty-cycle is to be varied over a small range about 50% only, the connection shown in Figure 5b is slightly more convenient. If no adjustment of the duty cycle is desired, terminals 4 and 5 can be shorted together, as shown in Figure 5c. This connection, however, causes an inherently larger variation of the duty-cycle, frequency, etc.

With two separate timing resistors, the frequency is given by

$$f = \frac{1}{t_1 + t_2} = \frac{1}{\frac{5}{3} R_A C \left(1 + \frac{R_B}{2R_A - R_B}\right)}$$

or, if $R_A = R_B = R$

$$f = \frac{0.3}{RC} \text{ (for Figure 5a)}$$

If a single timing resistor is used (Figure 5c only), the frequency is

$$f = \frac{0.15}{RC}$$

Note: All typical values have been guaranteed by characterization and are not tested.

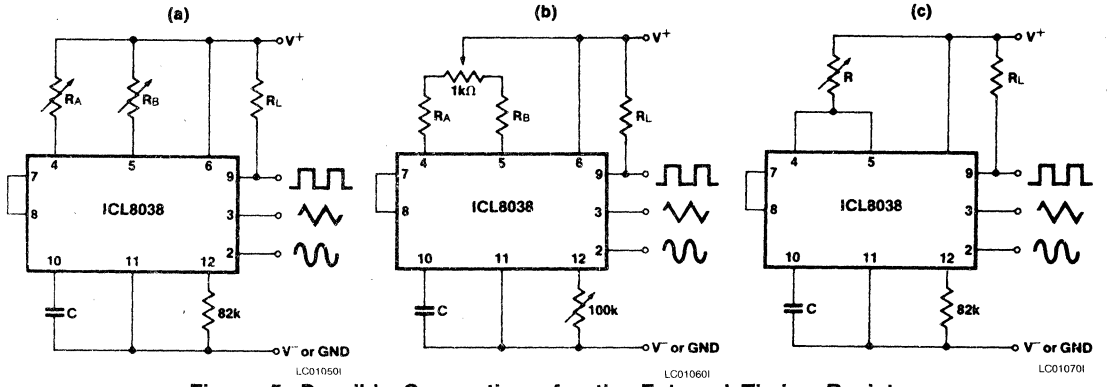


Figure 5: Possible Connections for the External Timing Resistors

Neither time nor frequency are dependent on supply voltage, even though none of the voltages are regulated inside the integrated circuit. This is due to the fact that both currents *and* thresholds are direct, linear functions of the supply voltage and thus their effects cancel.

To minimize *sine-wave* distortion the 82kΩ resistor between pins 11 and 12 is best made variable. With this arrangement distortion of less than 1% is achievable. To reduce this even further, two potentiometers can be connected as shown in Figure 6; this configuration allows a typical reduction of sine-wave distortion close to 0.5%.

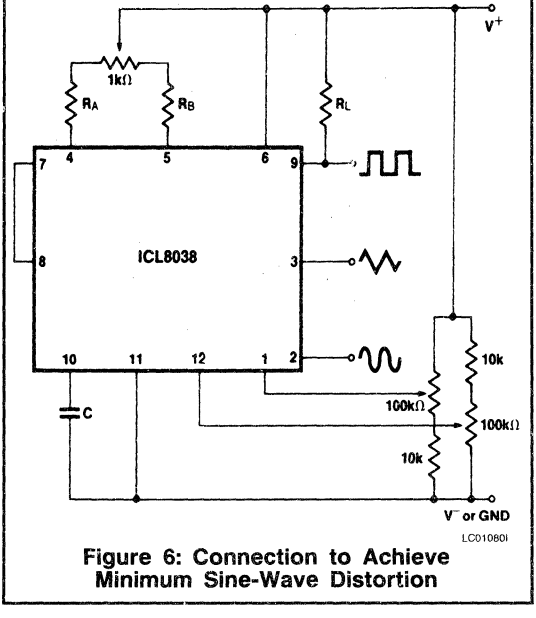


Figure 6: Connection to Achieve Minimum Sine-Wave Distortion

SELECTING R_A, R_B and C

For any given output frequency, there is a wide range of RC combinations that will work, however certain constraints are placed upon the magnitude of the charging current for optimum performance. At the low end, currents of less than 1μA are undesirable because circuit leakages will contribute significant errors at high temperatures. At higher currents (I > 5mA), transistor betas and saturation voltages will contribute increasingly larger errors. Optimum performance will, therefore, be obtained with charging currents of 10μA to 1mA. If pins 7 and 8 are shorted together, the magnitude of the charging current due to R_A can be calculated from:

$$I = \frac{R_1 \times (V^+ - V^-)}{(R_1 + R_2)} \times \frac{1}{R_A} = \frac{(V^+ - V^-)}{5R_A}$$

A similar calculation holds for R_B.

The capacitor value should be chosen at the upper end of its possible range.

WAVEFORM OUT LEVEL CONTROL AND POWER SUPPLIES

The waveform generator can be operated either from a single power-supply (10 to 30 Volts) or a dual power-supply (±5 to ±15 Volts). With a single power-supply the average levels of the triangle and sine-wave are at exactly one-half of the supply voltage, while the square-wave alternates between V^+ and ground. A split power supply has the advantage that all waveforms move symmetrically about ground.

The square-wave output is not committed. A load resistor can be connected to a different power-supply, as long as the applied voltage remains within the breakdown capability of the waveform generator (30V). In this way, the square-wave output can be made TTL compatible (load resistor connected to +5 Volts) while the waveform generator itself is powered from a much higher voltage.

Note: All typical values have been guaranteed by characterization and are not tested.

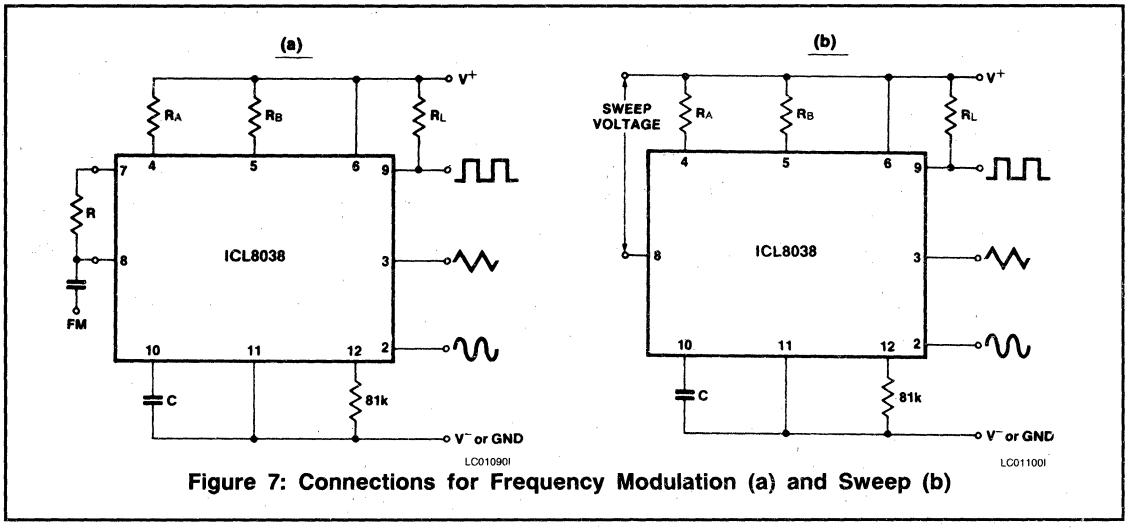


Figure 7: Connections for Frequency Modulation (a) and Sweep (b)

FREQUENCY MODULATION AND SWEEPING

The frequency of the waveform generator is a direct function of the DC voltage at terminal 8 (measured from V^+). By altering this voltage, frequency modulation is performed. For small deviations (e.g. ±10%) the modulating signal can be applied directly to pin 8, merely providing DC decoupling with a capacitor as shown in Figure 7a. An external resistor between pins 7 and 8 is not necessary, but it can be used to increase input impedance from about 8kΩ (pins 7 and 8 connected together), to about (R + 8kΩ).

The sine wave output has a relatively high output impedance (1kΩ Typ). The circuit of Figure 8 provides buffering, gain and amplitude adjustment. A simple op amp follower could also be used.

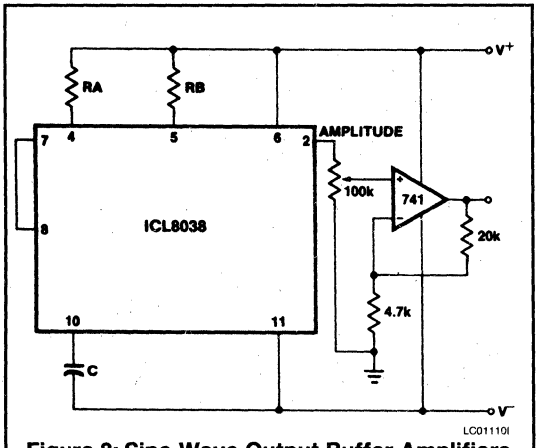


Figure 8: Sine Wave Output Buffer Amplifiers

For larger FM deviations or for frequency sweeping, the modulating signal is applied between the positive supply voltage and pin 8 (Figure 7b). In this way the entire bias for the current sources is created by the modulating signal, and a very large (e.g. 1000:1) sweep range is created (f = 0 at $V_{sweep} = 0$). Care must be taken, however, to regulate the supply voltage; in this configuration the charge current is no longer a function of the supply voltage (yet the trigger thresholds still are) and thus the frequency becomes dependent on the supply voltage. The potential on Pin 8 may be swept down from V^+ by $(1/3\ V_{SUPPLY} - 2V)$.

APPLICATIONS

With a dual supply voltage the external capacitor on Pin 10 can be shorted to ground to halt the ICL8038 oscillation. Figure 9 shows a FET switch, diode ANDed with an input strobe signal to allow the output to always start on the same slope.

To obtain a 1000:1 Sweep Range on the ICL8038 the voltage across external resistors R_A and R_B must decrease to nearly zero. This requires that the highest voltage on control Pin 8 exceed the voltage at the top of R_A and R_B by a few hundred millivolts.

The Circuit of Figure 10 achieves this by using a diode to lower the effective supply voltage on the ICL8038. The large resistor on pin 5 helps reduce duty cycle variations with sweep.

Note: All typical values have been guaranteed by characterization and are not tested.

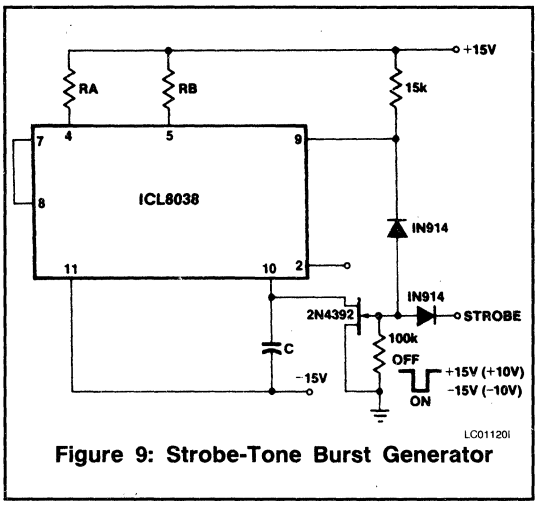


Figure 9: Strobe-Tone Burst Generator

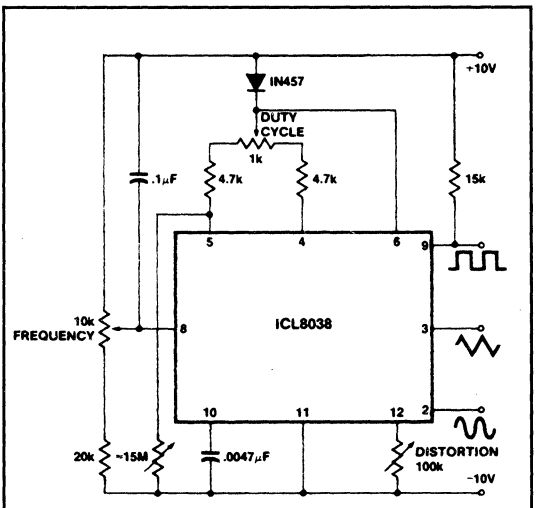


Figure 10: Variable Audio Oscillator, 20Hz to 20kHz

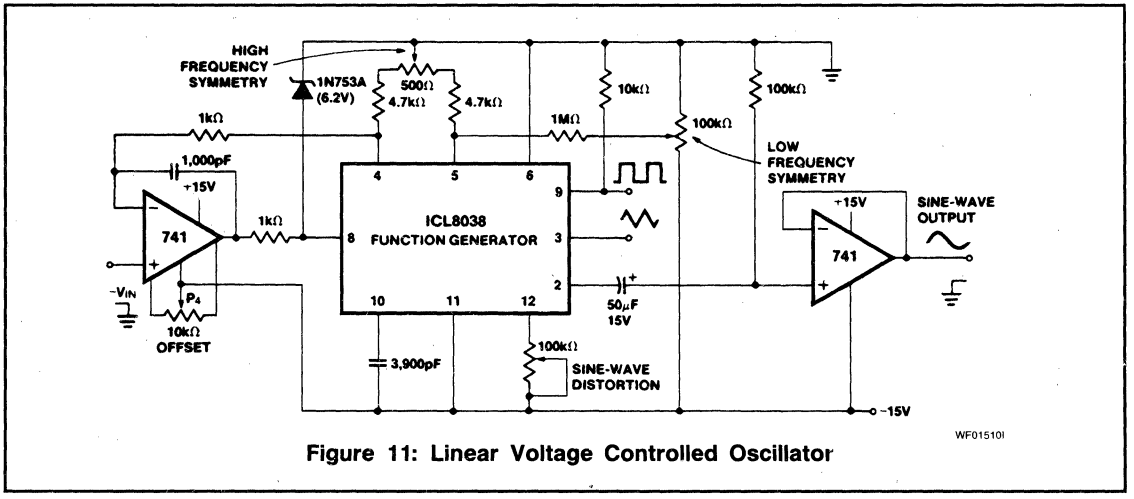


Figure 11: Linear Voltage Controlled Oscillator

The linearity of input sweep voltage versus output frequency can be significantly improved by using an op amp as shown in Figure 11.

USE IN PHASE-LOCKED LOOPS

Its high frequency stability makes the ICL8038 an ideal building block for a phase-locked loop as shown in Figure 12. In this application the remaining functional blocks, the phase-detector and the amplifier, can be formed by a number of available IC's (e.g. MC4344, NE562, HA2800, HA2820)

In order to match these building blocks to each other, two steps must be taken. First, two different supply voltages are used and the square wave output is returned to the supply of the phase detector. This assures that the VCO input voltage will not exceed the capabilities of the phase detector. If a smaller VCO signal is required, a simple resistive voltage divider is connected between pin 9 of the waveform generator and the VCO input of the phase-detector.

Second, the DC output level of the amplifier must be made compatible to the DC level required at the FM input of the waveform generator (pin 8, $0.8V^+$). The simplest solution here is to provide a voltage divider to V^+ (R_1, R_2 as shown) if the amplifier has a lower output level, or to ground if its level is higher. The divider can be made part of the low-pass filter.

This application not only provides for a free-running frequency with very low temperature drift, but it also has the

Note: All typical values have been guaranteed by characterization and are not tested.

unique feature of producing a large reconstituted sinewave signal with a frequency identical to that at the input.

For further information, see Intersil Application Note A013, "Everything You Always Wanted to Know About The ICL8038."

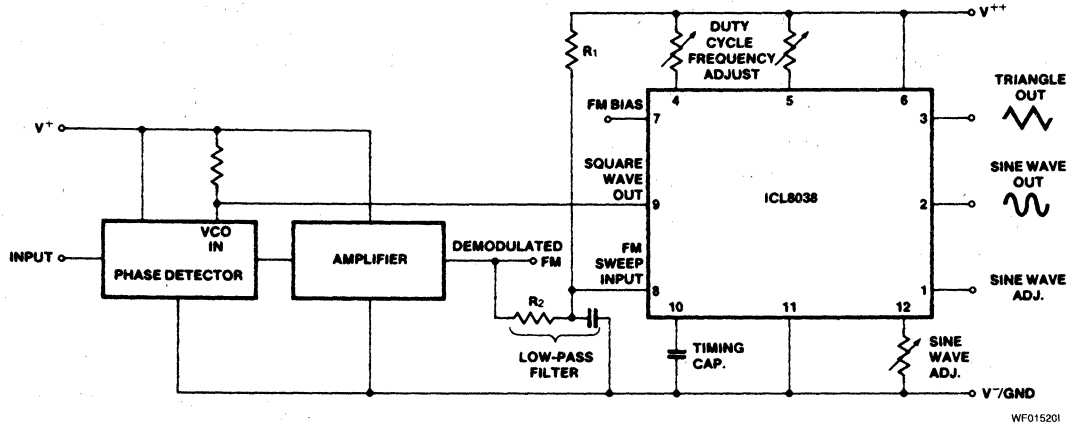


Figure 12: Waveform Generator Used as Stable VCO in a Phase-Locked Loop

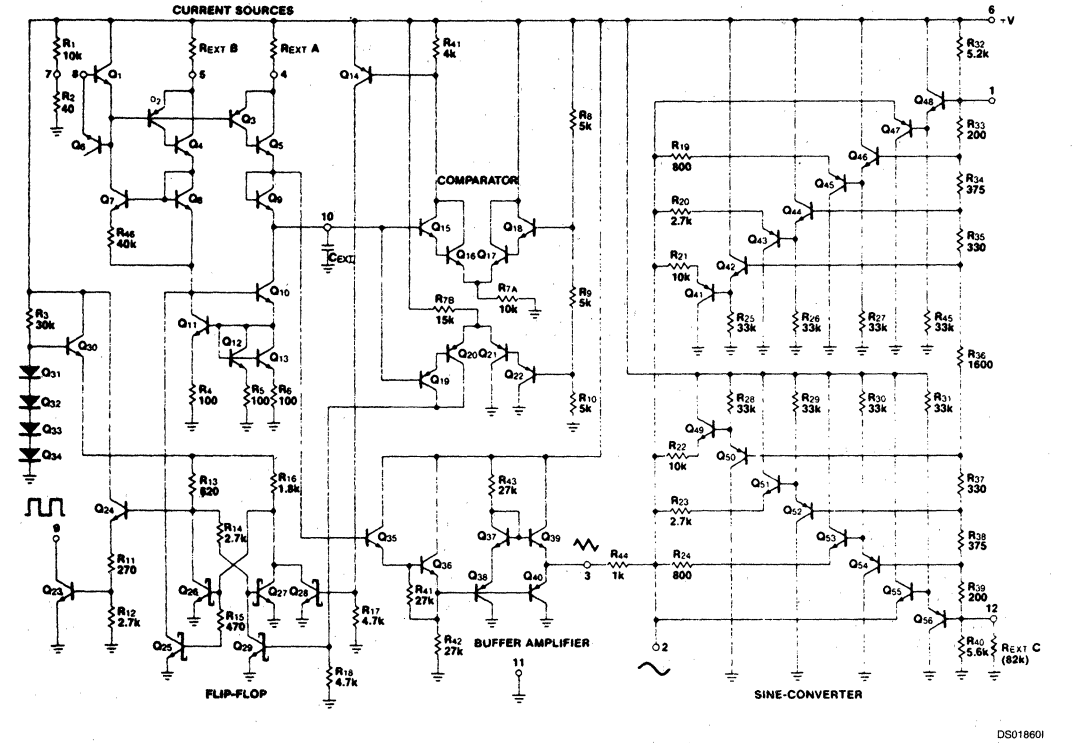


Figure 13: Detailed Schematic

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8069
Low Voltage Reference

GENERAL DESCRIPTION

The ICL8069 is a 1.2V temperature compensated voltage reference. It uses the band-gap principle to achieve excellent stability and low noise at reverse currents down to 50μA. Applications include analog-to-digital converters, digital-to-analog converters, threshold detectors, and voltage regulators. Its low power consumption makes it especially suitable for battery operated equipment.

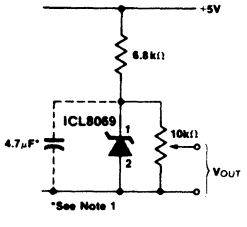
FEATURES

- **Temperature Coefficient Guaranteed to 25ppm/°C Max**
- **Low Bias Current — 50μA Min**
- **Low Dynamic Impedance**
- **Low Reverse Voltage**
- **Low Cost**

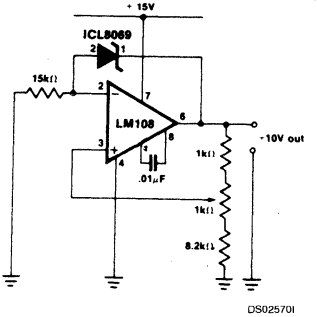
ORDERING INFORMATION

ORDER P/N TO-92	ORDER P/N TO-52	TEMPERATURE RANGE	MAX. TEMP. COEFF. OF V_{REF}
ICL8069CCZR	ICL8069CCSQ	0°C to +70°C	0.005%/°C
—	ICL8069CMSQ	−55°C to +125°C	0.005%/°C
ICL8089DCZR	ICL8069DCSQ	0°C to +70°C	0.01%/°C
—	ICL8069DMSQ	−55°C to +125°C	0.01%/°C
ICL8069/D	—	—	DICE**

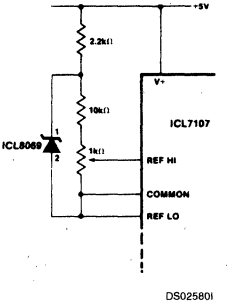
**Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.



(a) Simple Reference (1.2 volts or less)

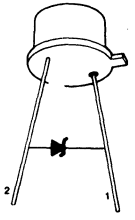


(b) Buffered 10V Reference using a single supply.

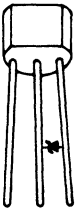


(c) Double regulated 100mV reference for ICL7107 one-chip DPM circuit.

Figure 1: Functional Diagrams



TO-52



TO-92

Figure 2: Pin Configurations

303120-002

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8069

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Reverse Voltage ..... See Note 2
Forward Current 10mA
Reverse Current 10mA
Power Dissipation ..... Limited by max forward/reverse current

Storage Temperature ..... −65°C to +150°C
Operating Temperature
ICL8069C ..... 0°C to +70°C
ICL8069M ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

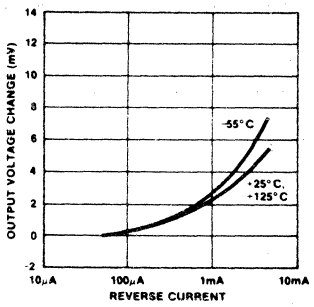
NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reverse breakdown Voltage	I_R = 500μA	1.20	1.23	1.25	V
Reverse breakdown Voltage change	50μA ≤ I_R ≤ 5mA		15	20	mV
Reverse dynamic impedance	I_R = 50μA I_R = 500μA		1 1	2 2	Ω
Forward Voltage Drop	I_F = 500μA		0.7	1	V
RMS Noise Voltage	10Hz ≤ f ≤ 10kHz I_R = 500μA		5		μV
Long Term Stability	I_R = 4.75mA T_A = 25°C		1		ppm/kHR
Breakdown voltage Temperature coefficient ICL8069C ICL8069D	I_R = 500μA T_A = operating Temperature range (Note 3)			 .005 .01	%/°C
Reverse Current Range		0.050		5	mA

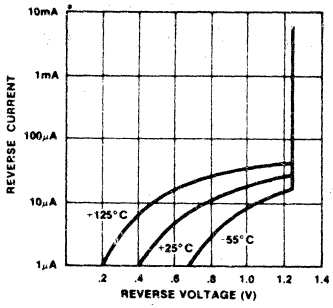
TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE CHANGE AS A FUNCTION OF REVERSE CURRENT



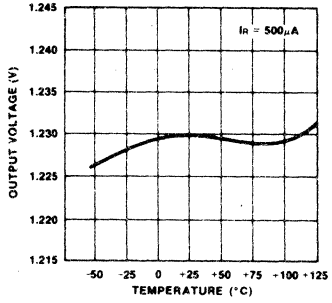
OP05620I

REVERSE VOLTAGE AS A FUNCTION OF CURRENT



OP05630I

REVERSE VOLTAGE AS A FUNCTION OF TEMPERATURE



OP05640I

Notes:

1) If circuit strays in excess of 200pF are anticipated, a 4.7μF shunt capacitor will ensure stability under all operating conditions.

2) In normal use, the reverse voltage cannot exceed the reference voltage. However when plugging units into a powered-up test fixture, an instantaneous voltage equal to the compliance of the test circuit will be seen. This should not exceed 20V.

3) For the military part, measurements are made at 25°C, −55°C, and +125°C. The unit is then classified as a function of the worst case T.C. from 25°C to −55°C, or 25°C to +125°C.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8211/ICL8212
Programmable Voltage Detector

GENERAL DESCRIPTION

The Intersil ICL8211/8212 are micropower bipolar monolithic integrated circuits intended primarily for precise voltage detection and generation. These circuits consist of an accurate voltage reference, a comparator and a pair of output buffer/drivers.

Specifically, the ICL8211 provides a 7mA current limited output sink when the voltage applied to the 'THRESHOLD' terminal is less than 1.15 volts (the internal reference). The ICL8212 requires a voltage in excess of 1.15 volts to switch its output on (no current limit). Both devices have a low current output (HYSTERESIS) which is switched on for input voltages in excess of 1.15V. The HYSTERESIS output may be used to provide positive and noise free output switching using a simple feedback network.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL8211CPA	0°C to +70°C	8 lead Mini DIP
ICL8211CBA	0°C to +70°C	8 lead SOIC
ICL8211CTY	0°C to +70°C	TO-99 Can
ICL8211MTY*	−55°C to +125°C	TO-99 Can
ICL8212CPA	0°C to +70°C	8 lead Mini DIP
ICL8212CBA	0°C to +70°C	8 lead SOIC
ICL8212CTY	0°C to +70°C	TO-99 Can
ICL8212MTY*	−55°C to +125°C	TO-99 Can
ICL8211/D	—	DICE **
ICL8212/D	—	DICE **

* Add /883B to part number if 883B processing is required.

**Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.

FEATURES

- **High Accuracy Voltage Sensing and Generation: Internal Reference 1.15 Volts Typical**
- **Low Sensitivity to Supply Voltage and Temperature Variations**
- **Wide Supply Voltage Range: Typ. 1.8 to 30 Volts**
- **Essentially Constant Supply Current Over Full Supply Voltage Range**
- **Easy to Set Hysteresis Voltage Range**
- **Defined Output Current Limit — ICL8211 High Output Current Capability — ICL8212**

APPLICATIONS

- **Low Voltage Sensor/Indicator**
- **High Voltage Sensor/Indicator**
- **Non Volatile Out-of-Voltage Range Sensor/ Indicator**
- **Programmable Voltage Reference or Zener Diode**
- **Series or Shunt Power Supply Regulator**
- **Fixed Value Constant Current Source**

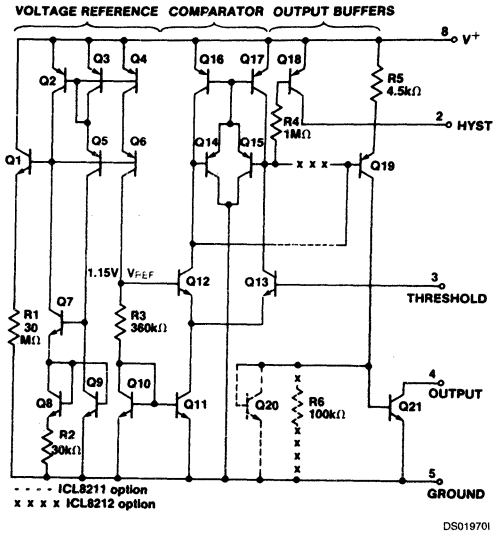


Figure 1: Functional Diagram

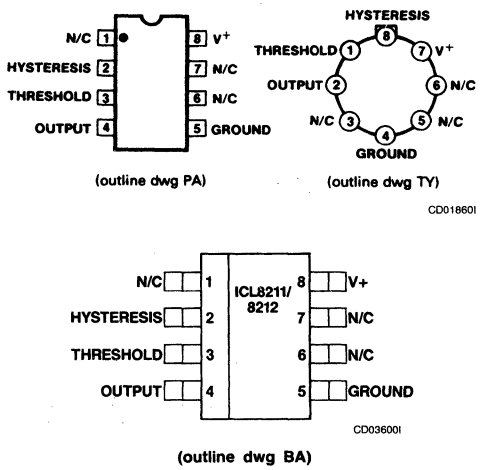


Figure 2: Pin Configurations

303200-002

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8211/ICL8212

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... −0.5 to +30 volts
Output Voltage ..... −0.5 to +30 volts
Hysteresis Voltage ..... +0.5 to −10 volts
Threshold Input Voltage .....
+30 to −5 volts with respect to GROUND and +0 to −30 volts with respect to V^+
Current into Any Terminal ..... ±30mA

Power Dissipation (Note 1 & 2) 300mW
Operating Temperature Range:
ICL8211M/8212M ..... −55°C to +125°C
ICL8211C/8212C ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) .....300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: Rating applies for case temperatures to 125°C to ICL8211MTY/8212MTY products. Derate linearly at −10mW/°C for ambient temperatures above 100°C.

NOTE 2: Derate linearly above 50°C by −10mW/°C for ICL8211C/8212C products. The threshold input voltage may exceed +7 volts for short periods of time. However for continuous operation this voltage must be maintained at a value less than 7 volts.

ELECTRICAL CHARACTERISTICS (V^+ = 5V, T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	ICL8211			ICL8212			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I^+	Supply Current	$2.0 < V^+ < 30$ V_T = 1.3V V_T = 0.9V	 10 50	 22 140	 40 250	 50 10	 110 20	 250 40	 µA µA
V_{TH}	Threshold Trip Voltage	I_{OUT} = 4mA V^+ = 5V I_{OUT} = 4mA V^+ = 2V V_{OUT} = 2V V^+ = 30V	0.98 0.98 1.00	1.15 1.145 1.165	1.19 1.19 1.20	1.00 1.00 1.05	1.15 1.145 1.165	1.19 1.19 1.20	V V V
V_{THP}	Threshold Voltage Disparity Between Output & Hysteresis Output	I_{OUT} = 4mA V_{OUT} = 2V I_{HYST} = 7µA V_{HYST} = 3V		−8.0			−0.5		mV
V_{SUPPLY}	Guaranteed Operating Supply Voltage Range (Note 5)	+25°C 0 to +70°C −55°C to +125°C	2.0 2.2 2.8		30 30 30	2.0 2.2 2.8		30 30 30	V V V
V_{SUPPLY}	Typical Operating Supply Voltage Range	+25°C +125°C −55°C	1.8 1.4 2.5		30 30 30	1.8 1.4 2.5		30 30 30	V V V
$\Delta V_{TH}/\Delta T$	Threshold Voltage Temperature Coefficient	I_{OUT} = 4mA V_{OUT} = 2V		+200			+200		ppm/°C
$\Delta V_{TH}/\Delta V^+$	Variation of Threshold Voltage with Supply Voltage	ΔV^+ = 10% at V^+ = 5V		1.0			1.0		mV
I_{TH}	Threshold Input Current	V_{TH} = 1.15V V_{TH} = 1.00V		100 5	250		100 5	250	nA nA
I_{OLK}	Output Leakage Current	V_{OUT} = 30V V_{TH} = 1.0V V_{OUT} = 30V V_{TH} = 1.3V V_{OUT} = 5V V_{TH} = 1.0V V V_{OUT} = 5V V_{TH} = 1.3V			10 1 			10 1 	µA µA µA µA
V_{SAT}	Output Saturation Voltage	V_{TH} = 1.0V I_{OUT} = 4mA V_{TH} = 1.3V		0.17	0.4		0.17	0.4	V V
I_{OH}	Max Available Output Current	(Note 3 & 4) V_{TH} = 1.0V V_{OUT} = 5V V_{TH} = 1.3V −55°C ≤ T_A ≤ 125°C V_{TH} = 1.0V	4	7.0	12 15	 15 12	 35 	 	mA mA mA
I_{LHYS}	Hysteresis Leakage Current	V^+ = 10V V_{TH} = 1.0V V_{HYST} = V^-			0.1			0.1	µA
$V_{HYS\ (max)}$	Hysteresis Sat Voltage	I_{HYST} = −7µA V_{TH} = 1.3V measured with respect to V^+		−0.1	−0.2		−0.1	−0.2	V
$I_{HYS\ (max)}$	Max Available Hysteresis Current	V_{TH} = 1.3V	−15	−21		−15	−21		µA

NOTES: 3. The maximum output current of the ICL8211 is limited by design to 15mA under any operating conditions. The output voltage may be sustained at any voltage up to +30V as long as the maximum power dissipation of the device is not exceeded.
4. The maximum output current of the ICL8212 is not defined, and systems using the ICL8212 must therefore ensure that the output current does not exceed 30mA and that the maximum power dissipation of the device is not exceeded.
5. Threshold Trip Voltage is 0.80V(min) to 1.30V(max).

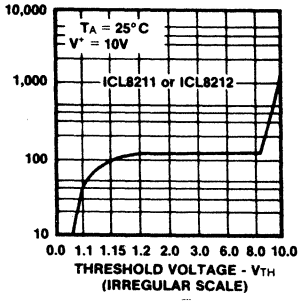
Note: All typical values have been guaranteed by characterization and are not tested.

ICL8211/ICL8212

INTERSIL

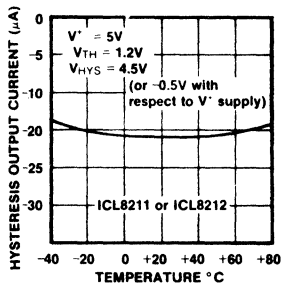
TYPICAL PERFORMANCE CHARACTERISTICS COMMON TO ICL8211 AND ICL8212

THRESHOLD INPUT CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE



OP03280I

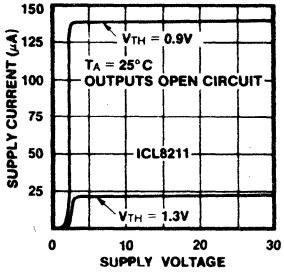
HYSTERESIS OUTPUT SATURATION CURRENT AS A FUNCTION OF TEMPERATURE



OP03290I

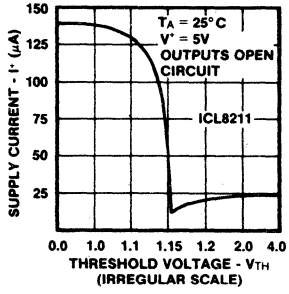
TYPICAL PERFORMANCE CHARACTERISTICS ICL8211 ONLY

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



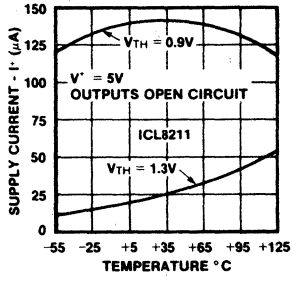
OP03300I

SUPPLY CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE



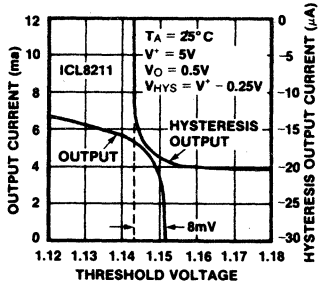
OP03310I

SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



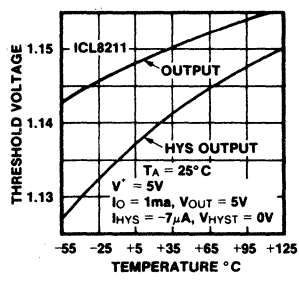
OP03320I

OUTPUT SATURATION CURRENTS AS A FUNCTION OF THRESHOLD VOLTAGE



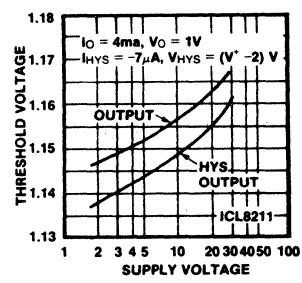
OP03330I

THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF TEMPERATURE



OP03340I

THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF SUPPLY VOLTAGE



OP03350I

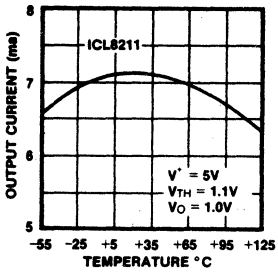
5

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8211/ICL8212

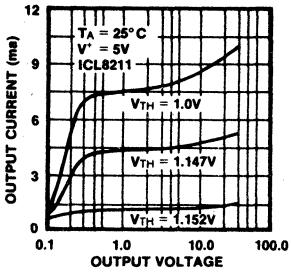
TYPICAL PERFORMANCE CHARACTERISTICS ICL8211 ONLY (CONT.)

OUTPUT SATURATION CURRENT AS A FUNCTION OF TEMPERATURE



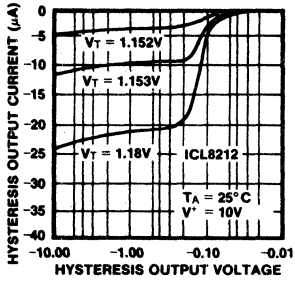
OP03360I

OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



OP03370I

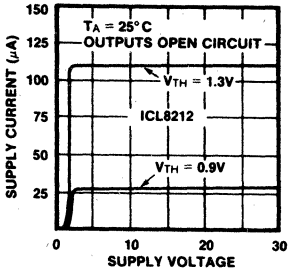
HYSTERESIS OUTPUT CURRENT AS A FUNCTION OF HYSTERESIS OUTPUT VOLTAGE



OP03380I

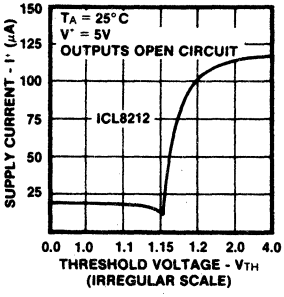
TYPICAL PERFORMANCE CHARACTERISTICS ICL8212 ONLY

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



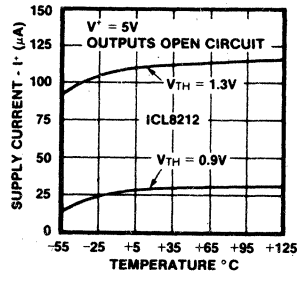
OP03390I

SUPPLY CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE



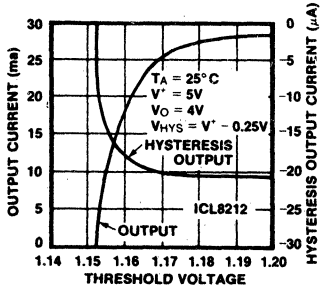
OP03400I

SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



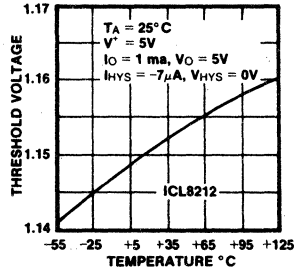
OP03410I

OUTPUT SATURATION CURRENTS AS A FUNCTION OF THRESHOLD VOLTAGE



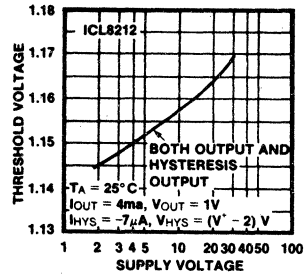
OP03420I

THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF TEMPERATURE



OP03430I

THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF SUPPLY VOLTAGE

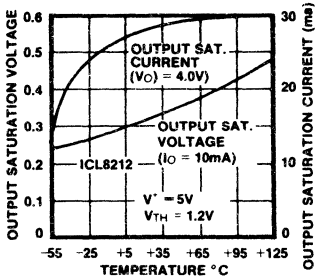


OP03440I

Note: All typical values have been guaranteed by characterization and are not tested.

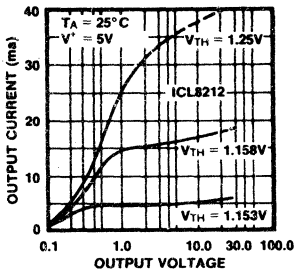
TYPICAL PERFORMANCE CHARACTERISTICS ICL8212 ONLY (CONT.)

OUTPUT SATURATION VOLTAGE AND CURRENT AS A FUNCTION OF TEMPERATURE



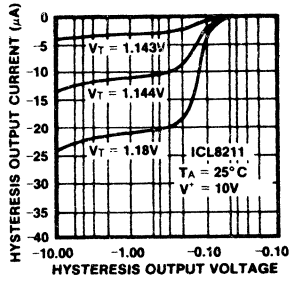
OP03450I

OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



OP03460I

HYSTERESIS OUTPUT CURRENT AS A FUNCTION OF HYSTERESIS OUTPUT VOLTAGE



OP03470I

DETAILED DESCRIPTION

The ICL8211 and ICL8212 use standard linear bipolar integrated circuit technology with high value thin film resistors which define extremely low value currents.

Components Q_1 thru Q_{10} and R_1, R_2 and R_3 set up an accurate voltage reference of 1.15 volts. This reference voltage is close to the value of the bandgap voltage for silicon and is highly stable with respect to both temperature and supply voltage. The deviation from the bandgap voltage is necessary due to the negative temperature coefficient of the thin film resistors (−5000 ppm per °C).

Components Q_2 thru Q_9 and R_2 make up a constant current source; Q_2 and Q_3 are identical and form a current mirror. Q_8 has 7 times the emitter area of Q_9, and due to the current mirror, the collector currents of Q_8 and Q_9 are forced to be equal and it can be shown that the collector current in Q_8 and Q_9 is

$$I_C\ (Q_8 \text{ or } Q_9) = \frac{1}{R_2} \times \frac{kT}{q} \ln 7$$

or approximately 1µA at 25°C

Where k = Boltzman's constant
q = charge on an electron
and T = absolute temperature in °K

Transistors Q_5, Q_6, and Q_7 assure that the V_{CE} of Q_3, Q_4, and Q_9 remain constant with supply voltage variations. This ensures a constant current supply free from variations.

The base current of Q_1 provides sufficient start up current for the constant source; there being two stable states for this type of circuit — either ON as defined above, or OFF if no start up current is provided. Leakage current in the transistors is not sufficient in itself to guarantee reliable startup.

Q_4 is matched to Q_3 and Q_2; Q_{10} is matched to Q_9. Thus the I_C and V_{BE} of Q_{10} are identical to that of Q_9 or Q_8. To generate the bandgap voltage, it is necessary to sum a voltage equal to the base emitter voltage of Q_9 to a voltage proportional to the difference of the base emitter voltages of two transistors Q_8 and Q_9 operating at two current densities.

$$\text{Thus } 1.15 = V_{BE}\ (Q_9 \text{ or } Q_{10}) + \frac{R_3}{R_2} \times \frac{kT}{q} \ln 7$$

which provides $\frac{R_3}{R_2} = 12$ (approx.)

The total supply current consumed by the voltage reference section is approximately 6µA at room temperature. A voltage at the THRESHOLD input is compared to the reference 1.15 volts by the comparator consisting of transistors Q_{11} thru Q_{17}. The outputs from the comparator are limited to two diode drops less than V^+ or approximately 1.1 volts. Thus the base current into the hysteresis output transistor is limited to about 500nA and the collector current of Q_{19} to 100µA.

In the case of the ICL8211, Q_{21} is proportioned to have 70 times the emitter area of Q_{20} thereby limiting the output current to approximately 7mA, whereas for the ICL8212 almost all the collector current of Q_{19} is available for base drive to Q_{21}, resulting in a maximum available collector current of the order of 30mA. It is advisable to externally limit this current to 25mA or less.

APPLICATIONS

The ICL8211 and ICL8212 are similar in many respects, especially with regard to the setup of the input trip conditions and hysteresis circuitry. The following discussion describes both devices, and where differences occur they are clearly noted.

General Information

THRESHOLD INPUT CONSIDERATIONS

Although any voltage between −5V and V^+ may be applied to the THRESHOLD terminal, it is recommended that the THRESHOLD voltage does not exceed about +6 volts since above that voltage the threshold input current increases sharply. Also, prolonged operation above this voltage will lead to degradation of device characteristics.

5

Note: All typical values have been guaranteed by characterization and are not tested.

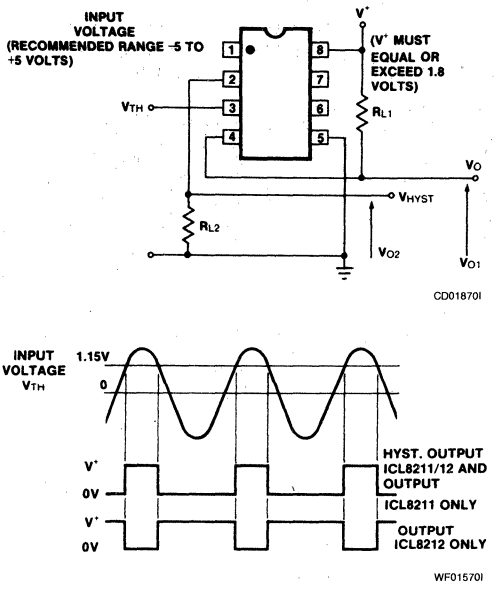


Figure 3: Voltage Level Detection

The outputs change states with an input THRESHOLD voltage of approximately 1.15 volts. Input and output waveforms are shown in Figure 3 for a simple 1.15 volt level detector.

The HYSTERESIS output is a low current output and is intended primarily for input threshold voltage hysteresis applications. If this output is used for other applications it is suggested that output currents be limited to 10μA or less.

The regular OUTPUT's from either the ICL8211 or ICL8212 may be used to drive most of the common logic families such as TTL or C-MOS using a single pullup resistor. There is a guaranteed TTL fanout of 2 for the ICL8211 and 4 for the ICL8212.

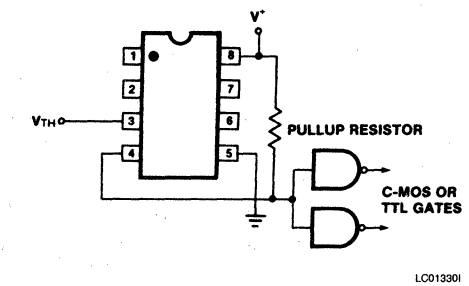


Figure 4: Output Logic Interface

A principal application of the ICL8211 is voltage level detection, and for that reason the OUTPUT current has been limited to typically 7mA to permit direct drive of an LED connected to the positive supply without a series current limiting resistor.

On the other hand the ICL8212 is intended for applications such as programmable zener references, and voltage regulators where output currents well in excess of 7mA are desirable. Therefore, the output of the ICL8212 is not current limited, and if the output is used to drive an LED, a series current limiting resistor must be used.

In most applications an input resistor divider network may be used to generate the 1.15V required for V_{TH}. For high accuracy, currents as large as 50μA may be used, however for those applications where current limiting may be desirable, (such as when operating from a battery) currents as low as 6μA may be considered without a great loss of accuracy. 6μA represents a practical minimum, since it is about this level where the device's own input current becomes a significant percentage of that flowing in the divider network.

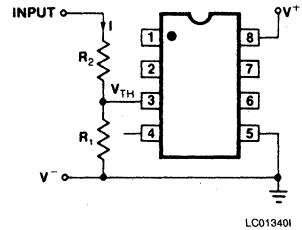


Figure 5: Input Resistor Network Considerations

Case 1. High accuracy required, current in resistor network unimportant Set I = 50μA for V_{TH} = 1.15 volts ∴ $R_1 \rightarrow 20k\Omega$.

Case 2. Good accuracy required, current in resistor network important Set I = 7.5μA for V_{TH} = 1.15 volts ∴ $R_1 \rightarrow 150k\Omega$.

SETUP PROCEDURES FOR VOLTAGE LEVEL DETECTION

Case 1. Simple voltage detection — no hysteresis

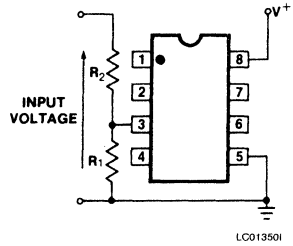
Unless an input voltage of approximately 1.15 volts is to be detected, resistor networks will be used to divide or multiply the unknown voltage to be sensed. Figure 7 shows procedures on how to set up resistor networks to detect INPUT VOLTAGES of any magnitude and polarity.

For supply voltage level detection applications the input resistor network is connected across the supply terminals as shown in Figure 8.

Conditions for correct operation of OUTPUT (terminal #4).

1. ICL8211
   $1.8V \leq V^+ \leq 30V$
2. ICL8212
   $0 \leq V^+ \leq 30V$

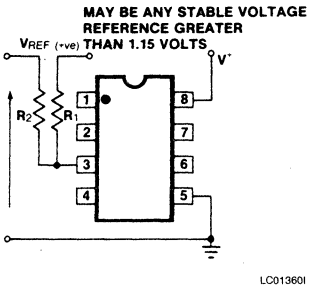
Note: All typical values have been guaranteed by characterization and are not tested.



Input voltage to change the output states

$$= \frac{(R_1 + R_2)}{R_1} \times 1.15 \text{ volts}$$

Figure 6: Range of Input Voltage Greater Than +1.15 Volts



Range of input voltage less than +1.15 volts. Input voltage to change the output states

$$= \frac{(R_1 + R_2) \times 1.15 R_2 V_{REF}}{R_1 \qquad R_1}$$

Figure 7: Input Resistor Network Setup Procedures

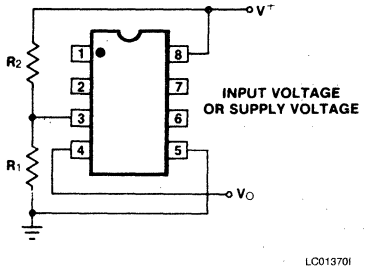


Figure 8: Combined Input and Supply Voltages

Case 2. Use of the HYSTERESIS function

The disadvantage of the simple detection circuits is that there is a small but finite input range where the outputs are neither totally 'ON' nor totally 'OFF'. The principle behind hysteresis is to provide positive feedback to the input trip point such that there is a voltage difference between the input voltage necessary to turn the outputs ON and OFF.

The advantage of hysteresis is especially apparent in electrically noisy environments where simple but positive voltage detection is required. Hysteresis circuitry, however, is not limited to applications requiring better noise performance but may be expanded into highly complex systems with multiple voltage level detection and memory applications — refer to specific applications section.

There are two simple methods to apply hysteresis to a circuit for use in supply voltage level detection. These are shown in Figure 9.

The circuit (a) of Figure 9 requires that the full current flowing in the resistor network be sourced by the HYSTERESIS output, whereas for circuit (b) the current to be sourced by the HYSTERESIS output will be a function of the ratio of the two trip points and their values. For low values of hysteresis, circuit (b) is to be preferred due to the offset voltage of the hysteresis output transistor.

A third way to obtain hysteresis (ICL8211 only) is to connect a resistor between the OUTPUT and the THRESHOLD terminals thereby reducing the total external resistance between the THRESHOLD and GROUND when the OUTPUT is switched on.

Practical Applications

a) Low Voltage Battery Indicator

This application is particularly suitable for portable or remote operated equipment which requires an indication of a depleted or discharged battery. The quiescent current taken by the system will be typically 35μA which will increase to 7mA when the lamp is turned on. R_3 will provide hysteresis if required.

b) |Non-Volatile| Low Voltage Detector

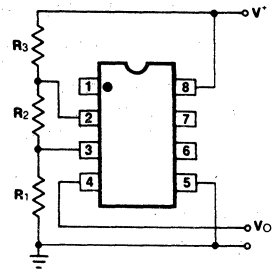
In this application the high trip voltage V_{TR2} is set to be above the normal supply voltage range. On power up the initial condition is A. On momentarily closing switch S_1 the operating point changes to B and will remain at B until the supply voltage drops below V_{TR1}, at which time the output will revert to condition A. Note that state A is always retained if the supply voltage is reduced below V_{TR1} (even to zero volts) and then raised back to V_{NOM}.

c) (Non-volatile) Power Supply Malfunction Recorder

In many systems a transient or an extended abnormal (or absence of a) supply voltage will cause a system failure. This failure may take the form of information lost in a volatile semiconductor memory stack, a loss of time in a timer or even possible irreversible damage to components if a supply voltage exceeds a certain value.

It is, therefore, necessary to be able to detect and store the fact that an **out-of-operating range** supply voltage condition has occurred, even in the case where a supply voltage may have dropped to zero. Upon power up to the normal operating voltage this record must have been retained and easily interrogated. This could be important in the case of a transient power failure due to a faulty component or intermittent power supply, open circuit, etc., where direct observation of the failure is difficult.

Note: All typical values have been guaranteed by characterization and are not tested.



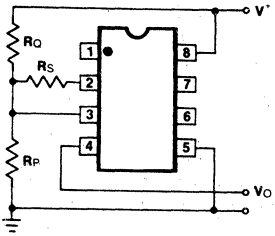
LC01380I

Low trip voltage

$$V_{TR1} = \left[\frac{(R_1 + R_2 \times 1.15}{R_1)} + 0.1\right] \text{volts}$$

High trip voltage

$$V_{TR2} = \frac{(R_1 + R_2 + R_3)}{R_1} \times 1.15 \text{ volts}$$



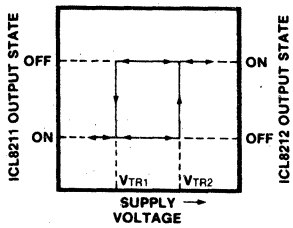
LC01400I

Low trip voltage

$$V_{TR1} = \left[\frac{R_Q R_S}{(R_Q + R_S)} + RP\right] \times \frac{1}{R_P} \times 1.15 \text{ volts}$$

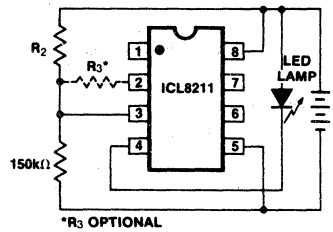
High trip voltage

$$V_{TR2} = \frac{(R_P + R_Q)}{R_P} \times 1.15 \text{ volts}$$

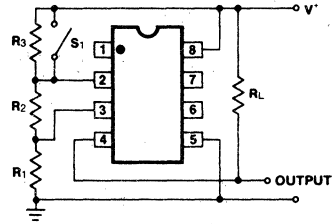


SC00620I

Figure 9: Two alternative voltage detection circuits employing hysteresis to provide pairs of well defined trip voltages.

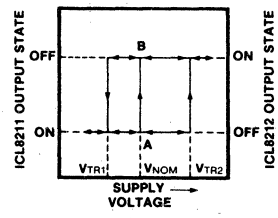


LC01390I



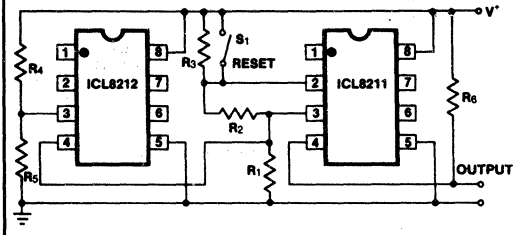
LC01410I

Figure 10: Low Voltage Battery Indicator



SC00630I

Figure 11: Low Voltage Detector and Memory



DS01980I

Figure 12: Schematic of Recorder

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8211/ICL8212

A simple circuit to record an out of range voltage excursion may be constructed using an ICL8211, an ICL8212 plus a few resistors. This circuit will operate to 30 volts without exceeding the maximum ratings of the I.C.'s. The two voltage limits defining the in range supply voltage may be set to any value between 2.0 and 30 volts.

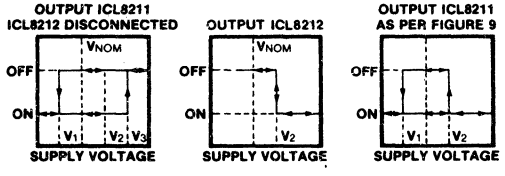


Figure 13: Output States of the ICL8211 and ICL8212 as a Function of the Supply Voltage

Referring to Figure 12, the ICL8212 is used to detect a voltage, V_2, which is the upper voltage limit to the operating voltage range. The ICL8211 detects the lower voltage limit of the operating voltage range, V_1. Hysteresis is used with the ICL8211 so that the output can be stable in either state over the operating voltage range V_1 to V_2 by making V_3 — the upper trip point of the ICL8211 much higher in voltage than V_2.

The output of the ICL8212 is used to force the output of the ICL8211 into the ON state above V_2. Thus there is no value of the supply voltage that will result in the output of the ICL8211 changing from the ON state to the OFF state. This may be achieved only by shorting out R_3 for values of supply voltage between V_1 and V_2.

d) Constant Current Sources

The ICL8212 may be used as a constant current source of value of approximately 25μA by connecting the THRESHOLD terminal to GROUND. Similarly the ICL8211 will provide a 130μA constant current source. The equivalent parallel resistance is in the tens of megohms over the supply voltage range of 2 to 30 volts. These constant current sources may be used to provide biasing for various circuitry including differential amplifiers and comparators. See Typical Operating Characteristics for complete information.

e) Zener or Precision Voltage Reference

The ICL8212 may be used to simulate a zener diode by connecting the OUTPUT terminal to the V_Z output and using a resistor network connected to the THRESHOLD terminal to program the zener voltage

$$(V_{zener} = \frac{(R_1 + R_2)}{R_1} \times 1.15 \text{ volts}).$$

Since there is no internal compensation in the ICL8212 it is necessary to use a large capacitor across the output to prevent oscillation.

Zener voltages from 2 to 30 volts may be programmed and typical impedance values between 300μA and 25mA will range from 4 to 7Ω. The knee is sharper and occurs at a significantly lower current than other similar devices available.

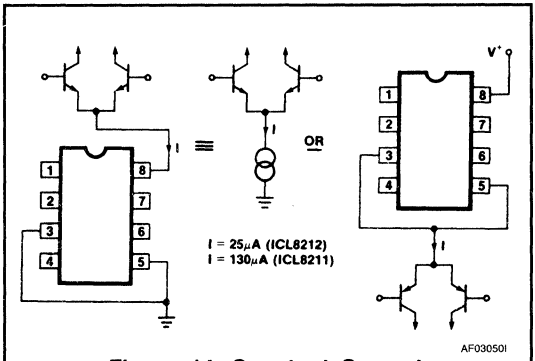


Figure 14: Constant Current Source Applications

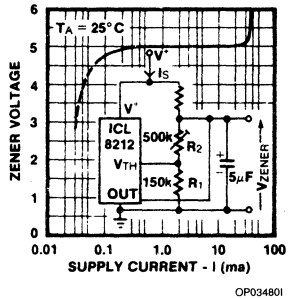


Figure 15: Programmable Zener or Voltage Reference

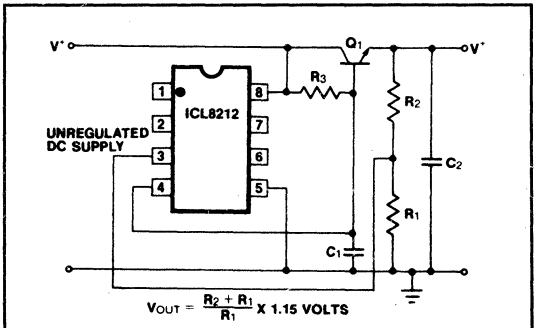


Figure 16: Simple Voltage Regulator

f) Precision Voltage Regulators

The ICL8212 may be used as the controller for a highly stable series voltage regulator. The output voltage is simply programmed, using a resistor divider network R_1 and R_2. Two capacitors C_1 and C_2 are required to ensure stability since the ICL8212 is uncompensated internally.

Note: All typical values have been guaranteed by characterization and are not tested.

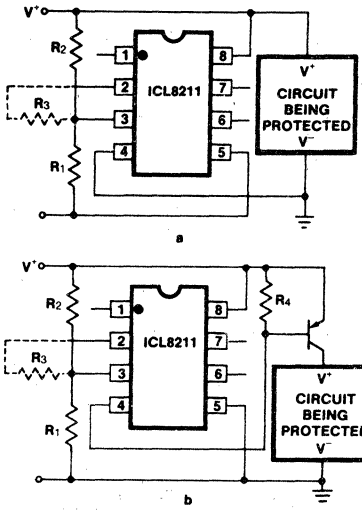


Figure 17: High Voltage Dump Circuits

This regulator may be used with lower input voltages than most other commercially available regulators and also consumes less power for a given output control current than any commercial regulator. Applications would therefore include battery operated equipment especially those operating at low voltages.

g) High supply voltage dump circuit

In many circuit applications it is desirable to remove the power supply in the case of high voltage overload. For circuits consuming less than 5mA this may be achieved using an ICL8211 driving the load directly. For higher load currents it is necessary to use an external pnp transistor or darlington pair driven by the output of the ICL8211. Resistors R_1 and R_2 set up the disconnect voltage and R_3 provides optional voltage hysteresis if so desired.

h) Frequency limit detectors

Simple frequency limit detectors providing a GO/NO-GO output for use with varying amplitude input signals may be conveniently implemented with the ICL8211/8212. In the application shown, the first ICL8212 is used as a zero crossing detector. The output circuit consisting of R_3, R_4 and C_2 results in a slow output positive ramp. The negative range is much faster than the positive range. R_5 and R_6 provide hysteresis so that under all circumstances the second ICL8212 is turned on for sufficient time to discharge C_3. The time constant of R_7 C_3 is much greater than R_4 C_2. Depending upon the desired output polarities for low and high input frequencies, either an ICL8211 or an ICL8212 may be used as the output driver.

This circuit is sensitive to supply voltage variations and should be used with a stabilized power supply. At very low frequencies the output will switch at the input frequency.

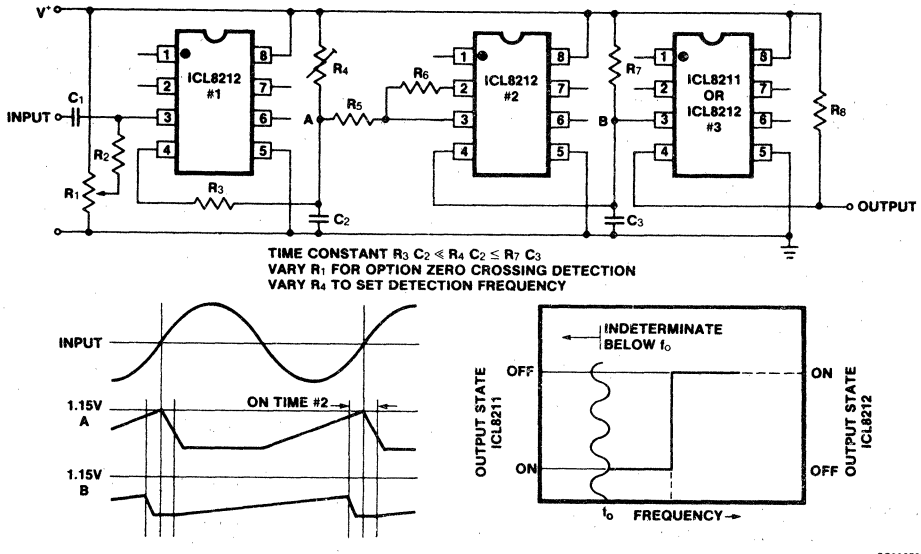


Figure 18: Frequency Limit Detector

Note: All typical values have been guaranteed by characterization and are not tested.

i) Switch bounce filter

Single pole single throw (SPST) switches are less costly and more available than single pole double throw (SPDT) switches. SPST switches range from push button and slide types to calculator keyboards. A major problem with the use of switches is the mechanical bounce of the electrical contacts on closure. Contact bounce times can range from a fraction of a millisecond to several tens of milliseconds depending upon the switch type. During this contact bounce time the switch may make and break contact several times. The circuit shown in Figure 19 provides a rapid charge up of C_1 to close to the positive supply voltage (V^+) on a switch closure and a corresponding slow discharge of C_1 on a switch break. By proportioning the time constant of R_1 C_1 to approximately the manufacturer's bounce time the output as terminal #4 of the ICL8211/8212 will be a single transition of state per desired switch closure.

j) Low voltage power disconnector

There are some classes of circuits that require the power supply to be disconnected if the power supply voltage falls below a certain value. As an example, the National LM199 precision reference has an on chip heater which malfunctions with supply voltages below 9 volts causing an excessive device temperature. The ICL8212 may be used to detect a power supply voltage of 9 volts and turn the power supply off to the LM199 heater section below that voltage.

For further applications, see A027 "Power Supply Design using the ICL8211 and ICL8212" by D. Watson.

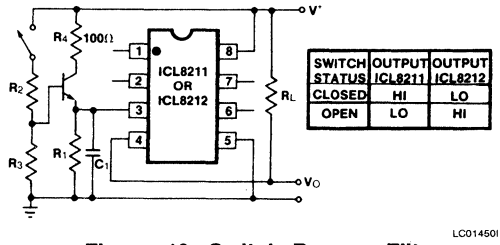


Figure 19: Switch Bounce Filter

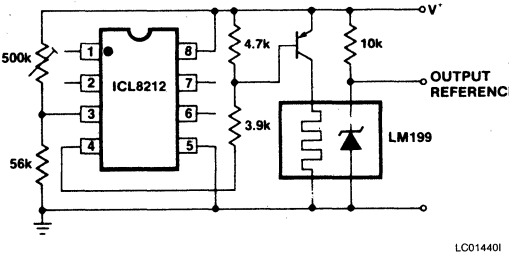


Figure 20: Low Voltage Power Supply Disconnect

5

Note: All typical values have been guaranteed by characterization and are not tested.

IH5110—IH5115
General Purpose Sample & Hold

INTERSIL

GENERAL DESCRIPTION

Each of the 5110 family is a complete Sample and Hold circuit, (except for sampling capacitor) including input buffer amplifier, output buffer amplifier and CMOS switching logic. The devices are designed to operate from ±15V and +5V supplies. The input logic is designed to "Sample" and "Hold" from standard TTL logic levels.

The design is such that the input and output buffering is performed with only one operational amplifier, by switching the sampling capacitor from the output back to input. Switches Q_1, Q_2, and Q_3 (see Figure 1) accomplish this switching. In the sampling mode Q_1 and Q_3 are shorted and Q_2 is open; thus the op. amp. charges up the sampling capacitor. In the hold mode Q_1 and Q_3 are open and Q_2 is shorted; thus the sampling cap. is switched back to the noninverting input of the op. amp.

This structure provides a very accurate d.c. gain of 1 with very fast settling times (i.e. 5μs). Additionally the design has internal feedback to cancel charge injection effects (sample to hold offsets). Q_1 and Q_2 are driven 180 degrees out of phase to accomplish this charge nulling.

FEATURES

- **Low Cost**
- **Military and Industrial Temperature Ranges**
- **±10V Input Voltage Range**
- **0.5mV/Sec Drift Typical @ C_S = 0.01μF**
- **TTL and CMOS Compatible**
- **Short Circuit Protected**
- **Input Offset Voltage Adjustable to < 100μV Using A 20kΩ Potentiometer**
- **0.1% Guaranteed Sample Accuracy With 10V Signals and C_S = 0.01μF**
- **Sample to Hold Offset Is 5mV Max**

ORDERING INFORMATION

IH5110 M JE

- JE = Package: 16 pin CERDIP
- DE = Package: 16 pin ceramic DIP (special order only)
- M = Temperature Range: Military (−55°C to +125°C)
- I = Temperature Range: Industrial (−20°C to +85°C)
- IH5110 = Basic Part Number

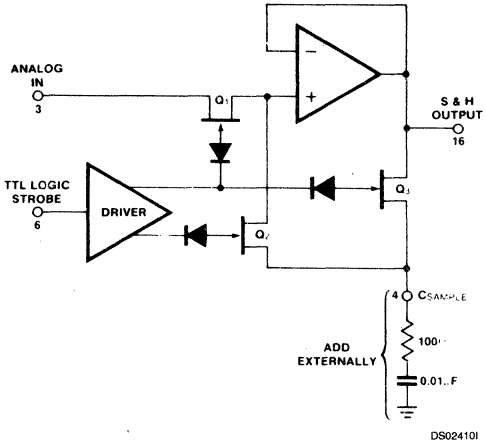


Figure 1: Functional Diagram

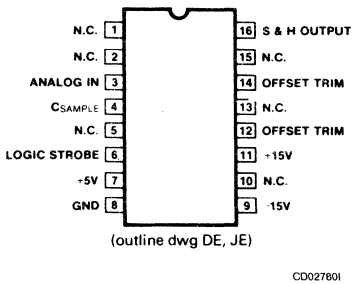


Figure 2: Pin Configuration

-002

Note: All typical values have been guaranteed by characterization and are not tested.

IH5110—IH5115

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltages ..... ±16V
Power Dissipation 500mW
Operating Temperature ..... −25°C to 85°C
−55°C to 125°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Pin 7 = 5V, Pin 8 = GND, Pin 9 = −15V, Pin 11 = 15V) Note 3

SYMBOL	CHARACTERISTIC	IH5110, 5112, 5114			IH5111, 5113, 5115			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Close	Aperture Time		120			200		ns
$t_{acq.}$	Acquisition Time for Max Analog Voltage Step C_S = 0.1μF (0.1% Accur.) C_S = 0.01μF (0.1% Accur.) C_S = 0.001μF (0.1% Accur.) See Figure 5		 25 4 4	 35 6 6		 25 4 4	 35 6 6	μs
V_{drift}	Drift Rate C_S = 0.1μF C_S = 0.01μF C_S = 0.001μF See Figure 3		 0.3 0.5 2.0	 2.5 5 10		 0.3 0.5 2.0	 2.5 5 10	mV/s
V_{inject}	Charge Injection or Sample to Hold Offsets C_S = 0.1μF C_S = 0.01μF C_S = 0.001μF See Note 1 & Figure 4		 < 1 < 1 12	 5 5 25		 < 1 < 1 12	 5 5 25	mVp-p
V_{switch}	Switching Transients or Spikes (Duration Less than 2μs) C_S = 0.1μF C_S = 0.01μF C_S = 0.001μF See Figure 4		 0.1 0.1 0.2	 0.5 0.5 0.5		 0.1 0.1 0.2	 0.5 0.5 0.5	V
V_{couple}	A. C. Feedthrough Coupled to Output		5			5		mVp-p
V_{offset}	D.C. Offset When in Sample Mode Trimmable to 0m V With Ext. 20kΩ Potentiometer 5110 5111			40			40	mV
	5112 5113			10			10	
	See Figure 3 5114 5115			5			5	
R_{in}	Input Impedance in Hold or Sample Mode (f ≤ 10Hz)		100			100		MΩ
$I_{\pm 15V}$	Plus or Minus 15V Supply Quiescent Current		3.4	6		3.4	6	mA
i_{5V}	5V Supply Quiescent Current		0.3	10		0.3	10	A
V_{analog}	D.C. Input Voltage Range			±7.5			±10	
ΔV_{IN}	A.C. Input Voltage Range See Note 2 & Figure 6	15			20			V
I_{strobe}	TTL Logic Strobe Input Current in Either Hold or Sample Mode		0.1	10		0.1	10	μA

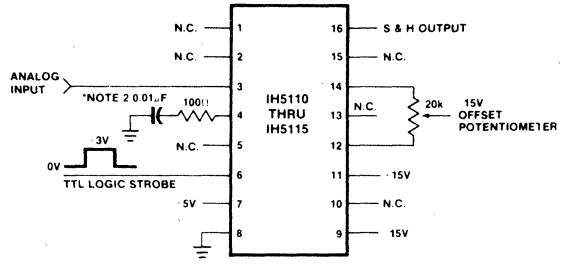
NOTES: 1. Offset voltage of op. amp. must be adjusted to 0mV (using 20kΩ potentiometer) before charge injection is measured.
2. The A.C. input voltage range differs from the D.C. input voltage range. All versions will handle any analog input within the range of plus 10V to minus 10V; however the IH5110, 5112, 5114 has the added restriction that the peak to peak swing should be less than 15Vp-p i.e. ±7.5 Vac.
3. All of the electrical characteristics specs, are guaranteed with C_S = 0.01μF in series with 100Ω as per Figure 3, C_S = 0.1μF & C_S = 0.001μF are for design aid only.
4. If supplies are reduced to ±12VDC, analog signal range will be reduced to ±7Vp-p.

Note: All typical values have been guaranteed by characterization and are not tested.

IH5110—IH5115

INTERSIL

APPLICATIONS INFORMATION



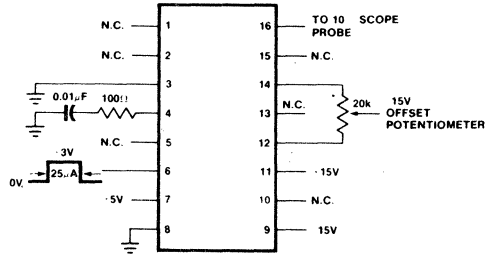
NOTES: 1. To trim output offset to 0mV, set strobe input to sample mode (3V), set analog input to GND, adjust potentiometer until S & H output is 0mV.

2. Use a low dielectric absorption capacitor such as polystyrene.

SAMPLE MODE occurs when logic input is greater than 2.4V.

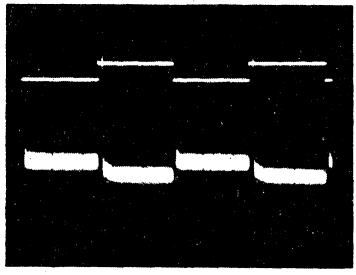
HOLD MODE occurs when logic input is less than 0.8V.

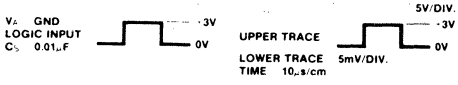
Figure 3: Typical Connection Diagram



Adjust offset to 0mV before testing for charge injection. See note 1.

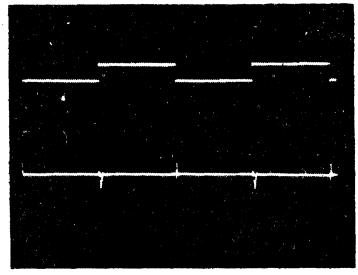
CHARGE INJECTION

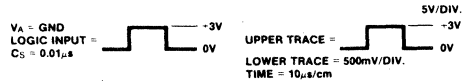




WF01620I

SWITCHING TRANSIENTS

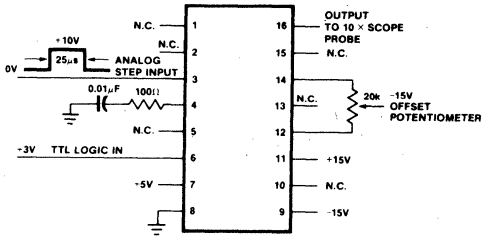


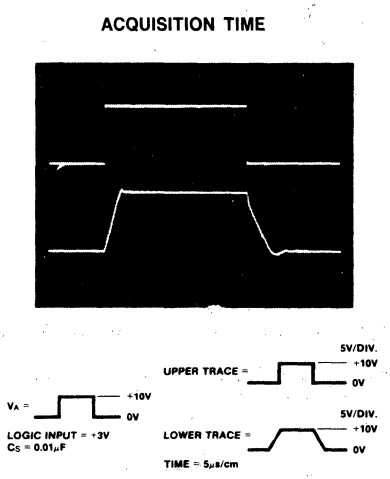


WF01630I

Figure 4: Charge Injection (sample to hold offset) Measurement Circuit; also Switching Transients Test Circuit

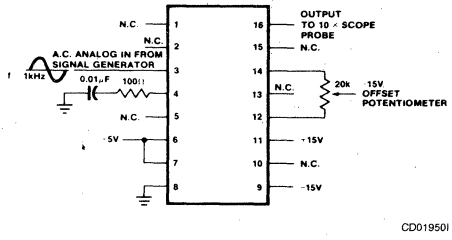
Note: All typical values have been guaranteed by characterization and are not tested.





NOTE: The acquisition time is actually a settling time spec. since the reading is only taken when the output has settled within 1% of its final value. The 6μs spec. (IH5111, 5113 & 5115 is the worst reading of the t_{on} or t_{off} settling time shown above. The above test can be performed with a 0 to +7.5V or 0 to −7.5V step for the IH5110, 5112, 5114.

Figure 5: Typical Circuit for Measurement of A.C. Signal Handling Capability



To test this parameter, increase the amplitude of the signal generator until the output starts to distort (it will always show up on the positive excursion of the sine wave first); then back off until all distortion is gone. The resultant peak to peak swing must be greater than 15Vpp for the IH5110, 5112, 5114 and greater than 20Vpp for the IH5111, 5113, 5115.

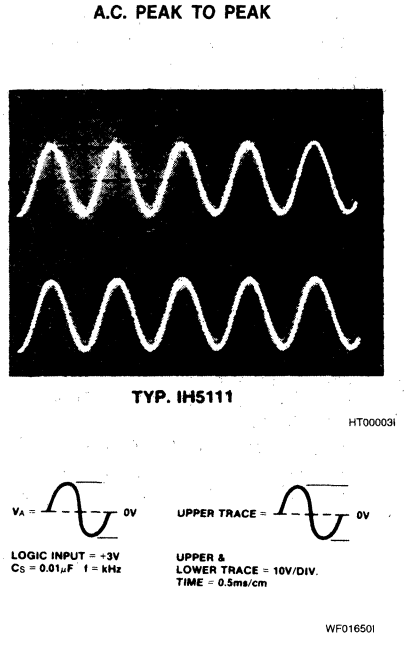


Figure 6: Typical Circuit for Measurement of A.C. Peak to Peak Signal Handling Capability

5

Note: All typical values have been guaranteed by characterization and are not tested.

IH5110—IH5115

APPLICATION TIPS

The following text serves as a guide in choosing the correct device from the IH5110 family.

First, determine the input voltage range.

The even numbered parts are designed to switch smaller A.C. signal amplitudes with the goal being to minimize the charge injection effects (sample to hold offsets). This charge injection error is shown in Figure 4. Once the voltage offset is zeroed, the 5110 has typical error amplitudes of 1 to 2mVp-p (corresponds to 10pc to 20pc of charge). Thus one could sample very low level d.c. signals with extreme accuracy. If very low level A.C. signals are being sampled, voltage offset potentiometer can be adjusted for a zero charge injection effect. Once the potentiometer has been adjusted, there will be a zero error going from sample to hold; however there will be a d.c. error caused by adjusting the potentiometer for zero charge injection and not for zero voltage offset. In general, this d.c. error will be in the area of 2mV to 5mV.

The odd numbered parts are primarily designed to handle any input in the plus or minus 10V range, regardless of whether it is A.C. or D.C.; to obtain this, the charge injection is about a factor of 2 higher than the even numbered parts.

The use of Varafet switching elements similar to Intersil's IH401/401A leads to a trade-off between AC signal swing and charge injection.

After the voltage range and charge injection requirements have been determined, all that remains is to determine the input offset voltage the system can tolerate. By using the higher numbered parts, it is possible to eliminate the offset potentiometer if system accuracy will allow 5mV (5114, 5115) or 10mV (5112, 5113) due to the low input offset voltage on these devices.

The drift rate is specified at 10mV/sec. Max. for all models: this corresponds to approximately 100pA total leakage into a 0.01μF sampling capacitor (C_S). While the 10mV/sec. is the Max. encountered, a more typical reading is less than 1mV/sec. (true for any input between −10V and +10V); thus the IH5110 family is ideal for applications requiring very low drift or droop rates.

The aperture time is spec'd at 200ns Max. for all models, but a more typical value is 150ns; this is basically the off time of switch Q_1. The way this aperture time affects system accuracy is shown below:

Assume the input signal to the Sample and Hold is an A.C. signal of peak amplitude A (peak to peak swing is 2A) and frequency $2\pi f = \omega$, then $V_{input} = Ae^{j\omega t}$ and $dV/dt = jA\omega e^{j\omega t}$. This means the slope of input signal = (dV/dt) is a maximum at t (time) = 0. This maximum value is ωA (in amplitude). (i.e.) input frequency is 10kHz, therefore $dV/dt = \omega A = 6.28 \times 10^4 \times 10V = 6.3 \times 10^5 V/sec.$ A = 10V, then slope or dV/dt = 0.63V/μs. Now if we wish error to be a Max. of say 1% of full scale 10V, we see that 100mV (1%/ aperture time = 0.63V/μs. Solving this equation we see that aperture time must be 160ns or less to get 1% holding accuracy. Since our aperture time is 150ns typical, we have 1% accuracy in holding 10kHz varying signals; for signal frequencies 1kHz and less, Max. error is 0.1%. The simple interpretation of just how the off time of the switch causes this system error is due to the fact a finite time is required for the switch to react to a hold command; this reaction time manifests itself with a system voltage error because the time varying input signal is changing to a new value before the switch has actually turned off. (i.e.) in the above example off = 10kHz and A = 10V, suppose we gave the hold command (thru TTL logic) at t = 0 (A.C. signal goes thru zero pt.) At this point we have calculated the slope to be a Max. and equal to 0.63V/μs. If there were no aperture time error, we would read 0V at output of Sample and Hold; however because of finite time for switch to respond to hold command, 150ns passes before switch goes off. During this 150ns, the input signal has gone to 100mV above or below 0V, thus the stored value of signal will be 100mV and that is the reading at the output of the Sample and Hold. If the input frequency were 1kHz, the "error voltage" would be 10mV.

DEFINITION OF TERMS

Aperture Time: The time it takes to switch from sample mode to hold mode and the actual opening of switch.

Charge Injection: The amount of charge coupled across the switch with no input voltage.

Drift Rate: The amount of drift of output voltage at a rate caused by current flow through the storage capacitor.

$$\left(\frac{dV}{dt} = \frac{i}{c}\right)$$

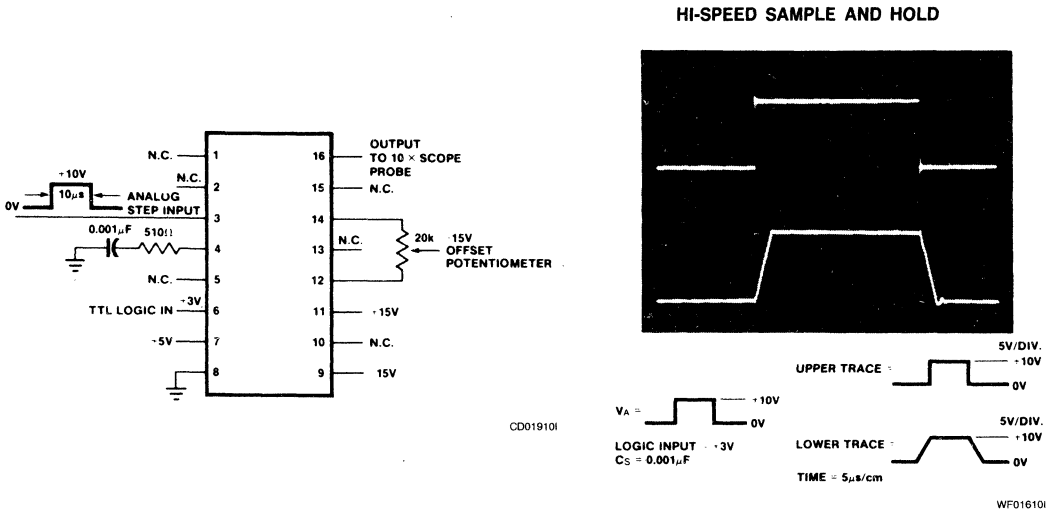
This current is the leakage across the switch and the amplifier's bias current.

Feed Through: The amount of input signal that appears at the output when in the hold mode. Normally caused by capacitance across the switch.

Offset Voltage: Voltage measured at output with no input voltage and circuit in sample mode.

Acquisition Time: The time it takes amplifier to reach full scale output either plus or minus.

Note: All typical values have been guaranteed by characterization and are not tested.



NOTE: Typical times for the Sample and Hold to acquire the input are 2μs for turn on (output) goes to + 10V and 3μs for turn off (output goes down to 0V). As a general note, all the electrical specifications are guaranteed with a sampling capacitor equal to 0.01μf. As the above application (Fig. 6) shows, other values of sampling capacitors can be used but the best combinations of S & H specs may not result with values other than 0.01μF. The only advantage of using a 0.001μF for C_S is the acquisition time is 2μs typical instead of 5μs typical (with 0.01μF; however the drift rate would be worse and charge injection would be affected). To minimize drift rate, use a 0.1μF capacitor; this should produce a 0.1mV/sec rate of change and a charge injection amplitude of 0.2mVp-p. Of course the acquisition time will be slowed down to the 25μs area. Also use a 0.1μs system for slow speed changes (i.e., input frequency is less than 1kHz. The series resistor should be about 100Ω – 200Ω to stabilize the system.

Figure 7: Connection For Hi-Speed Sample and Hold With Following Typical Performance: $W/C_S = 0.001$

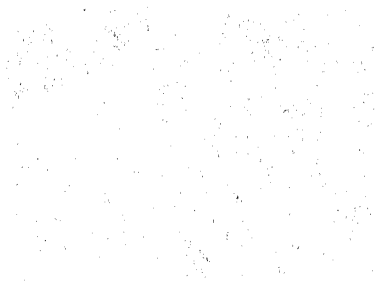
a. 2μs settling time (acquisition time) to 1% accuracy

b. 25mV charge injection amplitude

c. 10mV/sec drift rate

5

Note: All typical values have been guaranteed by characterization and are not tested.



Section 6 — Data Acquisition

AD7520/AD7530
AD7521/AD7531
10/12-Bit Multiplying D/A Converters

GENERAL DESCRIPTION

The AD7520/AD7530 and AD7521/AD7531 are monolithic, high accuracy, low cost 10-bit and 12-bit resolution, multiplying digital-to-analog converters (DAC). Intersil's thin-film on CMOS processing gives up to 10-bit accuracy with TTL/CMOS compatible operation. Digital inputs are fully protected against static discharge by diodes to ground and positive supply.

Typical applications include digital/analog interfacing, multiplication and division, programmable power supplies, CRT character generation, digitally controlled gain circuits, integrators and attenuators, etc.

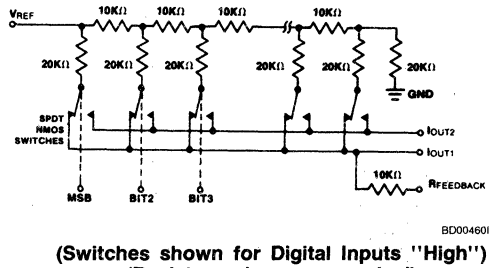
The AD7530 and AD7531 are identical to the AD7520 and AD7521, respectively, with the exception of output leakage current and feedthrough specifications.

FEATURES

- **AD7520/AD7530: 10 Bit Resolution; 8, 9 and 10 Bit Linearity**
- **AD7521/AD7531: 12 Bit Resolution; 8, 9 and 10 Bit Linearity**
- **Low Power Dissipation: 20mW (Max)**
- **Low Nonlinearity Tempco: 2 ppm of FSR/°C**
- **Current Settling Time: 500ns to 0.05% of FSR**
- **Supply Voltage Range: +5V to +15V**
- **TTL/CMOS Compatible**
- **Full Input Static Protection**
- **/883B Processed Versions Available**

ORDERING INFORMATION

NONLINEARITY	PART NUMBER/PACKAGE		
	PLASTIC DIP	CERDIP	CERDIP
0.2% (8-Bit)	AD75I20JN AD7530JN AD7521JN AD7531JN	AD7520JD AD7530JD AD7521JD AD7521JD	AD7520SD AD7521SD
0.1% (9-Bit)	AD7520KN AD7530KN AD7521KN AD7531KD	AD7520KD AD7530KD AD7521KD AD7531KD	AD7520TD AD7521TD
0.05% (10-Bit)	AD7520LN AD7530LN AD7521LN AD7531LN	AD7520LD AD7530LD AD7521LD AD7531LD	AD7520UD AD7521UD
TEMPERATURE RANGE	0°C to +70°C	−25°C to +85°C	−55°C to +125°C



(Switches shown for Digital Inputs "High")
(Resistor values are nominal)

Figure 1: Functional Diagram

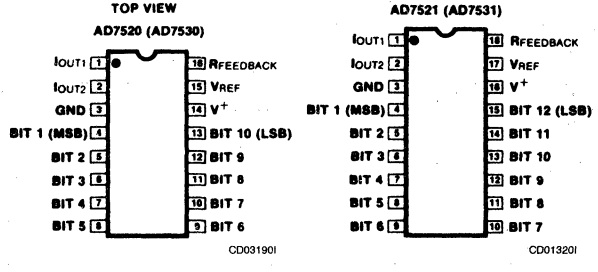


Figure 2: Pin Configurations

300105-002

Note: All typical values have been guaranteed by characterization and are not tested.

AD7520/7530/7521/7531

INTERSIL

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Supply Voltage (V^+) ..... +17V
V_{REF} ..... ±25V
Digital Input Voltage Range ..... V^+ to GND
Output Voltage Compliance ..... −100mV to V^+
Power Dissipation (package)
up to +75°C 450mW
derate above +75°C @ ..... 6mW/°C

Operating Temperature
JN, KN, LN Versions ..... 0°C to +70°C
JD, KD, LD Versions ..... −25°C to 85°C
SD, TD, UD Versions ..... −55°C to +125°C
Storage Temperature ..... −65°C to 150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

CAUTION:
1) The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
2) Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and $R_{FEEDBACK}$.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V^+ = +15V, V_{REF} = +10V, T_A = 25°C unless otherwise specified)

PARAMETER		TEST CONDITIONS		AD7520 (AD7530)	AD7521 (AD7531)	UNIT	LIMIT
DC ACCURACY (Note 1)							
Resolution				10	12	Bits	
Nonlinearity (Note 2)	VERSION J, S	S, T, U: over −55°C to +125°C	Fig. 3	0.2 (8-Bit)		% of FSR	Max
	VERSION K, T		Fig. 3	0.1 (9-Bit)		% of FSR	Max
	VERSION L, U	−10V ≤ V_{REF} ≤ +10V	Fig. 3	0.05 (10-Bit)		% of FSR	Max
Nonlinearity Tempco (Notes 2 and 3)				2		ppm of FSR/°C	Max
Gain Error (Note 2)		−10V ≤ V_{REF} ≤ +10V		0.3		% of FSR	Typ
Gain Error Tempco (Notes 2 and 3)				10		ppm of FSR/°C	Max
Output Leakage Current (either output)		Over the specified temperature range		200 (300)		nA	Max
Power Supply Rejection (Note 2)			Fig. 4	±0.005		% of FSR/%	Typ
AC ACCURACY (Note 3)							
Output Current Settling Time		To 0.05% of FSR (All digital inputs low to high and high to low)	Fig. 8	500		ns	Typ
Feedthrough Error		V_{REF} = 20V pp, 100kHz (50kHz) All digital inputs low	Fig. 7	10		mV pp	Max
REFERENCE INPUT							
Input Resistance		All digital inputs high I_{OUT1} at ground.		5k 10k 20k		Ω	Min Typ Max
ANALOG OUTPUT							
Voltage Compliance (both outputs)		(Note 3)		See absolute max. ratings			
Output Capacitance (Note 3)	I_{OUT1} I_{OUT2}	All digital inputs high	Fig. 6	120 37		pF pF	Typ Typ
	I_{OUT1} I_{OUT2}	All digital inputs low	Fig. 6	37 120		pF pF	Typ Typ
Output Noise (both outputs) (Note 3)			Fig. 5	Equivalent to 10kΩ Johnson noise			Typ
DIGITAL INPUTS							
Low State Threshold		Over the specified temp range		0.8		V	Max
High State Threshold				2.4		V	Min
Input Current (low to high state)				1		μA	Typ
Input Coding		See Tables 1 & 2		Binary/Offset Binary			

Note: All typical values have been guaranteed by characterization and are not tested.

AD7520/7530/7521/7531

ELECTRICAL CHARACTERISTICS (CONT.)

PARAMETER	TEST CONDITIONS		AD7520 (AD7530)	AD7521 (AD7531)	UNIT	LIMIT
POWER REQUIREMENTS						
Power Supply Voltage Range			+5 to +15		V	
I^+	All digital inputs at 0V or V^+		1		μA	Typ
	All digital inputs high or low		2		mA	Max
Total Power Dissipation (Including the ladder network)			20		mW	Typ

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design, not subject to test.
4. Accuracy not guaranteed unless outputs at GND potential.

TEST CIRCUITS NOTE: The following test circuits apply for the AD7520. Similar circuits are used for the AD7530, AD7521 and AD7531.

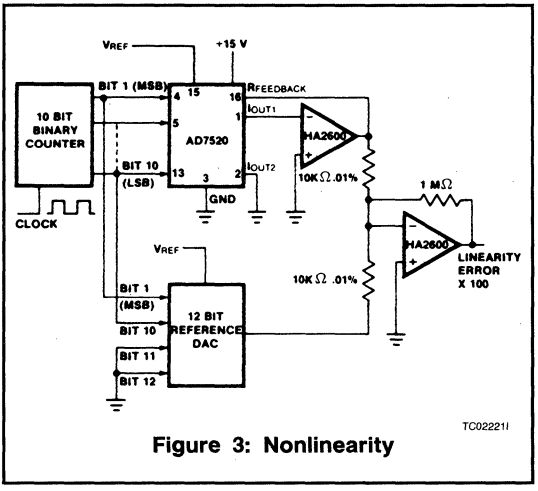


Figure 3: Nonlinearity

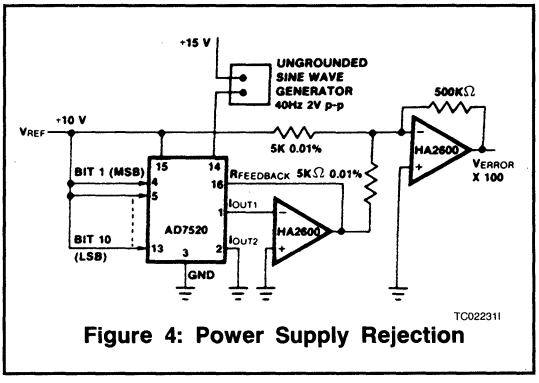


Figure 4: Power Supply Rejection

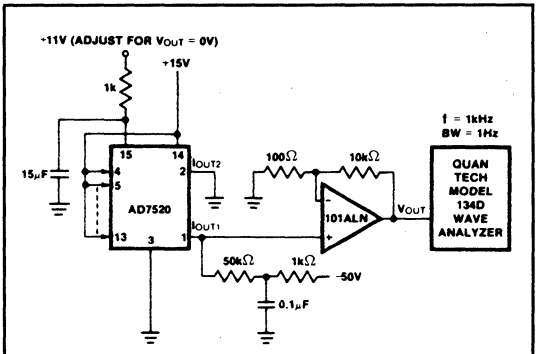


Figure 5: Noise

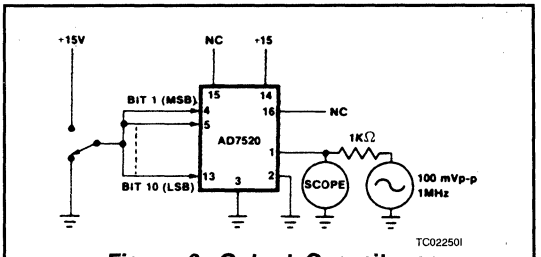


Figure 6: Output Capacitance

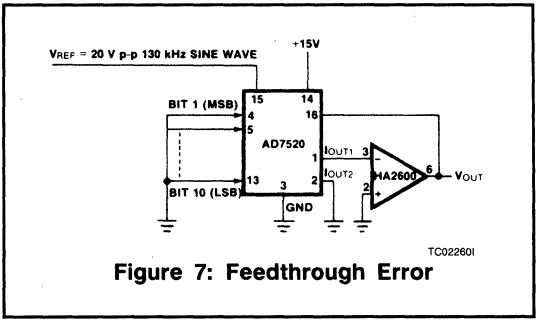


Figure 7: Feedthrough Error

Note: All typical values have been guaranteed by characterization and are not tested.

AD7520/7530/7521/7531

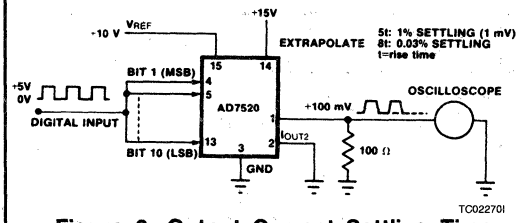


Figure 8: Output Current Settling Time

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

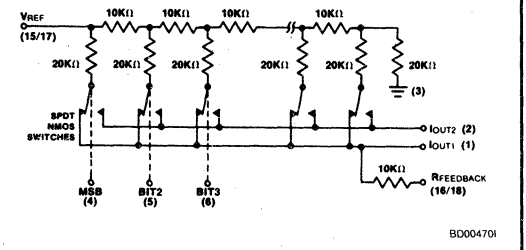
OUTPUT CAPACITANCE: Capacitance from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

DETAILED DESCRIPTION

The AD7520 (AD7530) and AD7521 (AD7531) are monolithic, multiplying D/A converters. A highly stable thin film R-2R resistor ladder network and NMOS SPDT switches form the basis of the converter circuit, CMOS level shifters permit low power TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in Figure 9. The NMOS SPDT switches steer the ladder leg currents between I_{OUT1} and I_{OUT2} buses which must be held either at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.



(Switches shown for Digital Inputs "High")

Figure 9: 7520/7521 Functional Diagram

Converter errors are further reduced by using separate metal interconnections between the major bits and the outputs. Use of high threshold switches reduces the offset (leakage) errors to a negligible level.

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first, (Figure 10). This configuration results in TTL/CMOS compatible operation over the full military temperature range. With the ladder SPDT switches driven by the level shifter, each switch is binarily weighted for an ON resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors and highly accurate leg currents.

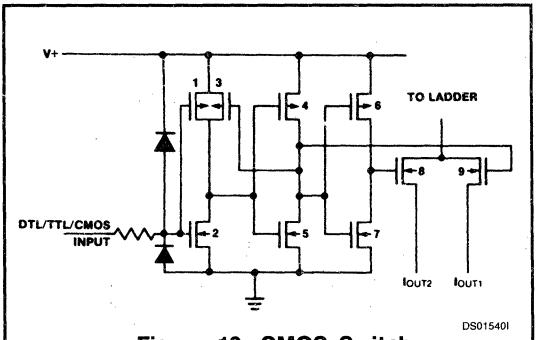


Figure 10: CMOS Switch

Note: All typical values have been guaranteed by characterization and are not tested.

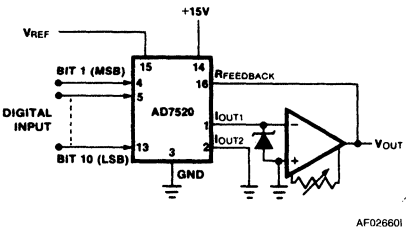


Figure 11: Unipolar Binary Operation (2-Quadrant Multiplication)

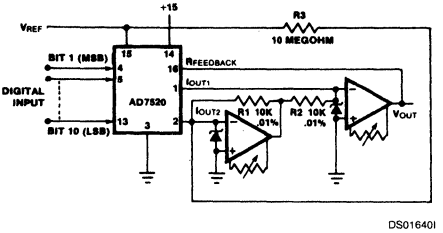


Figure 12: Bipolar Operation (4-Quadant Multiplication)

TABLE 1
CODE TABLE — UNIPOLAR BINARY OPERATION

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}\ (1-2^{-n})$
1000000001	$-V_{REF}\ (1/2+2^{-n})$
1000000000	$-V_{REF}/2$
0111111111	$-V_{REF}\ (1/2-2^{-n})$
0000000001	$-V_{REF}\ (2^{-n})$
0000000000	0

NOTE: 1. $LSB = 2^{-n}\ V_{REF}$ 2. n = 10 for 7520, 7530
n = 12 for 7521, 7531

TABLE 2
CODE TABLE — BIPOLAR (OFFSET BINARY) OPERATION

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}\ (1-2^{-(n-1)})$
1000000001	$-V_{REF}\ (2^{-(n-1)})$
1000000000	0
0111111111	$V_{REF}\ (2^{-(n-1)})$
0000000001	$V_{REF}\ (1-2^{-(n-1)})$
0000000000	V_{REF}

NOTE: 1. $LSB = 2^{-(n-1)}\ V_{REF}$
2. n = 10 for 7520 and 7521
n = 12 for 7530 and 7531

APPLICATIONS

Unipolar Binary Operation

The circuit configuration for operating the AD7520 (AD7530) and AD7521 (AD7531) in unipolar mode is shown in Figure 11. With positive and negative V_{REF} values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1.

ZERO OFFSET ADJUSTMENT

1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V ±1 mV at V_{OUT}.

GAIN ADJUSTMENT

1. Connect all AD7520 (AD7530) or AD7521 (AD7531) digital inputs to V^+.
2. Monitor V_{OUT} for a $-V_{REF}\ (1-2^{-n})$ reading. (n = 10 for AD7520 (AD7530) and n = 12 for AD7521 (AD7531)).
3. To decrease V_{OUT}, connect a series resistor (0 to 500Ω) between the reference voltage and the V_{REF} terminal.
4. To increase V_{OUT}, connect a series resistor (0 to 500Ω) in the I_{OUT1} amplifier feedback loop.

Bipolar (Offset Binary) Operation

The circuit configuration for operating the AD7520 (AD7530) or AD7521 (AD7531) in the bipolar mode is given in Figure 12. Using offset binary digital input codes and positive and negative reference voltage values, 4-Quadrant multiplication can be realized. The "Digital Input Code/ Analog Output Value" table for bipolar mode is given in Table 2.

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to I_{OUT1} bus. A "Logic 0" input forces the bit current to I_{OUT2} bus. For any code the I_{OUT1} and I_{OUT2} bus currents are complements of one another. The current amplifier at I_{OUT2} changes the polarity of I_{OUT2} current and the transconductance amplifier at I_{OUT1} output sums the two currents. This configuration doubles the output range but halves the resolution of the DAC. The difference current resulting at zero offset binary code, (MSB = "Logic 1", All other bits = "Logic 0"), is corrected by using an external resistor, (10 Megohm), from V_{REF} to I_{OUT2}.

OFFSET ADJUSTMENT

1. Adjust V_{REF} to approximately +10V.
2. Connect all digital inputs to "Logic 1".
3. Adjust I_{OUT2} amplifier offset adjust trimpot for 0V ±1mV at I_{OUT2} amplifier output.
4. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
5. Adjust I_{OUT1} amplifier offset adjust trimpot for 0V ±1 mV at V_{OUT}.

GAIN ADJUSTMENT

1. Connect all digital inputs to V^+.
2. Monitor V_{OUT} for a $-V_{REF}\ (1-2^{-(n-1)})$ volts reading. (n = 10 for AD7520 and AD7530, and n = 12 for AD7521 and AD7531).
3. To increase V_{OUT}, connect a series resistor of up to 500Ω between V_{OUT} and $R_{FEEDBACK}$.
4. To decrease V_{OUT}, connect a series resistor of up to 500Ω between the reference voltage and the V_{REF} terminal.

Note: All typical values have been guaranteed by characterization and are not tested.

AD7520/7530/7521/7531

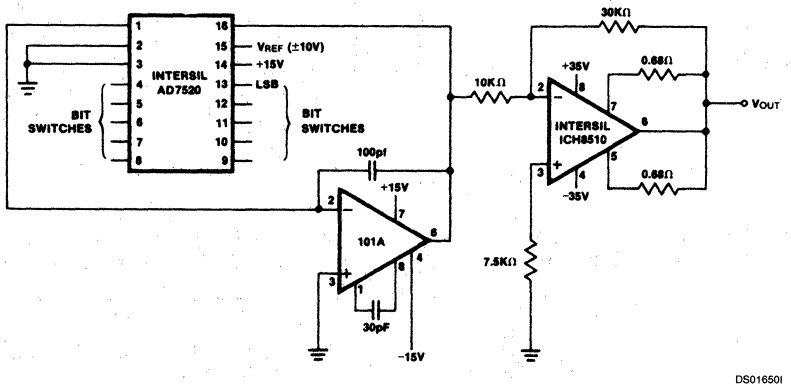


Figure 13: Basic Power DAC

POWER DAC DESIGN USING AD7520

A typical power DAC designed for 8 bit accuracy and 10 bit resolution is shown in Figure 13. An INTERSIL IH8510 power operational amplifier (1 Amp continuous output at up to ±25V) is driven by the AD7520.

A summing amplifier between the AD7520 and the IH8510 is used to separate the gain block containing the AD7520 on-chip resistors from the power amplifier gain stage whose gain is set only by the external resistors. This approach minimizes drift since the resistor pairs will track properly. Otherwise the AD7520 can be directly connected to the IH8510, by using a 25V reference for the DAC.

An important note on the AD7520/101A interface concerns the connection of pin 1 of the DAC and pin 2 of the 101A. Since this point is the summing junction of an amplifier with an AC gain of 50,000 or better, stray capacitance should be minimized; otherwise instabilities and poor noise performance will result. Note that the output of the 101A is fed into an inverting amplifier with a gain of −3, which can be easily changed to a non-inverting configuration. (For more information see: INTERSIL Application Bulletin A021: Power D/A Converters Using The IH8510 by Dick Wilenken.)

Analog/Digital Division

With the AD7520 connected in its normal multiplying configuration as shown in Figure 13, the transfer function is:

$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}\right)$$

where the coefficients A_X assume a value of 1 for an ON bit and 0 for an OFF bit.

By connecting the DAC in the feedback of an operational amplifier, as shown in Figure 14, the transfer function becomes:

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}}\right)$$

This is division of an analog variable (V_{IN}) by a digital word. With all bits off, the amplifier saturates to its bound, since division by zero isn't defined. With the LSB (Bit-10) ON, the gain is 1023. With all bits ON, the gain is 1 (±1 LSB).

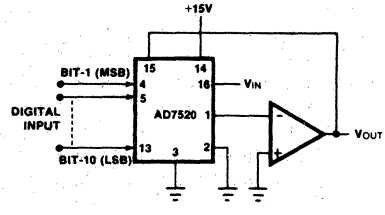


Figure 14: Analog/Digital Divider

For further information on the use of this device, see the following Application Bulletins:

A016 "Selecting A/D Converters," by David Fullagar
A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood
A020 "A Cookbook Approach to High-Speed Data Acquisition and Microprocessor Interfacing" by Ed Sliger
A021 "Power D/A Converters Using the IH8510," by Dick Wilenken

Note: All typical values have been guaranteed by characterization and are not tested.

AD7523
8-Bit Multiplying D/A Converter

GENERAL DESCRIPTION

The AD7523 is a monolithic, low cost, high performance, 10 bit accurate, multiplying digital-to-analog converter (DAC), in a 16-pin DIP.

Intersil's thin-film resistors on CMOS circuitry provide 8-bit resolution (8, 9 and 10-bit accuracy), with TTL/CMOS compatible operation.

The AD7523's accurate four quadrant multiplication, full military temperature range operation, full input protection from damage due to static discharge by clamps to V+ and GND, and very low power dissipation make it a very versatile converter.

Low noise audio gain controls, motor speed controls, digitally controlled gain and attenuators are a few of the wide range of applications of the 7523.

FEATURES

- **8, 9 and 10 Bit Linearity**
- **Low Gain and Linearity Temperature Coefficients**
- **Full Temperature Range Operation**
- **Static Discharge Input Protection**
- **DTL/TTL/CMOS Compatible**
- **+5 to +15 Volts Supply Range**
- **Fast Settling Time: 150ns Max at 25°C**
- **Four Quadrant Multiplication**

ORDERING INFORMATION

	PART NUMBER/PACKAGE		
NONLINEARITY	**PLASTIC DIP**	**CERDIP**	**CERDIP**
0.2% (8 Bit)	AD7523JN	AD7523AD	AD7523SD
0.1% (9 Bit)	AD7523KN	AD7523BD	AD7523TD
0.05% (10 Bit)	AD7523LN	AD7523CD	AD7523UD
TEMPERATURE RANGE	0°C to +70°C	−25°C to +85°C	−55°C to +125°C

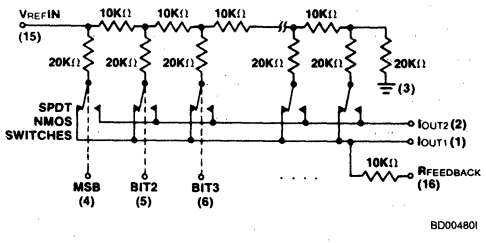


Figure 1: Functional Diagram (Switches shown for Digital Inputs "High")

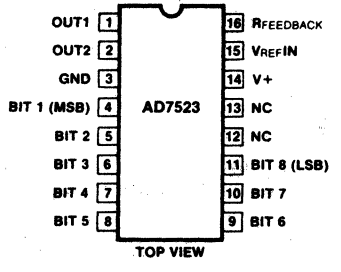


Figure 2: Pin Configuration Outline Drawings DE, PE

Note: All typical values have been guaranteed by characterization and are not tested.

AD7523

INTERSIL

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Supply Voltage (V^+) ..... +17V
V_{REF} ..... ±25V
Digital Input Voltage Range ..... V^+ to GND
Output Voltage Compliance ..... -100mV to V^+
Power Dissipation:
Plastic Package —
up to +70°C 670mW
derate above +70°C by ..... 8.3mW/°C
Ceramic Package —
up to 75°C 450mW
derate above 75°C by ..... 6mW/°C
Operating Temperatures
JN, KN, LN Versions ..... 0°C to +70°C
AD, BD, CD Versions ..... -25°C to +85°C
SD, TD, UD Versions ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C

CAUTION:
1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
2. Do not apply voltages higher than VDD and lower than GND to any terminal except V_{REF} + $R_{FEEDBACK}$.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V^+ = +15V, V_{REF} = +10V unless otherwise specified)

PARAMETER		TEST CONDITIONS	T_A +25°C	T_A MIN-MAX	UNIT	LIMIT
DC ACCURACY (Note 1)						
Resolution			8	8	Bits	Min
Nonlinearity (Note 2)	(±1/2 LSB)	-10V ≤ V_{REF} ≤ +10V V_{OUT1} = V_{OUT2} = 0V	±0.2	±0.2	% of FSR	Max
	(±1/4 LSB)		±0.1	±0.1	% of FSR	Max
	(±1/8 LSB)		±0.05	±0.05	% of FSR	Max
Monotonicity			Guaranteed			
Gain Error (Note 2)		Digital Inputs high.	±1.5	±1.8	% of FSR	Max
Nonlinearity Tempco (Notes 2 and 3)		-10V V_{REF} +10V	2		ppm of FSR/°C	Max
Gain Error Tempco (Notes 2 and 3)			10		ppm of FSR/°C	Max
Output Leakage Current (either output)		V_{OUT1} = V_{OUT2} = 0	±50	±200	nA	Max
AC ACCURACY						
Power Supply Rejection (Note 2)		V^+ = 14.0 to 15.0V	0.02	0.03	% of FSR	Max
Output Current Settling Time (Note 3)		To 0.2% of FSR, R_L = 100Ω	150	200	ns	Max
Feedthrough Error (Note 3)		V_{REF} = 20V pp, 200kHz sine wave. All digital inputs low.	±1/2	±1	LSB	Max
REFERENCE INPUT						
Input Resistance (Pin 15)		All digital inputs high. I_{OUT1} at ground.	5K		Ω	Min
			20K			Max
Temperature Coefficient (Note 3)			-500		ppm/°C	Max
ANALOG OUTPUT						
Output Capacitance (Note 3)	C_{OUT1}	All digital inputs high (VINH)	100		pF	Max
	C_{OUT2}		30		pF	Max
	C_{OUT1}	All digital inputs low (VINL)	30		pF	Max
	C_{OUT2}		100		pF	Max
DIGITAL INPUTS						
Low State Threshold (V_{INL})			0.8		V	Max
High State Threshold (V_{INH})			2.4		V	Min
Input Current (Low or high)		V_{IN} = 0V or +15V	±1		μA	Max
Input Coding		See Tables 1 & 2	Binary/Offset Binary			
Input Capacitance (Note 3)			4		pF	Max
POWER REQUIREMENTS						
Power Supply Voltage Range		Accuracy is tested and guaranteed at V^+ = +15V, only.	+5 to +16		V	
I^+		All digital inputs low or high.	2		mA	Max

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.

Note: All typical values have been guaranteed by characterization and are not tested.

AD7523

APPLICATIONS

UNIPOLAR OPERATION

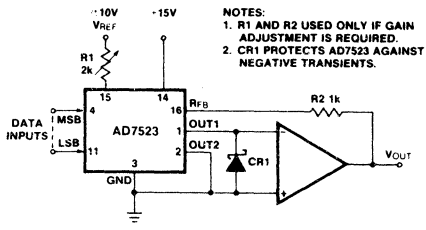


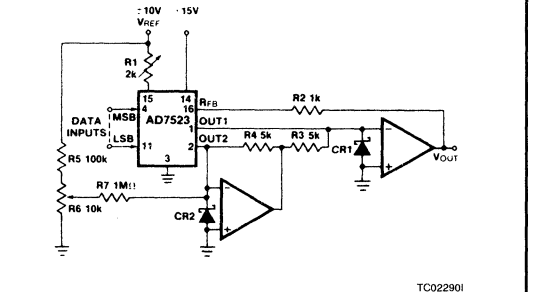
Figure 3: Unipolar Binary Operation

Table 1. Unipolar Binary Code Table

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
11111111	$-V_{REF}\left(\frac{255}{256}\right)$
10000001	$-V_{REF}\left(\frac{129}{256}\right)$
10000000	$-V_{REF}\left(\frac{128}{256}\right) = -\frac{V_{REF}}{2}$
01111111	$-V_{REF}\left(\frac{127}{256}\right)$
00000001	$-V_{REF}\left(\frac{1}{256}\right)$
00000000	$-V_{REF}\left(\frac{0}{256}\right) = 0$

NOTE: $1\ LSB = (2^{-8})\ (V_{REF}) = \left(\frac{1}{256}\right)\ (V_{REF})$

BIPOLAR OPERATION



NOTES:
1. R3/R4 MATCH 0.1% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
3. R5-R7 USED TO ADJUST $V_{OUT} = 0V$ AT INPUT CODE 10000000.
4. CR1 & CR2 PROTECT AD7523 AGAINST NEGATIVE TRANSIENTS.

Figure 4: Bipolar Operation

Table 2. Bipolar (Offset Binary) Code Table

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
11111111	$-V_{REF}\left(\frac{127}{128}\right)$
10000001	$-V_{REF}\left(\frac{1}{128}\right)$
10000000	0
01111111	$+V_{REF}\left(\frac{1}{128}\right)$
00000001	$+V_{REF}\left(\frac{127}{128}\right)$
00000000	$+V_{REF}\left(\frac{128}{128}\right)$

NOTE: $1\ LSB = (2^{-7})\ (V_{REF}) = \left(\frac{1}{128}\right)\ (V_{REF})$

A typical power DAC designed for 10 bit accuracy and 8 bit resolution is shown in Figure 5. The Intersil IH8510 power operational amplifier (1 Amp continuous output with up to +25V) is driven by the AD7523.

A summing amplifier between the AD7523 and the IH8510 is used to separate the gain block containing the AD7520 on-chip resistors from the power amplifier gain stage, whose gain is set only by the external resistors. This approach minimizes drift since the resistor pairs will track properly. Otherwise AD7523 can be directly connected to the IH8510, by using a 25 volt reference for the DAC.

Note: All typical values have been guaranteed by characterization and are not tested.

AD7523

POWER DAC DESIGN USING AD7523

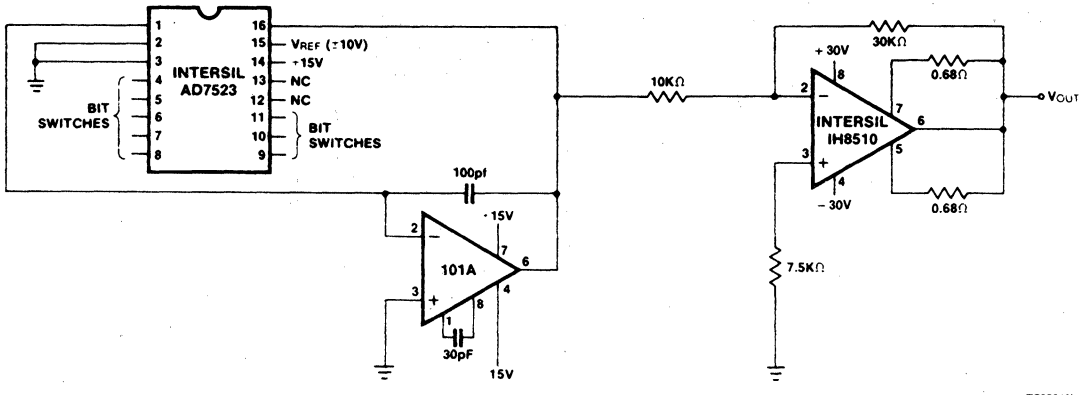


Figure 5: Basic Power DAC Design

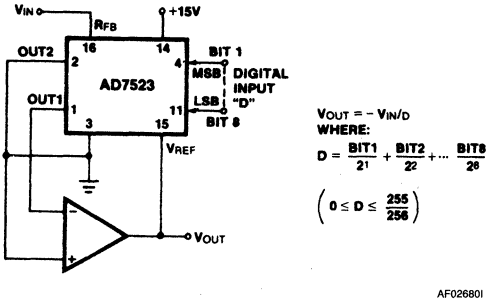


Figure 6: Divider (Digitally Controlled Gain)

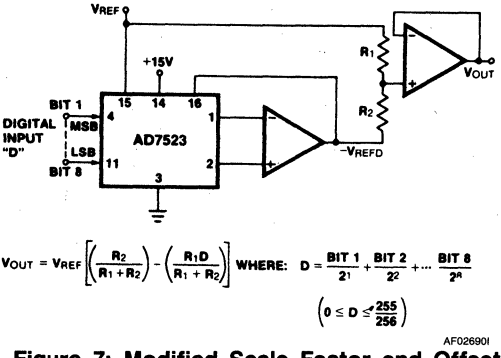


Figure 7: Modified Scale Factor and Offset

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within ½ LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

For further information on the use of this device, see the following Application Notes:

A016 "Selecting A/D Converters," by David Fullagar
A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood
A020 "A Cookbook Approach to High-Speed Data Acquisition and Microprocessor Interfacing" by Ed Sliger
A021 "Power D/A Converters Using the IH8510," by Dick Wilenken

Note: All typical values have been guaranteed by characterization and are not tested.

AD7533
10-Bit Multiplying D/A Converter

GENERAL DESCRIPTION

The Intersil AD7533 is a low cost, monolithic 10-bit, four-quadrant multiplying digital-to-analog converter (DAC). Intersil's thin-film resistor on CMOS circuitry provide 10, 9 and 8 bit accuracy, full temperature range operation, +5V to +15V supply voltage range, full input protection from damage due to static discharge by clamps to V^+ and ground and very low power dissipation.

Pin and function equivalent to the industry standard AD7520, the AD7533 is recommended as a lower cost alternative for old or new 10-bit DAC designs.

Applications for the AD7533 include programmable gain amplifiers, digitally controlled attenuators, function generators and control systems.

FEATURES

- **Lowest Cost 10-Bit DAC**
- **8, 9 and 10 Bit Linearity**
- **Low Gain and Linearity Tempcos**
- **Full Temperature Range Operation**
- **Full Input Static Protection**
- **TTL/CMOS Direct Interface**
- **+5 to +15 Volts Supply Range**
- **Low Power Dissipation**
- **Fast Settling Time**
- **Four Quadrant Multiplication**
- **Direct AD7520 Equivalent**
- **883B Processed Versions Available**

ORDERING INFORMATION

NONLINEARITY	TEMPERATURE RANGE 0°C to +70°C	-25°C to +85°C	-55°C to +125°C
±0.2% (8-bit)	AD7533JN	AD7533AD	AD7533SD
±0.1% (9-bit)	AD7533KN	AD7533BD	AD7533TD
±0.05% (10-bit)	AD7533LN	AD7533CD	AD7533UD

PACKAGE IDENTIFICATION

AD7533 T D

- D — Package: D — 18-Pin CERDIP DIP; N — 18-Pin Plastic DIP
- T — Nonlinearity and Temperature Range: J,K,L — Commercial 0°C to +70°C; A,B — Industrial -25°C to +85°C; S,T — Military -55°C to +125°C
- AD7533 — Basic Part Number

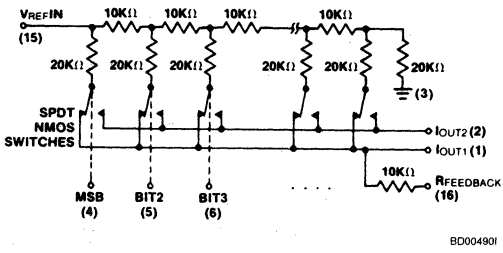


Figure 1: Functional Diagram

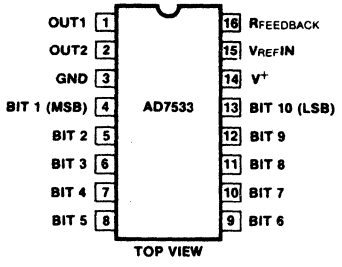


Figure 2: Pin Configuration

Note: All typical values have been guaranteed by characterization and are not tested.

AD7533

INTERSIL

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

V^+ ..... +17V
V_{REF} ..... ±25V
Digital Input Voltage Range ..... V^+ to GND
Output Voltage Compliance ..... −0.1V to V^+
Power Dissipation
Ceramic Package:
up to +75°C 450mW
derates above +75°C by ..... 6mW/°C
Plastic Package:
up to 70°C 670mW
derates above 70°C by ..... 8.3mW/°C
Operating Temperature Range:
JN, KN, LN Versions ..... 0°C to +70°C
AD, BD, CD Versions ..... −25°C to 85°C
SD, TD, UD Versions ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10sec) ..... +300°C

CAUTION:

1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

2. Do not apply voltages lower than ground or higher than V^+ to any pin except V_{REF} and R_{FB}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = +15V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0 unless otherwise specified.)

PARAMETER		TEST CONDITIONS	T_A +25°C	T_A MIN–MAX	LIMIT	UNIT
DC ACCURACY (Note 1)						
Resolution			10	10	Min	Bits
Nonlinearity (Note 2)			±0.2	±0.2	Max	% of FSR
		−10V ≤ V_{REF} ≤ +10V	±0.1	±0.1	Max	% of FSR
		V_{OUT1} = V_{OUT2} = 0V	±0.05	±0.05	Max	% of FSR
Gain Error (Note 2 and 5)		Digital Inputs = V_{INH}	±1.4	±1.5	Max	% of FS
Output Leakage Current (either output)		V_{REF} = ±10V	±50	±200	Max	nA
AC ACCURACY						
Power Supply Rejection (Note 2)		V^+ = 14.0 to 17.0V	0.005	0.008	Max	% of FSR/%
Output Current Settling Time (Note 3)		To 0.05% of FSR, R_L = 100Ω	600 (Note 6)	800 (Note 3)	Max	ns
Feedthrough Error (Note 3)		V_{REF} = ±10V, 100kHz sine wave. Digital inputs low.	±0.05	±0.1	Max	% FSR
REFERENCE INPUT						
Input Resistance (Pin 15)		All digital inputs high.	5k		Min	Ω
			20k		Max	
Temperature Coefficient			−300		Typ	ppm/°C
ANALOG OUTPUT						
Voltage Compliance (Note 3)		Both outputs. See maximum ratings	−100mV to V^+			
Output Capacitance (Note 3)	C_{OUT1}	All digital inputs high (V_{INH})	100		Max	pF
	C_{OUT2}		35		Max	pF
	C_{OUT1}	All digital inputs low (V_{INL})	35		Max	pF
	C_{OUT2}		100		Max	pF
DIGITAL INPUTS						
Low State Threshold (VINL)			0.8		Max	V
High State Threshold (VINH)			2.4		Min	V
Input Current (I_{IN})		V_{IN} = 0V and V^+	±1		Max	μA
Input Coding		See Tables 1 & 2	Binary/Offset Binary			
Input Capacitance (Note 3)			5		Max	pF

Note: All typical values have been guaranteed by characterization and are not tested.

AD7533

INTERSIL

ELECTRICAL CHARACTERISTICS (CONT.)

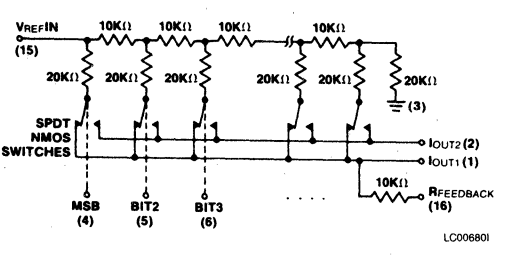
PARAMETER	TEST CONDITIONS	T_A +25°C	T_A MIN–MAX	LIMIT	UNIT
POWER REQUIREMENTS					
V_{DD}	Rated Accuracy	+15 ±10%			V
Power Supply Voltage Range		+5 to +16			V
I^+	Digital Inputs = V_{INL} to V_{INH}	2		Max	mA
	Digital Inputs = 0V or V^+	100	150	Max	μA

NOTES:
1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.
5. Full scale (FS) = $-(V_{REF}) \bullet (1023/1024)$
6. Sample tested to ensure specification compliance.

Specifications subject to change without notice.

DETAILED DESCRIPTION

The Intersil AD7533 is a 10 bit, monolithic, multiplying D/A converter. A highly stable thin film R-2R resistor ladder network and NMOS SPDT switches form the basis of the converter circuit. CMOS level shifters permit low power TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.



(Switches shown for Digital Inputs "High")

Figure 3

A simplified equivalent circuit of the DAC is shown in Figure 3. The NMOS SPDT switches steer the ladder leg currents between IOUT1 and IOUT2 busses which must be held at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.

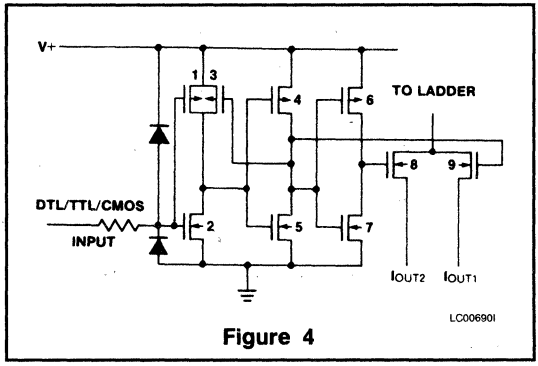


Figure 4

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first, (Figure 4). This configuration results in TTL/CMOS compatible operation over the full military temperature range. With the ladder SPDT switches driven by the level shifter, each switch is binarily weighted for an "ON" resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors resulting in accurate leg currents.

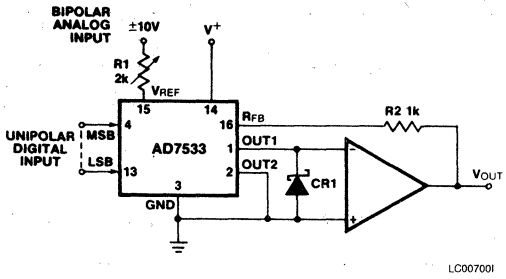
6

Note: All typical values have been guaranteed by characterization and are not tested.

AD7533

APPLICATIONS

UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)



NOTES: !nl1. R1 and R2 used only if gain adjustment is required.
2. Schottky diode CR1 (HP5082-2811 or equiv) protects OUT1 terminal against negative transients.

Figure 5: Unipolar Binary Operation (2-Quadrant Multiplication)

Table 1. Unipolar Binary Code

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 3)
1111111111	$-V_{REF}\left(\frac{1023}{1024}\right)$
1000000001	$-V_{REF}\left(\frac{513}{1024}\right)$
1000000000	$-V_{REF}\left(\frac{512}{1024}\right) = -\frac{V_{REF}}{2}$
0111111111	$-V_{REF}\left(\frac{511}{1024}\right)$
0000000001	$-V_{REF}\left(\frac{1}{1024}\right)$
0000000000	$-V_{REF}\left(\frac{0}{1024}\right) = 0$

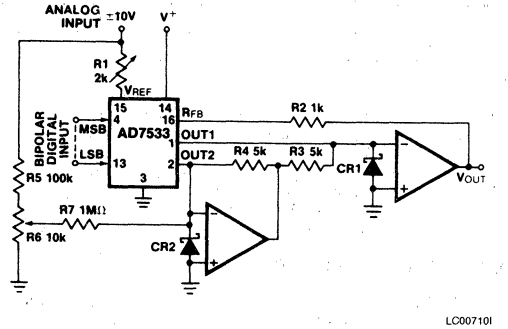
NOTES: 1. Nominal Full Scale for the circuit of Figure 3 is given by

$$FS = -V_{REF}\left(\frac{1023}{1024}\right)$$

2. Nominal LSB magnitude for the circuit of Figure 3 is given by

$$LSB = V_{REF}\left(\frac{1}{1024}\right)$$

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)



NOTES:
1. R3/R4 match 0.05% or better.
2. R1 and R2 used only if gain adjustment is required.
3. Schottky diodes CR1 and CR2 (HP5082-2811 or equiv) protect OUT1 and OUT2 terminals against negative transients.

Figure 6: Bipolar Operation (4-Quadrant Multiplication)

Table 2. Bipolar (Offset Binary) Code Table

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 4)
1111111111	$-V_{REF}\left(\frac{511}{512}\right)$
1000000001	$-V_{REF}\left(\frac{1}{512}\right)$
1000000000	0
0111111111	$+V_{REF}\left(\frac{1}{512}\right)$
0000000001	$+V_{REF}\left(\frac{511}{512}\right)$
0000000000	$+V_{REF}\left(\frac{512}{512}\right)$

NOTES: 1. Nominal Full Scale for the circuit of Figure 4 is given by

$$FSR = V_{REF}\left(\frac{1023}{512}\right)$$

2. Nominal LSB magnitude for the circuit of Figure 4 is given by

$$LSB = V_{REF}\left(\frac{1}{512}\right)$$

Note: All typical values have been guaranteed by characterization and are not tested.

POWER DAC DESIGN USING AD7533

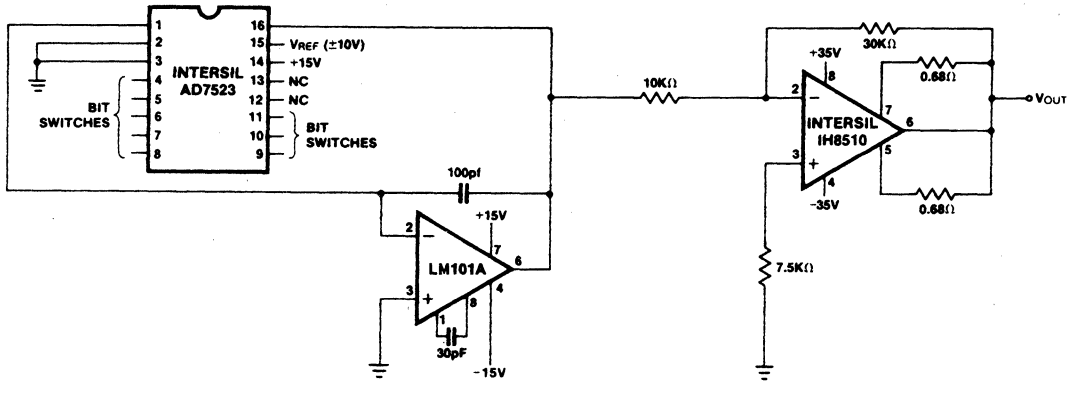


Figure 7: Basic Power DAC

A typical power DAC designed for 8 bit accuracy and 10 bit resolution is shown in Figure 7. INTERSIL IH8510 power amplifier (1 Amp continuous output with up to ±25V) is driven by the AD7533.

A summing amplifier between the AD7533 and the IH8510 is used to separate the gain block containing the AD7533 on-chip resistors from the power amplifier gain stage whose gain is set only by the external resistors. This approach minimizes drift since the resistor pairs will track properly. Otherwise the AD7533 can be directly connected to the IH8510, by using a 25 volts reference for the DAC. Notice that the output of the LM101A is fed into an inverting amplifier with a gain of −3, which can be easily changed to a non-inverting configuration. (For more information write for: INTERSIL Application Bulletin A021-Power D/A Converters Using The IH8510 by Dick Wilenken.)

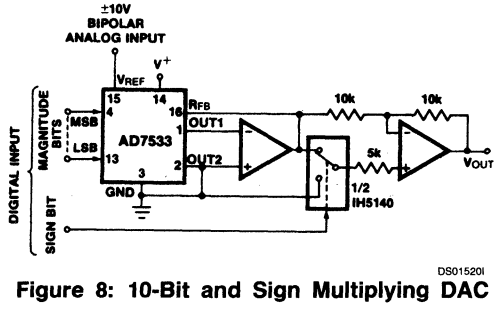


Figure 8: 10-Bit and Sign Multiplying DAC

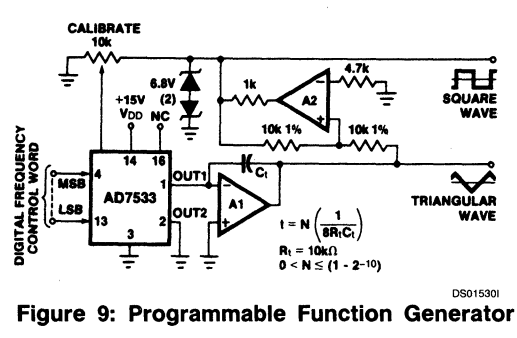


Figure 9: Programmable Function Generator

INPUT SIGNAL WARNING

Because of the input protection diodes on the logic inputs, it is important that no voltage greater than 4V outside the logic supply rails be applied to these inputs at any time, including power-up and other transients. To do so could cause destructive SCR latch-up.

Note: All typical values have been guaranteed by characterization and are not tested.

AD7541
12-Bit Multiplying D/A Converter

GENERAL DESCRIPTION

The Intersil AD7541 is a monolithic, low cost, high performance, 12-bit accurate, multiplying digital-to-analog converter (DAC).

Intersil's wafer level laser-trimmed thin-film resistors on CMOS circuitry provide true 12-bit linearity with TTL/CMOS compatible operation.

Special tabbed-resistor geometries (improving time stability), full input protection from damage due to static discharge by diode clamps to V + and ground, large I_{OUT1} and I_{OUT2} bus lines (improving superposition errors) are some of the features offered by Intersil AD7541.

Pin compatible with AD7521, this new DAC provides accurate four quadrant multiplication over the full military temperature range.

FEATURES

- **12 Bit Linearity (0.01%)**
- **Pretrimmed Gain**
- **Low Gain and Linearity Tempcos**
- **Full Temperature Range Operation**
- **Full Input Static Protection**
- **DTL/TTL/CMOS Compatible**
- **+5 to +15 Volts Supply Range**
- **Low Power Dissipation (20mW)**
- **Current Settling Time: 1μs to 0.01% of FSR**
- **Four Quadrant Multiplication**
- **883B Processed Versions Available**

ORDERING INFORMATION

	PART NUMBER/TEMPERATURE RANGE		
NONLINEARITY	0°C to +70°C	−25°C to +85°C	−55°C to +125°C
0.02% (11-bit)	AD7541JN	AD7541AD	AD7541SD
0.01% (12-bit)	AD7541KN	AD7541BD	AD7541TD
0.01% (12-bit) Guaranteed Monotonic	AD7541LN	–	–

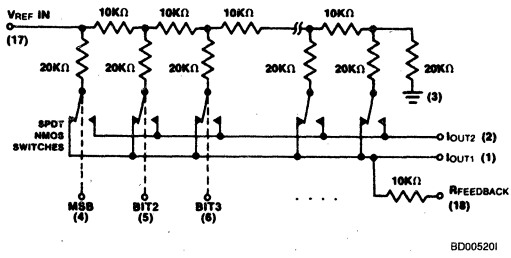


Figure 1: Functional Diagram (Switches shown for Digital Inputs 'High')

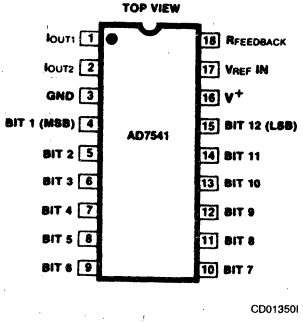


Figure 2: Pin Configuration (Outline dwgs DN, PN)

300150-002

Note: All typical values have been guaranteed by characterization and are not tested.

AD7541

INTERSIL

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

$V+$ ..... +17V
V_{REF} ..... ±25V
Digital Input Voltage Range ..... GND to V^+
Output Voltage Compliance ..... −100mV to V^+
Power Dissipation (package):
up to +75°C 450mW
derate above +75°C by ..... 6mW/°C

Operating Temperature Range:
JN, KN, LN Versions ..... 0°C to +70°C
AD, BD Versions ..... −25°C to +85°C
SD, TD Versions ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

CAUTION

1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
2. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{fb}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

ELECTRICAL CHARACTERISTICS (V^+ = +15V, V_{REF} = +10V, T_A = 25°C unless otherwise specified)

PARAMETER			TEST CONDITIONS	TA +25°C	TA MIN–MAX	LIMIT	FIG.	UNIT
DC ACCURACY (Note 1)								
Resolution				12	12	Min		Bits
Nonlinearity (Note 2)	S	J		±0.024	±0.024	Max		% of FSR
	T	K	$-10V \le V_{REF} \le +10V$	±0.012	±0.012	Max	1	% of FSR
		L	$V_{OUT1} = V_{OUT2} = 0V$	±0.012	±0.012 Guaranteed Monotonic	Max		% of FSR
Gain Error (Note 2)			$-10V \le V_{REF} \le +10V$	±0.3	±0.4	Max		% of FSR
Output Leakage Current (either output)			$V_{OUT1} = V_{OUT2} = 0$	±50	±200	Max		nA
AC ACCURACY (Note 3)								
Power Supply Rejection (Note 2)			V^+ = 14.5 to 15.5V	±0.01	±0.02	Max	2	% of FSR/%
Output Current Settling Time			To 0.01% of FSR	1		Max	6	µs
Feedthrough Error			V_{REF} = 20V pp, 10kHz. All digital inputs low.	1		Max	5	mV pp
REFERENCE INPUT								
Input Resistance				5K		Min		Ω
			All digital inputs high.	10K		Typ		
			I_{OUT1} at ground.	20K		Max		
ANALOG OUTPUT								
Voltage Compliance (Note 4)			Both outputs. See maximum ratings.	−100mV to V^+				
Output Capacitance (Note 3)	C_{OUT1} C_{OUT2}		All digital inputs high (V_{INH})	200 60		Max Max	4	pF pF
	C_{OUT1} C_{OUT2}		All digital inputs low (V_{INL})	60 200		Max Max	4	pF pF
Output Noise (both outputs)				Equivalent to 10KΩ Johnson noise		Typ	3	
DIGITAL INPUTS								
Low State Threshold (V_{INL})				0.8		Max		V
High State Threshold (V_{INH})				2.4		Min		V
Input Current			V_{IN} = 0 or V^+	±1		Max		µA
Input Coding			See Tables 1 & 2	Binary/Offset Binary				
Input Capacitance (Note 3)				8		Max		pF
POWER REQUIREMENTS								
Power Supply Voltage Range			Accuracy is not guaranteed over this range	+5 to +16				V
I^+			All digital inputs high or low	2.0/2.5		Max		mA
Total Power Dissipation (Including the ladder)				20		Typ		mW

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.

Specifications subject to change without notice.

Note: All typical values have been guaranteed by characterization and are not tested.

AD7541

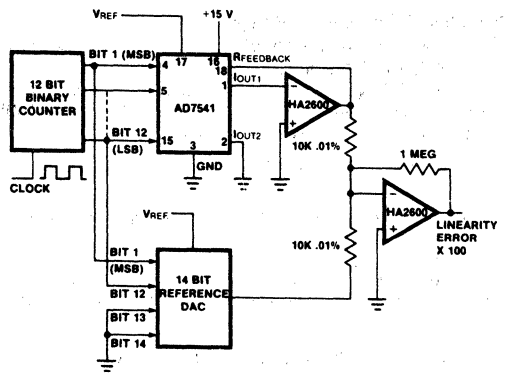


Figure 3: Nonlinearity Test Circuit

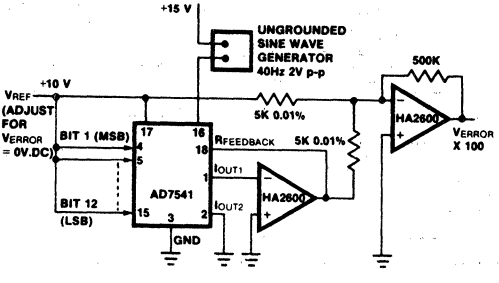


Figure 4: Power Supply Rejection Test Circuit

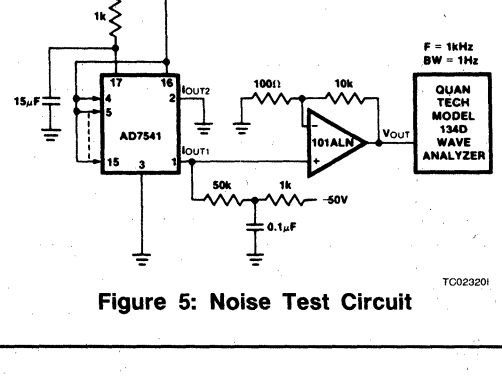


Figure 5: Noise Test Circuit

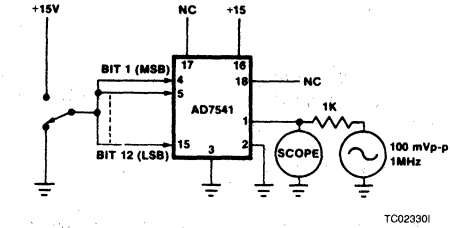


Figure 6: Output Capacitance Test Circuit

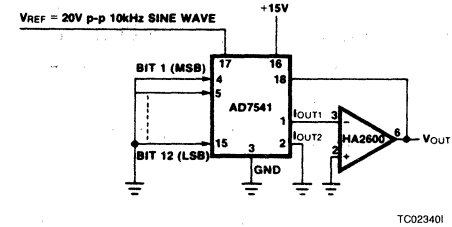


Figure 7: Feedthrough Error Test Circuit

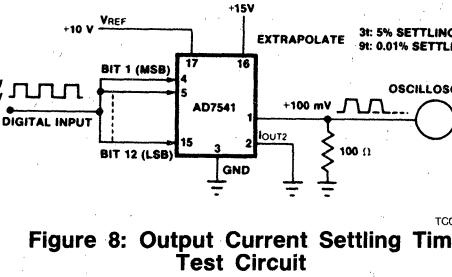


Figure 8: Output Current Settling Time Test Circuit

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

Note: All typical values have been guaranteed by characterization and are not tested.

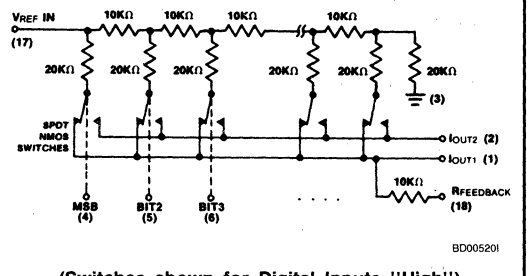
AD7541

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

DETAILED DESCRIPTION

The Intersil AD7541 is a 12 bit, monolithic, multiplying D/A converter. Highly stable thin film R-2R resistor ladder network and NMOS DPDT switches form the basis of the converter circuit. CMOS level shifters provide low power DTL/TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.



(Switches shown for Digital Inputs "High")

Figure 9: AD7541 Functional Diagram

A simplified equivalent circuit of the DAC is shown in Figure 9. The NMOS DPDT switches steer the ladder leg currents between IOUT1 and IOUT2 buses which must be held at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code. Converter errors are further eliminated by using wider metal interconnections between the major bits and the outputs. Use of high threshold switches reduces the offset (leakage) errors to a negligible level.

Each circuit is laser-trimmed, at the wafer level, to better than 12 bits linearity. For the first four bits of the ladder, special trim-tabbed geometries are used to keep the body of the resistors, carrying the majority of the output current, undisturbed. The resultant time stability of the trimmed circuits is comparable to that of untrimmed units.

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first (Figure 10). This configuration results in DTL/TTL/CMOS compatible operation over the full military temperature range. With the ladder DPDT switches driven by the level shifter, each switch is binarily weighted for an "ON" resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors, resulting in accurate leg currents.

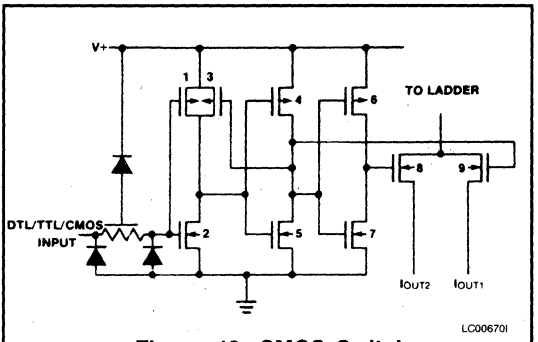


Figure 10: CMOS Switch

APPLICATIONS

General Recommendations

Static performance of the AD7541 depends on I_{OUT1} and I_{OUT2} (pin 1 and pin 2) potentials being exactly equal to GND (pin 3).

The output amplifier should be selected to have a low input bias current (typically less than 75nA), and a low drift (depending on the temperature range). The voltage offset of the amplifier should be nulled (typically less than $\pm 200\mu V$).

The bias current compensation resistor in the amplifier's non-inverting input can cause a variable offset. Non-inverting input should be connected to GND with a low resistance wire.

Ground-loops must be avoided by taking all pins going to GND to a common point, using separate connections.

The V^+ (pin 18) power supply should have a low noise level and should not have any transients exceeding +17 volts.

Unused digital inputs must be connected to GND or V_{DD} for proper operation.

A high value resistor (~1MΩ) can be used to prevent static charge accumulation, when the inputs are open-circuited for any reason.

When gain adjustment is required, low tempco (approximately 50ppm/°C) resistors or trim-pots should be selected.

UNIPOLAR BINARY OPERATION

The circuit configuration for operating the AD7541 in unipolar mode is shown in Figure 11. With positive and negative VREF values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1. A Schottky diode (HP5082-2811 or equivalent) prevents I_{OUT1} from negative excursions which could damage the device. This precaution is only necessary with certain high speed amplifiers.

Note: All typical values have been guaranteed by characterization and are not tested.

AD7541

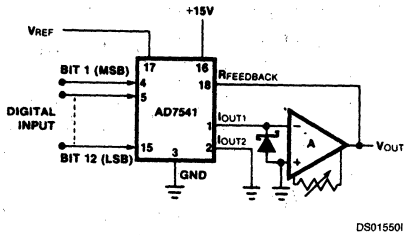


Figure 11: Unipolar Binary Operation (2-Quadrant Multiplication)

Zero Offset Adjustment

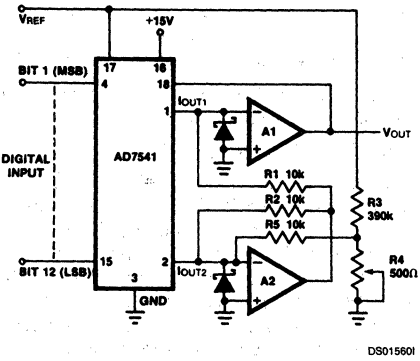
1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V ±0.5mV (max) at VOUT.

Gain Adjustment

1. Connect all digital inputs to VDD.
2. Monitor VOUT for a $-VREF\ (1-1/2^{12})$ reading.
3. To increase VOUT, connect a series resistor, (0 to 500 ohms), in the IOUT1 amplifier feedback loop.
4. To decrease VOUT, connect a series resistor, (0 to 500 ohms), between the reference voltage and the VREF terminal.

Table 1: Code Table — Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
111111111111	$-V_{REF}\ (1-1/2^{12})$
100000000001	$-V_{REF}\ (1/2+1/2^{12})$
100000000000	$-V_{REF}/2$
011111111111	$-V_{REF}\ (1/2-1/2^{12})$
000000000001	$-V_{REF}\ (1/2^{12})$
000000000000	0



Note: R1 and R2 should be 0.01%, low-TCR resistors.

Figure 12: Bipolar Operation (4-Quadrant Multiplication)

BIPOLAR (OFFSET BINARY) OPERATION

The circuit configuration for operating the AD7541 in the bipolar mode is given in Figure 12. Using offset binary digital input codes and positive and negative reference voltage values Four-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to IOUT1 bus. A "Logic 0" input forces the bit current to IOUT2 bus. For any code the IOUT1 and IOUT2 bus currents are complements of one another. The current amplifier at IOUT2 changes the polarity of IOUT2 current and the transconductance amplifier at IOUT1 output sums the two currents. This configuration doubles the output range but halves the resolution of the DAC. The difference current resulting at zero offset binary code, (MSB = "Logic 1", All other bits = "Logic 0"), is corrected by using an external resistive divider, from VREF to IOUT2.

Offset Adjustment

1. Adjust V_{REF} to approximately +10V.
2. Set R4 to zero.
3. Connect all digital inputs to "Logic 1".
4. Adjust I_{OUT2} amplifier offset zero adjust trimpot for 0V ±0.1mV at I_{OUT2} amplifier output.
5. Connect a short circuit across R2.
6. Connect all digital inputs to "Logic 0".
7. Adjust I_{OUT2} amplifier offset zero adjust trimpot for 0V ±0.1mV at I_{OUT1} amplifier output.
8. Remove short circuit across R2.
9. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
10. Adjust R4 for 0V ±0.2mV at V_{OUT}.

Gain Adjustment

1. Connect all digital inputs to VDD.
2. Monitor VOUT for a $-VREF\ (1-1/2^{11})$ volts reading.
3. To increase VOUT, connect a series resistor, (0 to 500 ohms), in the IOUT1 amplifier feedback loop.
4. To decrease VOUT, connect a series resistor, (0 to 500 ohms), between the reference voltage and the VREF terminal.

Table 2: Code Table Bipolar (Offset Binary) Operation

DIGITAL INPUT	ANALOG OUTPUT
111111111111	$-V_{REF}\ (1-1/2^{11})$
100000000001	$-V_{REF}\ (1/2^{11})$
100000000000	0
011111111111	$V_{REF}\ (1/2^{11})$
000000000001	$V_{REF}\ (1-1/2^{11})$
000000000000	V_{REF}

Note: All typical values have been guaranteed by characterization and are not tested.

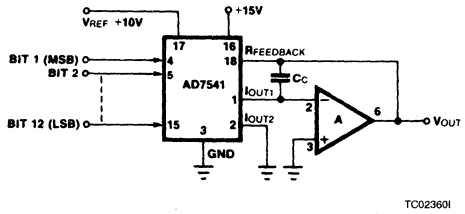


Figure 13: General DAC Circuit with Compensation Capacitor, C_C

DYNAMIC PERFORMANCE

The dynamic performance of the DAC, also depends on the output amplifier selection. For low speed or static applications, AC specifications of the amplifier are not very critical. For high-speed applications slew-rate, settling-time, openloop gain and gain/phase-margin specifications of the amplifier should be selected for the desired performance.

The output impedance of the AD7541 looking into I_{OUT1} varies between 10kΩ ($R_{Feedback}$ alone) and 5KΩ ($R_{Feedback}$) in parallel with the ladder resistance).

Similarly the output capacitance varies between the minimum and the maximum values depending on the input code. These variations necessitate the use of compensation capacitors, when high speed amplifiers are used.

A capacitor in parallel with the feedback resistor (as shown in Figure 13) provides the necessary phase compensation to critically damp the output.

A small capacitor connected to the compensation pin of the amplifier may be required for unstable situations causing oscillations. Careful PC board layout, minimizing parasitic capacitances, is also vital.

INPUT SIGNAL WARNING

Because of the input protection diodes on the logic inputs, it is important that no voltage greater than 4V outside the logic supply rails be applied to these inputs at any time, including power-up and other transients. To do so could cause destructive SCR latch-up.

Note: All typical values have been guaranteed by characterization and are not tested.

ADC0802-ADC0804
8-Bit μP-Compatible A/D Converters

INTERSIL

GENERAL DESCRIPTION

The ADC0802 family are CMOS 8-bit successive approximation A/D converters which use a modified potentiometric ladder, and are designed to operate with the 8080A control bus via three-state outputs. These converters appear to the processor as memory locations or I/O ports, and hence no interfacing logic is required.

The differential analog voltage input has good common-mode-rejection, and permits offsetting the analog zero-input-voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

FEATURES

- **80C48 and 80C80/85 Bus Compatible — No Interfacing Logic Required**
- **Conversion Time < 100μs**
- **Easy Interface to Most Microprocessors**
- **Will Operate in a "Stand Alone" Mode**
- **Differential Analog Voltage Inputs**
- **Works With Bandgap Voltage References**
- **TTL Compatible Inputs and Outputs**
- **On-Chip Clock Generator**
- **0V to 5V Analog Voltage Input Range (Single +5V Supply)**
- **No Zero-Adjust Required**

ORDERING INFORMATION

PART NUMBER	ERROR	TEMPERATURE RANGE	PACKAGE
ADC0802LCN	±1/2 bit no adjust	0°C to +70°C	20 pin Plastic DIP
ADC0802LCD		−25°C to +85°C	20 pin CERDIP
ADC0802LD		−55°C to +125°C	20 pin CERDIP
ADC0803LCN	±1/2 bit adjusted full-scale	0°C to +70°C	20 pin Plastic DIP
ADC0803LCD		−25°C to +85°C	20 pin CERDIP
ADC0803LD		−55°C to +125°C	20 pin CERDIP
ADC0804LCN	±1 bit no adjust	0°C to +70°C	20 pin Plastic DIP
ADC0804LCD		−25°C to +85°C	20 pin CERDIP

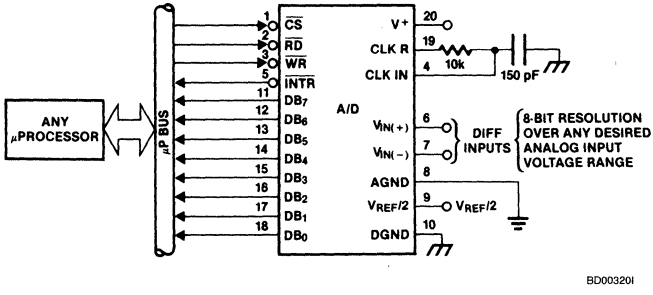
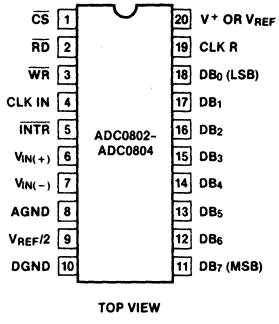


Figure 1: Typical Application



(Outline dwg. CD, CN)

Figure 2: Pin Configuration

Note: All typical values have been guaranteed by characterization and are not tested.

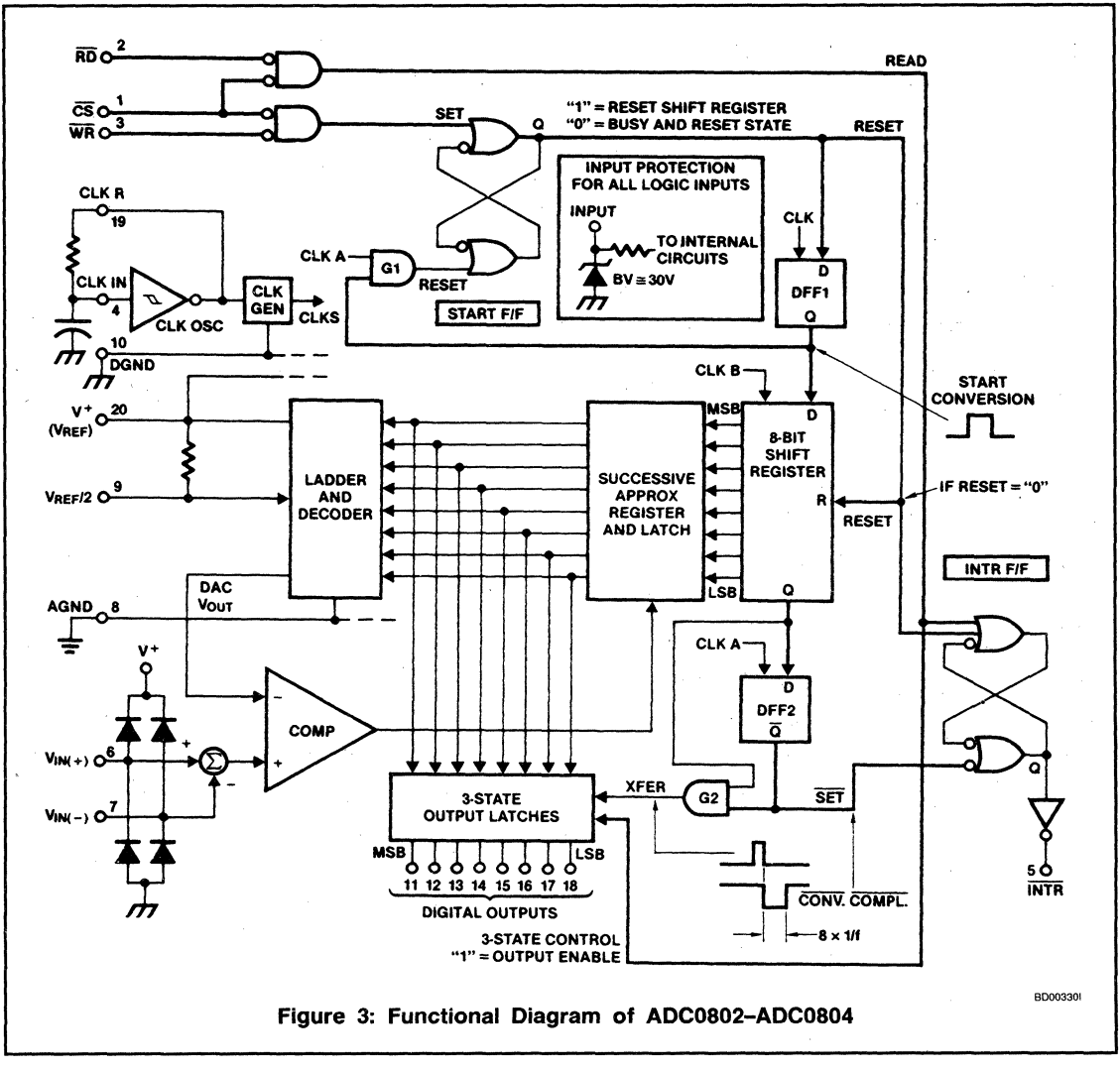


Figure 3: Functional Diagram of ADC0802–ADC0804

Note: All typical values have been guaranteed by characterization and are not tested.

ADC0802-ADC0804

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6.5V
Voltage at Any Input ..... −0.3V to (V^+ + 0.3V)
Storage Temperature Range ..... −65°C to +150°C
Package Dissipation at T_A = +25°C 875mW
Lead Temperature (Soldering, 10sec) ..... 300°C

OPERATING RATINGS

Temperature Range
ADC0802/03LD ..... −55°C to +125°C
ADC0802/03/04LCD ..... −40°C to +85°C
ADC0802/03/04LCN ..... 0°C to +70°C
Supply Voltage Range ..... 4.5V to 6.3V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Notes 1 and 7)

Converter Specifications: $V^+ = 5V$, $V_{REF}/2 = 2.500V$, $T_{MIN} \leq T_A \leq T_{MAX}$ and $f_{CLK} = 640kHz$ unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC0802: Total Unadjusted Error	Completely Unadjusted			±1/2	LSB
ADC0803: Total Adjusted Error	With Full Scale Adjust			±1/2	LSB
ADC0804: Total Unadjusted Error	Completely Unadjusted			±1	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3		kΩ
Analog Input Voltage Range	(Note 2)	GND − 0.05		V^+ + 0.05	V
DC Common-Mode Rejection	Over Analog Input Voltage Range		±1/16	±1/8	LSB
Power Supply Sensitivity	V^+ = 5V ±10% Over Allowed Input Voltage Range		± 1/16	± 1/8	LSB

DC ELECTRICAL CHARACTERISTICS

Digital Levels and DC Specifications: $V^+ = 5V$ and $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CONTROL INPUTS (Note 6)						
V_{INH}	Logical "1" Input Voltage (Except Pin 4 CLK IN)	$V^+ = 5.25V$	2.0		V^+	V
V_{INL}	Logical "0" Input Voltage (Except Pin 4 CLK IN)	$V^+ = 4.75V$			0.8	V
V^+_{CLK}	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V
V^-_{CLK}	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V
V_H	CLK IN (Pin 4) Hysteresis (V^+_{CLK}) − (V^-_{CLK})		0.6	1.3	2.0	V
I_{INHI}	Logical "1" Input Current (All Inputs)	$V_{IN} = 5V$		0.005	1	μA
I_{INLO}	Logical "0" Input Current (All Inputs)	$V_{IN} = 0V$	−1	−0.005		μA
I^+	Supply Current (Includes Ladder Current)	f_{CLK} = 640kHz, T_A = +25°C and $\overline{CS}$ = HI		1.3	2.5	mA
DATA OUTPUTS AND $\overline{INTR}$						
V_{OL}	Logical "0" Output Voltage	I_O = 1.6mA, V^+ = 4.75V			0.4	V
V_{OH}	Logical "1" Output Voltage	I_O = −360μA, V^+ = 4.75V	2.4			V
I_{LO}	3-State Disabled Output Leakage (All Data Buffers)	V_{OUT} = 0V V_{OUT} = 5V	−3		 3	μA μA

Note: All typical values have been guaranteed by characterization and are not tested.

ADC0802-ADC0804

INTERSIL

DC ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SOURCE}	Output Short Circuit Current	V_{OUT} Short to Gnd $T_A = +25°C$	4.5	6		mA
I_{SINK}	Output Short Circuit Current	V_{OUT} Short to V^+ $T_A = +25°C$	9.0	16		mA

NOTES: 1. All voltages are measured with respect to GND, unless otherwise specified. The separate AGND point should always be wired to the DGND, being careful to avoid ground loops.

2. For $V_{IN(-)} \geq V_{IN(+)}$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see **Block Diagram**) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V^+ supply. Be careful, during testing at low V^+ levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct-especially at elevated temperatures, and cause errors for analog inputs near full-scale. As long as the analog V_{IN} does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over temperature variations, initial tolerance and loading.
3. With $V^+ = 6V$, the digital logic interfaces are no longer TTL compatible.
4. With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process.
5. The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input so that timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see **Timing Diagrams**).
6. CLK IN (pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately.
7. None of these A/Ds requires a zero-adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.0V full-scale) the $V_{IN(-)}$ input can be adjusted to achieve this. See **Zero Error** on page 10 of this data sheet.

AC ELECTRICAL CHARACTERISTICS

Timing Specifications: $V^+ = 5V$ and $T_A = +25°C$ unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CLK}	Clock Frequency	$V^+ = 6V$ (Note 3) $V^+ = 5V$	100 100	640 640	1280 800	kHz kHz
t_{conv}	Clock Periods per Conversion (Note 4)		62		73	
CR	Conversion Rate In Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS} = 0V$, $f_{CLK} = 640kHz$			8888	conv/s
$t_{W(\overline{WR})I}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS} = 0V$ (Note 5)	100			ns
t_{acc}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	$C_L = 100pF$ (Use Bus Driver IC for Larger C_L)		135	200	ns
t_{1h}, t_{0h}	3-State Control (Delay from Rising Edge of $\overline{RD}$ to HI-Z State)	$C_L = 10pF$, $R_L = 10k$ (See **3-State Test Circuits**)		125	250	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF
C_{OUT}	3-State Output Capacitance (Data Buffers)			5	7.5	pF

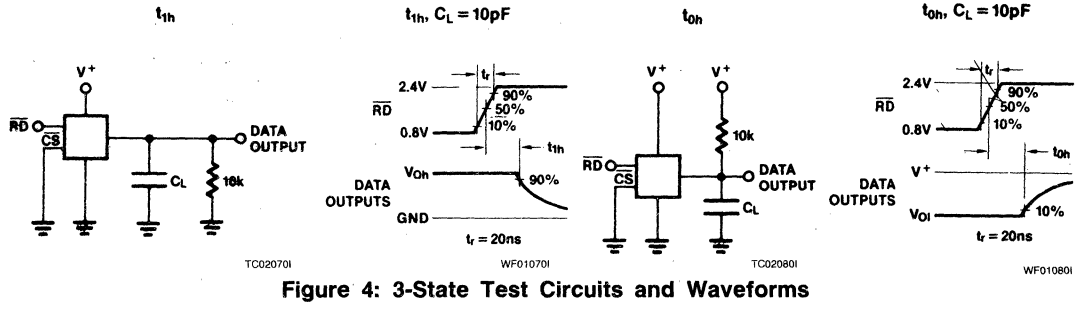


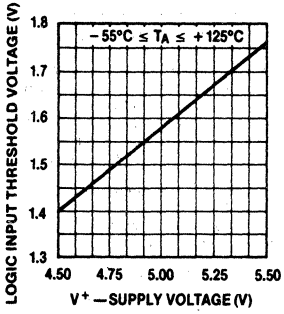
Figure 4: 3-State Test Circuits and Waveforms

Note: All typical values have been guaranteed by characterization and are not tested.

ADC0802-ADC0804

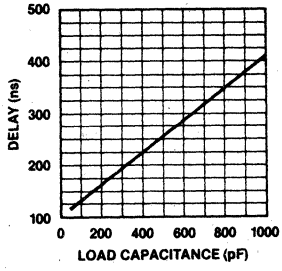
TYPICAL PERFORMANCE CHARACTERISTICS

Logic Input Threshold Voltage vs Supply Voltage



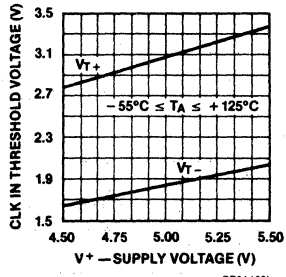
OP01440I

Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs Load Capacitance



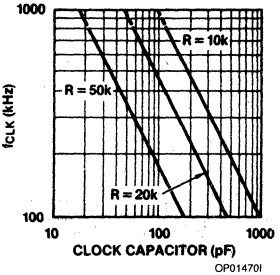
OP01450I

CLK IN Schmitt Trip Levels vs Supply Voltage



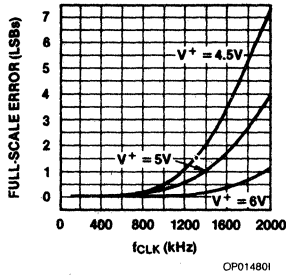
OP01460I

f_{CLK} vs Clock Capacitor



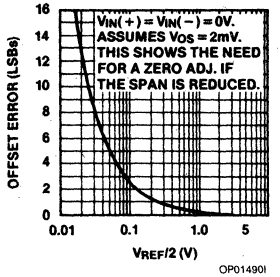
OP01470I

Full-Scale Error vs F_{CLK}



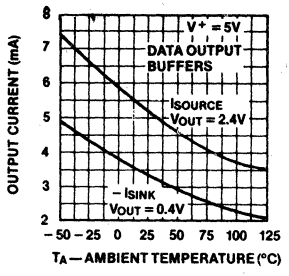
OP01480I

Effect of Unadjusted Offset Error



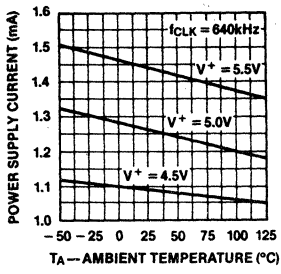
OP01490I

Output Current vs Temperature vs $V_{REF}/2$ Voltage



OP01500I

Power Supply Current vs Temperature



OP01510I

Note: All typical values have been guaranteed by characterization and are not tested.

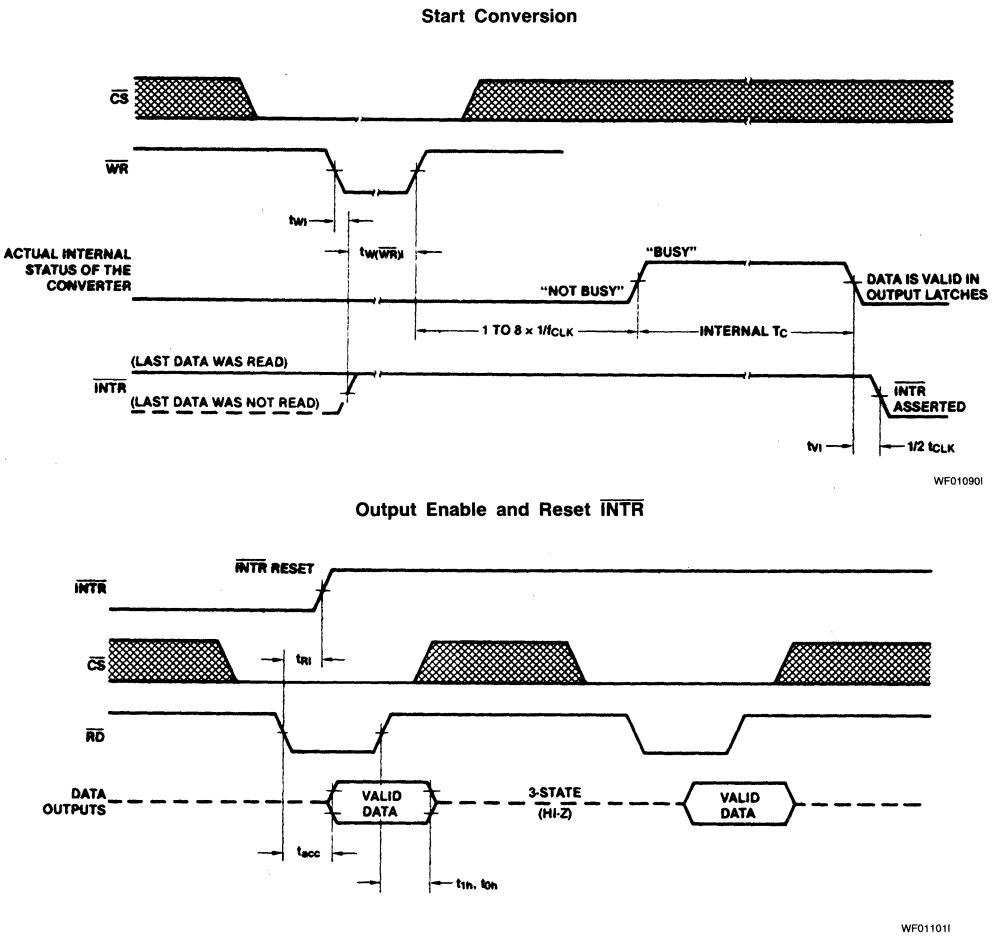


Figure 5: Timing Diagrams

Note: All timing is measured from the 50% voltage points.

UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in Figure 6a. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1LSB (19.53mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes which correspond to these inputs are shown as D – 1, D, and D + 1. For the perfect A/D, not only will center-value (A – 1,A,A + 1, . . .) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located ± ½ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages which extend ± ½ LSB from the ideal center-values. Each tread (the range of analog input voltage which provides the same digital output code) is therefore 1LSB wide.

The error curve of Figure 6b shows the worst case transfer function for the ADC0802. Here the specification guarantees that if we apply an analog input equal to the LSB analog voltage center-value, the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Notice that the error includes the quantization uncertainty of the A/D. For example, the error at point 1 of Figure 6a is + ½ LSB because the digital code appeared ½ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1LSB in magnitude, unless the device has missing codes.

FUNCTIONAL DESCRIPTION

A functional diagram of the ADC0802 series of A/D converters is shown in Figure 3. All of the package pinouts

Note: All typical values have been guaranteed by characterization and are not tested.

are shown and the major logic control paths are drawn in heavier-weight lines. The device operates on the successive approximation principle (see APPLICATION NOTE A016 and A020 for a more detailed description of this principle). Analog switches are closed sequentially by successive-approximation logic until the analog differential input voltage $[V_{IN(+)} - V_{IN(-)}]$ matches a voltage derived from a tapped resistor string across the reference voltage. The most significant bit is tested first and after 8 comparisons (64 clock cycles), an 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch.

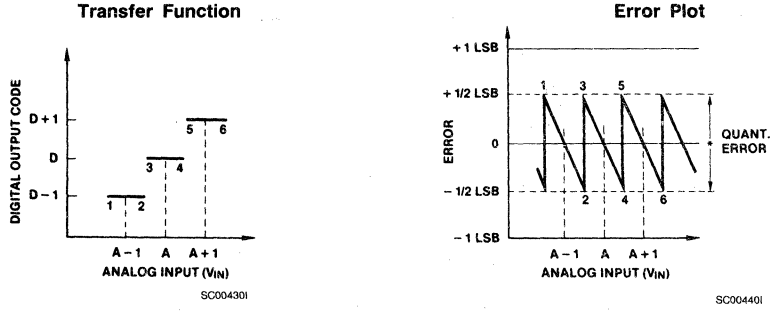
The normal operation proceeds as follows. On the high-to-low transition of the $\overline{WR}$ input, the internal SAR latches and the shift-register stages are reset, and the $\overline{INTR}$ output will be set high. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. **Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.** After the requisite number of clock pulses to complete the conversion, the $\overline{INTR}$ pin will make a high-to-low transition. This can be used to interrupt a processor, or otherwise signal the availability of a new conversion. A $\overline{RD}$ operation (with $\overline{CS}$ low) will clear the $\overline{INTR}$ line high again. The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS}$ = 0. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle. A conversion-in-process can be interrupted by issuing a second start command.

Digital Details

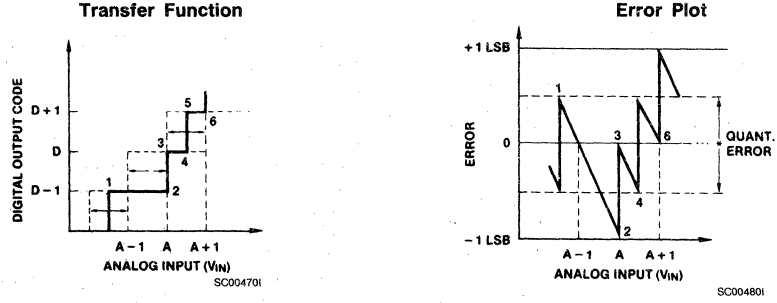
The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a "1" to the D flip-flop, DFF1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of DFF1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1"), the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This allows for asynchronous or wide $\overline{CS}$ and $\overline{WR}$ signals.

After the "1" is clocked through the 8-bit shift register (which completes the SAR operation) it appears as the input to DFF2. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the 3-state output latches. When DFF2 is subsequently clocked, the $\overline{Q}$ output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ output signal.

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the 3-state output latches will be enabled to provide the 8-bit digital outputs.



a) Accuracy = ±0 LSB; A Perfect A/D



b) Accuracy = ± ½ LSB

Figure 6: Clarifying the Error Specs of an A/D Converter

Note: All typical values have been guaranteed by characterization and are not tested.

Digital Control Inputs

The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet standard TTL logic voltage levels. These signals are essentially equivalent to the standard A/D Start and Output Enable control signals, and are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (pin 1) can be grounded and the standard A/D Start function obtained by an active low pulse at the $\overline{WR}$ input (pin 3). The Output Enable function is achieved by an active low pulse at the $\overline{RD}$ input (pin 2).

Analog Operation

The analog comparisons are performed by a capacitive charge summing circuit. Three capacitors (with precise ratioed values) share a common node with the input to an auto-zeroed comparator. The input capacitor is switched between $V_{IN(+)}$ and $V_{IN(-)}$, while two ratioed reference capacitors are switched between taps on the reference voltage divider string. The net charge corresponds to the weighted difference between the input and the current total value set by the successive approximation register. A correction is made to offset the comparison by 1/2 LSB (see Figure 6a).

Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D gains considerable applications flexibility from the analog differential voltage input. The $V_{IN(-)}$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4mA–20mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN(+)}$ and $V_{IN(-)}$ is 4 1/2 clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(MAX) = (V_p)(2\pi f_{cm})\left[\frac{4.5}{f_{CLK}}\right]$$

where:

ΔV_e is the error voltage due to sampling delay
V_P is the peak value of the common-mode voltage
f_{cm} is the common-mode frequency

For example, with a 60Hz common-mode frequency, f_{cm}, and a 640kHz A/D clock, f_{CLK}, keeping this error to 1/4 LSB (~5mV) would allow a common-mode voltage, V_P, given by:

$$V_p = \frac{[\Delta V_e(MAX)(f_{CLK})]}{(2\pi f_{cm})(4.5)}$$

or

$$V_p = \frac{(5 \times 10^{-3})\ (640 \times 10^{3})}{(6.28)\ (60)\ (4.5)} \simeq 1.9V$$

The allowed range of analog input voltage usually places more severe restrictions on input common-mode voltage levels than this.

An analog input voltage with a reduced span and a relatively large zero offset can be easily handled by making use of the differential input (see **Reference Voltage Span Adjust).**

Analog Input Current

The internal switching action causes displacement currents to flow at the analog inputs. The voltage on the on-chip capacitance to ground is switched through the analog differential input voltage, resulting in proportional currents entering the $V_{IN(+)}$ input and leaving the $V_{IN(-)}$ input. These current transients occur at the leading edge of the internal clocks. They rapidly decay and **do not inherently cause errors** as the on-chip comparator is strobed at the end of the clock period.

Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN(+)}$ input voltage at full-scale. For a 640kHz clock frequency with the $V_{IN(+)}$ input at 5V, this DC current is at a maximum of approximately 5μA. Therefore, **bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin** for high resistance sources (> 1kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the effects of the voltage drop across this input resistance, due to the average value of the input current, can be compensated by a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage at a constant conversion rate.

Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, **will not cause errors** since the input currents settle out prior to the comparison time. If a low-pass filter is required in the system, use a low-value series resistor (≤ 1kΩ) for a passive RC section or add an op amp RC active low-pass filter. For low-source-resistance applications, (≤ 1kΩ), a 0.1μF bypass capacitor at the inputs will minimize EMI due to the series lead inductance of a long wire. A 100Ω series resistor can be used to isolate this capacitor (both the R and C are placed outside the feedback loop) from the output of an op amp, if used.

Stray Pickup

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize stray signal pickup (EMI). Both EMI and undesired digital-clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5kΩ. Larger values of source resistance can cause undesired signal pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate this pickup but can create analog scale errors as these capcitors will average the transient input switching currents of the A/D (see **Analog Input Current).** This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be compensated by a full-scale adjustment of the A/D (see **Full-Scale Adjustment)** with the source resistance and input bypass capacitor in place, and the desired conversion rate.

Reference Voltage Span Adjust

For maximum application flexibility, these A/Ds have been designed to accommodate a 5V, 2.5V or an adjusted

Note: All typical values have been guaranteed by characterization and are not tested.

voltage reference. This has been achieved in the design of the IC as shown in Figure 7.

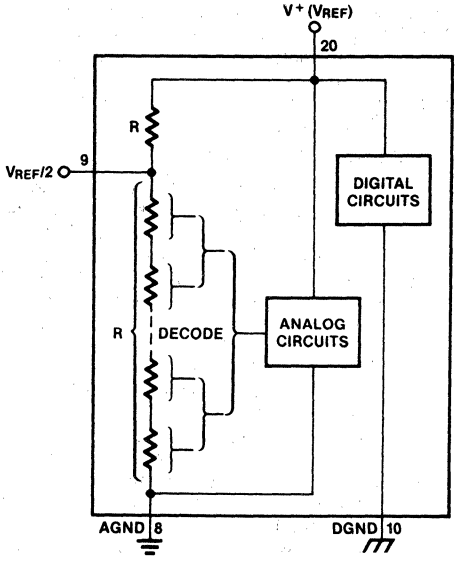


Figure 7: The $V_{REFERENCE}$ Design on the IC

Notice that the reference voltage for the IC is either $\frac{1}{2}$ of the voltage which is applied to the V^+ supply pin, or is equal to the voltage which is externally forced at the $V_{REF}/2$ pin. This allows for a pseudo-ratiometric voltage reference using, for the V^+ supply, a 5V reference voltage. Alternatively, a voltage less than 2.5V can be applied to the $V_{REF}/2$ input. The internal gain to the $V_{REF}/2$ input is 2 to allow this factor of 2 reduction in the reference voltage.

Such an adjusted reference voltage can accommodate a reduced span or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5V to 3.5V, instead of 0V to 5V, the span would be 3V. With 0.5V applied to the $V_{IN(-)}$ pin to absorb the offset, the reference voltage can be made equal to $\frac{1}{2}$ of the 3V span or 1.5V. The A/D now will encode the $V_{IN(+)}$ signal from 0.5V to 3.5V with the 0.5V input corresponding to zero and the 3.5V input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range. The requisite connections are shown in Figure 8. For expanded scale inputs, the circuits of Figures 9 and 10 can be used.

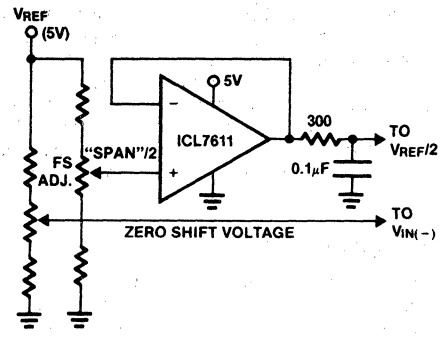


Figure 8: Offsetting the Zero of the ADC0802 and Performing an Input Range (Span) Adjustment

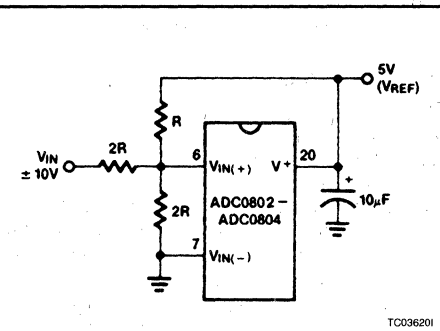


Figure 9: Handling ±10V Analog Input Range

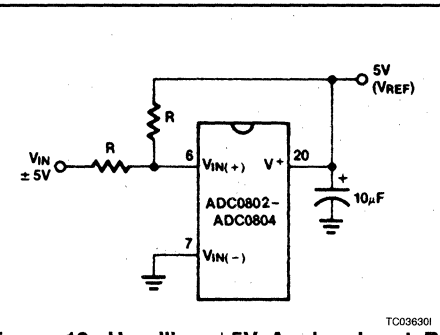


Figure 10: Handling ±5V Analog Input Range

Reference Accuracy Requirements

The converter can be operated in a pseudo-ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. In absolute conversion applications, both the initial value and the temperature stability of the

Note: All typical values have been guaranteed by characterization and are not tested.

reference voltage are important accuracy factors in the operation of the A/D converter. For $V_{REF}/2$ voltages of 2.5V nominal value, initial errors of ±10mV will cause conversion errors of ±1LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20mV (5V span) to 10mV and 1LSB at the $V_{REF}/2$ input becomes 5mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive.

Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN(-)}$ input at this $V_{IN(MIN)}$ value (see **Applications** section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN(-)}$ input and applying a small magnitude positive voltage to the $V_{IN(+)}$ input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8mV for $V_{REF}/2$ = 2.500V).

Full-Scale Adjust

The full-scale adjustment can be made by applying a differential input voltage which is 1½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9) for a digital output code which is just changing from 1111 1110 to 1111 1111. When offsetting the zero and using a span-adjusted $V_{REF}/2$ voltage, the full-scale adjustment is made by inputting V_{MIN} to the $V_{IN(-)}$ input of the A/D and applying a voltage to the $V_{IN(+)}$ input which is given by:

$$V_{IN(+)}\text{fsadj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right],$$

where:

V_{MAX} = the high end of the analog input range

and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

Clocking Option

The clock for the A/D can be derived from an external source such as the CPU clock or an external RC network can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in Figure 11.

Heavy capacitive or DC loading of the CLocK R pin should be avoided as this will disturb normal converter operation. Loads less than 50pF, such as driving up to 7 A/D converter clock inputs from a single CLK R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the CLK R pin (do not use a standard TTL buffer).

Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in progress is not completed. The data from the previous conversion remain in this latch.

Continuous Conversions

In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to insure circuit operation. See Figure 12 for details.

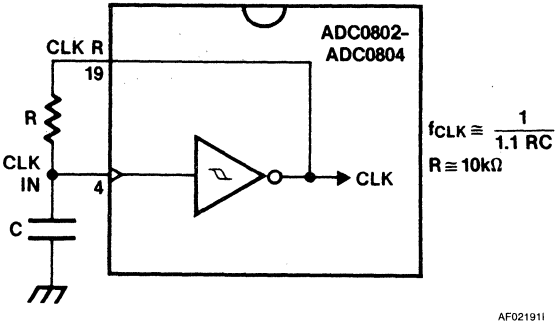


Figure 11: Self-Clocking the A/D

Note: All typical values have been guaranteed by characterization and are not tested.

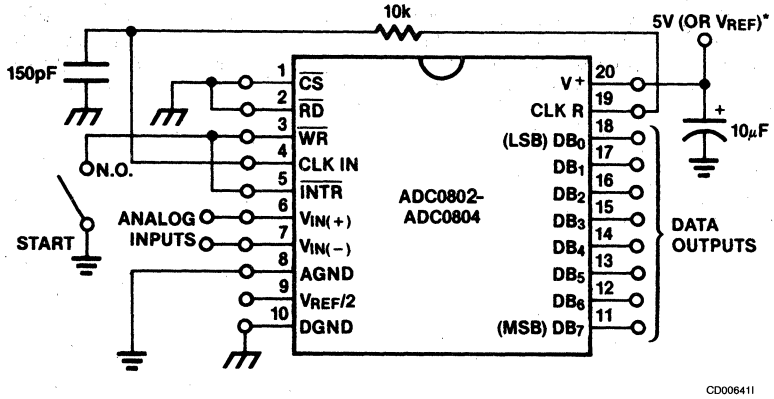


Figure 12: Free-Running Connection

Driving the Data Bus

This CMOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in 3-state (high-impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see **Typical Performance Characteristics).**

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock-extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be 3-state buffers (low power Schottky is recommended, such as the 74LS240 series) or special higher-drive-current products which are designed as bus drivers. High-current bipolar bus drivers with PNP inputs are recommended.

Power Supplies

Noise spikes on the V^+ supply line can cause conversion errors as the comparator will respond to this noise. A low-inductance tantalum filter capacitor should be used close to the converter V^+ pin, and values of 1μF or greater are recommended. If an unregulated voltage is available in the system, a separate 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V^+ supply. An ICL7663 can be used to regulate such a supply from an input as low as 5.2V.

Wiring and Hook-Up Precautions

Standard digital wire-wrap sockets are not satisfactory for breadboarding with this A/D converter. Sockets on PC boards can be used. All logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup; therefore, shielded leads may be necessary in many applications.

A single-point analog ground should be used which is separate from the logic ground points. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of $^1/_4$ LSB can usually be traced to improper board layout and wiring (see **Zero Error** for measurement). Further information can be found in A018.

Note: All typical values have been guaranteed by characterization and are not tested.

TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in Figure 13.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560V and a V^+ supply voltage of 5.12V should be used. This provides an LSB value of 20mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090V (5.120 – 1½ LSB) should be applied to the $V_{IN(+)}$ pin with the $V_{IN(-)}$ pin grounded. The value of the $V_{REF}/2$ input voltage should be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

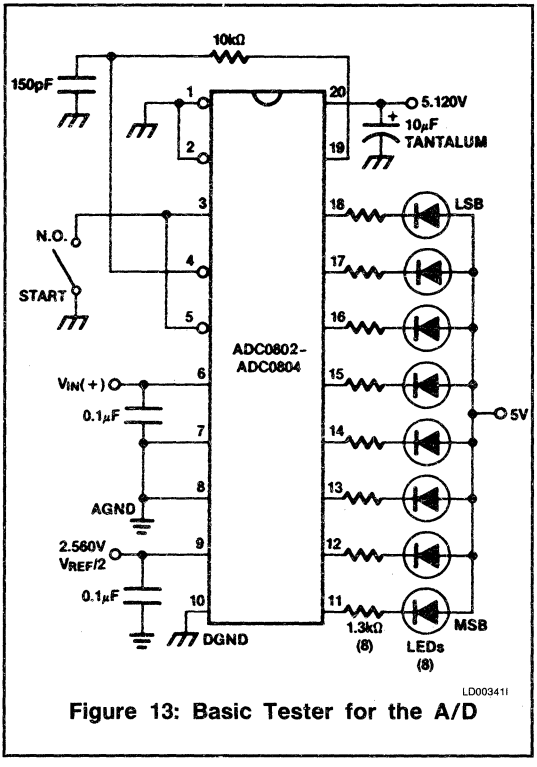


Figure 13: Basic Tester for the A/D

The digital-output LED display can be decoded by dividing the 8 bits into 2 hex characters, one with the 4 most-significant bits (MS) and one with the 4 least-significant bits (LS). The output is then interpreted as a sum of fractions times the full-scale voltage:

$$V_{OUT} = \left(\frac{MS}{16} + \frac{LS}{256}\right)(5.12)V.$$

For example, for an output LED display of 1011 0110, the MS character is hex B (decimal 11) and the LS character is hex (and decimal) 6, so

$$V_{OUT} = \left(\frac{11}{16} + \frac{6}{256}\right)(5.12) = 3.64V.$$

Figures 14 and 15 show more sophisticated test circuits.

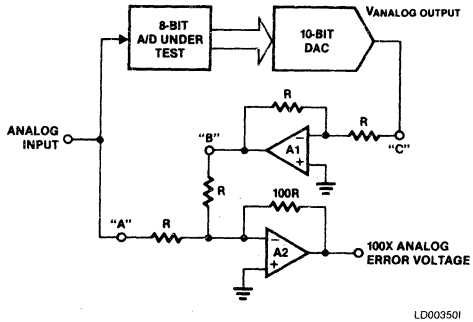


Figure 14: A/D Tester with Analog Error Output. This circuit can be used to generate "error plots" of Figure 6.

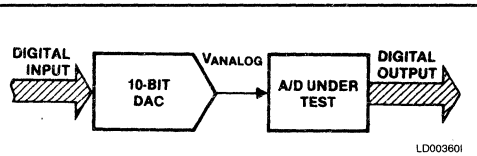


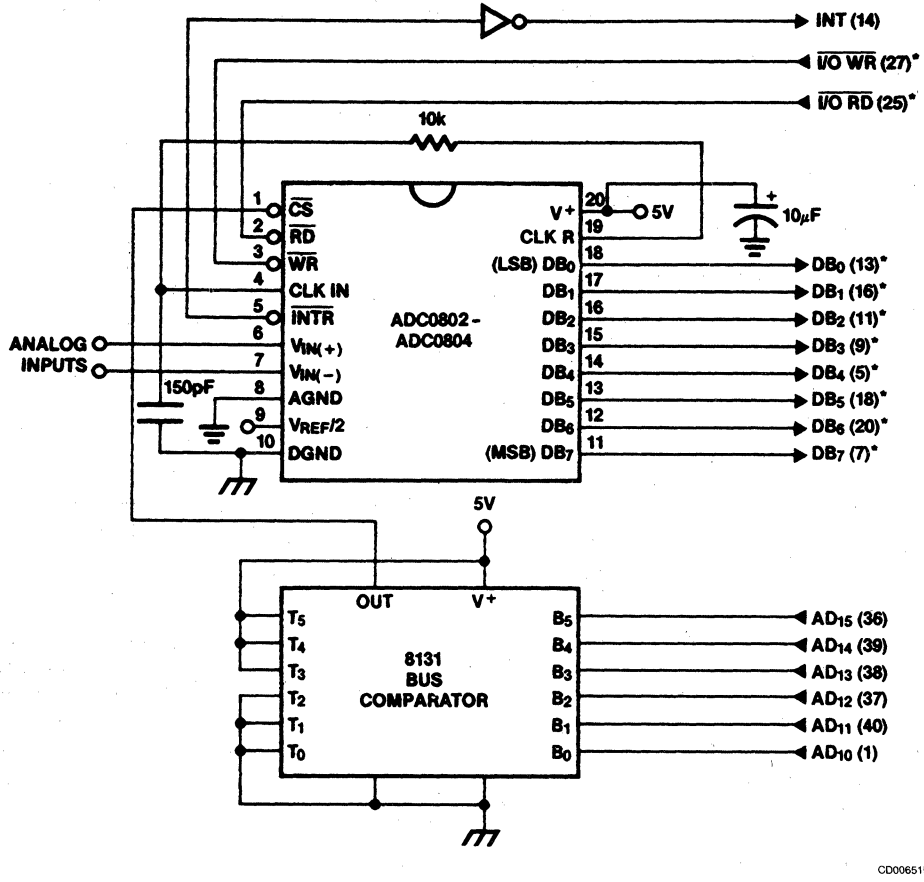
Figure 15: Basic "Digital" A/D Tester

APPLICATIONS

Interfacing 8080/85 or Z-80 Microprocessors

This converter has been designed to directly interface with 8080/85 or Z-80 Microprocessors. The 3-state output capability of the A/D eliminates the need for a peripheral interface device, although address decoding is still required to generate the appropriate $\overline{CS}$ for the converter. The A/D can be mapped into memory space (using standard memory-address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15, since they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder, but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. See A020 for more discussion of memory-mapped vs I/O-mapped interfaces. An example of an A/D in I/O space is shown in Figure 16.

Note: All typical values have been guaranteed by characterization and are not tested.



Note: Pin numbers for 8228 system controller: others are 8080A

Figure 16: ADC0802 to 8080A CPU Interface

The standard control-bus signals of the 8080 ($\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D, since the bus timing requirements, to allow both starting the converter, and outputting the data onto the data bus, are met. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100pF.

It is useful to note that in systems where the A/D converter is 1 of 8 or fewer I/O-mapped devices, no address-decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs, one for each I/O device.

Interfacing the Z-80 and 8085

The Z-80 and 8085 control buses are slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals have to be combined with the generalized strobes to provide the appropriate signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in Figure 17. By using $\overline{MREQ}$ in place of $\overline{IORQ}$, a memory-mapped configuration results.

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

The 8085 also provides a generalized $\overline{RD}$ and $\overline{WR}$ strobe, with an IO/$\overline{M}$ line to distinguish I/O and memory requests. The circuit of Figure 17 can again be used, with IO/$\overline{M}$ in place of $\overline{IORQ}$ for a memory-mapped interface, and an extra inverter (or the logic equivalent) to provide $\overline{IO}$/M for an I/O-mapped connection.

Note: All typical values have been guaranteed by characterization and are not tested.

Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it employs a single R/$\overline{W}$ line and additional timing, if needed, can be derived from the $\phi 2$ clock. All I/O devices are memory-mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. Figure 16 shows an interface schematic where the A/D is memory-mapped in the 6800 system. For simplicity, the $\overline{CS}$ decoding is shown using 1/2 DM8092. Note that in many 6800 systems, an already decoded $\overline{A15}$ line is brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HEX ADDR: 4XXX or 5XXX.

In Figure 19 the ADC0802 series is interfaced to the MC6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory-mapped in the MC6800 system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

APPLICATION NOTES

Some applications bulletins that may be found useful are listed here:

A016 "Selecting A/D Converters," by Dave Fullagar.
A018 "Do's and Dont's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.
A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Sliger.
A030 "The ICL7104 — A Binary Output A/D Converter for Microprocessors," by Peter Bradshaw.
R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976.

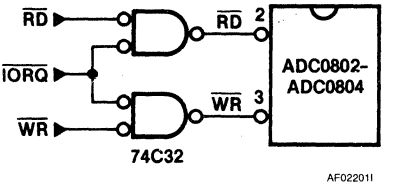
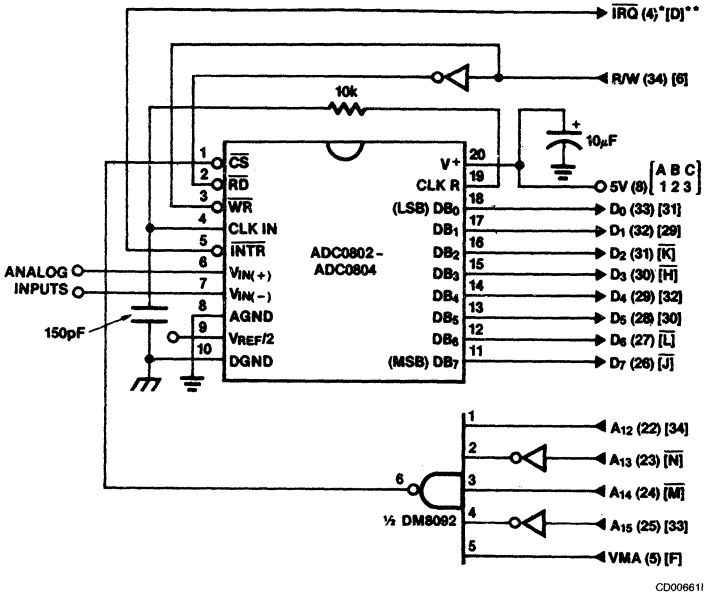


Figure 17: Mapping the A/D as an I/O device for use with the Z-80 CPU



***Note 1:** Numbers in parentheses refer to MC6800 CPU pinout.
****Note 2:** Numbers or letters in brackets refer to standard MC6800 system common bus code.

Figure 18: ADC0802 to MC6800 CPU Interface

Note: All typical values have been guaranteed by characterization and are not tested.

ADC0802-ADC0804

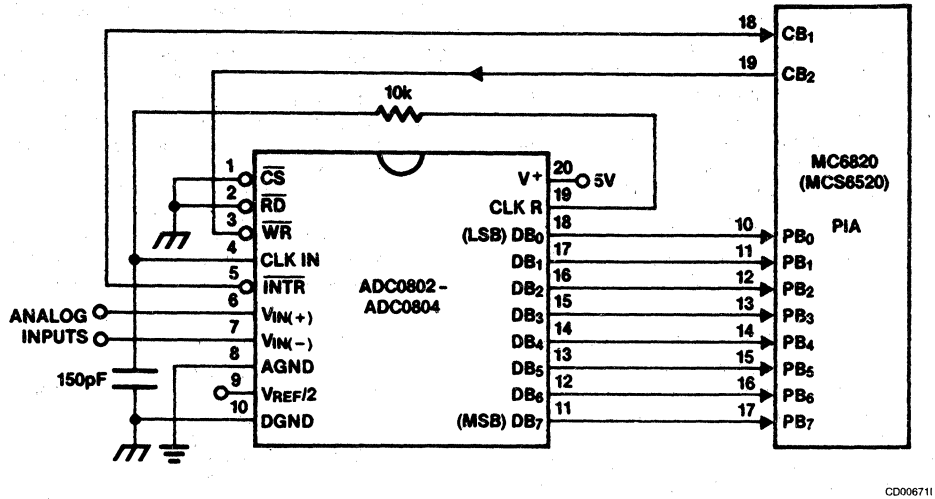


Figure 19: ADC0802 to MC6820 PIA Interface

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7106/ICL7107

3½-Digit LCD/LED Single-Chip A/D Converter

GENERAL DESCRIPTION

The Intersil ICL7106 and 7107 are high performance, low power 3½-digit A/D converters containing all the necessary active devices on a single CMOS I.C. Included are seven-segment decoders, display drivers, a reference, and a clock. The 7106 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive; the 7107 will directly drive an instrument-size light emitting diode (LED) display.

The 7106 and 7107 bring together an unprecedented combination of high accuracy, versatility, and true economy. It features auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10 pA max., and rollover error of less than one count. True differential inputs and reference are useful in all systems, but give the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. Finally, the true economy of single power supply operation (7106), enables a high performance panel meter to be built with the addition of only 10 passive components and a display.

FEATURES

- **Guaranteed Zero Reading for 0 Volts Input on All Scales**
- **True Polarity at Zero for Precise Null Detection**
- **1pA Typical Input Current**
- **True Differential Input and Reference**
- **Direct Display Drive — No External Components Required — LCD ICL7106**
  — LED ICL7107
- **Low Noise–Less Than 15μV p-p**
- **On-Chip Clock and Reference**
- **Low Power Dissipation–Typically Less Than 10mW**
- **No Additional Active Circuits Required**
- **New Small Outline Surface Mount Package Available**
- **Evaluation Kit Available**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7106CDL	0°C to +70°C	40 pin ceramic DIP
ICL7106CPL	0°C to +70°C	40 pin plastic DIP
ICL7106CJL	0°C to +70°C	40 pin CERDIP
ICL7106CM44	0°C to +70°C	44 pin Surface Mount
ICL7107CJL	0°C to +70°C	40 pin CERDIP
ICL7107CDL	0°C to +70°C	40 pin ceramic DIP
ICL7107CPL	0°C to +70°C	40 pin plastic DIP
ICL7106EV/Kit ICL7107EV/Kit	Evaluation kits contain IC, display, circuit board, passive components and hardware.	

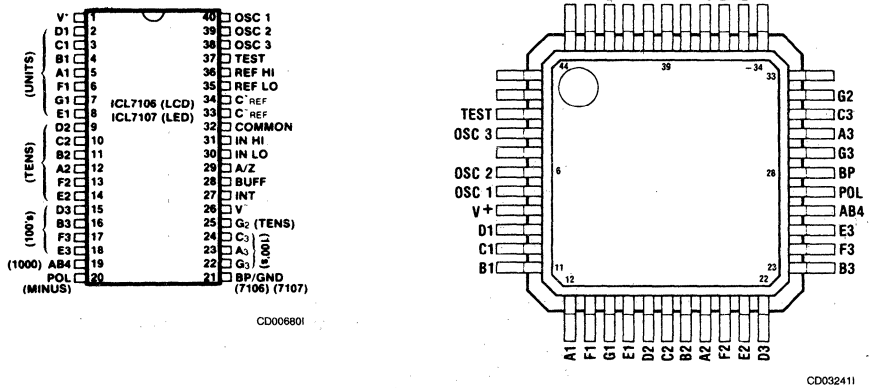


Figure 1: Pin Configurations

301650-002

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7106/ICL7107

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- ICL7106, V^+ to V^- 15V
- ICL7107, V^+ to GND ..... +6V
- ICL7107, V^- to GND ..... −9V

Analog Input Voltage (either input)(Note 1) ... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input
- ICL7106 ..... TEST to V^+
- ICL7107 ..... GND to V^+

Power Dissipation (Note 2)
- Ceramic Package 1000mW
- Plastic Package 800mW

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

ELECTRICAL CHARACTERISTICS (Note 3)

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative inputs near Full Scale)	$-V_{IN} = +V_{IN} \simeq$ 200.0mV	−1	±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200.0mV or full scale = 2.000V (Note 6)	−1	±.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		μV
Leakage Current Input	V_{IN} = 0 (Note 6)		1	10	pA
Zero Reading Drift	V_{IN} = 0 0° < T_A < 70°C (Note 6)		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° < T_A < 70°C (Ext. Ref. Oppm/°C) (Note 6)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current for 7107)	V_{IN} = 0		0.8	1.8	mA
V^- Supply Current (7107 only)			0.6	1.8	mA
Analog Common Voltage (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply		80		ppm/°C
7106 ONLY Pk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
7107 ONLY Segment Sinking Current (Except Pin 19 & 20)	V^+ = 5.0V Segment voltage = 3V	5	8.0		mA
(Pin 19 only) (Pin 20 only)		10 4	16 7		mA

NOTES: 3. Unless otherwise noted, specifications apply to both the 7106 and 7107 at T_A = 25°C, f_{clock} = 48kHz. 7106 is tested in the circuit of Figure 4. 7107 is tested in the circuit of Figure 5.
4. Refer to "Differential Input" discussion.
5. Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
6. Not tested, guaranteed by design.

Note: All typical values have been guaranteed by characterization and are not tested.

TEST CIRCUITS

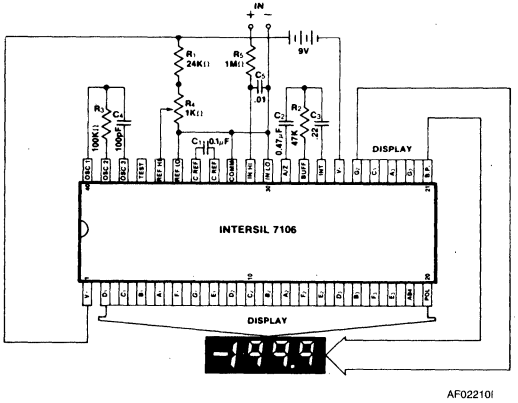


Figure 2: ICL7106 Test Circuit and Typical Application With Liquid Crystal Display

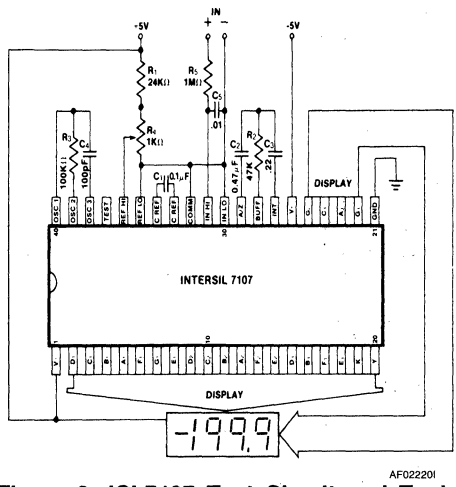


Figure 3: ICL7107 Test Circuit and Typical Application With LED Display

DETAILED DESCRIPTION

Analog Section

Figure 4 shows the Analog Section for the ICL7106 and 7107. Each measurement cycle is divided into three phases. They are (1) auto-zero (A/Z), (2) signal integrate (INT) and (3) de-integrate (DE).

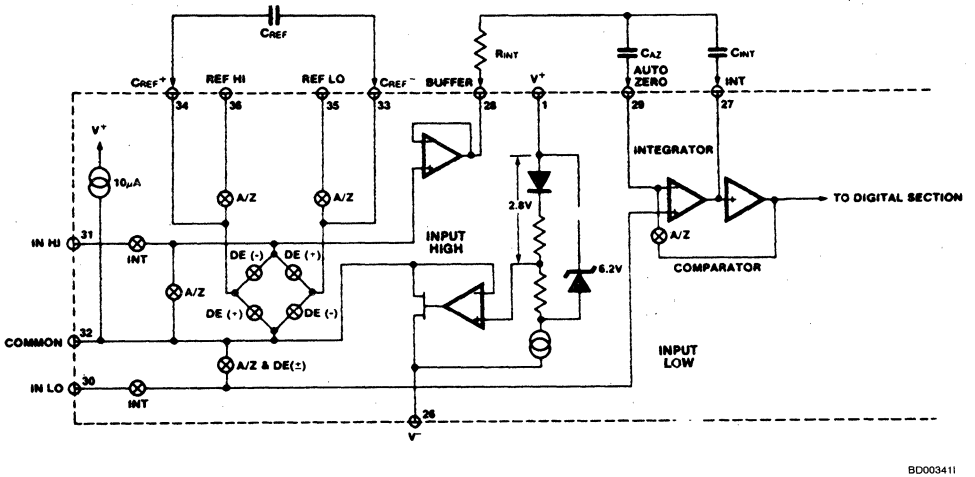


Figure 4: Analog Section of 7106/7107

Note: All typical values have been guaranteed by characterization and are not tested.

Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A/Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

Signal Integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range: up to one volt from either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is $1000\left(\frac{V_{IN}}{V_{REF}}\right)$.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier, or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range, the system has a CMRR of 86 dB typical. However, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator output swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing to within 0.3 volts of either supply without loss of linearity. See A032 for a discussion of the effects of stray capacitance.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for positive or negative input voltage will give a roll-over error. However, by selecting the reference capacitor such that it is large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count worst case. (See Component Value Selection.)

Analog COMMON

This pin is included primarily to set the common mode voltage for battery operation (7106) or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, the analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (> 7V), the COMMON voltage will have a low voltage coefficient (0.001%/V), low output impedance ($\simeq$15Ω), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on-chip reference should also be recognized, however. With the 7107, the internal heating which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full scale from 25 μV to 80μVp-p. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111(8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an overrange condition. This is because overrange is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between overrange and a nonoverrange count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

The 7106, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added, as shown in Figure 5.

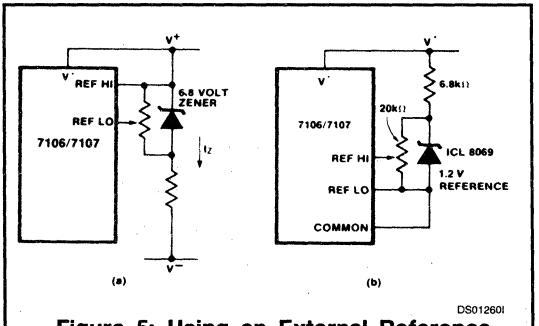


Figure 5: Using an External Reference

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for

Note: All typical values have been guaranteed by characterization and are not tested.

instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently tied to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET that can sink approximately 30mA of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10μA of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

TEST

The TEST pin serves two functions. On the 7106 it is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 8 and 9 show such an application. No more than a 1mA load should be applied.

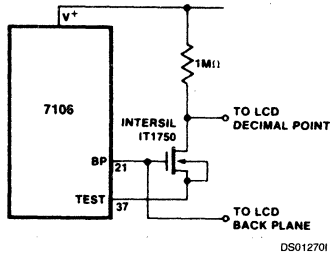


Figure 6: Simple Inverter for Fixed Decimal Point

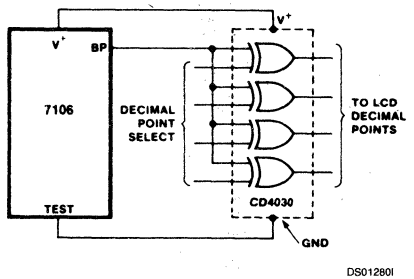


Figure 7: Exclusive 'OR' Gate for Decimal Point Drive

The second function is a "lamp test". When TEST is pulled high (to V^+) all segments will be turned on and the display should read — 1888. The TEST pin will sink about 10mA under these conditions.

Caution: on the 7106, in the lamp test mode, the segments have a constant DC voltage (no square-wave) and may burn the LCD display if left in this mode for several minutes.

DIGITAL SECTION

Figures 8 and 9 show the digital section for the 7106 and 7107, respectively. In the 7106, an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments.

Figure 9 is the Digital Section of the 7107. It is identical to the 7106 except that the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2 to 8 mA, typical for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16mA.

In both devices, the polarity indication is "on" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7106/ICL7107

DISPLAY FONT

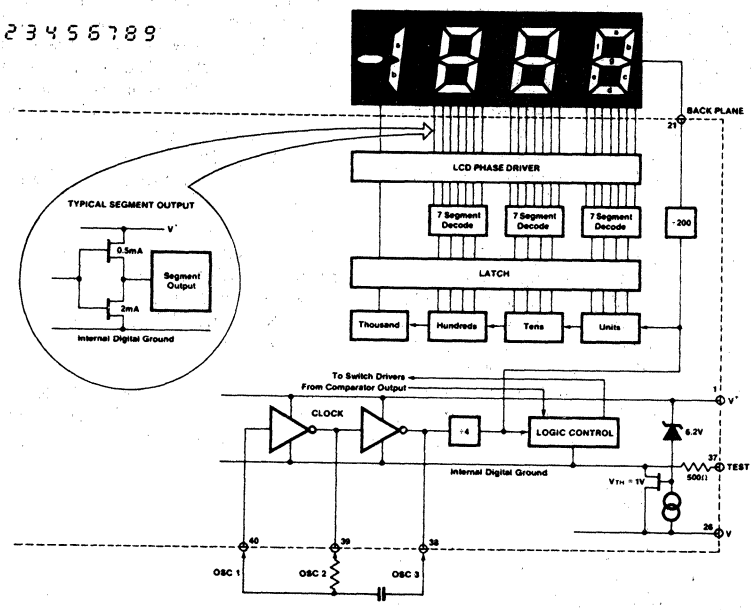


Figure 8: Digital Section 7106

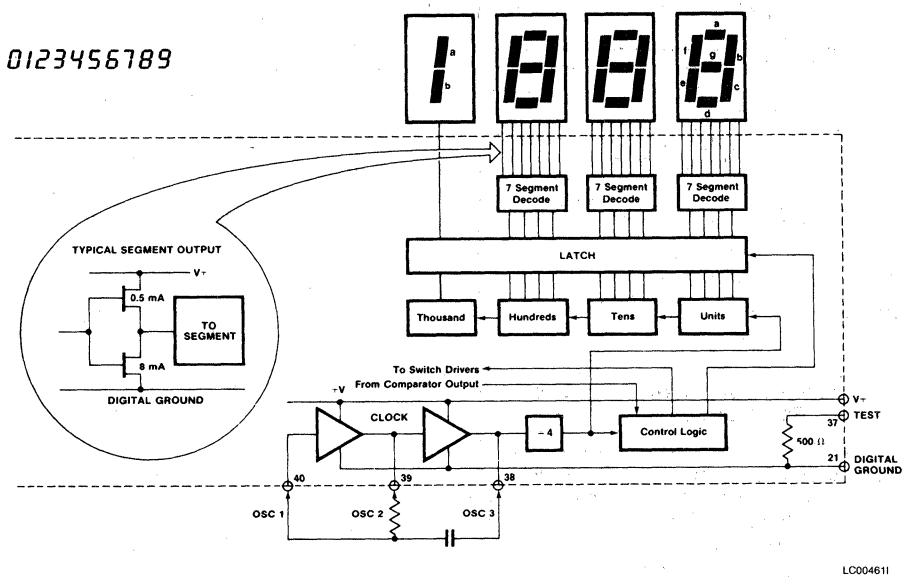


Figure 9: Digital Section 7107

Note: All typical values have been guaranteed by characterization and are not tested.

System Timing

Figure 10 shows the clocking arrangement used in the 7106 and 7107. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

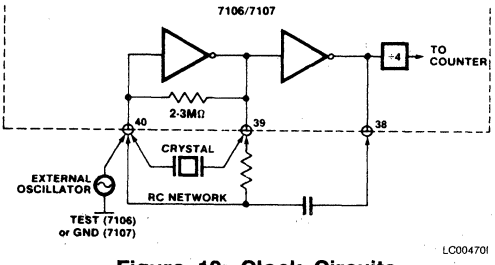


Figure 10: Clock Circuits

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 counts (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, 33 1/3kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, 66 2/3 kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

COMPONENT VALUE SELECTION

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They can supply 20μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full scale, 470kΩ is near optimum and similarly a 47kΩ for a 200.0 mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the 7106 or the 7107, when the analog COMMON is used as a reference, a nominal ±2 volt full scale integrator swing is fine. For the 7107 with ±5 volt supplies and analog COMMON tied to supply ground, a ±3.5 to ±4 volt swing is nominal. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.22μF and 0.10μF, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is that it must have a low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full scale where noise is very important, a 0.47μF capacitor is recommended. On the 2 volt scale, a 0.047μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e. the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally 1.0μF will hold the roll-over error to 0.5 count in this instance.

Oscillator Components

For all ranges of frequency a 100kΩ resistor is recommended and the capacitor is selected from the equation $f = \frac{0.45}{RC}$. For 48kHz clock (3 readings/second), C = 100pF.

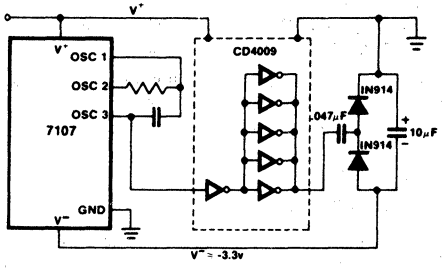
Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200.0mV and 2.000 volt scale, Vref should equal 100.0 mV and 1.000 volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select $V_{REF} = 0.341V$. Suitable values for integrating resistor and capacitor would be 120kΩ and 0.22μF. This makes the system slightly quieter and also avoids a divider network on the input. The 7107 with ±5V supplies can accept input signals up to ±4V. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

7107 Power Supplies

The 7107 is designed to work from ±5V supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors, and an inexpensive I.C. Figure 11 shows this application. See ICL7660 data sheet for an alternative.

Note: All typical values have been guaranteed by characterization and are not tested.



LC00480I

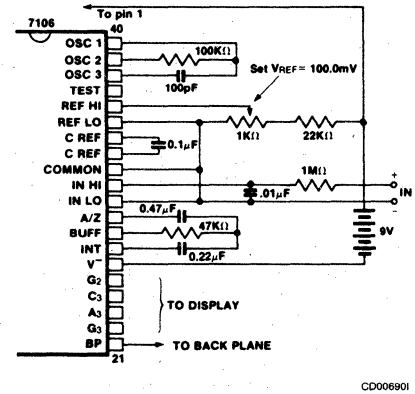
Figure 11: Generating Negative Supply from +5V

In fact, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5 volts.
3. An external reference is used.

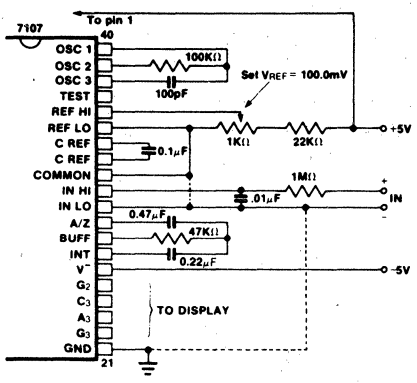
TYPICAL APPLICATIONS

The 7106 and 7107 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.



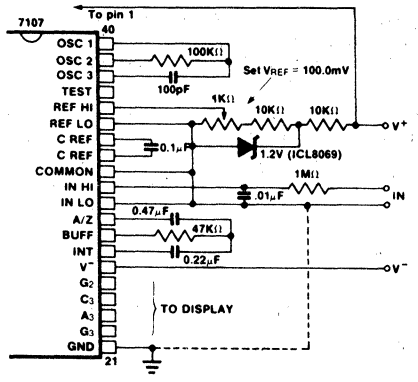
CD00690I

Figure 12: 7106 using the internal reference. Values shown are for 200.0 mV full scale, 3 readings per second, floating supply voltage (9V battery).



CD00700I

Figure 13: 7107 using the internal reference. Values shown are for 200.0mV full scale, 3 readings per second. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog COMMON.)

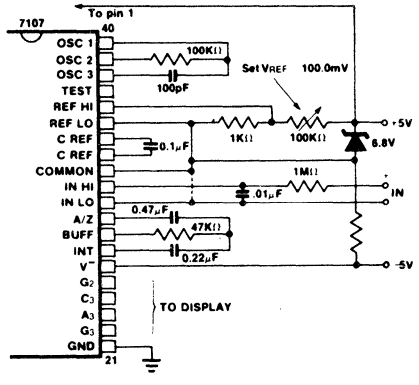


CD00710I

Figure 14: 7107 with an external band-gap reference (1.2V type). IN LO is tied to COMMON, thus establishing the correct common mode voltage. If COMMON is not shorted to GND, the input voltage may float with respect to the power supply and COMMON acts as a pre-regulator for the reference. If COMMON is shorted to GND, the input is single ended (referred to supply ground) and the pre-regulator is over-ridden.

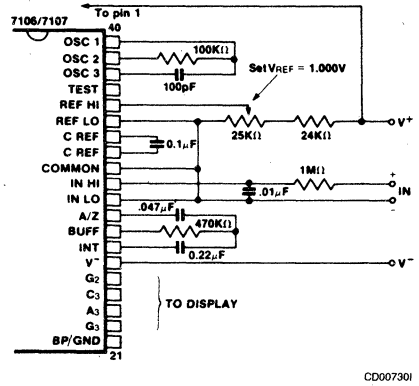
Note: All typical values have been guaranteed by characterization and are not tested.

TYPICAL APPLICATIONS (CONT.)



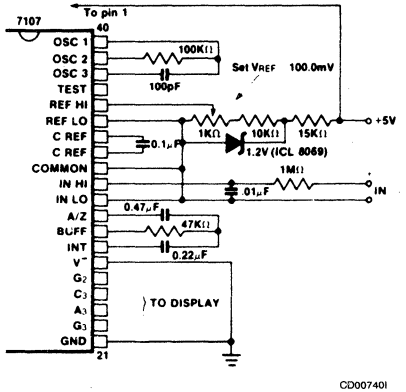
CD00720I

Figure 15: 7107 with Zener diode reference. Since low T.C. zeners have breakdown voltages ~ 6.8V, diode must be placed across the total supply (10V). As in the case of Figure 15, IN LO may be tied to either COMMON or GND.



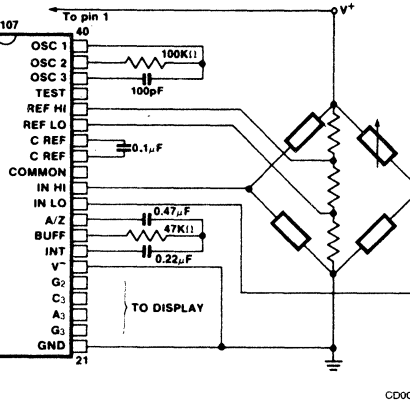
CD00730I

Figure 16: 7106/7107: Recommended component values for 2.000V full scale.



CD00740I

Figure 17: 7107 operated from single +5V supply. An external reference must be used in this application, since the voltage between V^+ and V^- is insufficient for correct operation of the internal reference.



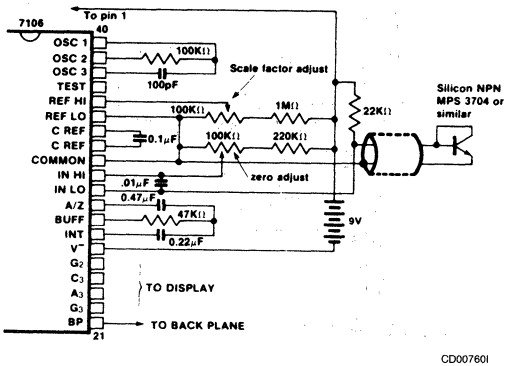
CD00750I

Figure 18: 7107 measuring ratiometric values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

Note: All typical values have been guaranteed by characterization and are not tested.

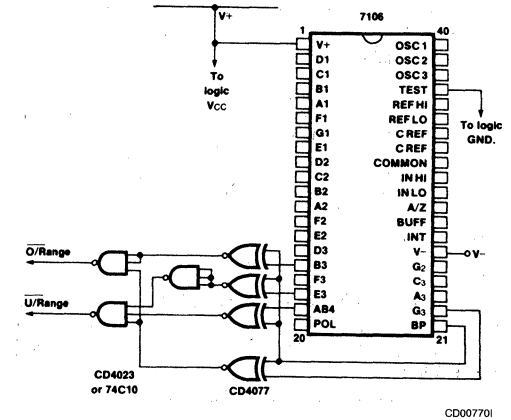
ICL7106/ICL7107

TYPICAL APPLICATIONS (CONT.)



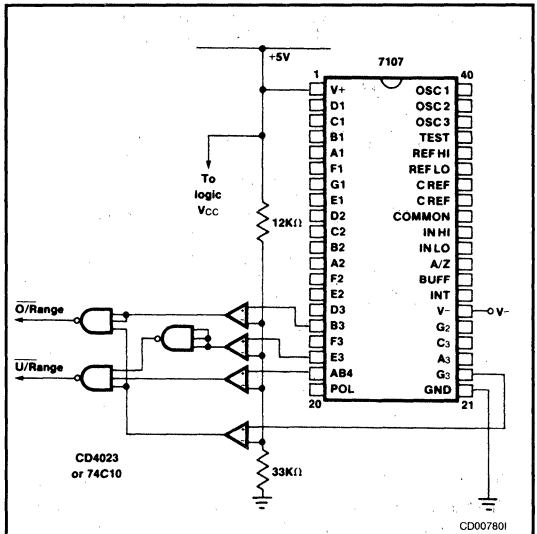
CD00760I

Figure 19: 7106 used as a digital centigrade thermometer. A silicon diode-connected transistor has a temperature coefficient of about −2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.



CD00770I

Figure 20: Circuit for developing Underrange and Overrange signals from 7106 outputs.



CD00780I

Figure 21: Circuit for developing Underrange and Overrange signals from 7107 outputs. The LM339 is required to ensure logic compatibility with heavy display loading.

7106/7107 EVALUATION KITS

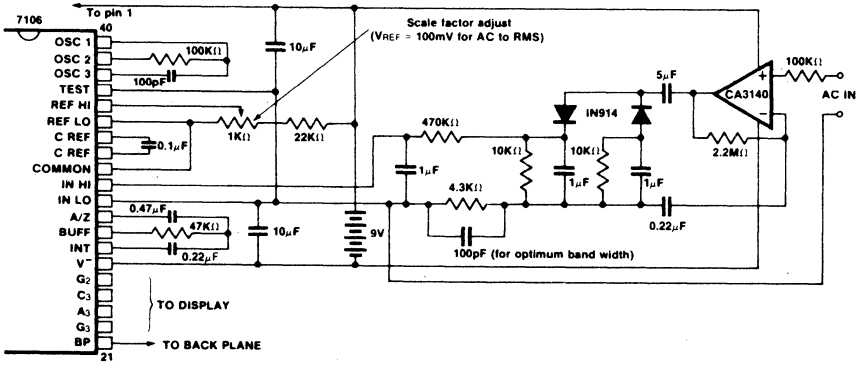
After purchasing a sample of the 7106 or the 7107, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application. However, locating and purchasing even the small number of additional components required, then wiring a breadboard, can often cause delays of days or sometimes weeks. To avoid this problem and facilitate evaluation of these unique circuits, Intersil is offering a kit which contains all the necessary components to build a 3½-digit panel meter. With the help of this kit, an engineer or technician can have the system "up and running" in about half an hour.

Two kits are offered, the ICL7106EV/KIT and the ICL7107EV/KIT. Both contain the appropriate IC, a circuit board, a display (LCD for 7106EV/KIT, LEDs for 7107EV/KIT), passive components, and miscellaneous hardware.

APPLICATION NOTES

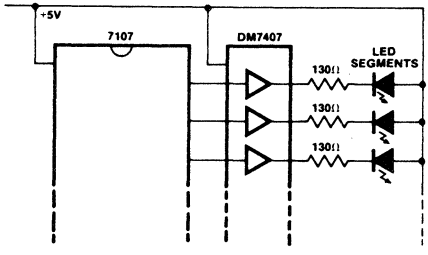
A016 "Selecting A/D Converters", by David Fullagar.
A017 "The Integrating A/D Converter", By Lee Evans.
A018 "Do's and Don'ts of Applying A/D Converters", by Peter Bradshaw and Skip Osgood.
A019 "4½-Digit Panel Meter Demonstrator/Instrumentation Boards", by Michael Dufort.
A023 "Low Cost Digital Panel Meter Designs", by David Fullagar and Michael Dufort.
A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106/7/9 Family", by Peter Bradshaw.
A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106", by Larry Goff.
A052 "Tips for Using Single-Chip 3½-Digit A/D Converters", by Dan Watson.

Note: All typical values have been guaranteed by characterization and are not tested.



CD007901

Figure 22: AC to DC Converter with 7106. TEST is used as a common mode reference level to ensure compatibility with most op-amps.



DS012901

Figure 23: Display Buffering for increased drive current. Requires four DM7407 Hex Buffers. Each buffer is capable of sinking 40 mA.

6

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7109
12-Bit μP-Compatible A/D Converter

GENERAL DESCRIPTION

The ICL7109 is a high performance, CMOS, low power integrating A/D converter designed to easily interface with microprocessors.

The output data (12 bits, polarity and overrange) may be directly accessed under control of two byte enable inputs and a chip select input for a simple parallel bus interface. A UART handshake mode is provided to allow the ICL7109 to work with industry-standard UARTs in providing serial data transmission, ideal for remote data logging applications. The RUN/HOLD input and STATUS output allow monitoring and control of conversion timing.

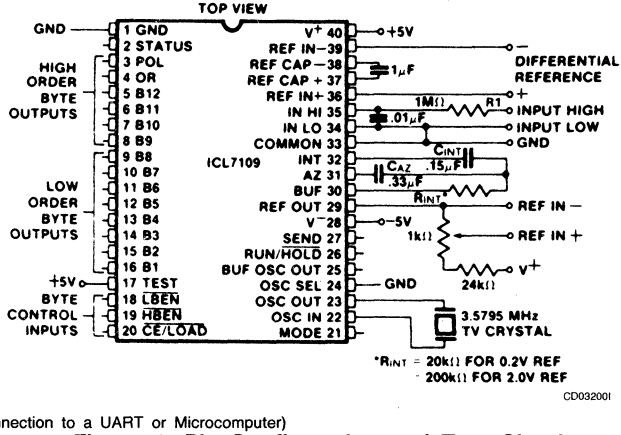
The ICL7109 provides the user with the high accuracy, low noise, low drift, versatility and economy of the dual-slope integrating A/D converter. Features like true differential input and reference, drift of less than 1μV/°C, maximum input bias current of 10pA, and typical power consumption of 20mW make the ICL7109 an attractive per-channel alternative to analog multiplexing for many data acquisition applications.

FEATURES

- **12 Bit Binary (Plus Polarity and Overrange) Dual Slope Integrating Analog-to-Digital Converter**
- **Byte-Organized TTL-Compatible Three-State Outputs and UART Handshake Mode for Simple Parallel or Serial Interfacing to Microprocessor Systems**
- **RUN/HOLD Input and STATUS Output Can Be Used to Monitor and Control Conversion Timing**
- **True Differential Input and Differential Reference**
- **Low Noise — Typically 15μV p-p**
- **1pA Typical Input Current**
- **Operates At Up to 30 Conversions Per Second**
- **On-Chip Oscillator Operates With Inexpensive 3.58MHz TV Crystal Giving 7.5 Conversions Per Second for 60Hz Rejection May Also Be Used With An RC Network Oscillator for Other Clock Frequencies**

ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ICL7109MDL	−55°C to +125°C	40-Pin Ceramic DIP
ICL7109IDL	−25°C to +85°C	40-Pin Ceramic DIP
ICL7109IJL	−25°C to +85°C	40-Pin CERDIP
ICL7109CPL	0°C to 70°C	40-Pin Plastic DIP



(See Figure 2 for typical connection to a UART or Microcomputer)

Figure 1: Pin Configuration and Test Circuit

Note: All typical values have been guaranteed by characterization and are not tested.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (GND to V^+) ..... +6.2V
Negative Supply Voltage (GND to V^-) ..... -9V
Analog Input Voltage (Lo or Hi) (Note 1) ..... V^+ to V^-
Reference Input Voltage (Lo or Hi) (Note 1) .. V^+ to V^-
Digital Input Voltage V^+ +0.3V
(Pins 2-27) (Note 2) ..... GND -0.3V

Power Dissipation (Note 3)
Ceramic Package ..... 1W @ +85°C
Plastic Package ..... 500mW @ +70°C
Operating Temperature
Ceramic Package (MDL) ..... -55°C to +125°C
Ceramic Package (IDL) ..... -25°C to +85°C
Plastic Package (CPL) ..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS ($V^+ = +5V$, $V^- = -5V$, GND = 0V, $T_A = 25°C$, unless otherwise indicated.) Test circuit as shown on first page of this data sheet.

ANALOG SECTION

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Zero Input Reading	V_{IN} = 0.0V Full Scale = 409.6mV	-0000_8	$\pm0000_8$	$+0000_8$	Octal Reading
	Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 204.8mV	3777_8	3777_8 4000_8	4000_8	Octal Reading
	Non-Linearity (Max deviation from best straight line fit)	Full Scale = 409.6mV to 2.048V Over full operating temperature range. (Note 4), (Note 6)	-1	±.2	+1	Counts
	Roll-over Error (difference in reading for equal pos. and neg. inputs near full scale)	Full Scale = 409.6mV to 2.048V (Note 5), (Note 6)	-1	±.2	+1	Counts
CMRR	Common Mode Rejection Ratio	V_{CM} ±1V V_{IN} = 0V Full Scale = 409.6mV		50		μV/V
VCMR	Input Common Mode Range	Input Hi, Input Lo, Common (Note 4)	V^- +1.5		V^+ -1.0	V
e_n	Noise (p-p value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 409.6mV		15		μV
I_{ILK}	Leakage current at Input	V_{IN} = 0 All devices at 25°C ICL7109CPL 0°C ≤ T_A ≤ +70°C (Note 4) ICL7109IDL -25°C ≤ T_A ≤ +85°C (Note 4) ICL7109MDL -55°C ≤ T_A ≤ +125°C		1 20 100 2	10 100 250 5	pA pA pA nA
	Zero Reading Drift	V_{IN} = 0V R_1 = 0Ω (Note 4)		0.2	1	μV/°C
	Scale Factor Temperature Coefficient	V_{IN} = 408.9mV = $>7770_8$ reading Ext. Ref. 0 ppm/°C (Note 4)		1	5	ppm/°C
I^+	Supply Current V^+ to GND	V_{IN} = 0, Crystal Osc 3.58MHz test circuit		700	1500	μA
I_{SUPP}	Supply Current V^+ to V^-	Pins 2-21, 25, 26, 27, 29; open		700	1500	μA
V_{REF}	Ref Out Voltage	Referred to V^+, 25kΩ between V^+ and REF OUT	-2.4	-2.8	-3.2	V
	Ref Out Temp. Coefficient	25kΩ between V^+ and REF OUT		80		ppm/°C

DIGITAL SECTION

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output High Voltage	I_{OUT} = 100μA Pins 2-16, 18, 19, 20	3.5	4.3		V
V_{OL}	Output Low Voltage	I_{OUT} = 1.6mA		0.2	0.4	V
	Output Leakage Current	Pins 3-16 high impedance		±.01	±1	μA
	Control I/O Pullup Current	Pins 18, 19, 20 $V_{OUT} = V^+ - 3V$ MODE input at GND		5		μA
	Control I/O Loading	$\overline{HBEN}$ Pin 19 $\overline{LBEN}$ Pin 18			50	pF
V_{IH}	Input High Voltage	Pins 18-21, 26, 27 referred to GND	2.5			V
V_{IL}	Input Low Voltage	Pins 18-21, 26, 27 referred to GND			1	V

Note: All typical values have been guaranteed by characterization and are not tested.

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INTERSIL

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input Pull-up Current		Pins 26, 27 $V_{OUT} = V^+ - 3V$		5		μA
	Input Pull-up Current		Pins 17, 24 $V_{OUT} = V^+ - 3V$		25		μA
	Input Pull-down Current		Pin 21 V_{OUT} = GND + 3V		5		μA
O_{OH}	Octillator Output	High	V_{OUT} = 2.5V		1		mA
O_{OL}	Current	Low	V_{OUT} = 2.5V		1.5		mA
BO_{OH}	Buffered Oscillator	High	V_{OUT} = 2.5V		2		mA
BO_{OL}	Output Current	Low	V_{OUT} = 2.5V		5		mA
t_W	MODE Input Pulse Width		(Note 4)	50			ns

NOTES:
1. Input voltages may exceed the supply voltages provided the input current is limited to ±100μA
2. Due to the SCR structure inherent in the process used to fabricate these devices, connecting any digital inputs or outputs to voltages greater than V^+ or less than GND may cause destructive device latchup. For this reason it is recommended that no inputs from sources other than the same power supply be applied to the ICL7109 before its power supply is established, and that in multiple supply systems the supply to the ICL7109 be activated first.
3. This limit refers to that of the package and will not be obtained during normal operation.
4. This parameter is not production tested, but is guaranteed by design.
5. Roll-over error for T_A = −55°C to +125°C is ±3 counts maximum.
6. A full scale voltage of 2.048V is used because a full scale voltage of 4.096V exceeds the devices Common Mode Voltage Range.

TABLE 1: — Pin Assignment and Function Description

PIN	SYMBOL	DESCRIPTION		
1	GND	Digital Ground, 0V. Ground return for all digital logic.		
2	STATUS	Output High during integrate and deintegrate until data is latched. Output Low when analog section is in Auto-Zero configuration.		
3	POL	Polarity — HI for Positive input.		All three state output data bits
4	OR	Overrange — HI if Overranged.		
5	B12	Bit 12	(Most Significant Bit)	
6	B11	Bit 11		
7	B10	Bit 10		
8	B9	Bit 9		
9	B8	Bit 8		
10	B7	Bit 7	HI = true	
11	B6	Bit 6		
12	B5	Bit 5		
13	B4	Bit 4		
14	B3	Bit 3		
15	B2	Bit 2		
16	B1	Bit 1	(Least Significant Bit)	
17	TEST	Input High — Normal Operation. Input Low — Forces all bit outputs high. Note: This input is used for test purposes only. Tie high if not used.		
18	$\overline{LBEN}$	Low Byte Enable — With Mode (Pin 21) low, and $\overline{CE/LOAD}$ (Pin 20) low, taking this pin low activates low order byte outputs B1 — B8. — With Mode (Pin 21) high, this pin serves as a low byte flag output used in handshake mode. See Figures 8, 9, 10.		
19	$\overline{HBEN}$	High Byte Enable — With Mode (Pin 21) low, and $\overline{CE/LOAD}$ (Pin 20) low, taking this pin low activates high order byte outputs B9 — B12, POL, OR. — With Mode (Pin 21) high, this pin serves as a high byte flag output used in handshake mode. See Figures 8, 9, 10.		

PIN	SYMBOL	DESCRIPTION
20	$\overline{CE/LOAD}$	Chip Enable Load — With Mode (Pin 21) low. $\overline{CE/LOAD}$ serves as a master output enable. When high, B1 — B12, POL, OR outputs are disabled. — With Mode (Pin 21) high, this pin serves as a load strobe used in handshake mode. See Figures 8, 9, 10.
21	MODE	Input Low — Direct output mode where $\overline{CE/LOAD}$ (Pin 20), $\overline{HBEN}$ (Pin 19) and $\overline{LBEN}$ (Pin 18) act as inputs directly controlling byte outputs. Input Pulsed High — Causes immediate entry into handshake mode and output of data as in Figure 10. Input High — Enables $\overline{CE/LOAD}$ (Pin 20), $\overline{HBEN}$ (Pin 19), and $\overline{LBEN}$ (Pin 18) as outputs, handshake mode will be entered and data output as in Figures 8 and 9 at conversion completion.
22	OSC IN	Oscillator Input
23	OSC OUT	Oscillator Output
24	OSC SEL	Oscillator Select — Input high configures OSC IN, OSC OUT, BUF OSC OUT as RC oscillator — clock will be same phase and duty cycle as BUF OSC OUT. — Input low configures OSC IN, OSC OUT for crystal oscillator — clock frequency will be 1/58 of frequency at BUF OSC OUT.
25	BUF OSC OUT	Buffered Oscillator Output
26	RUN/$\overline{HOLD}$	Input High — Conversions continuously performed every 8192 clock pulses. Input Low — Conversion in progress completed, converter will stop in Auto-Zero 7 counts before integrate.
27	SEND	Input — Used in handshake mode to indicate ability of an external device to accept data. Connect to +5V if not used.
28	V^-	Analog Negative Supply — Nominally −5V with respect to GND (Pin 1).
29	REF OUT	Reference Voltage Output — Nominally 2.8V down from V* (Pin 40).
30	BUFFER	Buffer Amplifier Output

Note: All typical values have been guaranteed by characterization and are not tested.

PIN	SYMBOL	DESCRIPTION
31	AUTO-ZERO	Auto-Zero Node — Inside foil of C_{AZ}
32	INTEGRATOR	Integrator Output — Outside foil of C_{INT}
33	COMMON	Analog Common — System is Auto-Zeroed to COMMON
34	INPUT LO	Differential Input Low Side
35	INPUT HI	Differential Input High Side

PIN	SYMBOL	DESCRIPTION
36	REF IN +	Differential Reference Input Positive
37	REF CAP +	Reference Capacitor Positive
38	REF CAP	Reference Capacitor Negative
39	REF IN	Differential Reference Input Negative
40	V^+	Positive Supply Voltage — Nominally +5V with respect to GND (Pin 1).

Note: All digital levels are positive true.

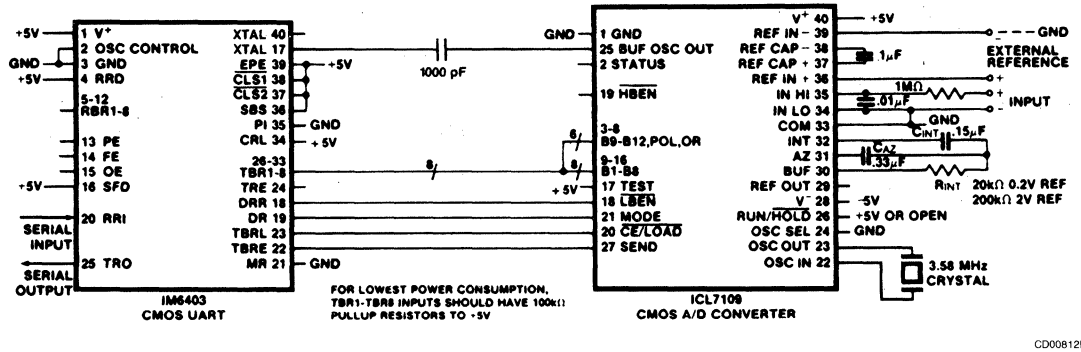


Figure 2A: Typical Connection Diagram UART Interface– To transmit latest result, send any word to UART

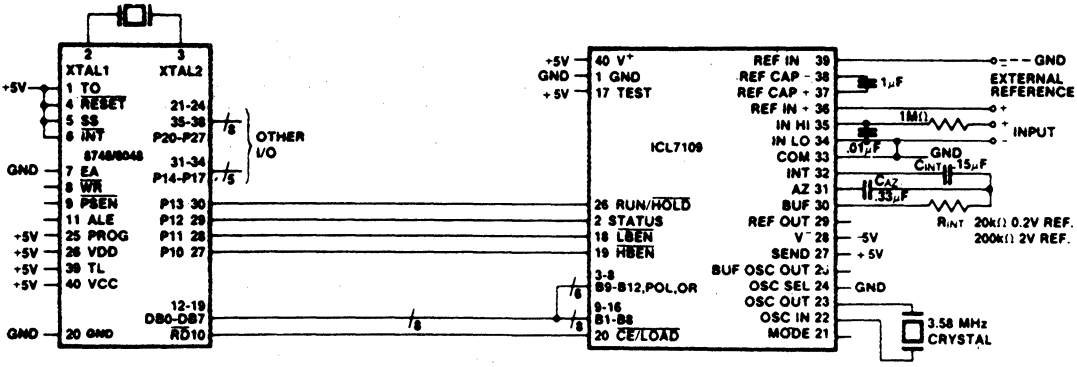


Figure 2B: Typical Connection Diagram Parallel Interface With 8048 Microcomputer

DETAILED DESCRIPTION

Analog Section

Figure 3 shows the equivalent circuit of the Analog Section of the ICL7109. When the RUN/$\overline{HOLD}$ input is left open or connected to V^+, the circuit will perform conversions at a rate determined by the clock frequency (8192 clock periods per cycle). Each measurement cycle is divided into three phases as shown in Figure 4. They are (1) Auto-Zero (AZ), (2) Signal Integrate (INT) and (3) Deintegrate (DE).

Auto-Zero Phase

During auto-zero three things happen. First, input high and low are disconnected from their pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the AZ accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

Note: All typical values have been guaranteed by characterization and are not tested.

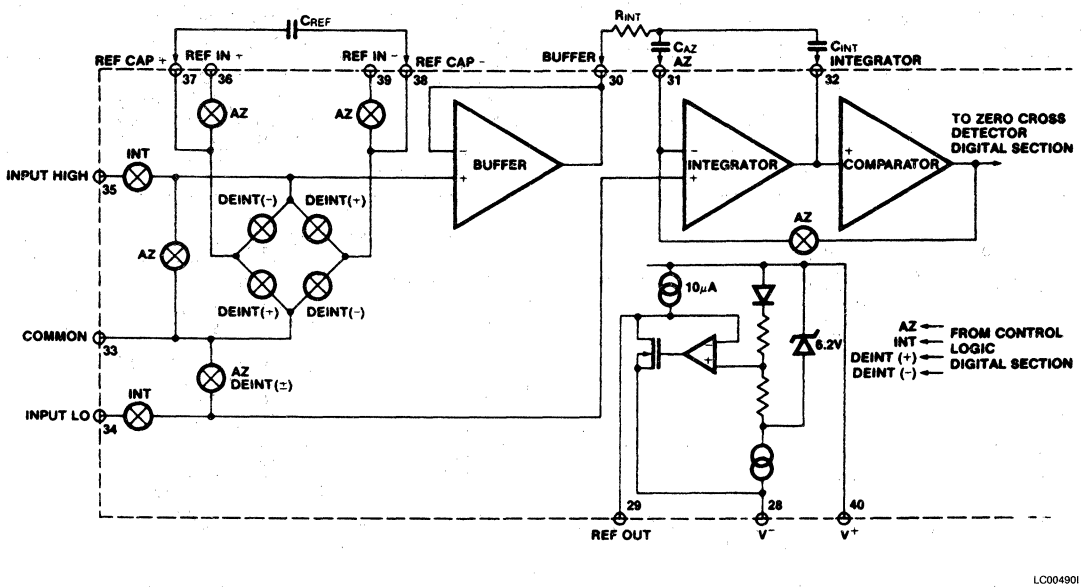


Figure 3: Analog Section

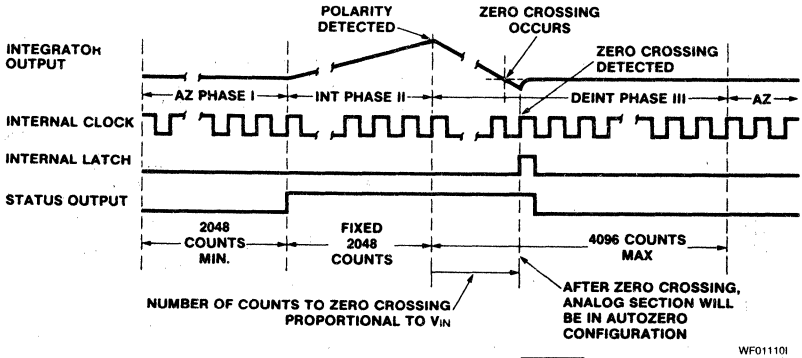


Figure 4: Conversion Timing (RUN/$\overline{\text{HOLD}}$ Pin High)

Signal Integrate Phase

During signal integrate the auto-zero loop is opened, the internal short is removed and the internal high and low inputs are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time of 2048 clock periods. Note that this differential voltage must be within the common mode range of the inputs. At the end of this phase, the polarity of the integrated signal is determined.

De-Integrate Phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged (during auto-zero) reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero crossing (established in Auto Zero) with a fixed slope. Thus the time for the output to return to zero (represented by the number of clock periods counted) is proportional to the input signal.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 1.0 volts below the positive supply to 1.5 volts above the negative supply. In this range the system has a CMRR of 86dB typical. However, since the integrator

Note: All typical values have been guaranteed by characterization and are not tested.

also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 4V full scale with some loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

The ICL7109 has, however, been optimized for operation with analog common near digital ground. With power supplies of +5V and −5V, this allows a 4V full scale integrator swing positive or negative thus maximizing the performance of the analog section.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to deintegrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition (see Component Values Selection below).

The roll-over error from these sources is minimized by having the reference common mode voltage near or at analog COMMON.

Component Value Selection

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

The most important consideration is that the integrator output swing (for full-scale input) be as large as possible. For example, with ±5V supplies and COMMON connected to GND, the nominal integrator output swing at full scale is ±4V. Since the integrator output can go to 0.3V from either supply without significantly affecting linearity, a 4V integrator output swing allows 0.7V for variations in output swing due to component value and oscillator tolerances. With ±5V supplies and a common mode range of ±1V required, the component values should be selected to provide ±3V integrator output swing. Noise and rollover errors will be slightly worse than in the ±4V case. For larger common mode voltage ranges, the integrator output swing must be reduced further. This will increase both noise and rollover errors. To improve the performance, supplies of ±6V may be used.

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They supply 20μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 4.096 volt full scale, 200kΩ is near optimum and similarly a 20kΩ for a 409.6mV scale. For other values of full scale voltage, R_{INT} should be chosen by the relation

$$R_{INT} = \frac{\text{full scale voltage}}{20\mu A}$$

Integrating Capacitor

The integrating capacitor C_{INT} should be selected to give the maximum integrator output voltage swing without saturating the integrator (approximately 0.3 volt from either supply). For the ICL7109 with ±5 volt supplies and analog common connected to GND, a ±3.5 to ±4 volt integrator output swing is nominal. For 7-1/2 conversions per second (61.72kHz clock frequency) as provided by the crystal oscillator, nominal values for C_{INT} and C_{AZ} are 0.15μF and 0.33μF, respectively. If different clock frequencies are used, these values should be changed to maintain the integrator output voltage swing. In general, the value of C_{INT} is given by

$$C_{INT} = \frac{(2048 \times \text{clock period})(20\mu A)}{\text{integrator output voltage swing}}$$

An additional requirement of the integrating capacitor is that it have low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost up to 85°C. For the military temperature range, Teflon® capacitors are recommended. While their dielectric absorption characteristics vary somewhat from unit to unit, selected devices should give less than 0.5 count of error due to dielectric absorption.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system: the smaller the capacitor the lower the overall system noise. However, C_{AZ} cannot be increased without limits since it, in parallel with the integrating capacitor forms an R-C time constant that determines the speed of recovery from overloads and more important the error that exists at the end of an auto-zero cycle. For 409.6mV full scale where noise is very important and the integrating resistor small, a value of C_{AZ} twice C_{INT} is optimum. Similarly for 4.096V full scale where recovery is more important than noise, a value of C_{AZ} equal to half of C_{INT} is recommended.

For optimal rejection of stray pickup, the outer foil of C_{AZ} should be connected to the R-C summing junction and the inner foil to pin 31. Similarly the outer foil of C_{INT} should be connected to pin 32 and the inner foil to the R-C summing junction. Teflon®, or equivalent, capacitors are recommended above 85°C for their low leakage characteristics.

Reference Capacitor

A 1μF capacitor gives good results in most applications. However, where a large reference common mode voltage exists (i.e. the reference low is not at analog common) and a 409.6mV scale is used, a larger value is required to prevent roll-over error. Generally 10μF will hold the roll-over error to 0.5 count in this instance. Again, Teflon®, or equivalent capacitors should be used for temperatures above 85°C for their low leakage characteristics.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7109

Reference Voltage

The analog input required to generate a full scale output of 4096 counts is $V_{IN} = 2V_{REF}$. Thus for a normalized scale, a reference of 2.048V should be used for a 4.096V full scale, and 204.8mV should be used for a 0.4096V full scale. However, in many applications where the A/D is sensing the output of a transducer, there will exist a scale factor other than unity between the absolute output voltage to be measured and a desired digital output. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 409.6mV, the input voltage should be measured directly and a reference voltage of 0.341V should be used. Suitable values for integrating resistor and capacitor are 34kΩ and 0.15μF. This avoids a divider on the input. Another advantage of this system occurs when a zero reading is desired for non-zero input. Temperature and weight measurements with an offset or tare are examples. The offset may be introduced by connecting the voltage output of the transducer between common and analog high, and the offset voltage between common and analog low, observing polarities carefully. However, in processor-based systems using the ICL7109, it may be more efficient to perform this type of scaling or tare subtraction digitally using software.

Reference Sources

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. The resolution of the ICL7109 at 12 bits is one part in 4096, or 244ppm. Thus if the reference has a temperature coefficient of 80ppm/°C (onboard reference) a temperature difference of 3°C will introduce a one-bit absolute error.

For this reason, it is recommended that an external high-quality reference be used where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made.

The ICL7109 provides a REFerence OUTput (pin 29) which may be used with a resistive divider to generate a suitable reference voltage. This output will sink up to about 20mA without significant variation in output voltage, and is provided with a pullup bias device which sources about 10μA. The output voltage is nominally 2.8V below V^+, and has a temperature coefficient of ±80ppm/°C typ. When using the onboard reference, REF OUT (Pin 29) should be connected to REF– (pin 39), and REF+ should be connected to the wiper of a precision potentiometer between REF OUT and V^+. The circuit for a 204.8mV reference is shown in the test circuit. For a 2.048mV reference, the fixed resistor should be removed, and a 25kΩ precision potentiometer between REF OUT and V^+ should be used.

Note that if pins 29 and 39 are tied together and pins 39 and 40 accidentally shorted (e.g., during testing), the reference supply will sink enough current to destroy the device. This can be avoided by placing a 1kΩ resistor in series with pin 39.

DETAILED DESCRIPTION

Digital Selection

The digital section includes the clock oscillator and scaling circuit, a 12-bit binary counter with output latches and TTL-compatible three-state output drivers, polarity, over-range and control logic, and UART handshake logic, as shown in Figure 5.

Throughout this description, logic levels will be referred to as "low" or "high". The actual logic levels are defined in the Electrical Characteristics Table. For minimum power consumption, all inputs should swing from GND (low) to V^+ (high). Inputs driven from TTL gates should have 3-5kΩ pullup resistors added for maximum noise immunity.

MODE Input

The MODE input is used to control the output mode of the converter. When the MODE pin is low or left open (this input is provided with a pulldown resistor to ensure a low level when the pin is left open), the converter is in its "Direct" output mode, where the output data is directly accessible under the control of the chip and byte enable inputs. When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in two bytes, then returns to "direct" mode. When the MODE input is left high, the converter will output data in the handshake mode at the end of every conversion cycle. (See section entitled "Handshake Mode" for further details).

STATUS Output

During a conversion cycle, the STATUS output goes high at the beginning of Signal Integrate (Phase II), and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Figure 4 for details of this timing. This signal may be used as a "data valid" flag (data never changes while STATUS is low) to drive interrupts, or for monitoring the status of the converter.

RUN/$\overline{\text{HOLD}}$ Input

When the RUN/$\overline{\text{HOLD}}$ input is high, or left open, the circuit will continuously perform conversion cycles, updating the output latches after zero crossing during the Deintegrate (Phase III) portion of the conversion cycle (See Figure 4). In this mode of operation, the conversion cycle will be performed in 8192 clock periods, regardless of the resulting value.

If RUN/$\overline{\text{HOLD}}$ goes low at any time during Deintegrate (Phase III) after the zero crossing has occurred, the circuit will immediately terminate Deintegrate and jump to Auto-Zero. This feature can be used to eliminate the time spent in Deintegrate after the zero-crossing. If RUN/$\overline{\text{HOLD}}$ stays or goes low, the converter will ensure minimum Auto-Zero time, and then wait in Auto-Zero until the RUN/$\overline{\text{HOLD}}$ input goes high. The converter will begin the Integrate (Phase II) portion of the next conversion (and the STATUS output will go high) seven clock periods after the high level is detected at RUN/$\overline{\text{HOLD}}$. See Figure 6 for details.

Note: All typical values have been guaranteed by characterization and are not tested.

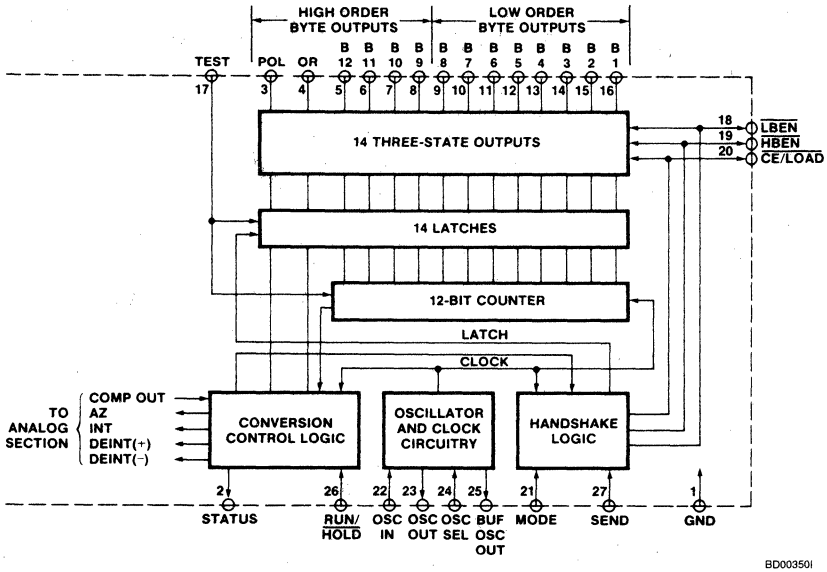


Figure 5: Digital Section

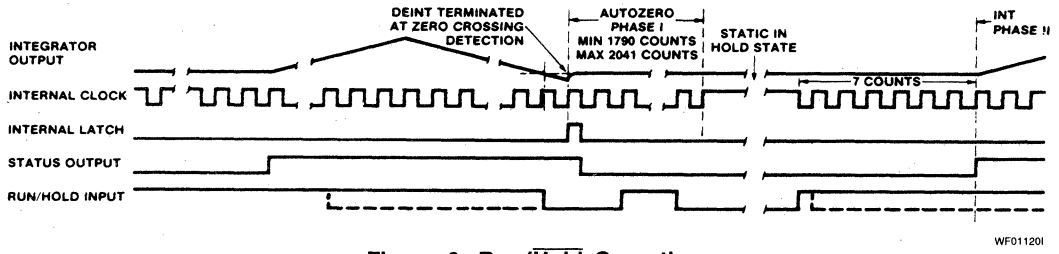


Figure 6: Run/Hold Operation

Using the RUN/HOLD input in this manner allows an easy "convert on demand" interface to be used. The converter may be held at idle in auto-zero with RUN/HOLD low. When RUN/HOLD goes high the conversion is started, and when the STATUS output goes low the new data is valid (or transferred to the UART — see Handshake Mode). RUN/HOLD may now be taken low which terminates deintegrate and ensures a minimum Auto-Zero time before the next conversion.

Alternately, RUN/HOLD can be used to minimize conversion time by ensuring that it goes low during Deintegrate, after zero crossing, and goes high after the hold point is reached. The required activity on the RUN/HOLD input can be provided by connecting it to the Buffered Oscillator Output. In this mode the conversion time is dependent on the input value measured. Also refer to Intersil Application Bulletin A032 for a discussion of the effects this will have on Auto-Zero performance.

If the RUN/HOLD input goes low and stays low during Auto-Zero (Phase I), the converter will simply stop at the end of Auto-Zero and wait for RUN/HOLD to go high. As above, Integrate (Phase II) begins seven clock periods after the high level is detected.

Direct Mode

When the MODE pin is left at a low level, the data outputs (bits 1 through 8 low order byte, bits 9 through 12, polarity and over-range high order byte) are accessible under control of the byte and chip enable terminals as inputs. These three inputs are all active low, and are provided with pullup resistors to ensure an inactive high level when left open. When the chip enable input is low, taking a byte enable input low will allow the outputs of that byte to become active (three-stated on). This allows a variety of parallel data accessing techniques to be used, as shown in the section entitled "Interfacing." The timing requirements for these outputs are shown in Figure 7 and Table 2.

Note: All typical values have been guaranteed by characterization and are not tested.

Table 2 — Direct Mode Timing Requirements

(See Note 4 of Electrical Characteristics)

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{BEA}	Byte Enable Width	350	220		ns
t_{DAB}	Data Access Time from Byte Enable		210	350	ns
t_{DHB}	Data Hold Time from Byte Enable		150	300	ns
t_{CEA}	Chip Enable Width	400	260		ns
t_{DAC}	Data Access Time from Chip Enable		260	400	ns
t_{DHC}	Data Hold Time from Chip Enable		240	400	ns

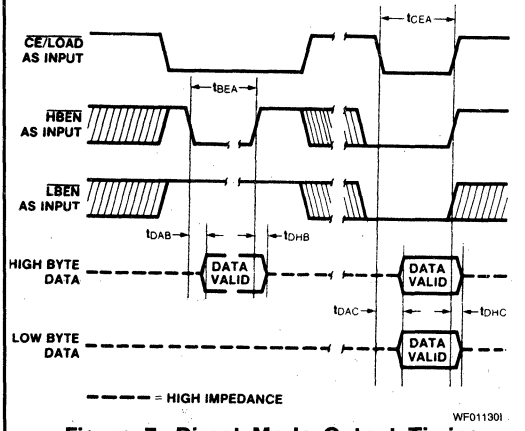


Figure 7: Direct Mode Output Timing

It should be noted that these control inputs are asynchronous with respect to the converter clock — the data may be accessed at any time. Thus it is possible to access the latches while they are being updated, which could lead to erroneous data. Synchronizing the access of the latches with the conversion cycle by monitoring the STATUS output will prevent this. Data is never updated while STATUS is low.

Handshake Mode

The handshake output mode is provided as an alternative means of interfacing the ICL7109 to digital systems, where the A/D converter becomes active in controlling the flow of data instead of passively responding to chip and byte enable inputs. This mode is specifically designed to allow a direct interface between the ICL7109 and industry-standard UARTs (such as the Intersil IM6402/3) with no external logic required. When triggered into the handshake mode, the ICL7109 provides all the control and flag signals necessary to sequentially transfer two bytes of data into the UART and initiate their transmission in serial form. This greatly eases the task and reduces the cost of designing remote data acquisition stations using serial data transmission.

Entry into the handshake mode is controlled by the MODE pin. When the MODE terminal is held high, the ICL7109 will enter the handshake mode after new data has been stored in the output latches at the end of a conversion (See Figures 8 and 9). The MODE terminal may also be used to trigger entry into the handshake mode on demand. At any time during the conversion cycle, the low to high transition of a short pulse at the MODE input will cause immediate entry into the handshake mode. If this pulse occurs while new data is being stored, the entry into handshake mode is delayed until the data is stable. While the converter is in the handshake mode, the MODE input is ignored, and although conversions will still be performed, data updating will be inhibited (See Figure 10) until the converter completes the output cycle and clears the handshake mode.

When the converter enters the handshake mode, or when the MODE input is high, the chip and byte enable terminals become TTL-compatible outputs which provide the control signals for the output cycle (See Figures 8, 9, and 10).

In handshake mode, the SEND input is used by the converter as an indication of the ability of the receiving device (such as a UART) to accept data.

Figure 8 shows the sequence of the output cycle with SEND held high. The handshake mode (Internal MODE high) is entered after the data latch pulse, and since MODE remains high the $\overline{CE/LOAD}$, $\overline{LBEN}$ and $\overline{HBEN}$ terminals are active as outputs. The high level at the SEND input is sensed on the same high to low internal clock edge that terminates the data latch pulse. On the next low to high internal clock edge the $\overline{CE/LOAD}$ and the $\overline{HBEN}$ outputs assume a low level, and the high-order byte (bits 9 through 12, POL, and OR) outputs are enabled. The $\overline{CE/LOAD}$ output remains low for one full internal clock period only, the data outputs remain active for 1-1/2 internal clock periods, and the high byte enable remains low for two clock periods. Thus the $\overline{CE/LOAD}$ output low level or low to high edge may be used as a synchronizing signal to ensure valid data, and the byte enable as an output may be used as a byte identification flag. With SEND remaining high the converter completes the output cycle using $\overline{CE/LOAD}$ and $\overline{LBEN}$ while the low order byte outputs (bits 1 through 8) are activated. The handshake mode is terminated when both bytes are sent.

Figure 9 shows an output sequence where the SEND input is used to delay portions of the sequence, or handshake to ensure correct data transfer. This timing diagram shows the relationships that occur using an industry-standard IM6402/3 CMOS UART to interface to serial data channels. In this interface, the SEND input to the ICL7109 is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the $\overline{CE/LOAD}$ terminal of the ICL7109 drives the TBRL (Transmitter Buffer Register Load) input to the UART. The data outputs are paralleled into the eight Transmitter Buffer Register inputs.

Note: All typical values have been guaranteed by characterization and are not tested.

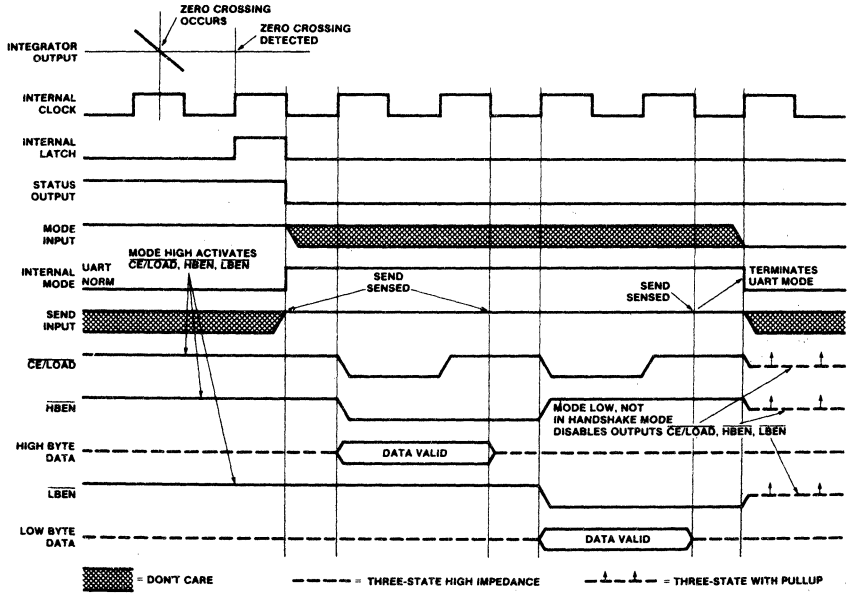


Figure 8: Handshake With Send Held Positive

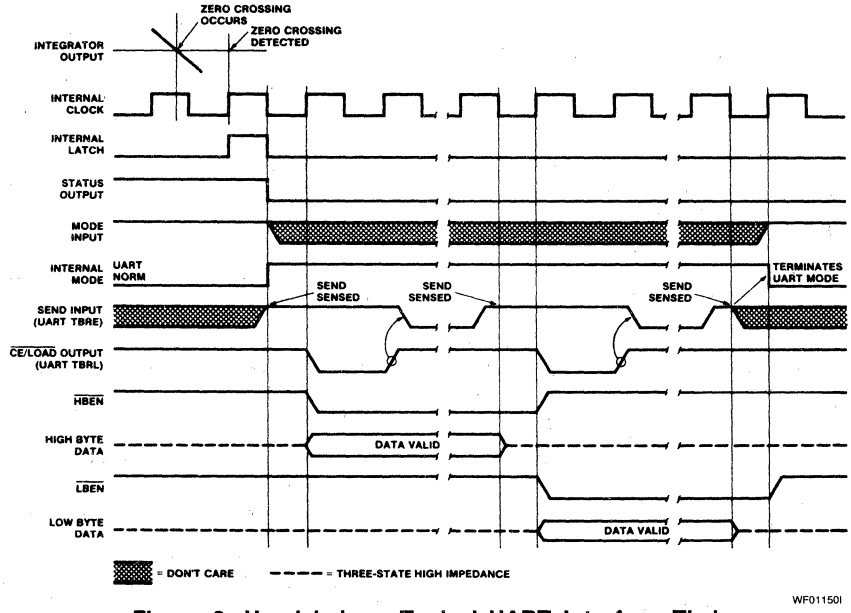


Figure 9: Handshake — Typical UART Interface Timing

Note: All typical values have been guaranteed by characterization and are not tested.

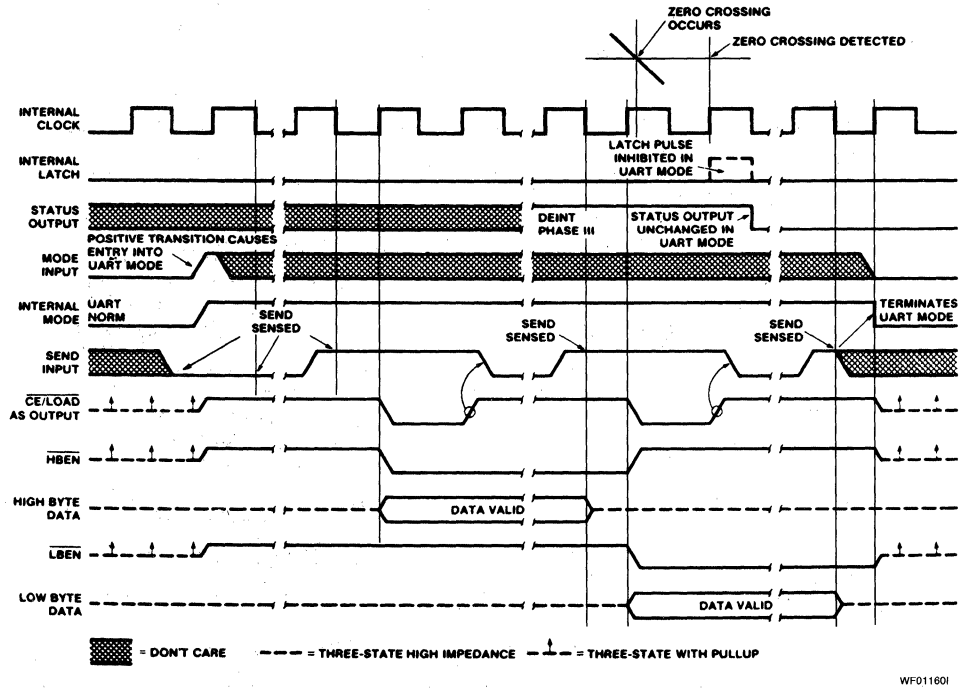


Figure 10: Handshake Triggered By Mode

Assuming the UART Transmitter Buffer Register is empty, the SEND input will be high when the handshake mode is entered after new data is stored. The $\overline{CE/LOAD}$ and $\overline{HBEN}$ terminals will go low after SEND is sensed, and the high order byte outputs become active. When $\overline{CE/LOAD}$ goes high at the end of one clock period, the high order byte data is clocked into the UART Transmitter Buffer Register. The UART TBRE output will now go low, which halts the output cycle with the $\overline{HBEN}$ output low, and the high order byte outputs active. When the UART has transferred the data to the Transmitter Register and cleared the Transmitter Buffer Register, the TBRE returns high. On the next ICL7109 internal clock high to low edge, the high order byte outputs are disabled, and one-half internal clock later, the $\overline{HBEN}$ output returns high. At the same time, the $\overline{CE/LOAD}$ and $\overline{LBEN}$ outputs go low, and the low order byte outputs become active. Similarly, when the $\overline{CE/LOAD}$ returns high at the end of one clock period, the low order data is clocked into the UART Transmitter Buffer Register, and TBRE again goes low. When TBRE returns to a high it will be sensed on the next ICL7109 internal clock high to low edge, disabling the data outputs. One-half internal clock later, the handshake mode will be cleared, and the $\overline{CE/LOAD}$, $\overline{HBEN}$, and $\overline{LBEN}$ terminals return high and stay active (as long as MODE stays high).

With the MODE input remaining high as in these examples, the converter will output the results of every conversion except those completed during a handshake operation. By triggering the converter into handshake mode with a low to high edge on the MODE input, handshake output sequences may be performed on demand. Figure 9 shows a handshake output sequence triggered by such an edge. In addition, the SEND input is shown as being low when the converter enters handshake mode. In this case, the whole output sequence is controlled by the SEND input, and the sequence for the first (high order) byte is similar to the sequence for the second byte. This diagram also shows the output sequence taking longer than a conversion cycle. Note that the converter still makes conversions, with the STATUS output and RUN/$\overline{HOLD}$ input functioning normally. The only difference is that new data will not be latched when in handshake mode, and is therefore lost.

Oscillator

The ICL7109 is provided with a versatile three terminal oscillator to generate the internal clock. The oscillator may be overdriven, or may be operated with an RC network or crystal. The OSCILLATOR SELECT input changes the internal configuration of the oscillator to optimize it for RC or crystal operation.

When the OSCILLATOR SELECT input is high or left open (the input is provided with a pullup resistor), the oscillator is configured for RC operation, and the internal clock will be of the same frequency and phase as the signal at the BUFFERED OSCILLATOR OUTPUT. The resistor and capacitor should be connected as in Figure 11. The circuit will oscillate at a frequency given by $f = 0.45/RC$. A 100kΩ resistor is recommended for useful ranges of

Note: All typical values have been guaranteed by characterization and are not tested.

frequency. For optimum 60Hz line rejection, the capacitor value should be chosen such that 2048 clock periods is close to an integral multiple of the 60Hz period (but should not be less than 50pF).

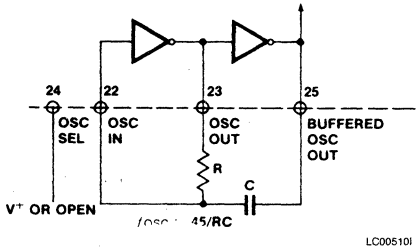


Figure 11: RC Oscillator

When the OSCILLATOR SELECT input is low a feedback device and output and input capacitors are added to the oscillator. In this configuration, as shown in Figure 11, the oscillator will operate with most crystals in the 1 to 5MHz range with no external components. Taking the OSCILLATOR SELECT input low also inserts a fixed ÷58 divider circuit between the BUFFERED OSCILLATOR OUTPUT and the internal clock. Using an inexpensive 3.58MHz TV crystal, this division ratio provides an integration time given by:

$$T = (2048 \text{ clock periods}) \times \left[\frac{58}{3.58\text{MHz}}\right] = 33.18\text{ms}$$

This time is very close to two 60Hz periods or 33.33ms. The error is less than one percent, which will give better than 40dB 60Hz rejection. The converter will operate reliably at conversion rates of up to 30 per second, which corresponds to a clock frequency of 245.8kHz.

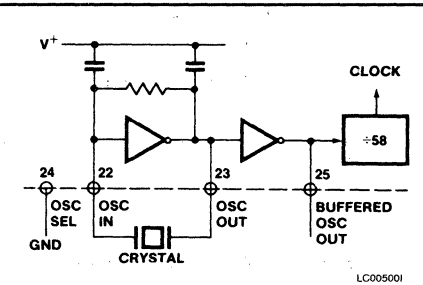


Figure 12: Crystal Oscillator

If at any time the oscillator is to be overdriven, the overdriving signal should be applied at the OSCILLATOR INPUT, and the OSCILLATOR OUTPUT should be left open. The internal clock will be of the same frequency, duty cycle, and phase as the input signal when OSCILLATOR SELECT is left open. When OSCILLATOR SELECT is at GND, the clock will be a factor of 58 below the input frequency.

When using the ICL7109 with the IM6403 UART, it is possible to use one 3.58MHz crystal for both devices. The BUFFERED OSCILLATOR OUTPUT of the ICL7109 may be used to drive the OSCILLATOR INPUT of the UART, saving the need for a second crystal. However, the BUFFERED OSCILLATOR OUTPUT does not have a great deal of drive capability, and when driving more than one slave device, external buffering should be used.

Test Input

When the TEST input is taken to a level halfway between V^+ and GND, the counter output latches are enabled, allowing the counter contents to be examined anytime.

When the TEST input is connected to GND, the counter outputs are all forced into the high state, and the internal clock is disabled. When the input returns to the 1/2 (V^+ −GND) voltage (or to V^+) and one clock is applied, all the counter outputs will be clocked to the low state. This allows easy testing of the counter and its outputs.

INTERFACING

Direct Mode

Figure 13 shows some of the combinations of chip enable and byte enable control signals which may be used when interfacing the ICL7109 to parallel data lines. The $\overline{CE/LOAD}$ input may be tied low, allowing either byte to be controlled by its own enable as in Figure 13A. Figure 13B shows a configuration where the two byte enables are connected together. In this configuration, the $\overline{CE/LOAD}$ serves as a chip enable, and the $\overline{HBEN}$ and $\overline{LBEN}$ may be connected to GND or serve as a second chip enable. The 14 data outputs will all be enabled simultaneously. Figure 13C shows the $\overline{HBEN}$ and $\overline{LBEN}$ as flag inputs, and $\overline{CE/LOAD}$ as a master enable, which could be the READ strobe available from most microprocessors.

6

Note: All typical values have been guaranteed by characterization and are not tested.

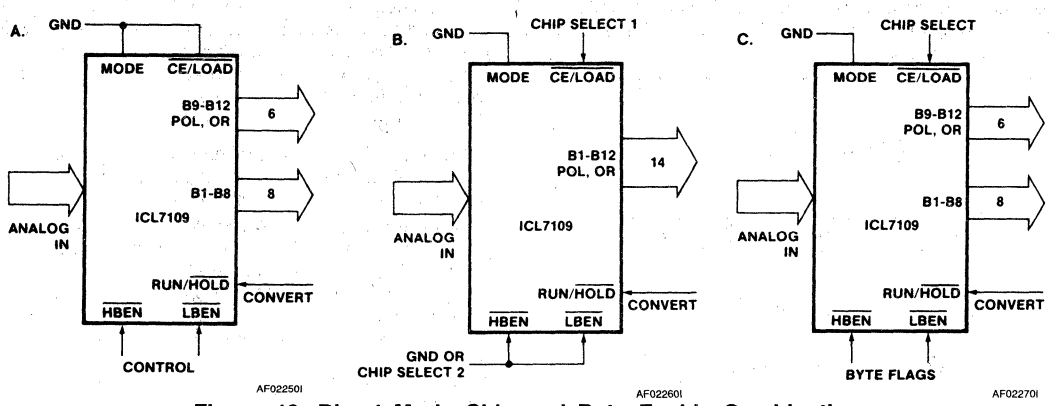


Figure 13: Direct Mode Chip and Byte Enable Combinations

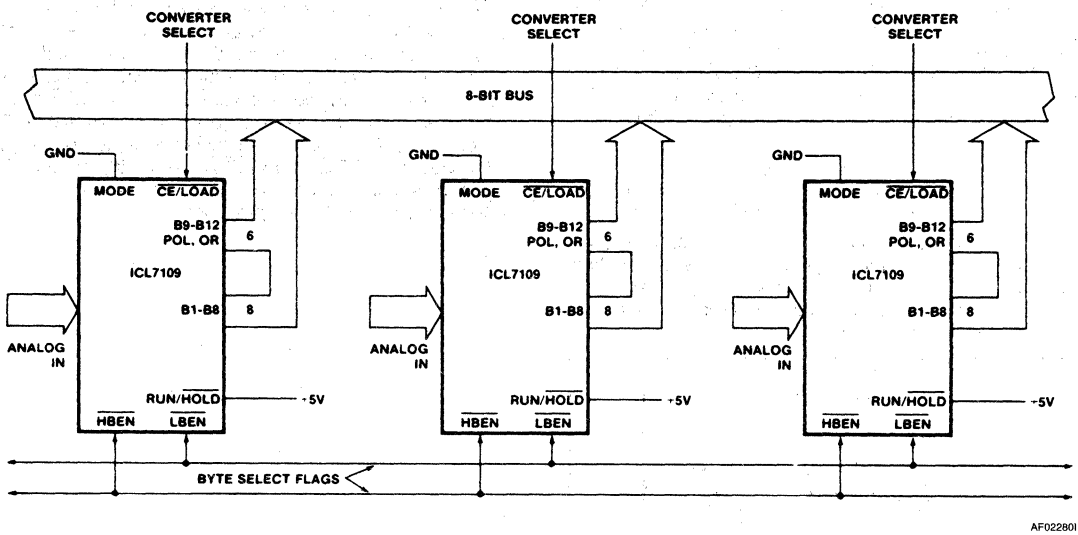


Figure 14: Tri-stating Several 7109's to a Small Bus

Figure 14 shows an approach to interfacing several ICL7109s to a bus, ganging the $\overline{\text{HBEN}}$ and $\overline{\text{LBEN}}$ signals to several converters together, and using the $\overline{\text{CE/LOAD}}$ inputs (perhaps decoded from an address) to select the desired converter.

Some practical circuits utilizing the parallel three-state output capabilities of the ICL7109 are shown in Figures 15 through 20. Figure 15 shows a straightforward application to the Intel 8048/80/85 microprocessors via an 8255PPI, where the ICL7109 data outputs are active at all times. The I/O ports of an 8155 may be used in the same way. This interface can be used in a read-anytime mode, although a read performed while the data latches are being updated will lead to scrambled data. This will occur very rarely, in the proportion of setup-skew times to conversion time. One way to overcome this is to read the STATUS output as well, and if it is high, read the data again after a delay of more than 1/2 converter clock period. If STATUS is now low, the second reading is correct, and if it is still high, the first reading is correct. Alternatively, this timing problem is completely avoided by using a read-after-update sequence, as shown in Figure 16. Here the high to low transition of the STATUS output drives an interrupt to the microprocessor causing it to access the data latches. This application also shows the RUN/$\overline{\text{HOLD}}$ input being used to initiate conversions under software control.

Note: All typical values have been guaranteed by characterization and are not tested.

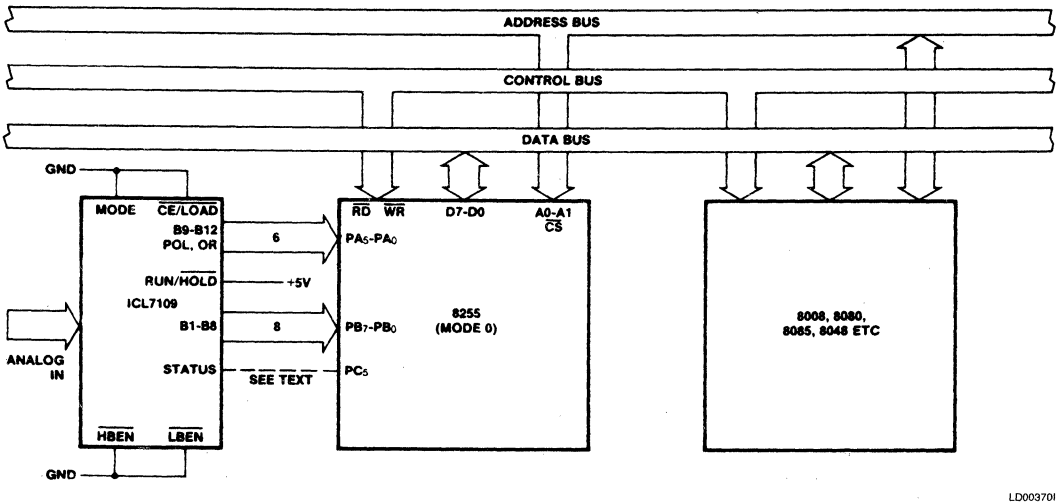


Figure 15: Full-time Parallel Interface to 8048/80/85 Microprocessors

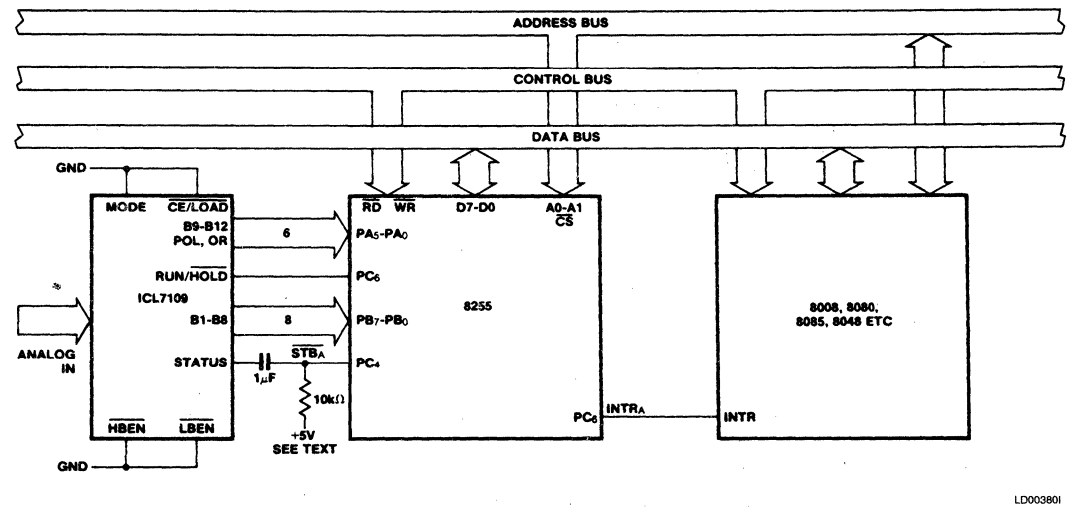


Figure 16: Full-time Parallel Interface to 8048/80/85 Microprocessors With Interrupt

A similar interface to Motorola MC6800 or MOS Technology MCS650X systems is shown in Figure 17. The high to low transition of the STATUS output generates an interrupt via the Control Register B CB1 line. Note that CB2 controls the RUN/$\overline{\text{HOLD}}$ pin through Control Register B, allowing software-controlled initiation of conversions in this system as well.

The three-state output capability of the ICL7109 allows direct interfacing to most microprocessor busses. Examples of this are shown in Figures 18 and 19. It is necessary to carefully consider the system timing in this type of interface, to be sure that requirements for setup and hold times, and minimum pulse widths are met. Note also the drive limitations on long buses. Generally this type of interface is only favored if the memory peripheral address density is low so that simple address decoding can be used. Interrupt handling can also require many additional components, and using an interface device will usually simplify the system in this case.

Note: All typical values have been guaranteed by characterization and are not tested.

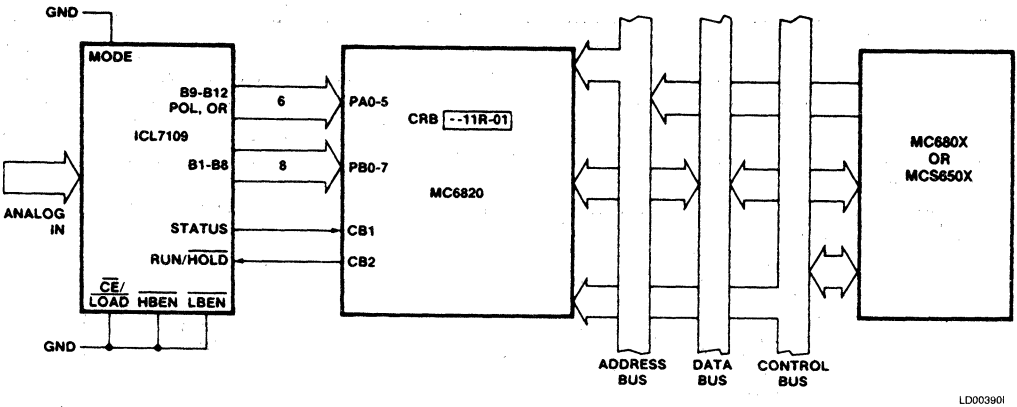


Figure 17: Full-time Parallel Interface to MC680X or MCS650X Microprocessors

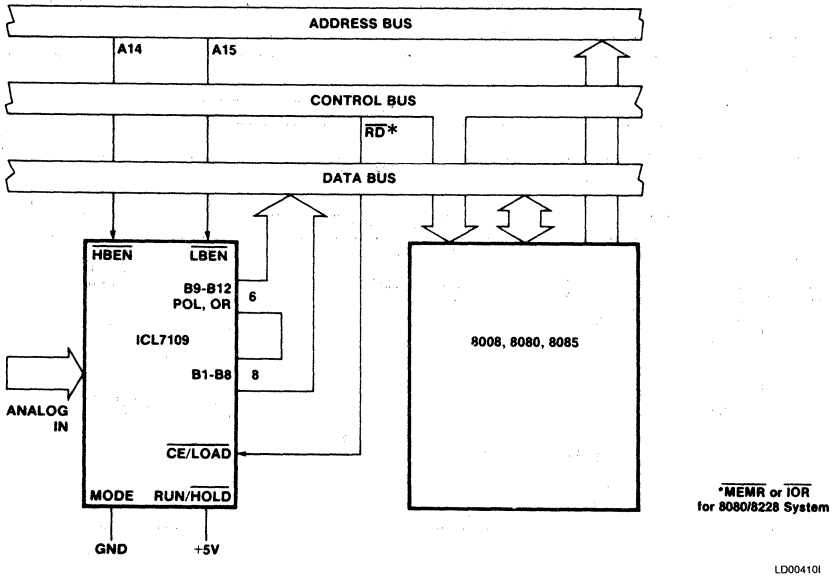


Figure 18: Direct Interface — ICL7109 to 8080/8085

Note: All typical values have been guaranteed by characterization and are not tested.

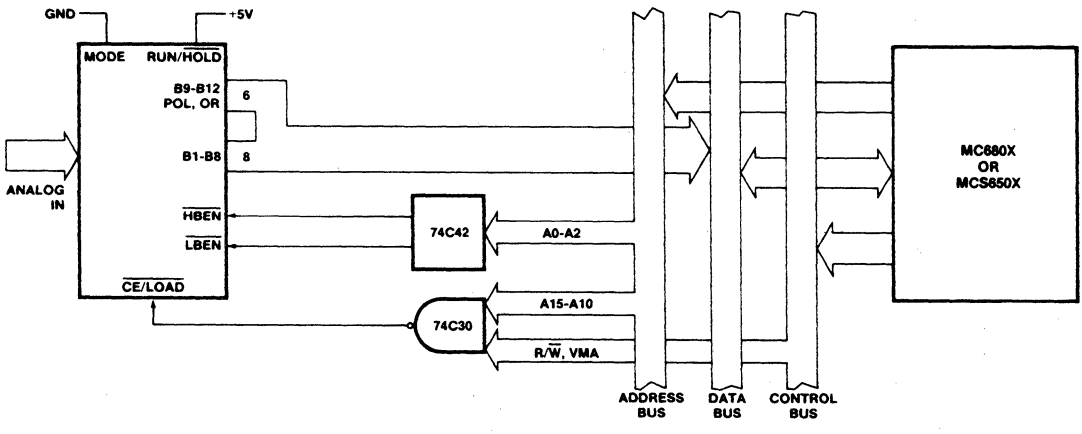


Figure 19: Direct ICL7109 — MC680X Bus Interface

Handshake Mode

The handshake mode allows ready interface with a wide variety of external devices. For instance, external latches may be clocked by the rising edge of $\overline{CE/LOAD}$, and the byte enables may be used as byte identification flags or as load enables.

Figure 20 shows a handshake interface to Intel microprocessors again using an 8255PPI. The handshake operation with the 8255 is controlled by inverting its Input Buffer Full (IBF) flag to drive the SEND input to the ICL7109, and using the $\overline{CE/LOAD}$ to drive the 8255 strobe. The internal control register of the PPI should be set in MODE 1 for the port used. If the 7109 is in handshake mode and the 8255 IBF flag is low, the next word will be strobed into the port. The strobe will cause IBF to go high (SEND goes low), which will keep the enabled byte outputs active. The PPI will generate an interrupt which when executed will result in the data being read. When the byte is read, the IBF will be reset low, which causes the ICL7109 to sequence into the next byte. This figure shows the MODE input to the ICL7109 connected to a control line on the PPI. If this output is left high, or tied high separately, the data from every conversion (provided the data access takes less time than a conversion) will be sequenced in two bytes into the system.

If this output is made to go from low to high, the output sequence can be obtained on demand, and the interrupt may be used to reset the MODE bit. Note that the RUN/$\overline{HOLD}$ input to the ICL7109 may also be driven by a bit of the 8255 so that conversions may be obtained on command under software control. Note that one port of the 8255 is not used, and can service another peripheral device. The same arrangement can also be used with the 8155.

Figure 21 shows a similar arrangement with the MC6800 or MCS650X microprocessors, except that both MODE and RUN/$\overline{HOLD}$ are tied high to save port outputs.

The handshake mode is particularly convenient for directly interfacing to industry standard UARTs (such as the Intersil IM6402/6403 or Western Digital TR1602) providing a minimum component count means of serially transmitting converted data. A typical UART connection is shown in Figure 2A. In this circuit, any word received by the UART causes the UART DR (Data Ready) output to go high. This drives the MODE input to the ICL7109 high, triggering the ICL7109 into handshake mode. The high order byte is output to the UART first, and when the UART has transferred the data to the Transmitter Register, TBRE (SEND) goes high and the second byte is output. When TBRE (SEND) goes high again, $\overline{LBEN}$ will go high, driving the UART DRR (Data Ready Reset) which will signal the end of the transfer of data from the ICL7109 to the UART.

Figure 22 shows an extension of the one converter — one UART scheme to several ICL7109s with one UART. In this circuit, the word received by the UART (available at the RBR outputs when DR is high) is used to select which converter will handshake with the UART. With no external components, this scheme will allow up to eight ICL7109s to interface with one UART. Using a few more components to decode the received word will allow up to 256 converters to be accessed on one serial line.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7109

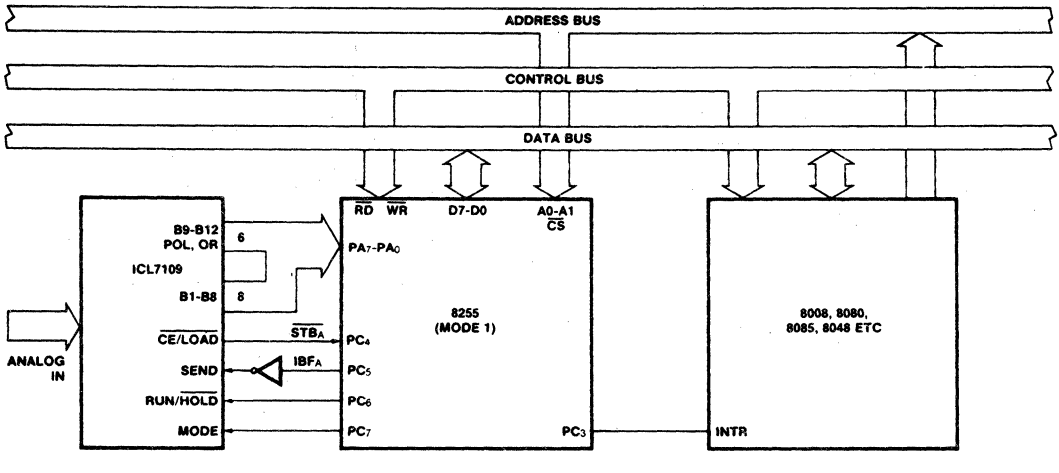


Figure 20: Handshake Interface — ICL7109 to 8048, 80/85

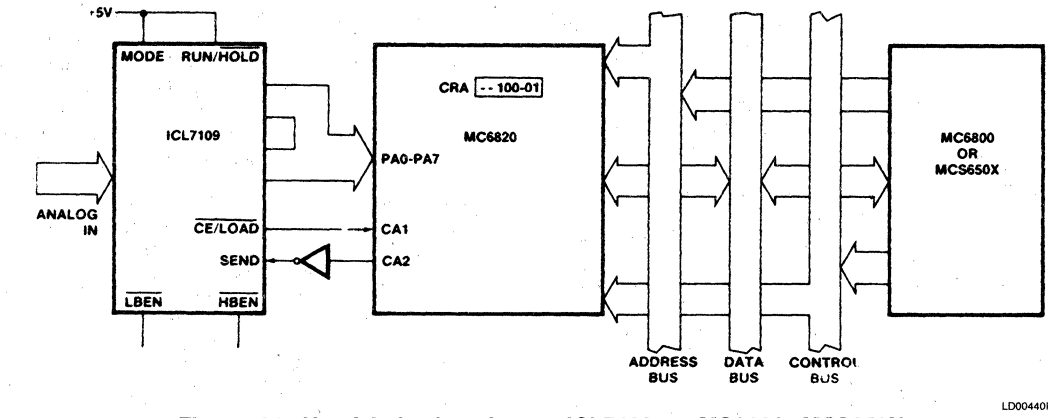


Figure 21: Handshake Interface — ICL7109 to MC6800, MCS650X

Note: All typical values have been guaranteed by characterization and are not tested.

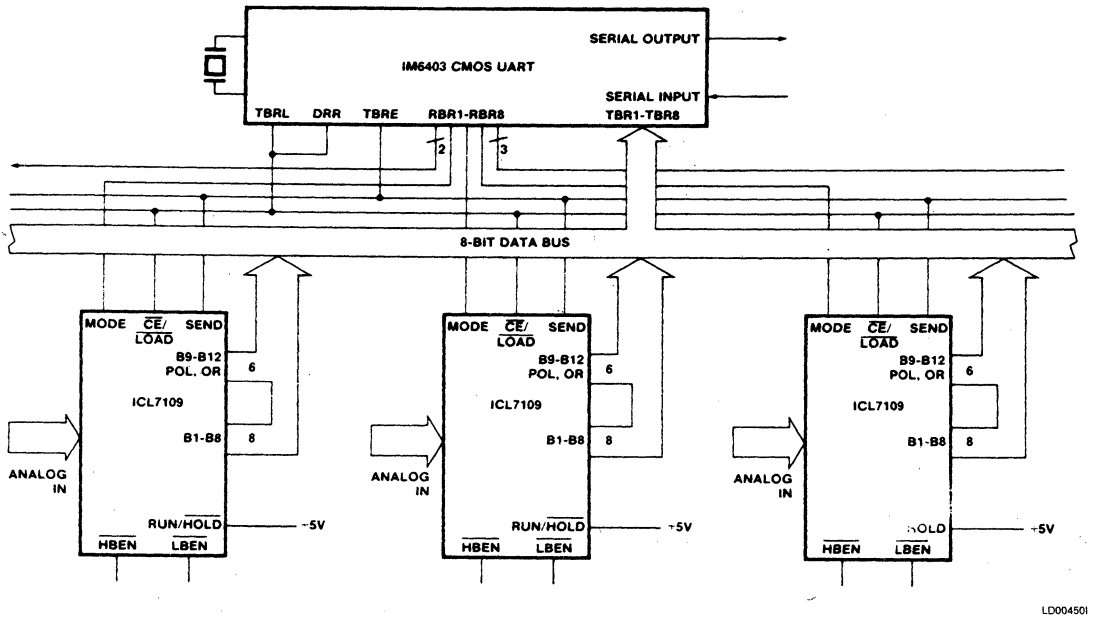


Figure 22: Multiplexing Converters with Mode Input

The applications of the ICL7109 are not limited to those shown here. The purpose of these examples is to provide a starting point for users to develop useful systems, and to show some of the variety of interfaces and uses of the ICL7109. Many of the ideas suggested here may be used in combination; in particular the uses of the STATUS, RUN/$\overline{\text{HOLD}}$, and MODE signals may be mixed.

APPLICATION NOTES

A016 "Selecting A/D Converters," by David Fullagar
A017 "The Integrating A/D Converters," by Lee Evans
A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood
A030 "The ICL7104 — A Binary Output A/D Converter for Microprocessors," by Peter Bradshaw
A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106 Family," by Peter Bradshaw
R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7115
14-Bit High-Speed CMOS μP-Compatible A/D Converter

GENERAL DESCRIPTION

The ICL7115 is the first monolithic 14-bit resolution, fast successive approximation A/D converter. It uses thin film resistors and CMOS circuitry combined with an on-chip PROM calibration table to achieve 13-bit linearity without laser trimming. Special design techniques used in the DAC and comparator result in high speed operation, while the fully static silicon-gate CMOS circuitry keeps the power dissipation very low.

Microprocessor bus interfacing is made easy by the use of standard WRite and ReaD cycle timing and control signals, combined with Chip Select and Address pins. The digital output pins are byte-organized and three-state gated for bus interface to 8 and 16-bit systems.

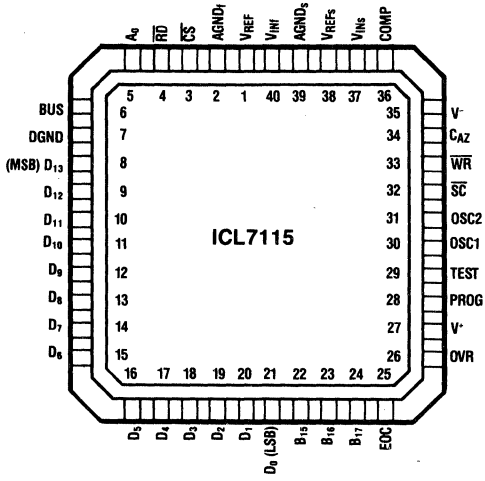
The ICL7115 provides separate Analog and Digital grounds. Analog ground, voltage reference and input voltage pins are separated into force and sense lines for increased system accuracy. Operating with ±5V supplies, the ICL7115 accepts 0V to +5V input with a −5V reference or 0V to −5V input with a +5V reference.

FEATURES

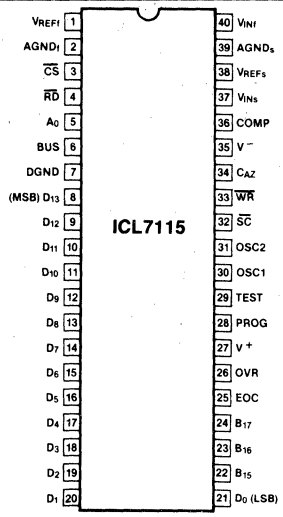
- **14-Bit Resolution (LSB = 305μV)**
- **No Missing Codes**
- **Microprocessor Compatible Byte-Organized Buffered Outputs**
- **Fast Conversion (40μs)**
- **Auto-Zeroed Comparator for Low Offset Voltage**
- **Low Linearity and Gain Tempco (1.5ppm/°C, 5ppm/°C)**
- **Low Power Consumption (60mW)**
- **No Gain or Offset Adjustment Necessary**
- **Provides 3% Useable Overrange**
- **FORCE/SENSE and Separate Digital and Analog Ground Pins for Increased System Accuracy**

ORDERING INFORMATION

PART NUMBER	RESOLUTION WITH NO MISSING CODES	TEMP. RANGE	PACKAGE
ICL7115JCDL	12 Bits	0°C to +70°C	40 Pin Ceramic
ICL7115KCDL	13 Bits	0°C to +70°C	40 Pin Ceramic
ICL7115JIDL	12 Bits	−25°C to 85°C	40 Pin Ceramic
ICL7115KIDL	13 Bits	−25°C to +85°C	40 Pin Ceramic
ICL7115JMDL	12 Bits	−55°C to +125°C	40 Pin Ceramic
ICL7115KMDL	13 Bits	−55°C to +125°C	40 Pin Ceramic
ICL7115JMLL	12 Bits	−55°C to +125°C	40 Pin LCC
ICL7115KMLL	13 Bits	−55°C to +125°C	40 Pin LCC



(Outline DWG LL)



(Outline DWG DL)

Figure 1: Pin Configuration

Note: All typical values have been guaranteed by characterization and are not tested.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage V^+ to DGND ..... −0.3V to +6.5V
Supply Voltage V^- to DGND ..... +0.3V to −6.5V
V_{REFs}, V_{REFf}, V_{INs}, V_{INf} to DGND ..... +25V to −25V
$AGND_s$, $AGND_f$ to DGND ..... +1V to −1V
Current in FORCE and SENSE Lines 25mA
Digital I/O Pin Voltages ..... −0.3V to V^+ +0.3V
PROG to DGND Voltage ..... V^- to V^+ +0.3V

Operating Temperature Range
ICL7115XCXX ..... 0°C to +70°C
ICL7115XIXX ..... −25°C to +85°C
ICL7115XMXX ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Power Dissipation 500mW
derate above 70°C @ 100mW/°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE 1: All voltages with respect to DGND, unless otherwise noted.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

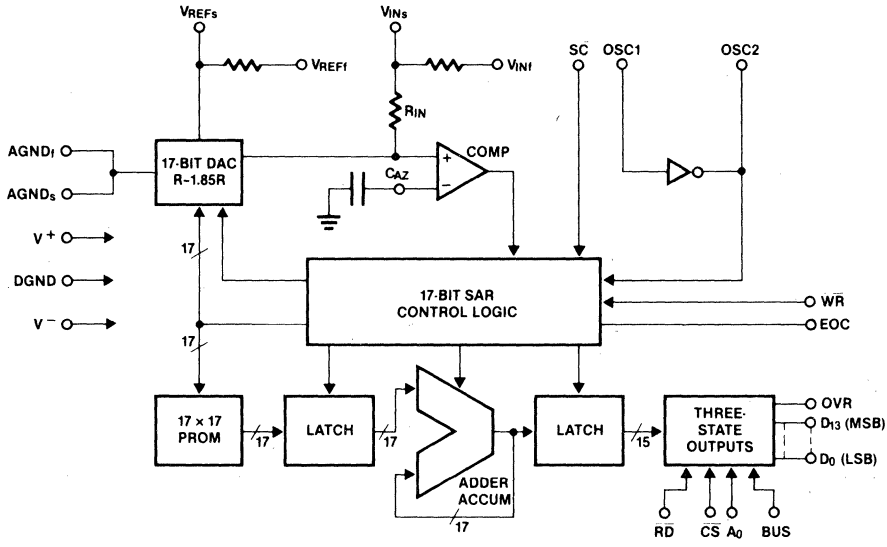


Figure 2: ICL7115 Functional Block Diagram

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7115

ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS $V^+ = +5.0V$, $V^- = -5.0V$, $V_{REFs} = -5.0V$, $T_A = +25°C$, $f_{CLK} = 500kHz$ unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Resolution	$\overline{SC} = V_{IH}$		14			Bits
		$\overline{SC} = V_{IL}$		12			
I_{LE}	Integral Linearity Error	Note 1	J			±0.018	%FSR
			K			±0.012	
$T_{C(ILE)}$	Temperature Coefficient of I_{LE}	TA = Operating Range			1	1.5	ppm/°C
$RES_{(NMC)}$	Min Resolution with No Missing Codes	$T_A = 25°C$	J	12			Bits
			K	13			
		T_A = Operating Range (Note 2)	J	11			
			K	12			
FSE	Full Scale Calibration Error (Adjustable to Zero)		J			±0.1	%FSR
			K			±0.08	
$T_{C(FSE)}$	Temperature Coefficient of FSE	T_A = Operating Range			2	5	ppm/°C
ZE	Zero Error	Notes 1,2				±1	LSB
$T_{C(ZE)}$	Temperature Coefficient of ZE	T_A = Operating Range				1	ppm/°C
PSRR	Power Supply Rejection Ratio	$T_A = 25°C$			±½	±1	LSB
		T_A = Operating Range				±2	
V_{IN}	Analog Input Range (V_{INs}, V_{REFs})			0 to +5			V
R_{IN}	Input Resistance (V_{INs}, V_{REFs})	Note 3		4		9	kΩ
$T_{C(R_{IN})}$		T_A = Operating Range			−300		ppm/°C
I_{SUPPLY}	Supply Current, I+, I−	$T_A = 25°C$			2	4	mA
		T_A=Operating Range				6	
V_{SUPPLY}	Supply Voltage Range	Functional Operation Only		±4.5		±6.0	V
V_{IL}	Low State Input Voltage	Operating Temperature Range				0.8	V
V_{IH}	High State Input Voltage	Operating Temperature Range		2.4			V
I_{LIH}	Logic Input Current	$0 < V_{IN} > V^+$			1	10	µA
V_{OL}	Low State Output Voltage	I_{OUT} = 1.6mA Operating Temperature Range				0.4	V
V_{OH}	High State Output Voltage	I_{OUT} = −200µA Operating Temperature Range		2.8			V
I_{OX}	Three-State Output Current	$0 < V_{OUT} > V_+$			1		µA
C_{IN}	Logic Input Capacitance	(Note 4)			15		pF
C_{OUT}	Logic Output Capacitance	Three-State (Note 4)			15		

NOTES: 1. Full-scale range (FSR) is 5V (reference adjusted).
2. Assume all leads soldered or welded to printed circuit board.
3. Assume all leads soldered or welded to printed circuit board.

Note: All typical values have been guaranteed by characterization and are not tested.

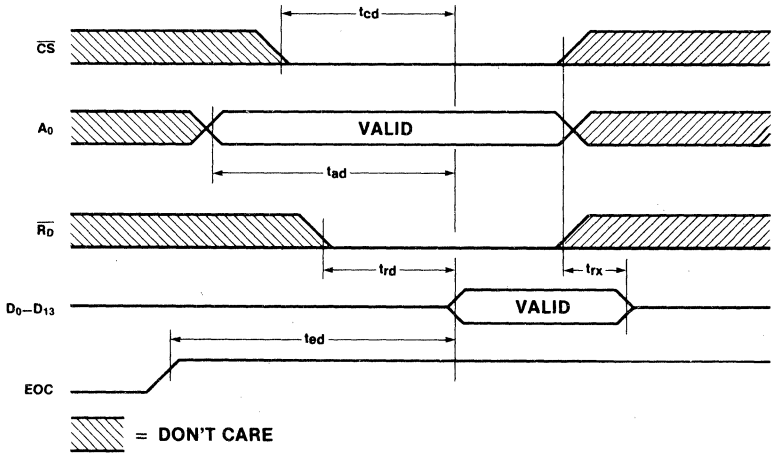


Figure 3: Read Cycle Timing with BUS = V_{IL}

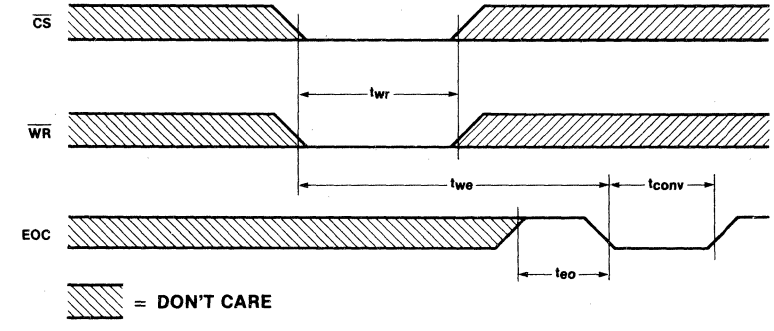


Figure 4: Write Cycle Timing

AC ELECTRICAL CHARACTERISTICS

$V^+ = +5.0V$, $V^- = -5.0V$, $T_A = +25°C$, $f_{clk} = 500kHz$ unles otherwise noted. Data derived from extensive characterization testing. Parameters are not 100% production tested.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
READ CYCLE TIMING						
t_{cd}	Prop. Delay $\overline{CS}$ to Data	$\overline{RD}$ Low, A_0 Valid			200	ns
t_{ad}	Prop. Delay A_0 to Data	$\overline{CS}$ Low, $\overline{RD}$ Low			200	
t_{rd}	Prop. Delay $\overline{RD}$ to Data	$\overline{CS}$ Low, A_0 Valid			200	
t_{rx}	Prop. Delay Data to Three State				100	
t_{ed}	Prop. Delay EDC High to Data				200	
WRITE CYCLE TIMING						
t_{wr}	$\overline{WR}$ Low Time		100			ns
t_{we}	Prop. Delay $\overline{WR}$ Low to EDC Low	Wait Mode	1		2	1/fclk
t_{eo}	EOC High Time	Free-Run Mode	0.5		1.5	
t_{conv}	Conversion Time	$\overline{SC} = V_{IH}$			20	
		$\overline{SC} = V_{IL}$			18	

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7115

TABLE 1: PIN DESCRIPTIONS

PIN	NAME	FUNCTION	
1	V_{REFf}	FORCE line for reference input.	
2	$AGND_f$	FORCE input for analog ground	
3	$\overline{CS}$	Chip Select enables reading and writing (active low)	
4	$\overline{RD}$	$\overline{ReaD}$ (active low)	
5	A_0	Byte select (low = D_0-D_7, high = D_8-D_{13}, OVR)	
6	BUS	Bus select (low = outputs enabled by A_0, high = all outputs enabled together)	
7	DGND	Digital GrouND return	
8	D_{13}	Bit 13 (most significant)	High Byte
9	D_{12}	Bit 12	
10	D_{11}	Bit 11	
11	D_{10}	Bit 10	
12	D_9	Bit 9 Output	
13	D_8	Bit 8 Data	
14	D_7	Bit 7 Bits	Low Byte
15	D_6	Bit 6 (High = True)	
16	D_5	Bit 5	
17	D_4	Bit 4	
18	D_3	Bit 3	
19	D_2	Bit 2	
20	D_1	Bit 1	
21	D_0	Bit 0 (least significant)	
22	B_{15}	Used for programming only (leave open)	
23	B_{16}		
24	B_{17}		
25	EOC	End Of Conversion flag (low = busy, high = conversion complete)	
26	OVR	OVerRange flag (valid at end of conversion when output code exceeds full-scale, three-state output enabled with high byte)	
27	V^+	Positive power supply input	
28	PROG	Used for programming only. Tie to V^+ for normal operation	
29	TEST	Used for programming only. Tie to V^+ for normal operation	
30	OSC1	Oscillator inverter input	
31	OSC2	Oscillator inverter output	
32	$\overline{SC}$	Short cycle input (high = 14-bit, low = 12-bit operation)	
33	$\overline{WR}$	$\overline{WR}$ite pulse input (low starts new conversion)	
34	C_{AZ}	Auto-zero capacitor connection	
35	V^-	Negative power supply input	
36	COMP	Used in test, tie to V^-	
37	V_{INs}	SENSE line for input voltage	
38	V_{REFs}	SENSE line for reference input	
39	$AGND_s$	SENSE line for analog ground	
40	V_{INf}	FORCE line for input voltage	

TABLE 2: I/O CONTROL

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	A_0	BUS	FUNCTION
0	0	x	x	x	Initiates a Conversion
1	x	x	x	x	Disables all Chip Commands
0	x	0	0	0	Low Byte is Enabled
0	x	0	1	0	High Byte is Enabled
0	x	0	x	1	Low and High Bytes Enabled Together
x	x	1	x	x	Disables Outputs (High-Impedance)

TABLE 3: TRANSFER FUNCTION

INPUT VOLTAGE	EXPECTED OUTPUT CODE			
$V_{REF} = -5.0V$	OVR	MSB		LSB
0	0	0	0 0 0 0 0 0 0 0 0 0 0 0 0	0
+0.0003	0	0	0 0 0 0 0 0 0 0 0 0 0 0 0	1
+0.150	0	0	0 0 0 0 1 1 1 1 0 1 0 1	1
+2.4997	0	0	1 1 1 1 1 1 1 1 1 1 1 1 1	1
+2.500	0	1	0 0 0 0 0 0 0 0 0 0 0 0 0	0
+4.9994	0	1	1 1 1 1 1 1 1 1 1 1 1 1 1	0
+4.9997	0	1	1 1 1 1 1 1 1 1 1 1 1 1 1	1
+5.000	1	0	0 0 0 0 0 0 0 0 0 0 0 0 0	0
+5.0003	1	0	0 0 0 0 0 0 0 0 0 0 0 0 0	1
+5.150	1	0	0 0 0 0 1 1 1 1 0 1 0 1	1

DETAILED DESCRIPTION

The ICL7115 is basically a successive approximation A/D converter with an internal structure much more complex than a standard SAR-type converter. Figure 2 shows the functional diagram of the ICL7115 14-bit A/D converter. The additional circuitry incorporated into the ICL7115 is used to perform error correction and to maintain the operating speed in the 40μs range.

The internal 17-bit DAC of the ICL7115 is designed around a radix of 1.85 rather than the traditional 2.00. This radix gives each bit of the DAC a weight of approximately 54% of the previous bit. The result is a useable range that extends to 3% beyond the full-scale input of the A/D. The actual value of each bit is measured and stored in the on-chip PROM. The absolute value of each bit weight then becomes relatively unimportant because of the error correction action of the ICL7115.

The output of the high-speed auto-zeroed comparator is fed to the data input of a 17-bit successive approximation register (SAR). This register is uniquely designed for the ICL7115 in that it tests bit pairs instead of individual bits in the manner of a standard SAR. At the beginning of the conversion cycle, the SAR turns on the MSB (B_{16}) and the MSB-4 bit (B_{12}). The sequence continues for each bit pair, B_x and B_{x-4}, until only the four LSBs remain. The sequence concludes by testing the four LSBs individually.

The SAR output is fed to the DAC register and to the preprogrammed 17-word by 17-bit PROM where it acts as PROM address. PROM data is fed to a 17-bit full-adder/accumulator where the decoded results from each successive phase of the conversion are summed with the previous results. After 20 clock cycles, the accumulator contains the

Note: All typical values have been guaranteed by characterization and are not tested.

final binary data which is latched and sent to the three-state output buffers. The accuracy of the A/D converter depends primarily upon the accuracy of the data that has been programmed into the PROM during the final test portion of the manufacturing process.

The error correcting algorithm built into the ICL7115 reduces the initial accuracy requirements of the DAC. The overlap in the testing of bit pairs reduces the accuracy requirements on the comparator which has been optimized for speed. Since the comparator is auto-zeroed, no external adjustment is required to get ZERO code for ZERO input voltage.

Twenty clock cycles are required for the complete 14-bit conversion. The auto-zero circuitry associated with the comparator is employed during the last three clock cycles of the conversion to cancel the effect of offset voltage. Also during this time, the SAR and accumulator are reset in preparation for the start of the next conversion. When the Short Cycle ($\overline{SC}$) input is low, 18 clock cycles are required to complete a 12-bit conversion.

The overflow output of the 17-bit full-adder is also the OVerRange (OVR) output of the ICL7115. Unlike standard SAR-type A/D converters, the ICL7115 has the capability of providing valid useable data for inputs that exceed the full-scale range by as much as 3%.

OPTIMIZING SYSTEM PERFORMANCE

The FORCE and SENSE inputs for V_{IN} and V_{REF} are also shown driven by external op-amps. This technique eliminates the effect of small voltage drops which can appear between the input pin of the IC package and the actual resistor on the chip. If the small gauge wire and the bonds that connect the chip to its package have more than 300mΩ of total series resistance, the result can be a voltage error equivalent to 1LSB. If no op-amps are used for V_{IN} and V_{REF}, connections should be made directly to the SENSE lines. The external op-amps also serve to transform the relatively low impedance at the V_{IN} and V_{REF} pins into a high impedance. The input offset voltages of these amplifiers should be kept low in order to maintain the overall A/D converter system accuracy.

When using A/D converters with more than 12 bits of resolution, special attention must be paid to grounding and the elimination of potential ground loops. A ground loop can be formed by allowing the return current from the ICL7115's DAC to flow through traces that are common to other analog circuitry. If care is not taken, this current can generate small unwanted voltages that add to or detract from the reference or input voltages of the A/D converter.

Ground loops can be eliminated by the use of the analog ground FORCE and SENSE lines provided on the ICL7115 as shown in Figures 5 and 6. In Figure 5 the FORCE line is the only point that is connected to system analog ground. In Figure 6, the op-amp A_3 forces the voltage at AGND to be equal to analog system ground. The addition of this op-amp overcomes the main deficiency of the arrangement in Figure 5: the V_{IN} and V_{REF} sources are not referenced to true analog system ground.

The clamp diodes in Figure 6 are required because spurious op-amp output on AGNDf during power-on can exceed the absolute max rating of ±1.0V between AGDf and DGND. The two inverse-parallel diodes clamp the voltage between AGNDs and DGND to ±0.7V.

INPUT WARNING

As with any CMOS integrated circuit, no input voltages should be applied to the ICL7115 until the ±5V power supplies have stabilized.

INTERFACING TO DIGITAL SYSTEMS

The ICL7115 provides three-state data output buffers, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, and bus select inputs (A_0 and BUS) for interfacing to a wide variety of microcomputers and digital systems. The I/O Control Truth Table shows the functions of the digital control lines. The BUS select and A_0 lines are provided to enable the output data onto either 8-bit or 16-bit data buses. A conversion is initiated by a $\overline{WR}$ pulse (pin 33) when $\overline{CS}$ (pin 3) is low. Data is enabled on the bus when the chip is selected and $\overline{RD}$ (pin 4) is low.

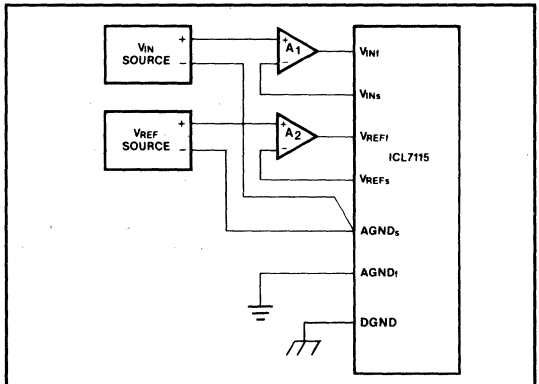


Figure 5: V_{IN} and V_{REF} Input Buffers

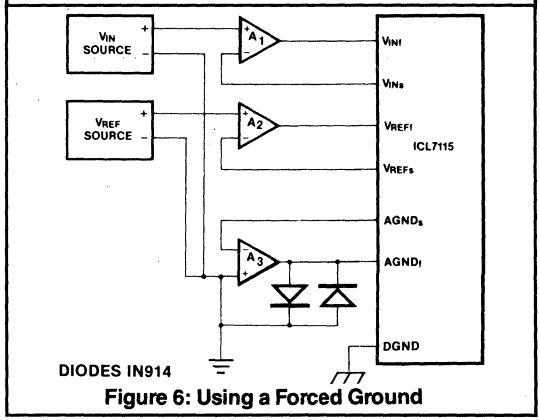
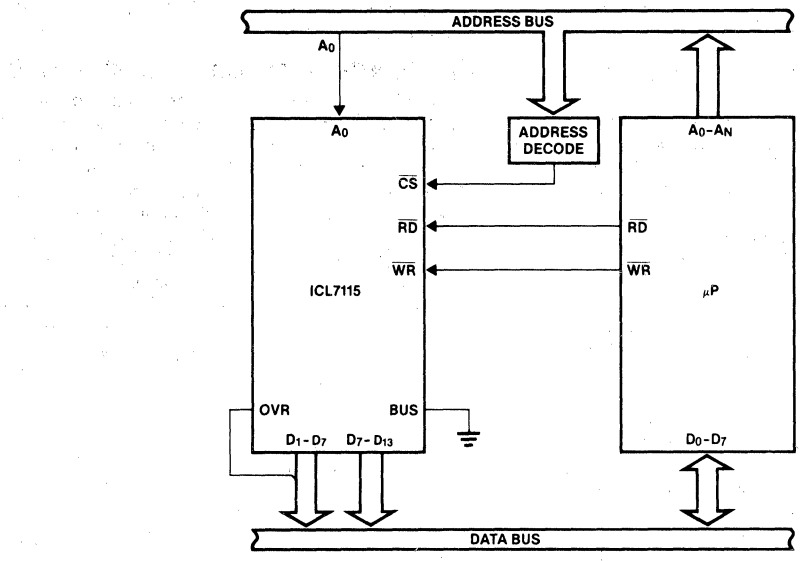


Figure 6: Using a Forced Ground

Figure 7 illustrates a typical interface to an 8-bit microcomputer. The "Start and Wait" operation requires the fewest external components and is initiated by a low level on the $\overline{WR}$ input to the ICL7115 after the I/O or memory-mapped address decoder has brought the $\overline{CS}$ input low. After executing a delay or utility routine for a period of time greater than the conversion time of the ICL7115, the processor issues two consecutive bus addresses to read output data into two bytes of memory. A low level on A_0 enables the LSBs and a high level enables the MSBs.

Note: All typical values have been guaranteed by characterization and are not tested.



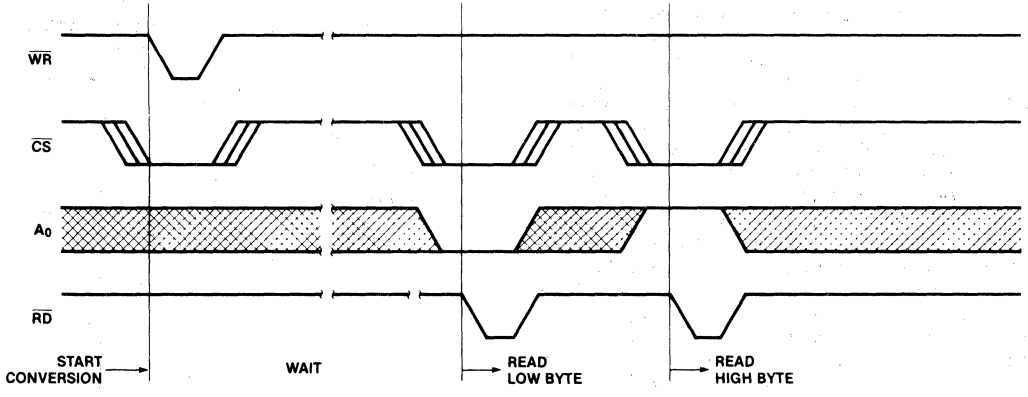


Figure 7: "Start and Wait" Operation

By adding a three-state buffer and two control gates, the End-of-Conversion (EOC) output can be used to control a "Start and Poll" interface (Figure 8). In this mode, the A_0 and $\overline{CS}$ lines connect the EOC output to the data bus along with the most significant byte of data. After pulsing the $\overline{WR}$ line to initiate a conversion, the microprocessor continually reads the most significant byte until it detects a high level on the EOC bit. The "Start and Poll" interface increases data throughput compared with the "Start and Wait" method by eliminating delays between the conversion termination and the microprocessor read operation.

Note: All typical values have been guaranteed by characterization and are not tested.

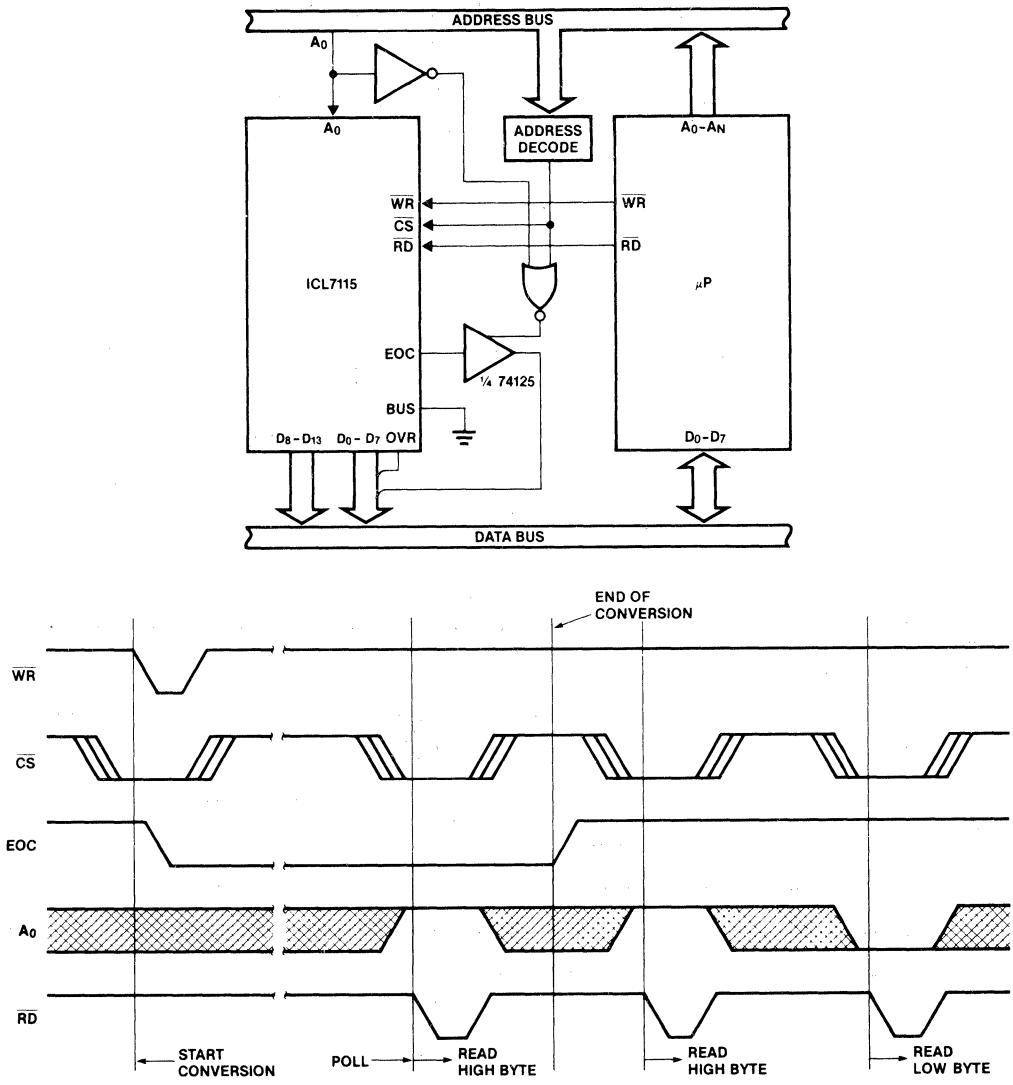
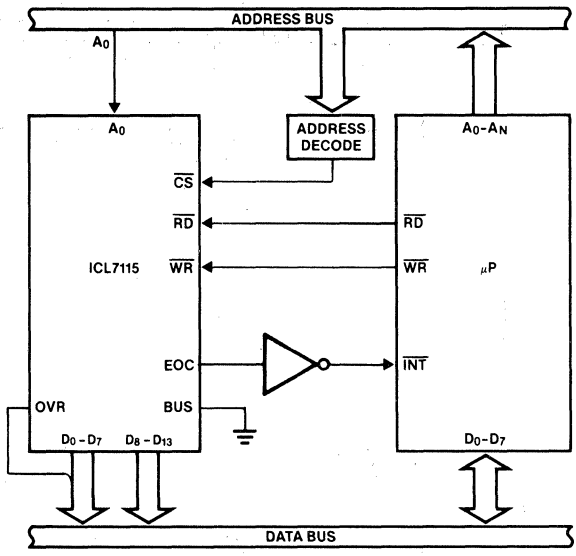


Figure 8: "Start and Poll" Operation

Other interface configurations can be used to increase data throughput without monopolizing the microprocessor during waiting or polling operations by using the EOC line as an interrupt generator as shown in Figure 9. After the conversion cycle is initiated, the microprocessor can continue to execute routines that are independent of the A/D converter until the converter's output register actually holds valid data. For fastest data throughput, the ICL7115 can be connected directly to the data bus but controlled by way of a Direct Memory Access (DMA) controller as shown in Figure 9.

Note: All typical values have been guaranteed by characterization and are not tested.



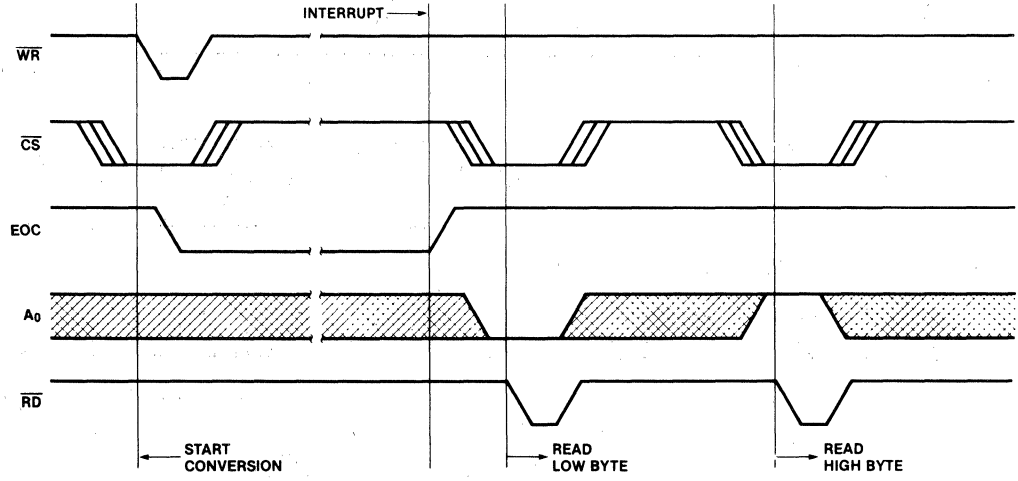


Figure 9: Using EOC as an Interrupt

Note: All typical values have been guaranteed by characterization and are not tested.

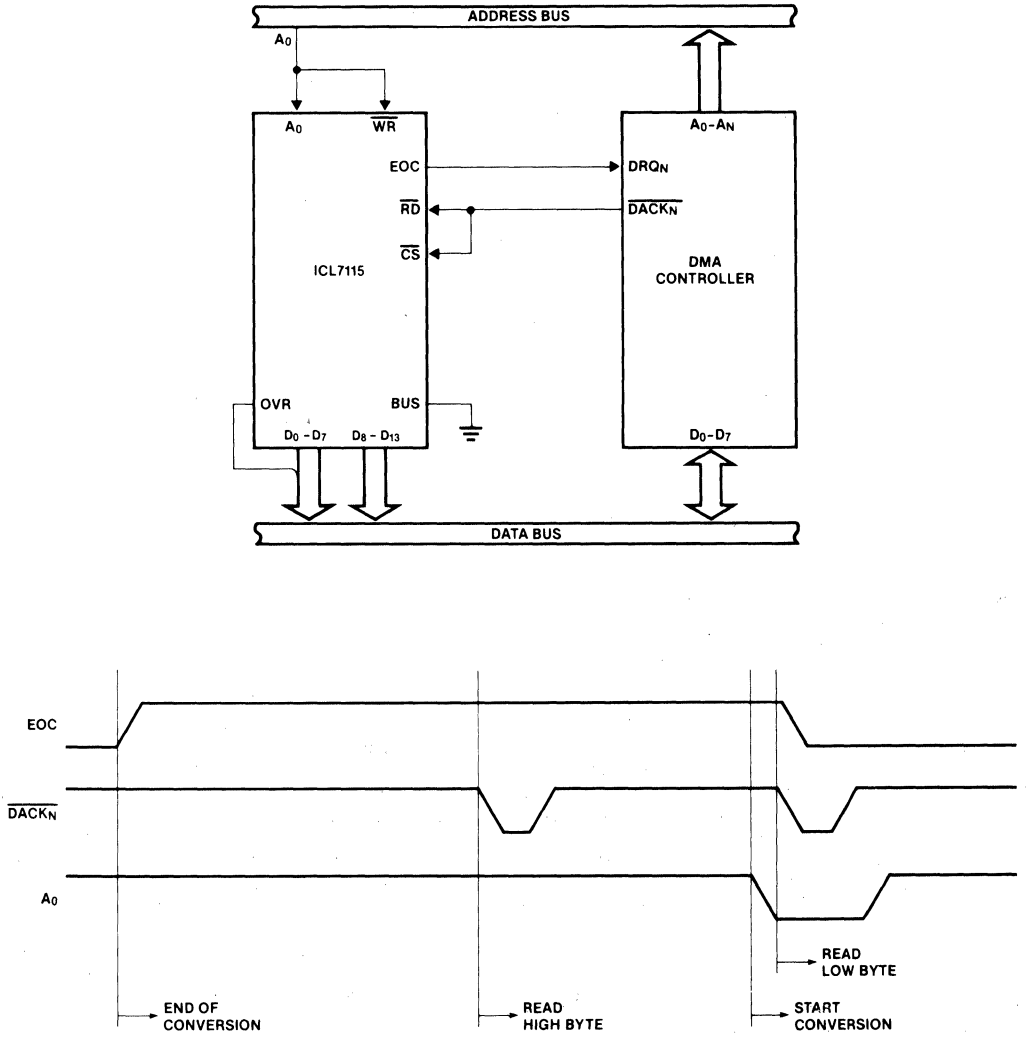


Figure 10: Data to Memory via DMA Controller

Note: All typical values have been guaranteed by characterization and are not tested.

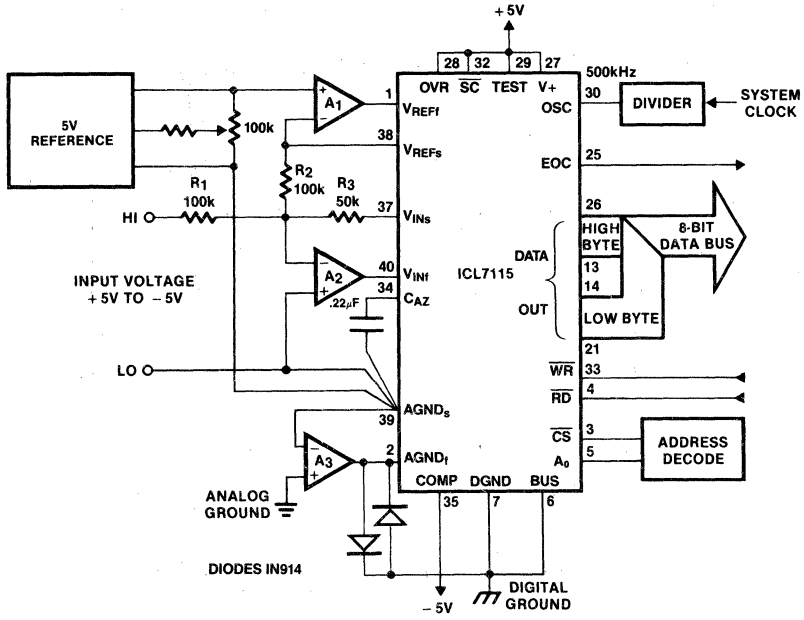


Figure 11: Typical Application with Bipolar Input Range, Forced Ground, and 5 Volt Ultra-Stable Reference

APPLICATIONS

Figure 11 shows a typical application of the ICL7115 14-bit A/D converter. A bipolar input voltage range of +5V to −5V is the result of using the current through R_2 to force a 1/2 scale offset on the input amplifier (A_2). The output of A_2 swings from 0V to −5V. The overall gain of the A/D is varied by adjusting the 100kΩ trim resistor, R_5. Since the ICL7115 is automatically zeroed every conversion, the system gain and offset stability will be superb as long as a reference with a tempco of 1ppm/°C and stable external resistors are used.

In Figure 11, note that the 0.22μF auto-zero capacitor is connected directly between the C_{AZ} pin and analog ground SENSE. A_3 forces the analog ground of the ICL7115 to be the zero reference for the input signal. Its offset voltage is not important in this example because the voltage to be digitized is referred to the analog ground SENSE line rather than system analog ground. It is important to note that since the 7115's DAC current flows in A_1, A_2 and A_3 these amplifiers should be wideband (GBW > 20MHz) types to minimize errors.

The clock for the ICL7115 is taken from whatever system clock is available and divided down to the 500kHz level for a conversion time of 40μs. Output data is controlled by the BUS and A_0 inputs. Here they are set for 8-bit bus operation with BUS grounded and A_0 under the control of the address decode section of the external system.

Because the ICL7115's internal accumulator generates accurate output data for input signals as much as 3% greater than full-scale, and because the converter's OVR output flags overrange inputs, a simple microprocessor routine can be employed to precisely measure and correct for system gain and offset errors. Figure 12 shows a typical data acquisition system that uses a 5.0V reference, input signal multiplexer, and input signal Track/Hold amplifier. Two of the multiplexer's input channels are dedicated to sampling the system analog ground and reference voltage. Here, as in Figure 11, bipolar operation is accommodated by an offset resistor between the reference voltage and the summing junction of A_1. A flip-flop in IC_3 sets IC_2's Track/Hold input after the microprocessor has initiated a WR command, and resets when EOC goes high at the end of the conversion.

The first step in the system calibration routine is to select the multiplexer channel that is connected to system analog ground and initiate a conversion cycle for the ICL7115. The results represent the system offset error which comes from the sum of the offsets from IC_1, IC_2, and A_1. Next the channel connected to the reference voltage is selected and measured. These results, minus the system offset error, represent the system full-scale range. A gain error correction factor can be derived from this data. Since the ICL7115 provides valid data for inputs that exceed full-scale by as much as 3%, the OVR output can be thought of as a valid 15th data bit. Whenever the OVR bit is high, however, the total 14-bit result should be checked to insure that it falls within 100% and 103% of full-scale. Data beyond 103% of full-scale should be discarded.

Note: All typical values have been guaranteed by characterization and are not tested.

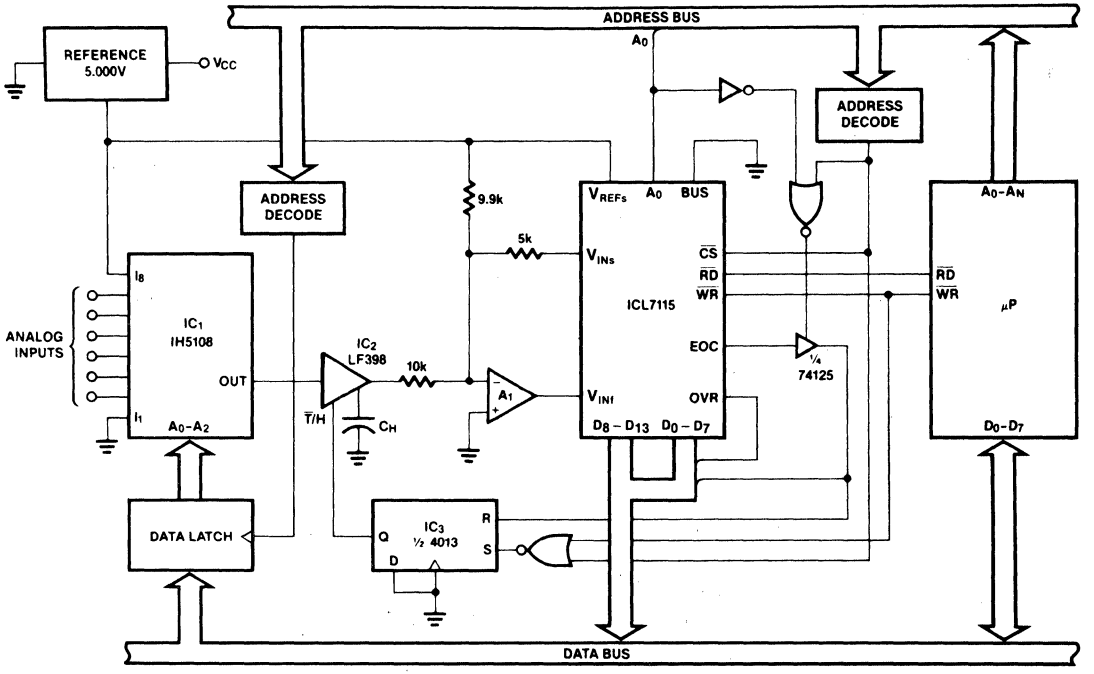


Figure 12: Multi-Channel Data Acquisition System with Zero and Reference Lines Brought to Multiplexer for System Gain and Offset Error Correction

The ICL7115 provides an internal inverter which is brought out to pins OSC1 and OSC2, for crystal or ceramic resonator oscillator operation. The clock frequency is calculated from:

$$f_{CLK} = \frac{20}{t_{conv}} \text{ for 14-bit operation}$$

and

$$f_{CLK} = \frac{18}{t_{conv}} \text{ for 12-bit operation}$$

6

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7116/7117
3½-Digit LCD/LED Single-Chip A/D Converter with Display Hold

GENERAL DESCRIPTION

The Intersil ICL7116 and 7117 are high performance, low power 3-½ digit A/D converters. All the necessary active devices are contained on a single CMOS I.C., including seven segment decoders, display drivers, reference, and a clock. The 7116 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive; the 7117 will directly drive an instrument-size light emitting diode (LED) display.

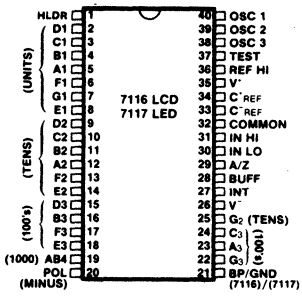
The 7116 and 7117 have almost all of the features of the 7106 and 7107 with the addition of a HoLD Reading input. With this input, it is possible to make a measurement and then retain the value on the display indefinitely. To make room for this feature the reference input has been referenced to Common rather than being fully differential. These circuits retain the accuracy, versatility, and true economy of the 7106 and 7107. They feature auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA maximum, and roll over error of less than one count. The versatility of true differential input is of particular advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally, the true economy of single power supply operation (7116) enables a high performance panel meter to be built with the addition of only eleven passive components and a display.

FEATURES

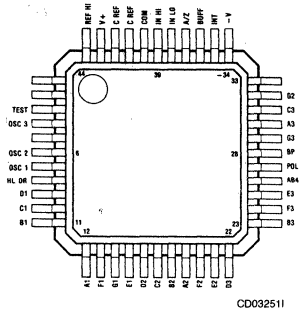
- **HoLD Reading Input Allows Indefinite Display Hold**
- **Guaranteed Zero Reading for 0 Volts Input**
- **True Polarity at Zero for Precise Null Detection**
- **1pA Input Current Typical**
- **True Differential Input**
- **Direct Display Drive — No External Components Required — LCD ICL7116**
  — LED ICL7117
- **Low Noise — Less Than 15μV pk-pk Typical**
- **On-Chip Clock and Reference**
- **Low Power Dissipation — Typically Less Than 10mW**
- **No Additional Active Circuits Required**
- **New Small Outline Surface Mount Package Available**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7116CDL	0°C to +70°C	40-Pin Ceramic DIP
ICL7116CPL	0°C to +70°C	40-Pin Plastic DIP
ICL7116CJL	0°C to +70°C	40-Pin CERDIP
ICL7116CM44	0°C to +70°C	44-Pin Surface Mount
ICL7117CDL	0°C to +70°C	40-Pin Ceramic DIP
ICL7117CPL	0°C to +70°C	40-Pin Plastic DIP
ICL7117CJL	0°C to +70°C	40-Pin CERDIP



CD00840I



CD03251I

Figure 1: Pin Configurations

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7116/7117

INTERSIL

ABSOLUTE MAXIMUM RATINGS

ICL7116

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input) (Note 1) . V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
HLDR, Clock Input..... Test to V^+
Power Dissipation (Note 2)
Ceramic Package 1000mW
Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) .....300°C

ICL7117

Supply Voltage V^+ ..... +6V
V^- ..... −9V
Analog Input Voltage (either input) (Note 1) ..V^+ to V^-
Reference Input Voltage (either input) .....V^+ to V^-
HLDR, Clock Input..... Gnd to V^+
Power Dissipation (Note 2)
Ceramic Package 1000mW
Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) .....300°C

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$\|V_{IN}\| \simeq$ 200.0mV	−1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200mV or Full Scale = 2.000V (Note 7)	−1	±0.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V, Full Scale = 200.0mV		50		μV/V
Noise (Pk — Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0V (Note 7)		1	10	pA
Zero Reading Drift	V_{IN} = 0 0°C < T_A < 70°C (Note 7)		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0°C < T_A < 70°C (Ext. Ref. 0ppm/°C) (Note 7)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current for 7117)	V_{IN} = 0		0.8	1.8	mA
V^- Supply Current (7117 only)			0.6	1.8	mA
Analog Common Voltage (With respect to pos. supply)	25kΩ between COMMON & pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to pos. Supply)	25kΩ between COMMON & pos. Supply		80		ppm/°C
Input Resistance, Pin 1 (Note 6)		30	70		kΩ
V_{IL}, Pin 1 (7116 only)				TEST + 1.5	V
V_{IL}, Pin 1 (7117 only)				GND + 1.5	V
V_{IH}, Pin 1 (Both)		V^+ − 1.5			V
7116 ONLY Pk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage (Note 5)	$V^+ - V^- = 9V$	 4 4	 5 5	 6 6	V

6

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7116/7117

ELECTRICAL CHARACTERISTICS (CONT.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
7117 ONLY Segment Sinking Current (Except Pin 19 and 20) (Pin 19 only) (Pin 20 only)	V^+ = 5.0V Segment Voltage = 3V	 5 10 4	 8.0 16 7		 mA

NOTES:
3. Unless otherwise noted, specifications apply to both the 7116 and 7117 at T_A = 25°C, f_{clock} = 48kHz. 7116 is tested in the circuit of Figure 4. 7117 is tested in the circuit of Figure 5.
4. Refer to "Differential Input" discussion.
5. Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
6. The 7116 logic input has an internal pull-down resistor connected from HLDR, pin 1, to TEST, pin 37. The 7117 logic input has an internal pull-down resistor connected from HLDR, pin 1 to GROUND, pin 21.
7. Not tested, guaranteed by design.

TEST CIRCUITS

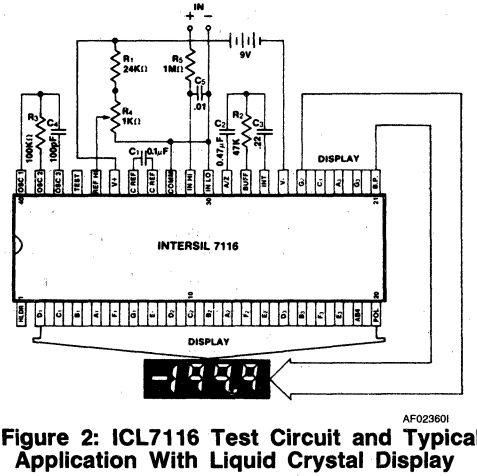


Figure 2: ICL7116 Test Circuit and Typical Application With Liquid Crystal Display

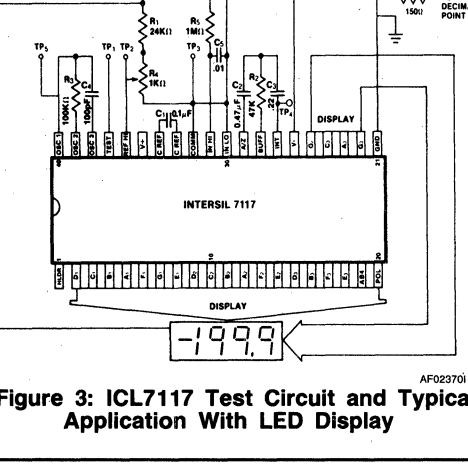


Figure 3: ICL7117 Test Circuit and Typical Application With LED Display

DETAILED DESCRIPTION

Analog Section

Figure 4 shows the Analog Section for the ICL7116 and 7117. Each measurement cycle is divided into three phases. They are (1) auto-zero (A/Z), (2) signal integrate (INT) and (3) de-integrate (DE).

Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

Signal Integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is $1000 \left(\frac{Vin}{Vref}\right)$.

Note: All typical values have been guaranteed by characterization and are not tested.

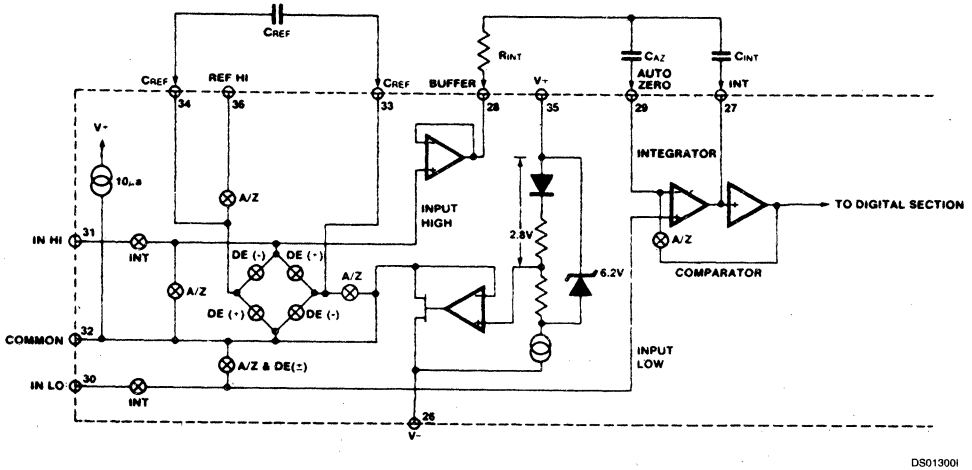


Figure 4: Analog Section of 7116/7117

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of typically 86dB. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worse case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing to within 0.3 volts of either supply without loss of linearity. See A032 for a discussion of the effects of stray capacitance.

Reference

The reference input must be generated as a positive voltage with respect to COMMON. Note that current flowing in the COMMON pins' internal resistance causes a slight shift in the effective reference voltage, disturbing ratiometric readings at low reference inputs. If possible, do not let this current vary.

Analog COMMON

This pin is included primarily to set the common mode voltage for battery operation (7116) or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8 volts less than the positive supply. This is selected to provide proper operation with a minimum end-of-life battery voltage of about 6V. However, the analog COMMON does have some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (> 7V), the COMMON voltage will have a low voltage coefficient (.001%/V), low output impedance ($\simeq$15Ω), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on-chip reference should also be recognized, however. With the 7117, the internal heating which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full scale from 25μV to 80μVpk-pk. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111 (8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an overload condition. This is because overload is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between overload and a nonoverload count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

The 7116, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added, as shown in Figure 5.

Analog COMMON is also the voltage that input low returns to during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7116/7117

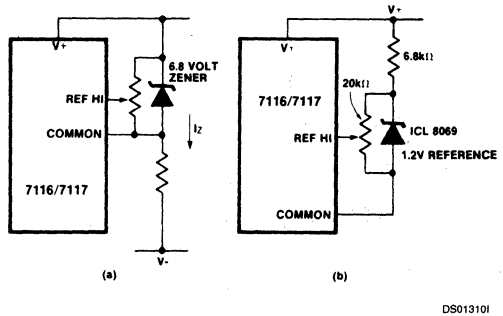


Figure 5: Using an External Reference

Within the IC, analog COMMON is tied to an N channel FET that can sink 30mA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10μA of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

TEST

The TEST pin serves two functions. On the 7116 it is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 6 and 7 show such an application. No more than a 1mA load should be applied.

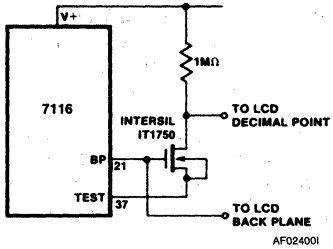


Figure 6: Simple Inverter for Fixed Decimal Point

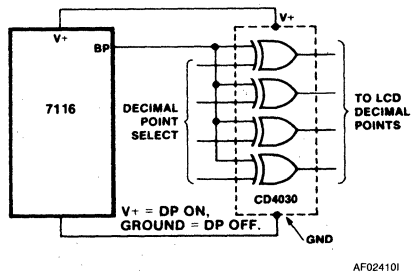


Figure 7: Exclusive 'OR' Gate for Decimal Point Drive

The second function is a "lamp test". When TEST is pulled to high (to V^+) all segments will be turned on and the display should read – 1888. **[Caution: on the 7116, in the lamp test mode, the segments have a constant DC voltage (no square-wave) and will burn the LCD display if left in this mode for several minutes.]**

DIGITAL SECTION

Figures 8 and 9 show the digital section for the 7116 and 7117, respectively. In the 7116, an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments.

Figure 9 is the Digital Section of the 7117. It is identical to that of the 7116 except the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2 to 8mA, typical for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16mA.

In both devices the polarity indicator is ON for negative analog inputs. This can be reversed by simply reversing IN LO and IN HI.

HOLD Reading Input

The HLDR input will prevent the latch from being updated when this input is at a logic "1". The chip will continue to make A/D conversions, however, the results will not be updated to the internal latches until this input goes low. This input can be left open or connected to TEST (7116) or GROUND (7117) to continuously update the display. This input is CMOS compatible, and has a 70kΩ typical resistance to either TEST (7116) or GROUND (7117).

Note: All typical values have been guaranteed by characterization and are not tested.

DISPLAY FONT

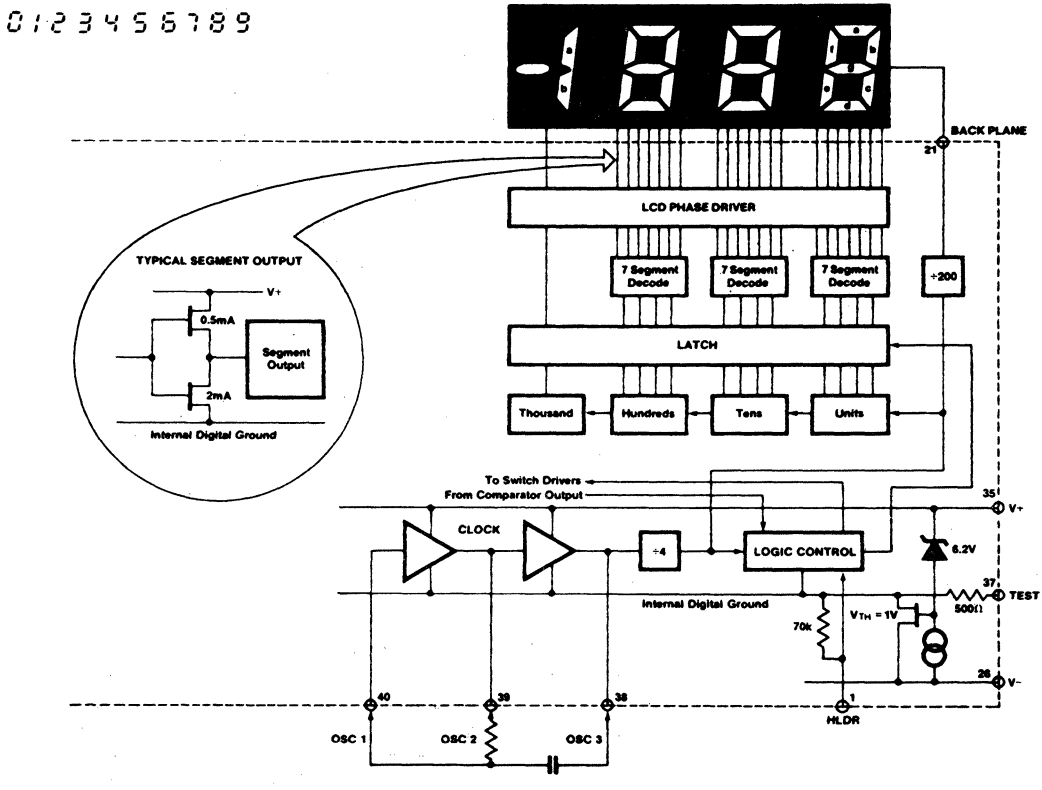


Figure 8: Digital Section 7116

Note: All typical values have been guaranteed by characterization and are not tested.

DISPLAY FONT (CONT.)

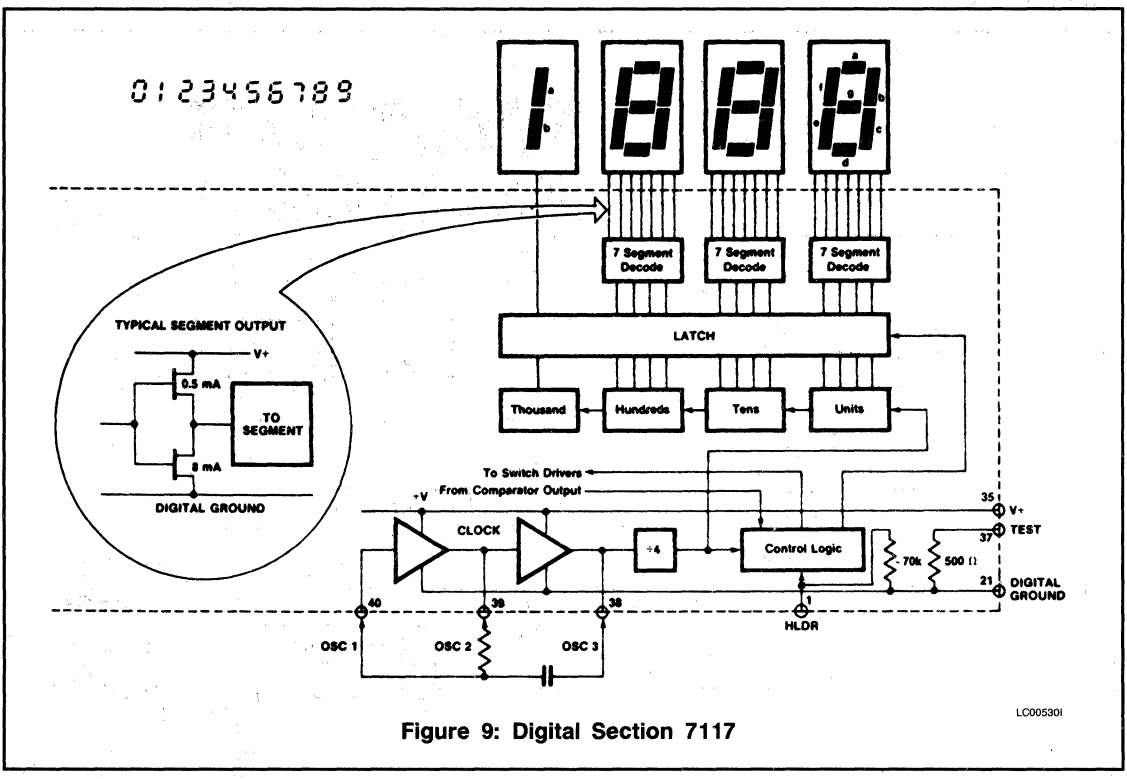


Figure 9: Digital Section 7117

System Timing

Figure 10 shows the clocking arrangement used in the 7116 and 7117. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

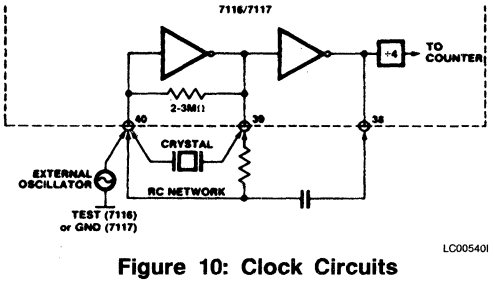


Figure 10: Clock Circuits

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, 33 1/3kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, 66 2/3kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

COMPONENT VALUE SELECTION

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They can supply 20μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volts full scale, 470kΩ is near optimum and similarly a 47kΩ resistor is optimum for a 200.0mV scale.

Note: All typical values have been guaranteed by characterization and are not tested.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the 7116 or the 7117, when the analog COMMON is used as a reference, a nominal ±2 volt full scale integrator swing is fine. For the 7117 with ±5 volt supplies and analog common tied to supply ground, a ±3.5 to ±4 volt swing is nominal. For three readings/second (48kHz clock), nominal values for C_{INT} are 0.22μF and 0.10μF, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is it have low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full scale where noise is very important, a 0.47μF capacitor is recommended. On the 2 volt scale, a 0.047μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1μF capacitor gives good results in most applications. If rollover errors occur a larger value, up to 1.0μF may be required.

Oscillator Components

For all ranges of frequency a 100kΩ resistor is recommended and the capacitor is selected from the equation $f \simeq \frac{0.45}{RC}$. For 48kHz clock (3 readings/second), C = 100pF.

Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200.0mV and 2.000 volt scale, V_{REF} should equal 100.0mV and 1.000 volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select $V_{REF} = 0.341V$. Suitable values for integrating resistor and capacitor would be 120kΩ and 0.22μF. This makes the system slightly quieter and also avoids a divider network on the input. The 7117 with ±5 volts supplies can accept input signals up to ±4 volts. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

7117 Power Supplies

The 7117 is designed to work from ±5 volt supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors, and an inexpensive I.C. Figure 11 shows this application. See ICL7660 data sheet for an alternative.

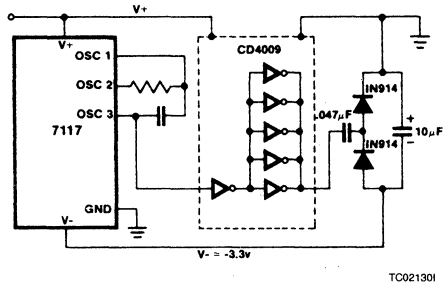


Figure 11: Generating Negative Supply from +5v

In fact, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5 volts in magnitude.
3. An external reference is used.

TYPICAL APPLICATIONS

The 7116 and 7117 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

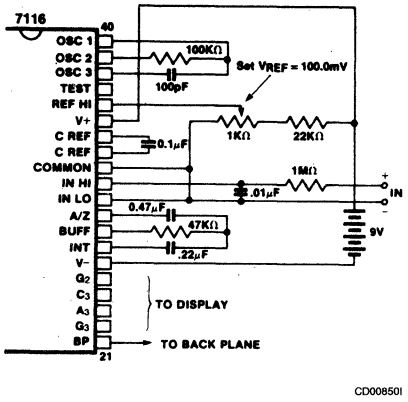
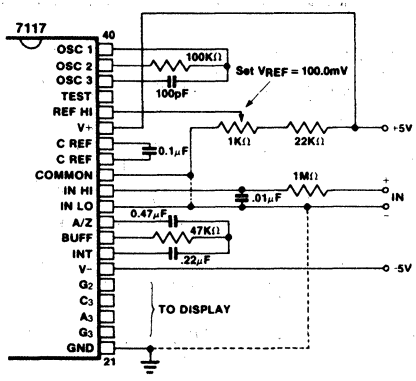


Figure 12: 7116 using the internal reference. Values shown are for 200.0mV full scale, 3 readings per second, floating supply voltage (9V battery).

Note: All typical values have been guaranteed by characterization and are not tested.

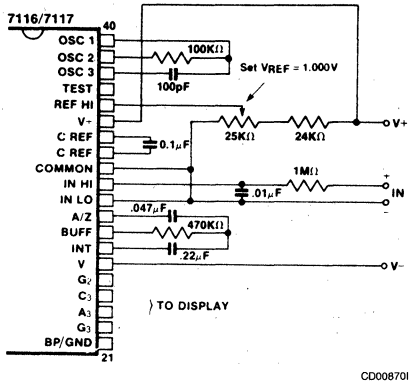
ICL7116/7117

TYPICAL APPLICATIONS (CONT.)



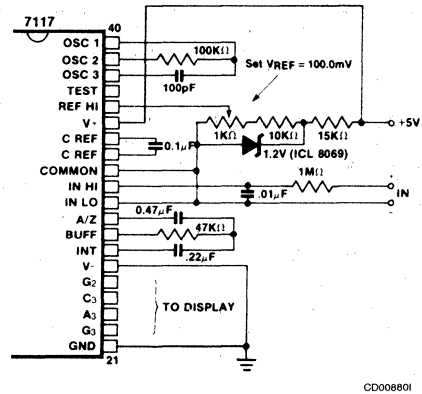
CD00860I

Figure 13: 7117 using the internal reference. Values shown are for 200.0mV full scale, 3 readings per second. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog Common.)



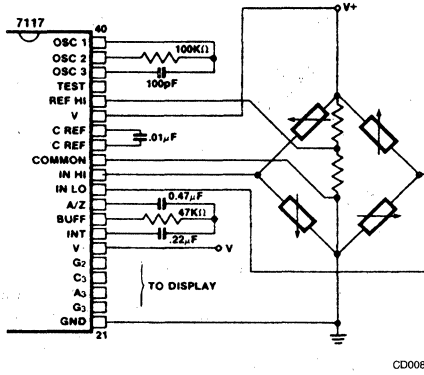
CD00870I

Figure 14: 7116/7117: Recommended component values for 2.000V full scale.



CD00880I

Figure 15: 7117 operated from single +5V supply. An external reference must be used in this application, since the voltage between V^+ and V^- is insufficient for correct operation of the internal reference.



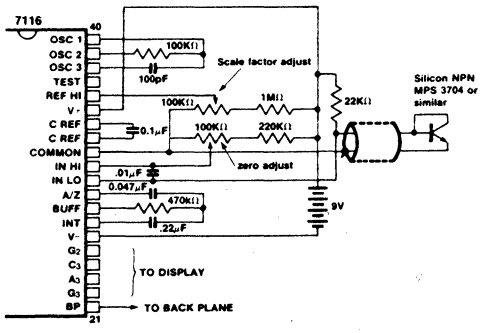
CD00890I

Figure 16: 7117 measuring ratiometric values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7116/7117

TYPICAL APPLICATIONS (CONT.)



CD009001

Figure 17: 7116 used as a digital centigrade thermometer. A silicon diode-connected transistor has a temperature coefficient of about −2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.

APPLICATION NOTES

A016 "Selecting A/D Converters," by David Fullagar.
A017 "The Integrating A/D Converter," by Lee Evans.
A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.
A019 "4½-Digit Panel Meter Demonstrator/ Instrumentation Boards," by Michael Dufort.
A023 "Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort.
A032 "Understanding the Auto-Zero and Common-Mode Behavior of the ICL7106/7/9 Family," by Peter Bradshaw.
A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106," by Larry Goff.
A047 "Games People Play with Intersil's A/D Converters," edited by Peter Bradshaw.
A052 "Tips for Using Single-Chip 3½-Digit A/D Converters," by Dan Watson.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7126
3½-Digit Low-Power Single-Chip A/D Converter

GENERAL DESCRIPTION

The Intersil ICL7126 is a high performance, very low power 3½-digit A/D converter. All the necessary active devices are contained on a single CMOS IC, including seven segment decoders, display drivers, reference, and clock. The 7126 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive. The supply current is 100μA, ideally suited for 9V battery operation.

The 7126 brings together an unprecedented combination of high accuracy, versatility, and true economy. It features auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA max., and rollover error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation allows a high performance panel meter to be built with the addition of only 10 passive components and a display.

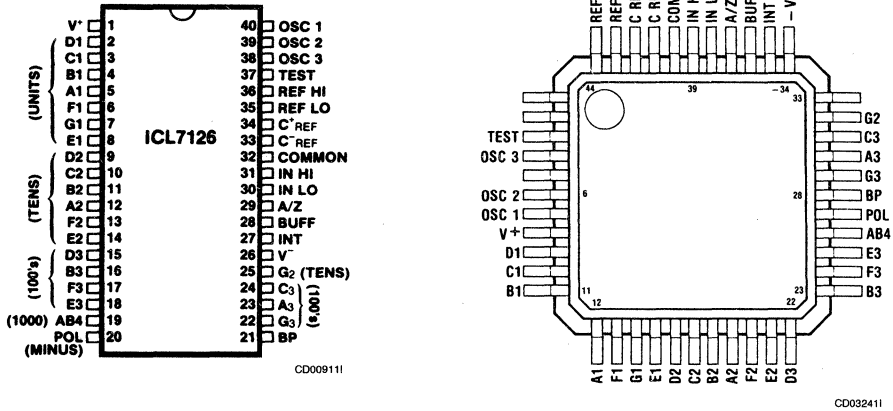
The ICL7126 can be used as a plug-in replacement for the ICL7106 in a wide variety of applications, changing only the passive components.

FEATURES

- **8,000 Hours Typical 9 Volt Battery Life**
- **Guaranteed Zero Reading for 0 Volts Input On All Scales**
- **True Polarity at Zero for Precise Null Detection**
- **1pA Typical Input Current**
- **True Differential Input and Reference**
- **Direct LCD Display Drive — No External Components Required**
- **Pin Compatible With The ICL7106**
- **Low Noise — Less Than 15μVp-p**
- **On-Chip Clock and Reference**
- **Low Power Dissipation Guaranteed Less Than 1mW**
- **No Additional Active Circuits Required**
- **Evaluation Kit Available (ICL7126EV/KIT)**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7126CDL	0°C to +70°C	40-Pin Ceramic DIP
ICL7126CPL	0°C to +70°C	40-Pin Plastic DIP
ICL7126CM44	0°C to +70°C	40-Pin Surface Mount
ICL7126RCPL	0°C to +70°C	40-Pin Plastic DIP
ICL7126CJL	0°C to +70°C	CERDIP
ICL7126EV/KIT		EVALUATION KIT



CD00911I

CD03241I

Figure 1: Pin Configurations

Note: All typical values have been guaranteed by characterization and are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (Either Input) (Note 1) .. V^+ to V^-
Reference Input Voltage (Either Input) ..... V^+ to V^-
Clock Input ..... TEST to V^+

Power Dissipation (Note 2)
Ceramic Package 1000mW
Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.

NOTE 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$\lvert -V_{IN} \rvert = +V_{IN} \simeq$ 200.0mV	−1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200mV or full scale = 2.000V	−1	±0.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200.0mV		50		μV/V
Noise (Pk - Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0V		1	10	pA
Zero Reading Drift	V_{IN} = 0 0°C < T_A < 70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0°C < T_A < 70°C (Ext. Ref. 0 ppm/°C)		1	5	ppm/°C
Supply Current (Does not include COMMON current)	V_{IN} = 0 (Note 6)		70	100	μA
Analog COMMON Voltage (With respect to pos. supply)	250kΩ between Common & pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog COMMON (with respect to pos. Supply)	250kΩ between Common & pos. Supply		150		ppm/°C
Pk-Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Power Dissipation Capacitance	vs. Clock Freq.		40		pF

NOTES: 3. Unless otherwise noted, specifications apply at T_A = 25°C, f_{clock} = 16kHz and are tested in the circuit of Figure 4.
4. Refer to "Differential Input" discussion.
5. Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
6. During auto zero phase, current is 10-20μA higher. 48kHz oscillator, Figure 5, increases current by 8μA (typ).
7. Extra capacitance of CERDIP package changes oscillator resistor value to 470kΩ or 150kΩ (1 reading/sec or 3 readings/sec).

Note: All typical values have been guaranteed by characterization and are not tested.

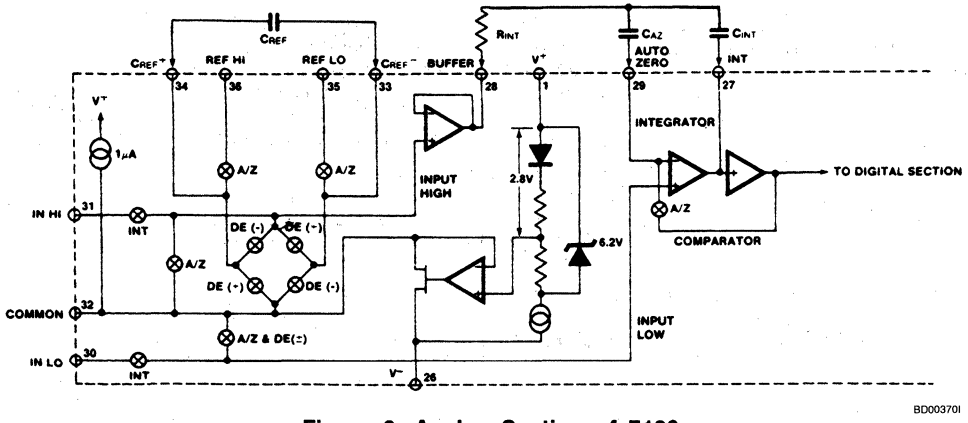


Figure 2: Analog Section of 7126

TEST CIRCUITS

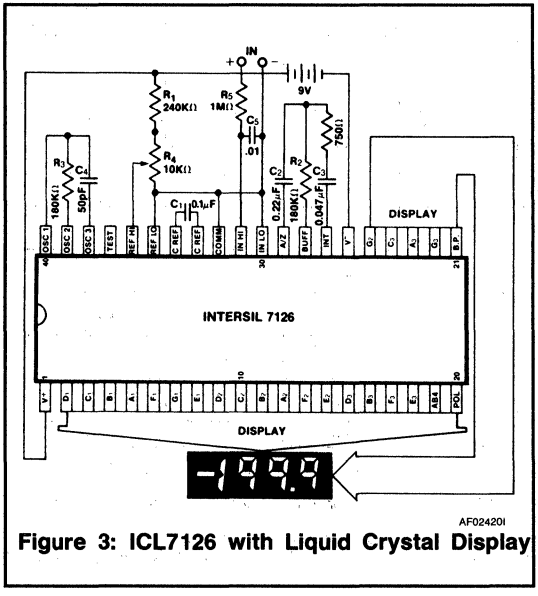


Figure 3: ICL7126 with Liquid Crystal Display

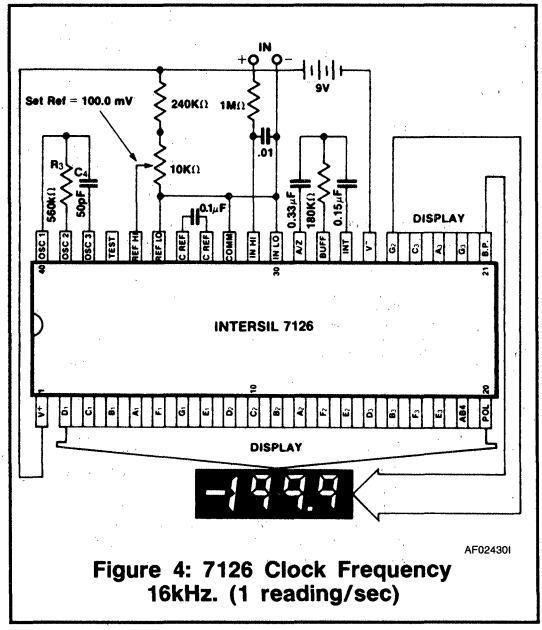


Figure 4: 7126 Clock Frequency 16kHz. (1 reading/sec)

Note: All typical values have been guaranteed by characterization and are not tested.

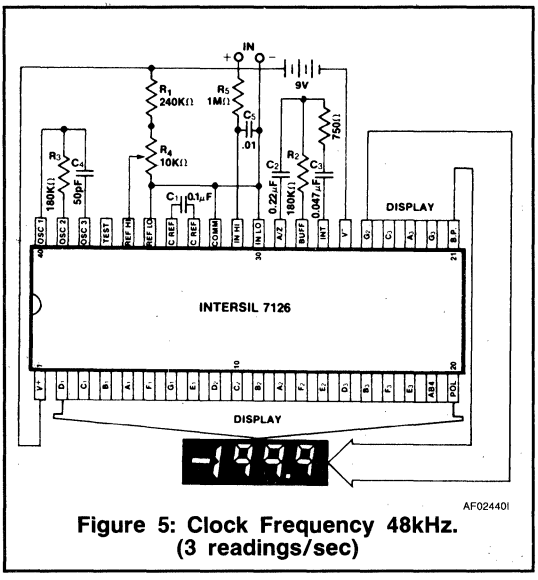


Figure 5: Clock Frequency 48kHz. (3 readings/sec)

DETAILED DESCRIPTION

Analog Section

Figure 2 shows the Functional Diagram of the Analog Section for the ICL7126. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) de-integrate (DE).

Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less then 10μV.

Signal Integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one Volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is $1000 \left(\frac{V_{IN}}{V_{REF}}\right)$.

Differential Input

The input can accept differential voltages anywhere within the common mode rante of the input amplifier; or specifically from 0.5 Volts below the positive supply to 1.0 Volt above the negative supply. In this range the system has a CMRR of 86 db typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing within 0.3 Volts of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition. (See Component Value Selection.)

Analog COMMON

This pin is included primarily to set the common mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8 Volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, the analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (< 7V), the COMMON voltage will have a low voltage coefficient (0.001%/%), low output impedance ($\simeq$15Ω), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on-chip reference should also be recognized, however. The reference temperature coefficient (TC) can cause some degradation in performance. Temperature changes of 2 to 8°C, typical for instruments, can give a scale factor error of a count or more. Also the common voltage will have a poor voltage coefficient when the total supply voltage is less than that which will cause the zener to regulate (< 7V). These problems are eliminated if an external reference is used, as shown in Figure 6.

Note: All typical values have been guaranteed by characterization and are not tested.

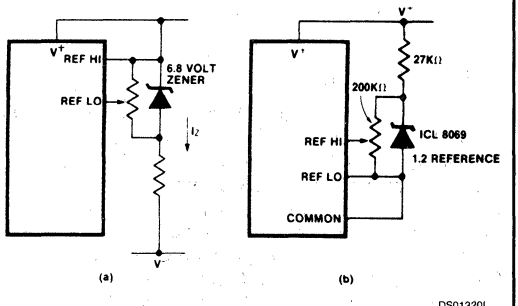


Figure 6: Using an External Reference

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET that can sink 3mA or more of current to hold the voltage 2.8 Volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 1μA of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

TEST

The TEST pin serves two functions. It is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 7 and 8 show such an application. No more than a 1mA load should be applied.

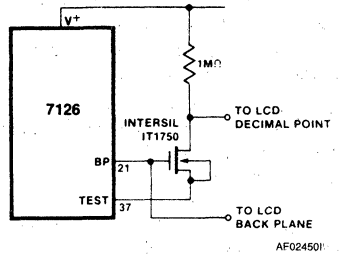


Figure 7: Simple Inverter for Fixed Decimal Point

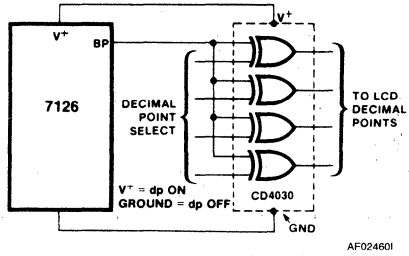


Figure 8: Exclusive 'OR' Gate for Decimal Point Drive

The second function is a "lamp test." When TEST is pulled high (to V^+) all segments will be turned on and the display should read — 1888. The TEST pin will sink about 10mA under these conditions.

Caution: In the lamp test mode, the segments have a constant D-C voltage (no square-wave) and may burn the LCD display if left in this mode for extended periods.

DIGITAL SECTION

Figure 9 shows the digital section for the 7126. An internal digital ground is generated from a 6 Volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 Volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments. The polarity indication is "ON" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

Note: All typical values have been guaranteed by characterization and are not tested.

DISPLAY FONT

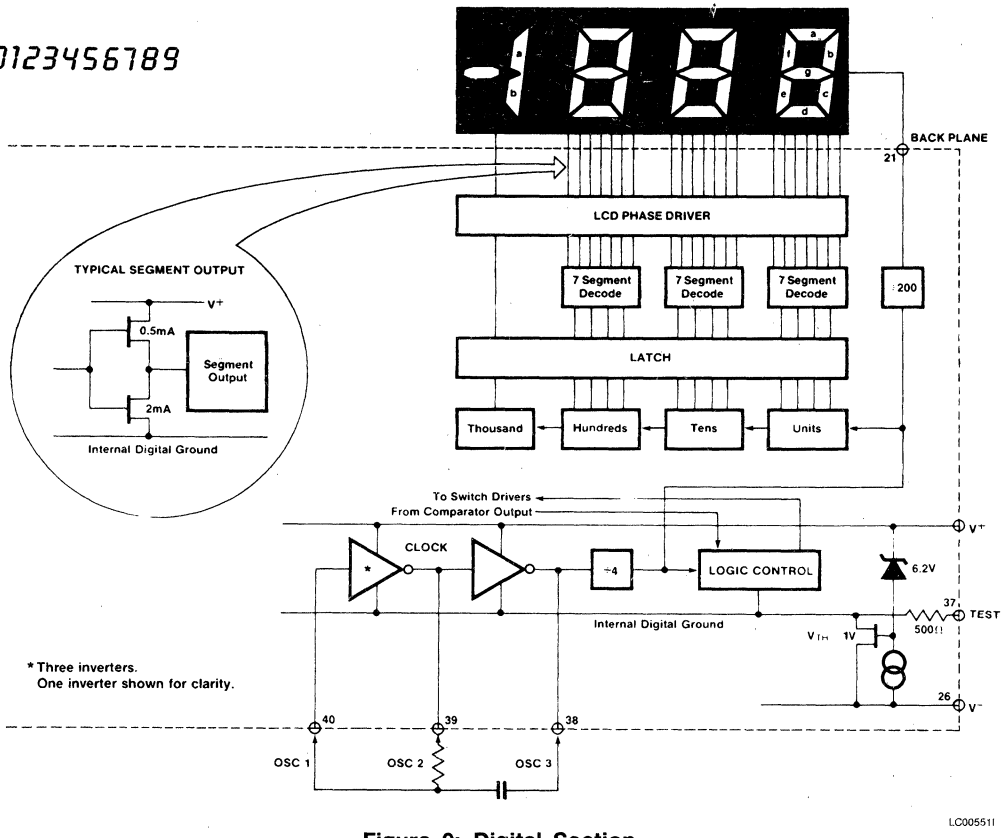


Figure 9: Digital Section

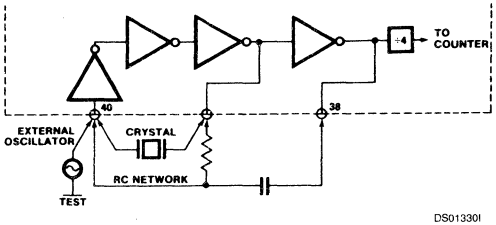


Figure 10: Clock Circuits

System Timing

Figure 10 shows the clocking arrangement used in the 7126. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 60kHz, 48kHz, 40kHz, 33-1/3kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 66-2/3kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

Note: All typical values have been guaranteed by characterization and are not tested.

COMPONENT VALUE SELECTION

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 6μA of quiescent current. They can supply ~1μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 Volt full scale, 1.8mΩ is near optimum and similarly 180kΩ for a 200.0mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 Volt from either supply). When the analog COMMON is used as a reference, a nominal ±2 Volt full scale integrator swing is fine. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.047μF, for 1/sec (16kHz) 0.15μF. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

The integrating capacitor should have low dielectric absorption to prevent roll-over errors. While other types may be adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

At three readings/sec., a 750Ω resistor should be placed in series with the integrating capacitor, to compensate for comparator delay. See App. Note A017 for a description of the need and effects of this resistor.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full scale where noise is very important, a 0.32μF capacitor is recommended. On the 2 Volt scale, a 0.033μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e., the REF LO pin is not analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally 1.0μF will hold the roll-over error to 0.5 count in this instance.

Oscillator Components

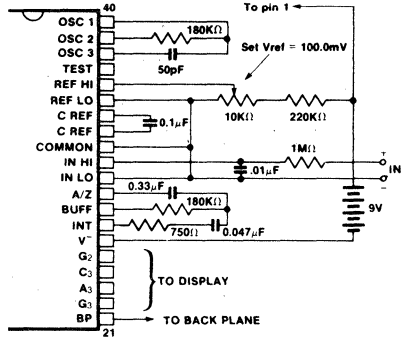
For all ranges of frequency a 50pF capacitor is recommended and the resistor is selected from the approximate equation $f \sim \frac{0.45}{RC}$. For 48kHz clock (3 readings/second), R = 180kΩ.

Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200.0mV and 2.000 Volt scale, V_{REF} should equal 100.0mV and 1.000 Volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select V_{REF} = 0.341V. A suitable value for integrating resistor would be 330kΩ. This makes the system slightly quieter and also avoids the necessity of a divider network on the input. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighting systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

TYPICAL APPLICATIONS

The 7126 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

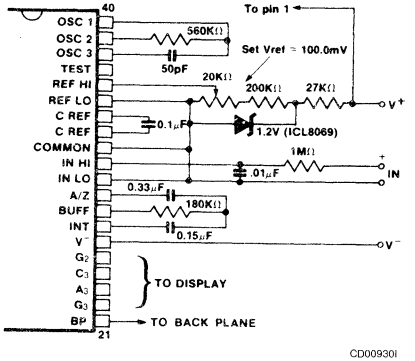


CD00920I

Figure 11: 7126 using the internal reference.

Values shown are for 200.0mV full scale, 3 readings per second, floating supply voltage (9V battery).

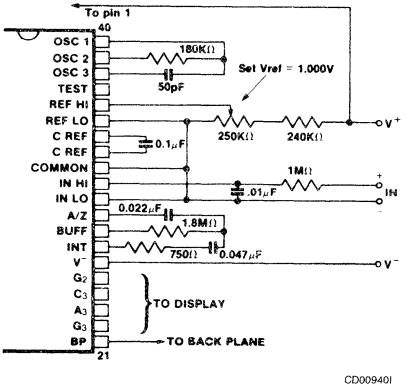
Note: All typical values have been guaranteed by characterization and are not tested.



CD00930I

Figure 12: 7126 with an external band-gap reference (1.2V type).

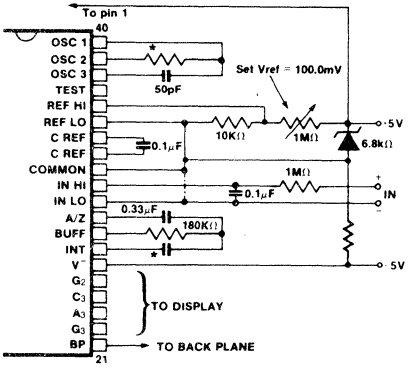
IN LO is tied to COMMON, thus establishing the correct common mode voltage. COMMON acts as a pre-regulator for the reference. Values shown are for 1 reading per second.



CD00940I

Figure 13: Recommended component values for 2.000V full scale, 3 readings per second.

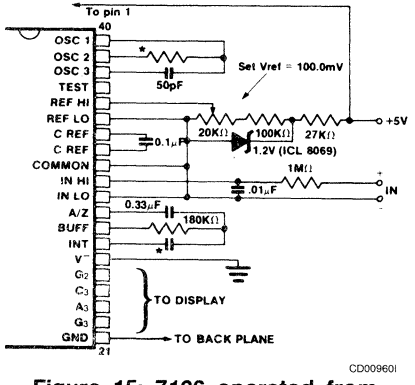
For 1 reading per second, delete 750Ω resistor, change C_{INT}, R_{OSC} to values of Figure 12.



CD00950I

Figure 14: 7126 with Zener diode reference.

Since low T.C. zeners have breakdown voltages ~6.8V, diode must be placed across the total supply (10V). As in the case of Figure 13, IN LO may be tied to COMMON.



CD00960I

Figure 15: 7126 operated from single +5V supply.

An external reference must be used in this application, since the voltage between V^+ and V^- is insufficient for correct operation of the internal reference.

6

Note: All typical values have been guaranteed by characterization and are not tested.

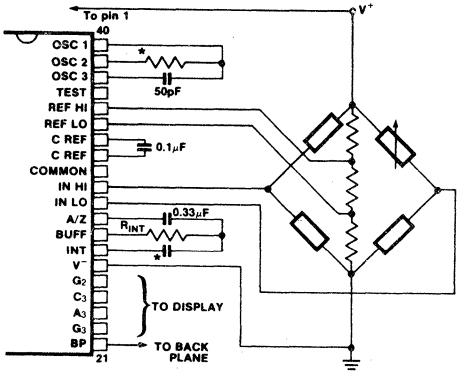


Figure 16: 7126 measuring ratiometric values of Quad Load Cell.

The resistor values within the bridge are determined by the desired sensitivity.

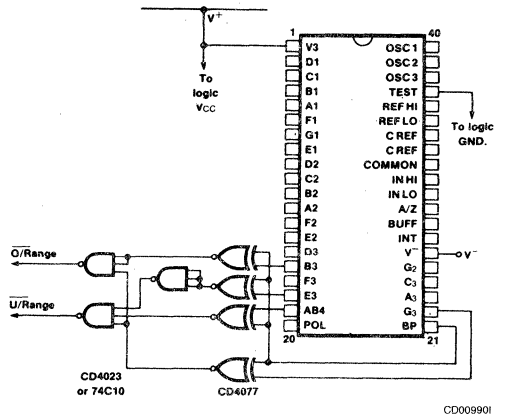


Figure 18: Circuit for developing Underrange and Overrange signals from 7126 outputs.

*Values depend on clock frequency. See Figure 11, 12, 13.

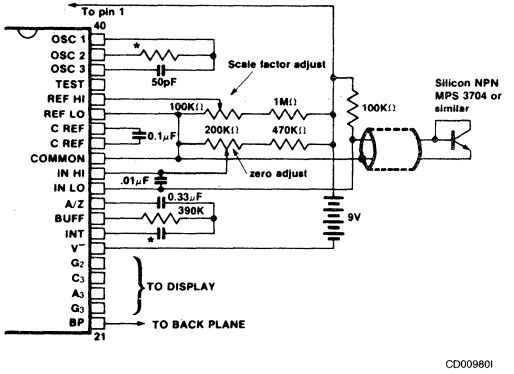
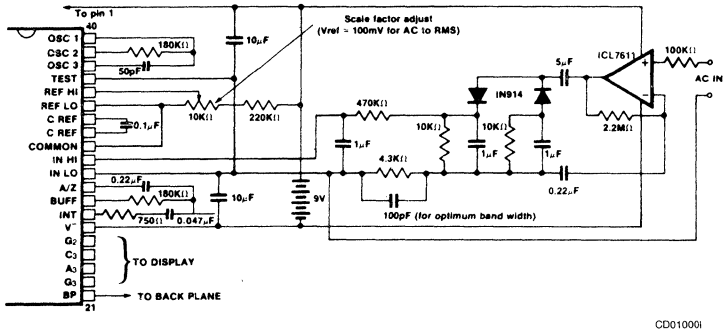


Figure 17: 7126 used as a digital centigrade thermometer.

A silicon diode-connected transistor has a temperature coefficient of about −2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.

Note: All typical values have been guaranteed by characterization and are not tested.



CD01000I

Figure 19: AC to DC Converter with 7126. Test is used as a common mode reference level to ensure compatibility with most op-amps.

APPLICATION NOTES

A016 "Selecting A/D Converters", by David Fullagar.
A017 "The Integrating A/D Converter", by Lee Evans.
A018 "Do's and Don'ts of Applying A/D Converters", by Peter Bradshaw and Skip Osgood.
A019 "4½-Digit Panel Meter Demonstrator/ Instrumentation Boards", by Michael Dufort.
A023 "Low Cost Digital Panel Meter Designs", by David Fullagar and Michael Dufort.
A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106/7/9 Family", by Peter Bradshaw.
A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106", by Larry Goff.
A052 "Tips for Using Single-Chip 3½-Digit A/D Converters", by Dan Watson.

7126 EVALUATION KIT

After purchasing a sample of the 7126, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application.

To facilitate evaluation of this unique circuit, Intersil is offering a kit which contains all the necessary components to build a 3½-digit panel meter. With the ICL7126EV/KIT and the small number of additional components required, an engineer or technician can have the system "up and running" in about half an hour. The kit contains a circuit board, a display (LCD), passive components, and miscellaneous hardware.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7129

4½ Digit LCD Single-Chip A/D Converter

GENERAL DESCRIPTION

The Intersil ICL7129 is a very high-performance 4½-digit analog-to-digital converter that directly drives a multiplexed liquid crystal display. This single-chip CMOS integrated circuit requires only a few passive components and a reference to operate. It is ideal for high-resolution hand-held digital multimeter applications.

The performance of the ICL7129 has not been equaled before in a single-chip A/D converter. The successive integration technique used in the ICL7129 results in accuracy better than 0.005% of full-scale and resolution down to 10μV/count.

The ICL7129, drawing only 1mA from a 9V battery, is well suited for battery powered instruments. Provision has been made for the detection and indication of a "LOW/BATTERY" condition. Autoranging instruments can be made with the ICL7129 which provides overrange and underrange outputs and 10:1 range changing input. The ICL7129 instantly checks for continuity, giving both a visual indication and a logic level output which can enable an external audible transducer. These features and the high performance of the ICL7129 make it an extremely versatile and accurate instrument-on-a-chip.

FEATURES

- **±19,999 Count A/D Converter Accurate to ±3 Count**
- **10μV Resolution On 200mV Scale**
- **110dB CMRR**
- **Direct LCD Display Drive**
- **True Differential Input and Reference**
- **Low Power Consumption**
- **Decimal Point Drive Outputs**
- **Overrange and Underrange Outputs**
- **Low Battery Detection and Indication**
- **10:1 Range Change Input**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE	PACKAGE
ICL7129CPL	0°C to +70°C	40-Pin Plastic

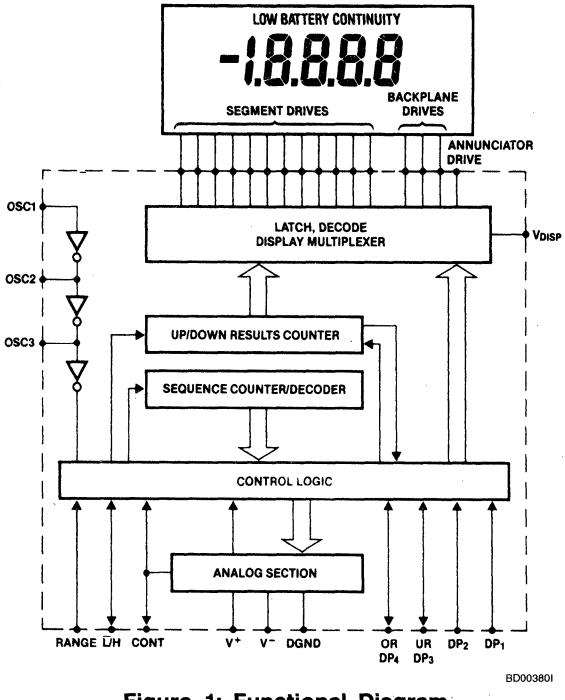


Figure 1: Functional Diagram

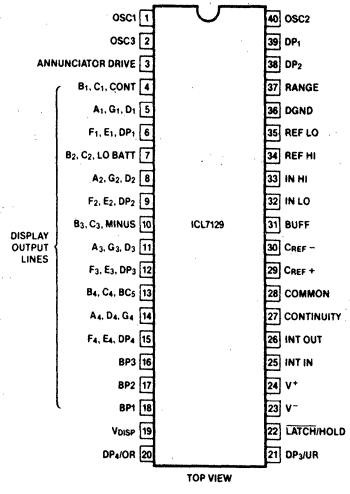


Figure 2: Pin Configuration (outline dwg PL)

Note: All typical values have been guaranteed by characterization and are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages (V^+ to V^-) 15V
Reference Voltage (REF HI or REF LO) ..... V^+ to V^-
Input Voltage (Note 1)
(IN HI or IN LO) ..... V^+ to V^-
V_{DISP} ..... DGND −0.3V to V^+
Digital Input Pins
1, 2, 19, 20, 21, 22, 27,
37, 38, 39, 40 ..... DGND to V^+

Power Dissipation (Note 2)
Plastic package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Note 1: Input voltages may exceed the supply voltages provided that input current is limited to ±400μA. Currents above this value may result in invalid display readings but will not destroy the device if limited to ±1mA.
Note 2: Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V^- to V^+ = 9V, V_{REF} = 1.00V. T_A = +25°C, f_{CLK} = 120kHz, unless otherwise noted.

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Zero Input Reading	V_{IN} = 0V 200mV Scale	−0000	0000	+0000	Counts
Zero Reading Drift	V_{IN} = 0V 0°C < T_A < +70°C		±0.5		μV/°C
Ratiometric Reading	V_{IN} = V_{REF} = 1000mV RANGE = 2V	9996	9999	10000	Counts
Range Change Accuracy	V_{IN} = 0.10000V on Low Range ÷ V_{IN} = 1.0000V on High Range	0.9999	1.0000	1.0001	Ratio
Rollover Error	$-V_{IN}$ = $+V_{IN}$ = 199mV		1.5	3.0	Counts
Linearity Error	200mV Scale		1.0		
Input Common-Mode Rejection Ratio	V_{CM} = 1.0V, V_{IN} = 0V 200mV Scale		110		dB
Input Common-Mode Voltage Range	V_{IN} = 0V 200mV Scale		(V^-) +1.5 (V^+) −1.0		V
Noise (p-p Value not Exceeding 95% of Time)	V_{IN} = 0V 200mV Scale		14		μV
Input Leakage Current	V_{IN} = 0V, Pin 32, 33		1	10	pA
Scale Factor Tempco	V_{IN} = 199mV 0°C < T_A < +70°C External V_{REF} = 0ppm/°C		2	7	ppm/°C
COMMON Voltage	V^+ to Pin 28	2.8	3.2	3.5	V
COMMON Sink Current	ΔCommon = +0.1V		0.6		mA
COMMON Source Current	ΔCommon = −0.1V		10		μA
DGND Voltage	V^+ to Pin 36 V^+ to V^- = 9V	4.5	5.3	5.8	V
DGND Sink Current	ΔDGND = +0.5V		1.2		mA
Supply Voltage Range	V^+ to V^- (Note 1)	6	9	12	V
Supply Current Excluding COMMON Current	V^+ to V^- = 9V		1.0	1.5	mA
Clock Frequency	(Note 1)		120	360	kHz
V_{DISP} Resistance	V_{DISP} to V^+		50		kΩ
Low Battery Flag Activation Voltage	V^+ to V^-	6.3	7.2	7.7	V
CONTINUITY Comparator Threshold Voltages	V_{OUT} Pin 27 = HI V_{OUT} Pin 27 = LO	100	200 200	400	mV
Pull-Down Current	Pins 37, 38, 39		2	10	μA
"Weak Output" Current Sink/Source	Pin 20, 21 Sink/Source		3/3		μA
	Pin 27 Sink/Source		3/9		
Pin 22 Source Current Pin 22 Sink Current			40 3		μA

NOTES: 1. Device functionality is guaranteed at the stated Min/Max limits. However, accuracy can degrade under these conditions.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7129

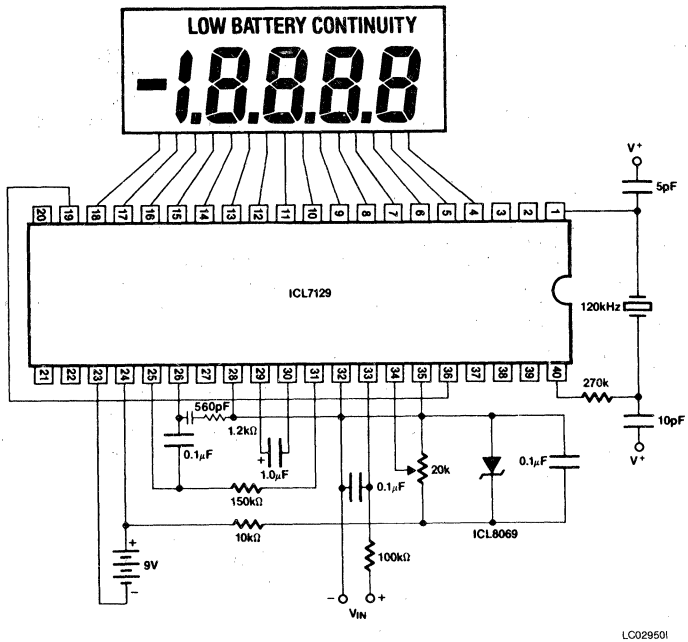


Figure 3: Typical Application

Table 1. Pin Descriptions

PIN	NAME	FUNCTION
1	OSC1	Input to first clock inverter.
2	OSC3	Output of second clock inverter.
3	ANNUNCIATOR DRIVE	Backplane squarewave output for driving annunciators.
4	B_1, C_1, CONT	Output to display segments.
5	A_1, G_1, D_1	Output to display segments.
6	F_1, E_1, DP_1	Output to display segments.
7	B_2, C_2, LO BATT	Output to display segments.
8	A_2, G_2, D_2	Output to display segments.
9	F_2, E_2, DP_2	Output to display segments.
10	B_3, C_3, MINUS	Output to display segments.
11	A_3, G_3, D_3	Output to display segments.
12	F_3, E_3, DP_3	Output to display segments.
13	B_4, C_4, BC_5	Output to display segments.
14	A_4, D_4, G_4	Output to display segments.
15	F_4, E_4, DP_4	Output to display segments.
16	BP3	Backplane #3 output to display.
17	BP2	Backplane #2 output to display.
18	BP1	Backplane #1 output to display.
19	V_{DISP}	Negative rail for display drivers.
20	DP_4/OR	INPUT: When HI, turns on most significant decimal point. OUTPUT: Pulled HI when result count exceeds ±19,999.
21	DP_3/UR	INPUT: Second most significant decimal point on when HI. OUTPUT: Pulled HI when result count is less than ±1,000.
22	$\overline{\text{LATCH}}$/HOLD	INPUT: When floating, A/D converter operates in the free-run mode. When pulled HI, the last displayed reading is held. When pulled LO, the result counter contents are shown incrementing during the de-integrate phase of cycle. OUTPUT: Negative going edge occurs when the data latches are updated. Can be used for converter status signal.
23	V^-	Negative power supply terminal.
24	V^+	Positive power supply terminal, and positive rail for display drivers.
25	INT IN	Input to integrator amplifier.
26	INT OUT	Output of integrator amplifier.
27	CONTINUITY	INPUT: When LO, continuity flag on the display is off. When HI, continuity flag is on. OUTPUT: HI when voltage between inputs is less than +200mV. LO when voltage between inputs is more than +200mV.

Note: All typical values have been guaranteed by characterization and are not tested.

Table 1. Pin Descriptions (Cont.)

PIN	NAME	FUNCTION
28	COMMON	Sets common-mode voltage of 3.2V below V^+ for DE, 10X, etc. Can be used as pre-regulator for external reference.
29	C_{REF}^+	Positive side of external reference capacitor.
30	C_{REF}^-	Negative side of external reference capacitor.
31	BUFFER	Output of buffer amplifier.
32	IN LO	Negative input voltage terminal.
33	IN HI	Positive input voltage terminal.
34	REF HI	Positive reference voltage input terminal.
35	REF LO	Negative reference voltage input terminal.
36	DGND	Ground reference for digital section.
37	RANGE	3μA pull-down for 200mV scale. Pulled HIGH externally for 2V scale.
38	DP_2	Internal 3μA pull-down. When HI, decimal point 2 will be on.
39	DP_1	Internal 3μA pull-down. When HI, decimal point 1 will be on.
40	OSC2	Output of first clock inverter. Input of second clock inverter.

DETAILED DESCRIPTION

Intersil's ICL7129 is a uniquely designed single-chip A/D converter. It features a new "successive integration" technique to achieve 10μV resolution on a 200mV full-scale range. To achieve this resolution a 10:1 improvement in noise performance over previous monolithic CMOS A/D converters was accomplished. Previous integrating converters used an external capacitor to store an offset correction voltage. This technique worked well but greatly increased the equivalent noise bandwidth of the converter. The ICL7129 removes this source of error (noise) by not using an auto-zero capacitor. Offsets are cancelled using digital techniques instead. Savings in external parts cost are realized as well as improved noise performance and elimination of a source of electromagnetic and electrostatic pick-up.

The overall functional diagram of the ICL7129 is shown in Figure 1. The heart of this A/D converter is the sequence counter/decoder which drives the control logic and keeps track of the many separate phases required for each conversion cycle. The sequence counter is constantly running and is a separate counter from the up/down results counter which is activated only when the integrator is de-integrating. At the end of a conversion the data remaining in the results counter is latched, decoded and multiplexed to the liquid crystal display.

The analog section block diagram shown in Figure 4 includes all of the analog switches used to configure the voltage sources and amplifiers in the different phases of the cycle. The input and reference switching schemes are very similar to those in other less accurate integrating A/D converters. There are 5 basic configurations used in the full conversion cycle. Figure 5 illustrates a typical waveform on the integrator output. INT, INT_1, and INT_2 all refer to the signal integrate phase where the input voltage is applied to the integrator amplifier via the buffer amplifier. In this phase, the integrator ramps over a fixed period of time in a direction opposite to the polarity of the input voltage.

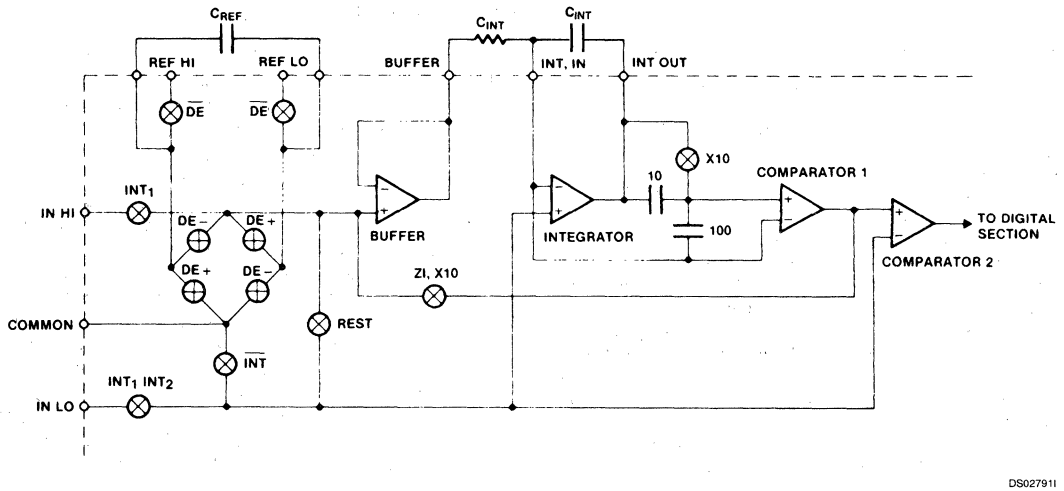


Figure 4: ICL7129 Analog Block Diagram

Note: All typical values have been guaranteed by characterization and are not tested.

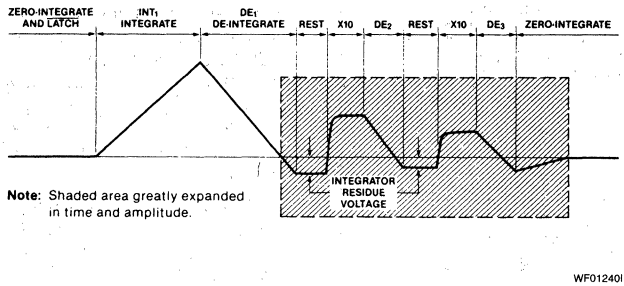


Figure 5: Integrator Waveform for Negative Input Voltage Showing Successive Integration Phases and Residue Voltage

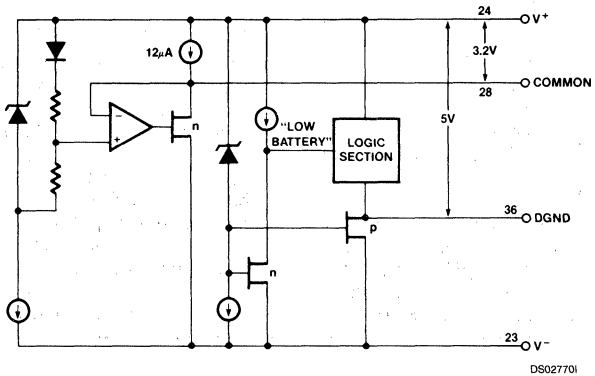


Figure 6: Biasing Structure for COMMON and DGND

DE_1, DE_2, and DE_3 are the de-integrate phases where the reference capacitor is switched in series with the buffer amplifier and the integrator ramps back down to the level it started from before integrating. However, since the de-integrate phase can terminate only at a clock pulse transition, there is always a small overshoot of the integrator past the starting point. The ICL7129 amplifies this overshoot by 10 and DE_2 begins. Similarly DE_2's overshoot is amplified by 10 and DE_3 begins. At the end of DE_3 the results counter holds a number with 5½ digits of resolution. This was obtained by feeding counts into the results counter at the 3½ digit level during DE_1, into the 4½ digit level during DE_2 and the 5½ digit level for DE_3. The effects of offset in the buffer, integrator, and comparator can now be cancelled by repeating this entire sequence with the inputs shorted and subtracting the results from the original reading. For this phase INT_2 switch is closed to give the same common-mode voltage as the measurement cycle. This assures excellent CMRR. At the end of the cycle the data in the up/down results counter is accurate to 0.005% of full-scale and is sent to the display driver for decoding and multiplexing.

COMMON, DGND, AND "LOW BATTERY"

The COMMON and DGND (Digital GrouND) outputs of the ICL7129 are generated from internal zener diodes (Figure 6). COMMON is included primarily to set the common-mode voltage for battery operation or for any system where the input signals float with respect to the power supplies. It also functions as a pre-regulator for an external precision reference voltage source. The voltage between DGND and V^+ is the supply voltage for the logic section of the ICL7129 including the display multiplexer and drivers. Both COMMON and DGND are capable of sinking current from external loads, but caution should be taken to ensure that these outputs are not overloaded. Figure 7 shows the connection of external logic circuitry to the ICL7129. This connection will work providing that the supply current requirements of the logic do not exceed the current sink capability of the DGND pin. If more supply current is required, the buffer in Figure 8 can be used to keep the loading on DGND to a minimum. COMMON can source approximately 12μA while DGND has no source capability.

The "LOW BATTERY" annunciator of the display is turned on when the voltage between V^+ and V^- drops below 7.2V typically. The exact point at which this occurs is determined by the 6.3V zener diode and the threshold voltage of the n-channel transistor connected to the V^- rail in Figure 6. As the supply voltage decreases, the n-channel transistor connected to the V-rail eventually turns off and

Note: All typical values have been guaranteed by characterization and are not tested.

the "LOW BATTERY" input to the logic section is pulled HIGH, turning on the "LOW BATTERY" annunciator.

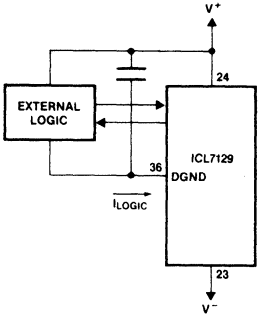


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Figure 7: DGND Sink Current

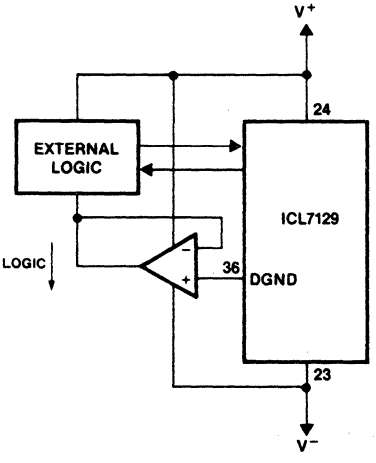

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Figure 8: Buffered DGND

I/O PORTS

Four pins of the ICL7129 can be used as either inputs or outputs. The specific pin numbers and functions are described in the Pin Description table (Table 1). If the output function of the pin is not desired in an application it can easily be overridden by connecting the pin to V^+ (HI) or DGND (LO). This connection will not damage the device because the output impedance of these pins is quite high. A simplified schematic of these input/output pins is shown in Figure 9. Since there is approximately 500kΩ in series with the output driver, the pin (when used as an output) can only drive very light loads such as 4000 series, 74CXX type CMOS logic, or other high input impedance devices. The output drive capability of these four pins is limited to 3μA, nominally, and the input switching threshold is typically DGND + 2V.

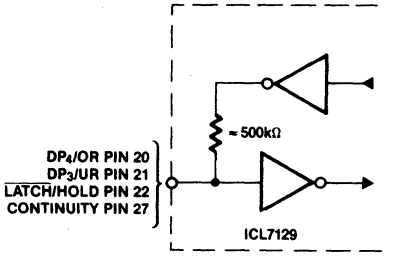

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Figure 9: "Weak Output"

LATCH/HOLD, OVERRANGE, AND UNDERRANGE TIMING

The LATCH/HOLD output (pin 22) will be pulled low during the last 100 clock cycles of each full conversion cycle. During this time the final data from the ICL7129 counter is latched and transferred to the display decoder and multiplexer. The conversion cycle and LATCH/HOLD timing are directly related to the clock frequency. A full conversion cycle takes 30,000 clock cycles which is equivalent to 60,000 oscillator cycles. OverRange (OR pin 20) an UnderRange (UR pin 21) outputs are latched on the falling edge of LATCH/HOLD and remain in that state until the end of the next conversion cycle. In addition, digits 1 through 4 are blanked during overrange. All three of these pins are "weak outputs" and can be overridden with external drivers or pull-up resistors to enable their input functions as described in the Pin Description table.

INSTANT CONTINUITY

A comparator with a built-in 200mV offset is connected directly between INPUT HI and INPUT LO of the ICL7129 (Figure 10). The CONTINUITY output (pin 27) will be pulled high whenever the voltage between the analog inputs is less than 200mV. This will also turn on the "CONTINUITY" annunciator on the display. The CONTINUITY output may be used to enable an external alarm or buzzer, thereby giving the ICL7129 an audible continuity checking capability. Since the CONTINUITY output is one of the four "weak outputs" of the ICL7129, the "continuity" annunciator on the display can be driven by an external source if desired. The continuity function can be overridden with a pull-down resistor connected between CONTINUITY pin and DGND (pin 36).

Note: All typical values have been guaranteed by characterization and are not tested.

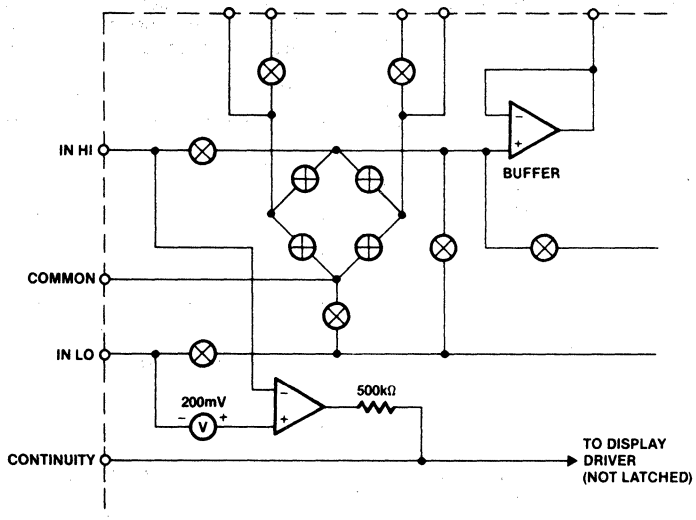

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Figure 10: "Instant Continuity" Comparator and Output Structure

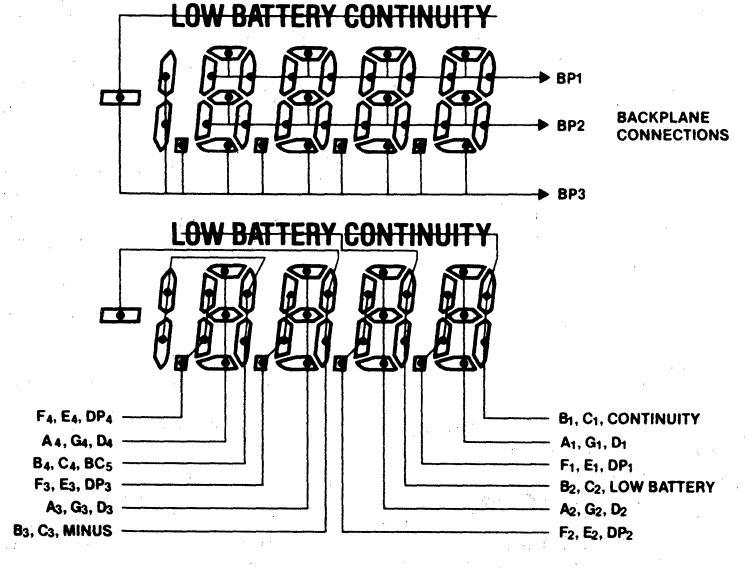

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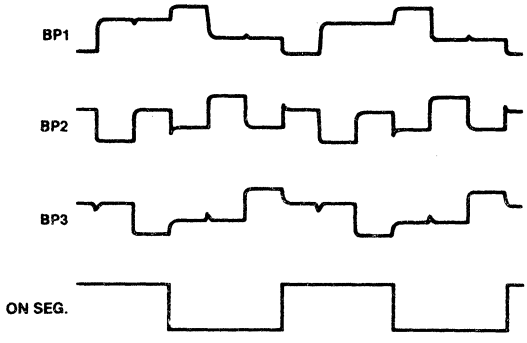
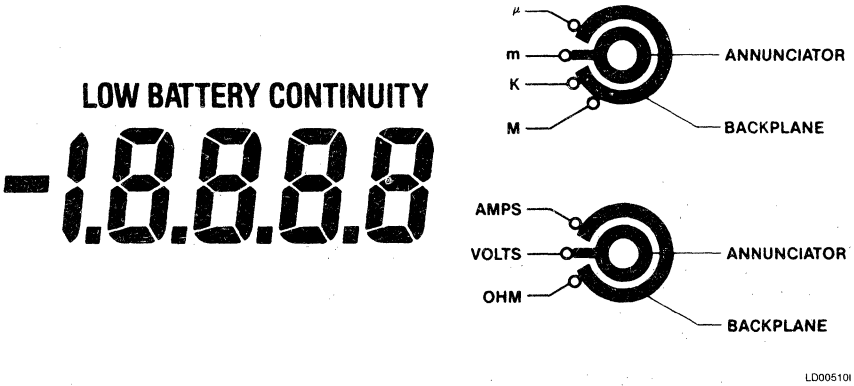
Figure 11: Triplexed Liquid Crystal Display Layout for ICL7129

Note: All typical values have been guaranteed by characterization and are not tested.



WF01250I

Figure 12: Typical Backplane and Annunciator Drive Waveforms



LD00510I

Figure 13: Multimeter Example Showing Use of Annunciator Drive Output

DISPLAY CONFIGURATION

The ICL7129 is designed to drive a triplexed liquid crystal display. This type of display has three backplanes and is driven in a multiplexed format similar to the ICM7231 display driver family. The specific display format is shown in Figure 11. Notice that the polarity sign, decimal points, "LOW BATTERY", and "CONTINUITY" annunciators are directly driven by the ICL7129. The individual segments and annunciators are addressed in a manner similar to row-column addressing. Each backplane (row) is connected to one-third of the total number of segments. BP1 has all F, A, and B segments of the four least significant digits. BP2 has all of the C, E, and G segments. BP3 has all D segments, decimal points, and annunciators. The segment lines (columns) are connected in groups of three bringing all segments of the display out on just 12 lines.

ANNUNCIATOR DRIVE

A special display driver output is provided on the ICL7129 which is intended to drive various kinds of annunciators on custom multiplexed liquid crystal displays. The ANNUNCIATOR DRIVE output (pin 3) is a squarewave signal running at the backplane frequency, approximately 100Hz. This signal swings from V_{DISP} to V^+ and is in sync with the three backplane outputs BP1, BP2, and BP3. Figure 12 shows these four outputs on the same time and voltage scales.

Any annunciator associated with any of the three backplanes can be turned on simply by connecting it to the ANNUNCIATOR DRIVE pin. To turn an annunciator off connect it to its backplane. An example of a display and annunciator drive scheme is shown in Figure 13.

Note: All typical values have been guaranteed by characterization and are not tested.

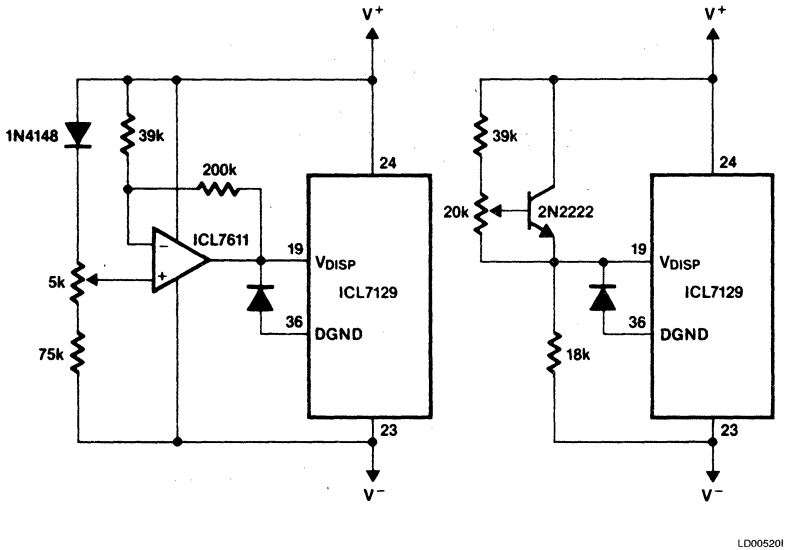


Figure 14: Two Methods for Temperature Compensating the Liquid Crystal Display

DISPLAY TEMPERATURE COMPENSATION

For most applications an adequate display can be obtained by connecting V_{DISP} (pin 19) to DGND (pin 36). In applications where a wide temperature range is encountered, the voltage drive levels for some triplexed liquid crystal displays may need to vary with temperature in order to maintain good display contrast and viewing angle. The amount of temperature compensation will depend upon the type of liquid crystal used. Display manufacturers can supply the temperature compensation requirements for their displays. Figure 14 shows two circuits that can be adjusted to give a temperature compensation of ≈+10mV/°C between V^+ and V_{DISP}. The diode between DGND and V_{DISP} should have a low turn-on voltage to assure that no forward current is injected into the chip if V_{DISP} is more negative than DGND.

COMPONENT SELECTION

There are only three passive components around the ICL7129 that need special consideration in selection. They are the reference capacitor, integrator resistor, and integrator capacitor. There is **no** auto-zero capacitor like that found in earlier integrating A/D converter designs.

The integrating resistor is selected to be high enough to assure good current linearity from the buffer amplifier and integrator and low enough that PC board leakage is not a problem. A value of 150kΩ should be optimum for most applications. The integrator capacitor is selected to give an optimum integrator swing at full-scale. A large integrator swing will reduce the effect of noise sources in the comparator but will affect rollover error if the swing gets too close to the positive rail (≈0.7V). This gives an optimum swing of ≈2.5V at full-scale. For a 150kΩ integrating resistor and 2 conversions per second the value is 0.10μF. For different conversion rates, the value will change in inverse proportion. A second requirement for good linearity is that the capacitor have low dielectric absorption. Polypropylene caps give good performance at a reasonable price. Finally the foil side of the cap should be connected to the integrator output to shield against pick-up.

The only requirement for the reference cap is that it be low leakage. In order to reduce the effects of stray capacitance, a 1.0μF value is recommended.

CLOCK OSCILLATOR

The ICL7129 achieves its digital range changing by integrating the input signal for 1000 clock pulses (2,000 oscillator cycles) on the 2V scale and 10,000 clock pulses on the 200mV scale. To achieve complete rejection of 60Hz on both scales, an oscillator frequency of 120kHz is required, giving two conversions per second.

In low resolution applications, where the converter uses only 3½ digits and 100μV resolution, an R-C type oscillator is adequate. In this application a C of 51pF is recommended and the resistor value selected from $f_{OSC} = 0.45/RC$. However, when the converter is used to its full potential (4½ digits and 10μV resolution) a crystal oscillator is recommended to prevent the noise from increasing as the input signal is increased due to frequency jitter of the R-C oscillator. Both R-C and crystal oscillator circuits are shown in Figure 15.

Note: All typical values have been guaranteed by characterization and are not tested.

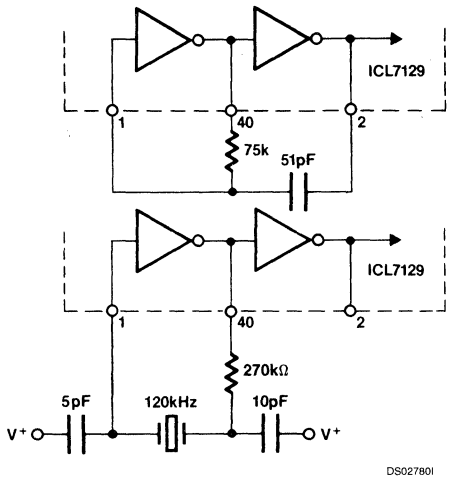


Figure 15: RC and Crystal Oscillator Circuits

POWERING THE ICL7129

The ICL7129 may be operated as a battery powered hand-held instrument or integrated into larger systems that have more sophisticated power supplies. Figures 16, 17, and 18 show various powering modes that may be used with the ICL7129.

The standard supply connection using a 9V battery is shown in Figure 3.

The power connection for systems with +5V and −5V supplies available is shown in Figure 16. Notice that measurements are with respect to ground. COMMON is not connected to INPUT LO but is used only as a pre-regulator for the external voltage reference.

It is important to notice that in Figure 16, digital ground of the ICL7129 (DGND pin 36) is **not** directly connected to power supply ground. DGND is set internally to approximately 5V less than the V^+ terminal and is not intended to be used as a power input pin. It may be used as the ground reference for external logic, as shown in Figure 7 and 8. In Figure 7, DGND is used as the negative supply rail for external logic provided that the supply current for the external logic does not cause excessive loading on DGND. The DGND output can be buffered as shown in Figure 8. Here, the logic supply current is shunted away from the ICL7129 keeping the load on DGND low. This treatment of the DGND output is necessary to insure compatibility when the external logic is used to interface directly with the logic inputs and outputs of the ICL7129.

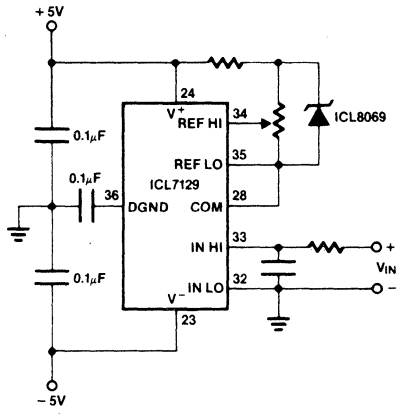


Figure 16: Powering the ICL7129 from +5V and −5V Power Supplies

When a battery voltage between 3.8V and 7V is desired for operation, a voltage doubling circuit should be used to bring the voltage on the ICL7129 up to a level within the power supply voltage range. This operating mode is shown in Figure 17.

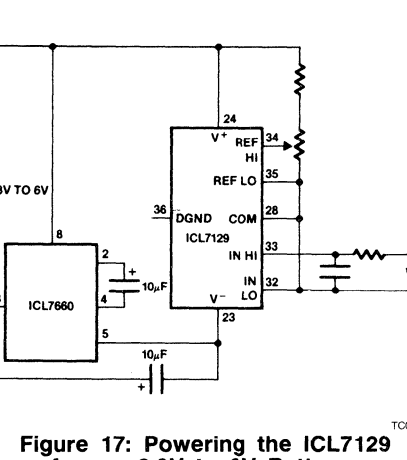


Figure 17: Powering the ICL7129 from a 3.8V to 6V Battery

Note: All typical values have been guaranteed by characterization and are not tested.

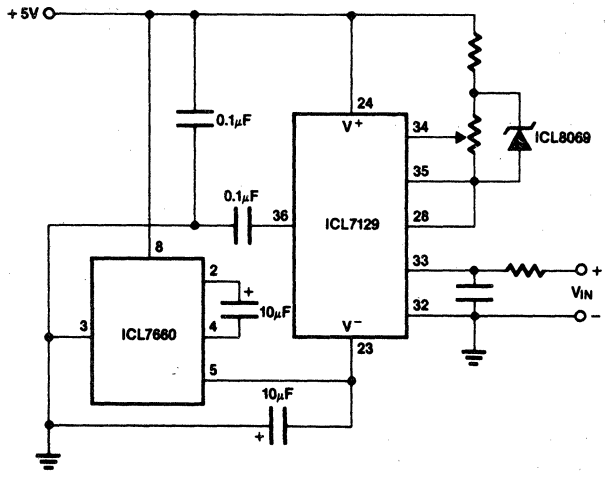
ICL7129

Again measurements are made with respect to COMMON since the entire system is floating. Voltage doubling is accomplished by using an ICL7660 CMOS voltage converter and two inexpensive electrolytic capacitors. The same principle applies in Figure 18 where the ICL7129 is being used in a system with only a single +5V power supply. Here measurements are made with respect to power supply ground.

A single polarity power supply can be used to power the ICL7129 in applications where battery operation is not appropriate or convenient **only** if the power supply is **isolated** from system ground. Measurements must be made with respect to COMMON or some other voltage within its input common-mode range.

VOLTAGE REFERENCES

The COMMON output of the ICL7129 has a temperature coefficient of ±80ppm/°C typically. This voltage is only suitable as a reference voltage for applications where ambient temperature variations are expected to be minimal. When the ICL7129 is used in most environments, other voltage references should be considered. The diagram in Figures 3 and 18 show the ICL8069 1.2V band-gap voltage source used as the reference for the ICL7129, and the COMMON output as its pre-regulator. The reference voltage for the ICL7129 is set to 1.000V for both 2V and 200mV full-scale operation.



DS01360I

Figure 18: Powering the ICL7129 from a Single Polarity Power Supply

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7134
14-Bit Multiplying μP-Compatible D/A Converter

GENERAL DESCRIPTION

The ICL7134 combines a four-quadrant multiplying DAC using thin film resistor and CMOS circuitry with an on-chip PROM-controlled correction circuit to achieve true 14-bit linearity without laser trimming.

Microprocessor bus interfacing is eased by standard memory WRite cycle timing and control signal use. Two input buffer registers are separately loaded with the 8 least significant bits (LS register) and the 6 most significant bits (MS register). Their contents are then transferred to the 14-bit DAC register, which controls the output switches. The DAC register can also be loaded directly from the data inputs, in which case the registers are transparent.

The ICL7134 is supplied in two versions. The ICL7134U is programmed for unipolar operation while the ICL7134B is programmed for bipolar applications. The V_{REF} input to the most significant bit of the DAC is separated from the reference input to the remainder of the ladder. For unipolar use, the two reference inputs are tied together, while for bipolar operation, the polarity of the MSB reference is reversed, giving the DAC a true 2's complement input transfer function. Two resistors which facilitate the reference inversion are included on the chip, so only an external op-amp is needed. The PROM is coded to correct for errors in these resistors as well as the inversion of the MSB.

FEATURES

- **14-Bit Linearity (0.003% FSR)**
- **No Gain Adjustment Necessary**
- **Microprocessor-Compatible With Double Buffered Inputs**
- **Bipolar Application Requires No Extra Adjustments or External Resistors**
- **Low Linearity and Gain Temperature Coefficients**
- **Low Power Dissipation**
- **Full Four-Quadrant Multiplication**

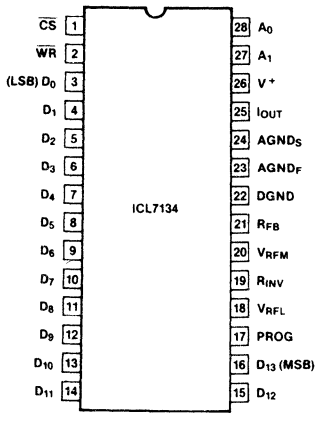


Figure 1: Pin Configuration (Outline dwg JI)

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ORDERING INFORMATION

NON-LINEARITY	TEMPERATURE RANGE		
	0°C to +70°C	-25°C to +85°C	-55°C to +125°C
Bipolar Versions			
0.01% (12-bit)	ICL7134BJCJI	ICL7134BJIJI	ICL7134BJMJI
0.006% (13-bit)	ICL7134BKCJI	ICL7134BKIJI	ICL7134BKMJI
0.003% (14-bit)	ICL7134BLCJI	ICL7134BLIJI	ICL7134BLMJI
Unipolar Versions			
0.01% (12-bit)	ICL7134UJCJI	ICL7134UJIJI	ICL7134UJMJI
0.006% (13-bit)	ICL7134UKCJI	ICL7134UKIJI	ICL7134UKMJI
0.003% (14-bit)	ICL7134ULCJI	ICL7134ULIJI	ICL7134ULMJI

PACKAGE: 28-pin CERDIP only

301664-002

Note: All typical values have been guaranteed by characterization and are not tested.

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ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V^+ to DGND) ..... −0.3V to 7.5V
V_{RFL}, V_{RFM}, R_{INV}, R_{FB} to DGND ..... ±15V
I_{OUT}, $AGND_F$, $AGND_S$ ..... −0.1V to V^+
Current in $AGND_S$, $AGND_F$ 25mA
An, Dn, $\overline{WR}$, $\overline{CS}$, PROG ..... −0.3V to V^+ +0.3V

Operating Temperature Range
ICL7134XXC ..... 0°C to +70°C
ICL7134XXI ..... −25°C to +85°C
ICL7134XXM ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Power Dissipation (Note 2) 500mW
Derate Linearly Above 70°C @ 10mW/°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Note 1: All voltages with respect to DGND.

Note 2: Assumes all leads soldered or welded to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

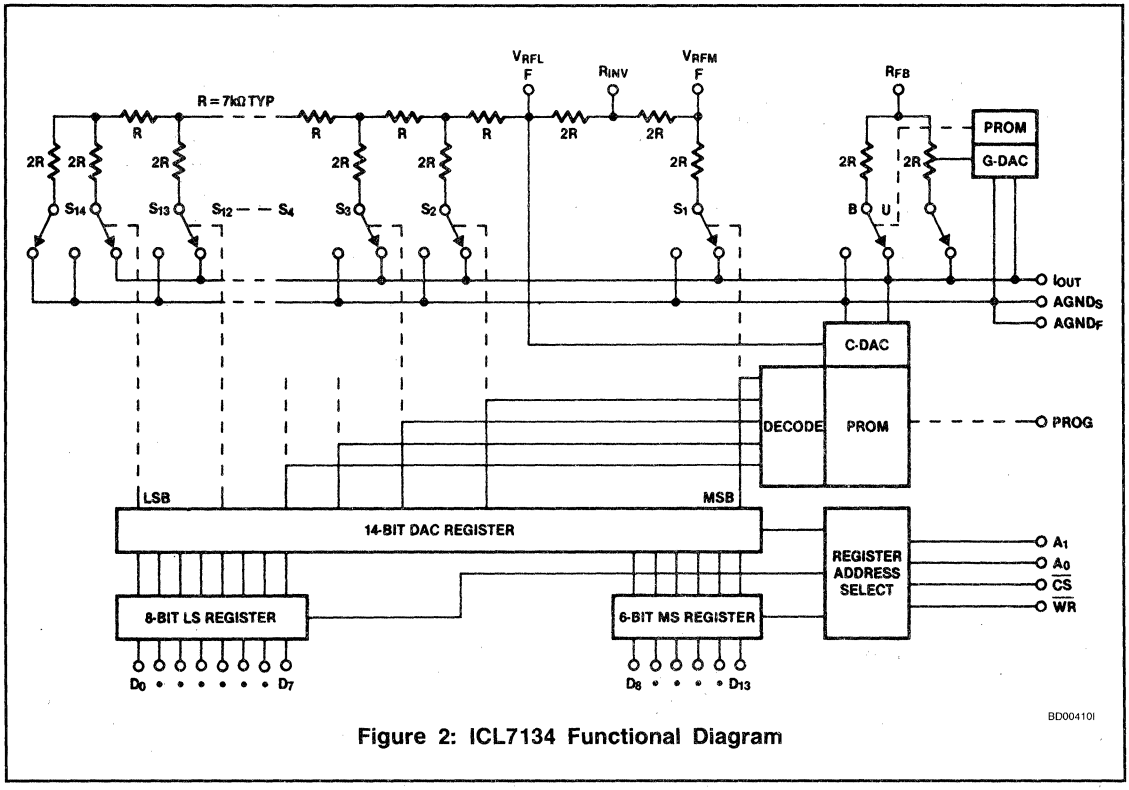

Figure 2: ICL7134 Functional Diagram

ELECTRICAL CHARACTERISTICS (V^+ = 5V, V_{REF} = 10V, T_A = 25°C unless otherwise specified.)

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
	Resolution			14			Bits
	Non-Linearity	J	Test Figure 4			0.012	% FSR
		K	(Notes 1 and 2)			0.006	% FSR
		L				0.003	% FSR
	Non-Linearity Temperature Coefficient (Note 3)		Operating Temperature Range		1	2	ppm/°C

Note: All typical values have been guaranteed by characterization and are not tested.

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
	Gain Error	J	Test Figure 4 (Notes 1 and 2)			0.024	% FSR
		K				0.012	% FSR
		L				0.006	% FSR
	Gain Error Temperature Coefficient (Note 3)				2	8	ppm/°C
	Monotonicity	J		12			Bits
		K		13			Bits
	(Note 3)	L		14			Bits
I_{OLK}	I_{OUT} Leakage Current		T_A = +25°C			10	nA
			Operating Temperature Range		50		
PSRR	Power Supply Rejection		T_A = +25°C, $\Delta V^+ = \pm 10\%$		10	100	ppm/V
			Operating Temperature Range			150	
	Output Current Settling Time				1		µs
	Feedthrough Error	ICL7134U	$V_{REF} = \pm 10V$, 2kHz Sinewave		250		µVp-p
		ICL7134B			500		
Z_{REF}	Reference Input Resistance		$V_{RFL} = V_{RFM}$ (Unipolar Mode)	4.0		10	kΩ
C_{OUT}	Output Capacitance		DAC Register = All 0's		160		pF
			DAC Register = All 1's		235		
	Output Noise		Equivalent Johnson Res.		7		kΩ
V_{INL}	Low State Input		Operating Temperature Range			0.8	V
V_{INH}	High State Input		Operating Temperature Range	2.4			V
I_{lin}	Logic Input Current		$0 \le V_{IN} \le V^+$			1.0	µA
C_{lin}	Logic Input Capacitance		(Note 3)		15		pF
V^+	Supply Voltage Range (Note 4)		Functional Operation	3.5		6.0	V
I^+	Supply Current		(Excluding Ladder)		1.0	2.5	mA
	Long Term Stability		1000 Hours, +125°C (Note 3)		10		ppm/month

NOTES: 1. Full-Scale Range (FSR) is 10V for unipolar mode, 20V (±10V) for bipolar mode.
2. Using internal feedback and reference inverting resistors.
3. Guaranteed by design, not production tested.
4. Full scale tested to 0.040% FSR.

AC CHARACTERISTICS (V^+ = 5V, see Timing Diagram)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{AWs}	Address-$\overline{WR}$ite Set-Up Time (Min)				100	ns
t_{AWh}	Address-$\overline{WR}$ite Hold Time (Min)	(Note 3)			0	
t_{CWs}	$\overline{Chip\ Select}$-$\overline{WR}$ite Set-Up Time (Min)	(Note 3)			0	
t_{CWh}	$\overline{Chip\ Select}$-$\overline{WR}$ite Hold Time (Min)	(Note 3)			0	
$t_{\overline{WR}}$	$\overline{WR}$ite Pulse Width Low (Min)				200	
t_{DWs}	Data-$\overline{WR}$ite Set-Up Time (Min)				200	
t_{DWh}	Data-$\overline{WR}$ite Hold Time (Min)	(Note 3)			0	

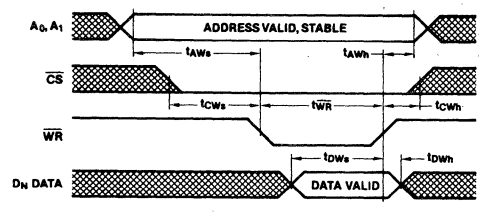

Figure 3: Timing Diagram

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a straight line function between endpoints. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to full-scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7134

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

Table 1: Pin Descriptions

PIN	SYMBOL	DESCRIPTION	
1	$\overline{CS}$	Chip Select (active low). Enables register write.	
2	$\overline{WR}$	WRite, (active low). Writes in register. Equivalent to $\overline{CS}$.	
3	D_0	Bit 0	Least significant
4	D_1	Bit 1	
5	D_2	Bit 2	
6	D_3	Bit 3	
7	D_4	Bit 4	
8	D_5	Bit 5	Input
9	D_6	Bit 6	Data
10	D_7	Bit 7	Bits
11	D_8	Bit 8	(High = True)
12	D_9	Bit 9	
13	D_{10}	Bit 10	
14	D_{11}	Bit 11	
15	D_{12}	Bit 12	
16	D_{13}	Bit 13	Most significant.

PIN	SYMBOL	DESCRIPTION	
17	PROG	Used for programming only. Tie to +5V for normal operation.	
18	V_{RFL}	V_{REF} for lower bits.	
19	R_{INV}	Summing node for reference inverting amplifier.	
20	V_{RFM}	V_{REF} for MSB only (bipolar).	
21	R_{FB}	Feedback resistor for voltage output applications.	
22	DGND	Digital GrouND return.	
23	$AGND_F$	Analog GrouND force lines. Use to carry current from internal Analog GrouND connections. Tied internally to $AGND_S$.	
24	$AGND_S$	Analog GrouND sense line. Reference point for external circuitry. Pin should carry minimal current; tied internally to $AGND_F$.	
25	I_{OUT}	Current output pin.	
26	V^+	Positive voltage.	
27	A_1	Address 1	Control register lines
28	A_0	Address 0	

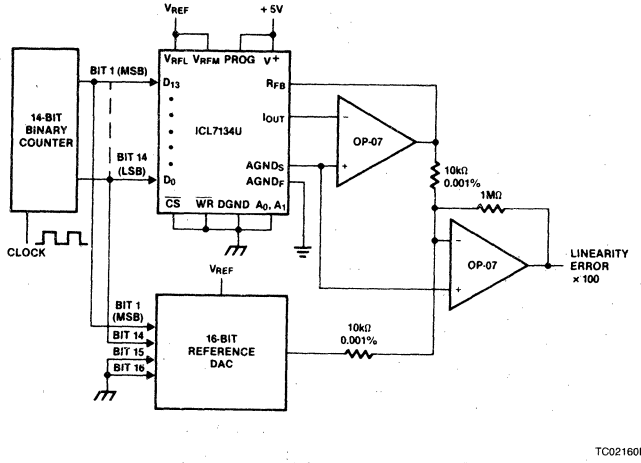

Figure 4: Non-Linearity Test Circuit

Note: All typical values have been guaranteed by characterization and are not tested.

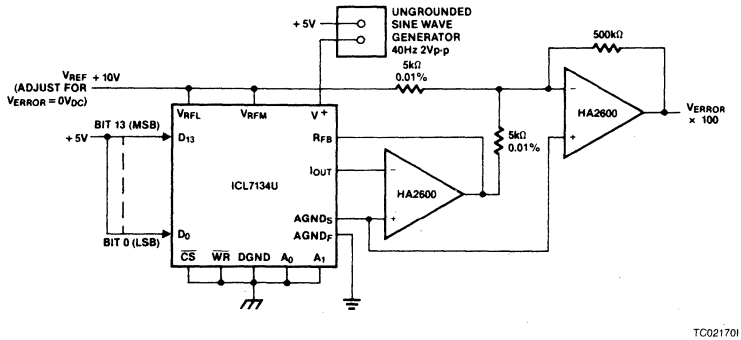

Figure 5: Power Supply Rejection Test Circuit

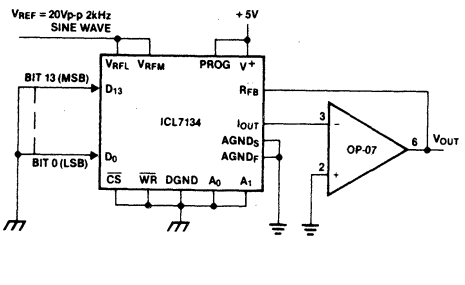

Figure 6: Feedthrough Error Test Circuit

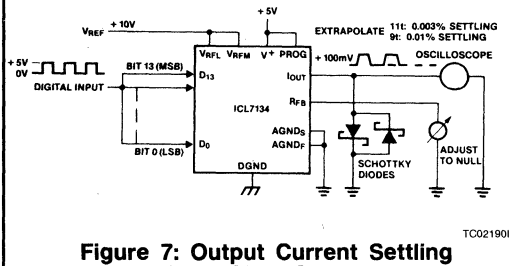

Figure 7: Output Current Settling Time Test Circuit

DETAILED DESCRIPTION

The ICL7134 consists of a 14-bit primary DAC, two PROM controlled correction DACs, input buffer registers, and microprocessor interface logic (Figure 2). The 14-bit primary DAC is an R-2R thin film resistor ladder with N-channel MOS SPDT current steering switches. Precise balancing of the switch resistances, and all other resistances in the ladder, results in excellent temperature stability.

True 14-bit linearity is achieved by programming a floating polysilicon gate PROM array which controls two correction DAC circuits. A 6-bit gain correction DAC, or G-DAC, diverts up to 2% of the feedback resistor's current to Analog GounND and reduces the gain error to less than 1 LSB, or 0.006%. The 5 most significant outputs of the DAC register address a 31-word PROM array that controls a 12-bit linearity correction DAC, or C-DAC. For every combination of the primary DAC's 5 most significant bits, a different C-DAC code is selected. This allows correction of superposition errors, caused by bit interaction on the primary resistor ladder's current output bus and by voltage non-linearity in the feedback resistor. Superposition errors cannot be corrected by any method which corrects individual bits only, such as laser trimming. Since the PROM programming occurs in packaged form, it corrects for resistor shifts caused by the thermal stresses of packaging. These packaging shifts limit the accuracy that can be achieved using wafer level correction methods such as laser trimming, which has also been found to degrade the time stability of thin film resistors at the 14-bit level.

Analog Section

The ICL7134 inherently provides both unipolar and bipolar operation. The bipolar application circuit (Figure 8) requires one additional op-amp but no external resistors. The two on-chip resistors, R_{INV1} and R_{INV2}, together with the op-amp, form a voltage inverter which drives the MSB reference terminal, V_{RFM}, to $-V_{REF}$, where V_{REF} is the voltage applied at the less significant bits' reference terminal, V_{RFL}. This reverses the weight of the MSB, and gives the DAC a 2's complement transfer function. The op-amp and reference connection to V_{RFM} and V_{RFL} can be reversed, without affecting linearity, but a small gain error will be introduced. For unipolar operation the V_{RFM} and V_{RFL} terminals are both tied to V_{REF}, and the R_{INV} pin is left unconnected.

Since the PROM correction codes required are different for bipolar and unipolar operation, the ICL7134 is available in two different versions; the ICL7134U, which is corrected for unipolar operation, and the ICL7134B, which is programmed for bipolar application. The feedback resistance is also different in the two versions, and is switched under PROM control from 'R' in the unipolar device to '2R' in the

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Note: All typical values have been guaranteed by characterization and are not tested.

bipolar part. These feedback resistors have a dummy (always ON) switch in series to compensate for the effect of the ladder switches. This greatly improves the gain temperature coefficient and the power supply rejection of the device.

Digital Section

Two levels of input buffer registers allow loading of data from an 8-bit or 16-bit data bus. The A_0 and A_1 pins select one of four operations: 1) load the LS-buffer register with the data at inputs D_0 to D_7; 2) load the MS-buffer register with the data at inputs D_8 to D_{13}; 3) load the DAC register with the contents of the MS and LS-buffer registers and 4) load the DAC register directly from the data input pins (see Table 2). The $\overline{CS}$ and $\overline{WR}$ pins must be low to allow data transfers to occur. When direct loading is selected ($\overline{CS}$, $\overline{WR}$, A_0 and A_1 low) the registers are transparent, and the data input pins control the DAC output directly. The other modes of operation allow double buffered loading of the DAC from an 8-bit bus.

These input data pins are also used to program the PROM under control of the PROG pin. This is done in manufacturing, and for normal read-only use the PROG pin should be tied to V^+ (+5V).

Table 2: Data Loading Controls

CONTROL I/P				ICL7134 OPERATION
A_0	A_1	$\overline{CS}$	$\overline{WR}$	
X	X	X	1	No operation, device not selected.
X	X	1	X	
0	0	0	0	Load all registers from data bus.
0	1	0	0	Load LS register from data bus.
1	0	0	0	Load MS register from data bus.
1	1	0	0	Load DAC register from MS and LS register.

Note: Data is latched on LO-HI transition of either $\overline{WR}$ or $\overline{CS}$.

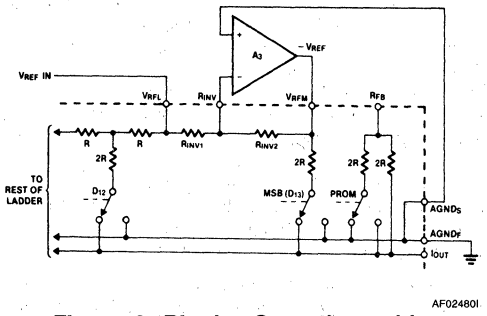


Figure 8: Bipolar Operation, with Inverted V_{REF} to MSB

APPLICATIONS

General Recommendations

GROUND LOOPS

Careful consideration must be given to ground loops in any 14-bit accuracy system. The current into the analog ground point inside the chip varies significantly with the input code value, and the inevitable resistances between this point and any external connection point can lead to significant voltage drop errors. For this reason, two separate leads are brought out from this point on the IC, the $AGND_F$ and $AGND_S$ pins. The varying current should be absorbed through the $AGND_F$ pin, and the $AGND_S$ pin will then accurately reflect the voltage on the internal current summing point, as shown in Figure 9. Thus output signals should be referenced to the sense pin $AGND_S$, as shown in the various application circuits.

OPERATIONAL AMPLIFIER SELECTION

To maintain static accuracy, the I_{OUT} potential must be exactly equal to the $AGND_S$ potential. Thus output amplifier selection is critical, in particular low input bias current (less than 2nA), low offset voltage drift (depending on the temperature range) and low offset voltage (less than 25μV) are advisable if the highest accuracy is needed. Maintaining a low input offset over a 0V to 10V range also requires that the output amplifier has a high open loop gain (A_{VOL} > 400k for effective input offset less than 25μV).

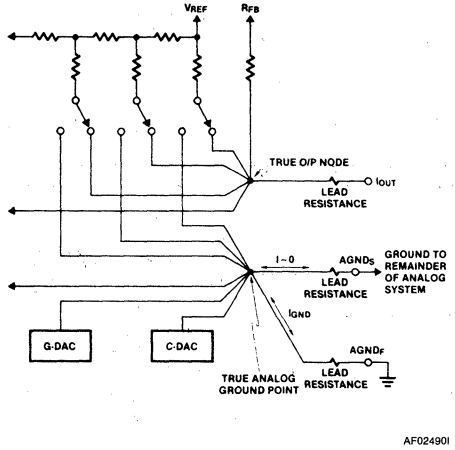


Figure 9: Eliminating Ground Loops

The reference inverting amplifier used in the bipolar mode circuit must also be selected carefully. If 14-bit accuracy is desired without adjustment, low input bias current (less than 1nA), low offset voltage (less than 50μV), and high gain (greater than 400k) are recommended. If a fixed reference voltage is used, the gain requirement can be relaxed. For highest accuracy (better than 13 bits), an additional op-amp may be needed to correct for IR drop on the Analog GrouND line (op-amp A_2 in Figure 11). This op-amp should be selected for low bias current (less than 2nA) and low offset voltage (less than 50μV).

Note: All typical values have been guaranteed by characterization and are not tested.

The op-amp requirements can be readily met by use of an ICL7650 chopper stabilized device. For faster settling time, an HA26XX can be used with an ICL7650 providing automatic offset null (see A053 for details).

The output amplifier's non-inverting input should be tied directly to $AGND_S$. A bias current compensation resistor is of limited use since the output impedance at the summing node depends on the code being converted in an unpredictable way. If gain adjustment is required, low tempco (approximately 50ppm/°C) resistors or trim-pots should be selected.

POWER SUPPLIES

The V^+ (pin 25) power supply should have a low noise level, and no transients exceeding 7 volts. Note that the absolute maximum digital input voltage allowed is V^+, which therefore must be applied before digital inputs are allowed to go high. Unused digital inputs must be connected to GND or V^+ for proper operation.

Unipolar Binary Operation (ICL7134U)

The circuit configuration for unipolar mode operation (ICL7134U) is shown in Figure 10. With positive and negative V_{REF} values the circuit is capable of two-quadrant multiplication. The "digital input code/analog output value" table for unipolar mode is given in Table 3. The Schottky diode (HP5082-2811 or equivalent) protects I_{OUT} from negative excursions which could damage the device, and is only necessary with certain high speed amplifiers. For applications where the output reference ground point is established somewhere other than at the DAC, the circuit of Figure 10 can be used. Here, op-amp A_2. removes the slight error due to IR voltage drop between the internal Analog GrouND node and the external ground connection. For 13-bit or lower accuracy, omit A_2 and connect $AGND_F$ and $AGND_S$ directly to ground through as low a resistance as possible.

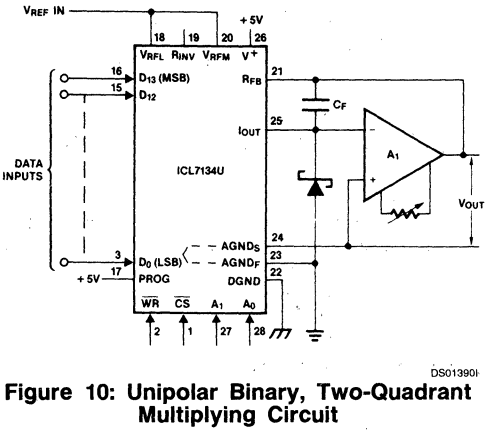


Figure 10: Unipolar Binary, Two-Quadrant Multiplying Circuit

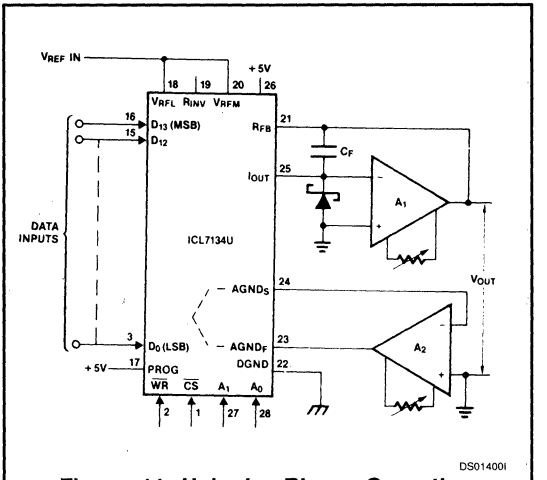


Figure 11: Unipolar Binary Operation with Forced Ground

Table 3: Code Table — Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1-1/2^{14})$
1 0 0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}(1/2+1/2^{14})$
1 0 0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}/2$
0 1 1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1/2-1/2^{14})$
0 0 0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}(1/2^{14})$
0 0 0 0 0 0 0 0 0 0 0 0 0 0	0

ZERO OFFSET ADJUSTMENT

1. Connect all data inputs and $\overline{WR}$, $\overline{CS}$, A_0 and A_1 to DGND.
2. Adjust offset zero-adjust trim-pot of the operational amplifier A_2, if used, for a maximum of 0V ±50μV at $AGND_S$.
3. Adjust the offset zero-adjust trim-pot of the output op-amp, A_1, for a maximum of 0V ±50μV at V_{OUT}.

GAIN ADJUSTMENT (OPTIONAL)

1. Connect all data inputs to V^+, connect $\overline{WR}$, $\overline{CS}$, A_0 and A_1 to DGND.
2. Monitor V_{OUT} for a $-V_{REF}\ (1-1/2^{14})$ reading.
3. To decrease V_{OUT}, connect a series resistor of 100Ω or less between the reference voltage and the V_{RFM} and V_{RFL} terminals (pins 20 and 18).
4. To increase V_{OUT}, connect a series resistor of 100Ω or less between A_1 output and the R_{FB} terminal (pin 21).

Note: All typical values have been guaranteed by characterization and are not tested.

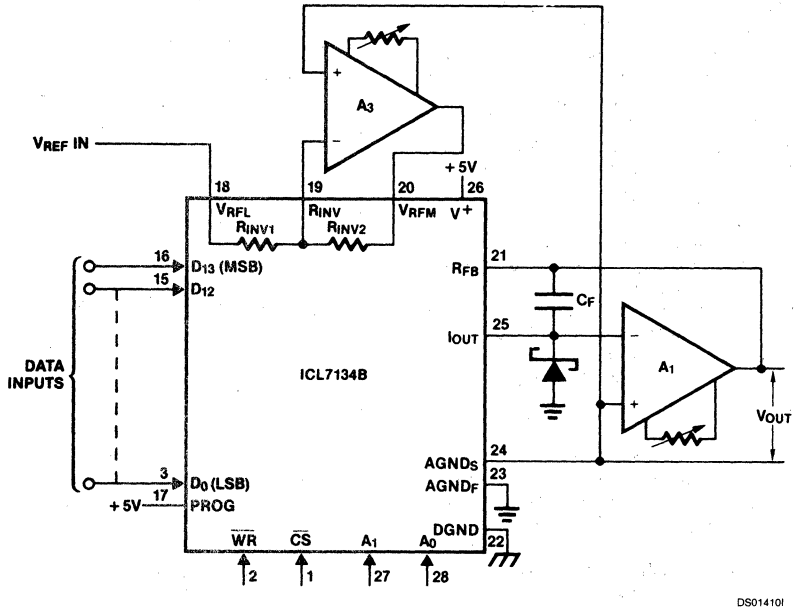


Figure 12: Bipolar (2's Complement), Four-Quadrant Multiplying Circuit

Bipolar (2's Complement) Operation (ICL7134B)

The circuit configuration for bipolar mode operation (ICL7134B) is shown in Figure 12. Using 2's complement digital input codes and positive and negative reference voltage values, four-quadrant multiplication is obtained. The "digital input code/analog output value" table for bipolar mode is given in Table 4. Amplifier A_3, together with internal resistors R_{INV1} and R_{INV2}, forms a simple voltage inverter circuit. The MSB ladder leg sees a reference input of approximately $-V_{REF}$, so the MSB's weight is reversed from the polarity of the other bits. In addition, the ICL7134B's feedback resistance is switched to 2R under PROM control, so that the bipolar output range is $+V_{REF}$ to $-V_{REF}$ $(1 - 1/2^{13})$. Again, the grounding arrangement of Figure 11 can be used, if necessary.

Table 4: Code Table — Bipolar (2's Complement) Operation

DIGITAL INPUT	ANALOG OUTPUT
0 1 1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1 - 1/2^{13})$
0 0 0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}(1/2^{13})$
0 0 0 0 0 0 0 0 0 0 0 0 0 0	0
1 1 1 1 1 1 1 1 1 1 1 1 1 1	$V_{REF}(1/2^{13})$
1 0 0 0 0 0 0 0 0 0 0 0 0 1	$V_{REF}(1 - 1/2^{13})$
1 0 0 0 0 0 0 0 0 0 0 0 0 0	V_{REF}

OFFSET ADJUSTMENT

1. Connect all data inputs and $\overline{WR}$, $\overline{CS}$, A_0 and A_1 to DGND.
2. Adjust the offset zero-adjust trim-pot of the operational amplifier A_2, if used, for a maximum of 0V $\pm 50\mu V$ at $AGND_S$.
3. Set data to 00000 . . . . 00. Adjust the offset zero-adjust trim-pot of the output op-amp A_1, for a maximum of 0V $\pm 50\mu V$ at V_{OUT}.
4. Connect D_{13} (MSB) data input to V^+.
5. Adjust the offset zero-adjust trim-pot of op-amp A_3 for a maximum of 0V $\pm 50\mu V$ at the R_{INV} terminal (pin 19).

GAIN ADJUSTMENT (OPTIONAL)

1. Connect $\overline{WR}$, $\overline{CS}$, A_0 and A_1 to DGND.
2. Connect D_0, D_1 . . . D_{12} to V^+, D_{13} (MSB) to DGND.
3. Monitor V_{OUT} for a $-V_{REF}$ $(1 - 1/2^{13})$ reading.
4. To increase V_{OUT}, connect a series resistor of 200Ω or less between the A_1 output and the R_{FB} terminal (pin 21).
5. To decrease V_{OUT}, connect a series resistor of 100Ω or less between the reference voltage and the V_{RFL} terminal (pin 18).

Processor Interfacing

The ease of interfacing to a processor can be seen from Figure 14, which shows the ICL7134 connected to an 8035 or any other processor such as an 8049. The data bus feeds into both register inputs; three port lines, in combination with the $\overline{WR}$ line, control the byte-wide loading into these registers and then the DAC register. A complete DAC set-up requires 4 write instructions to the port, to set up the address and $\overline{CS}$ lines, and 3 external data transfers, one a dummy for the final transfer to the DAC register.

Note: All typical values have been guaranteed by characterization and are not tested.

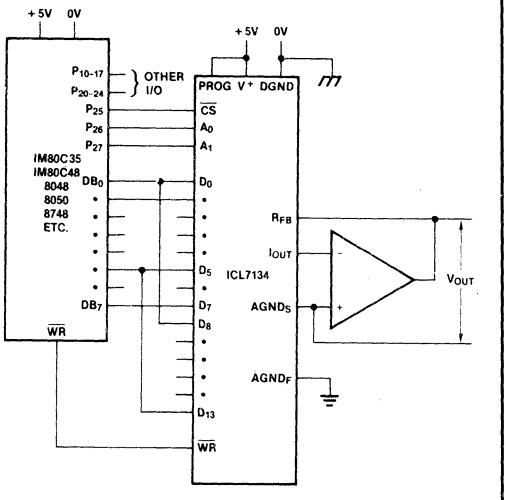


Figure 13: ICL7134 Interface to 8048 System

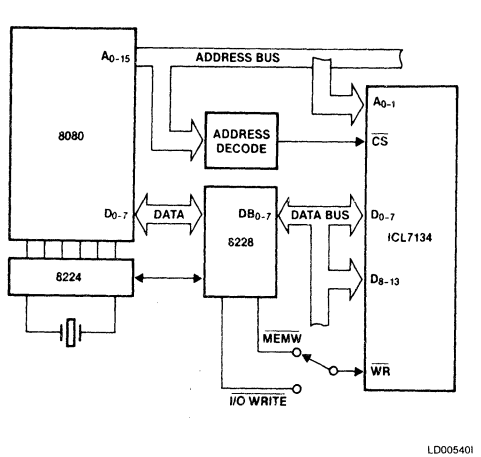


Figure 14: Interface to 8080 System

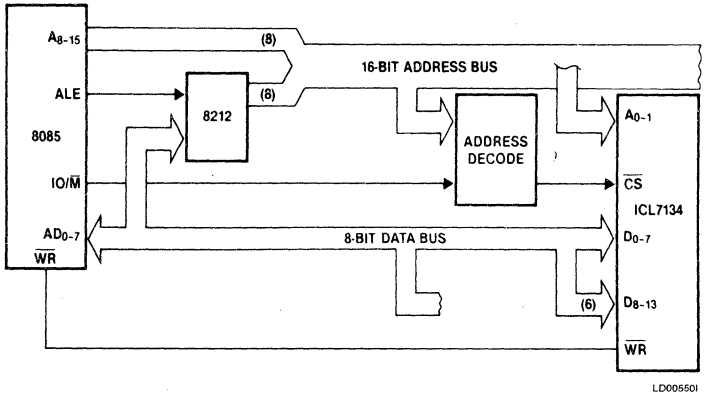


Figure 15: 8085 System Interface

A similar arrangement can be used with an 8080A, 8228, and 8224 chip set. Figure 14 shows the circuit, which can be arranged as a memory-mapped interface (using $\overline{\text{MEMW}}$) or as an I/O-mapped interface (using I/O $\overline{\text{WRITE}}$). See A020 and R005 for discussions of the relative merits of memory-mapped versus I/O-mapped interfacing, as well as some other ideas on interfacing with 8080 processors. The 8085 processor has a very similar interface, except that the control lines available are slightly different, as shown in Figure 15. The decoding of the IO/M line, which controls memory-mapped or I/O-mapped operation, is arbitrary, and can be omitted if not necessary. Neither the MC680X nor R650X processor families offer specific I/O operations. Figure 16 shows a suitable interface to either of these systems, using a direct connection. Several other decoding options can be used, depending on the other control signals generated in the system. Note that the R650X family does not require VMA to be decoded with the address lines.

Note: All typical values have been guaranteed by characterization and are not tested.

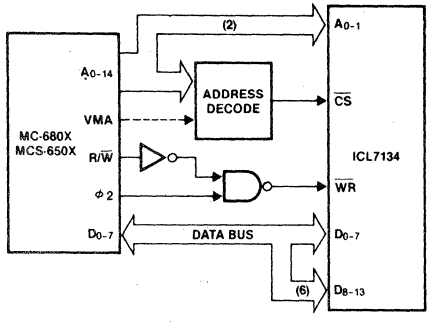


Figure 16: R650X and MC680X Families' Interface to ICL7134

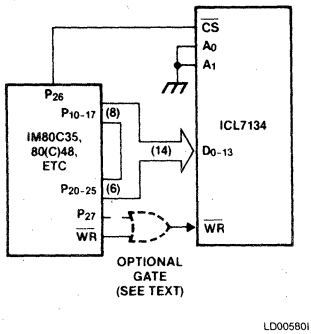


Figure 17: Avoiding Digital Feedthrough in an 8048 to ICL7134 Interface

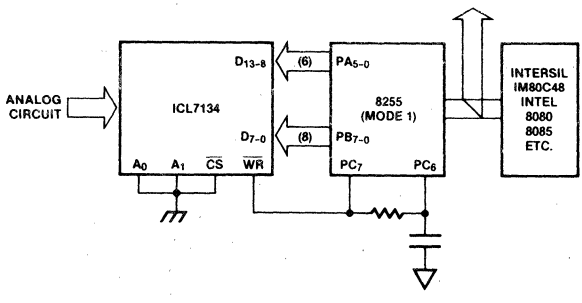


Figure 18: ICL7134 to 8048/80/85 Interface with Low Feedthrough

Digital Feedthrough

All of the direct interfaces shown above can suffer from a capacitive coupling problem. The 14 data pins, and 4 control pins, all tied to active lines on a microprocessor bus, and in close proximity to the sensitive DAC circuitry, can couple pseudo-random spikes into the analog output. Careful board layout and shielding can minimize the problems (see **PC layout**), and clearly wire-wrap type sockets should never be used. Nevertheless, the inherent capacitance of the package alone can lead to unacceptable digital feedthrough in many cases. The only solution is to keep the digital input lines as inactive as possible. One easy way to do this is to use the peripheral interface circuitry available with all the systems previously discussed. These generally allow only 8 bits to be updated at any one time, but a little ingenuity will avoid difficulties with DAC steps that would result from partial updates. The problem can be solved for the 8048 family by tying the 14 port lines to the data input lines, with CS, A_0 and A_1 held low, and using only the $\overline{WR}$ line to enter the data into the DAC (as shown in Figure 17). $\overline{WR}$ is well separated from the analog lines on the ICL7134, and is usually not a very active line in 8048 systems. Additional "protection" can be achieved by gating the processor $\overline{WR}$ line with another port line. The heavy use of port lines can be alleviated by use of the IM82C43 port expander. The same type of technique can be employed in the 8080/85 systems by using an 8255 PIA (peripheral Interface adapter) (Figure 18) and in the MC680X and R650X systems by using an MC6820 (R6520) PIA.

Note: All typical values have been guaranteed by characterization and are not tested.

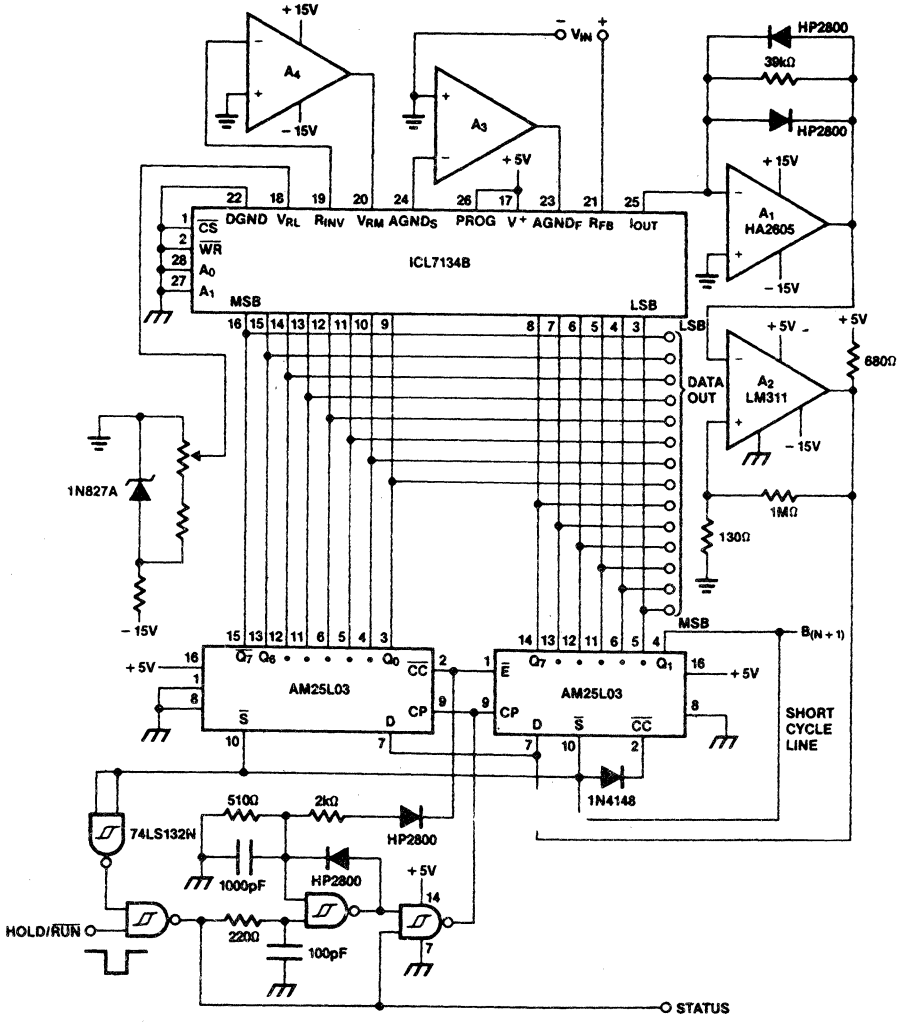
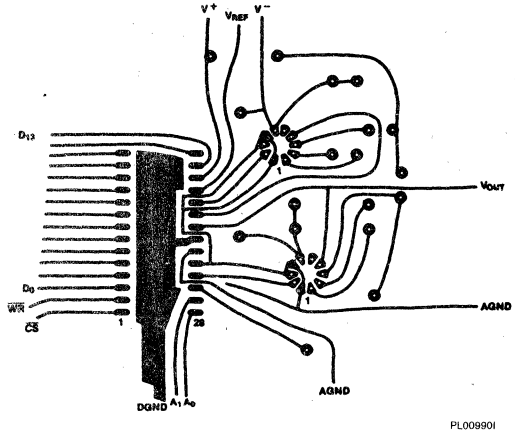


Figure 19: Successive Approximation A/D Converter

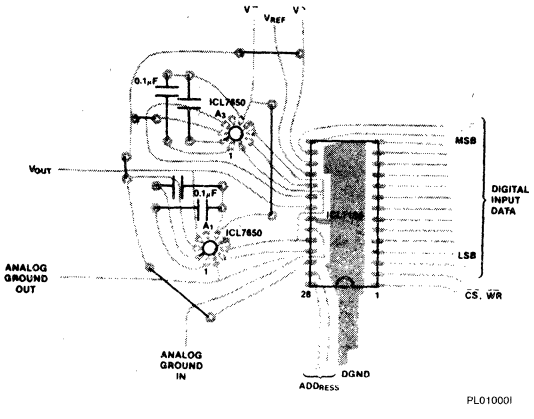
Successive Approximation A/D Converters

Figure 19 shows an ICL7134B-based circuit for a bipolar input high speed A/D converter, using two AM25L03s to form a 14-bit successive approximation register. The comparator is a two-stage circuit with an HA2605 front-end amplifier, used to reduce settling time problems at the summing node (see A020). Careful offset-nulling of this amplifier is needed, and if wide temperature range operation is desired, an auto-null circuit using an ICL7650 is probably advisable (see A053). The clock, using two Schmitt trigger TTL gates, runs at a slower rate for the first 8 bits, where settling-time is most critical, than for the last 6 bits. The short-cycle line is shown tied to the 15th bit; if fewer bits are required, it can be moved up accordingly. The circuit will free-run if the HOLD/$\overline{\text{RUN}}$ input is held low, but will stop after completing a conversion if the pin is high at that time. A low-going pulse will restart it. The STATUS output indicates when the device is operating, and the falling edge indicates the availability of new data. A unipolar version may be constructed by tying the MSB (D_{13}) on an ICL7134U to pin 14 on the first AM25L03, deleting the reference inversion amplifier A_4, and tying V_{RFM} to V_{RFL}.

Note: All typical values have been guaranteed by characterization and are not tested.



(a) Printed Circuit Side of Card (Single Sided Board)



(b) Top Side with Component Placement

Figure 20: Printed Circuit Board Layout (Bipolar Circuit, see Figure 12)

PC BOARD LAYOUT

Great care should be taken in the board layout to minimize ground loop and similar "hidden resistor" problems, as well as to minimize digital signal feedthrough. A suitable layout for the immediate vicinity of the ICL7134 is shown in Figure 20, and may be used as a guide.

APPLICATION NOTES

Some applications bulletins that may be found useful are listed here:

A016 "Selecting A/D Converters," by Dave Fullagar.
A017 "The Integrating A/D Converter," by Lee Evans.
A018 "Do's and Dont's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.
A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Sliger.
A021 "Power A/D Converters Using the ICH8510," by Dick Wilenken.
A030 "The ICL7104 — A Binary Output A/D Converter for Microprocessors," by Peter Bradshaw.
R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976.

Most of these are available in the Intersil Data Acquisition Handbook, together with other material.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7135
4½-Digit BCD Output A/D Converter

GENERAL DESCRIPTION

The Intersil ICL7135 precision A/D converter, with its multiplexed BCD output and digit drivers, combines dual-slope conversion reliability with ±1 in 20,000 count accuracy and is ideally suited for the visual display DVM/DPM market. The 2.0000V full scale capability, auto-zero and auto-polarity are combined with true ratiometric operation, almost ideal differential linearity and true differential input. All necessary active devices are contained on a single CMOS I.C., with the exception of display drivers, reference, and a clock.

The intersil ICL7135 brings together an unprecedented combination of high accuracy, versatility, and true economy. It features auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10 pA max., and rollover error of less than one count. The versatility of multiplexed BCD outputs is increased by the addition of several pins which allow it to operate in more sophisticated systems. These include $\overline{\text{STROBE}}$, OVERRANGE, UNDER-RANGE, RUN/$\overline{\text{HOLD}}$ and BUSY lines, making it possible to interface the circuit to a microprocessor or UART.

FEATURES

- **Accuracy Guaranteed to ±1 Count Over Entire ±20,000 Counts (2.0000 Volts Full Scale)**
- **Guaranteed Zero Reading for 0 Volts Input**
- **1pA Typical Input Current**
- **True Differential Input**
- **True Polarity at Zero Count for Precise Null Detection**
- **Single Reference Voltage Required**
- **Over-Range and Under-Range Signals Available for Auto-Range Capability**
- **All Outputs TTL Compatible**
- **Blinking Outputs Gives Visual Indication of Over-range**
- **Six Auxiliary Inputs/Outputs Are Available for Interfacing to UARTs, Microprocessors or Other Circuitry**
- **Multiplexed BCD Outputs**

ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ICL7135CJI	0°C to +70°C	28-Pin CERDIP
ICL7135CPI	0°C to +70°C	28-Pin Plastic DIP
ICL7135EV/KIT	Evaluation Kit (Pc Board, active, passive components)	

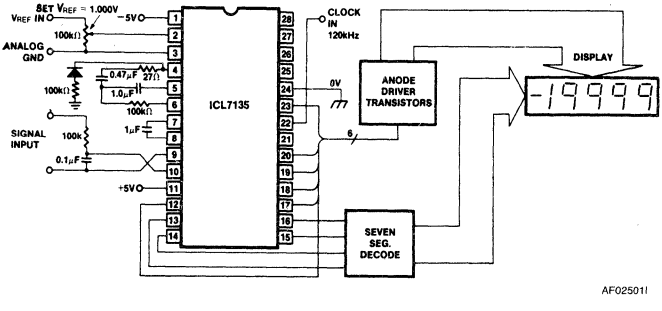


Figure 1: ICL7135 Connection Diagram

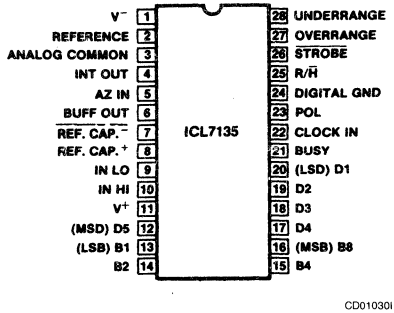


Figure 2: Pin Configuration (Outline dwgs JI, PI)

6

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7135

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V^+ ..... +6V
V^- ..... −9V
Analog Input Voltage (either input) (Note 1) .. V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... Gnd to V+

Power Dissipation (Note 2)
Ceramic Package 1000mW
Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to +100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 1)

(V^+ = +5V, V^- = −5V, T_A = 25°C, Clock Frequency Set for 3 Reading/Sec)

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG (Note 1) (Note 2)						
	Zero Input Reading	V_{IN} = 0.0V Full Scale = 2.000V	−0.0000	±0.0000	+0.0000	Digital Reading
	Ratiometric Reading (2)	$V_{IN} \equiv V_{REF}$ Full Scale = 2.000V	+0.9998	+0.9999	+1.0000	Digital Reading
	Linearity over ± Full Scale (error of reading from best straight line)	$-2V \le V_{IN} \le +2V$		0.5	1	Digital Count Error
	Differential Linearity (difference between worse case step of adjacent counts and ideal step)	$-2V \le V_{IN} \le +2V$		.01		LSB
	Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{IN} \equiv +V_{IN} \approx 2V$		0.5	1	Digital Count Error
e_n	Noise (P-P value not exceeded 95% of time)	V_{IN} = 0V Full scale = 2.000V		15		μV
I_{ILK}	Leakage Current at Input	V_{IN} = 0V		1	10	pA
	Zero Reading Drift	V_{IN} = 0V $0° \le T_A \le 70°C$		0.5	2	μV/°C
TC	Scale Factor Temperature Coefficient (3)	V_{IN} = +2V $0 \le T_A \le 70°C$ (ext. ref. 0 ppm/°C)		2	5	ppm/°C

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7135

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL						
INPUTS						
V_{INH}			2.8	2.2		V
V_{INL}				1.6	0.8	
I_{INL}	Clock in, Run/$\overline{Hold}$, See Figure 4	$V_{IN} = 0$		0.02	0.1	mA
I_{INH}		$V_{IN} = +5V$		0.1	10	μA
OUTPUTS						
V_{OL}	All Outputs	$I_{OL} = 1.6mA$		0.25	0.40	V
V_{OH}	B_1, B_2, B_4, B_8	$I_{OH} = -1mA$	2.4	4.2		V
	D_1, D_2, D_3, D_4, D_5					
V_{OH}	BUSY, $\overline{STROBE}$, OVER-RANGE, UNDER-RANGE POLARITY	$I_{OH} = -10\mu A$	4.9	4.99		V
SUPPLY						
V^+	+5V Supply Range		+4	+5	+6	V
V^-	-5V Supply Range		-3	-5	-8	V
I^+	+5V Supply Current	$f_C = 0$		1.1	3.0	mA
I^-	-5V Supply Current	$f_C = 0$		0.8	3.0	
C_{PD}	Power Dissipation Capacitance	vs. Clock Freq		40		pF
CLOCK						
	Clock Freq. (Note 4)		DC	2000	1200	kHz

NOTES: 1. Tested in 4-1/2 digit (20,000 count) circuit shown in Figure 3, clock frequency 120kHz.
2. Tested with a low dielectric absorption integrating capacitor. See Component Selection Section.
3. The temperature range can be extended to +70°C and beyond as long as the auto-zero and reference capacitors are increased to absorb the higher leakage of the ICL7135.
4. This specification relates to the clock frequency range over which the ICL7135 will correctly perform its various functions. See "Max Clock Frequency" below for limitations on the clock frequency range in a system.

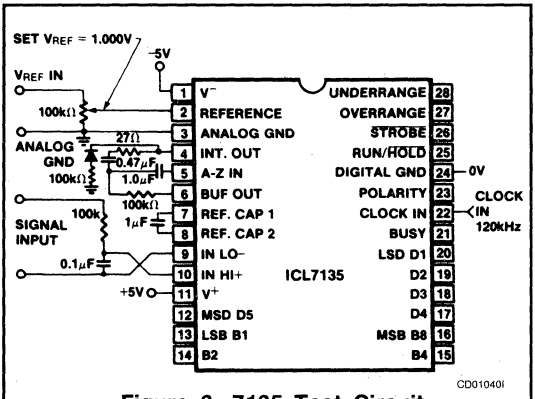


Figure 3: 7135 Test Circuit

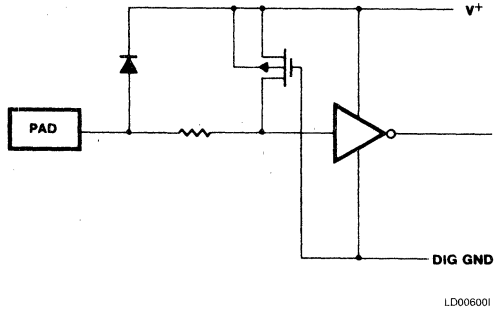


Figure 4: 7135 Digital Logic Input

Note: All typical values have been guaranteed by characterization and are not tested.

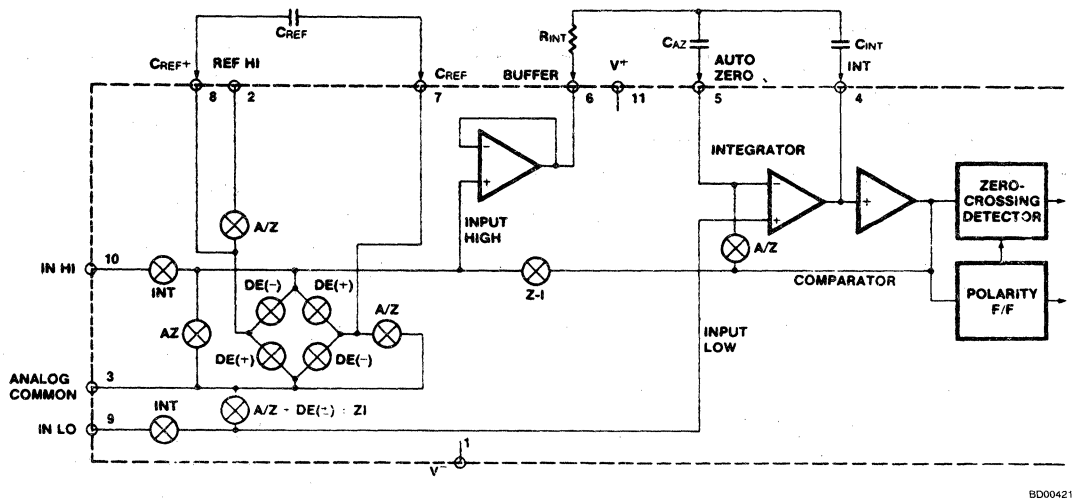


Figure 5: Analog Section of ICL7135

DETAILED DESCRIPTION

Analog Section

Figure 5 shows the Block Diagram of the Analog Section for the ICL7135. Each measurement cycle is divided into four phases. They are (1) auto-zero (A-Z), (2) signal-integrate (INT), (3) deintegrate (DE) and (4) zero-integrator (ZI).

AUTO-ZERO PHASE

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

SIGNAL INTEGRATE PHASE

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is latched into the polarity F/F.

DE-INTEGRATE PHASE

The Third phase is de-integrate, or reference integrate. Input LOW is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is $10{,}000 \left(\frac{V_{IN}}{V_{REF}}\right)$.

ZERO INTEGRATOR PHASE

The final phase is zero integrator. First, input low is shorted to analog COMMON. Second, a feedback loop is closed around the system to input high to cause the integrator output to return to zero. Under normal condition, this phase lasts from 100 to 200 clock pulses, but after an overrange conversion, it is extended to 6200 clock pulses.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 4V full scale swing with some loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

Note: All typical values have been guaranteed by characterization and are not tested.

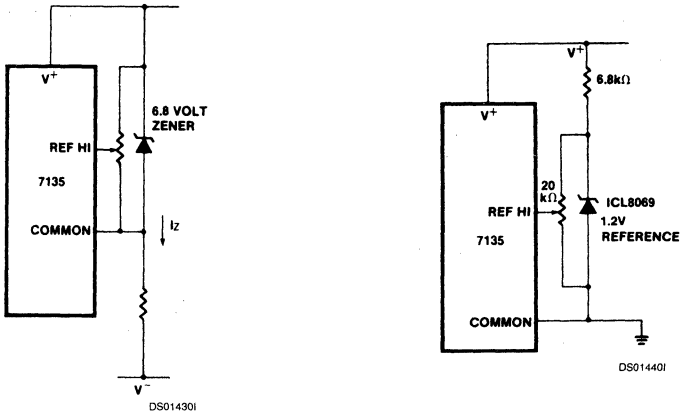


Figure 6: Using an External Reference

Analog Common

Analog COMMON is used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in most applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The reference voltage is referenced to analog COMMON.

Reference

The reference input must be generated as a positive voltage with respect to COMMON, as shown in Figure 6.

DETAILED DESCRIPTION

Digital Section

Figure 7 shows the Digital Section of the 7135. The 7135 includes several pins which allow it to operate conveniently in more sophisticated systems. These include:

Run/$\overline{\text{HOLD}}$ (Pin 25). When high (or open) the A/D will free-run with equally spaced measurement cycles every 40,002 clock pulses. It taken low, the converter will continue the full measurement cycle that it is doing and then hold this reading as long as R/$\overline{\text{H}}$ is held low. A short positive pulse (greater than 300ns) will now initiate a new measurement cycle, beginning with between 1 and 10,001 counts of auto zero. If the pulse occurs before the full measurement cycle (40,002 counts) is completed, it will not be recognized and the converter will simply complete the measurement it is doing. An external indication that a full measurement cycle has been completed is that the first strobe pulse (see below) will occur 101 counts after the end of this cycle. Thus, if Run/$\overline{\text{HOLD}}$ is low and has been low for at least 101 counts, the converter is holding and ready to start a new measurement when pulsed high.

$\overline{\text{STROBE}}$ (Pin 26). This is a negative going output pulse that aids in transferring the BCD data to external latches, UARTs or microprocessors. There are 5 negative going $\overline{\text{STROBE}}$ pulses that occur in the center of each of the digit drive pulses and occur once and only once for each measurement cycle starting 101 pulses after the end of the full measurement cycle. Digit 5 (MSD) goes high at the end of the measurement cycle and stays on for 201 counts. In the center of this digit pulse (to avoid race conditions between changing BCD and digit drives) the first $\overline{\text{STROBE}}$ pulse goes negative for $\frac{1}{2}$ clock pulse width. Similarly, after digit 5, digit 4 goes high (for 200 clock pulses) and 100 pulses later the $\overline{\text{STROBE}}$ goes negative for the second time. This continues through digit 1 (LSD) when the fifth and last $\overline{\text{STROBE}}$ pulse is sent. The digit drive will continue to scan (unless the previous signal was overrange) but no additional $\overline{\text{STROBE}}$ pulses will be sent until a new measurement is available.

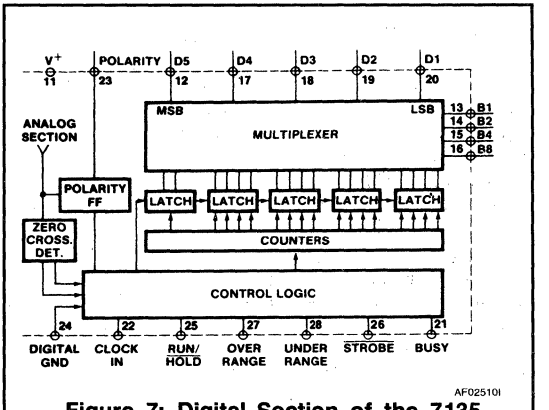


Figure 7: Digital Section of the 7135

BUSY (Pin 21). BUSY goes high at the beginning of signal integrate and stays high until the first clock pulse after zero-crossing (or after end of measurement in the case of an

Note: All typical values have been guaranteed by characterization and are not tested.

overrange). The internal latches are enabled (i.e., loaded) during the first clock pulse after busy and are latched at the end of this clock pulse. The circuit automatically reverts to auto-zero when not BUSY, so it may also be considered a $\overline{(ZI + AZ)}$ signal. A very simple means for transmitting the data down a single wire pair from a remote location would be to AND BUSY with clock and subtract 10,001 counts from the number of pulses received - as mentioned previously there is one "NO-count" pulse in each reference integrate cycle.

OVER-RANGE (Pin 27). This pin goes positive when the input signal exceeds the range (20,000) of the converter. The output F/F is set at the end of BUSY and is reset to zero at the beginning of Reference integrate in the next measurement cycle.

UNDER-RANGE (Pin 28). This pin goes positive when the reading is 9% of range or less. The output F/F is set at the end of BUSY (if the new reading is 1800 or less) and is reset at the beginning of signal integrate of the next reading.

POLARITY (Pin 23). This pin is positive for a positive input signal. It is valid even for a zero reading. In other words, +0000 means the signal is positive but less than the least significant bit. The converter can be used as a null detector by forcing equal frequency of (+) and (−) readings. The null at this point should be less than 0.1 LSB. This output becomes valid at the beginning of reference integrate and remains correct until it is re-validated for the next measurement.

Digit Drives (Pins 12, 17, 18, 19 and 20). Each digit drive is a positive going signal that lasts for 200 clock pulses. The scan sequence is D_5 (MSD), D_4, D_3, D_2 and D_1 (LSD). All five digits are scanned and this scan is continuous unless an over-range occurs. Then all digit drives are blanked from the end of the strobe sequence until the beginning of Reference Integrate when D_5 will start the scan again. This can give a blinking display as a visual indication of over-range.

BCD (Pins 13, 14, 15 and 16). The Binary coded Decimal bits B_8, B_4, B_2 and B_1 are positive logic signals that go on simultaneously with the digit driver signal.

COMPONENT VALUE SELECTION

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

Integrating Resistor

The integrating resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They can supply 20μA of drive current with negligible non-linearity. Values of 5 to 40μA give good results, with a nominal of 20μA, and the exact value of integrating resistor may be chosen by

$$R_{INT} = \frac{\text{full scale voltage}}{20\mu A}$$

Integrating Capacitor

The product of integrating resistor and capacitor should be selected to give the maximum voltage swing which ensures that the tolerance built-up will not saturate the integrator swing (approx. 0.3 volt from either supply). For ±5 volt supplies and analog COMMON tied to supply ground, a ±3.5 to ±4 volt full scale integrator swing is fine, and 0.47μF is nominal. In general, the value of C_{INT} is given by

$$C_{INT} = \left(\frac{[10{,}000 \times \text{clock period}] \times I_{INT}}{\text{integrator output voltage swing}}\right)$$

$$= \frac{(10{,}000)\ (\text{clock period})\ (20\mu A)}{\text{integrator output voltage swing}}$$

A very important characteristic of the integrating capacitor is that it has low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference.

This ratiometric condition should read half scale 0.9999, and any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

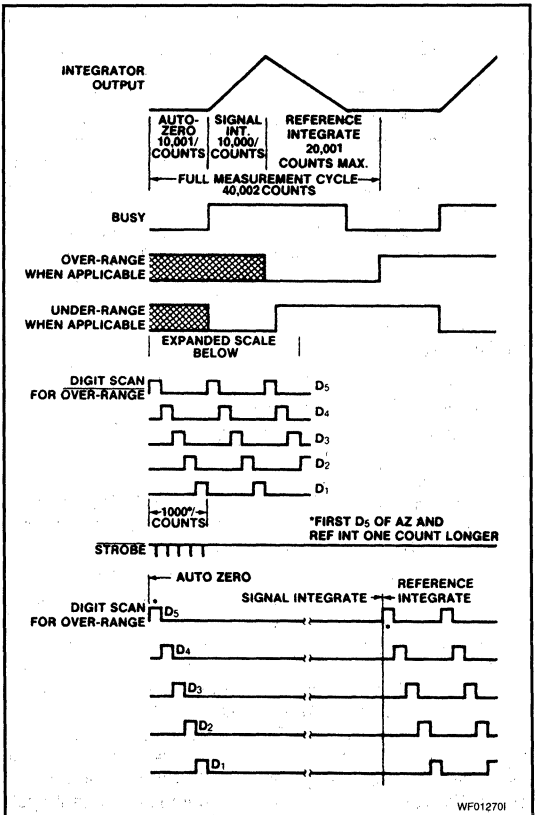


Figure 8: Timing Diagram for Outputs

Auto-Zero and Reference Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system, a large capacitor giving less noise. The reference capacitor should be large enough

Note: All typical values have been guaranteed by characterization and are not tested.

such that stray capacitance to ground from its nodes is negligible.

The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

Reference Voltage

The analog input required to generate a full-scale output is $V_{IN} = 2\ V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. For this reason, it is recommended that a high quality reference be used where high-accuracy absolute measurements are being made.

Rollover Resistor and Diode

A small rollover error occurs in the 7135, but this can be easily corrected by adding a diode and resistor in series between the INTegrator OUTput and analog COMMON or ground. The value shown in the schematics is optimum for the recommended conditions, but if integrator swing or clock frequency is modified, adjustment may be needed. The diode can be any silicon diode, such as 1N914. These components can be eliminated if rollover error is not important, and may be altered in value to correct other (small) sources of rollover as needed.

Max Clock Frequency

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. The comparator in this circuit follows the integrator ramp with a 3μs delay, and at a clock frequency of 160kHz (6μs period) half of the first reference integrate clock period is lost in delay. This means that the meter reading will change from 0 to 1 with a 50μV input, 1 to 2 with 150μV, 2 to 3 at 250μV, etc. This transition at mid-point is considered desirable by most users; however, if the clock frequency is increased appreciably above 160kHz, the instrument will flash "1" on noise peaks even when the input is shorted.

For many-dedicated applications where the input signal is always of one polarity, the delay of the comparator need not be a limitation. Since the non-linearity and noise do not increase substantially with frequency, clock rates of up to ~1MHz may be used. For a fixed clock frequency, the extra count or counts caused by comparator delay will be constant and can be subtracted out digitally.

The clock frequency may be extended above 160kHz without this error, however, by using a low value resistor in series with the integrating capacitor. The effect of the resistor is to introduce a small pedestal voltage on to the integrator output at the beginning of the reference integrate phase. By careful selection of the ratio between this resistor and the integrating resistor (a few tens of ohms in the recommended circuit), the comparator delay can be compensated and the maximum clock frequency extended by approximately a factor of 3. At higher frequencies, ringing and second order breaks will cause significant nonlinearities in the first few counts of the instrument - see Application Note A017.

The minimum clock frequency is established by leakage on the auto-zero and reference caps. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 300kHz, 200kHz, 150kHz, 120kHz, 100kHz, 40kHz, 33 1/3kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 250kHz, 166 2/3kHz, 125kHz, 100kHz, etc. would be suitable. Note that 100kHz (2.5 readings/second) will reject both 50 and 60Hz.

The clock used should be free from significant phase or frequency jitter. Several suitable low-cost oscillators are shown in the Applications section. The multiplexed output means that if the display takes significant current from the logic supply, the clock should have good PSRR.

Zero-Crossing Flip-Flop

The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. False zero-crossings caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by up to one count in every instance, and if a correction were not made, the display would always be one count too high. Therefore, the counter is disabled for one clock pulse at the beginning of phase 3. This one-count delay compensates for the delay of the zero-crossing flip-flop, and allows the correct number to be latched into the display. Similarly, a one-count delay at the beginning of phase 1 gives an overload display of 0000 instead of 0001. No delay occurs during phase 2, so that true ratiometric readings result.

EVALUATING THE ERROR SOURCES

Errors from the "ideal" cycle are caused by:

1. Capacitor droop due to leakage.
2. Capacitor voltage change due to charge "suck-out" (the reverse of charge injection) when the switches turn off.
3. Non-linearity of buffer and integrator.
4. High-frequency limitations of buffer, integrator and comparator.
5. Integrating capacitor non-linearity (dielectric absorption.)
6. Charge lost by C_{REF} in charging C_{stray}.
7. Charge lost by C_{AZ} and C_{INT} to charge C_{stray}.

Each of these errors is analyzed for its error contribution to the converter in application notes listed on the back page, specifically A017 and A032.

NOISE

The peak-to-peak noise around zero is approximately 15μV (pk-to-pk value not exceeded 95% of the time). Near full scale, this value increases to approximately 30μV. Much of the noise originates in the auto-zero loop, and is proportional to the ratio of the input signal to the reference.

ANALOG AND DIGITAL GROUNDS

Extreme care must be taken to avoid ground loops in the layout of ICL7135 circuits, especially in high-sensitivity circuits. It is most important that return currents from digital loads are not fed into the analog ground line.

Note: All typical values have been guaranteed by characterization and are not tested.

POWER SUPPLIES

The 7135 is designed to work from ±5V supplies. However, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5 volts.

See "differential input" for a discussion of the effects this will have on the integrator swing without loss of linearity.

TYPICAL APPLICATIONS

The circuits which follow show some of the wide variety of possibilities, and serve to illustrate the exceptional versatility of this A/D converter.

Figure 9 shows the complete circuit for a 4-½ digit (±2.000V) full scale) A/D with LED readout using the ICL8069 as a 1.2V temperature compensated voltage reference. It uses the band-gap principal to achieve excellent stability and low noise at reverse currents down to 50μA. The circuit also shows a typical R-C input filter. Depending on the application, the time-constant of this filter can be made faster, slower, or the filter deleted completely. The ½ digit LED is driven from the 7 segment decoder, with a zero reading blanked by connecting a D5 signal to RBI input of the decoder. The 2-gate clock circuit should use CMOS gates to maintain good power supply rejection.

Figure 10 is similar except the output drives a multiplexed common cathode LED Display with the 7-Common Emitter Transistor Array, for the digit driver transistors, making a lower component count possible. Both versions of the complete circuit will give a blinking display as a visual indication of overrange. A clock oscillator circuit using the ICM7555 CMOS timer is shown.

A suitable circuit for driving a plasma-type display is shown in Figure 11. The high voltage anode driver buffer is made by Dionics. The 3 AND gates and caps driving 'BI' are needed for interdigit blanking of multiple-digit display elements, and can be omitted if not needed. The 2.5kΩ & 3kΩ resistors set the current levels in the display. A similar arrangement can be used with Nixie® tubes.

The popular LCD displays can be interfaced to the O/P of the ICL7135 with suitable display drivers, such as the ICM7211A as shown in Figure 13. A standard CMOS 4030 QUAD XOR gate is used for displaying the ½ digit, the polarity, and an 'overrange' flag. A similar circuit can be used with the ICL7212A LED driver and the ICM7235A vacuum fluorescent driver with appropriate arrangements made for the 'extra' outputs. Of course, another full driver circuit could be ganged to the one shown if required. This would be useful if additional annunciators were needed. The Figure shows the complete circuit for a 4-½ digit (±2,000V) A/D.

Figure 12 shows a more complicated circuit for driving LCD displays. Here the data is latched into the ICM7211 by the $\overline{\text{STROBE}}$ signal and 'Overrange' is indicated by blanking the 4 full digits.

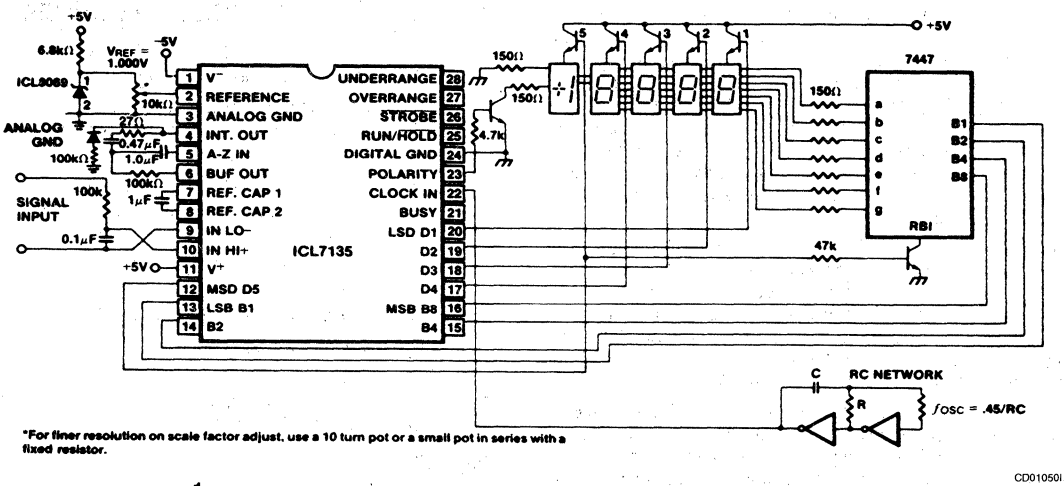
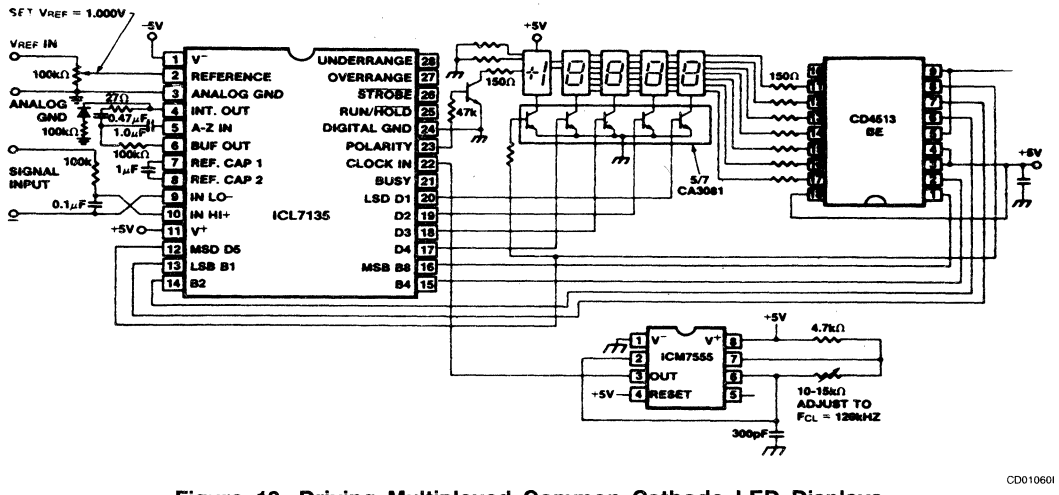


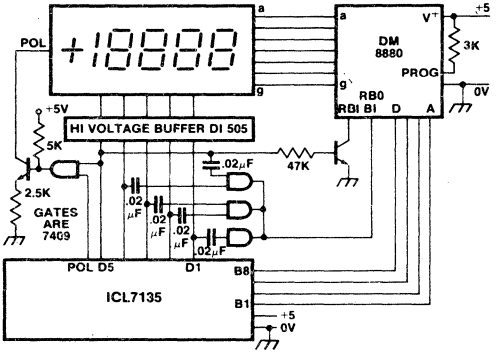
Figure 9: 4-½ Digit A/D Converter with a Multiplexed Common Anode LED Display

Note: All typical values have been guaranteed by characterization and are not tested.



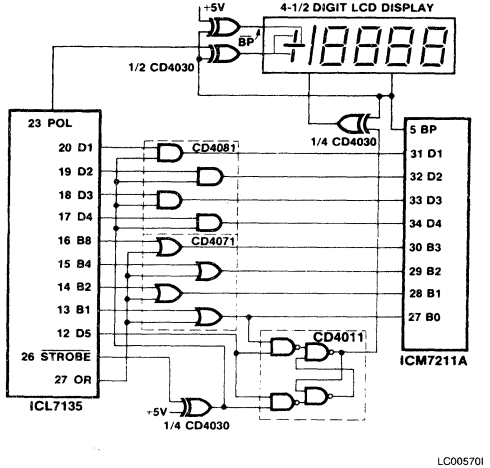
CD01060I

Figure 10: Driving Multiplexed Common Cathode LED Displays



LC00560I

Figure 11: ICL7135 Plasma Display Circuit



LC00570I

Figure 12: LCD Display with Digit Blanking on Overrange

Note: All typical values have been guaranteed by characterization and are not tested.

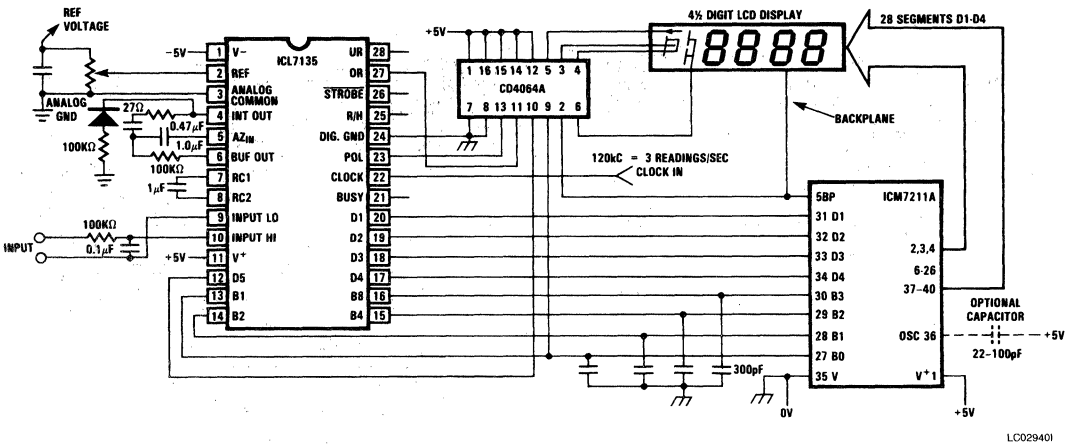


Figure 13: Driving LCD Displays

A problem sometimes encountered with both LED & plasma-type display driving is that of clock source supply line variations. Since the supply is shared with the display, any variation in voltage due to the display reading may cause clock supply voltage modulation. When in overrange the display alternates between a blank display and the 0000 overrange indication. This shift occurs during the reference integrate phase of conversion causing a low display reading just after overrange recovery. Both of the above circuits have considerable current flowing in the digital supply from drivers, etc. A clock source using an LM311 voltage comparator with positive feedback (Figure 14) could minimize any clock frequency shift problem.

The 7135 is designed to work from ±5 volt supplies. However, if a negative supply is not available, it can be generated with an ICL7660 and two capacitors (Figure 15).

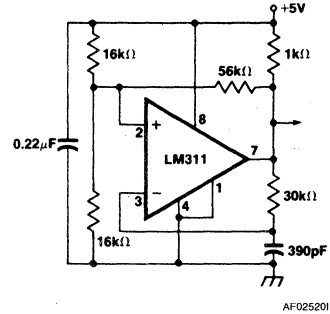


Figure 14: LM311 Clock Source

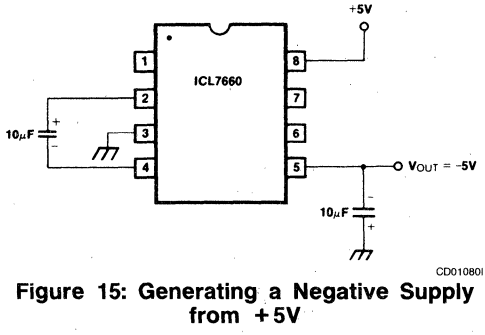


Figure 15: Generating a Negative Supply from +5V

INTERFACING WITH UARTS AND MICROPROCESSORS

Figure 16 shows a very simple interface between a free-running ICL7135 and a UART. The five $\overline{\text{STROBE}}$ pulses start the transmission of the five data words. The digit 5 word is 0000XXXX, digit 4 is 1000XXXX, digit 3 is 0100XXXX, etc. Also the polarity is transmitted indirectly by using it to drive the Even Parity Enable Pin (EPE). If EPE of the receiver is held low, a parity flag at the receiver can be decoded as a positive signal, no flag as negative. A complex arrangement is shown in Figure 17. Here the UART can instruct the A/D to begin a measurement sequence by a word on RRI. The BUSY signal resets the Data Ready Reset (DRR). Again $\overline{\text{STROBE}}$ starts the transmit sequence. A quad 2 input multiplexer is used to superimpose polarity, over-range, and under-range onto the D_5 word since in this instance it is known that $B_2 = B_4 = B_8 = 0$.

Note: All typical values have been guaranteed by characterization and are not tested.

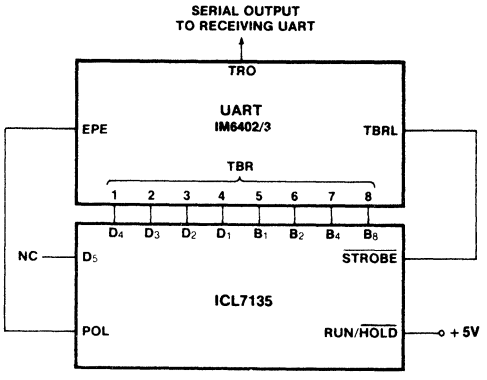


Figure 16: ICL7135 to UART Interface

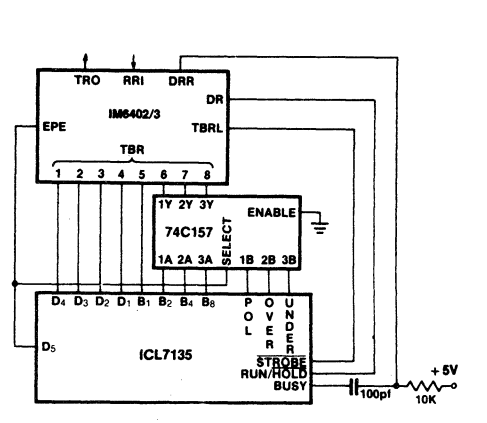


Figure 17: Complex ICL7135 to UART Interface

For correct operation it is important that the UART clock be fast enough that each word is transmitted before the next $\overline{\text{STROBE}}$ pulse arrives. Parity is locked into the UART at load time but does not change in this connection during an output stream.

Circuits to interface the ICL7135 directly with three popular microprocessors are shown in Figures 18 and 19. The 8080/8048 and the MC6800 groups with 8 bit buses need to have polarity, over-range and under-range multiplexed onto the Digit 5 word — as in the UART circuit. In each case the microprocessor can instruct the A/D when to begin a measurement and when to hold this measurement.

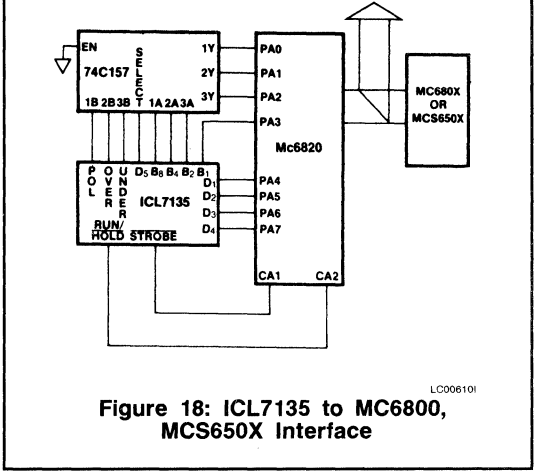


Figure 18: ICL7135 to MC6800, MCS650X Interface

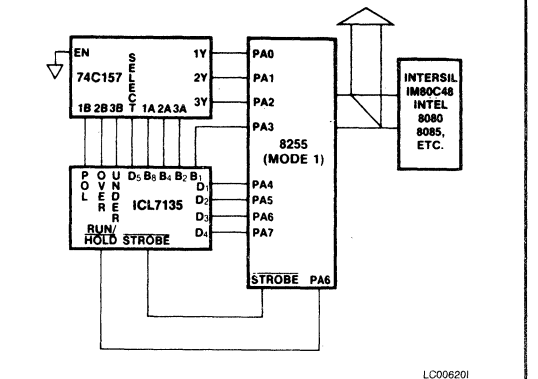


Figure 19: ICL7135 to MCS-48, -80, 85 Interface

APPLICATION NOTES

A016 "Selecting A/D Converters," by David Fullagar
A017 "The Integrating A/D Converters," by Lee Evans
A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood
A019 "4-½ Digit Plan Meter Demonstrator/ Instrumentation Boards," by Michael Dufort
A023 "Low Cost Digital Panel Meter Designs," by David Fullager and Michael Dufort
A028 "Building an Auto-Ranging DMM Using the 8052A/ 7103A A/D Converter Pair," by Larry Goff
A030 "The ICL7104 — A Binary Output A/D Converter for Microprocessors", by Peter Bradshaw
A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106 Family", by Peter Bradshaw
R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7136
3½-Digit LCD Low Power A/D Converter

GENERAL DESCRIPTION

The Intersil ICL7136 is a high performance, very low power 3½-digit A/D converter. All the necessary active devices are contained on a single CMOS IC, including seven-segment decoders, display drivers, reference, and clock. The 7136 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive. The supply current is under 100μA, ideally suited for 9V battery operation.

The 7136 brings together an unprecedented combination of high accuracy, versatility, and true economy. High accuracy, like auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA max., and rollover error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation allows a high performance panel meter to be built with the addition of only 7 passive components and a display.

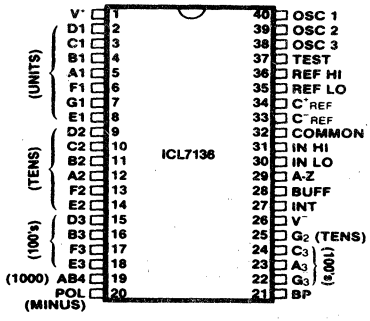
The ICL7136 is an improved version of the ICL7126, eliminating the overrange hangover and hysteresis effects, and should be used in its place in all applications. It can also be used as a plug-in replacement for the ICL7106 in a wide variety of applications, changing only the passive components.

FEATURES

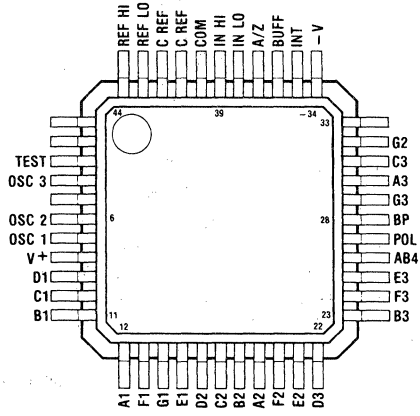
- **First-Reading Recovery From Overrange Gives Immediate "OHMS" Measurement**
- **Guaranteed Zero Reading for 0V Input**
- **True Polarity at Zero for Precise Null Detection**
- **1pA Typical Input Current**
- **True Differential Input and Reference**
- **Direct LCD Display Drive — No External Components Required**
- **Pin Compatible With The ICL7106, ICL7126**
- **Low Noise — 15μVp-p Without Hysteresis or Overrange Hangover**
- **On-Chip Clock and Reference**
- **Low Power Dissipation, Guaranteed Less Than 1mW — Gives 8,000 Hours Typical 9V Battery Life**
- **No Additional Active Circuits Required**
- **Evaluation Kit Available (ICL7136EV/Kit)**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7136CJL	0°C to +70°C	40-Pin CERDIP
ICL7136CDL	0°C to +70°C	40-Pin Ceramic DIP
ICL7136CM44	0°C to +70°C	44-Pin Surface Mount
ICL7136CPL	0°C to +70°C	40-Pin Plastic DIP
ICL7136RCPL	0°C to +70°C	40-Pin Plastic DIP
ICL7136EV/KIT		EVALUATION KIT



CD01090I



CD03241I

Figure 1: Pin Configurations

Note: All typical values have been guaranteed by characterization and are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input)(Note 1) .... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... TEST to V^+

Power Dissipation (Note 2)
Ceramic Package 1000mW
Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.
Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

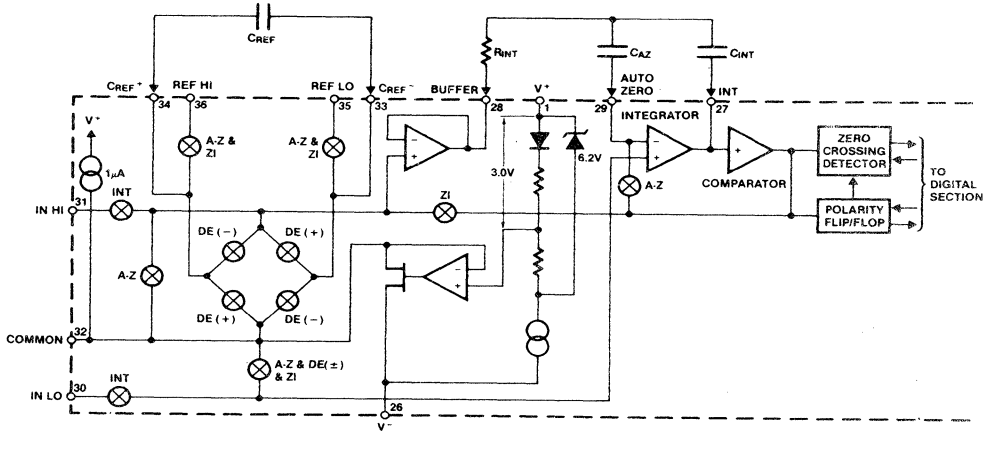


Figure 2: Functional Diagram

ELECTRICAL CHARACTERISTICS (Notes 3, 7)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Zero Input Reading	V_{IN} = 0.0V Full-Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$, V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Roll-Over Error (Difference in reading for equal positive and negative reading near full-scale)	$-V_{IN} = +V_{IN} \simeq$ 200.0mV	−1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full-scale = 200mV or Full-Scale = 2.000V	−1	±0.02	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V Full-Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V, Full Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0V		1	10	pA
Zero Reading Drift	V_{IN} = 0V, 0°C < T_A < +70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV, 0°C < T_A < +70°C (Ext. Ref. Oppm/°C)		1	5	ppm/°C
Supply Current (Does not include COMMON current)	V_{IN} = 0V (Note 6)		70	100	μA

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7136

ELECTRICAL CHARACTERISTICS (CONT.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog COMMON Voltage (With respect to positive supply)	250kΩ between Common and Positive Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog COMMON (With respect to positive supply)	250kΩ between Common and Positive Supply		150		ppm/°C
Pk-Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Power Dissipation Capacitance	vs Clock Frequency		40		pF

NOTES: 3. Unless otherwise noted, specifications apply at T_A = 25°C, f_{clock} = 16kHz and are tested in the circuit of Figure 3.
4. Refer to "Differential Input" discussion.
5. Backplane drive is in phase with segment drive for "off" segment, 180° out of phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
6. 48kHz oscillator, Figure 4, increases current by 20μA (typ).
7. Extra capacitance of CERDIP package changes oscillator resistor value to 470kΩ or 150kΩ (1 reading/sec or 3 readings/sec).

TEST CIRCUITS

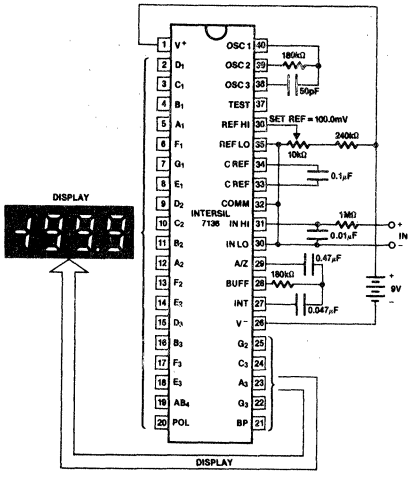


Figure 3: ICL7136 with Liquid Crystal Display

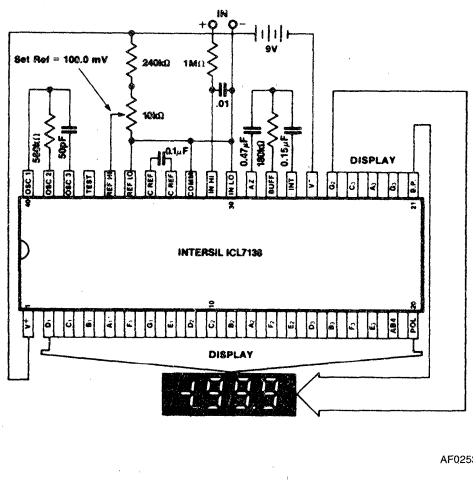
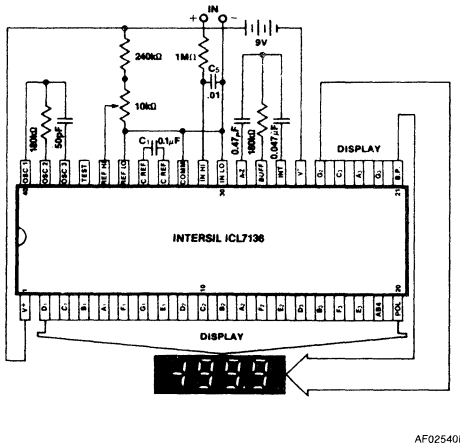


Figure 4: 7136 Clock Frequency 16kHz (1 reading/sec)

Note: All typical values have been guaranteed by characterization and are not tested.



AF02540I

Figure 5: Clock Frequency 48kHz (3 readings/sec)

DETAILED DESCRIPTION (Analog Section)

Figure 1 shows the Functional Diagram of the Analog Section for the ICL7136. Each measurement cycle is divided into four phases. They are 1) auto-zero (A-Z), 2) signal integrate (INT), 3) de-integrate (DE) and 4) zero integrator (ZI).

AUTO-ZERO PHASE

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor, C_{AZ}, to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

SIGNAL INTEGRATE PHASE

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common-mode range; within 1V of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

DE-INTEGRATE PHASE

The next phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically, the digital reading displayed is 1000 (V_{IN}/V_{REF}).

ZERO INTEGRATOR PHASE

The final phase is zero integrator. First, input low is shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Finally, a feedback loop is closed around the system to input high to cause the integrator output to return to zero. Under normal conditions, this phase lasts for between 11 to 140 clock pulses, but after a "heavy" overrange conversion, it is extended to 740 clock pulses.

Differential Input

The input can accept differential voltages anywhere within the common-mode range of the input amplifier; or specifically from 0.5V below the positive supply to 1.0V above the negative supply. In this range the system has a CMRR of 86dB typical. However, since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full-scale swing with little loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll-over voltage caused by the reference capacitance losing or gaining charge to stray capacity on its nodes. If there is a large common-mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition (see Component Values Selection).

Analog Common

This pin is included primarily to set the common-mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 3.0V more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (> 7V), the COMMON voltage will have a low voltage coefficient (0.001%/%), low output impedance (≈35Ω), and a temperature coefficient typically less than 80ppm/°C.

Note: All typical values have been guaranteed by characterization and are not tested.

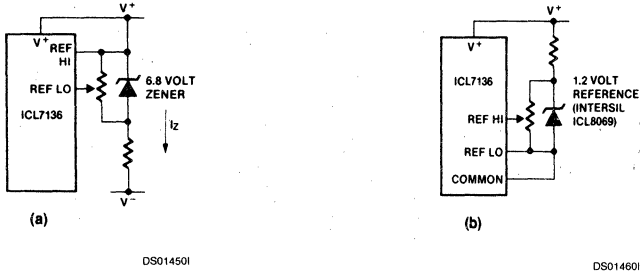


Figure 6: Using an External Reference

The limitations of the on-chip reference should also be recognized, however. The reference temperature coefficient (TC) can cause some degradation in performance. Temperature changes of 2°C to 8°C, typical for instruments, can give a scale factor error of a count or more. Also, the COMMON voltage will have a poor voltage coefficient when the total supply voltage is less than that which will cause the zener to regulate (< 7V). These problems are eliminated if an external reference is used, as shown in Figure 6.

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If the reference can be conveniently referred to analog COMMON, it should be since this removes the common-mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET which can sink 3mA or more of current to hold the voltage 3.0V below the positive supply (when a load is trying to pull the common line positive). However, there is only 1μA of source current, so COMMON may easily be tied to a more negative voltage, thus overriding the internal reference.

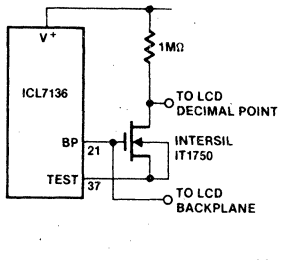


Figure 7: Simple Inverter for Fixed Decimal Point

TEST

The TEST pin serves two functions. It is coupled to the internally generated digital supply through a 500Ω resistor. Thus, it can be used as the negative supply for external segment drivers such as for decimal points or any other presentation the user may want to include on the LCD display. Figures 7 and 8 show such an application. No more than a 1mA load should be applied.

The second function is a "lamp test." When TEST is pulled high (to V^+) all segments will be turned on and the display should read −1888. The TEST pin will sink about 10mA under these conditions.

Caution: In the lamp test mode, the segments have a constant DC voltage (no square-wave). This may burn the LCD display if maintained for extended periods.

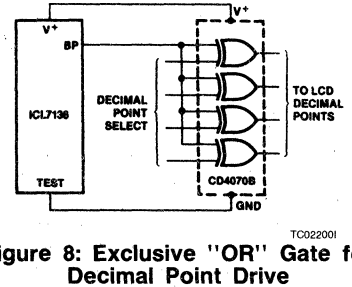


Figure 8: Exclusive "OR" Gate for Decimal Point Drive

DETAILED DESCRIPTION (Digital Section)

Figure 9 shows the digital section for the 7136. An internal digital ground is generated from a 6V Zener diode and a large P channel source follower. This supply is made stiff to absorb the relatively large capacitive currents when the backplane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60Hz square-wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments. The polarity indication is "ON" for

Note: All typical values have been guaranteed by characterization and are not tested.

negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

DISPLAY FONT

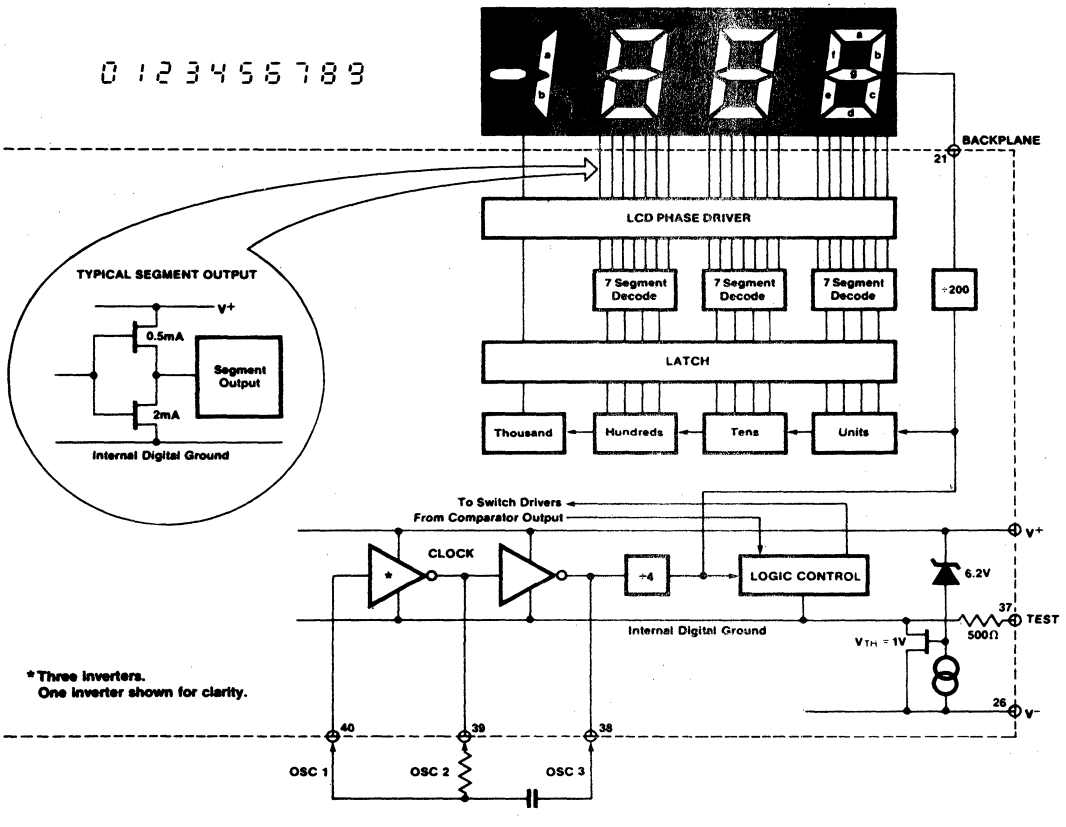


Figure 9: Digital Section

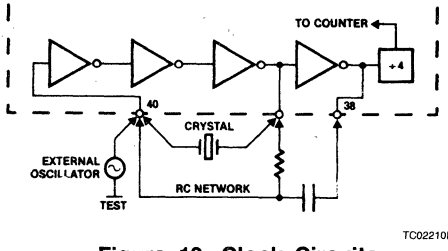


Figure 10: Clock Circuits

System Timing

Figure 10 shows the clock oscillator provided in the 7136. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An RC oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the four convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 counts to 2000 counts), zero integrator (11 counts to 140 counts*) and auto-zero (910 counts to 2900 counts). For signals less than full-scale, auto-zero gets the unused portion of reference de-integrate and zero integrator. This makes a complete measure cycle of 4000 (16,000 clock pulses) independent

*After an overranged conversion of more than 2060 counts, the zero integrator phase will last 740 counts, and auto-zero will last 260 counts.

Note: All typical values have been guaranteed by characterization and are not tested.

of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of the 60Hz period. Oscillator frequencies of 60kHz, 48kHz, 40kHz, 33 1/3kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 66 2/3kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50Hz and 60Hz (also 400Hz and 440Hz). See also A052.

COMPONENT VALUE SELECTION

(See also A052)

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 6μA of quiescent current. They can supply ~1μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full-scale, 1.8MΩ is near optimum, and similarly 180kΩ for a 200.0mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3V from either supply). When the analog COMMON is used as a reference, a nominal ±2V full-scale integrator swing is fine. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.047μF, for 1 reading/second (16kHz) 0.15μF. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

The integrating capacitor should have low dielectric absorption to prevent roll-over errors. While other types may be adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full-scale where noise is very important, a 0.47μF capacitor is recommended. The ZI phase allows a large auto-zero capacitor to be used without causing the hysteresis or overrange hangover problems that can occur with the ICL7126 or ICL7106 (see A032).

Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common-mode voltage exists (i.e., the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally, 1.0μF will hold the roll-over error to 0.5 count in this instance.

Oscillator Components

For all ranges of frequency a 50pF capacitor is recommended and the resistor is selected from the approximate equation f~0.45/RC. For 48kHz clock (3 readings/second), R = 180kΩ, for 16kHz, R = 560kΩ.

Reference Voltage

The analog input required to generate full-scale output (2000 counts) is $V_{IN} = 2V_{REF}$. Thus, for the 200.0mV and 2.000V scale, V_{REF} should equal 100.0mV and 1.000V, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full-scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select V_{REF} = 0.341V. A suitable value for the integrating resistor would be 330kΩ. This makes the system slightly quieter and also avoids the necessity of a divider network on the input. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

TYPICAL APPLICATIONS

The 7136 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

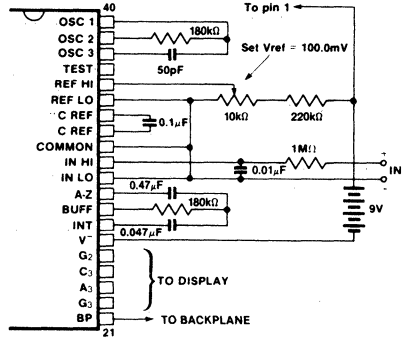
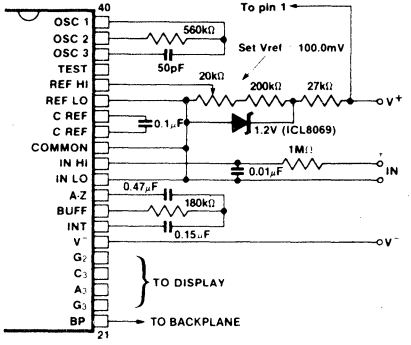


Figure 11: 7136 Using the Internal Reference

Values shown are for 200.0mV full-scale, 3 readings/sec, floating supply voltage (9V battery).

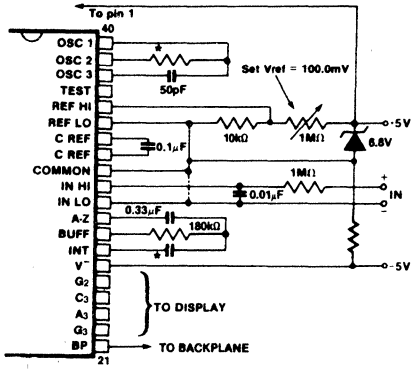
Note: All typical values have been guaranteed by characterization and are not tested.



CD01140I

Figure 12: 7136 with an External Band-Gap Reference (1.2V Type)

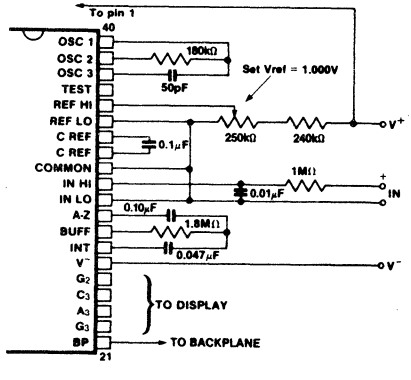
IN LO is tied to COMMON, thus establishing the correct common-mode voltage. COMMON acts as a pre-regulator for the reference. Values shown are for 1 reading/ sec.



CD01160I

Figure 14: 7136 with Zener Diode Reference

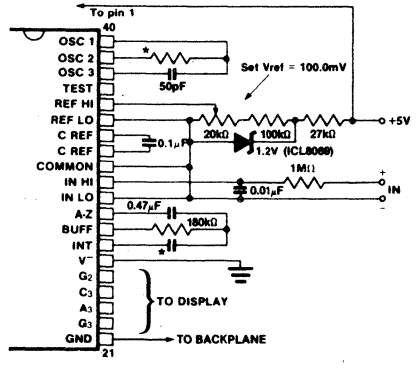
Since low TC zeners have breakdown voltages ~6.8V, diode must be placed across the total supply (10V). As in the case of Figure 13, IN LO may be tied to COMMON.



CD01150I

Figure 13: Recommended Component Values for 2.000V Full-Scale, 3 Readings/Sec

For 1 reading/sec, change C_{INT}, R_{OSC} to values of Figure 12.



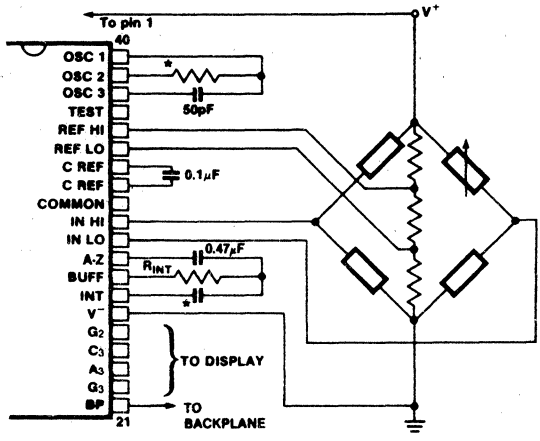
CD01170I

Figure 15: 7136 Operated from Single +5V Supply

An external reference must be used in this application, since the voltage between V^+ and V^- is insufficient for correct operation of the internal reference.

*Values depend on clock frequency. See Figures 11, 12, 13.

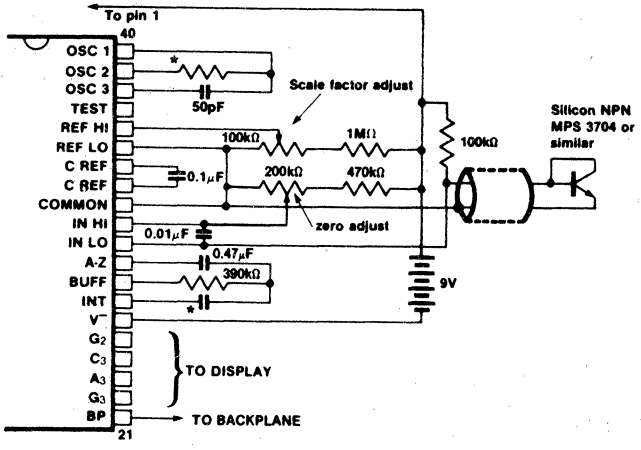
Note: All typical values have been guaranteed by characterization and are not tested.



CD01180I

Figure 16: 7136 Measuring Ratiometric Values of Quad Load Cell

The resistor values within the bridge are determined by the desired sensitivity.

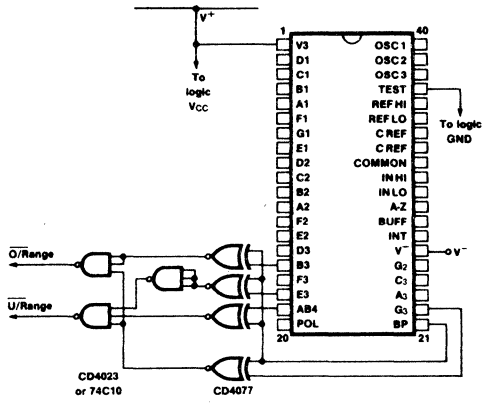


CD01190I

Figure 17: 7136 used as a Digital Centigrade Thermometer

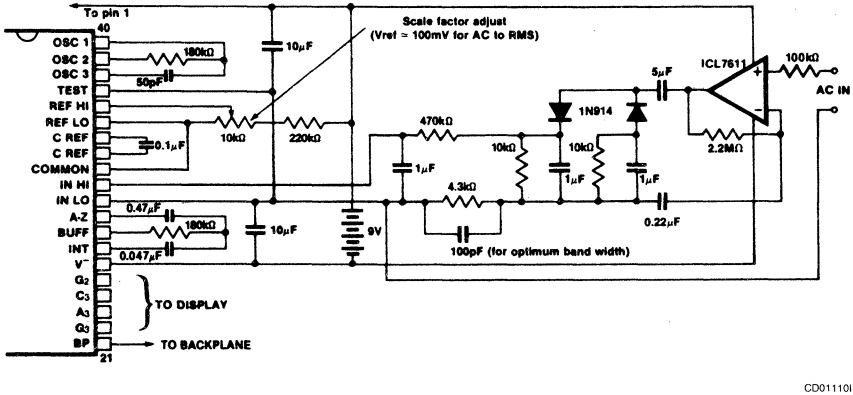
A silicon diode-connected transistor has a temperature coefficient of about −2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for a 100.0 reading. See ICL8073/4 and AD590 data sheets for alternative circuits.

Note: All typical values have been guaranteed by characterization and are not tested.



CD012001

Figure 18: Circuit for Developing Underrange and Overrange Signals from 7136 Outputs



CD011101

Figure 19: AC to DC Converter with 7136

Test is used as a common-mode reference level to ensure compatibility with most op amps.

APPLICATION NOTES

A016 "Selecting A/D Converters," by David Fullagar.
A017 "The Integrating A/D Converter," by Lee Evans.
A018 "Do's and Dont's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.
A019 "4½-Digit Panel Meter Demonstrator/ Instrumentation Boards," by Michael Dufort.
A023 "Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort.
A032 "Understanding the Auto-Zero and Common-Mode Behavior of the ICL7106/7/9 Family," by Peter Bradshaw.
A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106," by Larry Goff.
A047 "Games People Play with Intersil's A/D Converters," edited by Peter Bradshaw.
A052 "Tips for Using Single-Chip 3½-Digit A/D Converters," by Dan Watson.

7136 EVALUATION KIT

After purchasing a sample of the 7136, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application.

To facilitate evaluation of this unique circuit, Intersil is offering a kit which contains all the necessary components to build a 3½-digit panel meter. With the ICL7136EV/Kit and the small number of additional components required, an engineer or technician can have the system "up and running" in about half an hour. The kit contains a circuit board, a display (LCD), passive components, and miscellaneous hardware.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7137
3½-Digit LED Low Power Single-Chip A/D Converter

GENERAL DESCRIPTION

The Intersil ICL7137 is a high performance, very low power 3½-digit A/D converter. All the necessary active devices are contained on a single CMOS IC, including seven-segment decoders, display drivers, reference, and clock. The 7137 is designed to interface with a light emitting diode (LED) display. The supply current (exclusive of display) is under 200μA, ideally suited for battery operation.

The 7137 brings together an unprecedented combination of high accuracy, versatility, and true economy. The device features auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA max., and rollover error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of the ICL7137 allows a high performance panel meter to be built with the addition of only 10 passive components and a display.

The ICL7137 is an improved version of the ICL7107, eliminating the overrange hangover and hysteresis effects, and should be used in its place in all applications, changing only the passive component values.

FEATURES

- **First-Reading Recovery From Overrange allows Immediate "OHMS" Measurement**
- **Guaranteed Zero Reading for 0V Input**
- **True Polarity at Zero for Precise Null Detection**
- **1pA Typical Input Current**
- **True Differential Input and Reference**
- **Direct LED Display Drive — No External Components Required**
- **Pin Compatible With The ICL7107**
- **Low Noise — 15μVp-p Without Hysteresis or Overrange Hangover**
- **On-Chip Clock and Reference**
- **Improved Rejection of Voltage On COMMON Pin**
- **No Additional Active Circuits Required**
- **Evaluation Kit Available ICL7137EV/Kit**

ORDERING INFORMATION*

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7137CJL	0°C to +70°C	CERDIP
ICL7137CDL	0°C to +70°C	40-Pin Ceramic
ICL7137CPL	0°C to +70°C	40-Pin Plastic
ICL7137RCPL	0°C to +70°C	40-Pin Plastic
ICL7137EV/KIT		EVALUATION KIT

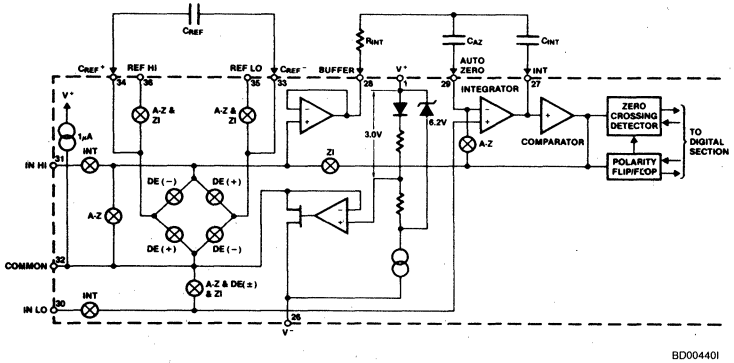


Figure 1: Functional Diagram

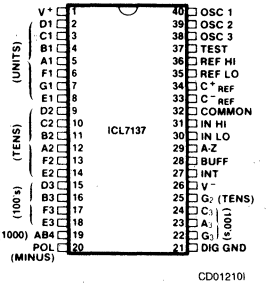


Figure 2: Pin Configuration* (Outline dwgs PL, JL, DL)

301669-002

Note: All typical values have been guaranteed by characterization and are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V^+ ..... +6V
V^- ..... −9V
Analog Input Voltage (either input)(Note 1) .... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... GND to V^+

Power Dissipation (Note 2)
Ceramic Package 1000mW
Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.
Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

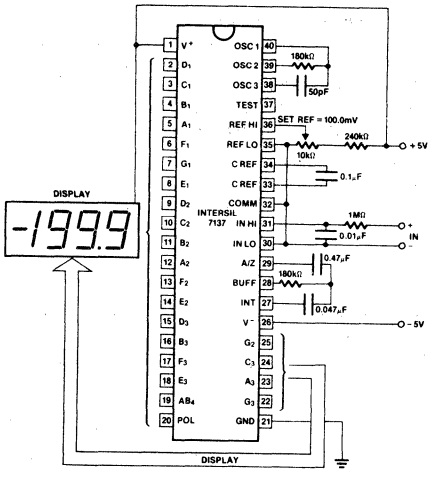
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Zero Input Reading	V_{IN} = 0.0V Full-Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$, V_{REF} = 100mV	998	999/1000	1000	Digital Reading
Roll-Over Error (Difference in reading for equal positive and negative reading near full-scale)	$-V_{IN} = +V_{IN} \simeq$ 200.0mV	−1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full-scale = 200mV or Full-Scale = 2.000V	−1	±0.02	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V Full-Scale = 200.0mV		30		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V, Full-Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0V		1	10	pA
Zero Reading Drift	V_{IN} = 0V, 0°C < T_A < +70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV, 0°C < T_A < +70°C (Ext. Ref. Oppm/°C)		1	5	ppm/°C
V^+ Supply Current (Does not Include LED current)	V_{IN} = 0V (Note 5)		70	200	μA
V^- Supply current			40		
Analog COMMON Voltage (With respect to positive supply)	250kΩ between Common and Positive Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog COMMON (With respect to positive supply)	250kΩ between Common and Positive Supply		150		ppm/°C
Segment Sinking Current (Except Pins 19 & 20) (Pin 19 only) (Pin 20 only)	V^+ = 5.0V Segment Voltage = 3V	5 10 4	8.0 16 7		mA
Power Dissipation Capacitance	vs. Clock Frequency		40		pF

NOTES: 3. Unless otherwise noted, specifications apply at T_A = 25°C, f_{clock} = 16kHz and are tested in the circuit of Figure 4.
4. Refer to "Differential Input" discussion.
5. 48kHz oscillator, Figure 5, increases current by 35μA (typ).
6. Extra capacitance of CERDIP package changes oscillator resistor value to 470kΩ or 150kΩ (1 reading/sec or 3 readings/sec).

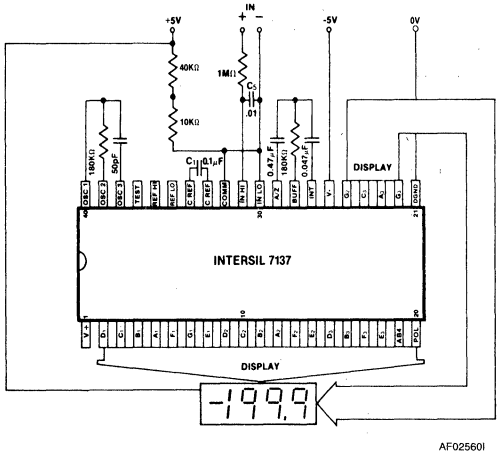
Note: All typical values have been guaranteed by characterization and are not tested.



CD01220I

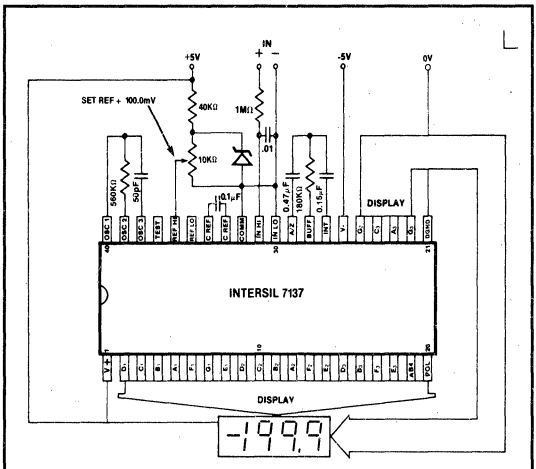
Figure 3: ICL7137 with LED Display

TEST CIRCUITS



AF02560I

Figure 4: 7137 Clock Frequency 16kHz (1 reading/sec)



AF02570I

Figure 5: Clock Frequency 48kHz (3 readings/sec)

DETAILED DESCRIPTION (Analog Section)

Figure 1 shows the Functional Diagram of the Analog Section for the ICL7137. Each measurement cycle is divided into four phases. They are 1) auto-zero (A-Z), 2) signal integrate (INT), 3) de-integrate (DE) and 4) zero-integrator (ZI).

AUTO-ZERO PHASE

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor, C_{AZ}, to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

SIGNAL INTEGRATE PHASE

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common-mode range; within 1V of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

Note: All typical values have been guaranteed by characterization and are not tested.

DE-INTEGRATE PHASE

The next phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically; the digital reading displayed is $1000(V_{IN}/V_{REF})$.

ZERO INTEGRATOR PHASE

The final phase is zero integrator. First, input low is shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Finally, a feedback loop is closed around the system to input high to cause the integrator output to return to zero. Under normal conditions, this phase lasts for between 11 to 140 clock pulses, but after a "heavy" overrange conversion, it is extended to 740 clock pulses.

Differential Input

The input can accept differential voltages anywhere within the common-mode range of the input amplifier; or specifically from 0.5V below the positive supply to 1.0V above the negative supply. In this range the system has a CMRR of 90dB typical. However, since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full-scale swing with little loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll-over voltage caused by the reference capacitance losing or gaining charge to stray capacity on its nodes. If there is a large common-mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition (see Component Value Selection).

Analog Common

This pin is included primarily to set the common-mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 3.0V more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (> 7V), the COMMON voltage will have a low voltage coefficient (0.001%/%), low output impedance($\simeq 35\Omega$), and a temperature coefficient typically less than 150ppm/°C.

The limitations of the on-chip reference should also be recognized, however. The reference temperature coefficient (TC) can cause some degradation in performance. Temperature changes of 2°C to 8°C, typical for instruments, can give a scale factor error of a count or more. Also, the COMMON voltage will have a poor voltage coefficient when the total supply voltage is less than that which will cause the zener to regulate (< 7V). These problems are eliminated if an external reference is used, as shown in Figure 6.

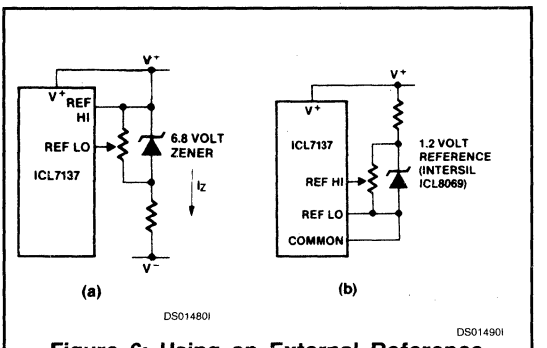


Figure 6: Using an External Reference

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If the reference can be conveniently referred to analog COMMON, it should be since this removes the common-mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET which can sink 100μA or more of current to hold the voltage 3.0V below the positive supply (when a load is trying to pull the common line positive). However, there is only 1μA of source current, so COMMON may easily be tied to a more negative voltage, thus overriding the internal reference.

TEST

The TEST pin is coupled to the internal digital supply through a 500Ω resistor, and functions as a "lamp test." When TEST is pulled high (to V^+) all segments will be turned on and the display should read — 1888. The TEST pin will sink about 10mA under these conditions.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL7137

DISPLAY FONT

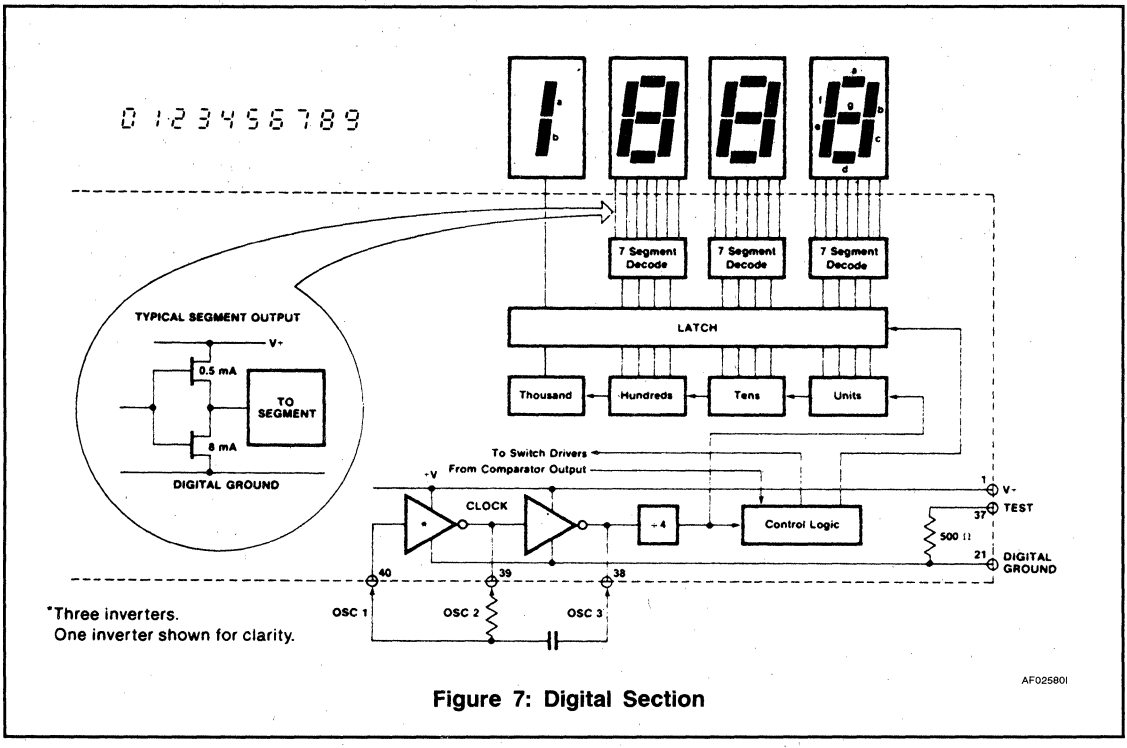


Figure 7: Digital Section

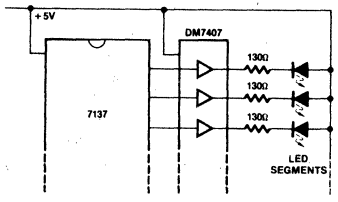


Figure 8: Display Buffering for Increased Drive Current

DETAILED DESCRIPTION (Digital Section)

Figure 7 shows the digital section for the 7137. The segments are driven at 8mA, suitable for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16mA. The polarity indication is "ON" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

Figure 8 shows a method of increasing the output drive current, using four DM7407 Hex Buffers. Each buffer is capable of sinking 40mA.

System Timing

Figure 9 shows the clock oscillator provided in the 7137. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An RC oscillator using all three pins.

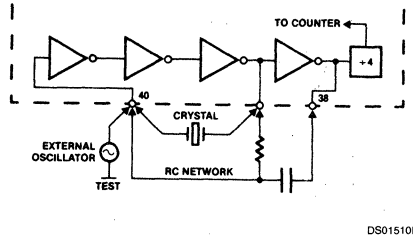


Figure 9: Clock Circuits

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the four convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 counts to 2000 counts),

Note: All typical values have been guaranteed by characterization and are not tested.

zero integrator (11 counts to 140 counts*) and auto-zero (910 counts to 2900 counts). For signals less than full-scale, auto-zero gets the unused portion of reference de-integrate and zero integrator. This makes a complete measure cycle of 4000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of the 60Hz period. Oscillator frequencies of 60kHz, 48kHz, 40kHz, 33 1/3kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 66 2/3kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50Hz and 60Hz (also 400Hz and 440Hz.) See also A052.

*After an overranged conversion of more than 2060 counts, the zero integrator phase will last 740 counts, and auto-zero will last 260 counts.

COMPONENT VALUE SELECTION

(See Application Note A052)

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 6μA of quiescent current. They can supply ~1μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full-scale, 1.8MΩ is near optimum, and similarly 180kΩ for a 200.0mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3V from either supply). When the analog COMMON is used as a reference, a nominal ±2V full-scale integrator swing is fine. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.047μF, for 1 reading/second (16kHz) 0.15μF. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

The integrating capacitor should have low dielectric absorption to prevent roll-over errors. While other types may be adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full-scale where noise is very important, a 0.47μF capacitor is recommended. The ZI phase allows a large auto-zero capacitor to be used without causing the hysteresis or overrange hangover problems that can occur with the ICL7107 or ICL7117 (See Application Note A032).

Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common-mode voltage exists (i.e., the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally, 1.0μF will hold the roll-over error to 0.5 count in this instance.

Oscillator Components

For all ranges of frequency a 50pF capacitor is recommended and the resistor is selected from the approximate equation $f \simeq 0.45/RC$. For 48kHz clock (3 readings/second), R = 180kΩ, while for 16kHz (1 reading/sec), R = 560kΩ.

Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200.0mV and 2,000V scale, V_{REF} should equal 100.0mV and 1.000V, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full-scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select V_{REF} = 0.341V. A suitable value for the integrating resistor would be 330kΩ. This makes the system slightly quieter and also avoids the necessity of a divider network on the input. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

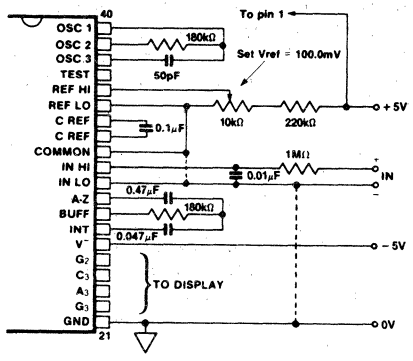
TYPICAL APPLICATIONS

The 7137 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

6

*After an overranged conversion of more than 2060 counts, the zero intergrator phase will last 740 counts, and auto-zero will last 260 counts.

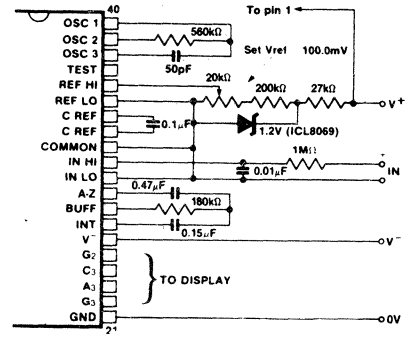
Note: All typical values have been guaranteed by characterization and are not tested.



CD01230I

Figure 10: 7137 Using the Internal Reference.

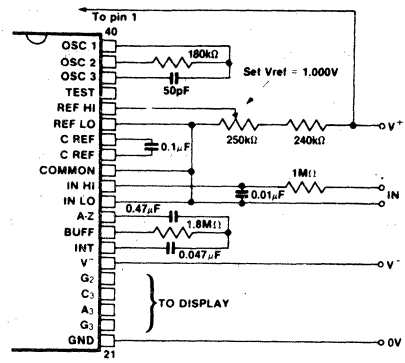
Values shown are for 200.0mV full-scale, 3 readings/sec. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog COMMON.)



CD01240I

Figure 11: 7137 with an External Band-Gap Reference (1.2V Type).

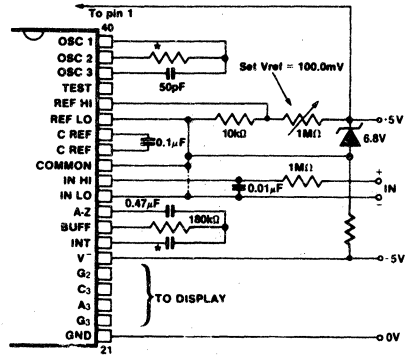
IN LO is tied to COMMON, thus establishing the correct common-mode voltage. COMMON acts as a pre-regulator for the reference. Values shown are for 1 reading/sec.



CD01250I

Figure 12: Recommended Component Values for 2.000V Full-Scale, 3 Readings/Sec.

For 1 reading/sec, change C_{INT}, R_{OSC} to values of Figure 11.



CD01260I

Figure 13: 7137 with Zener Diode Reference.

Since low TC zeners have breakdown voltages ~ 6.8V, diode must be placed across the total supply (10V). As in the case of Figure 11, IN LO may be tied to COMMON.

Note: All typical values have been guaranteed by characterization and are not tested.

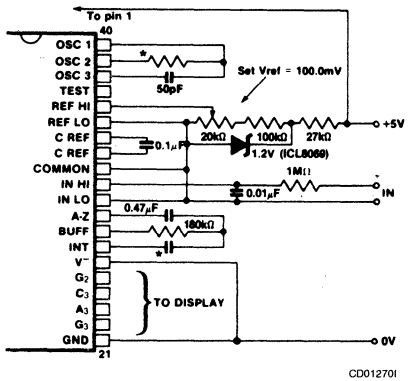


Figure 14: 7137 Operated from Single +5V Supply.

An external reference must be used in this application, since the voltage between V^+ and V^- is insufficient for correct operation of the internal reference.

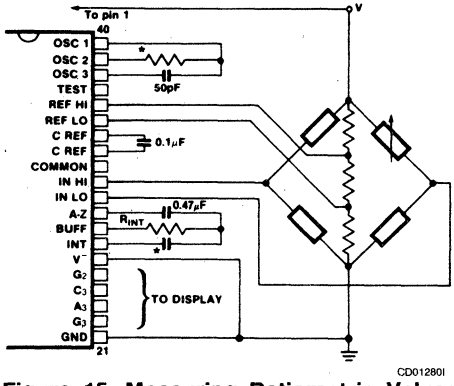


Figure 15: Measuring Ratiometric Values of Quad Load Cell.

The resistor values within the bridge are determined by the desired sensitivity.

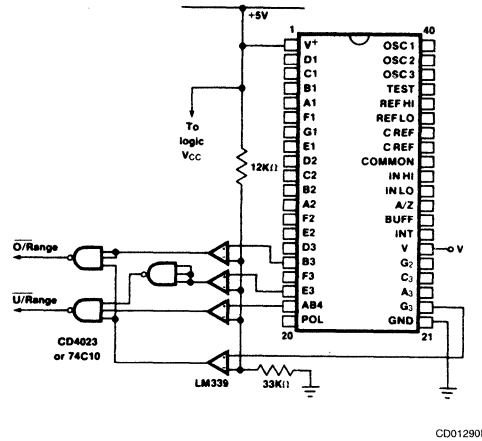


Figure 16: Circuit for developing Underrange and Overrange signals from outputs.

The LM339 is required to ensure logic compatibility with heavy display loading.

Note: All typical values have been guaranteed by characterization and are not tested.

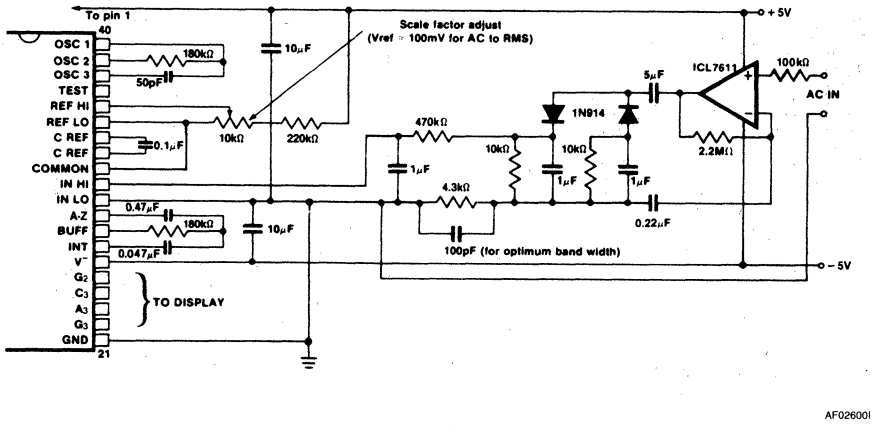


Figure 17: AC to DC Converter with 7137

APPLICATION NOTES

A016 "Selecting A/D converters," by David Fullagar.
A017 "The Integrating A/D Converter," by Lee Evans.
A018 "Do's and Dont's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.
A019 "4½-Digit Panel Meter Demonstrator/ Instrumentation Boards," by Michael Dufort.
A023 "Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort.
A032 "Understanding the Auto-Zero and Common-Mode Behavior of the ICL7106/7/9 Family," by Peter Bradshaw.
A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106," by Larry Goff.
A047 "Games People Play with Intersil's A/D Converters" edited by Peter Bradshaw.
A052 "Tips for Using Single-Chip 3½-Digit A/D Converters," by Dan Watson.

ICL7137 EVALUATION KITS

After purchasing a sample of the 7137, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application.

To facilitate evaluation of this unique circuit, Intersil is offering a kit which contains all the necessary components to build a 3½-digit panel meter. With the ICL7137EV/Kit, an engineer or technician can have the system "up and running" in about half an hour. The kit contains a circuit board, LED display, passive components, and miscellaneous hardware.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8018A/8019A/8020A
4–Bit Expandable Current–Switch

GENERAL DESCRIPTION

The Intersil ICL8018A family are high speed precision current switches for use in current summing digital-to-analog converters. They consist of four logically controlled current switches and a reference device on a single monolithic silicon chip. The reference transistor, combined with precision resistors and an external source, determines the magnitude of the currents to be summed. By weighting the currents in proportion to the binary bit which controls them, the total output current will be proportional to the binary number represented by the input logic levels.

The performance and economy of this family make them ideal for use in digital-to-analog converters for industrial process control and instrumentation systems.

FEATURES

- **TTL Compatible**
- **12 Bit Accuracy**
- **40ns, Switching Speed**
- **Wide Power Supply Range**
- **Low Temperature Coefficient**

APPLICATIONS:

- **D/A and A/D Converters**
- **Digital Threshold Control**
- **Programmable Voltage Source**
- **Meter Drive**
- **X-Y Plotters**

ORDERING INFORMATION

ACCURACY	MILITARY TEMP RANGE CERDIP	COMMERCIAL TEMP RANGE PLASTIC DIP
Individual Devices		
.01%	ICL8018AMJD	ICL8018ACPD
0.1%	ICL8019AMJD	ICL8019ACPD
1.0%	ICL8020AMJD	ICL8020ACPD
Matched Sets*		
.01%	ICL8018AMXJD	ICL8018ACXPD
0.1%	ICL8019AMXJD	ICL8019ACXPD
1.0%	ICL8020AMXJD	ICL8020ACXPD

***NOTE:** Units ordered in equal quantities will be matched such that the V_{BE}'s of the 8019 will be within ±10mV of the 8018 compensating transistor, and the V_{BE}'s of the 8020 will be within ±50mV. The ICL8018-X matched sets consist of one 8018, one 8019, and one 8020. The 8019-X contains one 8019 and one 8020, while the 8020-X contains two 8020's. Units shipped as matched sets will be marked with a unique set number.

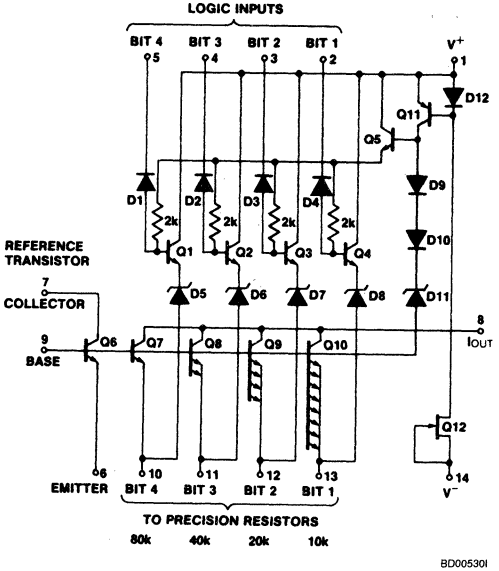


Figure 1: Functional Diagram

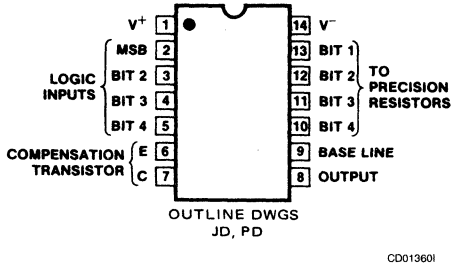


Figure 2: Pin Configuration

302200–002

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8018A/8019A/8020A

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Logic Input Voltage ..... −2V to V^+
$V_{BASELINE}$ ..... V^- to +5V
Output Voltage ..... $V_{BASELINE}$ to +20V
Storage Temperature ..... −65°C to +150°C

Operating Temperature ICL8018AM
ICL8019/20AM ..... −55°C to +125°C
ICL8018/19/20AC ..... 0°C to +70°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS ($4.5V \le V^+ \le 20V$, $V^- = -15V$, $T_A = 25°C$, Voltage @ pin 6 = −5V)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Absolute Error ICL8018A ICL8019A ICL8020A	V_{INHI} = 5.0V V_{INLO} = 0.0V			±.01 ±0.1 ±1	%
Error Temperature Coefficient ICL8018A ICL8019A ICL8020A			±2 ±2 ±2	±5 ±25 ±50	ppm/°C
Settling Time To ±1/2 LSB, $R_L = 1k\Omega$ 8 BIT 12 BIT			100 200		ns
Switching Time To Turn On LSB			40		ns
Output Current (Nominal) BIT 1 (MSB) BIT 2 BIT 3 BIT 4 (LSB)			1.0 0.5 0.25 0.125		mA
Zero Output Current	V_{IN} = 5.0V		10	50	nA
Output Voltage Range		$V_{BASELINE}$ +1V		+10	V
Input Coding-Complementary Binary (See Truth Table) Logic Input Voltage "0" (Switch ON) "1" (Switch OFF)	$\Delta I_{OUT} < 400nA$	 2.0		 0.8	V
Logic Input Current "0" "1" (into device)	V_{IN} = 0V V_{IN} = 5V		−1.0 0.01	−2 0.1	mA μA
Power Supply Rejection V^+ V^-			.005 .0005		%/V
Supply Voltage Range V^+ V^-		4.5 −10	5 −15	20 −20	V
Supply Current (V_{SUPP} = ±20V) I^+ I^-			7 1	10 3	mA

Note: All typical values have been guaranteed by characterization and are not tested.

BASIC D/A THEORY

The majority of digital to analog converters contain the elements shown in Figure 3. The heart of the D/A converter is the logic controlled switching network, whose output is an analog current or voltage proportional to the digital number on the logic inputs. The magnitude of the analog output is determined by the reference supply and the array of precision resistors, see Figure 4. If the switching network has a current output, often a transconductance amplifier is used to provide a voltage output.

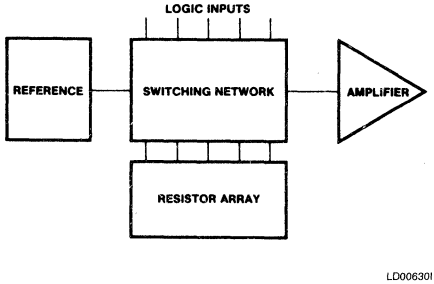


Figure 3: Elements of a D/A Converter

DEFINITION OF TERMS

The **resolution** of a D/A converter refers to the number of logic inputs used to control the analog output. For example, a D/A converter using two quad current sources would be an 8 bit converter. If three quads were used, a 12 bit converter would be formed. Resolution is often stated in terms of one part in, e.g., 256 since the number of controlling bits is related to total number of identifiable levels by the power of 2. The four bit quad has sixteen different levels (see Table 1) each output corresponding to a particular logic input word.

Table 1: ICL8018/19/20 Truth Table

LOGIC INPUT	NOMINAL OUTPUT CURRENT (mA)
0 0 0 0	1.875
0 0 0 1	1.750
0 0 1 0	1.625
0 0 1 1	1.500
0 1 0 0	1.375
0 1 0 1	1.250
0 1 1 0	1.125
0 1 1 1	1.000
1 0 0 0	0.825
1 0 0 1	0.750
1 0 1 0	0.625
1 0 1 1	0.500
1 1 0 0	0.375
1 1 0 1	0.250
1 1 1 0	0.125
1 1 1 1	0.000

Note that **maximum output** of the quad switch is 1 + 1/2 + 1/4 + 1/8 = 1-7/8 = 1.875 mA. If this series of bits were continued as 1/16 + 1/32 + 1/64 . . . . . $1/2^{(n-1)}$, the maximum output limit would approach 2.0 mA. This limiting value is called **full scale output.** The maximum output is always less than the full scale output by one least significant bit, LSB. For a twelve bit system (resolution 1 part in 4096) with a full scale output of 10.0 volts the maximum output would be 4095/4096 x 10V. Since the numbers are extremely close for high resolution systems, the terms are often used interchangeably.

The **accuracy** of a D/A converter is generally taken to mean the largest error of any output level from its nominal value. The accuracy or **absolute error** is often expressed as a **percentage of the full scale output.**

Linearity relates the maximum error in terms of the deviation from the best straight line drawn through all the possible output levels. Linearity is related to accuracy by the scale factor and output offset. If the scale factor is exactly the nominal value and offset is adjusted to zero, then accuracy and linearity are identical. Linearity is usually specified as being within ±1/2 LSB of the best straight line.

Another desirable property of D/A converter is that it be **monotonic.** This simply implies that each successive output level is greater than the preceding one. A possible worst case condition would be when the output changes from most significant bit (MSB) OFF, all other bits ON to the next level which has the MSB ON and all other bits OFF, e.g., 10000 . . . to 01111.

In applications where a quad current switch drives a transconductance amplifier (current to voltage converter), transient response is almost exclusively determined by the output amplifier itself. Where the quad output current drives a resistor to ground, switching time and settling time are useful parameters.

Switching time is the familiar 10% to 90% rise time type of measurement. Low capacitance scope probes must be used to avoid masking the high speeds that current source switching affords. The **settling time** is the elapsed time between the application of a fast input pulse and the time at which the output voltage has settled to or approached its final value within a specified limit of accuracy. This limit of accuracy should be commensurate with the resolution of the DAC to be used.

Typically, the settling time specification describes how soon after an input pulse the output can be relied upon as accurate to within ±1/2 LSB of an N bit converter. Since the 8018A family has been designed with all the collectors of the current switching transistors tied together, the output capacitance is constant. The transient response is, therefore, a simple exponential relationship, and from this the settling time can be calculated and related to the measured rise time as shown in Table 2.

Table 2: Settling Time vs. Rise Time Resistor Load

BITS OF RESOLUTION	±1/2 LSB ERROR % FULL SCALE	NUMBER OF TIME CONSTANTS	NUMBER OF RISE TIMES
8	.2%	6.2	2.8
10	.05%	7.6	3.4
12	.01%	9.2	4.2

Rise Time (10% – 90%) = 2.2 R_L C_{eff}

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8018A/8019A/8020A

DETAILED DESCRIPTION

An example of a practical circuit for the ICL8018A quad current switch is shown in Figure 4. The circuit can be analyzed in two sections; the first generates very accurate currents and the second causes these currents to be switched according to input logic signals. A reference current of 125μA is generated by a stable reference supply and a precision resistor. An op-amp with low offset voltage and low input bias current, such as the ICL8008, is used in conjunction with the internal reference transistor, Q_6, to force the voltage on the common base line, so that the collector current of Q_6 is equal to the reference current. The emitter current of Q_6 will be the sum of the reference current and a small base current causing a drop of slightly greater than 10 volts across the 80kΩ resistor in the emitter of Q_6. Since this resistor is connected to -15V, this puts the emitter of Q_6 at nearly -5V and the common base line at one V_{BE} more positive at -4.35V typically.

Also connected to the common base line are the switched current source transistors Q_7 through Q_{10}. The emitters of these transistors are also connected through weighted precision resistors to -15V and their collector currents summed at pin 8. Since all these transistors, Q_6 through Q_{10}, are designed to have equal emitter-base voltages, it follows that all the emitter resistors will have equal voltage drops across them. It is this constant voltage and the precision resistors at the emitter that determine the exact value of switched output current. The emitter resistor of Q_7 is equal to that of Q_6, therefore, Q_7's collector current will be I_{REF} or 125μA. Q_8 has 40kΩ in the emitter so that its collector current will be twice I_{REF} or 250μA. In the same way, the 20kΩ and 10kΩ in the emitters of Q_9 and Q_{10} contribute 0.5mA and 1mA to the total collector current.

The reference transistor and four current switching transistors are designed for equal emitter current density by making the number of emitters proportional to the current switched.

The remaining circuitry provides switching signals from the logic inputs. In the switch ON mode, zener diodes D_5 through D_8, connected to the emitter of each current switch transistor Q_7 thru Q_{10}, are reverse biased allowing the transistors to operate, producing precision currents summed in the collectors. The transistors are turned off by raising the voltage on the zeners high enough to turn on the zeners and raise the emitters of the switching transistor. This reverse biases the emitter base diode thereby shutting off that transistor's collector current.

The analog output current can be used to drive one load directly, (1kΩ to ground for FS = 1.875V for example) or can be used to drive a transconductance amplifier to give larger output voltages.

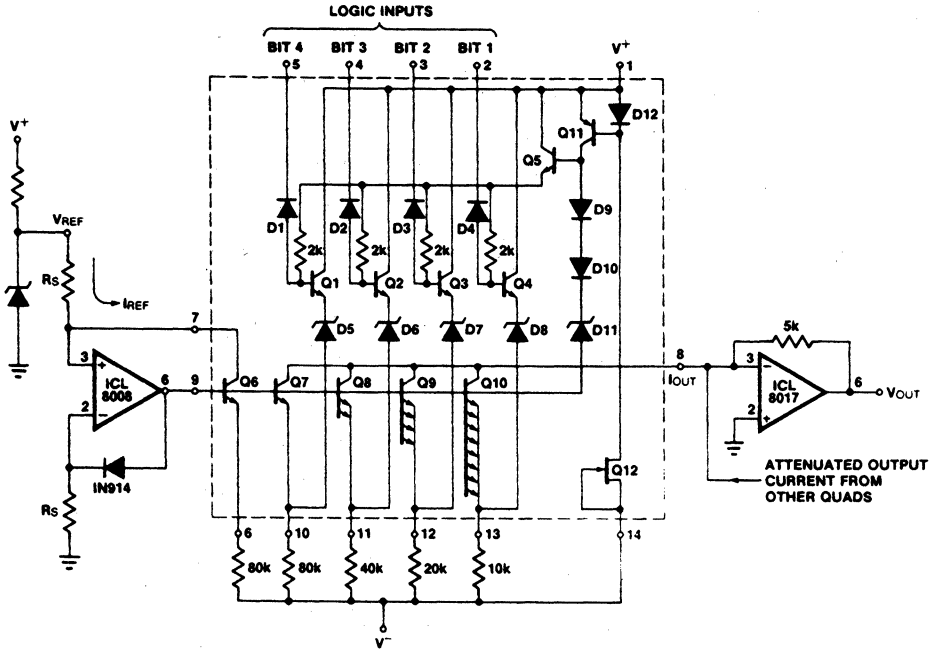


Figure 4: Typical Circuit

Note: All typical values have been guaranteed by characterization and are not tested.

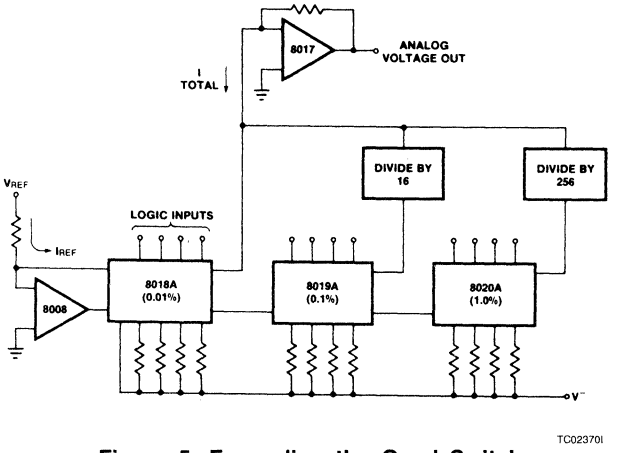


Figure 5: Expanding the Quad Switch

EXPANDING THE QUAD SWITCH

While there are few requirements for only 4 bit D to A converters, the 8018A is readily expanded to 8 and 12 bits with the addition of other quads and resistor dividers as shown in Figure 5.

To maintain the progression of binary weighted bit currents, the current output of the first quad drives the input of the transconductance amplifier directly, while a resistor divider network divides the output current of the second quad by 16 and the output current of the third by 256.

e.g., $I_{Total} = 1 \times (1 + 1/2 + 1/4 + 1/8) + 1/16(1 + 1/2 + 1/4 + 1/8) + 1/256(1 + 1/2 + 1/4 + 1/8)$
$= 1 + 1/2 + 1/4 + 1/8 + 1/16 + 1/32 + 1/64 + 1/128 + 1/256 + 1/512 + 1/1024 + 1/2048.$

Note that each current switch is operating at the same high speed current levels so that standard 10k, 20k, 40k and 80kΩ resistor networks can be used. Another advantage of this technique is that since the current outputs of the second and third quad are attenuated, so are the errors they contribute. This allows the use of less accurate switches and resistor networks in these positions; hence, the three accuracy grades of .01%, 0.1%, and 1% for the 8018A, 8019A and 8020A, respectively. It should be noted that only the reference transistor on the most significant quad is required to set up the voltage on the common base line joining the three sets of switching transistors (Pin 9).

GENERATING REFERENCE CURRENTS — ZENER REFERENCE

As mentioned above, the 8018A switches currents determined by a constant voltage across the external precision resistors in the emitter of each switch. There are several ways of generating this constant voltage. One of the simplest is shown in Figure 6. Here an external zener diode is driven by the same current source line used to bias internal Zener D_{11}.

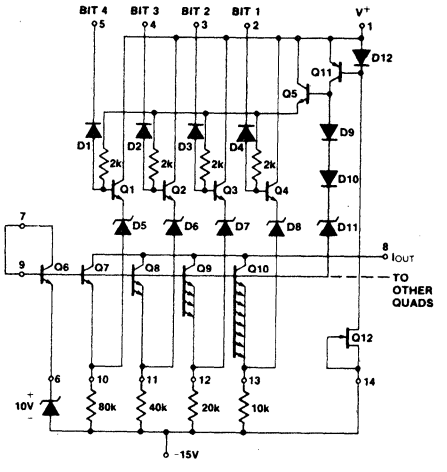


Figure 6: Simple Zener Reference

The zener current will be typically 1 mA per quad. The compensation transistor Q_6 is connected as a diode in series with the external zener. The V_{BE} of this transistor will approximately match the V_{BE}'s of the current switching transistors, thereby forcing the external zener voltage across each of the external resistors. The temperature coefficient of the external zener will dominate the temperature dependence of this scheme, however using a temperature compensated zener minimizes this problem. Since Q_6 is operating at a higher current density than the other switching transistors, the temperature matching of V_{BE}'s is not optimum, but should be adequate for a simple 8 or 10 bit converter.

Note: All typical values have been guaranteed by characterization and are not tested.

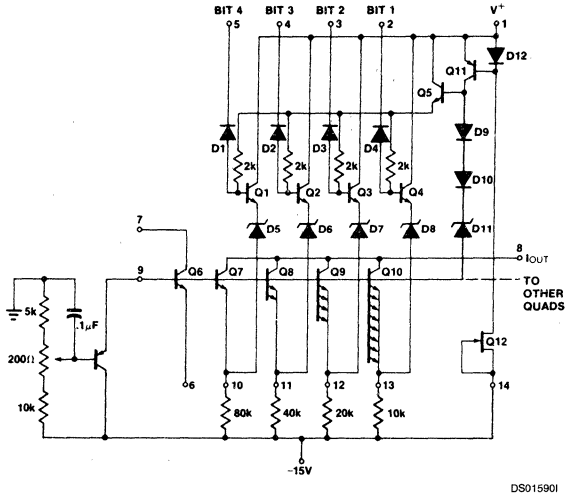


Figure 7: PNP Reference

The 8018A series is tested for accuracy with 10V reference voltage across the precision resistors, implying use of a 10 volt zener. Using a different external zener voltage will only slightly degrade accuracy if the zener voltage is above 5 or 6 volts.

When using other than 10 volt reference, the effects on logic thresholds should also be noted (see logic levels below). Full scale adjustment can be made at the output amplifier.

PNP REFERENCE

Another simple reference scheme is shown in Figure 7. Here an external PNP transistor is used to buffer a resistor divider. In this case, the −15 volt supply is used as a reference. Holding the V^- supply constant is not too difficult since the 8018A is essentially a constant current load. In this scheme, the internal compensation transistor is not necessary, since the V_{BE} matching is provided by the emitter-base junction of the external transistor. A small pot in series with the divider facilitates full scale output adjustment. A capacitor from base to collector of the external PNP will lower output impedance and minimize transient effects.

FULL COMPENSATION REFERENCE

For high accuracy, low drift applications, the reference scheme of Figure 4, offers excellent performance. In this circuit, a high gain op-amp compares two currents. The first is a reference current generated in R_S by the temperature compensated zener and the virtual ground at the non-inverting op-amp input. The second is the collector current of the reference transistor Q_6, provided on the quad switch. The output of the op-amp drives the base of Q_6 keeping its collector current exactly equal to the reference current. Since the switching transistor's emitter current densities are equal and since the precision resistors are proportional, all of the switched collector currents will have the proper value.

The op-amp feedback loop using the internal reference transistor will maintain proper currents in spite of V_{BE} drift, beta drift, resistor drift and changes in V^-. Using this circuit, temperature drifts of 2 ppm/°C are typical. A discrete diode connected as shown will keep Q_6 from saturating and prevent latch up if V^- is disconnected.

In any reference scheme, it is advisable to capacitively decouple the common base line to minimize transient effects. A capacitor, .001μF to .1μF from Pin 9 to analog ground is usually sufficient.

IMPROVED ACCURACY

As a final note on the subject of setting up reference levels, it should be pointed out that the largest contributor of error is the mismatch of V_{BE}'s of the current switching transistors. That is, if all the V_{BE}'s were identical, then all precision resistors would have exactly the same reference voltage across them. A one millivolt mismatch compared with ten volt reference across the precision resistors will cause a .01% error. While decreasing the reference voltage will decrease the accuracy, the voltage can be increased to achieve better than .01% accuracies. The voltage across the emitter resistors can be doubled or tripled with a proportional increase in resistor values resulting in improved absolute accuracy as well as improved temperature drift performance. This technique has been used successfully to implement up to 16 bit D/A converters.

For further information see the following Applications Bulletins.

A016 "Selecting A/D Converters" by Dave Fullagar.
A018 "Do's and Don'ts of Applying A/D Converters" by Peter Bradshaw and Skip Osgood.
A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing" by Ed Sliger.

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8052/ICL7104 and ICL8068/ICL7104

14/16-Bit μP-Compatible 2-Chip A/D Converter

GENERAL DESCRIPTION

The ICL7104, combined with the ICL8052 or ICL8068, forms a member of Intersil's high performance A/D converter family. The ICL7104-16, performs the analog switching and digital function for a 16-bit binary A/D converter, with full three-state output, UART handshake capability, and other outputs for easy interfacing. The ICL7014-14 is a 14-bit version. The analog section, as with all Intersil's integrating converters, provides fully precise Auto-Zero, Auto-Polarity (including ±0 null indication), single reference operation, very high input impedance, true input integration over a constant period for maximum EMI rejection, fully ratiometric operation, over-range indication, and a medium quality built-in reference. The chip pair also offers optional input buffer gain for high sensitivity applications, a built-in clock oscillator, and output signals for providing an external Auto-Zero capability in preconditioning circuitry, synchronizing external multiplexers, etc.

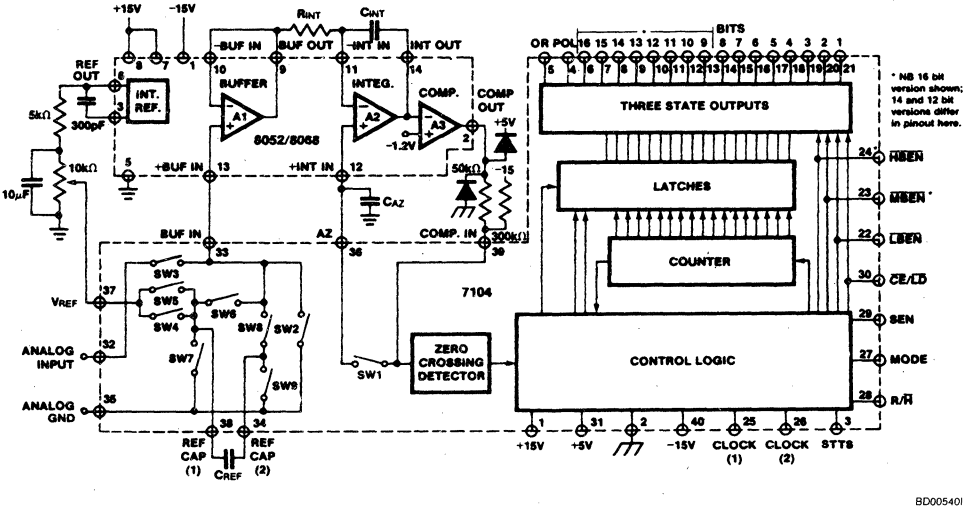
FEATURES

- **16/14 Bit Binary Three-State Latched Outputs Plus Polarity and Overrange**
- **Ideally Suited for Interface to UARTs and Microprocessors**
- **Conversion On Demand or Continuously**
- **Guaranteed Zero Reading for Zero Volts Input**
- **True Polarity at Zero Count for Precise Null Detection**
- **Single Reference Voltage for True Ratiometric Operation**
- **Onboard Clock and Reference**
- **Auto-Zero; Auto-Polarity**
- **Accuracy Guaranteed to 1 Count**
- **All Outputs TTL Compatible**
- **±4V Analog Input Range**
- **Status Signal Available for External Sync, A/Z in Preamp, etc**

ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ICL8052CPD	0°C to +70°C	14-Pin Plastic DIP
ICL8052CDD	0°C to +70°C	14-Pin Ceramic DIP
ICL8052ACPD	0°C to +70°C	14-Pin Plastic DIP
ICL8052ACDD	0°C to +70°C	14-Pin Ceramic DIP
ICL8068CJD	0°C to +70°C	14-Pin CERDIP
ICL8068ACJD	0°C to +70°C	14-Pin CERDIP

PART NUMBER	TEMP. RANGE	PACKAGE
ICL7104-14CJL	0°C to -70°C	40-Pin CERDIP
ICL7104-14CPL	0°C to +70°C	40-Pin Plastic DIP
ICL7104-14CDL	0°C to +70°C	40-Pin Ceramic DIP
ICL7104-16CJL	0°C to +70°C	40-Pin CERDIP
ICL7104-16CPL	0°C to +70°C	40-Pin Plastic DIP
ICL7104-16CDL	0°C to +70°C	40-Pin Ceramic DIP



BD00540I

Figure 1: ICL8052A (8068A)/ICL7104 16/14 Bit A/D Converter Functional Diagram

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8052/ICL7104

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (1) All Devices 500mW
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... 0°C to +70°C
Lead Temperature (Soldering, 10sec) ..... 300°C

ICL8052, 8068

Supply Voltage ..... ±18V
Differential Input Voltage (8068) ..... ±30V
(8052) ..... ±6V
Input Voltage (2) ..... ±15V
Output Short Circuit Duration,
All Outputs (3) ..... Indefinite

ICL7104

V+ Supply (GND to V+) 12V
V++ to V− 32V
Positive Supply Voltage (GND to V++) 17V
Negative Supply Voltage (GND to V−) 17V
Analog Input Voltage (Pins 32−39) (4) ..... V++ to V−
Digital Input Voltage
(Pins 2−30) (5) ..... (GND−0.3V) to (V^+ +0.3V)

Notes:

1: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70°C. For higher temperatures, derate 10mW/°C.

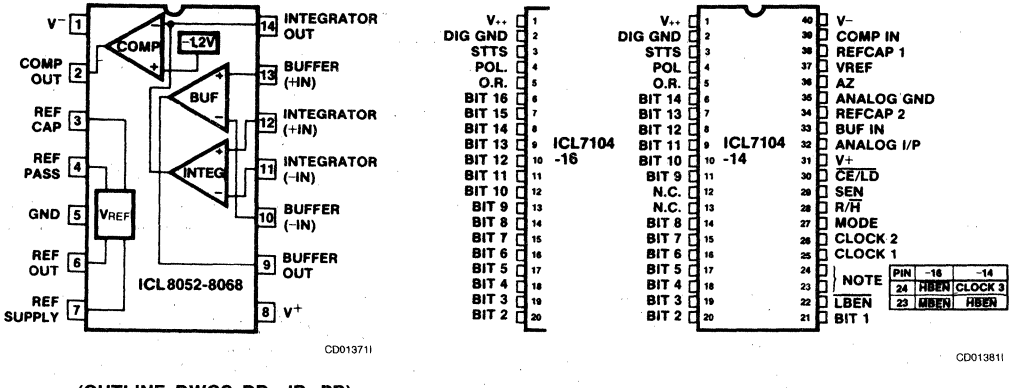
2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

3: Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

4: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.

5: Connecting any digital inputs or outputs to voltages greater than V+ or less than GND may cause destructive device latchup. For this reason it is recommended that no inputs from sources not on the same power supply be applied to the ICL7104 before its power supply is established.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



(OUTLINE DWGS DD, JD, PD)

(OUTLINE DWGS DL, JL, PL)

Figure 2: Pin Configurations

ICL7104 ELECTRICAL CHARACTERISTICS (V+ = +5V, V++ = +15V, V− = −15V, T_A = 25°C)

SYMBOL	CHARACTERISTICS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IN}	Clock Input	CLOCK 1	V_{in} = +5V to 0V	±2	±7	±30	μA
I_{IN}	Comparator I/P	COMP IN (Note 1)	V_{in} = 0V to +5V	−10	±0.001	+10	μA
I_{IH}	Inputs	MODE	V_{IN} = +5V	+1	+5	+30	μA
I_{IL}	with Pulldown		V_{in} = 0V	−10	±0.01	+10	μA
I_{IH}	Inputs	SEN, R/$\overline{H}$	V_{in} = +5V	−10	±0.01	+10	μA
I_{IL}	with Pullups	$\overline{LBEN}$, $\overline{MBEN}$, $\overline{HBEN}$, $\overline{CE/LD}$ (Note 2)	V_{in} = 0V	−30	−5	−1	μA
V_{IH}	Input High Voltage	All Digital Inputs		2.5	2.0	–	V

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8052/ICL7104

INTERSIL

ICL7104 ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	CHARACTERISTICS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input Low Voltage	All Digital Inputs			1.5	1.0	V
V_{OL}	Digital	$\overline{LBEN}$	I_{OL} = 1.6mA	—	0.27	.4	V
V_{OH}	Outputs	$\overline{MBEN}$ (16-only) (Note 3)	I_{OH} = −10μA		4.5	—	V
V_{OH}	Three-Stated	$\overline{HBEN}$	I_{OH} = −240μA	2.4	3.5	—	V
	On	$\overline{CE/LD}$					
		BIT n, POL, OR					
I_{OL}	Digital Outputs Three-Stated Off	BIT n, POL, OR	$0 \le V_{out} \le V+$	−10	±.001	+10	μA
V_{OL}	Non-Three State	STTS	I_{OL} = 3.2mA	—	0.3	.4	V
V_{OH}	Digital		I_{OH} = −400μA	2.4	3.3	—	V
V_{OL}	Output	CLOCK 2	I_{OL} = 320μA		0.5		V
V_{OH}			I_{OH} = −320μA		4.5		V
V_{OL}		CLOCK 3 (−14 ONLY)	I_{OL} = 1.6mA		0.27	.4	V
V_{OH}			I_{OH} = −320μA	2.4	3.5		V
$R_{DS(on)}$		Switch 1		—	25k		Ω
$R_{DS(on)}$		Switches 2,3		—	4k	20k	Ω
$R_{DS(on)}$	Switch	Switches 4,5,6,7,8,9		—	2k	10k	Ω
$I_{D(off)}$		Switch Leakage		—	15		pA
	Clock	Clock Freq. (Note 4)		DC	200	400	kHz
I+	Supply Currents	+5V Supply Current All outputs high impedance	Freq. = 200kHz		200	600	μA
I++		+15V Supply Current	Freq. = 200kHz		.3	1.0	mA
I−		−15V Supply Current	Freq. = 200kHz		25	200	μA
V+	Supply Voltage	Logic Supply	Note 5	4.0		+11.0	V
V++	Range	Positive Supply		+10.0		+16.0	V
V−		Negative Supply		−16.0		−10.0	V

NOTES: 1. This spec applies when not in Auto-Zero phase.
2. Apply only when these pins are inputs, i.e., the mode pin is low, and the 7104 is not in handshake mode.
3. Apply only when these pins are outputs, i.e., the mode pin is high or the 7104 is in handshake mode.
4. Clock circuit shown in Figs. 15 and 16.
5. V+ must not be more positive than V++.

ICL8068 ELECTRICAL CHARACTERISTICS (V_{SUPPLY} = ±15V unless otherwise specified)

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	8068			8068A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
EACH OPERATIONAL AMPLIFIER									
V_{OS}	Input Offset Voltage	V_{CM} = 0V		20	65		20	65	mV
I_{IN}	Input Current (either input) (Note 1)	V_{CM} = 0V		175	250		80	150	pA
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±10V	70	90		70	90		dB
	Non-Linear Component of Common-Mode Rejection Ratio (Note 2)	V_{CM} = ±2V		110			110		dB
A_V	Large Signal Voltage Gain	R_L = 50kΩ	20,000			20,000			V/V
SR	Slew Rate			6			6		V/μs
GBW	Unity Gain Bandwidth			2			2		MHz
I_{SC}	Output Short-Circuit Current			5	10		5	10	mA
COMPARATOR AMPLIFIER									
A_{VOL}	Small-signal Voltage Gain	R_L = 30kΩ		4000					V/V
$+V_O$	Positive Output Voltage Swing		+12	+13		+12	+13		V
$-V_O$	Negative Output Voltage Swing		−2.0	−2.6		−2.0	−2.6		V
VOLTAGE REFERENCE									
V_O	Output Voltage		1.5	1.75	2.0	1.60	1.75	1.90	V
R_O	Output Resistance			5			5		ohms
TC	Temperature Coefficient			50			40		ppm/°C

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8052/ICL7104

ICL8068 ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	8068			8068A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{SUPPLY}	Supply Voltage Range		±10		±16	±10		±16	V
I_{SUPPLY}	Supply Current Total				14		8	14	mA

ICL8052 ELECTRICAL CHARACTERISTICS (V_{SUPPLY} = ±15V unless otherwise specified)

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	8068			8068A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	EACH OPERATIONAL AMPLIFIER								
V_{OS}	Input Offset Voltage	V_{CM} = 0V		20	75		20	75	mV
I_{IN}	Input Current (either input) (Note 1)	V_{CM} = 0V		5	50		2	10	pA
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±10V	70	90		70	90		dB
	Non-Linear Component of Common-Mode Rejection Ratio (Note 2)	V_{CM} = ±2V		110			110		dB
A_V	Large Signal Voltage Gain	R_L = 50kΩ	20,000			20,000			V/V
SR	Slew Rate			6			6		V/μs
GBW	Unity Gain Bandwidth			1			1		MHz
I_{SC}	Output Short-Circuit Current			20	100		20	100	mA
	COMPARATOR AMPLIFIER								
A_{VOL}	Small-signal Voltage Gain	R_L = 30kΩ		4000					V/V
$+V_O$	Positive Output Voltage Swing		+12	+13		+12	+13		V
$-V_O$	Negative Output Voltage Swing		-2.0	-2.6		-2.0	-2.6		V
	VOLTAGE REFERENCE								
V_O	Output Voltage		1.5	1.75	2.0	1.60	1.75	1.90	V
R_O	Output Resistance			5			5		ohms
TC	Temperature Coefficient			50			40		ppm/°C
V_{SUPPLY}	Supply Voltage Range		±10		±16	±10		±16	V
I_{SUPPLY}	Supply Current Total			6	12		6	12	mA

NOTES: 1. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents are measured with junctions at ambient temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + R_{\theta JA}Pd$ where $R_{\theta JA}$ is the thermal resistance from junction to ambient. A heat sink can be used to reduce temperature rise.

2. This is the only component that causes error in dual-slope converter.

SYSTEM ELECTRICAL CHARACTERISTICS: ICL8068/7104 ($V++ = +15V$, $V^+ = +5V$, $V^- = -15V$, Clock Frequency = 200kHz)

CHARACTERISTICS	TEST CONDITIONS	8068A/7104-14			8068A/7104-16			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Zero Input Reading	V_{in} = 0.0V Full Scale = 4.000V	-0.0000	±0.0000	+0.0000	-0.0000	-0.0000	+0.0000	Hexadecimal Reading
Ratiometric Reading (1)	$V_{in} = V_{Ref.}$ Full Scale = 4.000V	1FFF	2000	2001	7FFF	8000	8001	Hexadecimal Reading
Linearity over ±Full Scale (error of reading from best straight line)	$-4V \le V_{in} \le +4V$		0.5	1		0.5	1	LSB
Differential Linearity (difference between worst case step of adjacent counts and ideal step)	$-4V \le V_{in} \le +4V$		.01			.01		LSB
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} = +V_{in} \simeq 4V$		0.5	1		0.5	1	LSB
Noise (P-P value not exceeded 95% of time)	V_{in} = 0V Full scale = 4.000V		2			2		μV
Leakage Current at Input (2)	V_{in} = 0V		100	165		100	165	pA
Zero Reading Drift	V_{in} = 0V 0°C ≤ T_A ≤ 70°C		0.5	2		0.5	2	μV/°C

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8052/ICL7104

INTERSIL

SYSTEM ELECTRICAL CHARACTERISTICS: ICL8068/7104 (CONT.)

CHARACTERISTICS	TEST CONDITIONS	8068A/7104-14			8068A/7104-16			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Scale Factor Temperature (3) Coefficient	V_{in} = +4V 0 ≤ T_A ≤ 50°C (ext. ref. 0ppm/°C		2	5		2	5	ppm/°C

SYSTEM ELECTRICAL CHARACTERISTICS: ICL8052/7104 ($V++ = +15V$, $V^+ = +5V$, $V^- = -15V$, Clock Frequency = 200kHz)

CHARACTERISTICS	TEST CONDITIONS	8052A/7104-14			8052A/7104-16			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Zero Input Reading	V_{in} = 0.0V Full Scale = 4.000V	-0.0000	±0.0000	+0.0000	-0.0000	±0.0000	+0.0000	Hexadecimal Reading
Ratiometric Reading (3)	$V_{in} = V_{Ref.}$ Full Scale = 4.000V	1FFF	2000	2001	7FFF	8000	8001	Hexadecimal Reading
Linearity over ±Full Scale (error of reading from best straight line)	-4V ≤ V_{in} ≤ +4V		0.5	1		0.5	1	LSB
Differential Linearity (difference between worst case step of adjacent counts and ideal step)	-4V ≤ V_{in} ≤ +4V		.01			.01		LSB
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} = +V_{in} \approx 4V$		0.5	1		0.5	1	LSB
Noise (P-P value not exceeded 95% of time)	V_{in} = 0V Full scale = 4.000V		30			30		μV
Leakage Current at Input (2)	V_{in} = 0V		20	30		20	30	pA
Zero Reading Drift	V_{in} = 0V 0° ≤ T_A ≤ 70°C		0.5	2		0.5	2	μV/°C
Scale Factor Temperature Coefficient	V_{in} = +4V 0 ≤ T_A ≤ 70°C (ext. ref. 0ppm/°C		2	5		2	5	ppm/°C

NOTES: 1. Tested with low dielectric absorption integrating capacitor.
2. the input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents are measured with junctions at ambient temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + R_{\theta JA}Pd$ where $R_{\theta JA}$ is the thermal resistance from junction to ambient. A heat sink can be used to reduce temperature rise.
3. The temperature range can be extended to 70°C and beyond if the Auto-Zero and Reference capacitors are increased to absorb the high temperature leakage of the 8068. See note 2 above.

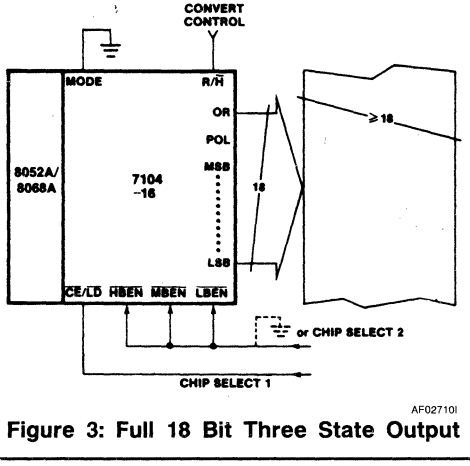


Figure 3: Full 18 Bit Three State Output

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Note: All typical values have been guaranteed by characterization and are not tested.

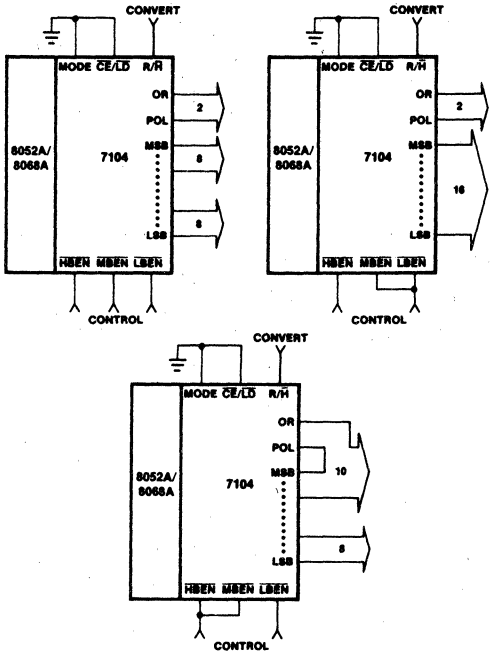


Figure 4: Various Combinations of Byte Disables

AC CHARACTERISTICS ($V++ = +15V$, $V+ = +5V$, $V- = -15V$)

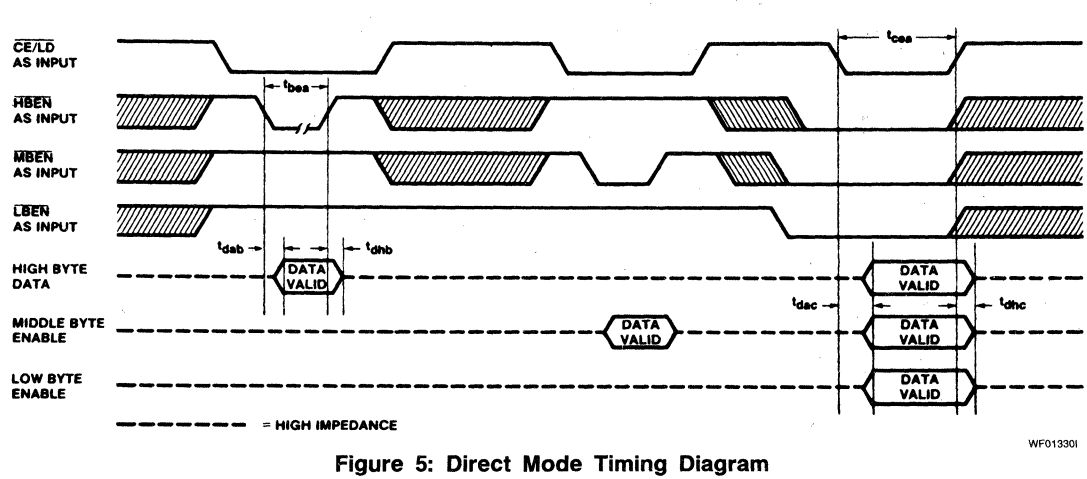


Figure 5: Direct Mode Timing Diagram

Note: All typical values have been guaranteed by characterization and are not tested.

Table 1: Direct Mode Timing Requirements (Note: Not tested in production)

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{bea}	$\overline{XBEN}$ Min. Pulse Width		300		ns
t_{dab}	Data Access Time from $\overline{XBEN}$		300		
t_{dhb}	Data Hold Time from $\overline{XBEN}$		200		
t_{cea}	$\overline{CE/LD}$ Min. Pulse Width		350		
t_{dac}	Data Access Time from $\overline{CE/LD}$		350		
t_{dhc}	Data Hold Time from $\overline{CE/LD}$		280		
t_{cwh}	CLOCK 1 High Time		1000		

Table 2: Handshake Timing Requirements

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{mw}	MODE Pulse (minimum)		20		ns
t_{sm}	MODE pin set-up time		−150		
t_{me}	MODE pin high to low Z $\overline{CE/LD}$ high delay		200		
t_{mb}	MODE pin high to $\overline{XBEN}$ low Z (high) delay		200		
t_{cel}	CLOCK 1 high to $\overline{CE/LD}$ low delay		700		
t_{ceh}	CLOCK 1 high to $\overline{CE/LD}$ high delay		600		
t_{cbl}	CLOCK 1 high to $\overline{XBEN}$ low delay		900		
t_{cbh}	CLOCK 1 high to $\overline{XBEN}$ high delay		700		
t_{cdh}	CLOCK 1 high to data enabled delay		1100		
t_{cdl}	CLOCK 1 low to data disabled delay		1100		
t_{ss}	Send ENable set-up time		−350		
t_{cbz}	CLOCK 1 high to $\overline{XBEN}$ disabled delay		2000		
t_{cez}	CLOCK 1 high to $\overline{CE/LD}$ disabled delay		2000		
t_{cwh}	CLOCK 1 High Time	1250	1000		

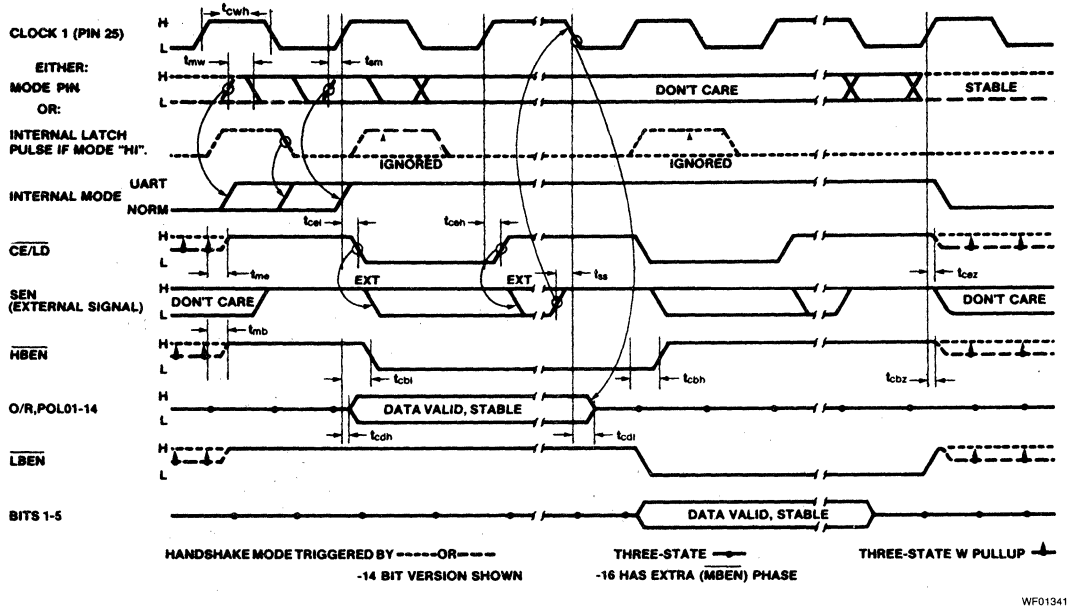


Figure 6: Handshake Mode Timing Diagram

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8052/ICL7104

Table 3: Pin Descriptions

PIN	SYMBOL	OPTION	DESCRIPTION
1	V(++)		Positive Supply Voltage Nominally +15V
2	GND		Digital Ground .0V, ground return
3	STTS		STaTuS output. HI during Integrate and Deintegrate until data is latched. LO when analog section is in Auto-Zero configuration.
4	POL		POLarity. Three-state output. HI for positive input.
5	OR		OverRange. Three-state output.
6	BIT 16 BIT 14	-16 -14	(Most significant bit)
7	BIT 15 BIT 13	-16 -14	Data Bits, Three-state outputs. See Table 4 for format of ENables and bytes. HIGH = true
8	BIT 14 BIT 12	-16 -14	
9	BIT 13 BIT 11	-16 -14	
10	BIT 12 BIT 10	-16 -14	
11	BIT 11 BIT 9	-16 -14	
12	BIT 10 nc	-16 -14	
13	BIT 9 nc	-16 -14	
14	BIT 8		
15	BIT 7		
16	BIT 6		
17	BIT 5		
18	BIT 4		
19	BIT 3		
20	BIT 2		
21	BIT 1		Least significant bit.
22	$\overline{LBEN}$		Low Byte ENable. If not in handshake mode (see pin 27) when LO (with $\overline{CE/LD}$, pin 30) activates low-order byte outputs, BITS 1-8 When in handshake mode (see pin 27), serves as a low-byte flag output. See Figures 12, 13, 14.

PIN	SYMBOL	OPTION	DESCRIPTION
	$\overline{MBEN}$	-16	Mid Byte ENable. Activates BITS 9-16, see $\overline{LBEN}$ (pin 22)
23	$\overline{HBEN}$	-14	High Byte ENable. Activates BITS 9-14, POL, OR, see $\overline{LBEN}$ (pin 22)
	$\overline{HBEN}$	-16	High Byte ENable. Activates POL, OR, see $\overline{LBEN}$ (pin 22).
24	CLOCK3	-14	RC oscillator pin. Can be used as clock output.

PIN	SYMBOL	DESCRIPTION
25	CLOCK1	Clock input. External clock or ocsillator.
26	CLOCK2	Clock output. Crystal or RC oscillator.
27	MODE	Input LO; Direct output mode where $\overline{CE/LD}$, $\overline{HBEN}$, $\overline{MBEN}$ and $\overline{LBEN}$ act as inputs directly controlling byte outputs. If pulsed HI causes immediate entry into handshake mode (see Figure 14). If HI, enables $\overline{CE/LD}$, $\overline{HBEN}$, $\overline{MBEN}$, and $\overline{LBEN}$ as outputs. Handshake mode will be entered and data output as in Figures 12 & 13 at conversion completion.
28	R/$\overline{H}$	Run/$\overline{Hold}$: Input HI-conversions continously performed every 2^{17}(-16) or 2^{15}(-14) clock pulses. Input LO-conversion in progress completed, converter will stop in Auto-Zero 7 counts before input integrate.
29	SEN	Send-ENable: Input controls timing of byte transmission in handshake mode. HI indicates 'send'.
30	$\overline{CE/LD}$	$\overline{Chip\text{-}Enable/LoaD}$. With MODE (pin 27) LO, $\overline{CE/LD}$ serves as a master output enable; when HI, the bit outputs and POL, OR are disabled. With MODE HI, pin serves as a $\overline{LoaD}$ strobe (-ve going) used in handshake mode. See Figures 12 & 13.
31	V(+)	Positive Logic Supply Voltage. Nominally +5V.
32	AN,IN	ANalog INput. High side.
33	BUF IN	BUFfer INput to analog chip (ICL8052 or ICL8068)
34	REFCAP2	REFerence CAPacitor (negative side)
35	AN.GND.	ANalog GrouND. Input low side and reference low side.
36	A-Z	Auto-Zero node.
37	VREF	Voltage REFerence input (positive side).
38	REFCAP1	REFerence CAPacitor (positive side).
39	COMP-IN	COMParator INput from 8052/8068
40	V(-)	Negative Supply Voltage. Nominally -15V.

Note: All typical values have been guaranteed by characterization and are not tested.

Table 4: Three-State Byte Formats and $\overline{EN}$able Pins

	$\overline{CE/LD}$															
	$\overline{HBEN}$		$\overline{MBEN}$							$\overline{LBEN}$						
7104-16	POL	O/R	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
			$\overline{HBEN}$								$\overline{LBEN}$							
7104-14		POL	O/R	B14	B13	B12	B11	B10	B9		B8	B7	B6	B5	B4	B3	B2	B1

Figure 1 shows the functional block diagram of the operating system. For a detailed explanation, refer to Figure 7 below.

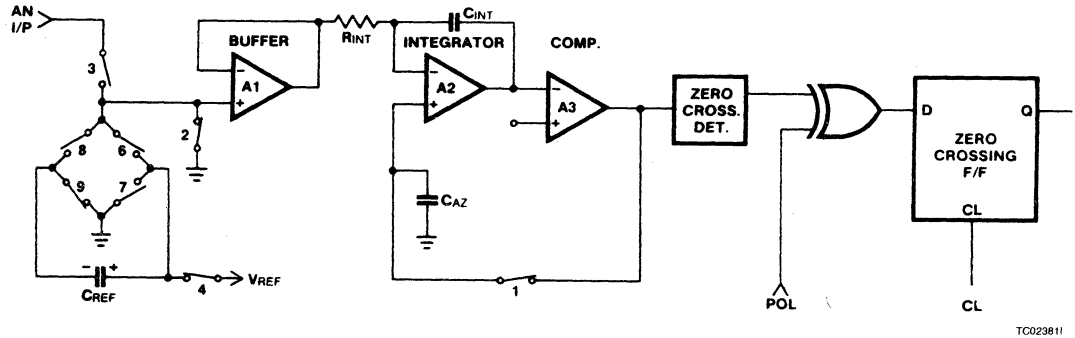


Figure 7A: Phase I Auto-Zero

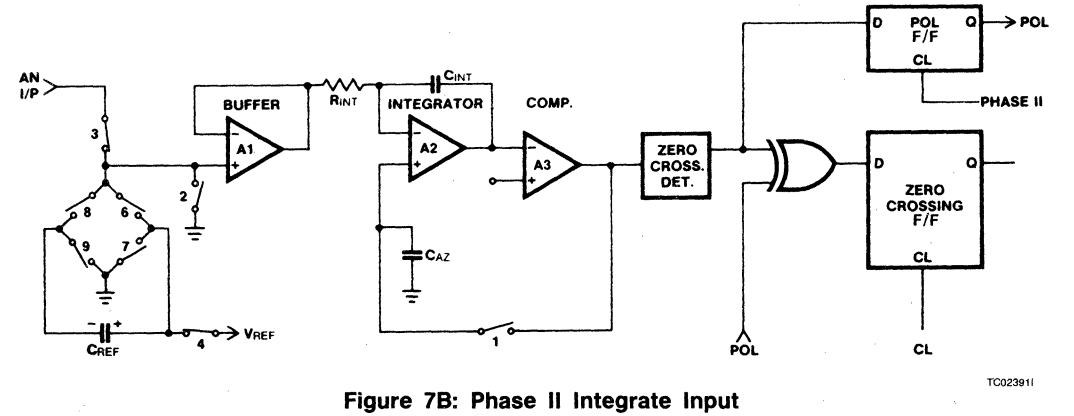


Figure 7B: Phase II Integrate Input

DETAILED DESCRIPTION

Analog Section

Figure 7 shows the equivalent Circuit of the Analog Section of both the ICL7104/8052 and the ICL7104/8068 in the 3 different phases of operation. If the Run/$\overline{Hold}$ pin is left open or tied to V+, the system will perform conversions at a rate determined by the clock frequency: 131,072 for — 16 and 32,368 for — 14 clock periods per cycle (see Figure 9 conversion timing).

Auto-Zero Phase I Figure 7A

During Auto-Zero, the input of the buffer is shorted to analog ground thru switch 2, and switch 1 closes a loop around the integrator and comparator. The purpose of the loop is to charge the Auto-Zero capacitor until the integrator output no longer changes with time. Also, switches 4 and 9 recharge the reference capacitor to V_{REF}.

Note: All typical values have been guaranteed by characterization and are not tested.

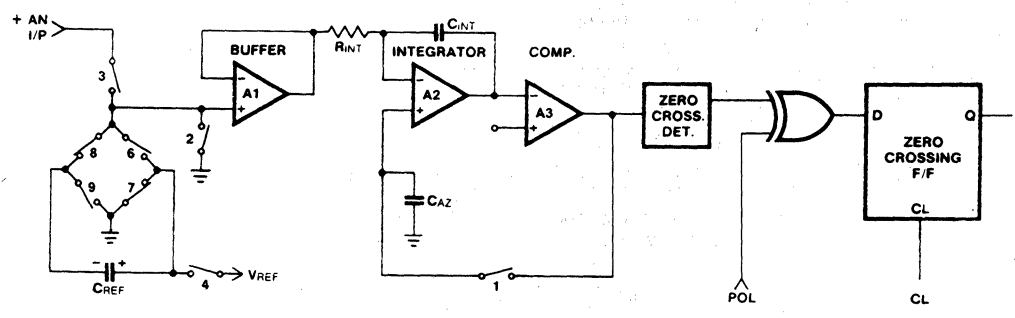


Figure 7C: Phase III + Deintegrate

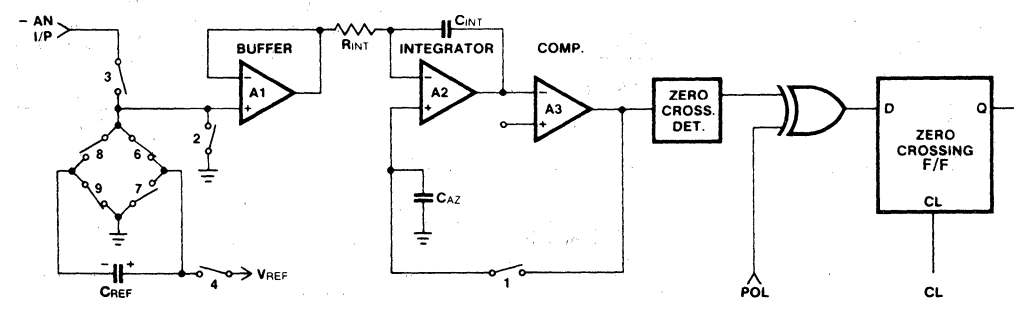


Figure 7D: Phase III – Deintegrate

Input Integrate Phase II Figure 7B

During input integrate the Auto-Zero loop is opened and the analog input is connected to the buffer input thru switch 3. (The reference capacitor is still being charged to V_{REF} during this time.) If the input signal is zero, the buffer, integrator and comparator will see the same voltage that existed in the previous state (Auto-Zero). Thus the integrator output will not change but will remain stationary during the entire Input Integrate cycle. If V_{IN} is not equal to zero, an unbalanced condition exists compared to the Auto-Zero phase, and the integrator will generate a ramp whose slope is proportional to V_{IN}. At the end of this phase, the sign of the ramp is latched into the polarity F/F.

Deintegrate Phase III Figure 7C & D

During the Deintegrate phase, the switch drive logic uses the output of the polarity F/F in determining whether to close switches 6 and 9 or 7 and 8. If the input signal was positive, switches 7 and 8 are closed and a voltage which is V_{REF} more negative than during Auto-Zero is impressed on the buffer input. Negative inputs will cause $+V_{REF}$ to be applied to the buffer input via switches 6 and 9. Thus, the reference capacitor generates the equivalent of a (+) reference or a (−) reference from the single reference voltage with negligible error. The reference voltage returns the output of the integrator to the zero-crossing point established in Phase I. The time, or number of counts, required to do this is proportional to the input voltage. Since the Deintegrate phase can be twice as long as the Input integrate phase, the input voltage required to give a full scale reading = $2V_{REF}$.

Note: Once a zero crossing is detected, the system automatically reverts to Auto-Zero phase for the leftover Deintegrate time (unless Run/$\overline{\text{Hold}}$ is manipulated, see Run/$\overline{\text{Hold}}$ Input in detailed description, digital section).

Buffer Gain

At the end of the auto-zero interval, the instantaneous noise voltage on the auto-zero capacitor is stored, and subtracts from the input voltage while adding to the reference voltage during the next cycle. The result is that this noise voltage effectively is somewhat greater than the input noise voltage of the buffer itself during integration. By introducing some voltage gain into the buffer, the effect of the auto-zero noise (referred to the input) can be reduced to the level of the inherent buffer noise. This generally occurs with a buffer gain of between 3 and 10. Further increase in buffer gain merely increases the total offset to be handled by the auto-zero loop, and reduces the available buffer and integrator swings, without improving the noise performance of the system. The circuit recommended for doing this with the ICL8068/ICL7104 is shown in Figure 8. With careful layout, the circuit shown can achieve effective input noise voltages on the order of 1 to 2 μV, allowing full 16-bit use

Note: All typical values have been guaranteed by characterization and are not tested.

with full scale inputs of as low as 150mV. Note that at this level, thermoelectric EMFs between PC boards, IC pins, etc., due to local temperature changes can be very troublesome. For further discussion, see App. Note A030.

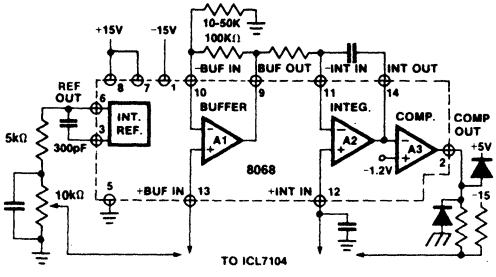
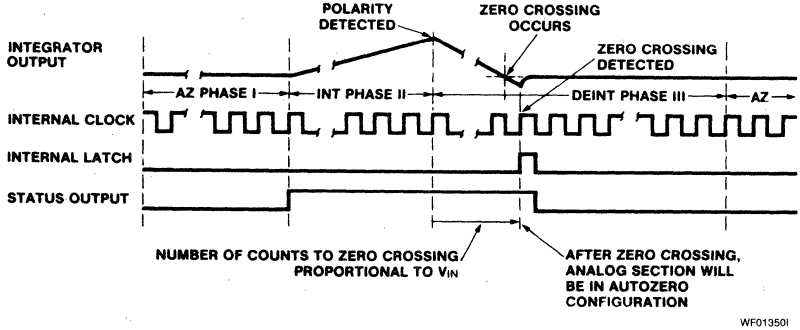


Figure 8: Adding Buffer Gain to ICL8068

Table 5: Typical Component Values ($V++ = +15V$, $V+ = 5V$, $V^- = -15V$, Clock Freq = 200kHz)

ICL8052/8068 WITH	ICL7104-16			ICL7104-14		UNIT
Full scale V_{IN}	200	800	4000	100	4000	mV
Buffer Gain	10	1	1	10	1	V/V
R_{INT}	100	43	200	47	180	kΩ
C_{INT}	.33	.33	.33	0.1	0.1	μF
C_{AZ}	1.0	1.0	1.0	1.0	1.0	μF
C_{ref}	10	1.0	1.0	10	1.0	μF
V_{REF}	100	400	2000	50	2000	mV
Resolution	3.1	12	61	6.1	244	μV



COUNTS			
	PHASE I	PHASE II	PHASE III
-16	32768	32768	65536
-14	8192	8192	16384

Figure 9: Conversion Timing

Note: All typical values have been guaranteed by characterization and are not tested.

ICL8052/ICL7104

ICL8052 vs ICL8068

The ICL8052 offers significantly lower input leakage currents than the ICL8068, and may be found preferable in systems with high input impedances. However, the ICL8068 has substantially lower noise voltage, and for systems where system noise is a limiting factor, particularly in low signal level conditions, will give better performance.

COMPONENT VALUE SELECTION

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

Integrating Resistor

The integrating resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. This current should be small compared to the output short circuit current such that thermal effects are kept to a minimum and linearity is not affected. Values of 5 to 40μA give good results with a nominal of 20μA. The exact value may be chosen by

$$R_{INT} = \frac{\text{full scale voltage}^*}{20\mu A}$$

*Note: If gain is used in the buffer amplifier then —

$$R_{INT} = \frac{\text{(Buffer gain) (full scale voltage)}}{20\mu A}$$

Integrating Capacitor

The product of integrating resistor and capacitor is selected to give 9 volt swing for full scale inputs. This is a compromise between possibly saturating the integrator (at +14 volts) due to tolerance build-up between the resistor, capacitor and clock and the errors a lower voltage swing could induce due to offsets referred to the output of the comparator. In general, the value of C_{INT} is given by

$$C_{INT} = \frac{\begin{bmatrix}\text{(32768 for } -16\text{)} \\ \text{(8192 for } -14\text{)}\end{bmatrix} \times 20\mu A \times \text{clock period}}{\text{Integrator Output Voltage Swing}}$$

A very important characteristic of the integrating capacitor is that it have low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference.

This ratiometric condition should read half scale (100 . . . 000) and any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

Auto-Zero and Reference Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system, a large capacitor giving less noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

Note: When gain is used in the buffer amplifier the reference capacitor should be substantially larger than the auto-zero capacitor. As a rule of thumb, the reference capacitor should be approximately the gain times the value of the auto-zero capacitor. The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

Reference Voltage

The analog input required to generate a full scale output is $V_{IN} = 2\ V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. The resolution of the ICL7104 at 16 bits is one part in 65536, or 15.26ppm. Thus, if the reference has a temperature coefficient of 50ppm/°C (on board reference) a temperature change of 1/3°C will introduce a one-bit absolute error. For this reason, it is recommended that an external high quality reference be used where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made.

DETAILED DESCRIPTION

Digital Section

The digital section includes the clock oscillator circuit, a 16 or 14 bit binary counter with output latches and TTL-compatible three-state output drivers, polarity, over-range and control logic and UART handshake logic, as shown in the Block Diagram Figure 10 (16 bit version shown).

Throughout this description, logic levels will be referred to as "low" or "high". The actual logic levels are defined under "ICL7104 Electrical Characteristics". For minimum power consumption, all inputs should swing from GND (low) to V^+ (high). Inputs driven from TTL gates should have 3–5kΩ pullup resistors added for maximum noise immunity.

MODE Input

The MODE input is used to control the output mode of the converter. When the MODE pin is connected to GND or left open (this input is provided with a pulldown resistor to ensure a low level when the pin is left open), the converter is in its "Direct" output mode, where the output data is directly accessible under the control of the chip and byte enable inputs. When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in three bytes for the 7104-16 or two bytes for the 7104-14 then returns to "direct" mode. When the MODE input is left high, the converter will output data in the handshake mode at the end of every conversion cycle. (See section entitled "Handshake Mode" for further details).

STaTuS Output

During a conversion cycle, the STaTuS output goes high at the beginning of Input Integrate (Phase II), and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Figure 9 for details of this timing. This signal may be used as a "data valid" flag (data never changes while STaTuS is low) to drive interrupts, or for monitoring the status of the converter.

Note: All typical values have been guaranteed by characterization and are not tested.

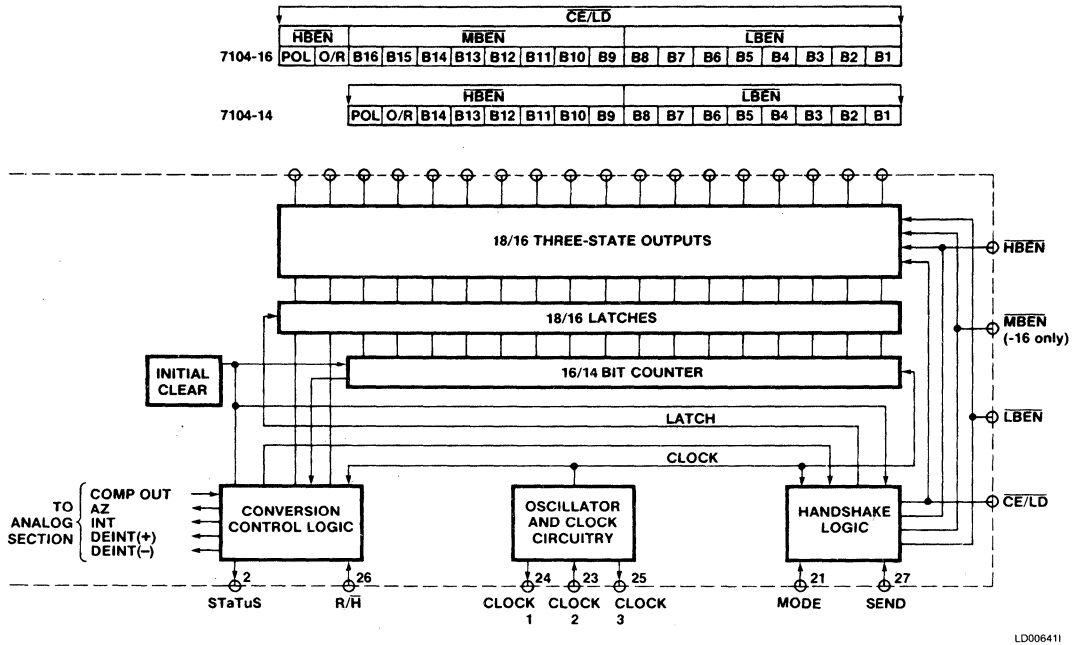


Figure 10: Digital Section

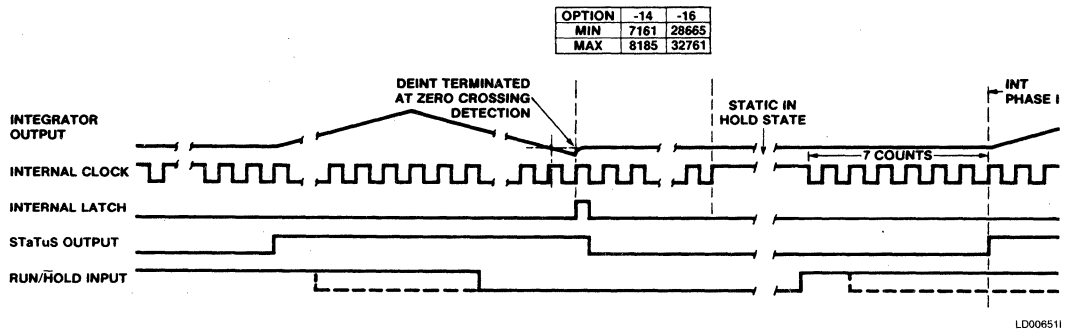


Figure 11: Run/Hold Operation

Run/Hold Input

When the Run/Hold input is connected to V^+ or left open (this input has a pullup resistor to ensure a high level when the pin is left open), the circuit will continuously perform conversion cycles, updating the output latches at the end of every Deintegrate (Phase III) portion of the conversion cycle (See Figure 9). (See under "Handshake Mode" for exception.) In this mode of operation, the conversion cycle will be performed in 131,072 for 7104-16 and 32768 for 7104-14 clock periods, regardless of the resulting value.

If Run/Hold goes low at any time during Deintegrate (Phase III) after the zero crossing has occurred, the circuit will immediately terminate Deintegrate and jump to Auto-Zero. This feature can be used to eliminate the time spent in Deintegrate after the zero-crossing. If Run/Hold stays or goes low, the converter will ensure a minimum Auto-Zero time, and then wait in Auto-Zero until the Run/Hold input goes high. The converter will begin the Integrate (Phase II) portion of the next conversion (and the STaTuS output will go high) seven clock periods after the high level is detected at Run/Hold. See Figure 11 for details.

Note: All typical values have been guaranteed by characterization and are not tested.

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Using the Run/$\overline{\text{Hold}}$ input in this manner allows an easy "convert on demand" interface to be used. The converter may be held at idle in Auto-Zero with Run/$\overline{\text{Hold}}$ low. When Run/$\overline{\text{Hold}}$ goes high the conversion is started, and when the STaTuS output goes low the new data is valid (or transferred) to the UART — see Handshake Mode). Run/$\overline{\text{Hold}}$ may now go low terminating Deintegrate and ensuring a minimum Auto-Zero time before stopping to wait for the next conversion. Alternately, Run/$\overline{\text{Hold}}$ can be used to minimize conversion time by ensuring that it goes low during Deintegrate, after zero crossing, and goes high after the hold point is reached. The required activity on the Run/$\overline{\text{Hold}}$ input can be provided by connecting it to the CLOCK3 (-14), CLOCK2 (-16) Output. In this mode the conversion time is dependent on the input value measured. Also refer to Intersil Application Bulletin A030 for a discussion of the effects this will have on Auto-Zero performance.

If the Run/$\overline{\text{Hold}}$ input goes low and stays low during Auto-Zero (Phase I), the converter will simply stop at the end of Auto-Zero and wait for Run/$\overline{\text{Hold}}$ to go high. As above, Integrate (Phase II) begins seven clock periods after the high level is detected.

Direct Mode

When the MODE pin is left at a low level, the data outputs [bits 1 through 8 low order byte, see Table 4 for format of middle (-16) and high order bytes] are accessible under control of the byte and chip ENable terminals as inputs. These $\overline{\text{ENable}}$ inputs are all active low, and are provided with pullup resistors to ensure an inactive high level when left open. When the chip $\overline{\text{ENable}}$ input is low, taking a byte $\overline{\text{ENable}}$ input low will allow the outputs of that byte to become active (three-stated on). This allows a variety of parallel data accessing techniques to be used. The timing requirements for these outputs are shown under AC Characteristics and Table 1.

It should be noted that these control inputs are asynchronous with respect to the converter clock — the data may be accessed at any time. Thus it is possible to access the data while it is being updated, which could lead to scrambled data. Synchronizing the access of data with the conversion cycle by monitoring the STaTuS output will prevent this. Data is never updated while STaTuS is low. Also note the potential bus conflict described under "Initial Clear Circuitry".

Handshake Mode

The handshake output mode is provided as an alternative means of interfacing the ICL7104 to digital systems, where the A/D converter becomes active in controlling the flow of data instead of passively responding to chip and byte $\overline{\text{ENable}}$ inputs. This mode is specifically designed to allow a direct interface between the ICL7104 and industry-standard UARTs (such as the Intersil CMOS UARTs, IM6402/3) with no external logic required. When triggered into the handshake mode, the ICL7104 provides all the control and flag signals necessary to sequence the three (ICL7106-16) or two (ICL7104-14) bytes of data into the UART and initiate their transmission in serial form. This greatly eases the task and reduces the cost of designing remote data acquisition stations using serial data transmission to minimize the number of lines to the central controlling processor.

Entry into the handshake mode will occur if either of two conditions are fulfilled; first, if new data is latched (i.e. a conversion is completed) while MODE pin (pin 27) is high, in which case entry occurs at the end of the latch cycle; or secondly, if the MODE pin goes from low to high, when entry will occur immediately (if new data is being latched, entry is delayed to the end of the latch cycle). While in the handshake mode, data latching is inhibited, and the MODE pin is ignored. (Note that conversion cycles will continue in the normal manner). This allows versatile initiation of handshake operation without danger of false data generation; if the MODE pin is held high, every conversion (other than those completed during handshake operations) will start a new handshake operation, while if the MODE pin is pulsed high, handshake operations can be obtained "on demand."

When the converter enters the handshake mode, or when the MODE input is high, the chip and byte $\overline{\text{ENable}}$ terminals become TTL-compatible outputs which provide the control signals for the output cycle. The Send $\overline{\text{ENable}}$ pin (SEN) (pin 29) is used as an indication of the ability of the external device to receive data. The condition of the line is sensed once every clock pulse, and if it is high, the next (or first) byte is enabled on the next rising CLOCK 1 (pin 25) clock edge, the corresponding byte $\overline{\text{ENable}}$ line goes low, and the Chip $\overline{\text{ENable}}$/LoaD pin (pin 30) (CE/LD) goes low for one full clock pulse only, returning high.

On the next falling CLOCK 1 clock pulse edge, if SEN remains high, or after it goes high again, the byte output lines will be put in the high impedance state (or three-stated off). One half pulse later, the byte $\overline{\text{ENable}}$ pin will be cleared high, and (unless finished) the $\overline{\text{CE}}/\overline{\text{LD}}$ and the next byte $\overline{\text{ENable}}$ pin will go low. This will continue until all three (2 in the case of the 14 bit device) bytes have been sent. The bytes are individually put into the low impedance state i.e.: three-stated on during most of the time that their byte $\overline{\text{ENable}}$ pin is (active) low. When receipt of the last byte has been acknowledged by a high SEN, the handshake mode will be cleared, re-enabling data latching from conversions, and recognizing the condition of the MODE pin again. The byte and chip ENable will be three-stated off, if MODE is low, but held high by their (weak) pullups. These timing relationships are illustrated in Figure 12, 13, and 14, and Table 2.

Figure 12 shows the sequence of the output cycle with SEN held high. The handshake mode (Internal MODE high) is entered after the data latch pulse (since MODE remains high the $\overline{\text{CE}}/\overline{\text{LD}}$, $\overline{\text{LBEN}}$, $\overline{\text{MBEN}}$ and $\overline{\text{HBEN}}$ terminals are active as outputs). The high level at the SEN input is sensed on the same high to low internal clock edge. On the next to high internal clock edge, the $\overline{\text{CE}}/\overline{\text{LD}}$ and the $\overline{\text{HBEN}}$ outputs assume a low level and the high-order byte (POL and OR, and except for -16, Bits 9–14) outputs are enabled. The $\overline{\text{CE}}/\overline{\text{LD}}$ output remains low for one full internal clock period only, the data outputs remain active for 1-1/2 internal clock periods, and the high byte $\overline{\text{ENable}}$ remains low for two clock periods. Thus the $\overline{\text{CE}}/\overline{\text{LD}}$ output low level or low to high edge may be used as a synchronizing signal to ensure valid data, and the byte $\overline{\text{ENable}}$ as an output may be used as a byte identification flag. With SEN remaining high the converter completes the output cycle using $\overline{\text{CE}}/\overline{\text{LD}}$, $\overline{\text{MBEN}}$ and $\overline{\text{LBEN}}$ while the remaining byte outputs (see Table 4) are activated. The handshake mode is terminated when all bytes are sent (3 for -16, 2 for -14).

Note: All typical values have been guaranteed by characterization and are not tested.

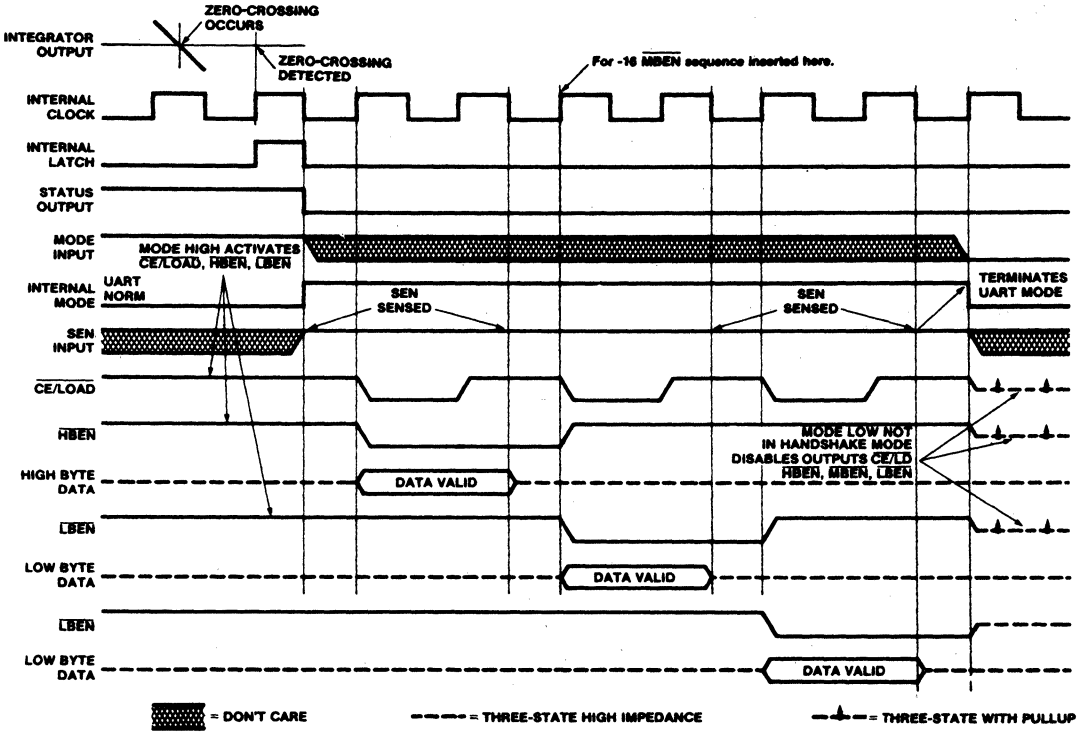

Figure 12: Handshake with SEN Held Positive

Note: All typical values have been guaranteed by characterization and are not tested.

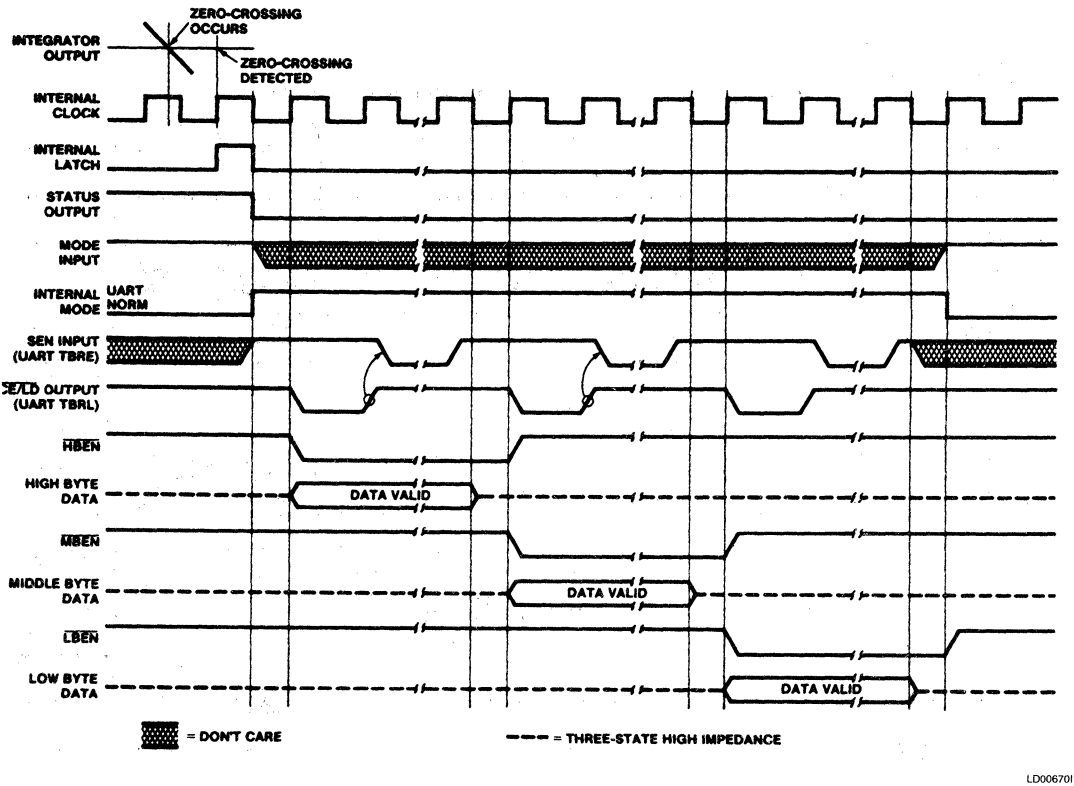

Figure 13: Handshake — Typical UART Interface Timing

Figure 13 shows an output sequence where the SEN input is used to delay portions of the sequence, or handshake, to ensure correct data transfer. This timing diagram shows the relationships that occur using an industry-standard IM6402/3 CMOS UART to interface to serial data channels. In this interface, the SEN input to the ICL7104 is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the $\overline{CE}/\overline{LD}$ terminal of the ICL7104 drives the TBRL (Transmitter Buffer Register Load) input to the UART. The data outputs are paralleled into the eight Transmitter Buffer Register inputs.

Assuming the UART Transmitter Buffer Register is empty, the SEN input will be high when the handshake mode is entered after new data is stored. The $\overline{CE}/\overline{LD}$ and $\overline{HBEN}$ terminals will go low after SEN is sensed, and the high order byte outputs become active. When $\overline{CE}/\overline{LD}$ goes high at the end of one clock period, the high order byte data is clocked into the UART Transmitter Buffer Register. The UART TBRE output will now go low, which halts the output cycle with the $\overline{HBEN}$ output low, and the high order byte outputs active. When the UART has transferred the data to the Transmitter Register and cleared the Transmitter Buffer Register, the TBRE returns high. On the next ICL7104 internal clock high to low edge, the high order byte outputs are disabled, and one-half internal clock later, the $\overline{HBEN}$ output returns high. At the same time, the $\overline{CE}/\overline{LD}$ and $\overline{MBEN}$ (-16) or $\overline{LBEN}$ outputs go low, and the corresponding byte outputs become active. Similarly, when the $\overline{CE}/\overline{LD}$ returns high at the end of one clock period, the enabled data is clocked into the UART Transmitter Buffer Register, and TBRE again goes low. When TBRE returns to a high it will be sensed on the next ICL7104 internal clock high to low edge, disabling the data outputs. For the 16 bit device, the sequence is repeated for $\overline{LBEN}$. One-half internal clock later, the handshake mode will be cleared, and the chip and byte $\overline{EN}$able terminals return high and stay active (as long as MODE stays high).

Note: All typical values have been guaranteed by characterization and are not tested.

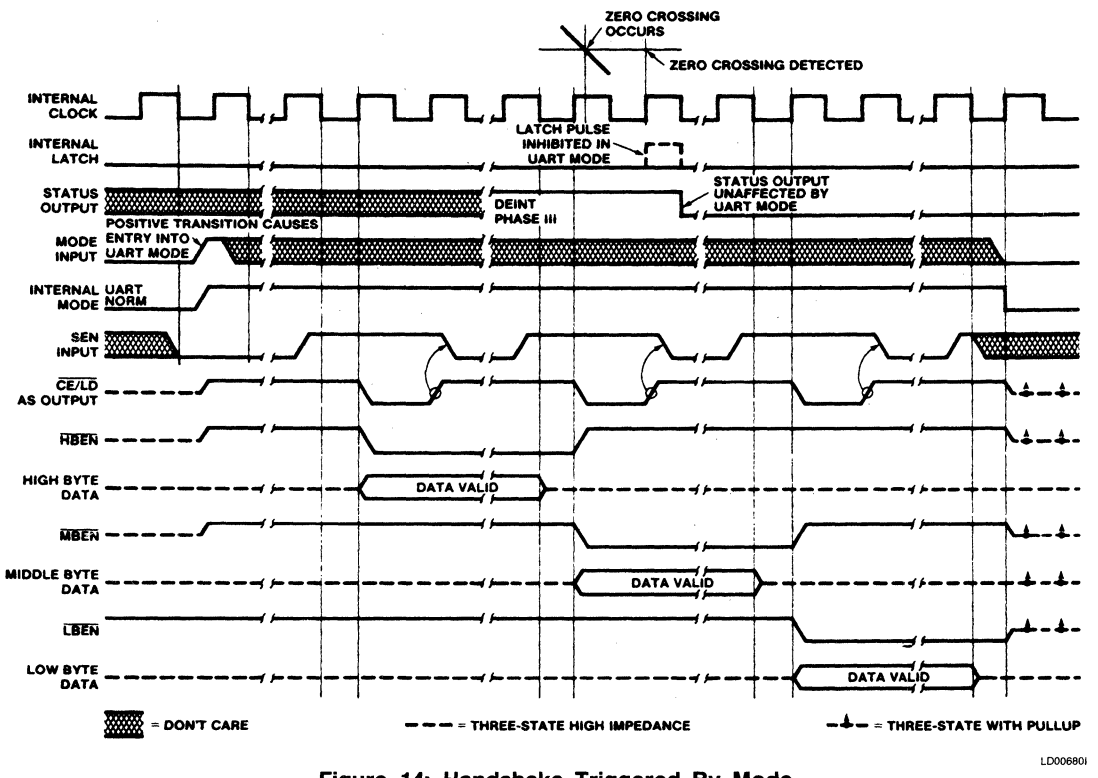

Figure 14: Handshake Triggered By Mode

With the MODE input remaining high as in these examples, the converter will output the results of every conversion except those completed during a handshake operation. By triggering the converter into handshake mode with a low to high edge on the MODE input, handshake output sequences may be performed on demand. Figure 14 shows a handshake output sequence triggered by such an edge. In addition, the SEN input is shown as being low when the converter enters handshake mode. In this case, the whole output sequence is controlled by the SEN input, and the sequence for the first (high order) byte is similar to the sequence for the other bytes. This diagram also shows the output sequence taking longer than a conversion cycle. Note that the converter still makes conversions, with the STaTuS output and Run/Hold input functioning normally. The only difference is that new data will not be latched when in handshake mode, and is therefore lost.

Initial Clear Circuitry

The internal logic of the 7104 is supplied by an internal regulator between V ++ and Digital Ground. The regulator includes a low-voltage detector that will clear various registers. This is intended to ensure that on initial power-up, the control logic comes up in Auto-Zero, with the 2nd, 3rd, and 4th MSB bits cleared, and the "mode" F/F cleared (i.e. in "direct" mode). This, however, will also clear these registers if the supply voltage "glitches" to a low enough value. Additionally, if the supply voltage comes up too fast, this clear pulse may be too narrow for reliable clearing. In general, this is not a problem, but if the UART internal "MODE" F/F should come up set, the byte and chip ENable lines will become active outputs. In many systems this could lead to bus conflicts, especially in non-handshake systems. In any case, SEN should be high (held high for non-handshake systems) to ensure that the MODE F/F will be cleared as fast as possible (see Figure 12 for timing). For these and other reasons, adequate supply bypass is recommended.

Oscillator

The ICL7104-14 is provided with a versatile three terminal oscillator to generate the internal clock. The oscillator may be overdriven, or may be operated as an RC or crystal oscillator.

Figure 15 shows the oscillator configured for RC operation. The internal clock will be of the same frequency and phase as the voltage on the CLOCK 3 pin. The resistor and capacitor should be connected as shown. The circuit will oscillate at a frequency given by f = .45/RC. A 50–100kΩ resistor is recommended for useful ranges of frequency. For optimum 60Hz line rejection, the capacitor value should be

Note: All typical values have been guaranteed by characterization and are not tested.

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chosen such that 32768 (-16), 8192 (-14) clock periods is close to an integral multiple of the 60Hz period.

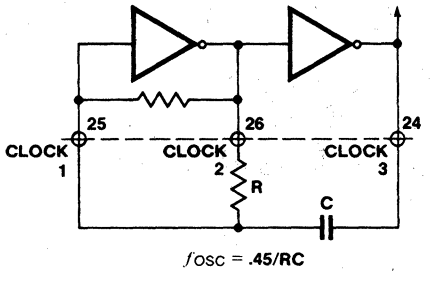


Figure 15: RC Oscillator

Note that CLOCK 3 has the same output drive as the bit outputs.

As a result of pin count limitations, the ICL7104-16 has only CLOCK 1 and CLOCK 2 available, and cannot be used as an RC oscillator. The internal clock will correspond to the inverse of the signal on CLOCK 2. Figure 16 shows a crystal oscillator circuit, which can be used with both 7104 versions. If an external clock is to be used, it should be applied to CLOCK 1. The internal clock will correspond to the signal applied to this pin.

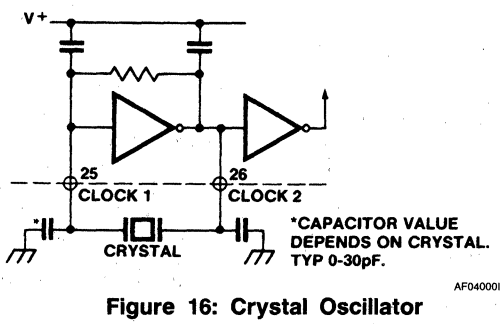


Figure 16: Crystal Oscillator

POWER SUPPLY SEQUENCING

Because of the nature of the CMOS process used to fabricate the ICL7104, and the multiple power supplies used, there are certain conditions of these supplies under which a disabling and potentially damaging SCR action can occur. All of these conditions involve the V+ supply (nom. +5V) being more positive than the V++ supply. If there is any possibility of this occuring during start-up, shut down, under transient conditions during operation, or when inserting a PC board into a "hot" socket, etc., a diode should be placed between V^+ and V++ to prevent it. A germanium or Schottky rectifier diode would be best, but in most cases a silicon rectifier diode is adequate.

ANALOG AND DIGITAL GROUNDS

Extreme care must be taken to avoid ground loops in the layout of ICL8068 or ICL8052/7104 circuits, especially in 16-bit and high sensitivity circuits. It is most important that return currents from digital loads are not fed into the analog ground line. A recommended connection sequence for the ground lines is shown in Figure 17.

APPLICATIONS INFORMATION

Some applications bulletins that may be found useful are listed here:

A016 "Selecting A/D Converters", by Dave Fullagar
A017 "The Integrating A/D Converter", by Lee Evans
A018 "Do's and Dont's of Applying A/D Converters", by Peter Bradshaw and Skip Osgood
A025 "Building a Remote Data Logging Station", by Peter Bradshaw
A030 "The ICL7104 — A Binary Output A/D Converter for Microprocessors", by Peter Bradshaw
R005 "Interfacing Data Converter & Microprocessors", by Peter Bradshaw et al, Electronics, Dec. 9, 1976.

Note: All typical values have been guaranteed by characterization and are not tested.

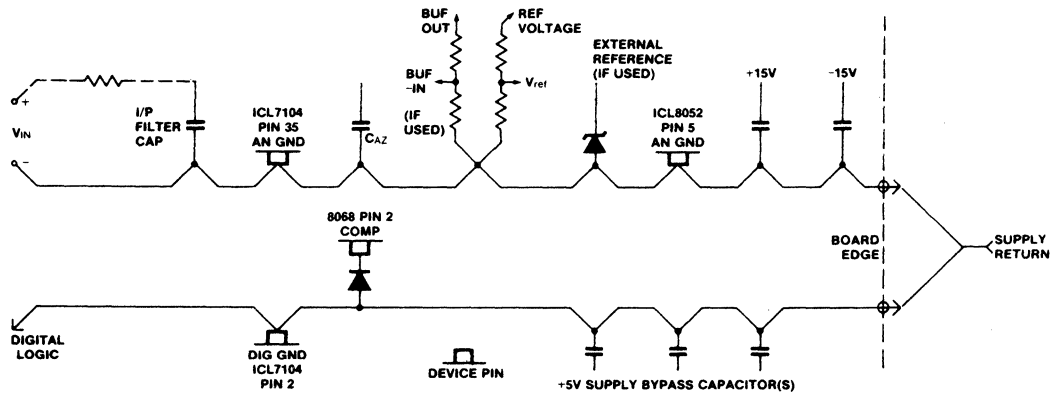


Figure 17: Grounding Sequence

Note: All typical values have been guaranteed by characterization and are not tested.

Section 7 — Timer/Counter Circuits

ICM7206
CMOS Touch-Tone Encoder

GENERAL DESCRIPTION

The Intersil ICM7206/A/B/C/D are 2-of-8 sine wave tone encoders for use in telephone dialing systems. Each circuit contains a high frequency oscillator, two separate programmable dividers, a D/A converter, and a high level output driver.

FEATURES

- **Low Cost**
- **Oscillator Uses 3.58MHz Color TV Crystal**
- **High Current Bipolar Output Driver**
- **Low Output Harmonic Distortion**
- **Wide Operating Supply Voltage Range: 3 to 6 Volts**
- **Uses 3 x 4 or 4 x 4 Single Contact Keypad**
- **Low Power (≤ 5.5mW With A 5.5V Supply)**
- **Single and Dual Tone Capabilities**
- **Multiple Key Lockout**
- **Disable Output: Provides Output Switch Function Whenever A Key Is Pressed**
- **Custom Options Available**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7206IPE	−40°C to +85°C	16 Pin PLASTIC DIP
ICM7206AIPE	−40°C to +85°C	16 Pin PLASTIC DIP
ICM7206BIPE	−40°C to +85°C	16 Pin PLASTIC DIP
ICM7206CIPE	−40°C to +85°C	16 Pin PLASTIC DIP
ICM7206DIPE	−40°C to +85°C	16 Pin PLASTIC DIP
ICM7206/D	−40°C to +85°C	DICE
ICM7206A/D	−40°C to +85°C	DICE
ICM7206B/D	−40°C to +85°C	DICE
ICM7206C/D	−40°C to +85°C	DICE
ICM7206D/D	−40°C to +85°C	DICE

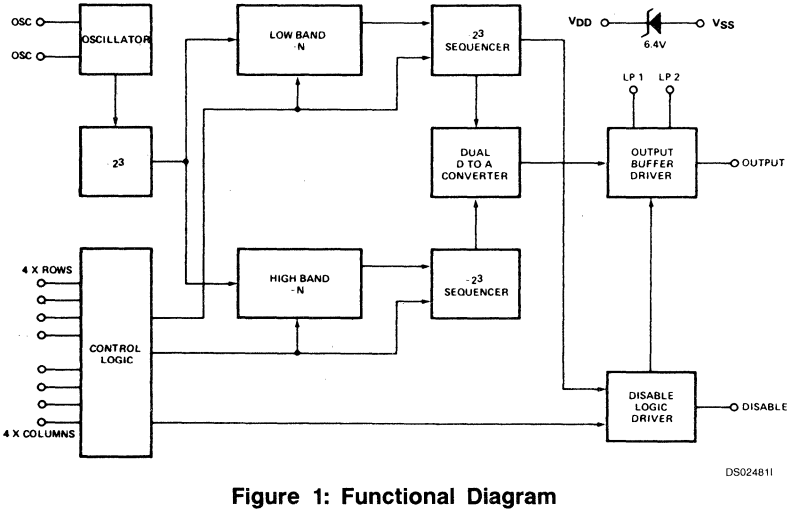


Figure 1: Functional Diagram

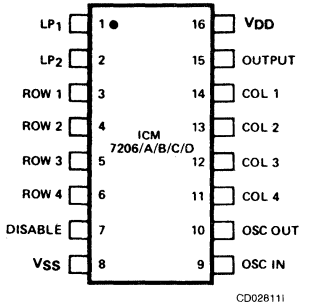


Figure 2: Pin Configuration (Outline Dwg PE)

202100-002

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7206

INTERSIL

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage $V_{DD}-V_{SS}$ (Note 2) 6.0V
Supply Current V_{SS} (terminal 8) 25mA
Supply Current V_{DD} (terminal 16) 40mA
Disable Output Voltage (term. 7) ..... (V_{DD} – 6V) to V_{DD}
Output Voltage (term 15) ..... (V_{SS} – 1.0V) to (V_{DD} + 5.0V)
Input Voltage ..... V_{SS} – 0.3V to V_{DD} + 0.3V

Output Current (terminal 15) 25mA
Power Dissipation 300mW
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE 1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. The ICM7206 family has a zener diode connected between V_{DD} and V_{SS} having a breakdown voltage between 6.2 and 7.0 volts. If the currents into terminals 8 and 16 are limited to 25 and 40mA maximum respectively, the supply voltage may be increased above 6 volts to zener voltage. With no such current limiting, the supply voltage must not exceed 6 volts.

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: V_{DD} = 5.5V, Test Circuit, V_{SS} = 0V T_A = 25°C unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD}	Supply Current	R_L disconnected			450	1000	μA
V_{SUPPLY}	Guaranteed Operating Supply Voltage Range (Note 3)	$-40°C \le T_A \le +85°C$		3.0		6.0	V
V_{OUT}	Peak to Peak Output Voltage	C_1, C_2 disconnected — Low Band		0.90	1.15	1.45	V
		R_L = 1kΩ, no filtering — High Band		1.10	1.40	1.70	V
	RMS Output Voltage	R_L = 1kΩ, f_{OUT} = 697Hz	C_2 Only		480		mV
			C_1 to C_2		480		mV
			No filtering		490		mV
		R_L = 1kΩ, f_{OUT} = 1633Hz	C_1		490		mV
			C_1 to C_2		580		mV
			No filtering		655		mV
	Skew Between High and Low Band Output Voltages	R_L = 1kΩ, C_1, C_2 disconnected			2.5	3.0	dB
Z_O	Output Impedance	R_L = 1kΩ	Operating		90	200	Ω
			Quiescent		25		kΩ
THD1	Total Output Harmonic Distortion	Either Hi or Low Bands			20	25	%
		No Low Pass Filtering					%
THD2	Total Output Harmonic Distortion	R_L = 1kΩ, C_1 = .002μF	f_{OUT} = 697Hz		2.3	10	%
		C_2 = 0.02μF	f_{OUT} = 1633Hz		1.0	10	%
V_{OH}	Maximum Output Voltage Level	R_L = 1kΩ				4.6	V
V_{OL}	Minimum Output Voltage Level	R_L = 1kΩ		0.5			V
R_{IN}	Keyboard Input Pullup Resistors	Terminals 3,4,5,6,11,12,13,14		35	100	150	kΩ
C_{IN}	Keyboard Input Capacitance	Terminals 3,4,5,6,11,12,13,14				5	pF
f_{OSC}	Guaranteed Oscillator Fequency Range (Note 4)	$3 \le (V_{DD} - V_{SS}) \le 6V$		2.0		4.5	MHz
	Guaranteed Oscillator Frequency Range	$4V \le (V_{DD} - V_{SS}) \le 6V$		2.0		7	MHz
t_{on}	System Startup Time on Application of Power	ICM7206, ICM7206A			10		ms
	System Startup Time on Application of Power and Key Depressed Simultaneously	ICM7206B, ICM7206C, ICM7206D				7	ms
R_D	DISABLE Output Saturation Resistance (ON STATE)	See Logic Table for Input Conditions Current = 4mA			330	700	Ω
I_{OLK}	DISABLE Output Leakage (OFF STATE)	See Logic Table for Input Conditions				10	μA
C_{OSC}	Oscillator Load Capacitance	Measured between terminals 9 & 10, no supply voltage applied to circuit $-40°C \le T_A \le 85°C$			7		pF

Note: All typical values have been guaranteed by characterization and are not tested.

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_O	Guaranteed Output Frequency Tolerance	Any output frequency Crystal tolerance ±60ppm Crystal load capacitance CL = 30pF			±0.75	%
t_{start}	Oscillator Startup Time ICM7206B,C,D	$V_{DD} - V_{SS}$ = 3V (Note 5)			7	ms

NOTES: **3.** Operation above 6 volts must employ supply current limiting. Refer to 'ABSOLUTE MAXIMUM RATINGS' and the Application Notes for further information.
4. The ICM7206 family uses dynamic high frequency circuitry in the initial 2^3 divider resulting in low power dissipation and excellent performance over a restricted frequency range. Thus, for reliable operation with a 6 volt supply an oscillator frequency of not less than 2MHz must be used.
5. After row input is enabled.

TRUTH TABLE

LINE	ROWS(1) ACTIVATED	COLS(2) ACTIVATED	OUTPUT (TERMINAL #15)	DISABLE (TERMINAL #7)	COMMENTS
1	0	0	Off	Off	Quiescent State
2	1	1	$f_{row} + f_{col}$	On	Dual Tone
3	1	2 or 3 (incl. col #4)	f_{row}	On	Single Tone
4	2 or 3	1	f_{col}	On	Single Tone
5	2 or 3	2 or 3 (excl. col #3)	D.C. Level	On	No Tone
6	1	4 or 3 (must excl. col #4)	f_{row}, 50% Duty Cycle	f_{row}, 50% Duty Cycle	f_{row} Test
7	4	1	f_{col}, 50% Duty Cycle	f_{col}, 50% Duty Cycle	f_{col} Test
8	0	1 or 2 or 3 or 4	Off	Off	n/a*
9	1	0	902Hz + f_{row}	On	n/a*
10	2 or 3	0	902Hz	On	n/a*
11	4	0	902Hz, 50% Duty Cycle	902Hz, 50% Duty Cycle	n/a*
12	2 or 3 or 4	4	D.C. Level	Indeterminate	Multiple Key Lockout
13	4	2 or 3 or 4	D.C. Level	Indeterminate	Multiple Key Lockout

*n/a — not applicable to telephone calling.
NOTES: **1.** Rows are activated for the ICM7206/C by connecting to a negative supply voltage with respect to V_{DD} (terminal 16) at least 33% of the value of the supply voltage ($V_{DD} - V_{SS}$). For the ICM7206A rows (and columns) are activated by connecting to a positive supply voltage with respect to V_{SS} (terminal 8) at least 33% of the value of the supply voltage ($V_{DD} - V_{SS}$). The rows and columns of the ICM7206B are activated by connecting to a negative supply voltage.
2. Columns (ICM7206) are activated by being connected to a positive supply voltage with respect to V_{SS} (terminal 8) at least 33% of the value of the supply voltage ($V_{DD} - V_{SS}$).

OPTIONS

(For additional information consult the factory)

Options can be achieved using metal mask additions to provide the following.

1) The sequence or position of either the row or column terminals can be interchanged i.e., row 1 terminal 3 could become terminal 11, etc.
2) Any frequency oscillator from approximately 0.5MHz to 7MHz can be chosen. Note that the accuracy of the output frequencies will depend on the exact oscillator frequency. For instance, a 1MHz crystal could be used with worst case output frequency error of 0.8%. Or, if high accuracy is required, ±0.25%, oscillator frequencies of 5,117,376Hz or 2,558,688Hz could be selected. ROM's are used to program the dividers.
3) The 'DISABLE' output may be changed to an inverter or an uncommitted drain n-channel transistor.
4) The oscillator may be disabled until a key is depressed.

COMMENTS

All combinations of row and column activations are given in the truth table. Lines 1 through 7 and 12, 13 represent conditions obtainable with a matrix keyboard. Lines 8 thru 11 are given only for completeness and are not pertinent to telephone dialing.

Lines 6 and 7 show conditions for generating 50% duty cycle full amplitude signals useful for rapid testing of the row and column frequencies on automatic test equipment. In all other cases, output frequencies on terminal 15 are single or dual 4 level synthesized sine waves.

A 'DC LEVEL' on terminal 15 may be any voltage level between approximately 1.2 and 4.3 volts with respect to V_{SS} (terminal 8) for a 5.5 volt supply voltage.

The impedance of the OUTPUT (terminal 15) is approximately 20k ohms in the OFF state. The 'DISABLE OUT-OUT' ON and OFF conditions are defined in the TYPICAL PERFORMANCE CHARACTERISTICS.

Note: All typical values have been guaranteed by characterization and are not tested.

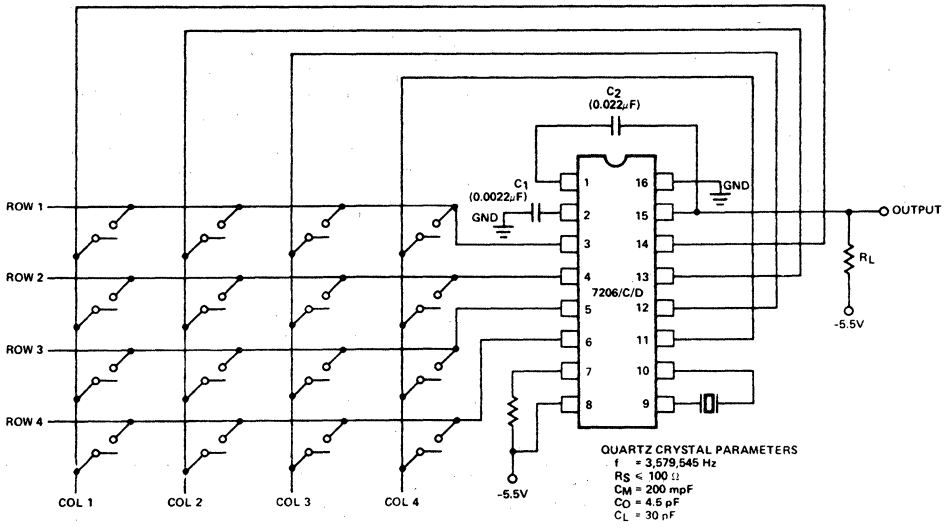
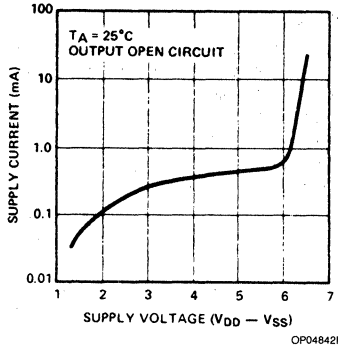


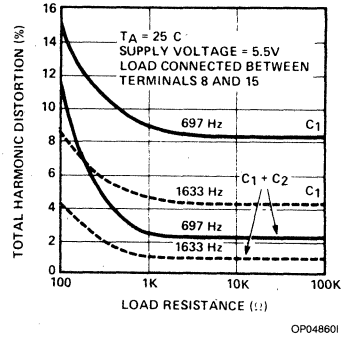
Figure 3: Test Circuit (single contact keyboard devices shown)

TYPICAL PERFORMANCE CHARACTERISTICS

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



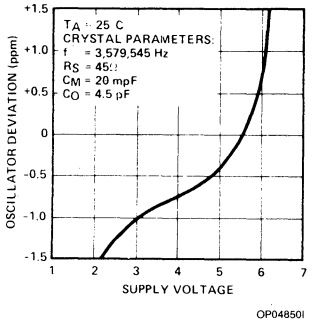
TOTAL HARMONIC DISTORTION AS A FUNCTION OF LOAD RESISTANCE



Note: All typical values have been guaranteed by characterization and are not tested.

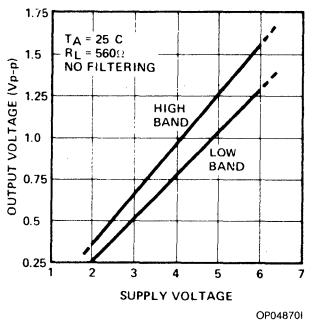
TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

OSCILLATOR FREQUENCY DEVIATION AS A FUNCTION OF SUPPLY VOLTAGE

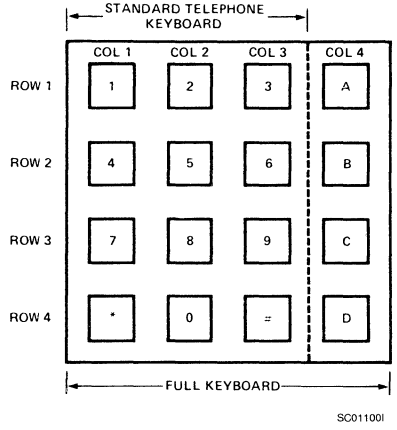


OP04850I

PEAK TO PEAK OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



OP04870I



SC011001

KEY	LOW BAND FREQ. Hz	HI BAND FREQ. Hz
1	697	1209
2	697	1336
3	697	1477
4	770	1209
5	770	1336
6	770	1477
7	852	1209
8	852	1336
9	852	1477
*	941	1209
0	941	1336
#	941	1477
A	697	1633
B	770	1633
C	852	1633
D	941	1633

Figure 4: Keyboard Frequencies

DETAILED DESCRIPTION

The reference frequency is generated from a fully integrated oscillator requiring only a 3.58MHz color TV crystal. This frequency is divided by 8 and is then gated into two divide by N counters (possible division ratios 1 through 128) which provide the correct division ratios for the upper and lower band of frequencies. The outputs from these two divide by N counters are further divided by 8 to provide the time sequencing for a 4 voltage level synthesis of each sinewave. Both sinewaves are added and buffered to a high current output driver, with provisions made for up to two external capacitors for low pass filtering, if desired. Typically, the total output harmonic distortion is 20% with no L.P. filtering and it may be reduced to typically less than 5% with filtering. The output drive level of the tone pairs will be approximately −3dBV into a 900 ohm termination. The skew between the high and low groups is typically 2.5 dB without low pass filtering.

The 7206 uses either a 3 x 4 or 4 x 4 single contact keyboard; the oscillator will run whenever the power is applied, and the DISABLE output consists of a p-channel open drain FET whose source is connected to V_{DD}.

The 7206A can also use a 3 x 4 or 4 x 4 keyboard, but requires a double contact type with the common line tied to V_{DD}. The oscillator will be on whenever power is applied; the DISABLE output consists of a p-channel open drain FET; its source is connected to V_{DD}.

The 7206B requires a 4 + 4 double contact keyboard with the common line tied to V_{SS}. The oscillator will be on only during the time that a ROW is enabled, and the DISABLE

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7206

output consists of an n-channel open drain FET with its source tied to V_{SS}.

The 7206C uses either a 3 x 4 or 4 x 4 single contact keyboard; the oscillator will be on only during the time that a key is depressed. The DISABLE output consists of an n-channel open drain FET with its source tied to V_{SS}.

The 7206D uses a single contact 3 x 4 or 4 x 4 keyboard. The oscillator will be on only during the time that a key is depressed. DISABLE output consists of a p-channel open drain FET with its source tied to V_{DD}.

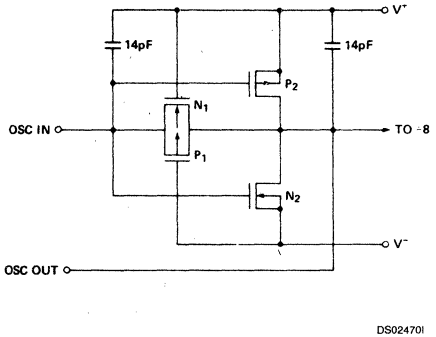


Figure 5: Schematic Diagram ICM7206 Oscillator

Figure 6 shows individual currents of a low band and high band frequency pair into the summing node A (see Figure 7) and the resultant voltage waveform.

DESIRED FREQUENCY Hz	ACTUAL FREQUENCY Hz	FREQUENCY DEVIATION %	DIVIDE BY N RATIO
697	699.13	+0.30	80
770	766.17	−0.50	73
852	847.43	−0.54	66
941	947.97	+0.74	59
1209	1215.88	+0.57	46
1336	1331.68	−0.32	42
1477	1471.85	−0.35	38
1633	1645.01	+0.74	34

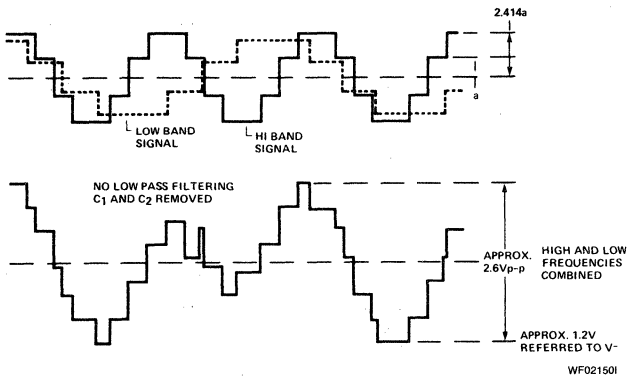


Figure 6

Note: All typical values have been guaranteed by characterization and are not tested.

APPLICATION NOTES

Device Description

The ICM7206 family is manufactured with a standard metal gate CMOS technology having proven reliability and excellent reproducability resulting in extremely high yields. The techniques used in the design have been developed over many years and are characterized by wide operating supply voltage ranges and low power dissipation.

To minimize chip size, all diffusions used to define source-drain regions and field regions are butted up together. This results in approximately 6.3 volt zener breakdown between the supply terminals, and between all components on chip. As a consequence, the usual CMOS static charge problems and handling problems are not experienced with the ICM7206.

The oscillator consists of a medium size CMOS inverter having on chip a feedback resistor and two capacitors of 14pF each, one at the oscillator input and the other at the oscillator output. The oscillator is followed by a dynamic $\div 2^3$ circuit which divides the oscillator frequency to 447, 443Hz. This is applied to two programmable dividers each capable of division ratios of any integer between 1 and 128, and each counter is controlled by a ROM. The outputs from the programmable counters drive sequencers (divide by 8) which generate the eight time slots necessary to synthesize the 4-level sine waves.

The control logic block recognizes signals on the row and column inputs that are only a small fraction of the supply voltage, thereby permitting the use of a simple matrix single contact per key keyboard, rather than the more usual two contacts per key type having a common line. The row and column pullup resistors are equal in value and connected to the opposite supply terminals (ICM7206/C only; for the ICM7206A all pullup resistors are connected to the V_{SS} terminal and for the ICM7206B they are tied to the V_{DD}. Therefore, connecting a row input to a column input generates a voltage on those inputs which is one half of the supply voltage.

The ICM7206 family employs a unique but extremely simple digital to analog (D to A) converter. This D to A converter produces a 4 level synthesized sine wave having an intrinsic total harmonic distortion level of approximately 20%. Figure 8 shows a single channel D to A converter. The current sources Q_2 and Q_3 are proportioned in the ratio of 1:1.414. During time slots 1 and 8 both S_1 and S_2 are off, during time slots 2 and 7 only S_1 is on, during time slots 3 and 6 only S_2 is on, and during time slots 4 and 5 both S_1 and S_2 are on. The resultant currents are summed at node A, buffered by Q_4 and further buffered by R_3, R_4 and Q_5. Switch S_3 allows the output to go into a high impedance mode under quiescent conditions.

Node A is the common summing point for both the high and low band frequencies although this is not shown in Figure 8.

The synthesized sine wave has negligible even harmonic distortion and very low values of third and fifth harmonic distortion thereby minimizing the filtering problems necessary to reduce the total harmonic distortion to well below the 10% level required for touch tone telephone encoding. Figure 9 shows the low pass filter characteristic of the output buffer for $C_1 = 0.0022\mu F$ and $C_2 = 0.022\mu F$. A small peak of 0.4dB occurs at 1100Hz with sharp attention (12dB per octave) above 2500Hz. This type of active filter produces a sharper and more desirable knee characteristic than would two simple cascaded RC networks.

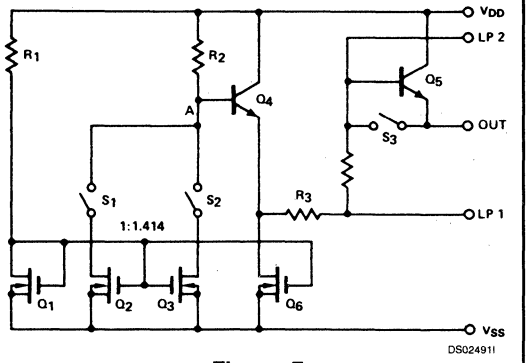


Figure 7

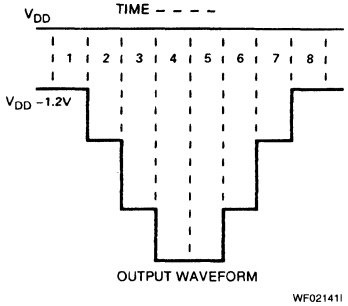


Figure 8: D to A Converter and Output Buffer

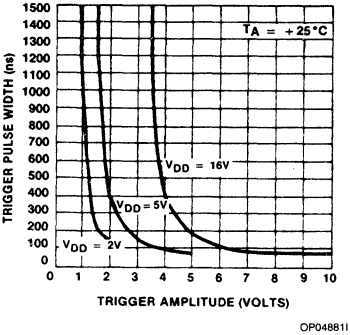


Figure 9: Frequency Attentuation Characteristics of the Output Buffer

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7206

Latchup Considerations

Most junction isolated CMOS integrated circuits, especially those of moderate or high complexity, exhibit latchup phenomena whereby they can be triggered into an uncontrollable low impedance mode between the supply terminals. This can be due to gross forward biasing of inputs or outputs (with respect to the supply terminals), high voltage supply transients, or more rarely by exceptional fast rate of rise of supply voltages.

The ICM7206 family is no exception, and precautions must be taken to limit the supply current to those values shown in the ABSOLUTE MAXIMUM RATINGS. For an example, do not use a 6 volt very low impedance supply source in an **extremely electrically noisy** environment unless a 500ohm current limiting resistor is included in series with the V_{SS} terminal. For normal telephone encoding applications no problems are envisioned, even with low impedance transients of 100 volts or more, if circuitry similar to that shown in the next section is used.

Telephone Handset

A typical encoder for telephone handsets is shown in Figure 10. This encoder uses a single contact per key keyboard and provides all other switching functions electronically. The diode connected between terminals 8 and 15 prevents the output going more than 1 volt negative with respect to the negative supply V_{SS} and the circuit operates over the supply voltage range from 3.5 volts to 15 volts on the device side of the bridge rectifier. Transients as high as 100 volts will not cause system failure, although the encoder will not operate correctly under these conditions. Correct operation will resume immediately after the transient is removed.

The output voltage of the synthesized sine wave is almost directly proportional to the supply voltage (V_{DD}–V_{SS}) and will increase with increase of supply voltage until zener breakdown occurs (approximately 6.3 volts between terminals 8 and 16) after which the output voltage remains constant.

Portable Tone Generator

The ICM7206A/B require a two contact key keyboard with the common line connected to the positive supply (neg for ICM7206B) (terminal 16). A simple diode matrix may be used with this keyboard to provide power to the system whenever a key is depressed, thus avoiding the need for an on/off switch. In Figure 11 the tone generator is shown using a 9 volt battery. However, if instead, a 6 volt battery is used, the diode D_4 is not required. It is recommended that a 470ohm resistor still be included in series with a negative (positive) supply to prevent accidental triggering of latchup.

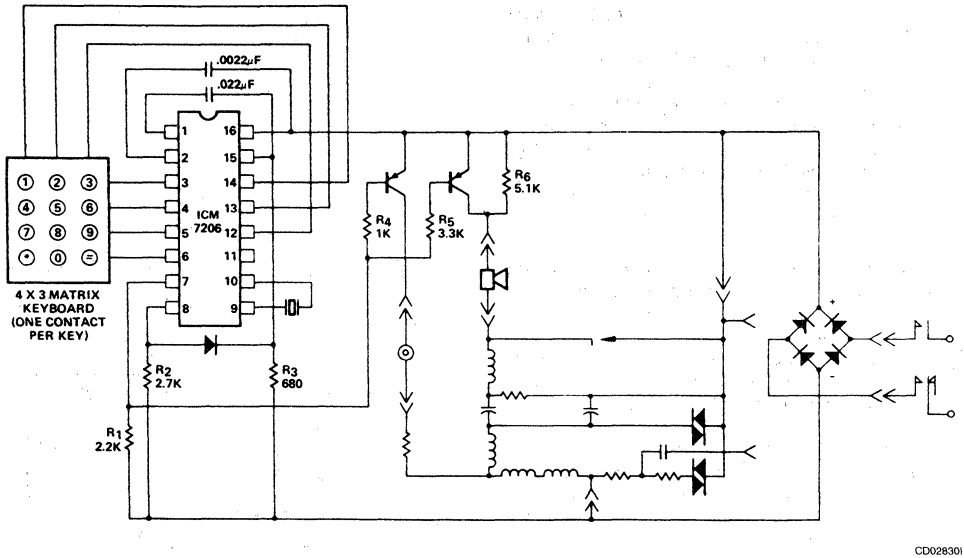


Figure 10: Telephone Handset Touch Tone Encoder

NOTE: If dual contact keyboard is used, common should be left floating.

Note: All typical values have been guaranteed by characterization and are not tested.

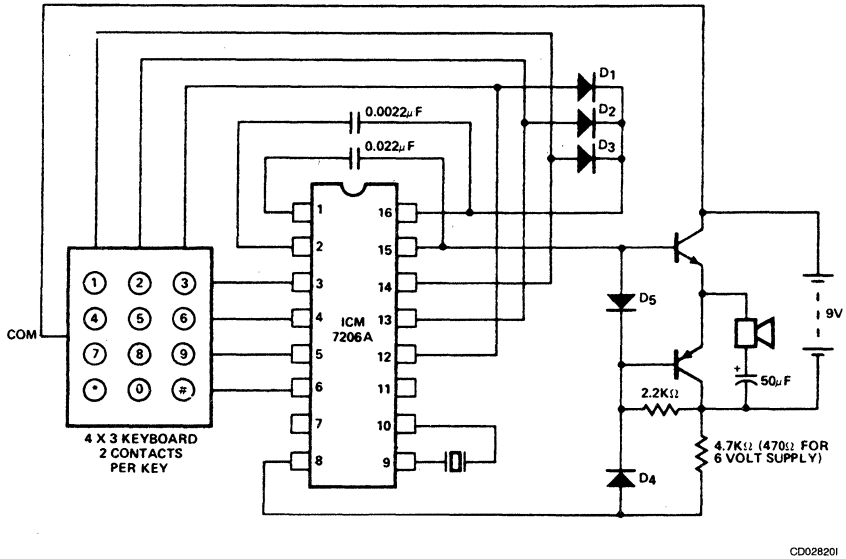


Figure 11: Portable Tone Generator

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7207/A
CMOS Timebase Generator

INTERSIL

GENERAL DESCRIPTION

The ICM7207/A consist of a high stability oscillator and frequency divider providing 4 control outputs suitable for frequency counter timebases. Specifically, when used as a frequency counter timebase in conjunction with the ICM7208 frequency counter, the four outputs provide the gating signals for the count window, store function, reset function and multiplex frequency reference. Additionally, the duration of the count window may be changed by a factor of 10 to provide a 2 decade range counting system.

The normal operating voltage of the ICM7207/A is 5 volts. The typical power dissipation is less than 2mW when using an oscillator frequency of 6.5536MHz with the 7207 and 5.24288mHz with the 7207A.

In the 7207/A the GATING OUTput, $\overline{\text{ReSeT}}$, and the MULTIPLEX output provide both pull up and pull down, eliminating the need for 3 external resistors; although, buffering must be provided if interfacing with TTL is required.

ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7207IJD	−20°C to +85°C	14-Pin CERDIP
ICM7207IPD	−20°C to +85°C	14-Pin PLASTIC DIP
ICM7207/D	−20°C to +85°C	DICE
ICM7207EV/Kit	—	EV/Kit*
ICM7207AIJD	−20°C to +85°C	14-Pin CERDIP
ICM7207AIPD	−20°C to +85°C	14-Pin PLASTIC DIP
ICM7207A/D	−20°C to +85°C	DICE
ICM7207AEV/Kit	—	EV/Kit*

*These EV/Kits contain just the IC and the corresponding crystal. The ICM7207A is also used in the 4½-Digit Counter/Driver kits, the ICM7224 EV/Kit, ICM7225 EV/Kit, and ICM7236 EV/Kit, which include several ICs, a crystal, PC board, and some passive components.

FEATURES

- **Stable HF Oscillator**
- **Low Power Dissipation ≤ 2mW With 5 Volt Supply**
- **Counter Chain Has Outputs at $\div 2^{12}$ and $\div 2^n$ or $\div(2^n \times 10)$; n = 17 for 7207, and 20 for 7207A**
- **Low Impedance Output Drivers ≤ 100 Ohms**
- **Count Windows of 10/100ms (7207 With 6.5536MHz Crystal) or 0.1/1 Sec. (7207A With 5.24288MHz Crystal)**

APPLICATIONS

- **System Timebases**
- **Oscilloscope Calibration Generators**
- **Marker Generator Strobes**
- **Frequency Counter Controllers**

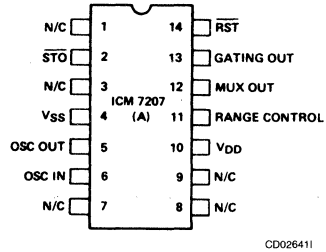


Figure 1: Pin Configuration (Outline dwg PD)

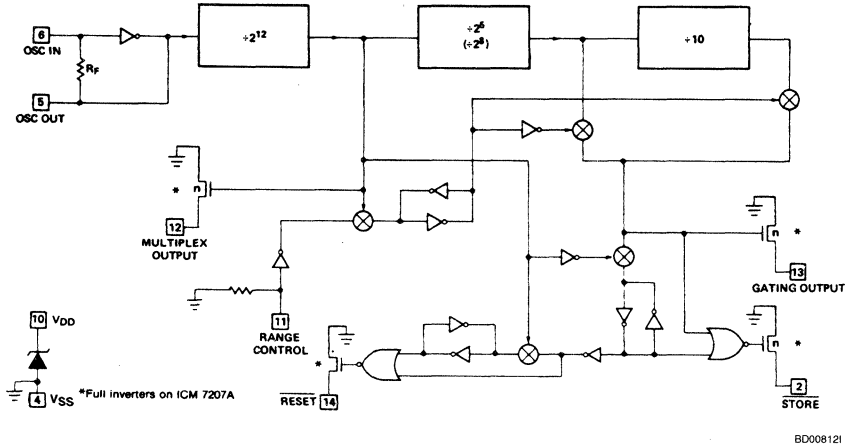


Figure 2: Functional Diagram

202200-002

Note: All typical values have been guaranteed by characterization and are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD} - V_{SS}$) 6.0V
Input Voltages ..... $V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Output Voltages:
7207 ..... V_{SS} to +6V
7207A ..... V_{DD} to V_{SS}

Output Currents 25mA
Power Dissipation @ 25°C Note 1 ..... 200mW
Operating Temperature Range ..... −20°C to +85°C
Storage Temperature Range ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE 1: Derate by 2mW/°C above 25°C.

Absolute maximum ratings refer to values which if exceeded may permanently change or destroy the device. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

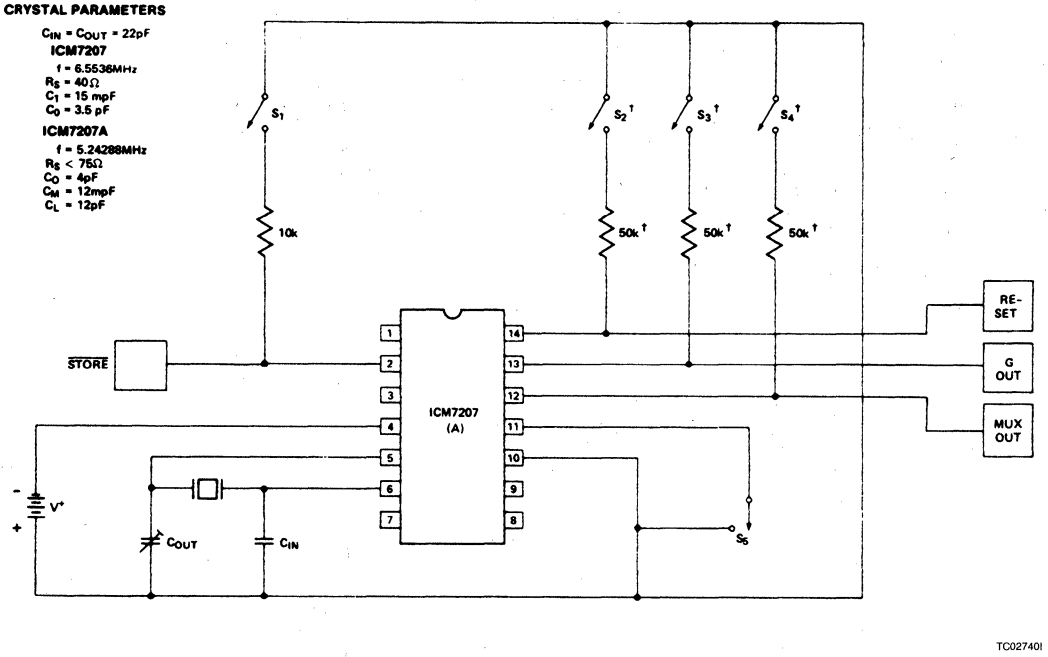
ELECTRICAL CHARACTERISTICS

f_{osc} = 6.5536MHz(7207), 5.24288MHz(7207A), V_{DD} = 5V, T_A = 25°C, V_{SS} = 0V, test circuit unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Operating Voltage Range	−20°C to +85°C	4		5.5	V
I_{DD}	Supply Current	All outputs open circuit		260	1000	μA
$R_{ds}(on)$	Output on Resistances	Output current = 5mA All outputs		50	120	Ω
I_{OLK}	Output Leakage Currents	All outputs (STORE only)			50	μA
(R_{OUT})	(Output Resistance Terminals 12,13,14)	Output current = 50μA, 7207A only			33K	Ω
I_{pd}	Input Pulldown Current	Terminal 11 connected to V_{DD}		50	200	μA
	Input Noise Immunity		25			% supply voltage
f_{osc}	Oscillator Frequency Range	Note 2	2		10	MHz
f_{STAB}	Oscillator Stability	$C_{IN} = C_{OUT}$ = 22pF		0.2	1.0	ppm/V
r_{OSC}	Oscillator Feedback Resistance	Quartz crystal open circuit Note 3	3			MΩ

NOTES: 2. Dynamic dividers are used in the initial stages of the divider chain. These dividers have a lower frequency of operation determined by transistor sizes, threshold voltages and leakage currents.
3. The feedback resistor has a non-linear value determined by the oscillator instantaneous input and output voltage voltages and the supply voltage.

Note: All typical values have been guaranteed by characterization and are not tested.

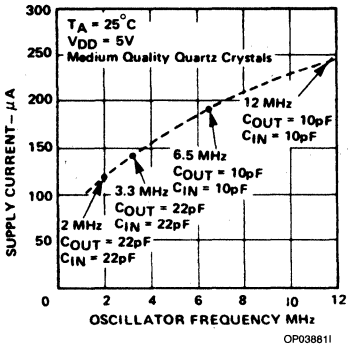


SWITCHES S_1, S_2, S_3, S_4 OPEN CIRCUIT FOR SUPPLY CURRENT MEASUREMENT.
SWITCH S_5 OPEN CIRCUIT FOR SLOW GATING PERIOD.
† SWITCHES S_2, S_3, S_4 and 50k RESISTORS ARE NOT NEEDED WHEN USING THE ICM7207A.

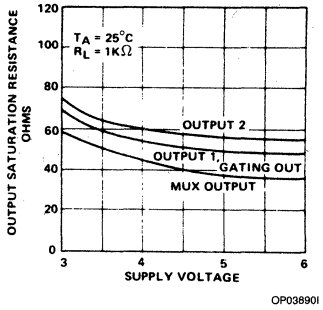
Figure 3: Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

SUPPLY CURRENT AS A FUNCTION OF OSCILLATOR FREQUENCY



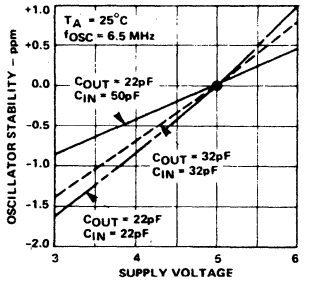
OUTPUT SATURATION RESISTANCES AS A FUNCTION OF SUPPLY VOLTAGE



Note: All typical values have been guaranteed by characterization and are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

OSCILLATOR STABILITY AS A FUNCTION OF SUPPLY VOLTAGE



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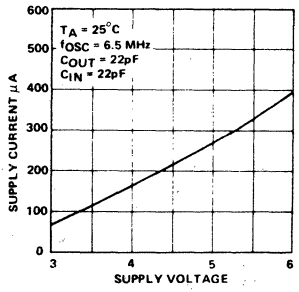
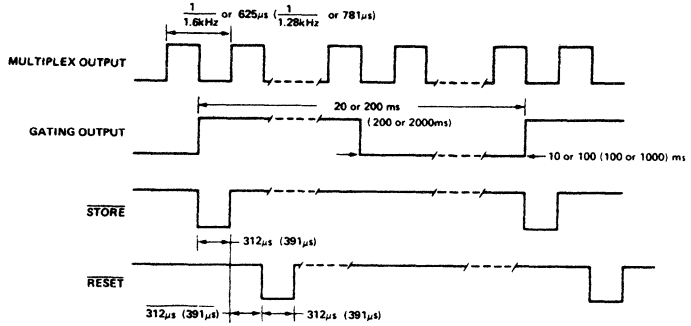
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



OP03910I

OUTPUT TIMING WAVEFORMS 7207 (7207A)
Crystal Frequency = 6.5536(5.24288)MHz



WF01680I

Figure 4: Output Waveform

DETAILED DESCRIPTION

Referring to the Test Circuit, Figure 3, the crystal oscillator frequency is divided by 2^{12} to provide both the multiplex frequency and generate the output pulse widths. The GATING OUTPUT provides a 50% duty cycle signal whose period depends upon whether the RANGE CONTROL terminal is connected to V_{DD} or V_{SS} (open circuit).

OSCILLATOR CONSIDERATIONS

The oscillator consists of a CMOS inverter with a non-linear resistor connected between the input and output terminals to provide biasing. Oscillator stabilities of approximately 0.1 ppm per 0.1 volt change are achievable at a supply voltage of 5 volts, using low cost crystals. The crystal specifications are shown in the TEST CIRCUIT.

It is recommended that the crystal load capacitance (C_L) be no greater than 15pF for a crystal having a series resistance equal to or less than 75Ω, otherwise the output amplitude of the oscillator may be too low to drive the divider reliably.

If a very high quality oscillator is desired, it is recommended that a quartz crystal be used having a tight tuning tolerance ±10ppm, a low series resistance (less than 25Ω), a low motional capacitance of 5mpF and a load capacitance of 20pF. The fixed capacitor C_{IN} should be 39pF and the oscillator tuning capacitor should range between approximately 8 and 60pF.

Use of a high quality crystal will result in typical oscillator stabilities of 0.05ppm per 0.1 volt change of supply voltage.

FREQUENCY LIMITATIONS

The ICM7207/A uses dynamic frequency counters in the initial divider sections. Dynamic frequency counters are faster and consume less power than static dividers but suffer from the disadvantage that there is a minimum operating frequency at a given supply voltage.

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7207/A

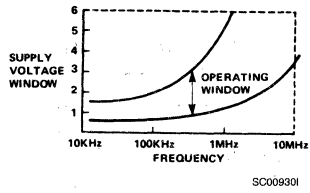


Figure 5

For example, if instead of 6.5MHz, a 1MHz oscillator is required, it is recommended that the supply voltage be reduced to between 2 and 2.5 volts. This may be realized by using a series resistor in series with the 5V positive supply line plus a decoupling capacitor. The quartz crystal parameters, etc., will determine the value of this resistor. NOTE: Except for the output open drain n-channel transistors no other terminal is permitted to exceed the supply voltage limits.

APPLICATION

A PRACTICAL FREQUENCY COUNTER

A complete frequency counter using the ICM7207/A together with the ICM7208 Frequency Counter is described in the ICM7208 data sheet. Other frequency counters using the ICM7207/A can be constructed using the ICM7224, ICM7225, and ICM7236, for LCD, LED and VF displays. The latter are available as EV/Kits also.

QUARTZ CRYSTAL MANUFACTURERS

The following list of possible suppliers is intended to be of assistance in putting a design into production. It should not be interpreted as a comprehensive list of suppliers, nor does it constitute an endorsement by Intersil.

a) CTS Knights, Sandwich, Illinois, (815) 786-8411
b) Motorola Inc., Franklin Park, Illinois (312) 451-1000
c) Sentry Manufacturing Co., Chickasaw, Oklahoma (405) 224-6780
d) Tyco Filters Division, Phoenix, Arizona (602) 272-7945
e) M-Tron Inds., Yankton, South Dakota (605) 665-9321
f) Saronix, Palo Alto, California (415) 856-6900

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7208
7-Digit LED Display Counter

GENERAL DESCRIPTION

The ICM7208 is a fully integrated seven decade counter-decoder-driver and is manufactured using Intersil's low voltage metal gate C-MOS process.

Specifically the ICM7208 provides the following on chip functions: a 7 decade counter, multiplexer, 7 segment decoder, digit & segment driver, plus additional logic for display blanking, reset, input inhibit, and display on/off.

For unit counter applications the only additional components are a 7 digit common cathode display, 3 resistors and a capacitor to generate the multiplex frequency reference, and the control switches.

The ICM7208 is intended to operate over a supply voltage of 2 to 6 volts as a medium speed counter, or over a more restricted voltage range for high frequency applications.

As a frequency counter it is recommended that the ICM7208 be used in conjunction with the ICM7207 Oscillator Controller, which provides a stable HF oscillator, and output signal gating.

FEATURES

- **Low Operating Power Dissipation < 10mW**
- **Low Quiescent Power Dissipation < 5mW**
- **Counts and Displays 7 Decades**
- **Wide Operating Supply Voltage Range $2V \leq V_{DD} \leq 6V$**
- **Drives Directly 7 Decade Multiplexed Common Cathode LED Display**
- **Internal Store Capability**
- **Internal Inhibit to Counter Input**
- **Test Speedup Point**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7208IPI	−20°C to +85°C	28 Lead Plastic DIP
ICM7208IJI	−20°C to +85°C	28 Lead CERDIP
ICM7208/D	–	DICE

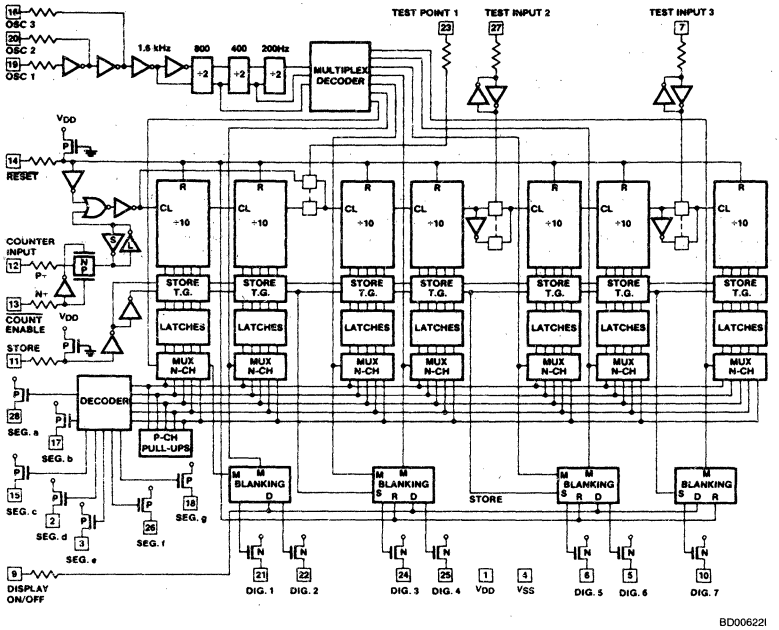


Figure 1: Functional Diagram

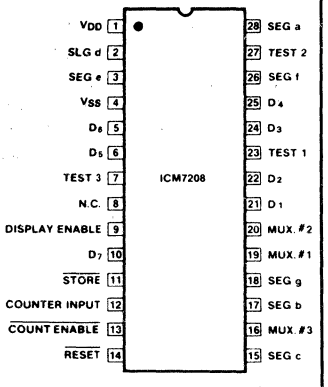


Figure 2: Pin Configuration (Outline Drawing PI)

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7208

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 2) ($V_{DD} - V_{SS}$) 6V
Input Voltage Range (any input terminal)
(Note 2) ..... $V_{SS}-0.3V$ to $V_{DD}+0.3V$
Output Digit Drive Current (Note 3) 150mA
Output Segment Drive Current 30mA
Power Dissipation (Note 1) 1W
Operating Temperature Range ..... −20°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{DD} = 5V, V_{SS} = 0V, T_A = 25°C, display off, unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{Q1}	Quiescent Current	All controls plus terminal 19 connected to V_{DD} No multiplex oscillator		30	300	μA
I_{Q2}	Quiescent Current	All control inputs plus terminal 19 connected to V_{DD} except STORE which is connected to V_{SS}		70	350	
I_{DD1}	Operating Supply Current	All inputs connected to V_{DD}, RC multiplexer osc operating f_{in} < 25kHz		210	500	
I_{DD2}	Operating Supply Current	f_{in} = 2MHz			700	
V_{SUPPLY}	Supply Voltage Range	$f_{in} \leq$ 2MHz	3.5		5.5	V
R_{DIG}	Digit Driver On Resistance			4	12	Ω
I_{DIG}	Digit Driver Leakage Current				500	μA
r_{SEG}	Segment Driver On Resistance			40		Ω
I_{SLK}	Segment Driver Leakage Current				500	μA
R_P	Pullup Resistance of RESET or STORE Inputs		100	400		kΩ
R_{IN}	COUNTER INPUT Resistance	Terminal 12 either at V_{DD} or V_{SS}			100	
V_{HIN}	COUNTER INPUT Hysteresis Voltage			25	50	mV

NOTES: 1. This value of power dissipation refers to that of the package and will not be obtained under normal operating conditions.
2. The supply voltage must be applied before or at the same time as any input voltage. This poses no problems with a single power supply system. If a multiple power supply system is used, it is mandatory that the supply for the ICM7208 is switched on before the other supplies otherwise the device may be permanently damaged.
3. The output digit drive current must be limited to 150mA or less under steady state conditions. (Short term transients up to 250mA will not damage the device.) Therefore, depending upon the LED display and the supply voltage to be used it may be necessary to include additional segment series resistors to limit the digit currents.

Note: All typical values have been guaranteed by characterization and are not tested.

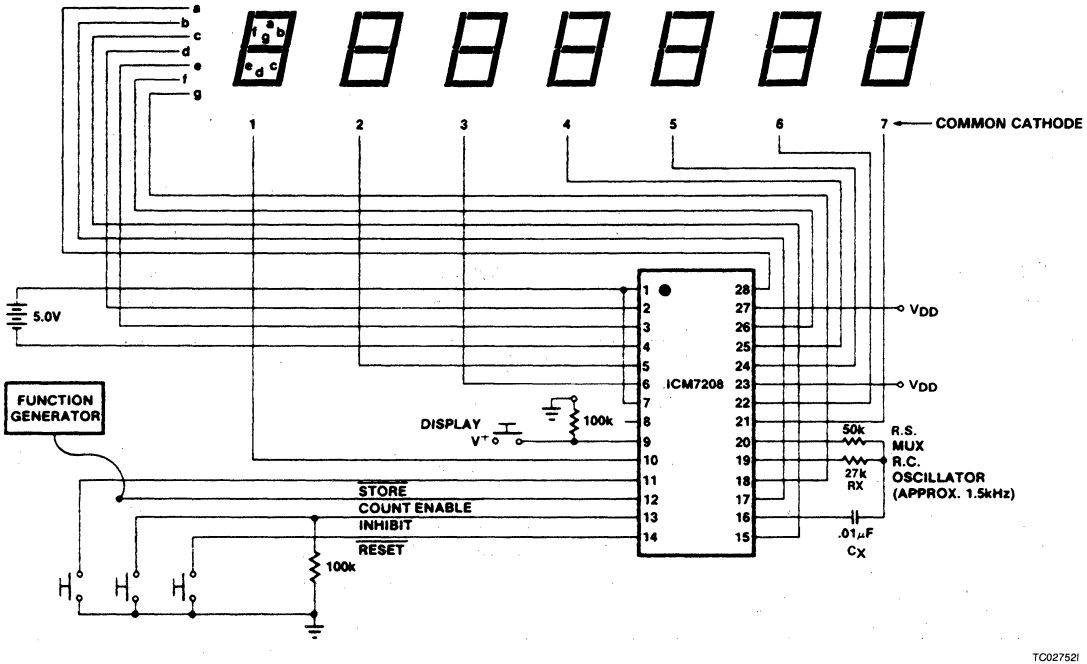
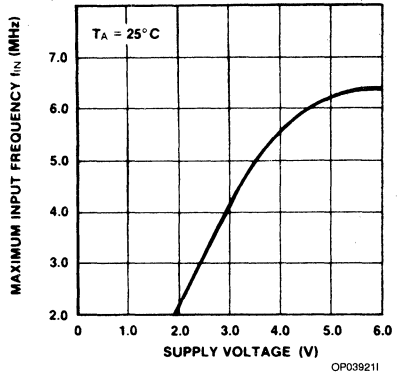


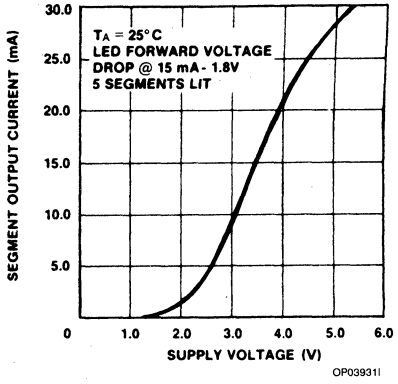
Figure 3: Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

MAXIMUM COUNTER INPUT FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



SEGMENT OUTPUT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

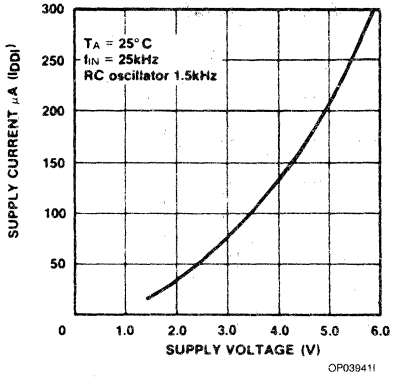


Note: All typical values have been guaranteed by characterization and are not tested.

ICM7208

TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



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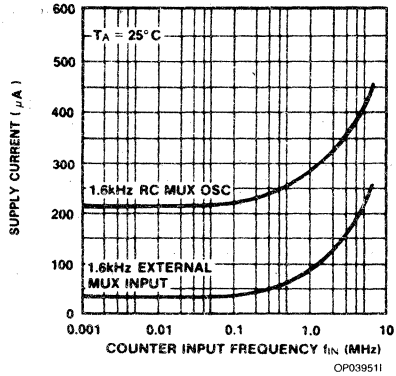
SUPPLY CURRENT AS A FUNCTION OF COUNTER INPUT FREQUENCY



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TEST PROCEDURES

The ICM7208 is provided with three input terminals 7, 23, 27 which may be used to accelerate testing. The least two significant decade counters may be tested by applying an input to the 'COUNTER INPUT' terminal 12. 'TEST POINT' terminal 23 provides an input which bypasses the 2 least significant decade counters and permits an injection of a signal into the third decade counter. Similarly terminals 7 and 27 permit rapid counter advancing at two points further along the string of decade counters.

CONTROL INPUT DEFINITIONS

INPUT	TERMINAL	VOLTAGE	FUNCTION
1. DISPLAY	9	V_{DD} V_{SS}	Display On Display Off
2. STORE	11	V_{DD} V_{SS}	Counter Information Latched Counter Information Transferring
3. ENABLE	13	V_{DD} V_{SS}	Input to Counter Blocked Normal Operation
4. RESET	14	V_{DD} V_{SS}	Normal Operation Counters Reset

COUNTER INPUT DEFINITION

The internal counters of the ICM7208 index on the negative edge of the input signal at terminal #12.

DETAILED DESCRIPTION

Format of Signal to be Counted

The noise immunity of the COUNTER INPUT Terminal is approximately 1/3 the supply voltage. Consequently, the input signal should be at least 50% of the supply in peak to peak amplitude and preferably equal to the supply.

The optimum input signal is a 50% duty cycle square wave equal in amplitude to the supply. However, as long as the rate of change of voltage is not less than approximately $10^{-4}V/\mu s$ at 50% of the power supply voltage, the input waveshape can be sinusoidal, triangular, etc.

When driving the input of the ICM7208 from TTL, a 1k–5kΩ pull-up resistor to the positive supply must be used to increase peak to peak input signal amplitude.

Display Considerations

Any common cathode multiplexable LED display may be used. However, if the peak digit current exceeds 150mA for any prolonged time, it is recommended that resistors be included in series with the segment outputs to limit digit current to 150mA.

The ICM7208 is specified with 500µA of possible digit leakage current. With certain new LED displays that are extremely efficient at low currents, it may be necessary to include resistors between the cathode outputs and the positive supply to bleed off this leakage current.

Display Multiplex Rate

The ICM7208 has approximately 0.5µs overlap between output drive signals. Therefore, if the multiplex rate is very fast, digit ghosting will occur. The ghosting determines the upper limit for the multiplex frequency. At very low multiplex rates flicker becomes visible.

It is recommended that the display multiplex rate be within the range of 50Hz to 200Hz, which corresponds to 400Hz to 1600Hz for the multiplex frequency input. For stand alone systems, two inverters are provided so that a simple but stable RC oscillator may be built using only 2 resistors and a capacitor.

The multiplex oscillator is eight times the multiplex rate. The frequency is given using the following formulii:

$$f = \frac{1}{2.2R_XC_X}$$

R_S should always be $\leq 1M\Omega$ and $R_S = kR_X$ where k is in the range 2-10.

An external generator may be used to provide the multiplex frequency input. This signal, applied to terminal 19 (terminals 16 and 20 open circuit), should be approximately equal to the supply voltage, and should be a square wave for minimum of power dissipation.

Note: All typical values have been guaranteed by characterization and are not tested.

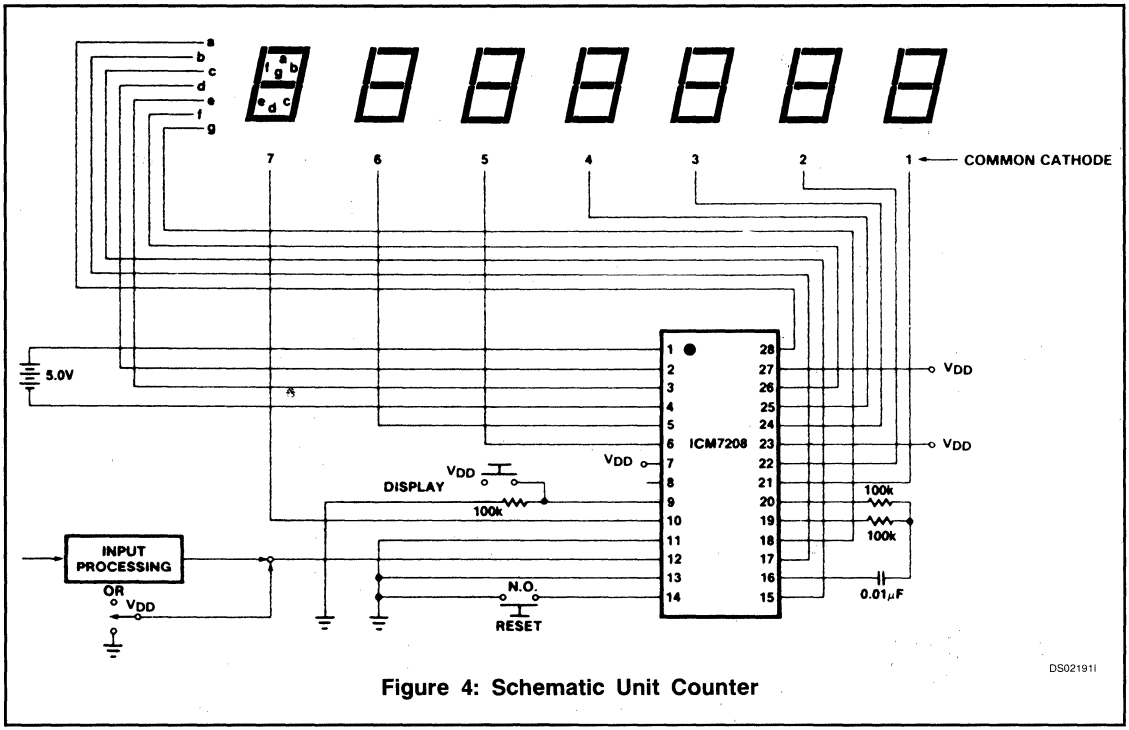


Figure 4: Schematic Unit Counter

Unit Counter

Figure 4 shows the schematic of an extremely simple unit counter that can be used for remote traffic counting, to name one application. The power cell stack should consist of 3 or 4 nickel cadmium rechargeable cells (nominal 3.6 or 4.8 volts). If 4 x 1.5 volt cells are used it is recommended that a diode be placed in series with the stack to guarantee that the supply voltage does not exceed 6 volts.

The input switch is shown to be a single pole double throw switch (SPDT). A single pole single throw switch (SPST) could also be used (with a pullup resistor), however, anti-bounce circuitry must be included in series with the counter input. In order to avoid contact bounce problems due to the SPDT switch the ICM7208 contains an input latch on chip.

The unit counter updates the display for each negative transition of the input signal. The information on the display will count, after reset, from 00 to 9,999,999 and then reset to 0000000 and begin to count up again. To blank leading zeros, actuate reset at the beginning of a count. Leading zero blanking affects two digits at a time.

For battery operated systems the display may be switched off to conserve power.

Frequency Counter

The ICM7208 may be used as a frequency counter when used with an external frequency reference and gating logic. This can be achieved using the ICM7207 Oscillator Controller (Figure 5). The ICM7207 uses a crystal controlled oscillator to provide the store and reset pulses together with the counting window. Figure 6 shows the recommended input gating waveforms to the ICM7208. At the end of a counting period (50% duty cycle) the counter input is inhibited. The counter information is then transferred and stored in latches, and can be displayed. Immediately after this information is stored, the counters are cleared and are ready to start a new count when the counter input is enabled.

Using a 6.5536MHz quartz crystal and the ICM7207 driving the ICM7208, two ranges of counting may be obtained, using either 0.01 sec or 0.1 sec counter enable windows.

Previous comments on leading zero blanking, etc., apply as per the unit counter.

The ICM7207 provides the multiplex frequency reference of 1.6kHz.

Period Counter

For this application, as opposed to the frequency counter, the gating and the input signal to be measured are reversed to the frequency counter. The input period is multiplied by two to produce a single polarity signal (50% duty cycle) equal to the input period, which is used to gate into the counter the frequency reference (1MHz in this case). Figure 8 shows a block schematic of the input waveform generator. The 1MHz frequency reference is generated by the ICM7209 Clock Generator using an 8MHz oscillator frequency and internally dividing this frequency by 8. Alternatively, a 1MHz signal could be applied directly to COUNTER INPUT. Waveforms are shown in Figure 7.

Note: All typical values have been guaranteed by characterization and are not tested.

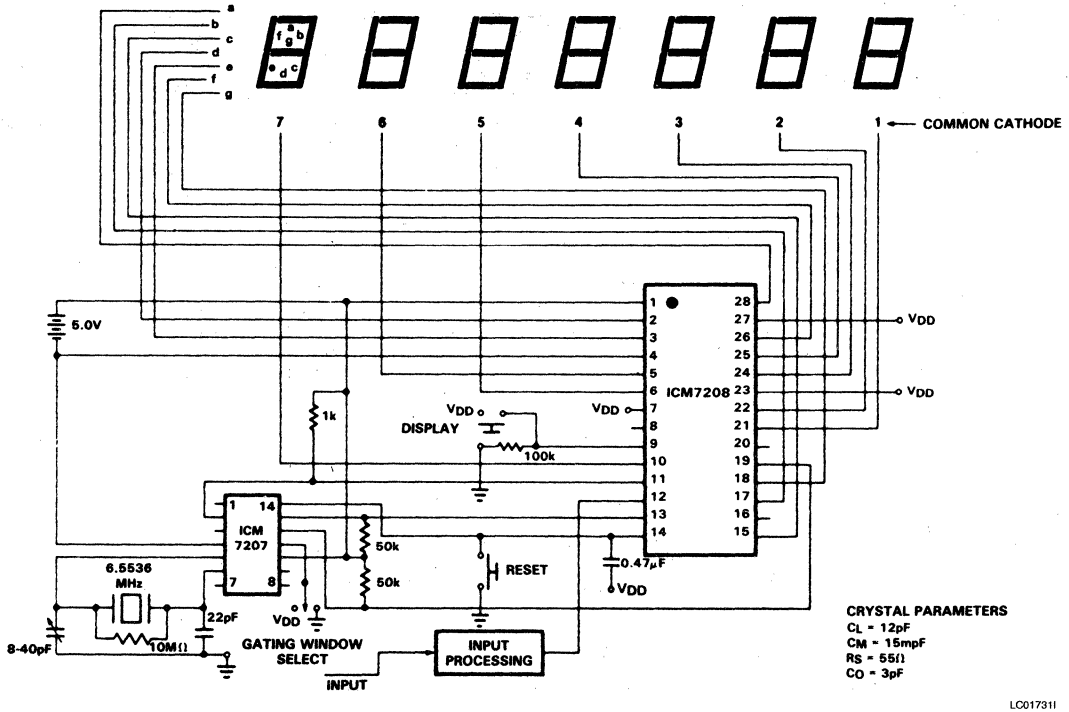


Figure 5: Frequency Counter

Note: For a 1 sec count window which allows all 7 digits to be used with a resolution of 1Hz, the ICM7207 can be replaced with the ICM7207A. Circuit details are given on the 7207A data sheet.

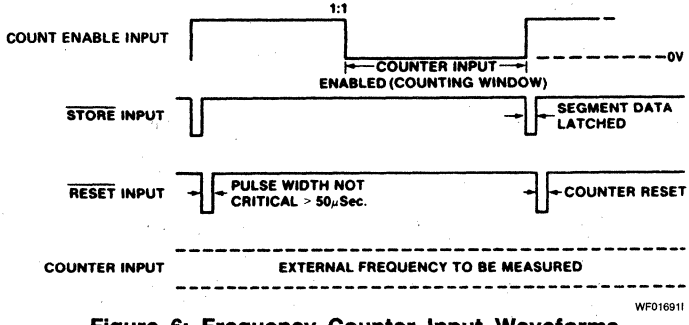


Figure 6: Frequency Counter Input Waveforms

Note: All typical values have been guaranteed by characterization and are not tested.

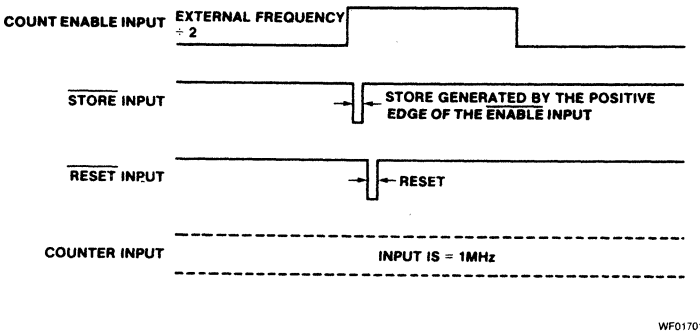


Figure 7: Period Counter Input Waveforms

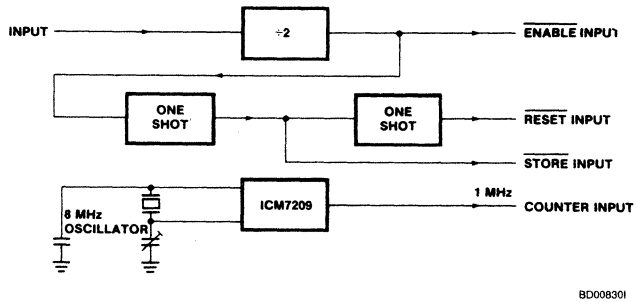


Figure 8: Period Counter Input Generator

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7209
Timebase Generator

GENERAL DESCRIPTION

The Intersil ICM7209 is a versatile CMOS clock generator capable of driving a number of 5 volt systems with a variety of input requirements. When used to drive up to 5 TTL gates, the typical rise and fall times are 10ns.

The ICM7209 consists of an oscillator, a buffered output equal to the oscillator frequency and a second buffered output having an output frequency one-eighth that of the oscillator. The guaranteed maximum oscillator frequency is 10MHz. Connecting the DISABLE terminal to the negative supply forces the ÷8 output into the '0' state and the output 1 into the '1' state.

FEATURES

- **High Frequency Operation — 10MHz Guaranteed**
- **Requires Only A Quartz Crystal and Two Capacitors**
- **Bipolar, CMOS Compatibility**
- **High Output Drive Capability — 5 x TTL Fanout With 10ns Rise and Fall Times**
- **Low Power — 50mW at 10MHz**
- **Choice of Two Output Frequencies — Osc., and Osc. ÷ 8 Frequencies**
- **Disable Control for Both Outputs**
- **Wide Industrial Temperature Range — 20°C to +85°C**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7209IJA	−20°C to +85°C	8 pin CERDIP
ICM7209IPA	−20°C to +85°C	8 pin PLASTIC
ICM7209/D	—	DICE

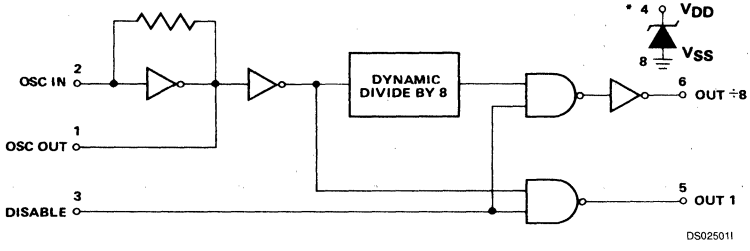


Figure 1: Functional Diagram
*Zener Voltage is Typically 6.3 Volts

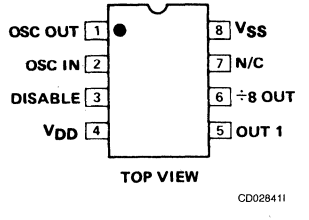


Figure 2: Pin Configuration (Outline dwg PA)
Pin 1 is designated by either a dot or a notch

Note: All typical values have been guaranteed by characterization and are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6V
Output Voltages ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Input Voltages ..... V_{SS} – 0.3V to V_{DD} + 0.3V

Power Dissipation (25°C) 300mW
Storage Temperature ..... –55°C to +125°C
Operating Temperature Range ..... –20°C to +85°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{DD} - V_{SS} = 5V \pm 10\%$, test circuit, $f_{osc} = 10MHz$, $T_A = 25°C$ unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply Current	Note 1 No Load		11	20	mA
C_D	Disable Input Capacitance			5		pF
I_{ILK}	Disable Input Leakage	Either '1' or '0' state			±10	µA
V_{OL}	Output Low State	Either OUT 1 or OUT ÷8 simulated 5 x TTL loads			0.4	V
V_{OH}	Output High State	Either OUT 1 or OUT ÷8 simulated 5 x TTL loads	4.0	4.9		
t_R	Output Rise Time (Note 3)	Either OUT 1 or OUT ÷8 simulated 5 x TTL loads		10		ns
t_F	Output Fall Time (Note 3)	Either OUT 1 or OUT ÷8 simulated 5 x TTL loads		10		
f_{OSC}	Minimum OSC Frequency for ÷8 Output	Note 2	2			MHz
	Output ÷8 duty cycle	Any operating frequency Low state : High state		7:9		
GM	Oscillator Transconductance		80	200		µs

NOTES: 1. The power dissipation is a function of the oscillator frequency (1st ORDER EFFECT see curve) but is also effected to a small extent by the oscillator tank components.
2. The ÷8 circuitry uses a dynamic scheme. As with any dynamic system, information or data is stored on very small nodal capacitances instead of latches (static systems) and there is a lower cutoff frequency of operation. Dynamic dividers are used in the ICM7209 to significantly improve high frequency performance and to decrease power consumption.
3. Rise and fall times are defined between the output levels of 0.5 and 2.4 volts.

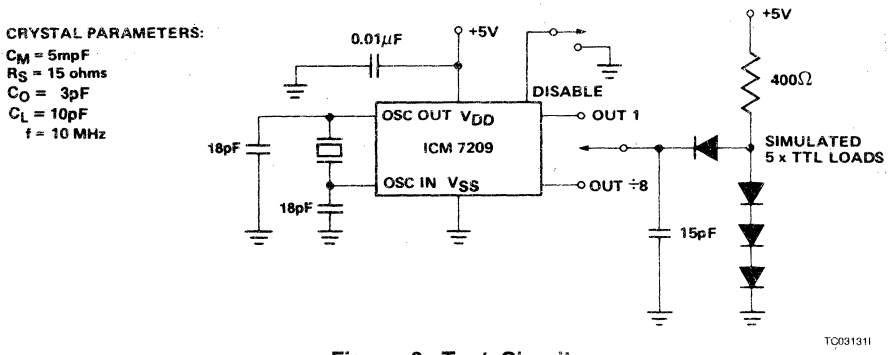


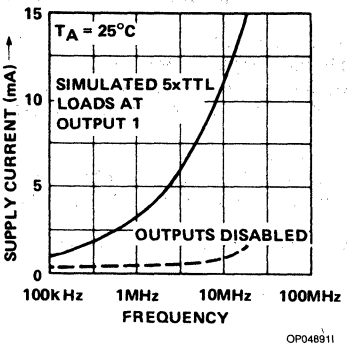
Figure 3: Test Circuit

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7209

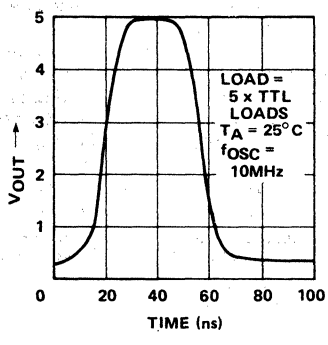
TYPICAL PERFORMANCE CHARACTERISTICS ($V_{DD} - V_{SS} = 5V$)

SUPPLY CURRENT AS A FUNCTION OF OSCILLATOR FREQUENCY



OP04891I

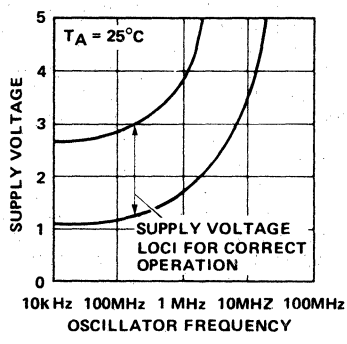
TYPICAL OUT 1 RISE AND FALL TIMES



OP04900I

Rise and fall times of OUT ÷8 are similar to those of OUT 1.

SUPPLY VOLTAGE RANGE FOR CORRECT OPERATION OF ÷8 COUNTER AS A FUNCTION OF OSCILLATOR FREQUENCY.



OP04911I

DETAILED DESCRIPTION

OSCILLATOR CONSIDERATIONS

The oscillator consists of a CMOS inverter with a non-linear resistor connected between the oscillator input and output to provide D.C. biasing. Using commercially obtainable quartz crystals the oscillator will operate from low frequencies (10kHz) to 10MHz.

The oscillator circuit consumes about 500μA of current using a 10MHz crystal with a 5 volt supply, and is designed to operate with a high impedance tank circuit. It is therefore necessary that the quartz crystal be specified with a load capacitance (C_L) of 10pF instead of the standard 30pF. To maximize the stability of the oscillator as a function of supply voltage and temperature, the motional capacitance of the crystal should be low (5mpF or less). Using a fixed input capacitor of 18pF and a variable capacitor of nominal value of 18pF on the output will result in oscillator stabilities of typically 1ppm per volt change in supply voltage.

THE ÷ 8 OUTPUT

A dynamic divider is used to divide the oscillator frequency by 8. Dynamic dividers use small nodal capacitances to store voltage levels instead of latches (which are used in static dividers). The dynamic divider has advantages in high speed operation and low power but suffers from limited low frequency operation. This results in a window of operation for any oscillator frequency (see TYPICAL PERFORMANCE CHARACTERISTICS).

OUTPUT DRIVERS

The output drivers consist of CMOS inverters having active pullups and pulldowns. Thus the outputs can be used to directly drive TTL gates, other CMOS gates operating with a 5 volt supply, or TTL compatible MOS gates. The guaranteed fanout is 5 TTL loads although typical fanout capability is at least 10 TTL loads with slightly increased output rise and fall times.

DEVICE POWER CONSUMPTION

At low frequencies the principal component of the power consumption is the oscillator. At high oscillator frequencies the major portion of the power is consumed by the output drivers, thus by disabling the outputs (activating the DISABLE INPUT) the device power consumption can be dramatically reduced.

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7213
One Second/One Minute Timebase Generator

GENERAL DESCRIPTION

The ICM7213 is a fully integrated micropower oscillator and frequency divider with four buffered outputs suitable for interfacing with most logic families. The power supply may be either a two battery stack (Ni-cad, alkaline, etc.) or a regular power supply greater than 2 volts. Depending upon the state of the WIDTH, INHIBIT, and TEST inputs, using a 4.194304MHz crystal will produce a variety of output frequencies including 2048Hz, 1024Hz, 34.133Hz, 16Hz, 1Hz, and 1/60Hz (plus composites).

The ICM7213 utilizes a very high speed low power metal gate CMOS technology which uses 6.4 volt zeners between the drains and sources of each transistor and also across the supply terminals. Consequently, the ICM7213 is limited to a 6 volt maximum supply voltage, although a simple dropping network can be used to extend the supply voltage range well above 6 volts (See Figure 7).

FEATURES

- **Guaranteed 2 Volts Operation**
- **Very Low Current Consumption: Typ. 100μA @ 3V**
- **All Outputs TTL Compatible**
- **On Chip Oscillator Feedback Resistor**
- **Oscillator Requires Only 3 External Components: Fixed Capacitor, Trim Capacitor, and A Quartz Crystal**
- **Output Inhibit Function**
- **4 Simultaneous Outputs: One Pulse/Sec, One Pulse/Min, 16Hz and Composite 1024 + 16 + 2Hz Outputs**
- **Test Speed-Up Provides Other Frequency Outputs**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7213IJD	−20°C to +85°C	14 pin CERDIP
ICM7213IPD	−20°C to +85°C	14 pin PLASTIC DIP
ICM7213/D	—	DICE

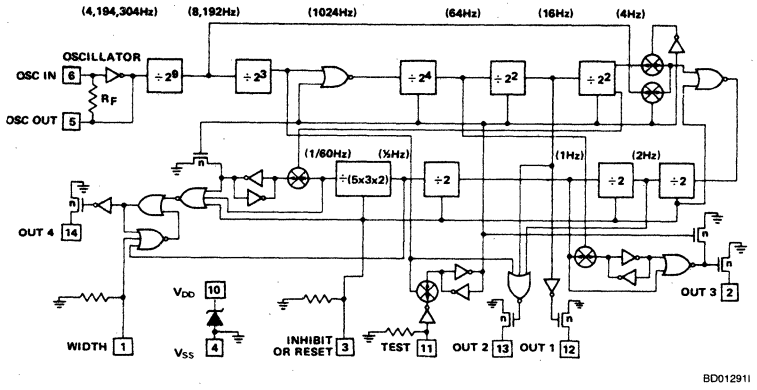


Figure 1: Functional Diagram

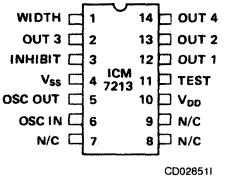


Figure 2: Pin Configuration (Outline drawing PD)

202800-002

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7213

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD} - V_{SS}$) 6.0V
Output Current (Any output) 20mA
All Input and Oscillator Voltages (Note 1) .....
$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
All Output Voltages (Note 1) ..... V_{SS} to 6.0V

Operating Temperature Range ..... −20°C to +85°C
Storage Temperature Range ..... −40°C to +125°C
Power Dissipation (Note 2) 200mW
Lead Temperature (Soldering, 10sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: The ICM7213 like most CMOS devices, may enter a destructive latchup mode if an input or output voltage is applied in excess of those defined and there is no supply current limiting.

NOTE 2: Derate linearly power rating of 200mW at 25°C to 50mW at 70°C.

ELECTRICAL CHARACTERISTICS

($V_{DD} - V_{SS} = 3.0V$, $f_{osc} = 4.194304MHz$, Test Circuit, $T_A = 25°C$ unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply Current			100	140	µA
V_{SUPPLY}	Guaranteed Operating Supply Voltage Range ($V_{DD} - V_{SS}$)	$-20°C < T_A < 85°C$	2		4	V
I_{OLK}	Output Leakage Current	Any output, $V_{OUT} = 6$ Volts			10	µA
R_{OUT}	Output Sat. Resistance	Any output, $I_{OLK} = 2.5mA$		120	200	Ω
I_I	Inhibit Input Current	Inhibit terminal connected to V_{DD}		10	40	µA
I_{TP}	Test Point Input Current	Test point terminal connected to V_{DD}		10	40	
I_W	Width Input Current	Width terminal connected to V_{DD}		10	40	
g_m	Oscillator g_m	$V_{DD} = 2V$	100			µs
f_{OSC}	Oscillator Frequency Range (Note 3)		1		10	MHz
f_{STAB}	Oscillator Stability	$2V < V_{DD} < 4V$		1.0		ppm
t_s	Oscillator Start Time			0.1		sec
		$V_{DD} = 2.0$ volts		0.2		

NOTE: 3. The ICM7213 uses dynamic dividers for high frequency division. As with any dynamic system, information is stored on very small nodal capacitances instead of latches (static system), therefore there is a lower frequency of operation. Dynamic dividers are used to improve the high frequency performance while at the same time significantly decreasing power consumption. At low supply voltages, operation at less than 1MHz is possible. See application notes.

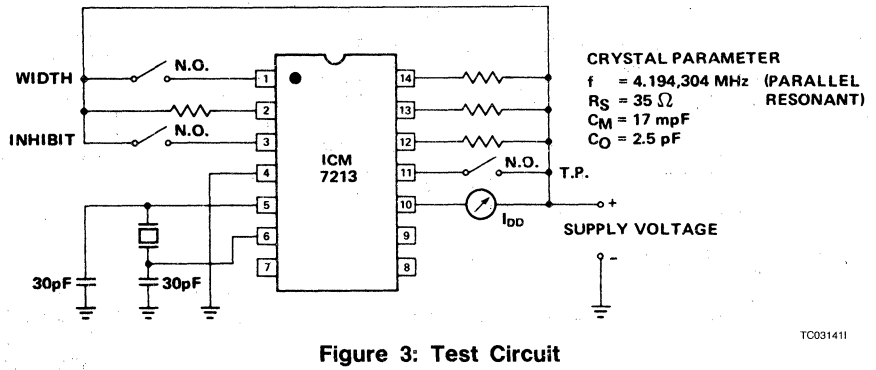
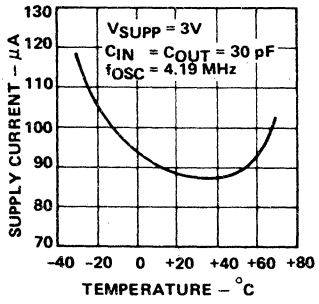


Figure 3: Test Circuit

Note: All typical values have been guaranteed by characterization and are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



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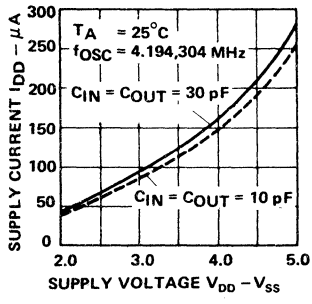
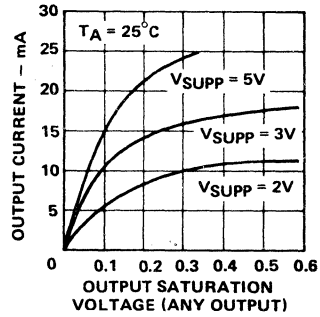
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



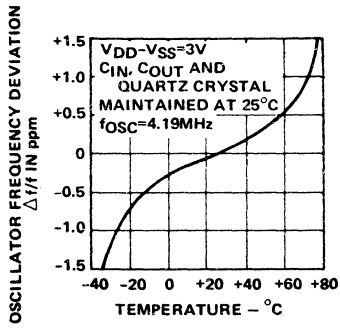
OP04931I

OUTPUT CURRENT AS A FUNCTION OF OUTPUT SATURATION VOLTAGE



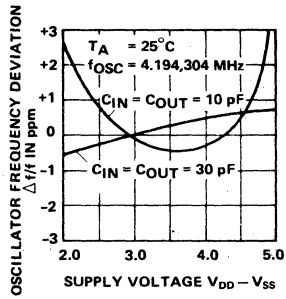
OP04940I

OSCILLATOR STABILITY AS A FUNCTION OF DEVICE TEMPERATURE



OP04950I

OSCILLATOR STABILITY AS A FUNCTION OF SUPPLY VOLTAGE



OP04961I

OUTPUT DEFINITIONS

INPUT STATES*			PIN 12 OUT 1	PIN 13 OUT 2	PIN 2 OUT 3	PIN 14 OUT 4
TEST	INHIBIT	WIDTH				
L	L	L	16Hz $\div 2^{18}$	$\overline{1024 + 16 + 2}$Hz ($\div 2^{12} \div 2^{18} \div 2^{21}$) composite	1Hz, 7.8ms $\div 2^{22}$	1/60Hz, 1 Sec. $\div(2^{24} \times 3 \times 5)$
L	L	H	16Hz $\div 2^{18}$	$\overline{1024 + 16 + 2}$Hz ($\div 2^{12} \div 2^{18} \div 2^{21}$) composite	1Hz, 7.8ms $\div 2^{22}$	1/60Hz, 125ms
L	H	L	16Hz $\div 2^{18}$	$\overline{1024 + 16}$Hz ($\div 2^{12} \div 2^{18}$) composite	OFF	OFF
L	H	H	16Hz $\div 2^{18}$	$\overline{1024 + 16}$Hz ($\div 2^{12} \div 2^{18}$) composite	OFF	SEE WAVEFORMS
H	L	L	ON	$\overline{4096 + 1024}$Hz ($\div 2^{10} \div 2^{12}$) composite	2048Hz $\div 2^{11}$	34.133Hz, 50% D.C. $\div(2^{13} \times 5 \times 3)$
H	L	H	ON	$\overline{4096 + 1024}$Hz ($\div 2^{10} \div 2^{12}$) composite	2048Hz $\div 2^{11}$	34.133Hz, 50% D.C. $\div(2^{13} \times 5 \times 3)$
H	H	L	ON	1024Hz $\div 2^{12}$	ON	OFF
H	H	H	ON	1024Hz $\div 2^{12}$	ON	OFF

NOTE: When TEST and RESET are connected to ground, or left open, all outputs except for OUT 3 and OUT 4 have a 50% duty cycle.

Note: All typical values have been guaranteed by characterization and are not tested.

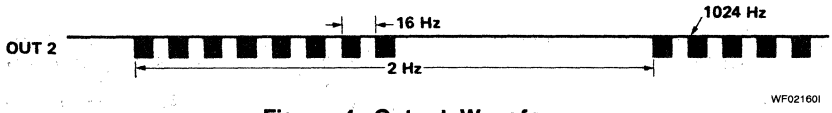


Figure 4: Output Waveforms

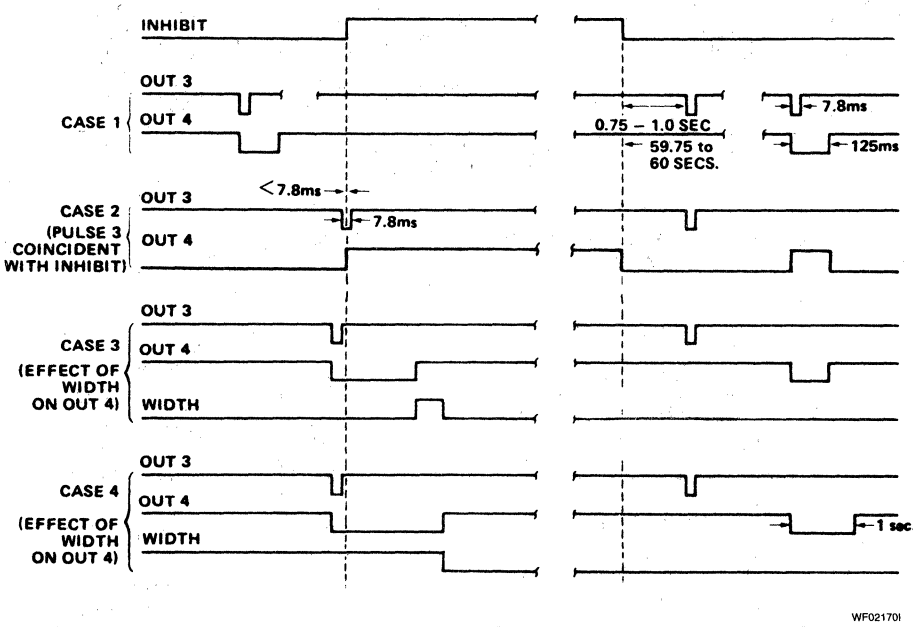


Figure 5: Effect of Input Inhibit (Test Connected to V_{SS} or Left Open)

All time scales are arbitrary, and in the case of OUT 3 only the pulses coinciding with the negative edge of OUT 4 are shown. Where time intervals are relevant they are clearly shown.

APPLICATIONS

Supply Voltage Considerations

The ICM7213 may be used to provide various precision outputs with frequencies from 2048Hz to 1/60Hz using a 4,194,304Hz quartz oscillator, and other output frequencies may be obtained using other quartz crystal frequencies. Since the ICM7213 uses dynamic high frequency dividers for the initial frequency division there are limitations on the supply voltage range depending on the oscillator frequency. If, for example, a low frequency quartz crystal is selected, the supply voltage should be selected in the center of the operating window, or approximately 1.7 volts.

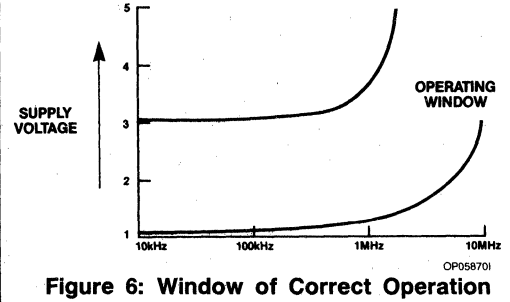


Figure 6: Window of Correct Operation

The supply voltage to the ICM7213 may be derived from a high voltage supply by using a simple resistor divider (if power is of no concern), by using a series resistor for minimum current consumption, or by means of a regulator.

Note: All typical values have been guaranteed by characterization and are not tested.

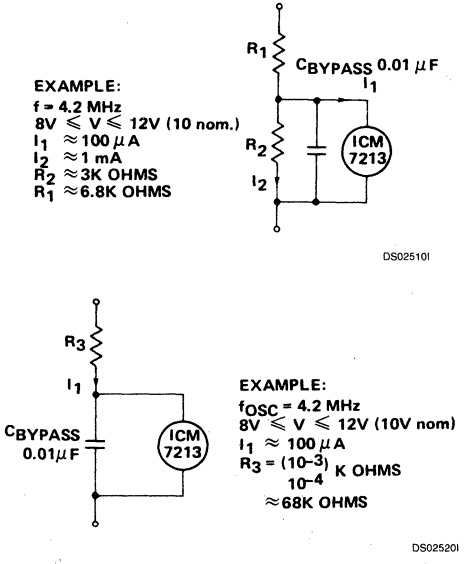


Figure 7: Biasing Schemes with High Voltage Supplies

Logic Family Compatibility

Pull up resistors will generally be required to interface with other logic families. These resistors must be connected between the various outputs and the positive power supply.

Oscillator Considerations

The oscillator consists of a CMOS inverter and a feedback resistor whose value is dependent on the voltage at the oscillator input and output terminals and the supply voltage. Oscillator stabilities of approximately 0.1ppm per 0.1 volt variation are achievable with a nominal supply voltage of 5 volts and a single voltage dropping resistor. The crystal specifications are shown in the TEST CIRCUIT.

It is recommended that the crystal load capacitance (CL) be no greater than 22pF for a crystal having a series resistance equal to or less than 75 ohms, otherwise the output amplitude of the oscillator may be too low to drive the divider reliably.

If a very high quality oscillator is desired, it is recommended that a quartz crystal be used having a tight tuning tolerance ±10ppm, a low series resistance (less than 25 ohms), a low motional capacitance of 5mpF and a load capacitance of 20pF. The fixed capacitor C_{IN} should be 30pF and the oscillator tuning capacitor should range between approximately 16 and 60pF.

Use of a high quality crystal will result in typical stabilities of 0.05ppm per 0.1 volt change of supply voltage.

Control Inputs

The TEST input inhibits the 2^{18} output and applies the 2^{9} output to the 2^{21} divider, thereby permitting a speedup of the testing of the ÷60 section by a factor of 2048 times. This also results in alternative output frequencies (see table).

The WIDTH input may be used to change the pulse width of OUT 4 from 125ms to 1 sec, or to change the state of OUT 4 from ON to OFF during INHIBIT.

7

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7215
6-Digit LED Display 4-Function Stopwatch

INTERSIL

GENERAL DESCRIPTION

The ICM7215 is a fully integrated six digit LED stopwatch circuit fabricated with Intersil's low threshold metal gate CMOS process. The circuit interfaces directly with a six digit/seven segment common cathode LED display. The low battery indicator can be connected to the decimal point anode or to a separate LED. The only components required for a complete stopwatch are the display, three SPST switches, a 3.2768MHz crystal, a trimming capacitor, three AA batteries and an ON-OFF switch. For a two function stopwatch, or to add a display off feature, one additional slide switch is required. The circuit divides the oscillator frequency by 2^{15} to obtain 100Hz, which is fed to the fractional seconds, seconds and minutes counters, while an intermediate frequency is used to obtain the 1/6 duty cycle 1.07kHz multiplex waveforms. The blanking logic provides leading zero blanking for seconds and minutes independently of the clock. The ICM7215 is packaged in a 24-lead plastic DIP.

FEATURES

- **Four Functions: Start/Stop/Reset, Split, Taylor, Time Out**
- **Six Digit Display: Ranges Up to 59 Minutes 59.99 Seconds**
- **High LED Drive Current: 13mA Peak Per Segment at 16.7% Duty Cycle With 4.0 Volt Supply**
- **Requires Only Three Low Cost SPST Switches Without Loss of Accuracy: Start/Stop, Reset, Display Unlock**
- **Chip Enable Pin Turns Off Both Segment and Digit Outputs; Can Be Used for Multiple Circuits Driving One Display**
- **Low Battery Indicator**
- **Digit Blanking On Seconds and Minutes**
- **Wide Operating Range: 2.0 to 5.0 Volts**
- **1kHz Multiplex Rate Prevents Flickering Display**
- **Can Be Used Easily In Four Different Single Function Stopwatches or Two Two-Function Stopwatches: Start/Stop/Reset With Time-out, Split With Taylor. The Component Count for A Three- or Four-Function Stopwatch Will Be Slightly Greater**
- **Retrofit to ICM7205 for Split and/or Taylor Applications**

ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ICM7215IPG	−20°C to +70°C	24-Pin PLASTIC DIP
ICM7215/D	—	DICE

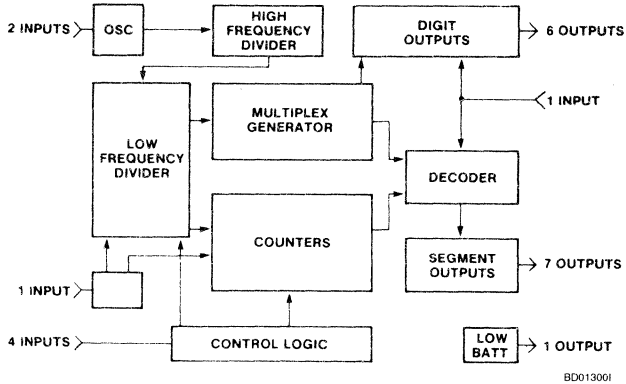


Figure 1: Functional Diagram

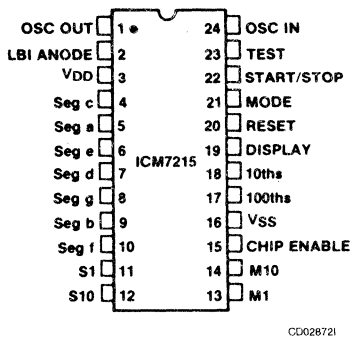


Figure 2: Pin Configuration (Outline dwg PG)

Note: All typical values have been guaranteed by characterization and are not tested.

ABSOLUTE MAXIMUM RATINGS

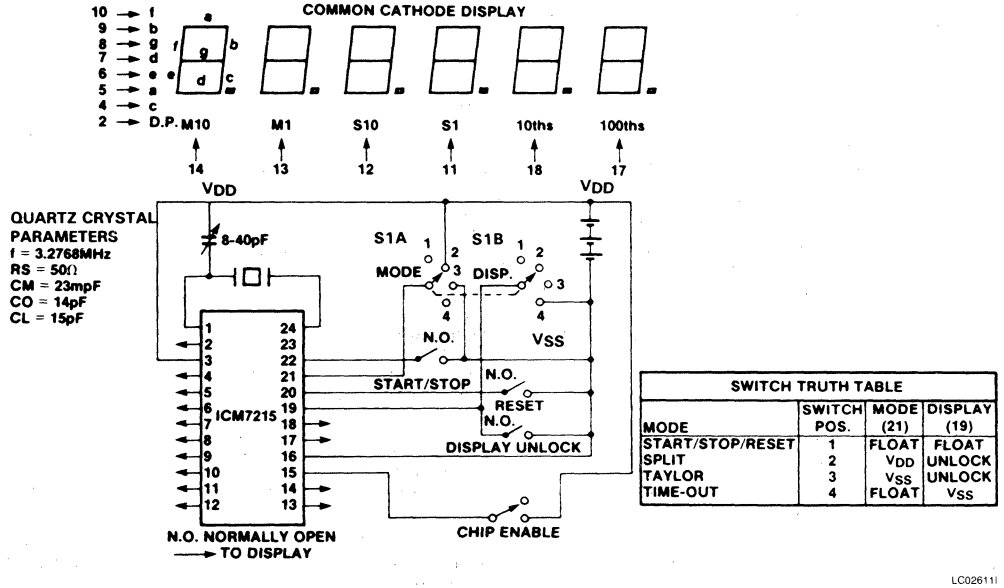
Supply Voltage (V_{DD} to V_{SS}) 5.5V
Power Dissipation (Note 1) 0.75W
Operating Temperature ..... −20°C to +70°C
Storage Temperature ..... −55°C to +125°C
Input Voltage ..... V_{SS} −0.3V to V_{DD} +0.3V
Output Voltage ..... V_{SS} to V_{DD}

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: (T_A = +25°C, stopwatch circuit, V_{DD} = 4.0V, V_{SS} = 0V, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SUPPLY}	Supply Voltage (V_{DD} − V_{SS})	−20°C ≤ T_A ≤ +70°C	2.0		5.0	V
I_{DD}	Supply Current	Display off		0.6	1.5	mA
I_{SEG}	Segment Current Peak Average	5 segments lit 1.8 Volts across display	9.0	 13.2 2.2		
I_{SW}	Switch Actuation Current	All inputs except CHIP ENABLE		20	50	µA
	Switch Actuation Current	Chip enable		50	200	
I_{DLK}	Digit Leakage Current	V_{DIG} = 2.0V			50	
I_{SLK}	Segment Leakage Current	V_{SEG} = 2.0V			100	
V_{LBI}	Low Battery Indicator Trigger Voltage		2.2		2.8	V
I_{LBI}	LBI Output Current	V_{DD} = 2.0V, V_{LBI} = 1.6V		2.0		mA
f_{STAB}	Oscillator Stability	V_{DD} = 2.0V to V_{DD} = 5.0V		6		ppm
g_m	Oscillator Transconductance	V_{DD} = 2.0V	120			µs
C_{OSCI}	Oscillator Input Capacitance			30		pF

NOTE: 1. The output devices on the ICM7215 have very low impedence characteristics, especially the digit cathode drivers. If these devices are shorted to a low impedance power supply, the current could be as high as 300mA.



SWITCH TRUTH TABLE

MODE	SWITCH POS.	MODE (21)	DISPLAY (19)
START/STOP/RESET	1	FLOAT	FLOAT
SPLIT	2	V_{DD}	UNLOCK
TAYLOR	3	V_{SS}	UNLOCK
TIME-OUT	4	FLOAT	V_{SS}

LC02611I

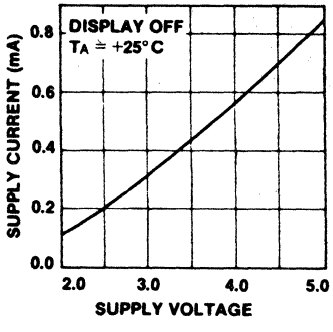
Figure 3: Stopwatch Circuit

Note: All typical values have been guaranteed by characterization and are not tested.

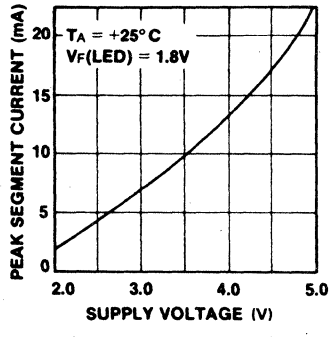
ICM7215

TYPICAL PERFORMANCE CHARACTERISTICS

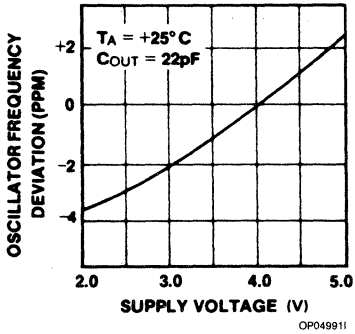
SUPPLY CURRENT VS VOLTAGE



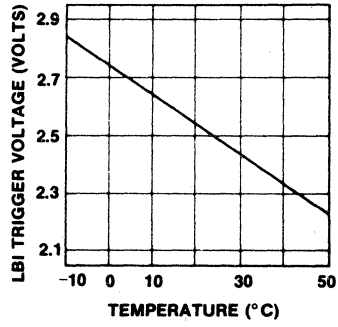
SEGMENT CURRENT VS SUPPLY VOLTAGE



OSC. STABILITY VS SUPPLY VOLTAGE



LOW BATTERY INDICATOR (LBI) TRIGGER VOLTAGE VS TEMPERATURE



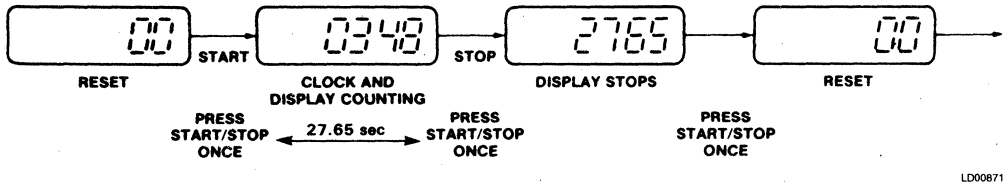


Figure 4: Start/Stop/Reset Mode

DETAILED DESCRIPTION

FUNCTIONAL OPERATION

Turning on the stopwatch will bring up the reset state with the fractional seconds displaying 00 and the other digits blanked. This display always indicates that the stopwatch is ready to go.

The display can be turned off in any mode by connecting the CHIP ENABLE input to V_{DD}.

START/STOP/RESET MODE

When the MODE input is floating and the DISPLAY input is floating or connected to V_{DD} the circuit is in the Start/Stop/Reset mode. (Figure 4).

The Start/Stop/Reset mode can be used for single event timing in a one-button stopwatch; an additional switch can be used to provide an instant reset. To time another event, the display must be reset before the start of the event. Seconds will be displayed after one second, minutes after one minute. The range of the stopwatch is 59 minutes 59.99 seconds, and if an event exceeds one hour, the number of hours must be remembered by the user. Leading zeroes are not blanked after one hour.

Note: All typical values have been guaranteed by characterization and are not tested.

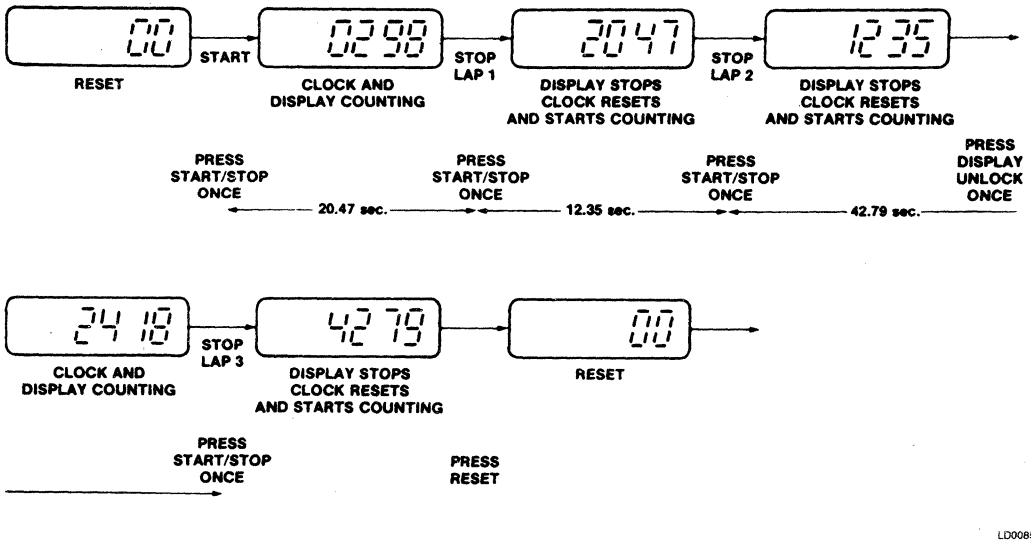


Figure 5: Taylor or Sequential Mode

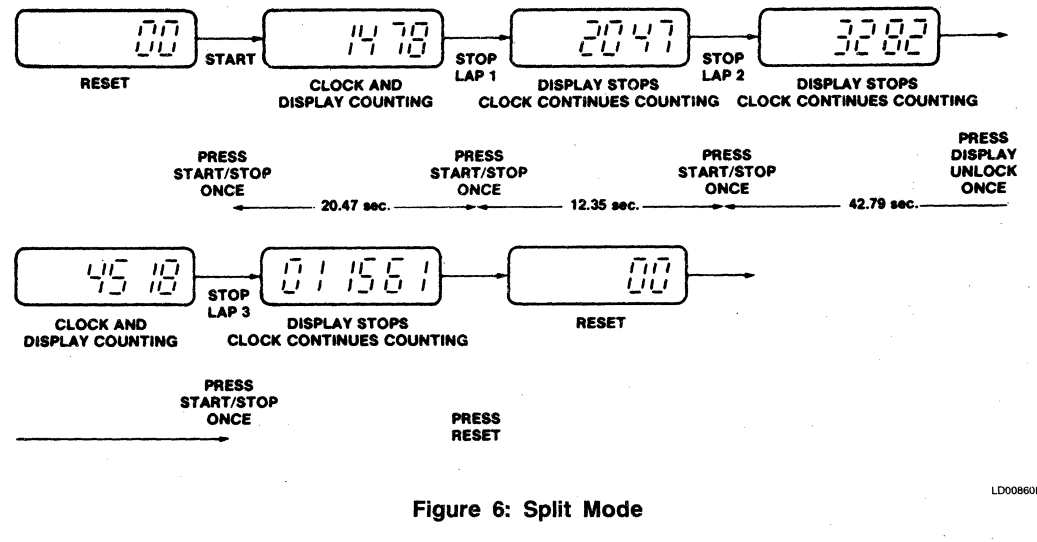


Figure 6: Split Mode

TAYLOR OR SEQUENTIAL MODE

When the MODE input is connected to V_{SS}, the stopwatch is in the Taylor or Sequential mode. (Figure 5).

Each split time is measured from zero in the Taylor mode; i.e., after stopping the watch, the counters reset momentarily and start counting the next interval. The time displayed is that elapsed since the last activation of START/STOP. The display is stationary after the first interval unless the display unlock is used, by connecting the DISPLAY input to V_{SS}, to show the running clock. RESET can be used at any time.

Note: All typical values have been guaranteed by characterization and are not tested.

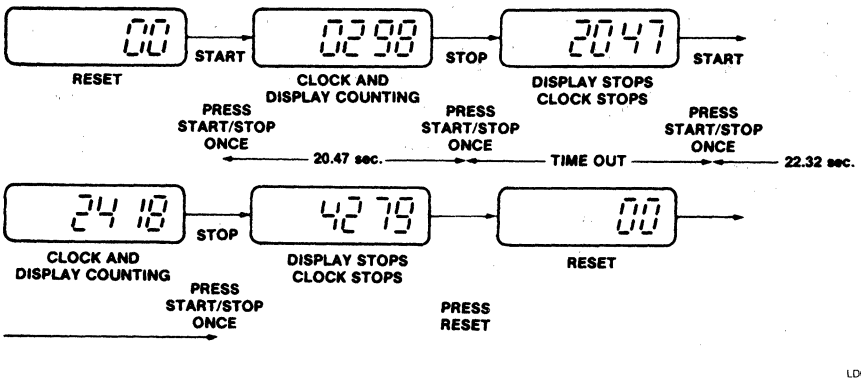


Figure 7: Time-Out Mode

SPLIT MODE

When the MODE input is connected to V_{DD} the stopwatch is in the Split mode. (Figure 6).

The Split mode differs from the Taylor in that the lap times are cumulative in the Split mode. The counters do not reset or stop after the first start until RESET is activated. Time displayed is the cumulative time elapsed since the first start after reset. Display unlock can be used, by connecting the DISPLAY input to V_{SS}, to let the display 'catch up' with the clock, and RESET can be used at any time.

TIME OUT MODE

When the MODE input is floating and the DISPLAY input is tied to V_{SS}, the stopwatch is in the Time-out mode. (Figure 7).

In the Time-out mode the clock and display alternately start and stop with activations of the START/STOP switch. RESET can be used at any time. The display unlock button is bypassed in this mode.

APPLICATION NOTES

LOW BATTERY INDICATOR

The on-chip low battery indicator is intended for use with a small LED or the decimal points on a standard LED display. The output is the drain of a p-channel transistor two-thirds the size of the segment drivers which will typically source 2mA of current. The threshold voltage is approximately 2.5 volts at room temperature. Normal AA type batteries will provide many hours of accurate timekeeping after the indicator comes on, however the wide voltage spread between the LBI threshold voltage and minimum operating voltage is required to guarantee low battery indication under worst case conditions.

CHIP ENABLE

The CHIP ENABLE input is used to disable both segment and digit drivers without affecting any of the functions of the device. When the CHIP ENABLE input is floating or connected to V_{SS}, the display is enabled, and when the tied to V_{DD} the display is turned off. One example of the many possible uses of this feature is driving one display from two ICM7215 devices, one in the split mode and the other in the Taylor mode. The circuit, Figure 8, shows how the user can obtain lap and cumulative readings of the same event.

SWITCH CHARACTERISTICS

The ICM7215 is designed for use with SPST switches throughout. On the DISPLAY and RESET inputs the characteristics of the switches are unimportant, since the circuit responds to a logic level held for any length of time however short. Switch bounce on these inputs does not need to be specified. The START/STOP input, however, responds to an edge and so requires a switch with less than 15ms of switch bounce. The bounce protection circuitry has been specifically designed to let the circuit respond to the first edge of the signal, so as to preserve the full accuracy of the system.

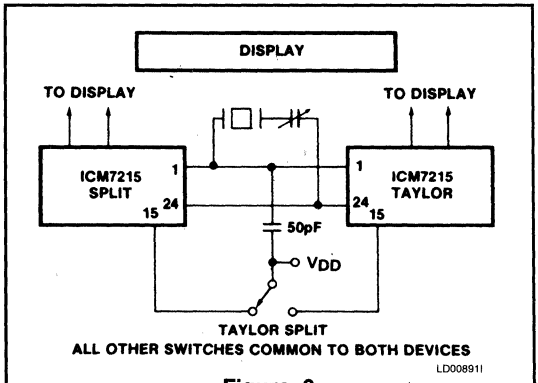


Figure 8

LATCHUP CONSIDERATIONS

Due to the inherent structure of junction isolated CMOS devices, the circuit can be put in a latchup mode if large currents are injected into device inputs or outputs. For this reason special care should be taken in a system with multiple power supplies to prevent voltages being applied to inputs and/or outputs before power is applied to the 7215. If only inputs are affected, latchup can also be prevented by limiting the current into the input terminal to less than 1mA.

Note: All typical values have been guaranteed by characterization and are not tested.

OSCILLATOR DESIGN

The oscillator of the ICM7215 includes all components on chip except the 3.2768MHz crystal and the trimming capacitor. The oscillator input capacitance has a nominal value of 30pF, and the circuit is designed to work with a crystal with a load capacitance of approximately 15pF. If the crystal has characteristics as shown in the Typical Performance Characteristics, an 8–40pF trimming capacitor will be adequate for a tuning tolerance of ±30PPM on the crystal. If the crystal's static capacitance is significantly lower, a narrower trimming range may be selected.

After deciding on a crystal and a nominal load capacitance, take the worst case values of C_{in}, C_{out} and R_S and calculate the g_m required by:

$$g_m = \omega^2 C_{in} C_{out} R_S \left[1 + \frac{C_o (C_{in} + C_{out})}{C_{in} C_{out}}\right]^2$$

C_o = static capacitance

R_S = series resistance

C_{in} = input capacitance

C_{out} = output capacitance

$\omega = 2\pi$ x crystal frequency

The resulting g_m should be less than half the g_m specified for the device. If it is not, a lower value of crystal series resistance and/or load capacitance should be specified.

OSCILLATOR TUNING

Tuning can be accomplished by using the 10th or 100th seconds with the device reset. The frequency on the cathode should be tuned to 1066.667Hz, which is equivalent to a period of 937.5 microseconds. Note that a frequency counter cannot be connected directly to the oscillator because of possible loading.

TEST

The TEST input is used for high speed testing of the device. When the input is pulsed low, a latch is set which speeds up counting by a factor of 32; each pulse on the TEST input rapidly advances both minutes and seconds in a parallel mode. To accurately rapid advance the signal applied to the TEST input must be free of switch bounce. The circuit is taken out of the test mode by using either RESET or START/STOP.

REPLACING THE ICM7205 WITH THE ICM7215

The ICM7215 is designed to be compatible with circuits using the ICM7205. If the 7205 is used only in the Split mode no changes are required. If the 7205 is used in the Taylor mode and the Split-Taylor input (pin 21) is left open, a jumper from pin 21 to V_{SS} must be added when converting to the 7215. A jumper may also be needed if the 7205 is used with a Split/Taylor switch. Once the jumper has been added the board can be used with either device.

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7216A/B/C/D
8-Digit Multi-Function Frequency Counter/Timer

INTERSIL

GENERAL DESCRIPTION

The ICM7216A and B are fully integrated Timer Counters with LED display drivers. They combine a high frequency oscillator, a decade timebase counter, an 8-decade data counter and latches, a 7-segment decoder, digit multiplexers and 8 segment and 8 digit drivers which directly drive large multiplexed LED displays. The counter inputs have a maximum frequency of 10MHz in frequency and unit counter modes and 2MHz in the other modes. Both inputs are digital inputs. In many applications, amplification and level shifting will be required to obtain proper digital signals for these inputs.

The ICM7216A and B can function as a frequency counter, period counter, frequency ratio (f_A/f_B) counter, time interval counter or as a totalizing counter. The counter uses either a 10MHz or 1MHz quartz crystal timebase. For period and time interval, the 10MHz timebase gives a 0.1 μs resolution. In period average and time interval average, the resolution can be in the nanosecond range. In the frequency mode, the user can select accumulation times of 0.01 sec, 0.1 sec, 1 sec and 10 sec. With a 10 sec accumulation time, the frequency can be displayed to a resolution of 0.1Hz in the least significant digit. There is 0.2 seconds between measurements in all ranges.

The ICM7216C and D function as frequency counters only, as described above.

All versions of the ICM7216 incorporate leading zero blanking. Frequency is displayed in kHz. In the ICM7216A and B, time is displayed in μs. The display is multiplexed at 500Hz with a 12.2% duty cycle for each digit. The ICM7216A and C are designed for common anode display with typical peak segment currents of 25mA. The ICM7216B and D are designed for common cathode displays with typical peak segment currents of 12mA. In the display off mode, both digit and segment drivers are turned off, enabling the display to be used for other functions.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7216A/D	−20°C to +85°C	DICE
ICM7216AIJL	−20°C to +85°C	28 pin CERDIP
ICM7216B/D	−20°C to +85°C	DICE
ICM7216BIPI	−20°C to +85°C	28 pin PLASTIC DIP
ICM7216BIJL	−20°C to +85°C	28 pin CERDIP
ICM7216C/D	−20°C to +85°C	DICE
ICM7216CIJL	−20°C to +85°C	28 pin CERDIP
ICM7216D/D	−20°C to +85°C	DICE
ICM7216DIPI	−20°C to +85°C	28 pin PLASTIC DIP
ICM7216DIJL	−20°C to +85°C	28 pin CERDIP

FEATURES

ALL VERSIONS:

- **Functions as a Frequency Counter (DC to 10MHz)**
- **Four Internal Gate Times: 0.01 Sec, 0.1 Sec, 1 Sec, 10 Sec in Frequency Counter Mode**
- **Directly Drives Digits and Segments of Large Multiplexed LED Displays (Common Anode and Common Cathode Versions)**
- **Single Nominal 5V Supply Required**
- **Highly Stable Oscillator, Uses 1MHz or 10MHz Crystal**
- **Internally Generated Decimal Points, Interdigit Blanking, Leading Zero Blanking and Overflow Indication**
- **Display Off Mode Turns Off Display and Puts Chip Into Low Power Mode**
- **Hold and Reset Inputs for Additional Flexibility**

ICM7216A AND ICM7216B

- **Functions Also as a Period Counter, Unit Counter, Frequency Ratio Counter or Time Interval Counter**
- **1 Cycle, 10 Cycles, 100 Cycles, 1000 Cycles in Period, Frequency Ratio and Time Interval Modes**
- **Measures Period From 0.5μs to 10s**

ICM7216C AND ICM7216D

- **Decimal Point and Leading Zero Blanking May Be Externally Selected**

202815-002

Note: All typical values have been guaranteed by characterization and are not tested.

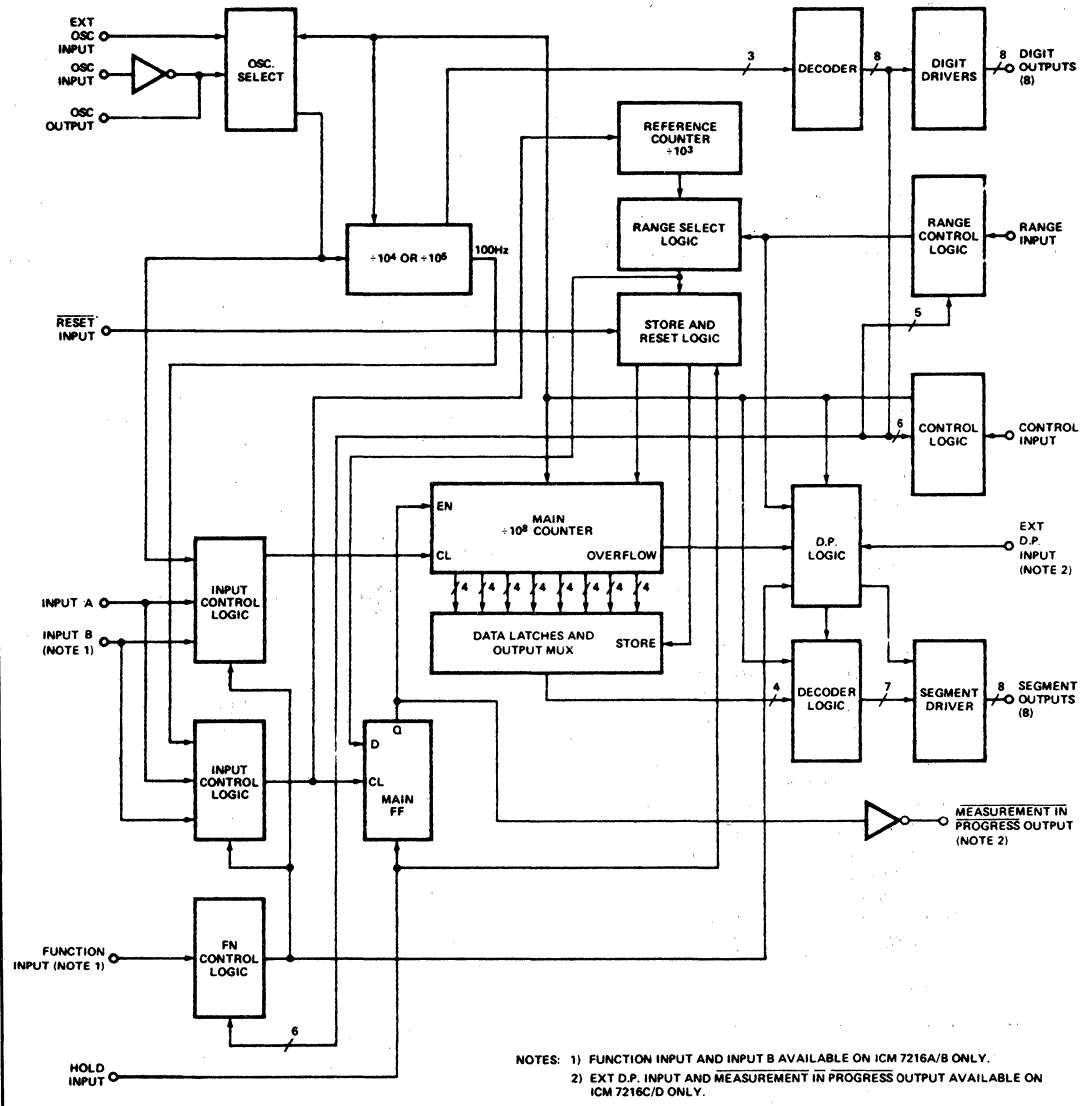


Figure 1: Functional Diagram

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7216A/B/C/D

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Maximum Supply Voltage ($V_{DD} - V_{SS}$) 6.5V
Maximum Digit Output Current 400mA
Maximum Segment Output Current.....60mA
Voltage On Any Input or
Output Terminal[1].....V_{DD} + 0.3V to V_{SS} - 0.3V

Maximum Power Dissipation at
70°C.....1.0W (ICM7216A & C)
0.5W (ICM7216B & D)
Operating Temperature Range .....-20°C to +85°C
Storage Temperature Range .....-55°C to +125°C
Lead Temperature (Soldering, 10sec) .....300°C

Note: 1. The ICM7216 may be triggered into a destructive latchup mode if either input signals are applied before the power supply is applied or if input or outputs are forced to voltages exceeding V_{DD} to V_{SS} by more than 0.3 volts.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

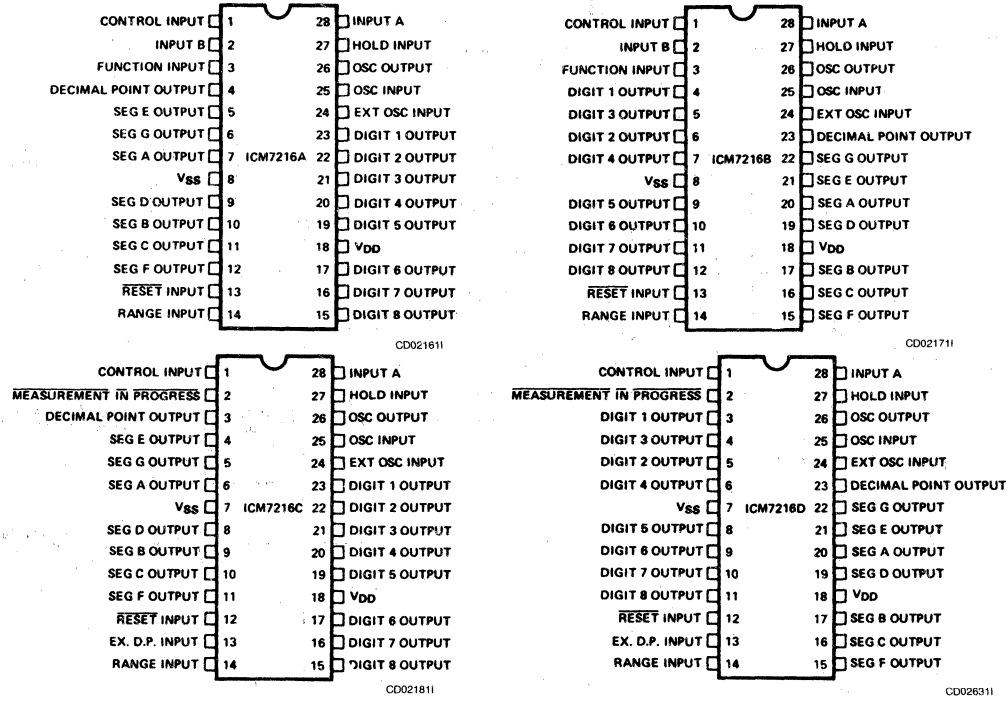


Figure 2: Pin Configurations

EVALUATION KIT

The ICM7226 Universal Counter System has all of the features of the ICM7216 plus a number of additional features. The ICM7226 Evaluation Kit consists of the ICM7226AIJL (Common Anode LED Display), a 10MHz quartz crystal, eight 7 segment 0.3" LED's, P.C. board, resistors, capacitors, diodes, switches, socket: everything needed to quickly assemble a functioning ICM7226 Universal Counter System.

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7216A/B/C/D

INTERSIL

ELECTRICAL CHARACTERISTICS (ICM7216A/B)

(V_{DD} = 5.0V ±5%, V_{SS} = 0, T_A = 25°C, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	ICM7216A/B					
I_{DD}	Operating Supply Current	Display Off, Unused Inputs to V_{SS}		2	5	mA
V_{SUPPLY}	Supply Voltage Range ($V_{DD} - V_{SS}$)	$-20°C < T_A < +85°C$, INPUT A, INPUT B Frequency at f_{max}	4.75		6.0	V
$f_{A(max)}$	Maximum Frequency INPUT A, Pin 28	$-20°C < T_A < +85°C$ $4.75 < V_{DD} \leq 6.0V$, Figure 3, Function = Frequency, Ratio, Unit Counter Function = Period, Time Interval	 10 2.5			 MHz MHz
$f_{B(max)}$	Maximum Frequency INPUT B, Pin 2	$-20°C < T_A < +85°C$ $4.75 < V_{DD} \leq 6.0V$, Figure 4	 2.5			 MHz
	Minimum Separation INPUT A to INPUT B Time Interval Function	$-20°C < T_A < +85°C$ $4.75 < V_{DD} \leq 6.0V$, Figure 5	 250			 ns
f_{osc}	Maximum Osc. Freq. and Ext. Osc. Frequency	$-20°C < T_A < +85°C$ $4.75 < V_{DD} \leq 6.0V$	 10			 MHz
f_{osc}	Minimum Ext. Osc. Freq.				100	kHz
g_m	Oscillator Transconductance	V_{DD} = 4.75V, T_A = +85°C	2000			µs
f_{mux}	Multiplex Frequency	f_{osc} = 10MHz		500		Hz
	Time Between Measurements	f_{osc} = 10MHz		200		ms
 V_{INL} V_{INH}	Input Voltages: Pins 2,13,25,27,28 Input Low Voltage Input High Voltage	$-20°C < T_A < +85°C$	 3.5		 1.0	 V V
R_{IN}	Input Resistance to V_{DD} Pins 13,24	$V_{IN} = V_{DD} - 1.0V$	100	400		kΩ
I_{ILK}	Input Leakage Pin 27,28,2				20	µA
dV_{IN}/dt	Input Range of Change	Supplies Well Bypassed		15		mV/µs
	ICM7216A					
 I_{OH} I_{OL}	Digit Driver: Pins 15,16,17,19,20,21,22,23 High Output Current Low Output Current	 $V_{OUT} = V_{DD} - 2.0V$ $V_{OUT} = V_{SS} + 1.0V$	 -140	 -180 +0.3		 mA mA
 I_{OL} I_{OH}	SEGment Driver: Pins 4,5,6,7,9,10,11,12 Low Output Current High Output Current	 $V_{OUT} = V_{SS} + 1.5V$ $V_{OUT} = V_{DD} - 2.5V$	 20	 35 -100		 mA µA
 V_{INL} V_{INH} R_{IN}	Multiplex Inputs: Pins 1,3,14 Input Low Voltage Input High Voltage Input Resistance to V_{SS}	 $V_{IN} = V_{SS} + 1.0V$	 2.0 50	 100	 0.8	 V V kΩ
	ICM7216B					
 I_{OL} I_{OH}	Digit Driver: Pins 4,5,6,7,9,10,11,12 Low Output Current High Output Current	 $V_{OUT} = V_{SS} + 1.3V$ $V_{OUT} = V_{DD} - 2.5V$	 50	 75 -100		 mA µA
 I_{OH} I_{SLK}	SEGment Driver: Pins 15,16,17,19,20,21,22,23 High Output Current Leakage Current	 $V_{OUT} = V_{DD} - 2.0V$ $V_{OUT} = V_{DD} - 2.5V$	 -10		 10	 mA µA
 V_{INL} V_{INH} R_{IN}	Multiplex Inputs: Pins 1,3,14 Input Low Voltage Input High Voltage Input Resistance to V_{DD}	 $V_{IN} = V_{DD} - 2.5V$	 $V_{DD} - 0.8$ 100	 360	 $V_{DD} - 2.0$	 V V kΩ

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7216A/B/C/D

INTERSIL

ELECTRICAL CHARACTERISTICS (ICM7216C/D)

(V_{DD} = 5.0V ±5%, V_{SS} = 0, T_A = 25°C, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	ICM7216C/D					
I_{DD}	Operating Supply Current	Display Off, Unused Inputs to V_{SS}		2	5	mA
V_{SUPPLY}	Supply Voltage Range ($V_{DD} - V_{SS}$)	$-20°C < T_A < +85°C$, INPUT A Frequency at f_{max}	4.75		6.0	V
$f_{A(max)}$	Maximum Frequency INPUT A, Pin 28	$-20°C < T_A < +85°C$ $4.75 < V_{DD} < 6.0V$, Figure 3	10			MHz
f_{osc}	Maximum Osc. Freq. and Ext. Osc. Frequency	$-20°C < T_A < +85°C$ $4.75 < V_{DD} < 6.0V$	10			MHz
f_{osc}	Minimum Ext. Osc. Freq.				100	kHz
g_m	Oscillator Transconductance	V_{DD} = 4.75V, T_A = +85°C	2000			µs
f_{mux}	Multiplex Frequency	f_{osc} = 10MHz		500		Hz
	Time Between Measurements	f_{osc} = 10MHz		200		ms
V_{INL} V_{INH}	Input Voltages: Pins 12,27,28 Input Low Voltage Input High Voltage	$-20°C < T_A < +85°C$	3.5		1.0	V V
R_{IN}	Input Resistance to V_{DD} Pins 12,24	$V_{IN} = V_{DD} - 1.0V$	100	400		kΩ
I_{ILK}	Input Leakage Pin 27, Pin 28				20	µA
I_{OL}	Output Current	V_{OL} = +.4V	0.36			mA
I_{OH}	Pin 2	$V_{OH} = V_{DD} - 0.8V$	265			µA
dV_{IN}/dt	Input Rate of Change	Supplies Well Bypassed		15		mV/µs
	ICM7216C					
I_{OH} I_{OL}	Digit Driver: Pins 15,16,17,19,20,21,22,23 High Output Current Low Output Current	$V_{OUT} = V_{DD} - 2.0V$ $V_{OUT} = V_{SS} + 1.0V$	−140	−180 0.3		mA mA
I_{OL} I_{OH}	SEGment Driver: Pins 3,4,5,6,8,9,10,11 Low Output Current High Output Current	$V_{OUT} = V_{SS} + 1.5V$ $V_{OUT} = V_{DD} - 2.5V$	20	30 −100		mA µA
V_{INL} V_{INH} R_{IN}	Multiplex Inputs: Pins 1,13,14 Input Low Voltage Input High Voltage Input Resistance to V_{SS}	V_{IN} = +1.0V	2.0 50	100	0.8	V V kΩ
	ICM7216D					
I_{OL} I_{OH}	Digit Driver: Pins 3,4,5,6,8,9,10,11 Low Output Current High Output Current	V_{OUT} = +1.3V $V_{OUT} = V_{DD} - 2.5V$	50	75 100		mA µA
I_{OH} I_{SLK}	SEGment Driver: Pins 15,16,17,19,20,21,22,23 High Output Current Leakage Current	$V_{OUT} = V_{DD} - 2.0V$ $V_{OUT} = V_{DD} - 2.5V$	10	15	10	mA µA
V_{INL} V_{INH} R_{IN}	Multiplex Inputs: Pins 1,13,14 Input Low Voltage Input High Voltage Input Resistance to V_{DD}	$V_{IN} = V_{DD} - 1.0V$	$V_{DD} - 0.8$ 100	360	$V_{DD} - 2.0$	V V kΩ

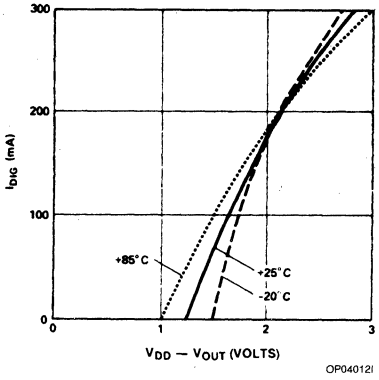
Note: All typical values have been guaranteed by characterization and are not tested.

ICM7216A/B/C/D

INTERSIL

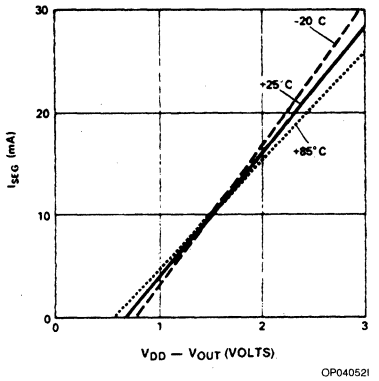
TYPICAL PERFORMANCE CHARACTERISTICS

ICM7216A & C Typical I_{DIG} vs. V_{DD} $-V_{OUT}$, $4.5 \leq V_{DD} \leq 6.0V$



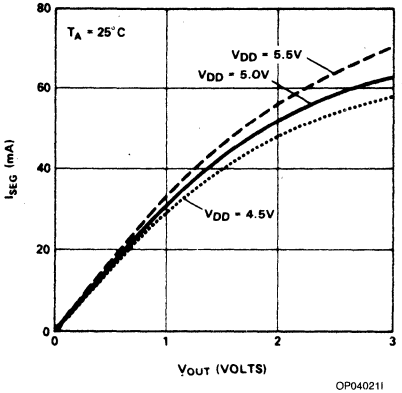
OP04012I

ICM7216B & D Typical I_{SEG} vs. V_{DD} $-V_{OUT}$, $4.5 \leq V_{DD} \leq 6.0V$

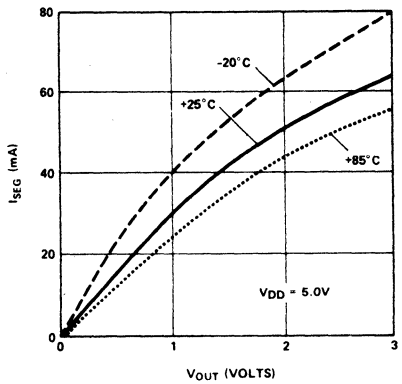


OP04052I

ICM7216A & C Typical I_{SEG} vs. V_{OUT}

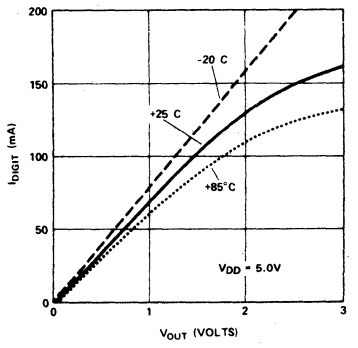


OP04021I

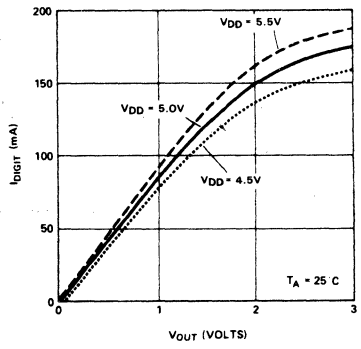


OP04031I

ICM7216B & D Typical I_{DIGIT} vs. V_{OUT}



(a)



(b)

OP04041I

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7216A/B/C/D

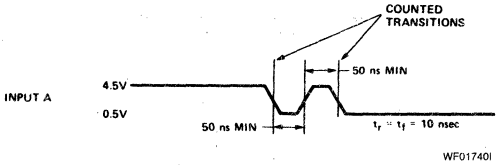


Figure 3: Waveform for Guaranteed Minimum f_A(max) Function = Frequency, Frequency Ratio, Unit Counter.

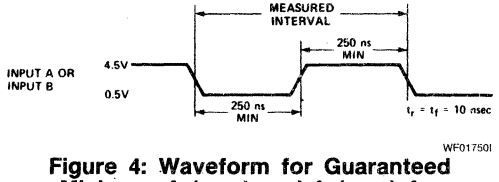


Figure 4: Waveform for Guaranteed Minimum f_B(max) and f_A(max) for Function = Period and Time Interval.

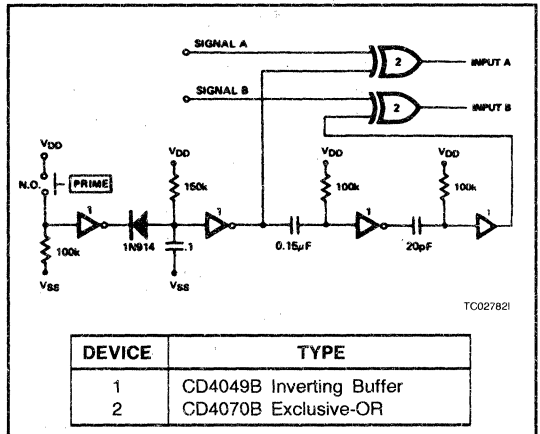
TIME INTERVAL MEASUREMENT

The ICM7216A/B can be used to accurately measure the time interval between two events. With a 10MHz time-base crystal, the time between the two events can be as long as ten seconds. Accurate resolution in time interval measurement is 100ns.

The feature operates with Channel A going low at the start of the event to be measured, followed by Channel B going low at the end of the event.

When in the **time interval** mode and measuring a single event, the ICM7216A/B must first be "primed" prior to measuring the event of interest. This is done by first generating a negative going edge on Channel A followed by a negative going edge on Channel B to start the "measurement interval." The inputs are then primed ready for the measurement. Positive going edges on A and B, before or after the priming, will be needed to restore the original condition.

This can be easily accomplished with the following circuit: (Figure 5).



DEVICE	TYPE
1	CD4049B Inverting Buffer
2	CD4070B Exclusive-OR

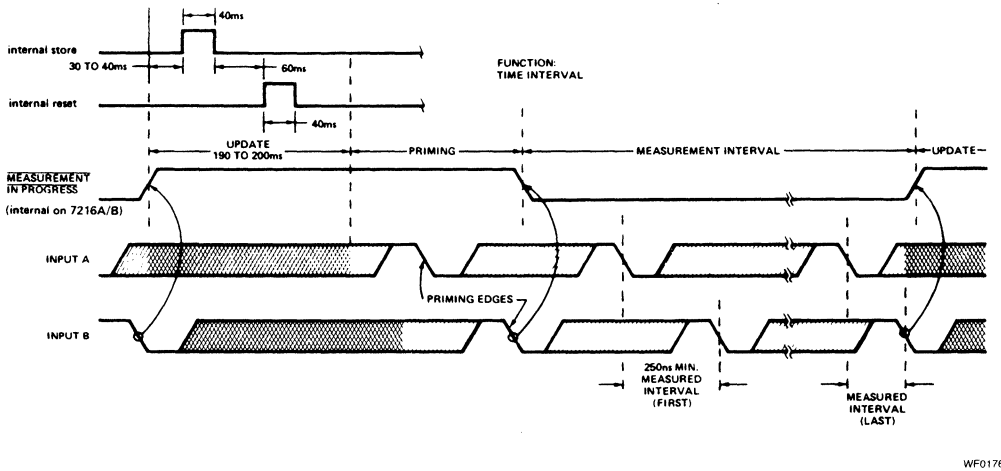
Figure 5: Priming Circuit, Signal A&B High or Low.

Following the priming procedure (when in single event or 1 cycle range input) the device is ready to measure one (only) event.

When timing repetitive signals, it is not necessary to "prime" the ICM7216A/B as the first alternating signal states automatically prime the device. See Figure 5.

During any time interval measurement cycle, the ICM7216A/B requires 200ms following B going low to update all internal logic. A new measurement cycle will not take place until completion of this internal update time.

Note: All typical values have been guaranteed by characterization and are not tested.



NOTE: IF RANGE IS SET TO 1 EVENT, FIRST AND LAST MEASURED INTERVAL WILL COINCIDE.

Figure 6: Waveforms for Time Interval Measurement (Others are similar, but without priming phase).

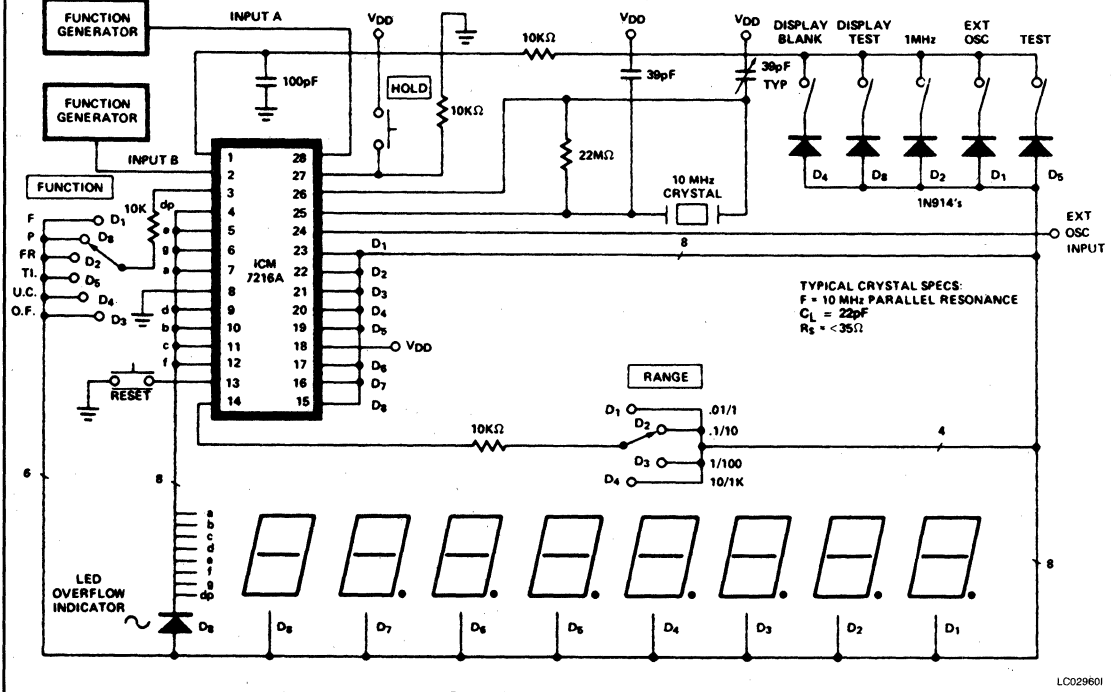
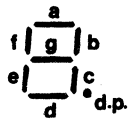


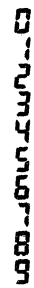
Figure 7: Test Circuit (7216A shown; others similar)

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7216A/B/C/D



LC01780I



LC01790I

Overflow will be indicated on the decimal point output of digit 8.

A separate LED overflow indicator can be connected as follows:

	CATHODE	ANODE
ICM7216A/C	DEC. PT.	D_8
ICM7216B/D	D_8	DEC. PT.

Figure 8: Segment Identification and Display Font

DETAILED DESCRIPTION

INPUTS A and B

INPUTS A and B are digital inputs with a typical switching threshold of 2.0V at V_{DD} = 5.0V. For optimum performance the peak-to-peak input signal should be at least 50% of the supply voltage and centered about the switching voltage. When these inputs are being driven from TTL logic, it is desirable to use a pullup resistor. The circuit counts high to low transitions at both inputs. (INPUT B is available only on ICM7216A/B).

Note: The amplitude of the input should not exceed the supply, otherwise, the circuit may be damaged.

Multiplexed Inputs

The FUNCTION, RANGE, CONTROL and EXTERNAL DECIMAL POINT inputs are time multiplexed to select the input function desired. This is achieved by connecting the appropriate Digit driver output to the inputs. The input function, range and control inputs must be stable during the last half of each digit output, (typically 125μs). The multiplex inputs are active high for the common anode ICM7216A and C and active low for the common cathode ICM7216B and D.

Noise on the multiplex inputs can cause improper operation. This is particularly true when the **unit counter** mode of operation is selected, since changes in voltage on the digit drivers can be capacitively coupled through the LED diodes to the multiplex inputs. For maximum noise immunity, a 10kΩ resistor should be placed in series with the multiplex inputs as shown in the application circuits.

Table 1 shows the functions selected by each digit for these inputs.

CONTROL INPUT Functions

Display Test — All segments are enabled continuously, giving a display of all 8's with decimal points. The display will be blanked if Blank Display is selected at the same time.

Display Off — To disable the drivers, it is necessary to tie D_4 to the CONTROL INPUT and have the HOLD input at V_{DD}. The chip will remain in this "Display Off" mode until HOLD is switched back to V_{SS}. While in the "Display Off" mode, the segment and digit driver outputs are open, the oscillator continues to run with a typical supply current of 1.5mA with a 10MHz crystal, and no measurements are made. In addition, inputs to the multiplexed inputs will have no effect. A new measurement is initiated when the HOLD input is switched to V_{SS}. Segment and Digit Drive outputs may thus be bussed to drive a common display (up to 6 circuits).

1MHz Select — The 1MHz select mode allows use of a 1MHz crystal with the same digit multiplex rate and time between measurements as with a 10MHz crystal. The decimal point is also shifted one digit to the right in Period and Time Interval, since the least significant digit will be in μs increments rather than 0.1μs increments.

External Oscillator Enable — In this mode the EXTERNAL OSCILLATOR INPUT is used instead of the on-chip oscillator for Timebase input and Main Counter input in **period** and **time interval modes**. The on-chip oscillator will continue to function when the external oscillator is selected. The external oscillator input frequency must be greater than 100kHz or the chip will reset itself to enable the on-chip oscillator. OSCillator INPUT (pin 25) must also be connected to EXT.OSC. input when using EXT.OSC. input.

External Decimal Point Enable — When external decimal point is enabled a decimal point will be displayed whenever the digit driver connected to EXTERNAL DECIMAL POINT input is active. Leading Zero Blanking will be disabled for all digits following the decimal point (7216C/D only).

RANGE INPUT

The RANGE INPUT selects whether the measurement is made for 1, 10, 100, 1000 counts of the reference counter. In all functional modes except **unit counter** a change in the RANGE INPUT will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the RANGE INPUT is changed.

Note: All typical values have been guaranteed by characterization and are not tested.

Table 1: Multiplexed Input Functions

	FUNCTION	DIGIT
FUNCTION INPUT Pin 3 (ICM7216A & B Only)	Frequency	D_1
	Period	D_8
	Frequency Ratio	D_2
	Time Interval	D_5
	Unit Counter	D_4
	Oscillator Frequency	D_3
RANGE INPUT Pin 14	.01 sec/1 Cycle	D_1
	.1 sec/10 Cycles	D_2
	1 sec/100 Cycles	D_3
	10 sec/1K Cycles	D_4
CONTROL INPUT Pin 1	Blank Display	D_4 and Hold
	Display Test	D_8
	1 MHz Select	D_2
	External Oscillator Enable	D_1
	External Decimal Point Enable	D_3
EXT. D.P. INPUT Pin 13, ICM7216C & D Only	Decimal point is output for same digit that is connected to this input	

FUNCTION INPUT

The six functions that can be selected are: **Frequency, Period, Time Interval, Unit Counter, Frequency Ratio** and **Oscillator Frequency.** This input is available on the ICM7216A and B only.

These functions select which signal is counted into the Main Counter and which signal is counted by the Reference Counter, as shown in Table 2. In all cases, only 1→0 transitions are counted or timed. In **time interval**, a flip-flop is toggled first by a 1→0 transition of INPUT A and then by a 1→0 transition of INPUT B. The oscillator is gated into the Main Counter from the time INPUT A toggles the flip-flop until INPUT B toggles it. In **unit counter** mode, the main counter contents are continuously displayed. A change in the FUNCTION INPUT will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the FUNCTION INPUT is changed.

Table 2: 7216A/B Input Routing

DESCRIPTION	MAIN COUNTER	REFERENCE COUNTER
Frequency (f_A)	Input A	100 Hz (Oscillator $\div 10^5$ or 10^4)
Period (t_A)	Oscillator	Input A
Ratio (f_A/f_B)	Input A	Input B
Time Interval (A→B)	Osc•(Time Interval FF)	Time Interval FF
Unit Counter (Count A)	Input A	Not Applicable
Osc. Freq. (f_{osc})	Oscillator	100 Hz (Oscillator $\div 10^5$ or 10^4)

EXTernal DECimal Point INput

When the **external decimal point** is selected this input is active. Any of the digits, except D_8, can be connected to this point. D_8 should not be used since it will override the overflow output and leading zeros will remain unblanked after the decimal point. This input is available on the ICM7216C and D only.

HOLD Input — Except in the **unit counter** mode, when the HOLD Input is at V_{DD}, any measurement in progress (before $\overline{\text{STORE}}$ goes low) is stopped, the main counter is reset and the chip is held ready to initiate a new measurement as soon as HOLD goes low. The latches which hold the main counter data are not updated, so the last complete measurement is displayed. In **unit counter** mode when HOLD input is at V_{DD}, the counter is not stopped or reset, but the display is frozen at that instantaneous value. When HOLD goes low the count continues from the new value in the counter.

$\overline{\text{RESET}}$ Input — The $\overline{\text{RESET}}$ input resets the main counter, stops any measurement in progress, and enables the main counter latches, resulting in an all zero output. A capacitor to ground will prevent any hang-ups on power-up.

DISPLAY CONSIDERATIONS

The display is multiplexed at a 500Hz rate with a digit time of 244 μs. An interdigit blanking time of 6 μs is used to prevent ghosting between digits. The decimal point and leading zero blanking assume right hand decimal point displays, and zeros following the decimal point will not be blanked. Also, the leading zero blanking will be disabled when the Main Counter overflows. Overflow is indicated by the decimal point on digit 7 turning on.

The ICM7216A and C are designed to drive common anode LED displays at peak current of 25mA/segment, using displays with $V_F = 1.8V$ at 25mA. The average DC current will be over 3mA under these conditions. The ICM7216B and D are designed to drive common cathode displays at peak current of 15mA/segment using displays with $V_F = 1.8V$ at 15mA. Resistors can be added in series with the segment drivers to limit the display current in very efficient displays, if required. The Typical Performance Characteristics curves show the digit and segment currents as a function of output voltage.

To get additional brightness out of the displays, V_{DD} may be increased up to 6.0V. However, care should be taken to see that maximum power and current ratings are not exceeded.

The segment and digit outputs in ICM7216's are not directly compatible with either TTL or CMOS logic when driving LEDs. Therefore, level shifting with discrete transistors may be required to use these outputs as logic signals.

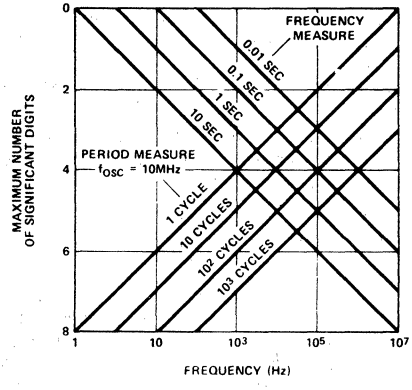
ACCURACY

In a Universal Counter crystal drift and quantization effects cause errors. In **frequency, period** and **time interval** modes, a signal derived from the oscillator is used in either the Reference Counter or Main Counter. Therefore, in these modes an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficient of 20ppm/°C will cause a measurement error of 20ppm/°C.

In addition, there is a quantization error inherent in any digital measurement of ±1 count. Clearly this error is reduced by displaying more digits. In the **frequency** mode the maximum accuracy is obtained with high frequency inputs and in **period** mode maximum accuracy is obtained with low frequency inputs. As can be seen in Figure 9, the least accuracy will be obtained at 10kHz. In **time interval**

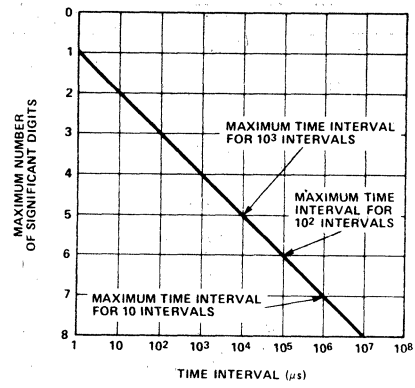
Note: All typical values have been guaranteed by characterization and are not tested.

measurements there can be an error of 1 count per interval. As a result there is the same inherent accuracy in all ranges as shown in Figure 10. In **frequency ratio** measurement can be more accurately obtained by averaging over more cycles of INPUT B as shown in Figure 11.



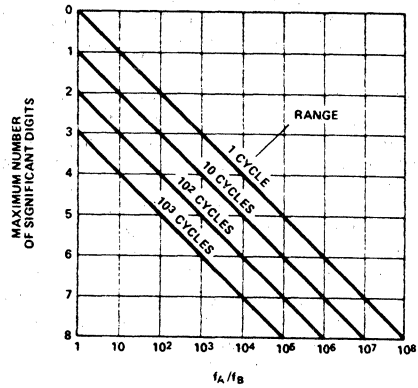
OP04060I

Figure 9: Maximum Accuracy of Frequency and Period Measurements Due to Limitations of Quantization Errors



OP04070I

Figure 10: Maximum Accuracy of Time Interval Measurement Due to Limitations of Quantization Errors



OP04080I

Figure 11: Maximum Accuracy for Frequency Ratio Measurement Due to Limitation of Quantization Errors

Note: All typical values have been guaranteed by characterization and are not tested.

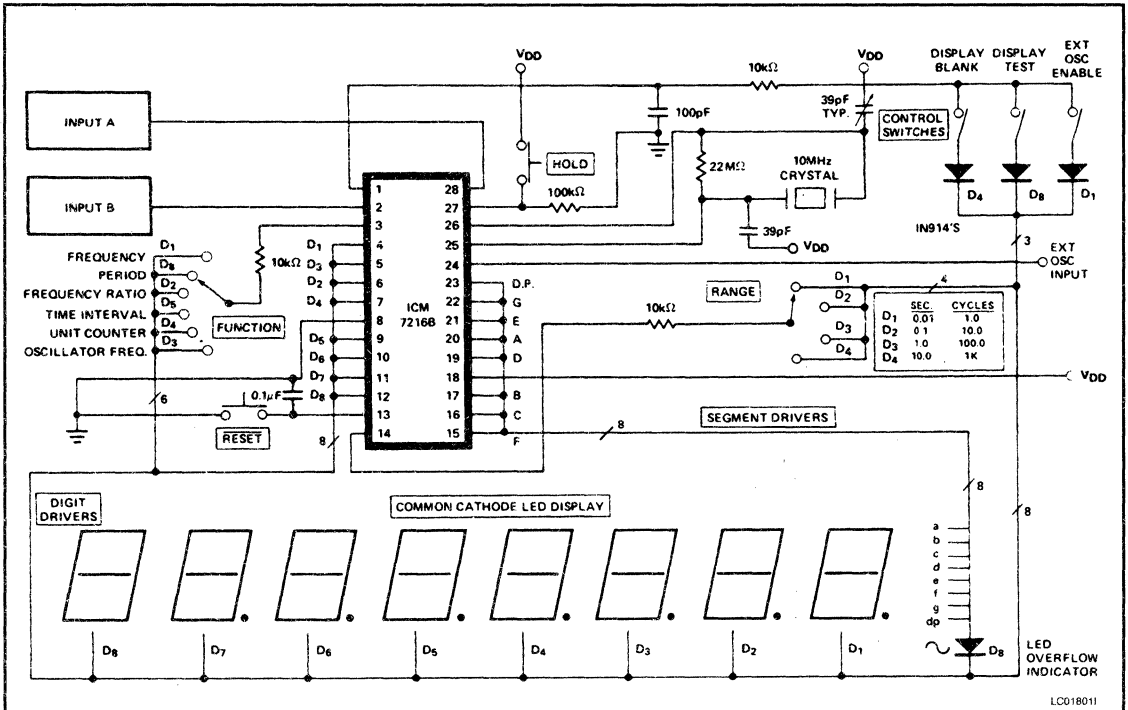


Figure 12: 10MHz Universal Counter

CIRCUIT APPLICATIONS

The ICM7216 has been designed for use in a wide range of Universal and Frequency counters. In many cases, prescalers will be required to reduce the input frequencies to under 10MHz. Because INPUT A and INPUT B are digital inputs, additional circuitry is often required for input buffering, amplification, hysterisis, and level shifting to obtain a good digital signal.

The ICM7216A or B can be used as a minimum component complete Universal Counter as shown in Figure 12. This circuit can use input frequencies up to 10MHz at INPUT A and 2MHz at INPUT B. If the signal at INPUT A has a very low duty cycle it may be necessary to use a 74121 monostable multivibrator or similar circuit to stretch the input pulse width to be able to guarantee that it is at least 50ns in duration.

7

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7216A/B/C/D

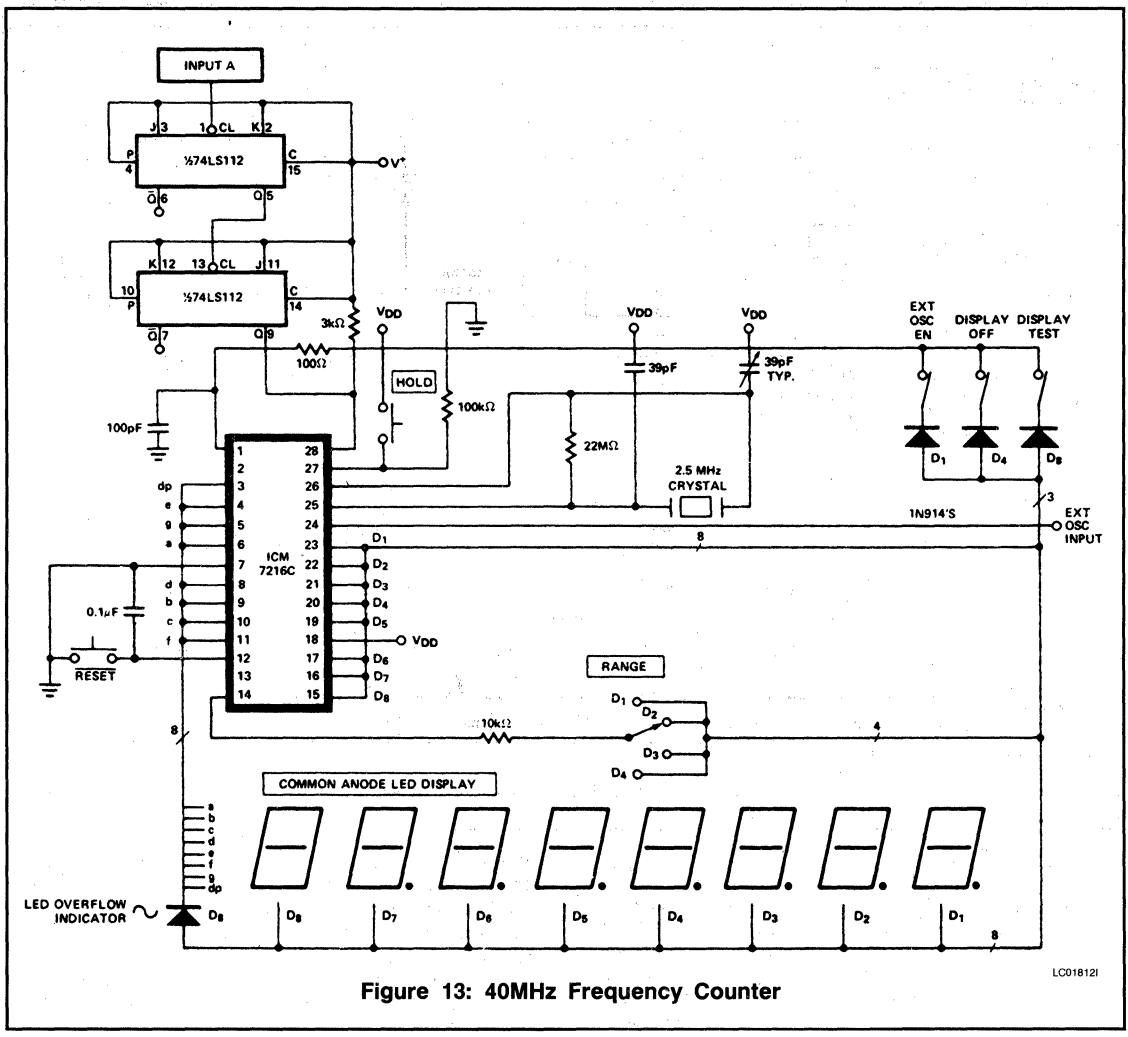


Figure 13: 40MHz Frequency Counter

To measure frequencies up to 40MHz the circuit of Figure 13 can be used. To obtain the correct measured value, it is necessary to divide the oscillator frequency by four as well as the input frequency. In doing this the time between measurements is also lengthened to 800ms and the display multiplex rate is decreased to 125Hz.

Note: All typical values have been guaranteed by characterization and are not tested.

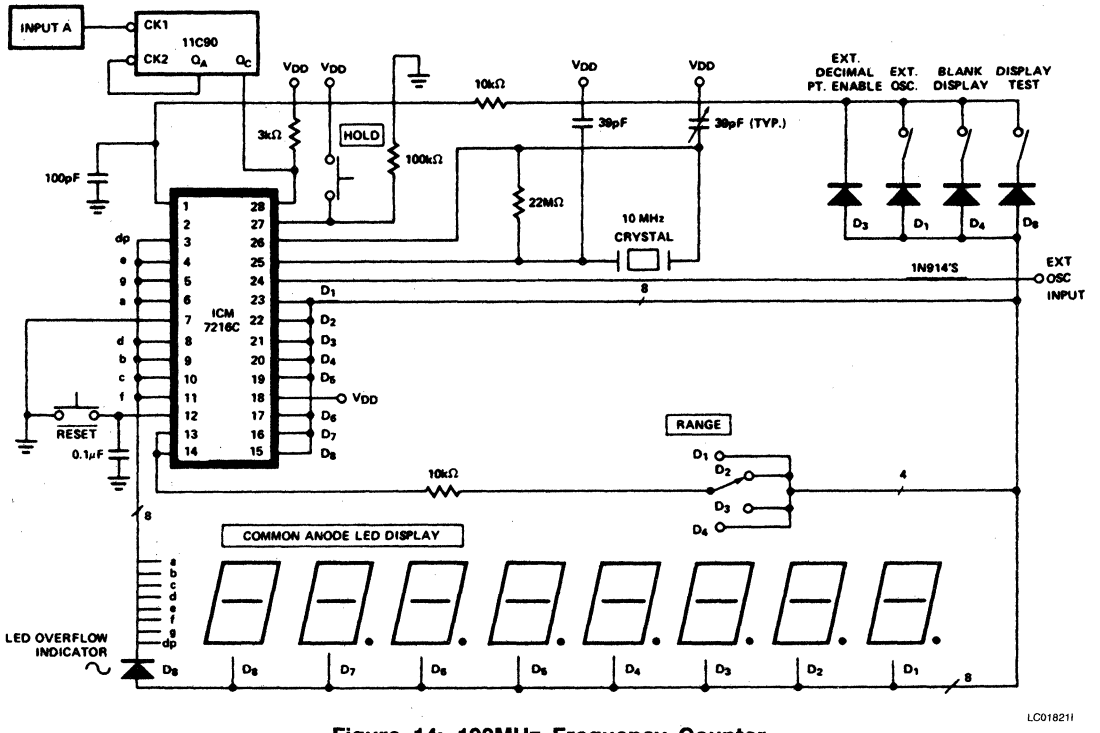


Figure 14: 100MHz Frequency Counter

If the input frequency is prescaled by ten, then the oscillator can remain at 10 or 1MHz, but the decimal point must be moved one digit to the right. Figure 14 shows a frequency counter with a ÷10 prescaler and an ICM7216C. Since there is no external decimal point control with the ICM7216A/B, the decimal point may be controlled externally with additional drivers as shown in Figure 15. Alternatively, if separate anodes are available for the decimal points, they can be wired up to the adjacent digit anodes. Note that there can be one zero to the left of the decimal point since the internal leading zero blanking cannot be changed. In Figure 16 additional logic has been added to count the input directly in **period** mode for maximum accuracy. In Figures 14 through 16, INPUT A comes from Q_C of the prescaler rather than Q_D to obtain an input duty cycle of 40%.

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7216A/B/C/D

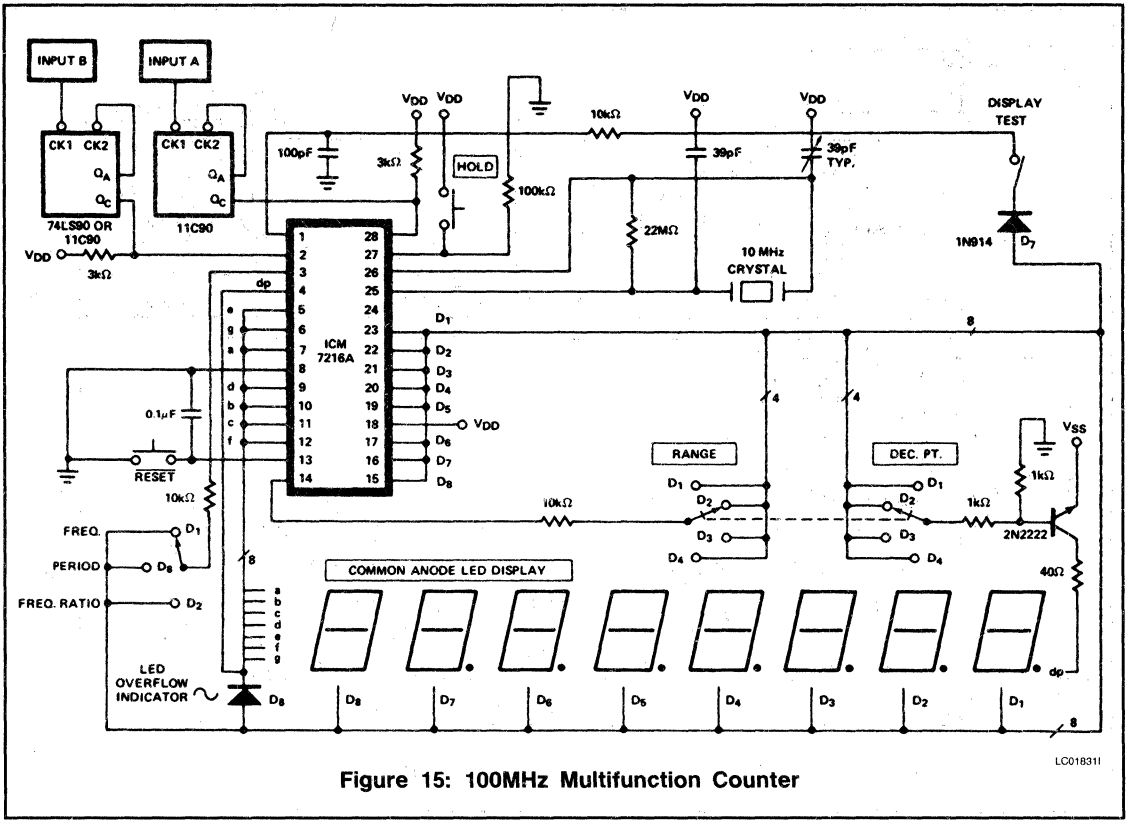


Figure 15: 100MHz Multifunction Counter

OSCILLATOR CONSIDERATIONS

The oscillator is a high gain complementary FET inverter. An external resistor of 10MΩ to 22MΩ should be connected between the OSCillator INPUT and OUTPUT to provide biasing. The oscillator is designed to work with a parallel resonant 10MHz quartz crystal with a static capacitance of 22pF and a series resistance of less than 35 ohms.

For a specific crystal and load capacitance, the required g_m can be calculated as follows:

$$g_m = \omega^2 C_{in} C_{out} Rs\left(1 + \frac{C_O}{C_L}\right)^2$$

where $C_L = \left(\frac{C_{in}C_{out}}{C_{in} + C_{out}}\right)$

C_O = Crystal Static Capacitance

R_S = Crystal Series Resistance

C_{in} = Input Capacitance

C_{out} = Output Capacitance

$\omega = 2\pi f$

The required g_m should not exceed 50% of the g_m specified for the ICM7216 to insure reliable startup. The OSCillator INPUT and OUTPUT pins each contribute about 5pF to C_{in} and C_{out}. For maximum stability of frequency, C_{in} and C_{out} should be approximately twice the specified crystal static capacitance.

In cases where non decade prescalers are used it may be desirable to use a crystal which is neither 10MHz or 1MHz. In that case both the multiplex rate and time between measurements will be different. The multiplex rate is $f_{mux} = \frac{f_{osc}}{2 \times 10^4}$ for 10MHz mode and $f_{mux} = \frac{f_{osc}}{2 \times 10^3}$ for the 1MHz mode. The time between measurements is $\frac{2 \times 10^6}{f_{osc}}$ in the 10MHz mode and $\frac{2 \times 10^5}{f_{osc}}$ in the 1MHz mode.

The crystal and oscillator components should be located as close to the chip as practical to minimize pickup from other signals. Coupling from the EXTERNAL OSCILLATOR INPUT to the OSCILLATOR OUTPUT or INPUT can cause undesirable shifts in oscillator frequency.

Note: All typical values have been guaranteed by characterization and are not tested.

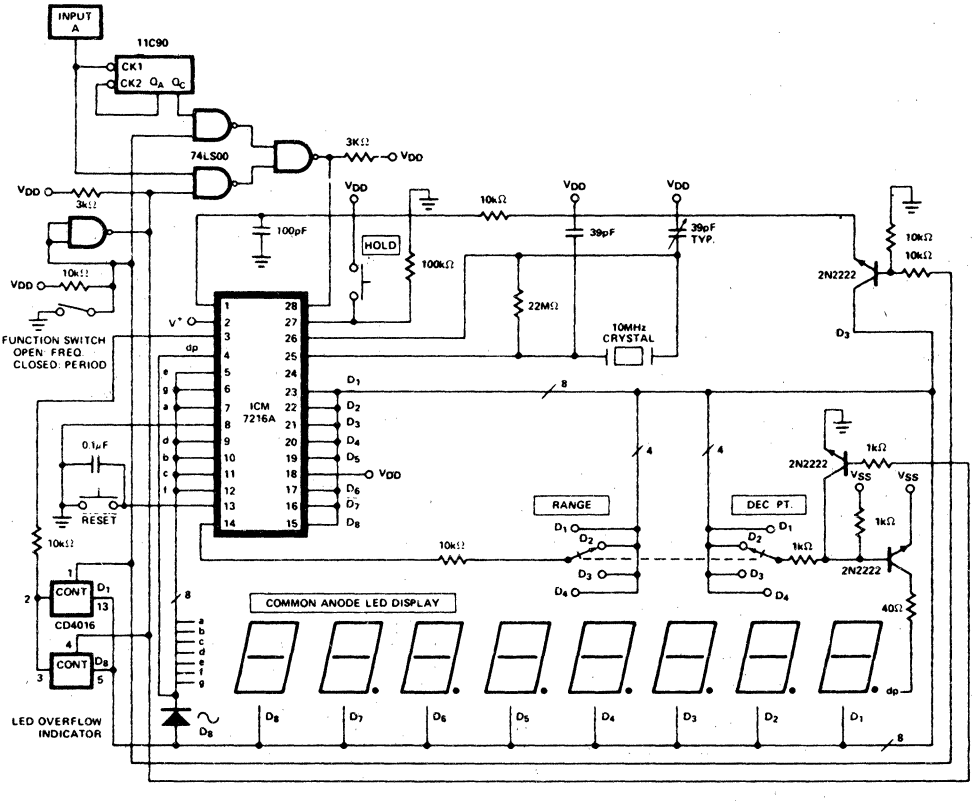
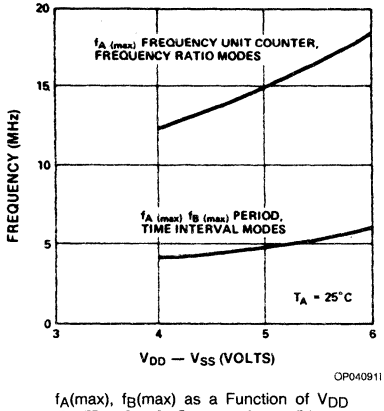


Figure 16: 100MHz Frequency, 2MHz Period Counter



f_A(max), f_B(max) as a Function of V_{DD}

Figure 17: Typical Operating Characteristics

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7217/ICM7227
4-Digit LED Display Programmable Up/Down Counter

INTERSIL

GENERAL DESCRIPTION

The ICM7217 and ICM7227 are four digit, presettable up/down counters, each with an onboard presettable register continuously compared to the counter. The ICM7217 versions are intended for use in hardwired applications where thumbwheel switches are used for loading data, and simple SPDT switches are used for chip control. The ICM7227 versions are for use in processor-based systems, where presetting and control functions are performed under processor control.

These circuits provide multiplexed 7 segment LED display outputs, with common anode or common cathode configurations available. Digit and segment drivers are provided to directly drive displays of up to 0.8" character height (common anode) at a 25% duty cycle. The frequency of the onboard multiplex oscillator may be controlled with a single capacitor, or the oscillator may be allowed to free run. Leading zeros can be blanked. The data appearing at the 7 segment and BCD outputs is latched; the content of the counter is transferred into the latches under external control by means of the Store pin.

The ICM7217/7227 (common anode) and ICM7217A/7227A (common cathode) versions are decade counters, providing a maximum count of 9999, while the ICM7217B, 7227B (common anode) and ICM7217C/7227C (common cathode) are intended for timing purposes, providing a maximum count of 5959.

These circuits provide 3 main outputs; a CARRY/BORROW output, which allows for direct cascading of counters, a $\overline{\text{ZERO}}$ output, which indicates when the count is zero, and an $\overline{\text{EQUAL}}$ output, which indicates when the count is equal to the value contained in the register. Data is multiplexed to and from the device by means of a three-state BCD I/O port. The CARRY/BORROW, $\overline{\text{EQUAL}}$, $\overline{\text{ZERO}}$ outputs, and the BCD port will each drive one standard TTL load.

To permit operation in noisy environments and to prevent multiple triggering with slowly changing inputs, the count input is provided with a Schmitt trigger.

Input frequency is guaranteed to 2MHz, although the device will typically run with f_{in} as high as 5MHz. Counting and comparing ($\overline{\text{EQUAL}}$ output) will typically run 750kHz maximum.

FEATURES

- **Four Decade, Presettable Up-Down Counter With Parallel Zero Detect**
- **Settable Register With Contents Continuously Compared to Counter**
- **Directly Drives Multiplexed 7 Segment Common Anode or Common Cathode LED Displays**
- **On-Board Multiplex Scan Oscillator**
- **Schmitt Trigger On Count Input**
- **TTL Compatible BCD I/O Port, Carry/Borrow, Equal, and Zero Outputs**
- **Display Blank Control for Lower Power Operation; Quiescent Power Dissipation < 5mW**
- **All Terminals Fully Protected Against Static Discharge**
- **Single 5V Supply Operation**

ORDERING INFORMATION

PART NUMBER	PACKAGE	DISPLAY OPTION	COUNT OPTION MAX COUNT
ICM7217IJI	28 Lead CERDIP	Common Anode	Decade/9999
ICM7217AIPI	28 Lead PLASTIC	Common Cathode	Decade/9999
ICM7217BIJI	28 Lead CERDIP	Common Anode	Timer/5959
ICM7217CIPI	28 Lead PLASTIC	Common Cathode	Timer/5959
ICM7227IJI	28 Lead CERDIP	Common Anode	Decade/9999
ICM7227AIPI	28 Lead PLASTIC	Common Cathode	Decade/9999
ICM7227BIJI	28 Lead CERDIP	Common Anode	Timer/5959
ICM7227CIPI	28 Lead PLASTIC	Common Cathode	Timer/5959
ICM7217/D	DICE	Common Anode	Decade/9999
ICM7217A/D	DICE	Common Cathode	Decade/9999
ICM7217B/D	DICE	Common Anode	Timer/5959
ICM7217C/D	DICE	Common Cathode	Timer/5959
ICM7227/D	DICE	Common Anode	Decade/9999
ICM7227A/D	DICE	Common Cathode	Decade/9999
ICM7227B/D	DICE	Common Anode	Timer/5959
ICM7227C/D	DICE	Common Cathode	Timer/5959

202816-002

Note: All typical values have been guaranteed by characterization and are not tested.

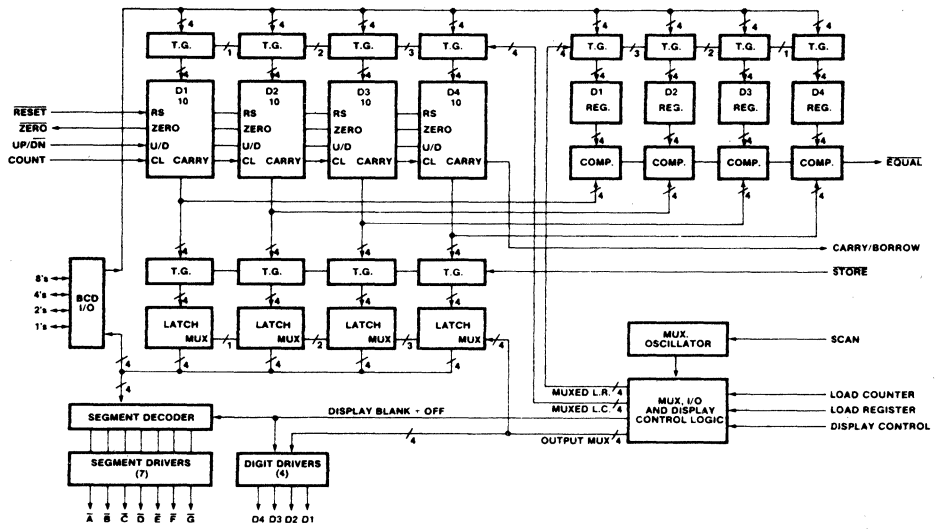


Figure 1: ICM7217 Functional Diagram

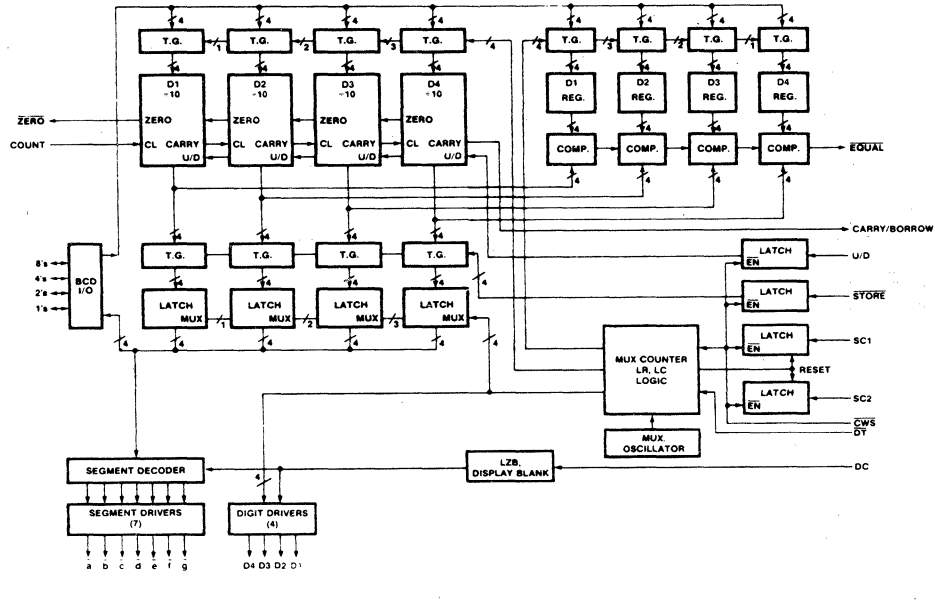


Figure 2: ICM7227 Functional Diagram

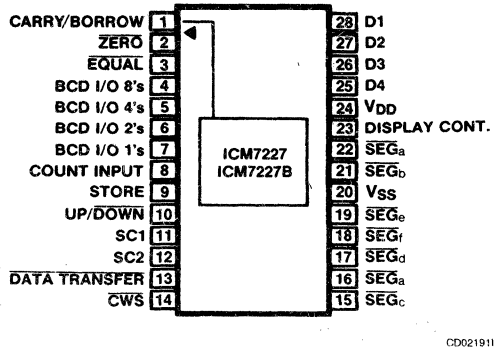
Note: All typical values have been guaranteed by characterization and are not tested.

ICM7217/ICM7227

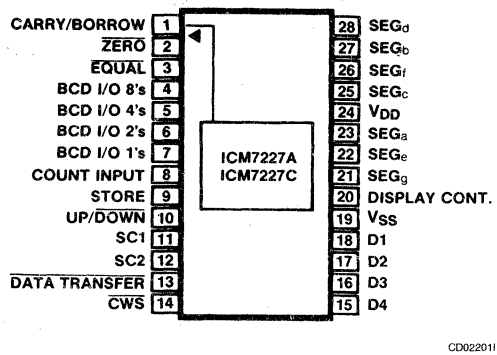
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD} – V_{SS}) 6V
Input Voltage (any terminal) ..... V_{SS} +0.3V, V_{SS} –0.3V Note 2
Power Dissipation (common anode/Cerdip) ... 1W Note 1
Power Dissipation (common cathode/Plastic) ..... 0.5W Note 1
Operating Temperature Range ..... –25°C to +85°C
Storage Temperature Range ..... –55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.



COMMON ANODE



COMMON CATHODE

Figure 3: Pin Configurations (Outline dwgs JI, PI)

ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = 25°C, Display Diode Drop 1.7V, unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD} (7217)	Supply Current (Lowest power mode)	Display Off, LC, DC, UP/DN, ST, RS, BCD I/O Floating or at V_{DD} (Note 3)		350	500	µA
I_{DD} (7227)	Supply current (Lowest power mode)	Display off (Note 3)		300	500	µA
I_{OP}	Supply Current OPERATING	Common Anode, Display On, all "8's"	140	200		mA
		Common Cathode, Display On, all "8's"	50	100		mA
V_{DD}	Supply Voltage		4.5	5	5.5	V
I_{DIG}	Digit Driver output current	Common anode, $V_{OUT} = V_{DD} - 2.0V$	140	200		mA peak
I_{SEG}	SEGment driver output current	Common anode, V_{OUT} = +1.5V	–20	–35		mA peak
I_{DIG}	Digit Driver output current	Common cathode, V_{OUT} = +1.0V	–50	–75		mA peak
I_{SEG}	SEGment driver output current	Common cathode $V_{OUT} = V_{DD} - 2V$	9	12.5		mA peak
I_P	$\overline{ST}$, $\overline{RS}$, UP/$\overline{DN}$ input pullup current	$V_{OUT} = V_{DD} - 2V$ (See Note 3)	5	25		µA
Z_{IN}	3 level input impedance		40		75	kΩ
V_{BIH}	BCD I/O input high voltage	ICM7217 common anode (Note 4) (V_{DD} = 5.0V)	1.5			V
		ICM7217 common cathode (Note 4)	4.40			V
		ICM7227 with 50pF effective load	3			V
V_{BIL}	BCD I/O input low voltage	ICM7217 common anode (Note 4) (V_{DD} = 5.0V)			0.60	V
		ICM7217 common cathode (Note 4)			3.2V	V
		ICM7227 with 50pF effective load			1.5	V

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7217/ICM7227

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{BPU}	BCD I/O input pullup current	ICM7217 common cathode $V_{IN} = V_{DD} - 2V$ (Note 3)	5	25		μA
I_{BPD}	BCD I/O input pulldown current	ICM7217 common anode $V_{IN} = +2V$ (Note 3)	5	25		μA
V_{OH}	BCD I/O, $\overline{ZERO}$, $\overline{EQUAL}$ Outputs output high current	$I_{OH} = 100\mu A$	3.5			V
V_{OL}	BCD I/O, CARRY/BORROW $\overline{ZERO}$, $\overline{EQUAL}$ Outputs output low current	$I_{OL} = -1.6mA$			0.4	V
f_{in}	Count input frequency (Guaranteed)	$V_{DD} = 5V \pm 10\%$, $-20°C < T_A < +70°C$	0	5	2	MHz
V_{TH}	Count input threshold	$V_{DD} = 5V$ (Note 5)		2		V
V_{HYS}	Count input hysteresis	$V_{DD} = 5V$ (Note 5)		0.5		V
V_{CIL}	Count input LO	$V_{DD} = 5V$	0.40			V
V_{CIH}	Count Input HI	$V_{DD} = 5V$			3.5	V
f_{ds}	Display scan oscillator frequency	Free-running (SCAN terminal open circuit)			10	kHz
T_A	Operating Temperature Range	Industrial temperature range	−25		+85	°C

NOTES:
1. These limits refer to the package and will not be obtained during normal operation.
2. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason it is recommended that the power supply to the device be established before any inputs are applied and that in multiple systems the supply to the ICM7217/7227 be turned on first.
3. In the ICM7217 the UP/$\overline{DOWN}$, $\overline{STORE}$, $\overline{RESET}$ and the BCD I/O as inputs have pullup or pulldown devices which consume power when connected to the opposite supply. Under these conditions, with the display off, the device will consume typically 750 μA. The ICM7227 devices do not have these pullups or pulldowns and thus are not subject to this condition.
4. These voltages are adjusted to allow the use of thumbwheel switches for the ICM7217 versions. Note that a positive level is taken as an input logic zero for ICM7217 common-cathode versions.
5. Parameters not tested (Guaranteed by Design).

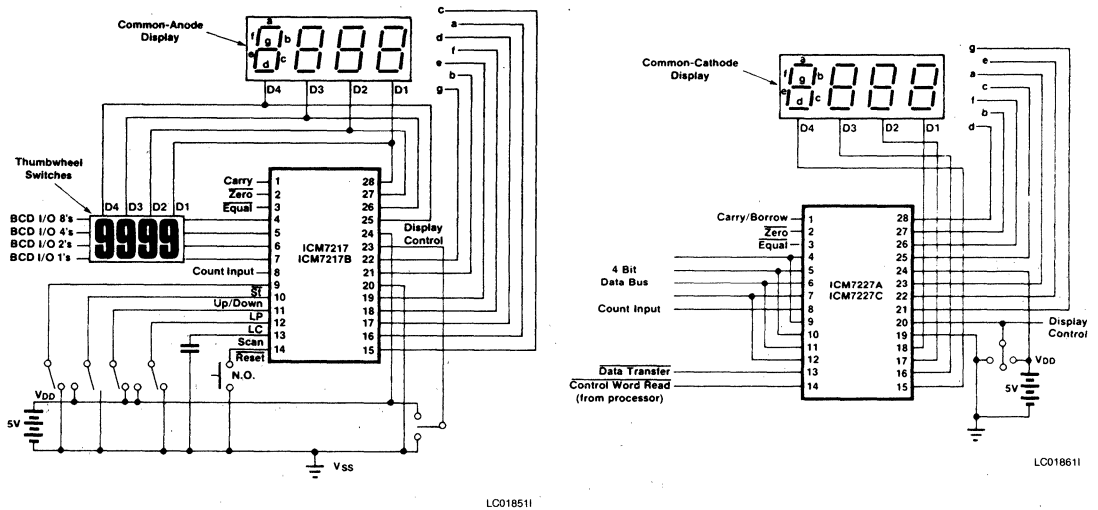
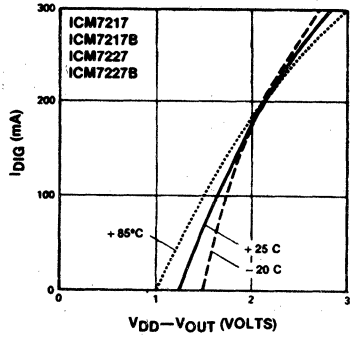


Figure 4: Test Circuits, showing the ICM7217 in the Common-Anode Version and the ICM7227 in the Common-Cathode Version

Note: All typical values have been guaranteed by characterization and are not tested.

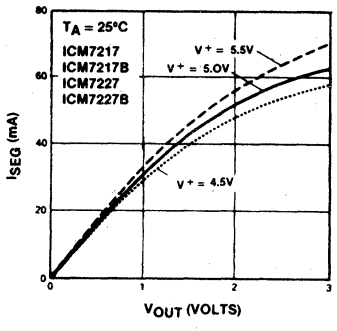
ICM7217/ICM7227

TYPICAL PERFORMANCE CHARACTERISTICS (DIGIT AND SEGMENT DRIVERS)

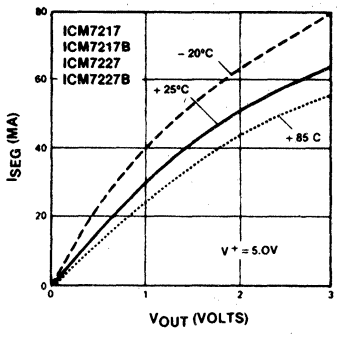


OP04101I

Typical I_{DIG} vs. $V_+ - V_{OUT}$, $4.5V \leq V^+ \leq 6.0V$

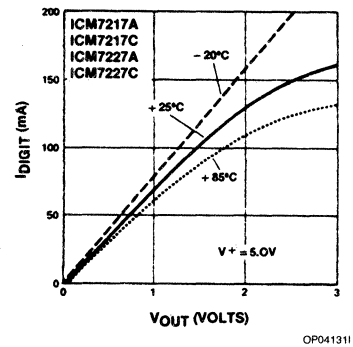


OP04111I

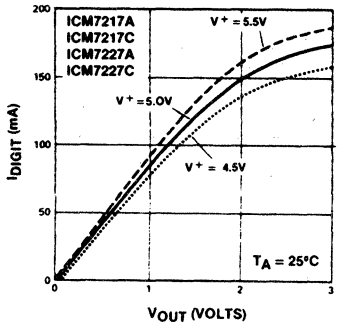


OP04121I

Typical I_{SEG} vs. V_{OUT}

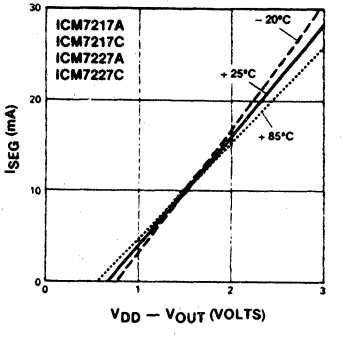


OP04131I



OP04141I

Typical I_{DIGIT} vs. V_{OUT}



OP04151I

Typical I_{SEG} vs. $V_{DD} - V_{OUT}$, $4.5 \leq V_{DD} - V_{SS} \leq 6.0V$

DETAILED DESCRIPTION

OUTPUTS

The CARRY/BORROW output is a positive going pulse occurring typically 500ns after the positive going edge of the COUNT INPUT. It occurs when the counter is clocked from 9999 to 0000 when counting up and from 0000 to 9999 when counting down. This output allows direct cascading of counters.

The $\overline{\text{EQUAL}}$ output assumes a negative level when the contents of the counter and register are equal.

The $\overline{\text{ZERO}}$ output assumes a negative level when the content of the counter is 0000.

The CARRY/BORROW, $\overline{\text{EQUAL}}$ and $\overline{\text{ZERO}}$ outputs will drive a single TTL load over the full range of supply voltage and ambient temperature; for a logic zero, these outputs will sink 1.6mA @ 0.4V (on resistance 250Ω), and for a logic one, the outputs will source > 60μA. A 10kΩ pull-up resistor to V_{DD} on the $\overline{\text{EQUAL}}$ or $\overline{\text{ZERO}}$ outputs is recommended for highest speed operation, and on the CARRY/BORROW output when it is being used for cascading.

The Digit and SEGment drivers provide a decoded 7 segment display system, capable of directly driving common anode LED displays at typical peak currents of 40mA/seg. This corresponds to average currents of 10mA/seg at a 25% multiplex duty cycle. For the common cathode versions, peak segment currents are 12.5mA, corresponding to average segment currents of 3.1mA. Figure 5 shows the multiplex timing, while Figure 6 shows the Output Timing. The DISPLAY pin controls the display output using three level logic. The pin is self-biased to a voltage approximately 1/2 (V_{DD}); this corresponds to normal operation. When this pin is connected to V_{DD}, the segments are inhibited, and when connected to V_{SS}, the leading zero blanking feature is inhibited. For normal operation (display on with leading zero blanking) the pin may be left open. The display may be controlled with a 3 position SPDT switch; see Figure 4.

Note: All typical values have been guaranteed by characterization and are not tested.

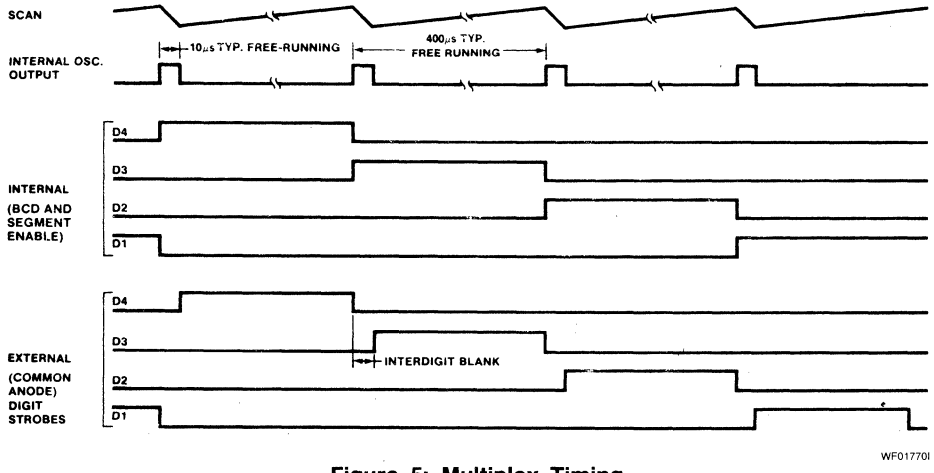
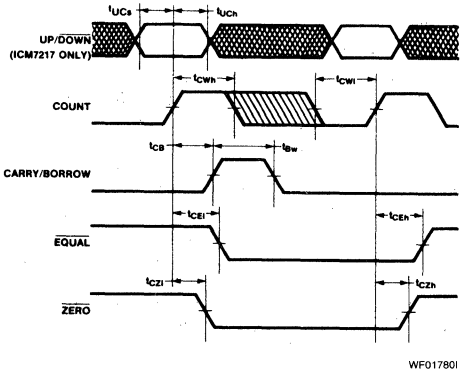


Figure 5: Multiplex Timing



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{UCs}	UP/$\overline{DOWN}$ setup time (min)		300		
t_{UCh}	UP/$\overline{DOWN}$ hold time (min)		0		
t_{CUh}	COUNT pulse high (min)		100	250	ns
t_{CUl}	COUNT pulse low (min)		100	250	
t_{CB}	COUNT to CARRY/ BORROW delay		750		
t_{Bw}	CARRY/BORROW pulse width		100		
t_{CEl}	COUNT to $\overline{EQUAL}$ delay		500		
t_{CZl}	COUNT to $\overline{ZERO}$ delay		300		

Figure 6: ICM7217/27 COUNT and Output Timing

Multiplex SCAN Oscillator

The on-board multiplex scan oscillator has a nominal free-running frequency of 2.5kHz. This may be reduced by the addition of a single capacitor between the SCAN pin and the positive supply. Capacitor values and corresponding nominal oscillator frequencies, digit repetition rates, and loading times (for ICM7217 versions) are shown in Table 1 below.

The internal oscillator output has a duty cycle of approximately 25:1, providing a short pulse occurring at the oscillator frequency. This pulse clocks the four-state counter which provides the four multiplex phases. The short pulse width is used to delay the digit driver outputs, thereby providing inter-digit blanking which prevents ghosting. The digits are scanned from MSD (D4) to LSD (D1). See Figure 4 for the display digit multiplex timing.

Table 1: ICM7217 Multiplexed Rate Control

SCAN CAPACITOR	NOMINAL OSCILLATOR FREQUENCY	DIGIT REPETITION RATE	SCAN CYCLE TIME (4 digits)
None	2.5kHz	625Hz	1.6ms
20pF	1.25kHz	300Hz	3.2ms
90pF	600Hz	150Hz	8ms

Note: All typical values have been guaranteed by characterization and are not tested.

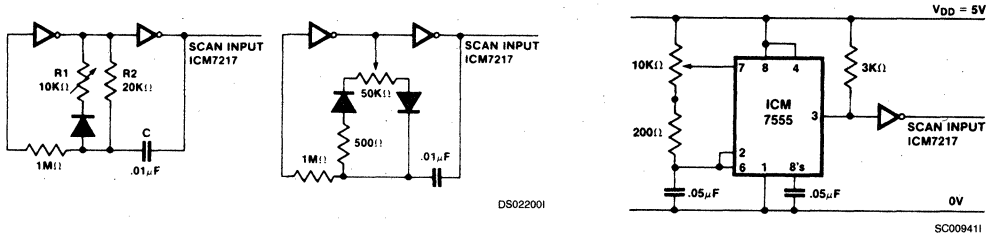


Figure 7: Brightness Control Circuits

During **load counter** and **load register** operations, the multiplex oscillator is disconnected from the SCAN input and is allowed to free-run. In all other conditions, the oscillator may be directly overdriven to about 20kHz, however the internal oscillator signal will be of the same duty cycle and phase as the overdriving signal, and the digits are blanked during the time the external signal is at a positive level. To insure proper leading zero blanking, the interdigit blanking time should not be less than about 2μs. Overdriving the oscillator at less than 200Hz may cause display flickering.

The display brightness may be altered by varying the duty cycle. Figure 7 shows several variable-duty-cycle oscillators suitable for brightness control at the ICM7217 SCAN input. The inverters should be CMOS CD4000 series and the diodes may be any inexpensive device such as IN914.

Counting Control

As shown in Figure 6, the counter is incremented by the rising edge of the COUNT INPUT signal when UP/$\overline{\text{DOWN}}$ is high. It is decremented when UP/$\overline{\text{DOWN}}$ is low. A Schmitt trigger on the COUNT INPUT provides hysteresis to prevent double triggering on slow rising edges and permits operation in noisy environments. The COUNT INPUT is inhibited during reset and **load counter** operations.

The $\overline{\text{STORE}}$ pin controls the internal latches and consequently the signals appearing at the 7-segment and BCD outputs. Bringing the $\overline{\text{STORE}}$ pin low transfers the contents of the counter into the latches.

The counter is asynchronously reset to 0000 by bringing the $\overline{\text{RESET}}$ pin low. The circuit performs the reset operation by forcing the BCD input lines to zero, and "presetting" all four decades of counter in parallel. This affects register loading; if LOAD REGISTER is activated when the $\overline{\text{RESET}}$ input is low, the register will also be set to zero. The $\overline{\text{STORE}}$, $\overline{\text{RESET}}$ and UP/$\overline{\text{DOWN}}$ pins are provided with pullup resistors of approximately 75kΩ.

BCD I/O Pins

The BCD I/O port provides a means of transferring data to and from the device. The ICM7217 versions can multiplex data into the counter or register via thumbwheel switches, depending on inputs to the LOAD COUNTER or LOAD REGISTER pins; (see below). When functioning as outputs, the BCD I/O pins will drive one standard TTL load. Common anode versions have internal pull down resistors and common cathode versions have internal pull up resistors on the four BCD I/O lines as inputs.

LOADing the COUNTER and REGISTER

The BCD I/O pins, the LOAD COUNTER (LC), and LOAD REGISTER (LR) pins combine to provide presetting and compare functions. LC and LR are three-level inputs, being self-biased at approximately $1/2V_{DD}$ for normal operation. With both LC and LR open, the BCD I/O pins provide a multiplexed BCD output of the latch contents, scanned from MSD to LSD by the display multiplex.

When either the LOAD COUNTER (Pin 12) or LOAD REGISTER (Pin 11) is taken high, the drivers are turned off and the BCD pins become high-impedance inputs. When LC is connected to V_{DD}, the count input is inhibited and the levels at the BCD pins are multiplexed into the counter. When LR is connected to V_{DD}, the levels at the BCD pins are multiplexed into the register without disturbing the counter. When both are connected to V_{DD}, the count is inhibited and both register and counter will be loaded.

The LOAD COUNTER and LOAD REGISTER inputs are edge-triggered, and pulsing them high for 500ns at room temperature will initiate a full sequence of data entry cycle operations (see Figure 7). When the circuit recognizes that either or both of the LC or LR pins input is high, the multiplex oscillator and counter are reset (to D4). The internal oscillator is then disconnected from the SCAN pin and the preset circuitry is enabled. The oscillator starts and runs with a frequency determined by its internal capacitor, (which may vary from chip to chip). When the chip finishes a full 4 digit multiplex cycle (loading each digit from D4 to D3 to D2 to D1 in turn), it again samples the LOAD REGISTER and LOAD COUNTER inputs. If either or both is still high, it repeats the load cycle, if both are floating or low, the oscillator is reconnected to the SCAN pin and the chip returns to normal operation. Total load time is digit "on" time multiplied by 4. If the Digit outputs are used to strobe the BCD data into the BCD I/O inputs, the input will be automatically synchronized to the appropriate digit (Figure 8). Input data must be valid at the trailing edge of the digit output.

When LR is connected to GROUND, the oscillator is inhibited, the BCD I/O pins go to the high impedance state, and the segment and digit drivers are turned off. This allows the display to be used for other purposes and minimizes power consumption. In this display off condition, the circuit will continue to count, and the CARRY/BORROW, $\overline{\text{EQUAL}}$, $\overline{\text{ZERO}}$, UP/$\overline{\text{DOWN}}$, $\overline{\text{RESET}}$ and $\overline{\text{STORE}}$ functions operate as normal. When LC is connected to ground, the BCD I/O pins are forced to the high impedance state without disturbing the counter or register. See "Control Input

Note: All typical values have been guaranteed by characterization and are not tested.

Definitions" (Table 2) for a list of the pins that function as three-state self-biased inputs and their respective operations.

Note that the ICM7217 and 7217B have been designed to drive common anode displays. The BCD inputs are high true, as are the BCD outputs.

The ICM7217A and the 7217C are used to drive common cathode displays, and the BCD inputs are low true. BCD outputs are high true.

Notes on Thumbwheel Switches & Multiplexing

The thumbwheel switches used with these circuits (both common anode and common cathode) are TRUE BCD coded; i.e. all switches open corresponds to 0000. Since the thumbwheel switches are connected in parallel, diodes must be provided to prevent crosstalk between digits. See Figure 8. In order to maintain reasonable noise margins, these diodes should be specified with low forward voltage drops (IN914). Similarly, if the BCD outputs are to be used, resistors should be inserted in the Digit lines to avoid loading problems.

Output and Input Restrictions

The CARRY/BORROW output is not valid during load counter and reset operations.

The $\overline{\text{EQUAL}}$ output is not valid during load counter or load register operations.

The $\overline{\text{ZERO}}$ output is not valid during a load counter operation.

The $\overline{\text{RESET}}$ input may be susceptible to noise if its input rise time (coming out of reset) is greater than about 500μs. This will present no problems when this input is driven by active devices (i.e., TTL or CMOS logic) but in hardwired systems adding virtually any capacitance to the $\overline{\text{RESET}}$ input can cause trouble. A simple circuit which provides a reliable power-up reset and a fast rise time on the $\overline{\text{RESET}}$ input is shown below.

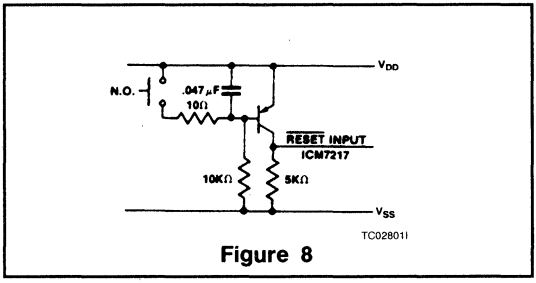


Figure 8

When using the circuit as a programmable divider (÷ by n with equal outputs) a short time delay (about 1μs) is needed from the $\overline{\text{EQUAL}}$ output to the $\overline{\text{RESET}}$ input to establish a pulse of adequate duration. (See Figure 9)

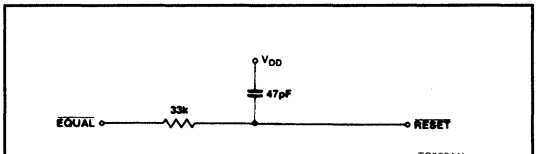


Figure 9

When the circuit is configured to reload the counter or register with a new value from the BCD lines (upon reaching $\overline{\text{EQUAL}}$), loading time will be digit "on" time multiplied by four. If this load time is longer than one period of the input count, a count can be lost. Since the circuit will retain data in the register, the register need only be updated when a new value is to be entered. $\overline{\text{RESET}}$ will not clear the register.

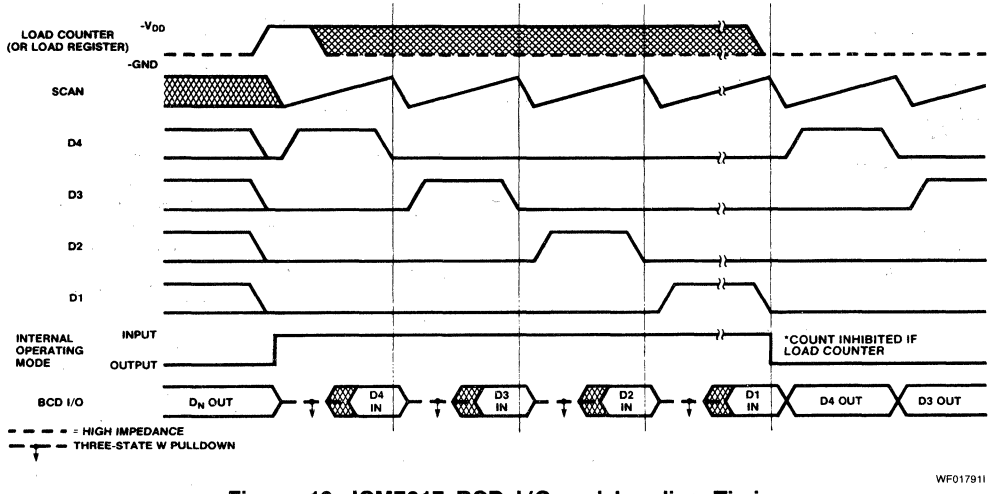
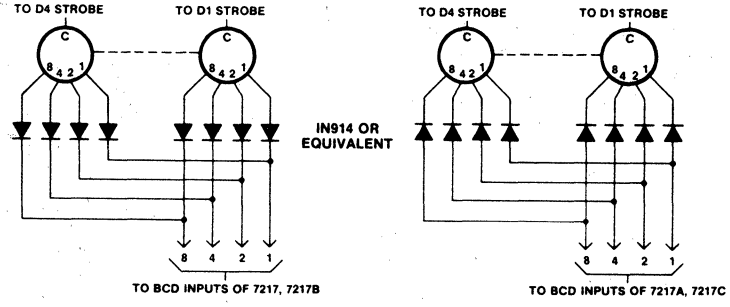


Figure 10: ICM7217 BCD I/O and Loading Timing

Note: All typical values have been guaranteed by characterization and are not tested.



Note: If the BCD pins are to be used for outputs a 10kΩ resistor should be placed in series with each digit line to avoid loading problems through the switches.

Figure 11: Thumbwheel Switch/Diode Connections

Table 2: Control Input Definitions ICM7217

INPUT	TERMINAL	VOLTAGE	FUNCTION
$\overline{\text{STORE}}$	9	V_{DD} (or floating) V_{SS}	Output latches not updated Output latches updated
UP/$\overline{\text{DOWN}}$	10	V_{DD} (or floating) V_{SS}	Counter counts up Counter counts down
$\overline{\text{RESET}}$	14	V_{DD} (or floating) V_{SS}	Normal Operation Counter Reset
LOAD COUNTER/ I/O $\overline{\text{OFF}}$	12	Unconnected V_{DD} V_{SS}	Normal operation Counter loaded with BCD data BCD port forced to Hi Z condition
LOAD REGISTER/ $\overline{\text{OFF}}$	11	Unconnected V_{DD} V_{SS}	Normal operation Register loaded with BCD data Display drivers disabled; BCD port forced to Hi Z condition, mpx counter reset to D4; mpx oscillator inhibited
DISPLAY CONTrol (DC)	23 Common Anode 20 Common Cathode	Unconnected V_{DD} V_{SS}	Normal Operation Segment drivers disabled Leading zero blanking inhibited

Table 3: Control Input Definitions ICM7227

INPUT		TERMINAL	VOLTAGE	FUNCTION
	$\overline{\text{DATA TRANSFER}}$	13	V_{DD} V_{SS}	Normal Operation Causes transfer of data as directed by select code
Control Word Port	STORE	9	V_{DD} (During $\overline{\text{CWS}}$ Pulse) V_{SS}	Output latches updated Output latches not updated
''	UP/$\overline{\text{DOWN}}$	10	V_{DD} (During $\overline{\text{CWS}}$ Pulse) V_{SS}	Counter counts up Counter counts down
'' 2''	Select Code Bit 1 (SC1) Select Code Bit 2 (SC2)	11 12	V_{DD} = "1" V_{SS} = "0"	SC1, SC2 control:— 00 Change store and up/down latches. No data transfer. 01 Output latch data active 10 Counter to be preset 11 Register to be preset
	$\overline{\text{Control Word Strobe}}$ ($\overline{\text{CWS}}$)	14	V_{DD} V_{SS}	Normal operation Causes control word to be written into control latches
	DISPLAY CONTrol (DC)	23 Common Anode 20 Common Cathode	Unconnected V_{DD} V_{SS}	Normal operation Display drivers disabled Leading zero blanking inhibited

Note: All typical values have been guaranteed by characterization and are not tested.

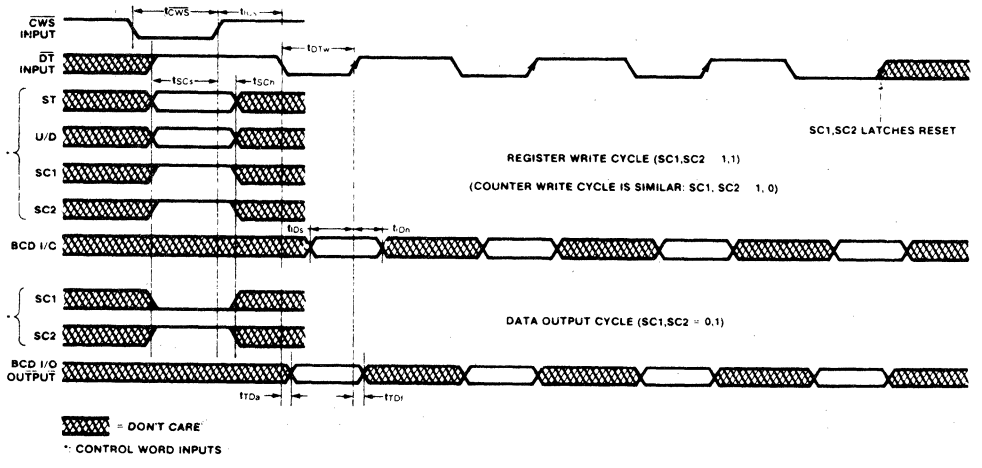


Figure 12: ICM7227 I/O Timing (see Table 4)

CONTROL OF ICM7227 VERSIONS

The ICM7227 series has been designed to permit microprocessor control of the inputs. BCD inputs and outputs are active high.

In these versions, the STORE, UP/$\overline{\text{DOWN}}$, SC1 and SC2 (Select Code bits 1 and 2) pins form a four-bit control word input. A negative-going pulse on the $\overline{\text{CWS}}$ (Control Word Strobe) pin writes the data on these pins into four internal control latches, and resets the multiplex counter in preparation for sequencing a data transfer operation. The select code 00 is reserved for changing the state of the Store and/or Up/$\overline{\text{Down}}$ latches without initiating a data transfer. Writing a one into the Store latch sets the latch and causes the data in the counter to be transferred into the output latches, while writing a zero resets the latches causing them to retain data and not be updated. Similarly, writing a one into the Up/$\overline{\text{Down}}$ latch causes the counter to count up and writing a zero causes the counter to count down. The state of the Store and Up/$\overline{\text{Down}}$ latches may also be changed with a non-zero select code.

Writing a nonzero select code initiates a **data transfer** operation. Writing select code of 01 (SC1, SC2) indicates that the data in the output latches will be active and enables the BCD I/O port to output the data. Writing a select code of 11 indicates that the register will be preset, and a 10 indicates that the counter will be preset.

When a nonzero select code is read, the clock of the four-state multiplex counter is switched to the $\overline{\text{DATA TRANSFER}}$ pin. Negative-going pulses at this pin then sequence a digit-by-digit data transfer, either outputting data or presetting the counter or register as determined by the select code. The output drivers of the BCD I/O port will be enabled only while $\overline{\text{DT}}$ is low during a data transfer initiated with a 01 select code.

The sequence of digits will be D4-D3-D2-D1, i.e. when outputting, the data from D4 will be valid during the first $\overline{\text{DT}}$ pulse, then D3 will be valid during the second pulse, etc. When presetting, the data for D4 must be valid at the positive-going transition (trailing edge) of the first $\overline{\text{DT}}$ pulse, the data for D3 must be valid during the second $\overline{\text{DT}}$ pulse, etc.

At the end of a **data transfer** operation, on the positive going transition of the fourth $\overline{\text{DT}}$ pulse, the SC1 and SC2 control latches will automatically reset, terminating the data transfer and reconnecting the multiplex counter clock to the oscillator. In the ICM7227 versions, the multiplex oscillator is always free-running, except during a **data transfer** operation when it is disabled.

Figure 12 shows the timing of data transfers initiated with a 11 select code (writing into the register) and a 01 select code (reading out of the output latches). Typical times during which data must be valid at the control word and BCD I/O ports are indicated in Table 4.

Table 4: ICM7227 I/O Timing Requirements

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
$t_{\overline{CWS}}$	Control Word Strobe Width (min)		275		ns
t_{ICs}	Internal Control Set-up (min)		2.5	3	μs
$t_{\overline{DT}w}$	DATA TRANSFER pulse width (min)		300		ns
t_{SCs}	Control to Strobe setup (min)		300		ns
t_{SCh}	Control to Strobe hold (min)		300		ns
t_{IDs}	Input Data setup (min)		300		ns
t_{IDh}	Input Data Hold (min)		300		ns
t_{TDacc}	Output Data access		300		ns
t_{TDf}	Output Transfer to Data float		300		ns

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7217/ICM7227

APPLICATIONS

FIXED DECIMAL POINT

In the common anode versions, a fixed decimal point may be activated by connecting the D.P. segment lead from the appropriate digit (with separate digit displays) through a 39Ω series resistor to Ground. With common cathode devices, the D.P. segment lead should be connected through a 75Ω series resistor to V_{DD}.

To force the device to display leading zeroes after a fixed decimal point, use a bipolar transistor and base resistor in a configuration like that shown below with the resistor connected to the digit output driving the D.P. for left hand D.P. displays, and to the next least significant digit output for right hand D.P. display. See Performance Characteristics for a similarly operating multi-digit connection.

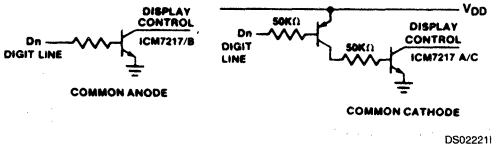


Figure 13: Forcing Leading Zero Display

DRIVING LARGER DISPLAYS

For displays requiring more current than the ICL7217/7227 can provide, the circuits of Figure 14 can be used.

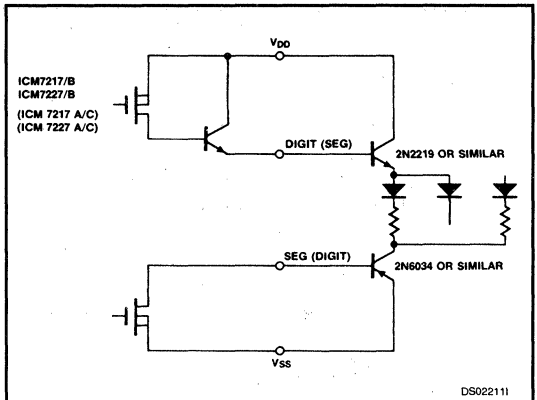


Figure 14: Driving High Current Displays

LCD DISPLAY INTERFACE

The low-power operation of the ICM7217 makes an LCD interface desirable. The Intersil ICM7211 4 digit BCD to LCD display driver easily interfaces to the ICM7217 as shown in Figure 15. Total system power consumption is less than 5mW. System timing margins can be improved by using capacitance to ground to slow down the BCD lines. A similar circuit can be used to drive Vacuum Fluorescent displays, with the ICM7235.

The 10–20kΩ resistors on the switch BCD lines serve to isolate the switches during BCD output.

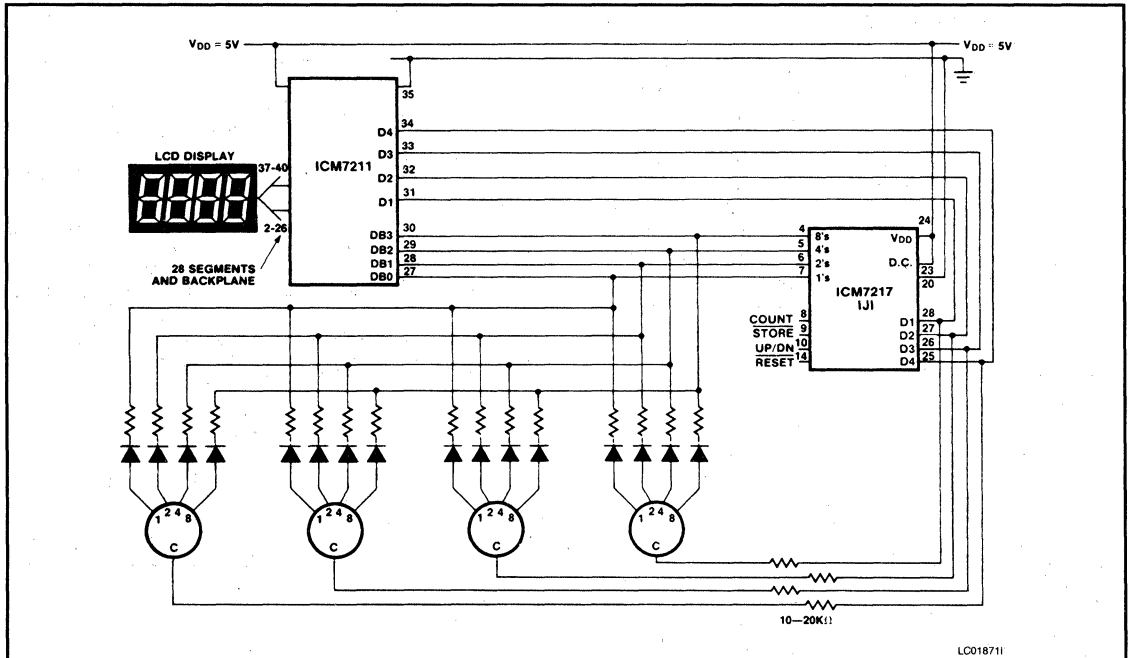


Figure 15: LCD Display Interface (with Thumbwheel Switches)

Note: All typical values have been guaranteed by characterization and are not tested.

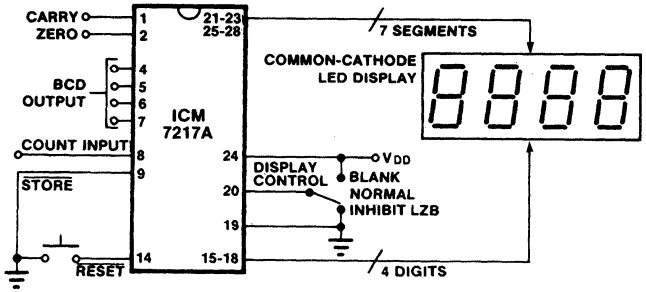


Figure 16: Unit Counter

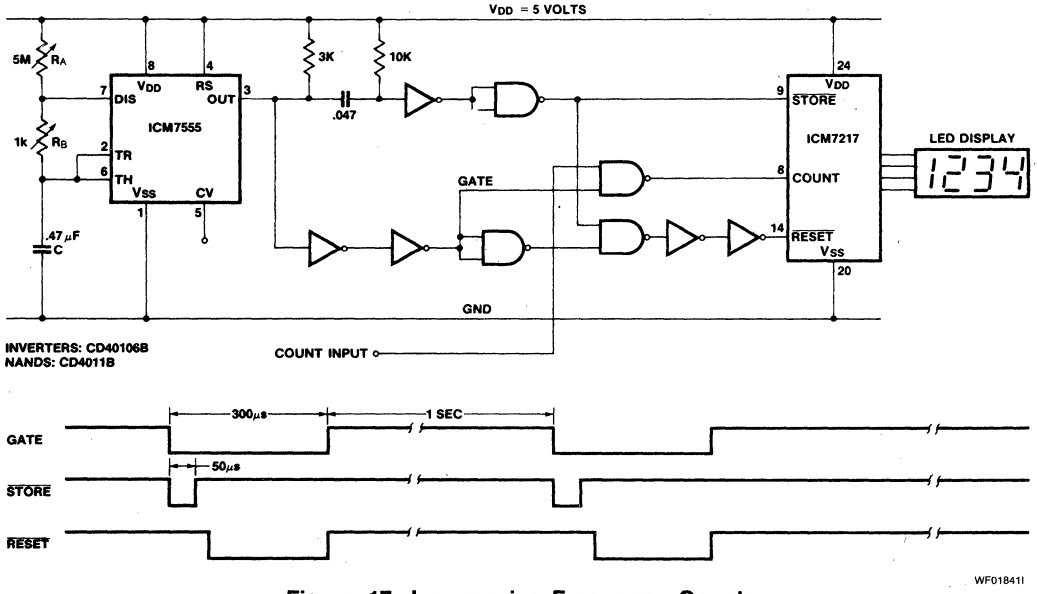


Figure 17: Inexpensive Frequency Counter

UNIT COUNTER WITH BCD OUTPUT

The simplest application of the ICM7217 is a 4 digit unit counter (Figure 16). All that is required is an ICM7217, a power supply and a 4 digit display. Add a momentary switch for reset, an SPDT center-off switch to blank the display or view leading zeroes, and one more SPDT switch for up/down control. Using an ICM7217A with a common-cathode calculator-type display results in the least expensive digital counter/display system available.

INEXPENSIVE FREQUENCY COUNTER/ TACHOMETER

This circuit uses the low power ICM7555 (CMOS 555) to generate the gating, $\overline{\text{STORE}}$ and $\overline{\text{RESET}}$ signals as shown in Figure 17. To provide the gating signal, the timer is configured as an astable multivibrator, using R_A, R_B and C to provide an output that is positive for approximately one second and negative for approximately 300–500μs. The positive waveform time is given by $t_{wp} = 0.693\ (R_A + R_B)C$ while the negative waveform is given by $t_{wn} = 0.693\ R_BC$. The system is calibrated by using a 5MΩ potentiometer for R_A as a "coarse" control and a 1kΩ potentiometer for R_B as a "fine" control. CD40106B's are used as a monostable multivibrator and reset time delay.

Note: All typical values have been guaranteed by characterization and are not tested.

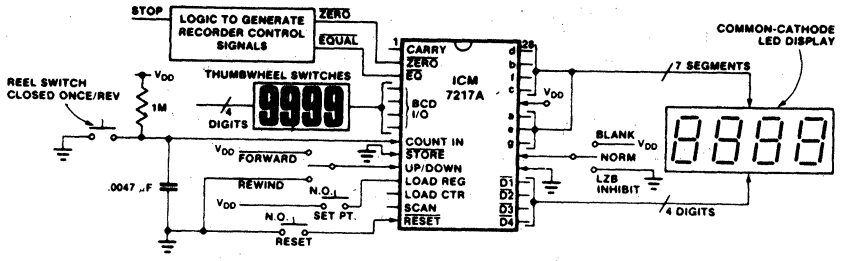


Figure 18: Tape Recorder Position Indicator

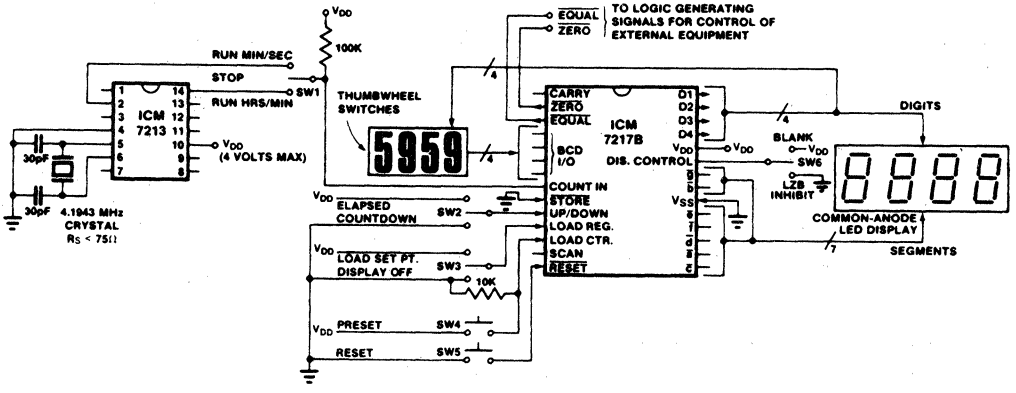


Figure 19: Precision Timer

TAPE RECORDER POSITION INDICATOR/ CONTROLLER

The circuit in Figure 18 shows an application which uses the up/down counting feature of the ICM7217 to keep track of tape position. This circuit is representative of the many applications of up/down counting in monitoring dimensional position. For example, an ICM7227 as a peripheral to a processor can monitor the position of a lathe bed or digitizing head, transfer the data to the processor, drive interrupts to the processor using the $\overline{\text{EQUAL}}$ or $\overline{\text{ZERO}}$ outputs, and serve as a numerical display for the processor.

In the tape recorder application, the LOAD REGISTER, $\overline{\text{EQUAL}}$ and $\overline{\text{ZERO}}$ outputs are used to control the recorder. To make the recorder stop at a particular point on the tape, the register can be set with the stop point and the $\overline{\text{EQUAL}}$ output used to stop the recorder either on fast forward, play or rewind.

To make the recorder stop before the tape comes free of the reel on rewind, a leader should be used. Resetting the counter at the starting point of the tape, a few feet from the end of the leader, allows the $\overline{\text{ZERO}}$ output to be used to stop the recorder on rewind, leaving the leader on the reel.

The 1MΩ resistor and .0047µF capacitor on the COUNT INPUT provide a time constant of about 5ms to debounce the reel switch. The Schmitt trigger on the COUNT INPUT of the ICM7217 squares up the signal before applying it to the counter. This technique may be used to debounce switch-closure inputs in other applications.

PRECISION ELAPSED TIME/COUNTDOWN TIMER

The circuit in Figure 19 uses an ICM7213 precision one minute/one second timebase generator using a 4.1943MHz crystal for generating pulses counted by an ICM7217B. The thumbwheel switches allow a starting time to be entered into the counter for a preset-countdown type timer, and allow the register to be set for compare functions. For instance, to make a 24-hour clock with BCD output the register can be preset with 2400 and the $\overline{\text{EQUAL}}$ output used to reset the counter. Note the 10k resistor connected between the LOAD COUNTER terminal and Ground. This resistor pulls the LOAD COUNTER input low when not loading, thereby inhibiting the BCD output drivers. This resistor should be eliminated and SW4 replaced with an SPDT center-off switch if the BCD outputs are to be used.

Note: All typical values have been guaranteed by characterization and are not tested.

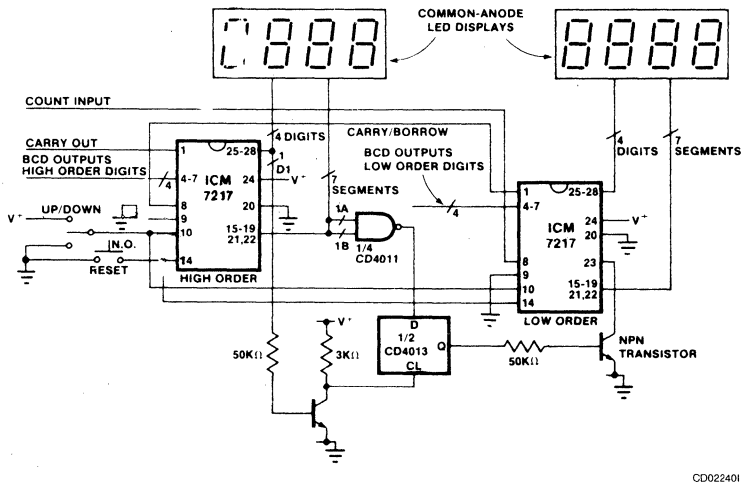


Figure 20: 8 Digit Up/Down Counter

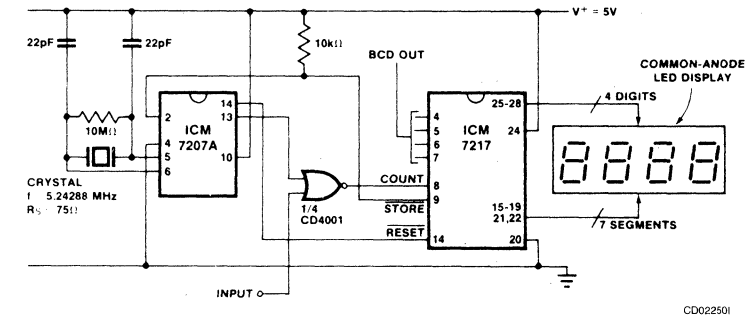


Figure 21: Precision Frequency Counter (MHz Maximum)

This technique may be used on any 3-level input. The 100kΩ pullup resistor on the count input is used to ensure proper logic voltage swing from the ICM7213. For a less expensive (and less accurate) timebase, an ICM7555 timer may be used in a configuration like that shown in Figure 17 to generate a 1Hz reference.

8-DIGIT UP/DOWN COUNTER

This circuit (Figure 20) shows how to cascade counters and retain correct leading zero blanking. The NAND gate detects whether a digit is active since one of the two segments $\overline{a}$ or $\overline{b}$ is active on any unblanked number. The flip flop is clocked by the least significant digit of the high order counter, and if this digit is not blanked, the Q output of the flip flop goes high and turns on the NPN transistor, thereby inhibiting leading zero blanking on the low order counter.

It is possible to use separate thumbwheel switches for presetting, but since the devices load data with the oscillator free-running, the multiplexing of the two devices is difficult to synchronize. This presents no problems with the ICM7227 devices, since the two devices are operated as peripherals to a processor.

PRECISION FREQUENCY COUNTER/ TACHOMETER

The circuit shown in Figure 21 is a simple implementation of a four digit frequency counter, using an ICM7207A to provide the one second gating window and the $\overline{\text{STORE}}$ and $\overline{\text{RESET}}$ signals. In this configuration, the display reads hertz directly. With Pin 11 of the ICM7027A connected to V_{DD}, the gating time will be 0.1 second; this will display tens of hertz as the least significant digit. For shorter gating times, an ICM7207 may be used (with a 6.5536MHz crystal), giving a 0.01 second gating with Pin 11 connected to V_{DD}, and a 0.1 second gating with Pin 11 open.

To implement a four digit tachometer, the ICM7207A with one second gating should be used. To get the display to read directly in RPM, the rotational frequency of the object to be measured must be multiplied by 60. This can be done electronically using a phase-locked loop, or mechanically by

Note: All typical values have been guaranteed by characterization and are not tested.

using a disc rotating with the object with the appropriate number of holes drilled around its edge to interrupt the light from an LED to a photo-dector. For faster updating, use 0.1 second gating, and multiply the rotational frequency by 600.

For more "intelligent" instrumentation, the ICM7227 interfaced to a microprocessor may be more convenient (see Figure 21). For example, an ICM7207A can be used with two ICM7227's to provide an 8 digit, 2MHz frequency counter. Since the ICM7207A gating output has a 50% duty cycle, there is 1 second for the processor to respond to an interrupt, generated by the negative going edge of this signal while it inhibits the count. The processor can respond to the interrupt using ROM based subroutines, to store the data, reset the counter, and read the data into main memory. To add simultaneous period display, the processor inverts the data and an ICM7218 Universal Display Driver stores and displays it.

AUTO-TARE SYSTEM

This circuit uses the count-up and count-down functions of the ICM7217, controlled via the $\overline{\text{EQUAL}}$ and $\overline{\text{ZERO}}$ outputs, to count in SYNC with an ICL7109 A/D Converter as shown in Figure 22. By $\overline{\text{RESET}}$ing the ICM7217 on a "tare" value conversion, and $\overline{\text{STORE}}$-ing the result of a true value conversion, an automatic tare subtraction occurs in the result.

The ICM7217 stays in step with the ICL7019 by counting up and down between 0 and 4095, for 8192 total counts, the same number as the ICL7109 cycle. See A047 for more details.

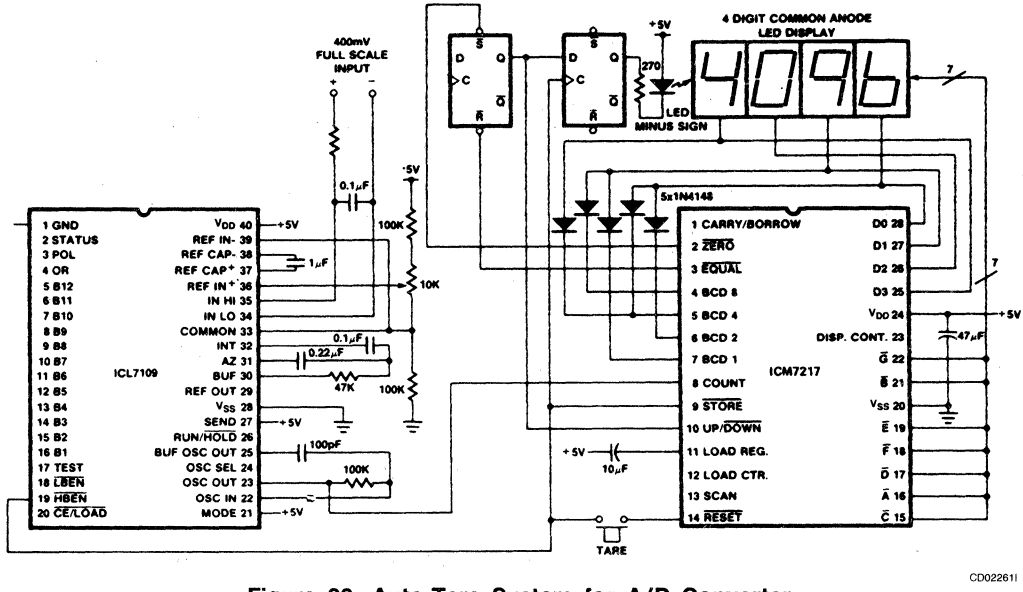


Figure 22: Auto-Tare System for A/D Converter

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7224/ICM7225

4½-Digit LCD/LED Display Counter

GENERAL DESCRIPTION

The ICM7224 and ICM7225 devices constitute a family of high-performance CMOS 4 1/2-digit counters, including decoders, output latches, display drivers, count inhibit, leading zero blanking, and reset circuitry.

The counter section provides direct static counting, guaranteed from DC to 15 MHz, using a 5V ±10% supply over the operating temperature range. At normal ambient temperatures, the devices will typically count up to 25 MHz. The COUNT input is provided with a Schmitt trigger to allow operation in noisy environments and correct counting with slowly changing inputs. The COUNT INHIBIT, STORE and RESET inputs allow a direct interface with the ICM7207/A to implement a low cost, low power frequency counter with a minimum component count.

These devices also incorporate several features intended to simplify cascading four-digit blocks. The CARRY output allows the counter to be cascaded, while the Leading Zero Blanking INput and OUTput allows correct Leading Zero Blanking between four-decade blocks. The BackPlane driver of the LCD devices may be disabled, allowing the segments to be slaved to another backplane signal, necessary when using an eight or twelve digit, single backplane display. In LED systems, the BRighTness input to several ICM7225 devices may be ganged to one potentiometer.

The ICM7224/ICM7225 family are packaged in a standard 40-pin dual-in-line plastic or CERDIP package, or in dice.

FEATURES

- **High Frequency Counting — Guaranteed 15MHz, Typically 25MHz at 5V**
- **Low Power Operation — Typically Less Than 100μW Quiescent**
- **$\overline{\text{STORE}}$ and $\overline{\text{RESET}}$ Inputs Permit Operation as Frequency or Period Counter**
- **True $\overline{\text{COUNT INHIBIT}}$ Disables First Counter Stage**
- **$\overline{\text{CARRY}}$ Output for Cascading Four-Digit Blocks**
- **Schmitt-Trigger On The COUNT Input Allows Operation in Noisy Environments or With Slowly Changing Inputs**
- **Leading Zero Blanking INput and OUTput for Correct Leading Zero Blanking With Cascaded Devices**
- **LCD Devices Provide Complete Onboard Oscillator and Divider Chain to Generate Backplane Frequency, or Backplane Driver May Be Disabled Allowing Segments to be Slaved to A Master Backplane Signal**
- **LED Devices Provide BRighTness Input Which Can Function Digitally As A Display Enable or As A Continuous Display Brightness Control With A Single Potentiometer and Directly Drive Common Anode LED Displays**

ORDERING INFORMATION

PART NUMBER	DISPLAY TYPE	COUNT OPTION
ICM7224IPL	LCD	19999
ICM7224AIPL	LCD	15959
ICM7224/D	LCD	19999
ICM7224A/D	LCD	15959
ICM7224AIJL	LCD	15959
ICM7224IJL	LCD	19999
ICM7225IPL	LED	19999
ICM7225AIPL	LED	15959
ICM7225/D	LED	19999
ICM7225A/D	LED	15959
ICM7225AIJL	LED	15959
ICM7225IJL	LED	19999

Evaluation Kits, order ICM7224 EV/Kit or ICM7225 EV/Kit

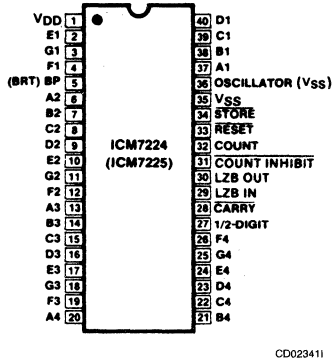
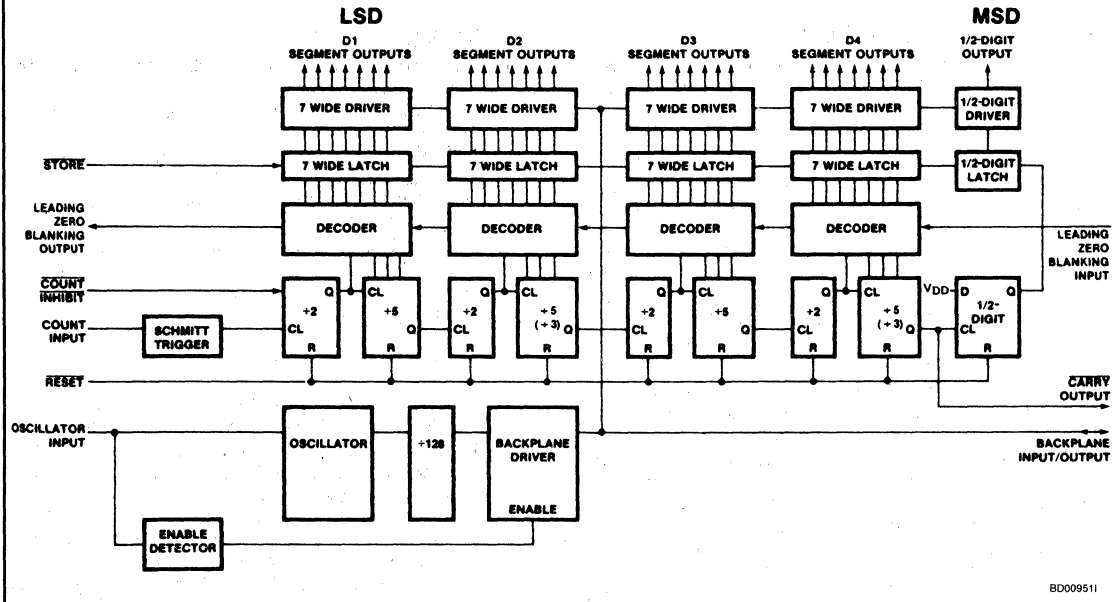


Figure 1: Pin Configuration (Outline dwg PL)

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7224(A)



ICM7225(A)

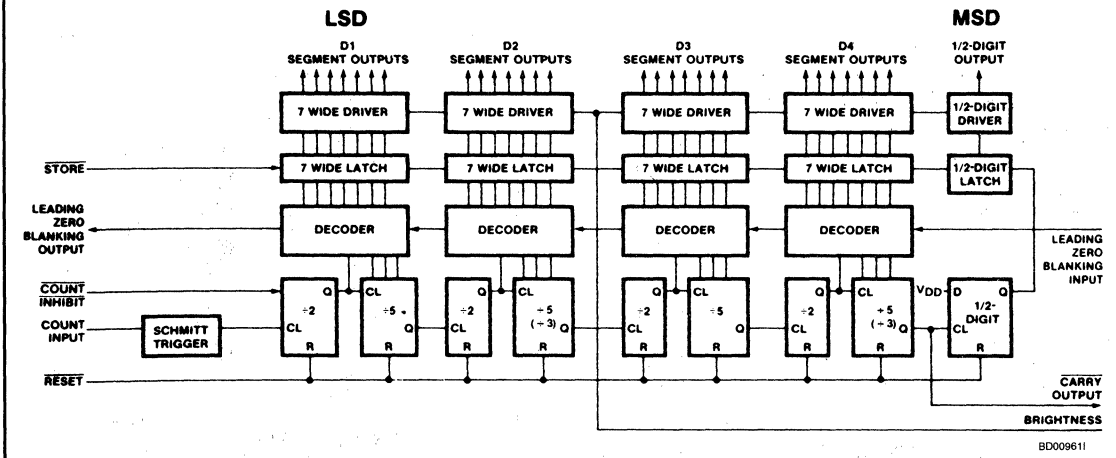


Figure 2: Functional Diagrams

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7224/ICM7225

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage $V_{DD} - V_{SS}$ 6.5V
Input Voltage (Any Terminal) (Note 2) ..... $V_{DD} + 0.3V$ to $V_{SS} - 0.3V$
Power Dissipation (Note 1) ..... 0.5W @ 70°C
Operating Temperature Range ..... −20°C to +85°C
Storage Temperature Range ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE 1: This limit refers to that of the package and will not be obtained during normal operation.

NOTE 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from sources operating on a different power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7224/ICM7225 be turned on first.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Theses are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ±10%, T_A = 25°C, V_{SS} = 0V unless otherwise indicated)

ICM7224 CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Operating current	Test circuit, Display blank		10	50	µA
V_{SUPPLY}	Operating supply voltage range ($V_{DD} - V_{SS}$)		3		6	V
I_{OSCI}	OSCILLATOR input current	Pin 36		±2	±10	µA
t_R, t_F	Segment rise/fall time	C_{load} = 200pF		0.5		µs
t_R, t_F	BackPlane rise/fall time	C_{load} = 5000pF		1.5		µs
f_{OSC}	Oscillator frequency	Pin 36 Floating		19		kHz
f_{BP}	Backplane frequency	Pin 36 Floating		150		Hz

ICM7225 CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{STBY}	Operating current display off	Pin 5 (BRighTness) at V_{SS} Pins 29, 31-34 at V_{DD}		10	50	µA
V_{SUPP}	Operating supply voltage range ($V_{DD} - V_{SS}$)		4		6	V
I_{DD}	Operating current	Pin 5 at V_{DD}, Display 18888		200		mA
I_{SLK}	Segment leakage current	Segment Off		±0.01	±1	µA
I_{SEG}	Segment on current	Segment On, Vout = +3V	5	8		mA
I_H	Half-digit on current	Half-digit on, Vout = +3V	10	16		mA

FAMILY CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_P	Input Pullup Currents	Pins 29, 31, 33, 34 Vout = V_{DD} − 3V		10		µA
V_{IH}	Input High Voltage	Pins 29, 31, 33, 34	3			V
V_{IL}	Input Low Voltage	Pins 29, 31, 33, 34			1	V
V_{CT}	$\overline{COUNT}$ Input Threshold			2		V
V_{CH}	$\overline{COUNT}$ Input Hysteresis			0.5		V
I_{OH}	Output High Current	$\overline{CARRY}$ Pin 28 Leading Zero Blanking OUT Pin 30 Vout = V_{DD} − 3V	350	500		µA
I_{OL}	Output Low Current	$\overline{CARRY}$ Pin 28 Leading Zero Blanking Out Pin 30 Vout = +3V	350	500		µA
f_{COUNT}	Count Frequency	4.5V < V_{DD} < 6V	0		15	MHz
t_S,t_R	$\overline{STORE}$, $\overline{RESET}$ Minimum Pulse Width		3			µs

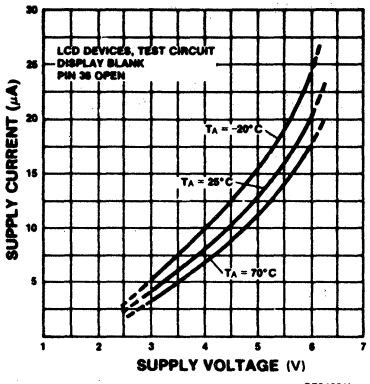
7

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7224/ICM7225

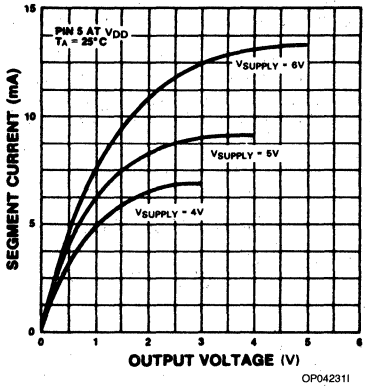
TYPICAL PERFORMANCE CHARACTERISTICS

7224 OPERATING SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



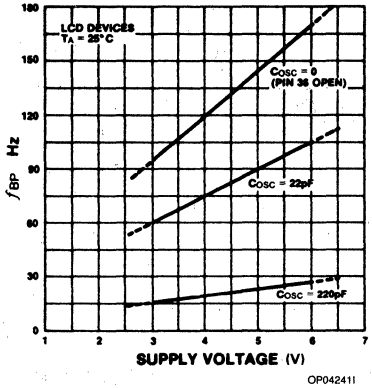
OP04221I

7225 LED SEGMENT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



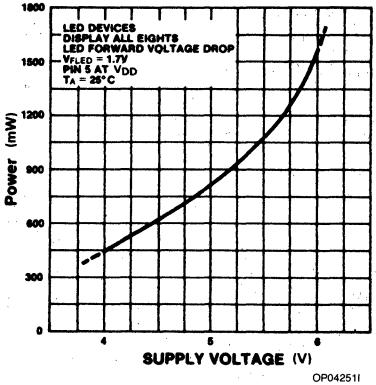
OP04231I

7224 BACKPLANE FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



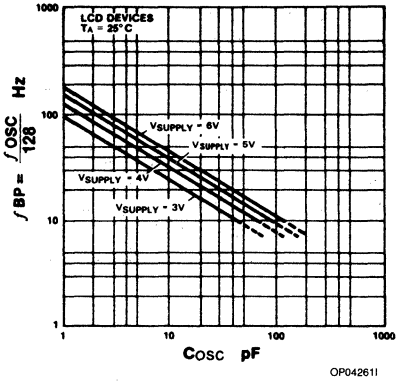
OP04241I

7225 OPERATING POWER (LED DISPLAY) AS A FUNCTION OF SUPPLY VOLTAGE



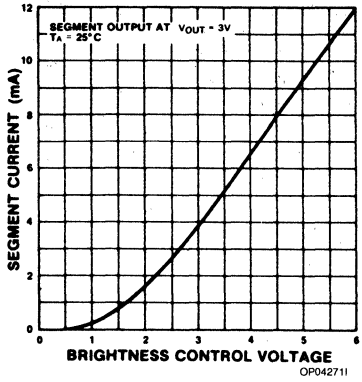
OP04251I

7224 BACKPLANE FREQUENCY AS A FUNCTION OF OSCILLATOR CAPACITOR COSC



OP04261I

7225 LED SEGMENT CURRENT AS A FUNCTION OF BRIGHTNESS CONTROL VOLTAGE



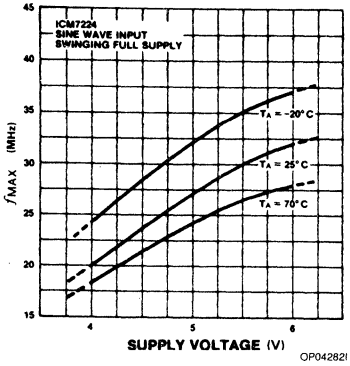
OP04271I

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7224/ICM7225

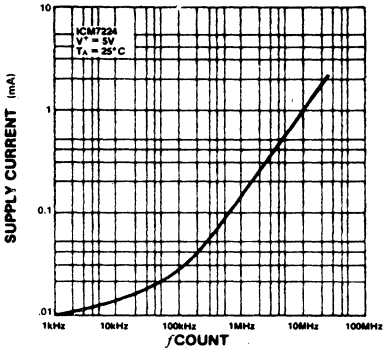
TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

MAXIMUM COUNT FREQUENCY (TYPICAL) AS A FUNCTION OF SUPPLY VOLTAGE



OP04282I

SUPPLY CURRENT AS A FUNCTION OF COUNT FREQUENCY



OP04292I

INPUT	TERMINAL	VOLTAGE	FUNCTION
Leading Zero Blanking INput	29	V_{DD} or Floating V_{SS}	Leading Zero Blanking Enabled Leading Zeroes Displayed
$\overline{\text{COUNT INHIBIT}}$	31	V_{DD} or Floating V_{SS}	Counter Enabled Counter Disabled
$\overline{\text{RESET}}$	33	V_{DD} or Floating V_{SS}	Inactive Counter Reset to 0000
$\overline{\text{STORE}}$	34	V_{DD} or Floating V_{SS}	Output Latches not Updated Output Latches Updated

CONTROL INPUT DEFINITIONS

In this table, V_{DD} and V_{SS} are considered to be normal operating input logic levels. Actual input low and high levels are specified in the Operating Characteristics. For lowest power consumption, input signals should swing over the full supply.

DETAILED DESCRIPTION

LCD Devices

The LCD devices in the family (ICM7224 and ICM7224A) provide outputs suitable for driving conventional 4½-digit by seven segment LCD displays, including 29 individual segment drivers, backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency.

The segment and backplane drivers each consist of a CMOS inverter, with the n- and p-channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any D.C. component which could arise from differing rise and fall times, and ensures maximum display life.

The backplane output devices can be disabled by connecting the OSCILLATOR input (pin 36) to V_{SS}. This synchronizes the 29 segment outputs directly with a signal input at the BP terminal (pin 5) and allows cascading of several slave devices to the backplane output of one master device. The backplane may also be derived from an external source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device will represent a load of approximately 200pF (comparable to one additional segment). The limitation on the number of devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits, and the effect of that load on the backplane rise and fall times. A good rule of thumb to observe in order to minimize power consumption is to keep the rise and fall times less than about 5 microseconds. The backplane driver devices of one device should handle the backplane to a display of 16 one-half-inch characters without the rise and fall times exceeding 5μs (ie, 3 slave devices and the display backplane driven by a fourth master device). It is recommended that if more than four devices are to be slaved together, that the backplane signal be derived externally and all the ICM7224 devices be slaved to it.

This external signal should be capable of driving very large capacitive loads with short (1-2μs) rise and fall times. The maximum frequency for a backplane signal should be about 150Hz, although this may be too fast for optimum display response at lower display temperatures, depending on the display used.

The onboard oscillator is designed to free run at approximately 19kHz, at microampere power levels. The oscillator frequency is divided by 128 to provide the backplane frequency, which will be approximately 150Hz with the oscillator free-running. The oscillator frequency may be reduced by connecting an external capacitor between the OSCillator terminal (pin 36) and V_{DD}; see the plot of oscillator/backplane frequency in "Typical Characteristics" for detailed information.

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7224/ICM7225

The oscillator may also be overdriven if desired, although care must be taken to insure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a D.C. component to the display). This can be done by driving the OSCILLATOR input between the positive supply and a level out of the range where the backplane disable is sensed, about one fifth of the supply voltage above the negative supply. Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

LED Devices

The LED devices in the family (ICM7225, ICM7225A) provide outputs suitable for directly driving 4½-digit by seven segment common-anode LED displays, including 28 individual segment drivers and one half-digit driver, each consisting of a low-leakage current-controlled open-drain n-channel transistor.

The drain current of these transistors can be controlled by varying the voltage at the BRighTness input (pin 5). The voltage at this pin is transferred to the gates of the output devices for "on" segments, and thus directly modulates the transistor's "on" resistance. A brightness control can be easily implemented with a single potentiometer controlling the voltage at pin 5, connected as in Figure 3. The potentiometer should be a high value (100kΩ to 1MΩ) to minimize power consumption, which can be significant when the display is off.

The BRighTness input may also be operated digitally as a display enable; when a V_{DD}, the display is fully on, and at V_{SS}, fully off. The display brightness may also be controlled by varying the duty cycle of a signal swinging between the two supplies at the BRighTness input.

Note that the LED devices have two connections for V_{SS}; both should be connected. The double connection is necessary to minimize effects of bond wire resistance with the large total display currents possible.

When operating the LED devices at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperatures. The maximum power dissipation is 1 watt at 25°C, derated linearly above 35°C to 500mW at 70°C (15mW/°C above 35°C). Power dissipation for the device is given by:

$$P = (V_{DD} - V_{FLED}) \times (I_{SEG}) \times (n_{SEG})$$

where V_{FLED} is the LED forward voltage drop, I_{SEG} is segment current, and n_{SEG} is the number of "ON" segments. It is recommended that if the device is to be operated at elevated temperatures the segment current be limited by use of the BRighTness input to keep power dissipation within the limits described above.

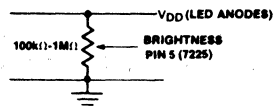


Figure 3: Brightness Control

COUNTER SECTION

The devices in the ICM7224/ICM7225 family implement a four-digit ripple carry resettable counter, including a Schmitt trigger on the COUNT input and a $\overline{\text{CARRY}}$ output. Also included is an extra D-type flip-flop, clocked by the $\overline{\text{CARRY}}$ signal and outputting to the half-digit segment driver, which can be used as either a true half-digit or as an overflow indicator. The counter will index on the negative-going edge of the signal at the COUNT input, while the $\overline{\text{CARRY}}$ output provides a negative-going edge following the count which indexes the counter from 9999 (or 5959) to 10000. Once the half-digit flip-flop has been clocked, it can only be reset (with the rest of the counter) by a negative level at the $\overline{\text{RESET}}$ terminal, pin 33. However, the four decades will continue to count in a normal fashion after the half-digit is set, and subsequent $\overline{\text{CARRY}}$ outputs will not be affected.

A negative level at the $\overline{\text{COUNT INHIBIT}}$ input disables the first divide-by-two in the counter chain without affecting its clock. This provides a true inhibit, not sensitive to the state of the COUNT input, which prevents false counts that can result from using a normal logic gate to prevent counting.

Each decade of counter drives directly into a four-to-seven decoder which develops the seven-segment output code. The output data is latched at the driver, when the $\overline{\text{STORE}}$ pin is low, these latches are updated, and when high or floating, the latches hold their contents.

The decoders also include zero detect and blanking logic to provide leading zero blanking. When the Leading Zero Blanking INput is floating or at a positive level, this circuitry is enabled and the device will blank leading zeroes; when low, or the half-digit is set, leading zero blanking is inhibited, and zeroes in the four digits will be displayed. The Leading Zero Blanking OUTput is provided to allow cascaded devices to blank leading zeroes correctly. This output will assume a positive level only when all four digits are blanked; this can only occur when the Leading Zero Blanking INput is at a positive level and the half-digit is not set.

For example, in an eight-decade counter with overflow using two ICM7224/ICM7225 devices, the Leading Zero Blanking OUTput of the high order digit would be connected to the Leading Zero Blanking INput of the low order digit device. This will assure correct leading zero blanking for all eight digits.

The $\overline{\text{STORE}}$, $\overline{\text{RESET}}$, $\overline{\text{COUNT INHIBIT}}$, and Leading Zero Blanking INputs are provided with pullup devices, so that they may be left open when a positive level is desired. The $\overline{\text{CARRY}}$ and Leading Zero Blanking OUTputs are suitable for interfacing to CMOS logic in general, and are specifically designed to allow cascading of ICM7224 to ICM7225 devices in four-digit blocks.

Note: All typical values have been guaranteed by characterization and are not tested.

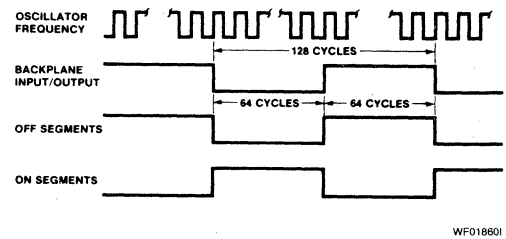


Figure 4: Display Waveforms

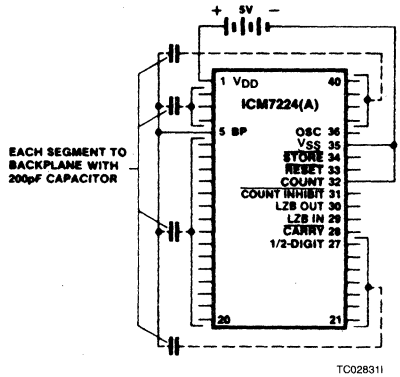


Figure 5: Test Circuit

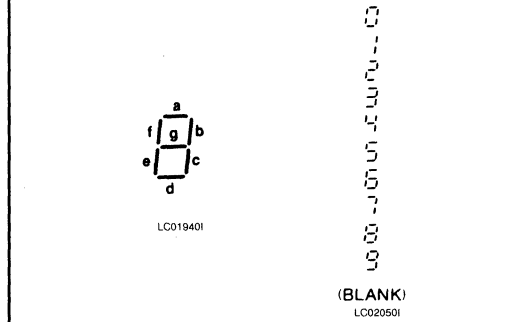


Figure 6: Segment Assignment and Display Font

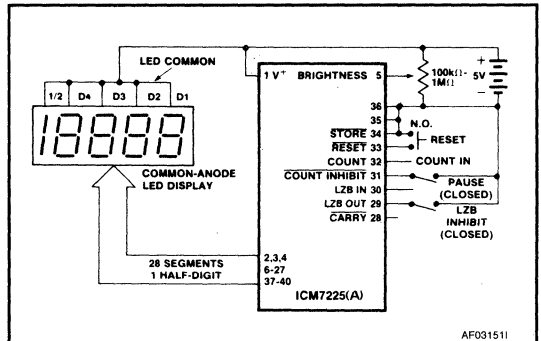


Figure 7: Typical Application (Unit Counter)

APPLICATIONS

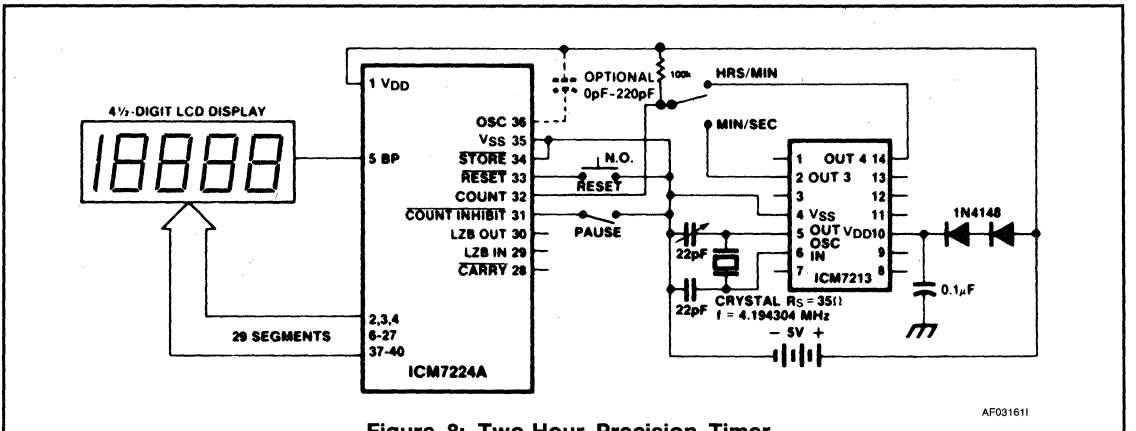


Figure 8: Two-Hour Precision Timer

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7224/ICM7225

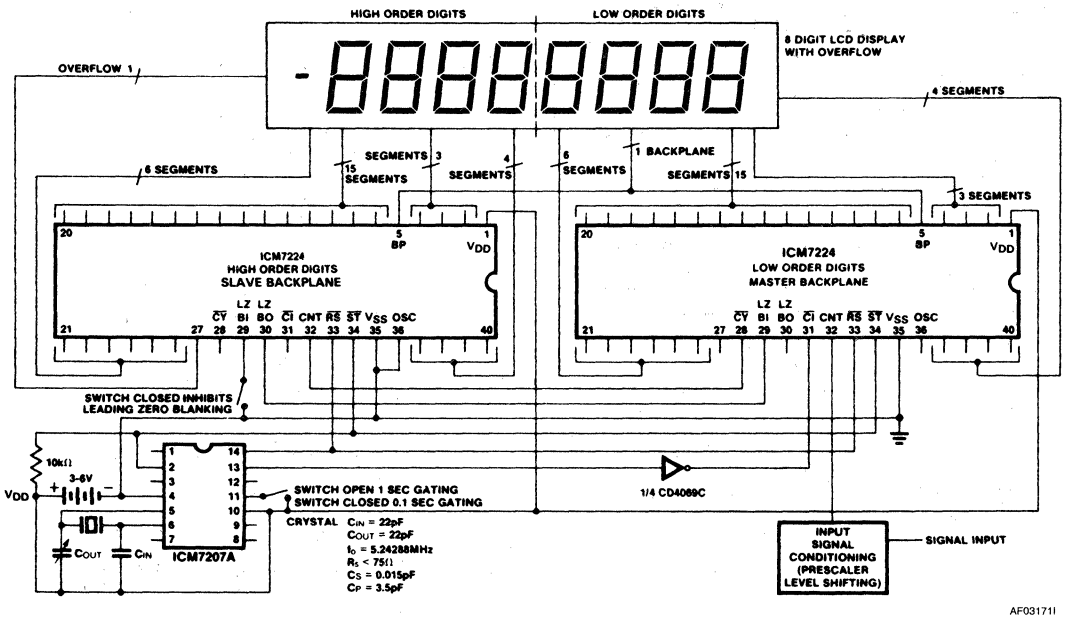


Figure 9: Eight-Digit Precision Frequency Counter

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7226A/B
8-Digit Multi-Function Frequency Counter/Timer

GENERAL DESCRIPTION

The ICM7226 is a fully integrated Universal Counter and LED display driver. It combines a high frequency oscillator, a decade timebase counter, an 8 decade data counter and latches, a 7 segment decoder, digit multiplexer, and segment and digit drivers which can directly drive large LED displays. The counter inputs accept a maximum frequency of 10MHz in **frequency** and **unit counter** modes and 2MHz in the other modes. Both inputs are digital inputs. In many applications, amplification and level shifting will be required to obtain proper digital signals for these inputs.

The ICM7226 can function as a frequency counter, period counter, frequency ratio (f_A/f_B) counter, time interval counter or a totalizing counter. The devices require either a 10MHz or 1MHz crystal timebase, or if desired an external timebase can also be used. For **period** and **time interval,** the 10MHz timebase gives a 0.1μs resolution. In **period average** and **time interval average,** the resolution can be in the nanosecond range. In the **frequency** mode, the user can select accumulation time of 10ms, 100ms, 1s and 10s. With a 10s accumulation time, the frequency can be displayed to a resolution of 0.1Hz. There is a 0.2s interval between measurements in all ranges. Control signals are provided to enable gating and storing of prescaler data.

Leading zero blanking has been incorporated with frequency display in kHz and time in μs. The display is multiplexed at a 500Hz rate with a 12.2% duty cycle for each digit. The ICM7226A is designed for common anode displays with typical peak segment currents of 25mA, and the ICM7226B is designed for common cathode displays with typical segment currents of 12mA. In the **display off** mode, both digit drivers & segment drivers are turned off, allowing the display to be used for other functions.

FEATURES

- **CMOS Design for Very Low Power**
- **Output Drivers Directly Drive Both Digits and Segments of Large 8 Digit LED Displays. Both Common Anode and Common Cathode Versions Are Available**
- **Measures Frequencies From DC to 10MHz; Periods From 0.5μs to 10s**
- **Stable High Frequency Oscillator Uses Either 1MHz or 10MHz Crystal**
- **Control Signals Available for External Systems Operation**
- **Multiplexed BCD Outputs**

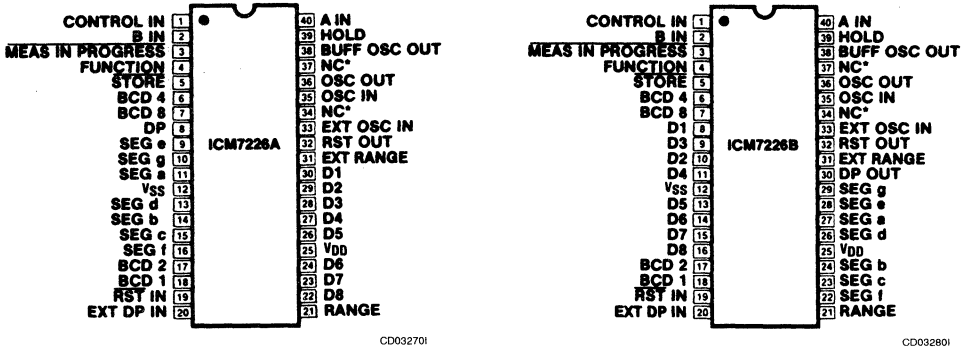
APPLICATIONS

- **Frequency Counter**
- **Period Counter**
- **Unit Counter**
- **Frequency Ratio Counter**
- **Time Interval Counter**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7226AIPL	-25°C to +55°C	40 pin PLASTIC DIP
ICM7226A/D	—	DICE
ICM7226BIJL	-25°C to +85°C	40 pin CERDIP
ICM7226B/D	—	DICE
ICM7226AIJL	-25°C to 85°C	40 pin CERDIP
ICM7226BIPL	-25°C to 85°C	40 pin PLASTIC DIP

NOTE: An evaluation kit is available for these devices — order ICM7226AEV/KIT.



*For maximum frequency stability, connect to V_{DD} or V_{SS}

Figure 1: Pin Configurations

-002

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7226A/B

ABSOLUTE MAXIMUM RATINGS

Maximum Supply Voltage ($V_{DD} - V_{SS}$) 6.5V
Maximum Digit Output Current 400mA
Maximum Segment Output Current.....60mA
Voltage on any Input or Output Terminal (Note 1).....
(V_{SS} −0.3V) to (V_{DD} +0.3V)

Maximum Power Dissipation at 70°C (Note 2)
ICM7226A.....1.0W
ICM7226B.....0.5W
Operating Temperature Range .....−25°C to +85°C
Storage Temperature Range.....−55°C to +125°C
Lead Temperature (Soldering, 10sec) .....300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

***Note 1:** Destructive latchup may occur if input signals are applied before the power supply is established or if inputs or outputs are forced to voltages exceeding V_{DD} or V_{SS} by 0.3V.

Note 2: Assumes all leads soldered or welded to PC board and free air flow.

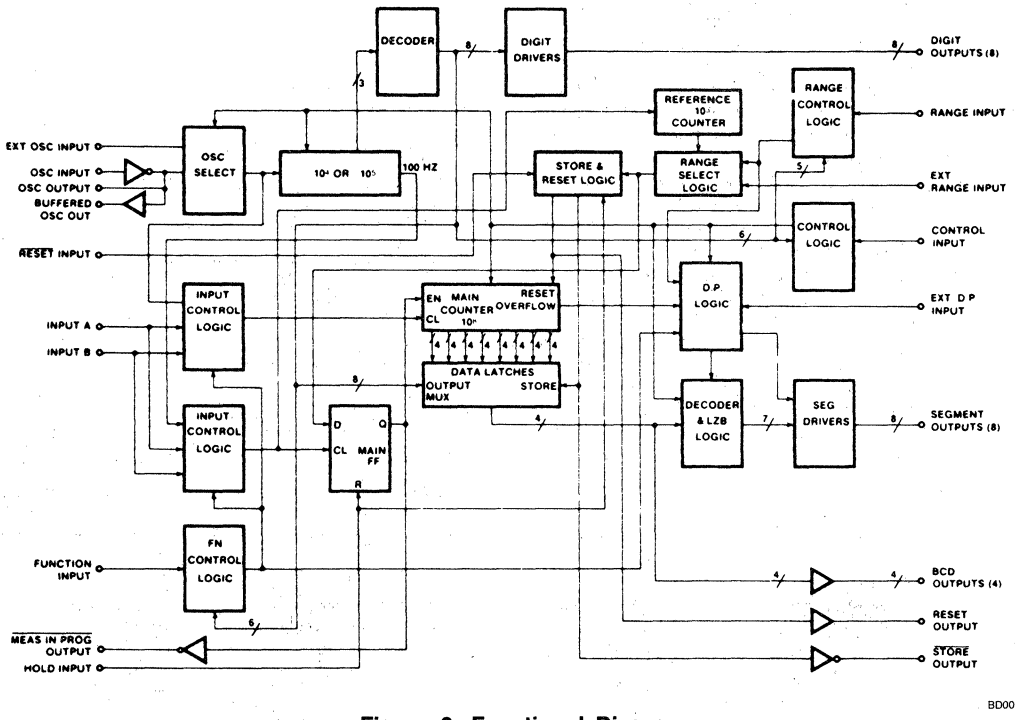


Figure 2: Functional Diagram

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7226A/B

INTERSIL

ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0V, T_A = 25°C, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Operating Supply Current	Display Off Unused inputs to V_{SS}		2	5	mA
V_{SUPPLY}	Supply Voltage Range $V_{DD} - V_{SS}$	$-25°C < T_A < 85°C$ Input A, Input B Frequency at f_{MAX}	4.75		6.0	V
$f_{A(max)}$	Maximum Guaranteed Frequency Input A, Pin 40	$-25°C < T_A < 85°C$ $4.75V < V_{DD} < 6.0V$ Figure 4 Function = Frequency, Ratio, Unit Counter Function = Period, Time Interval	 10 2.5	 14		MHz
$f_{B(max)}$	Maximum Frequency Input B, Pin 2	$-25°C < T_A < 85°C$ $4.75V < V_{DD} < 6.0V$ Figure 5	2.5			
	Minimum Separation Input A to Input B Time Interval Function	$-25°C < T_A < 85°C$ $4.75V < V_{DD} < 6.0V$ Figure 6	250			ns
f_{OSC}	Osc. freq. and ext. osc. freq. (minimum ext. osc. freq.)	$-25°C < T_A < 85°C$ $4.75V < V_{DD} < 6.0V$	10 (0.1)			MHz
g_m	Oscillator Transconductance	V_{DD} = 4.75V T_A = +85°C	2000			μs
f_{mux}	Multiplex Frequency	f_{osc} = 10MHz		500		Hz
	Time Between Measurements	f_{osc} = 10MHz		200		ms
dV_{in}/dt	Input Rate of Charge	Inputs A, B		15		mV/μs
V_{IL}	INPUT VOLTAGES PINS 2, 19, 33, 39, 40, 35 input low voltage	$-25°C < T_A < +85°C$			1.0	V
V_{IH}	input high voltage		3.5			
I_{ILK}	PIN 2, 39, 40 INPUT LEAKAGE, A, B				20	μA
R_{IN}	Input resistance to V_{DD} PINS 19,33	$V_{IN} = V_{DD} - 1.0V$	100	400		kΩ
R_{IN}	Input resistance to V_{SS} PIN 31	$V_{IN} = +1.0V$	50	100		
I_{OL}	Output Current PINS 3,5,6,7,17,18,32,38	$V_{OL} = +0.4V$	400			μA
I_{OH}	PINS 5,6,7,17,18,32	$V_{OH} = +2.4V$	100			μA
I_{OH}	PINS 3,38	$V_{OH} = V_{DD} - 0.8V$	265			
I_{OH}	**ICM7226A** PINS 22,23,24,26,27,28,29,30 DIGIT DRIVER high output current	$V_O = V_{DD} - 2.0V$	150	180		mA
I_{OL}	low output current	$V_O = +1.0V$		−0.3		
I_{OL}	SEGMENT DRIVER PINS 8,9,10,11,13,14,15,16 low output current	$V_O = +1.5V$	25	35		mA
I_{OH}	high output current	$V_O = V_{DD} - 1.0V$		100		μA
V_{IL}	MULTIPLEX INPUTS PINS 1,4,20,21 input low voltage				0.8	V
V_{IH}	input high voltage		2.0			
R_{IN}	input resistance to V_{SS}	$V_{IN} = +1.0V$	50	100		kΩ

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7226A/B

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	ICM7226B					
	DIGIT DRIVER					
	PINS 8,9,10,11,13,14,15,16					
I_{OL}	low output current	V_O = +1.0V	50	75		mA
I_{OH}	high output current	$V_O = V_{DD} - 2.5V$		100		µA
	SEGMENT DRIVER					
	PINS 22,23,24,26,27,28,29,30					
I_{OH}	high output current	$V_O = V_{DD} - 2.0V$	10	15		mA
I_L	leakage current	$V_O = V_{SS}$			10	µA
	MULTIPLEX INPUTS					
	PINS 1,4,20,21					
V_{IL}	input low voltage				$V_{DD} - 2.0$	V
V_{IH}	input high voltage		$V_{DD} - 0.8$			
R_{IN}	input resistance to V_{DD}	$V_{IN} = V_{DD} - 1.0V$	100	360		kΩ

NOTE: Typical values are not tested.

EVALUATION KIT

An evaluation kit is available for the ICM7226A. It includes all the components necessary to assemble and evaluate a universal frequency/period counter based on the ICM7226A. With the help of this kit, an engineer or technician can have the ICM7226A "up-and-running" in less than an hour. Specifically, the kit contains an ICM7226AIJL, a 10MHz quartz crystal, eight each 7-segment 0.3" LEDs, PC board, resistors, capacitors, diodes, switches and IC socket. Order Number ICM7226AEV/Kit.

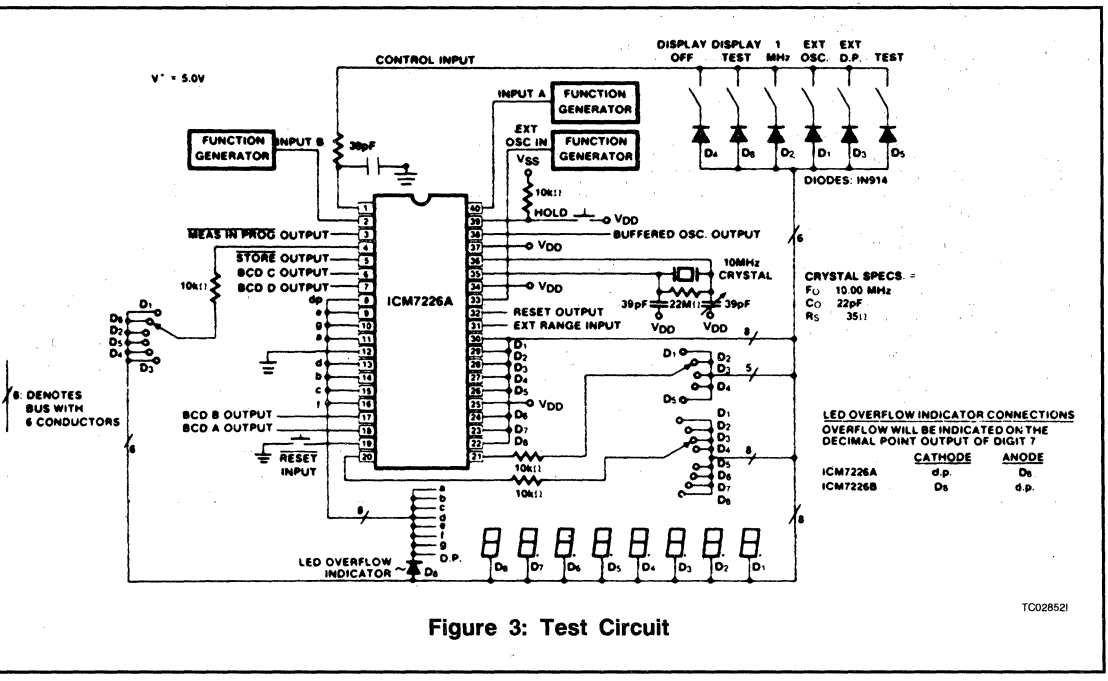
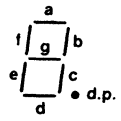
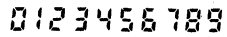


Figure 3: Test Circuit

Note: All typical values have been guaranteed by characterization and are not tested.



LC01960I



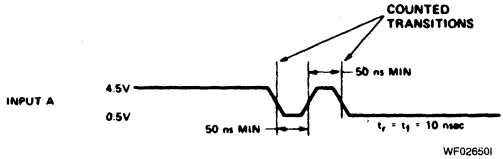
LC01970I

LED overflow indicator connections:

Overflow will be indicated on the decimal point output of digit 8.

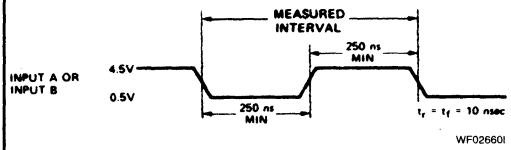
	CATHODE	ANODE
ICM7226A	d.p.	D_8
ICM7226B	D_8	d.p.

Figure 4: Segment Identification and Display Font



WF02650I

Figure 5: Waveform for Guaranteed Minimum f_A(max) Function = Frequency, Frequency Ratio, Unit Counter.



WF02660I

Figure 6: Waveform for Guaranteed Minimum f_B(max) and f_A(max) for Function = Period and Time Interval.

TIME INTERVAL MEASUREMENT

The ICM7226A/B can be used to accurately measure the time interval between two events. With a 10 MHz time-base crystal, the time between the two events can be as long as ten seconds. Accurate resolution in time interval measurement is 100ns.

The feature operates with Channel A going low at the start of the event to be measured, followed by Channel B going low at the end of the event.

When in the **time interval** mode and measuring a single event, the ICM7226A/B must first be "primed" prior to measuring the event of interest. This is done by first generating a negative going edge on Channel A followed by a negative going edge on Channel B to start the "measurement interval." The inputs are then primed ready for the measurement. Positive going edges on A and B, before or after the priming, will be needed to restore the original condition.

Following the priming procedure (when in single event or 1 cycle range input) the device is ready to measure one (only) event.

When timing repetitive signals, it is not necessary to "prime" the ICM7226A/B as the first alternating signal states automatically prime the device. See Figure 7.

During any time interval measurement cycle, the ICM7226A/B requires 200ms following B going low to update all internal logic. A new measurement cycle will not take place until completion of this internal update time.

DETAILED DESCRIPTION

INPUTS A & B

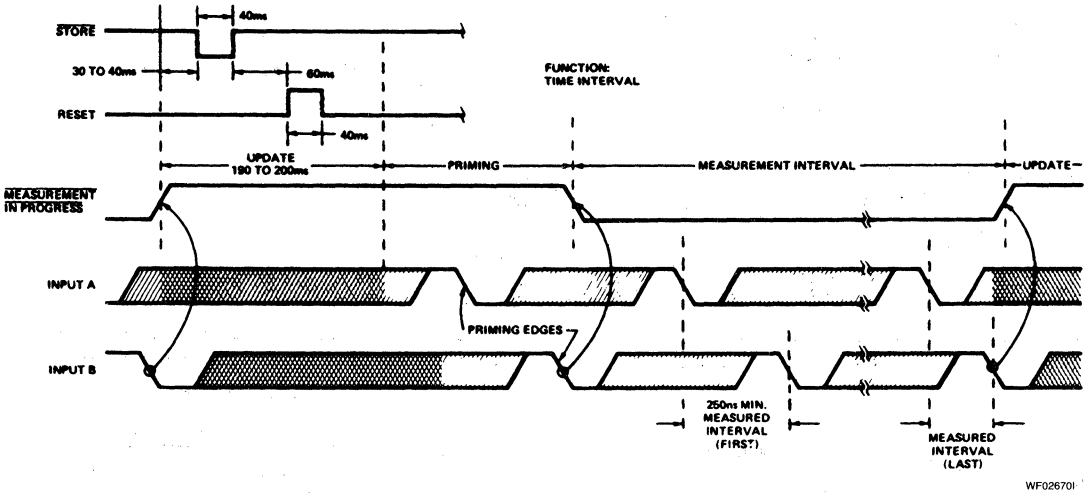
The signal to be measured is applied to INPUT A in **frequency period, unit counter, frequency ratio** and **time interval** modes. The other input signal to be measured is applied to INPUT B in **frequency ratio** and **time interval.** f_A should be higher than f_B during **frequency ratio**.

Both inputs are digital inputs with a typical switching threshold of 2.0V at V_{DD} = 5.0V and input impedance of 250kΩ. For optimum performance, the peak to peak input signal should be at least 50% of the supply voltage and centered about the switching voltage. When these inputs are being driven from TTL logic, it is desirable to use a pullup resistor. The circuit counts high to low transitions at both inputs.

Note: The amplitude of the input should not exceed the supply by more than 0.3V otherwise, the circuit may be damaged.

7

Note: All typical values have been guaranteed by characterization and are not tested.



NOTE: IF RANGE IS SET TO 1 EVENT, FIRST AND LAST MEASURED INTERVAL WILL COINCIDE.

Figure 7: Waveforms for Time Interval Measurement (Others are similar, without priming phase)

This can be easily accomplished with the following circuit: (Figure 8).

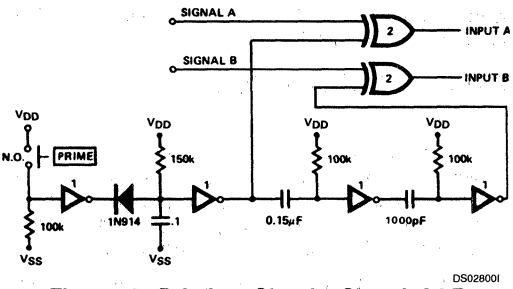


Figure 8: Priming Circuit, Signal A&B High or Low

DEVICE	TYPE
1	CD4049B Inverting Buffer
2	CD4070B Exclusive-OR

MULTIPLEXED INPUTS

The FUNCTION, RANGE, CONTROL and EXTERNAL DECIMAL POINT inputs are time multiplexed to select the input function desired. This is achieved by connecting the appropriate digit driver output to the inputs. The input function, range and control inputs must be stable during the last half of each digit output, (typically 125μs). The multiplex inputs are active high for the common anode ICM7226A, and active low for the common cathode ICM7226B.

Noise on the multiplex inputs can cause improper operation. This is particularly true when the **unit counter** mode of operation is selected, since changes in voltage on the digit drivers can be capacitively coupled through the LED diodes to the multiplex inputs. For maximum noise immunity, a 10kΩ resistor should be placed in series with the multiplex inputs as shown in the application notes.

Table 1 shows the functions selected by each digit for these inputs.

Table 1: Multiple Input Control

	FUNCTION	DIGIT
FUNCTION INPUT Pin 4	Frequency	D_1
	Period	D_8
	Frequency Ratio	D_2
	Time Interval	D_5
	Unit Counter	D_4
	Oscillator Frequency	D_3
RANGE INPUT PIN 21	0.01 Sec/1 Cycle	D_1
	0.1 Sec/10 cycles	D_2
	1 Sec/100 Cycles	D_3
	10 Sec/1k Cycles	D_4
PIN 31	Enable External Range Input	D_5
CONTROL INPUT PIN 1	Display Off	D_4 & Hold
	Display Test	D_8
	1MHz Select	D_2
	External Oscillator Enable	D_1
	External Decimal Point Enable	D_3
EXTERNAL DECIMAL POINT INPUT, PIN 20	Decimal Point is Output for Same Digit That is Connected to This Input	

CONTROL INPUTS

Display Test — All segments are enabled continuously, giving a display of all 8's with decimal points. The display will be blanked if **display off** is selected at the same time.

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7226A/B

Display Off — To enable the **display off** mode it is necessary to tie D_4 to the CONTROL input and have the HOLD input at V_{DD}. The chip will remain in this mode until HOLD is switched low. While in the **display off** mode, the segment and digit driver outputs are open and the oscillator continues to run (with a typical supply current of 1.5mA with a 10MHz crystal) but no measurements are made. In addition, signals applied to the multiplexed inputs have no effect. A new measurement is initiated after the HOLD input goes low. (This mode does not operate when functioning as a unit counter.)

1MHz Select — The **1MHz select** mode allows use of a 1MHz crystal with the same digit multiplex rate and time between measurements as a 10MHz crystal. The internal decimal point is also shifted one digit to the right in **period** and **time interval,** since the least significant digit will be in 1μs increments rather than 0.1μs.

External Oscillator Enable — In this mode, the EXTernal OSCillator INput is used, rather than the on-chip oscillator, for the Timebase and Main Counter inputs in **period** and **time interval** modes. The on-chip oscillator will continue to function when the external oscillator is selected, but have no effect on circuit operation. The external oscillator input frequency must be greater than 100kHz or the chip will reset itself and enable the on-chip oscillator. Connect external oscillator to **both** OSC IN (pin 35) and EXT OSC IN (pin 33), or provide crystal for "default" oscillation, to avoid hang-up problems if an external OSC or TXCO will always be used, AC couple to OSC IN.

External Decimal Point Enable — When **external decimal point** is enabled, a decimal point will be displayed whenever the digit driver connected to the EXTERNAL DECIMAL POINT pin is active. Leading Zero Blanking will be disabled for all digits following the decimal point.

RANGE INPUT

The range input selects whether the measurement is made for 1, 10, 100 or 1000 counts of the reference counter, or if the EXTernal RANGE INput determines the measurement time. In all functional modes except **unit counter,** a change in the RANGE input will stop the measurement in progress, without updating the display, and initiate a new measurement. This prevents an erroneous first reading after the RANGE input is changed.

FUNCTION INPUT

Six functions can be selected. They are: **Frequency, Period, Time Interval, Unit Counter, Frequency Ratio and Oscillator Frequency.**

These functions select which signal is counted into the main counter and which signal is counted by the reference counter, as shown in Table 2. In **time interval** a flip flop is set first by a 1→ 0 transition at INPUT A and then reset by a 1→ 0 transition at INPUT B. The oscillator is gated into the Main Counter during the time the flip flop is set. A change in the FUNCTION input will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the FUNCTION input is changed. If the main counter overflows, an overflow indication is output on the Decimal Point Output during D_8.

Table 2: Input Routing

DESCRIPTION	MAIN COUNTER	REFERENCE COUNTER
Frequency (f_A)	Input A	100 Hz (Oscillator ÷ 10^5 or 10^4)
Period (t_A)	Oscillator	Input A
Ratio (f_A/f_B)	Input A	Input B
Time Interval (A→B)	Osc ON Gate	Osc OFF Gate
Unit Counter (Count A)	Input A	Not Applicable
Osc. Freq. (f_{osc})	Oscillator	100 Hz (Oscillator ÷ 10^5 or 10^4)

EXTERNAL DECIMAL POINT INPUT

When the **external decimal point** is selected, this input is active. Any of the digits, except D_8, can be connected to this point. D_8 should not be used since it will override the overflow output and leading zeros will remain unblanked after the decimal point.

HOLD Input — Except in the **unit counter** mode, when the HOLD input is at V_{DD}, any measurement in progress (before $\overline{\text{STORE}}$ goes low) is stopped, the main counter is reset and the chip is held ready to initiate a new measurement as soon as HOLD goes low. The latches which hold the main counter data are not updated, so the last complete measurement is displayed. In **unit counter** mode when HOLD input is at V_{DD}, the counter is not stopped or reset, but the display is frozen at that instantaneous value. When HOLD goes low the count continues from the new value in the counter.

$\overline{\text{RESET}}$ Input — The $\overline{\text{RESET}}$ Input resets the main counter, stops any measurement in progress, and enables the main counter latches, resulting in an all zero output. A capacitor to ground will prevent any hang-ups on power-up.

EXTernal RANGE Input — The EXTernal RANGE Input is used to select other ranges than those provided on the chip. Figure 9 shows the relationship between $\overline{\text{MEASurement IN PROGRESS}}$ and EXTernal RANGE Input.

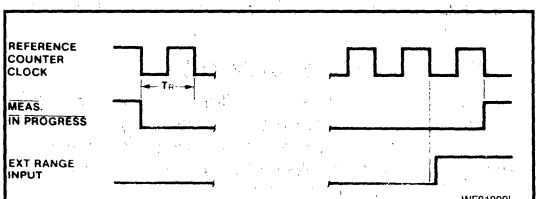


Figure 9: External Range Input to End of MEASUREMENT IN PROGRESS.

$\overline{\text{MEASUREMENT IN PROGRESS}}$, $\overline{\text{STORE}}$ AND RESET Outputs — These Outputs are provided to facilitate external interfacing. Figure 10 shows the relationship between these signals during the time between measurements. All three outputs can drive a low power Schottky TTL load. The $\overline{\text{MEASUREMENT IN PROGRESS}}$ output can directly drive one ECL load, if the ECL device is powered from the same power supply as the ICM7226.

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7226A/B

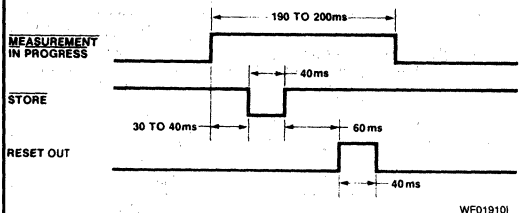


Figure 10: RESET OUT, STORE, and MEASUREMENT IN PROGRESS Outputs Between Measurements.

BCD Outputs — The BCD representation of each digit output is available at the BCD outputs; see Table 3 for Truth Table. The positive going (ICM7226A-Common Anode) or negative going (ICM7226B — Common Cathode) digit drivers lag the BCD data by 2 to 6 microseconds; the leading edge of the digit drive signal should be used to externally latch the BCD data. Each BCD output will drive one low power Schottky TTL load. The display is multiplexed from MSD to LSD. Leading zero blanking has no effect on the BCD outputs.

Table 3: Truth Table BCD Outputs

NUMBER	BCD 8 PIN 7	BCD 4 PIN 6	BCD 2 PIN 17	BCD 1 PIN 18
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

BUFFered OSCillator OUTput — The BUFFered OSCillator OUTput has been provided to enable use of the on chip oscillator signal without loading the oscillator itself. This output will drive one low power Schottky TTL load. Care should be taken to minimize capacitive loading on this pin.

DISPLAY CONSIDERATIONS

The display is multiplexed at a 500Hz rate with a digit time of 244μs, and an interdigit blanking time of 6μs to prevent ghosting between digits. The decimal point and leading zero blanking have been implemented for right hand decimal point displays; zeros following the decimal point will not be blanked. Leading zero blanking will also be disabled if the Main Counter overflows. The internal decimal point control displays frequency in kHz and time in μs.

The ICM7226A is designed to drive common anode LED displays at a peak current of 25mA/segment, using displays with V_F = 1.8V at 25mA. The average DC current will be greater than 3mA under these conditions. The ICM7226B is designed to drive common cathode displays at a peak current of 15mA/segment, using displays with V_F = 1.8V at 15mA. Resistors can be added in series with the segment drivers to limit the display current, if required. Figures 11, 12, 13 and 14 show the digit and segment currents as a function of output voltage for common anode and common cathode drivers.

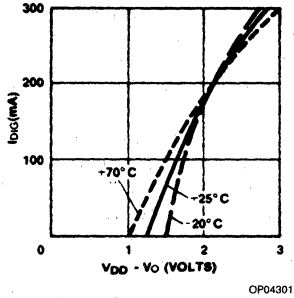


Figure 11: ICM7226A Typical I_{DIG} vs. $V_{DD}-V_O$ 4.5 ≤ V_{DD} ≤ 6.0V

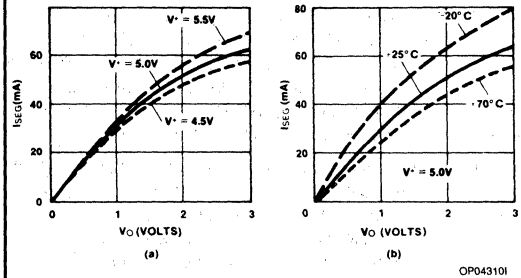


Figure 12: ICM7226A Typical I_{SEG} vs. V_O

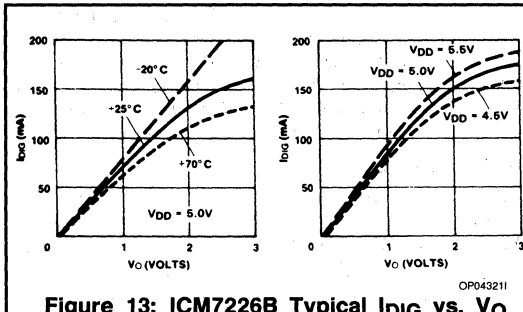


Figure 13: ICM7226B Typical I_{DIG} vs. V_O

Note: All typical values have been guaranteed by characterization and are not tested.

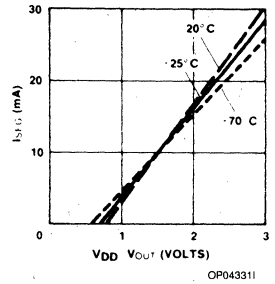


Figure 14: ICM7226B Typical I_{SEG} vs. (V_{DD}-V_O) 4.5V ≤ V_{DD} ≤ 6.0V

To increase the light output from the displays, V_{DD} may be increased to 6.0V, however care should be taken to see that maximum power and current ratings are not exceeded.

The SEGment and Digit outputs in both the 7226A and B are not directly compatible with either TTL or CMOS logic. Therefore, level shifting with discrete transistors may be required to use these outputs as logic signals. External latching should be done on the leading edge of the digit signal.

ACCURACY

In a Universal Counter, crystal drift and quantization errors cause errors. In **frequency, period** and **time interval** modes, a signal derived from the oscillator is used either in the Reference Counter or Main Counter, and in these modes, an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficient of 20ppm/°C will cause a measurement error of 20ppm/°C.

In addition, there is a quantization error inherent in any digital measurement of ±1 count. Clearly this error is reduced by displaying more digits. In the **frequency** mode, maximum accuracy is obtained with high frequency inputs, and in **period** mode maximum accuracy is obtained with low frequency inputs. As can be seen in Figure 15, the least accuracy will be obtained at 10kHz. In **time interval** measurements there is a maximum error of 1 count per interval. As a result there is the same inherent accuracy in all ranges, as shown in Figure 16. In **frequency ratio** measurement more accuracy can be obtained by averaging over more cycles of INPUT B as shown in Figure 17.

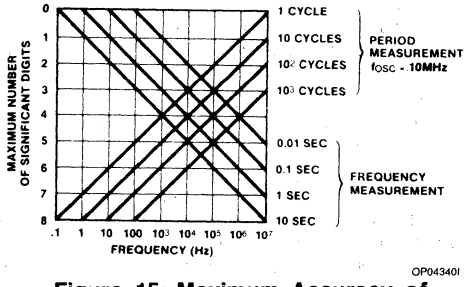


Figure 15: Maximum Accuracy of Frequency and Period Measurements Due to Limitations of Quantization Errors.

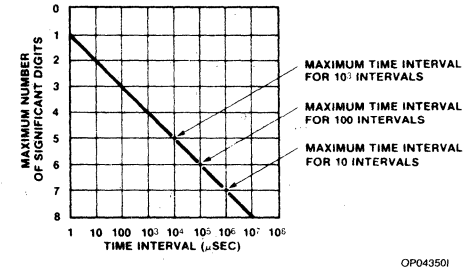


Figure 16: Maximum Accuracy of Time Interval Measurement Due to Limitations of Quantization Errors.

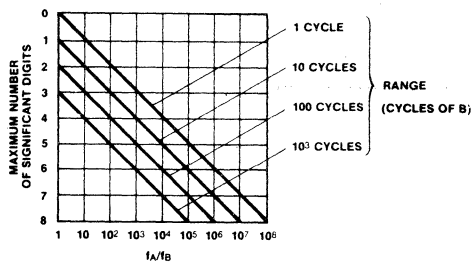


Figure 17: Maximum Accuracy for Frequency Ratio Measurement Due to Limitations of Quantization Errors.

CIRCUIT APPLICATIONS

The ICM7226 has been designed as a complete stand alone Universal Counter, or used with prescalers and other circuitry in a variety of applications. Since A IN and B IN are digital inputs, additional circuitry will be required in many applications, for input buffering, amplification, hysteresis, and level shifting to obtain the required digital voltages. For many applications an FET source follower can be used for input buffering, and an ECL 10116 line receiver can be used for amplification and hysteresis to obtain high impedance

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7226A/B

input, sensitivity and bandwidth. However, cost and complexity of this circuitry can vary widely, depending upon the sensitivity and bandwidth required. When TTL prescalers or input buffers are used, pull up resistors to V_{DD} should be used to obtain optimal voltage swing at A IN and B IN.

If prescalers aren't required, the ICM7226 can be used to implement a minimum component Universal counter as shown in Figure 18.

For input frequencies up to 40MHz, the circuit shown in figure 14 can be used to implement a **frequency and period counter.** To obtain the correct value when measuring frequency and period, it is necessary to divide the 10MHz oscillator frequency down to 2.5MHz. In doing this the time between measurements is lengthened to 800ms and the display multiplex rate is decreased to 125Hz.

If the input frequency is prescaled by ten, the oscillator frequency can remain at either 10MHz or 1MHz, but the decimal point must be moved. Figure 20 shows use of a ÷ 10 prescaler in **frequency counter** mode. Additional logic has been added to enable the 7226 to count the input directly in **period** mode for maximum accuracy. Note that A IN comes from Q_C rather than Q_D, to obtain an input duty cycle of 40%. If an output with a duty cycle not near 50% must be used then it may be necessary to use a 74LS121 monostable multivibrator or similar circuit to stretch the input pulse to guarantee a 50ns minimum pulse width.

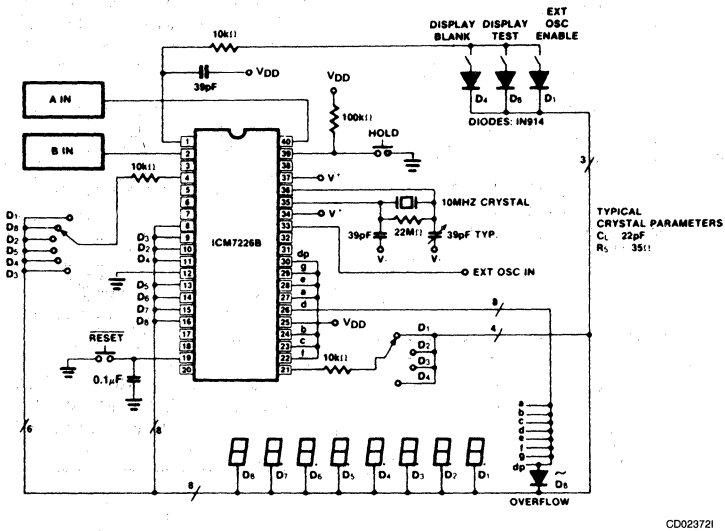
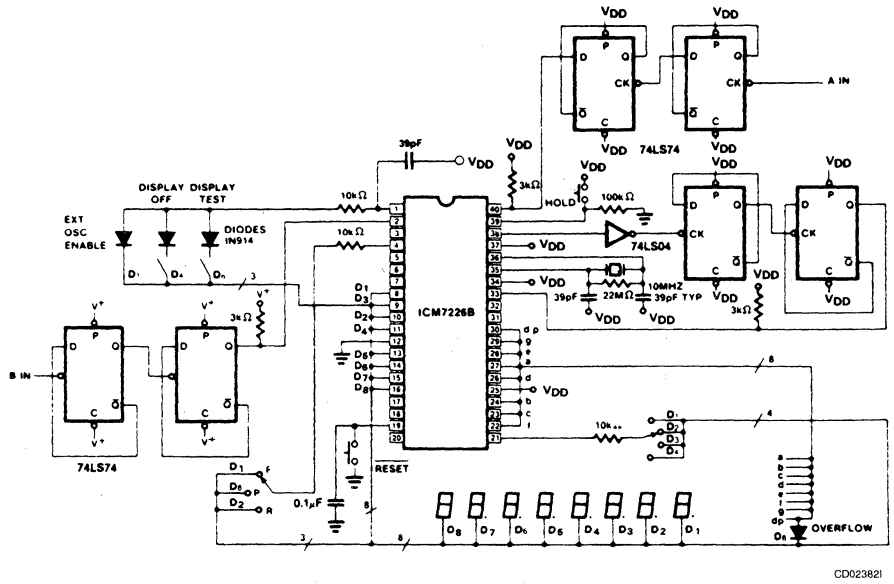


Figure 18: 10MHz Universal Counter

Note: All typical values have been guaranteed by characterization and are not tested.



Notes: 1) If a 2.5MHz crystal is used, diode D1 and I.C.'s 1 and 2 can be eliminated.

Figure 19: 40MHz Frequency, Period Counter

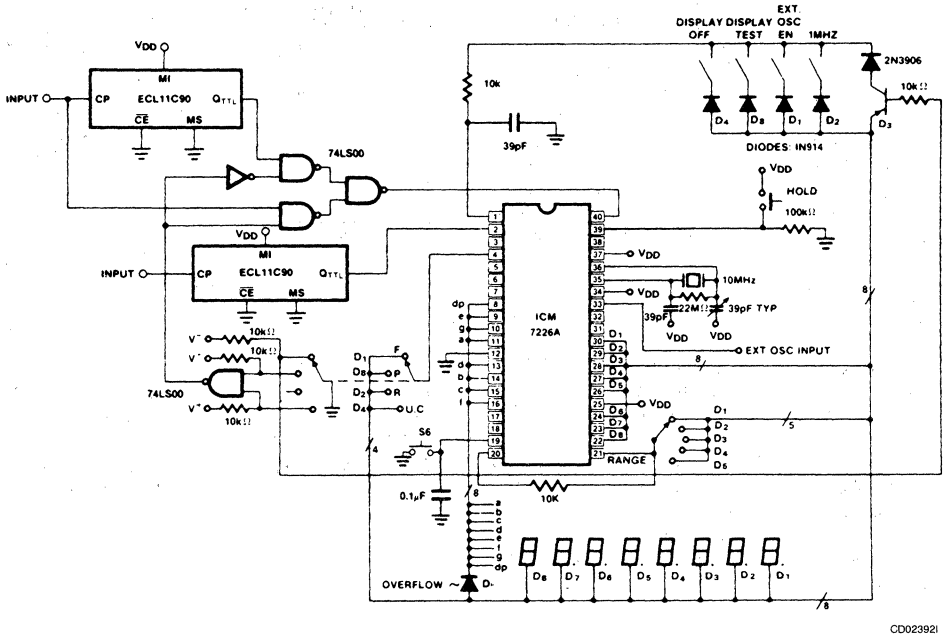


Figure 20: 100MHz Multi Function Counter

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7226A/B

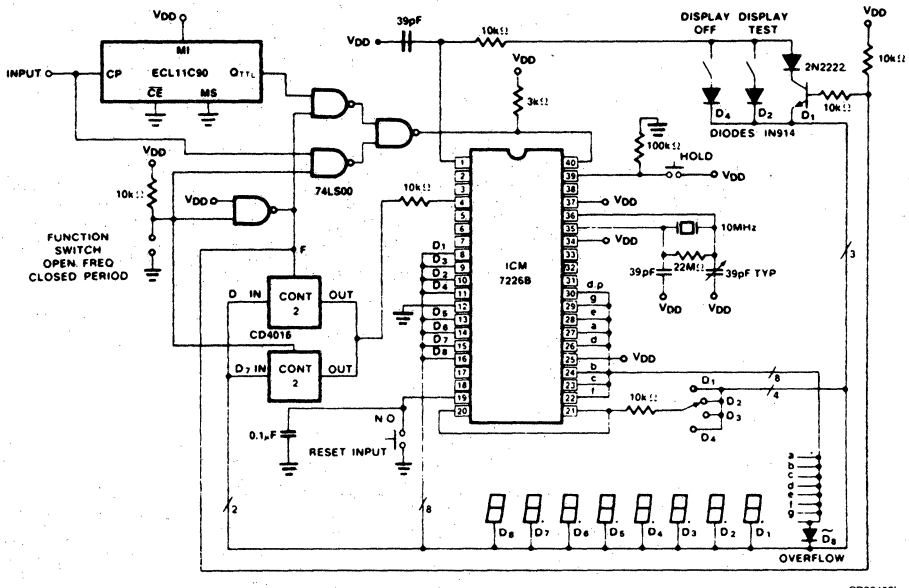
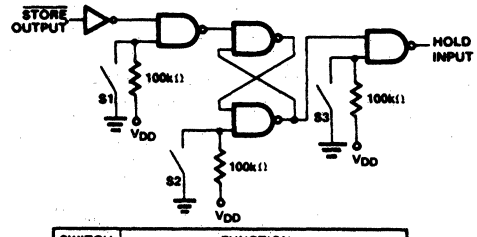


Figure 21: 100MHz Frequency, Period Counter

Figure 21 shows the use of a CD4016 analog multiplexer to multiplex the digital outputs back to the FUNCTION Input. Since the CD4016 is a digitally controlled analog transmission gate, no level shifting of the digit output is required. CD4051's or CD4052's could also be used to select the proper inputs for the multiplexed input on the ICM7226 from 2 or 3 bit digital inputs. These analog multiplexers may also be used in systems in which the mode of operation is controlled by a microprocessor rather than directly from front panel switches. TTL multiplexers such as the 74LS153 or 74LS251 may also be used, but some additional circuitry will be required to convert the digit output to TTL compatible logic levels.

The circuit shown in Figure 22 can be used in any of the circuit applications shown to implement a single measurement mode of operation. This circuit uses the $\overline{\text{STORE}}$ output to put the ICM7226 into a hold mode. The HOLD input can also be used to reduce the time between measurements. The circuit shown in Figure 23 puts a short pulse into the HOLD input a short time after STORE goes low. A new measurement will be initiated at the end of the pulse on the HOLD Input. This circuit reduces the time between measurements to less than 40ms from 200ms; use of the circuit shown in Figure 23 on the circuit shown in Figure 19 will reduce the time between measurements from 1600ms to 800ms.



SWITCH	FUNCTION
S1	OPEN = SINGLE MEAS MODE ENABLED
S2	CLOSED = INITIATE NEW MEASUREMENT
S3	CLOSED = HOLD INPUT

TC028811

SWITCH	FUNCTION
S1	OPEN-SINGLE MEAS MODE ENABLED
S2	CLOSED-INITIATE NEW MEASUREMENT
S3	CLOSED-HOLD INPUT

Figure 22: Single Measurement Circuit for Use With ICM7226

Note: All typical values have been guaranteed by characterization and are not tested.

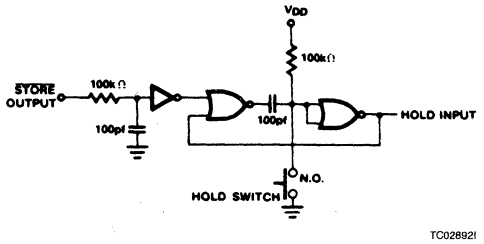


Figure 23: Circuit for Reducing Time Between Measurements

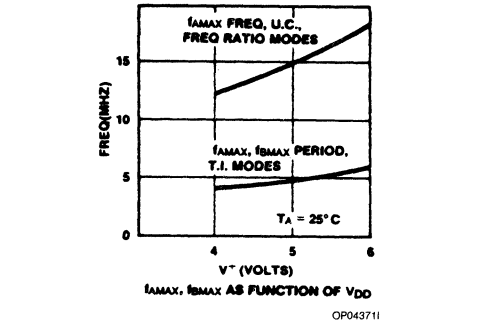


Figure 24: Typical Operating Characteristics

Figure 25 shows the ICM7226 being interfaced to LCD displays, by using its BCD outputs and 8 digit lines to drive two ICM7211 display drivers. The ICM7226 EV/Kit may easily be interfaced to 2 ICM7211 EV/Kits in this way. A similar arrangement can be used for driving vacuum fluorescent displays with the ICM7235.

OSCILLATOR CONSIDERATIONS

The oscillator is a high gain complementary FET inverter. An external resistor of 10MΩ or 22MΩ should be connected between the oscillator input and output to provide biasing. The oscillator is designed to work with a parallel resonant 10MHz quartz crystal with a load capacitance of 22pF and a series resistance of less than 35Ω. Among suitable crystals is the 10MHz CTS KNIGHTS ISI-002.

For a specific crystal and load capacitance, the required g_m can be calculated as follows:

$$g_m = \omega^2 \, C_{IN} \, C_{OUT} \, Rs \left(1 + \frac{C_O}{C_L}\right)^2$$

where $C_L = \left(\frac{C_{IN}C_{OUT}}{C_{IN} + C_{OUT}}\right)$

C_O = Crystal static capacitance
R_S = Crystal Series Resistance
Cin = Input Capacitance
Cout = Output Capacitance
$\omega = 2\pi f$

The required g_m should not exceed 50% of the g_m specified for the ICM7226 to insure reliable startup. The oscillator input and output pins each contribute about 4pF to C_{IN} and C_{OUT}. For maximum frequency stability, C_{IN} and C_{OUT} should be approximately twice the specified crystal load capacitance.

In cases where nondecade prescalers are used, it may be desirable to use a crystal which is neither 10MHz nor 1MHz. In this case both the multiplex rate and the time between measurements will be different. The multiplex rate is $f_{mux} = \frac{f_{osc}}{2 \times 10^4}$ for 10MHz mode and $f_{mux} = \frac{f_{osc}}{2 \times 10^3}$ for the 1MHz mode. The time between measurements is $\frac{2 \times 10^6}{f_{osc}}$ in the 10MHz mode and $\frac{2 \times 10^5}{f_{osc}}$ in the 1MHz mode. The buffered oscillator output should be used as an oscillator test point or to drive additional logic; this output will drive one low power Schottky TTL load. When the buffered oscillator output is used to drive CMOS or the external oscillator input, a 10kΩ resistor should be added from the buffered oscillator output to V_{DD}.

The crystal and oscillator components should be located as close to the chip as practical to minimize pickup from other signals. In particular, coupling from the BUFFfered OSCillator OUTput and EXTernal OSCillator INput to the OSCillator OUTput or OSCillator INput can cause undesirable shifts in oscillator frequency. To minimize this coupling, pins 34 and 37 should be connected to V_{DD} or V_{SS} and these two signals should be kept away from the oscillator circuit.

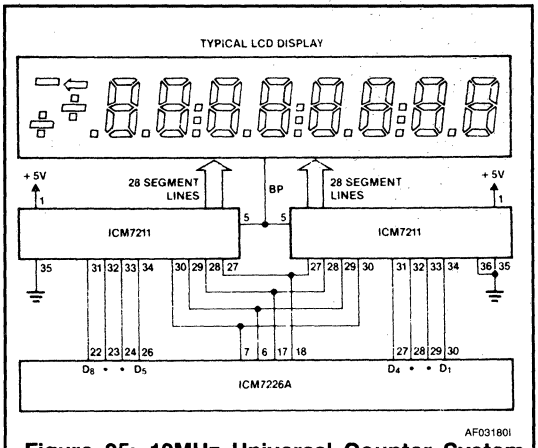


Figure 25: 10MHz Universal Counter System with LCD Display

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7236

4½-Digit Counter/Vacuum Fluorescent Display Driver

INTERSIL

GENERAL DESCRIPTION

The ICM7236 and ICM7236A devices are high-performance CMOS 4½-digit counters. They include 7-segment decoders, output latches, count inhibit, reset, and leading zero blanking circuitry, as well as twenty-nine high-voltage open drain P-channel transistor outputs suitable for driving non-multiplexed (static) vacuum fluorescent displays.

The ICM7236 is a decade counter, providing a maximum count of 19999, while the ICM7236A is intended for timing purposes, and provides a maximum count of 15959.

The counter section of the two devices in the ICM7236 family provides direct static counting from DC to 15MHz guaranteed (with a 5V ±10% supply) over the operating temperature range. At normal room temperatures, the device will typically count up to 25MHz. The COUNT input is provided with a Schmitt trigger for operation in noisy environments and allows correct counting with slowly changing inputs. These devices also provide count inhibit, store and reset circuitry which allow a direct interface to the ICM7207 devices. This results in a low cost, low power frequency counter with minimum component count.

These devices also incorporate features intended to simplify cascading in four-digit blocks. The $\overline{\text{CARRY}}$ output allows the counter to be cascaded, while the Leading Zero Blanking INput and OUTput allow correct leading zero blanking between four-decade blocks.

The ICM7236 and ICM7236A are packaged in a standard 40-pin dual-in-line plastic and CERDIP packages.

ORDERING INFORMATION

ORDER PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7236IJL	−40°C to +85°C	40-PIN CERDIP
ICM7236AIJL	−40°C to +85°C	40-PIN CERDIP
ICM7236IPL	−40°C to +85°C	40-PIN PLASTIC DIP
ICM7236AIPL	−40°C to +85°C	40-PIN PLASTIC DIP
ICM7236/D	−40°C to +85°C	DICE
ICM7236A/D	−40°C to +85°C	DICE
ICM7236EV/KIT		EVALUATION KIT

FEATURES

- **High Frequency Counting — Guaranteed 15MHz, Typically 25MHz at T_A −25°C**
- **Low Power Operation — Less Than 100μW Quiescent**
- **Direct 4½-Digit Seven-Segment Display Drive for Non-Multiplexed Vacuum Fluorescent Displays**
- **$\overline{\text{STORE}}$ and $\overline{\text{RESET}}$ Inputs Permit Operation As Frequency or Period Counter**
- **True $\overline{\text{COUNT INHIBIT}}$ Disables First Counter Stage**
- **$\overline{\text{CARRY}}$ Output for Cascading Four-Digit Blocks**
- **Schmitt-Trigger On COUNT Input Allows Operation in Noisy Environments or With Slowly Changing Inputs**
- **Leading Zero Blanking INput and OUTput for Correct Leading Zero Blanking With Cascaded Devices**

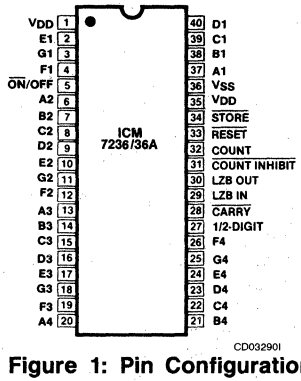


Figure 1: Pin Configuration

Note: All typical values have been guaranteed by characterization and are not tested.

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 0.5W @ +70°C
Supply Voltage ($V_{DD} - V_{SS}$) 6.5V
Display Voltage (Note 3) ..... V_{DD} -35V
Input Voltage ..... V_{SS} -0.3V to V_{DD} +0.3V

Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliabiity.

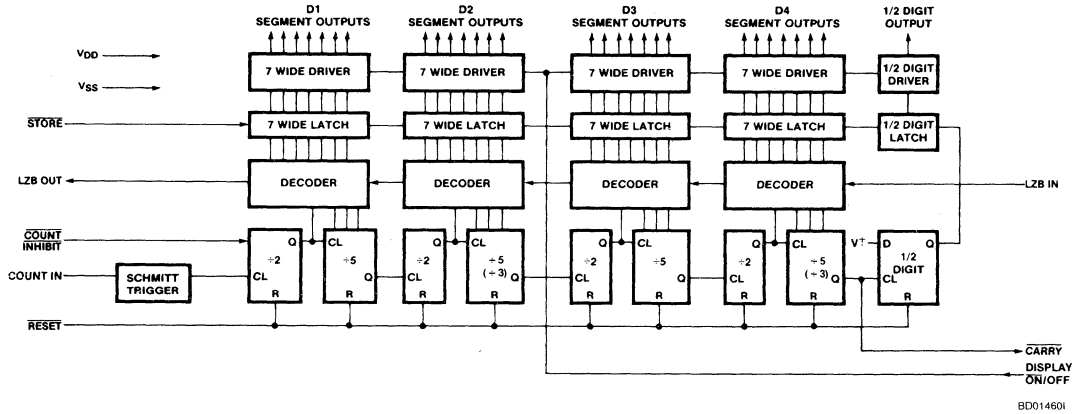


Figure 2: Functional Diagram

ELECTRICAL CHARACTERISTICS (All parameters measured with $V_{DD} = 5V$, $T_A = 25°C$, $V_{SS} = 0V$ unless otherwise indicated).

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SUPPLY}	Operating Supply Voltage Range ($V_{DD} - V_{SS}$)		3	5	6	V
I_{DD}	Operating Current	Test circuit, Display blank		10	50	µA
V_{DISP}	Display Voltage				30	V
I_{DLK}	Display Output Leakage	Output OFF, $V_{DISP} = V_{DD} - 30V$		0.1	10	µA
I_P	Input Pullup Currents	Pins 29, 31, 33, 34 $V_{IN} = V_{DD} - 3V$		10		µA
V_{IH}	Input High Voltage	Pins 29, 31, 33, 34	3			V
V_{IL}	Input Low Voltage	Pins 29, 31, 33, 34			2	V
V_{CT}	COUNT Input Threshold			2		V
V_{CH}	COUNT Input Hysteresis			0.5		V
I_{OH}	Output High Current	$\overline{CARRY}$ (Pin 28), LZB OUT (Pin 30) $V_{OUT} = V_{DD} - 3V$.	350	500		µA
I_{OL}	Output Low Current	$\overline{CARRY}$ (Pin 28), LZB OUT (Pin 30) $V_{OUT} = +3V$.	350	500		µA
f_{count}	Count Frequency	$4.5V < V_{DD} < 6V$	0	25	15	MHz
t_s, t_w	$\overline{STORE}$, $\overline{RESET}$ Minimum Pulse Width		3			µs

NOTES:
1. This limit refers to that of the package and will not occur during normal operation.
2. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than V_{DD} or less than ground may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7236/7236A be turned on first.
3. This limit refers to the display output terminals only.

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7236

OPERATING CHARACTERISTICS

INPUT	TERMINAL	VOLTAGE	FUNCTION
Leading Zero Blanking Input (LZB IN)	29	V_{DD} or Floating V_{SS}	Leading Zero Blanking Enabled Leading Zeroes Displayed
$\overline{\text{COUNT INHIBIT}}$	31	V_{DD} or Floating V_{SS}	Counter Enabled Counter Disabled
$\overline{\text{RESET}}$	33	V_{DD} or Floating V_{SS}	Inactive Counter Reset to 0000
$\overline{\text{STORE}}$	34	V_{DD} or Floating V_{SS}	Output Latches Not Updated Output Latches Updated
Display $\overline{\text{ON}}$/OFF	5	V_{DD} V_{SS}	Display Outputs Disabled Display Outputs Enabled

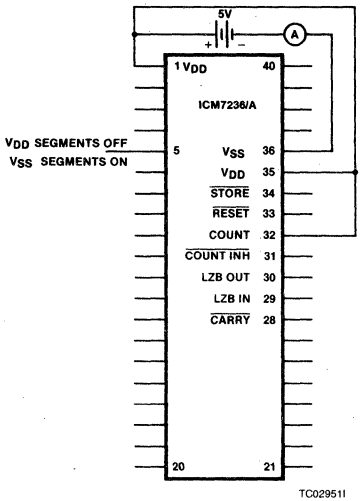
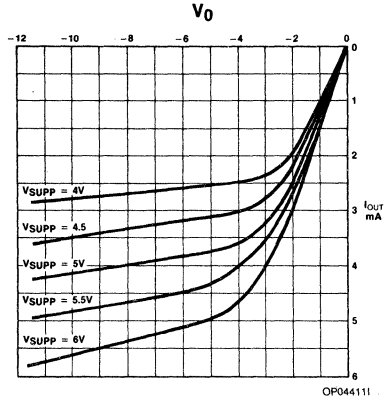


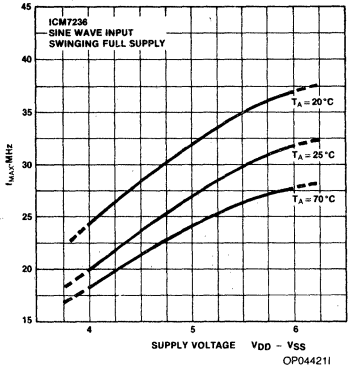
Figure 3: Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

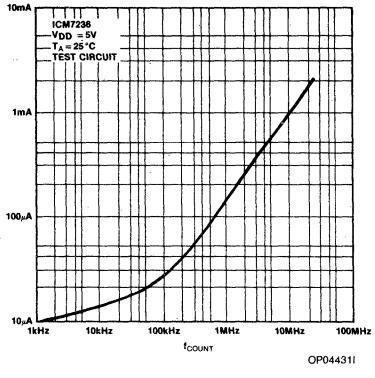
Output Characteristics



Maximum Count Frequency (Typical) as a Function of Supply Voltage



Supply Current as a Function of Count Frequency



Note: All typical values have been guaranteed by characterization and are not tested.

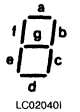
DESCRIPTION OF OPERATION

Both devices in the ICM7236 family provide twenty-nine outputs suitable for directly driving the anode terminals of 4½ digit seven-segment non-multiplexed (static) vacuum-fluorescent displays. Each display output is the drain of a high-voltage low-leakage P-channel transistor, capable of withstanding typically greater than −35 volts with respect to V_{DD}. The output characteristics are shown graphically under "Typical Characteristics."

These chips also provide a display $\overline{ON}$/OFF input which may be used to disable all the segment outputs and thus blank the display. This input may also be used to control the display brightness by varying the duty cycle of a signal at the input swinging between V_{DD} and V_{SS}.

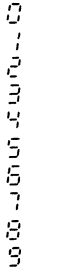
Note that these circuits have two terminals for V_{DD}; both of these pins should be connected to the power supply positive terminal. The double connection is necessary to minimize effects of bond wire resistance with the large total display currents possible.

These chips may also be used to directly drive non-multiplexed common-cathode LED displays, where each segment of the display is driven by one ICM7236 output, and the common cathode is connected to ground. With a 5V power supply and a 1.7V LED diode forward voltage drop, the current in an "ON" segment will be typically 3mA. This should provide sufficient brightness in displays up to about 0.3" character height.



LC02040I

Figure 4: Segment Assignment



(BLANK)

LC02050I

Figure 5: Display Font

COUNTER SECTION

The devices in the ICM7236 family implement a four-digit ripple-carry resettable counter, including a Schmitt trigger COUNT input and a $\overline{CARRY}$ output. Also included is an extra D-type flip-flop, clocked by the carry signal, which controls the half-digit segment driver. This can be used as either a true half-digit or as an overflow indicator. The counter will increment on the negative-going edge of the signal at the COUNT input, and the $\overline{CARRY}$ output will provide a negative-going edge following the count which increments the counter from 9999 (or 5959) to 10000. Once half-digit flip-flop has been clocked, it can only be reset (with the rest of the counter) by a negative level at the $\overline{RESET}$ terminal, pin 33. However, the four decades will continue to count in a normal fashion after the half-digit is set, and subsequent $\overline{CARRY}$ outputs will not be affected.

A negative level at the $\overline{COUNT\ INHIBIT}$ disables the first divide-by-two flip-flop in the counter chain without affecting its clock. This provides a true **count** inhibit which is not sensitive to the state of the COUNT input, and prevents false counts which can result from a normal logic gate forcing the state of the clock to prevent counting.

Each decade is fed directly into a four-to-seven line decoder which generates the seven-segment output code. Each decoder output corresponds to one-segment terminal of the device. The output data is latched at the driver. When the $\overline{STORE}$ pin is at a negative level, the latches are updated, and when the pin is left open or at a positive level, the latches hold their contents.

The decoders also include zero detect and blanking logic to provide leading zero blanking. When the Leading Zero Blanking INput is floating, or at a positive level, this circuitry is enabled and the device will blank leading zeroes. When the Leading Zero Blanking INput is at a negative level, or the half-digit is set, leading zero blanking is inhibited, and zeroes in the four digits will be displayed. The Leading Zero Blanking OUTput is provided to allow cascaded devices to blank leading zeroes correctly. This output will assume a positive level only when all four digits are blanked, and can only occur when the Leading Zero Blanking INput is at a positive level and the half-digit is not set.

For example, on an eight-decade counter with overflow using two ICM7236 devices, the Leading Zero Blanking OUTput of the high-order digit device would be connected to the Leading Zero Blanking INput of the low-order digit device. This will assure correct leading zero blanking for all eight digits.

The $\overline{STORE}$, $\overline{RESET}$, $\overline{COUNT\ INHIBIT}$, and Leading Zero Blanking INputs are provided with internal pullup devices, so that they may be left open when a positive level is desired. The $\overline{CARRY}$ and Leading Zero OUTputs are suitable for interfacing to CMOS logic in general, and are specifically designed to allow cascading of ICM7236 devices in four-digit blocks.

CONTROL INPUT DEFINITIONS

In this table, V_{DD} and V_{SS} are considered to be normal operating input logic levels. Actual input low and high levels are specified under Operating Characteristics. For lowest power consumption, input signals should swing over the full supply.

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7236

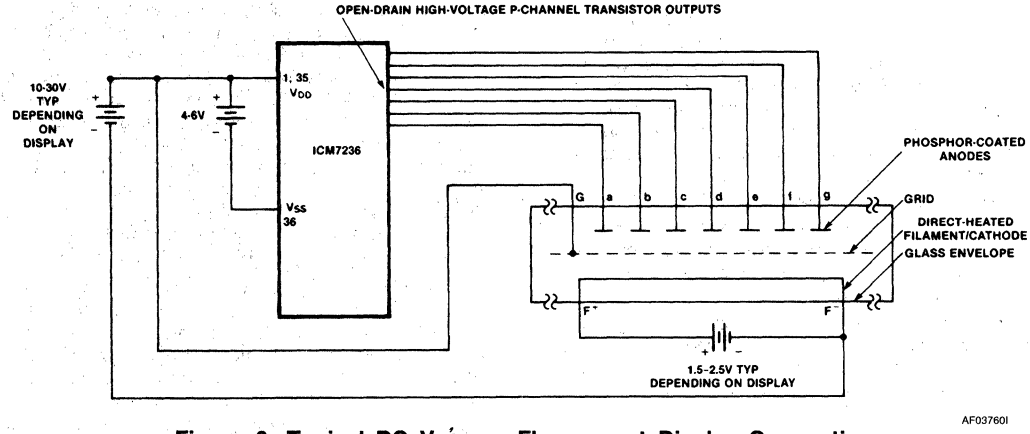


Figure 6: Typical DC Vacuum Fluorescent Display Connection

VACUUM FLUORESCENT DISPLAYS (4½-DIGIT):
N.E.C. Electronics, Inc.
Model FIP5F8S

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7240/ICM7250
ICM7260
Programmable Timer

GENERAL DESCRIPTION

The ICM7240/50/60 is a family of CMOS Timer/Counter circuits intended to replace Intersil's ICM8240/50/60 and the 2240 in most applications. Together with the ICM7555/56 (CMOS versions of the SE/NE 555/6), they provide a complete line of RC oscillators/timers/counters offering lower supply currents, wider supply voltage ranges, higher operating frequencies, lower component counts and a wider range of timing components. They are intended to simplify the selection of various time delays or frequency outputs from a fixed RC oscillator circuit.

Each device consists of a counter section, control circuitry, and an RC oscillator requiring an external resistor and capacitor. For counter/divider applications, the oscillator may be inhibited and an input clock applied to the TB terminal. The ICM7240 is intended for straight binary counting or timing, whereas the ICM7250 is optimized for decimal counting or timing. The ICM7260 is specifically designed for the time delays in seconds, minutes and hours. All three devices use open drain output transistors, thereby allowing wire AND-ing. Manual programming is easily accomplished by the use of standard thumbwheel switches or hardwired connections. The ICM7240/50/60 are packaged in 16 pin CERDIP packages.

Applications include programmable timing, long delay generation, cascadeable counters, programmable counters, low frequency oscillators, and sequence timing.

FEATURES

- **Replaces 8240/50/60, 2240 in Most Applications**
- **Timing From Microseconds to Days**
- **May Be Used As Fixed or Programmable Counter**
- **Programmable With Standard Thumbwheel Switches**
- **Select Output Count From**
  1_{RC} to 255_{RC} (ICM7240)
  1_{RC} to 99_{RC} (ICM7250)
  1_{RC} to 59_{RC} (ICM7260)
- **Monostable or Astable Operation**
- **Low Supply Current: 115μA @ 5 Volts**
- **Wide Supply Voltage Range: 2–16 Volts**
- **Cascadeable**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7240IJE	−25°C to +85°C	16 Lead CERDIP
ICM7250IJE	−25°C to +85°C	16 Lead CERDIP
ICM7260IJE	−25°C to +85°C	16 Lead CERDIP
ICM7240/D	—	DICE**
ICM7250/D	—	DICE**
ICM7260/D	—	DICE**

**Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.

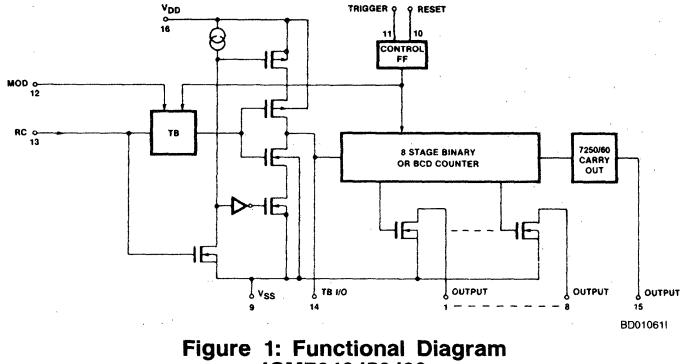


Figure 1: Functional Diagram ICM7240/50/60

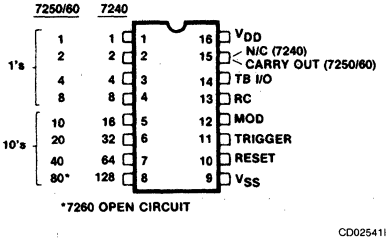


Figure 2: Pin Configuration (Outline dwg JE) ICM7240/7250/7260

203403-002

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7240/ICM7250/ICM7260

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD}–V_{SS}) 18V
Input Voltage[1]
Terminals 10,11,12,13,14..... V_{SS} −0.3V to V_{DD} + 0.3V
Maximum continuous output
current (each output)..... 50mA

Power Dissipation[2] 200mW
Operating Temperature Range .....−25°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) .....300°C

NOTES: 1. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7240/50/60 be turned on first.

2. Derate at −2mW/°C above 25°C.

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

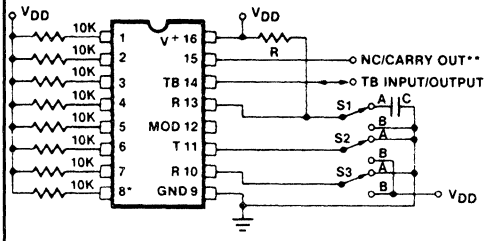
ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V, T_A = +25°C, R = 10kΩ, V_{DD} = 0V C = 0.1μF, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SUPPLY}	Guaranteed Supply Voltage (V_{DD}-V_{SS})		2		16	V
I_{DD}	Supply Current	Reset Operating, R = 10kΩ, C = 0.1μF Operating, R = 1MΩ, C = 0.1μF TB Inhibited, RC Connected to GND		125 300 120 125	 800 600	μA μA μA μA
	Timing Accuracy			5		%
Δf/ΔT	RC Oscillator Frequency Temperature Drift	(Exclusive of RC Drift)		250		ppm/°C
V_{OTB}	Time Base Output Voltage	I_{SOURCE} = 100μA I_{SINK} = 1.0mA		3.50 0.40		V
I_{TBLK}	Time Base Output Leakage Current	RC = Ground			25	μA
V_{MOD}	Mod Voltage Level	V_{DD} = 5V V_{DD} = 15V		3.5 11.0		V V
V_{TRIG}	Trigger Input Voltage	V_{DD} = 5V V_{DD} = 15V		1.6 3.5	2.0 4.5	V V
V_{RST}	Reset Input Voltage	V_{DD} = 5V V_{DD} = 15V		1.3 2.7	2.0 4.0	V V
f_t	Max Count Toggle Rate 7240	V_{DD} = 2V V_{DD} = 5V } Counter/Divider Mode V_{DD} = 15V 50% Duty Cycle Input with Peak to Peak Voltages Equal to V_{DD} and V_{SS}	2	1 6 13		MHz MHz MHz
f_t	Max Counter Toggle Rate 7250, 7260	V_{DD} = 5V (Counter/Divider Mode)	2	5		MHz
f_t	Max Count Toggle Rate 7240, 7250, 7260	Programmed Timer — Divider Mode			100	kHz
V_{SAT}	Output Saturation Voltage	All Outputs except TB Output V_{DD} = 5V, I_{OUT} = 3.2 mA		0.22	0.4	V
I_{OLK}	Output Leakage Current	V_{DD} = 5V, per Output			1	μA
C_t	MIN Timing Capacitor (Note 1)		10			pF
R_t	Timing Resistor Range (Note 1)	V_{DD} ≤ 5.5V V_{DD} ≤ 16V	1K 1K		12M 12M	Ω Ω

NOTE: 1. For Design only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.



TC02961I

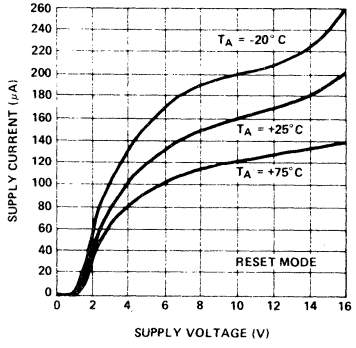
S1-A = RC RUN S2-A = INACTIVE S3-A = INACTIVE
B = T.B. INPUT RUN B = TRIGGER B = RESET

NOTE: S1-B INHIBITS THE TIMEBASE SECTION, ALLOWING TERMINAL 14 TO BECOME THE COUNTER INPUT.
** TERMINAL 15 IS CARRY OUTPUT FOR 7250/60 DEVICES.
* TERMINAL 8 IS OPEN CIRCUIT FOR 7260.

Figure 3: Test Circuit

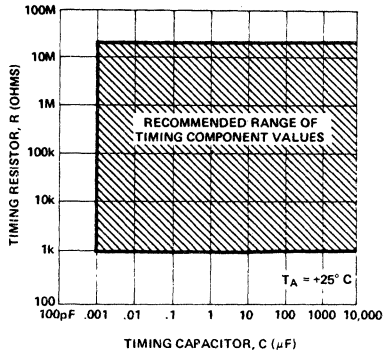
TYPICAL PERFORMANCE CHARACTERISTICS

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



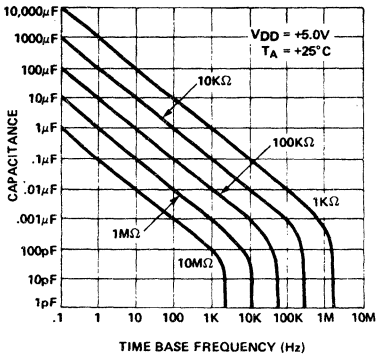
OP04440I

RECOMMENDED RANGE OF TIMING COMPONENT VALUES FOR ACCURATE TIMING



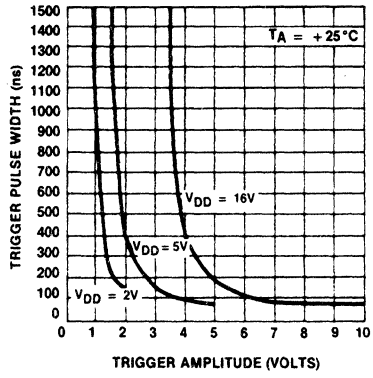
OP04471I

TIMEBASE FREE RUNNING FREQUENCY AS A FUNCTION OF R AND C



OP04451I

MINIMUM TRIGGER PULSE WIDTH AS A FUNCTION OF TRIGGER AMPLITUDE



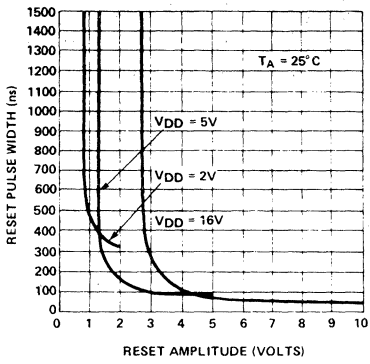
OP04581I

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7240/ICM7250/ICM7260

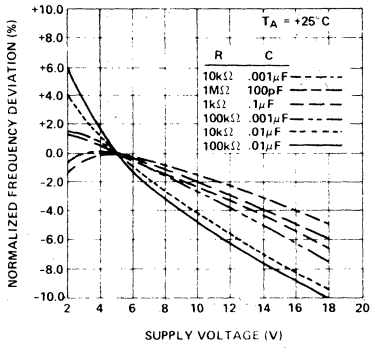
TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

MINIMUM RESET PULSE WIDTH AS A FUNCTION OF RESET AMPLITUDE



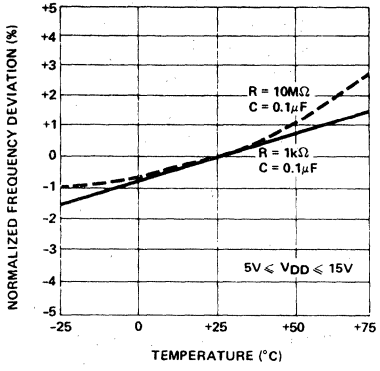
OP04461I

NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE



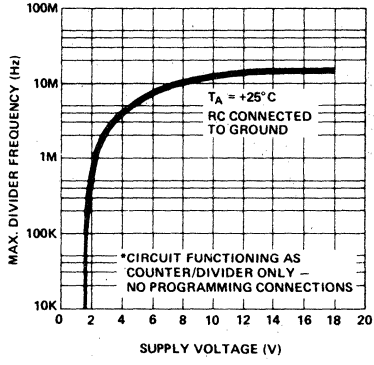
OP04490I

NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE



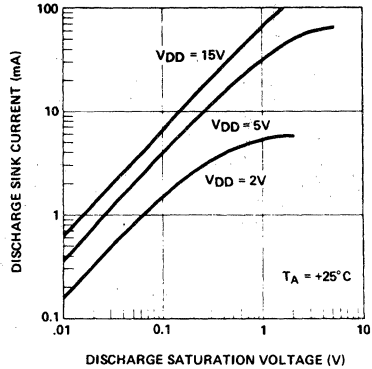
OP04501I

MAXIMUM DIVIDER FREQUENCY vs. SUPPLY VOLTAGE*



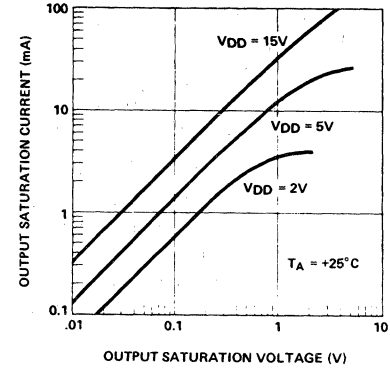
OP04520I

DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE



OP04531I

OUTPUT SATURATION CURRENT AS A FUNCTION OF OUTPUT SATURATION VOLTAGE



OP04511I

Note: All typical values have been guaranteed by characterization and are not tested.

CIRCUIT DESCRIPTION

The timing cycle is initiated by applying a positive-going trigger pulse to pin 11. This pulse enables the counter section, sets all counter outputs to the LOW or ON state, and starts the time base oscillator. Then, external C is charged through external R from 20% to 70% of V_{DD}–V_{SS}, generating a timing waveform with period t, equal to 1_{RC}. A short negative clock or time base pulse occurs during the capacitor discharge portion of the waveform. These clock pulses are counted by the binary counter of the 7240 or by two cascaded Binary Coded Decimal (BCD) Counters in the 7250/60. The timing cycle terminates when a positive level is applied to RESET. When the circuit is at reset, both the time base and the counter sections are disabled and all the counter outputs are at a HIGH or OFF state. The carry-out is also HIGH. Each of the three devices utilizes an identical timebase, control flip-flops, and basic counters, with the outputs consisting of open drain n-channel transistors. Only the ICM7250/60 have CARRY outputs.

In most timing applications, one or more of the counter outputs are connected back to RESET the circuit will start timing when a TRIGGER is applied and will automatically reset itself to complete the timing cycle when a programmed count is completed. If none of the counter outputs are connected back to the RESET (switch S_1 open), the circuit operates in its astable, or free-running mode, after initial triggering.

DESCRIPTION OF PIN FUNCTIONS

COUNTER OUTPUTS (PINS 1 THROUGH 8)

Each binary counter output is a buffered "open-drain" type. At reset condition, all the counter outputs are at a high, or non-conducting state. After a trigger input or when using the internal timebase, the outputs change state (see timing diagram, Figure 4). If an external clock input is used, the trigger input must overlap at least the first falling edge of the clock. The counter outputs can be used individually, or can be connected together in a wired-AND configuration, as described in the Programming section.

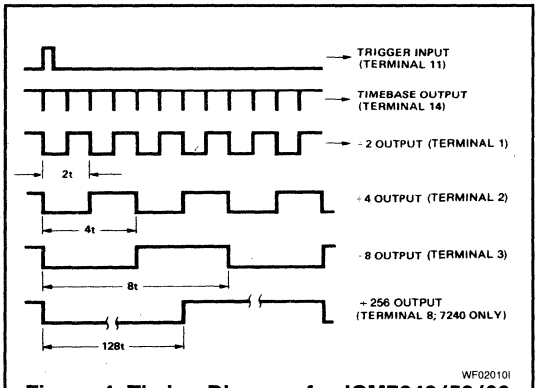


Figure 4: Timing Diagram for ICM7240/50/60

V_{SS} (PIN 9)

This is the return or most negative supply pin. It should have a very low impedance as the capacitor discharge and other switched currents could create transients.

RESET AND TRIGGER INPUTS (PINS 10 AND 11)

The circuits are reset or triggered by a positive level applied to pins 10 and 11, and once triggered they ignore additional trigger inputs until either the timing cycle is completed or a reset signal is applied. If both reset and trigger are applied simultaneously trigger overrides reset. Minimum input pulse widths are shown in the typical performance characteristics. Note that all devices feature power ON reset.

MODULATION AND SYNC INPUT (PIN 12)

The period, t, of the time base oscillator can be modulated by applying a DC voltage to this terminal. The time base oscillator can be synchronized to an external clock by applying a sync pulse to pin 12.

TIMEBASE INPUT/OUTPUT PIN (PIN 14)

While this pin can be used as either a time base input or output terminal, it should only be used as an input if the RC pin is connected to V_{SS}.

If the counter is to be externally driven, care should be taken to ensure that fall times are fast (see Operating Limits section).

Under no conditions is a 300pF capacitor on this terminal useful and should be removed if a 7240/50/60 is used to replace an 8240/50/60 or 2240.

CARRY OUTPUT (PIN 15, ICM7250/60 ONLY)

This pin will go HI for the last 10 counts of a 59 or 99 count, and can be used to drive another 7250 or 7260 counter stage while still using all the counter outputs of the first. Thus, by cascading several 7250's a large BCD countdown can be achieved.

The basic timing diagrams for the ICM7240/50/60 are shown in Figure 4. Assuming that the device is in the RESET mode, which occurs on powerup or after a positive level on the RESET terminal (if TRIGGER is low), a positive level on the trigger input signal will initiate normal operation. The discharge transistor turns on, discharging the timing capacitor C, and all the flip-flops in the counter chain change states.

Note that for straight binary counting the outputs are symmetrical; that is, a 50% duty cycle HI-LO. This is not the case when using BCD counting. (See Figure 6.)

PROGRAMMING CAPABILITY

The counter outputs, pins 1 through 8, are open-drain N-channel FETs, and can be shorted together to a common pull-up resistor to form a "wired-AND" connection. The combined output will be LOW as long as **any one** of the outputs is low. Each output is capable of sinking ≈5mA. In this manner, the time delays associated with each counter output can be summed by simply shorting them together to a common output. For example, if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle (monostable mode) t_o would be 32t for a 7240 and 20t for a 7250/60. Similarly, if pins, 1, 5, and 6 were shorted to the output bus, the total time delay would be $t_o = (1 + 16 + 32)t$ for the 7240 or $(1 + 10 + 20)t$ for the 7250/60. Thus, by selecting the number of counter terminals connected to the output bus, the timing cycle can be programmed from:

$1t \leq t_o \leq 255t$ (7240)

$1t \leq t_o \leq 99t$ (7250)

$1t \leq t_o \leq 59t$ (7260)

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7240/ICM7250/ICM7260

Note that for the 7250 and 7260, invalid count states (BCD values ≥ 10) will not be recognized and the counter will not stop.

The 7240/50/60 can be configured to initiate a controlled timing cycle upon power up, and also reset internally; see Figure 5. Applications for this could include lawn watering sprinkler timing, pump operation, etc.

BINARY OR DECIMAL PATTERN GENERATION

In astable operation, as shown in Figure 5, the output of the 7240/50 appears as a complex pulse pattern. The waveform of the output pulse train can be determined directly from the timing diagram of Figure 4, which shows the phase relations between the counter outputs. Figure 6 shows some of these complex pulse patterns. The pulse pattern repeats itself at a rate equal to the period of the *highest* counter bit connected to the common output bus. The minimum pulse width contained in the pulse train is determined by the *lowest* counter bit connected to the output.

THUMBWHEEL SWITCHES

While the ICM7240 is frequently hard wired for a particular function, the ICM7250 and ICM7260 can easily be programmed using thumbwheel switches. Standard BCD thumbwheel switches have one common and four inputs (1,2,4 and 8) which are connected according to the binary equivalent to the digits 0 through 9.

For a single ICM7250 two such switches would select a time of 1_{RC} to 99_{RC}. Cascading two ICM7250's (using the carry out gate) would expand selection to 9999_{RC}. For a ICM7260, there are standard BCD thumbwheel switches for the 0 through 5 digit (twelve position 0 to 5 repeated).

NOTES ON THE COUNTER SECTION

Used as a straight binary counter (ICM7240), as a ÷100 (ICM7250), or ÷60 (ICM7260) all devices are significantly faster than their bipolar equivalents. However, when using these devices as *programmable* counters the maximum frequency of operation is reduced by more than an order of magnitude. For any division ratio other than 256 (ICM7240), 100 (ICM7250), or 60 (ICM7260) the maximum input frequency must be limited to approximately 100kHz or less (with V_{DD} equal to +5 volts). The reason for this is two-fold:

a. Since Ripple counters are used, there is a propagation delay between each individual ÷2 counter (8 counters for the ICM7240/50 and 7 for the ICM7260). Outputs from the individual ÷2 counters are AND'ed together to provide the output signal and the RESET/TRIGGER signal.

b. There must be a delay of the positive going output to RESET, (pin 10) and TRIGGER (pin 11). The RESET signal must therefore be generated first, and from this signal another signal is obtained through a delay network. The TRIGGER overrides RESET.

The delay between TRIGGER and RESET is generated by the signal RC network consisting of the 56kΩ resistor and the 330pF capacitor.

The delay caused by the counter ripple delays can be as long as 2μs (5 volt supply), and the delay between RESET and TRIGGER should be at least 2μs. The sum of these two delays cannot be greater than one-half of the input clock period for reliable operation. See Figure 7 and 8.

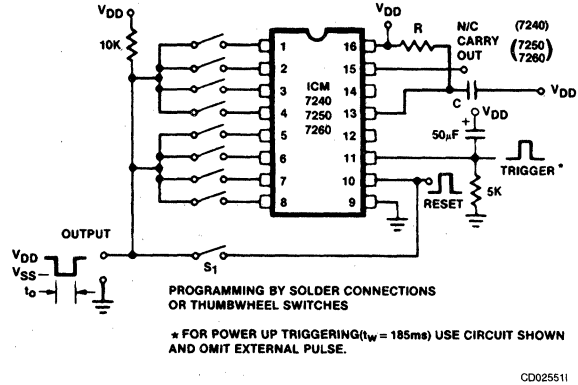


Figure 5: Generalized Circuit for Timing Applications (Switch S_1 open for astable operation, closed for monostable operation)

Note: All typical values have been guaranteed by characterization and are not tested.

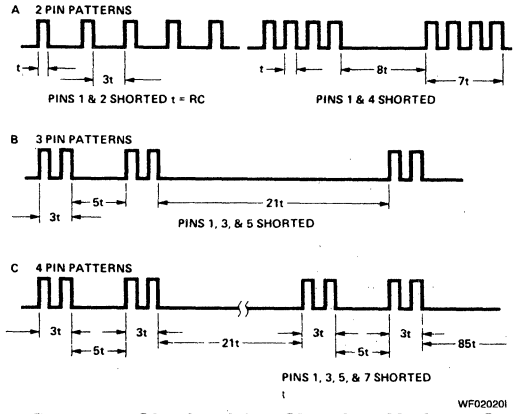


Figure 6: Pulse Patterns Obtained by Shorting Various Counter Outputs

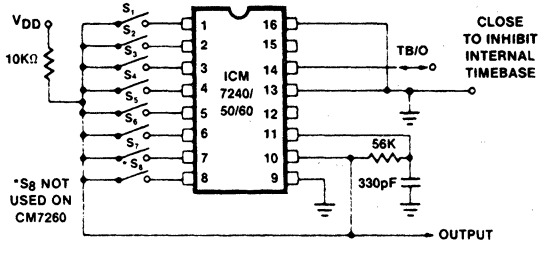


Figure 7: Programming the Counter Section of the ICM7240/50/60

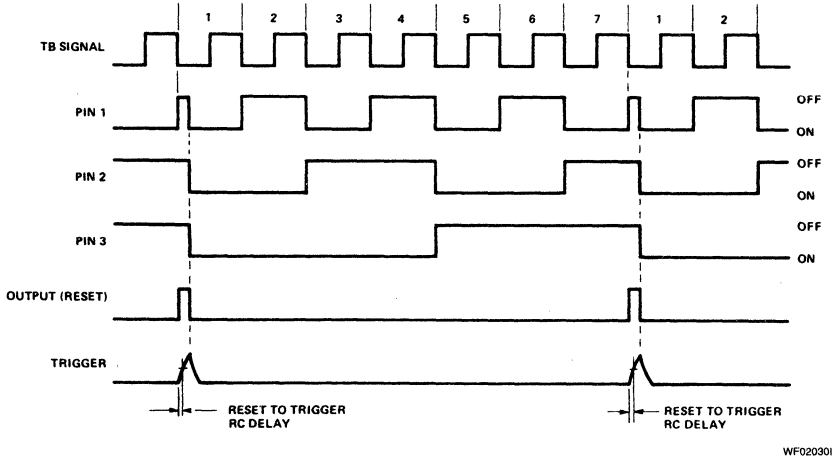


Figure 8: Waveforms for Programming the Counter Section

7

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7240/ICM7250/ICM7260

APPLICATIONS

GENERAL CONSIDERATIONS

Shorting the RC terminal or output terminals to V_{DD} may exceed dissipation ratings and/or maximum DC current limits (especially at high supply voltages).

There is a limit of 50pF maximum loading on the TB I/O terminal if the timebase is being used to drive the counter section. If higher value loading is used, the counter sections may miscount.

For greatest accuracy, use timing component values shown in the graph under Typical Performance Characteristics. For highest frequency operation it will be desirable to use very low values for the capacitor; accuracy will decrease for oscillator frequencies in excess of 200kHz.

When driving the counter section from an external clock, the optimum drive waveform is a square wave with an amplitude equal to supply voltage. If the clock is a very slow ramp triangular, sine wave, etc., it will be necessary to "square up" the waveform (rise/fall time $\leq 1\mu s$); this can be done by using two CMOS inverters in series, operating from the same supply voltage as the ICM 7240/50/60.

By cascading devices, use of low cost CMOS AND/OR gates and appropriate RC delays between stages, numerous sequential control variations can be obtained. Typical applications include injection molding machine controllers, phonograph record production machines, automatic sequencers (no metal contacts or moving parts), milling machine controllers, process timers, automatic lubrication systems, etc.

By selection of R and C, a wide variety of sequence timing can be realized. A typical flow chart for a machine tool controller could be as follows:

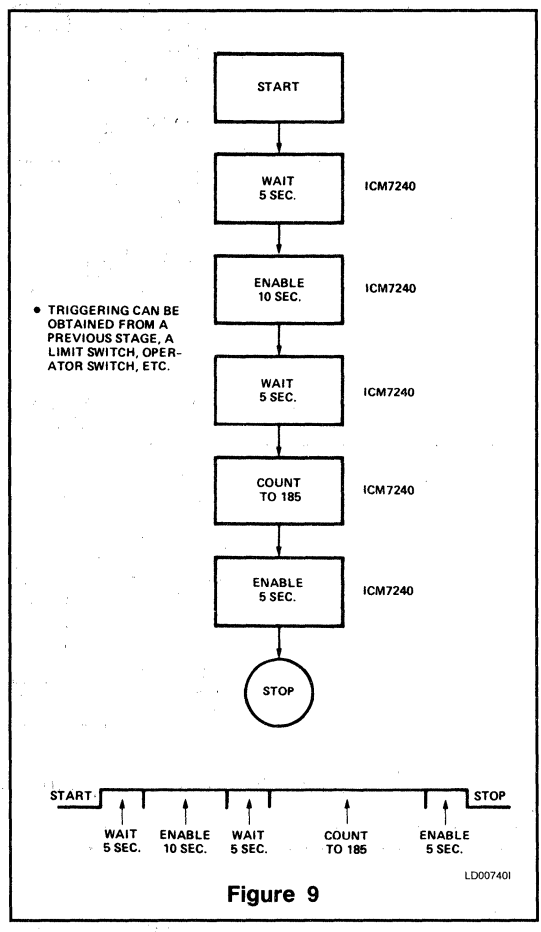


Figure 9

Note: All typical values have been guaranteed by characterization and are not tested.

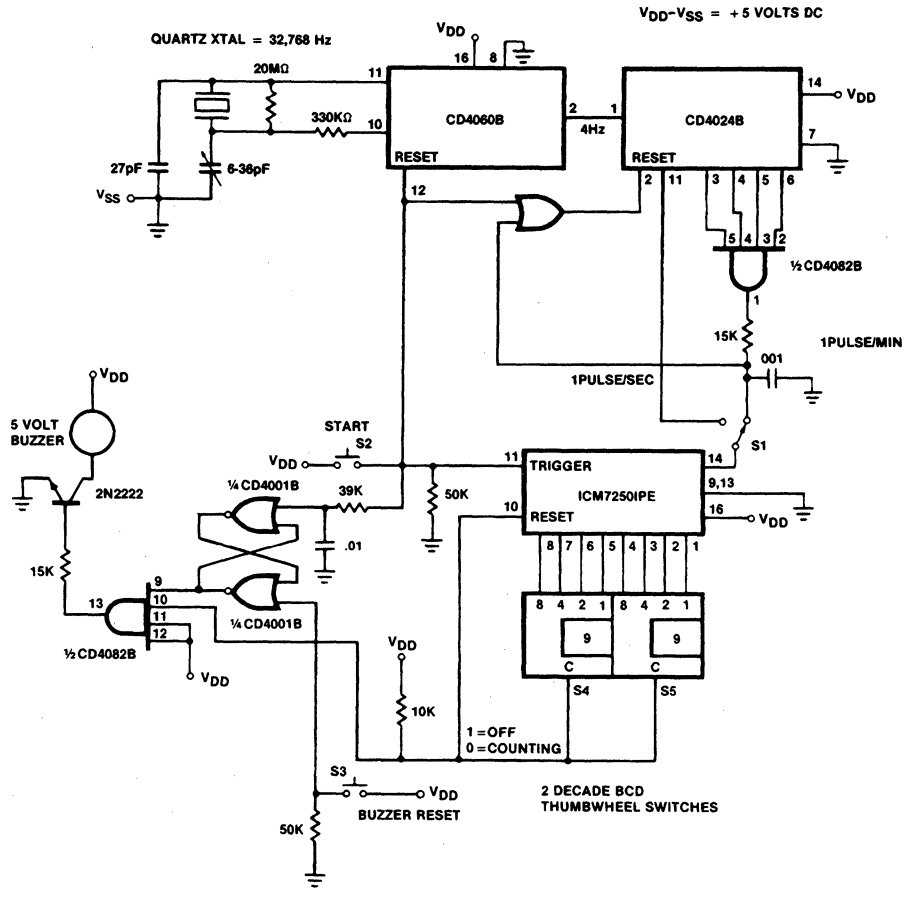


Figure 10

CMOS PRECISION PROGRAMMABLE 0–99 SECONDS/MINUTES LABORATORY TIMER

The ICM7250 is well suited as a laboratory timer to alert personnel of the expiration of a preselected interval of time.

When connected as shown in Figure 10, the timer can accurately measure preselected time intervals of 0–99 seconds or 0–99 minutes. A 5 volt buzzer alerts the operator when the preselected time interval is over.

The circuit operates as follows:

The time base is first selected with S1 (seconds or minutes), then units 0–99 are selected on the two thumbwheel switches S4 and S5. Finally, switch S2 is depressed to start the timer. Simultaneously the quartz crystal controlled divider circuits are reset, the ICM7250 is triggered and counting begins. The ICM7250 counts until the preprogrammed value is reached, whereupon it is reset, pin 10 of the CD4082B is enabled and the buzzer is turned on. Pressing S3 turns the buzzer off.

Note: All typical values have been guaranteed by characterization and are not tested.

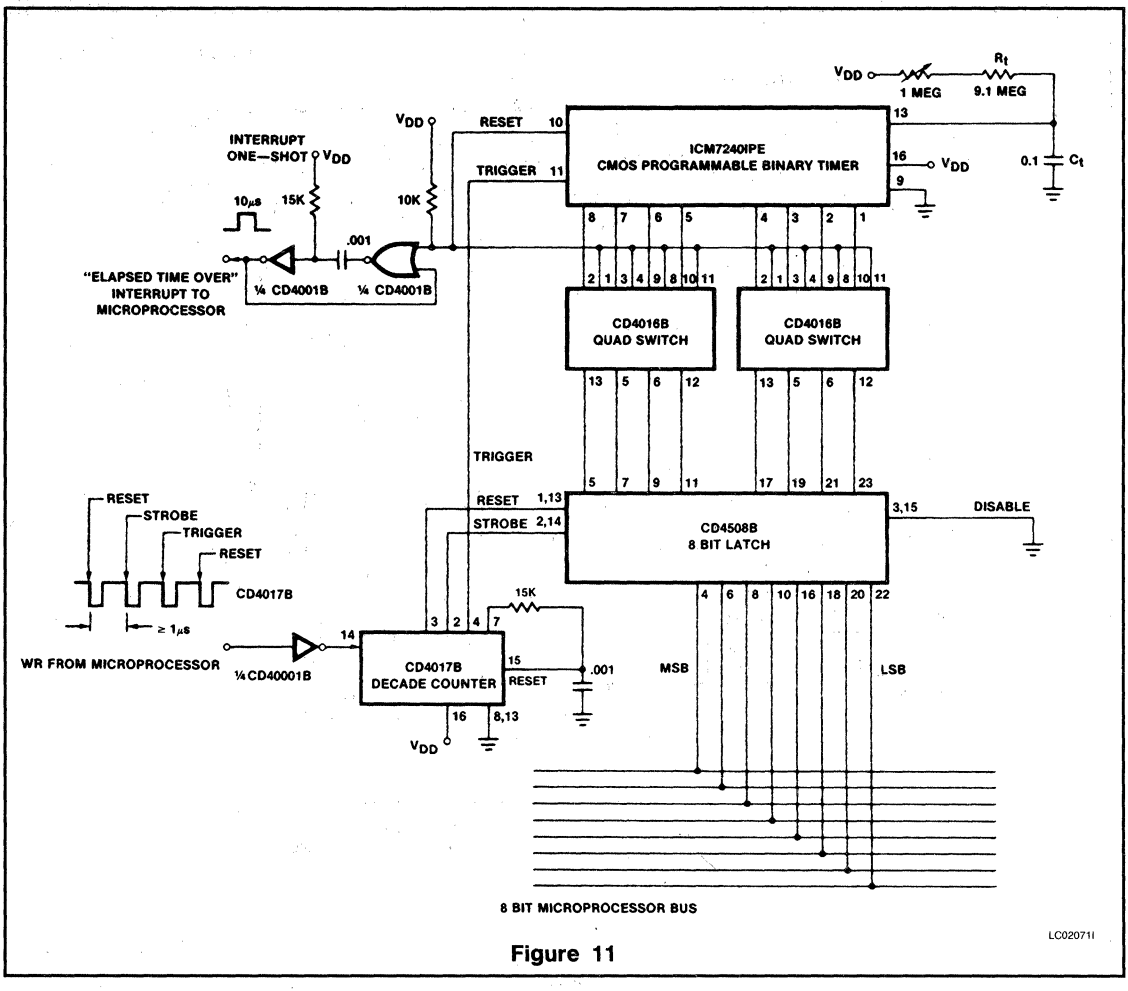


Figure 11

LOW POWER MICROPROCESSOR PROGRAMMABLE INTERVAL TIMER

The ICM7240 CMOS programmable binary timer can be configured as a low cost microprocessor controlled interval timer with the addition of a few inexpensive CD4000 series devices.

With the devices connected as shown in Figure 11, the sequence of operation is as follows:

The microprocessor sends out an 8 bit binary code on its 8 bit I/O bus (the binary value needed to program the ICM7240), followed by four $\overline{\text{WRITE}}$ pulses into the CD4017B decade counter. The first pulse resets the 8 bit latch, the second strobes the binary value into the 8 bit latch, the third triggers the ICM7240 to begin its timing cycle and the fourth resets the decade counter.

The ICM7240 then counts the interval of time determined by the R-C value on pin 13, and the programmed binary count on pins 1 through 8. At the end of the programmed time interval, the interrupt one-shot is triggered, informing the microprocessor that the programmed time interval is over.

With a resistor of approximately 10MΩ and capacitor of 0.1μF, the time base of the ICM7240 is one second. Thus, a time of 1–255 seconds can be programmed by the microprocessor, and by varying R or C, longer or shorter time bases can be selected.

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7241
Timebase Generator

GENERAL DESCRIPTION

The ICM7241 is a fully integrated oscillator, 2 divider and output driver which efficiency converts 4.194304MHz to 32.768kHz using a minimum of power. Only three external components are necessary for complete oscillator operation; a 4.194304MHz crystal, a fixed input capacitor, and an output trimmer capacitor. The output has a low enough impedance to satisfy most drive requirements.

FEATURES

- **Single Battery Operation (1.2 – 1.8V)**
- **Low Power Consumption — Typ. 40μA @ 1.5V**
- **Oscillator Biasing Resistor Included On-Chip**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7241IPA	–20°C to +70°C	8-Lead Plastic

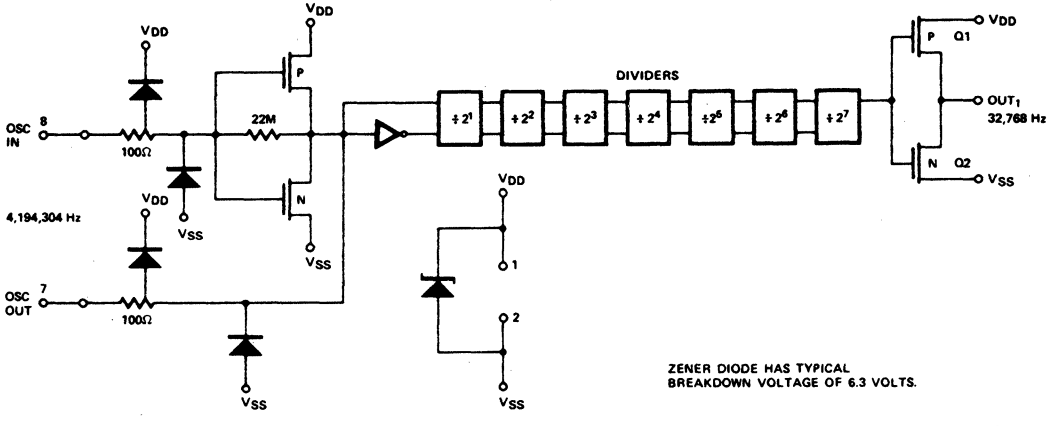


Figure 1: Functional Diagram

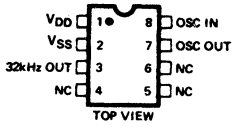


Figure 2: Pin Configuration (Outline dwg PA)

PIN 1 IS DESIGNATED BY EITHER A DOT OR A NOTCH.

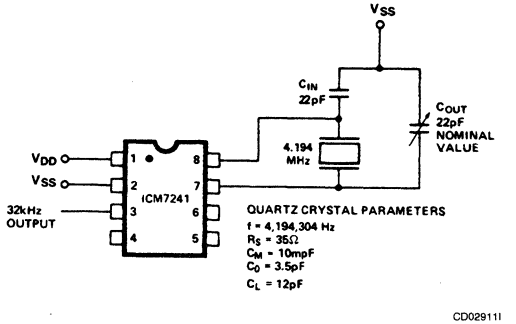


Figure 3: Typical Connection

–002

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7241

ABSOLUTE MAXIMUM RATINGS

Power Dissipation Output Short Circuit[2] 300mW
Supply Voltage (V_{DD}–V_{SS}) 3V
Output Voltage[1] ..... V_{SS}–0.3V to V_{DD}+0.3V
Input Voltage[1] ..... V_{SS}–0.3V to V_{DD}+0.3V

Storage Temperature ..... –30°C to +125°C
Operating Temperature ..... –20°C to 70°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTES:

1. All terminals may exceed the supply voltage (2.0V max) by ±0.3 volt provided that the currents in these terminals are limited to 2mA each.
2. This value of power dissipation refers to that of the package and will not be obtained under normal operating conditions.

ELECTRICAL CHARACTERISTICS

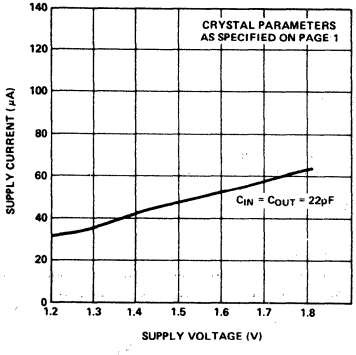
(V_{SS} = 1.5V, V_{SS} = 0V, f_{OSC} = 4,194,304Hz, T_A = 25°C, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply Current			40	70	µA
V_{SUPPLY}	Guaranteed Operating Voltage Range	–20°C ≤ to ≤ 70°C	1.2		1.8	V
R_{SAT}	P-Ch Output Saturation Resistance	I_{OUT} = .5mA		680	2	kΩ
R_{SAT}	N-Ch Output Saturation Resistance	I_{OUT} = .5mA		240	1	kΩ
f_{STAB}	Oscillator Stability	1.2V < V_{DD} < 1.6V C_{IN} = C_{OUT} = 15pF		1		ppm
t_{START}	Oscillator Start-Up Time	V_{DD} = 1.2V			1.0	s

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

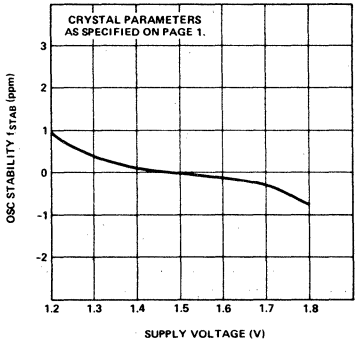
TYPICAL PERFORMANCE CHARACTERISTICS

SUPPLY CURRENT vs. SUPPLY VOLTAGE



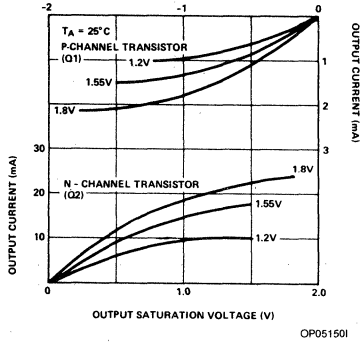
OP05130I

OSCILLATOR STABILITY vs. SUPPLY VOLTAGE



OP05140I

CURRENT (SOURCE) vs. OUTPUT SATURATION VOLTAGE



OP05150I

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7242
Long-Range Fixed Timer

GENERAL DESCRIPTION

The ICM7242 is a CMOS timer/counter circuit consisting of an RC oscillator followed by an 8-bit binary counter. It will replace the 2242 in most applications, with a significant reduction in the number of external components.

Three outputs are provided. They are the oscillator output, and buffered outputs from the first and eighth counters.

The ICM7242 is packaged in an 8-pin CERDIP.

FEATURES

- **Replaces The 2242 in Most Applications**
- **Timing From Microseconds to Days**
- **Cascadeable**
- **Monostable or Astable Operation**
- **Wide Supply Voltage Range: 2–16 volts**
- **Low Supply Current: 115μA @ 5 volts**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7242D	—	DICE**
ICM7242IPA	−25°C to +85°C	8 pin MINI-DIP
ICM7242IJA	−25°C to +85°C	8 pin CERDIP
ICM7242CBA	0°C to +70°C	8 pin S.O.I.C.

**Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.

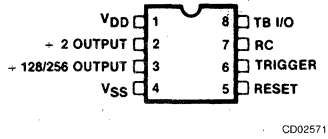


Figure 1: Pin Configuration (Outline Drawing JA, PA)

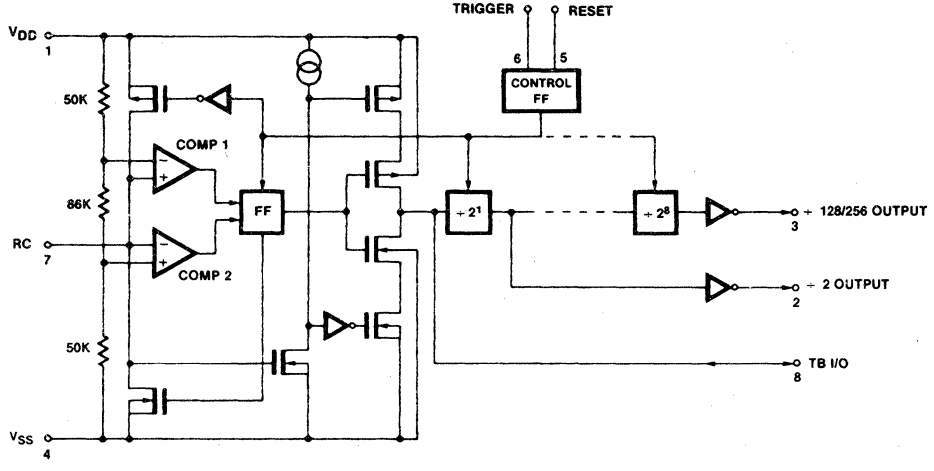


Figure 2: Functional Diagram

7

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7242

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD} to V_{SS}) 18V
Input Voltage[1]
Terminals (Pins 5, 6, 7, 8) (V_{SS} −0.3V) to (V_{DD} +0.3V)
Maximum continuous output current
(each output) 50mA

Power Dissipation[2] 200mW
Operating Temperature Range ..... −25°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTES: 1. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same supply be applied to the device before its supply is established and, that in multiple supply systems, the supply to the ICM7242 be turned on first.

2. Derate at −2mW/°C above 25°C.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

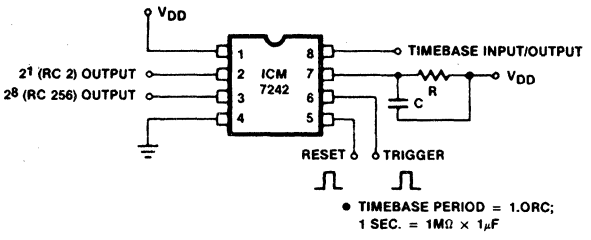
ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V, T_A = +25°C, R = 10kΩ, C = 0.1μF, V_{SS} = 0V unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Guaranteed Supply Voltage		2		16	V
I_{DD}	Supply Current	Reset Operating, R = 10kΩ, C = 0.1μF Operating, R = 1MΩ, C = 0.1μF TB Inhibited, RC Connected to V_{SS}		125 340 220 225	 800 600	μA μA μA μA
	Timing Accuracy			5		%
Δf/ΔT	RC Oscillator Frequency Temperature Drift	Independent of RC Components		250		ppm/°C
V_{OTB}	Time Base Output Voltage	I_{SOURCE} = 100μA I_{SINK} = 1.0mA		3.5 0.40		V V
I_{TBLK}	Time Base Output Leakage Current	RC = Ground			25	μA
V_{TRIG}	Trigger Input Voltage	V_{DD} = 5V V_{DD} = 15V		1.6 3.5	2.0 4.5	V V
V_{RST}	Reset Input Voltage	V_{DD} = 5V V_{DD} = 15V		1.3 2.7	2.0 4.0	V V
I_{TRIG}, I_{RST}	Trigger/Reset Input Current			10		μA
f_t	Max Count Toggle Rate	V_{DD} = 2V V_{DD} = 5V V_{DD} = 15V Counter/Divider Mode 50% Duty Cycle Input with Peak to Peak Voltages Equal to V_{DD} and V_{SS}	2	1 6 13		MHz MHz MHz
V_{SAT}	Output Saturation Voltage	All Outputs except TB Output V_{DD} = 5V, I_{OUT} = 3.2mA		0.22	0.4	V
I_{SOURCE}	Output Sourcing Current 7242	V_{DD} = 5V Terminals 2 & 3, V_{OUT} = 1V		300		μA
C_t	MIN Timing Capacitor (Note 1)		10			pF
R_t	Timing Resistor Range (Note 1)	V_{DD} = 2–16V	1K		22M	Ω

NOTE: 1. For Design only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

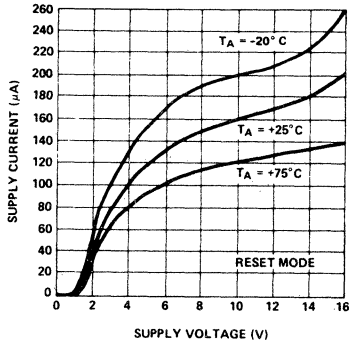


NOTE: OUTPUTS $\div 2^1$ AND $\div 2^8$ ARE INVERTERS AND HAVE ACTIVE PULLUPS.

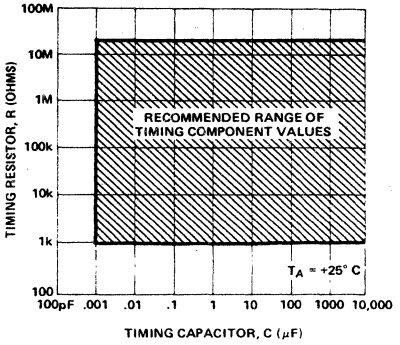
Figure 3: Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

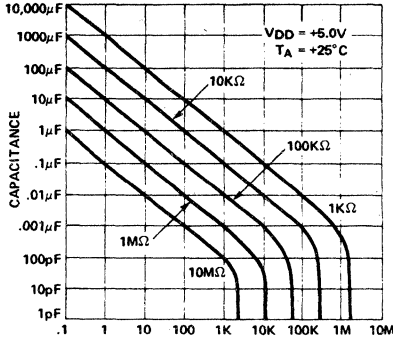
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



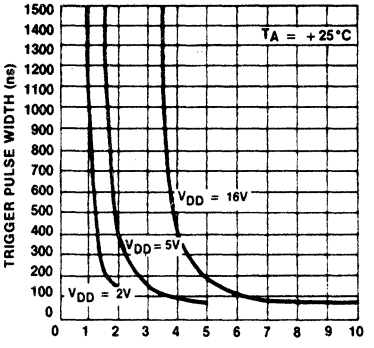
RECOMMENDED RANGE OF TIMING COMPONENT VALUES FOR ACCURATE TIMING



TIMEBASE FREE RUNNING FREQUENCY AS A FUNCTION OF R AND C



MINIMUM TRIGGER PULSE WIDTH AS A FUNCTION OF TRIGGER AMPLITUDE

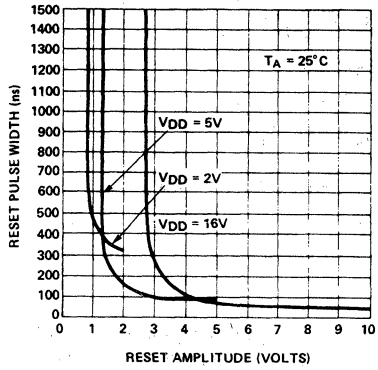


Note: All typical values have been guaranteed by characterization and are not tested.

ICM7242

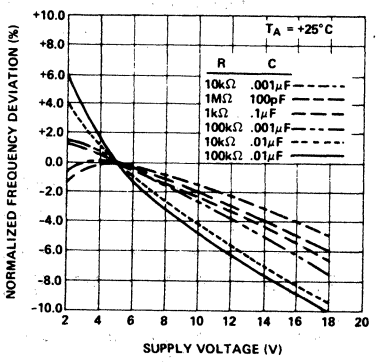
TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

MINIMUM RESET PULSE WIDTH AS A FUNCTION OF RESET AMPLITUDE



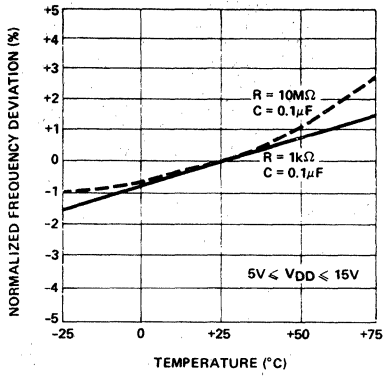
OP04561I

NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE



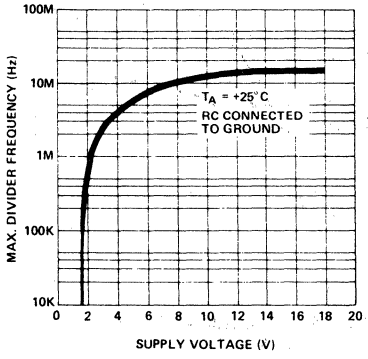
OP04590I

NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE



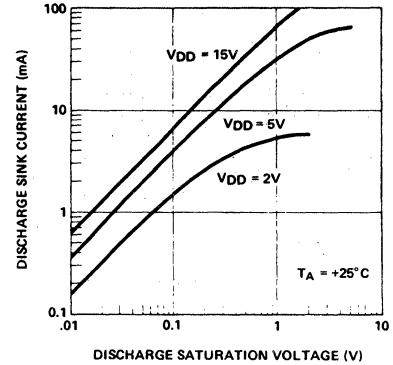
OP04601I

MAXIMUM DIVIDER FREQUENCY vs. SUPPLY VOLTAGE



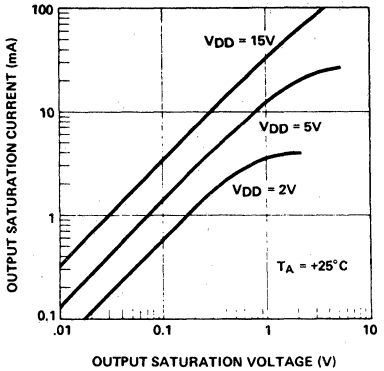
OP04620I

DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE



OP04611I

OUTPUT SATURATION CURRENT AS A FUNCTION OF OUTPUT SATURATION VOLTAGE



OP04631I

Note: All typical values have been guaranteed by characterization and are not tested.

OPERATING CONSIDERATIONS

Shorting the RC terminal or output terminals to V_{DD} may exceed dissipation ratings and/or maximum DC current limits (especially at high supply voltages).

There is a limitation of 50pF maximum loading on the TB I/O terminal if the timebase is being used to drive the counter section. If higher value loading is used, the counter sections may miscount.

For greatest accuracy, use timing component values shown in the graph under typical performance characteristics. For highest frequency operation it will be desirable to use very low values for the capacitor; accuracy will decrease for oscillator frequencies in excess of 200KHz.

When driving the counter section from an external clock, the optimum drive waveform is a square wave with an amplitude equal to supply voltage. If the clock is a very slow ramp triangular, sine wave, etc., it will be necessary to "square up" the waveform; this can be done by using two CMOS inverters in series, operating from the same supply voltage as the ICM7242.

The ICM7242 is a non-programmable timer whose principal applications will be very low frequency oscillators and long range timers; it makes a much better low frequency oscillator/timer than a 555 or ICM7555, because of the on-chip 8-bit counter. Also, devices can be cascaded to produce extremely low frequency signals.

Because outputs will not be AND'd, output inverters are used instead of open drain N-channel transistors, and the external resistors used for the 2242 will not be required for the ICM7242. The ICM7242 will, however, plug into a socket for the 2242 having these resistors.

The timing diagram for the ICM7242 is shown in Figure 4. Assuming that the device is in the RESET mode, which occurs on powerup or after a positive signal on the RESET terminal (if TRIGGER is low), a positive edge on the trigger input signal will initiate normal operation. The discharge transistor turns on, discharging the timing capacitor C, and all the flip-flops in the counter chain change states. Thus, the outputs on terminals 2 and 3 change from high to low states. After 128 negative timebase edges, the $\div 2^8$ output returns to the high state.

To use the 8-bit counter without the timebase, terminal 7 (RC) should be connected to ground and the outputs taken from terminals 2 and 3.

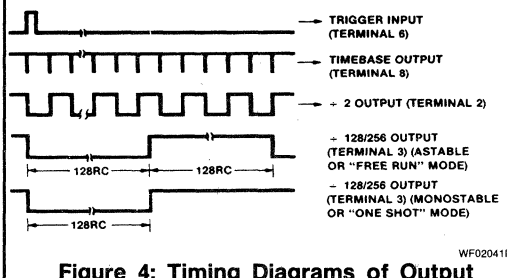


Figure 4: Timing Diagrams of Output Waveforms for the ICM7242. (Compare with Figure 8)

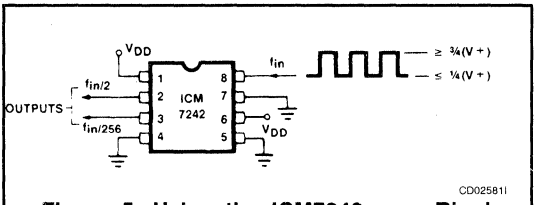


Figure 5: Using the ICM7242 as a Ripple Counter (Divider)

The ICM7242 may be used for a very low frequency square wave reference. For this application the timing components are more convenient than those that would be required by a 555 timer. For very low frequencies, devices may be cascaded (see Figure 6).

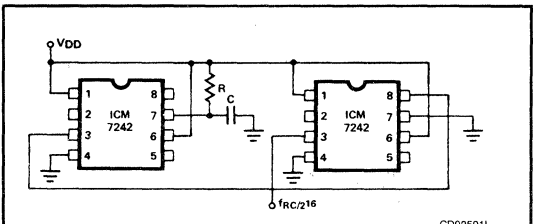


Figure 6: Low Frequency Reference (Oscillator)

For monostable operation the $\div 2^8$ output is connected to the RESET terminal. A positive edge on TRIGGER initiates the cycle (NOTE: TRIGGER overrides RESET).

THE ICM7242 is superior in all respects to the 2242 except for initial accuracy and oscillator stability. This is primarily due to the fact that high value p⁻resistors have been used on the ICM7242 to provide the comparator timing points.

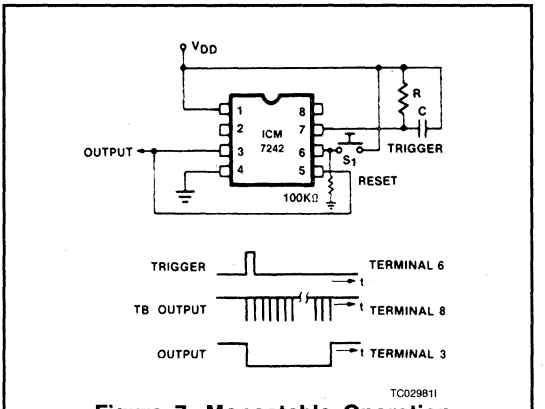


Figure 7: Monostable Operation

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7242

COMPARING THE ICM7242 WITH THE 2242

		ICM7242	2242
a.	Operating Voltage	2–16V	4–15V
b.	Operating Temp. Range	−25°C to +85°C	0°C to +70°C
c.	Supply Current V_{DD} = 5V	0.7mA Max.	7mA Max.
d.	Pullup Resistors		
	TB Output	No	Yes
	÷2 Output	No	Yes
	÷256 Output	No	Yes
e.	Toggle Rate	3.0MHz	0.5MHz
f.	Resistor to Inhibit Oscillator	No	Yes
g.	Resistor in Series with Reset for Monostable Operation	No	Yes
h.	Capacitor TB Terminal for HF Operation	No	Sometimes

By selection of R and C, a wide variety of sequence timing can be realized. A typical flow chart for a machine tool controller could be as follows:

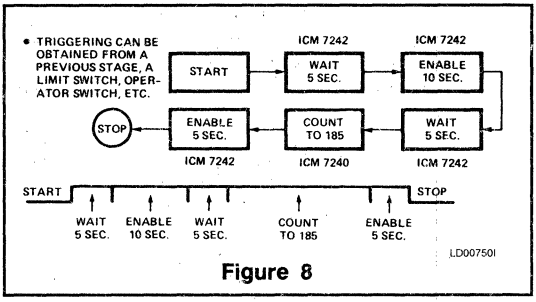
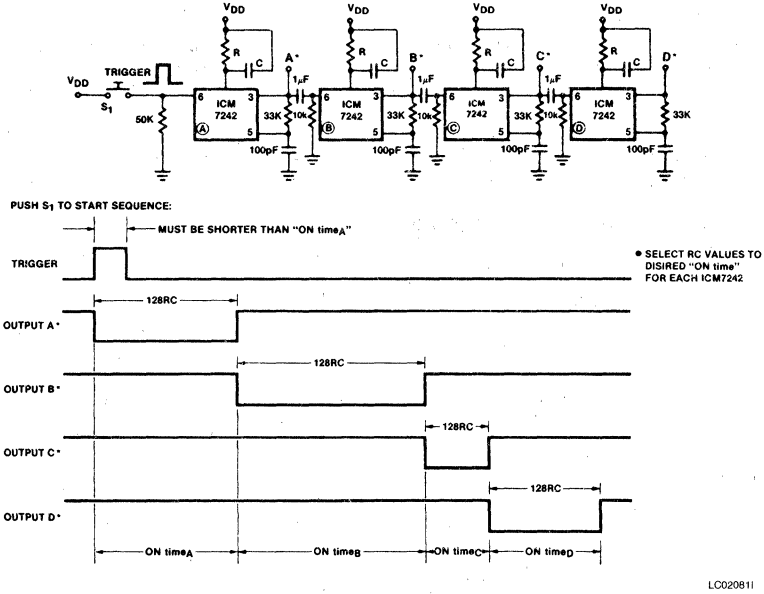


Figure 8

By cascading devices, use of low cost CMOS AND/OR gates and appropriate RC delays between stages, numerous sequential control variations can be obtained. Typical applications include injection molding machine controllers, phonograph record production machines, automatic sequencers (no metal contacts or moving parts), milling machine controllers, process timers, automatic lubrication systems, etc.

SEQUENCE TIMING

- **Process Control**
- **Machine Automation**
- **Electro—pneumatic Drivers**
- **Multi—operation (Serial or Parallel Controlling)**



- **Process Control**
- **Machine Automation**
- **Electro-Pneumatic Drivers**
- **Multi-Operation (Serial or Parallel Controlling)**

Figure 9: Sequence Timer

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7245
Stepper Motor Quartz Clock

GENERAL DESCRIPTION

The ICM7245 is a very low current, low voltage microcircuit for use in analog watches. It consists of an oscillator, dividers, logic and drivers necessary to provide either bipolar or unipolar stepper motor drive for minimum-component count watches. The oscillator is extremely stable over wide ranges of voltage and temperature, and thus combines high accuracy with low system power. The ICM7245 is fabricated using Intersil's low threshold metal-gate CMOS process.

The inverter oscillator contains all components on-chip except for the tuning capacitor and quartz crystal. The binary divider consists of 15 stages, the last 5 of which may be reset. If a reset (stop) occurs during an output pulse, the duration of the pulse is not affected. When the reset is released, the first output occurs approximately 1 second later. For the bipolar version, memory reset logic is included to make sure the first pulse after a "stop" occurs on the opposite output from the one just before the "stop".

The bipolar bridge output consists of two large inverters, normally high. The output ON resistance of the P and N channel devices in series is 200Ω maximum @ 1mA. In unipolar operation, the output is made up of a single normally high inverter. The ON resistance of the N-channel device is 50Ω maximum @ 3mA.

FEATURES

- **Very Low Current Consumption: 0.4μA at 1.55 Volt Typical**
- **32kHz Oscillator Requires Only Quartz Crystal and Trimming Capacitor**
- **Bipolar Stepper Drive With Low Output On Resistance: 200ohms Maximum (7245 A/B/D/E/F)**
- **Unipolar Stepper Drive With Very Low Output On Resistance: 50ohms Maximum (7245U)**
- **Extremely Accurate: Oscillator Stability Typically 0.1ppm**
- **STOP Function for Easy Time Synchronization**
- **Wide Temperature Range: −25°C to +85°C**
- **On Chip Fixed Oscillator Capacitor: 20pF ±20%**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7245AIPA	−25°C to +85°C	8 pin Plastic DIP
ICM7245BIPA	−25°C to +85°C	8 pin Plastic DIP
ICM7245DIPA	−25°C to +85°C	8 pin Plastic DIP
ICM7245EIPA	−25°C to +85°C	8 pin Plastic DIP
ICM7245FIPA	−25°C to +85°C	8 pin Plastic DIP
ICM7245UIPA	−25°C to +85°C	8 pin Plastic DIP

TABLE 1

DEVICE NUMBER	BIPOLAR/ UNIPOLAR	PULSE WIDTH (ms)	PULSE FREQUENCY	OSCILLATOR CAPACITOR
ICM7245A	B	9.7	1Hz	C_{OUT}
ICM7245B	B	7.8	1Hz	C_{IN}
ICM7245D	B	7.8	0.1Hz (1 pulse/ 10 seconds)	C_{OUT}
ICM7245E	B	7.8	0.0833Hz (1 pulse/ 12 seconds)	C_{IN}
ICM7245F	B	7.8	0.05Hz (1 pulse/ 20 seconds)	C_{IN}
ICM7245U	U	3.9	1Hz	C_{IN}

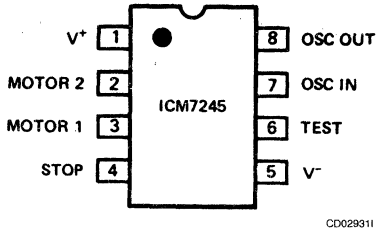


Figure 1: Pin Configuration (Outline dwg PA)

002

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7245

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD}-V_{SS}$) 3.0V
Input Voltages ..... $V_{SS}-0.3 < V_{IN} < V_{DD}+0.3$
Power Dissipation (Note 1) 25mW

Storage Temperature ..... −60°C to +150°C
Operating Temperature ..... −25°C to +85°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

Note 1: This value of power dissipation refers to that of the package and will not normally be obtained under normal operating conditions.

ELECTRICAL CHARACTERISTICS (V_{DD} = 1.55V, V_{SS} = 0V, f_{osc} = 32,768Hz, circuit in Figure 2, T_A = 25°C, unless otherwise stated. Numbers are in absolute values.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply Current	No Load		0.4	0.8	µA
V_{SUPPLY}	Operating Voltage ($V_{DD}-V_{SS}$)	0°C < T_A < 50°C	1.2		1.8	V
g_m	Oscillator Transconductance	Start-up (Note 1)	15			µs
C_{OSC}	Oscillator Capacitance	(Note 1)	16	20	24	pF
I_{STOP}	STOP Input Current				0.3	µA
I_{TEST}	TEST Input Current				10	µA
f_{STAB}	Oscillator Stability	$\Delta(V_{SUPPLY})$ = 0.6V		0.1		ppm
I_{DD}	Supply Current During Stop	'STOP' Connected to V_{DD}			1.0	µA
R_O	Output Saturation Resistance	Bipolar (N-CH. + P-CH) I_L = 1mA			200	Ω
R_{O-P}	Output Saturation Resistance P-CH	Unipolar I_L = 3mA			200	Ω
R_{O-N}	Output Saturation Resistance N-CH	Unipolar I_L = 3mA			50	Ω

NOTE 1: For design reference only, not 100% tested.

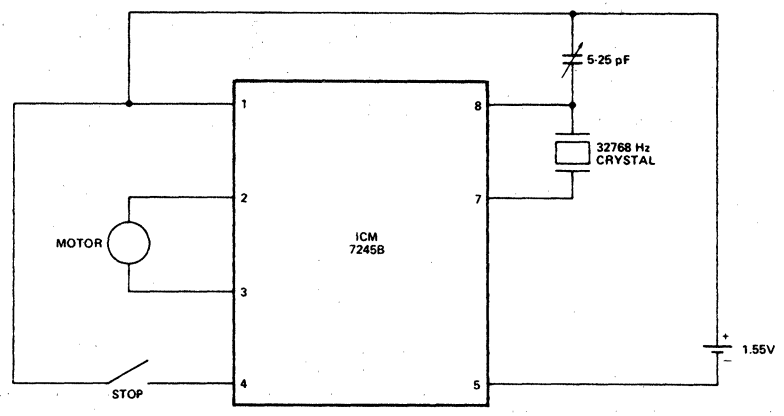


Figure 2: Typical Watch Circuit

Note: All typical values have been guaranteed by characterization and are not tested.

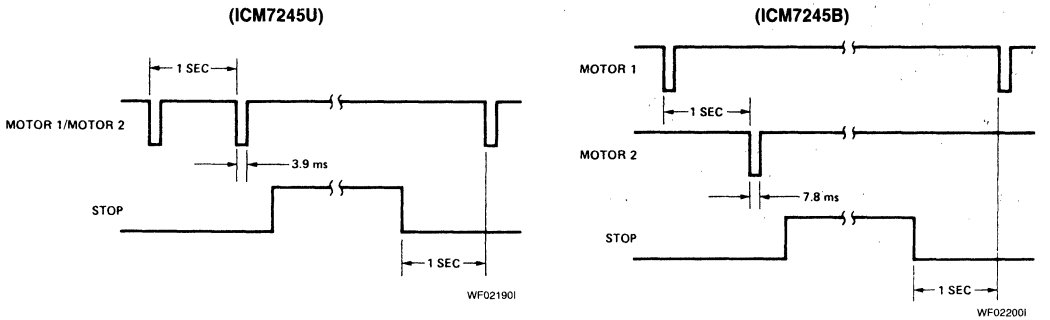
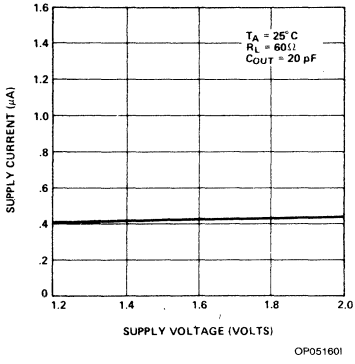


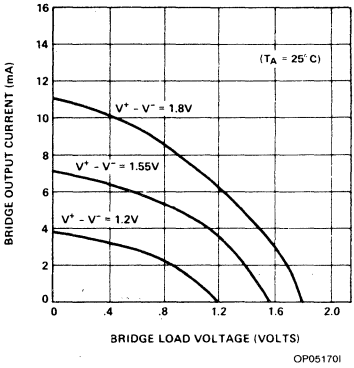
Figure 3: Timing Waveforms

TYPICAL PERFORMANCE CHARACTERISTICS

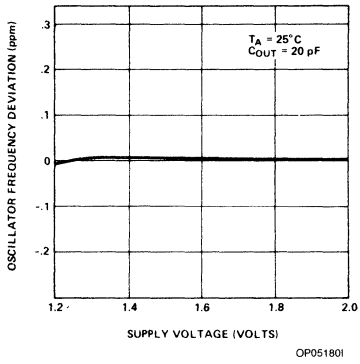
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



BRIDGE OUTPUT CURRENT AS A FUNCTION OF LOAD VOLTAGE



OSCILLATOR STABILITY AS A FUNCTION OF SUPPLY VOLTAGE



APPLICATION NOTES

OSCILLATOR

The oscillator of the ICM7245 is designed for low frequency operation at very low current from a 1.55 volt supply. The oscillator is of the inverter type, using a non-linear feedback resistor having maximum resistance under start-up conditions. The nominal load capacitance of the crystal should be less than 12pF, with a preferred range of 7-10pF. In specifying the crystal, the motional capacitance, series resistance and tuning tolerance must be compatible with the characteristics of the circuit to insure start-up and operation over a wide voltage range under worst case conditions.

The following expressions can be used to arrive at a crystal specification:

Tuning Range

$$\frac{\Delta f}{f} = \frac{C_m}{2(C_O + C_L)};\ C_L = \frac{C_{IN}\ C_{OUT}}{C_{IN} + C_{OUT}}$$

g_m required for start-up

$$g_m = 4\pi 2f2\ C_{IN}\ C_{OUT}\ R_S \left(1 + \frac{C_O}{C_L}\right)^2$$

where

R_S = Series Resistance of Crystal

f = Frequency of the Crystal

Δf = Frequency Shift from Series Resonance Frequency

C_O = Static Capacitance of Crystal

C_{IN} = Input Capacitance

C_{OUT} = Output Capacitance

C_L = Load Capacitance

C_m = Motional Capacitance of Crystal

The g_m required for start-up calculated should not exceed 50% of the g_m guaranteed for the device.

TEST POINT

The TEST input, when connected to V^-, causes the ICM7245B/U to speed-up the outputs by 16 times. On long

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7245

period output versions (12,20,60 sec) the speed-up factor will be larger. This allows easy testing of the finished watch module. The pulse width is not affected by the speed-up of the pulse frequency.

CUSTOM VERSIONS

The ICM7245 may be modified with alternative metal masks to provide different number of dividers, various pulse widths, and different output configurations.

In addition, MOS capacitors on-chip up to a total of 50 pF may be connected to either the input and/or the output of the oscillator. Consult your Intersil representative or the factory for further information.

Note: All typical values have been guaranteed by characterization and are not tested.

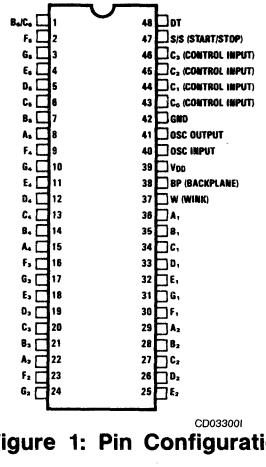
ICM7249

5½ Digit LCD μ-Power Event/Hour Meter

GENERAL DESCRIPTION

The ICM7249 Timer/Counter is intended for long-term battery-supported industrial applications. The ICM7249 typically draws 1μA during active timing or counting, due to Intersil's special low-power design techniques. This allows more than 10 years of continuous operation without battery replacement. The chip offers four timing modes, eight counting modes and four test modes.

The ICM7249 is a 48-lead device, powered by a single DC voltage source and controlled by a 32.768kHz quartz crystal. No other external components are required. Inputs to the chip are TTL-compatible and outputs drive standard LCD segments. The chip is available in dice and in ceramic side-brazed packages.



CD00330I

Figure 1: Pin Configuration

FEATURES

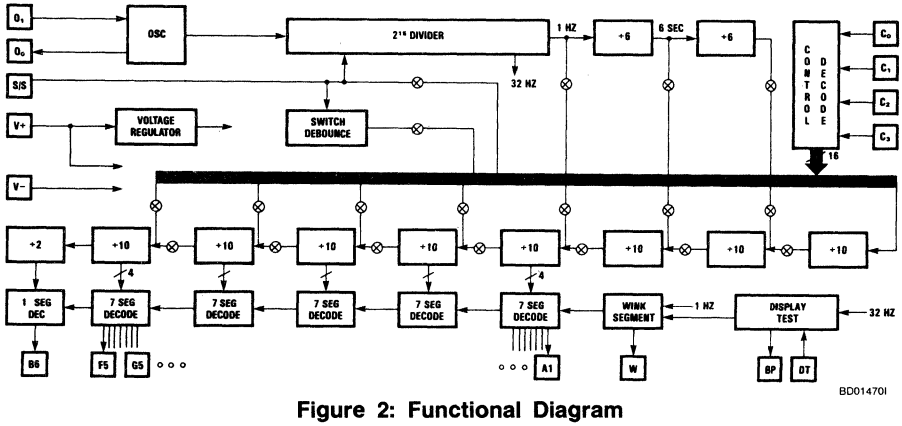
- **Hour Meter Requires Only 4 Parts Total**
- **Micropower Operation: < 1μA at 2.8V Typical**
- **10 Year Operation On One Lithium Cell**
  2½ Year Battery Life With Display Connected
- **Directly drives 5½ Digit LCD**
- **14 Programmable Modes of Operation**
- **Times Hrs., 0.1 Hrs., .01 Hrs., .1 Mins.**
- **Counts 1's, 10's, 100's, 1000's**
- **Dual Funtion Input Circuit:**
  – Selectable Debounce for Counter
  – High-Pass Filter for Timer
- **Direct AC Line Triggering With Input Resistor**
- **Winking "Timer Active" Display Output**
- **Display Test Feature**

APPLICATIONS

- **AC or DC Hour Meters**
- **AC or DC Totalizers**
- **Portable Battery Powered Equipment**
- **Long Range Service Meters**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7249IDM	–40°C to +85°C	48-Pin Ceramic
ICM7249/D	25°C	Die



BD01470I

Figure 2: Functional Diagram

203500-003

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7249

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6V
Input Voltage
Pins 43-48 (Note 1) ..... (V_{SS} −0.3V) to (V_{DD} +0.3V)
Power Dissipation (Note 2) 200mW

Operating Temperature Range ..... −40°C to 85°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Temperature = −40°C to +85°C, V_{DD} = 2.2V to 5.5V, V_{SS} = 0V, unless otherwise noted. Typical specifications measured at temperature = 25°C and V_{DD} = 2.8V unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{DD}	Operating Voltage	Note 3	2.2		5.5	V
I_{DD}	Operating Current	Note 4, All inputs = V_{DD} or GND V_{DD} = 2.8V V_{DD} = 5.5V		1.0 4.0	3.0 10.0	µA µA
I_{IN} I_{SS} I_{DT}	**Input Current:** C_0-C_3, S/S DT	All Inputs V_{DD} or GND Note 5		 1.5	1 3.0 90	µA µA µA
V_{IL} V_{IH}	**Input Voltage:** C_0-C_3, DT, S/S		 0.7 V_{DD}		0.3 V_{DD}	V V
V_{OL} V_{OH}	Segment Output Voltage	I_{OL} = 1µA I_{OH} = 1µA	 V_{DD} − 0.8		0.8	V
V_{OL} V_{OH}	Backplane Output Voltage	I_{OL} = 10µA I_{OH} = 10µA	 V_{DD} − 0.8	 V	0.8	V
—	**Oscillator Stability:** Temp. = 25°C, V_{DD} = 2.2V to 5.5V Temp. = −40°C to +85°C, V_{DD} = 2.2V to 5.5V			0.1 5		ppm ppm
T_{HP} T_{DE} T_{DE}	**S/S Pulse Width:** High-pass Filter (Modes 0-3) Debounce (Modes 4, 6, 8, 10) w/o Debounce (Modes 5, 7, 9, 11)		5 10,000 5		10,000	µs µs µs

NOTES:
1. Due to the SCR structure inherent in junction-isolated CMOS devices, the circuit can be put in a latchup mode if large currents are injected into device inputs or outputs. For this reason special care should be taken in a system with multiple power supplies to prevent voltages being applied to inputs or outputs before power is applied. If only inputs are affected, latchup also can be prevented by limiting the current into the input terminal to less than 1mA.
2. This limit refers to that of the package and will not occur during normal operation.
3. Internal reset to 00000 requires a maximum V_{DD} rise time of 1µs. Longer rise times at power-up may cause improper reset.
4. Operating current is measured with the LCD disconnected and input current I_{SS} supplied externally.
5. Inputs C_0-C_3 are latched internally and draw no DC current after switching. During switching, a 90µA peak current may be drawn for 10 nanoseconds.

Note: All typical values have been guaranteed by characterization and are not tested.

Table 1. Pin Assignment and Function

PIN	NAME	DESCRIPTION
1	B_6/C_6	Half-digit LCD segment output.
2	F_5	Seven-segment LCD outputs.
3	G_5	
4	E_5	
5	D_5	
6	C_5	
7	B_5	
8	A_5	
9	F_4	
10	G_4	
11	E_4	
12	D_4	
13	C_4	
14	B_4	
15	A_4	
16	F_3	
17	G_3	
18	E_3	
19	D_3	
20	C_3	
21	B_3	
22	A_3	
23	F_2	
24	G_2	
25	E_2	
26	D_2	
27	C_2	
28	B_2	
29	A_2	
30	F_1	
31	G_1	
32	E_1	
33	D_1	
34	C_1	
35	B_1	
36	A_1	

PIN	NAME	DESCRIPTION
37	W	Wink-segment output.
38	BP	Backplane for LCD reference.
39	V+	Positive supply voltage.
40	OSC_I	Quartz Crystal connections
41	OSC_O	
42	GND	Chip GRouND.
43	C_0	Mode-select control inputs.
44	C_1	
45	C_2	
46	C_3	
47	S/S	Start / Stop
48	DT	Display Test

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7249

Table 2. Mode Select Table

Mode	Control Pin Inputs				Function
	C_3	C_2	C_1	C_0	
0	0	0	0	0	1 hour interval timer
1	0	0	0	1	0.1 hour interval timer
2	0	0	1	0	0.01 hour interval timer
3	0	0	1	1	0.1 minute interval timer
4	0	1	0	0	1's counter with debounce
5	0	1	0	1	1's counter
6	0	1	1	0	10's counter with debounce
7	0	1	1	1	10's counter
8	1	0	0	0	100's counter with debounce
9	1	0	0	1	100's counter
10	1	0	1	0	1000's counter with debounce
11	1	0	1	1	1000's counter
12	1	1	0	0	Test display digits
13	1	1	0	1	Internal test
14	1	1	1	0	Internal test
15	1	1	1	1	Reset

DETAILED DESCRIPTION

After power is applied, the ICM7249 requires a rise time of t_R to become active and for oscillation to begin, as seen in Figure 3. Initially the backplane output BP is a logic '1' level, but then changes after every 512 crystal oscillation cycles, giving BP a square-wave frequency of 32Hz. Segments are turned off when the voltage levels of the segment drive pins are the same as and in phase with BP. Segments are turned on by having the drive pin voltages out of phase with BP.

The 16 modes are selected by placing the binary equivalent of the mode number on inputs C_0–C_3 (Table 2). In the four timer modes, timing is controlled by the Start/Stop input S/S. Because of internal high-pass filtering, timing is active when either S/S is held high for more than 25ms, or the input signal has a frequency of at least 50Hz and less than 120kHz as shown in Figure 4. Driving S/S with an input frequency between 40Hz and 50Hz has an indeterminate effect on the timing.

The timing intervals are different for each mode. For example, in Mode 0 the display is incremented every hour, while in Mode 3 the display is incremented every tenth of a minute.

While timing is active, the wink-segment output W will flash, as seen in Figure 1. On the upward transistion of S/S, the wink output turns off. It remains off for 16 backplane cycles and turns back on for another 16 cycles. If timing is still active, the wink segment repeats this process, giving it a flash rate of 1Hz: otherwise the wink output remains on until timing begins again. In counting modes 4-11, the count is registered and latched on each positive transition of S/S. The display is keyed to the specific counting mode. In the 1's counter mode, the display is incremented for each count; in the 10's counter mode, the display is incremented after every count.

Note: All typical values have been guaranteed by characterization and are not tested.

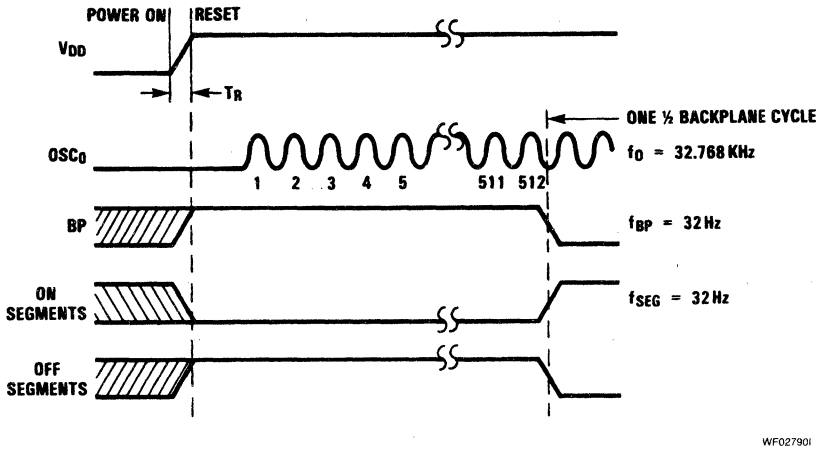


Figure 3: Power On/Reset Waveforms

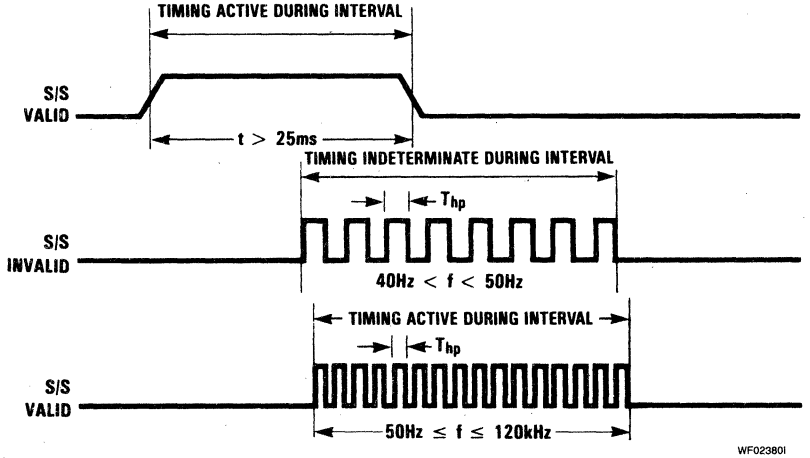


Figure 4: Start/Stop Input High-Pass Filtering in Timing Modes

Note: All typical values have been guaranteed by characterization and are not tested.

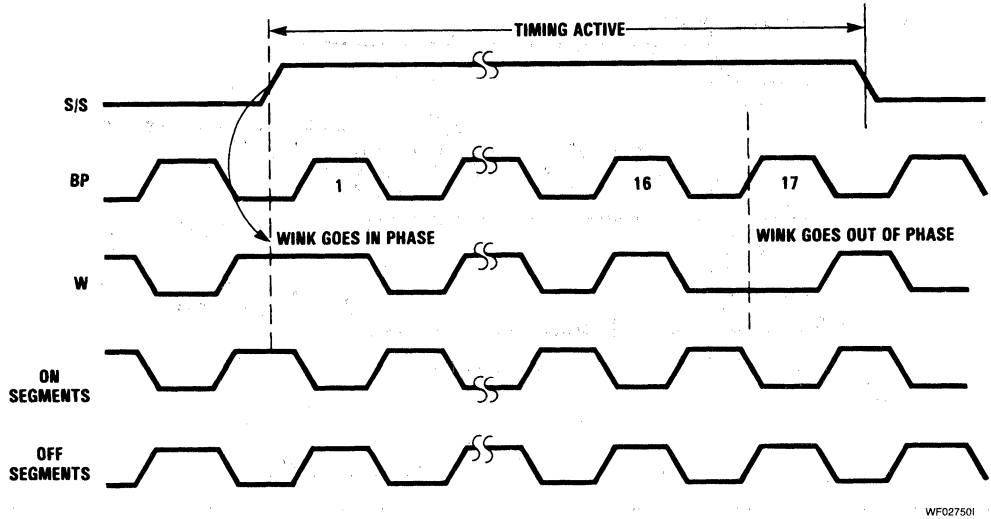


Figure 5: Wink Waveforms in Timing Modes

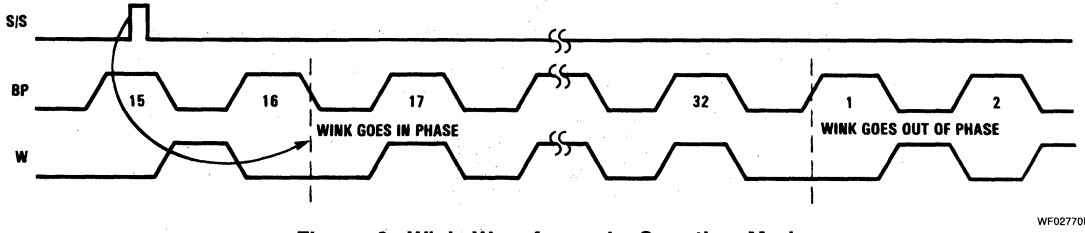


Figure 6: Wink Waveforms in Counting Modes

During counting, the display will wink off at each count input regardless of whether the display is incremented. When a count occurs, the wink segment output turns off at the end of the 16th BP cycle and turns back on at the end of the 32nd BP cycle, creating a half-second wink, as shown in Figure 6. If counting occurs more frequently than once a second, the wink output will default to a constant 1Hz flash rate.

In counter modes 4, 6, 8 and 10, the count pulse is subject to debounce filtering. Figure 7 shows that only pulses with a frequency of less than 40Hz are valid. Pulses with a frequency between 50Hz and 120kHz are ignored, while those with a frequency between 40Hz and 50Hz have an indeterminate effect on the count.

Note: All typical values have been guaranteed by characterization and are not tested.

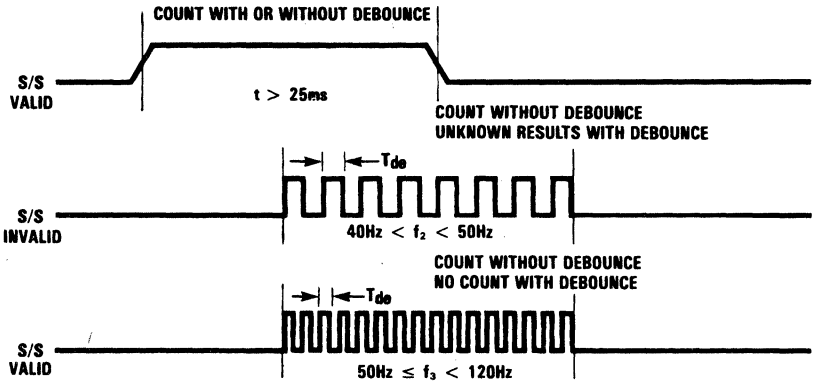


Figure 7: Start/Stop Input Debounce Filtering in Counting Modes

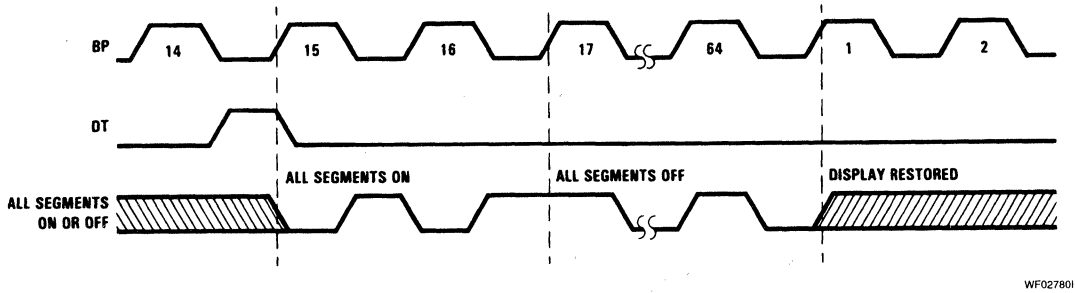


Figure 8: Display Testing

The display may be tested at any time without disturbing operation by pulsing DT high, as seen in Figure 8. On the next positive transition of BP, all the segments turn on and remain on until the end of the 16th BP cycle. This takes a half-second or less. All the segments then turn off for an additional 48 BP cycles (the end of the 64th cycle), after which valid data returns to the display. As long as DT is held high, the segments will remain on.

Additional display testing is provided by using mode 12. In this mode each displayed decade is incremented on each positive transition of S/S. Modes 13 and 14 are for manufacturer testing only.

Mode 15 resets all the decades and internal counters to zero, essentially bringing everything back to power-up status.

APPLICATION NOTES

A typical use of the ICM7249 is seen in Figure 9, the Motor Hour Meter. In this application the ICM7249 is configured as an hours-in-use meter and shows how many whole hours of line voltage have been applied. The 20MΩ resistor and high-pass filtering allow AC line activation of the S/S input. This configuration, which is powered by a 3V lithium cell, will operate continuously for 2½ years. Without the display, which only needs to be connected when a reading is required, the span of operation is extended to 10 years.

When the ICM7249 is configured as an attendance counter, as shown in Figure 10, the display shows each increment. By using mode 2, external debouncing of the gate switch is unnecessary, provided the switch bounce is less than 35ms.

The 3V lithium battery can be replaced without disturbing operation if a suitable capacitor is connected in parallel with it. The display should be disconnected, if possible, during the procedure to minimize current drain. The capacitor should be large enough to store charge for the amount of time needed to physically replace the battery ($\Delta t = \Delta VC/I$). A 10μF capacitor initially charged to 3V will supply a current of 1.0μA for 8 seconds before its voltage drops to 2.2V, which is the minimum operating voltage for the ICM7249.

Before the battery is removed, the capacitor should be placed in parallel, across the V_{DD} and GND terminals. After the battery is replaced, the capacitor can be removed and the display reconnected.

Note: All typical values have been guaranteed by characterization and are not tested.

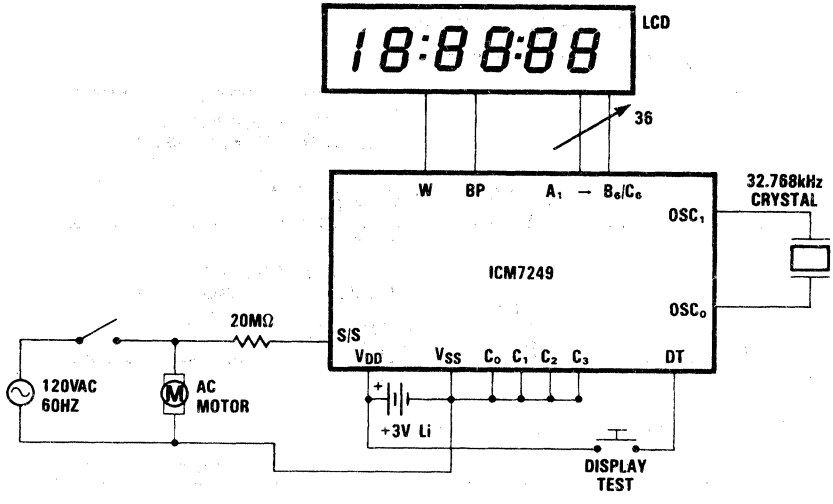


Figure 9: Motor Hour Meter

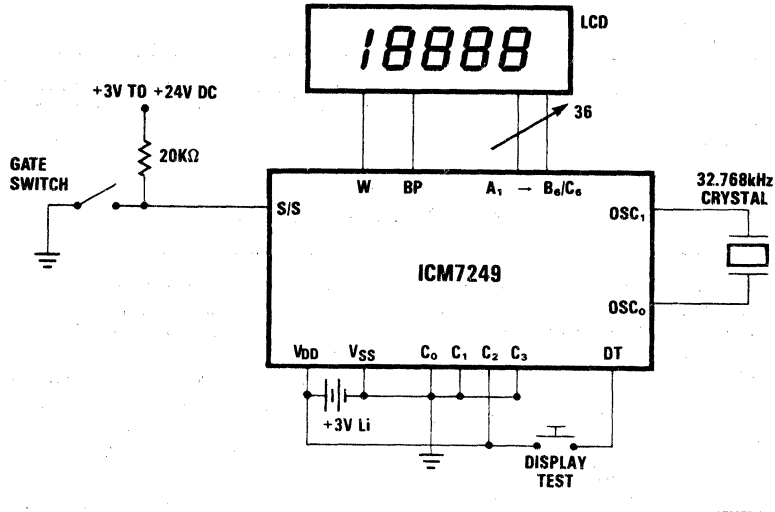


Figure 10: Attendance Counter

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7555/ICM7556
General Purpose Timer

GENERAL DESCRIPTION

The ICM7555/6 are CMOS RC timers providing significantly improved performance over the standard SE/NE555/6 and 355 timers, while at the same time being direct replacements for those devices in most applications. Improved parameters include low supply current, wide operating supply voltage range, low THRESHOLD, $\overline{\text{TRIGGER}}$ and $\overline{\text{RESET}}$ currents, no crowbarring of the supply current during output transitions, higher frequency performance and no requirement to decouple CONTROL VOLTAGE for stable operation.

Specifically, the ICM7555/6 are stable controllers capable of producing accurate time delays or frequencies. The ICM7556 is a dual ICM7555, with the two timers operating independently of each other, sharing only V^+ and GND. In the one shot mode, the pulse width of each circuit is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled by two external resistors and one capacitor. Unlike the regular bipolar 555/6 devices, the CONTROL VOLTAGE terminal need not be decoupled with a capacitor. The circuits are triggered and reset on falling (negative) waveforms, and the output inverter can source or sink currents large enough to drive TTL loads, or provide minimal offsets to drive CMOS loads.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7555CBA	0°C to +70°C	8 Lead S.O.I.C.
ICM7555IPA	−25°C to +85°C	8 Lead MiniDip
ICM7555ITV	−25°C to +85°C	TO-99 Can
ICM7555MTV*	−55°C to +125°C	TO-99 Can
ICM7556IPD	−25°C to +85°C	14 Lead Plastic DIP
ICM7556MJD*	−55°C to +125°C	14 Lead CERDIP
ICM7555/D	—	DICE**
ICM7556/D	—	DICE**

*Add /883B to part number if 883B processing is desired.

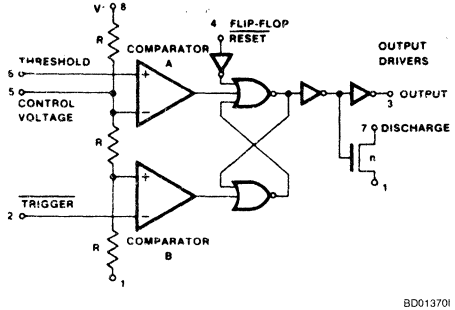
**Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.

FEATURES

- **Exact Equivalent in Most Cases for SE/NE555/556 or TLC555/556**
- **Low Supply Current — 60μA Typ. (ICM7555) 120μA Typ. (ICM7556)**
- **Extremely Low Trigger, Threshold and Reset Currents — 20pA Typical**
- **High Speed Operation — 1MHz Typical**
- **Wide Operation Supply Voltage Range Guaranteed 2 to 18 Volts**
- **Normal Reset Function – No Crowbarring of Supply During Output Transition**
- **Can Be Used With Higher Impedance Timing Elements Than Regular 555/6 for Longer RC Time Constants**
- **Timing From Microseconds Through Hours**
- **Operates in Both Astable and Monostable Modes**
- **Adjustable Duty Cycle**
- **High Output Source/Sink Driver Can Drive TTL/CMOS**
- **Typical Temperature Stability of 0.005% Per °C at 25°C**
- **Outputs Have Very Low Offsets, HI and LO**

APPLICATIONS

- **Precision Timing**
- **Pulse Generation**
- **Sequential Timing**
- **Time Delay Generation**
- **Pulse Width Modulation**
- **Pulse Position Modulation**
- **Missing Pulse Detector**



This Functional Diagram reduces the circuitry down to its simplest equivalent components. Tie down unused inputs. R = 100kΩ, ±20% typ.

Figure 1: Functional Diagram

Note: All typical values have been guaranteed by characterization and are not tested.

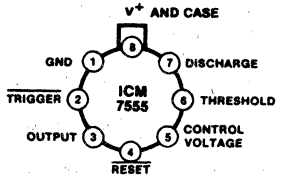
ICM7555/ICM7556

ABSOLUTE MAXIMUM RATINGS

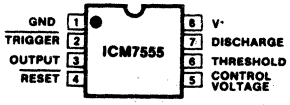
Supply Voltage ..... +18 Volts
Input Voltage: $\overline{\text{Trigger}}$,
Control Voltage, Threshold, $\leq V^+ + 0.3V$ to $\geq V^- - 0.3V$
$\overline{\text{Reset}}$
Output Current 100mA
Power Dissipation[2] ICM7556 ..... 300mW
ICM7555 ..... 200mW
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C

Operating Temperature Range[2]
ICM7555IPA ..... −25°C to +85°C
ICM7555ITV ..... −25°C to +85°C
ICM7556IPD ..... −25°C to +85°C
ICM7555MTV ..... −55°C to +125°C
ICM7556MJD ..... −55°C to +125°C

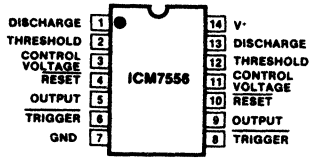
NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



(OUTLINE DRAWING TV)

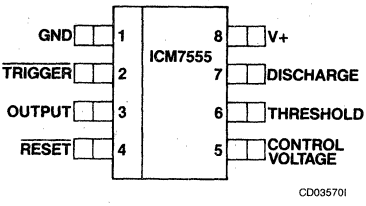


(OUTLINE DRAWING PA)



(OUTLINE DRAWING JD, PD)

CD02990I



CD03570I

(OUTLINE DRAWING BA)

Figure 2: Pin Configuration (Top View)

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7555/ICM7556

INTERSIL

ELECTRICAL CHARACTERISTICS ICM7555 T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I^+	Static Supply Current	T_A = −55°C to 125°C V_{DD} = 5V V_{DD} = 15V		40 60	200 300	µA µA
	Monostable Timing Accuracy	RA = 10k, C = 0.1µF V_{DD} = 5V		2		%
	Drift with Temp*	T_A = −55 to 125°C V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		 150 200 250		 ppm/°C ppm/°C ppm/°C
	Drift with Supply*	V_{DD} = 5 to 15V		0.5		%/V
	Astable Timing Accuracy	RA = RB = 10k, C = 0.1µF, V_{DD} = 5V		2		%
	Drift with Temp*	T_A = −55°C to 125°C V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		 150 200 250		 ppm/°C ppm/°C ppm/°C
	Drift with Supply*	V_{DD} = 5 to 15V		0.5		%/V
V_{TH}	Threshold Voltage	V_{DD} = 15V		67		% V_{DD}
V_{TRIG}	Trigger Voltage	V_{DD} = 15V		32		% V_{DD}
I_{TRIG}	Trigger Current	V_{DD} = 15V			10	nA
I_{TH}	Threshold Current	V_{DD} = 15V			10	nA
V_{CV}	Control Voltage	V_{DD} = 15V		67		% V_{DD}
V_{RST}	Reset Voltage	V_{DD} = 2 to 15V	0.4		1.0	V
I_{RST}	Reset Current	V_{DD} = 15V			10	nA
I_{DIS}	Discharge Leakage	V_{DD} = 15V			10	nA
V_{OL}	Output Voltage Drop	V_{DD} = 15V I_{sink} = 20mA V_{DD} = 5V I_{sink} = 3.2mA		0.4 0.2	1.0 0.4	V V
V_{OH}	Output Voltage Drop	V_{DD} = 15V I_{source} = 0.8mA V_{DD} = 5V I_{source} = 0.8mA	14.3 4.0	14.6 4.3		V V
V_{DIS}	Discharge Output Voltage Drop	V_{DD} = 5 to 15V I_{sink} = 15mA		0.2	0.4	V
V^+	Supply Voltage*	Functional Oper.	2.0		18.0	V
t_R	Output Rise Time*	RL = 10M, CL = 10pF, V_{DD} = 5V		75		ns
t_F	Output Fall Time*	RL = 10M, CL = 10pF, V_{DD} = 5V		75		ns
f_{MAX}	Oscillator Frequency*	V_{DD} = 5V RA = 470ohm, RB = 270ohm C = 200pF		1		MHz

* This parameter not tested. The majority of all parts meet this specification.

7

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7555/ICM7556

INTERSIL

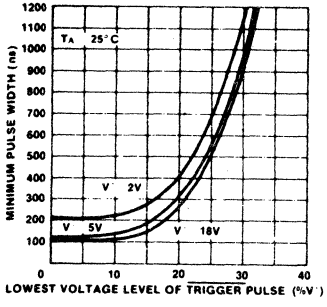
ELECTRICAL CHARACTERISTICS ICM7556 T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I^+	Static Supply Current	T = −55°C to 125°C V_{DD} = 5V V_{DD} = 15V		80 120	400 600	μA μA
	Monostable Timing Accuracy	RA = 10k, C = 0.1μF V_{DD} = 5V		2		%
	Drift with Temp*	T = −55 to 125°C V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		 150 200 250		 ppm/°C ppm/°C ppm/°C
	Drift with Supply*	V_{DD} = 5 to 15V		0.5		%/V
	Astable Timing Accuracy	RA = RB = 10k, C = 0.1μF, V_{DD} = 5V		2		%
	Drift with Temp*	T = −55°C to 125°C V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		 150 200 250		 ppm/°C ppm/°C ppm/°C
	Drift with Supply*	V_{DD} = 5 to 15V		0.5		% V
V_{TH}	Threshold Voltage	V_{DD} = 15V		67		% V_{DD}
V_{TRIG}	Trigger Voltage	V_{DD} = 15V		32		% V_{DD}
I_{TRIG}	Trigger Current	V_{DD} = 15V			10	nA
I_{TH}	Threshold Current	V_{DD} = 15V			10	nA
V_{CV}	Control Voltage	V_{DD} = 15V		67		% V_{DD}
V_{RST}	Reset Voltage	V_{DD} = 2 to 15V	0.4		1.0	V
I_{RST}	Reset Current	V_{DD} = 15V			10	nA
I_{DIS}	Discharge Leakage	V_{DD} = 15V			10	nA
V_{OL}	Output Voltage Drop	V_{DD} = 15V I_{sink} = 20mA V_{DD} = 5V I_{sink} = 3.2mA		0.4 0.2	1.0 0.4	V V
V_{OH}	Output Voltage Drop	V_{DD} = 15V I_{source} = 0.8mA V_{DD} = 5V I_{source} = 0.8mA	14.3 4.0	14.6 4.3		V V
V_{DIS}	Discharge Output Voltage Drop	V_{DD} = 5 to 15V I_{sink} = 15mA		0.2	0.4	V
V^+	Supply Voltage*	Functional Oper.	2.0		18.0	V
t_R	Output Rise Time*	RL = 10M, CL = 10pF, V_{DD} = 5V		75		ns
t_F	Output Fall Time*	RL = 10M, CL = 10pF, V_{DD} = 5V		75		ns
f_{MAX}	Oscillator Frequency*	V_{DD} = 5V RA = 470ohm, RB = 270ohm C = 200pF		1		MHz

* This parameter not tested. The majority of all parts meet this specification.

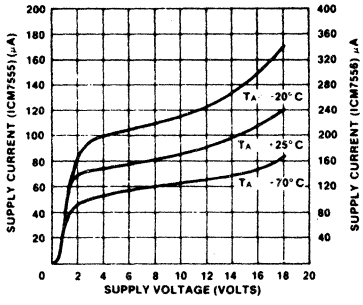
TYPICAL PERFORMANCE CHARACTERISTICS

MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



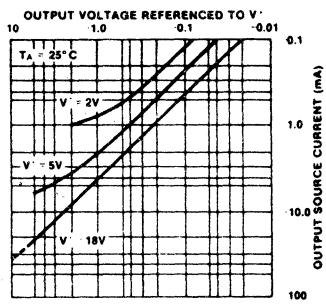
OP05490I

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



OP05500I

OUTPUT SOURCE CURRENT AS A FUNCTION OF OUTPUT VOLTAGE

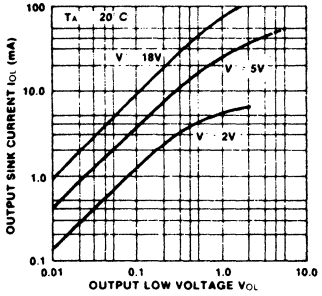


OP05510I

Note: All typical values have been guaranteed by characterization and are not tested.

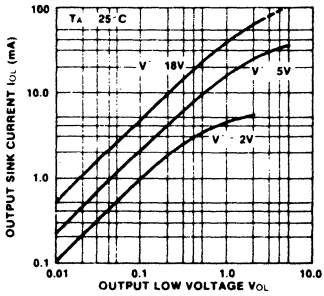
TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



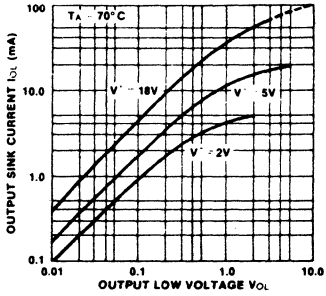
OP05520I

OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



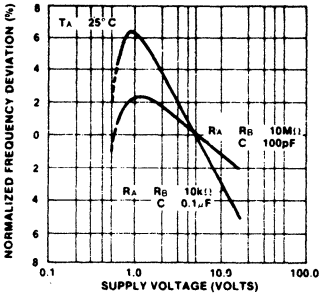
OP05530I

OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



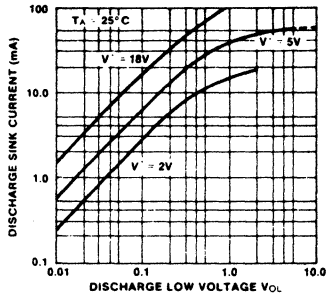
OP05540I

NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE



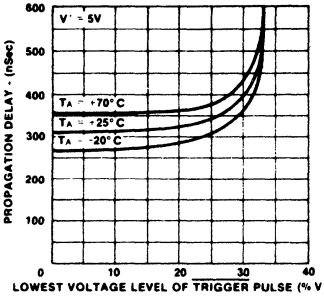
OP05550I

DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE



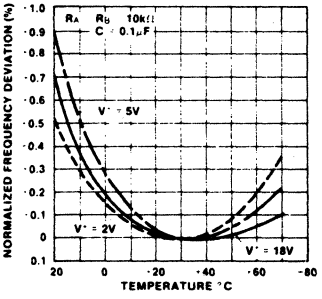
OP05560I

PROPAGATION DELAY AS A FUNCTION OF VOLTAGE LEVEL OF TRIGGER PULSE



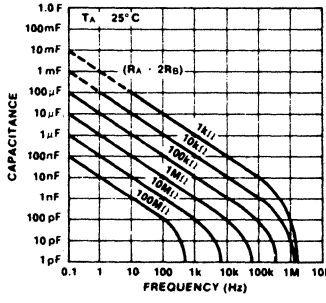
OP05570I

NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE



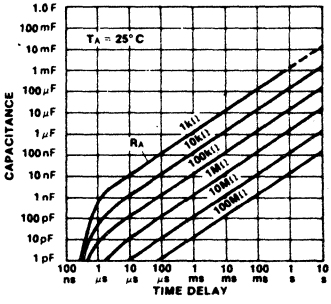
OP05580I

FREE RUNNING FREQUENCY AS A FUNCTION OF R_A, R_B and C



OP05590I

TIME DELAY IN THE MONOSTABLE MODE AS A FUNCTION OF R_A AND C



OP05600I

7

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7555/ICM7556

APPLICATION NOTES

GENERAL

The ICM7555/6 devices are, in most instances, direct replacements for the NE/SE 555/6 devices. However, it is possible to effect economies in the external component count using the ICM7555/6. Because the bipolar 555/6 devices produce large crowbar currents in the output driver, it is necessary to decouple the power supply lines with a good capacitor close to the device. The 7555/6 devices produce no such transients. See Figure 3.

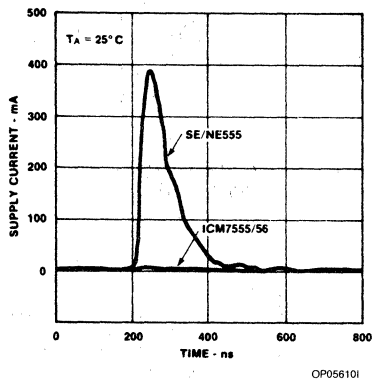


Figure 3: Supply Current Transient Compared with a Standard Bipolar 555 During an Output Transition

The ICM7555/6 produces supply current spikes of only 2–3mA instead of 300–400mA and supply decoupling is normally not necessary. Secondly, in most instances, the CONTROL VOLTAGE decoupling capacitors are not required since the input impedance of the CMOS comparators on chip are very high. Thus, for many applications 2 capacitors can be saved using an ICM7555, and 3 capacitors with an ICM7556.

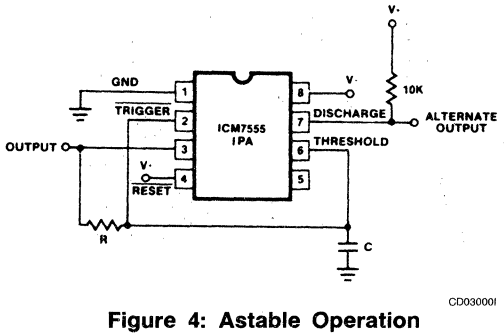


Figure 4: Astable Operation

POWER SUPPLY CONSIDERATIONS

Although the supply current consumed by the ICM7555/6 devices is very low, the total system supply can be high unless the timing components are high impedance. Therefore, use high values for R and low values for C in Figures 4 and 5.

OUTPUT DRIVE CAPABILITY

The output driver consists of a CMOS inverter capable of driving most logic families including CMOS and TTL. As such, if driving CMOS, the output swing at all supply voltages will equal the supply voltage. At a supply voltage of 4.5 volts or more the ICM7555/6 will drive at least 2 standard TTL loads.

ASTABLE OPERATION

The circuit can be connected to trigger itself and free run as a multivibrator, see Figure 4. The output swings from rail to rail, and is a true 50% duty cycle square wave. (Trip points and output swings are symmetrical). Less than a 1% frequency variation is observed, over a voltage range of +5 to +15V.

$$f = \frac{1}{1.4\ RC}$$

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot. Initially the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative $\overline{\text{TRIGGER}}$ pulse to pin 2, the internal flip flop is set which releases the short circuit across the external capacitor and drives the OUTPUT high. The voltage across the capacitor now increases exponentially with a time constant $t = R_A C$. When the voltage across the capacitor equals 2/3 V^+, the comparator resets the flip flop, which in turn discharges the capacitor rapidly and also drives the OUTPUT to its low state. $\overline{\text{TRIGGER}}$ must return to a high state before the OUTPUT can return to a low state.

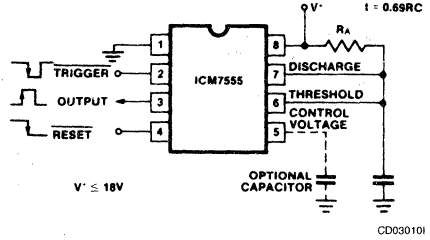


Figure 5: Monostable Operation

CONTROL VOLTAGE

The CONTROL VOLTAGE terminal permits the two trip voltages for the THRESHOLD and $\overline{\text{TRIGGER}}$ internal comparators to be controlled. This provides the possibility of oscillation frequency modulation in the astable mode or even inhibition of oscillation, depending on the applied voltage. In the monostable mode, delay times can be changed by varying the applied voltage to the CONTROL VOLTAGE pin.

$\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ terminal is designed to have essentially the same trip voltage as the standard bipolar 555/6, i.e. 0.6 to 0.7 volts. At all supply voltages it represents an extremely high input impedance. The mode of operation of the $\overline{\text{RESET}}$

Note: All typical values have been guaranteed by characterization and are not tested.

function is, however, much improved over the standard bipolar 555/6 in that it controls only the internal flip flop, which in turn controls simultaneously the state of the OUTPUT and DISCHARGE pins. This avoids the multiple threshold problems sometimes encountered with slow falling edges in the bipolar devices.

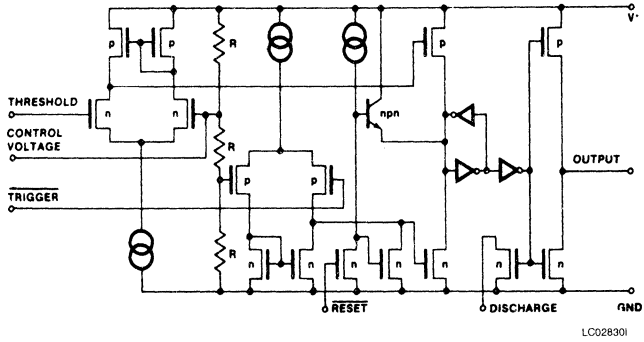


Figure 6: Equivalent Circuit

TRUTH TABLE

THRESHOLD VOLTAGE	TRIGGER VOLTAGE	$\overline{\text{RESET}}$	OUTPUT	DISCHARGE SWITCH
DON'T CARE	DON'T CARE	LOW	LOW	ON
$> 2/3(V^+)$	$> 1/3(V^+)$	HIGH	LOW	ON
$V_{TH} < 2/3$	$V_{TR} > 1/3$	HIGH	STABLE	STABLE
DON'T CARE	$< 1/3(V^+)$	HIGH	HIGH	OFF

NOTE: $\overline{\text{RESET}}$ will dominate all other inputs: $\overline{\text{TRIGGER}}$ will dominate over THRESHOLD.

Note: All typical values have been guaranteed by characterization and are not tested.

Section 8 — Display Drivers

ICM7211/12
4-Digit LCD/LED Display Driver

GENERAL DESCRIPTION

The ICM7211 (LCD) and ICM7212 (LED) devices constitute a family of non-multiplexed four-digit seven-segment CMOS display decoder-drivers.

The ICM7211 devices are configured to drive conventional LCD displays by providing a complete RC oscillator, divider chain, backplane driver, and 28 segment outputs.

The ICM7212 devices are configured to drive common-anode LED displays, providing 28 current-controlled, low leakage, open-drain n-channel outputs. These devices provide a BRighTness input, which may be used at normal logic levels as a display enable, or with a potentiometer as a continuous display brightness control.

Both the LCD and LED devices are available with multiplexed or microprocessor input configurations. The multiplexed versions provide four data inputs and four Digit Select inputs. This configuration is suitable for interfacing with multiplexed BCD or binary output devices, such as the ICM7217, ICM7226 and ICL7135. The microprocessor versions provide data input latches and Digit Address latches under control of high-speed Chip Select inputs. These devices simplify the task of implementing a cost-effective alphanumeric seven-segment display for microprocessor systems, without requiring extensive ROM or CPU time for decoding and display updating.

The standard devices will provide two different decoder configurations. The basic device will decode the four bit binary inputs into a seven-segment alphanumeric hexadecimal output. The "A" versions will provide the "Code B" output code, i.e., 0-9, dash, E, H, L, P, blank. Either device will correctly decode true BCD to seven-segment decimal outputs.

Devices in the ICM7211/7212 family are packaged in a standard 40 pin plastic dual-in-line package and all inputs are fully protected against static discharge.

ICM7211 (LCD) FEATURES

- **Four Digit Non-Multiplexed 7 Segment LCD Display Outputs With Backplane Driver**
- **Complete Onboard RC Oscillator to Generate Backplane Frequency**
- **Backplane Input/Output Allows Simple Synchronization of Slave-Devices to a Master**
- **ICM7211 Devices Provide Separate Digit Select Inputs to Accept Multiplexed BCD Input (Pinout and Functionally Compatible With Siliconix DF411)**
- **ICM7211M Devices Provide Data and Digit Address Latches Controlled by Chip Select Inputs to Provide a Direct High Speed Processor Interface**
- **ICM7211 Decodes Binary Hexadecimal; ICM7211A Decodes Binary to Code B (0-9, Dash, E, H, L, P, Blank)**

ICM7212 (LED) FEATURES

- **28 Current-Limited Segment Outputs Provide 4-Digit Non-Multiplexed Direct LED Drive at > 5mA Per Segment**
- **Brightness Input Allows Direct Control of LED Segment Current With a Single Potentiometer or Digitally as a Display Enable**
- **ICM7212M and ICM7212A Devices Provide Same Input Configuration and Output Decoding Options as the ICM7211**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7211/D	—	DICE
ICM7211M/D	—	DICE
ICM7211AIJL	-40°C to +85°C	40 Pin CERDIP
ICM7211AMIJL	-40°C to +85°C	40 Pin CERDIP
ICM7211IJL	-40°C to +85°C	40 Pin CERDIP
ICM7211IPL	-40°C to +85°C	40 Pin PLASTIC
ICM7211AIPL	-40°C to +85°C	40 Pin PLASTIC
ICM7211AMIPL	-40°C to +85°C	40 Pin PLASTIC
ICM7211MIPL	-40°C to +85°C	40 Pin PLASTIC
ICM7211MIJL	-40°C to +85°C	40 Pin CERDIP
ICM7211AEV/KIT	—	EVALUATION KIT
ICM7212/D	—	DICE

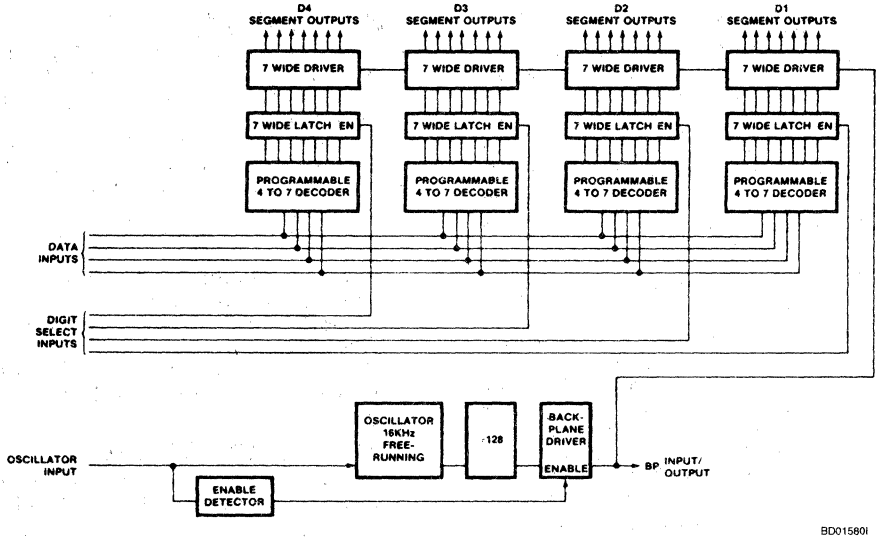
PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7212A/D	—	DICE
ICM7212AIJL	-40°C to +85°C	40 Pin CERDIP
ICM7212AIPL	-40°C to +85°C	40 Pin PLASTIC
ICM7212AM/D	—	DICE
ICM7212AMIJL	-40°C to +85°C	40 Pin CERDIP
ICM7212IJL	-40°C to +85°C	40 Pin CERDIP
ICM7212IPL	-40°C to +85°C	40 Pin PLASTIC
ICM7212MIJL	-40°C to +85°C	40 Pin CERDIP
ICM7212MIPL	-40°C to +85°C	40 Pin PLASTIC
ICM7212AMIPL	-40°C to +85°C	40 Pin PLASTIC
ICM7212AEV/KIT	—	EVALUATION KIT

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7211/12

INTERSIL

ICM7211 (A)



ICM7212 (A)

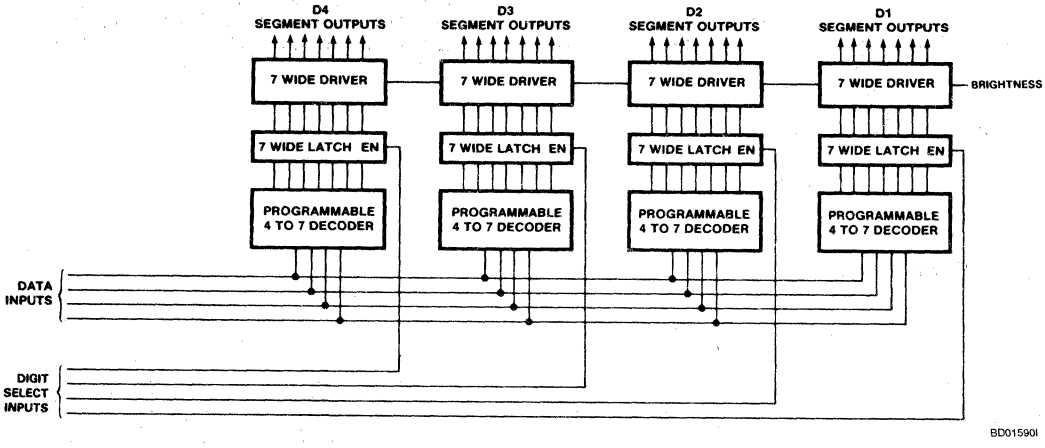
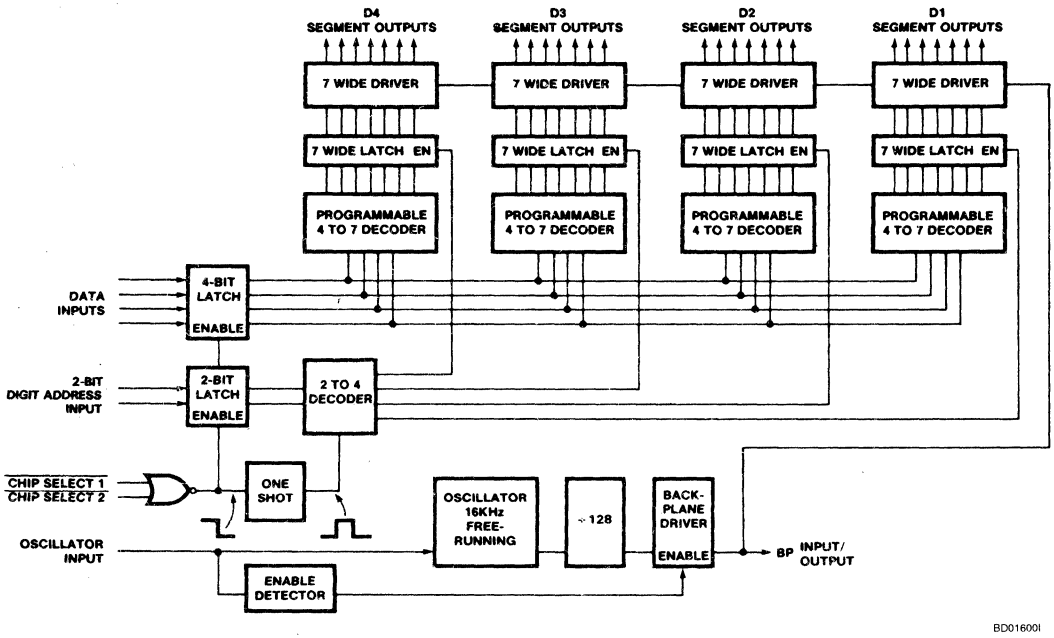


Figure 1: Functional Diagrams

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7211(A)M



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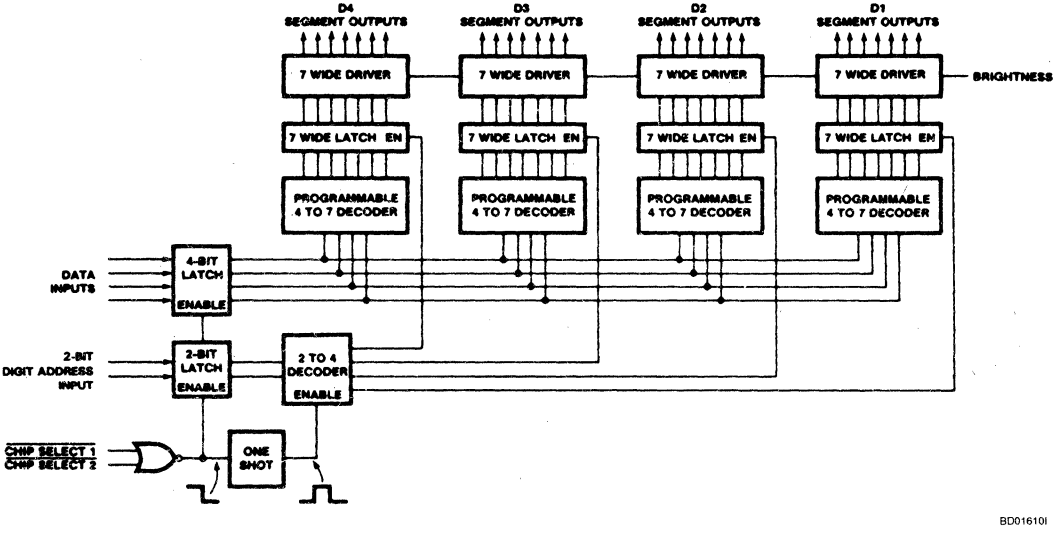
ICM7212(A)M



BD01610I

Figure 1: Functional Diagrams (Cont.)

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7211/12

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 0.5W@70°C
Supply Voltage ($V_{DD} - V_{SS}$) 6.5V
Input Voltage (Any Terminal) (Note 2) .....
V_{SS} − 0.3V to V_{DD} + 0.3V

Operating Temperature Range ..... −40°C to +85°C
Storage Temperature Range ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE 1: This limit refers to that of the package and will not be realized during normal operation.

NOTE 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7211/ICM7212 be turned on first.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

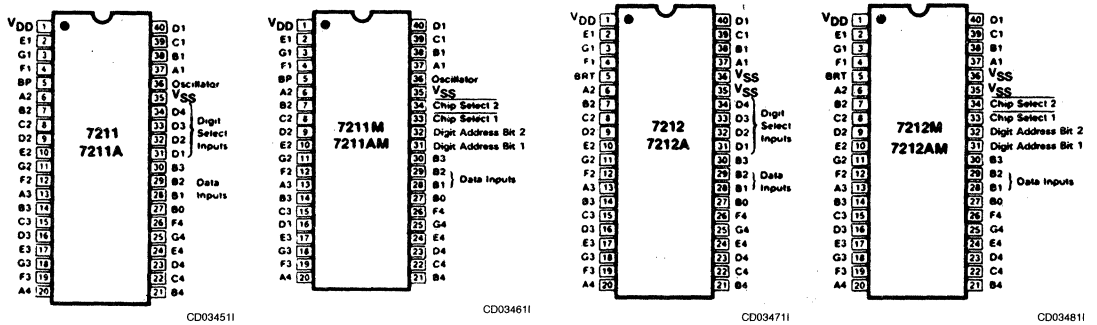


Figure 2: Pin Configurations (Outline Drawing PL)

ELECTRICAL CHARACTERISTICS

ICM7211 CHARACTERISTICS (LCD) V_{DD} = 5V ±10%, T_A = 25°C, V_{SS} = 0V unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SUPPLY}	Operating Supply Voltage Range ($V_{DD} - V_{SS}$)		3	5	6	V
I_{DD}	Operating Current	Test circuit, Display blank		10	50	µA
I_{OSCI}	Oscillator Input Current	Pin 36		±2	±10	
t_R, t_F	Segment Rise/Fall Time	C_L = 200pF		0.5		µs
t_R, t_F	Backplane Rise/Fall Time	C_L = 5000pF		1.5		
f_{OSC}	Oscillator Frequency	Pin 36 Floating		19		kHz
f_{BP}	Backplane Frequency	Pin 36 Floating		150		Hz

ICM7212 CHARACTERISTICS (COMMON ANODE LED)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SUPPLY}	Operating Supply Voltage Range ($V_{DD} - V_{SS}$)		4	5	6	V
I_{STBY}	Operating Current Display Off	Pin 5 (Brightness), Pins 27–34 — V_{SS}		10	50	µA
I_{DD}	Operating Current	Pin 5 at V_{DD}, Display all 8's		200		mA
I_{SLK}	Segment Leakage Current	Segment Off		±0.01	±1	µA
I_{SEG}	Segment On Current	Segment On, V_O = +3V	5	8		mA

Note: All typical values have been guaranteed by characterization and are not tested.

INPUT CHARACTERISTICS (ICM7211 AND ICM7212)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Logical "1" input voltage		4			V
V_{IL}	Logical "0" input voltage				1	
I_{ILK}	Input leakage current	Pins 27–34		±.01	±1	μA
C_{IN}	Input capacitance	Pins 27–34		5		pF
I_{BPLK}	BP/Brightness input leakage	Measured at Pin 5 with Pin 36 at V_{SS}		±.01	±1	μA
C_{BPI}	BP/Brightness input capacitance	All Devices		200		pF
AC CHARACTERISTICS — MULTIPLEXED INPUT CONFIGURATION						
t_{WH}	Digit Select Active Pulse Width	Refer to Timing Diagrams	1			μs
t_{DS}	Data Setup Time		500			ns
t_{DH}	Data Hold Time		200			
t_{IDS}	Inter-Digit Select Time		2			μs
AC CHARACTERISTICS — MICROPROCESSOR INTERFACE						
t_{WL}	Chip Select Active Pulse Width	other Chip Select either held active, or both driven together	200			ns
t_{DS}	Data Setup Time		100			
t_{DH}	Data Hold Time		10	0		
t_{ICS}	Inter-Chip Select Time		2			μs

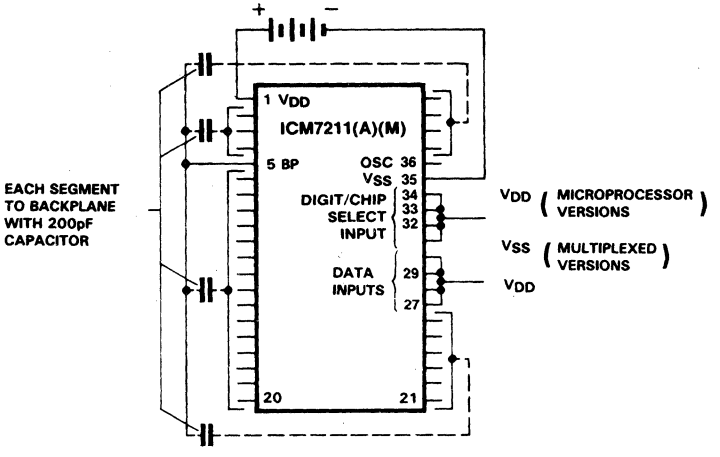


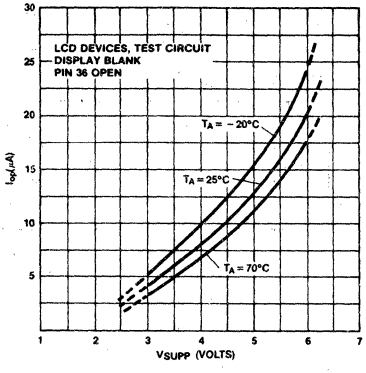
Figure 3: Test Circuits

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7211/12

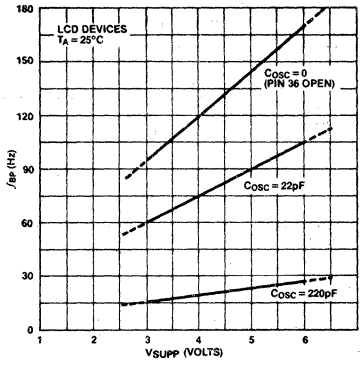
TYPICAL PERFORMANCE CHARACTERISTICS

ICM7211 OPERATING SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



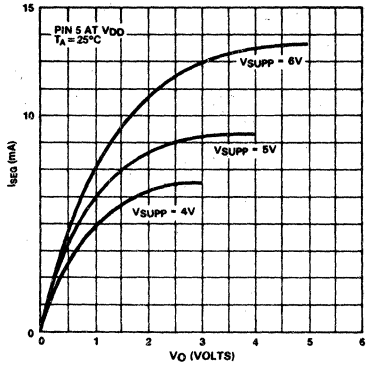
OP06100I

ICM7211 BACKPLANE FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



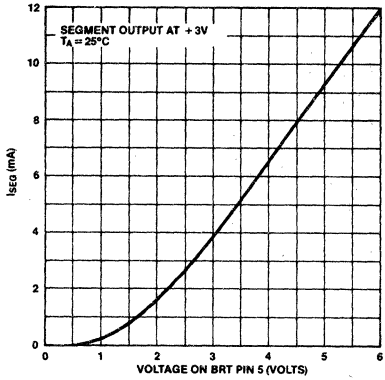
OP06110I

ICM7212 LED SEGMENT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



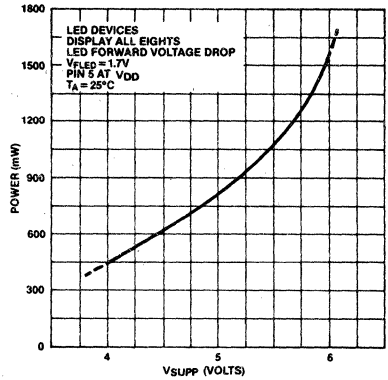
OP06121I

ICM7212 LED SEGMENT CURRENT AS A FUNCTION OF BRIGHTNESS CONTROL VOLTAGE



OP06130I

ICM7212 OPERATING POWER (LED DISPLAY) AS A FUNCTION OF SUPPLY VOLTAGE



OP06140I

INPUT DEFINITIONS

In this table, V_{DD} and V_{SS} are considered to be normal operating input logic levels. Actual input low and high levels are specified under Operating Characteristics. For lowest power consumption, input signals should swing over the full supply.

INPUT	TERMINAL	TEST CONDITIONS	FUNCTION	
B0	27	V_{DD} = Logical One V_{SS} = Logical Zero	Ones (Least Significant)	Data Input Bits
B1	28	V_{DD} = Logical One V_{SS} = Logical Zero	Twos	
B2	29	V_{DD} = Logical One V_{SS} = Logical Zero	Fours	
B3	30	V_{DD} = Logical One V_{SS} = Logical Zero	Eights (Most significant)	
OSC (LCD Devices Only)	36	Floating or with external capacitor to V_{DD} V_{SS}	Oscillator input Disables BP output devices, allowing segments to be synchronized to an external signal input at the BP terminal (Pin 5)	

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7211/ICM7212 MULTIPLEXED-BINARY INPUT CONFIGURATION

INPUT	TERMINAL	TEST CONDITIONS	FUNCTION
D1	31	V_{DD} = Active V_{SS} = Inactive	D1 Digit Select (Least significant)
D2	32		D2 Digit Select
D3	33		D3 Digit Select
D4	34		D4 Digit Select (Most significant)

ICM7211M/ICM7212M MICROPROCESSOR INTERFACE INPUT CONFIGURATION

INPUT	DESCRIPTION	TERMINAL	TEST CONDITIONS	FUNCTION
DA1	Digit Address Bit 1 (LSB)	31	V_{DD} = Logical One V_{SS} = Logical Zero	DA1 & DA2 serve as a two bit Digit Address Input DA2, DA1 = 00 selects D4 DA2, DA1 = 01 selects D3 DA2, DA1 = 10 selects D2 DA2, DA1 = 11 selects D1
DA2	Digit Address Bit 2 (MSB)	32		
$\overline{CS1}$	Chip Select 1	33	V_{DD} = Inactive V_{SS} = Active	When **both** $\overline{CS1}$ and $\overline{CS2}$ are taken low, the data at the Data and Digit Select code inputs are written into the input latches. On the rising edge of **either** $\overline{Chip\ Select}$, the data is decoded and written into the output latches.
$\overline{CS2}$	Chip Select 2	34		

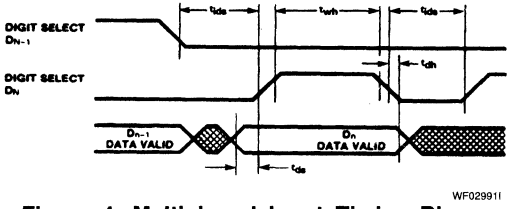


Figure 4: Multiplexed Input Timing Diagram

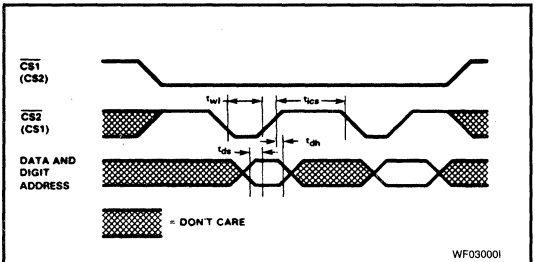


Figure 5: Microprocessor Interface Input Timing Diagram

DESCRIPTION OF OPERATION

LCD DEVICES

The LCD devices in the family (ICM7211, 7211A, 7211M, 7211AM) provide outputs suitable for driving conventional four-digit, seven-segment LCD displays. These devices include 28 individual segment drivers, backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency.

The segment and backplane drivers each consist of a CMOS inverter, with the n- and p-channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any DC component, which could arise from differing rise and fall times, and ensures maximum display life.

The backplane output devices can be disabled by connecting the OSCillator input (pin 36) to V_{SS}. This allows the 28 segment outputs to be synchronized directly to a signal input at the BP terminal (pin 5). In this manner, several slave devices may be cascaded to the backplane output of one master device, or the backplane may be derived from an external source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device represents a load of approximately 200pF (comparable to one additional segment). Thus the limitation of the number of devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits. A good rule of thumb to observe in order to minimize power consumption is to keep the backplane rise and fall times less than about 5 microseconds. The backplane output driver should handle the backplane to a display of 16 one-half-inch characters. It is recommended that if more than four devices are to be slaved together, that the backplane signal be derived externally and all the ICM7211 devices be slaved to it. This external signal should be capable of driving very large capacitive loads with short (1-2μs) rise and fall times. The maximum frequency for a backplane signal should be about 150Hz although this may be too fast for optimum display response at lower display temperatures, depending on the display used.

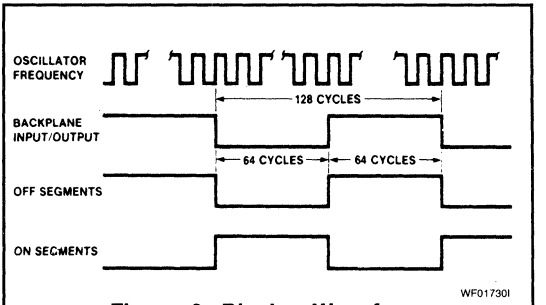


Figure 6: Display Waveforms

The onboard oscillator is designed to free run at approximately 19kHz at microampere power levels. The oscillator

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7211/12

frequency is divided by 128 to provide the backplane frequency, which will be approximately 150Hz with the oscillator free-running; the oscillator frequency may be reduced by connecting an external capacitor between the OSCillator terminal and V_{DD}.

The oscillator may also be overdriven if desired, although care must be taken to ensure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a D.C. component to the display). This can be done by driving the OSCillator input between the positive supply and a level out of the range where the backplane disable is sensed (about one fifth of the supply voltage above V_{SS}). Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

LED DEVICES

The LED devices in the family (ICM7212, 7212A, 7212M, 7212AM) provide outputs suitable for directly driving four-digit, seven-segment common-anode LED displays. These devices include 28 individual segment drivers, each consisting of a low-leakage, current-controlled, open-drain, n-channel transistor.

The drain current of these transistors can be controlled by varying the voltage at the BRighTness input (pin 5). The voltage at this pin is transferred to the gates of the output devices for "on" segments, and thus directly modulates the transistor's "on" resistance. A brightness control can be easily implemented with a single potentiometer controlling the voltage at pin 5, connected as in Figure 7. The potentiometer should be a high value (100KΩ to 1MΩ) to minimize power consumption, which can be significant when the display is off.

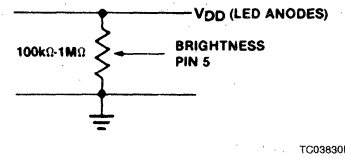
The BRighTness input may also be operated digitally as a display enable; when high, the display is fully on, and low fully off. The display brightness may also be controlled by varying the duty cycle of a signal swinging between the two voltages at the BRighTness input.

Note that the LED devices have two connections for V_{SS}; both of these pins should be connected. The double connection is necessary to minimize effects of bond wire resistance with the large total display currents possible.

When operating LED devices at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperatures. The maximum power dissipation is 1 watt at 25°C, derated linearly above 35°C to 500mW at 70°C (−15mW/°C above 35°C). Power dissipation for the device is given by:

$$P = (V_{SUPP} - V_{FLED})(I_{SEG})(n_{SEG})$$

where V_{FLED} is the LED forward voltage drop, I_{SEG} is segment current, and n_{SEG} is the number of "on" segments. It is recommended that if the device is to be operated at elevated temperatures the segment current be limited by use of the BRighTness input to keep power dissipation within the limits described above.



TC03830I

Figure 7: Brightness control

INPUT CONFIGURATIONS AND OUTPUT CODES

The standard devices in the ICM7211/12 family accept a four-bit true binary (ie, positive level = logical one) input at pins 27 thru 30, least significant bit at pin 27 ascending to the most significant bit at pin 30. The ICM7211, ICM7211M, ICM7212, and ICM7212M devices decode this binary input into a seven-segment alphanumeric hexadecimal output, while the ICM7211A, ICM7211AM, ICM7212A, and ICM7212AM decode the binary input into the same seven-segment output as in the ICM7218 "Code B", ie 0-9, dash, E. H, L, P, blank. These codes are shown explicitly in Table 1. Either decoder option will correctly decode true BCD to a seven-segment decimal output.

TABLE 1: Output Codes

BINARY				HEXADECIMAL ICM7235 ICM7235M	CODE B ICM7235A ICM7235AM
B3	B2	B1	B0		
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	(BLANK)

TB00070I

These devices are actually mask-programmable to provide any 16 combinations of the seven segment outputs decoded from the four input bits. For large quantity orders custom decoder options can be arranged. Contact the factory for details.

The ICM7211, ICM7211A, ICM7212, and ICM7212A devices are designed to accept multiplexed binary or BCD input. These devices provide four separate digit lines (least significant digit at pin 31 ascending to most significant digit at pin 34), each of which when taken to a positive level

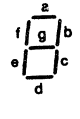
Note: All typical values have been guaranteed by characterization and are not tested.

decodes and stores in the output latches of its respective digit the character corresponding to the data at the input port, pins 27 through 30.

The ICM7211M, ICM7211AM, ICM7212M, and ICM7212AM devices are intended to accept data from a data bus under processor control.

In these devices, the four data input bits and the two-bit digit address (DA1 pin 31, DA2 pin 32) are written into input buffer latches when both chip select inputs ($\overline{CS1}$ pin 33, $\overline{CS2}$ pin 34) are taken low. On the rising edge of either chip select input, the content of the data input latches is decoded and stored in the output latches of the digit selected by the contents of the digit address latches.

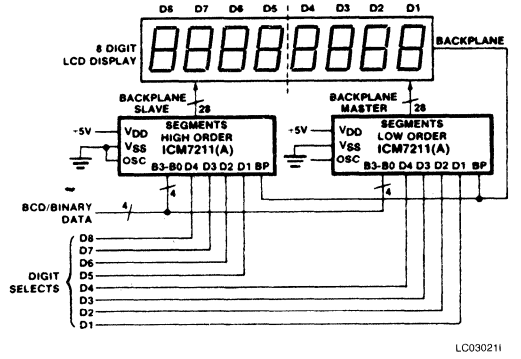
An address of 00 writes into D4, DA2 = 0, DA1 = 1 writes into D3, DA2 = 1, DA1 = 0 writes into D2, and 11 writes into D1. The timing relationships for inputting data are shown in Figure 5, and the chip select pulse widths and data setup and hold times are specified under Operating Characteristics.



LC01940I

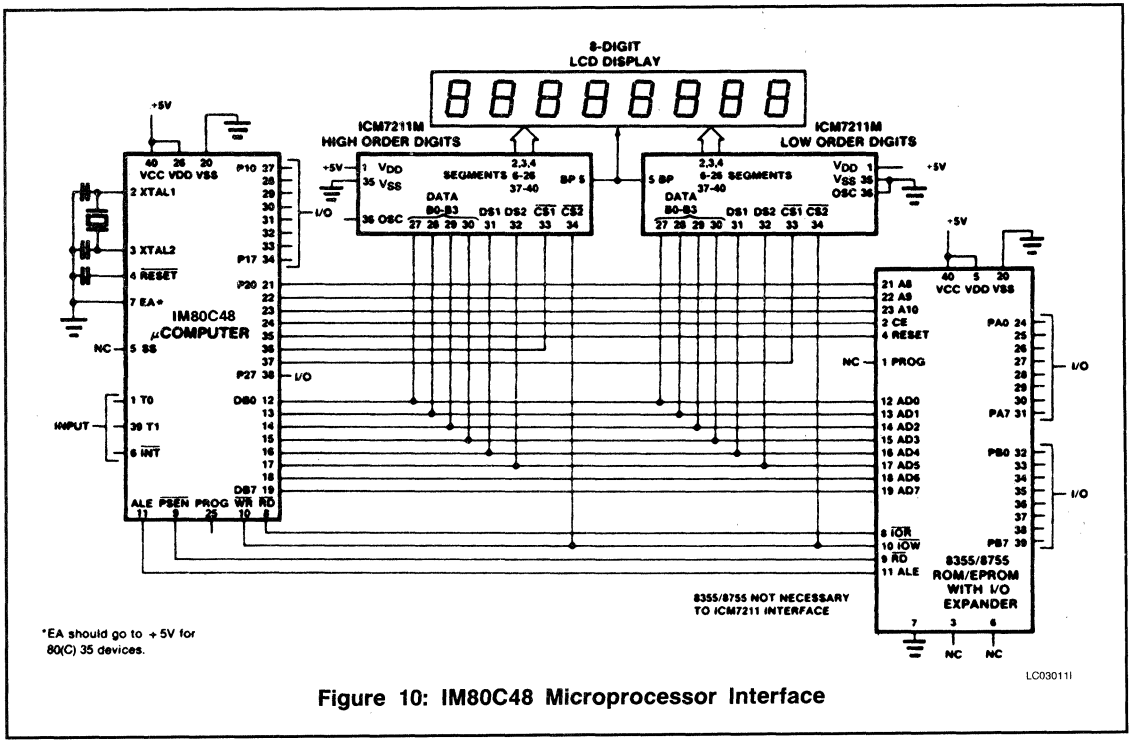
Figure 8: Segment Assignment

APPLICATIONS



LC03021I

Figure 9: Ganged ICM7211's Driving 8-Digit LCD Display



LC03011I

Figure 10: IM80C48 Microprocessor Interface

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7218
8-Digit LED Multiplexed Display Driver

INTERSIL

GENERAL DESCRIPTION

The ICM7218 series of universal LED driver systems provide, in a single package, all the circuitry necessary to interface most common microprocessors or digital systems to an LED display. Included on chip are an 8-byte static display memory, 2 types of 7-segment decoders, multiplex scan circuitry, and high current digit and segment drivers for either common-cathode or common-anode displays.

The ICM7218A and ICM7218B feature 2 control lines ($\overline{\text{WRITE}}$ and MODE) which write either 4 bits of control information (DATA COMING, $\overline{\text{SHUTDOWN}}$,$\overline{\text{DECODE}}$, and HEXA/$\overline{\text{CODE B}}$) or 8 bits of display input data. Display data is automatically sequenced into the 8-byte internal memory on successive positive going $\overline{\text{WRITE}}$ pulses. Data may be displayed either directly or decoded in Hexadecimal or Code B formats.

The ICM7218C and ICM7218D feature 2 control lines ($\overline{\text{WRITE}}$ and HEXA/CODE B/$\overline{\text{SHUTDOWN}}$), 4 separate display data input lines, and 3 digit address lines. Display data is written into the internal memory by setting up a digit address and strobing the $\overline{\text{WRITE}}$ line low. Only Hexadecimal and Code B formats are available for display outputs.

The ICM7218E provides 4 input lines for control information ($\overline{\text{WRITE}}$, HEXA/CODE B, $\overline{\text{DECODE}}$ and $\overline{\text{SHUTDOWN}}$), 8 separate display data input lines, and 3 digit address lines. Display data is written into the internal memory by setting up a digit address and strobing the $\overline{\text{WRITE}}$ line. Data may be displayed either directly or decoded in Hexadecimal or Code B formats.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7218AIJI	-40°C to +85°C	28-PIN CERDIP
ICM7218A/D	—	DICE
ICM7218B/D	—	DICE
ICM7218BIJI	-40°C to +85°C	28-PIN CERDIP
ICM7218CIJI	-40°C to +85°C	28-PIN CERDIP
ICM7218C/D	—	DICE
ICM7218DIJI	-40°C to +85°C	28-PIN CERDIP
ICM7218D/D	—	DICE
ICM7218EIJL	-40°C to +85°C	40-PIN CERDIP
ICM7218E/D	—	DICE

FEATURES

- **Microprocessor Compatible — C, D, E Versions**
- **Total Circuit Integration On Chip Includes:**
  - **a) Digit and Segment Drivers**
  - **b) All Multiplex Scan Circuitry**
  - **c) 8 Byte Static Display Memory**
  - **d) 7 Segment Hexadecimal and Code B Decoders (Pin Selectable)**
- **Output Drive Suitable for Large LED Displays**
- **Common Anode and Common Cathode Versions**
- **Single 5 Volt Supply Required**
- **Data Retention to 2 Volts Supply**
- **Shutdown Feature — Turns Off Display and Puts Chip Into Low Power Dissipation Mode**
- **Sequential and Random Access Versions**
- **Decimal Point Drive On Each Digit**

Note: All typical values have been guaranteed by characterization and are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD} - V_{SS}$) 6V
Digit Output Current 300mA
Segment Output Current 50mA
Input Voltage
(any terminal) ..... V_{SS} −0.3V to V_{DD} + 0.3V
(Note 1)

Power Dissipation (28 Pin CERDIP)..... 1 W (Note 2)
Power Dissipation (40 Pin CERDIP)..... 1 W (Note 2)
Operating Temperature Range ..... −40°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason it is recommended that no inputs from sources operating on a different power supply be applied to the device before its own supply is established, and when using multiple supply systems the supply to the ICM7218 should be turned on first.

NOTE 2: These limits refer to the package and will not be obtained during normal operation. Derate above 50°C by 25mW per °C.

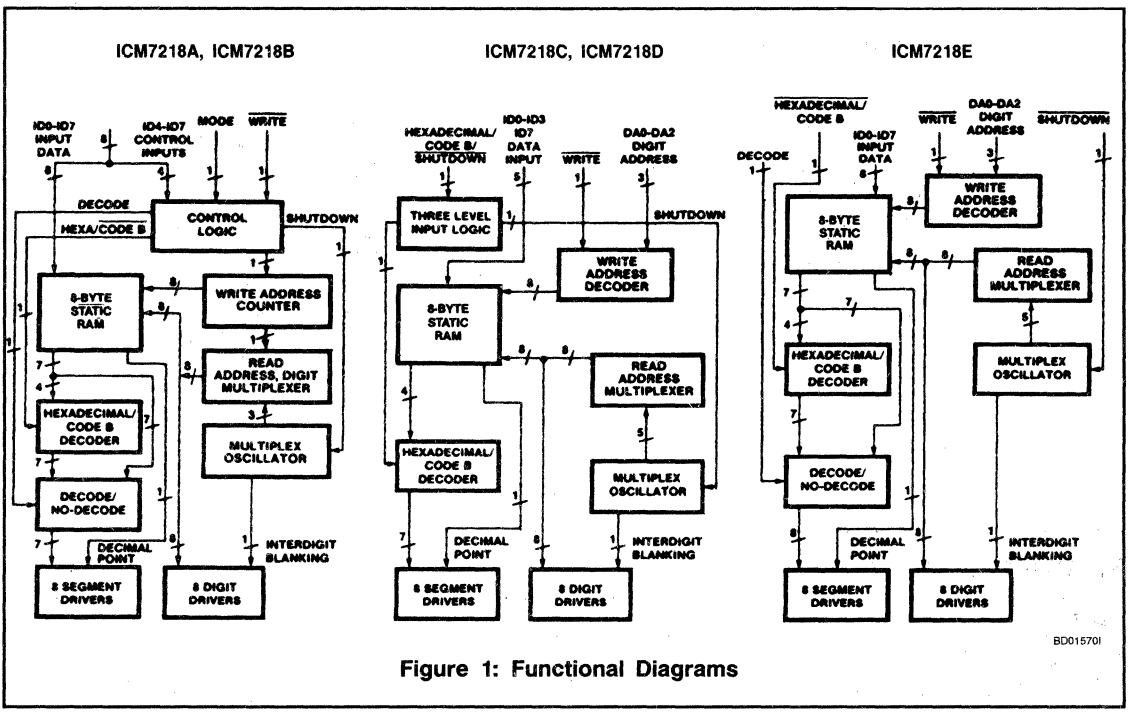
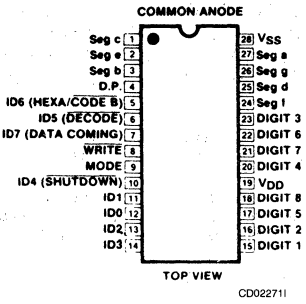


Figure 1: Functional Diagrams

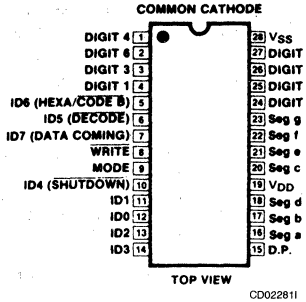
Note: All typical values have been guaranteed by characterization and are not tested.

ICM7218A*
(OUTLINE DWG JI)



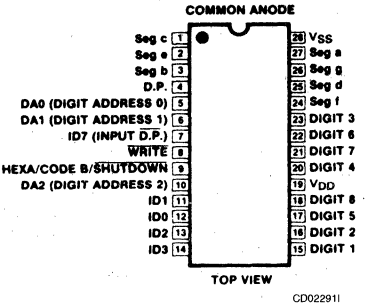
CD022711

ICM7218B*
(OUTLINE DRAWING JI)



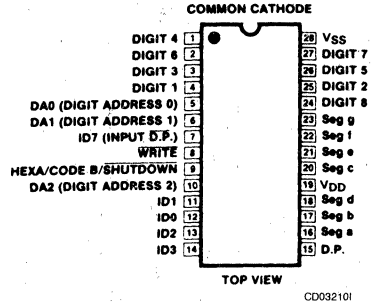
CD022811

ICM7218C
(OUTLINE DRAWING JI)



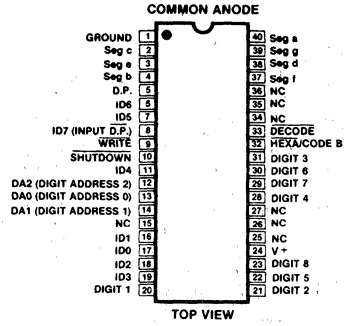
CD022911

ICM7218D
(OUTLINE DRAWING JI)



CD032101

ICM7218E*
(OUTLINE DRAWING DL)



CD032211

*** Note: Pins 5,6,7,10 are under control of Mode pin 9.**

Figure 2: Pin Configurations

ELECTRICAL CHARACTERISTICS V_{DD} = 5V, V_{SS} = 0V, T_A = 25°C, Display Diode drop = 1.7V

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SUPPLY}	Supply Voltage Range	Operating Power Down Mode	4 2		6 6	V V
I_Q	Quiescent Supply Current	Shutdown (Note 3)	6	10	300	µA
I_{DD}	Operating Supply Current	Common Anode SEGS On SEGS Off Common Cathode SEGS On SEGS Off Note 4 (Outputs Open Circuit)			2.5 500 700 250	mA µA µA µA
I_{DIG}	Digit Drive Current	Common Anode $V_{out} = V_{DD} - 2.0V$ Common Cathode $V_{out} = V_{SS} + 1.0V$	140 50	200 100		mA mA
I_{DLK}	Digit Leakage Current	Shutdown Mode Common Anode V_{out} = 2V Common Cathode V_{out} = 5V			100 100	µA µA
I_{SEG}	Peak Segment Drive Current	Common Anode $V_{out} = V_{SS} + 1.0V$ Common Cathode $V_{out} = V_{DD} - 2.0V$	20 −10	40 −20		mA mA
I_{SLK}	Segment Leakage Current	Shutdown Mode Common Anode $V_{out} = V_{DD}$ Common Cathode $V_{out} = V_{SS}$			100 100	µA µA
f_{MUX}	Display Scan Rate	Per Digit		250		Hz

Note: All typical values have been guaranteed by characterization and are not tested.

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Three Level Input: Pin 9 ICM7218C/D					
V_{IH}	Logical "1" Input Voltage	Hexadecimal	4.5			V
V_{IF}	Floating Input	Code B	2.0		3.0	V
V_{IL}	Logical "0" Input Voltage	Shutdown			0.4	V
Z_{IN}	Three Level Input Impedance	Note 3		100		kΩ
V_{IH}	Logical "1" Input Voltage		3.5			V
V_{IL}	Logical "0" Input Voltage				0.8	V
t_{WL}	Write Pulse Width (Low)	7218A, B	550	400		ns
t_{WL}	Write Pulse Width (Low)	7218C, D, E	400	250		ns
t_{MH}	Mode Hold Time	7218A, B	150			ns
t_{MS}	Mode Set Up Time	7218A, B	500			ns
t_{DS}	Data Set Up Time		500			ns
t_{DH}	Data Hold Time	7218 A,B	50			ns
		7218 C,D,E	125			ns
t_{AS}	Digit Address Set Up Time	ICM7218C, D, E	500			ns
t_{AH}	Digital Address Hold Time	ICM7218C, D, E	0			ns
Z_{IN}	Data Input Impedance	5-10 pF Gate Capacitance		10^{10}		Ohms

TABLE 1: INPUT DEFINITIONS ICM7218A and B

INPUT		TERMINAL	LOGIC LEVEL	FUNCTION
$\overline{\text{WRITE}}$		8	High Low	Input Not Loaded Into Memory Input Loaded Into Memory
MODE		9	High Low	Load Control bits on Write Pulse Load Input Data on Write Pulse
ID4 $\overline{\text{SHUTDOWN}}$	MODE High	10	High Low	Normal Operation Shutdown (Oscillator, Decoder and Display Disabled)
ID5 ($\overline{\text{DECODE}}$)	MODE High	6	High Low	No Decode Decode
ID6 (HEXA/$\overline{\text{CODE B}}$)	MODE High	5	High Low	Hexadecimal Decoding Code B Decoding
ID7 (DATA COMING)	MODE High	7	High Low	Data Coming No Data Coming } Control Word
ID0-ID7	MODE Low	11,12,13,14, 5,6,10,7		Display Data Inputs (Notes 4, 5)

TABLE 2: INPUT DEFINITIONS ICM7218C and D

INPUT	TERMINAL	LOGIC LEVEL	FUNCTION
$\overline{\text{WRITE}}$	8	High Low	Input Not Loaded Into Memory Input Loaded Into Memory
HEXA/CODE B/$\overline{\text{SHUTDOWN}}$	9 (Note 3)	High Floating Low	Hexadecimal Decoding Code B Decoding Shutdown (Oscillator, Decoder and Display Disabled)
DA0 – DA2	10,6,5		Digit Address Inputs
ID0 – ID3	14,13,11,12		Display Data Inputs
ID (INPUT $\overline{\text{D.P.}}$)	7		Decimal Point Input

NOTE 3: In the ICM7218C and D (random access versions) the HEXA/CODE B/$\overline{\text{SHUTDOWN}}$ Input (Pin 9) has internal biasing resistors to hold it at $V_{DD}/2$ when Pin 9 is open circuited. These resistors consume power and result in a quiescent supply current (I_Q) of typically 50μA. The ICM7218A, B, and E devices do not have these biasing resistors and thus are not subject to this condition.

NOTE 4: ID0-ID3 = Don't care when writing control data
ID4-ID6 = Don't care when writing Hex/Code B data
(The display blanks on ICM7218A/B versions when writing in data)

NOTE 5: In the No Decode format, "Ones" represents "on" segments for all inputs except for the Decimal Point, where "Zero" represents an "on" segment, (i.e. segments are positive true, decimal point is negative true).

NOTE 6: Common Anode segment drivers and Common Cathode Digit Drivers have 20kΩ pullup resistors.

Note: All typical values have been guaranteed by characterization and are not tested.

TABLE 3: INPUT DEFINITIONS ICM7218E

INPUT	TERMINAL	LOGIC LEVEL	FUNCTION
$\overline{\text{WRITE}}$	9	High Low	Input Latches Not Updated Input Latches Updated
$\overline{\text{SHUTDOWN}}$	10	High Low	Normal Operation Shutdown (Oscillator, Decoder and Displays Disabled)
$\overline{\text{DECODE}}$	33	High Low	No Decode Decode
$\overline{\text{HEXA}}$/CODE B	32	High Low	Code B Decoding Hexadecimal Decoding
DA0 – DA2 Digit Address (0,1,2)	13,14,12		Digit Address Inputs
ID0 – ID6 ID7 (INPUT $\overline{\text{D.P.}}$)	17,16,18,19,11,7,6 8		Display Data Inputs (Note 5) Display Data/Decimal Point Input

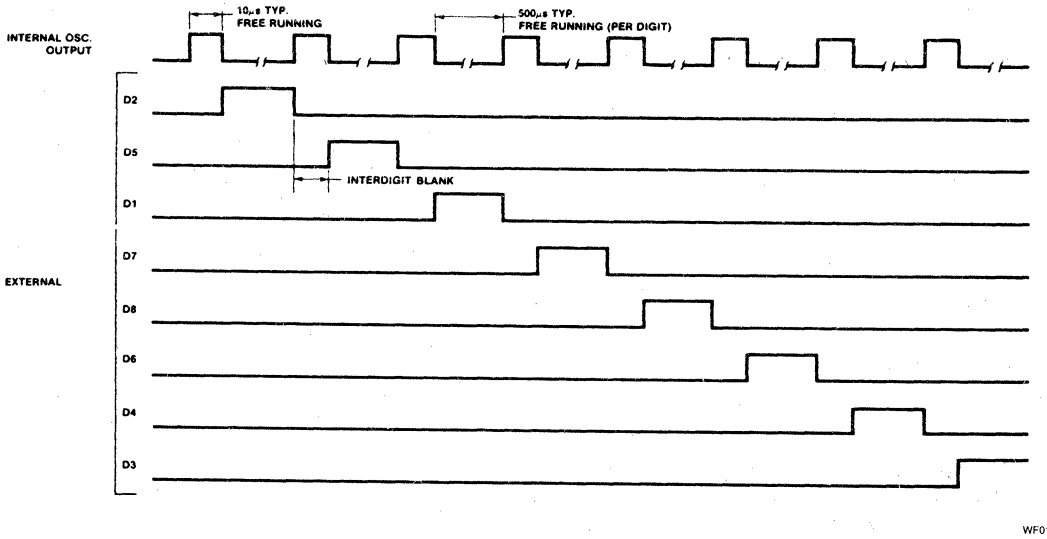


Figure 3: Multiplex Timing

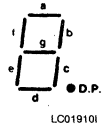


Figure 4: Segment Assignments

DETAILED DESCRIPTION

$\overline{\text{DECODE}}$ Operation

For the ICM7218A/B/E products, there are 3 input data formats possible; either direct segment and decimal point information (8 bits per digit) or two Binary code plus decimal point information (Hexadecimal/Code B formats with 5 bits per digit).

The 7 segment decoder on chip is disabled when direct segment information is to be written. In this format, the inputs directly control the outputs as follows:

Input Data: ID7 ID6 ID5 ID4 ID3 ID2 ID1 ID0

Output Segments: $\overline{\text{D.P.}}$ a b c e g f d

Here, "Ones" represent "on" segments for all inputs except the Decimal Point. For the Decimal Point "zero" represents an "on" segment.

HEXAdecimal/CODE B Decoding

For all products, a choice of either HEXA or Code B decoding may be made, HEXA decoding provides 7 segment numeric plus six alpha characters while Code B provides a negative sign (–), a blank (for leading zero blanking), certain useful alpha characters and all numeric formats.

The four bit binary code is set up on inputs ID3-ID0.

Note: All typical values have been guaranteed by characterization and are not tested.

Decimal	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
HEXA CODE	0 1 2 3 4 5 6 7 8 9 A b C d E F
CODE B	0 1 2 3 4 5 6 7 8 9 - E H L P (BLANK)

SHUTDOWN

SHUTDOWN performs several functions: it puts the device into a very low dissipation mode (typically 10μA at V_{DD} = 5V), turns off both the digit and segment drivers, and stops the multiplex scan oscillator (this is the only way the scan oscillator can be disabled). However, it is still possible to input data to the memory during shutdown — only the display output sections of the device are disabled in this mode.

Powerdown

In the Shutdown Mode, the supply voltage may be reduced to 2 volts without data in memory being lost. However, data should not be written into memory if the supply voltage is less than 4 volts.

Output Drive

The common anode output drive is approximately 200 mA per digit at a 12% duty cycle. With segment peak drive current of 40mA typically, this results in 5mA average drive. The common cathode drive capability is approximately one half that of the common anode drive. If high impedance LED displays are used, the drive current will be correspondingly less.

Inter Digit Blanking

A blanking time of approximately 10μs occurs between digit strobes. This ensures that the segment information is correct before the next digit drive, thereby avoiding display ghosting.

Driving Larger Displays

If a higher average drive current per digit is required, it is possible to connect digit drive outputs together. For example, by paralleling pairs of digit drives together to drive a 4 digit display, 5mA average segment drive current can be obtained.

Power Dissipation Considerations

Assuming common anode drive at V_{DD} = 5 volts and all digits on with an average of 5 segments driven per digit, the average current would be approximately 200mA. Assuming a 1.8 volt drop across the LED display, there will be a 3.2 volt drop across the ICM7218. The device power dissipation will therefore be 640mW, rising to about 900mW, for all '8' 's displayed. **Caution: Position device in system such that air can flow freely to provide maximum cooling. The common cathode dissipation is approximately one half that of the common anode dissipation.**

Sequential Addressing Considerations (ICM7218A/B)

The control instructions are read from the input bus lines if MODE is high and WRITE low. The instructions occur on 4 lines and are — DECODE/no Decode, type of Decode (if desired), SHUTDOWN/no Shutdown and DATA COMING/not Coming. After the control word has been written (with the Data Coming instruction), display data can be written into memory with each successive negative going WRITE pulse. After all 8 digit memory locations have been written to, additional transitions of the WRITE input are ignored until a new control word is written. It is not possible to change one individual digit without refreshing the data for all the other digits.

Random Access Input Drive Considerations (ICM7218C/D/E)

Control instructions are provided to the ICM7218C/D by a single three level input terminal (Pin 9), which operates independently of the WRITE pulse. The ICM7218E control instructions are also independent but are on three separate pins (10, 32, 33).

Data can be written into memory on the ICM7218C/D/E by setting up a 3 bit binary code (one of eight) on the digit address inputs and applying a low level to the WRITE pin. For example, it is possible to change only digit 7 without altering the data for the other digits. (See Figure 7).

Supply Capacitor

A 0.1μF capacitor is recommended between V_{DD} and V_{SS} to bypass multiplex noise.

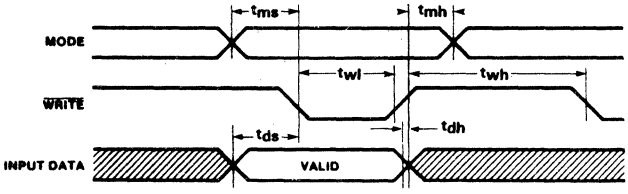


Figure 5: Timing Diagram for ICM7218A/B

Note: All typical values have been guaranteed by characterization and are not tested.

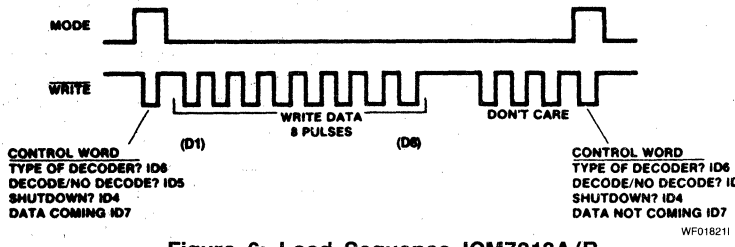


Figure 6: Load Sequence ICM7218A/B

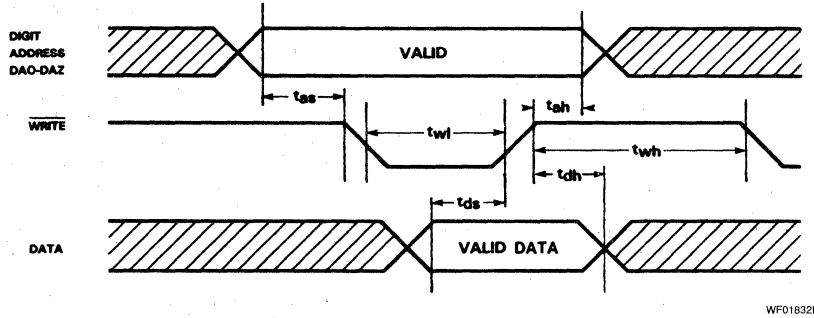


Figure 7: Timing Diagram for ICM7218C/D/E

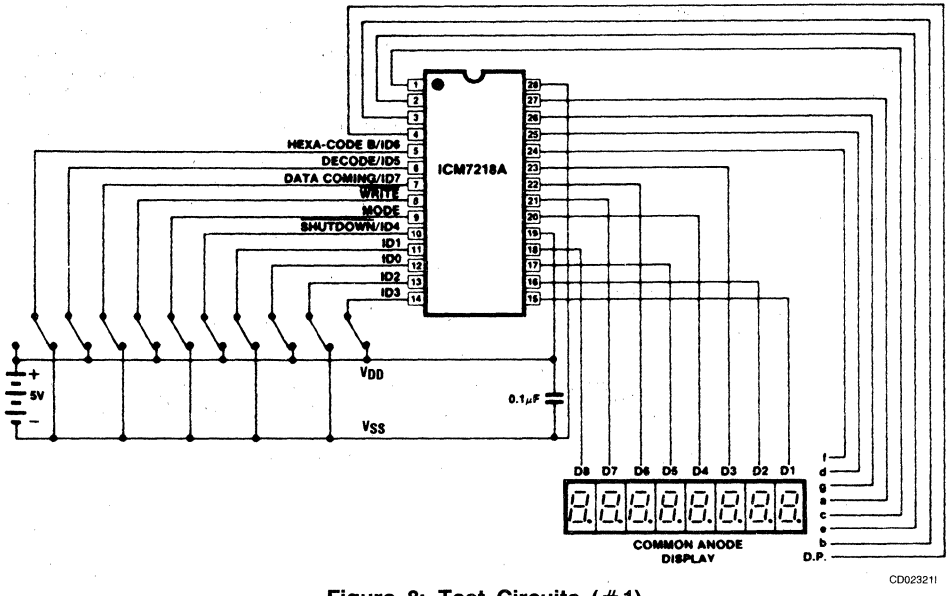


Figure 8: Test Circuits (#1)

Note: All typical values have been guaranteed by characterization and are not tested.

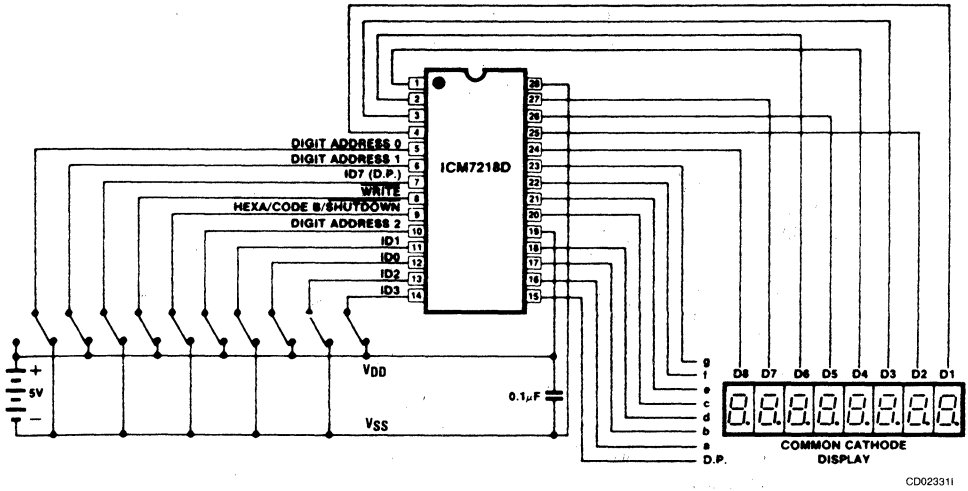
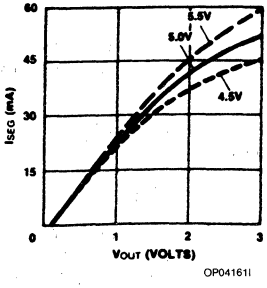


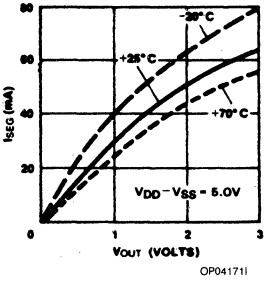
Figure 9: Test Circuits (#2)

TYPICAL PERFORMANCE CHARACTERISTICS

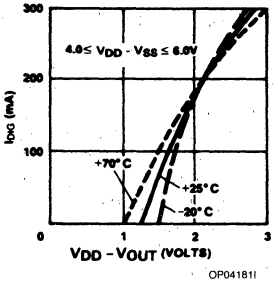
COMMON ANODE SEG. DRIVER I_{SEG} vs. V_{OUT} AT 25°C



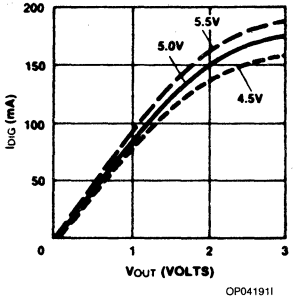
COMMON ANODE SEG. DRIVER I_{SEG} vs. V_{OUT}



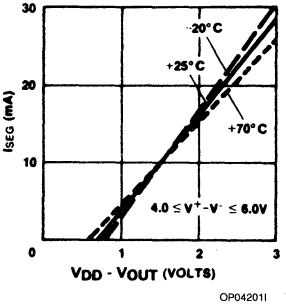
COMMON ANODE DIGIT DRIVER I_{DIG} vs. (V_{DD} - V_{OUT})



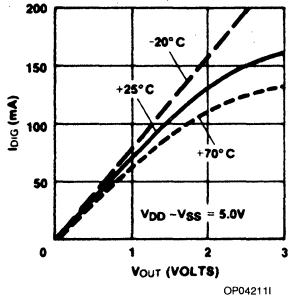
COMMON CATHODE DIGIT DRIVER I_{DIG} vs. V_{OUT} AT 25°C



COMMON CATHODE SEG. DRIVER I_{SEG} vs. (V_{DD} - V_{OUT})



COMMON CATHODE DIGIT DRIVER I_{DIG} vs. V_{OUT}



Note: All typical values have been guaranteed by characterization and are not tested.

ICM7218

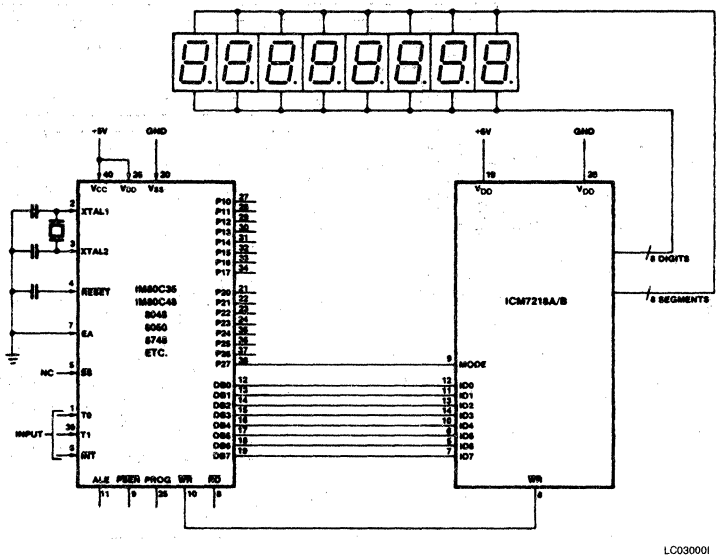


Figure 10: 8 Digit Microprocessor Display

APPLICATION EXAMPLES

8 DIGIT MICROPROCESSOR DISPLAY APPLICATION

Figure 10 shows a display interface using the ICM7218A/B with an 8048 family microcontroller. The 8 bit data bus (DB0/DB7-ID0/ID7) transfers control and data information to the 7218 display interface on successive $\overline{\text{WRITE}}$ pulses. The MODE input to the 7218 is connected to one of the I/O port pins on the microcontroller. When MODE is high a control word is transferred; when MODE is low data is transfered. Sequential locations in the 8-byte static memory are automatically loaded on each successive $\overline{\text{WRITE}}$ pulse. After eight $\overline{\text{WRITE}}$ pulses have occurred, further pulses are ignored until a new control word is transferred. (See Figure 6). This also allows writing to other peripheral devices without disturbing the ICM7218A/B.

16 DIGIT MICROPROCESSOR DISPLAY

In this application (see Figure 11), both ICM7218's are addressed simultaneously with a 3 bit word, DA2-DA0. Display data from the 8048 I/O bus (DB7-DB0) is transferred to both ICM7218's simultaneously.

The display digits from both ICM7218's are interleaved to allow adjacent pairs of digits to be loaded simultaneously from a single 8 bit data bus.

Decimal point information is supplied to the ICM7218's from the processor on port lines P26 and P27.

NO DECODE APPLICATION

The ICM7218 can also be used as a microprocessor based LED status panel driver. The microprocessor selected control word must include "No Decode" and "Data Coming". The processor writes "Ones" and "Zeroes" into the ICM7218 which in turn directly drives appropriate discrete LEDs. LED indicators can be red or green (8 segments x 8 digits = 64 dots ÷2 per red or green = 32 channels).

Note: All typical values have been guaranteed by characterization and are not tested.

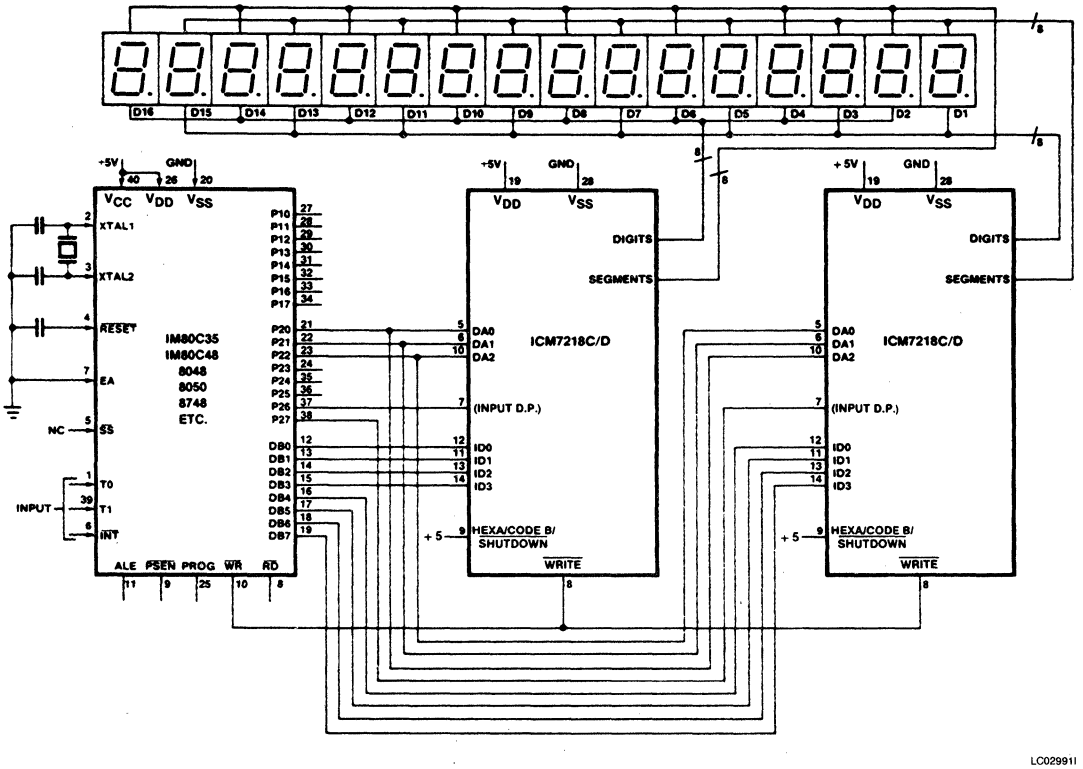


Figure 11: 16 Digit Display

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7231-ICM7234
Numeric/Alphanumeric Triplexed LCD Display Driver

INTERSIL

GENERAL DESCRIPTION

The ICM7231-7234 family of integrated circuits are designed to generate the voltage levels and switching waveforms required to drive triplexed liquid-crystal displays. These chips also include input buffer and digit address decoding circuitry and contain a mask-programmed ROM allowing six bits of input data to be decoded into 64 independent combinations of the output segments of the selected digit.

The family is designed to interface to modern high performance microprocessors and microcomputers and ease system requirements for ROM space and CPU time needed to service a display.

FEATURES

- **ICM7231: Drives 8 Digits of 7 Segments With Two Independent Annunciators Per Digit Address and Data Input in Parallel Format**
- **ICM7232: Drives 10 Digits of 7 Segments With Two Independent Annunciators Per Digit Address and Data Input in Serial Format**
- **ICM7233: Drives 4 Characters of 18 Segments Address and Data Input in Parallel Format**
- **ICM7234: Drives 5 Characters of 18 Segments Address and Data Input in Serial Format**
- **All Signals Required to Drive Rows and Columns of Triplexed LCD Display Are Provided**
- **Display Voltage Independent of Power Supply**
- **On-Chip Oscillator Provides All Display Timing**
- **Total Power Consumption Typically 200μW, Maximum 500μW at 5V**
- **Low-Power Shutdown Mode Retains Data With 5μW Typical Power Consumption at 5V, 1μW at 2V**
- **Direct Interface to High-Speed Microprocessors**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7231AFIJL	−25°C to +85°C	40 pin CERDIP
ICM7231AFIPL	−25°C to +85°C	40 pin PLASTIC Dip
ICM7231BFIJL	−25°C to +85°C	40 pin CERDIP
ICM7231BFIPL	−25°C to +85°C	40 pin PLASTIC Dip
ICM7231CFIJL	−25°C to +85°C	40 pin CERDIP
ICM7231CFIPL	−25°C to +85°C	40 pin PLASTIC Dip
ICM7232AFIJL	−25°C to +85°C	40 pin CERDIP
ICM7232AFIPL	−25°C to +85°C	40 pin PLASTIC Dip
ICM7232BFIJL	−25°C to +85°C	40 pin CERDIP
ICM7232BFIPL	−25°C to +85°C	40 pin PLASTIC Dip

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7232CR/D	—	DICE
ICM7232CRIJL	−25°C to +85°C	40 pin CERDIP
ICM7232CRIPL	−25°C to +85°C	40 pin PLASTIC Dip
ICM7233AEV/KIT		Evaluiation Kit.
ICM7233AF/D	—	DICE
ICM7233AFIJL	−25°C to +85°C	40 pin CERDIP
ICM7233AFIPL	−25°C to +85°C	40 pin PLASTIC Dip
ICM7233AF/D	—	DICE
ICM7234AFIJL	−25°C to +85°C	40 pin CERDIP
ICM7234AFIPL	−25°C to +85°C	40 pin PLASTIC Dip

203299-002

Note: All typical values have been guaranteed by characterization and are not tested.

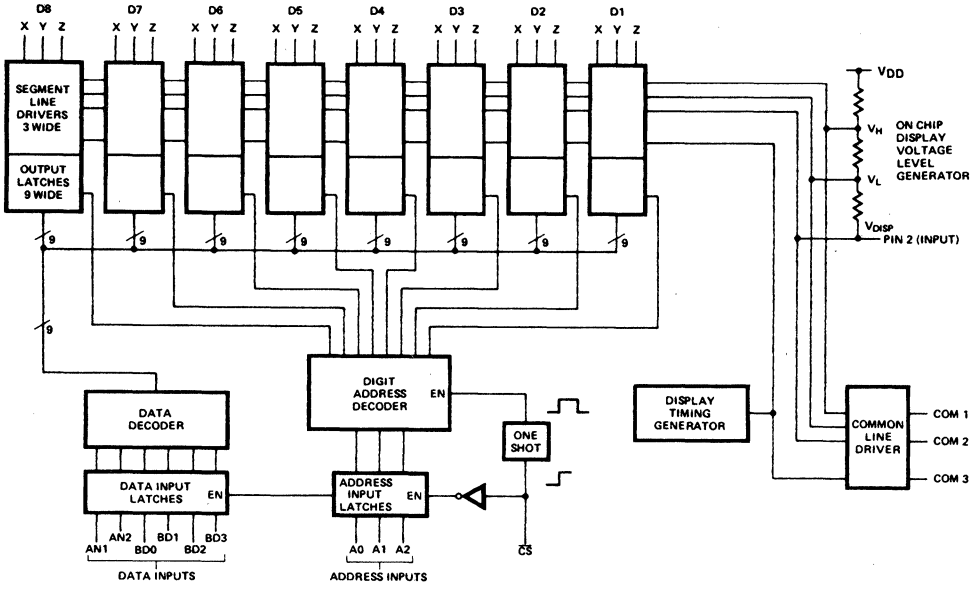


Figure 1: ICM7231 Functional Diagram

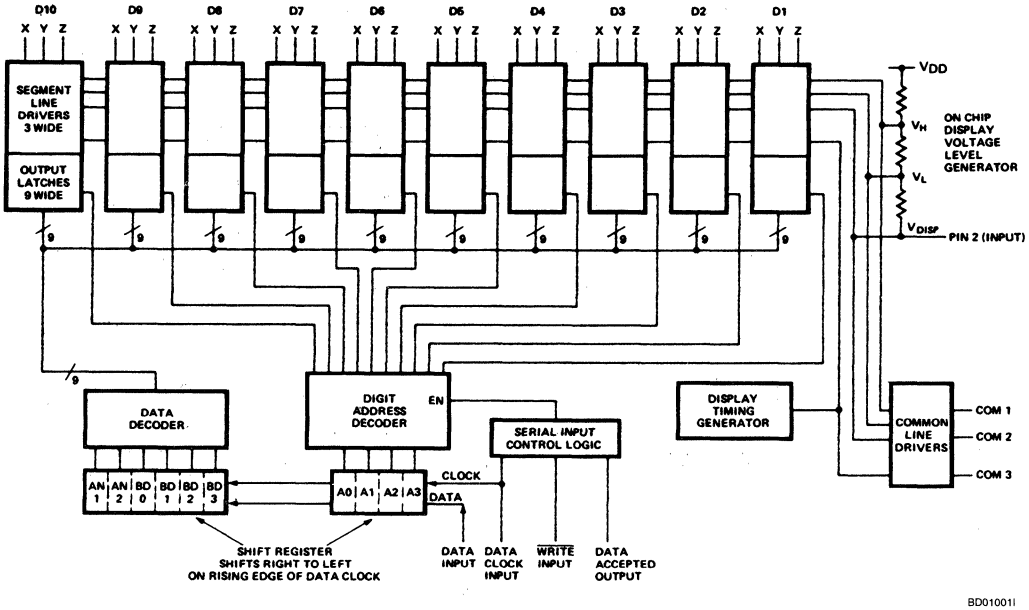


Figure 2: ICM7232 Functional Diagram

Note: All typical values have been guaranteed by characterization and are not tested.

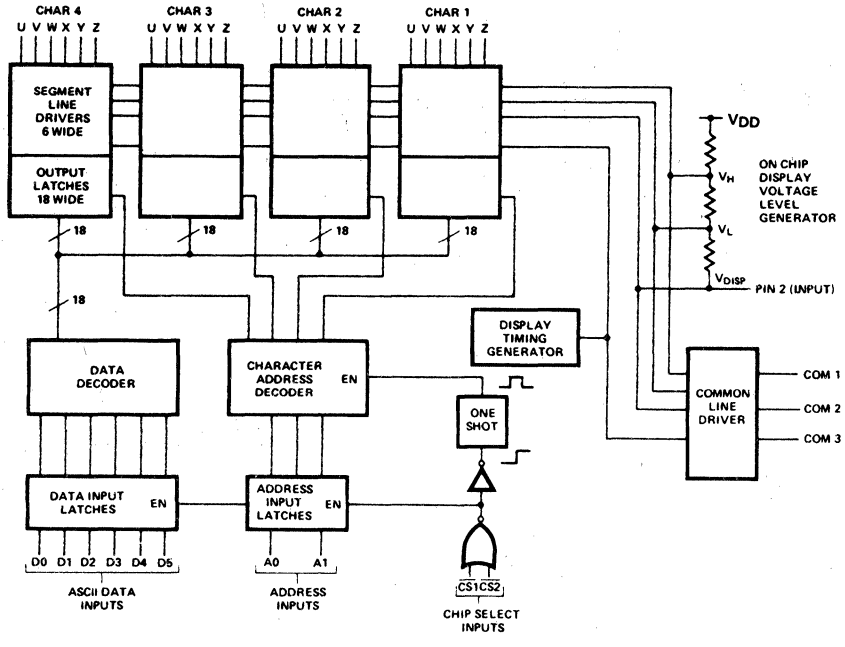


Figure 3: ICM7233 Functional Diagram

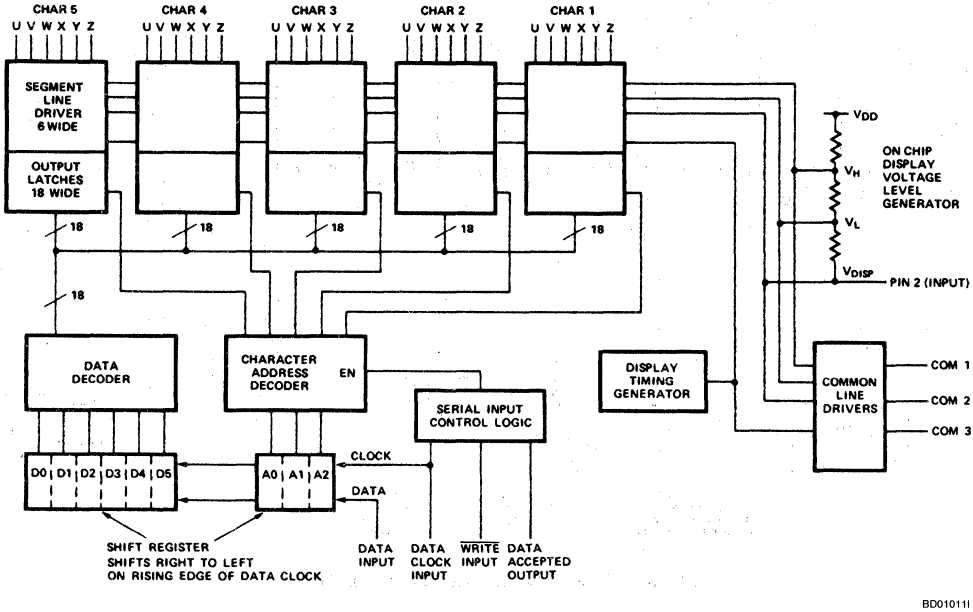


Figure 4: ICM7234 Functional Diagram

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7231-ICM7234

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD} - V_{SS}$) 6.5V
Input Voltage[2] ..... $V_{SS} - 0.3 \le V_{IN} \le 6.5$
Display Voltage[2] ..... $-0.3 \le V_{DISP} \le +0.3$

Power Dissipation[1] ..... 0.5W @ 70°C
Operating Temperature Range ..... −25°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes: 1. This limit refers to that of the package and will not be obtained during normal operation.

2. Due to the SCR structure inherent in these devices, connecting any display terminal or the display voltage terminal to a voltage outside the power supply to the chip may cause destructive device latchup. The digital inputs should never be connected to a voltage less than −0.3 volts below ground, but may be connected to voltages above V_{DD} but not more than 6.5 volts above V_{SS}.

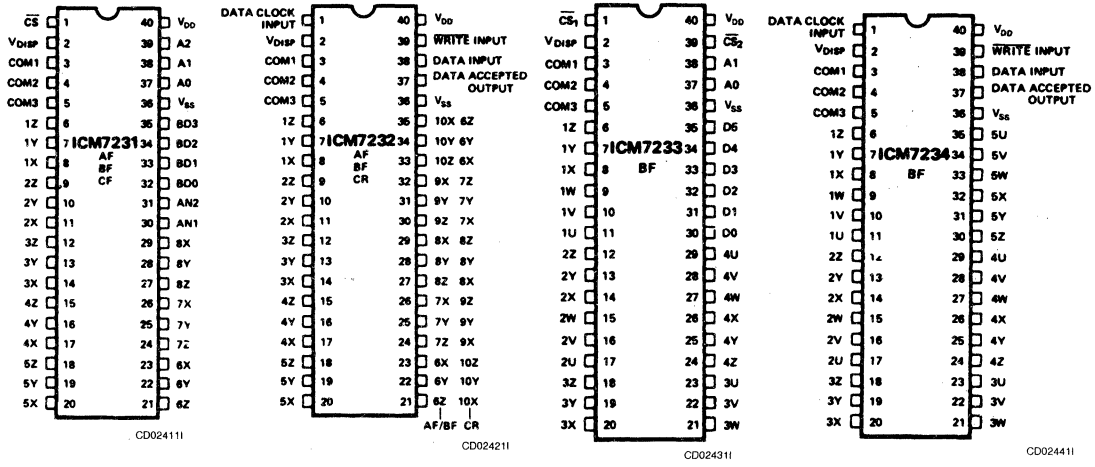


Figure 5: Pin Configuration (Outline dwg PL)

ELECTRICAL CHARACTERISTICS ($V^+ = 5V \pm 10\%$, $V_{SS} = 0V$, $T_A = -25°C$ to $+85°C$ unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS/DESCRIPTION	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage		4.5	> 4	5.5	V
V_{DD}	Data Retention Supply Voltage	Guaranteed Retention at 2V	2	1.6		V
I_{DD}	Logic Supply Current	Current from V_{DD} to Ground excluding Display. $V_{DISP} = 2V$		30	100	µA
I_S	Shutdown Total Current	V_{DISP} Pin 2 Open		1	10	µA
V_{DISP}	Display Voltage Range	$V_{SS} \le V_{DISP} \le V_{DD}$	0		V_{DD}	V
I_{DISP}	Display Voltage Setup Current	$V_{DISP} = 2V$ Current from V_{DD} to V_{DISP} On-Chip		15	30	µA
R_{DISP}	Display Voltage Setup Resistor Value	One of Three Identical Resistors in String	40	75		kΩ
	DC Component of Display Signals	(Sample Test only)		1/4	1	% (V_{DD} − V_{DISP})
f_{DISP}	Display Frame Rate	See Figure 7	60	90	120	Hz
V_{IL}	Input Low Level	ICM7231, ICM7233 Pins 30-35, 37-39, 1			0.8	V
V_{IH}	Input High Level		2.0			V
I_{ILK}	Input Leakage	ICM7232, ICM7234 Pins 1, 38, 39 (Note 1)		0.1	1	µA
C_{IN}	Input Capacitance			5		pF
V_{OL}	Output Low Level	Pin 37, ICM7232, ICM7234, $I_{OL} = 1mA$,			0.4	V
V_{OH}	Output High Level	$V_{DD} = 4.5V$, $I_{OH} = -500\mu A$	4.1			V
T_{OP}	Operating Temperature Range	Industrial Range	−25		+85	°C

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7231-ICM7234

AC CHARACTERISTICS (V_{DD} = 5V±10% V_{SS} = 0V, −20°C ≤ T_A ≤ +85°C)

PARALLEL INPUT (ICM7231, ICM7233) See Figure 13

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{cs}	$\overline{\text{Chip Select}}$ Pulse Width	(Note 1)	500	350		ns
t_{ds}	Address/Data Setup Time	(Note 1)	200			ns
t_{dh}	Address/Data Hold Time	(Note 1)	0	−20		ns
t_{ics}	Inter-Chip Select Time	(Note 1)	3			μs

SERIAL INPUT (ICM7232, ICM7234) See Figures 16, 17, 18

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{\overline{cl}}$	Data Clock Low Time	(Note 1)	350			ns
t_{cl}	Data Clock High Time	(Note 1)	350			ns
t_{ds}	Data Setup Time	(Note 1)	200			ns
t_{dh}	Data Hold Time	(Note 1)	0	−20		ns
t_{wp}	$\overline{\text{Write}}$ Pulse Width	(Note 1)	500	350		ns
t_{wll}	$\overline{\text{Write}}$ Pulse to Clock at Initialization	(Note 1)	1.5			μs
t_{odl}	Data Accepted Low Output Delay	(Note 1)		200	400	ns
t_{odh}	Data Accepted High Output Delay	(Note 1)		1.5	3	μs
t_{cws}	Write Delay After Last Clock	(Note 1)	350			ns

NOTE 1: For design reference only, not 100% tested.

TABLE OF FEATURES

TYPE NUMBER	OUTPUT CODE	ANNUNCIATOR LOCATIONS	INPUT	OUTPUT
ICM7231AF	Hexadecimal	Both Annunciators on COM3	Parallel Entry 4 bit Data 2 bit Annunciators 3 bit Address	8 Digits plus 16 Annunciators
ICM7231BF	Code B			
ICM7231CF	Code B	1 Annunciator COM1 1 Annunciator COM3		
ICM7232AF	Hexadecimal	Both Annunciators on COM3	Serial Entry 4 bit Data 2 bit Annunciators 4 bit Address	10 Digits plus 20 Annunciators
ICM7232B	Code B			
ICM7232CR	Code B	1 Annunciator COM1 1 Annunciator COM3		
ICM7233AF	64 Character (ASCII) 18 Segment (Half width numbers)	No Independent Annunciators	Parallel Entry 6 bit (ASCII) Data 2 bit Address	Four Characters
ICM7233BF	64 Character (ASCII) 18 Segment (Full width numbers)	No Independent Annunciators	Parallel Entry 6 bit (ASCII) Data 2 bit Address	Four Characters
ICM7234AF	64 Character (ASCII) 18 Segment (Half width numbers)	No Independent Annunciators	Serial Entry 6 bit (ASCII) Data 3 bit Address	Five Characters
ICM7234BF	64 Character (ASCII) 18 Segment (Full width numbers)	No Independent Annunciators	Serial Entry 6 bit (ASCII) Data 3 bit Address	Five Characters

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7231-ICM7234

TERMINAL DEFINITIONS

ICM7231 PARALLEL INPUT NUMERIC DISPLAY

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION
AN1 AN2	30 31	Annunciator 1 Control Bit Annunciator 2 Control Bit	High = ON Low = OFF — See Table 3
BD0 BD1 BD2 BD3	32 33 34 35	Least Significant Most Significant 4 Bit Binary Data Inputs	Input Data (See Table 1) — HIGH = Logical One (1), LOW = Logical Zero (0)
A0 A1 A2	37 38 39	Least Significant Most Significant 3 Bit Digit Address Inputs	Input Address (See Table 2)
$\overline{CS}$	1	Data Input Strobe/Chip Select (Note 3)	Trailing (Positive going) edge latches data, causes data input to be decoded and sent out to addressed digit

NOTE: 3. $\overline{CS}$ has a special" mid-level" sense ci rcuit that establishes a **test** mode if it is held near 3V for several msec. Inadvertent triggering of this mode can be avoided by pulling it high when inactive, or ensuring frequent activity.

ICM7233 PARALLEL INPUT ALPHA DISPLAY

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION
D0 D1 D2 D3 D4 D5	30 31 32 33 34 35	Least Significant Most Significant 6 Bit (ASCII) Data Inputs	Input Data See Table 4 — HIGH = Logical One (1), LOW = Logical Zero (0)
A0 A1	37 38	Least Significant Most Significant Address Inputs	Input Add. See Table 5
$\overline{CS1}$ $\overline{CS2}$	39 1	Chip Select Inputs (Note 3)	Both inputs LOW load data into input latches. Rising edge of either input causes data to be latched, decoded and sent out to addressed character.

NOTE: $\overline{CS1}$ has a special "mid-level" sense circuit that establishes a **test** mode if it is held near 3V for several msec. Inadvertent triggering of this mode can be avoided either by pulling it high when inactive, or ensuring frequent activity.

ICM7232 and ICM7234 SERIAL DATA AND ADDRESS INPUT

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION
Data Input	38	Data + Address Shift Register Input	HIGH = Logical One (1) LOW = Logical Zero (0)
$\overline{WRITE}$ Input	39	Decode, Output, and Reset Strobe	When DATA ACCEPTED Output is LOW, positive going edge of WRITE causes data in shift register to be decoded and sent to addressed digit, then shift register and control logic to be reset. When DATA ACCEPTED Output is HIGH, positive going edge of $\overline{WRITE}$ triggers reset only.
Data Clock Input	1	Data Shift Register and Control Logic Clock	Positive going edge advances data in shift register. ICM7232: Eleventh edge resets shift register and control logic. ICM7234: Tenth edge resets shift register and control logic.
DATA ACCEPTED Output	37	Handshake Output	Output LOW when correct number of bits entered into shift register; ICM7232 8, 9 or 10 bits ICM7234 9 bits

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7231-ICM7234

ALL DEVICES

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION
Display Voltage V_{DISP}	2	Negative end of on-chip resistor string used to generate intermediate voltage levels for display. Shutdown Input.	Display voltage control. When open (or less than 1V from V_{DD}) chip is shutdown; oscillator stops, all display pins to V_{DD}.
Common Line Driver Outputs	3,4,5		Drive display commons, or rows.
Segment Line Driver Outputs	6–29 6–35	(On ICM7231/33) (On ICM7232/34)	Drive display segments, or columns.
V_{DD}	40	Chip Positive Supply	
V_{SS}	36	Chip Negative Supply	

ICM7231 FAMILY DESCRIPTION

The ICM7231 drives displays with 8 seven-segment digits with two independent annunciators per digit, accepting six data bits and three digit address bits from parallel inputs controlled by a chip select input. The data bits are subdivided into four binary code bits and two annunciator control bits.

The ICM7232 drives 10 seven-segment digits with two independent annunciators per digit. To write into the display, six bits of data and four bits of digit address are clocked serially into a shift register, then decoded and written to the display.

The ICM7233 has a parallel input structure similar to the ICM7231, but the decoding and the outputs are organized to drive four 18-segment alphanumeric characters. The six data bits represent a 6-bit ASCII code.

The ICM7234 uses a serial input structure like that of the ICM7232, and drives five 18-segment characters. Again, the input bits represent a 6-bit ASCII code.

Input levels are TTL compatible, and the DATA ACCEPTED output on the serial input devices will drive one LSTTL load. The intermediate voltage levels necessary to drive the display properly are generated by an on-chip resistor string, and the output of a totally self-contained on-chip oscillator is used to generate all display timing. All devices in this family have been fabricated using Intersil's MAXCMOS® process and all inputs are protected against static discharge.

TRIPLEXED (1/3 MULTIPLEXED) LIQUID CRYSTAL DISPLAYS

Figure 6 shows the connection diagram for a typical 7-segment display font with two annunciators such as would be used with an ICM7231 or ICM7232 numeric display driver. Figure 7 shows the voltage waveforms of the common lines and one segment line, chosen for this example to be the "Y" segment line. This line intersects with COM1 to form the "a" segment, COM2 to form the "g" segment and COM3 to form the "d" segment. Figure 7 also shows the waveform of the "Y" segment line for four different ON/OFF combinations of the "a", "g" and "d" segments. Each intersection (segment or annunciator) acts as a capacitance from segment line to common line, shown schematically in Figure 8. Figure 9 shows the voltage across the "g" segment for the same four combinations of ON/OFF segments in Figure 7.

The degree of polarization of the liquid crystal material and thus the contrast of any intersection depends on the RMS voltage across the intersection capacitance. Note from Figure 4 that the RMS OFF voltage is always $V_P/3$ and that the RMS ON voltage is always 1.92 $V_P/3$.

For a 1/3 multiplexed LCD, the ratio of RMS ON to OFF voltages is fixed at 1.92, achieving adequate display contrast with this ratio of applied RMS voltage makes some demands on the liquid crystal material used.

Figure 10 shows the curve of contrast versus applied RMS voltage for a liquid crystal material tailored for $V_P = 3.1V$, a typical value for 1/3-multiplexed displays in calculators. Note that the RMS OFF voltage $V_P/3 \approx 1V$ is just below the "threshold" voltage where contrast begins to increase. This places the RMS ON voltage at 2.1V, which provides about 85% contrast when viewed straight on.

All members of the ICM7231/ICM7234 family use an internal resistor string of three equal value resistors to generate the voltages used to drive the display. One end of the string is connected on the chip to V_{DD} and the other end (user input) is available at pin 2 (V_{DISP}) on each chip. This allows the display voltage input (V_{DISP}) to be optimized for the particular liquid crystal material used. Remember that $V_P = V_{DD} - V_{DISP}$ and should be three times the threshold voltage of the liquid crystal material used. Also it is very important that pin 2 never be driven below V_{SS}. This can cause device latchup and destruction of the chip.

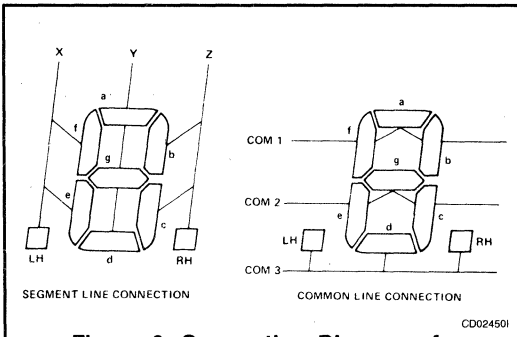


Figure 6: Connection Diagrams for Typical 7-Segment Displays

Note: All typical values have been guaranteed by characterization and are not tested.

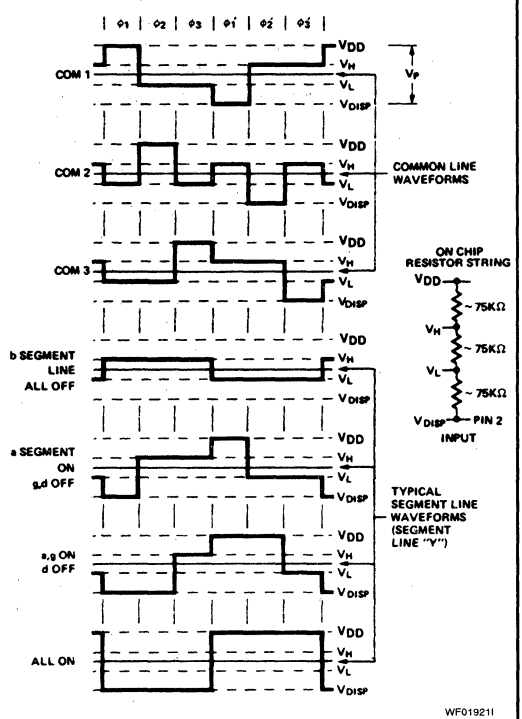


Figure 7: Display Voltage Waveforms

NOTE: ϕ_1, ϕ_2, ϕ_3 — COMMON HIGH WITH RESPECT TO SEGMENT.

ϕ_1', ϕ_2', ϕ_3' — COMMON LOW WITH RESPECT TO SEGMENT.

COM 1 ACTIVE DURING ϕ_1 AND ϕ_1'

COM 2 ACTIVE DURING ϕ_2 AND ϕ_2'

COM 3 ACTIVE DURING ϕ_3 AND ϕ_3'

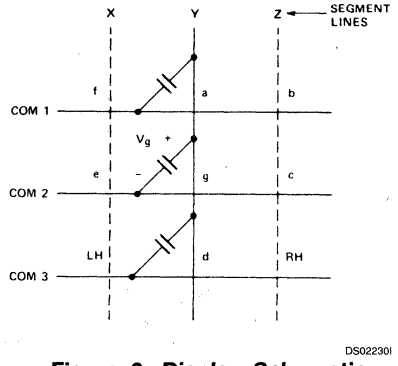


Figure 8: Display Schematic

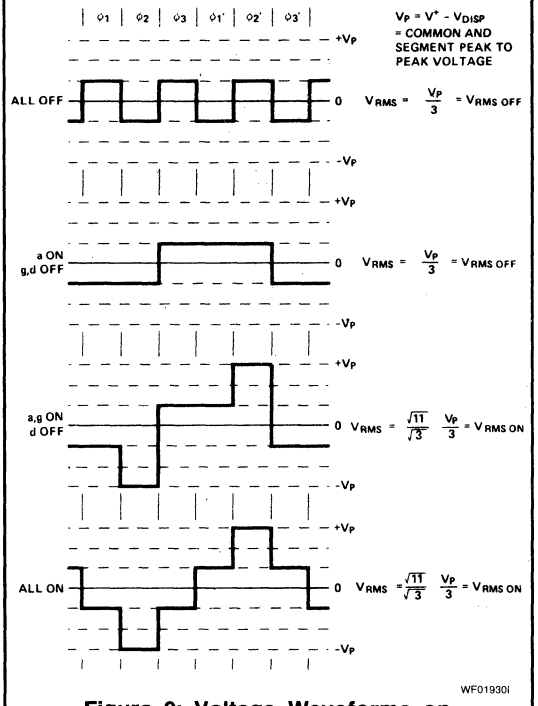


Figure 9: Voltage Waveforms on Segment g(V_g)

$$\text{VOLTAGE CONTRAST RATIO} = \frac{V_{RMS\ ON}}{V_{RMS OFF}} = \frac{\sqrt{11}}{\sqrt{3}} = 1.92$$

NOTE: ϕ_1, ϕ_2, ϕ_3 - COMMON HIGH WITH RESPECT TO SEGMENT.

ϕ_1', ϕ_2', ϕ_3' - COMMON LOW WITH RESPECT TO SEGMENT.

COM 1 ACTIVE DURING ϕ_1 AND ϕ_1'

COM 2 ACTIVE DURING ϕ_2 AND ϕ_2'

COM 3 ACTIVE DURING ϕ_3 AND ϕ_3'

Note: All typical values have been guaranteed by characterization and are not tested.

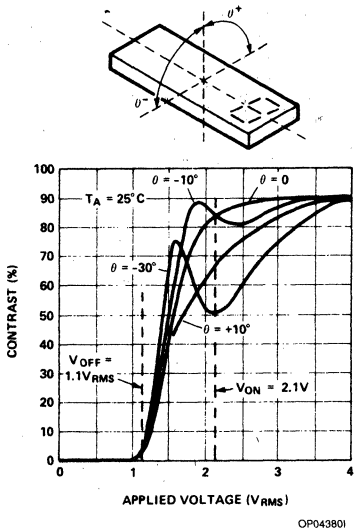


Figure 10: Contrast vs. Applied RMS Voltage

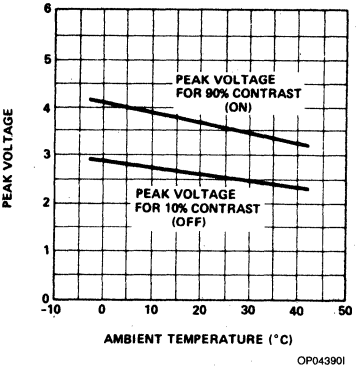


Figure 11: Temperature Dependence of LC Threshold

TEMPERATURE EFFECTS AND TEMPERATURE COMPENSATION

The performance of the IC material is affected by temperature in two ways. The response time of the display to changes in applied RMS voltage gets longer as the display temperature drops. At very low temperatures (−20°C) some displays may take several seconds to change a new character after the new information appears at the outputs. However, for most applications above 0°C this will not be a problem with available multiplexed LCD materials, and for low-temperature applications, high-speed liquid crystal materials are available. One high temperature effect to consider deals with plastic materials used to make the polarizer. Some polarizers become soft at high temperatures and permanently lose their polarizing ability, thereby seriously degrading display contrast. Some displays also use sealing materials unsuitable for high temperature use. Thus, when specifying displays the following must be kept in mind: liquid crystal material, polarizer, and seal materials.

A more important effect of temperature is the variation of threshold voltage. For typical liquid crystal materials suitable for multiplexing, the peak voltage has a temperature coefficient of −7 to −14 mV/°C. This means that as temperature rises, the threshold voltage goes down. Assuming a fixed value for V_P, when the threshold voltage drops below $V_P/3$ OFF segments begin to be visible. Figure 11 shows the temperature dependence of peak voltage for the same liquid crystal material of Figure 10.

For applications where the display temperature does not vary widely, V_P may be set at a fixed voltage chosen to make the RMS OFF voltage, $V_P/3$, just below the threshold voltage at the highest temperature expected. This will prevent OFF segments turning ON at high temperature (this at the cost of reduced contrast for ON segments at low temperatures).

For applications where the display temperature may vary to wider extremes, the display voltage V_{DISP} (and thus V_P) may require temperature compensation to maintain sufficient contrast without OFF segments becoming visible.

DISPLAY VOLTAGE AND TEMPERATURE COMPENSATION

These circuits allow control of the display peak voltage by bringing the bottom of the voltage divider resistor string out at pin 2. The simplest means for generating a display voltage suitable to a particular display is to connect a potentiometer from pin 2 to V_{SS} as shown in Figure 12. A potentiometer with a maximum value of 200 kΩ should give sufficient range of adjustment to suit most displays. This method for generating display voltage should be used only in applications where the temperature of the chip and display won't vary more than ±5°C (±9°F), as the resistors on the chip have a positive temperature coefficient, which will tend to increase the display peak voltage with an increase in temperature. The display voltage also depends on the power supply voltage, leading to tighter tolerances for wider temperature ranges.

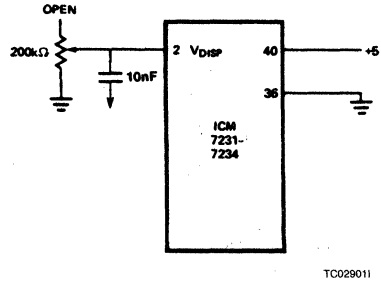


Figure 12: Simple Display Voltage Adjustment

Figure 13(a) shows another method of setting up a display voltage using five silicon diodes in series. These diodes, 1N914 or equivalent, will each have a forward drop of approximately 0.65V, with approximately 20μA flowing

Note: All typical values have been guaranteed by characterization and are not tested.

through them at room temperature. Thus, 5 diodes will give 3.25V, suitable for a 3V display using the material properties shown in Figures 10 and 11. For higher voltage displays, more diodes may be added. This circuit provides reasonable temperature compensation, as each diode has a negative temperature coefficient of −2 mV/°C; five in series gives −10 mV/°C, not far from optimum for the material described.

The disadvantage of the diodes in series is that only integral multiples of the diode voltage can be achieved. The diode voltage multiplier circuit shown in Figure 13(b) allows fine-tuning the display voltage by means of the potentiometer; it likewise provides temperature compensation since the temperature coefficient of the transistor base-emitter junction (about −2 mV/°C) is also multipled. The transistor should have a beta of at least 100 with a collector current of 10 μA. The inexpensive 2N2222 shown in the figure is a suitable device.

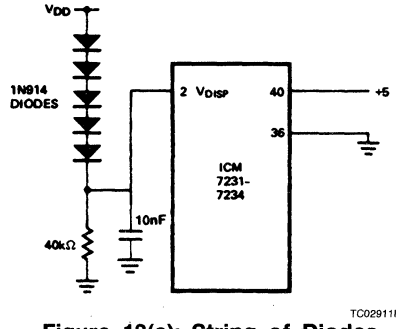


Figure 13(a): String of Diodes

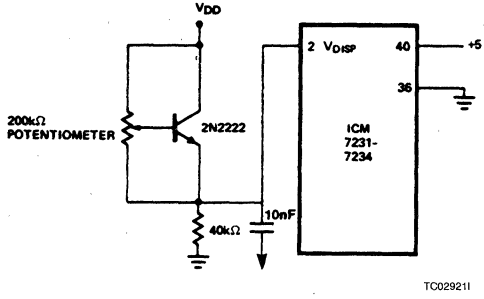


Figure 13(b): Transistor-Multiplier

Figure 13: Diode-based Temperature Compensation

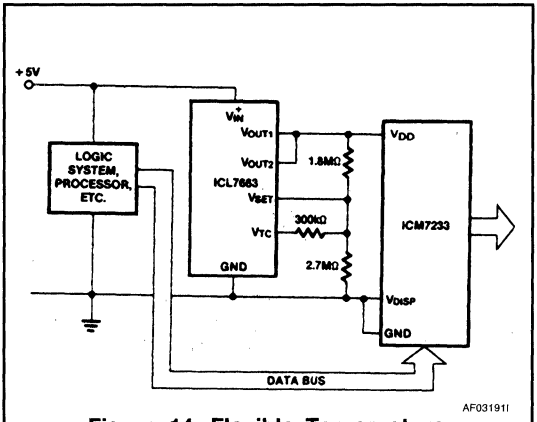


Figure 14: Flexible Temperature Compensation

Note: All typical values have been guaranteed by characterization and are not tested.

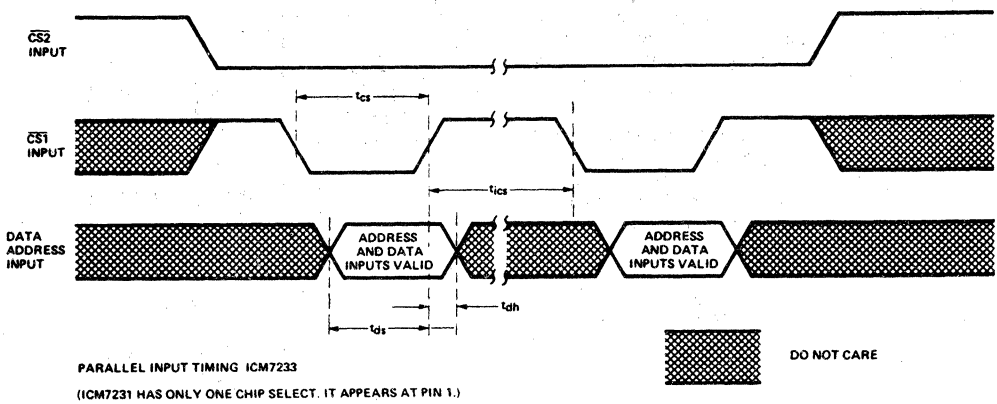


Figure 15: Parallel Input Timing

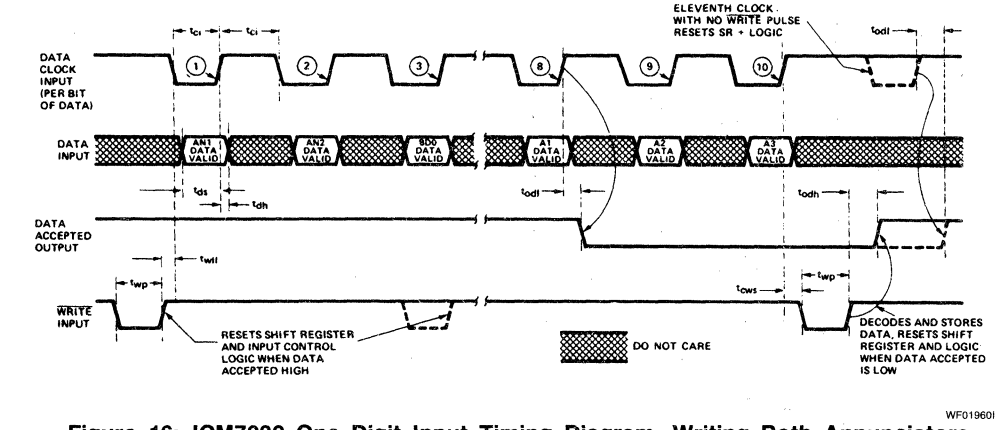


Figure 16: ICM7232 One Digit Input Timing Diagram, Writing Both Annunciators

For battery operation, where the display voltage is generally the same as the battery voltage (usually 3-4.5V), the chip may be operated at the display voltage, with V_{DISP} connected to V_{SS}. The inputs of the chip are designed such that they may be driven above V_{DD} without damaging the chip. This allows, for example, the chip and display to operate at a regulated 3V, and a microprocessor driving its inputs to operate with a less well controlled 5V supply. (The inputs should not be driven more than 6.5V above GND under any circumstances.) This also allows temperature compensation with the ICL7663, as shown in Figure 14. This circuit allows independent adjustment of both voltage and temperature compensation.

DESCRIPTION OF OPERATION

PARALLEL INPUT OF DATA AND ADDRESS (ICM7231, ICM7233)

The parallel input structure of the ICM7231 and ICM7233 devices is organized to allow simple, direct interfacing to all microprocessors, (see functional diagrams Figures 1 and 3). In the ICM7231, address and data bits are written into the input latches on the rising edge of the Chip Select input. In the ICM7233, the two Chip Selects are equivalent; when both are low, the latches are transparent and the data is latched on the rising edge of either Chip Select.

Note: All typical values have been guaranteed by characterization and are not tested.

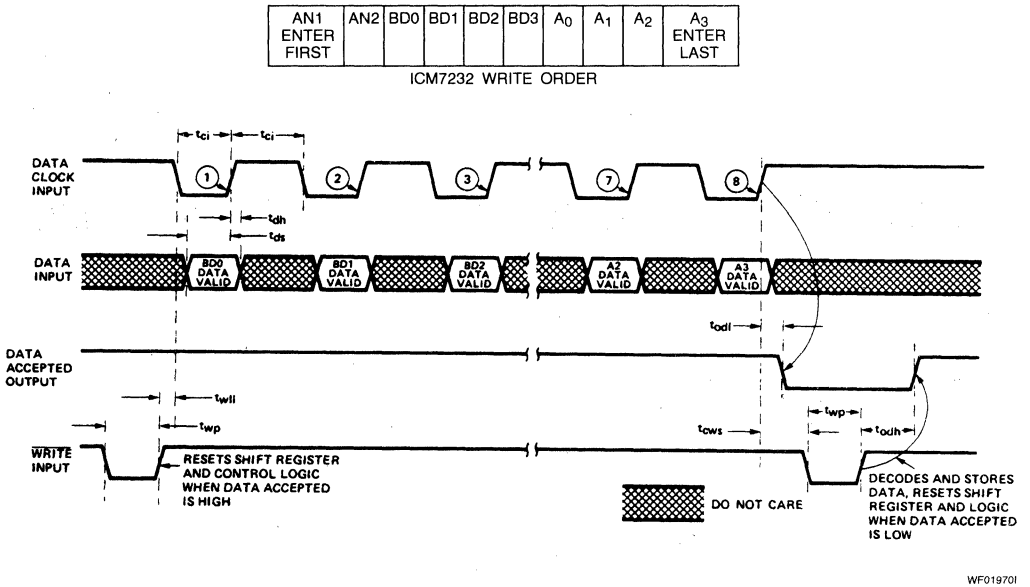


Figure 17: ICM7232 Input Timing Diagram, Leaving Both Annunciators Off

The rising edge of the Chip Select also triggers an on-chip pulse which enables the address decoder and latches the decoded data into the addressed digit/character outputs. The timing requirements for the parallel input devices are shown in Figure 15, with the values for setup, hold, and pulse width times shown in the AC Characteristics section. Note that there is a minimum time between Chip Select pulses; this is to allow sufficient time for the on-chip enable pulse to decay, and ensures that new data doesn't appear at the decoder inputs before the decoded data is written to the outputs.

SERIAL INPUT OF DATA AND ADDRESS (ICM7232, ICM7234)

The ICM7232 and ICM7234 trade six pins used as data inputs on the ICM7231 and ICM7233 for six more segment lines, allowing two more 9-segment digits (ICM7232) or one more 18-segment character (ICM7234). This is done at the cost of ease in interfacing, and requires that data and address information be entered serially. Refer to functional diagrams, Figures 2 and 4 and timing diagrams, Figures 16, 17, and 18. The interface consists of four pins: DATA Input, DATA CLOCK Input, $\overline{\text{WRITE}}$ Input and DATA ACCEPTED Output. The data present at the DATA Input is clocked into a shift register on the rising edge of the DATA CLOCK Input signal, and when the correct number of bits has been shifted into the shift register (8 in the ICM7232, 9 in the ICM7234), the DATA ACCEPTED Output goes low. Following this, a low-going pulse at the $\overline{\text{WRITE}}$ input will trigger the chip to decode the data and store it in the output latches of the addressed digit/character. After the data is latched at the outputs, the shift register and the control logic are reset, returning the DATA ACCEPTED Output high. After this occurs, a pulse at the $\overline{\text{WRITE}}$ input will not change the outputs, but will reset the control logic and shift register, assuring that each data bit will be entered into the correct position in the shift register depending on subsequent DATA CLOCK inputs.

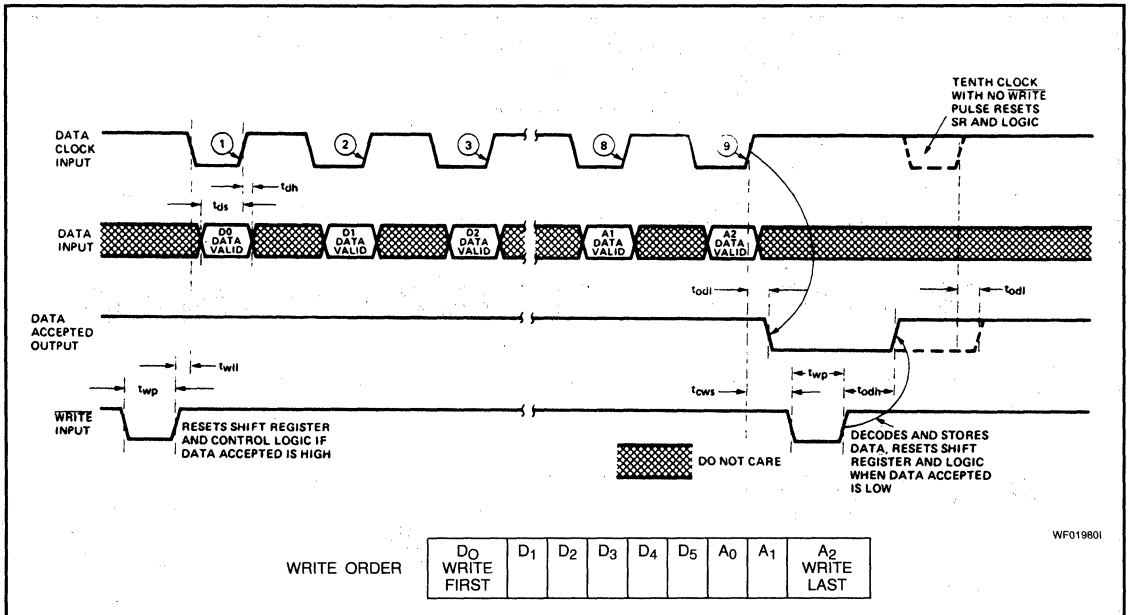
The shift register and control logic will also be reset if too many DATA CLOCK INPUT edges are received; this prevents incorrect data from being decoded. In the ICM7232, the eleventh clock resets the shift register and control logic, while in the ICM7234 it is the tenth.

The recommended procedure for entering data is shown in the serial input timing diagram, Figure 16. First, when DATA ACCEPTED is high, send a $\overline{\text{WRITE}}$ pulse. This resets the shift register and control logic and initializes the chip for the data input sequence. Next clock in the appropriate number of correct data and address bits. The DATA ACCEPTED Output may be monitored if desired, to determine when the chip is ready to output the decoded data. When the correct number of bits has been entered, and the DATA ACCEPTED Output is low, a pulse at $\overline{\text{WRITE}}$ will cause the data to be decoded and stored in the latches of the addressed digit/character. The shift register and control logic are reset, causing DATA ACCEPTED to return high, and leaving the chip ready to accept data for the next digit/character.

Note that for the ICM7232 the eleventh clock resets the shift register and control logic, but the DATA ACCEPTED Output goes low after the eighth clock. This allows the user to abbreviate the data to eight bits, which will write the correct character to the 7-segment display, but will leave the annunciators off, as shown in Figure 17.

If only AN2 is to be turned on, nine bits are clocked in; if AN1 is to be turned on, all ten bits are used.

Note: All typical values have been guaranteed by characterization and are not tested.



WRITE ORDER	D_0 WRITE FIRST	D_1	D_2	D_3	D_4	D_5	A_0	A_1	A_2 WRITE LAST

Figure 18: ICM7234 One Character Input Timing Diagram

In the ICM7234, nine bits are always required; the control logic is similar, but allows only a $\overline{\text{WRITE}}$ (DATA ACCEPTED Low) with nine bits entered in the shift register, as shown in Figure 18.

The DATA ACCEPTED Output will drive one low-power Schottky TTL input, and has equal current drive capability pulling high or low.

Note that in the serial input devices, it is possible to address digits/characters which don't exist. As shown in Tables 2 and 5, when an incorrect address is applied together with a $\overline{\text{WRITE}}$ pulse, none of the outputs will be changed.

DISPLAY FONTS AND OUTPUT CODES

The standard versions of the ICM7231 and ICM7232 chips are programmed to drive a 7-segment display plus two annunciators per digit. See Table 3 for annunciator input controls.

The "A" and "B" suffix chips place both annunciators on COM3. The display connections for one digit of this display are shown in Figure 19. The "A" devices decode the input data into a hexadecimal 7-segment output, while the "B" devices supply Code B outputs (see Table 1).

The "C" devices place the left hand annunciator on COM1 (AN2) and the right hand annunciator (usually a decimal point) on COM3 (AN1). (See Figure 20). The "C" devices provide only a "Code B" output for the 7-segments.

The ICM7233 and ICM7234 are supplied in "A" and "B" versions. Both versions decode an ASCII 6-bit subset to an 18-segment display, with 16 "flag" segments and two "dots". The "A" devices have numbers which are half width and the "B" devices have full width numbers. The layout for a single character is shown in Figure 21 with output decoding shown in Table 4.

TABLE 1. BINARY DATA DECODING (ICM7231/32)

CODE INPUT				DISPLAY OUTPUT	
BD 3	BD 2	BD 1	BD 0	HEX	CODE B
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	BLANK

TB00080I

Note: All typical values have been guaranteed by characterization and are not tested.

TABLE 2. ADDRESS DECODING (ICM7231/32)

CODE INPUT				DISPLAY OUTPUT
ICM7232 ONLY A3	A2	A1	A0	DIGIT SELECTED
0	0	0	0	D1
0	0	0	1	D2
0	0	1	0	D3
0	0	1	1	D4
0	1	0	0	D5
0	1	0	1	D6
0	1	1	0	D7
0	1	1	1	D8
1	0	0	0	D9
1	0	0	1	D10
1	0	1	0	NONE
1	0	1	1	NONE
1	1	0	0	NONE
1	1	0	1	NONE
1	1	1	0	NONE
1	1	1	1	NONE

TABLE 3. ANNUNCIATOR DECODING

CODE INPUT		DISPLAY OUTPUT	
AN 2	AN 1	ICM7231 A/B ICM7232 A/B BOTH ANNUNCIATORS ON COM 3	ICM7231C ICM7232C LH ANNUNCIATOR COM 1 RH ANNUNCIATOR COM 3
0	0		
0	1		
1	0		
1	1		

TB00090I

EVALUATION KITS

After purchasing a sample of the ICM7231/32/33/34, the majority of users will want to build a sample display. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application. However, locating and purchasing even the small number of additional components required, then wiring a breadboard, can often cause delays of days or sometimes weeks. To avoid this problem and facilitate evaluation of these unique circuits, Intersil is offering kits which contain all the necessary components to build 8 character displays. With the help of such a kit, an engineer or technician can have the system "up and running" in about half an hour.

The ICM7233EV/KIT contains the appropriate ICs, a circuit board, a Multiplexed LCD display 16/18 segment, passive components, and miscellaneous hardware.

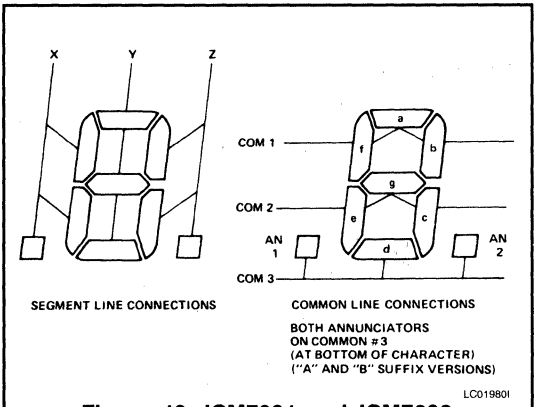


Figure 19: ICM7231 and ICM7232 Display Fonts ("A" and "B" Suffix Versions)

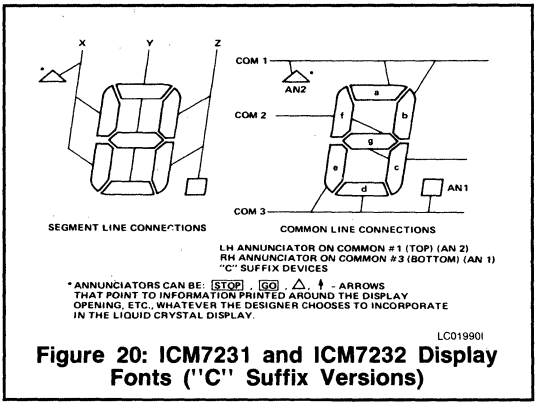


Figure 20: ICM7231 and ICM7232 Display Fonts ("C" Suffix Versions)

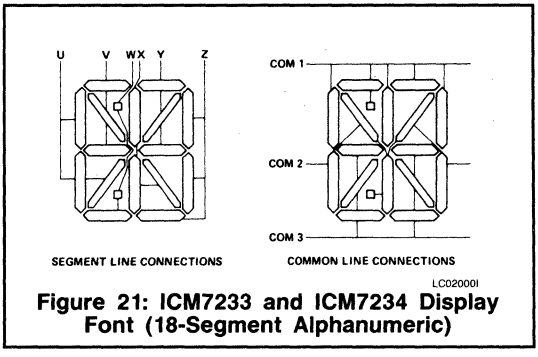


Figure 21: ICM7233 and ICM7234 Display Font (18-Segment Alphanumeric)

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7231-ICM7234

COMPATIBLE DISPLAYS

Compatible displays are manufactured by:

G.E. Displays Inc., Beechwood, Ohio (216)831-8100 (#356E3R99HJ)

Epson America Inc., Torrance CA (Model Numbers LDB726/7/8).

Seiko Instruments USA Inc., Torrance CA (Custom Displays)

Crystaloid, Hudson, OH

TABLE 4. DATA DECODING 6-BIT ASCII→ 18 SEGMENT (ICM7233/34)

CODE INPUT				DISPLAY OUTPUT				
				D5, D4			A	B
D3	D2	D1	D0	0, 0	0, 1	1, 0	1, 1	
0	0	0	0	P	p		0	0
0	0	0	1	A	Q	!	1	1
0	0	1	0	B	R	"	2	2
0	0	1	1	C	S	#	3	3
0	1	0	0	D	T	$	4	4
0	1	0	1	E	U	%	5	5
0	1	1	0	F	V	&	6	6
0	1	1	1	G	W	'	7	7
1	0	0	0	H	X	(	8	8
1	0	0	1	I	Y	)	9	9
1	0	1	0	J	Z	*	:	
1	0	1	1	K	[	+	;	
1	1	0	0	L	\	,	<	
1	1	0	1	M	]	-	=	
1	1	1	0	N	↑	.	>	
1	1	1	1	O	←	/	?	

TB001001

TABLE 5. ADDRESS DECODING (ICM7233/34)

CODE INPUT			DIGIT SELECTED
ICM7234 ONLY			
A2	A1	A0	
0	0	0	D1
0	0	1	D2
0	1	0	D3
0	1	1	D4
1	0	0	D5
1	0	1	NONE
1	1	0	NONE
1	1	1	NONE

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7231-ICM7234

TYPICAL APPLICATIONS

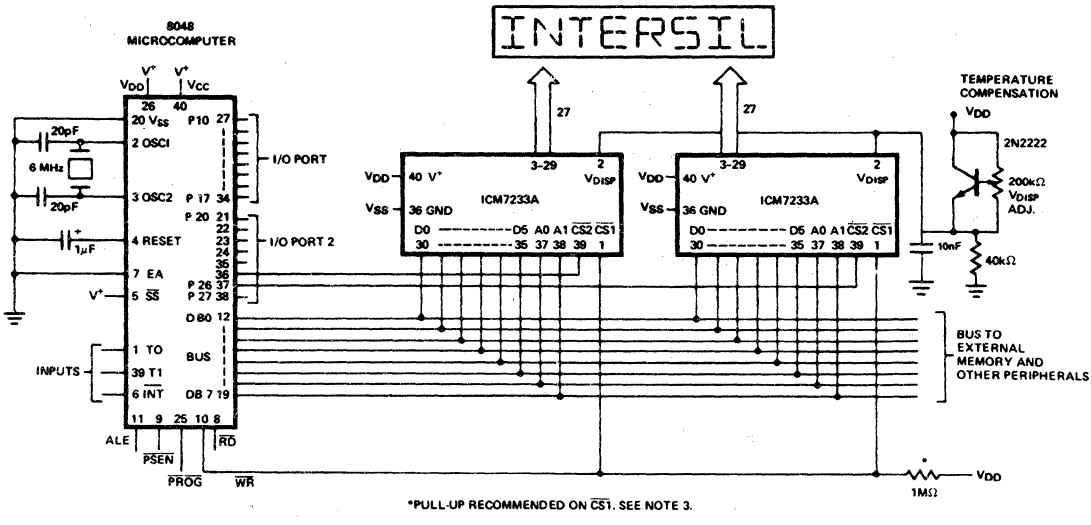


Figure 22: 8048/IM80C48 Microcomputer with 8 Character 16 Segment ASCII Triplex Liquid Crystal Display.

The two bit character address is merged with the data and written to the display driver under the control of the $\overline{WR}$ line. Port lines are used to either select the target driver, or deselect all of them for other bus operations.

Note: All typical values have been guaranteed by characterization and are not tested.

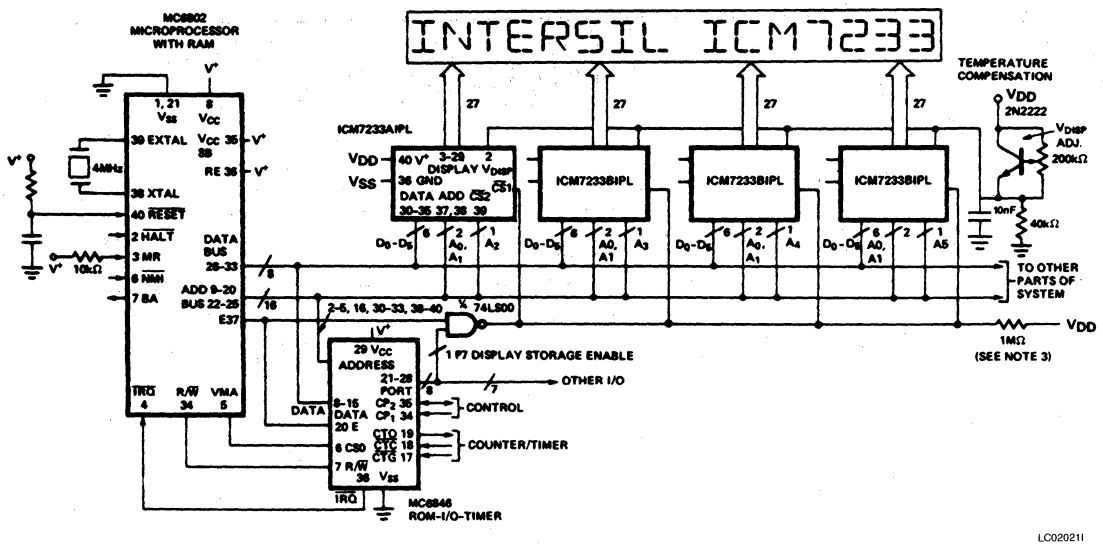


Figure 23: MC6802 Microprocessor with 16 Character 16 Segment ASCII Liquid Crystal Display.

The peripheral device provides ROM and Timer functions in addition to port line control of the display bank. Individual character locations are addressed via the address bus. Note that VMA is not decoded on these lines, which could cause problems with the TST instruction.

Note: All typical values have been guaranteed by characterization and are not tested.

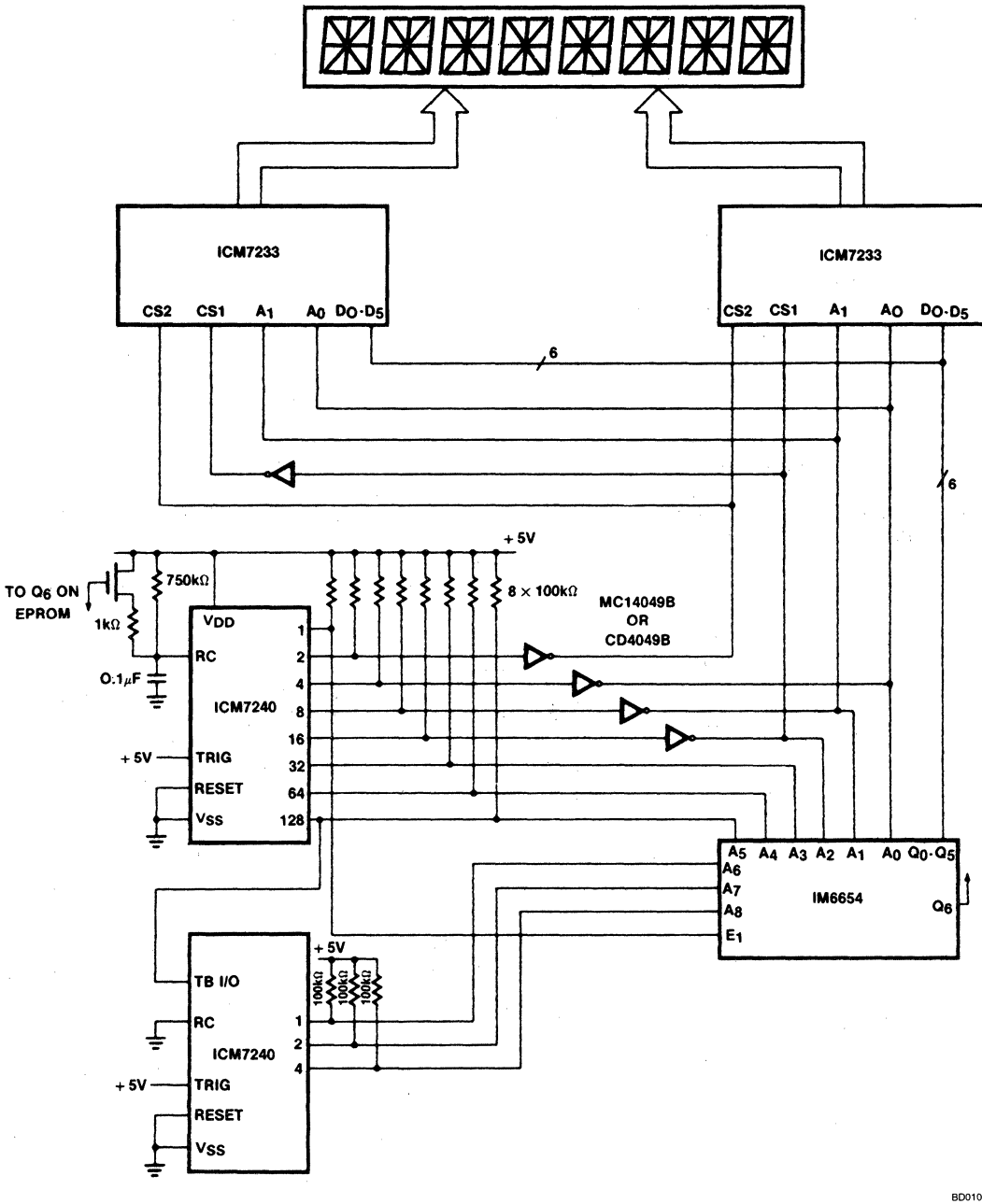


Figure 24: EPROM-Coded Message System.

This circuit cycles through a message coded in the EPROM, pausing at the end of each line, or whenever coded on Q_6.

Note: All typical values have been guaranteed by characterization and are not tested.

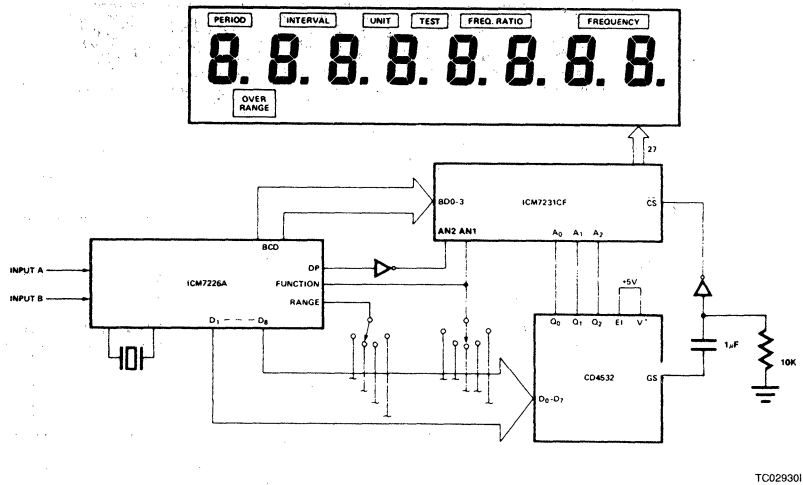


Figure 25: 10MHz Frequency/Period Pointer with LCD Display.

The annunciators show function and the decimal points indicate the range of the current operation. The system can be efficiently battery operated.

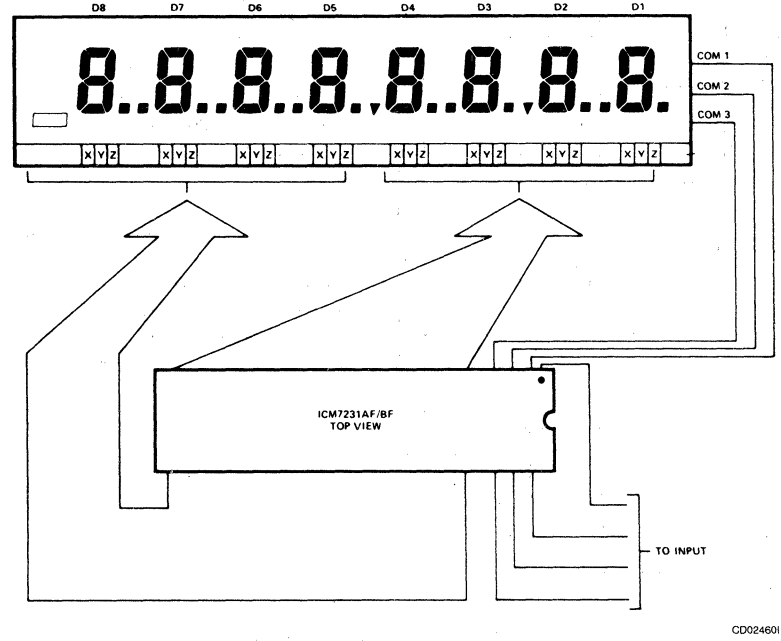
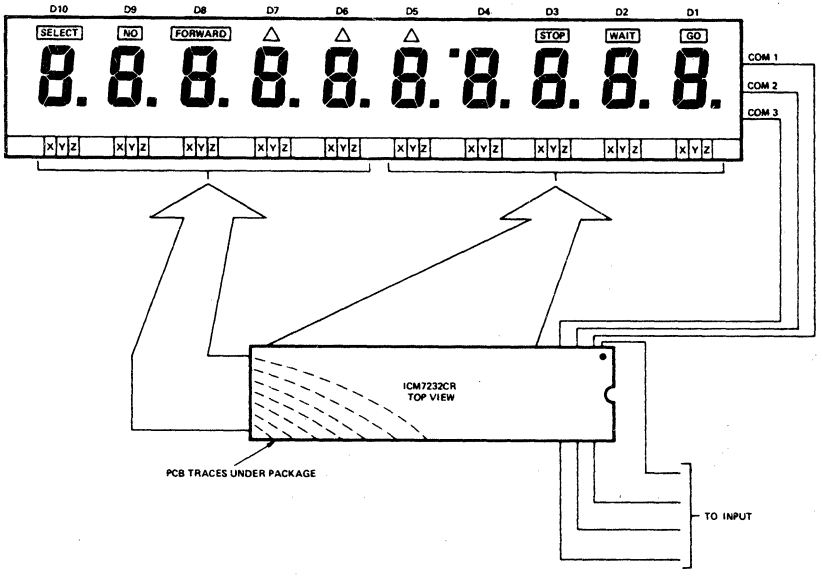


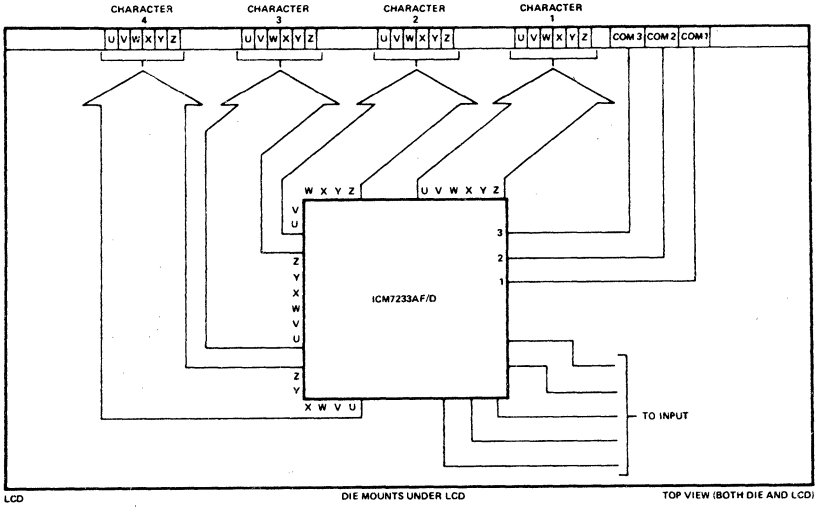
Figure 26: "Forward" Pin Orientation and Display Connections

Note: All typical values have been guaranteed by characterization and are not tested.



CD024701

Figure 27: "Reverse" Pin Orientation and Display Connections



CD024801

Figure 28: "Forward" Die Pad Orientation and Typical Triplex Alphanumeric Display Connections

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7235
4-Digit Vacuum Fluorescent Display Driver

GENERAL DESCRIPTION

The ICM7235 family of display driver circuits provides the user with a single chip interface between digital logic or microprocessors to non-multiplexed 7-segment vacuum fluorescent displays.

The chips provide 28 high voltage open drain P-channel transistor outputs organized as four 7-segment digits. The devices are available with two input configurations. The basic devices provide four data-bit inputs and four digit select inputs. This configuration is suitable for interfacing with multiplexed BCD or binary output devices, such as the Intersil ICM7217, ICM7226 and ICL7135. The microprocessor interface devices (suffix M) provide data input latches and digit address latches under control of high-speed chip select inputs. These devices simplify the task of implementing a cost-effective alphanumeric 7-segment display for microprocessor systems, without requiring extensive ROM or CPU time for decoding and display updating.

The standard devices available will provide two different decoder configurations. The basic device will decode the four bit binary input into a seven-segment alphanumeric hexadecimal output (0–9, A–F). The "A" versions provide the Code "B" output (0–9, dash, E, H, L, P, blank). Either device will correctly decode true BCD to seven-segment decimal outputs.

FEATURES

- **28 High Voltage Outputs Drive Four 7-Segment Digits**
- **Multiplexed BCD Input (7235)**
- **High Speed Processor Interface (7235M)**
- **7-Segment Hexadecimal or Code-B Output Versions Available**
- **Display Blanking Input**
- **Low Power Operation**

ORDERING INFORMATION

ORDER PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7235IPL	–20°C to +85°C	40 Pin CERDIP
ICM7235MIJL	–20°C to +85°C	40 Pin CERDIP
ICM7235MIPL	–20°C to +85°C	40 Pin PLASTIC
ICM7235AIJL	–20°C to +85°C	40 Pin PLASTIC
ICM7235AIPL	–20°C to +85°C	40 Pin PLASTIC
ICM7235AMIJL	–20°C to +85°C	40 Pin CERDIP
ICM7235AMIPL	–20°C to +85°C	40 Pin PLASTIC
ICM7235/D		DICE
ICM7235A/D		DICE
ICM7235AM/D		DICE
ICM7235M/D		DICE

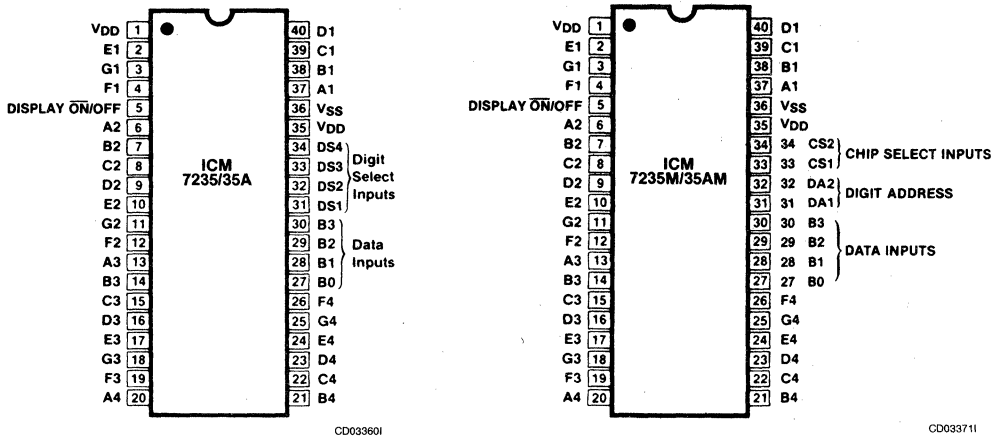


Figure 1: Pin Configurations

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7235

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 0.5W @ +70°C
Supply Voltage ($V_{DD}-V_{SS}$) ..... 6.5 Volts
Input Voltage (Note 2) ..... V_{SS} −0.3V to V_{DD} +0.3V
Output Voltage (Note 3) ..... V_{DD} −35V

Operating Temperature Range ..... −20°C to +85°C
Storage Temperature Range ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Stresses above listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

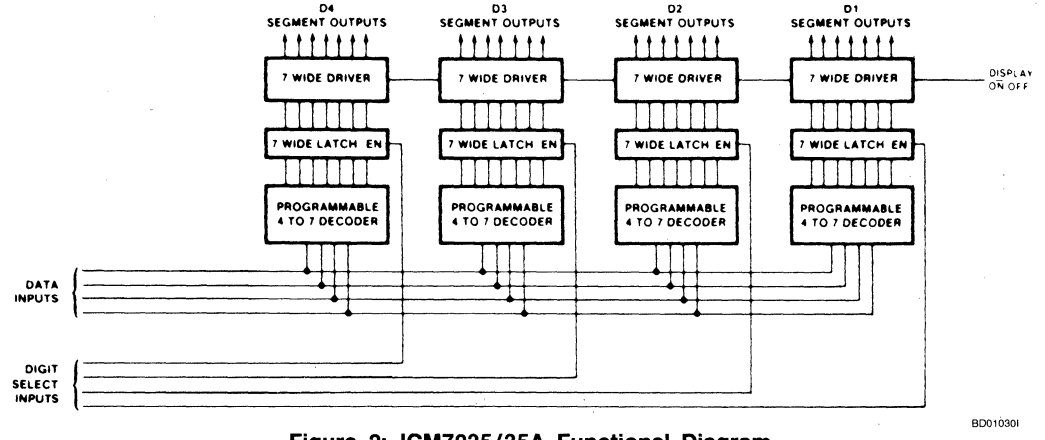


Figure 2: ICM7235/35A Functional Diagram

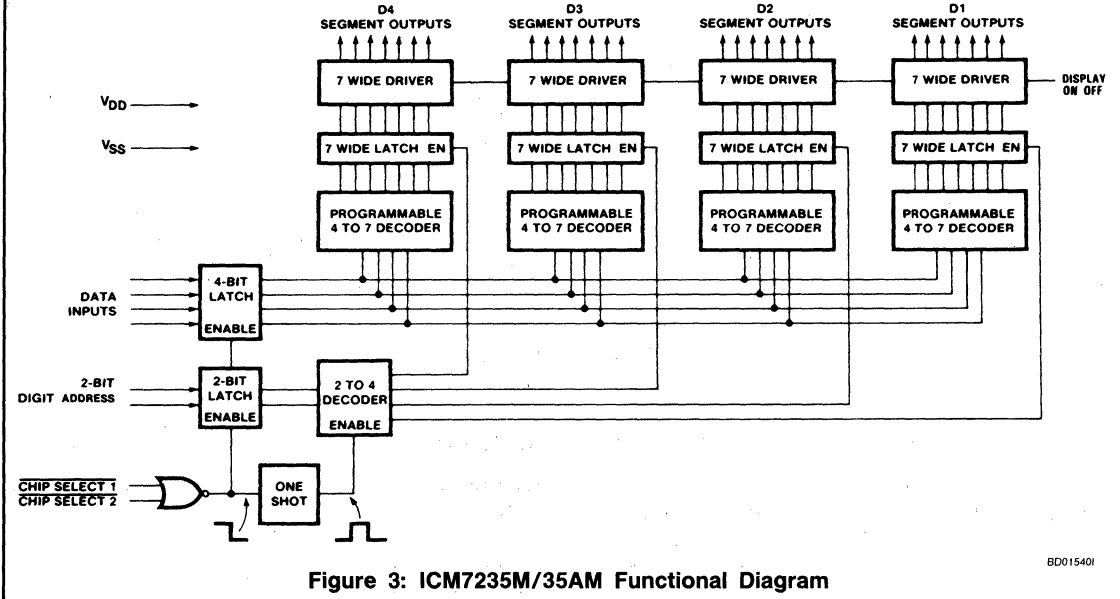


Figure 3: ICM7235M/35AM Functional Diagram

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7235

INTERSIL

ELECTRICAL CHARACTERISTICS (All parameters measured with V_{DD} = 5V±10%, V_{SS} = 0V, T_A = 25°C, unless stated otherwise).

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SUPP}	Operating Supply Voltage Range (V_{DD} – V_{SS})		4		6	V
I_{STBY}	Supply Current	Measured V_{DD} to V_{SS} Test circuit; display blank or OFF		10	50	µA
I_{DD}	Supply Current	Measured V_{DD} to Display			100	mA
V_{SEG}	Segment OFF Output Voltage	I_{SLK} = 10µA	30			V
I_{LS}	Segment OFF Leakage Current	V_{SEG} = V_{DD} – 30V		0.1	10	µA
I_{SEG}	Segment ON Current	V_{SEG} = V_{DD} – 2V	1.5	2.5		mA

INPUT CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Logical "1" Input Voltage	Referred to V_{SS}	3			V
V_{IL}	Logical "0" Input Voltage	Referred to V_{SS}			1.5	V
I_{ILK}	Input Leakage Current	Pins 27-34		±0.1	±1	µA
C_{IN}	Input Capacitance	Pins 27-34		5		pF
$I_{ILK(\overline{ON}/OFF)}$	$\overline{ON}$/OFF Input Leakage	All Devices		±0.1	±1	µA
$C_{IN(\overline{ON}/OFF)}$	$\overline{ON}$/OFF Input Capacitance	All Devices		200		pF
AC CHARACTERISTICS – MULTIPLEXED INPUT CONFIGURATION						
t_{WH}	Digit Select Active Pulse Width		1			µs
t_{DS}	Data Setup Time		500			ns
t_{DH}	Data Hold Time		200			ns
t_{IDS}	Inter-Digit Select Time		2			µs
AC CHARACTERISTICS – MICROPROCESSOR INTERFACE						
t_{WL}	$\overline{Chip}$ $\overline{Select}$ Active Pulse Width	Other $\overline{Chip}$ $\overline{Select}$ either held active, or both driven together	200			ns
t_{DS}	Data Setup Time		100			ns
t_{DH}	Data Hold Time		10	0		ns
t_{ICS}	Inter-$\overline{Chip}$ $\overline{Select}$ Time		2			µs

NOTES: 1. This limit refers to that of the package and will not be realized during normal operation.
2. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any input terminal to a voltage in excess of V_{DD} or V_{SS} may cause destructive device latch-up. For this reason, it is recommended that inputs from external sources operating on a different power supply be applied only after the device's own power supply has been established, and that on multiple supply systems the supply to the ICM7235 be turned on first.
3. This value refers to the display outputs only.

INPUT DEFINITIONS

In this table, V_{DD} and V_{SS} are considered to be normal operating input logic levels. Actual input low and high levels are specified under Operating Characteristics. For lowest power consumption, input signals should swing to either V_{DD} or V_{SS}.

INPUT	TERMINAL	TEST CONDITIONS	FUNCTION	
B0	27	V_{DD} = Logical One V_{SS} = Logical Zero	Ones (Least Significant)	Data Input Bits
B1	28	V_{DD} = Logical One V_{SS} = Logical Zero	Twos	
B2	29	V_{DD} = Logical One V_{SS} = Logical Zero	Fours	
B3	30	V_{DD} = Logical One V_{SS} = Logical Zero	Eights (Most Significant)	
$\overline{ON}$/OFF	5	V_{DD} = OFF, V_{SS} = ON		Display $\overline{ON}$/OFF Input

ICM7235, ICM7235A MULTIPLEXED-BINARY INPUT CONFIGURATION

INPUT	TERMINAL	TEST CONDITIONS	FUNCTION
D1	31	V_{DD} = Active V_{SS} = Inactive	D1 Digit Select (Least Significant)
D2	32		D2 Digit Select
D3	33		D3 Digit Select
D4	34		D4 Digit Select (Most Significant)

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7235M, ICM7235AM MICROPROCESSOR INTERFACE INPUT CONFIGURATION

INPUT	DESCRIPTION	TERMINAL	TEST CONDITIONS	FUNCTION
DA1	Digit ADDRESS Bit 1 (LSB)	31	V_{DD} = Logical One V_{SS} = Logical Zero	DA2 & DA1 serve as a two bit Digit Address Input DA2, DA1 = 00 selects D4 DA2, DA1 = 01 selects D3 DA2, DA1 = 10 selects D2 DA2, DA1 = 11 selects D1
DA2	Digit ADDRESS Bit 2 (MSB)	32		
$\overline{CS1}$	Chip Select 1	33	V_{DD} = Inactive V_{SS} = Active	When **both** $\overline{CS1}$ and $\overline{CS2}$ are taken to V_{SS} the data at the Data and Digit Address inputs are written into the input latches. On the rising edge of **either** Chip Select, the data is decoded and written into the output latches.
$\overline{CS2}$	Chip Select 2	34		

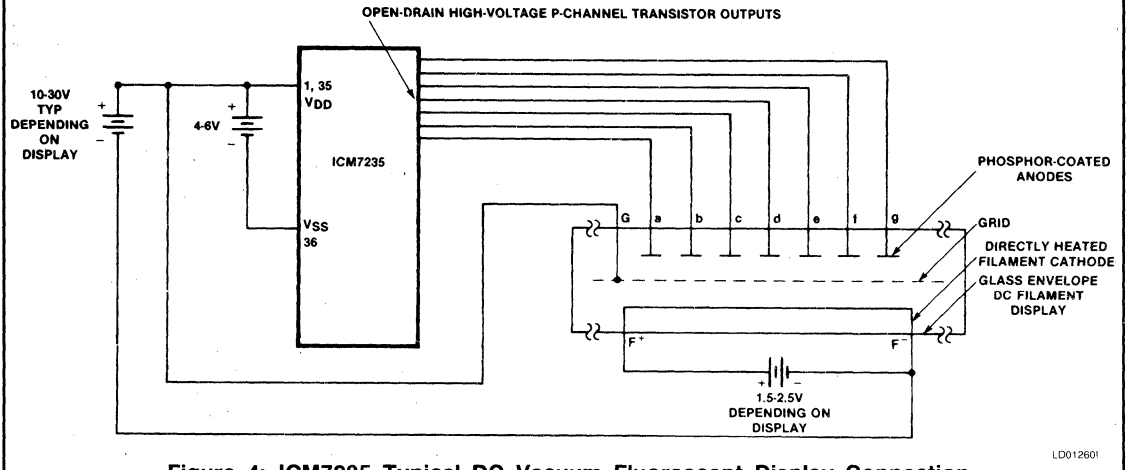


Figure 4: ICM7235 Typical DC Vacuum Fluorescent Display Connection

VACUUM FLUORESCENT DISPLAYS (4 DIGIT) AVAILABLE FROM:

N.E.C. Electronics, Inc.

Models FIP4F8S and FIP5F8S

CIRCUIT DESCRIPTION

Each device in the ICM7235 family provides signals for directly driving the anode terminals of a four-digit, 7-segment non-multiplexed vacuum fluorescent display. The outputs are taken from the drains of high-voltage, low-leakage P-channel FETs. Each is capable of withstanding $> -35V$ with respect to V_{DD}. In addition, the inclusion of an $\overline{ON}$/OFF input allows the user to disable all segments by connecting pin 5 to V_{DD}; this same input may also be used as a brightness control by applying a signal swinging between V_{DD} and V_{SS} and varying its duty cycle.

The ICM7235 may also be used to drive nonmultiplexed common cathode LED displays by connecting each segment output to its corresponding display input, and tying the common cathode to V_{SS}. Using a power supply of 5V and an LED with a forward drop of 1.7V results in an "ON" segment current of about 3mA, enough to provide sufficient brightness for displays of up to 0.3" character height.

Note that these devices have two V_{DD} terminals, and each should be connected to the positive supply voltage. This double connection is necessary to minimize the effects of bond wire resistance, which could be a problem due to the high display currents.

Input Configurations and Output Codes

The standard devices in the ICM7235 family accept a four-bit true binary (i.e., positive level = logical one) input at pins 27 through 30, least significant bit at pin 27 ascending to the most significant bit at pin 30. The ICM7235 and ICM7235M decode this binary input into a 7-segment alphanumeric hexadecimal output, while the ICM7235A and ICM7235AM decode the binary input into the same 7-segment output as the ICM7218 "Code B," i.e., 0–9, dash, E, H, L, P, blank. These codes are shown explicitly in Table 1. Either decoder option will correctly decode true BCD to a 7-segment decimal output.

These devices are actually mask-programmable to provide any 16 combinations of the 7-segment outputs decoded from the four input bits. For larger quantity orders, (10K pcs. minimum) custom decoder options can be arranged. Contact your Intersil Sales Office for details.

The ICM7235 and ICM7235A devices are intended to accept multiplexed binary or BCD output. These devices provide four separate Digit select lines (least significant digit at pin 31 ascending to most significant digit at pin 34). Each Digit Select line when taken to a positive level decodes and stores in its respective output latches the character corresponding to the data at the input port, pins 27 through 30.

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7235

The ICM7235M and 7235AM devices are intended to accept data from a data bus under processor control.

In these devices, the four data input bits and the 2-bit Digit Select code (DA1 pin 31, DA2 pin 32) are written into input buffer latches when both Chip Select inputs ($\overline{CS1}$ pin 33, $\overline{CS2}$ pin 34) are taken to V_{SS}. On the rising edge of either Chip Select input, the content of the data input latches is decoded and stored in the output latches of the digit selected by the contents of the select code latches. A select code of 00 writes into D4, 01 writes into D3, 10 writes into D2 and 11 writes into D1. The timing relationships for inputting data are shown in Figure 7, and the chip select pulse widths and data setup and hold times are specified under Operating Characteristics.

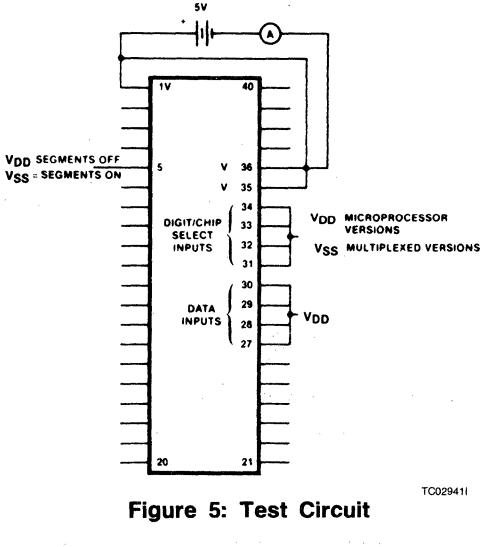
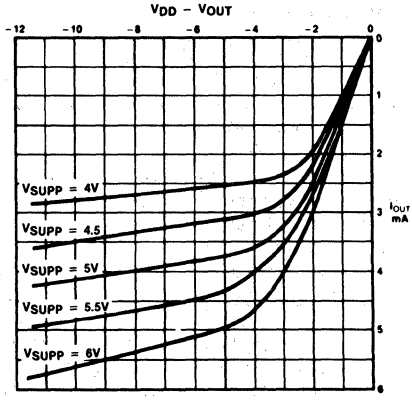


Figure 5: Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS



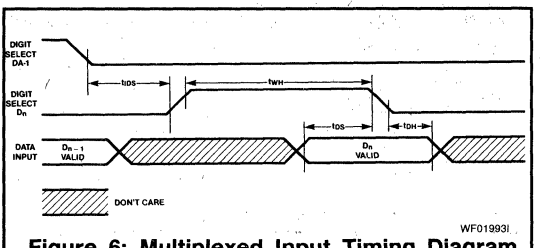


Figure 6: Multiplexed Input Timing Diagram

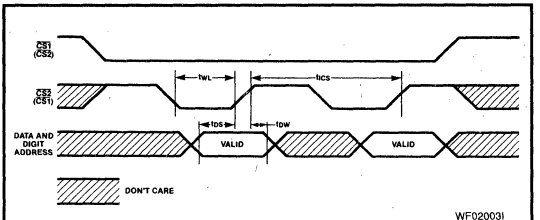


Figure 7: Microprocessor Interface Input Timing Diagram

TABLE 1: Output Codes

BINARY				HEXADECIMAL ICM7235 ICM7235M	CODE B ICM7235A ICM7235AM
B3	B2	B1	B0		
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	(BLANK)

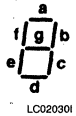


Figure 8: Segment Assignment

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7243
8-Character LED
μP-Compatible Display Driver

GENERAL DESCRIPTION

The ICM7243 is an 8-character alphanumeric display driver and controller which provides all the circuitry required to interface a microprocessor or digital system to a 14- or 16-segment display. It is primarily intended for use in microprocessor systems, where it minimizes hardware and software overhead. Incorporated on-chip are a 64-character ASCII decoder, 8 x 6 memory, high power character and segment drivers, and the multiplex scan circuitry.

Six-bit ASCII data to be displayed is written into the memory directly from the microprocessor data bus. Data location depends upon the selection of either **Serial** (MODE = 1) or **Random** (MODE = 0). In the **Serial Access** mode the first entry is stored in the lowest location and displayed in the "left-most" character position. Each subsequent entry is automatically stored in the next higher location and displayed to the immediate "right" of the previous entry. A DISPlay FULL signal is provided after 8 entries; this signal can be used for cascading. A $\overline{\text{CLeaR}}$ pin is provided to clear the memory and reset the location counter. The **Random Access** mode allows the processor to select the memory address and display digit for each input word.

The character multiplex scan runs whenever data is not being entered. It scans the memory and CHARacter drivers, and ensures that the decoding from memory to display is done in the proper sequence. Intercharacter blanking is provided to avoid display ghosting.

FEATURES

- **14- and 16-Segment Fonts With Decimal Point**
- **Mask Programmable For Other Font-Sets Up to 64 Characters**
- **Microprocessor Compatible**
- **Directly Drives Small Common Cathode Displays**
- **Cascadable Without Additional Hardware**
- **Standby Feature Turns Display Off; Puts Chip in Low Power Mode**
- **Serial Entry or Random Entry of Data Into Display**
- **Single +5V Operation**
- **Character and Segment Drivers, All MUX Scan Circuitry, 8 x 6 Static Memory and 64-Character ASCII Font Generator Included On-Chip**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7243AIJL	−20°C to +85°C	CERDIP
ICM7243BIJL	−20°C to +85°C	CERDIP
ICM7243B EV/KIT		
ICM7243BIPL	−20°C to +85°C	PLASTIC
ICM7243B/D	—	DICE
ICM7243BCPL	0°C to +70°C	PLASTIC

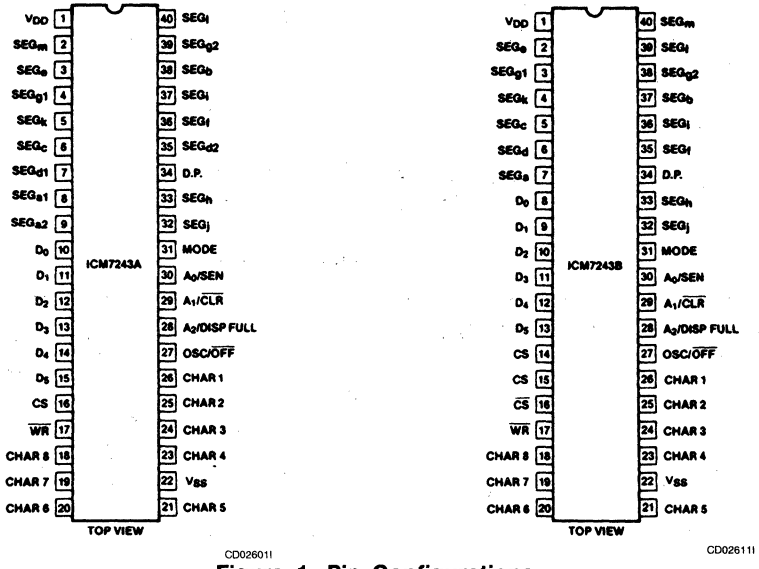


Figure 1: Pin Configurations

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7243

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD} - V_{SS}$) 6V
CHARacter Output Current 300mA
SEGment Output Current 30mA
Input Voltage (Any Terminal) ($V_{DD} + 0.3V$) to ($V_{SS} - 0.3V$)
Power Dissipation 1W

Operating Temperature Range (I) ..... −25°C to +85°C
(C) ..... 0°C to 70°C
Storage Temperature Range ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

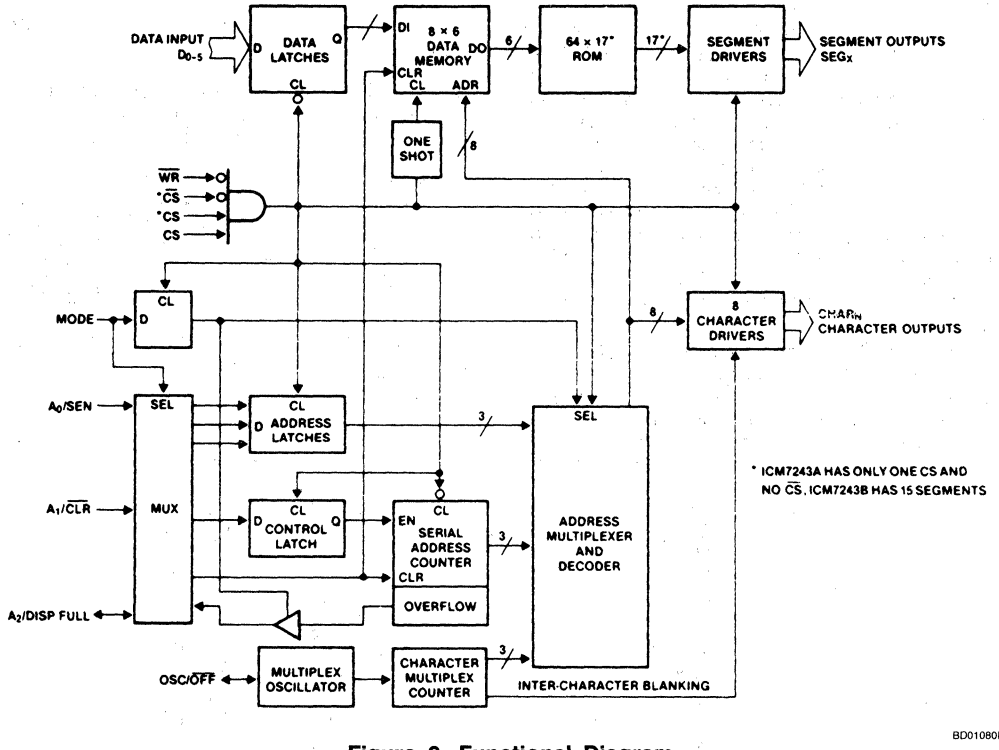


Figure 2: Functional Diagram

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5V, V_{SS} = 0V, T_A = 25°C unless otherwise stated)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{SUPP}	Supply Voltage ($V_{DD} - V_{SS}$)		4.75	5.0	5.25	V
I_{DD}	Operating Supply Current	V_{SUPP} = 5.25V, 10 Segments ON, All 8 Characters		180		mA
I_{STBY}	Quiescent Supply Current	V_{SUPP} = 5.25V, OSC/$\overline{OFF}$ Pin < 0.5V, CS = V_{SS}		30	250	µA
V_{IH}	Input High Voltage		2			V
V_{IL}	Input Low Voltage				0.8	V
I_{IN}	Input Current		−10		+10	µA
I_{CHAR}	CHARacter Drive Current	V_{SUPP} = 5V, V_{OUT} = 1V	140	190		mA
I_{CHLK}	CHARacter Leakage Current				100	µA
I_{SEG}	SEGment Drive Current	V_{SUPP} = 5V, V_{OUT} = 2.5V	14	19		mA

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7243

DC ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I_{SLK}	SEGment Leakage Current			0.01	10	μA
V_{OL}	DISPlay FULL Output Low	I_{OL} = 1.6mA			0.4	V
V_{OH}	DISPlay FULL Output High	I_{IH} = 100μA	2.4			V
f_{ds}	Display Scan Rate			400		Hz

AC ELECTRICAL CHARACTERISTICS (Drive levels 0.4V and 2.4V, timing measured at 0.8V and 2.0V. V_{DD} = 5V, T_A = 25°C unless otherwise stated).

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{WPI}	$\overline{WR}$, $\overline{CLeaR}$ Pulse Width Low		250			ns
t_{WPH}	$\overline{WR}$, $\overline{CLeaR}$ Pulse Width High (Note 1)		250			
t_{DH}	Data Hold Time		0	-100		
t_{DS}	Data Setup Time		250	150		
t_{AH}	Address Hold Time		125			
t_{AS}	Address Setup Time		40	15		
t_{CS}	CS, $\overline{CS}$ Setup Time		0			
t_T	Pulse Transition Time				100	
t_{SEN}	SEN Setup Time		0	-25		
t_{WDF}	Display Full Delay		600	480		

CAPACITANCE

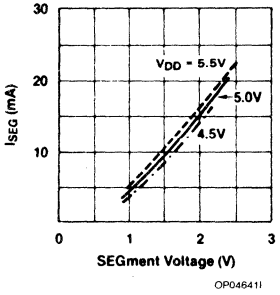
SYMBOL	TEST	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance (Note 2)		5		pF
C_O	Output Capacitance (Note 2)		5		pF

*Not tested. (Guaranteed)

NOTES: 1. In Serial mode $\overline{WR}$ high must be $\geq T_{SEN} + T_{WDF}$.
2. For design reference only, not 100% tested.

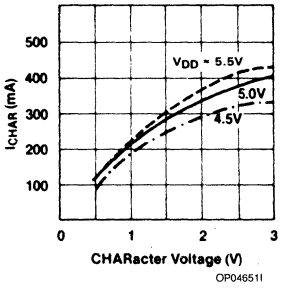
TYPICAL PERFORMANCE CHARACTERISTICS

SEGment Current vs Output Voltage



OP04641I

CHARacter Current vs Output Voltage



OP04651I

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7243A/B DISPLAY FONT AND SEGMENT ASSIGNMENTS

Note: Some display manufacturers use different designations for some of the segments. Check data sheets carefully.

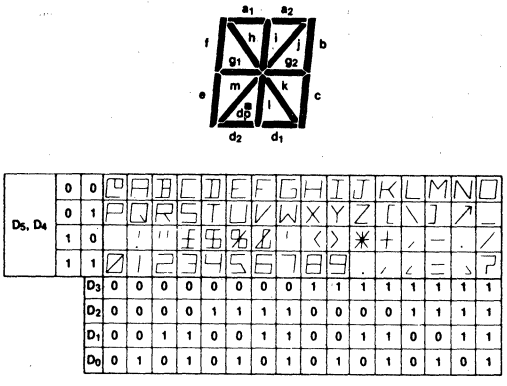
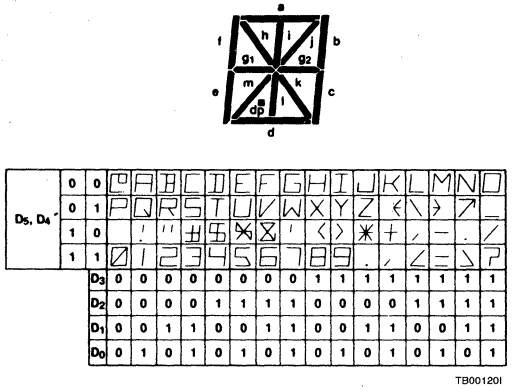


Figure 3: ICM7243A 16-Segment Character Font with Decimal Point



NOTE: Segments a and d appear as 2 segments each, but both halves are driven together.

Figure 4: ICM7243B 14-Segment Character Font with Decimal Point

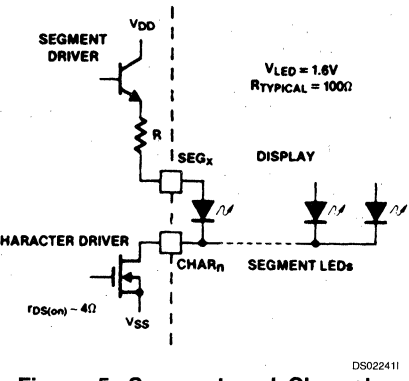


Figure 5: Segment and Character Drivers Output Circuit

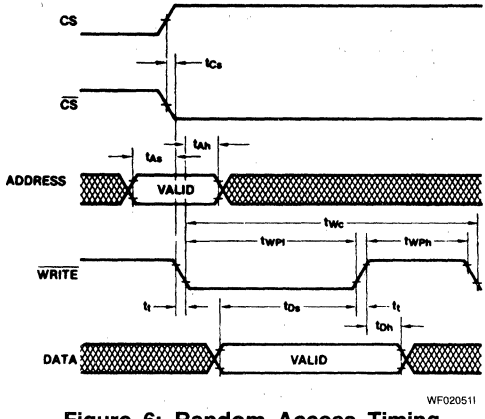


Figure 6: Random Access Timing

Note: All typical values have been guaranteed by characterization and are not tested.

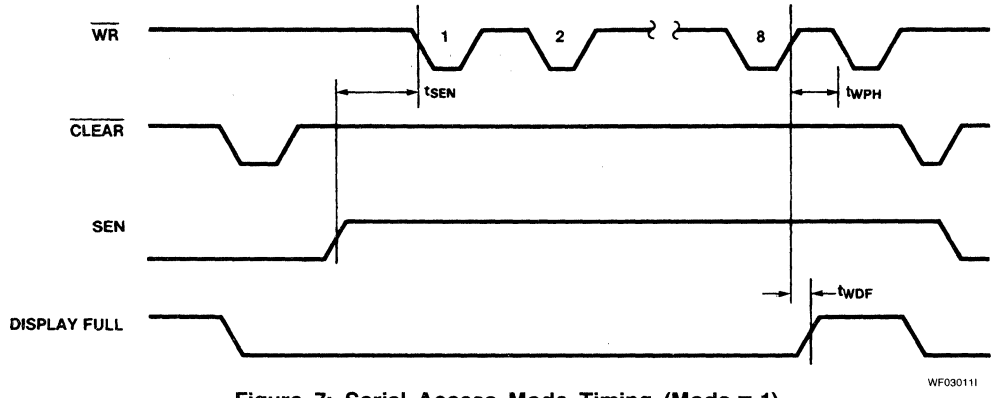


Figure 7: Serial Access Mode Timing (Mode = 1)

TABLE 1: PIN DESCRIPTIONS, ICM7243A*(B)*

SIGNAL	PIN	FUNCTION
$D_0 - D_5$	10–15 *(8 – 13)*	Six-Bit ASCII Data input pins (active high).
CS, $\overline{CS}$	16 *(14–16)*	Chip Select for decoding from μP address bus, etc.
$\overline{WR}$	17	WRite pulse input pin (active low). For an active high write pulse, CS can be used, and $\overline{WR}$ can be used as $\overline{CS}$.
MODE	31	Selects data entry MODE. High selects **Serial Access (SA)** mode where first entry is displayed in "leftmost" character and subsequent entries appear to the "right". Low selects the **Random Access (RA)** mode where data is displayed on the character addressed via $A_0 - A_2$ Address pins.
A_0/SEN	30	In **RA** mode it is the LSB of the character Address. In **SA** mode it is used for cascading display driver/controllers for displays of more than 8 characters (active high enables driver controller).
$A_1/\overline{CLeaR}$	29	In **RA** mode this is the second bit of the address. In **SA** mode, a low input will CLeaR the Serial Address Counter, the Data Memory and the display.
A_2/DISPlay FULL	28	In **RA** mode this is the MSB of the Address. In **SA** mode, the output goes high after eight entries, indicating DISPlay FULL.
OSC/$\overline{OFF}$	27	OSCillator input pin. Adding capacitance to V_{DD} will lower the internal oscillator frequency. An external oscillator is also applied to this pin. A low puts the display controller/driver into a quiescent mode, shutting OFF the display and oscillator but retaining data stored in memory.
$SEG_a - SEG_m$, D.P.	2 – 9 *(7)*, 32 – 40	SEGment driver outputs.
CHARacter 1 – 8	18 – 21, 23 – 26	CHARacter driver outputs.

8

Note: All typical values have been guaranteed by characterization and are not tested.

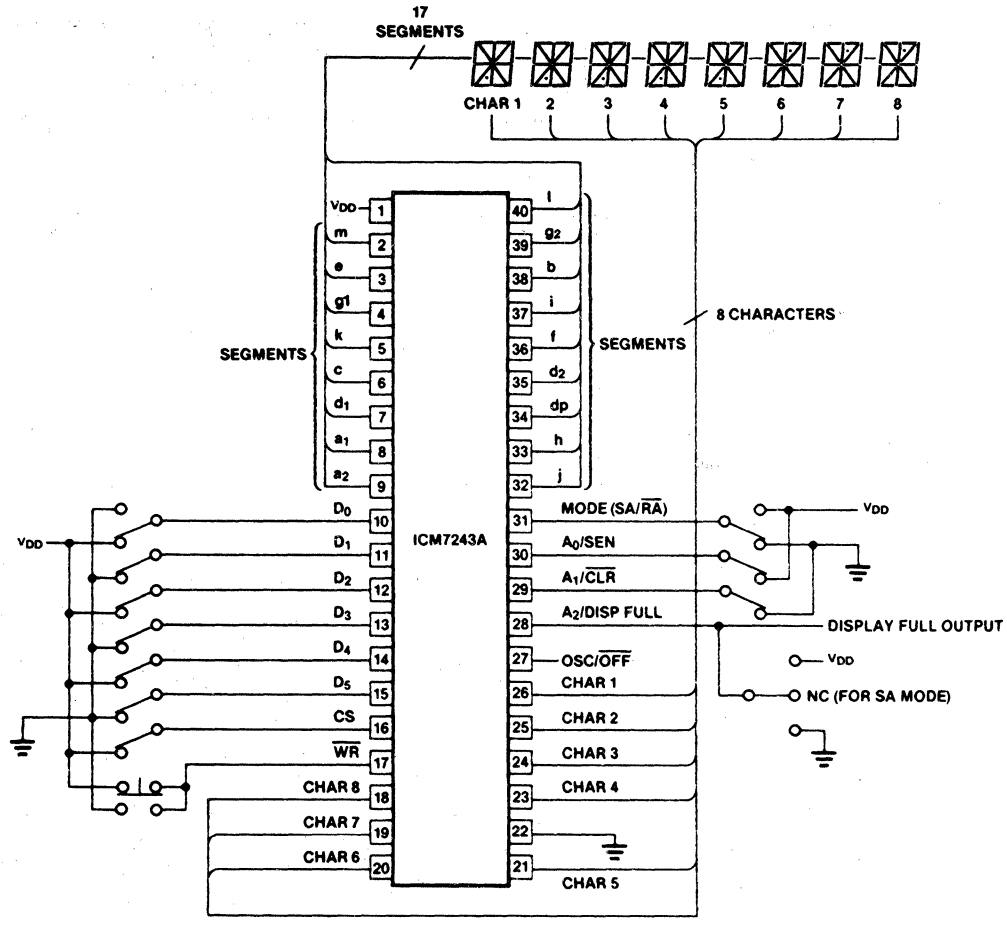


Figure 8: Test Circuit

DETAILED DESCRIPTION

$\overline{WR}$, $\overline{CS}$, CS. These pins are immediately functionally ANDed, so all actions described as occurring on an edge of $\overline{WR}$, with CS and $\overline{CS}$ enabled, will occur on the equivalent (last) enabling or (first) disabling edge of any of these inputs. The delays from CS pins are slightly (about 5ns) greater than from $\overline{WR}$ or $\overline{CS}$ due to the additional inverter required on the former.

MODE. The MODE pin input is latched on the falling edge of $\overline{WR}$ (or its equivalent, see above). The location in Data Memory where incoming data will be placed is determined either from the Address pins or the Serial Address Counter, under control of this latch, which also controls the function of A_0/SEN, $A_1/\overline{CLR}$, and A_2/DISPlay FULL.

Random Access Mode. When the internal mode latch is set for **Random Access (RA)** (MODE latched low), the Address input on A_0, A_1 and A_2 will be latched by the falling edge of $\overline{WR}$ (or its equivalent). Subsequent changes on the Address lines will not affect device operation. This allows use of a multiplexed 6-bit bus controlling both address and data, with timing controlled by $\overline{WR}$.

Serial Access Mode. If the internal latch is set for **Serial Access (SA),** (MODE latched high), the Serial ENable input on SEN will be latched on the falling edge of $\overline{WR}$ (or its equivalent). The $\overline{CLR}$ input is asynchronous, and will force-clear the Serial Address Counter to address 000 (CHARacter 1), and set all Data Memory contents to 100000 (blank) at any time. The DISPlay FULL output is always active in **SA** mode also, and indicates the overflow status of the Serial Address Counter. If this output is low, and SEN is (latched as) high, the contents of the Counter will be used to establish the Data Memory location for the Data input. The Counter is then incremented on the rising edge of $\overline{WR}$. If SEN is low, or DISPlay FULL is high, no action will occur.

Note: All typical values have been guaranteed by characterization and are not tested.

This allows easy "daisy-chaining" of display drivers for multiple character displays in a **Serial Access** mode.

Changing Modes. Care must be exercised in any application involving changing from one mode to another. The change will occur only on a falling edge of $\overline{WR}$ (or its equivalent). When changing mode from **Serial Access** to **Random Access**, note that A_2/DISPlay FULL will be an output until $\overline{WR}$ has fallen low, and an Address drive here could cause a conflict. When changing from **Random Access** to **Serial Access**, $A_1/\overline{CLR}$ should be high to avoid inadvertent clearing of the Data Memory and Serial Address Counter. DISPlay FULL will become active immediately after the falling edge of $\overline{WR}$.

Data Entry. The input Data is latched on the rising edge of $\overline{WR}$ (or its equivalent) and then stored in the Data Memory location determined as described above. The six Data bits can be multiplexed with the Address information on the same lines in **Random Access** mode. Timing is controlled by the $\overline{WR}$ input.

OSC/$\overline{OFF}$. The device includes a one-pin relaxation oscillator with an internal capacitor and a nominal frequency of 200kHz. By adding external capacitance to V_{DD} at the OSC/$\overline{OFF}$ pin, this frequency can be reduced as far as desired. Alternatively, an external signal can be injected on this pin. The oscillator (or external) frequency is pre-divided by 64, and then further divided by 8 in the Multiplex Counter, to drive the CHARacter strobe lines (see **Display Output).** An intercharacter blanking signal is derived from the pre-divider. An additional comparator on the OSC/$\overline{OFF}$ input detects a level lower than the relaxation oscillator's range, and blanks the display, disables the DISPlay FULL output (if active), and clears the pre-divider and Mutliplex Counter. This puts the circuit in a low-power-dissipation mode in which all outputs are effectively open circuits, except for parasitic diodes to the supply lines. Thus a display connected to the output may be driven by another circuit (including another ICM7243) without driver conflicts.

Display Output. The address output of the Multiplex Counter is multiplexed into the address input of the Data Memory, except during $\overline{WR}$ operations (in **Serial Access** mode, with SEN high and DISPlay FULL low), to control display operations. The address decoder also drives the CHARacter outputs, except during the inter-character blanking interval (nominally about 5μs). Each CHARacter output lasts nominally about 300μs, and is repeated nominally every 2.5ms, i.e., at a 400Hz rate (times are based on internal oscillator without external capacitor).

The 6 bits read from the Data Memory are decoded in the ROM to the 17 (15 for ICM7243B) segment signals, which drive the SEGment outputs. Both CHARacter and SEGment outputs are disabled during $\overline{WR}$ operations (with SEN high and DISPlay FULL Low for **Serial Access** mode). The outputs may also be disabled by pulling OSC/$\overline{OFF}$ low.

The decode pattern from 6 bits to 17 (15) segments is done by a ROM pattern according to the ASCII font shown. Custom decode patterns can be arranged, within these limitations, by consultation with the factory.

APPLICATIONS

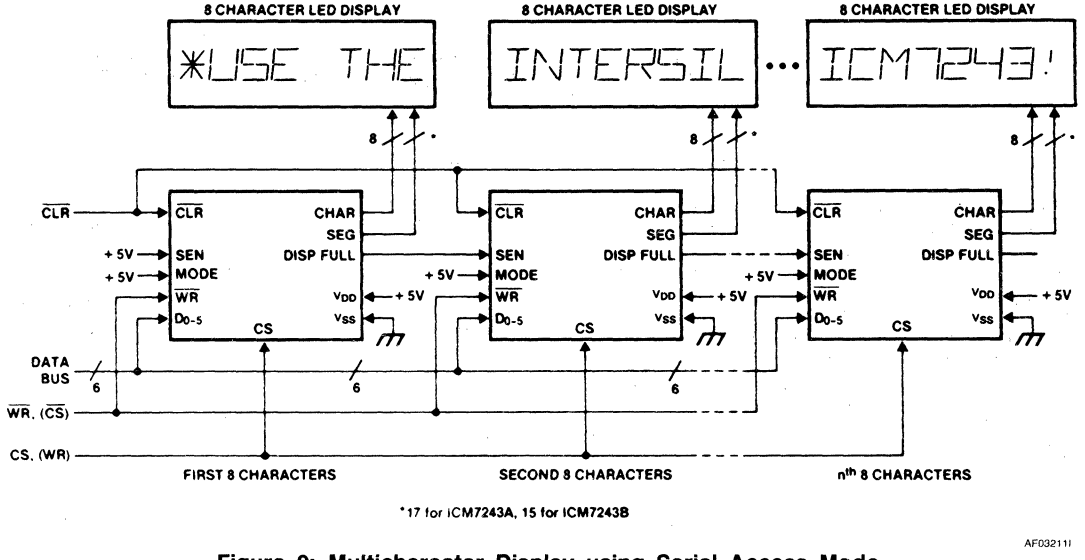


Figure 9: Multicharacter Display using Serial Access Mode

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7243

APPLICATIONS (CONT.)

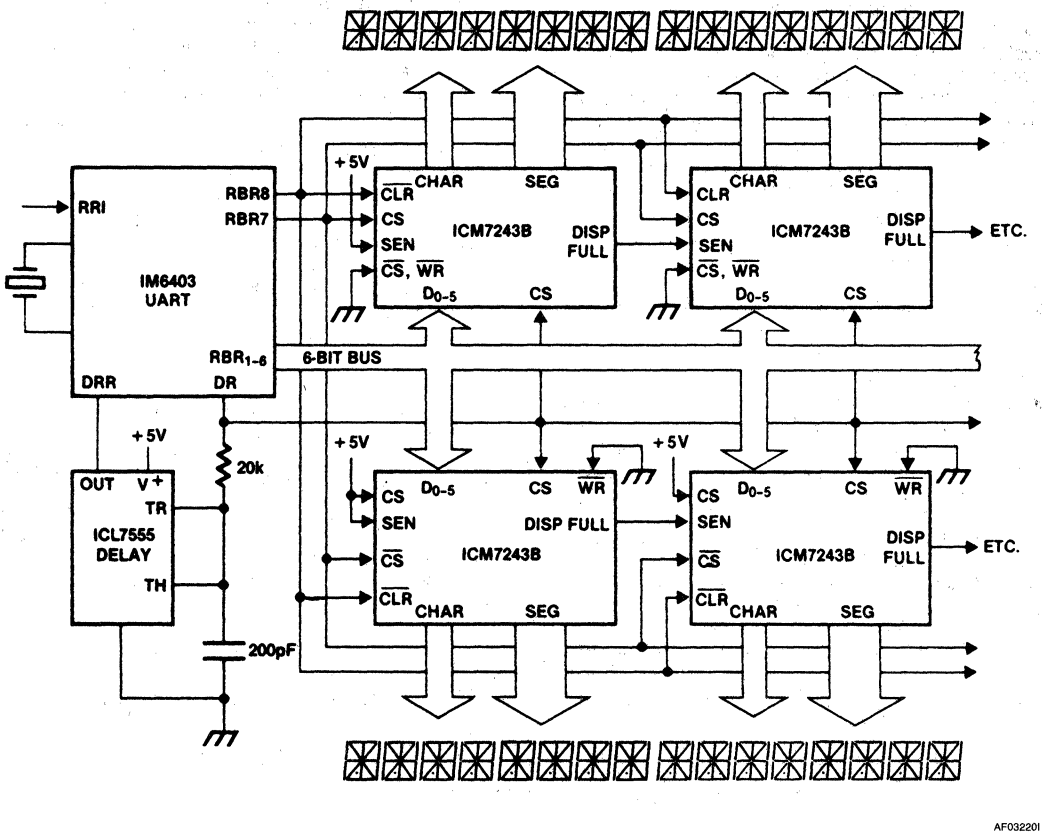


Figure 10: Driving Two Rows of Characters from a Serial Input.

UART converts data stream to parallel bytes. Bit 7 of each word sets which row data will be entered into. Bit 8 will blank and reset whole display if low. Each MODE pin should be tied high. ICM7243A can also be used, with inverter on RBR7 for one row.

COMPONENT SELECTION

Displays suitable for use with the ICM7243 may be obtained from the following manufacturers; among others:

Hewlett Packard Components, Palo Alto, California (415) 857-6620 (part #HDSP6508, HDSP6300)

General Instruments Inc., Palo Alto, California (415) 493-0400 (part #MAN2815)

Texas Instruments Inc., Dallas, Texas (214) 995-6611 (part #HDSP6508)

A.N.D., Burlingame, California (415) 347-9916 (part #AND370R)

IEE Inc., Van Nuys, California (213) 787-0311 (part #LR3784R)

Note: All typical values have been guaranteed by characterization and are not tested.

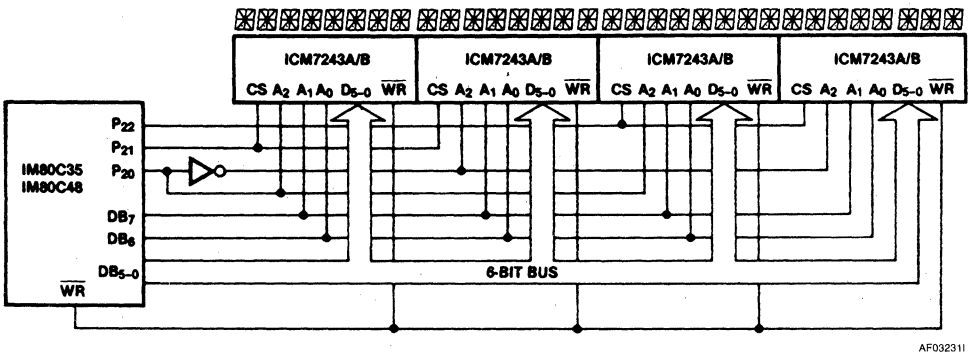
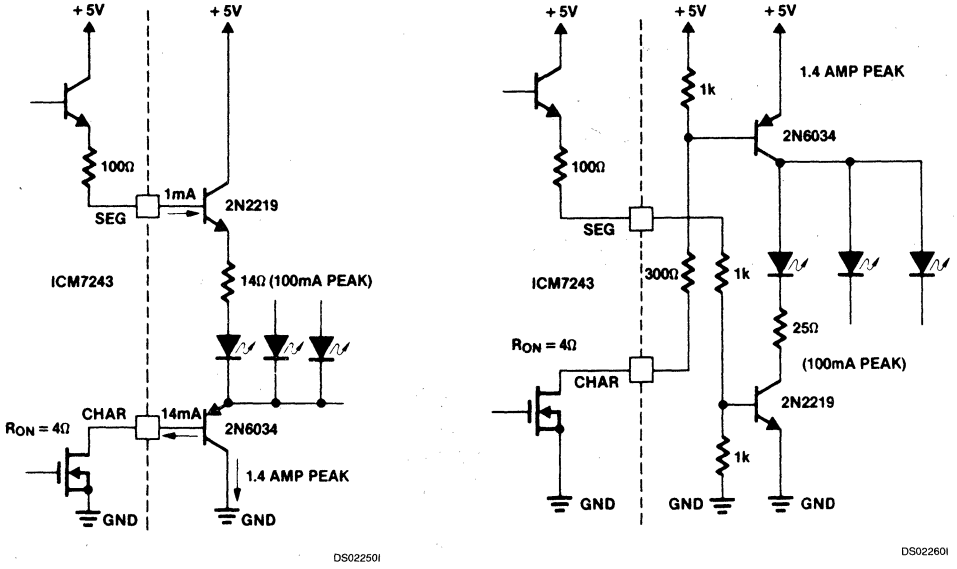


Figure 11: Random Access 32-Character Display in IM80C48 system.

One port line controls A_2, other two are CS lines. 8-bit data bus drives 6 data and 2 address lines. MODE should be GrouNDed on each part.



(5a.) Common Cathode Displays **(5b.) Common Anode Displays**

Figure 12: Driving Large Displays.

The circuits of Figures 12a and 12b can be used to drive 0.5" or larger alphanumeric displays, either common cathode (12a) or common anode (12b).

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7280
Dot Matrix LCD Controller/Row Driver

GENERAL DESCRIPTION

The ICM7280 is designed to provide a complete microprocessor interface for an 80-character alphanumeric LCD display system. It includes a character generator, display voltage generator and resistor string, row drivers, and control circuitry. Interface to a host microprocessor is achieved through either a multiplexed or non-multiplexed parallel bus.

The ICM7280 is designed to offload all display-related tasks from the host microprocessor and to provide an easy-to-program software interface. Since the internal circuitry operates at full microprocessor speeds, there is no waiting for completion of internal operations. Testing of a "Busy" flag, when characters or commands are written, is not required.

Character data can be loaded with an auto-incremented cursor or in a random-access mode. Versatile control functions allow all or selected portions of the display to be underlined, blinked, blanked, or displayed in reverse video. Display start offset and power-down features are provided, and both an underline and a blinking-box cursor are available.

The ICM7280 can display four user-defined characters in addition to the standard 96 ASCII upper and lower-case characters and 14 European and graphics characters.

ORDERING INFORMATION

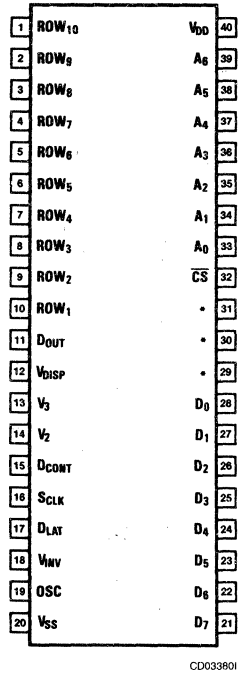
PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7280AIPL	−40°C to +85°C	40-Pin Plastic DIP
ICM7280AIJL	−40°C to +85°C	40-Pin CERDIP
ICM7280A/D	—	DIE
ICM7280BIPL	−40°C to +85°C	40-Pin Plastic DIP
ICM7280BIJL	−40°C to +85°C	40-Pin CERDIP
ICM7280B/D	—	DIE

FEATURES

- **80 Character Wide Display Memory**
  - **Directly Drives 10 ICM7281 Column Drivers**
- **High Speed μP Interface**
  - **ICM7280A: Intel, Zilog Compatible**
  - **ICM7280B: Motorola, Rockwell Compatible**
- **120 Character Font With Multiple Attributes**
  - **Underline, Cursor, Blinking, Reverse**
- **4 User Definable Characters**
- **Versatile Character Font Matrix**
  - **5 or 6 Columns By 7 to 10 Rows**
- **High Speed Internal Architecture**
  - **No Busy Flag Needed**

APPLICATIONS

- **Battery Hand-Held Terminals**
- **Portable Computers**
- **Instrument Control Panels**
- **LCD Display Modules**



CD03380I

PART #	PIN 29	PIN 30	PIN 31
7280A	$\overline{RD}$	$\overline{WR}$	ALE
7280B	E	R/$\overline{W}$	AS

Figure 1: Pin Configuration

Note: All typical values have been guaranteed by characterization and are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD} - V_{SS}) ..... +6.5V
Display Voltage (V_{DD} - V_{DISP}) ..... +12V
Input Voltage ..... V_{SS} -0.5V to V_{DD} +0.5V
Power Dissipation ..... 500mW @ 70°C

Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

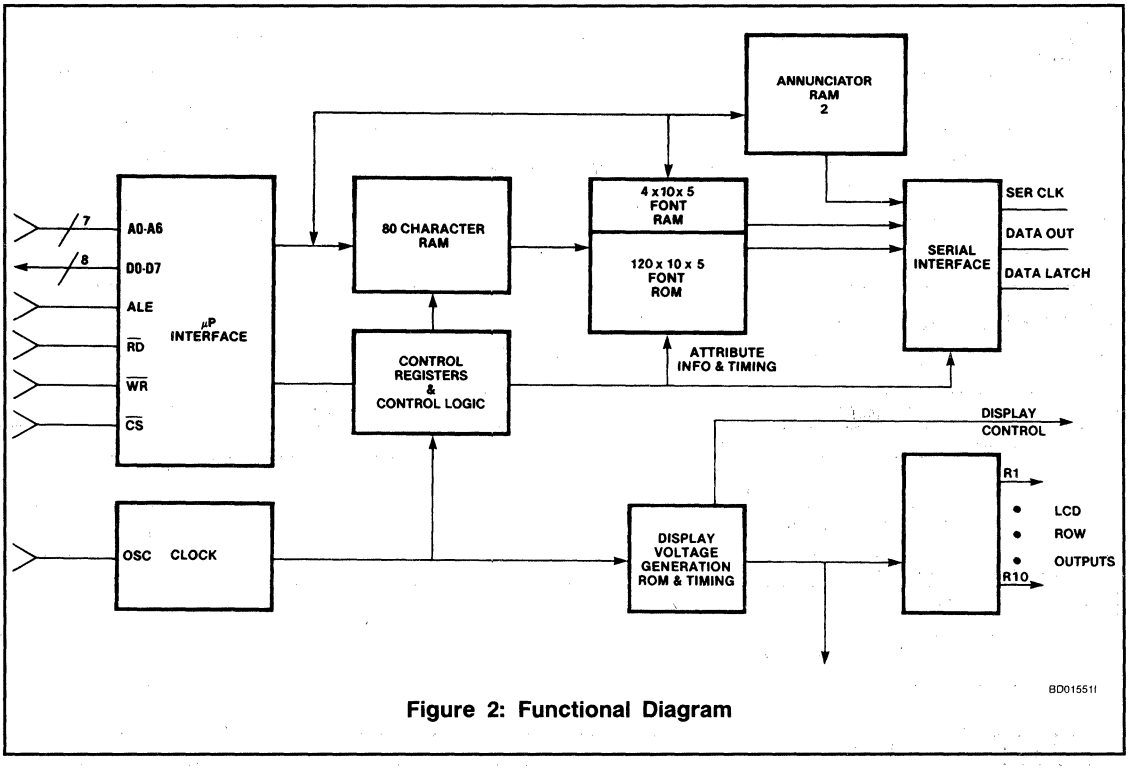


Figure 2: Functional Diagram

ELECTRICAL CHARACTERISTICS
AC CHARACTERISTICS

(V_{DD} = 5.0V±10%, T_A = -40 to +85°C, V_{DISP} = V_{DD} -8V, V_{SS} = 0V, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL}	Input Leakage	Address/Data pins high impedance $0 < V_{IN} < V_{DD}$	-10		+10	µA
I_{SS}	Supply Current	Osc open ckt, V_{IL} = 0V, V_{IH} = V_{DD}			2.5	mA
I_{STBY}	Shutdown Current	V_{IL} = 0V, V_{IH} = V_{DD}			100	µA
V_{SUPP}	Operating Voltage Range		4.5		5.5	V
f_{OSC}	Osc. Frequency	Osc. open ckt.	0.2		1.0	MHz
Serial Outputs						
V_{OL}	Output Voltage, Low	I_{OL} = 1mA			1.0	V

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7280

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output Voltage, High	I_{OH} = 1mA	V_{DD} – 1.0			V
Data I/O, μP Interface Inputs						
V_{OL}	Output Voltage, Low	I_{OL} = 1.6mA			0.4	V
V_{OH}	Output Voltage, High	I_{OH} = 400μA	2.4			V
V_{IL}	Input Voltage, Low				0.8	V
V_{IH}	Input Voltage, High		3.0			V
Row Driver Outputs						
R_{ON}	Output Resistance, ON	D_{CONT} high, $V_O = V_{DISP} + 0.5V$ D_{CONT} low, $V_O = -0.5V$			1	kΩ
R_{OFF}	Output Resistance, OFF	D_{CONT} high, $V_O = V_4 \pm .5V$ D_{CONT} low, $V_O = V_1 \pm 0.5V$			2.5	kΩ
V_1		D_{CONT} high	–1.5	–1.0	0.5	V
V_2, V_3			0.5	1.0	1.0	V
V_4		D_{CONT} low	2.5	3.0	3.5	V

AC CHARACTERISTICS (See Timing Diagram)

(V_{DD} = 5.0V±10%, V_{DISP} = 0V, V_{SS} = 0V, T_A = –40 to +85°C, C_L = 150pF, unless otherwise specified.)

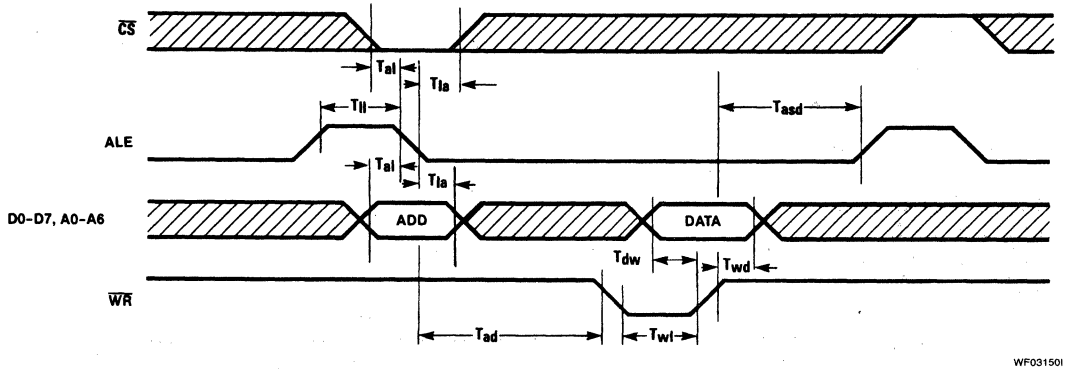
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Serial Output Timing						
T_{scdl}	Prop. Delay S_{CLK} to D_{LAT}				200	ns
T_{scdo}	Prop Delay S_{CLK} to D_{OUT}				400	ns
Microprocessor Interface						
T_{LL}	ALE/AS Pulse Width, High		55			ns
T_{AL}	Address to ALE Setup time		30			ns
T_{la}	Address to ALE Hold Time		30			ns
Intel/Zilog Option (ICM7280A)						
T_{ad}	Address Setup Time		50			ns
T_{ah}	Address Hold Time		30			ns
T_{wl}	WRITE Pulse Width, Low		100			ns
T_{dw}	Data to WRITE Setup Time		150			ns
T_{wd}	Data to WRITE Hold Time		30			ns
T_{rd}	READ to Valid Data				550	ns
T_{rx}	READ to Data Hold Time				150	ns
T_{asd}	ALE Setup Time		60			ns
Motorola/Rockwell Option (ICM7280B)						
T_{ad}	Address to E Setup Time		50			ns
T_{ah}	Address to E Hold Time		30			ns

Note: All typical values have been guaranteed by characterization and are not tested.

AC CHARACTERISTICS (See Timing Diagram) (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{ee}	E Pulse Width, High		200			ns
T_{dw}	Data to E Setup Time		100			ns
T_{wd}	Data to E Hold Time		30			ns
T_{rd}	E to Valid Data	T_{ee} = 400ns			550	ns
T_{rx}	E to Data Hold Time				150	ns
T_{asd}	E to AS Setup Time		60			ns

WRITE CYCLE TIMING ($\overline{RD}$ = "1")



READ CYCLE TIMING ($\overline{WR}$ = "1")

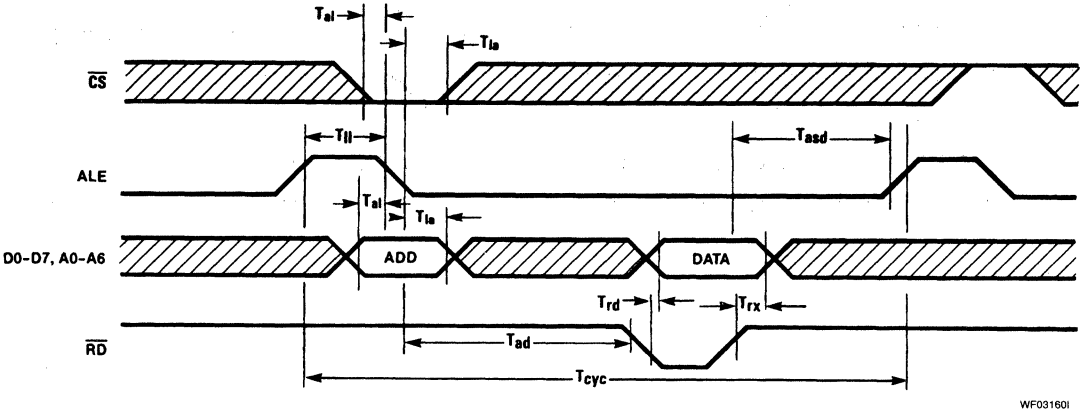
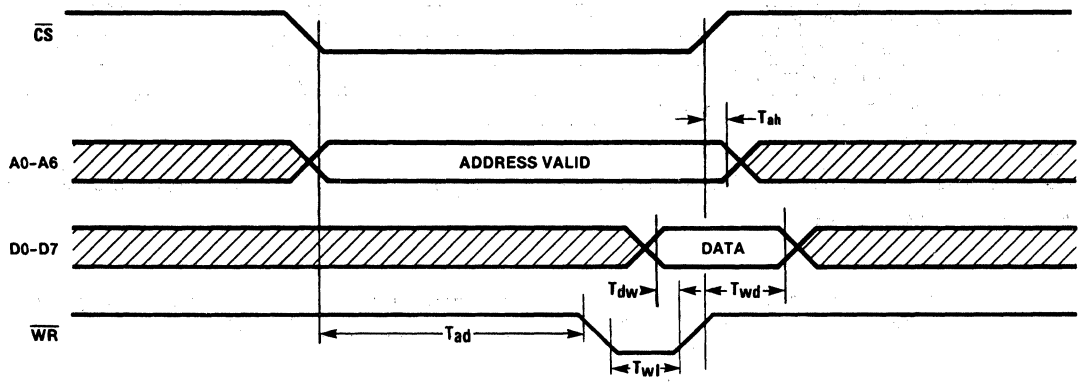


Figure 3: ICM7280A Timing Diagrams (Multiplexed Operation)

Note: All typical values have been guaranteed by characterization and are not tested.

WRITE CYCLE TIMING ($\overline{RD}$ = "1") (ALE = "1")



READ CYCLE TIMING ($\overline{WR}$ = "1")

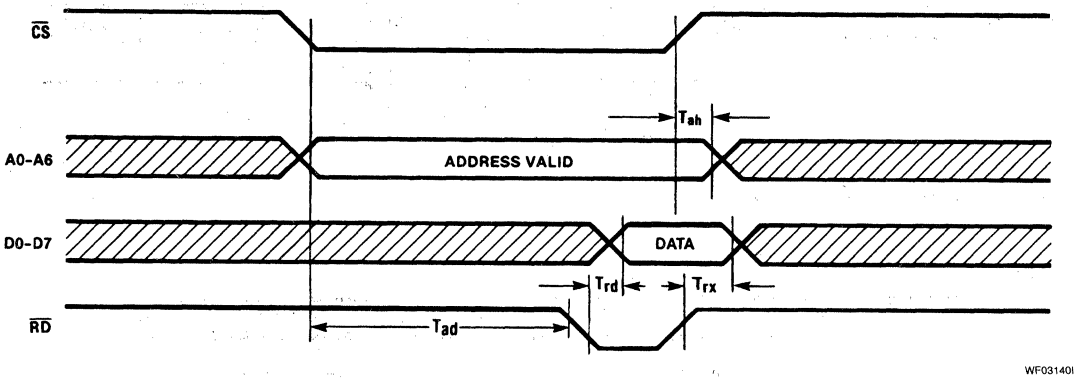
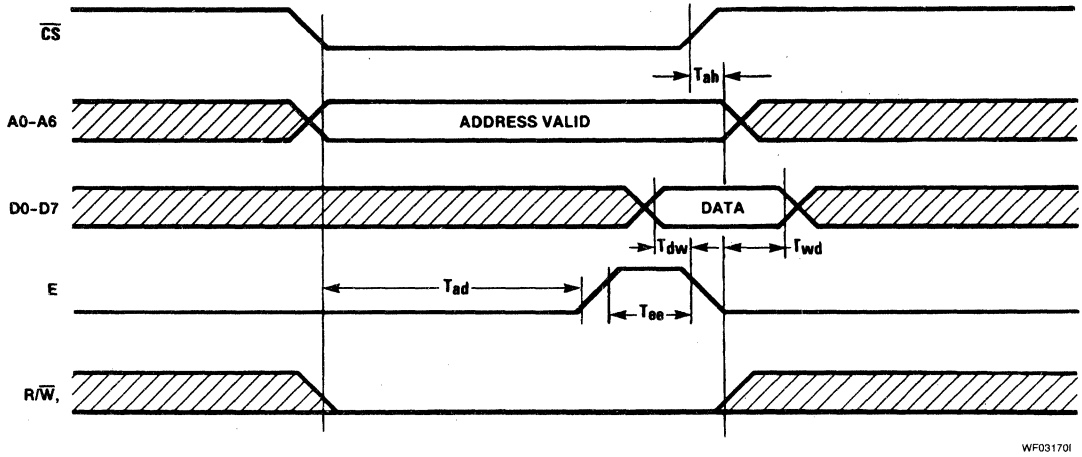


Figure 4: ICM7280A Timing Diagrams (Non-Multiplexed Operation)

Note: All typical values have been guaranteed by characterization and are not tested.

WRITE CYCLE TIMING (AS = "1")



READ CYCLE TIMING (AS = "1")

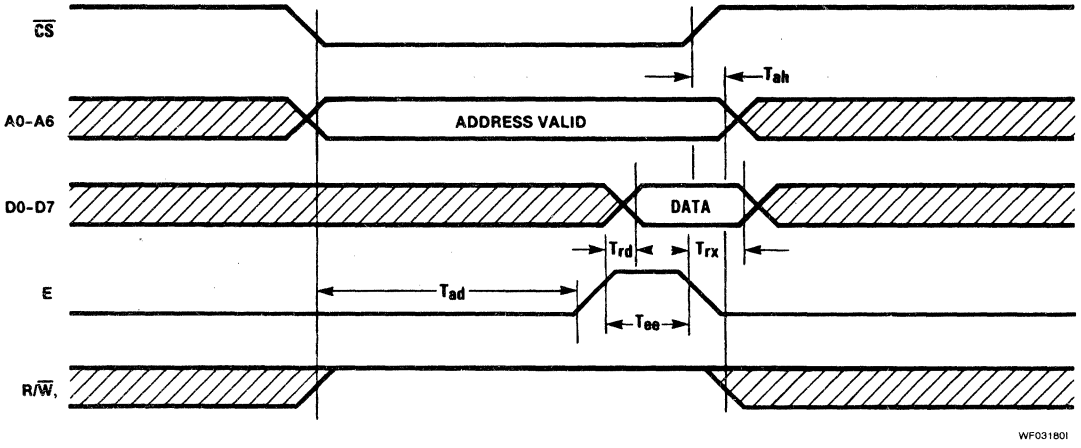
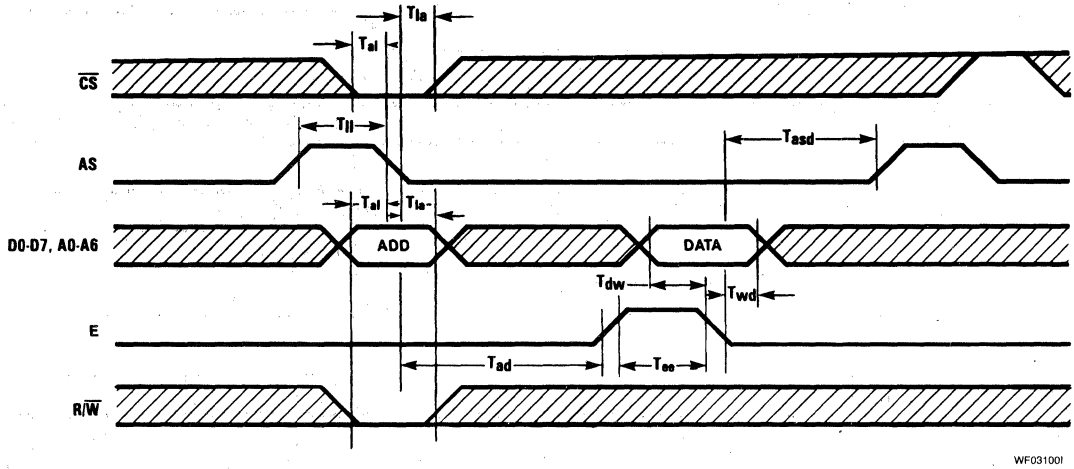


Figure 5: ICM7280B Timing Diagrams (Non-Multiplexed Operation)

8

Note: All typical values have been guaranteed by characterization and are not tested.

WRITE CYCLE TIMING



READ CYCLE TIMING

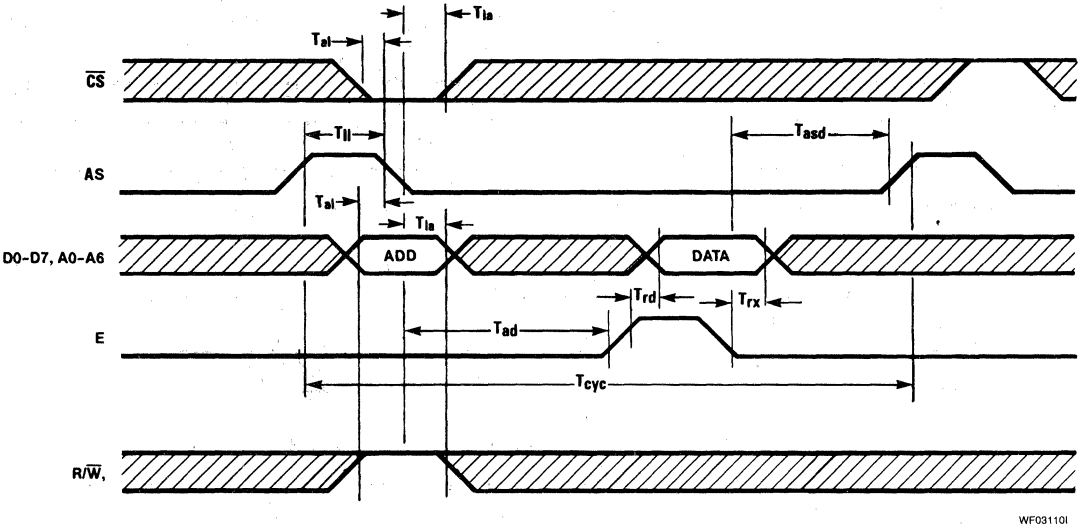


Figure 6: ICM7280B Timing Diagrams (Multiplexed Operation)

Note: All typical values have been guaranteed by characterization and are not tested.

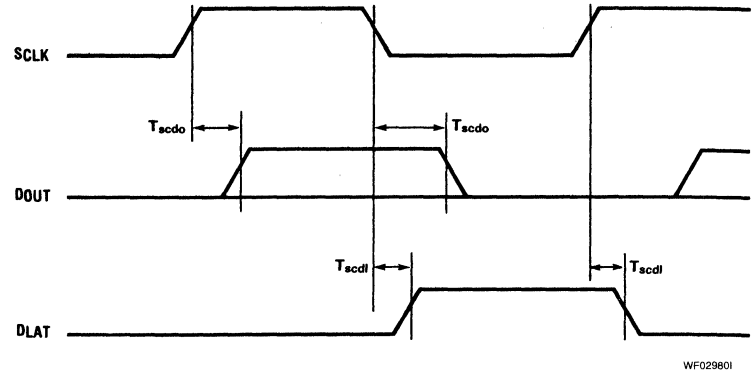


Figure 7: ICM7280 Serial Output Timing Diagram

Table 1: Pin Descriptions

SIGNAL	PIN	DESCRIPTION
ROW10–1	1–10	LCD row drivers
D_{OUT}	11	Serial data
V_{DISP}	12	Negative LCD supply voltage
V2, V3	13, 14	LCD column voltage
D_{CONT}	15	Column driver control output
S_{CLK}	16	Serial data clock output
D_{LAT}	17	Row data latch output
V_{INV}	18	Negative voltage generator clock
OSC	19	Oscillator input
V_{SS}	20	Digital ground
D0–D7	28–21	Data I/O
$\overline{RD}$(7280A) E(7280B)	29 29	Read input Enable input
$\overline{WR}$(7280A) R/$\overline{WR}$(7280B)	30 30	Write input Read/write input
ALE(7280A) AS(7280B)	31 31	Address latch enable Address strobe
$\overline{CS}$	32	Chip select input
A0–A6	39–33	Address inputs
V_{DD}	40	Positive digital and LCD supply voltage

DETAILED DESCRIPTION

Hardware Interface

Figure 1 is a simplified block diagram of the ICM7280. It is a dedicated hardware IC and the speed of data entry and command processing is limited only by gate delays. Unlike other display controllers, the ICM7280 will not "go busy" for milliseconds at a time while processing data or commands.

Microprocessor Bus Interface

There are two versions of the ICM7280. The ICM7280A has $\overline{WR}$ and $\overline{RD}$ pins, as well as ALE and $\overline{CS}$. This version can be interfaced to standard multiplexed or non-multiplexed data buses of parts such as the 8085, Z80, 8088 and other microprocessors. The ICM7280B has R/$\overline{W}$, E and AS pins instead of $\overline{WR}$ and $\overline{RD}$ and ALE. The ICM7280B is intended for use on 6800 and 6500 family buses.

To use the ICM7280 on a multiplexed bus, tie the A0-A6 lines to the D0-D6 lines and ALE/AS driven with the system address latch enable or strobe signal. For a non-multiplexed bus, A0-A6 should be connected to the least significant address lines, D0-D7 connected to the data bus and ALE/AS tied high. The only external circuitry needed is a chip select or address decoder. The ICM7280 uses an address space of 128 bytes.

ICM7281 Data Interface

The ICM7280 Row Drivers require ICM7281 Column Drivers to operate an LCD display. Three lines are used to load data serially into the ICM7281 column drivers, D_{OUT}, S_{CLK}, and D_{LAT}. The data is latched and shifted with each negative going edge of S_{CLK}, and the data is transferred from the ICM7281 shift register to its latches with the negative going edge of D_{LAT}. The frequency of the S_{CLK} is set by the oscillator frequency of the ICM7280 and is normally about 600kHz.

Oscillator

The ICM7280 oscillator will free run at 600kHz in die form, when not loaded with any capacitance. With 15pF of external capacitance at pin 19, the frequency will be about 250kHz. Figure 8 shows the relationship between oscillator period and the value of $C_{external}$. Table 1 shows the relationship between the oscillator frequency and various display system signals and features. Standard CMOS logic gates can be used to overdrive the oscillator to control frequency. A suitable frequency can also be derived by dividing down the host processor's clock.

8

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7280

Table 2: ICM7280 Display System Frequencies

SIGNAL NAME	FREQUENCY	COMMENTS
S_{CLK}	OSC	Sets data transfer rate to ICM7281 column drivers
D_{LAT} Display Control	OSC/M OSC/M	Once per row multiples period.
LCD Multiplex Freq.	OSC/(NxMx2)	Should be above 30Hz to avoid flicker.
Blink Rate	OSC/(NxMx64)	Blink rate for blinking cursor and blinking characters
V_{INV}	OSC	AC waveform for generating a negative voltage for V_{DISP}

NOTES: Where N = number of rows – 7, 8, 9, or 10.
M = 80 x number of columns (5 or 6) per character. Add 14 if annunciators enabled.

Table 3: ICM7280 Memory Map

ADDRESS		FUNCTION
DECIMAL	HEX	
0-79	00H-4FH	Character RAM. Loaded with ASCII data characters to be displayed. Address 0 is the leftmost character (assuming the Preset Display Position Register is 0.)
80-119	50H-77H	Font RAM. Holds bit pattern for four user-definable characters. See Table 4.
120	78H	Instruction register 0 (IR0)
121	79H	Instruction register 1 (IR1)
122	7AH	Instruction register 2 (IR2)
123	7BH	Cursor Register (IR3)
124	7CH	Preset Display Position Register (IR4)
125	7DH	Annunciator Register 1 (AR1)
126	7EH	Annunciator Register 2 (AR2)
127	7FH	Cursor-Addressed Entry Register

NOTE: See Table 6 for more detail about addresses 120-127 (78H-7FH).

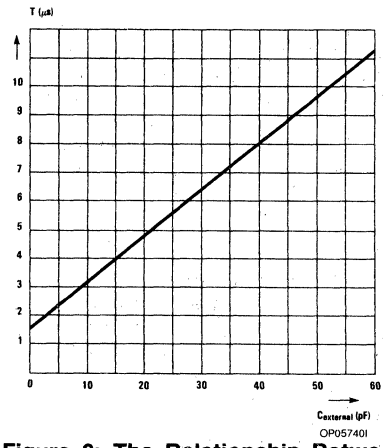


Figure 8: The Relationship Between Oscillator Period and $C_{external}$.

Display Interface

The ICM7280 will support a dot matrix LCD display which has 7, 8, 9, or 10 rows, and either evenly-spaced columns or a space after every fifth column. If the display has evenly-spaced columns, then 6 columns per character should be selected and the sixth column is always blank. If the display provides a blank after every fifth column, then 5 columns per character should be selected. The character font is automatically changed to take advantage of all rows. The ICM7280 will automatically use one of the 6 evenly-spaced columns for a space.

The ICM7280 can drive LCD displays with threshold voltages up to 2.5 volts. There is no minimum display threshold voltage since V_{DISP} can be above V_{SS}.

The ICM7280 also has 10 onboard row drivers designed to handle large dot matrix displays. These drivers provide fast slew rates, and have a minimum offset voltage.

Note: All typical values have been guaranteed by characterization and are not tested.

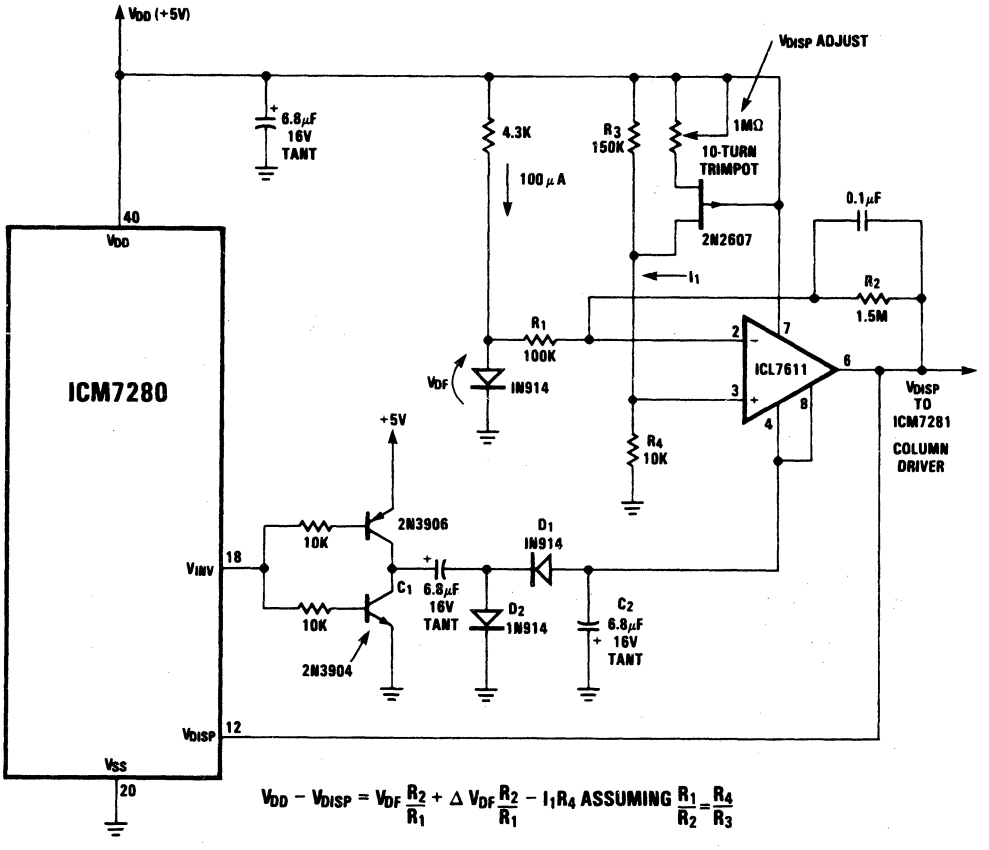


Figure 9: ICM7280 V_{DISP} Temperature Compensation Circuit

Display Voltage Generator

The ICM7280 not only has an onboard resistor string to generate the required V_1, V_2, V_3, and V_4, but also has an output that assists in generating a negative voltage for V_{DISP}. The V_{INV} pin is a low-impedance output that swings from V_{DD} to V_{SS} at the oscillator frequency. The circuit of Figure 9 connected to the V_{INV} pin generates a temperature-compensated V_{DISP}. Diodes D_1 and D_2, with capacitors C_1 and C_2 form a charge-pump negative voltage generator. The ICL7611 CMOS op-amp and its associated circuitry form an adjustable temperature compensated voltage source that provides V_{DISP} to the ICM7280, as well as the ICM7281 column drivers. Temperature compensation for V_{DISP} is necessary because the threshold voltage of LCD fluids have a pronounced negative tempco.

SOFTWARE INTERFACE

Table 3 provides a memory map of the ICM7280. The ICM7280 uses 128 bytes of memory space: 80 bytes for character data storage, 2 bytes for 14 independent annunciators or flags, 40 bytes for storing 4 user-programmable characters, 5 bytes for control registers, and one dummy address to identify cursor-addressed character entry.

Character RAM

Data may be entered in a random-access mode by simply writing to the desired character address. Address 0 corresponds to the leftmost character of the display, and address 79 corresponds to the rightmost character (assuming the Preset Display Position register has been loaded with a 0). Block moves or other high-speed data transfers can be used to move data from the host system's RAM or ROM to the ICM7280's character RAM. Character data format is standard ASCII for the 96 upper and lower case characters, with the eighth data bit ignored. As shown in Figure 10, the ICM7280 Character Font Table, the display controller also recognizes three special control characters and 14 additional European and graphics characters. The characters 08 through 17 are alternate lower case characters that are used with 8, 9, and 10 row displays.

Note: All typical values have been guaranteed by characterization and are not tested.

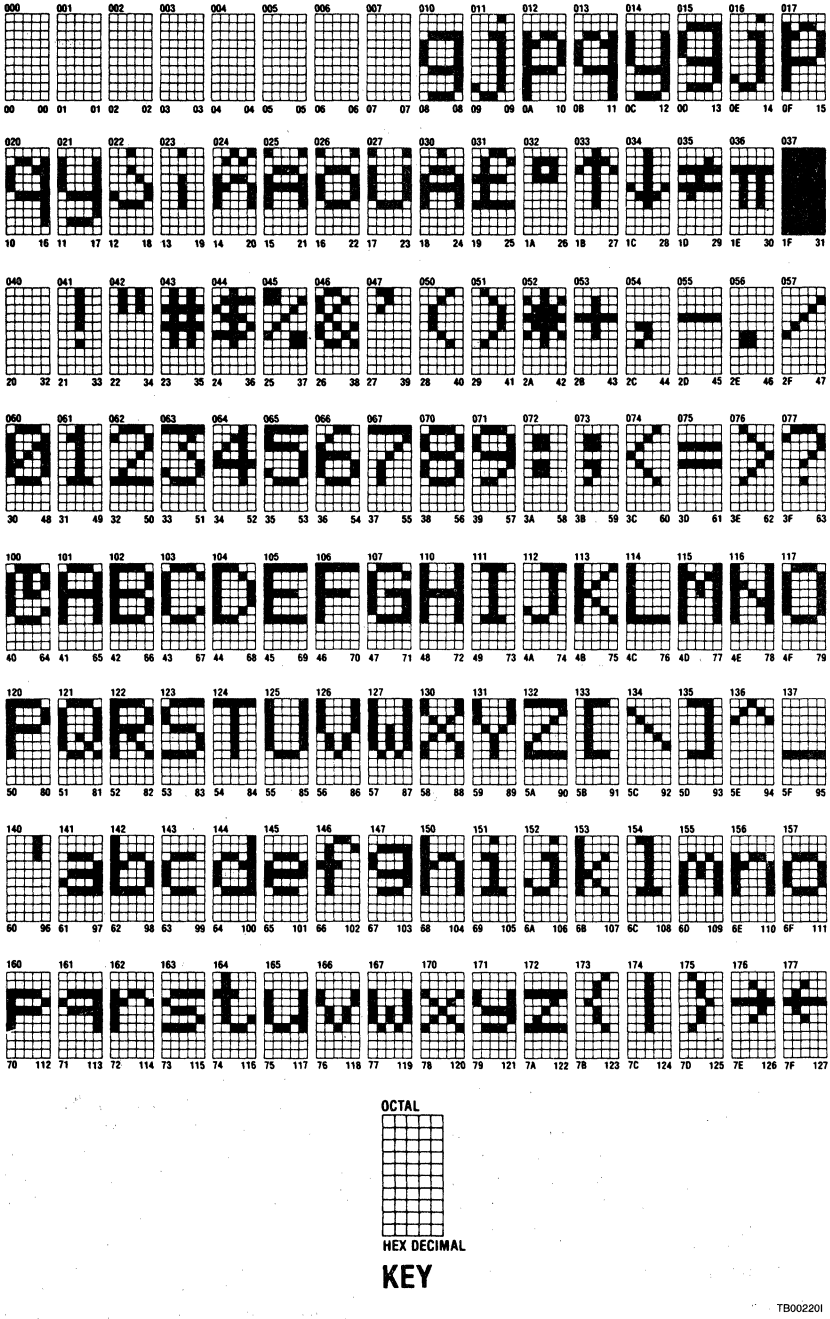


Figure 10: ICM7280 Character Font

Note: All typical values have been guaranteed by characterization and are not tested.

Table 4: Font RAM for User-Definable Characters

ROW	ASCII CHARACTER 0 FONT ADDRESS		ASCII CHARACTER 1 FONT ADDRESS		ASCII CHARACTER 2 FONT ADDRESS		ASCII CHARACTER 3 FONT ADDRESS	
	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex
Row 1 (top row)	80	50H	90	5AH	100	64H	110	6EH
–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–
Row 7	86	56H	96	60H	106	6AH	116	74H
–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–
Row 10 (bottom row)	89	59H	99	63H	109	6DH	119	77H

Font RAM

In addition to the 120 characters available in the built-in character ROM, 4 characters may be user-defined. Table 4 shows the mapping between the Font RAM and the user-defined character font. An example of an additional character is provided in Figure 11. Note that addresses 80-119 (50H-77H) hold 5 bit words that correspond to the bit pattern of the four user-definable characters, such that each 5 bit word defines the pattern for one row of the character. The LSB corresponds to the right-hand dot. Each character uses 10 words, with the lowest address representing the top row. Once defined, these characters are treated the same as the predefined characters from the Font ROM. Enter ASCII data 0, 1, 2, or 3 into Character RAM to call up one of those characters.

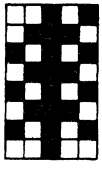


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Figure 11: An Example of a User-Defined Character

Instruction and Annunciator Registers

Table 5 details the bit assignments of the control registers. All registers are write-only registers.

Attributes are enabled by bit 5 of Instruction Register IR2, at address 122 (7AH). Blinking, underlined, and reverse video characters are controlled by attribute characters in the character RAM. These attribute characters are displayed as blanks, but signal the ICM7280 that the characters to the right of the attribute character are to be displayed with one of the three attributes (5 = underline, 6 = reverse video, and 7 = blinking). Each attribute is cancelled by a second occurence of the attribute character. The entire display can be blinked or blanked by setting the appropriate bits in IR0.

Table 5: ASCII Character 0 Example

Row	Font Address		Data	
	Decimal	Hex	Decimal	Hex
1	80	50H	5	05H
2	81	51H	14	0EH
3	82	52H	21	15H
4	83	53H	14	0EH
5	84	54H	21	15H
6	85	55H	14	0EH
7	86	56H	21	15H
8	87	57H	4	04H
9	88	58H	4	04H
10	89	59H	14	0EH

The starting point of the display can be offset by changing the value stored in IR4, the Preset Display Position Register, at address 124 (7CH). The number in this register (usually 0) specifies the address of the character in character RAM that will appear at the leftmost position on the display. For example, a 5 in this register causes the sixth character in the RAM to be displayed at the left end of the display. The Preset Display Position Register can be loaded with a value, or it can be incremented and decremented by writing to bits 2 and 3 of IR2, address 122 (7AH). The Preset Display Position Register will automatically wrap around from 79 to 0 when incremented, and wrap around from 0 to 79 when decremented past 0.

CAUTION: If a number greater than 79 is loaded into the Preset Display Position Register, display multiplexing stops. The LCD can be damaged if left in this condition for an extended period of time.

The Cursor Register determines the location of the cursor on the display, depending upon value in the Preset Display Position Register. If for example, the Cursor Register is set to 5 and the Preset Display Register is set to 0, the cursor will then be displayed in the 6th character of the display. If, however, the Cursor Register is set to 14 and the Preset Display Position Register is also set to 14, then the cursor will be displayed in the leftmost character position. If data is written to address 127 (7FH), the data is entered at the current location of the cursor and the cursor position is incremented. The cursor position may be directly set by writing to Cursor Register address 123 (7BH). The cursor

Note: All typical values have been guaranteed by characterization and are not tested.

may also be incremented or decremented by writing the appropriate instructions to IR2 at address 122 (7AH). The cursor location will wrap around from 79 to 0 or vice versa when incremented or decremented. A number greater than 79 written to the Cursor Register causes no cursor to be displayed, but the ICM7280 will otherwise function normally. If bit 4 of IR1 at address 121 (79H) is at "1", then all characters to the right of the cursor are blanked but the data in the character RAM is retained.

The IR0 register is a bit set/reset register. The MSB selects either set (1) or reset (0) operation. A "1" in any other bit position selects that bit to be set/reset. For example, a bit pattern of 10011001 will set bits 0, 3 and 4, while a bit pattern of 00010000 will clear bit 4. Unselected bits are not affected.

The Annunciator Registers are bit set/reset registers that operate similarly to IR0. When used with the ICM7281 column drivers, bit 0 of Annunciator Register 1 will be the last bit shifted out, and will appear at the column 1 output of the ICM7281. Bit 6 of Annunciator Register 2 is the first annunciator bit to be shifted out, and will appear on column 14 of the ICM7281. The annunciator outputs, if enabled, appear on all rows in columns 1-14. Annunciators are enabled by bit 7 at IR1.

Bit 6 of instruction register 2 resets all instruction registers and annunciator registers, as well as the Cursor Register and Preset Display Position Register. Bit 6 of Instruction Register 2 also resets and stops the display multiplex and blink counters.

All register bits except bit 6 of IR2 are reset upon power-up. Since bit 6 of IR2 is indeterminate at power-up, and the instruction registers cannot be written to while bit 6 is set, the initialization routine should first clear bit 6 before the other registers of the ICM7280 display controller, are accessed. When normal operation resumes after bit 6 of IR2 is cleared, the attributes will be off, the cursor will be present at 0, and the 5 x 7 character format will be engaged.

CAUTION: The ICM7280 should not be left in the reset mode for extended periods, because in this condition there is a DC bias on the liquid crystal display which can permanently damage it.

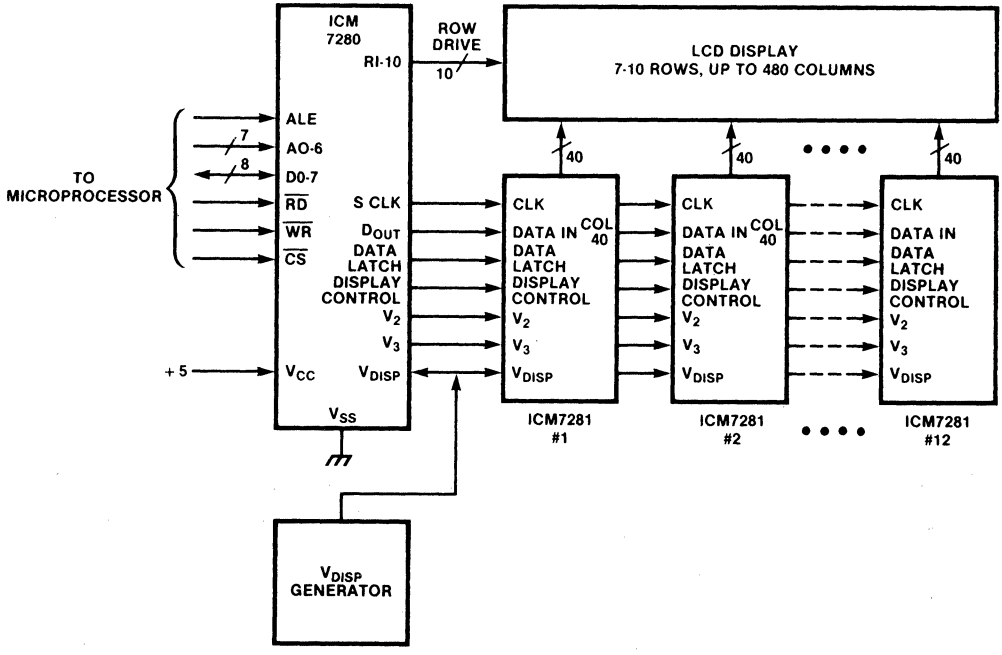
80 CHARACTER LIQUID CRYSTAL DISPLAY SYSTEM

Figure 10 shows a complete 80 character Intel/Zilog compatible display system without annunciators. The ICM7280A receives ASCII character data from the host microprocessor, converts it to a serial data stream for the ICM7281 column drivers, and provides the row drive voltages and overall display system timing and control. The power consumption of this display system is typically 6 milliwatts during normal operation and 5 microwatts when shutdown (but retaining data and control setup).

If less than 80 characters are desired, the ICM7281's that would normally drive the right-hand characters of the display may be left out. This means that an 80 character display module and a module with fewer characters can have exactly the same hardware and software interface, except that extra ICM7281's are missing from the module with fewer characters.

The Preset Display Position Register is most useful when the LCD system has fewer than 80 characters. For example, if the display has only 16 characters, all 80 characters stored in RAM can be displayed by first setting the Preset Display Position Register to 0, waiting 2 seconds, setting it to 16, waiting 2 seconds, and so forth, on up through a character preset of 64. The host processor would need to do just one write of the data and then use one command to write to the Preset Display Position Register. This requires much less time than shifting all of the data around byte by byte. Another use of the preset display feature is to implement a character-by-character scroll. Each time the Preset Display Position Register is incremented by one, the displayed characters will shift left one character position.

Note: All typical values have been guaranteed by characterization and are not tested.



LC00440I

Figure 12: 80-Character LCD Display System

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7280

Table 6: Instruction and Annunciator Registers

120 Decimal 78 Hex	Instruction Register 0 IRO
D7	1 = SET 0 = RESET
D6	1 = Blank Display
D5	1 = Blink Display
D4	1 = Cursor Enabled
D3	1 = Power Down Mode
D2	unassigned, set to 0
D1	SET to 0
D0	0 = Normal Operation, 1 = Test Mode
121 Decimal 79 Hex	**Instruction Register 1 IR1**
D7	1 = Enable Annunciators
D6	1 = Blinking Box Cursor 0 = Underline Cursor
D5	1 = Blank characters to the right of the cursor
D4	1 = 6 columns per character 0 = 5 columns per character
D3	1 = All on test mode. All dots and annunciators turned on.
D2	unassigned, set to 0
D1, D0	Controls number of rows per character, according to the following table: D_1 D_0 Character Size 0 0 7 Rows/character 0 1 8 Rows/character 1 0 9 Rows/character 1 1 10 Rows/character
122 Decimal 7A Hex	**Instruction Register 2 IR2**
D7	Production test mode only. Must be set to 0.
D6	1 = Resets all registers. See test on previous page.
D5	1 = Enable Attributes
D4	unassigned, set to 0
D3, D2	Preset Display Position Increment/Decrement D_3 D_2 Control Bit Designators 0 0 No operation 0 1 Decrement Preset Display Position Register 1 0 Increment Preset Display Position Register 1 1 Increment Preset Display Position Register
D1, D0	See the following table: D_1 D_0 Control Bit Designators 0 0 No operation 0 1 Decrement Cursor Register 1 0 Increment Cursor Register 1 1 Increment Cursor Register
123 Decimal 7B Hex	**Cursor Register IR3**
This register specifies the address of the cursor using a 7 bit value in the range of 0-79 decimal, 0-4F hexadecimal. The location of the cursor on the display is determined by both the Cursor Register and the Preset Display Position Register. The eighth bit is ignored.	
124 Decimal 7C Hex	**Preset Display Position Register IR4**
The Preset Display Position Register is normally set to 0. If set in the range of 0 to 79, the character at that address appears in the leftmost location on the display.	
125 Decimal 7D Hex	**Annunciator Register 1 AR1**
126 Decimal 7E Hex	**Annunciator Register 2 AR2**
The 7 LSBs of each annunciator register (D0-D6) each control one annunciator. To set, write a 1 to the MSB and a 1 to the bits to be set. To clear, write a 0 to the MSB and a 1 to the bits to be cleared. The annunciators will appear left to right AR1:D0 to D6 then AR2:D0 to D6.	
127 Decimal 7F Hex	**Cursor-Addressed Entry**
When character data is written to this address, the data is loaded into the character RAM using the Cursor Register as a pointer and the Cursor Register is incremented.	

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7281
40-Column LCD Dot Matrix Display Driver

GENERAL DESCRIPTION

The ICM7281 LCD Dot Matrix Column Driver is designed to convert a serial data stream into drive signals for a multiplexed dot matrix LCD. Easily cascadable, up to 16 ICM7281's can be driven by one ICM7280 Intelligent Row Driver to make an 80 character dot matrix display. The ICM7281 also serves as both a Row Driver and Column Driver in LCD dot matrix graphics displays. The low output resistance and the 15V drive capability make it well suited for graphics displays with up to 256 x 256 dots (with 10pF/dot capacitance).

The ICM7281 consists of a 40 bit shift register, a 40 bit latch and 40 level-shifters/drivers. The 4 display drive voltages are generated externally, usually by a Row Driver. A serial data interface is used to minimize the number of pins needed for digital interfacing. A data Carry Output is included for cascading several ICM7281's to drive large LCD displays.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7281IPL	−40°C to +85°C	40-Pin PLASTIC DIP
ICM7281IJL	−40°C to +85°C	40-Pin CERDIP
ICM7281/D	−	DICE

FEATURES

- **40 High Voltage LCD Column Drive Outputs**
- **Easy Interface**
  — Serial Input Shift Register with Parallel Latch and Carry Outputs
- **Directly Compatible with ICM7280 Row Driver**
  — Up to 16 ICM7281's can be Driven by an ICM7280 with No External Components
- **Low Resistance Outputs**
  — Can Drive Both Columns and Rows of LCD Graphics Displays
- **Will Drive 1.5V Threshold LCDs with Only Single 5V Supply**
  — Can Drive Up to 4.5V Threshold LCDs with 15V V_{DISP}

APPLICATIONS

- **Column Drivers For Dot Matrix Alphanumeric Displays Using ICM7280 Row Driver**
- **Row and Column Drivers For LCD Dot Matrix Graphics Displays**
- **Segment Driver For LCD Bargraphs and Annunciators**
- **Serial Input I/O Expander**

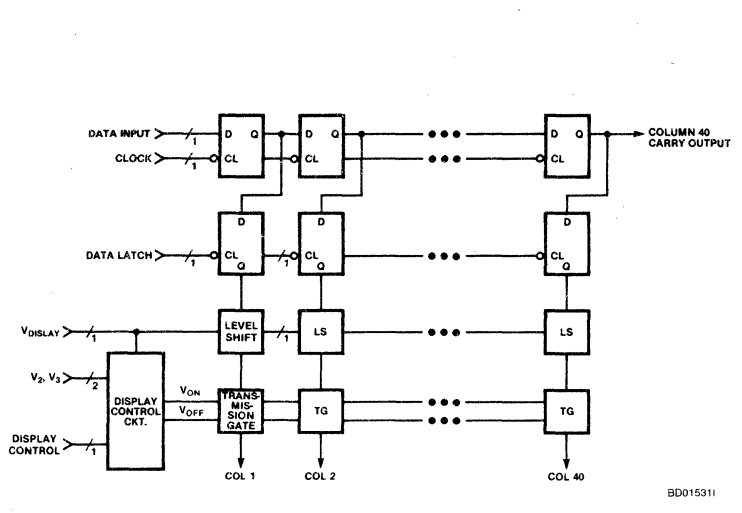


Figure 1: Functional Diagram

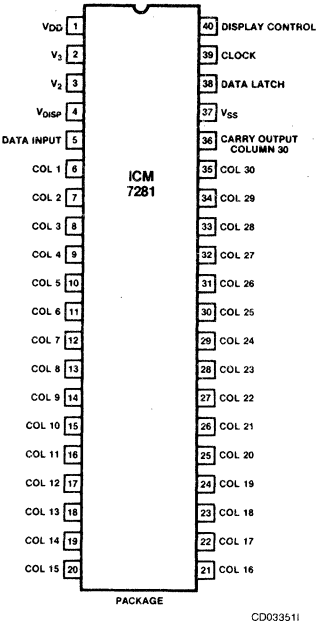


Figure 2: Pin Configuration (Outline dwg. PL)

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7281

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD} - V_{SS}$) 6V
Display Voltage ($V_{DD} - V_{DISP}$) 18V
V_2, V_3 ..... V_{DISP} to V_{DD}
Input Voltage (Note 1) ..... (V_{SS} −0.3V) to (V_{DD} +0.3V)

Power Dissipation (Note 2) ..... 0.3W @ +85°C
Operating Temperature Range ..... −40°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: Due to the SCR structure inherent in any junction isolated CMOS device, connecting an input to any voltage greater than V_{DD} or less than V_{SS} may cause destructive device latch-up. If the input voltage can exceed the recommended range, the input should be limited to less than 1mA to avoid latch-up.

NOTE 2: This limit refers to that of the package and will not occur during normal operation.

ELECTRICAL CHARACTERISTICS (V_{DD} = 5V, V_{DISP} = −10V, V_2 = 1/3 ($V_{DD} - V_{DISP}$). V_3 = 2/3 ($V_{DD} - V_{DISP}$), V_{SS} = 0V, T_A = −40°C to +85°C. Unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CHARACTERISTICS						
V_{SUPP}	Operating Supply Range		4.5	5.0	5.5	V
V_{DISP}	Display Voltage		−10		V_{DD}	V
I_{STBY} I_{DD}	Supply Current Quiescent Dynamic	 F_{CLK} = 0 F_{CLK} = 500kHz		 .1 500	 10 1000	µA
INPUT CHARACTERISTICS						
V_{IH}	Logic 1 Input Range	DATA INPUT, DATA LATCH, CLOCK and DISPLAY CONTROL	0.7V_{DD}			V
V_{IL}	Logic 0 Input Voltage	DATA INPUT, DATA LATCH, CLOCK and DISPLAY CONTROL			0.3V_{DD}	V
I_{IN}	Input Current	DATA INPUT, DATA LATCH, CLOCK and DISPLAY CONTROL 0 < V_{IN} < V_{DD}	−10	0.01	+10	µA
C_{IN}	Input Capacitance	DATA INPUT, DATA LATCH, CLOCK and DISPLAY CONTROL Dice Plastic Packaged Parts		 3 5		pF
OUTPUT CHARACTERISTICS, CARRY OUTPUTS						
V_{OH}	Output High Voltage	I_{OH} = 400µA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 1.6mA			0.4	V
OUTPUT CHARACTERISTICS, COLUMN OUTPUTS						
R_{OUT1}	Output Resistance	$V_{DD} - V_{DISP}$ = 10V, I_{OUT} = 0.1mA, V_{COL} = 0V, 1 Column ON		1.5	3	kΩ
R_{OUT2}	Output Resistance	$V_{DD} - V_{DISP}$ = 10V, V_{COL} = 0V I_{OUT} = 0.05mA per Column All Columns ON		200	400	Ω
T_R	Column Rise Time	$V_{DD} - V_{DISP}$ = 10V, C_L = 150pF per Column, 0-63% V3 to V_{DD} or 0-63% V2 to V_{DISP} One Column ON All Columns ON		 0.3 1.5		µs
T_F	Column Fall Time	$V_{DD} - V_{DISP}$ = 10V, C_L = 150pF per Column, 0-63% V_{DD} to V3 or 0−63% V_{DISP} to V2 One Column ON All Columns ON		 0.3 1.5		µs

Note: All typical values have been guaranteed by characterization and are not tested.

ELECTRICAL CHARACTERISTICS (CONT.) (V_{DD} = 5V, V_{DISP} = −10V, V_2 = 1/3 (V_{DD} − V_{DISP}). V_3 = 2/3 (V_{DD} − V_{DISP}), V_{SS} = 0V, T_A = −40°C to +85°C. Unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC CHARACTERISTICS (See Timing Diagram)						
T_{DS}	Data Setup		150	90		ns
T_{DH}	Data Hold		10	−20		ns
T_{WH}	Data Latch Width, High		250	100		ns
T_{WL}	Data Latch Width, Low			500		
T_{LS}	Data Latch Setup		400	250		ns
T_{LH}	Data Latch Hold		0	−130		ns
F_{CLK}	Clock Frequency		D.C.	2	1	MHz
T_{CH}	Clock High Period		500	100		ns
T_{CL}	Clock Low Period		500	150		ns
T_{PD}	Carry Prop Delay	C_L = 15pF		200	350	ns

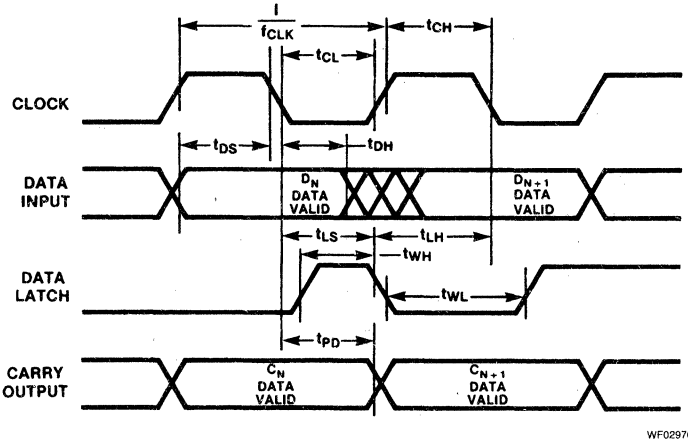


Figure 3: Timing Diagram

TYPICAL PERFORMANCE CURVES, T_A = 25°C, V_{DD} = 5V.

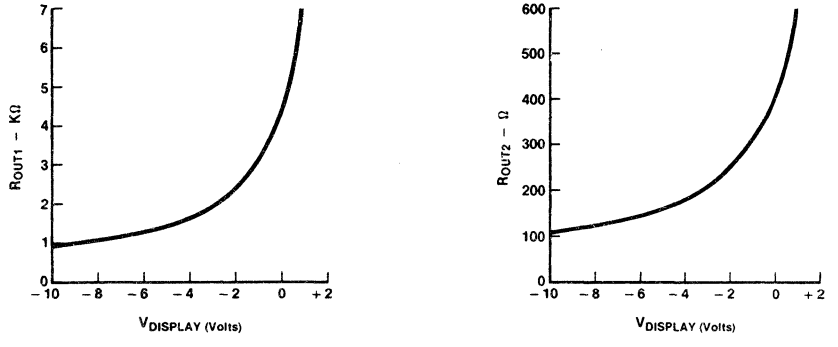


Figure 4: Output Resistance vs. $V_{DISPLAY}$

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7281

DETAILED DESCRIPTION

Data Interface

The data on DATA INPUT is shifted into the shift register with each falling edge of CLOCK. The data in the shift register is also shifted one bit with each falling edge of CLOCK. The data in the 20th and 40th registers is available as COL 20 OUTPUT and COL 40 OUTPUT on the ICM7281 dice. The packaged part has only one CARRY OUTPUT, which is the 30th column. These outputs are normally used as the DATA INPUT for an adjacent ICM7281.

The DATA LATCH input is used to transfer data from the shift register to the 40 bit latch, which consists of 40 negative edge-triggered D flip-flops. The data in the shift register is stored by the falling edge of DATA LATCH and this latched data will be held until the next falling edge of DATA LATCH.

The DISPLAY CONTROL pin is used to convey multiplex timing information to the Column Drivers. This input is used as one of the two control inputs to the 1 of 4 analog multiplexer that drives each column output.

LCD Interface

The ICM7281 uses a modified Alt and Pleshko multiplexing scheme, in which the Column Driver uses 4 voltages: V_{DD}, V2, V3, and V_{DISP}. These drive voltages are generated externally, usually by the ICM7280 Intelligent Row Driver. Each column output is driven by an analog multiplexer. The truth table and a schematic of this multiplexer are shown in Figure 7. The column data is the data that is serially loaded into the shift register, then parallel loaded into the data latch. The DISPLAY CONTROL signal, generated by the ICM7280 Row Driver, tells the ICM7281 which half of the multiplex cycle is occuring.

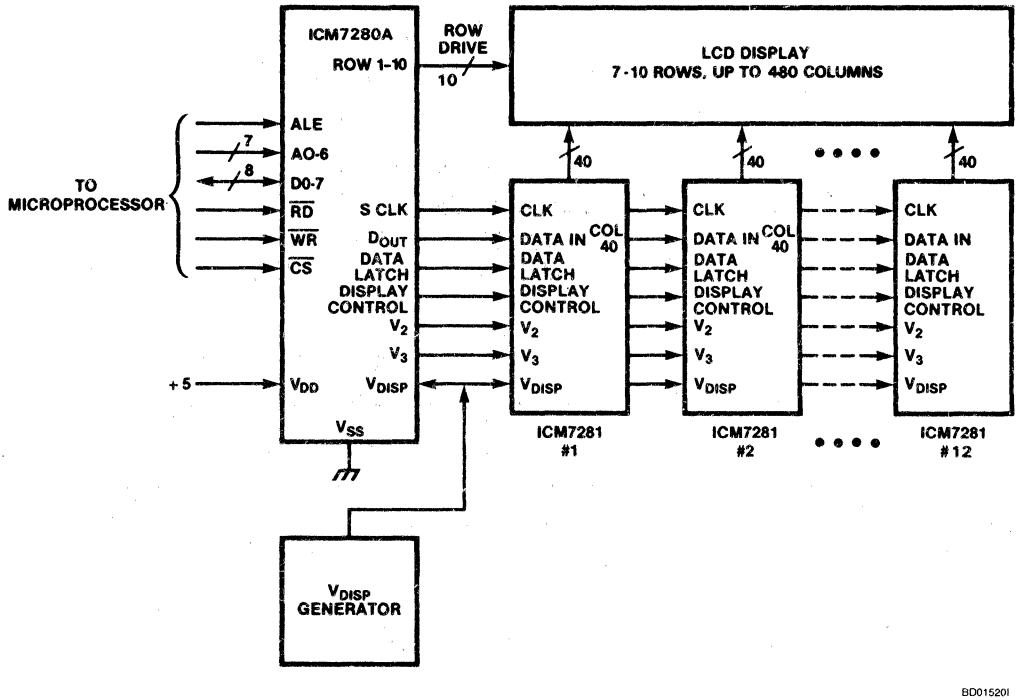


Figure 5: Alphanumeric LCD Display System

Note: All typical values have been guaranteed by characterization and are not tested.

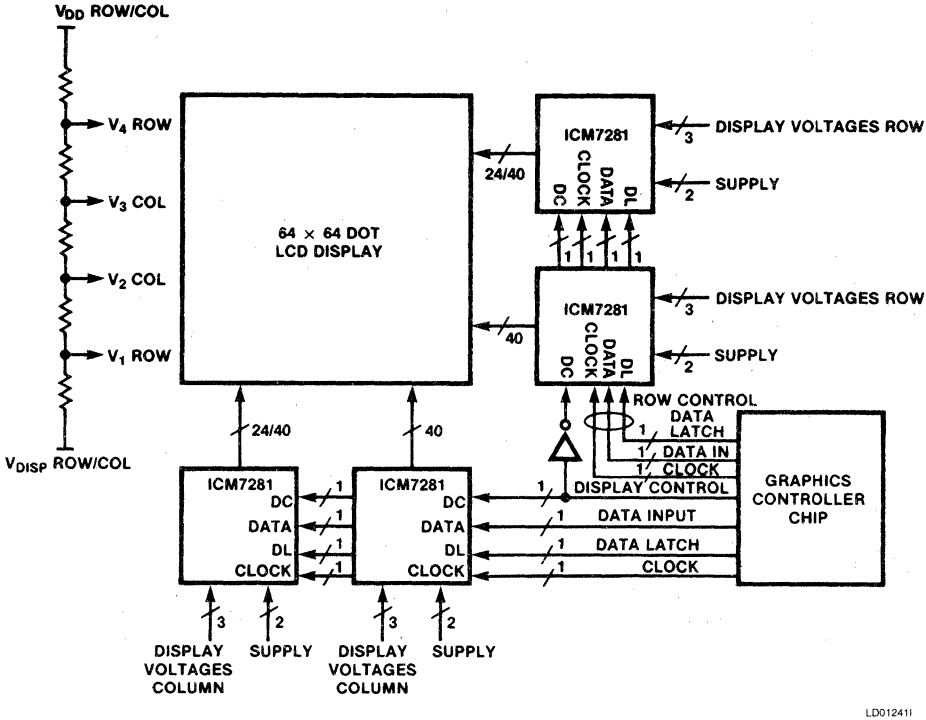


Figure 6: ICM7281 Column Driver Used in a Graphics Application

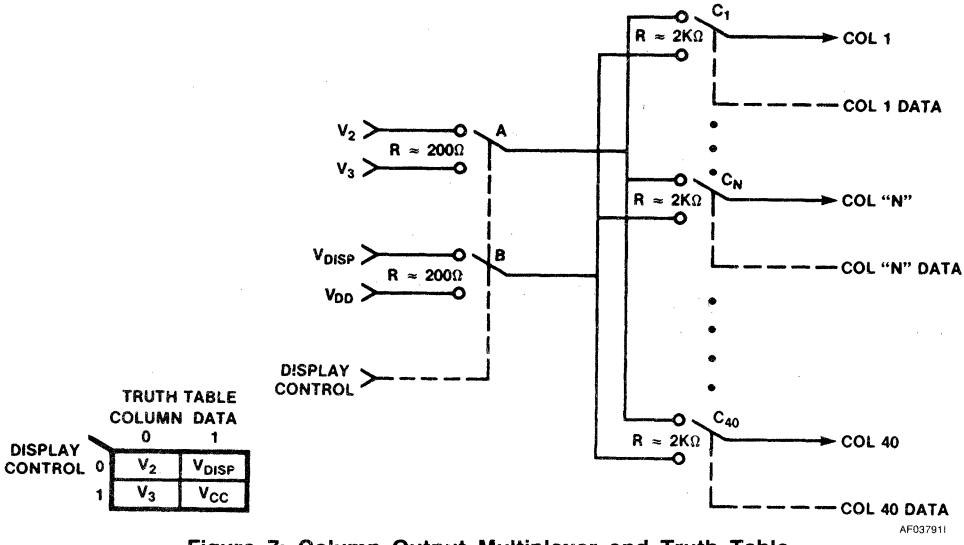


Figure 7: Column Output Multiplexer and Truth Table

Note: All typical values have been guaranteed by characterization and are not tested.

LCD MULTIPLEXING

Multiplexing Schemes

The goal in LCD multiplexing is to increase the number of segments a given number of column lines can drive, while not unacceptably degrading the viewability of the LCD display. Increasing the number of rows driven by a column decreases the ratio between the voltage across an ON segment and the voltage across an OFF segment. This ON/OFF voltage ratio is critical since the contrast of an LCD segment is determined by the RMS voltage across that segment. Figure 8 shows a typical curve of contrast vs. RMS voltage. For an acceptable display, the RMS OFF voltage must be below the 10% contrast point and the RMS ON voltage must be above the 50% contrast point. The RMS on voltages for different multiplex ratios are also shown in Figure 8. Note that as the number of rows or backplanes goes up, the RMS ON voltage decreases.

The ICM7281 can drive either columns or rows using the modified Alt and Pleshko waveforms as shown in Figure 9. The ON/OFF voltage ratio formula and the calculated values for common multiplex ratios are shown in Table 1. Table II shows the optimum voltages for V1 to V5 for different multiplex ratios.

Temperature Effects and Temperature Compensation of V_{DISP}

The performance of LCD fluids is affected by temperature in two ways. The response time of the display to changes in applied RMS voltage gets longer as the display temperature drops. At very low temperatures some displays may take several seconds to change to a new character after the new information appears at the LCD driver outputs. However, for most applications above 0°C this will not be a problem, and for low temperature applications, high-speed liquid crystal materials are available. High temperature operation is generally limited by long term degradation of the polarizer and the sealing materials above +70°C or +85°C.

The temperature effect most important in the 0–70°C range is the variation of threshold voltage with temperature. For typical liquid crystal materials, the threshold voltage, V_{THRESH}, has temperature coefficient of −7 to −14mV/°C. Since the V_{DISP} is 3.27 times V_{THRESH} (for 7 row multiplex, see Table 1), the V_{DISP} has a tempco of about −25 to −50mV/°C, depending on LCD fluid tempco. As can be seen in Figure 8, for optimum viewability and contrast ratio, the driving voltage must be accurately matched to the LCD threshold voltage. If a significant variation in temperature is expected, a method of adjusting the V_{DISP} must be provided. Figure 10 is a typical Temperature Compensation circuit using an ICL7660 negative voltage converter to give the required V_{DISP} range, if necessary.

With the fluids now available for 32 and 64 multiplex operation it is quite common to have a "Contrast" adjustment accessible to the user. This "Contrast" adjustment varies the V_{DISP} to compensate for both temperature variations and for variations in the viewing angle.

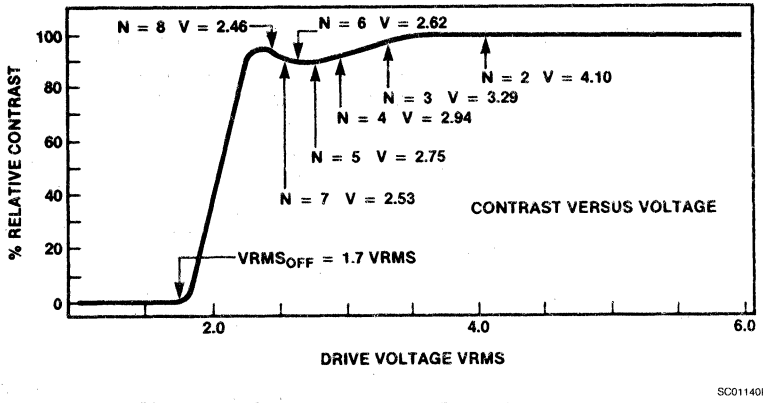


Figure 8: Contrast Versus RMS Drive Voltage

Note: All typical values have been guaranteed by characterization and are not tested.

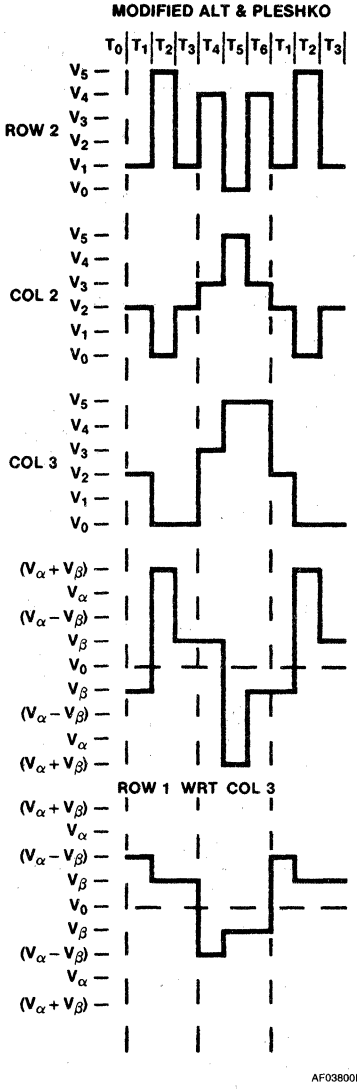
Table 1: Optimum Multiplex Drive

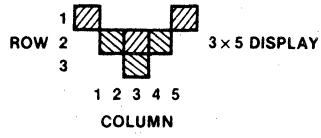
ROWS	$V_{ON/OFF}$	ALT AND PLESHKO V_{DD} – V DISPLAY/V_T	ICM7280/ICM7281 V_{DD} – V DISPLAY/V_T
4	1.73	4	3
7	1.488	4.74	3.27
8	1.447	4.97	3.37
9	1.414	5.20	3.46
10	1.387	5.41	3.56
12	1.346	5.81	3.74
14	1.315	6.18	3.917
16	1.290	6.532	4.08
32	1.196	8.817	5.19
64	1.134	12.01	6.804

Table 2: Optimum Drive Voltages

N	V1	V2	V3	V4	V5	ON/OFF VOLTAGE RATIO
4	1.000	2.000	1.000	2.000	3.000	1.732
5	0.951	1.902	1.176	2.127	3.078	1.618
6	0.919	1.838	1.332	2.252	3.171	1.543
7	0.897	1.793	1.476	2.372	3.269	1.488
8	0.879	1.759	1.608	2.488	3.367	1.447
9	0.866	1.732	1.732	2.598	3.464	1.414
10	0.855	1.710	1.849	2.704	3.559	1.387
11	0.846	1.692	1.960	2.806	3.652	1.365
12	0.838	1.677	2.066	2.904	3.743	1.346
16	0.816	1.633	2.449	3.266	4.082	1.291
20	0.802	1.605	2.786	3.589	4.391	1.255
24	0.793	1.585	3.090	3.883	4.676	1.23
30	0.782	1.564	3.502	4.284	5.066	1.203
32	0.779	1.559	3.629	4.409	5.188	1.196
40	0.771	1.541	4.103	4.874	5.645	1.173
48	0.764	1.529	4.332	5.296	6.061	1.156
54	0.761	1.522	4.830	5.590	6.351	1.147
64	0.756	1.512	5.292	6.047	6.803	1.134

Note: All typical values have been guaranteed by characterization and are not tested.





WITH

$V_0 = 0$

$V_1 = V_\beta$

$V_2 = 2V_\beta$

$V_3 = V_\alpha - V_\beta$

$V_4 = V_\alpha$

$V_5 = V_{DISPLAY} = V_\alpha + V_\beta$

$$V_\alpha = \frac{\sqrt{(K+1)^3}}{2(K-1)} V_{TH}, \quad V_\beta = \frac{\sqrt{K+1}}{2} V_{TH}$$

WHERE: $K = \dfrac{\sqrt{N}+1}{\sqrt{N}-1}$

V_{TH} = THRESHOLD VOLTAGE OF LCD

$$V_{ON}\ RMS = \sqrt{\frac{(V_\alpha + V_\beta)^2 + (N-1)V_\beta{}^2}{N}}$$

$$V_{OFF}\ RMS = \sqrt{\frac{(V_\alpha - V_\beta)^2 + (N-1)V_\beta{}^2}{N}}$$

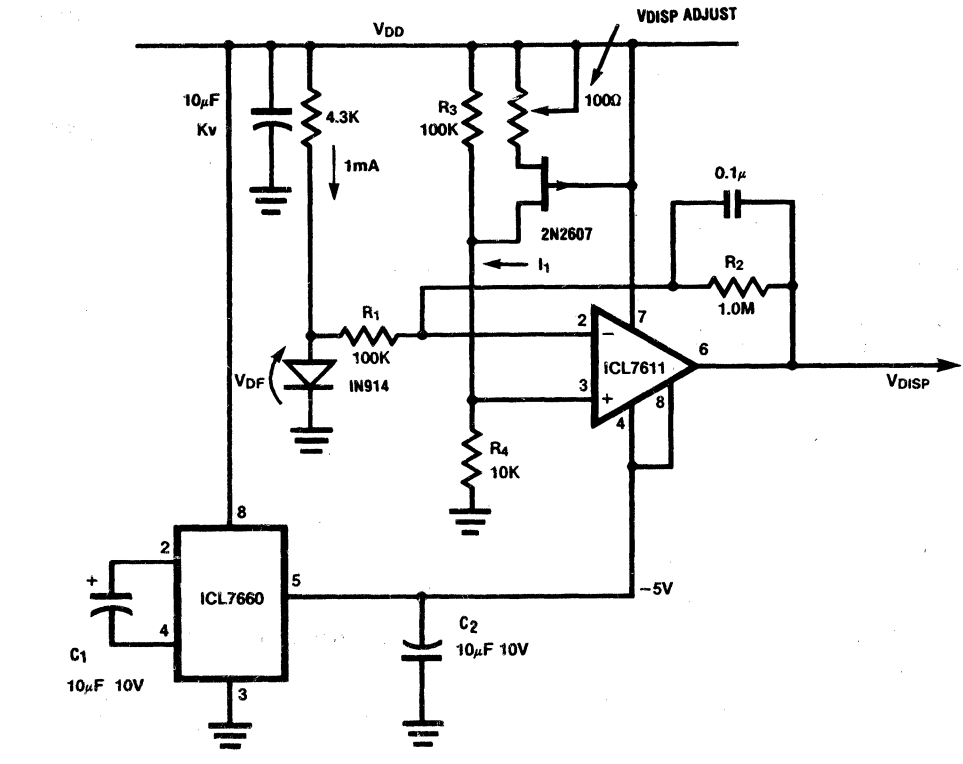
$$\frac{V_{ON}}{V_{OFF}} = \sqrt{\frac{(M+1)^2 + (N-1)}{(M-1)^2 + (N-1)}}$$

$$M = \frac{V_\alpha}{V_\beta}$$

FOR OPTIMUM CONTRAST $M = \sqrt{N \geq 4}$

Figure 9: ICM7281 Display Multiplexing Scheme

Note: All typical values have been guaranteed by characterization and are not tested.



$$V_{DISP} = I_1 R_4 + V_{DD} - V_{DF}\frac{R_2}{R_1} - \Delta V_{DF}\frac{R_2}{R_1}$$

$$\text{ASSUMING } \frac{R_4}{R_3} = \frac{R_1}{R_2}$$

DS028101

Figure 10: Temperature Compensated V_{DISP} Generator

Multiplex Rate and Maximum Drive Capability

The minimum multiplex rate is determined by the response time of the LCD. To avoid flicker, the multiplex rate should be above 30Hz. The maximum multiplex rate is determined by power dissipation limits and the drive capability of the ICM7281.

The drive capability of the ICM7281 indirectly sets the upper limit of the multiplex rate. The absolute maximum limit of DC voltage across an LCD is usually specified as 50mV. As the multiplex rate increases, any asymmetry in the rise and fall times will cause a DC offset, in addition to any offset caused by V2 and V3 not being exactly symmetrical with respect to V_{DISP} and V_{DD}. The ICM7281 was designed to have equal rise and fall times, as well as low resistance drivers which make the rise and fall times short. This allows the ICM7281 to drive over 2000pF at multiplex rate of 100Hz. Normally an LCD dot matrix display will have less than 1000pF capacitance per 40 columns (each ICM7281 drives 40 columns).

POWER DISSIPATION

The power dissipation of a display system driven by the ICM7281 has several components:

1) Quiescent or DC power dissipation of the ICM7281
2) Dynamic or AC power dissipation of the ICM7281
3) Power consumed in driving the LCD display.

ICM7281 Power Dissipation

The quiescent current of the ICM7281 is very low, typically less than 1μA, and can generally be ignored. The dynamic current is proportional to the clock frequency, with a typical value of 1.0mA per MHz. This means that at a 500kHz clock the dynamic current will be 0.5mA.

LCD Display Drive Dissipation

Since the LCD has very low leakage currents, most of the power used to drive the LCD is used to charge and discharge the LCD capacitance. The power is

Note: All typical values have been guaranteed by characterization and are not tested.

$$P_{LCD} = CV^2f_{EFF}$$

Where:

P_{LCD} is the power dissipated in driving the display

C is the display capacitance

V is Voltage across the display

f_{EFF} is the effective multiplex frequency

The effective multiplex frequency ranges from f_{MUX} to $N \times f_{MUX}$, where f_{MUX} is the multiplex rate and N is the number of rows. The actual effective multiplex frequency is dependent on which characters or bit pattern is being displayed and is typically about $N/3 \times f_{MUX}$

Low Power Shutdown

If the data clock is stopped and the voltages across the LCD are not changing, the power consumption will drop to the 5 to 50 microwatt range. Set V_{DISP}, V2 and V3 equal to V_{DD} to prevent permanent damage to the LCD display by a DC bias.

APPLICATIONS

Alphanumeric Display Using ICM7280 Intelligent Row Driver

The ICM7280 Intelligent Row Driver is specifically designed to drive multiple ICM7281 LCD Column Drivers. Figure 5 shows a typical 80 character display. The ICM7280 and ICM7281's will drive either 7, 8, 9 or 10 row displays, with the characters having either 5 or 6 columns. The Row Driver receives ASCII data, converts that data to bit-by-bit column data for the ICM7281's and serially shifts data into the ICM7281's. This process is repeated for each phase of the multiplex cycle.

Temperature compensation and generation of V_{DISP} for the ICM7280/81 system is shown in Figure 10. For further details refer to the ICM7280 Intelligent LCD Row Driver data sheet.

LCD Graphics Display

In this circuit, ICM7281's are used to drive both the rows and columns of the LCD dot matrix. An external controller is used to generate the row and column data that is serially transferred into the ICM7281's. (See Figure 6).

The display drive voltages are generated in a resistor divider network. The optimum voltages for V1 through V5 can be calculated using the equations of Figure 9. Optimum voltages for common multiplex ratios are shown in Table 2.

The LCD shown in Figure 6 is a 32 row display, divided into two sections of 16 rows to increase the ON/OFF RMS voltage ratio, thereby improving the contrast of the display. As LCD fluids improve it will become practical to use 32 or 64 row multiplexing, reducing the number of column drivers by a factor of 2 or 4.

As the number of rows increases, the V_{DISP} required by the ICM7281's modified Alt and Pleshko multiplex scheme increases less than the V_{DISP} required by a classic Alt and Pleshko multiplex scheme. For example: a 64 row display with a 1.45V threshold would require +5V and −12.4V supplies using standard Alt and Pleshko multiplexing. The ICM7281 would require only +5V and −4.9V to drive this same display with 64 row multiplexing. The negative voltage could easily be generated using a charge pump such as the ICL7660. (See Figure 10).

Serial Input I/O Expander

In addition to driving LCD's, the ICM7281 can be used as an I/O expander as shown in Figure 11. In this case, the data can be serially entered into the ICM7281 shift register using the 80C51 serial port. The 80C51 then transfers the data to the output latch by pulsing the DATA LATCH input with an I/O port line. Note that multiple ICM7281's can be cascaded to get more than 30 output lines. This cascading does not require any additional logic since the ICM7281 CARRY OUTPUTs are used.

DISPLAY CONTROL is tied to V_{DD} so that the data on the column outputs is the same as the data that was entered. If DISPLAY CONTROL is grounded, the column outputs will be inverted data. with V_3 grounded, the logic level at the column outputs will be CMOS compatible, swinging from ground to V_{DD}. The output resistance of the column outputs is about 2k ohms.

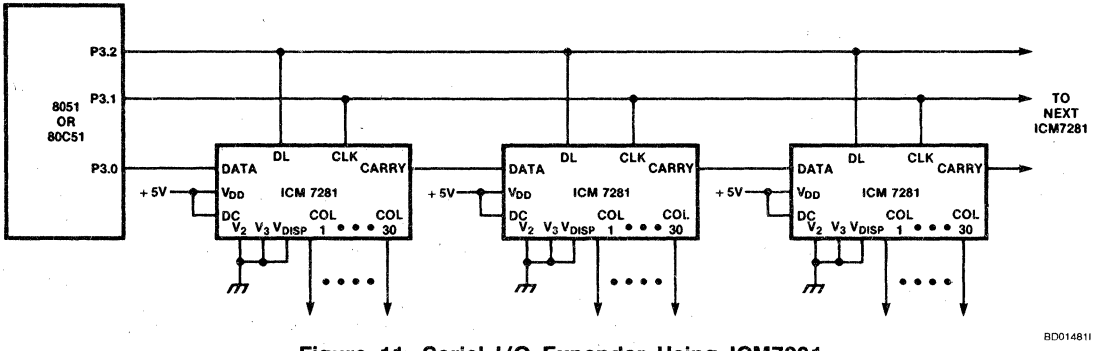


Figure 11: Serial I/O Expander Using ICM7281

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7283
LCD Dot Matrix Controller/Row Driver

GENERAL DESCRIPTION

The ICM7283 is designed to provide a complete microprocessor interface for an 2 line by 40-character alphanumeric LCD display system. It includes a character generator, display voltage generator and resistor string, row drivers, and control circuitry. Interface to a host microprocessor is achieved through either a multiplexed or non-multiplexed parallel bus.

The ICM7283 is designed to offload all display-related tasks from the host microprocessor and to provide an easy-to-program software interface. Since the internal circuitry operates at full microprocessor speeds, there is no waiting for completion of internal operations. Testing of a "Busy" flag, when characters or commands are written, is not required.

Character data can be loaded with an auto-incremented cursor or in a random-access mode. Versatile control functions allow all or selected portions of the display to be underlined, blinked, blanked, or displayed in reverse video. Power-down features are provided, and both an underline and a blinking-box cursor are available.

The ICM7283 can display four user-defined characters in addition to the standard 96 ASCII upper and lower-case characters and 14 European and graphics characters.

ORDERING INFORMATION

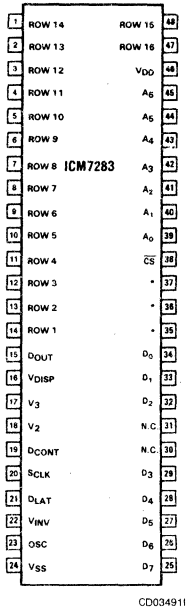
PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7283AIDM	−40°C to +85°C	48-Pin Side Braze Ceramic
ICM7283A/D	—	DIE
ICM7283BIDM	−40°C to +85°C	48-Pin Side Braze Ceramic
ICM7283B/D	—	DIE

FEATURES

- **Two Lines by 40 Characters Wide Display Memory**
  - **Directly Drives up to 6 ICM7281 Column Drivers**
- **High Speed μP Interface**
  - **ICM7283A: Intel, Zilog Compatible**
  - **ICM7283B: Motorola, Rockwell Compatible**
- **120 Character Font With Multiple Attributes**
  - **Underline, Cursor, Blinking, Reverse**
- **4 User Definable Characters**
- **Versatile Character Font Matrix**
  - **5 or 6 Columns By 8 Rows**
- **High Speed Internal Architecture**
  - **No Busy Flag Needed**

APPLICATIONS

- **Battery Hand-Held Terminals**
- **Portable Computers**
- **Instrument Control Panels**
- **LCD Display Modules**



CD034911

PART #	PIN 33	PIN 34	PIN 35
7283A	$\overline{RD}$	$\overline{WR}$	ALE
7283B	E	R/$\overline{W}$	AS

Figure 1: Pin Configuration

301691-001

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7283

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD} – V_{SS}) ..... +6.5V
Display Voltage (V_{DD} – V_{DISP}) ..... +12V
Input Voltage ..... V_{SS} –0.5V to V_{DD} +0.5V
Power Dissipation ..... 500mW @ 70°C

Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

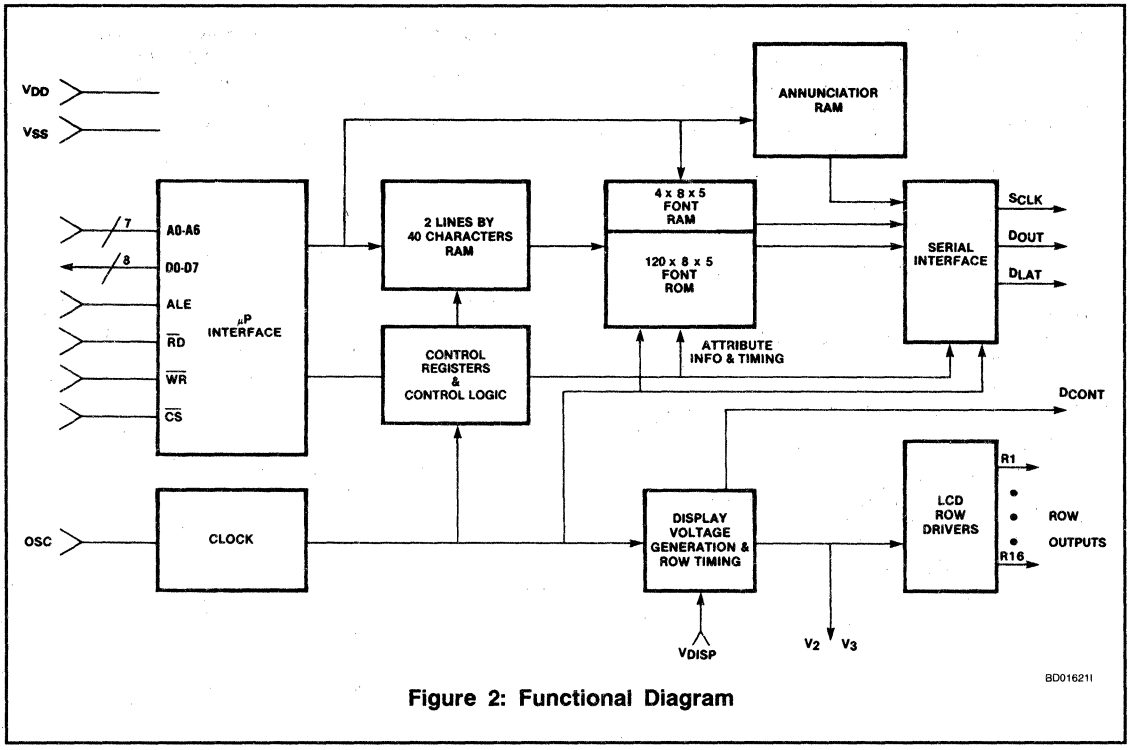


Figure 2: Functional Diagram

ELECTRICAL CHARACTERISTICS
AC CHARACTERISTICS

(V_{DD} = 5.0V±10%, T_A = –40 to +85°C, V_{DISP} = V_{DD} –8V, V_{SS} = 0V, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL}	Input Leakage	Address/Data pins high impedance $0 < V_{IN} < V_{DD}$	–10		+10	µA
I_{DD}	Supply Current	Osc open ckt, V_{IL} = 0V, V_{IH} = V_{DD}			2.5	mA
I_{STBY}	Shutdown Current	V_{IL} = 0V, V_{IH} = V_{DD}			100	µA
V_{SUPP}	Operating Voltage Range	V_{IL} = 0.4V, V_{IH} = 2.4V	4.5		5.5	V
f_{OSC}	Osc. Frequency	Pin 23 open ckt.	0.2		1.0	MHz
Serial Outputs						
V_{OL}	Output Voltage, Low	I_{OL} = 1mA			1.0	V

Note: All typical values have been guaranteed by characterization and are not tested.

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output Voltage, High	I_{OH} = 1mA	V_{DD} – 1.0			V
Data I/O, μP Interface Inputs						
V_{OL}	Output Voltage, Low	I_{OL} = 1.6mA			0.4	V
V_{OH}	Output Voltage, High	I_{OH} = 400μA	2.4			V
V_{IL}	Input Voltage, Low				0.8	V
V_{IH}	Input Voltage, High		3.0			V
Row Driver Outputs						
R_{ON}	Output Resistance, ON	D_{CONT} high, $V_0 = V_{DISP} + 0.5V$ D_{CONT} low, $V_0 = -0.5V$			1	kΩ
R_{OFF}	Output Resistance, OFF	D_{CONT} high, $V_0 = V_4 \pm .5V$ D_{CONT} low, $V_0 = V_1 \pm 0.5V$			2.5	kΩ
V_1		D_{CONT} high		–1.0		V
V_2, V_3				1.0		V
V_4		D_{CONT} low		3.0		V

AC CHARACTERISTICS (See Timing Diagram)

(V_{DD} = 5.0V±10%, V_{DISP} = 0V, T_A = –40°C to +85°C, C_L = 150pF, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Serial Output Timing						
T_{scdl}	Prop. Delay S_{CLK} to D_{LAT}				200	ns
T_{scdo}	Prop Delay S_{CLK} to D_{OUT}				400	ns
Microprocessor Interface						
T_{ll}	ALE/AS Pulse Width, High		55			ns
T_{ol}	Address to ALE Setup time		30			ns
T_{la}	Address to ALE Hold Time		30			ns
Intel/Zilog Option (ICM7280A)						
T_{ad}	Address Setup Time		50			ns
T_{ah}	Address Hold Time		30			ns
T_{wl}	WRITE Pulse Width, Low		100			ns
T_{dw}	Data to WRITE Setup Time		150			ns
T_{wd}	Data to WRITE Hold Time		30			ns
T_{rd}	READ to Valid Data				550	ns
T_{rx}	READ to Data Hold Time				150	ns
T_{asd}	ALE Setup Time		60			ns
Motorola/Rockwell Option (ICM7280B)						
T_{ad}	Address to E Setup Time		50			ns
T_{ah}	Address to E Hold Time		30			ns
T_{ee}	E Pulse Width, High		200			ns

Note: All typical values have been guaranteed by characterization and are not tested.

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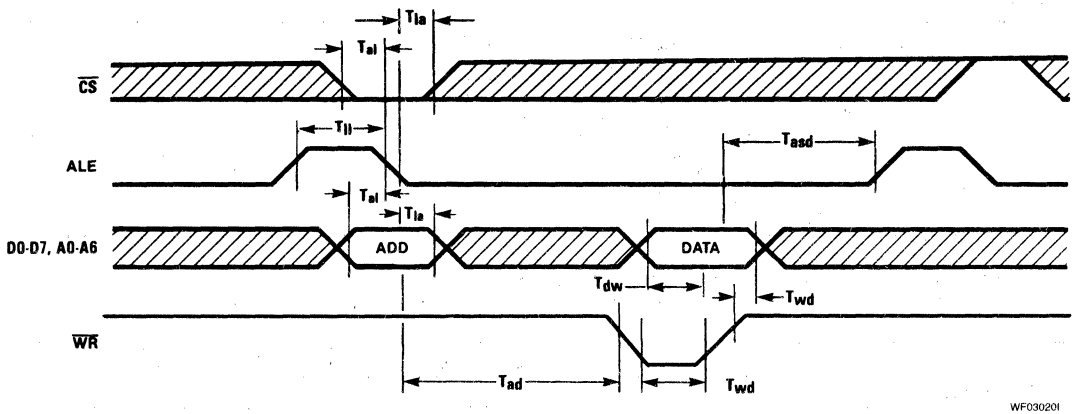
INTERSIL

AC CHARACTERISTICS (See Timing Diagram) (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{dw}	Data to E Setup Time		150			ns
T_{wd}	Data to E Hold Time		30			ns
T_{rd}	E to Valid Data	T_{ee} = 400ns			550	ns
T_{rx}	E to Data Hold Time				150	ns
T_{asd}	E to AS Setup Time		60			ns

WRITE CYCLE TIMING ($\overline{RD}$ = "1")



READ CYCLE TIMING ($\overline{WR}$ = "1")

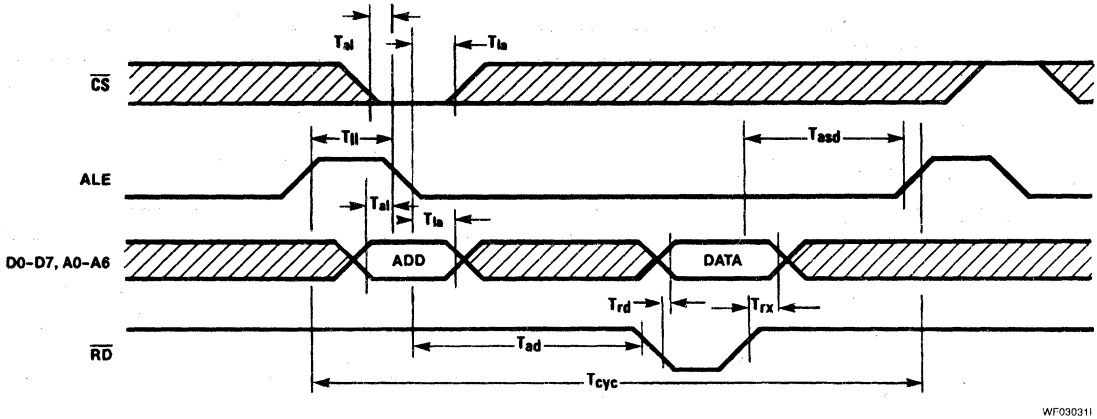
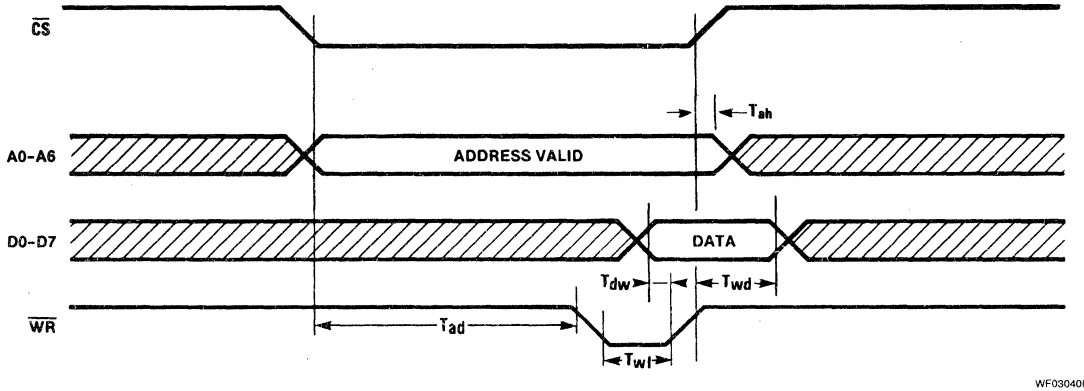


Figure 3: ICM7283A Timing Diagrams (Multiplexed Operation)

Note: All typical values have been guaranteed by characterization and are not tested.

WRITE CYCLE TIMING ($\overline{RD}$ = "1") (ALE = "1")



READ CYCLE TIMING ($\overline{WR}$ = "1") (ALE = "1")

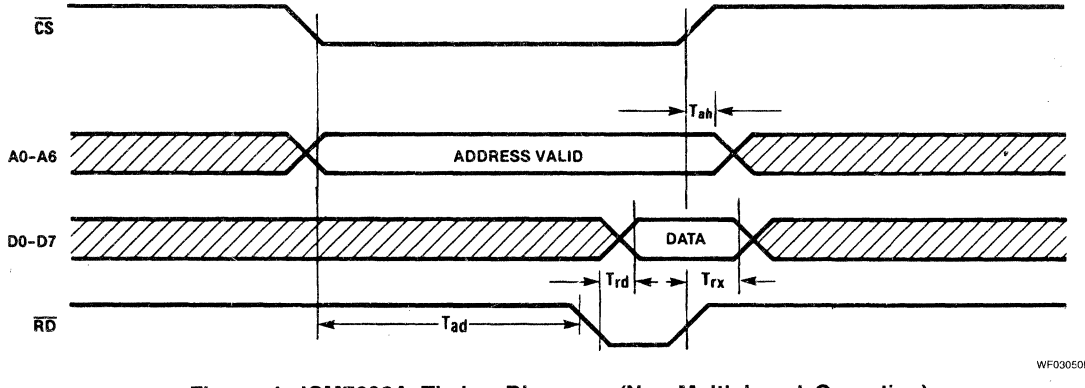
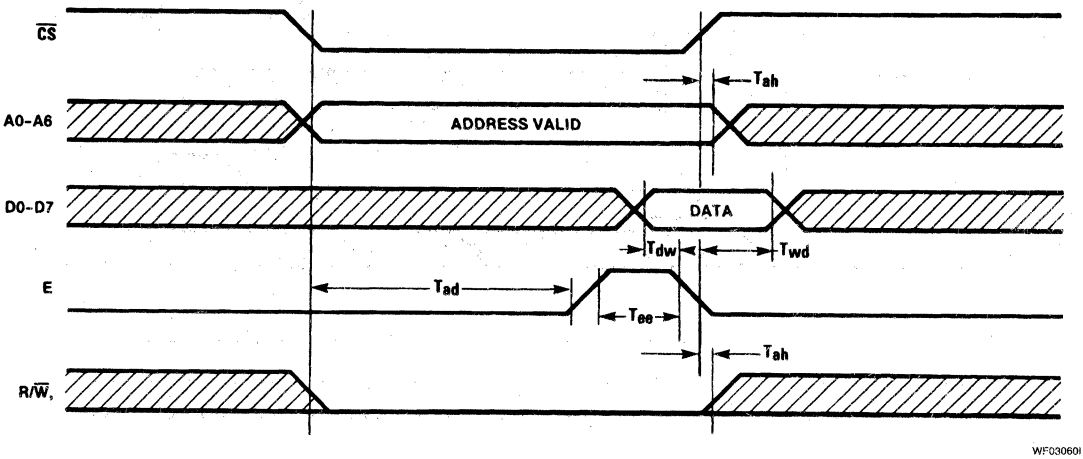


Figure 4: ICM7283A Timing Diagrams (Non-Multiplexed Operation)

Note: All typical values have been guaranteed by characterization and are not tested.

WRITE CYCLE TIMING (AS = "1")



READ CYCLE TIMING (AS = "1")

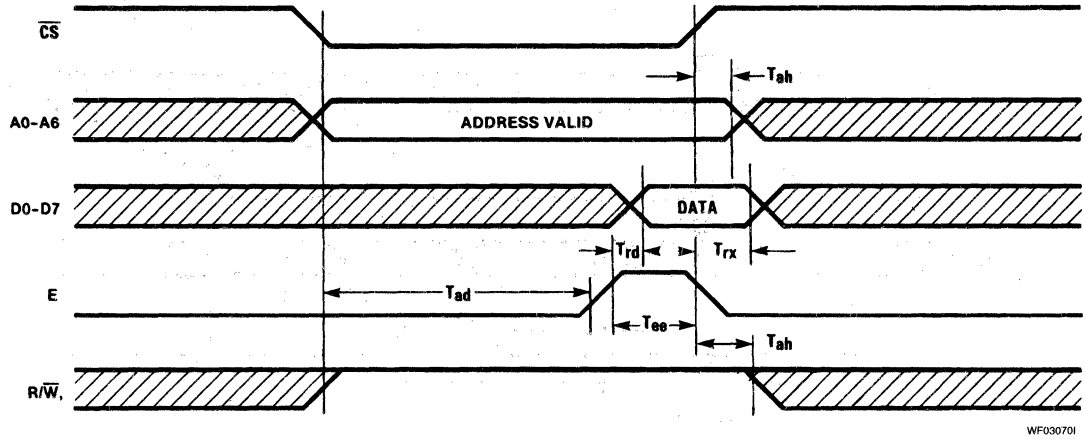
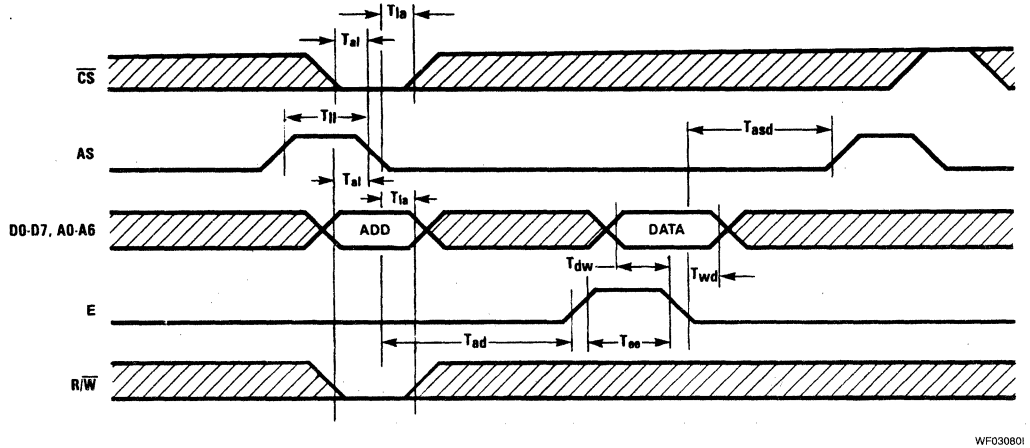


Figure 5: ICM7283B Timing Diagrams (Non-Multiplexed Operation)

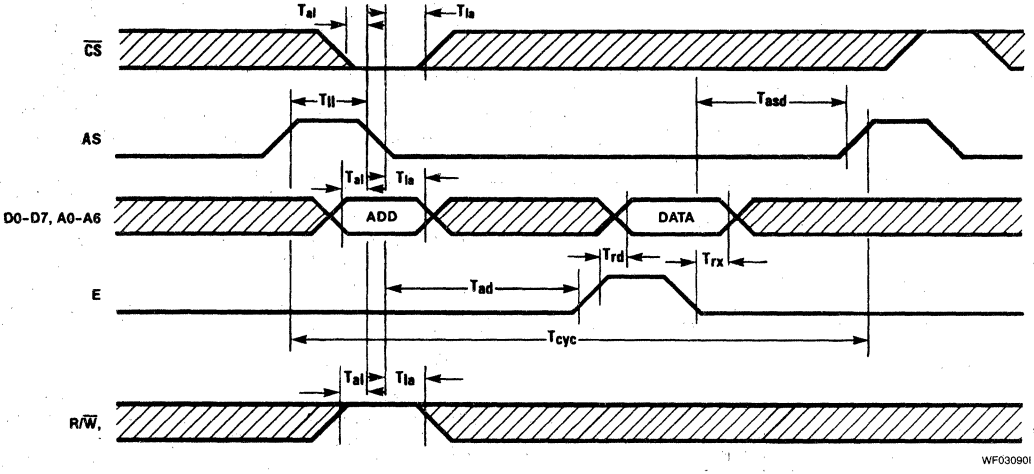
Note: All typical values have been guaranteed by characterization and are not tested.

WRITE CYCLE TIMING



WF030801

READ CYCLE TIMING



WF030901

Figure 6: ICM7283B Timing Diagrams (Multiplexed Operation)

Note: All typical values have been guaranteed by characterization and are not tested.

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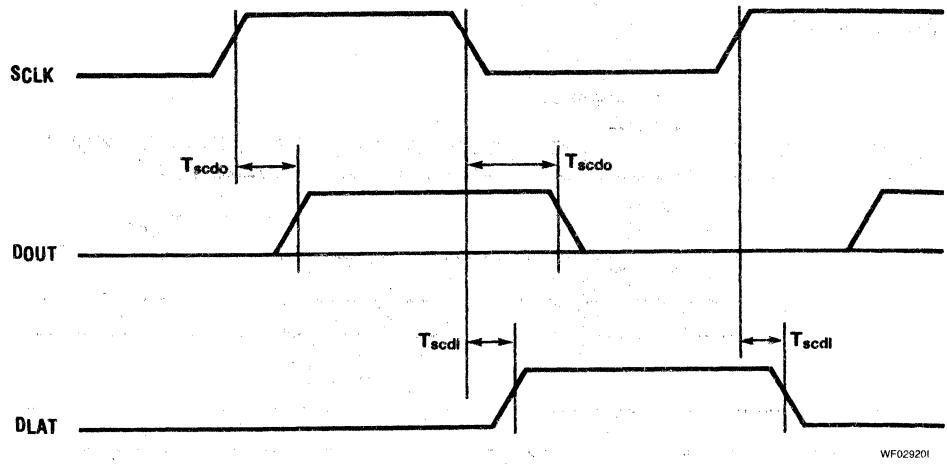

Figure 7: ICM7283 Serial Output Timing Diagram

Table 1: Pin Descriptions

SIGNAL	PIN	DESCRIPTION
ROW1-16	10-1, 48, 47	LCD row drivers
D_{OUT}	15	Serial data
V_{DISP}	16	Negative LCD supply voltage
V2, V3	17, 18	LCD column voltage
D_{CONT}	19	Column driver control output
S_{CLK}	20	Serial data clock output
D_{LAT}	21	Row data latch output
V_{INV}	22	Negative voltage generator clock
OSC	23	Oscillator input
V_{SS}	24	Digital ground
D0-D7	25-29 32-34	Data I/O
$\overline{RD}$(7280A) E(7280B)	35 35	Read input Enable input
$\overline{WR}$(7280A) R/$\overline{W}$(7280B)	36 36	Write input Read/write input
ALE(7280A) AS(7280B)	37 37	Address latch enable Address strobe
$\overline{CS}$	38	Chip select input
A0-A6	39-45	Address inputs
V_{DD}	46	Positive digital and LCD supply voltage

DETAILED DESCRIPTION

Hardware Interface

Figure 1 is a simplified block diagram of the ICM7283. It is a dedicated hardware IC and the speed of data entry and command processing is limited only by gate delays. Unlike other display controllers, the ICM7283 will not "go busy" for milliseconds at a time while processing data or commands.

Microprocessor Bus Interface

There are two versions of the ICM7283. The ICM7283A has $\overline{WR}$ and $\overline{RD}$ pins, as well as ALE and $\overline{CS}$. This version can be interfaced to standard multiplexed or non-multiplexed data buses of parts such as the 8085, Z80, 8088 and other microprocessors. The ICM7283B has R/$\overline{W}$, E and AS pins instead of $\overline{WR}$ and $\overline{RD}$ and ALE. The ICM7283B is intended for use on 6800 and 6500 family buses.

To use the ICM7283 on a multiplexed bus, tie the A0-A6 lines to the D0-D6 lines and ALE/AS driven with the system address latch enable or strobe signal. For a non-multiplexed bus, A0-A6 should be connected to the least significant address lines, D0-D7 connected to the data bus and ALE/AS tied high. The only external circuitry needed is a chip select or address decoder. The ICM7283 uses an address space of 128 bytes.

ICM7281 Data Interface

The ICM7283 Row Drivers require ICM7281 Column Drivers to operate an LCD display. Three lines are used to load data serially into the ICM7281 column drivers, D_{OUT}, S_{CLK}, and D_{LAT}. The data is latched and shifted with each negative going edge of S_{CLK}, and the data is transferred from the ICM7281 shift register to its latches with the negative going edge of D_{LAT}. The frequency of the S_{CLK} is set by the oscillator frequency of the ICM7283 and is normally about 600kHz.

Oscillator

The ICM7283 oscillator will free run at 600kHz in die form, when not loaded with any capacitance. With 15pF of external capacitance, the frequency will be about 250kHz. Figure 8 shows the relationship between oscillator period and the value of $C_{external}$. Table 1 shows the relationship between the oscillator frequency and various display system signals and features. Standard CMOS logic gates can be used to overdrive the oscillator to control frequency. A

Note: All typical values have been guaranteed by characterization and are not tested.

suitable frequency can also be derived by dividing down the host processor's clock.

Table 2: ICM7283 Display System Frequencies

SIGNAL NAME	FREQUENCY	COMMENTS
S_{CLK}	OSC	Sets data transfer rate to ICM7281 column drivers
D_{LAT} Display Control	OSC/M OSC/M	Once per row multiples period.
LCD Multiplex Freq.	OSC/(NxMx2)	Should be above 30Hz to avoid flicker.
Blink Rate	OSC/(NxMx64)	Blink rate for blinking cursor and blinking characters
V_{INV}	OSC	AC waveform for generating a negative voltage for V_{DISP}

NOTES: Where N = number of rows - i.e. 16.
M = 40 x number of columns (5 or 6) per character. Add 14 if annunciators enabled.

Table 3: ICM7283 Memory Map

ADDRESS		FUNCTION
DECIMAL	HEX	
0-79	00H-4FH	Character RAM. Loaded with ASCII data characters to be displayed. Address 0 is the upper leftmost character and Address 40 (28H) is the lower leftmost character.
80-119	50H-77H	Font RAM. Holds bit pattern for four user-definable characters. See Table 4.
120	78H	Instruction register 0 (IR0)
121	79H	Instruction register 1 (IR1)
122	7AH	Instruction register 2 (IR2)
123	7BH	Cursor Register (IR3)
124	7CH	Unassigned
125	7DH	Annunciator Register 1 (AR1)
126	7EH	Annunciator Register 2 (AR2)
127	7FH	Cursor-Addressed Entry Register

NOTE: See Table 6 for more detail about addresses 120-127 (78H-7FH).

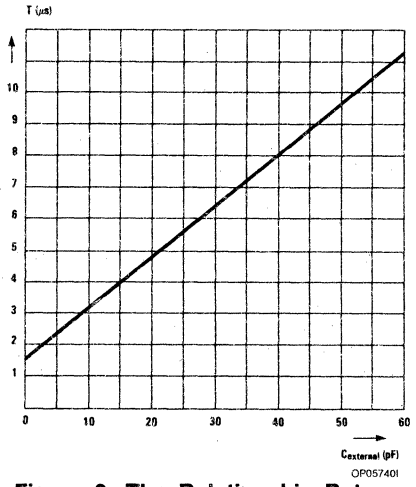

Figure 8: The Relationship Between Oscillator Period and $C_{external}$.

Display Interface

The ICM7283 will support a dot matrix LCD display which has 16 rows, and either evenly-spaced columns or a space after every fifth column. If the display has evenly-spaced columns, then 6 columns per character should be selected and the sixth column is always blank. If the display provides a blank after every fifth column, then 5 columns per character should be selected. The character font is automatically changed to take advantage of all rows. The ICM7283 will automatically use one of the 6 evenly-spaced columns for a space.

The ICM7283 can drive LCD displays with threshold voltages up to 2.5 volts. There is no minimum display threshold voltage since V_{DISP} can be above V_{SS}.

The ICM7283 also has 16 onboard row drivers designed to handle large dot matrix displays. These drivers provide fast slew rates, and have a minimum offset voltage.

Note: All typical values have been guaranteed by characterization and are not tested.

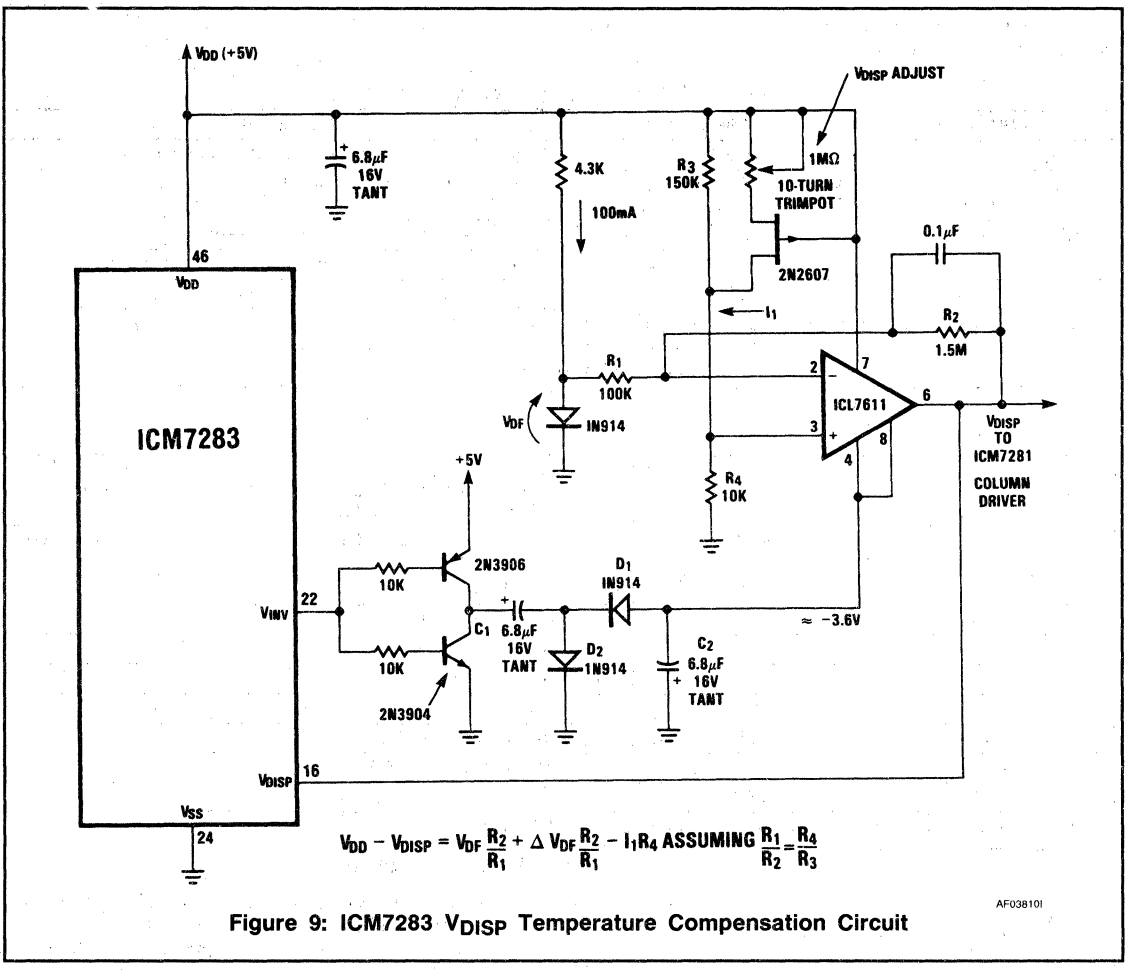

Figure 9: ICM7283 V_{DISP} Temperature Compensation Circuit

Display Voltage Generator

The ICM7283 not only has an onboard resistor string to generate the required V_1, V_2, V_3, and V_4, but also has an output that assists in generating a negative voltage for V_{DISP}. The V_{INV} pin is a low-impedance output that swings from V_{DD} to V_{SS} at the oscillator frequency. The circuit of Figure 9 connected to the V_{INV} pin generates a temperature-compensated V_{DISP}. Diodes D_1 and D_2, with capacitors C_1 and C_2 form a charge-pump negative voltage generator. The ICL7611 CMOS op-amp and its associated circuitry form an adjustable temperature compensated voltage source that provides V_{DISP} to the ICM7283, as well as the ICM7281 column drivers. Temperature compensation for V_{DISP} is necessary because the threshold voltage of LCD fluids have a pronounced negative tempco.

SOFTWARE INTERFACE

Table 3 provides a memory map of the ICM7283. The ICM7283 uses 128 bytes of memory space: 80 bytes for character data storage, 2 bytes for 14 independent annunciators or flags, 32 bytes for storing 4 user-programmable characters, 4 bytes for control registers, and one dummy address to identify cursor-addressed character entry.

Character RAM

Data may be entered in a random-access mode by simply writing to the desired character address. Address 0 corresponds to the upper leftmost character of the display, and address 79 corresponds to the lower rightmost character. Block moves or other high-speed data transfers can be used to move data from the host system's RAM or ROM to the ICM7283's character RAM. Character data format is standard ASCII for the 96 upper and lower case characters, with the eighth data bit ignored. As shown in Figure 10, the ICM7283 Character Font Table, the display controller also recognizes three special control characters and 14 additional European and graphics characters. The characters 08 through 17 are alternate lower case characters.

Note: All typical values have been guaranteed by characterization and are not tested.

Figure 10: ICM7283 Character Font

Note: All typical values have been guaranteed by characterization and are not tested.

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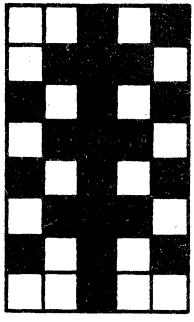
Table 4: Font RAM for User-Definable Characters

ROW	ASCII CHARACTER 0 FONT ADDRESS		ASCII CHARACTER 1 FONT ADDRESS		ASCII CHARACTER 2 FONT ADDRESS		ASCII CHARACTER 3 FONT ADDRESS	
	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex
Row 1 (top row)	80	50H	90	5AH	100	64H	110	6EH
–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–
Row 8 (bottom row)	87	57H	97	61H	107	68H	117	75H

Font RAM

In addition to the 120 characters available in the built-in character ROM, 4 characters may be user-defined. Table 4 shows the mapping between the Font RAM and the user-defined character font. An example of an additional character is provided in Figure 11. Note that addresses 80-119 (50H-77H) hold 5 bit words that correspond to the bit pattern of the four user-definable characters, such that each 5 bit word defines the pattern for one row of the character. The LSB corresponds to the right-hand dot. Each character uses 8 words, with the lowest address representing the top row. Once defined, these characters are treated the same as the predefined characters from the Font ROM. Enter ASCII data 0, 1, 2, or 3 into Character RAM to call up one of those characters.



TB00201I

Figure 11: An Example of a User-Defined Character

Instruction and Annunciator Registers

Table 5 details the bit assignments of the control registers. All registers are write-only registers.

Attributes are enabled by bit 5 of Instruction Register IR2, at address 122 (7AH). Blinking, underlined, and reverse video characters are controlled by attribute characters in the character RAM. These attribute characters are displayed as blanks, but signal the ICM7283 that the characters to the right of the attribute character are to be displayed with one of the three attributes (5 = underline, 6 = reverse video, and 7 = blinking). Each attribute is cancelled by a second occurence of the attribute character. The entire display can be blinked or blanked by setting the appropriate bits in IR0.

Table 5: ASCII Character 0 Example

Row	Font Address		Data	
	Decimal	Hex	Decimal	Hex
1	80	50H	5	05H
2	81	51H	14	0EH
3	82	52H	21	15H
4	83	53H	14	0EH
5	84	54H	21	15H
6	85	55H	14	0EH
7	86	56H	21	15H
8	87	57H	4	04H

The Cursor Register determines the location of the cursor on the display. If data is written to address 127 (7FH), the data is entered at the current location of the cursor and the cursor position is incremented. The cursor position may be directly set by writing to Cursor Register address 123 (7BH). The cursor may also be incremented or decremented by writing the appropriate instructions to IR2 at address 122 (7AH). The cursor location will wrap around from 79 to 0 or vice versa when incremented or decremented. A number greater than 79 written to the Cursor Register causes no cursor to be displayed, but the ICM7283 will otherwise function normally. If bit 4 of IR1 at address 121 (79H) is at "1", then all characters to the right of the cursor are blanked but the data in the character RAM is retained.

The IR0 register is a bit set/reset register. The MSB selects either set (1) or reset (0) operation. A "1" in any other bit position selects that bit to be set/reset. For example, a bit pattern of 10011001 will set bits 0, 3 and 4, while a bit pattern of 00010000 will clear bit 4. Unselected bits are not affected.

The Annunciator Registers are bit set/reset registers that operate similarly to IR0. When used with the ICM7281 column drivers, bit 0 of Annunciator Register 1 will be the last bit shifted out, and will appear at the column 1 output of the ICM7281. Bit 6 of Annunciator Register 2 is the first annunciator bit to be shifted out, and will appear on column 14 of the ICM7281. The annunciator outputs, if enabled, appear on all rows in columns 1-14. Annunciators are enabled by bit 7 at IR1.

Note: All typical values have been guaranteed by characterization and are not tested.

Bit 6 of instruction register 2 resets all instruction registers, annunciator registers, and the Cursor Register. Bit 6 of Instruction Register 2 also resets and stops the display multiplex and blink counters.

All register bits except bit 6 of IR2 are reset upon power-up. Since bit 6 of IR2 is indeterminate at power-up, and the instruction registers cannot be written to while bit 6 is set, the initialization routine should first clear bit 6 before the other registers of the ICM7283 display controller, are accessed. When normal operation resumes after bit 6 of IR2 is cleared, the attributes will be off and the cursor will be present at 0.

CAUTION: The ICM7283 should not be left in the reset mode for extended periods, because in this condition there is a DC bias on the liquid crystal display which can permanently damage it.

2x40 CHARACTER LIQUID CRYSTAL DISPLAY SYSTEM

Figure 10 shows a complete 2 line by 40 character Intel/Zilog compatible display system without annunciators. The ICM7283A receives ASCII character data from the host microprocessor, converts it to a serial data stream for the ICM7281 column drivers, and provides the row drive voltages and overall display system timing and control. The power consumption of this display system is typically 6 milliwatts during normal operation and 5 microwatts when shutdown (but retaining data and control setup).

If less than 80 characters are desired, the ICM7281's that would normally drive the right-hand characters of the display may be left out. This means that an 80 character display module and a module with fewer characters can have exactly the same hardware and software interface, except that extra ICM7281's are missing from the module with fewer characters.

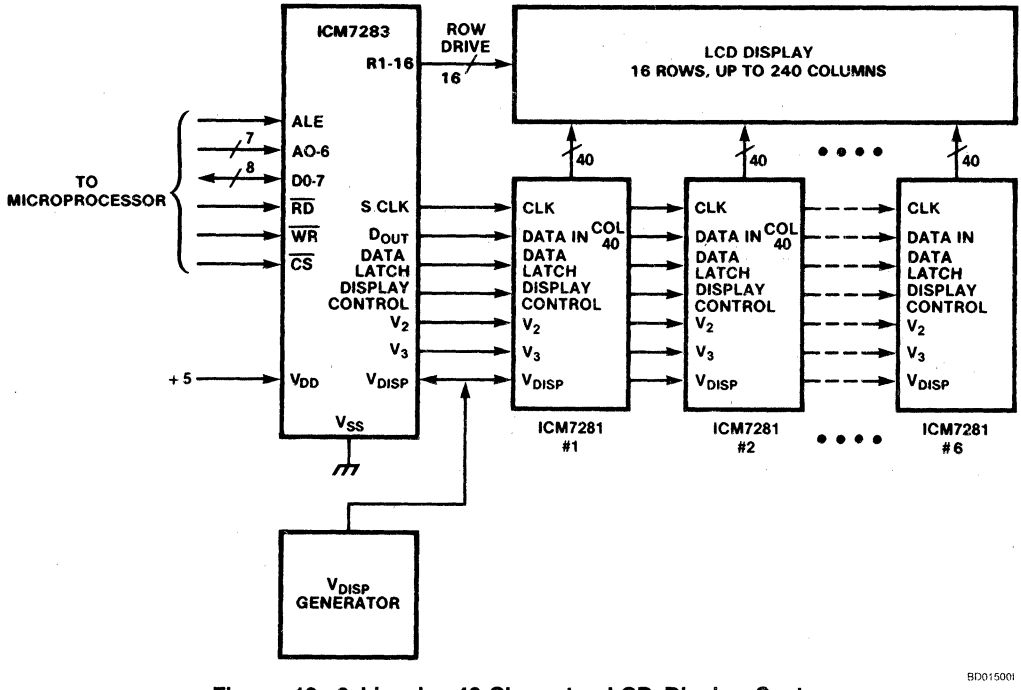


Figure 12: 2 Line by 40-Character LCD Display System

Note: All typical values have been guaranteed by characterization and are not tested.

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Table 6: Instruction and Annunciator Registers

120 Decimal 78 Hex	**Instruction Register 0 IRO**
D7	1 = SET 0 = RESET
D6	1 = Blank Display
D5	1 = Blink Display
D4	1 = Cursor Enabled
D3	1 = Power Down Mode
D2	unassigned, set to 0.
D1	unassigned, set to 0.
D0	0 = Normal Operation, 1 = Test Mode
121 Decimal 79 Hex	**Instruction Register 1 IR1**
D7	1 = Enable Annunciators
D6	1 = Blinking Box Cursor 0 = Underline Cursor
D5	1 = Blank characters to the right of the cursor
D4	1 = 6 columns per character 0 = 5 columns per character
D3	1 = All on test mode. All dots and annunciators turned on, 0 = Normal Operation
D2, D1, D0	unassigned, set to 0.
122 Decimal 7A Hex	**Instruction Register 2 IR2**
D7	Production test mode only. Must be set to 0.
D6	1 = Resets all registers. See test on previous page.
D5	1 = Enable Attributes
D4, D3, D2	unassigned, set to 0.
D1, D0	See the following table: D_1 D_0 Control Bit Designators 0 0 No operation 0 1 Decrement Cursor Register 1 0 Increment Cursor Register 1 1 Increment Cursor Register
123 Decimal 7B Hex	**Cursor Register IR3**
This register specifies the address of the cursor using a 7 bit value in the range of 0-79 decimal, 0-4F hexadecimal. The eighth bit is ignored.	
124 Decimal 7C Hex	**Unassigned**
125 Decimal 7D Hex	**Annunciator Register 1 AR1**
126 Decimal 7E Hex	**Annunciator Register 2 AR2**
The 7 LSBs of each annunciator register (D0-D6) each control one annunciator. To set, write a 1 to the MSB and a 1 to the bits to be set. To clear, write a 0 to the MSB and a 1 to the bits cleared. Then annunciator will appear left to right AR1:D0 to D6 then AR2:D0 to D6.	
127 Decimal 7F Hex	**Cursor-Addressed Entry**
When character data is written to this address, the data is loaded into the character RAM using the Cursor Register as a pointer and the Cursor Register is incremented.	

Note: All typical values have been guaranteed by characterization and are not tested.

Section 9 — Microcontrollers, Microperipherals, Memory

ICM7170
μP-Compatible Real-Time Clock

GENERAL DESCRIPTION

The ICM7170 real time clock is a microprocessor bus compatible peripheral, fabricated using Intersil's silicon gate CMOS LSI process. An 8-bit bidirectional bus is used for the data I/O circuitry. The clock is set or read by accessing the 8 internal separately addressable and programmable counters from 1/100 seconds to years. The counters are controlled by a pulse train divided down from a crystal oscillator circuit, and the frequency of the crystal is selectable with the on-chip command register. An extremely stable oscillator frequency is achieved through the use of an on-chip regulated power supply.

The device access time (t_{acc}) of 300ns eliminates the need for any microprocessor wait states or software overhead. Furthermore, the ALE (Address Latch Enable) input is provided for interfacing to microprocessors with a multiplexed address/data bus. With these two special features, the ICM7170 can be easily interfaced to any available microprocessor.

The ICM7170 generates two types of interrupts. The first type is the periodic interrupt (i.e., 100Hz, 10Hz, etc.) which can be programmed by the internal interrupt control register to provide 7 different output signals. The second type is the alarm interrupt. The alarm time is set by loading an on-chip 51-bit RAM that activates an interrupt output through a comparator. The alarm interrupt occurs when the real time counter and alarm RAM time are equal. A status register is available to indicate the interrupt source.

An on-chip Power-Down Detector eliminates the need for external components to support the battery back-up function. When a power-down or power failure occurs, internal logic switches the on-chip counters to battery back-up operation. Input/output and read/write functions become disabled and operation is limited to time-keeping and interrupt generation, resulting in low power consumption.

Internal latches prevent clock roll-over during a read cycle. Counter data is latched on the chip by reading the 100th-seconds counter and is held indefinitely until the counter is read again, assuring a stable and reliable time value.

FEATURES

- **8-Bit μP Bus Compatible**
  - **Multiplexed or Direct Addressing**
- **Binary Time Data Format Lowers Software Overhead**
- **Time From 1/100 Seconds to 99 Years**
- **Software Selectable 12/24 Hour Format**
- **Latched Time Data Ensures No Roll-Over During Read**
- **Full Calendar With Automatic Leap Year Correction**
- **On-Chip Battery Backup Switchover Circuit**
- **Access Time Less Than 300ns**
- **4 Programmable Crystal Oscillator Frequencies**
- **On-Chip Alarm Comparator and RAM**
- **Interrupts from Alarm and 6 Selectable Periodic Intervals**
- **Standby Micro-Power Operation: 2μA Typ. at 3.0V and 32kHz Crystal**

APPLICATIONS

- **Portable and Personal Computers**
- **Industrial Control Systems**
- **Data Logging**
- **Point Of Sale**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7170IPG	−40°C to +85°C	24-PIN PLASTIC DIP
ICM7170IJG	−40°C to +85°C	24-PIN CERDIP

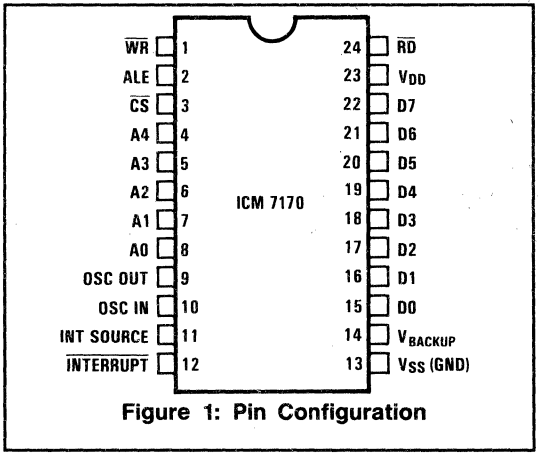

Figure 1: Pin Configuration

9

301680-005

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7170

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 8V
Power Dissipation (Note 1) 500mW
Input Voltage (Any Terminal)
(Note 2) ..... V_{DD} +0.3V to V_{SS} −0.3V

Operating Temperature ..... −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE 1: T_A = 25°C.

NOTE 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal at voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7170 be turned on first.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

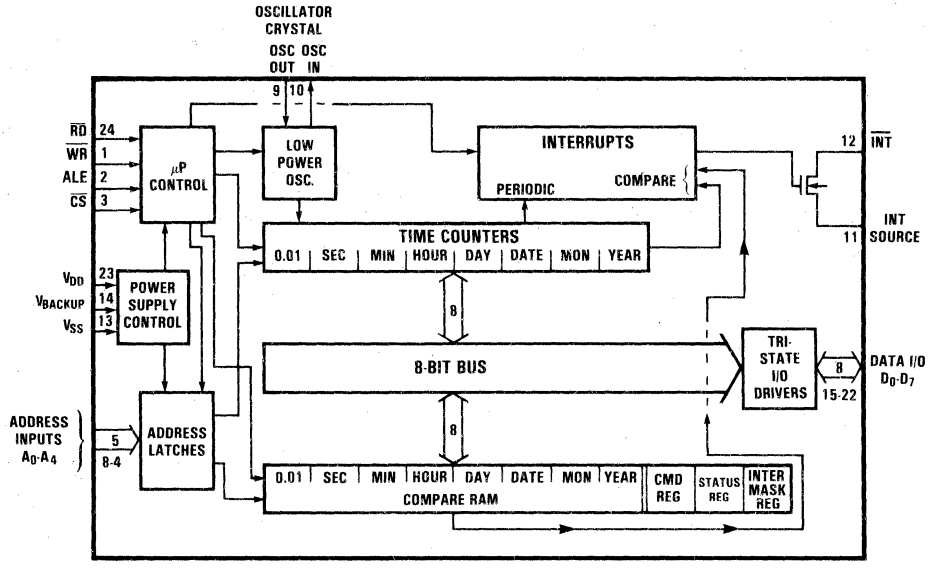

Figure 2: Functional Diagram

ELECTRICAL CHARACTERISTICS

D.C. CHARACTERISTICS (T_A = −40°C to +85°C, V_{DD} = +5V ±10%, V_{BACKUP} = V_{DD}, V_{SS} = 0V unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	SPECIFICATION			UNIT
			MIN	TYP	MAX	
V_{DD}	V_{DD} Supply Range (32kHz/4MHz)		2.6		5.5	V
$I_{STBY(1)}$	Standby Current	F_{XTAL} = 32kHz Pins 1-8,15-22 & 24 = V_{DD} V_{DD} = V_{SS}; V_{BACKUP} = V_{DD}−3.0V		2.0	20	µA
$I_{STBY(2)}$	Standby Current	F_{XTAL} = 4MHz Pins 1-8,15-22 & 24 = V_{DD} V_{DD} = V_{SS}; V_{BACKUP} = V_{DD}−3.0V		20	150	µA
$I_{DD(1)}$	Operating Supply Current	F_{XTAL} = 32kHz Read/Write Operation at 100Hz		0.3	1.2	mA
$I_{DD(2)}$	Operating Supply Current	F_{XTAL} = 32kHz Read/Write Operation at 1MHz		1.0	2.0	mA
V_{IL}	Input low voltage	V_{DD} = 4.5V			0.8	V
V_{IH}	Input high voltage	V_{DD} = 4.5V	3.5			V
V_{OL}	Output low voltage except $\overline{INTERRUPT}$	I_{OL} = 1.6mA			0.4	V

Note: All typical values have been guaranteed by characterization and are not tested.

ELECTRICAL CHARACTERISTICS (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS		SPECIFICATION			UNIT
				MIN	TYP	MAX	
V_{OH}	Output high voltage except $\overline{INTERRUPT}$	I_{OH} = 400μA		2.4			V
I_{IL}	Input leakage current	$V_{IN} = V_{DD}$ or V_{SS}		−10	0.5	+10	μA
I_{OL}	Tristate leakage current (D_0–D_7)	$V_0 = V_{DD}$ or V_{SS}		−10	0.5	+10	μA
$V_{BATTERY}$	Backup Battery Voltage	F_{XTAL} = 1, 2, 4MHz		2.6		3.2	V
$V_{BATTERY}$	Backup Battery Voltage	F_{XTAL} = 32kHz			2.0	3.2	V
V_{OL}	Output low voltage $\overline{INTERRUPT}$	I_{OL} = 1.6mA	INT SOURCE connected to V_{SS}			0.4	V
I_{OL}	Leakage current $\overline{INTERRUPT}$	$V_0 = V_{DD}$ or V_{SS}			10		μA

AC CHARACTERISTICS (T_A = −40°C to +85°C, V_{DD} = +5V ±10% D_0–D_7 $V_{BACKUP} = V_{DD}$ Load Capacitance = 150pF, V_{IL} = 0.4V, V_{IH} = 3.5V unless otherwise specified)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
READ CYCLE TIMING					
t_{rd}	READ to DATA valid		170	250	ns
t_{acc}	ADDRESS valid to DATA valid		200	300	ns
t_{cyc}	READ cycle time	400			ns
t_{rx}	$\overline{RD}$ high to bus tristate		85	100	ns
t_{as}	ADDRESS to READ set up time*		100		ns
t_{ar}	ADDRESS HOLD time after READ*	0			ns
t_{rl}	READ pulse width, low*	0.25		9,000*	μs
*Guaranteed Parameter by Design (Not 100% Tested)					
WRITE CYCLE TIMING		**MIN**	**TYP**	**MAX**	**UNIT**
t_{ad}	ADDRESS valid to WRITE strobe	100			ns
t_{wa}	ADDRESS hold time for WRITE	0			ns
t_{wl}	WRITE pulse width, low	100			ns
t_{dw}	DATA IN to WRITE set up time	100			ns
t_{wd}	DATA IN hold time after WRITE	30	10		ns
t_{cyc}	WRITE cycle time	400			ns
MULTIPLEXED MODE TIMING		**MIN**	**TYP**	**MAX**	**UNIT**
t_{ll}	ALE Pulse Width, High	50			ns
t_{al}	ADDRESS to ALE set up time	30			ns
t_{la}	ADDRESS hold time after ALE	30			ns

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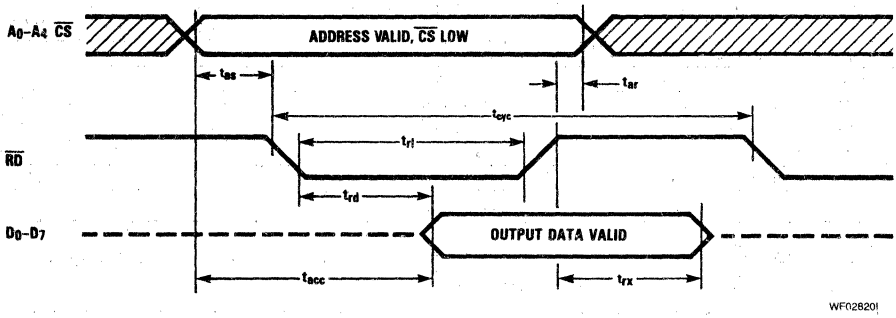
Note: All typical values have been guaranteed by characterization and are not tested.

READ CYCLE TIMING FOR NON-MULTIPLEXED BUS (ALE = "1", $\overline{WR}$ = 1)



WRITE CYCLE TIMING FOR NON-MULTIPLEXED BUS (ALE = "1", $\overline{RD}$ = 1)

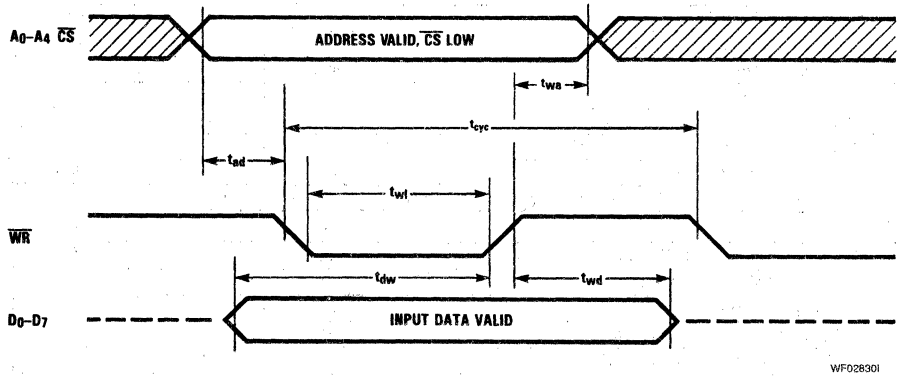
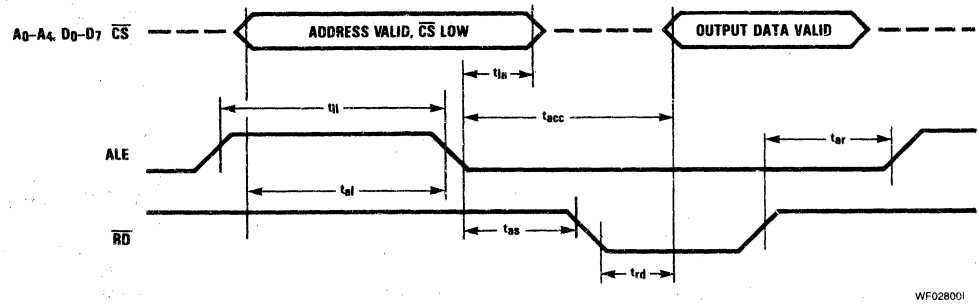


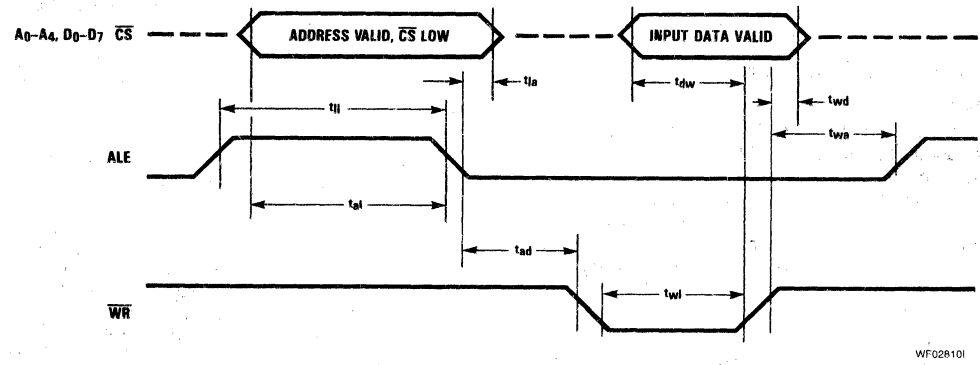
Figure 3: Timing Diagrams — Nonmultiplexed Bus

Note: All typical values have been guaranteed by characterization and are not tested.

READ CYCLE TIMING FOR MULTIPLEXED BUS ($\overline{WR}$ = 1)



WRITE CYCLE TIMING FOR MULTIPLEXED BUS ($\overline{RD}$ = 1)



NOTE: The A0 to A4 address inputs may be connected to the D0 to D4 data lines when a multiplexed bus is used.

Figure 4: Timing Diagrams — Multiplexed Bus

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7170

Table 1

SIGNAL	PIN	DESCRIPTION
$\overline{WR}$	1	$\overline{Write}$ input
ALE	2	Address latch enable input
$\overline{CS}$	3	Chip select bar input
A4-A0	4-8	Address inputs
OSC OUT	9	Oscillator output
OSC IN	10	Oscillator input
INT SOURCE	11	Interrupt common
$\overline{INTERRUPT}$	12	$\overline{Interrupt}$ output
V_{SS}(GND)	13	Digital common
V_{BACKUP}	14	Battery negative side
D0-D7	15-22	Data I/O
V_{DD}	23	Positive digital supply
$\overline{RD}$	24	$\overline{Read}$ input

DETAILED DESCRIPTION

Oscillator

This circuit uses a standard CMOS Pierce oscillator, for maximum accuracy, stability, and low-power consumption. Externally, one crystal and two capacitors are required. One of the capacitors is variable and is used to trim or tune the oscillator output. Typical values for these capacitors are C_{IN} = 18pF and C_{OUT} = 10 – 35pF, or approximately double the recommended C_{LOAD} for the crystal being used. Both capacitors must be connected from the respective oscillator pins to V_{DD} for maximum stability.

The oscillator output is divided down to 4000Hz by one of four selected ratios, via a variable prescaler. The ICM7170 can use any one of four different low-cost crystals: 4.194304MHz, 2.097152MHz, 1.048576MHz, or 32.768kHz. The command register must be programmed for the frequency of the crystal chosen, and this in turn will determine the prescaler's divide ratio.

Command Register frequency selection is written to the D0 and D1 bits at address 11H and the 12 or 24 hour format is determined by bit D2, as shown in Table 4.

The 4000Hz signal is divided down further to 100Hz, which is used as the clock for the counters. Time and calendar information is provided by 8 consecutive addressable, programmable counters: 100ths of seconds, seconds, minutes, hours, day of week, date, month, and year. The data is in binary format and is configured into 8 bits per digit. See Table 4 for address information. Any unused bits are held at logic "0" during a read and ignored during a write operation.

Compare Interrupts

On the chip are 51 bits of Alarm Compare RAM grouped into words of different lengths. These are used to store the time, ranging from 100ths of seconds to years, for comparison to the real-time counters. Each counter has a corresponding RAM word. In the Alarm Mode an interrupt is generated when the current time is equal to the alarm time. The RAM contents are compared to the counters on a word by word basis. If a comparison to a particular counter is unnecessary, then the appropriate 'M' bit in Compare RAM should be set to logic "1".

The 'M' bit, referring to Mask bit, causes a particular RAM word to be masked off or ignored during a compare. Table 4 shows addresses and Mask bit information.

Periodic Interrupts

The interrupt output can be programmed for 6 periodic signals: 100Hz, 10Hz, once per second, once per minute, once per hour, or once per day. "The 100Hz Interrupt, 10Hz Interrupt and the hundreths of a second counter have instantaneous errors of ±2.5%, ±0.15% and ±2.5% respectively; the time average, however, is zero." These can occur concurrently and in addition to Alarm Interrupts. Both the Periodic and the Alarm Interrupts are controlled by the Interrupt Mask Register. The desired interrupt is enabled by writing a logic "1" to the appropriate bit, as shown in Table 5.

The Interrupt Status Register, when read, indicates the cause of the interrupt and resets itself on the trailing edge of the read pulse. Once one or more bits have been set in the Mask Register, a roll-over in a corresponding counter will strobe the appropriate bit in the Interrupt Status Register. The interrupt pin (#12) is then pulled to the potential of the interrupt source pin (#11) through an internal open-drain N-channel MOSFET. This facilitates wire-ORing the ICM7170 with other interrupt generators that must be connected to the system MPU.

Table 2: Command Register Format

COMMAND REGISTER ADDRESS (10001b, 11h) WRITE-ONLY							
D7	D6	D5	D4	D3	D2	D1	D0
n/a	n/a	Test	Int.	Run	12/24	Freq	Freq

Table 3: Command Register Bit Assignments

D1	D0	CRYSTAL FREQUENCY	D2	24/12 HOUR FORMAT	D3	RUN/STOP	D4	INTERRUPT ENABLE	D5	TEST BIT
0	0	32.768kHz	0	12 hour mode	0	Stop	0	Interrupt disabled	0	Normal Mode
0	1	1.048576MHz	1	24 hour mode	1	Run	1	Interrupt enable	1	Test Mode
1	0	2.097152MHz								
1	1	4.194304MHz								

Note: All typical values have been guaranteed by characterization and are not tested.

Table 4: Address Codes and Functions

ADDRESS						FUNCTION	DATA								VALUE
A4	A3	A2	A1	A0	HEX		D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	00	Counter-1/100 seconds	–	.	.	.	.	.	.	.	0-99
0	0	0	0	1	01	Counter-hours	–	–	.	.	.	.	.	.	0-23
						12 Hour Mode	*	–	–	–	.	.	.	.	1-12
0	0	0	1	0	02	Counter-minutes	–	–	.	.	.	.	.	.	0-59
0	0	0	1	1	03	Counter-seconds	–	–	.	.	.	.	.	.	0-59
0	0	1	0	0	04	Counter-month	–	–	–	–	.	.	.	.	1-12
0	0	1	0	1	05	Counter-date	–	–	–	.	.	.	.	.	1-31
0	0	1	1	0	06	Counter-year	–	.	.	.	.	.	.	.	0-99
0	0	1	1	1	07	Counter-day of week	–	–	–	–	–	.	.	.	0-6
0	1	0	0	0	08	RAM-1/100 seconds	M	.	.	.	.	.	.	.	0-99
0	1	0	0	1	09	RAM-hours	–	M	–	.	.	.	.	.	0-23
						12 hour Mode	*	M	–	–	.	.	.	.	1-12
0	1	0	1	0	0A	RAM-minutes	M	–	.	.	.	.	.	.	0-59
0	1	0	1	1	0B	RAM-seconds	M	–	.	.	.	.	.	.	0-59
0	1	1	0	0	0C	RAM-month	M	–	–	–	.	.	.	.	1-12
0	1	1	0	1	0D	RAM-date	M	–	–	.	.	.	.	.	1-31
0	1	1	1	0	0E	RAM-year	M	.	.	.	.	.	.	.	0-99
0	1	1	1	1	0F	RAM-day of week	M	–	–	–	–	.	.	.	0-6
1	0	0	0	0	10	Interrupt Status and Mask Register	+	.	.	.	.	.	.	.	
1	0	0	0	1	11	Command register	–	–	.	.	.	.	.	.	

NOTES: Address 10010 to 11111 (12h to 1Fh) are unused.
'+' Unused bit for Interrupt Mask Register, MSB bit for Interrupt Status Register.
'–' Indicates unused bits.
'*' AM/PM indicator bit in 12 hour format. Logic "0" indicates AM, logic "1" indicates PM.
'M' Alarm compare for particular counter will be enabled if bit is set to logic "0".

Table 5: Interrupt and Status Registers Format

INTERRUPT MASK REGISTER ADDRESS (10000b, 10h) WRITE-ONLY							
D7	D6	D5	D4	D3	D2	D1	D0
n/a	Day	Hour	Min.	Sec.	1/10 sec.	1/100 sec.	Alarm

INTERRUPT STATUS REGISTER ADDRESS (10000b, 10h) READ-ONLY							
D7	D6	D5	D4	D3	D2	D1	D0
Int.	Day	Hour	Min.	Sec.	1/10 sec.	1/100 sec.	Alarm

Interrupt Operation

The interrupt output N-channel MOSFET is active at all times when the Interrupt Enable bit is set (bit 4 of the Command Register), and operates in both the standby and battery backup modes.

Since system power is usually applied between V_{DD} and V_{SS}, the user can connect the Interrupt Source (pin #11) to V_{SS}. This allows the Interrupt Output to turn on only while system power is applied and will not be pulled to V_{SS} during standby operation. If interrupts are required only during standby operation, then the interrupt source pin should be connected to the battery's negative side (V_{BACKUP}). In this configuration, for example, the interrupt could be used to turn on power for a cold boot.

Power-Down Detector

The ICM7170 contains an on-chip power-down detector that eliminates the need for external components for the battery back-up function. Whenever the voltage from the V_{BACKUP} pin to the V_{SS} pin is less than approximately 1.0Volt, the chip automatically switches to battery backup operation. Until power is restored, operation is limited to time counting and interrupt generation only. All other functions are disabled to achieve micropower standby power and to preserve time integrity.

If standby battery operation is not required the V_{BACKUP} should be connected to V_{DD}.

APPLICATION NOTES

Time Synchronization

Time synchronization is achieved through bit D3 of the Command Register, which is used to enable or disable the 100Hz clock from the counters. A logic "1" allows the counters to function and a logic "0" disables the counters. To accurately set the time, a logic "0" should be written into D3 and then the desired times entered into the appropriate counters. The clock is then started at the proper time by writing a logic "1" into D3 of the Command Register.

Latched Data

To prevent ambiguity while the processor is gathering data from the registers, the ICM7170 incorporates data latches and a transparent transition delay circuit.

By accessing the 100ths of seconds counter an internal store signal is generated and data from all the counters is stored into a 36-bit latch. A transition delay circuit will delay a 100Hz transition during a READ cycle until the internal store operation is completed. The data stored by the latches is then available for further processing until the 100ths of seconds counter is read again.

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7170

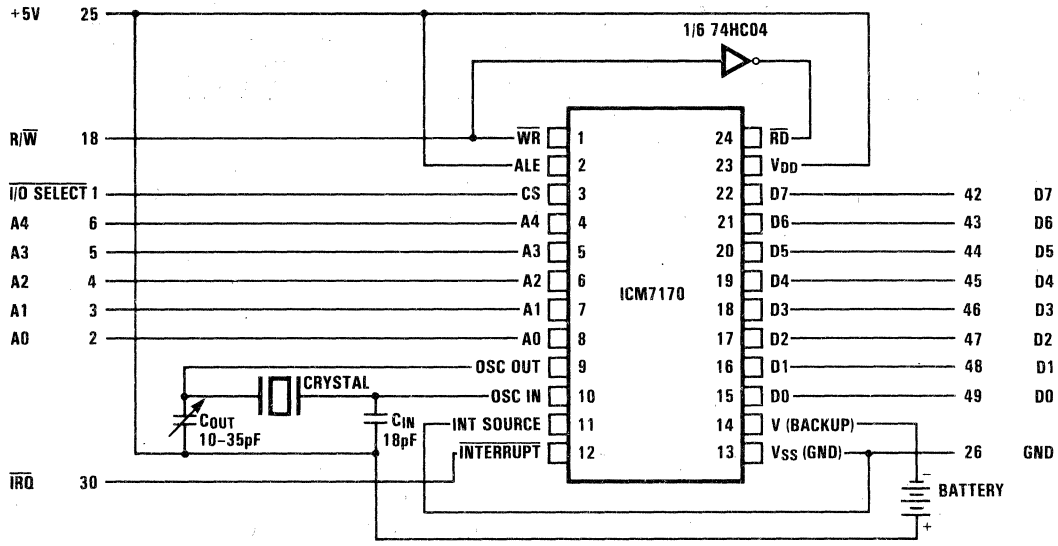


Figure 5: Apple II Plus Board Schematic

Control Lines

The $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ signals are active low inputs. Data is placed on the bus from counters or registers when $\overline{RD}$ is a logic "0". Data is transferred to counters or registers when $\overline{WR}$ is a logic "0". $\overline{RD}$ and $\overline{WR}$ must be accompanied by a logical "0" $\overline{CS}$ as shown in Figures 3 and 4.

With the ALE (Address Latch Enable) input, the ICM7170 can be interfaced directly to microprocessors that use a multiplexed address/data bus by connecting the address lines A0-A4 to the data lines D0-D4. To address the chip, the address is placed on the bus and ALE is strobed. On the falling edge, the address and $\overline{CS}$ information is read into the address latch and buffer. $\overline{RD}$ and $\overline{WR}$ are used in the same way as on a non-multiplexed bus. If a non-multiplexed bus is used, ALE should be connected to V_{DD}.

Test Mode

The test mode is entered by setting D5 of the Command Register to a logic "1". This connects the 100Hz pulse train to the seconds counter, and speeds up the counting functions.

Oscillator Tuning

Oscillator tuning should not be attempted by direct monitoring of the oscillator pins, unless very specialized equipment is used. External connections to the oscillator pins cause capacitive loading of the crystal, and shift the oscillator frequency. As a result, the precision setting being attempted is corrupted. One indirect method of determining the oscillator frequency is to measure the period between interrupts on the Interrupt Output pin (#12). This measurement must be relative to the falling edges of the $\overline{INTERRUPT}$ pin. The oscillator set-up and tuning can be performed as follows:

1) Select one of 4, readily-available oscillator frequencies and place the crystal between OSC IN (pin #10) and OSC OUT (pin #9).
2) Connect a fixed capacitor from OSC IN to V_{DD}.
3) Connect a variable capacitor from OSC OUT to V_{DD}. In cases where the crystal selected is a 32kHz Statek type (C_L = 9pF), the typical value of C_{IN} = 18pF and C_{OUT} = 10-35pF.
4) Place a 5KΩ resistor from the $\overline{INTERRUPT}$ pin to V_{DD}, and connect the INT SOURCE pin to V_{SS}.
5) Apply 5V power and insure the clock is not in standby mode.
6) Write all 0's to the Interrupt Mask Register, disabling all interrupts.
7) Write to the Command Register with the desired oscillator frequency, Hours mode (12 hour or 24 hour), Run = "1", Interrupt Enable = "1", and Test = "0".
8) Write to the Interrupt Mask Register, enabling one-second interrupts only.
9) Monitor the $\overline{INTERRUPT}$ output pin with a precision period counter and trim the OSC OUT capacitor for a reading of 1.000000 seconds. The period counter must be triggered on the falling edge of the interrupt output for this measurement to be accurate.
10) Read the Interrupt Status Register. This action resets the interrupt output back to a logic "1" level.
11) Repeat steps 9 and 10 with a software loop. A suitable computer should be used.

CIRCUIT APPLICATIONS

Apple II Plus Real-Time Clock

Figure 5 shows the schematic of a board, using the ICM7170, that has been fabricated to plug into a slot in an Apple II Plus microcomputer. Very few external components are needed on the board to provide an interface to the Apple's 6502 MPU.

Note: All typical values have been guaranteed by characterization and are not tested.

IM4702/4712
Baud Rate Generator

GENERAL DESCRIPTION

The IM4702/12 Baud Rate Generators provide necessary clock signals for digital data transmission systems, such as UARTs, using a 2.4576MHz crystal oscillator as an input. They control up to 8 output channels and can be cascaded for output expansion.

Output rate is controlled by four digital input lines, and with the specified crystal, is selectable from "zero" through 9600 Baud. In addition, 19200 Baud is possible via hardwiring.

Multi-channel operation is facilitated by making the clock frequency and the ÷8 prescaler outputs available externally. This allows up to eight simultaneous Baud rates to be generated.

The IM4712 is identical to the IM4702 with the exception that the IM4712 integrates the oscillator feedback resistor and two load capacitors on-chip.

FEATURES

- **Provides 14 Most Commonly Used BAUD Rates**
- **On-Chip Oscillator Requires Only One External Part (IM4712)**
- **Controls Up to Eight Transmission Channels**
- **TTL Compatible Outputs Will Sink 1.6mA**
- **Uses Standard 2.4576MHz Crystal**
- **Low Power Consumption: 5.5mW Guaranteed Maximum Standby**
- **Pin and Function Compatible With 4702B and HD-4702**
- **Inputs Feature Active Pull-Ups**

ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE
IM4702IJE	−40°C to +85°C	16-pin CERDIP
IM4702IPE	−40°C to +85°C	16-pin PLASTIC
IM4712IJE	−40°C to +85°C	16-pin CERDIP
IM4712IPE	−40°C to +85°C	16-pin PLASTIC

PIN DESCRIPTION

SIGNAL	PIN	DESCRIPTION
$Q_0 - Q_2$	1,2,3	Prescaler Outputs
$\overline{ECP}$	4	External Clock Enable Input
CP	5	External Clock Input
O_X	6	Crystal Output
I_X	7	Crystal Input
V_{SS}	8	Negative Supply
C_0	9	Clock Output
Z	10	Baud Rate Output
$S_0 - S_3$	14-11	Baud Rate Select Inputs
I_M	15	Multiplexed Input
V_{DD}	16	Positive Supply

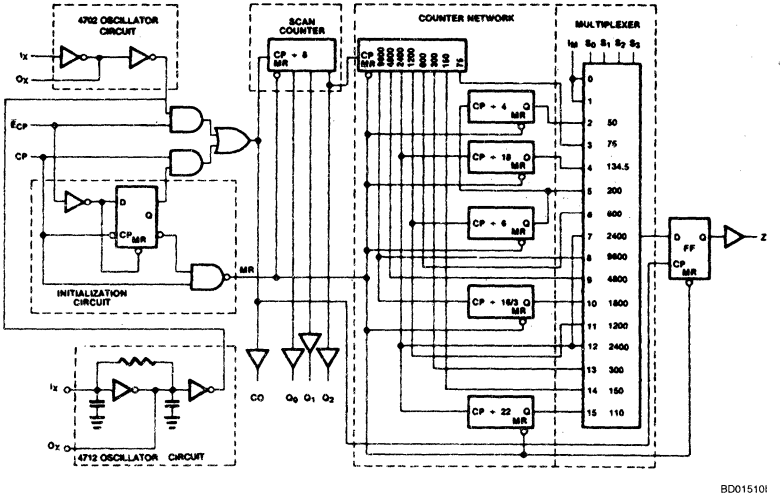


Figure 1: Functional Diagram

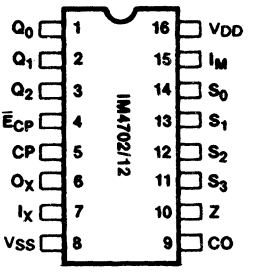


Figure 2: Pin Configuration (Outline drawings JE, PE)

002

Note: All typical values have been guaranteed by characterization and are not tested.

IM4702/4712

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD} - V_{SS}$) ..... +8.0V
Input or Output Voltage ..... V_{SS} −0.3V to V_{DD} + 0.3V
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range ..... −40°C to +85°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS V_{DD} = +5V±10% V_{SS} = 0V, T_A = −40°C to +85°C

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS		UNIT
				MIN	MAX	
V_{IH}	Input Voltage High			70% V_{CC}		V
V_{IL}	Input Voltage Low				30% V_{CC}	V
I_{IH}	Input Current High	Other Inputs	$V_{IN} = V_{DD}$		+1	
		I_X 4712	All other pins grounded		+10	
I_{IL}	Input Current Low	I_X 4702	Pin under test at ground		−1	µA
		I_X 4712	All other Inputs at V_{DD}		+10	µA
		Other Inputs		−15	−100	µA
V_{OH}	Output Voltage High		$I_{OH} < -1\mu A$; Inputs at V_{SS} or V_{DD}	V_{DD}−.05		V
V_{OL}	Output Voltage Low		$I_{OL} < +1\mu A$; Inputs at V_{SS} or V_{DD}		0.05	V
I_{OH}	Output Current High	O_X	Inputs at V_{SS} or V_{DD}	−0.1		mA
		All other Outputs	$V_O = V_{DD}$−.5	−0.3		mA
			V_O = +2.5V	−1.0		mA
I_{OL}	Output Current Low	O_X	V_O = 0.4; Inputs at V_{SS} or V_{DD}	−0.1		mA
		All other Outputs		1.6		mA
I_{STBY}	Quiescent Supply Current		$\overline{E}_{CP} = V_{DD}$; CP = V_{SS} All other Inputs = V_{SS} or V_{DD}, All outputs open		1.0	mA

Note: All typical values have been guaranteed by characterization and are not tested.

IM4702/4712

INTERSIL

AC CHARACTERISTICS V_{DD} = +5V V_{SS} = 0V, T_A = 25°C

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS		UNIT
				MIN	MAX	
t_{plh}(4702)	Propagation delay(1), I_x to CO		C_L (except O_x) = 50pF $C_{L(O_x)}$ = 7pF R_L = 200kΩ Input Transition times ≤ 20ns Input low = 1.0V Input high = V_{CC} − 1.0V		350	ns
t_{phl}(4702)					275	
t_{plh}(4712)					350	
t_{pll}(4712)					275	
t_{plh}	Propagation delay(1), CP to CO				260	
t_{phl}					220	
t_{plh}	Propagation delay(1), CO to Q_n				(2)	
t_{phl}					(2)	
t_{plh}	Propagation delay(1), CO to Z				85	
t_{phl}					75	
t_{tlh}	Output Transition Time, (1)				160	
t_{thl}	(except O_x)				75	
t_s	Set Up Time	Select to CO		350		
		I_M to CO		350		
t_h	Hold Time	Select to CO		0		
		I_M to CO		0		
$t_wCP(L)$	Clock pulse width(3)			120		
$t_wCP(H)$				120		
$t_wI_x(L)$(4702)				160		
$t_wI_x(H)$(4702)	I_x Pulse Width			160		
$t_wI_x(L)$(4712)				190		
$t_wI_x(H)$(4712)				190		

NOTES: 1. Propagation delays and output transition times will vary with output load capacitance.
2. For multichannel operation, propagation delay (CO to Q_n) plus set-up time (Select to CO) is guaranteed to be less than 367ns for the IM4702/12.
3. The first high level clock pulse after $\overline{E}_{cp}$ goes low must be at least 200ns wide to ensure reseting of all counters.
4. For design reference only, not 100% tested.

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Note: All typical values have been guaranteed by characterization and are not tested.

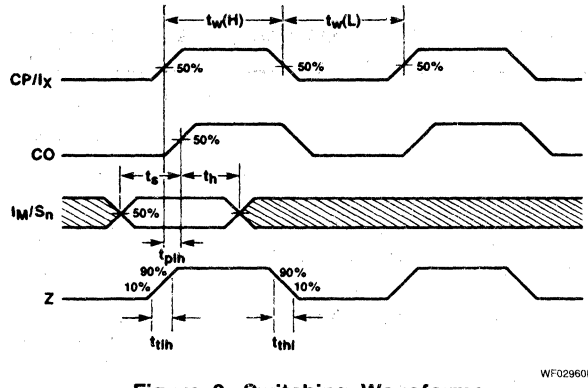


Figure 3: Switching Waveforms

FUNCTIONAL DESCRIPTION

Digital data transmission systems employ a wide range of standardized bit rates, ranging from 50 baud (for electromechanical devices) to 9600 baud (for high speed modems). Modern electronic systems commonly use Universal Asynchronous Receiver and Transmitter circuits (UARTs) to convert parallel data inputs into a serial bit stream (transmitter) and to reconvert the serial bit stream into parallel outputs (receiver). In order to resynchronize the incoming serial data, the reciever requires a clock rate which is a multiple of the incoming bit rate. Popular MOSLSI UART circuits use a clock that is 16 times the transmitted bit rate. The IM4702/12 can generate 14 standard clock rates from one common high frequency input.

The IM4702/12 contains the following five function subsystems.

Oscillator — For conventional operation generating 16 output clock pulses per bit period, the input clock frequency must be 2.4576MHz (i.e. 9600 baud x 16 x 16, since the scan counter and the first flip-flop of the counter chain act as an internal ÷ 16 prescaler). A lower input frequency will result in a proportionally lower output frequency.

The IM4702/12 can be driven from two alternate clock sources: (1) When the $\overline{E}_{CP}$ (External Clock Enable) input is LOW, the CP input is the clock source. (2) When the $\overline{E}_{CP}$ input is HIGH, a crystal connected between I_X and O_X, or a signal applied to the I_X input, is the clock source.

Prescaler (Scan Counter) — The clock frequency is made available on the CO (Clock Output) pin and is applied to the ÷ 8 prescaler with buffered outputs Q_0, Q_1, and Q_2.

Table 1: Clock Modes and Initialization

I_X	$\overline{E}_{CP}$	CP	OPERATION
⎍⎍⎍	H	L	Clocked from I_X
X	L	⎍⎍⎍	Clocked from CP
X	H	H	Continuous Reset
X	L	⎍	Reset During First CP = HIGH Time

H = HIGH Level
L = LOW Level
X = Don't Care
⎍ = 1st HIGH Level Clock Pulse After $\overline{E}_{CP}$ Goes LOW
⎍⎍⎍ = Clock Pulses

Counter Network — The prescaler output Q_2 is a square wave of 1/8 the input frequency, and is used to drive the frequency counter network generating 13 standardized frequencies. Note that the frequencies are labeled in the block diagram and described in terms of the transmission bit rate. In a conventional system using a 2.4576MHz clock input, the actual output frequencies are 16 times higher.

The output from the first frequency divider flip-flop is thus labeled 9600, since it is used to transmit or receive 9600 baud (bits per second). The actual frequency at this node is 16 x 9.6kHz = 153.6kHz. Seven more cascaded binaries generate the appropriate frequencies for bit rates 4800, 2400, 1200, 600, 300, 150, and 75.

Note: All typical values have been guaranteed by characterization and are not tested.

The other five bit rates are generated by individual counters:

bit rate 1200 is divided by 6 to generate bit rate 200,
bit rate 200 is divided by 4 to generate bit rate 50,
bit rate 2400 is divided by 18 to generate bit rate 134.5 with a frequency error of −0.87%,
bit rate 2400 is also divided by 22 to generate bit rate 110 with a frequency error of −0.83%, and
bit rate 9600 is divided by 16/3 to generate bit rate 1800.

The 16/3 division is accomplished by alternating the divide ratio between 5 (twice) and 6 (once). The result is an exact average output frequency with some frequency modulation. Taking advantage of the ÷ 16 feature of the UART, the resulting distortion is less than 0.78% regardless of the number of elements in a character, and therefore well within the timing accuracy specified for high speed communications equipment. All signals except 1800, have a 50% duty cycle.

Output Multiplexer — The outputs of the counter network are fed to a 16-input multiplexer, which is controlled by the Rate Select inputs ($S_0 - S_3$). The multiplexer output is then resynchronized with the incoming clock in order to cancel all cumulative delays and to present an output signal at the buffered output (Z) that is synchronous with the prescaler outputs ($Q_0 - Q_2$). Table 2 lists the correspondance between select code and output bit rate. Two of the 16 codes do not select an internally generated frequency, but select an input into which the user can feed either a different, nonstandardized frequency, or a static level (HIGH or LOW) to generate "zero baud".

The bit rates most commonly used in modern data terminals (110, 150, 300, 1200, 2400 baud) require that no more than one input be grounded, easily achieved with a single pole, 5-position switch. 2400 baud is selected by two different codes, so that the whole spectrum of modern digital communication rates has a common HIGH on the S_3 input.

Initialization (Reset) — The initialization circuit generates a common master reset signal for all flip-flops in the IM4702/12. This signal is derived from a digital differentiator that senses the first HIGH level on the CP input after the $\overline{E}_{CP}$ input goes LOW. Upon initialization, all counters are reset and all outputs will be in the LOW state. When $\overline{E}_{CP}$ is HIGH, selecting the Crystal input, CP must be LOW; a HIGH level on CP would apply a continuous reset.

All inputs to the 4702/12 except I_X have on-chip pull-up circuits; the I_X input of the 4712 has a high value resistor tied to O_X.

Table 2: Truth Table for Rate Select Inputs

S_3	S_2	S_1	S_0	Output Rate (Z) Note 1
L	L	L	L	Multiplexed Input (I_M)
L	L	L	H	Multiplexed Input (I_M)
L	L	H	L	50 Baud
L	L	H	H	75 Baud
L	H	L	L	134.5 Baud
L	H	L	H	200 Baud
L	H	H	L	600 Baud
L	H	H	H	2400 Baud
H	L	L	L	9600 Baud
H	L	L	H	4800 Baud
H	L	H	L	1800 Baud
H	L	H	H	1200 Baud
H	H	L	L	2400 Baud
H	H	L	H	300 Baud
H	H	H	L	150 Baud
H	H	H	H	110 Baud

L = LOW Level
H = HIGH Level

Note 1: Actual output frequency is 16 times the indicated output rate, assuming a clock frequency of 2.4576MHz.

Table 3: Crystal Specifications

PARAMETERS	TYPICAL CRYSTAL SPEC
Frequency	2.4576MHz "AT" Cut
Series Resistance (Max)	250Ω
Unwanted Modes	−6dB (Min)
Type of Operation	Parallel
Load Capacitance	32pF±0.5pF

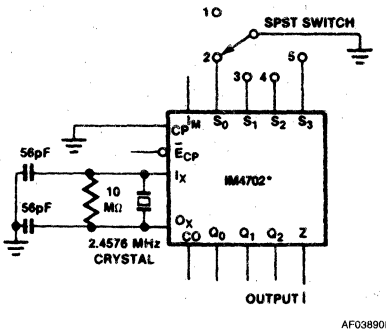
APPLICATIONS

Single Channel Bit Rate Generator

Figure 4 shows the simplest application of the IM4702/12. This circuit generates one of five possible bit rates as determined by the setting of a single pole, 5-position switch. The Bit Rate Output (Z) drives one standard TTL load or four low power Schottky loads over the full temperature range. The possible output frequencies correspond to 100, 150, 300, 1200, and 2400 or 3600 Baud. For many low cost terminals, these five bit rates are adequate.

This mode of operation is commonly chosen for applications using industry standard 1402/6402 UARTs.

Note: All typical values have been guaranteed by characterization and are not tested.



SWITCH POSITION	BIT RATE
1	110 Baud
2	150 Baud
3	300 Baud
4	1200 Baud
5	2400 Baud

Figure 4: Switch Selectable Bit Rate Generator Configuration Providing Five Bit Rates

Simultaneous Generation of Several Bit Rates

Figure 5 shows a simple scheme that generates eight bit rates on eight output lines, using one IM4702/12 and one 93L34 Bit Addressable Latch. This and the following applications take advantage of the built-in scan counter (prescaler) outputs. As shown in the block diagram, these outputs (Q_0 to Q_2) go through a complete sequence of eight states for every half-period of the highest output frequency (9600 Baud). Feeding these Scan Counter Outputs back to the Select inputs of the multiplexer causes the IM4702/12 to sequentially interrogate the state of eight different frequency signals. The 93L34 Bit Addressable Latch, addressed by the same Scan Counter Outputs, reconverts the multiplexed single Output (Z) into eight parallel output frequency signals. In the simple scheme of Figure 5, input S_3 is left open (HIGH) and the following bit rates are generated:

Q_0: 110 Baud
Q_1: 9600 Baud
Q_2: 4800 Baud
Q_3: 1800 Baud
Q_4: 1200 Baud
Q_5: 2400 Baud
Q_6: 300 Baud
Q_7: 150 Baud

Other bit rate combinations can be generated by changing the Scan Counter to Selector interconnection or by inserting logic gates into this path.

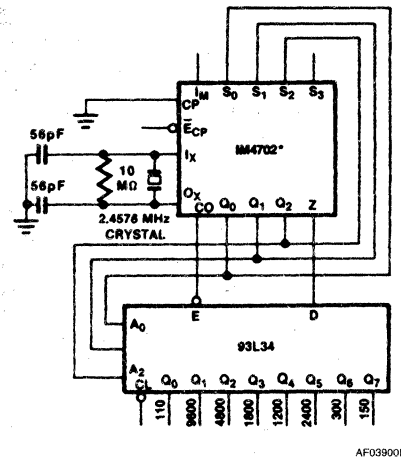


Figure 5: Bit Rate Generator Configuration With Eight Simulataneous Frequencies

19200 Baud Operation

Though a 19200 Baud signal is not internally routed to the multiplexer, the IM4702/12 can be used to generate this bit rate by connecting the Q_2 output to the I_M input and applying select code. An additional 2-input NOR gate can be used to retain the "Zero Baud" feature on select code 1 for the IM4702/12. (See Figure 6).

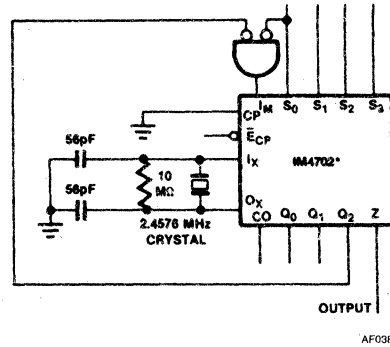


Figure 6: 19200 Baud Operation

* The 4712 may replace the 4702 in the above applications with the standard 2.4576MHz crystal. The two external capacitors and one resistor are not required when using the 4712.

Note: All typical values have been guaranteed by characterization and are not tested.

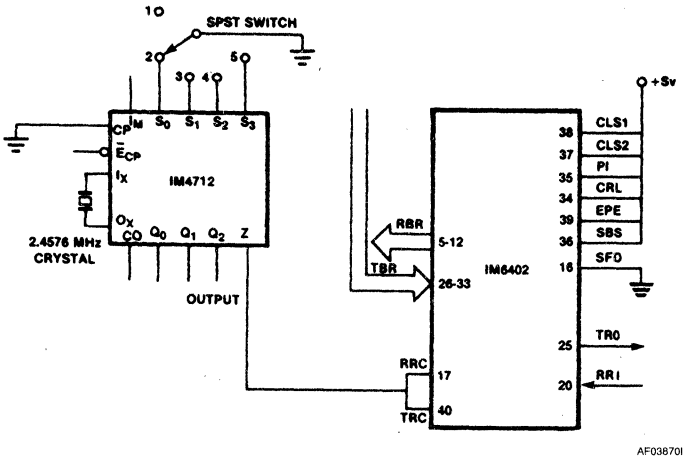


Figure 7: IM4712 Baud Rate Generator With IM6402 CMOS UART

Note: All typical values have been guaranteed by characterization and are not tested.

IM6402/IM6403
Universal Asynchronous Receiver Transmitter (UART)

INTERSIL

GENERAL DESCRIPTION

The IM6402 and IM6403 are CMOS/LSI UART's for interfacing computers or microprocessors to asynchronous serial data channels. The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits.

The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even, and parity checking and generation can be inhibited. The stop bits may be one or two (or one and one-half when transmitting 5 bit code). Serial data format is shown in Figure 8.

The IM6402 and IM6403 can be used in a wide range of applications including modems, printers, peripherals and remote data acquisition systems. CMOS/LSI technology permits clock frequencies up to 4.0MHz (250K Baud), an improvement of 10 to 1 over previous PMOS UART designs. Power requirements, by comparison, are reduced from 670mW to 10mW. Status logic increases flexibility and simplifies the user interface.

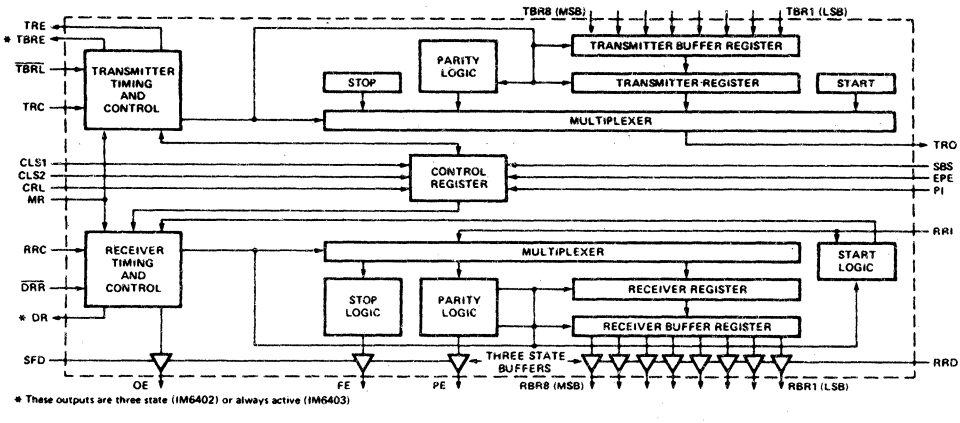
The IM6402 differs from the IM6403 in the use of five device pins as indicated in Tabie 1 and Figure 4.

FEATURES

- **Low Power — Less Than 10mW Typ. at 2MHz**
- **Operation Up to 4MHz Clock (IM6402A)**
- **Programmable Word Length, Stop Bits and Parity**
- **Automatic Data Formatting and Status Generation**
- **Compatible With Industry Standard UART's (IM6402)**
- **On-Chip Oscillator With External Crystal (IM6403)**
- **Operating Voltage —**
  IM6402-1/03-1: 5V
  IM6402A/03A: 4–11V
  IM6402/03: 5V

ORDERING INFORMATION

ORDER CODE	IM6402-1/03-1	IM6402A/03A	IM6402/03
PLASTIC PKG	IM6402-1/03-IPL	IM6402/03AIPL	IM6402/03IPL
CERAMIC PKG	IM6402-1/03-1IJL	IM6402/03AIJL	IM6402/03IJL
MILITARY TEMP.	IM6042-1/03-1MJL	IM6402/03AMJL	—
MILITARY TEMP. WITH /Hi-Rel processing	IM6402-1/03-1MJL/HR	IM6402/03AMJL/HR	—



BD002301

Figure 1: Functional Diagram

-002

Note: All typical values have been guaranteed by characterization and are not tested.

IM6402/IM6403

INTERSIL

ABSOLUTE MAXIMUM RATINGS (IM6402/03)

Operating Temperature
IM6402/03 (I) ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to 150°C
Supply Voltage ($V_{DD} - V_{SS}$) ..... +8.0V

Voltage On Any Input or Output Pin ..... (V_{SS} -0.3V) to (V_{DD} +0.3V)
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

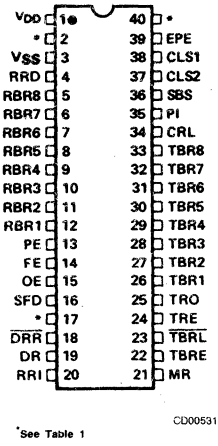


Figure 2: Pin Configuration

TABLE 1

PIN	IM6402	IM6403 w/XTAL	IM6403 w/EXT TTL CLOCK	IM6402 w/EXT CMOS CLOCK
2	N/C	Divide Control	Divide Control	Divide Control
17	RRC	XTAL	External Clock Input	No Connection
19	Tri-State	Always Active	Always Active	Always Active
22	Tri-State	Always Active	Always Active	Always Active
40	TRC	XTAL	V_{SS}	External Clock Input

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0V ±10% V_{SS} = 0V, T_A = Operating Temperature Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
V_{IH}	Input Voltage High		V_{DD}-2.0			V
V_{IL}	Input Voltage Low				0.8	V
I_{IL}	Input Leakage [1]	$V_{SS} \le V_{IN} \le V_{DD}$	-5.0		5.0	µA
V_{OH}	Output Voltage High	I_{OH} = -0.2mA	2.4			V
V_{OL}	Output Voltage Low	I_{OL} = 1.6mA			0.45	V
I_{OLK}	Output Leakage	$V_{SS} \le V_{OUT} \le V_{DD}$	-5.0		5.0	µA
I_{STBY}	Power Supply Current Standby	$V_{IN} = V_{SS}$ or V_{DD}		1.0	800	µA
I_{DD}	Power Supply Current IM6402	f_c = 500kHz			1.2	mA
I_{DD}	Power Supply Current IM6403	$f_{crystal}$ = 2.46MHz			3.7	mA
C_{IN}	Input Capacitance [1] [3]	T_A = 25°C		7.0	8.0	pF
C_O	Output Capacitance [1] [3]	T_A = 25°C		8.0	10.0	pF

NOTE: 1. Except IM6403 XTAL input pins (i.e. pins 17 and 40).
2. V_{DD} = 5V, T_A = 25°C.
3. These parameters are guaranteed but not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.

IM6402/IM6403

AC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0V ±10% V_{SS} = 0V, C_L = 50pF, T_A = Operating Temperature Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
f_c	Clock Frequency IM6402	See Timing Diagrams (Figures 4,5,6)	D.C.		1.0	MHz
$f_{crystal}$	Crystal Frequency IM6403				2.46	MHz
t_{pw}	Pulse Widths CRL, $\overline{DRR}$, $\overline{TBRL}$		225	50		ns
t_{mr}	Pulse Width MR		600	200		ns
t_{ds}	Input Data Setup Time		75	20		ns
t_{dh}	Input Data Hold Time		90	40		ns
t_{en}	Output Enable Time			80	190	ns

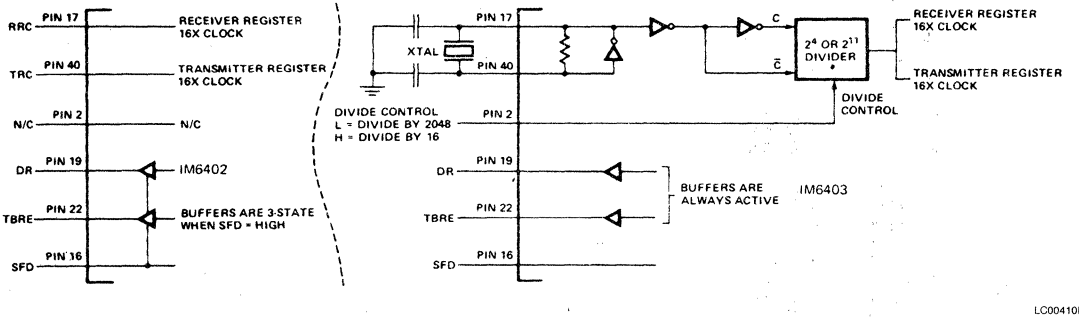


Figure 3: Functional Difference Between IM6402 and IM6403 UART (IM6403 has On-Chip 4/11 Stage Divider)

The IM6403 differs from the IM6402 on three Inputs (RRC, TRC, pin 2) as shown in Figure 3. Two outputs (TBRE, DR) are not three-state as on the IM6402, but are always active. The on-chip divider and oscillator allow an inexpensive crystal to be used as a timing source rather than additional circuitry such as baud rate generators. For example, a color TV crystal at 3.579545MHz results in a baud rate of 109.2Hz for an easy teletype interface (Figure 12). A 9600 baud interface may be implemented using a 2.4576MHz crystal with the divider set to divide by 16.

Note: All typical values have been guaranteed by characterization and are not tested.

IM6402/IM6403

INTERSIL

(IM6402AI/AM, IM6403AI/AM) ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD} - V_{SS}$) ..... +12.0V
Voltage On Any Input or Output Pin .....(V_{SS} −0.3V) to (V_{DD} +0.3V)

Operating Temperature Range
IM6402AI/03AI .....−40°C to +85°C
IM6402AM/03AM .....−55°C to +125°C
Storage Temperature Range .....−65°C to 150°C
Lead Temperature (Soldering, 10sec) .....300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 4.0V to 11.0V V_{SS} = 0V, T_A = Operating Temperature Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
V_{IH}	Input Voltage High		70% V_{DD}			V
V_{IL}	Input Voltage Low				10% V_{DD}	V
I_{IL}	Input Leakage [1] [3]	$V_{SS} \le V_{IN} \le V_{DD}$	−1.0		1.0	μA
V_{OH}	Output Voltage High	I_{OH} = 0mA		V_{DD}−0.01		V
V_{OL}	Output Voltage Low	I_{OL} = 0mA		V_{SS} + 0.01		V
I_{OLK}	Output Leakage	$V_{SS} \le V_{OUT} \le V_{DD}$	−1.0		1.0	μA
I_{CC}	Power Supply Current Standby	V_{IN} = V_{SS} or V_{DD}		5.0	500	μA
I_{CC}	Power Supply Current IM6402A	$f_{crystal}$ = 4MHz			9.0	mA
I_{CC}	Power Supply Current IM6403A	$f_{crystal}$ = 3.58MHz			13.0	mA
C_{IN}	Input Capacitance [1] [3]	T_A = 25°C		7.0	8.0	pF
C_O	Output Capacitance [1] [3]	T_A = 25°C		8.0	10.0	pF

NOTE: 1. Except IM6403 XTAL input pins (i.e. pins 17 and 40).
2. V_{DD} = 5V, T_A = 25°C.
3. These parameters are guaranteed but not 100% tested.

AC ELECTRICAL CHARACTERISTICS (V_{DD} = 10.0V ±5% V_{SS} = 0V, C_L = 50pF, T_A = Operating Temperature Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
f_c	Clock Frequency IM6402A	See Timing Diagrams (Figures 4,5,6)	D.C.		4.0	MHz
$f_{crystal}$	Crystal Frequency IM6403A				6.0	MHz
t_{pw}	Pulse Widths CRL, $\overline{DRR}$, $\overline{TBRL}$		100	40		ns
t_{mr}	Pulse Width MR		400	200		ns
t_{ds}	Input Data Setup Time		40	0		ns
t_{dh}	Input Data Hold Time		30	30		ns
t_{en}	Output Enable Time			40	70	ns

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Note: All typical values have been guaranteed by characterization and are not tested.

IM6402/IM6403

INTERSIL

(IM6402-1I/1M, IM6403-1I/1M) ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD} - V_{SS}$) ..... +8.0V
Voltage On Any Input or Output Pin ..... (V_{SS} -0.3V) to (V_{DD} +0.3V)

Operating Temperature Range
IM6402-1I/03-1I ..... -40°C to +85°C
IM6402-1M/03-1M ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 ±10% V_{SS} = 0V, T_A = Operating Temperature Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
V_{IH}	Input Voltage High		V_{DD}-2.0			V
V_{IL}	Input Voltage Low				0.8	V
I_{IL}	Input Leakage [1] [3]	$V_{SS} \le V_{IN} \le V_{DD}$	-1.0		1.0	µA
V_{OH}	Output Voltage High	I_{OH} = -0.2mA	2.4			V
V_{OL}	Output Voltage Low	I_{OL} = 2.0mA			0.45	V
I_{OLK}	Output Leakage	$V_{SS} \le V_{OUT} \le V_{DD}$	-1.0		1.0	µA
I_{CC}	Power Supply Current Standby	$V_{IN} = V_{SS}$ or V_{DD}		1.0	100	µA
I_{CC}	Power Supply Current IM6402 Dynamic	f_c = 2MHz			1.9	mA
I_{CC}	Power Supply Current IM6403 Dynamic	$f_{crystal}$ = 3.58MHz			5.5	mA
C_{IN}	Input Capacitance [1] [3]	T_A = 25°C		7.0	8.0	pF
C_O	Output Capacitance [1] [3]	T_A = 25°C		8.0	10.0	pF

NOTE: 1. Except IM6403 XTAL input pins (i.e. pins 17 and 40).
2. V_{DD} = 5V, T_A = 25°C.
3. These parameters are guaranteed but not 100% tested.

AC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0V ±10% V_{SS} = 0V, C_L = 50pF, T_A = Operating Temperature Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
f_c	Clock Frequency IM6402-1	See Timing Diagrams (Figures 4,5,6)	D.C.		2.0	MHz
$f_{crystal}$	Crystal Frequency IM6403-1				3.58	MHz
t_{pw}	Pulse Widths CRL, $\overline{DRR}$, $\overline{TBRL}$		150	50		ns
t_{mr}	Pulse Width MR		400	200		ns
t_{ds}	Input Data Setup Time		50	20		ns
t_{dh}	Input Data Hold Time		60	40		ns
t_{en}	Output Enable Time			80	160	ns

TIMING DIAGRAMS

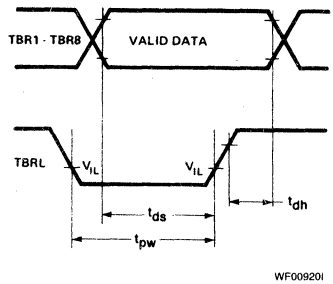


Figure 4: Data Input Cycle

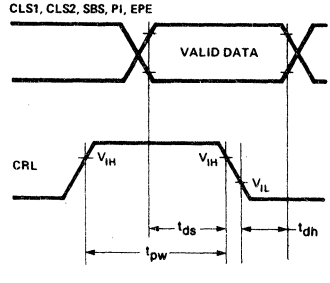


Figure 5: Control Register Load Cycle

Note: All typical values have been guaranteed by characterization and are not tested.

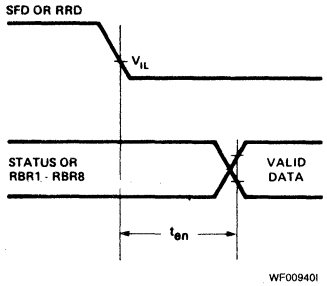


Figure 6: Status Flag Enable Time or Data Output Enable Time

Table 1: IM6402/3 Pin Description

PIN	SYMBOL	DESCRIPTION
1	V_{DD}	Positive Power Supply
2	IM6402-N/C IM6403-Control	No Connection Divide Control High: 2^4 (16) Divider Low: 2^{11} (2048) Divider
3	V_{SS}	Negative Supply
4	RRD	A high level on RECEIVER REGISTER DISABLE forces the receiver holding register outputs RBR1-RBR8 to a high impedance state.
5	RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.
6	RBR7	See Pin 5 — RBR8
7	RBR6	See Pin 5 — RBR8
8	RBR5	See Pin 5 — RBR8
9	RBR4	See Pin 5 — RBR8
10	RBR3	See Pin 5 — RBR8
11	RBR2	See Pin 5 — RBR8
12	RBR1	See Pin 5 — RBR8
13	PE	A high level on PARITY ERROR indicates that the received parity does not match parity programmed by control bits. The output is active until parity matches on a succeeding character. When parity is inhibited, this output is low.
14	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid. FE will stay active until the next valid character's stop bit is received.
15	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register. The Error is reset at the next character's stop bit if $\overline{DRR}$ has been performed (i.e., $\overline{DRR}$: active low).
16	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR*, TBRE* to a high impedance state. See Block Diagram and Figure 6. * IM6402 only.
17	IM6402-RRC IM6403-XTAL	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.
18	$\overline{DRR}$	A low level on DATA RECEIVED RESET clears the data received output (DR), to a low level.
19	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.
21	MR	A high level on MASTER RESET (MR) clears PE, FE, OE, DR, TRE and sets TBRE, TRO high. Less than 18 clocks after MR goes low, TRE returns high. MR does not clear the receiver buffer register, and is required after power-up.
22	TBRE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
23	$\overline{TBRL}$	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transition on $\overline{TBRL}$ requests data transfer to the transmitter register. If the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end. See Figure 4.
24	TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.

Note: All typical values have been guaranteed by characterization and are not tested.

IM6402/IM6403

Table 1: IM6402/3 Pin Description (CONT.)

PIN	SYMBOL	DESCRIPTION
25	TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.
26	TBR1	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-TBR8. For character formats less than 8-bits, the TBR8, 7, and 6 Inputs are ignored corresponding to the programmed word length.
27	TBR2	See Pin 26 — TBR1
28	TBR3	See Pin 26 — TBR1
29	TBR4	See Pin 26 — TBR1
30	TBR5	See Pin 26 — TBR1
31	TBR6	See Pin 26 — TBR1
32	TBR7	See Pin 26 — TBR1
33	TBR8	See Pin 26 — TBR1
34	CRL	A high level on CONTROL REGISTER LOAD loads the control register. See Figure 5.
35	PI*	A high level on PARITY INHIBIT inhibits parity generation, parity checking and forces PE output low.
36	SBS*	A high level on STOP BIT SELECT selects 1.5 stop bits for a 5 character format and 2 stop bits for other lengths.
37	CLS2*	These inputs program the CHARACTER LENGTH SELECTED. (CLS1 low CLS2 low 5-bits)(CLS1 high CLS2 low 6-bits)(CLS1 low CLS2 high 7-bits)(CLS1 high CLS2 high 8-bits)
38	CLS1*	See Pin 37 — CLS2
39	EPE*	When PI is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
40	IM6402-TRC IM6403-XTAL	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

*See Table 2 (Control Word Function)

TRANSMITTER OPERATION

The transmitter section accepts parallel data, formats it and transmits it in serial form (Figure 7) on the TROutput terminal.

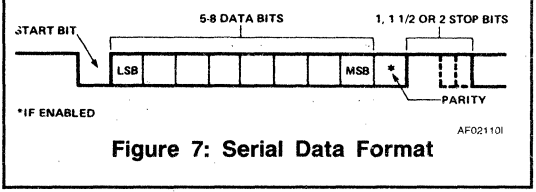


Figure 7: Serial Data Format

Transmitter timing is shown in Figure 8. Data is loaded into the transmitter buffer register from the inputs TBR1 through TBR8 by a logic low on the $\overline{TBRL}$ load input. Valid data must be present at least t_{DS} prior to and t_{DH} following the rising edge of $\overline{TBRL}$. If words less than 8 bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TBR1. The rising edge of $\overline{TBRL}$ clears TBREmpty. 0 to 1 clock cycles later, data is transferred to the transmitter register, TREmpty is cleared and transmission starts. TBREmpty is reset to a logic high. Output data is clocked by TRClock, which is 16 times the data rate. A second pulse on TBRLoad loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the current character is complete. Data is automatically transferred to the transmitter register and transmission of that character begins.

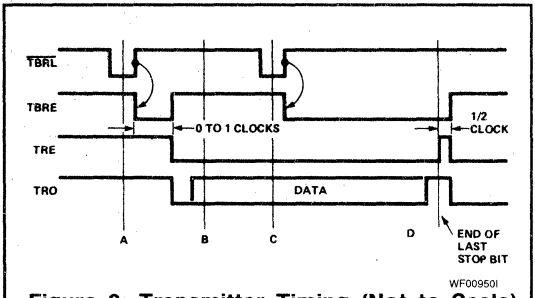


Figure 8: Transmitter Timing (Not to Scale)

Note: All typical values have been guaranteed by characterization and are not tested.

Table 2: Control Word Function

CONTROL WORD					DATA BITS	PARITY BIT	STOP BIT(S)
CLS2	CLS1	PI	EPE	SBS			
L	L	L	L	L	5	ODD	1
L	L	L	L	H	5	ODD	1.5
L	L	L	H	L	5	EVEN	1
L	L	L	H	H	5	EVEN	1.5
L	L	H	X	L	5	DISABLED	1
L	L	H	X	H	5	DISABLED	1.5
L	H	L	L	L	6	ODD	1
L	H	L	L	H	6	ODD	2
L	H	L	H	L	6	EVEN	1
L	H	L	H	H	6	EVEN	2
L	H	H	X	L	6	DISABLED	1
L	H	H	X	H	6	DISABLED	2
H	L	L	L	L	7	ODD	1
H	L	L	L	H	7	ODD	2
H	L	L	H	L	7	EVEN	1
H	L	L	H	H	7	EVEN	2
H	L	H	X	L	7	DISABLED	1
H	L	H	X	H	7	DISABLED	2
H	H	L	L	L	8	ODD	1
H	H	L	L	H	8	ODD	2
H	H	L	H	L	8	EVEN	1
H	H	L	H	H	8	EVEN	2
H	H	H	X	L	8	DISABLED	1
H	H	H	X	H	8	DISABLED	2

x = Don't Care

RECEIVER OPERATION

Data is received in serial form at the RI input. When no data is being received, RI input must remain high. The data is clocked by the RRClock, which is 16 times the data rate. Receiver timing is shown in Figure 9.

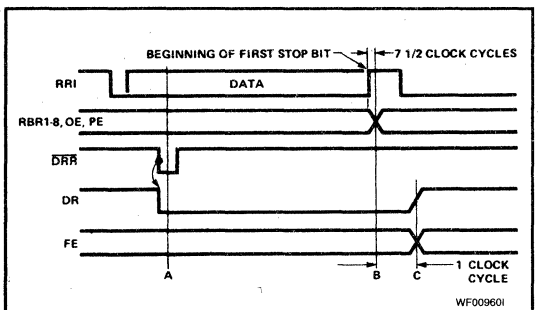


Figure 9: Receiver Timing (Not to Scale)

A low level on $\overline{DRR}$eset clears the DReady line. During the first stop bit, data is transferred from the receiver register to the RBRegister. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on OError indicates an overrun which occurs when DReady has not been cleared before the present character was transferred to the RBRegister. A logic high on PError indicates a parity error. 1/2 clock cycle later, DReady is set to a logic high and FError is evaluated. A logic high on FError indicates an invalid stop bit was received. The receiver will not begin searching for the next start bit until a stop bit is received.

START BIT DETECTION

The receiver uses a 16X clock for timing. (See Figure 10.) The start bit (A) could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The center of the start bit is defined as clock count 7½. If the receiver clock is a symmetrical square wave, the center of the start bit will be located within ±1/2 clock cycle, ±1/32 bit or ±3.125%. The receiver begins searching for the next start bit at the center of the first stop bit.

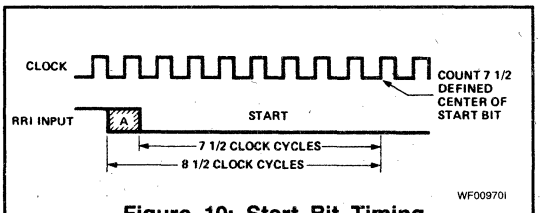


Figure 10: Start Bit Timing

TYPICAL APPLICATION

Microprocessor systems, which are inherently parallel in nature, often require an asynchronous serial interface. This function can be performed easily with the IM6402/03 UART. Figure 11 shows how the IM6402 can be interfaced to an IM80C48 microcomputer system.

Note: All typical values have been guaranteed by characterization and are not tested.

IM6402/IM6403

In this example the characters to be received or transmitted will be eight bits long (CLS 1 and 2: both HIGH) and transmitted with no parity (PI:HIGH) and two stop bits (SBS:HIGH). Since these control bits will not be changed during operation, Control Register Load (CRL) can be tied high. Remember, since the IM6402/03 is a CMOS device, all unused inputs *should be tied to either V_{DD} or V_{SS}.*

The baud rate at which the transmitter and receiver will operate is determined by the IM4702 Baud Rate Generator.

To ensure consistent and correct operation, the IM6402/03 must be reset after power-up. The Master Reset (MR) pin is active high, and can be driven reliably from a Schmitt trigger inverter and R-C delay. In this example, the IM80C48 is reset through still another inverter. The Schmitt trigger between the processor and R-C network is needed to assure that a slow rising capacitor voltage does not retrigger RESET. A long reset pulse after power-up (~20ms) is required by the processor to assure that the on-board crystal oscillator has sufficient time to start.

If parity is not inhibited, a parity error will cause the PE pin to go high until the next valid character is received.

A framing error is generated when an expected stop bit is not received. FE will stay high after the error until the next complete character's stop bit is received.

The overrun error flag is set if a received character is transferred to the RECEIVER BUFFER REGISTER when the previous character has not been read. The OE pin will stay high until the next received stop bit after a $\overline{DRR}$ is performed.

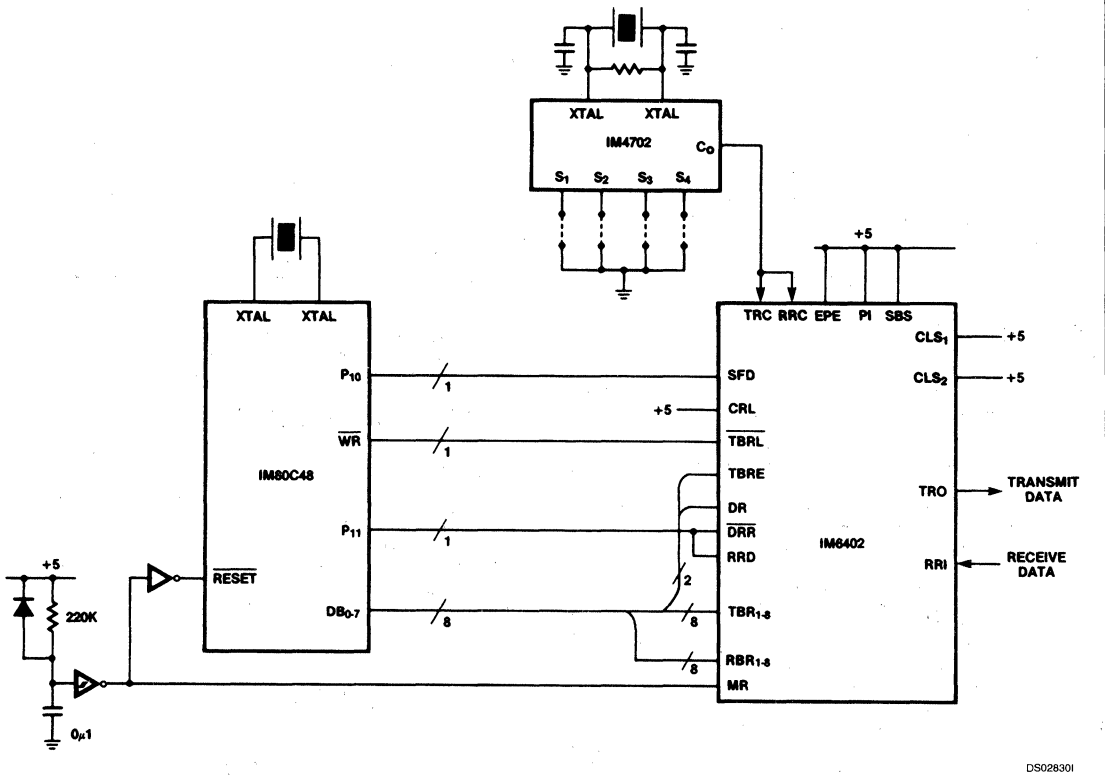


Figure 11: IM80C48 Interface to IM6402

Note: All typical values have been guaranteed by characterization and are not tested.

IM6653/IM6654
4096-Bit CMOS UV EPROM

GENERAL DESCRIPTION

The Intersil IM6653 and IM6654 are fully decoded 4096 bit CMOS electrically programmable ROMs (EPROMs) fabricated with Intersil's advanced CMOS processing technology. In all static states these devices exhibit the microwatt power dissipation typical of CMOS. Inputs and three-state outputs are TTL compatible and allow for direct interface with common system bus structures. On-chip address registers and chip select functions simplify system interfacing requirements.

The IM6653 and IM6654 are specifically designed for program development applications where rapid turn-around for program changes is required. The devices may be erased by exposing their transparent lids to ultra-violet light, and then re-programmed.

FEATURES

- **Organization — IM6653: 1024 x 4**
  IM6654: 512 x 8
- **Low Power — 770μW Maximum Standby**
- **High Speed**
  - 300ns 10V Access Time For IM6653/54 AI
  - 450ns 5V Access Time For IM6653/54-1I
- **Single +5V Supply Operation**
- **UV Erasable**
- **Synchronous Operation For Low Power Dissipation**
- **Three-State Outputs and Chip Select for Easy System Expansion**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IM6653/4IJG	−40°C to +85°C	24-Pin CERDIP
IM6653/4-1IJG	−40°C to +85°C	24-Pin CERDIP
IM6653/4AIJG	−40°C to +85°C	24-Pin CERDIP
IM6653/4MJG*	−55°C to +125°C	24-Pin CERDIP
IM6653/4AMJG*	−55°C to +125°C	24-Pin CERDIP

* Add /HR for HiRel processing

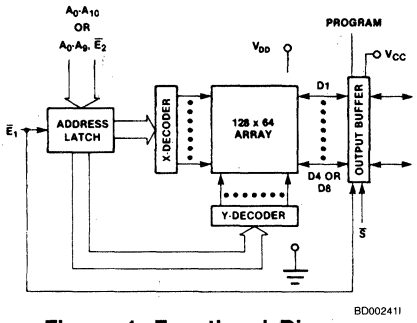


Figure 1: Functional Diagram

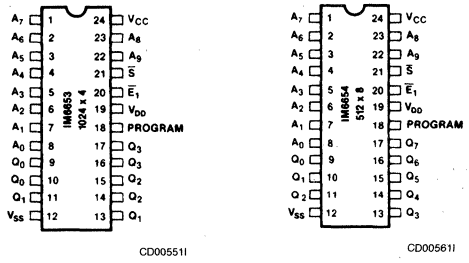


Figure 2: Pin Configurations

9

002

Note: All typical values have been guaranteed by characterization and are not tested.

IM6653/IM6654

INTERSIL

ABSOLUTE MAXIMUM RATINGS (IM6653/54 I, -1I, M)

Supply Voltages
- $V_{DD} - V_{SS}$ ..... +8.0V
- $V_{CC} - V_{SS}$ ..... +8.0V

Input or Output Voltage ....(V_{SS} -0.3V) to (V_{DD} +0.3V)

Operating Range Range (T_A)
- Industrial ..... -40°C to +85°C
- Military ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (Soldering, 10sec) .....300°C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = V_{DD} = 5V \pm 10\%$ $V_{SS} = 0V$, T_A = Operating Temperature Range)

SYMBOL	PARAMETER	TEST CONDITIONS	IM6653/54I, -1I, M		UNIT
			MIN	MAX	
V_{IH}	Logical "1" Input Voltage	$\overline{E}_1$, $\overline{S}$	$V_{DD} - 2.0$		V
V_{IH}		Address Pins	2.7		
V_{IL}	Logical "0" Input Voltage			0.8	
I_I	Input Leakage	$GND \le V_{IN} \le V_{DD}$	-1.0	1.0	µA
V_{OH}	Logical "1" Output Voltage	$I_{OH} = -0.2mA$	2.4		V
V_{OL}	Logical "0" Output Voltage	$I_{OL} = 2.0mA$		0.45	
I_{OLK}	Output Leakage	$GND \le V_O \le V_{CC}$	-1.0	1.0	µA
I_{STBY}	Standby Supply Current	$V_{IN} = V_{DD}$		100	
I_{CC}		$V_{IN} = V_{DD}$		40	
I_{DD}	Operating Supply Current (1)	f = 1MHz		6	mA
C_I	Input Capacitance	Note 1		7.0	pF
C_O	Output Capacitance	Note 1		10.0	

Note: 1. For design reference only, not 100% tested.

AC ELECTRICAL CHARACTERISTICS

($V_{CC} = V_{DD} = 5V \pm 10\%$ $V_{SS} = 0V$, $C_L = 50pf$, T_A = Operating Temperature Range)

SYMBOL	PARAMETER	IM6653/54-1I		IM6653/54 I		IIM6653/54 M		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
TE_1LQV	Access Time From $\overline{E}_1$		450		550		600	ns
TSLQV	Output Enable Time		110		140		150	
TE_1HQZ	Output Disable Time		110		140		150	
TE_1HE_1L	$\overline{E}_1$ Pulse Width (Positive)	130		150		150		
TE_1LE_1H	$\overline{E}_1$ Pulse Width (Negative)	450		550		600		
$TAVE_1L$	Address Setup Time	0		0		0		
TE_1LAX	Address Hold Time	80		100		100		
TE_2VE_1L	Chip Enable Setup Time (6654)	0		0		0		
TE_1LE_2X	Chip Enable Hold Time (6654)	80		100		100		

Note: All typical values have been guaranteed by characterization and are not tested.

IM6653/IM6654

ABSOLUTE MAXIMUM RATINGS (IM6653/54AI, AM)

Supply Voltages
- $V_{DD} - V_{SS}$ ..... +11.0V
- $V_{CC} - V_{SS}$ ..... +11.0V

Input or Output Voltage ....(V_{SS} −0.3V) to (V_{DD} +0.3V)

Operating Temperature Range
- Industrial .....−40°C to +85°C
- Military .....−55°C to +125°C

Storage Temperature Range ..... −65°C to +150°C

Lead Temperature (Soldering, 10sec) .....300°C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = V_{DD} = 4.5V$ to 10.5V $V_{SS} = 0V$, T_A = Operational Temperature Range)

SYMBOL	PARAMETER	TEST CONDITIONS	IM6653/54AI, AM		UNIT
			MIN	MAX	
V_{IH}	Logical "1" Input Voltage	$\overline{E}_1$, $\overline{S}$	$V_{DD} - 2.0$		V
V_{IH}		Address Pins	$V_{DD} - 2.0$		
V_{IL}	Logical "0" Input Voltage			0.8	
I_I	Input Leakage	$GND \le V_{IN} \le V_{DD}$	−1.0	1.0	μA
V_{OH}	Logical "1" Output Voltage	$I_{OUT} = 0$ (Note 1)	$V_{CC} - 0.01$		V
V_{OL}	Logical "0" Output Voltage	$I_{OUT} = 0$ (Note 1)		$V_{SS} + 0.01$	
I_{OLK}	Output Leakage	$V_{SS} \le V_O \le V_{CC}$	−1.0	1.0	μA
I_{STBY}	Standby Supply Current	$V_{IN} = V_{DD}$		100	
I_{CC}		$V_{IN} = V_{DD}$		40	
I_{DD}	Operating Supply Current	f = 1MHz		12	mA
C_I	Input Capacitance	Note 1		7.0	pF
C_O	Output Capacitance	Note 1		10.0	

Note: 1. For design reference only, not 100% tested.

AC ELECTRICAL CHARACTERISTICS

($V_{CC} = V_{DD} = 10V \pm 5\%$ $V_{SS} = 0V$, $C_L = 50pf$, T_A = Operating Temperature Range)

SYMBOL	PARAMETER	IM6653/54 AI		IM6653/54 AM		UNIT
		MIN	MAX	MIN	MAX	
TE_1LQV	Access Time From $\overline{E}_1$		300		350	ns
TSLQV	Output Enable Time		60		70	
TE_1HQZ	Output Disable Time		60		70	
TE_1HE_1L	$\overline{E}_1$ Pulse Width (Positive)	125		125		
TE_1LE_1H	$\overline{E}_1$ Pulse Width (Negative)	300		350		
$TAVE_1L$	Address Setup Time	0		0		
TE_1LAX	Address Hold Time	60		60		
TE_2VE_1L	Chip Enable Setup Time (6654)	0		0		
TE_1LE_2X	Chip Enable Hold Time (6654)	60		60		

Note: All typical values have been guaranteed by characterization and are not tested.

IM6653/IM6654

PIN ASSIGNMENTS

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1-8,23	A_0-A_7,A_8	–	Address Lines
9-11, 13-17	Q_0-Q_7 Q_0-Q_3	– –	Data Out lines, 6654 Data Out lines, 6653
12	V_{SS}	–	Negative Supply
18	Program	–	Programming pulse input
19	V_{DD}	–	Chip positive supply, normally tied to V_{CC}
20	$\overline{E}_1$	L	Strobe line, latches both address lines and, for 6654, Chip enable $\overline{E}_2$
21	$\overline{S}$	L	Chip select line, must be low for valid data out
22	Ag $\overline{E}_2$	– L	Additional address line for 6653 Chip enable line, latched by Chip enable $\overline{E}_1$ on 6654
24	V_{CC}	–	Output buffer positive supply

READ MODE OPERATION

In a typical READ operation address lines and chip enable $\overline{E}_2$* are latched by the falling edge of chip enable $\overline{E}_1$ (T = 0). Valid data appears at the outputs one access time (TELQV) later, provided level-sensitive chip select line $\overline{S}$ is low (T = 3). Data remains valid until either $\overline{E}_1$ or $\overline{S}$ returns to a high level (T = 4). Outputs are then forced to a high-Z state.

Address lines and $\overline{E}_2$ must be valid one setup time before (TAVEL), and one hold time after (TELAX), the falling edge of $\overline{E}_1$ starting the read cycle. Before becoming valid, Q output lines become active (T = 2). The Q output lines return to a high-Z state one output disable time (TE_1HQZ) after any rising edge on $\overline{E}_1$ or $\overline{S}$.

The program line remains high throughout the READ cycle.

Chip enable line $\overline{E}_1$ must remain high one minimum positive pulse width (TEHEL) before the next cycle can begin.

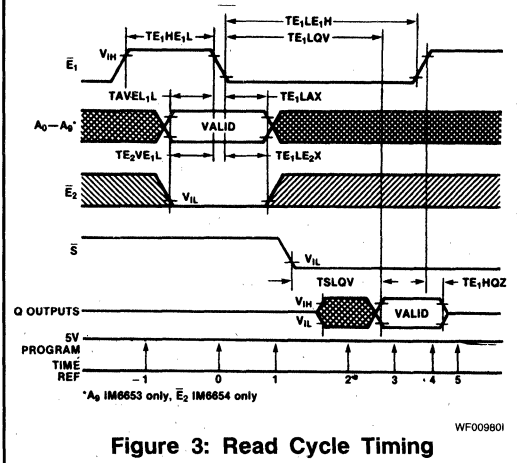


Figure 3: Read Cycle Timing

FUNCTION TABLE

TIME REF	INPUTS				OUTPUTS Q	NOTES
	$\overline{E}1$	$\overline{E}2$	$\overline{S}$	A		
–1	H	X	X	X	Z	DEVICE INACTIVE
0	↘	L	X	V	Z	CYCLE BEGINS; ADDRESSES, $\overline{E}_2$ LATCHED*
1	L	X	X	X	Z	INTERNAL OPERATIONS ONLY
2	L	X	L	X	A	OUTPUTS ACTIVE UNDER CONTROL OF $\overline{E}_1$, $\overline{S}$
3	L	X	L	X	V	OUTPUTS VALID AFTER ACCESS TIME
4	↗	X	L	X	V	READ COMPLETE
5	H	X	X	X	Z	CYCLE ENDS (SAME AS –1)

Note: All typical values have been guaranteed by characterization and are not tested.

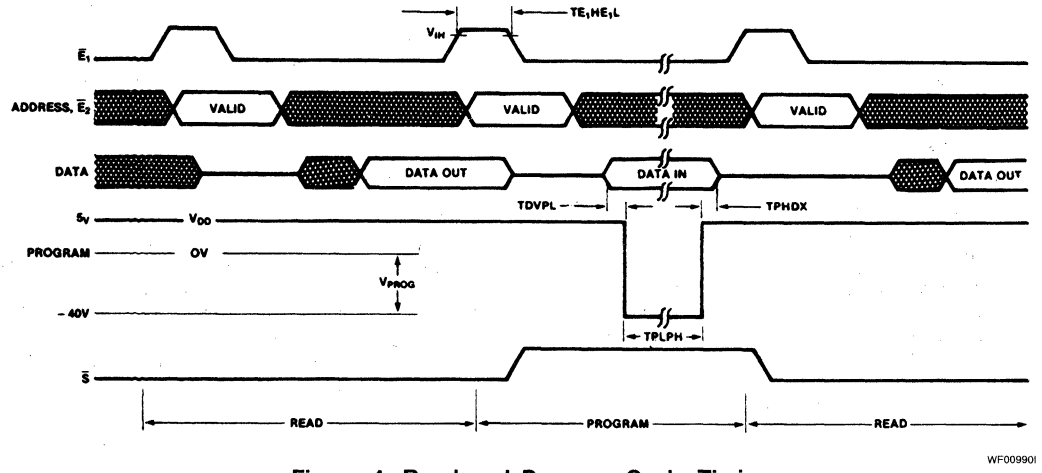


Figure 4: Read and Program Cycle Timing

DC CHARACTERISTICS FOR PROGRAMMING OPERATION

($V_{CC} = V_{DD} = 5V \pm 5\%$ $V_{SS} = 0V$, $T_A = 25°C$)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{PROG}	Program Pin Load Current			80	100	mA
V_{PROG}	Programming Pulse Amplitude		-38	-40	-42	V
I_{CC}	V_{CC} Current			0.1	5	mA
I_{DD}	V_{DD} Current			40	100	
V_{IHA}	Address Input High Voltage		$V_{DD}-2.0$			V
V_{ILA}	Address Input Low Voltage				0.8	
V_{IH}	Data Input High Voltage		$V_{DD}-2.0$			
V_{IL}	Data Input Low Voltage				0.8	

AC CHARACTERISTICS FOR PROGRAMMING OPERATION

($V_{CC} = V_{DD} = 5V \pm 5\%$ $V_{SS} = 0V$, $T_A = 25°$)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TPLPH	Program Pulse Width	$t_{rise} = t_{fall} = 5\mu s$	18	20	22	ms
	Program Pulse Duty Cycle				75%	
TDVPL	Data Setup Time		9			μs
TPHDX	Data Hold Time		9			
TE_1HE_1L	Strobe Pulse Width		150			ns
$TAVE_1L$	Address Setup Time		0			
TE_1LE_1X	Address Hold Time		100			
TE_1LQV	Access Time				1000	

PROGRAM MODE OPERATION

Initially, all 4096 bits of the EPROM are in the logic one (output high) state. Selective programming of proper bit locations to "0"s is performed electrically.

In the PROGRAM mode for all EPROMs, V_{CC} and V_{DD} are tied together to a +5V operating supply. High logic levels at all of the appropriate chip inputs and outputs must be set at V_{DD} -2V minimum. Low logic levels must be set at V_{SS} +0.8V maximum. Addressing of the desired location in PROGRAM mode is done as in the READ mode. Address and data lines are set at the desired logic levels, and PROGRAM and chip select ($\overline{S}$) pins are set high. The address is latched by the downward edge on the strobe line ($\overline{E}_1$). During valid DATA IN time, the PROGRAM pin is pulsed from V_{DD} to -40V. This pulse initiates the program-

Note: All typical values have been guaranteed by characterization and are not tested.

IM6653/IM6654

ming of the device to the levels set on the data outputs. Duty cycle limitations are specified from chip heat dissipation considerations. PULSE RISE AND FALL TIMES MUST NOT BE FASTER THAN 5μs.

Intelligent programmer equipment with successive READ/PROGRAM/VERIFY sequences is recommended.

PROGRAMMING SYSTEM CHARACTERISTICS

1. During programming the power supply should be capable of limiting peak instantaneous current to 100mA.
2. The programming pin is driven from V_{DD} to −40 volts (±2V) by pulses of 20 milliseconds duration. These pulses should be applied in the sequence shown in the flow chart. Pulse rise and fall times of 10 microseconds are recommended. Note that any individual location may be programmed at any time.
3. Addresses and data should be presented to the device within the recommended setup/hold time and high/low logic level margins. Both "A" (10V) and non "A" EPROMs are programmed at V_{CC}, V_{DD} of 5V ±5%.
4. Programming is to be done at room temperature.

ERASING PROCEDURE

The IM6653/54 are erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 2537Å. The recommended integrated dose (i.e., UV intensity x exposure time) is 10W sec/cm^2. The lamps should be used without short-wave filters, and the IM6653/54 to be erased should be placed about one inch away from the lamp tubes. For best results it is recommended that the device remain inactive for 5 minutes after erasure, before reprogramming.

The erasing effect of UV light is cumulative. Care should be taken to protect EPROMs from exposure to direct sunlight or fluorescent lamps radiating UV light in the 2000Å to 4000Å range.

Note: All typical values have been guaranteed by characterization and are not tested.

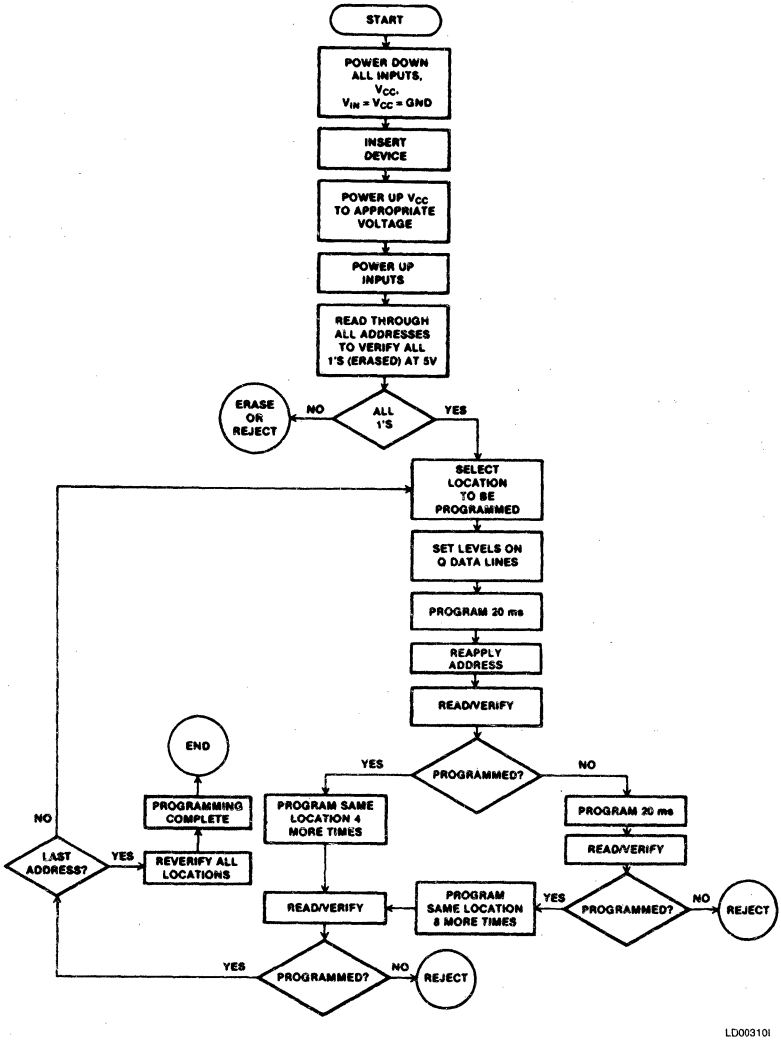


Figure 5: Programming Flow Chart

9

Note: All typical values have been guaranteed by characterization and are not tested.

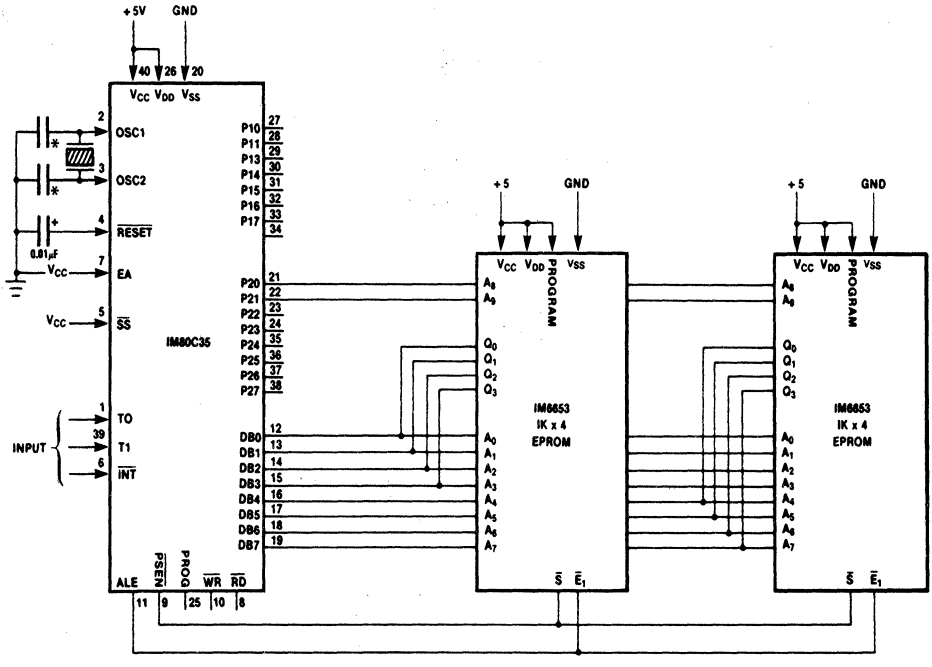


Figure 6: IM6653 CMOS EPROMS as External Program Memory with the IM80C35

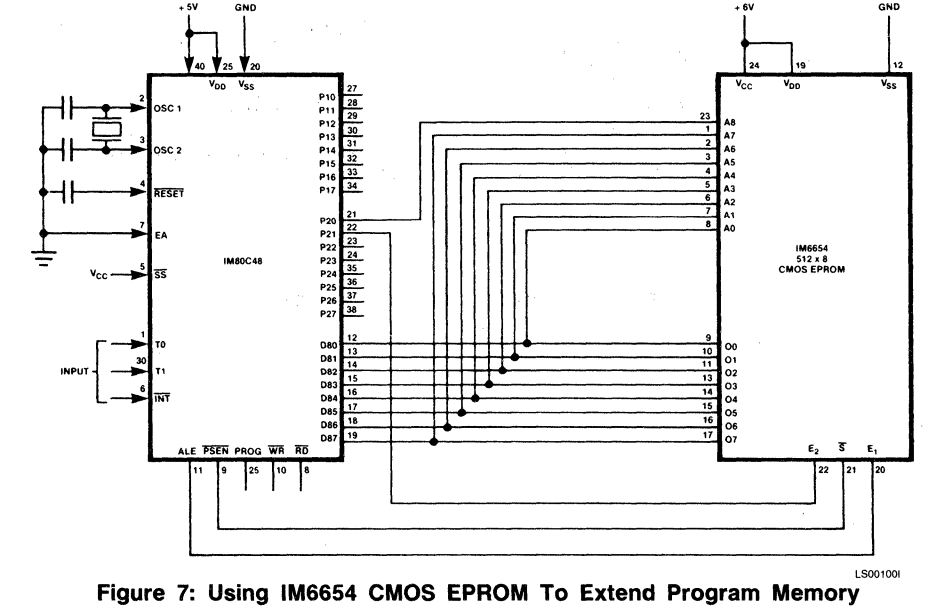


Figure 7: Using IM6654 CMOS EPROM To Extend Program Memory

Note: All typical values have been guaranteed by characterization and are not tested.

IM80C48/49/35/39
CMOS Microcontroller

GENERAL DESCRIPTION

The Intersil IM80C48 family of CMOS microcontrollers combines the speed of the industry standard NMOS8048 with the low power consumption of CMOS. In addition to the low operating current, the IM80C48 family has three versatile power-down modes that reduce power dissipation even further. The HALT mode, entered by software command, shuts down selected portions of the CPU to reduce power consumption while retaining rapid response time to an interrupt or reset. The STandBY and STOP modes shut down all but the onboard RAM, reducing the supply current to typically 1 microamp.

The IM80C48 family microcontrollers include 27 I/O lines, RAM, and an 8-bit timer/counter on-chip, and are well suited for control applications. The low power consumption of the IM80C48 makes it particularly desirable in applications that require battery operation or long term battery backup of on-chip RAM during AC power interruptions.

FEATURES

- **Industry Standard NMOS 8048 Family Compatible**
- **Expanded Instruction Set Includes Software STandBY**
- **Ultra Low Power Consumption**
  - **Operating Supply Current: 3mA at 6MHz**
  - **IDLe Supply Current: 800μA at 6MHz**
  - **STandBY and STOP Modes: 1μA**
- **Wide Operating Voltage Range — 3.5V to 6V**
- **Compatible with 8048/80/85 Peripherals**
- **4 Standard ROM and ROM-Less Versions**

APPLICATIONS

- **Portable Instrumentation**
- **Telecom**
- **Industrial Control**
- **Battery Operated Equipment**

ORDERING INFORMATION

BASIC PART NUMBER	SUFFIX				INTERNAL MEMORY	
	TEMP. RANGE: 0°C to +70°C		TEMP. RANGE: -40°C to +85°C		ROM	RAM
	40-PIN PLASTIC	40-PIN CERDIP	40-PIN PLASTIC	40-PIN CERDIP		
IM80C48	CPL	CJL	IPL	IJL	1K x 8	64 x 8
IM80C49	CPL	CJL	IPL	IJL	2K x 8	128 x 8
IM80C35	CPL	CJL	IPL	IJL	NONE	64 x 8
IM80C39	CPL	CJL	IPL	IJL	NONE	128 x 8

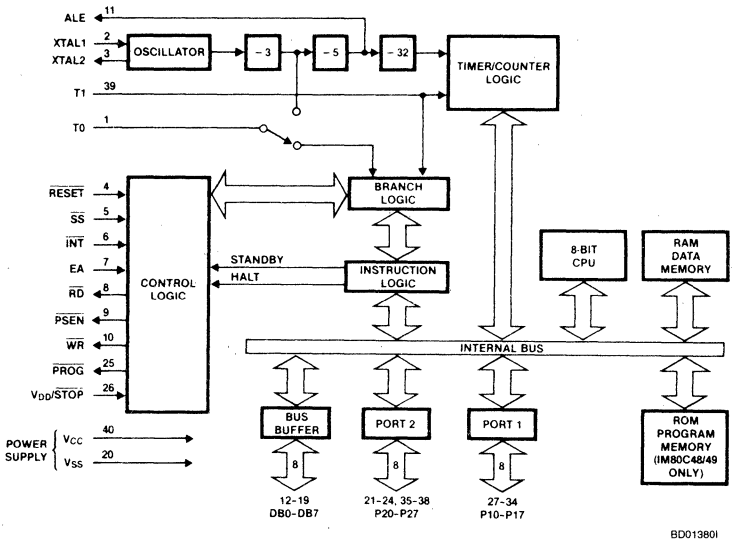


Figure 1: Functional Diagram

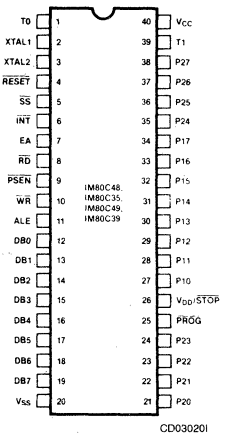


Figure 2: Pin Configuration

105003-003

Note: All typical values have been guaranteed by characterization and are not tested.

IM80C48/49/35/39

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin .....(V_{SS} − 0.3V) to (V_{CC} + 0.3V)
Supply Voltage.....(V_{CC} − V_{SS}) + 8V
Storage Temperature (Plastic) ..... −65°C to + 150°C

Operating Temperature Range:
IM80CXXCXL ..... 0°C to + 70°C
IM80CXXIXL .....−40°C to + 85°C
Lead Temperature (Soldering, 10sec) .....300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS
DC CHARACTERISTICS

Test Conditions: V_{CC} = 5V±10% V_{SS} = 0V, T_A = −40°C to + 85°C

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{IL}	Input Low Voltage (All Except XTAL1)		−0.3		0.8	V
V_{IL1}	Input Low Voltage XTAL1				V_{CC} − 0.8	V
V_{IH}	Input High Voltage (All Except $\overline{RESET}$, XTAL1, $V_{DD}/\overline{STOP}$)		V_{CC} − 2V		V_{CC}	V
V_{IH1}	Input High Voltage $\overline{RESET}$, XTAL1, XTAL2, $V_{DD}/\overline{STOP}$		V_{CC} − 0.5V		V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA			0.45	V
V_{OH}	Output High Voltage BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE	I_{OH} = −100μA	2.4			V
V_{OH1}	Output High Voltage All Other Outputs	I_{OH} = −50μA	2.4			V
I_{ILP}	Input Pullup Current Port 1, Port 2	$V_{IN} \le V_{IL}$		−150	−300	μA
I_{IL}	Input Pullup Current $\overline{SS}$, $\overline{RESET}$	$V_{IN} \le V_{IL}$		−20	−40	μA
I_{IL}	Input Leakage Current T1, EA, $\overline{INT}$	$V_{SS} \le V_{CC}$		0	±1	μA
I_{OL}	Output Leakage Current Bus, TO-High Impedance	$V_{SS} \le V_{IN} \le V_{CC}$		0	±1	μA
I_{CC}	Total Supply Current	T_A = 25°C, 6MHz		3	8	mA
I_{CC1}	IDLE Power Supply Current	6MHz		0.8	2.0	mA
I_{CC2}	STandBY and STOP Modes Supply Current	$V_{IN} = V_{CC}$		1	20	μA

AC CHARACTERISTICS
PORT 2 TIMING

Test Conditions: V_{CC} = 5V±10% V_{SS} = 0V, T_A = −40°C to + 85°C, f_{CLK} = 6MHz

SYMBOL	PARAMETER	TEST CONDITIONS (Note 1)	LIMITS			UNIT
			MIN	TYP	MAX	
t_{CP}	Port Control Setup Before Falling Edge of $\overline{PROG}$		110			nS
t_{PC}	Port Control Hold after Falling Edge of $\overline{PROG}$		140			nS
t_{PR}	$\overline{PROG}$ to Time Port 2 Input Data must be valid				810	nS
t_{DP}	Output Data Setup Time		220			ns
t_{PD}	Output Data Hold Time		65			ns
t_{PF}	Input Data Hold Time		0		150	ns
t_{PP}	$\overline{PROG}$ Pulse Width		1200			ns
t_{PL}	Port 2 I/O Data Setup		350			ns
t_{LP}	Port 2 I/O Data Hold		150			ns

Note 1: Inputs are driven to 0.45V and 2.4V. Output timing measurements are made at 0.8V and 2.0V.

Note: All typical values have been guaranteed by characterization and are not tested.

READ, WRITE AND INSTRUCTION FETCH — EXTERNAL DATA AND PROGRAM MEMORY

Test Conditions: V_{CC} = 5V±10% V_{SS} = 0V, T_A = −40°C to +85°C, f_{CLK} = 6MHz

SYMBOL	PARAMETER	TEST CONDITIONS (Note 1)	LIMITS			UNIT
			MIN	TYP	MAX	
t_{LL}	ALE Pulse Width		400			ns
t_{AL}	Address Setup before ALE Falling		120			ns
t_{LA}	Address Hold from ALE Falling		80			ns
t_{CC}	Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)		700			ns
t_{DW}	Data Setup before $\overline{WR}$ Rising		500			ns
t_{WD}	Data Hold after $\overline{WR}$ Rising	C_L = 20pF	120			ns
t_{CY}	Cycle Time		2.5		150	μs
t_{DR}	Data Hold		0		200	ns
t_{RD}	$\overline{PSEN}$, $\overline{RD}$ to Data in Valid				500	ns
t_{AW}	Address Setup before $\overline{WR}$		230			ns
t_{AD}	Address Setup before Data in				950	ns
t_{AFC}	Address Float to $\overline{RD}$, $\overline{PSEN}$		0			ns

Note 1: For Control Outputs C_L = 80pF, for Bus Outputs C_L = 150pF. Inputs are driven to 0.45V and 2.4V. Output timing measurements are made at 0.8V and 2.0V.

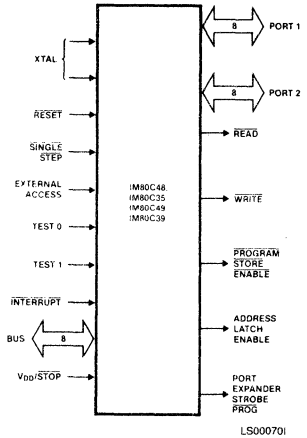


Figure 3: Logic Symbol

ROM CODE DATA ENTRY

Intersil can accept customer ROM codes in a variety of media, including standard byte-wide EPROMs (2176, 2732, 2764, 27C16, 27C32, etc.) or (8048, 8748, 8049, 8749) microcomputers.

Contact GE-Intersil sales office for other formats.

ROM CODE VERIFICATION (IM80C48/49)

The IM80C48/49 ROM code can be verified by applying negative 5V to the EA pin while $\overline{RESET}$ is low. The address is then applied to DB0-DB7 and P20-P22. Bringing $\overline{RESET}$ high will internally latch the address and cause the ROM content for that address to appear on DB0-DB7. This verify cycle can then be repeated by returning $\overline{RESET}$ low and applying the next address to DB0-DB7 and P20-P22; then bringing $\overline{RESET}$ high to read the ROM content. To exit the verify mode first set $\overline{RESET}$ low then return EA to 0V.

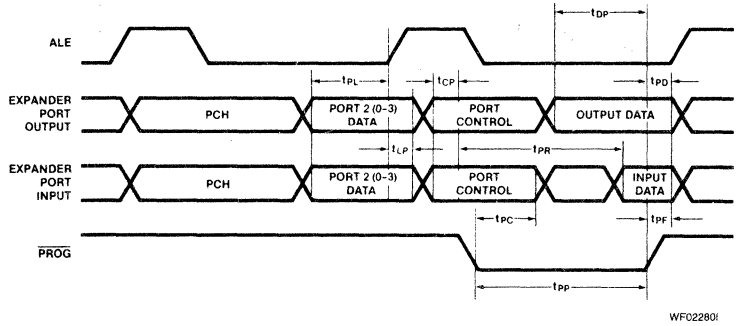


Figure 4: Port 2 Timing

Note: All typical values have been guaranteed by characterization and are not tested.

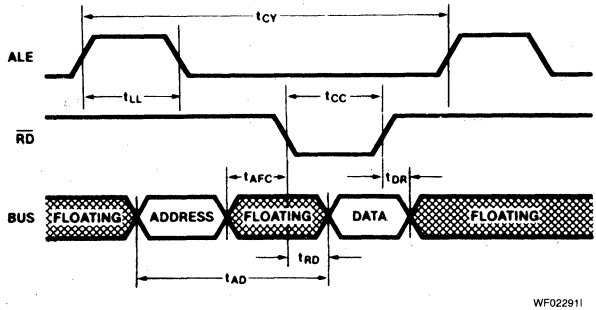


Figure 5: Read From External Data Memory

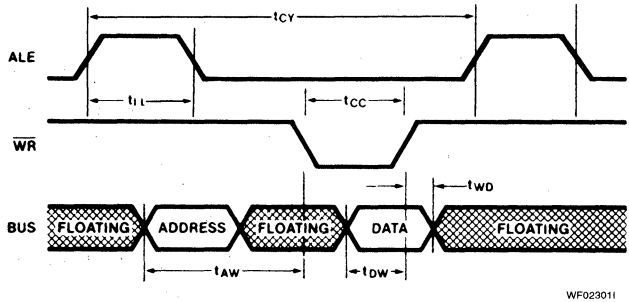


Figure 6: Write to External Data Memory

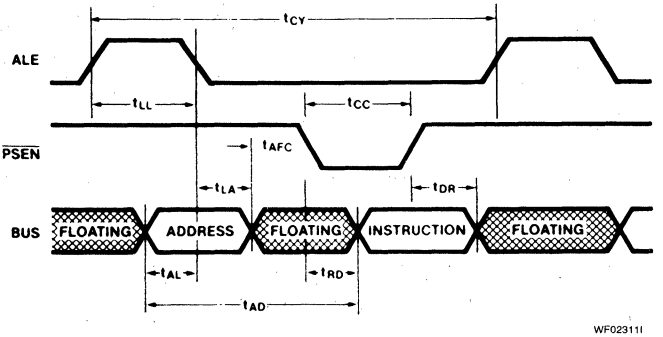


Figure 7: Instruction Fetch From External Program Memory

Note: All typical values have been guaranteed by characterization and are not tested.

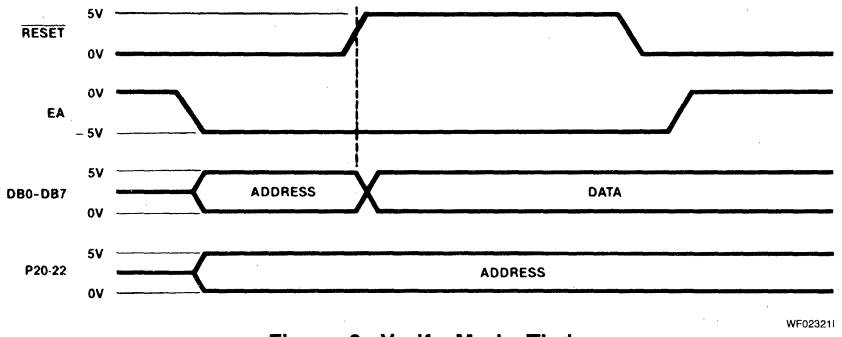


Figure 8: Verify Mode Timing

Table 1: Pin Description

PIN NAME	PIN	FUNCTION
T0	1	An input pin that is tested by the conditional jump instructions JT0 and JNT0. This pin can be designated as a clock output using the ENT0 CLK instruction.
XTAL1	2	Connected to one side of the crystal for internal oscillator operation. Also used as the external clock input when using an external oscillator.
XTAL2	3	Connected to one side of the crystal when using the internal oscillator. Leave open when using an external oscillator.
$\overline{RESET}$	4	Active low input used to reset the microcomputer. A capacitor from this pin to ground will automatically reset the device on power-up.
$\overline{SS}$	5	Single-Step input, active low, that can be used in conjunction with ALE to single-step the processor through each instruction.
$\overline{INT}$	6	$\overline{INT}$errupt input, active low. Initiates an interrupt if external interrupt is enabled.
EA	7	External Access input, active high, is used to force all program memory accesses to reference external memory.
$\overline{RD}$	8	This output, active low, is used by external devices to place data onto the bus during a bus read operation.
$\overline{PSEN}$	9	$\overline{P}$rogram $\overline{S}$tore $\overline{EN}$able. This output, active low, occurs only during fetches to external program memory. The system uses this signal to strobe external program memory.
$\overline{WR}$	10	This output, active low, is used to strobe data into external devices during a bus write operation.
ALE	11	Address Latch Enable. This output, active high, occurs once during each cycle. The falling edge of this timing signal is used to strobe the address bits appearing on the data bus.
DB0 – DB7 (Bus)	12 – 19	Data Bus. These eight lines form a true bidirectional port which can store data as a latched output port or serve as a non-latching input/output port.
V_{SS}	20	Circuit GND potential.
P20 – P27	21 – 24 35 – 38	Port 2. Identical to Port 1 except that P20 – P23 contain the four high-order program counter bits during external program memory fetches. If IM82C43 I/O Expanders are being used in the system, they communicate with the IM80C48 through these four lines.
$\overline{PROG}$	25	Output strobe for IM82C43 I/O Expander.
$V_{DD}/\overline{STOP}$	26	Used to select low power hardware STOP mode.
P10 – P17	27 – 34	Port 1. An 8-bit quasi-bidirectional port. The I/O structure on these eight lines allows each to be used separately as an input or output.
T1	39	An input pin tested by the conditional jump instructions, JT1 and JNT1. The pin can also be programmed as the input to the counter.
V_{DD}	40	Main power supply.

Note: All typical values have been guaranteed by characterization and are not tested.

IM80C48/49/35/39

Table 2. Instruction Set by Mnemonic

Accumulator Mnemonic	Description	Bytes	Cycles
ADD A, R	Add register to A	1	1
ADD A, @R	Add data memory to A	1	1
ADD A, # data	Add immediate to A	2	2
ADDC A, R	Add register with carry	1	1
ADDC A, @R	Add data memory with carry	1	1
ADDC A, # data	Add immediate with carry	2	2
ANL A, R	And register to A	1	1
ANL A, @R	And data memory to A	1	1
ANL A, # data	And immediate to A	2	2
ORL A, R	Or register to A	1	1
ORL A, @R	Or data memory to A	1	1
ORL A, # data	Or immediate to A	2	2
XRL A, R	Exclusive or register to A	1	1
XRL A, @R	Exclusive or data memory to A	1	1
XRL, A, # data	Exclusive or immediate to A	2	2
INC A	Increment A	1	1
DEC A	Decrement A	1	1
CLR A	Clear A	1	1
CPL A	Complement A	1	1
DA A	Decimal adjust A	1	1
SWAP A	Swap nibbles of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1

Input/Output Mnemonic	Description	Bytes	Cycles
IN A, P	Input port to A	1	2
OUTL P, A	Output A to port	1	2
ANL P, # data	And immediate to port	2	2
ORL P, # data	Or immediate to port	2	2
INS A, BUS	Input BUS to A	1	2
OUTL BUS, A	Output A to BUS	1	2
ANL BUS, # data	And immediate to BUS	2	2
ORL BUS, # data	Or immediate to BUS	2	2
MOVD A, P	Input expander port to A	1	2
MOVD P, A	Output A to expander port	1	2
ANLD P, A	And A to expander port	1	2
ORLD P, A	Or A to expander port	1	2

Registers Mnemonic	Description	Bytes	Cycles
INC R	Increment register	1	1
INC @R	Increment data memory	1	1
DEC R	Decrement register	1	1

Branch Mnemonic	Description	Bytes	Cycles
JMP addr	Jump unconditional	2	2
JMPP @A	Jump indirect	1	2
DJNZ R, addr	Decrement register and skip	2	2
JC addr	Jump on carry = 1	2	2
JNC addr	Jump on carry = 0	2	2
JZ addr	Jump on Z zero	2	2
JNZ addr	Jump on A not zero	2	2
JT0 addr	Jump on T0 = 1	2	2
JNT0 addr	Jump on T0 = 0	2	2
JT1 addr	Jump on T1 = 1	2	2
JNT1 addr	Jump on T1 = 0	2	2
JF0 addr	Jump on F0 = 1	2	2
JF1 addr	Jump on F1 = 1	2	2
JTF addr	Jump on timer flag	2	2
JNI addr	Jump on INT = 0	2	2
JBb addr	Jump on accumulator bit	2	2

Table 2. Instruction Set by Mnemonic (Cont.)

Subroutine Mnemonic	Description	Bytes	Cycles
CALL addr	Jump to subroutine	2	2
RET	Return	1	2
RETR	Return and restore status	1	2

Flags Mnemonic	Description	Bytes	Cycles
CLR C	Clear carry	1	1
CPL C	Complement carry	1	1
CLR F0	Clear flag 0	1	1
CPL F0	Complement flag 0	1	1
CLR F1	1	1	
CPL F1	Complement flag 1	1	1

Data Moves Mnemonic	Description	Bytes	Cycles
MOV A, R	Move register to A	1	1
MOV A, @R	Move data memory to A	1	1
MOV A, # data	Move immediate to A	2	2
MOV R, A	Move A to register	1	1
MOV @R, A	Move A to data memory	1	1
MOV R # data	Move immediate to register	2	2
MOV @R, # data	Move immediate to data memory	2	2
MOV A, PSW	Move PSW to A	1	1
MOV PSW, A	Move A to PSW	1	1
XCH A, R	Exchange A and register	1	1
XCH A, @R	Exchange A and data memory	1	1
XCHD A, @R	Exchange nibble of A and register	1	1
MOVX A, @R	Move external data memory to A	1	2
MOVX @R, A	Move A to external data memory	1	2
MOVP A, @A	Move to A from current page	1	2
MOVP3 A, @A	Move to A from page 3	1	2

Timer/Counter Mnemonic	Description	Bytes	Cycles
MOV A, T	Read timer/counter	1	1
MOV T, A	Load timer/counter	1	1
STRT T	Start timer	1	1
STRT CNT	Start counter	1	1
STOP TCNT	Stop timer/counter	1	1
EN TCNTI	Enable timer/counter interrupt	1	1
DIS TCNTI	Disable timer/counter interrupt	1	1

Control Mnemonic	Description	Bytes	Cycles
EN I	Enable external interrupt	1	1
DIS I	Disable external interrupt	1	1
SEL RB0	Select register bank 0	1	1
SEL RB1	Select register bank 1	1	1
SEL MB0	Select memory bank 0	1	1
SEL MB1	Select memory bank 1	1	1
ENTO CLK	Enable clock output on T0	1	1

Mnemonic	Description	Bytes	Cycles
NOP	No operation	1	1
IDL	Low power Mode, OSC. on	1	1
STBY	Low power Mode, OSC. off	1	1

Note: All typical values have been guaranteed by characterization and are not tested.

LOW POWER MODES

The Intersil IM80C48 family incorporates IDLE and STandBY instructions as well as the hardware STOP mode. The IDLE instruction, opcode 01H, operates as shown in Figure 1. Execution of opcode 01H disables the internal clock and timing circuits while leaving the oscillator running. Power consumption drops to less than 1mW. Either a $\overline{\text{RESET}}$ or external $\overline{\text{INT}}$errupt will terminate the IDLE mode. A $\overline{\text{RESET}}$ will start execution from address 00H. An external $\overline{\text{INT}}$errupt will start execution from 03H if $\overline{\text{INT}}$errupt is enabled, or start execution from the next sequential instruction following the IDLE instruction if the $\overline{\text{INT}}$errupt is disabled.

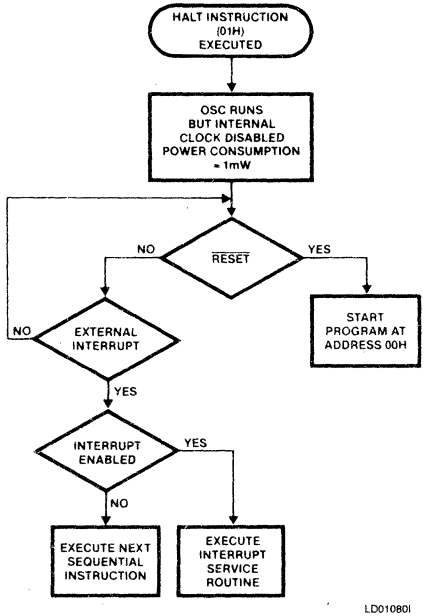


Figure 9: IDLe Mode

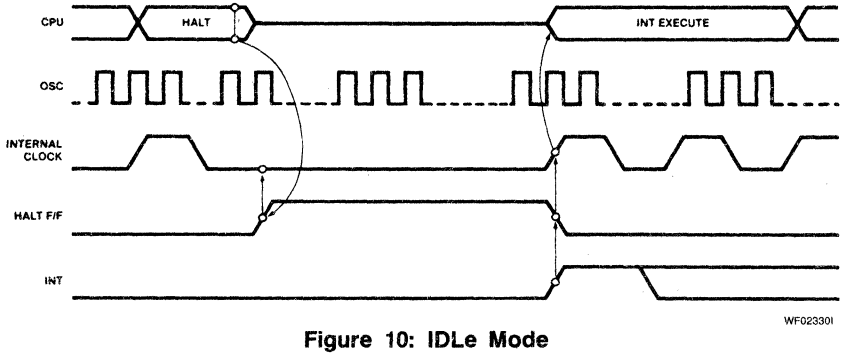


Figure 10: IDLe Mode

Note: All typical values have been guaranteed by characterization and are not tested.

IM80C48/49/35/39

Figure 11 illustrates the STOP mode. To enter the STOP mode, first take $\overline{RESET}$ low, then pull V_{DD}/ $\overline{STOP}$ low. The STOP mode, like the STandBY mode, shuts down the oscillator and causes the device to draws less than 1μA of current. To exit the STOP mode, take V_{DD}/ $\overline{STOP}$ high, wait for the oscillator to stabilize, then pull $\overline{RESET}$ high. Execution starts at address 0000H.

Since the power consumption of the IM80C48 is directly proportional to the clock frequency, significant power savings can be achieved by selecting the lowest clock frequency that provides sufficient processing power for the specific application. For example, while operating with a 32.768kHz clock, the IM80C48 will typically draw less than 2μA of current.

Figure 13 shows the operation of the STandBY instruction, opcode 63H. This instruction is similar to IDLE except that the oscillator is also turned off, reducing current drain to less than 1μA. A $\overline{RESET}$ or $\overline{INT}$errupt will restart the oscillator and execution will resume after the oscillator start-up time, plus a delay of 2-3 instruction cycles that allows the oscillator to stabilize. The start-up time of the oscillator, which depends on the operating voltage and the crystal parameters, is normally 5-50msec. The address at which execution resumes is the same as for the IDLe instruction.

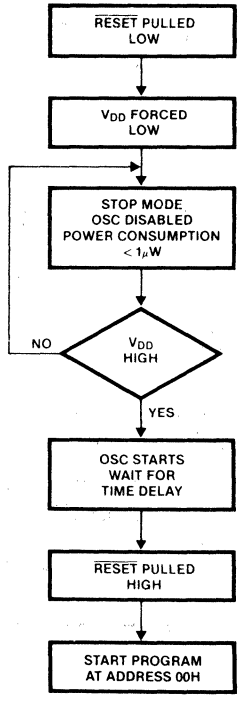


Figure 11: STOP Mode

Note: All typical values have been guaranteed by characterization and are not tested.

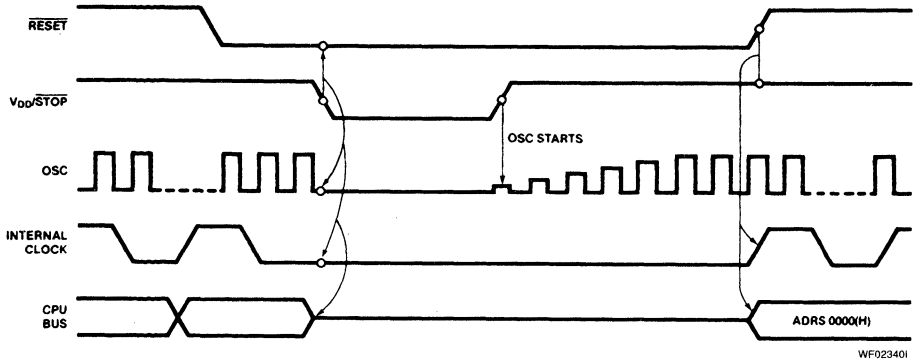


Figure 12: STOP Mode

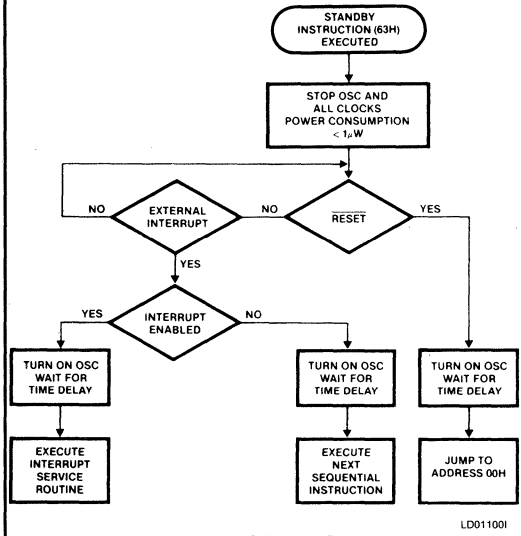


Figure 13: STANDBY Mode

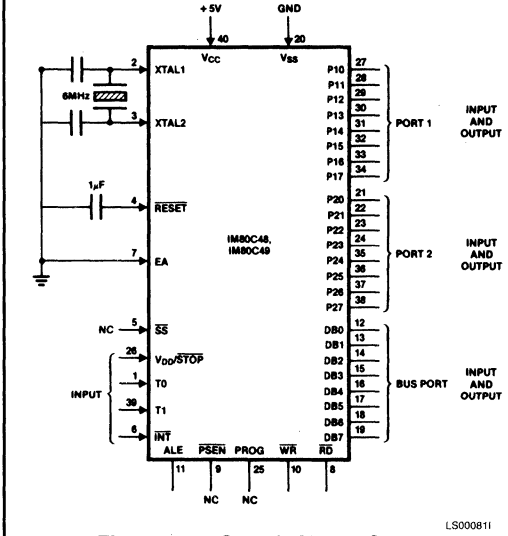
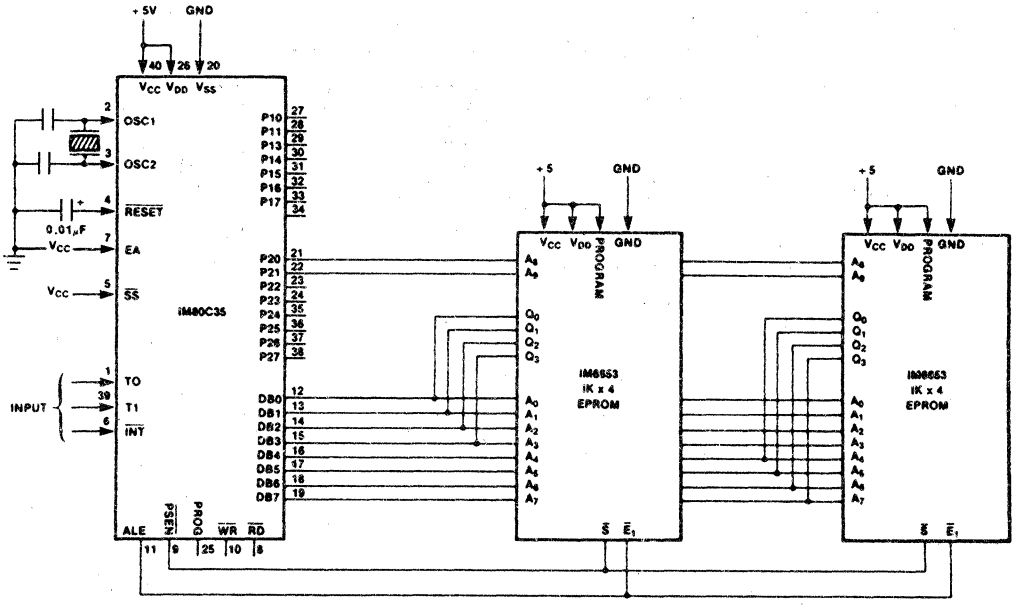


Figure 14: Stand Alone System

9

Note: All typical values have been guaranteed by characterization and are not tested.

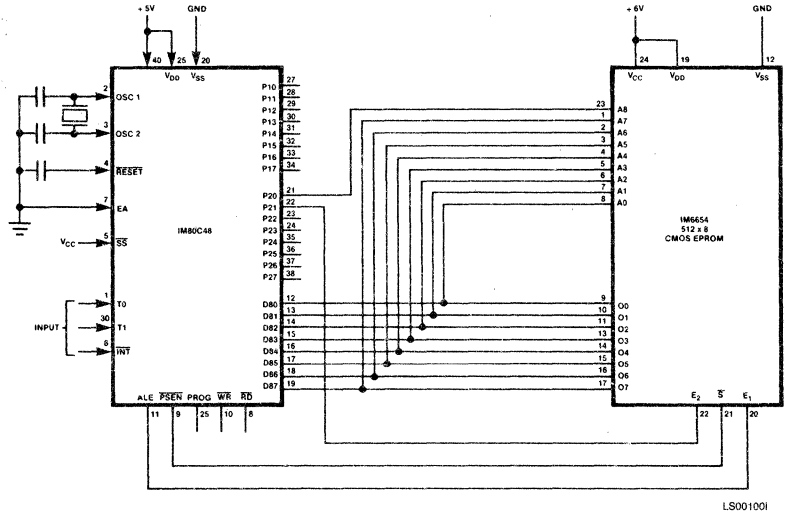


LS000911

Figure 15: IM6653 CMOS EPROMSs As External Program Memory with The IM80C35

*Capacitance values dependent on package type

USING IM6654 CMOS EPROM TO EXTEND PROGRAM MEMORY



LS001001

Figure 16: Using IM6654 CMOS EPROM to Extend Program Memory

Note: All typical values have been guaranteed by characterization and are not tested.

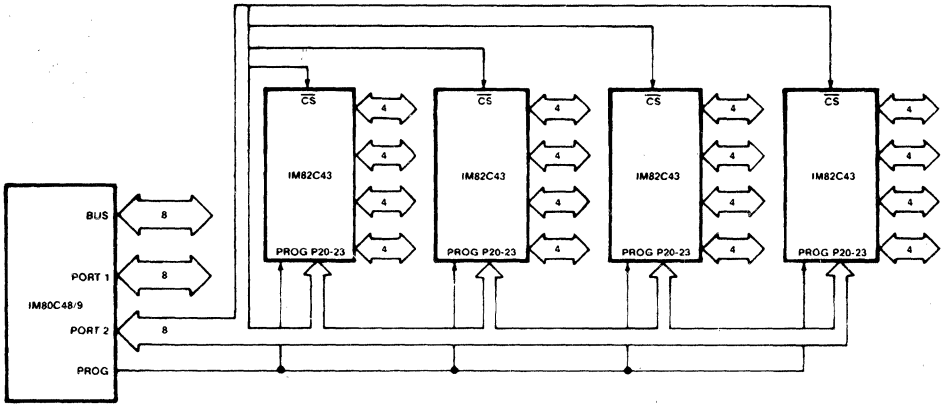


Figure 17: Using IM82C43 I/O Expanders, This Five Chip System Has 80 I/O Lines

*Capacitance values dependent on package type

Note: All typical values have been guaranteed by characterization and are not tested.

IM80C48/49/35/39

Table 3: Instruction Summary By Hexadecimal Opcode

HEX	MNEMONIC	HEX	MNEMONIC	HEX	MNEMONIC	HEX	MNEMONIC
00	NOP	30	XCHD A,@R0	70	ADDC A,@R0	A0	MOV @R0,A
01	IDL	31	XCHD A,@R1	71	ADDC A,@R1	A1	MOV @R1,A
02	OUTL BUS,A	32	JB1	72	JB3	A2	undefined
03	ADD A,#data	33	undefined	73	undefined	A3	MOVP A,@A
04	JMP (page 0)	34	CALL (page 1)	74	CALL (page 3)	A4	JMP (page 5)
05	EN I	35	DIS TCNTI	75	ENT0 CLK	A5	CLR F1
06	undefined	36	JT0	76	JF1	A6	undefined
07	DEC A	37	CPL A	77	RR A	A7	CPL C
08	undefined	38	undefined	78	ADDC A,R0	A8	MOV R0,A
09	IN A,P1	39	OUTL P1,A	79	ADDC A,R1	A9	MOV R1,A
0A	IN A,P2	3A	OUTL P2,A	7A	ADDC A,R2	AA	MOV R2,A
0B	undefined	3B	undefined	7B	ADDC A,R3	AB	MOV R3,A
0C	MOVD A,P4	3C	MOVD P4,A	7C	ADDC A,R4	AC	MOV R4,A
0D	MOVD A,P5	3D	MOVD P5,A	7D	ADDC A,R5	AD	MOV R5,A
0E	MOVD A,P6	3E	MOVD P6,A	7E	ADDC A,R6	AE	MOV R6,A
0F	MOVD A,P7	3F	MOVD P7,A	7F	ADDC A,R7	AF	MOV R7,A
10	INC @R0	40	ORL A,@R0	80	MOVX A,@R0	B0	MOV @R0,#data
11	INC @R1	41	ORL A,@R1	81	MOVX A,@R1	B1	MOV @R1,#data
12	JB0	42	MOV A,T	82	undefined	B2	JB5
13	ADDC A,#data	43	ORL A,#data	83	RET	B3	JMPP @A
14	CALL (page 0)	44	JMP (page 2)	84	JMP (page 4)	B4	CPL F1
15	DIS I	45	STRT CNT	85	CLR F0	B5	CPL F1
16	JFT	46	JNT1	86	JNI	B6	JF0
17	INC A	47	SWAP A	87	undefined	B7	undefined
18	INC R0	48	ORL A,R0	88	ORL BUS,#data	B8	MOV R0,#data
19	INC R1	49	ORL A,R1	89	ORL P1,#data	B9	MOV R1,#data
1A	INC R2	4A	ORL A,R2	8A	ORL P2,#data	BA	MOV R2,#data
1B	INC R3	4B	ORL A,R3	8B	undefined	BB	MOV R3,#data
1C	INC R4	4C	ORL A,R4	8C	ORLD P4,A	BC	MOV R4,#data
1D	INC R5	4D	ORL A,R5	8D	ORLD P5,A	BD	MOV R5,#data
1E	INC R6	4E	ORL A,R6	8E	ORLD P6,A	BE	MOV R6,#data
1F	INC R7	4F	ORL A,R7	8F	ORLD P7,A	BF	MOV R7,#data
20	XCH A,@R0	50	ANL A,@R0	C0	undefined	E0	undefined
21	XCH A,@R1	51	ANL A,@R1	C1	undefined	E1	undefined
22	undefined	52	JB2	C2	undefined	E2	undefined
23	MOV A,#data	53	ANL A,#data	C3	undefined	E3	MOVP3 A,@A
24	JMP (page 1)	54	CALL (page 2)	C4	JMP (page 6)	E4	JMP (page 7)
25	EN TCNTI	55	STRT T	C5	SEL RB0	E5	SEL MB0
26	JNT0	56	JT 1	C6	JZ	E6	JNC
27	CLR A	57	DA A	C7	MOV A,PSW	E7	RL A
28	XCH A,R0	58	ANL A,R0	C8	DEC R0	E8	DJNZ R0,addr
29	XCH A,R1	59	ANL A,R1	C9	DEC R1	E9	DJNZ R1,addr
2A	XCH A,R2	5A	ANL A,R2	CA	DEC R2	EA	DJNZ R2,addr
2B	XCH A,R3	5B	ANL A,R3	CB	DEC R3	EB	DJNZ R3,addr
2C	XCH A,R4	5C	ANL A,R4	CC	DEC R4	EC	DJNZ R4,addr
2D	XCH A,R5	5D	ANL A,R5	CD	DEC R5	ED	DJNZ R5,addr
2E	XCH A,R6	5E	ANL A,R6	CE	DEC R6	EE	DJNZ R6,addr
2F	XCH A,R7	5F	ANL A,R7	CF	DEC R7	EF	DJNZ R7,addr
60	ADD A,@R0	90	MOVX @R0,A	D0	XRL A,@R0	F0	MOV A,@R0
61	ADD A,@R1	91	MOVX @R1,A	D1	XRL A,@R1	F1	MOV A,@R1
62	MOV T,A	92	JB4	D2	JB6	F2	JB7
63	STBY	93	RETR	D3	XRL A,#data	F3	undefined
64	JMP (page 3)	94	CALL (page 4)	D4	CALL (page 6)	F4	CALL (page 7)
65	STOP TCNT	95	CPL F0	D5	SEL RB1	F5	SEL MB1
66	undefined	96	JNZ	D6	undefined	F6	JC
67	RRC A	97	CLR C	D7	MOV PSW,A	F7	RLC A
68	ADD A,R0	98	ANL BUS,#data	D8	XRL A,R0	F8	MOV A,R0
69	ADD A,R1	99	ANL P1,#data	D9	XRL A,R1	F9	MOV A,R1
6A	ADD A,R2	9A	ANL P2,#data	DA	XRL A,R2	FA	MOV A,R2
6B	ADD A,R3	9B	undefined	DB	XRL A,R3	FB	MOV A,R3
6C	ADD A,R4	9C	ANLD P4,A	DC	XRL A,R4	FC	MOV A,R4
6D	ADD A,R5	9D	ANLD P5,A	DD	XRL A,R5	FD	MOV A,R5
6E	ADD A,R6	9E	ANLD P6,A	DE	XRL A,R6	FE	MOV A,R6
6F	ADD A,R7	9F	ANLD P7,A	DF	XRL A,P7	FF	MOV A,R7

Note: All typical values have been guaranteed by characterization and are not tested.

IM82C43
CMOS I/O Expander

DESCRIPTION

The Intersil IM82C43 is a CMOS input/output expander equivalent to the NMOS 8243. It is designed to provide I/O expansion for the CMOS IM80C48 and NMOS 8048 families of single-chip microcomputers.

The 24-pin IM82C43 provides four 4-bit bidirectional I/O ports: 8048/41 instructions control bidirectional transfers between theIM82C43 and the 8048 family microcomputers, and can execute logical AND/OR operations directly on the data contained in the IM82C43 ports.

FEATURES

- **8048/41 Compatible I/O Expander**
- **CMOS Pin-For-Pin Replacement for Standard NMOS 8243**
- **Low Power Dissipation — Maximum 25mW Active**
- **Four 4-Bit I/O Ports in 24-Pin DIP**
- **Logical AND/OR Directly to Ports**
- **High Output Drive**
- **Single +5V Supply**

ORDERING INFORMATION

PART NO.	TEMP. RANGE	PACKAGE
IM82C43CJG	0°C to +70°C	24 PIN CERDIP
IM82C43CPG	0°C to +70°C	24 PIN PLASTIC
IM82C43IJG	−40°C to +85°C	24 PIN CERDIP
IM82C43IPG	−40°C to +85°C	24 PIN PLASTIC

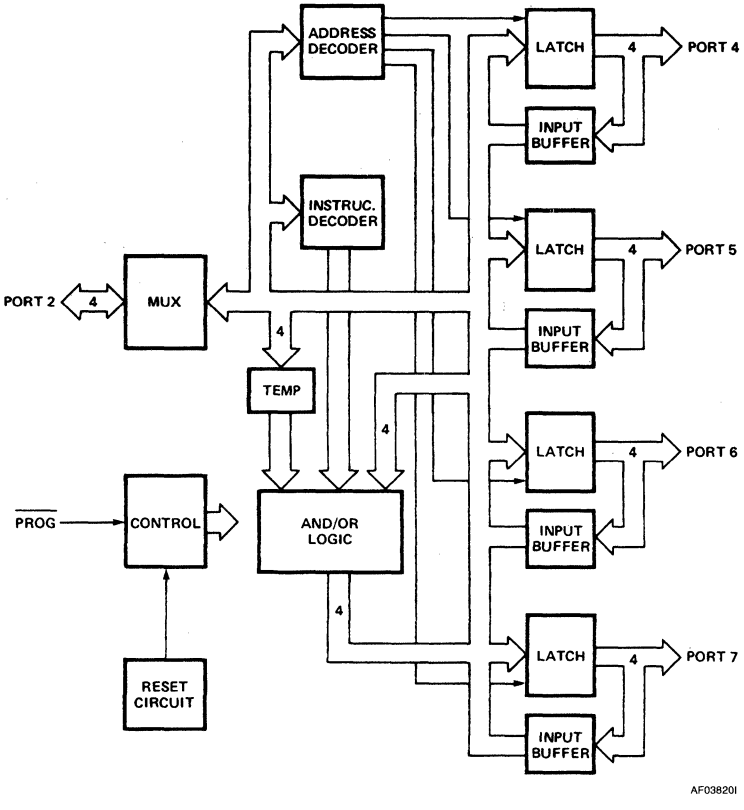


Figure 1: Functional Diagram

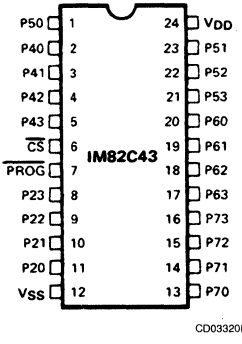


Figure 2: Pin Configuration (Outline dwgs JG, PG)

002

Note: All typical values have been guaranteed by characterization and are not tested.

IM82C43

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD} - V_{SS}$) ..... +8V
Voltage on Any Pin .....(V_{SS} −0.5V) to (V_{DD} + 0.5V)
Power Dissipation 1W
Operating Temperature (C) ..... 0°C to +70°C
(I) .....−40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) .....300°C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

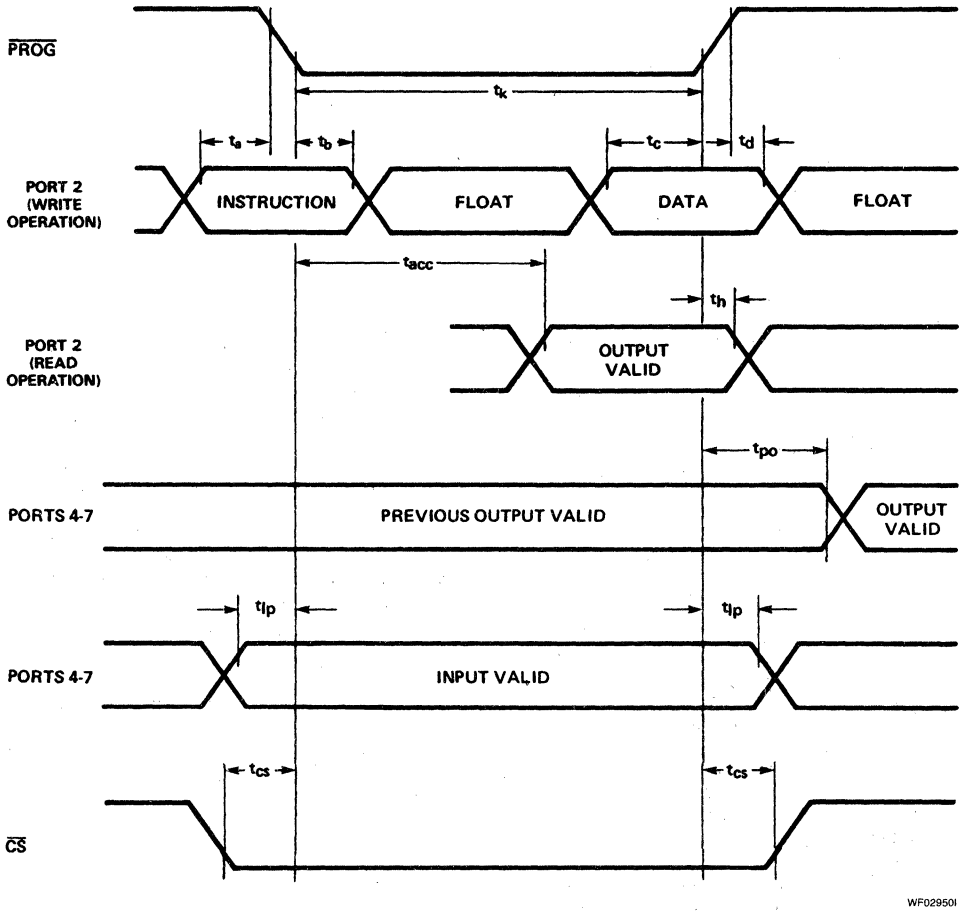
DC ELECTRICAL CHARACTERISTICS (T_A = Operating Temperature Range, V_{DD}=5V±10%, V_{SS} = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input Low Voltage		−0.5		0.8	V
V_{IH}	Input High Voltage	V_{DD} = 4.5	2.0			
		V_{DD} = 5.5	2.4			
V_{OL}	Output Low Voltage Ports 4–7	I_{OL} = 10mA			0.4	
		I_{OL} = 20mA			0.8	
	Output Low Voltage Port 2	I_{OL} = 1.6mA			0.4	
V_{OH1}	Output High Voltage Ports 4–7	I_{OH} = 3.2mA	2.8			
V_{OH2}	Output Voltage Port 2	I_{OH} = 1.6mA	2.8			
I_{ILK}	Input Leakage Ports 4–7, Port 2, $\overline{CS}$, $\overline{PROG}$	V_{IN} = V_{DD} to V_{SS}	−10		10	µA
I_{DD}	Supply Current	WRITE mode, All outputs open, t_k = 700ns		1.6	5.0	mA
I_{STBY}	Standby Current	V_{IN} = 0 or V_{DD}, $\overline{CS}$ = V_{DD}, All outputs open			100	µA
ΣI_{OL}	Sum of all I_{CL} from 16 Outputs	5mA each pin average			80	mA

AC ELECTRICAL CHARACTERISTICS (T_A = Operating Temperature Range, V_{DD} = 5V±10%, V_{SS} = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_a	Code Valid Before $\overline{PROG}$	80pF Load	100		ns
t_b	Code Valid After $\overline{PROG}$	20pF Load	60		
t_c	Data Valid Before $\overline{PROG}$	80pF Load	140		
t_d	Data Valid After $\overline{PROG}$	20pF Load	20		
t_h	Floating After $\overline{PROG}$	20pF Load	0	150	
t_k	$\overline{PROG}$ Negative Pulse Width		700		
t_{cs}	$\overline{CS}$ Valid Before/After $\overline{PROG}$		50		
t_{po}	Ports 4–7 Valid After $\overline{PROG}$	100pF Load		700	
t_{ip}	Ports 4–7 Valid Before/After $\overline{PROG}$		0		
t_{acc}	Port 2 Valid After $\overline{PROG}$	80pF Load		650	

Note: All typical values have been guaranteed by characterization and are not tested.



AC TEST CONDITIONS

V_{IH} = 2.8V

INPUT RISE AND FALL TIMES: 5ns (10% TO 90%)

INPUT AND OUTPUT TIMING VOLTAGE REFERENCE LEVELS: 0.8V AND 2.0V

Figure 3: Timing Diagram

9

Note: All typical values have been guaranteed by characterization and are not tested.

IM82C43

PIN DESCRIPTIONS

Designator	Pin Number	Function
$\overline{PROG}$	7	**Strobe input.** The falling edge of $\overline{PROG}$ implies valid address and control information on P20–P23, while the rising edge implies valid data on P20–P23.
$\overline{CS}$	6	**Chip select input.** When HIGH, it disables $\overline{PROG}$, thus inhibiting change in output or internal status.
P20–P23	8–11	**Four bit directional port** carrying address and control bits on the falling edge of $\overline{PROG}$ and I/O data on the rising edge of $\overline{PROG}$.
P40–43 P50–P53 P60–P63 P70–P73	2–5 1,21–23 17–20 13–16	**Four bit bidirectional I/O ports.** May be configured for input, tri-state output (READ mode) or latched output. Data on pins P20–23 may be directly written. ANDed, or ORed with previous data.
V_{SS}	12	**Circuit ground potential**
V_{DD}	24	**Positive supply.**

DETAILED DESCRIPTION

The IM82C43 has four 4-bit I/O ports, which are addressed as Ports 4 thru 7 by the processor. The following operations may be performed on these ports:

- Transfer accumulator to port (write)
- Transfer port to accumulator (read)
- AND accumulator to port
- OR accumulator to port

All communication between the microcomputer and the IM82C43 occurs over Port 2 (P20–P23) with timing provided by an output pulse on the $\overline{PROG}$ pin of the processor. Each data transfer consists of two 4-bit nibbles:

- The first contains the port address and command to the IM82C43. This is latched from Port 2 during the high-to-low transition of $\overline{PROG}$ and is encoded as shown in the table on page 3.
- The second contains the four bits of data associated with the instruction. The low-to-high transition of $\overline{PROG}$ indicates the presence of data.

Port Address And Command Format

P23	P22	INSTRUCTION CODE	P21	P20	ADDRESS CODE
0	0	Read	0	0	Port 4
0	1	Write	0	1	Port 5
1	0	ORLD	1	0	Port 6
1	1	ANLD	1	1	Port 7

Write Modes

The device has three modes. MOVD P,A directly writes new data into the selected port with old data being lost; ORLD P,A ORs the new data with the old data and writes it to the port; and ANLD P,A ANDs new data with old data and writes it to the selected port.

After the designated operation is performed, the data is latched and directed to the port. The old data remains latched until the new data is written by the rising edge of $\overline{PROG}$.

Read Mode

The device has one read mode. The command and port address are latched from port 2 on the high-to-low transition of the $\overline{PROG}$ pin. As soon as the read operation and port address are decoded, the designated port output buffers are disabled and the input buffers enabled. The read operation is terminated by the low-to-high transition of the $\overline{PROG}$ pin. The port selected is switched to the high impedance state while port 2 is returned to the input mode.

Normally a port will be in an output mode (write) or input mode (read). The first read of a port, following a mode change from write to read should be ignored; all following reads are valid. This is to allow the external driver on the port to settle after the first read instruction removes the low impedance drive from the IM82C43 output. A read of any port will leave that port in a high impedance state.

I/O Expansion

The use of a single IM82C43 with an 8048 or 8021 is shown in Figure 4. If more ports are required, more IM82C43s can be added as shown in Figure 5. Here, the upper nibble of port 2 is used to select one of the IM82C43s. Two lines could have been decoded but that would require additional hardware. Assuming that the left-most IM82C43 chip select is connected to P24, the instructions to select and de-select would be:

```
MOV A, #0EFH      P24 = 0
OUTL P2, A        Enable IM82C43
.
.
.
MOV A, #0FFH      Disable All
OUTL P2, A        Send it
```

Power On Initialization

Initial application of power to the device forces ports 4, 5, 6, and 7 to the high impedance state. Port 2 will be in an input state if $\overline{PROG}$ or $\overline{CS}$ are high when power is applied. The first high-to-low transition of $\overline{PROG}$ causes the device to exit the power-on mode. The power-on sequence is initiated if V_{DD} drops below one volt.

Note: All typical values have been guaranteed by characterization and are not tested.

TYPICAL APPLICATIONS

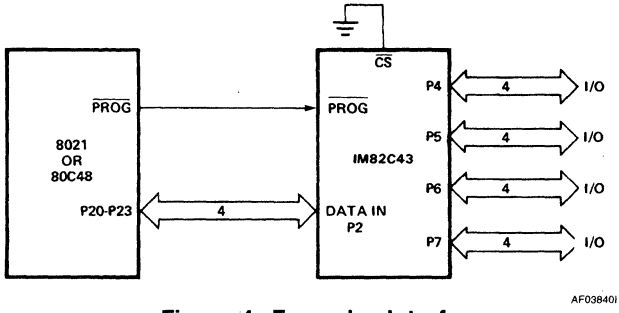


Figure 4: Expander Interface

Note: The IM82C43 does not have the same quasi-bidirectional port structure as P1/P2 of the 8048. When a "1" is written to P4–7 of the IM82C43 it is a "hard 1" (low impedance to +5V) which cannot be pulled low by an external device. All 4 bits of any port can be switched from output mode to input mode by executing a dummy read which leaves the port in a high impedance (no pullup or pulldown) state.

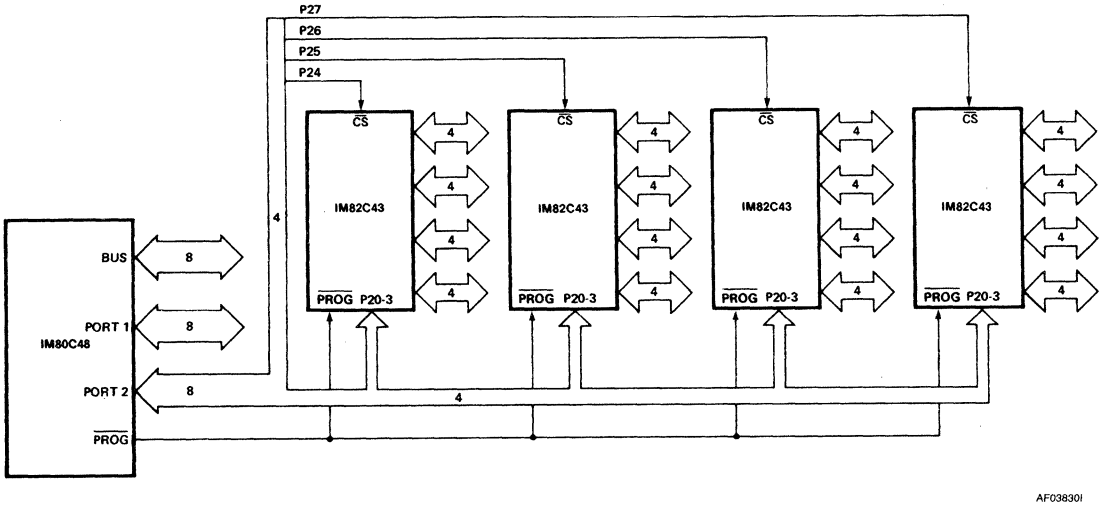


Figure 5: Using Multiple IM82C43s

Note: All typical values have been guaranteed by characterization and are not tested.

Section 10 — High Reliability/ Military Products and Ordering Information

DIE & WAFER ORDERING INFORMATION

INTERSIL

FET, MOSFET, AND DUAL TRANSISTOR CHIPS

INTRODUCTION

Intersil recognizes the increasing need for transistors and FETs in die form. To fulfill this need, Intersil offers a full line of JFETs, MOSFETs, and dual transistors in die form.

Die sales do, however, present some unique problems. In many cases the chips cannot be guaranteed to the same electrical specifications as the packaged part. This is due to the fact that leakage, noise, AC parameters and temperature testing cannot be tested to the same degree of accuracy for dice as it can for packaged devices. This is due to equipment limitations and handling problems.

PURCHASE OPTIONS

Intersil offers dice which are delivered in a number of forms:

- Chips which have been electrically probed, inked, visually inspected and diced.
- Wafers which have been electrically probed, inked, scribed, and mounted on rings with adhesive tape.
- Wafers which have been electrically probed, inked, and visually inspected only.

GENERAL PHYSICAL INFORMATION

- Consult individual product information sheets for dimensions. Except for the aluminum bonding pads, the chips are completely covered with vapox (silicon dioxide). This minimizes damage to the chip caused by handling problems.
- Dice are 100% tested to D.C, +25°C electrical specifications, then visually inspected. When wafers are ordered, dice which fail the electrical test are inked out.
- Generally the minimum size of the die-attaching pad metallization should be at least 5 mils larger (on every edge) than the chip dimensions. For example, a 15 mil chip should be attached on at least a 25 mil pad.

Small Signal Devices

- Chips are available with exact length X width dimensions plus tolerance (see individual data sheets). Chip height ranges from .003″ to .006″.
- To facilitate die attaching, chips are gold backed. Approximate thickness is 1000 angstroms. In general, dice should be attached to gold, platinum, or palladium metallization. Thin-film gold, moly-gold and most of the thick-film metallization materials are compatible.
- All chips have aluminum metallization and aluminum bonding pads. Typical aluminum thickness is 12,000 angstroms.

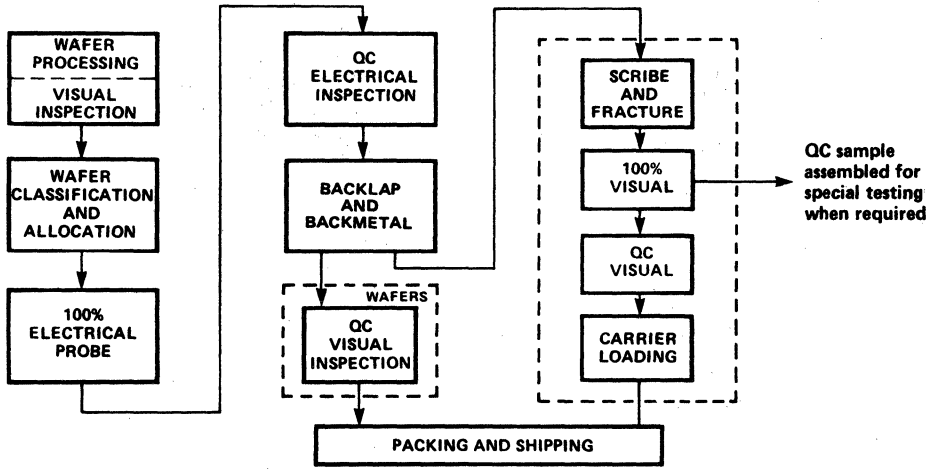


Figure 1: Chip and Wafer Processing Flow Chart

10

RECOMMENDED DICE ASSEMBLY PROCEDURE

CLEANING

Dice supplied in die form do not require cleaning prior to assembly. Dice supplied in wafer form should be cleaned after scribing and breaking. Freon TF in a vapor degreaser is the preferred cleaning method. However, an alternative is to boil the die in TCE for five minutes with a rinse in isopropyl alcohol for 1-2 minutes.

DIE ATTACH:

The die attach operation should be done under a gaseous nitrogen ambient atmosphere to prevent oxidation. A preform should be used if the mounting surface has less than 50 microinches of gold and the die should be handled on the edges with tweezers. Die attach temperature should be between 385°C and 400°C with eutectic visible on three sides of the die after attachment.

BONDING:

Thermocompression gold ball or aluminum ultrasonic bonding may be used. The gold ball should be about 3 times the diameter of the gold wire. The ball should cover the bonding pad, but not excessively, or it may short out surrounding metallization. 1-mil aluminum wire may be used on most dice, but should not be used if the assembled unit will be plastic encapsulated.

HANDLING OF DICE:

All dice shown in this catalog are passivated devices and Intersil warrants that they will meet or exceed published specifications when handled with the following precautions:

- Dice should be stored in a dry inert-gas atmosphere.
- Dice should be assembled using normal semiconductor techniques.
- Dice should be attached in a gaseous nitrogen spray at a temperature less than 430°C.

ELECTRICAL TEST LIMITATIONS

DUAL BIPOLAR TRANSISTORS

LV_{CEO}	100V max. @ ≤1 mA
BV_{CBO}	100V max. @ ≥1 μA
BV_{EBO}	100V max. @ ≤10 mA
h_{FE}	≤1000 @ ≥10 μA
$V_{CE(sat)}$	≥10 mV @ ≤10 mA
I_{CBO}	≥100 pA @ ≤100V
V_{BE1}–V_{BE2}	≥1 mV @ ≥10 μA
I_{B1}–I_{B2}	≥2 nA

FETS

Breakdown voltage	100V max. @ 1 μA
Pinch-off voltage	0–20V @ ≥ 1nA
$V_{GS(th)}$	0–5 @ ≥ 10 μA
$r_{DS(on)}$	5 Ωmin.@ V_{GS} = 0 (V_{GS} = 30 MOSFETs)
I_{DSS}	100mA max.
g_{fs}	20,000 μMHOS max.
$I_{D(off)}$, $I_{S(off)}$, I_{GSS}	100pA min.
V_{GS1}–V_{GS2}	5mV min.

Electrical testing is guaranteed to a 10% LTPD. AC parameters such as capitance and switching time cannot be tested in wafer or dice form.

STANDARD DIE CARRIER PACKAGE

- Easy to handle, store and inventory.
- 100% electrically probed dice with electrical rejects removed.
- 100% visually sorted with mechanical and visual rejects removed.
- Easy visual inspection — dice in carriers, geometry side up.
- Individual compartment for each die.
- Carriers usable in customer production area.
- Carrier may be storage container for unused dice.
- Carriers hold 25, 100, or 400 dice, depending on die size and quantity ordered.
- Part numbers shown in this catalog are for carrier packaging.

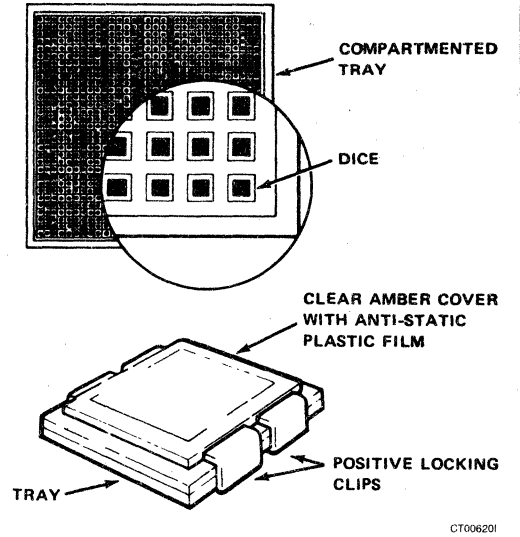
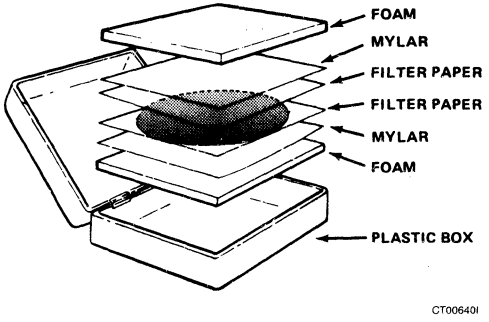


Figure 2

DIE & WAFER ORDERING INFORMATION

OPTIONAL WAFER PACKAGE

- 100% electrically probed — rejects inked.
- 10% extra good dice included (no charge) to cover possible breakage and/or visual rejects.
- Preferred for production quantities.
- Lowest cost.
- Wafer is supplied unscribed.
- For wafer package — replace "D" in catalog number with "W", e.g.: 2N4416/D (2N4416 dice in carrier) becomes 2N4416/W (2N4416 dice in wafer).



NOTE: Intersil reserves the right to improve device geometries and manufacturing processes as required. These improvements may result in slight geometry changes. However, they will not affect the electrical limits, basic pad layouts or maximum die sizes in this catalog.

Figure 3

ELECTRICAL TEST CAPABILITY

As an example of how to use the capability chart to see what Intersil actually guarantees and tests for, on a 100% basis, compare the 2N4391 in a TO-18 package to the 2N4391 delivered as a chip.

ELECTRICAL TEST SPEC.	2N4391 IN A TO-18	2N4391 CHIP
I_{GSS} @ 25C	100pA max.	100pA max.
BV_{GSS}	40V min.	40V min.
$I_{D(off)}$ @ 25C	100pA max.	100pA max.
V_{GS}(forward)	See note 1	1V max.
$V_{GS(off)}$ or V_P	4V to 10V	4V to 10V
I_{DSS}	50 to 150mA	50 to 150mA
$V_{DS(on)}$	0.4V max.	0.4 max.
$r_{DS(on)}$	30Ω max.	30Ω max.
C_{iss}	14pF max.	Guaranteed by Design
C_{rss}	3.5pF max.	Guaranteed by Design
t_d	15ns max.	Guaranteed by Design
t_r	5ns max.	Guaranteed by Design
t_{off}	20ns max.	Guaranteed by Design
t_f	15ns max.	Guaranteed by Design

NOTE 1. This parameter is very dependent upon quality of metalization to which chip is attached.

SUMMARY

Of the 14 items specified for the package part, only 8 can be tested and guaranteed in die form. It is to be noted that those specifications which cannot be tested in die form can be sample tested in package form as an indicator of lot performance. Many of the tests, however, such as capacitance tests, are design parameters.

The above electrical testing is guaranteed to a 10% LTPD. However, there are occasions where customer requirements cannot be satisfied by wafer sort testing alone. While the previously described tests will be done on a 100% basis, Intersil recognizes the need for additional testing to obtain confidence that a particular customer's needs can be met with a reasonably high yield. Toward this end Intersil has instituted a dice sampling plan which is two-fold. First, random samples of the dice are packaged and tested to assure adherence to the electrical specification. When required, wafers are identified and wafer identity is tied to the samples. This tests both the electrical character of the die and its ability to perform electrically after going through the high temperature dice attachment stage. Second, more severe testing can be performed on the packaged devices per individual customer needs. When testing is required other than that called out in the data sheet, Intersil issues an ITS number to describe the part. Examples of tighter testing which can be performed on packaged samples is shown as follows:

FET & DUAL FET PAIRS

1. Leakages to 1 pA (I_{GSS})
2. $R_{DS(on)}$ to as low as 3 ohms
3. $I_{D(off)}$ to 10 pA
4. I_{DSS} to 1 amp (pulsed)
5. g_{fs} to 20,000 μmho
6. g_{os} to 1 μmho
7. e_n noise to 5 nV/$\sqrt{Hz}$ at frequencies of 10Hz to 100Hz
8. CMRR to 100dB
9. $\Delta(V_{GS1}-V_{GS2})/\Delta T$ down to 10μV/°C to an LTPD of 20%
10. g_m match to 3%
11. I_{DSS} match to 3%

TRANSISTOR PAIRS

1. Leakages to as low as 1pA
2. Beta with collector current up to 50mA and as low as 100nA
3. f_T up to 500MHz with collector currents in the range of 10μA to 10mA
4. Noise measurements as low as 5nV/$\sqrt{Hz}$ from 10Hz to 100kHz
5. $\Delta(V_{BE1}-V_{BE2})/\Delta T$ to 10μV/°C to an LTPD of 20%

VISUAL INSPECTION

Individual chips are 100% inspected to MIL-STD-750, Method 2072 or, as an option, MIL-STD-883, Level B. Inspection is done to an LTPD of 20%. As an option, Intersil offers S.E.M. capability on all wafers.

DIE & WAFER ORDERING INFORMATION

INTERSIL

CMOS INTEGRATED CIRCUIT CHIPS

INTRODUCTION

In addition to discrete device chips, Intersil also offers a full line of metal gate CMOS integrated circuits in die form. Die sales, however, present some unique problems. In many cases, chips cannot be guaranteed to the same electrical specifications as can the packaged parts. This is because leakage, noise, AC parameters and temperature testing cannot be guaranteed to the same degree of accuracy for dice as for packaged devices.

GENERAL PHYSICAL INFORMATION

- Chips are available with precise length and width dimensions, ±2 mils in either dimension.
- Chip thickness is 9 to 20 mils, depending on device type.
- Bonding pad and interconnected material is aluminum, 10K to 15K A thick.
- Each die surface is protected by planar passivation and additional surface glassivation except for bonding pads and scribe lines. The surface passivation is removed from the bonding pad areas by an HF etchant; bonding pads may appear discolored at low magnification due to surface roughness of the aluminum caused by the etchant.
- Dice are 100% tested to DC electrical specifications, at 25°C then visually inspected according to MIL-STD-883, Method 2010.2, condition B, with modifications reflecting CMOS requirements.
- Bonding pad dimensions are 4.0 x 4.0 mils minimum.
- Storage temperature is −40°C to +150°C.
- Guaranteed AQL Levels:

Visual	2.0%
Functional electrical testing	1.0%
Parametric DC testing	4.0%

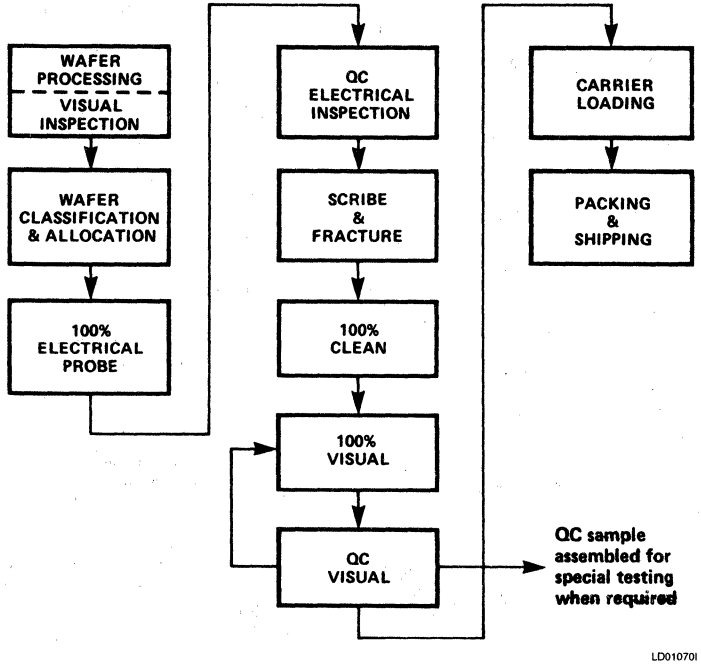


Figure 4: CMOS Integrated Circuit Chip Processing Flow Chart

RECOMMENDED DICE ASSEMBLY PROCEDURES

CLEANING

Dice supplied in die form do not require cleaning prior to assembly. However, if cleaning is desired, dice should be subjected to freon TF in a vapor degreaser and then vapor-dried.

RECOMMENDED HANDLING

Intersil recommends that dice be stored in the vacuum-sealed plastic bags which hold the dice carriers. Once removed from the sealed bags, the dice should be stored in a dry, inert-gas atmosphere.

Extreme care should be used when handling dice. Both electrical and visual damage can occur as the result of an unclean environment or harsh handling techniques.

DIE ATTACH

The die attach operation should be done under a gaseous nitrogen ambient atmosphere to prevent oxidization. If a eutectic die attach is used, it is recommended that a 98% gold/2% silicon preform be used at a die attach temperature between 385°C and 435°C. If an epoxy die attach is used, the epoxy cure temperature should not exceed 150°C. If hermetic packages are used, epoxy die attach should be carried out with caution so that there will be no "outgassing" of the epoxy.

BONDING

Thermocompression gold ball or aluminum ultrasonic bonding may be used. The wire should be 99.99% pure gold and the aluminum wire should be 99% aluminum/1% silicon. In either case, it is recommended that 1.0 mil wire be used for normal power circuits.

STANDARD DIE CARRIER PACKAGE

- Easy to handle, store and inventory.
- 100% electrically probed with electrical rejects removed.
- 100% visually sorted with mechanical and visual rejects removed.
- Easy visual inspection — dice are in carriers, geometry side up.
- Individual compartment for each die.
- Carriers usable in customer production area.
- Carrier may be used as storage contained for unused dice.
- Carriers hold 25, 100 or 400 dice, depending on die size and quantity ordered.
- Packing of integrated circuit dice in carriers is identical to illustration shown earlier for discrete device, except that IC chips are not available in vial packs or in wafer form.

CHANGES

Intersil reserves the right in improve device geometries and manufacturing processes without prior notice. Although these improvements may result in slight geometry changes, they will not affect dice electrical limits, pad layouts, or maximum die sizes.

USER RESPONSIBILITY

Written notification of any non-conformance by Intersil of Intersil's dice specifications must be made within 75 days of the shipment date of the die to the user. Intersil assumes no responsibility for the dice after 75 days or after further user processing such as, but not limited to, chip mounting or wire bonding.

100% INTEGRATED CIRCUIT PROCESSING

Intersil is committed to build and process integrated circuits for the Military/High-Rel market segments in conformance with MIL-STD-883 and MIL-M-38510. Any customer drawing which specifies testing as set forth in these documents will be automatically processed to the latest revisions of MIL-STD-883 and MIL-M-38510, unless specific requests are made to the contrary.

HI-REL PROCESS OFFERINGS

38510 PRODUCTS

Intersil holds QPL1 status on a number of JAN MIL-M-38510 products as listed herein. As required by JAN specifications, these products are fabricated, assembled, and 100% processed within the United States and are fully compliant with all the requirements, procedures, and methods as given in MIL-M-38510 Revision F and MIL-STD-883 Revision C.

883B PRODUCTS

The 883B flow diagram represents product processed in accordance with Method 5004 and Method 5005 of MIL-STD-883 Rev. C, Class B. Most products listed as /883B herein are available as compliant to paragraph 1.2 of MIL-STD-883B Rev. C while others are available only as non-compliant at this time (Allowances for sale of non-compliant /883B products are covered in notice 3 of MIL-STD-883 Rev. C). Check with Intersil Customer Service as to the compliant status of individual product offerings at any point in time.

HR PRODUCTS

The HR flow diagram, newly offered by Intersil, represents high reliability hermetic product utilizing many, but not necessarily all, of the test methods and requirements of MIL-STD-883 Rev. C, to be used in high reliability applications where some deviations from Rev. C may be justified and economic advantages realized. Such product may not be branded /883B but may be branded /HR or a special brand as required as purchase order.

BR PRODUCTS

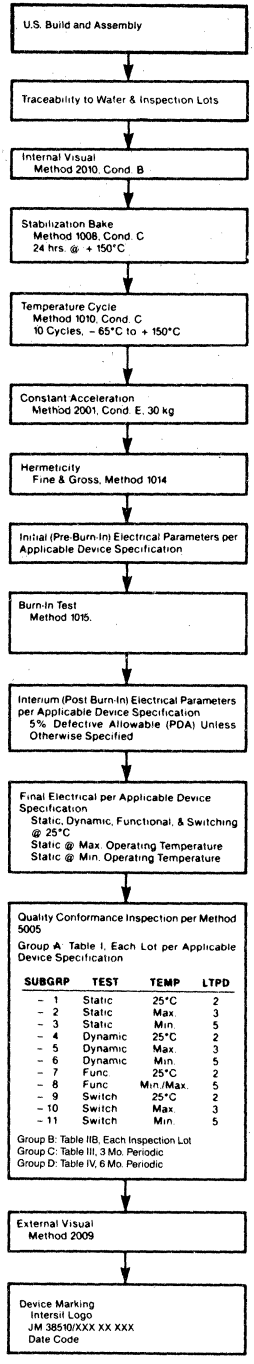
The BR flow diagram, newly offered by Intersil, represents hermetic or plastic encapsulated product intended for application in the computer, industrial, or hi-rel commercial marketplace. In addition to 100% burn-in, many other reliability processing steps are included to enhance quality levels on shipped parts and to improve long term reliability characteristics. Such product may be branded /BR or as required by purchase order.

Contact Product Marketing for availability and pricing on 883B, HR and BR products not listed here.

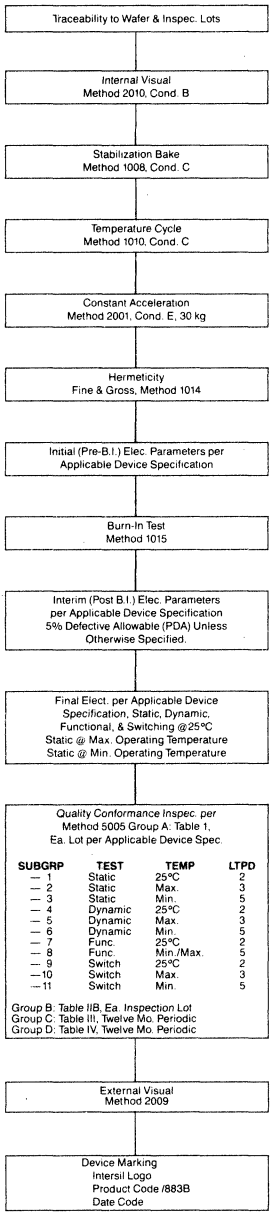
100% DISCRETE DEVICE PROCESSING

Intersil also offers several QPL-approved discrete products carrying the JANTX designation, which are screened and qualified to the latest revisions of MIL-STD-750 and MIL-S-19500.

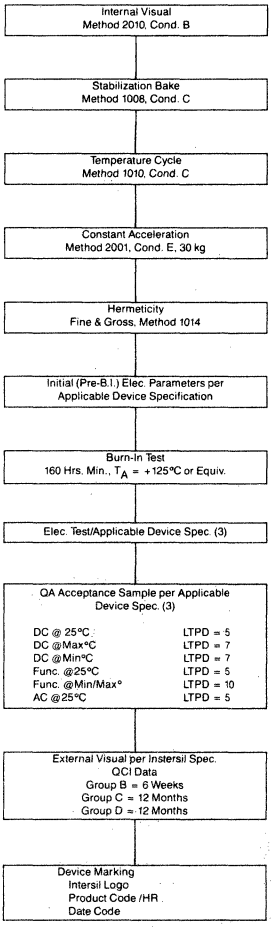
38510
Per MIL-M-38510
Slash Sheet



/883B (1, 2, 4)
Per MIL-STD-883
Rev. C, Class B
Screening per Method 5004

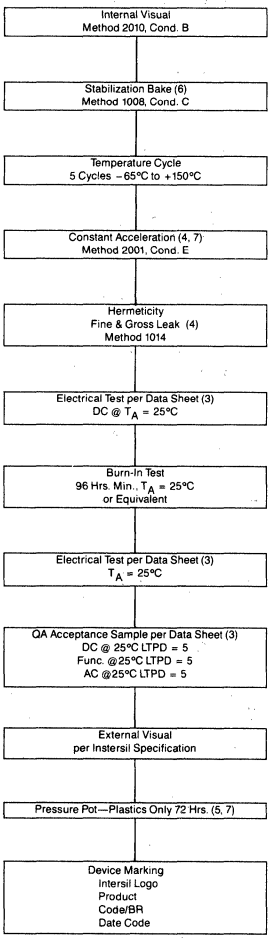


HR (1, 2, 4)
In-House Hi Rel Processing
Flows Performed 100% Unless
Otherwise Noted Applies to
IC's and Hybrids

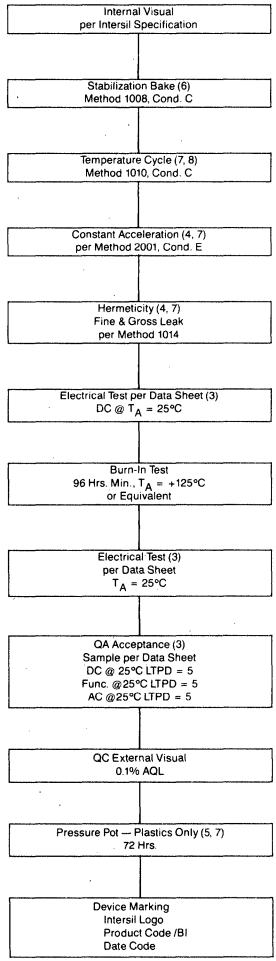


10

BR (1, 2)
Performed 100% Unless Otherwise Noted
APPLIES TO IC'S AND HYBRIDS



BI (1, 2)
Performed 100% Unless Otherwise Noted
APPLIES TO IC'S ANY HYBRIDS AND TRANSISTORS



FOOTNOTES:

(1) Governing Document, Order of Precedence
- A. Purchase Order Contract
- B. Detail Specification
- C. This Flow

(2) Where test methods are indicated, the test will be performed to MIL-STD-883.

(3) With exception of parameters guaranteed by basic design, not tested.

(4) Does not apply to plastic packages.

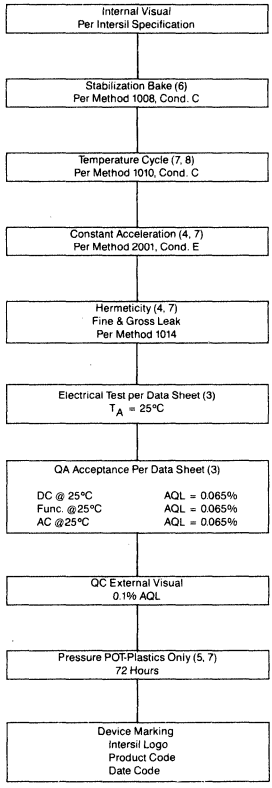
(5) May be performed any time after encapsulation.

(6) For Plastic 12 Hrs @ 140°C ± 10°C.

(7) Weekly Reliability Monitor.

(8) For Plastics-Thermal Shock Method 1011.

Standard Product (1, 2)
Performed 100% Unless Otherwise Noted
APPLIES TO IC'S AND HYBRIDS AND TRANSISTORS



FOOTNOTES:

(1) Governing Document, Order of Precedence
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- B. Detail Specification
- C. This Flow

(2) Where test methods are indicated, the test will be performed to MIL-STD-883.

(3) With exception of parameters guaranteed by basic design, not tested.

(4) Does not apply to plastic packages.

(5) May be performed any time after encapsulation.

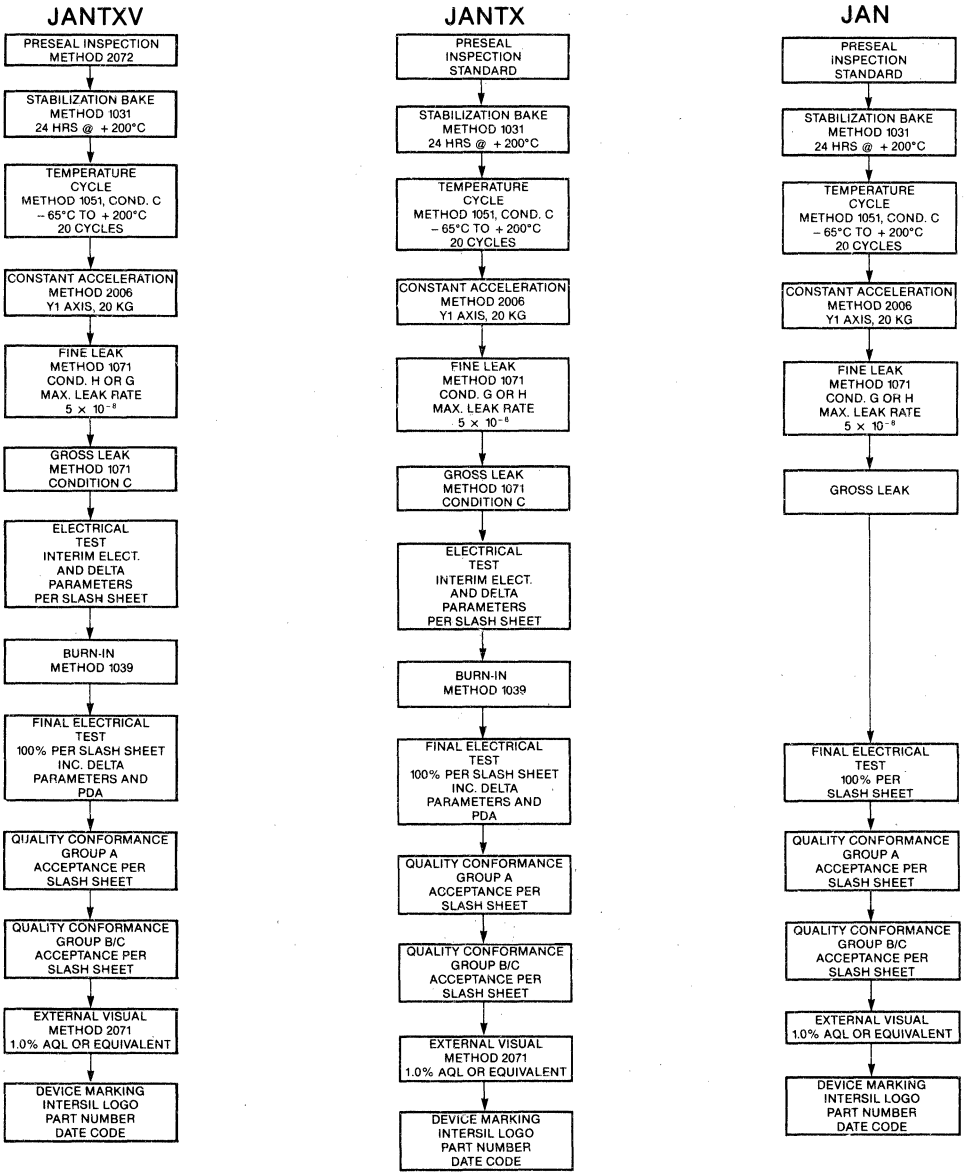
(6) For Plastic 12 Hrs @ 140°C ± 10°C.

(7) Weekly Reliability Monitor.

(8) For Plastics-Thermal Shock Method 1011.

High-Reliability/Military Products
Discrete Products JANTXV, JANTX and JAN
Per MIL-S-19500 and MIL-STD-750

Performed 100% unless otherwise noted



HIGH RELIABILITY PROCESSING
PROCESS FLOW SELECTION GUIDE
- STANDARD IC PROCESS FLOWS -

	38510 JAN	883B REV. C.	HR	BR	BI	COMMERCIAL	NOTES
ON-SHORE BUILD	X						
WAFER LOT TRACEABILITY	X	X					2
PRE-CAP VISUAL M2010B	X	X	X	X			
STABILIZATION BAKE	X	X	X	X	X	X	
TEMPERATURE CYCLE	X	X	X	X	S	S	3
CENTRIFUGE	X	X	X	S	S	S	
HERMETICITY	X	X	X	X	S	S	
ELECTRICAL TEST	X	X	X	X	X		
BURN-IN	X	X	X	X	X		
ELECTRICAL TEST	X	X	X	X	X	X	
POST BURN-IN PDA	X	X					
D.C. ELECT. @ 3 TEMPS.	X	X					
A.C. ELECT. @ 25°C	X	X	X				
GROUP A SAMPLE INSPECTION	X	X	X	X	X	X	
GROUP B EAC INSP. LOT	X	X	S	S	S	S	3
STRICT DOCUMENTATION	X	X					
GROUP C & D INSPECTION	S	S	G	G			3

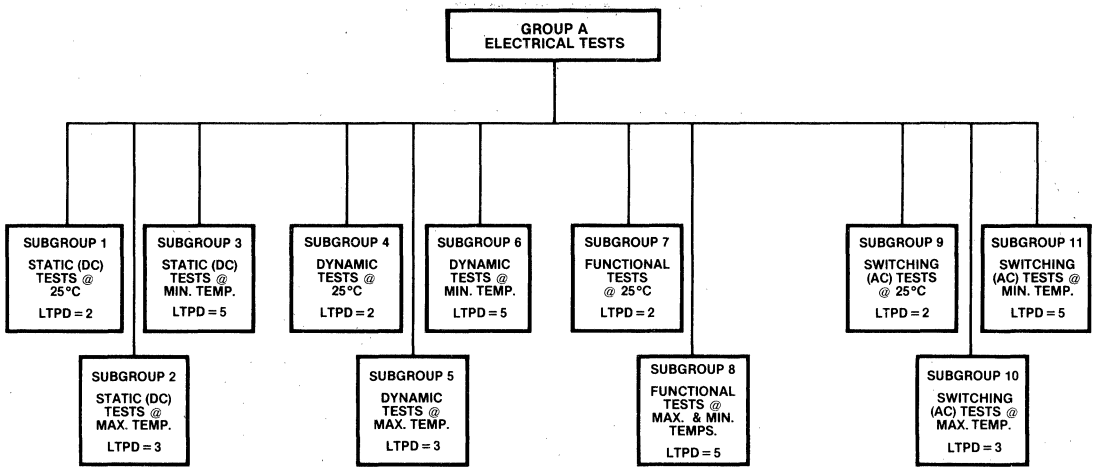
NOTES:
1. ONLY MAJOR IC PROCESSING DIFFERENCES ARE SHOWN HERE. SEE DETAIL FLOWS ON FOLLOWING PAGES FOR MORE SECIFIC DATA. CHART IS FOR HERMETIC PACKAGES. ONLY MINIMUM REQUIREMENTS ARE SHOWN. 38510 IS CLASS B.
2. WAFER LOT TRACEABILITY MAINTAINED AND AVAILABLE AT EXTRA CHARGE FOR OTHER PRODUCTS.
3. S = SAMPLE TEST ON REGULAR BASIS.
   X = PERFORMED 100%. G = GENERIC DATA.
4. INTERSIL ALSO OFFERS "SPECIALS" TO SPECIFIC CUSTOMER SCD'S. SPECIALS ARE AVAILABLE WITH ANY OF THE ABOVE PROCESSING PLUS SEM, PIND, ETC.

HIGH RELIABILITY PROCESSING
PROCESS FLOW SELECTION GUIDE
- STANDARD TRANSISTOR PROCESS FLOWS -

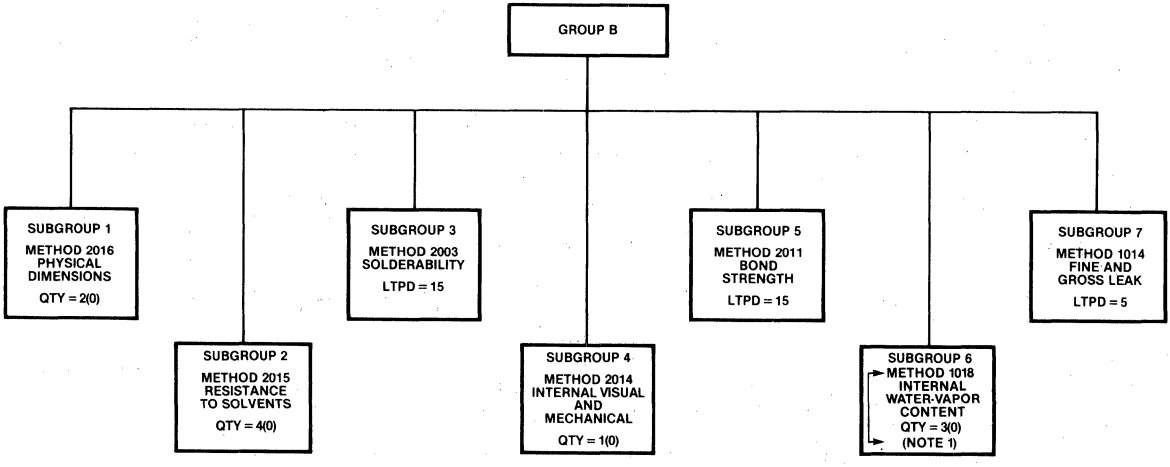
	JANTXV	JANTX	JAN	BI	COMMERCIAL	NOTES
ON-SHORE BUILD	X					
INSPECTION LOT TRACEABILITY	X	X				2
PRE-CAP VISUAL	X	X	X			
STABILIZATION BAKE	X	X	X	X	X	
TEMPERATURE CYCLE	X	X	X	S	S	3
CENTRIFUGE	X	X		S	S	
HERMETICITY	X	X	X	S	S	
ELECTRICAL TEST	X	X		X		
BURN-IN	X	X		X		
ELECTRICAL TEST	X	X				
POST BURN-IN PDA	X	X				
D.C. ELECT. @ 25°C	X	X	X	X	X	
A.C. ELECT. @ 25°C	X	X	X	X	X	
GROUP A	X	X	X	X	X	
GROUP B EACH INSP. LOT	X	X	S	G	G	3
STRICT DOCUMENTATION	X	X	X			
GROUP C INSPECTION	S	S	S			

NOTES:
1. ONLY MAJOR TRANSISTOR PROCESSING DIFFERENCES ARE SHOWN HERE. SEE DETAIL FLOWS ON FOLLOWING PAGES FOR MORE SPECIFIC DATA. CHART IS FOR HERMETIC PACKAGES. ONLY MINIMUM REQUIREMENTS ARE SHOWN.
2. WAFER LOT TRACEABILITY MAINTAINED AND AVAILABLE AT EXTRA CHARGE FOR OTHER PRODUCTS.
3. S = SAMPLE TEST ON REGULAR BASIS.
   X = PERFORMED 100%. G = GENERIC DATA.
4. INTERSIL ALSO OFFERS "SPECIALS" TO SPECIFIC CUSTOMER SCD'S. SPECIALS ARE AVAILABLE WITH ANY OF THE ABOVE PROCESSING PLUS SEM, PIND, ETC.

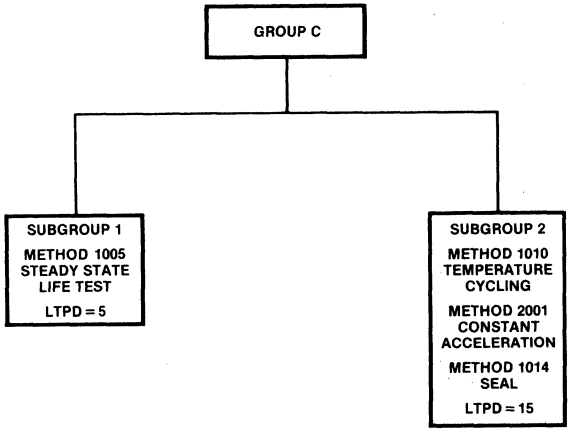
MIL-STD-883 REV. C, CLASS B

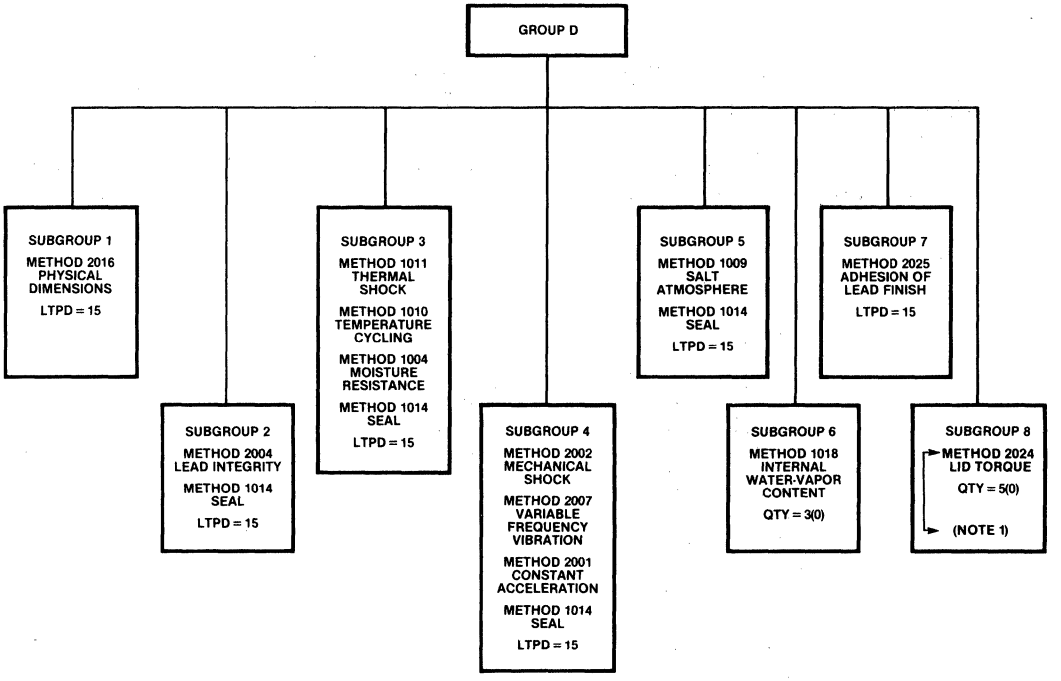


Notes:
1. The specific parameters to be included for tests in each subgroup shall be specified in the applicable procurement document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no Group A testing is required for that subgroup or test.
2. A single sample may be used for all subgroup testing. Where required size exceeds the lot size, 100% inspection shall be allowed.
3. Maximum accept number is 2.



Notes:
1. Required only if package contains a desiccant.
2. Where no LTPD is shown, QTY = sample size and (#) = maximum allowed rejects.





Notes:

1. Applies if package has a Frit-Seal.
2. Where no LTPD is shown, QTY = sample size and (#) = maximum allowed rejects.

10

Ordering Information for MIL-S-19500 Processed Devices

The following Intersil devices are available as a standard Processed to MIL-S-19500. To order, order by the part number as shown below:

Part Number	MIL-S-19500 Slashsheet	Part Number	MIL-S-19500 Slashsheet
2N3821JAN	MIL-S-19500/375	2N4856JTXV	MIL-S-19500/385
2N3821JTX	MIL-S-19500/375	2N4857JAN	MIL-S-19500/385
2N3821JTXV	MIL-S-19500/375	2N4857JTX	MIL-S-19500/385
2N3823JAN	MIL-S-19500/375	2N4857JTXV	MIL-S-19500/385
2N3823JTX	MIL-S-19500/375	2N4858JAN	MIL-S-19500/385
2N3823JTXV	MIL-S-19500/375	2N4858JTX	MIL-S-19500/385
2N4091JAN	MIL-S-19500/431	2N4858JTXV	MIL-S-19500/385
2N4091JTX	MIL-S-19500/431	2N5114JAN	MIL-S-19500/476
2N4091JTXV	MIL-S-19500/431	2N5114JTX	MIL-S-19500/476
2N4092JAN	MIL-S-19500/431	2N5114JTXV	MIL-S-19500/476
2N4092JTX	MIL-S-19500/431	2N5115JAN	MIL-S-19500/476
2N4092JTXV	MIL-S-19500/431	2N5115JTX	MIL-S-19500/476
2N4093JAN	MIL-S-19500/431	2N5115JTXV	MIL-S-19500/476
2N4093JTX	MIL-S-19500/431	2N5116JAN	MIL-S-19500/476
2N4093JTXV	MIL-S-19500/431	2N5116JTX	MIL-S-19500/476
2N4856JAN	MIL-S-19500/385	2N5116JTXV	MIL-S-19500/476
2N4856JTX	MIL-S-19500/385		

Ordering Information for MIL-M-38510 Slash Sheet Processed Devices

The following Intersil devices are available as a standard processed to the 38510 Slash Sheets. To order, use the part number as shown below:

Part Number	Generic Number
JM38510/11101BAC	(DG181AL)
JM38510/11101BCC	(DG181AP)
JM38510/11101BIC	(DG181AA)
JM38510/11102BAC	(DG182AL)
JM38510/11102BCC	(DG182AP)
JM38510/11102BIC	(DG182AA)
JM38510/11103BAC	(DG184AL)
JM38510/11103BEC	(DG184AP)
JM38510/11104BAC	(DG185AL)
JM38510/11104BEC	(DG185AP)
JM38510/11105BAC	(DG187AL)
JM38510/11105BCC	(DG187AP)
JM38510/11105BIC	(DG187AA)
JM38510/11106BAC	(DG188AL)
JM38510/11106BCC	(DG188AP)
JM38510/11106BIC	(DG188AA)
JM38510/11107BAC	(DG190AL)
JM38510/11107BEC	(DG190AP)
JM38510/11108BAC	(DG191AL)
JM38510/11108BEC	(DG191AP)
JM38510/12704BVC	(AD7541TD)

Ordering Information for DESC Drawing Processed Devices

The following Intersil devices are available as a standard processed to the DESC Drawings. To order, use the part number as shown below:

Part Number	Generic Number	Part Number	Generic Number
DESC77052-01EB	(IH6108MJE)	DESC81006-05AC	(IH5044MFD)
DESC77052-01EX	(IH6108MJE)	DESC81006-05AX	(IH5044MFD)
DESC77053-01EB	(DG201AK)	DESC81006-05EB	(IH5044MJE)
DESC77053-01EX	(DG201AK)	DESC81006-05EX	(IH5044MJE)
DESC81006-01AC	(IH5040MFD)	DESC81006-06AC	(IH5045MFD)
DESC81006-01AX	(IH5040MFD)	DESC81006-06AX	(IH5045MFD)
DESC81006-01EB	(IH5040MJE)	DESC81006-06EB	(IH5045MJE)
DESC81006-01EX	(IH5040MJE)	DESC81006-06EX	(IH5045MJE)
DESC81006-02AC	(IH5041MFD)	DESC81006-07AC	(IH5046MFD)
DESC81006-02AX	(IH5041MFD)	DESC81006-07AX	(IH5046MFD)
DESC81006-02EB	(IH5041MJE)	DESC81006-07EB	(IH5046MJE)
DESC81006-02EX	(IH5041MJE)	DESC81006-07EX	(IH5046MJE)
DESC81006-02IC	(IH5041MTW)	DESC81006-08AC	(IH5047MFD)
DESC81006-02IX	(IH5041MTW)	DESC81006-08AX	(IH5047MFD)
DESC81006-03AC	(IH5042MFD)	DESC81006-08EB	(IH5047MJE)
DESC81006-03AX	(IH5042MFD)	DESC81006-08EX	(IH5047MJE)
DESC81006-03EB	(IH5042MJE)		
DESC81006-03EX	(IH5042MJE)		
DESC81006-04AC	(IH5043MFD)		
DESC81006-04AX	(IH5043MFD)		
DESC81006-04EB	(IH5043MJE)		
DESC81006-04EX	(IH5043MJE)		

GLOSSARY OF MILITARY/AEROSPACE HI-REL DEFINITIONS/TERMINOLOGY

ACCELERATED BURN-IN — Same as "Burn-In", except that testing is carried out at an increased temperature (nominally 150°C) for reduced dwell time. Accelerated testing is not permissible for Class S devices.

ATTRIBUTES DATA — Go-No-Go data. Strictly pass/fail and number of rejects recorded. A typical requirement for post burn-in electrical tests on Class B devices.

BASELINE — Technique used to define manufacturing and test processes at time of order placement. Baselining usually involves development of a Program Plan and an Acceptance Test Plan which include flow charts, specification identification/revision letters, QA procedures, and actual specimens of certain important specifications. During subsequent manufacture and testing of parts, it is not permissible to make revisions or changes to any of the identified specifications, unless prior notification and possible customer approval occurs.

BURN-IN — A screening operation. Devices are subjected to high temperature (typically 125°C) and normal power/operation for 160 hours (Class B devices) or 240 hours (Class S devices).

CLASS S AND B INTEGRATED CIRCUITS — These classes set forth the screening, sampling and document control requirements for IC testing. Terminology is defined in MIL-M-38510 and in Test Methods 5004 and 5005 of MIL-STD-883. Classes, S and B are sometimes referred to as "Levels S and B." The Classes cover:

> **CLASS S** — For space and satellite programs. Includes Condition A Precap, SEM, 240 hour burn-in, PIND test and elaborate qualification and quality conformance testing. Normally requires extensive data, documentation, and program planning. Formerly referred to as Class A. Class S devices are quite expensive.
>
> **CLASS B** — For manned flight, and includes most frequently-procured military integrated circuits. Used for all but highest reliability requirements. Class B uses burn-in, pre-cap visual, etc.

CORRECTIVE ACTION — Those actions which a given supplier (or user) agrees to perform so that a detected problem does not reoccur.

DESC — Defense Electronic Supply Center, located in Dayton, Ohio.

DESC LINE CERTIFICATION — The document which approves a supplier's facilities as an appropriate site to manufacture JAN parts.

DPA — Destructive Physical Analysis. Finished products are opened and analyzed, in accordance with customer or MIL Spec criteria.

GENERIC DATA — Data pertaining to a device family; not necessarily the specific part number ordered by the customer, but representative of parts in the family. Group B, C and D generic data is frequently requested in lieu of the performance of special qual tests on a given order.

GROUP A — Sample electrical test which are performed on each lot. Group A is defined in Test Method 5005 for integrated circuits and in MIL-S-19500 for diodes and transistors.

GROUP B — For Integrated Circuits, Package-Related Environmental Tests are performed for Class B Products per MIL-STD-883, Method 5005 (For Revision Products) or per the "HR" program. For Class S, Group B includes Additional Processing, including steady state life test.

For Diodes and Transistors, both enviromental and life test are performed per MIL-S-19500.

GROUP C — For Class B or "HR" program I.C.'s, Die-Related Tests are performed. Not required for Class S I.C.'s. Group C includes life testing temperature cycling and constant acceleration per MIL-M-38510. For diodes transistors, Group C includes both environmental and life tests per MIL-S-19500.

GROUP D — Additional Package-Related Environmental Test for I.C.'s for Class B or Class S products or per the "HR" program.

JAN — "Joint Army Navy", a registered trademark of the U.S. Government. The JAN marking denotes a device which is in full compliance to MIL-M-38510 or MIL-S-19500.

JAN TX — A JAN-qualified diode or transistor which has been subjected to additional screening and burn-in tests. MIL-S-19500 only.

JAN TXV — A JAN-qualified diode or transistor which, in additional to burn-in testing, has been subjected to additional screening including pre-cap visual inspection, as witnessed by a government source inspector. Equivalent to Class B screening for integrated circuits. MIL-S-19500 only.

LTPD-Lot Tolerance Percent Defective is a sampling plan measurement criteria.

MIL-M-38510 — The general military specification for integrated circuits.

M38510/XXX — Detail specifications (or "slash sheets") for integrated circuits. For example, the 101 specification covers Operational Amplifiers, with electrical requirements for the 741, LM101, 108, 747 types, etc.

MIL-S-19500 — The general military specifications for diodes and transistors.

MIL-S-19500/XXX — Detail specifications (or "slash sheets" for diodes and transistors.

MIL-STD-750 — Specifies Test Methods for diodes and transistors, such as burn-in, pre-cap, temperature cycling, etc.

MIL-STD-883 — Specifies Test Methods for integrated circuits, such as pre-cap, burn-in, hermeticity, storage life, etc.

NPFC — Naval Publications and Forms Center, Philadelphia Printing and distribution source for military specifications.

NON-STANDARD PARTS — In government terminology, refers to non-JAN devices. Non-standard parts are typically covered by user Source Control Drawings (SCD).

NON-STANDARD PARTS APPROVAL — Approval by the government (frequently RADC) of non-JAN parts, typically on source control drawings, for use in a military system or program. This approval is essentially a waiver which permits non-JAN 38510 parts in a system which otherwise mandatorially requires JAN parts only.

OPERATING LIFE TEST — Same conditions as burn-in, but duration is usually 1000 hours. This is a sample test (Qualification and Quality Conformance).

PCA — Parts Configuration Analysis. A new term which has much the same meaning as "Baseline".

PDA — Percent Defective Allowable. Criteria sometimes applied to burn-in screening. MIL-STD-883 and MIL-M-38510 typically require either a 5% or 10% PDA. A 10% PDA means that if more than 10% of that lot fails as a result of burn-in (as determined by pre- and post-burn-in electrical tests) the entire lot is considered to have failed.

PDS — Parameter Drift Screening. Measures the changes (Δs) in electrical parameters through burn-in. Common for Class S devices.

PIND — Particle Impact Noise Detection. This is an audio screening test to locate and eliminate those parts which have loose internal particles. The test can isolate a high percentage of defectives, even in otherwise good lots. Repeatability of the tests is questionable. This test is one of the screening items for Class S integrated circuits.

PREPARING ACTIVITY — The organizational element of the government which writes specifications, frequently RADC.

PRESEAL VISUAL — A screening inspection which involves observation of a die through a microscope.

PROCURING ACTIVITY — Per MIL-M-38510, this is the organizational element in the government which contracts for articles or services. The Procuring Activity can be a subcontractor (OEM), providing that the government delegates this responsibility. In such a case, the subcontractor does not have the power to grant waivers, unless this authority has been approved by the government.

PRODUCT RELIABILITY — Pertains to the level of quality of a product over a period of time. Reliability is usually measured or expressed in terms of Failure Rate (such as "0.002% per 1000 hours) or MTBF (mean time between failure in hours). MTBF is the reciprocal of Failure Rate.

QPL — Qualified Products List. In the case of JAN products, QPLs are identified as QPL-38510 for integrated circuits and QPL-19500 for diodes and transistors. QPL-38510 revisions occur approximately quarterly and QPL-19500 revisions occur approximately annually. In the interim, the government will notify suppliers via letter of any new device qualifications which may have been granted. Two types of QPLs exist for MIL-M-38510:

PART II QPL — This is an interim or temporary QPL which is granted on the basis of having obtained line certification and approval of an Application to Conduct Qualification Testing. A PART II QPL is automatically voided after 90 days whenever any one supplier is granted a PART I QPL.

PART I QPL — A "permanent" QPL, granted after all qualification testing is completed and test data is approved by the government.

QUALIFYING ACTIVITY — Per MIL-M-38510, the organizational element in the government which designates certification (i.e., DESC).

QUALIFICATION TESTING — Initial one-time sample tests which are performed to determine whether device types and processes are good. For integrated circuits, this usually means testing to Groups A, B, C and D per MIL-STD-883. For diodes and transistors, this usually means testing to Groups A, B and C per MIL-STD-750.

QUALITY CONFORMANCE TESTING — These are sample tests which must be performed at prescribed intervals per MIL-M-38510 or MIL-S-19500, assuring that processes remain in control and that individual lots are passed.

RADC — Rome Air Development Command, Griffiss AFB, New York. This is the government organization which created semiconductor specifications; MIL-M-38510 and MIL-STD-883 were developed at RADC. This Air Force unit develops specifications for all U.S. military services. RADC is frequently involved in granting waivers for non-standard parts for Air Force systems.

READ AND RECORD DATA — Same as variable data.

REWORK PROVISION — For semiconductor devices, permissible rework of parts is usually limited to re-testing (screening), re-marking, and cleaning.

SCREENING — Operations which are performed on devices on a 100% basis (not sampling). Examples include pre-cap visual, burn-in hermeticity, 100% electrical test, etc.

SEM INSPECTION — Inspection by Scanning Electron Microscope. Die samples are examined at very high magnification for metallization defects.

SERIALIZATION — The marking of a unique part number on each part, with assigned numbers marked sequentially/consecutively.

SCDs — Source Control Drawings. Typically user-generated drawings which require development of internal IC vendor sheets. Although each drawing may be slightly different, all will be modelled around MIL-M-38510, MIL-S-19500, MIL-STD-883, or MIL-STD-750.

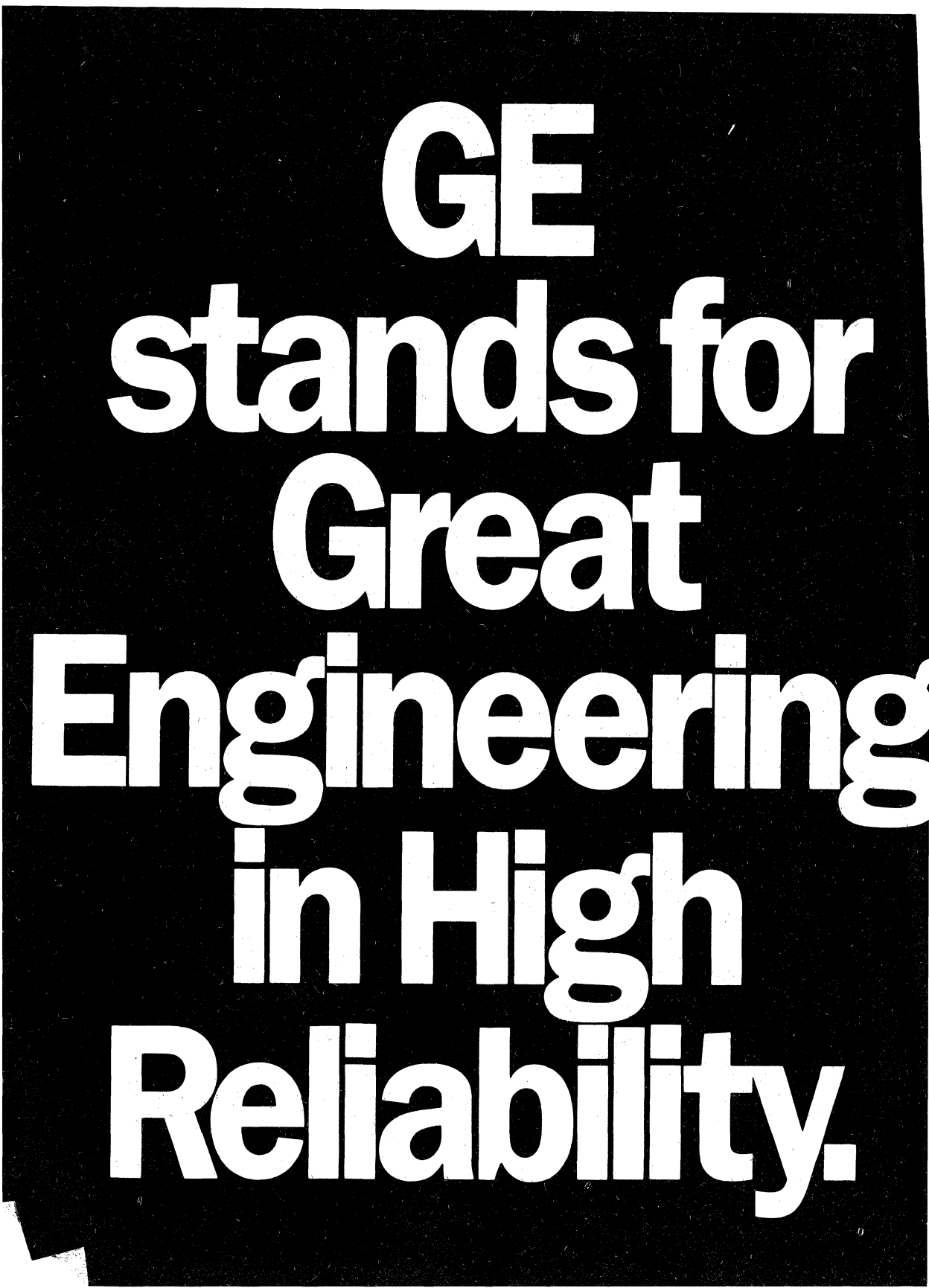
SOURCE INSPECTION — Can be either Customer Source Inspection (CSI) or Government Source Inspection (GSI). Source Inspection is initiated via purchase order, and can typically occur at one or more points:

- Pre-cap Visual. Expensive and adds to throughput time.
- Final Inspection.

TRACEABILITY — A production and manufacturing control system which includes:

- Wafer run identification number.
- Date pre-cap visual inspection was performed, identity of inspector, and specification number and revision.
- Lot number and inspection history.
- QA Group A electrical results.

VARIABLE DATA — Read and recorded electrical measurements (parametric values). Usually required for pre- and post-burn-in electrical tests. Also common for Group C and D testing.


GE
stands for
Great
Engineering
in High
Reliability.

PART NUMBERING SYSTEM

INTERSIL

Examples of Intersil Part Numbers

BASIC	ELECTRICAL OPTION	TEMP	PKG	PIN	ORDER #
ICH8500	A	C	T	V	ICH8500ACTV
ICL8038	C	C	P	D	ICL8038CCPD
IH5040		M	D	E	IH5040MDE

ON ALL INTERSIL IC PART NUMBERS. THE LAST THREE LETTERS ARE TEMPERATURE, PACKAGE, AND NUMBER OF PINS, RESPECTIVELY.

PACKAGE:

A	TO-237
B	Plastic flat-pack
C	TO-220
D	Ceramic dual-in-line
E	Small TO-8
F	Ceramic flat-pack
H	TO-66
I	16 pin (.6 x .7 pin spacing) hermetic hybrid dip
J	Cerdip dual-in-line
K	TO-3
L	Leadless, ceramic
P	Plastic dual-in-line
S	TO-52
T	TO-5 type (also TO-78, TO-99, TO-100)
U	TO-72 type (also TO-18, TO-71)
V	TO-39
Z	TO-92
/W	Wafer
/D	Dice

NUMBER OF PINS:

A	8	P	20
B	10	Q	2
C	12	R	3
D	14	S	4
E	16	T	6
F	22	U	7
G	24	V	8 (0.200" pin circle, isolated case)
H	42		
I	28	W	10 (0.230" pin circle, isolated case)
J	32		
K	35	Y	8 (0.200" pin circle, case to pin 4)
L	40		
M	48	Z	10 (0.230" pin circle, case to pin 5)
N	18		

10

APPLICATION NOTE SUMMARY

The following are brief descriptions of current Intersil Application notes.

A003 UNDERSTANDING AND APPLYING THE ANALOG SWITCH
Introduces analog switches and compares them to relays. Describes CMOS, hybrid (FET + driver), J-FET "virtual ground" and J-FET "positive signal" types. Application information included.

A004 IH5009 LOW COST ANALOG SWITCH SERIES
Compares the members of the IH5009 "virtual ground" analog switches and provides suggested applications.

A005 THE 8007 — A HIGH PERFORMANCE FET INPUT OP AMP
Compares the 8007 with the 741, which is pin compatible and suggests applications such as logantilog amplifier, sample and hold circuit, photometer, peak detector, etc.

A007 USING THE 8048/8049 MONOLITHIC LOG-ANTILOG AMPLIFIER
Describes in detail the operation of the 8048 logarithmetic amplifier, and its counterpart, the 8049 antilog amp.

A011 A PRECISION FOUR QUADRANT MULTIPLIER — THE 8013
Describes, in detail, the operation of the 8013 analog multiplier. Included are multiplication, division, and square root applications.

A013 EVERYTHING YOU ALWAYS WANTED TO KNOW ABOUT THE 8038
This note includes 17 of the most asked questions regarding the use of the 8038.

A015 DESIGN FOR A BATTERY OPERATED FREQUENCY COUNTER
Describes a low cost battery operated frequency/period counter using the 7207A and 7208. Includes specifications, schematics, PC layout, etc.

A016 SELECTING A/D CONVERTERS
Describes the differences between integrating converters and successive approximation converters. Includes a checklist for decision making, and a note on multiplexed data systems.

A017 THE INTEGRATING A/D CONVERTER
Provides an explanation of integrating A/D converters, together with a detailed error analysis.

A018 DO'S AND DONT'S OF APPLYING A/D CONVERTERS
An analysis of proper design techniques using D/A converters.

A019 4½ DIGIT PANEL METER DEMONSTRATION/INSTRUMENTATION BOARDS
Describes two typical PC board layouts using the 8052A/7103A 4½ digit A/D pair. Includes schematics, parts layout, list of materials, etc. Also see A028.

A020 A COOKBOOK APPROACH TO HIGH SPEED DATA ACQUISITION AND MICROPROCESSOR INTERFACING
Uses the building block approach to design a complete 12 volt system. Explains the significance of each component and demonstrates methods for microprocessor interfacing, including the use of control signals.

A021 POWER D/A CONVERTERS USING THE ICH 8510
Detailed analysis of the 8510. Included are a section describing the linearity of the device and application notes for driving servo motors, linear and rotary actuators, etc. Also see A026.

A022 A NEW J-FET STRUCTURE — THE VARAFET
Describes in detail the operation of the varafet, a standard J-FET with the analog gate interfacing components monolithically built-in.

A023 LOW COST DIGITAL PANEL METER DESIGNS
Provides a detailed explanation of the 7106 and 7107 3½ digit panel meter IC's, and describes two of the evaluation kits available from Intersil.

A026 DC SERVO MOTOR SYSTEMS USING THE ICH8510
This companion note to A021 explains the design techniques utilized in using the ICH8510 family to drive closed loop servo motor systems.

A027 POWER SUPPLY DESIGN USING THE ICL8211 AND ICL8212
Explains the operation of the ICL8211/12 and describes various power supply configurations. Included are positive and negative voltage regulators, constant current source, programmable current source, current limiting, voltage crowbarring, power supply window detector, etc.

A028 BUILDING AN AUTO RANGING DMM WITH THE ICL7103A/8052A CONVERTER PAIR
This companion app note to A019 explains the use of the 8052A/7103A converter pair to build a ±4½ digit auto ranging digital multimeter. Included are schematics, circuit descriptions, tips and hints, etc.

A029 POWER OP AMP HEAT SINK KIT
Describes the heat sinks for the ICH8510 family. These heat sinks may be ordered from the factory.

A030 THE ICL7104: A BINARY OUTPUT A/D CONVERTER FOR MICROPROCESSORS
Describes in detail the operation of the 7104. Includes in digital interfacing, handshake mode, buffer gain, auto-zero and external zero. Appendix includes detailed discussion of auto-zero loop residual errors in dual slope A/D conversion.

A031 COIL DRIVE ALARM DESIGN CONSIDERATIONS
Explains the procedure used when using watch circuits to drive piezoelectric transducers.

A032 UNDERSTANDING THE AUTO-ZERO AND COMMON MODE PERFORMANCE OF THE ICL7106/7107/7109 FAMILY
Explains in detail the operation of the ICL7106/7/9 family of A/D Converters.

A046 BUILDING A BATTERY OPERATED AUTO RANGING DVM WITH THE ICL7106
Explains principles of auto ranging, problems and solutions. Includes clock circuits, power supply requirements, design hints, schematics, etc.

A047 GAMES PEOPLE PLAY WITH A/D CONVERTERS
Describes 25 different integrating A/D converter applications. Input circuits, conversion modifications,

display and microprocessor interfaces are shown in detail.

A050 USING THE IT500 FAMILY TO IMPROVE THE INPUT BIAS CURRENT OF BIFET OP AMPS
A brief description of a preamplifier for BIFET OP AMPS.

A051 PRINCIPLES AND APPLICATIONS OF THE ICL7660 CMOS VOLTAGE CONVERTER
Describes internal operation of the ICL7660. Includes a wide range of possible applications.

A052 TIPS FOR USING SINGLE CHIP 3½ DIGIT A/D CONVERTERS
Answers frequently asked questions regarding the operation of 3½ digit single chip A/D converters. Included are sections on power supplies, displays, timing and component selection.

A053 THE ICL7650 A NEW ERA IN GLITCH-FREE CHOPPER STABILIZER AMPLIFIERS
A brief discussion of the internal operation of the ICL7650, followed by an extensive applications section including amplifiers, comparators, log-amps, pre-amps, etc.

A054 DISPLAY DRIVER FAMILY COMBINES CONVENIENCE OF USE WITH MICROPROCESSOR INTERFACABILITY
Compares and describes the various display drivers. Includes design examples for 7 segment, Alpha-numeric, and bargraph systems.

M011 AVOIDING PROBLEMS IN CMOS MEMORY OPERATION
Discusses input overvoltage and SCR latchup and the multiple address access problem in CMOS RAMs.

ORDERING INFORMATION

INTERSIL

Device Family Prefixes

AD —Analog Devices Alternate Source
D —Driver/Level Translator IC
DG —Siliconix Analog Switch Alternate Source
DGM—Monolithic DG Analog Switch Replacement
ICL —Linear IC
ICM —Microperipheral IC
ICH —Hybrid IC
IM —Microcontroller IC
LH —National Semiconductor Hybrid Alternate Source
LM —National Semiconductor Alternate Source
MM —High Voltage Analog Switch
NE —Signetics Alternate Source
SE —Signetics Alternate Source

Electrical Option/Variation of Basic Device Type Designators

These designators are datasheet dependent, and are not always used.

Temperature Range Designators

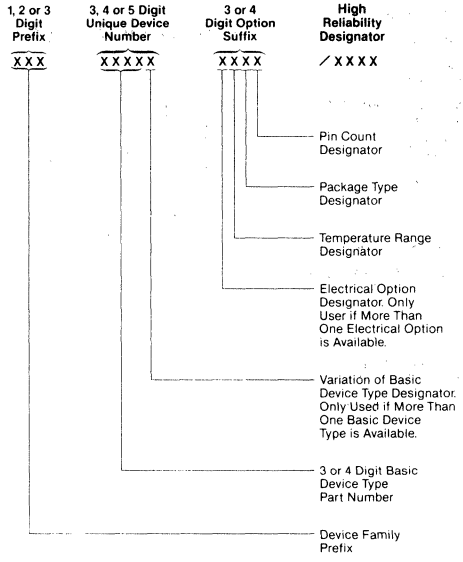
C —Commercial: 0°C to +70°C
I —Industrial: Either −25°C to +85°C or −40°C to +85°C (Specified on Datasheet)
M —Military: −55°C to +125°C

Package Type Designators

A —TO-237
B —Small Outline IC (SOIC)
C —TO-220
D —Ceramic Dual-In-Line
E —Small TO-8
F —Ceramic Flat Pack
H —TO-66
I —16 Pin (.6 x .7 Pin Spacing) Hermetic Hybrid Dip
J — CERDIP Dual-In Line
K —TO-3
L —Leadless, Ceramic
P —Plastic Dual-In-Line
S —TO-52
T —TO-5 Type (Also TO-78, TO-99, TO-100)
U —TO-72 Type (Also TO-18, TO-71)
V —TO-39
Z —TO-92
/W —Wafer
/D —Dice

Part Numbering System

All Intersil IC part numbers consist of a device family prefix, a basic numeric part number, and an option suffix, as follows:



ORDERING INFORMATION

INTERSIL

Pin Count Designator

A	B	P	20
B	10	Q	2
C	12	R	3
D	14	S	4
E	16	T	6
F	22	U	7
G	24	V	8 (0.200" pin circle, isolated case)
H	42		
I	28	W	10 (0.230" pin circle isolated case)
J	32		
K	35	Y	8 (0.200" pin circle, case to pin 4)
L	40		
M	48	Z	10 (0.230" pin circle, case to pin 5)
N	18		

HIGH RELIABILITY DESIGNATOR

/883B — MIL-STD-883B Screened Device

/HR — High-Reliability Device

/BR — Cost Effective High-Reliability Device

/BI — Burn-In Only Process Flow

Example Part Numbers

1) ICL7129CPL

- 40 Pins on Package
- Plastic Dual-In-Line Package
- 0°C to + 70°C Temp. Range
- Basic Part Number: 7129 A/D Converter
- Linear IC Family Device

2) ICM7170IJG

- 24 Pins on Package
- CERDIP Dual-In Line Package
- – 40°C to + 85°C Temp. Range
- Basic Part Number: 7170 Real Time Clock
- Microperipheral IC Family Device

3) IH5043BMFD

- 14 Pins on Package
- Ceramic Flat-Pack Package
- – 55°C to + 125°C Temp. Range
- B Type Electrical Option
- Basic Part Number: 5043 Analog Switch
- Hybrid IC Family Device

4) ICL7134BLCJI

- 28 Pins on Package
- CERDIP Dual-In Line Package
- – 0°C to + 70°C Temp. Range
- L Type Electrical Option
- B Type Device Designator
- Basic Part Number: 7134 D/A Converter
- Linear IC Family Device

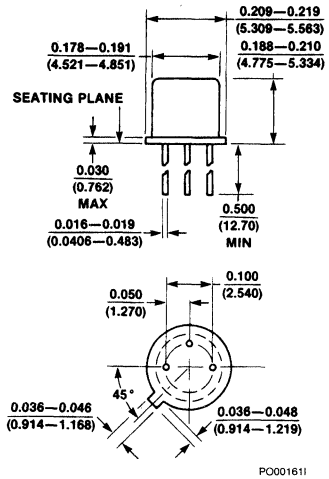
5) IH5009MJD/883B

- MIL-STD-883B Screened Device
- 14 Pins on Package
- CERDIP Dual In-Line Package
- – 55°C to + 125°C Temp. Range
- Basic Part Number: 5009 Analog Switch
- Hybrid IC Family Device

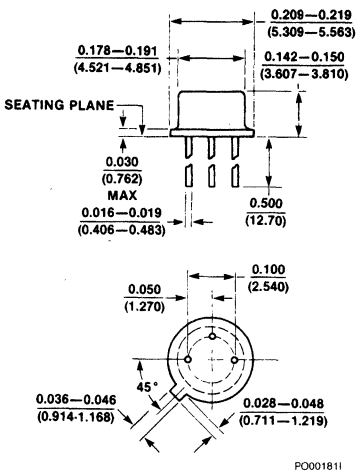
EVALUATION KITS

PRODUCT DESCRIPTION	PART NUMBER	CONTENTS
Power Amplifier Kits	ICH8510IEV/KIT	ICH8510i + Socket + Heat Sink
	ICH8510MEV/KIT	ICH8510 + Socket + Heat Sink
	ICH85201IEV/KIT	ICH8520i + Socket + Heat Sink
	ICH8520MEV/KIT	ICH8520M + Socket + Heat Sink
	ICH85301IEV/KIT	ICH8530i + Socket + Heat Sink
	ICH8530MEV/KIT	ICH8530M + Socket + Heat Sink
3½ Digit LCD Panel Meter Kit	ICL7106EV/KIT	ICL7106 + PC Card + All Passive Components
3½ Digit LED Panel Meter Kit	ICL7107EV/KIT	ICL7107 + PC Card + All Passive Components
3½ Digit Low Power LCD Panel Meter Kit	ICL7126EV/KIT	ICL7126 + PC Card + All Passive Components
4½ Digit A/D Converter Kit	ICL7129EV/KIT	ICL7129 + 4½ Digit LCD Display + ICL8069 + PC Card + Active, Passive Components
4½ Digit A/D Converter Kit	ICL7135EV/KIT	ICL7135 + ICL7660 + ICL8069 + PC Card + Active, Passive Components
4½ Digit LCD Display Driver Kit	ICM7211EV/KIT	ICM7211 + 4½ Digit LCD Display + PC Card + Active, Passive Components
8 Character Multiplexed LCD Display Driver Kit	ICM7233AEV/KIT	2 of ICM7233A + PC Card + 8 Character Triplexed LCD Display
8 Character Multiplexed LED Display Driver Kit	ICM7243BEV/KIT	ICM7243B + PC Card + 8 Character LED
4½ Digit LCD Display Counter Kit	ICL7224EV/KIT	ICM7224 + ICM7207A + 5.24288MHz Crystal + 4½ Digit LCD Display + PC Card + Passive Components
4½ Digit LED Display Counter Kit	ICM7225EV/KIT	ICM7225 + ICM7207A + 5.24288MHz Crystal + 4½ Digit LED Display + PC Card + Passive Components
4½ Digit VF Display Counter Kit	ICM7236EV/KIT	ICM7236 + ICM7207A + 5.24288MHz Crystal + 4½ Digit VF Display + PC Card + Passive Components
Touch Tone Encoder		
One contact per key	ICM7206EV/KIT	ICM7206 + 3.579545MHz Crystal
Two contacts per key, common to positive supply	ICM7206AEV/KIT	ICM7206A + 3.579545MHz Crystal
Common to negative supply, oscillator enabled when key depressed	ICM7206BEV/KIT	ICM7206B + 3.579545MHz Crystal
8 Digit Frequency/Period Counter		
5 Function	ICM7226AEV/KIT	ICM7226A + 10MHz Crystal + PC Card + LEDs + All Passive Components
Oscillator Controller		
For Application as freq. counter with ICM7208	ICM7207EV/KIT	ICM7207 + 6.5536MHz Crystal
	ICM7207AEV/KIT	ICM7207A + 5.24288MHz Crystal

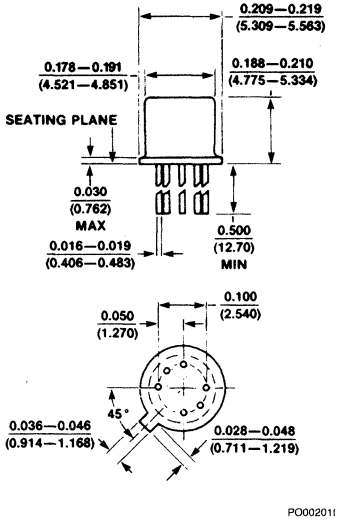
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



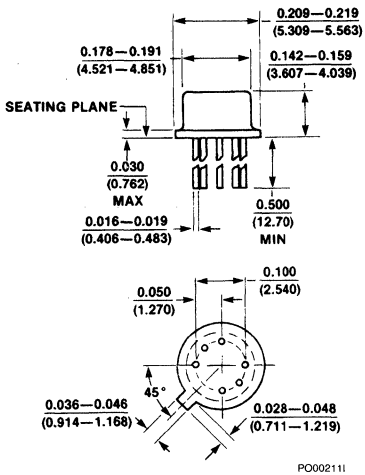
TO-18



TO-52 (SQ*, SR)



TO-71

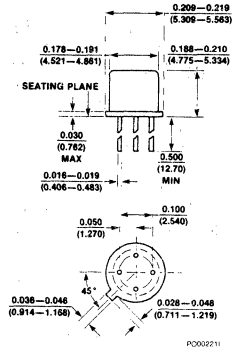


TO-71 LOW PROFILE

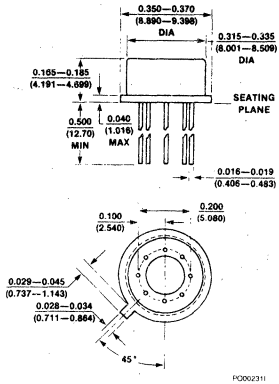
SQ* denotes a two lead package; center lead missing.

10

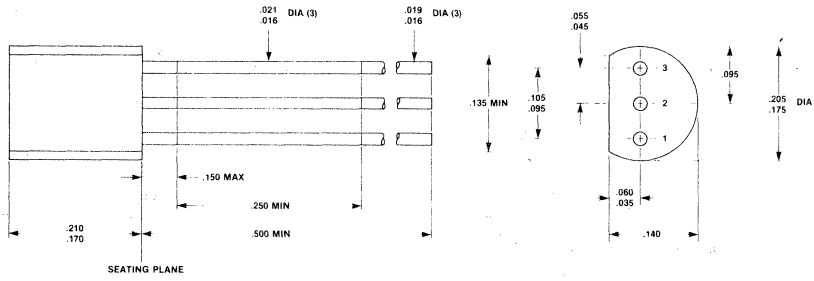
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



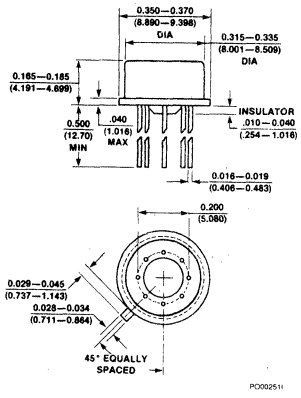
TO-72



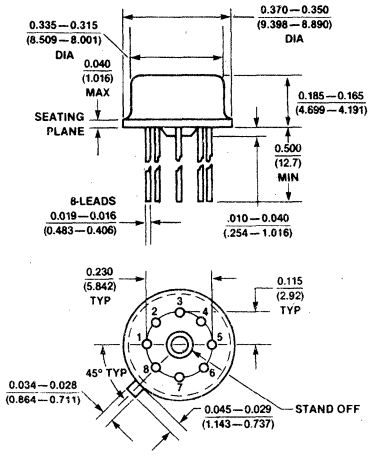
TO-78



TO-92

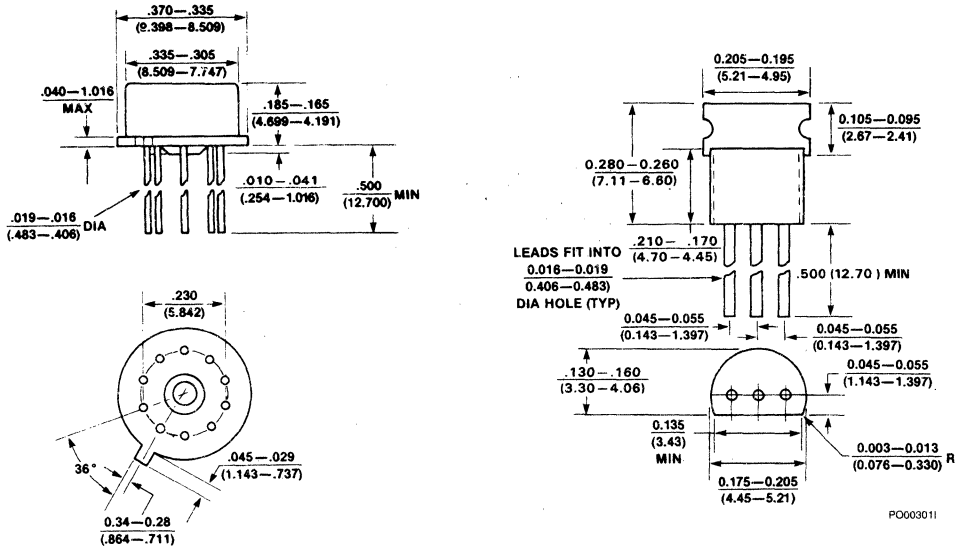


TO-99 TV



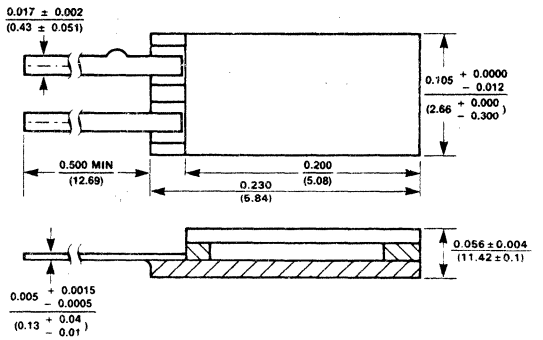
TO-99 TY

PACKAGE OUTLINES All dimensions given in inches and (millimeters).



TO-100 (TW, TX)

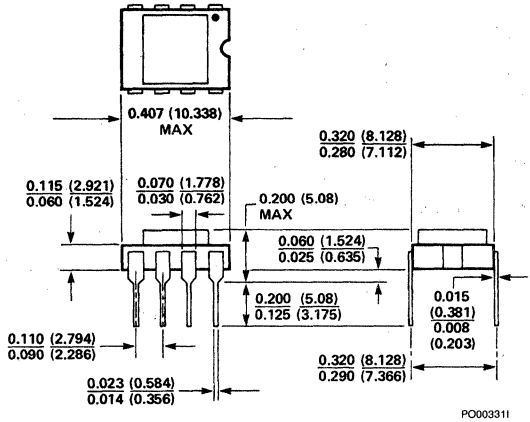
TO-237 JEDEC



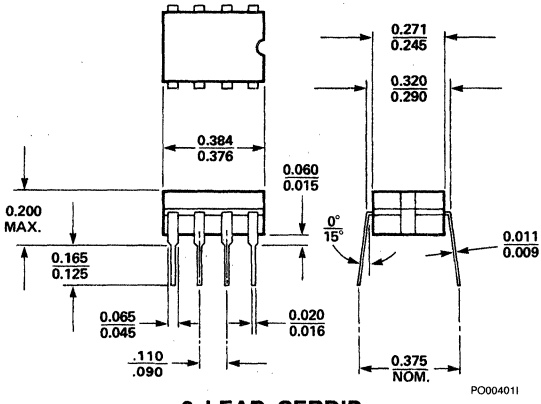
2 LEAD CERAMIC (DH)

10

PACKAGE OUTLINES All dimensions given in inches and (millimeters).

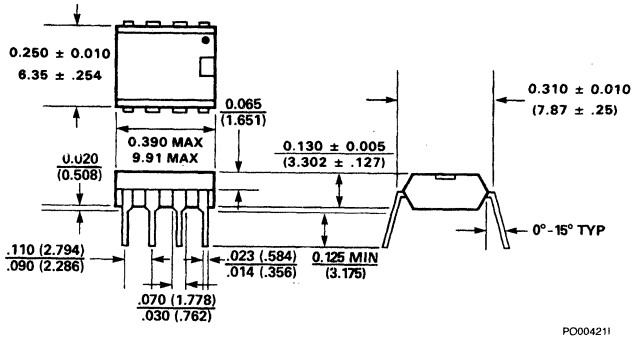


8 LEAD CERAMIC (DA)

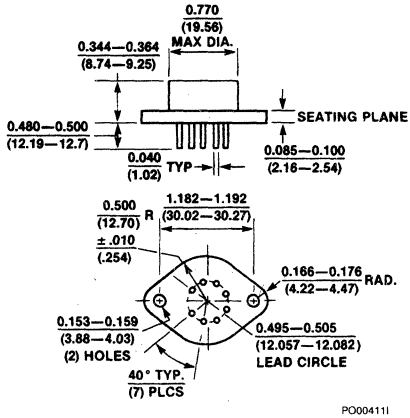


8 LEAD CERDIP

PACKAGE OUTLINES All dimensions given in inches and (millimerters).

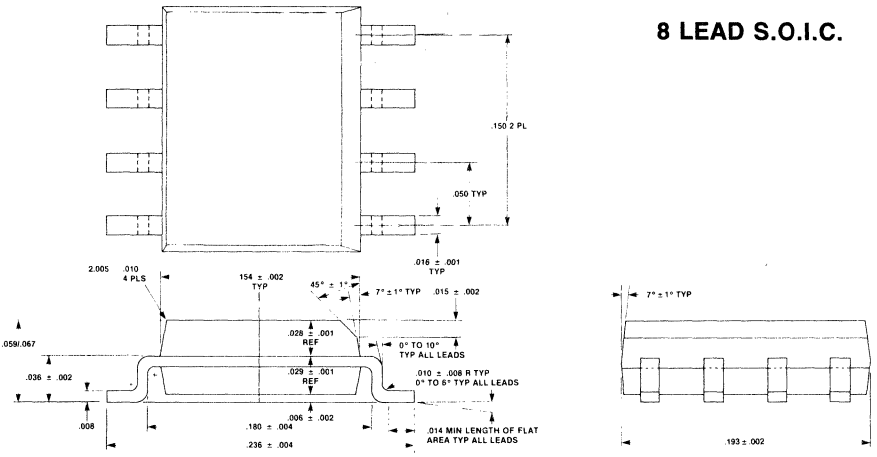


8 LEAD PLASTIC (PA)

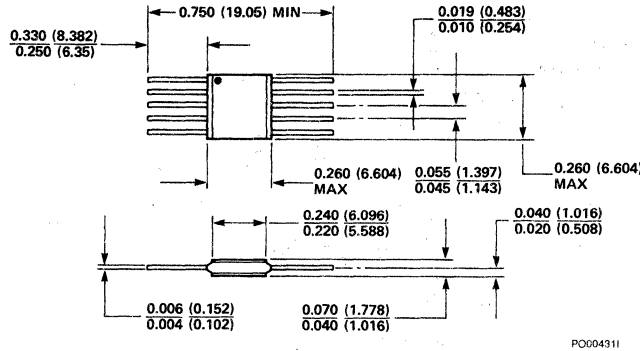


8 LEAD TO-3 METAL CAN

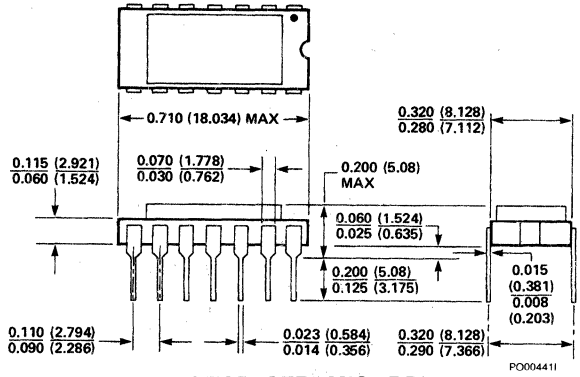
8 LEAD S.O.I.C.



PACKAGE OUTLINES All dimensions given in inches and (millimeters).

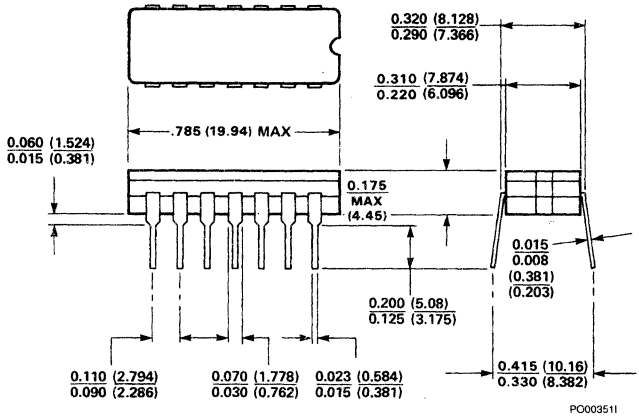


10 LEAD FLATPACK (FB)

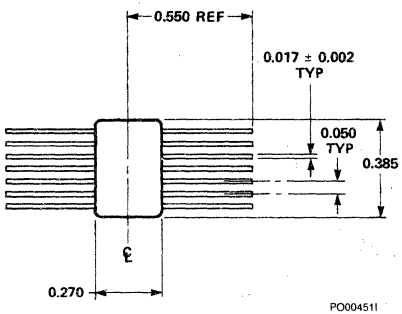


14 LEAD CERAMIC (DD)

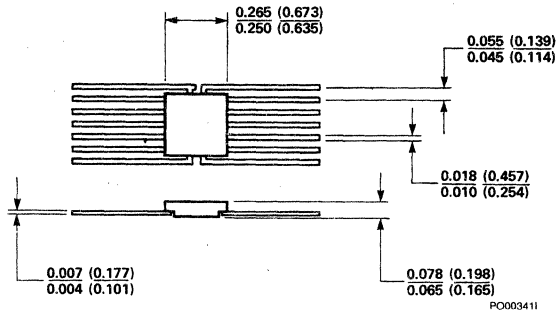
PACKAGE OUTLINES All dimensions given in inches and (millimetes).



14 LEAD CERDIP (JD)



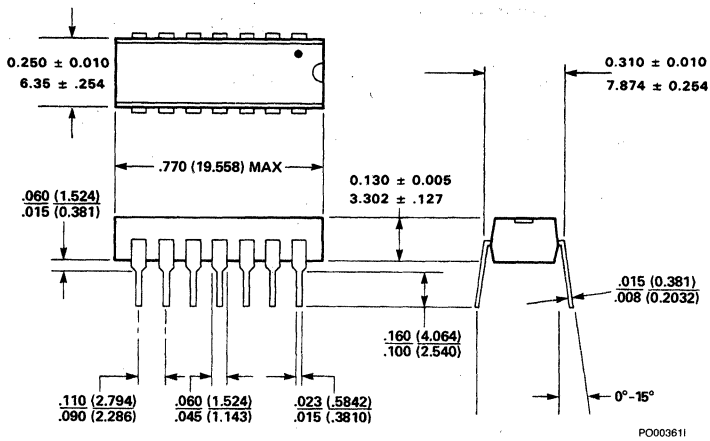
14 LEAD FLATPACK



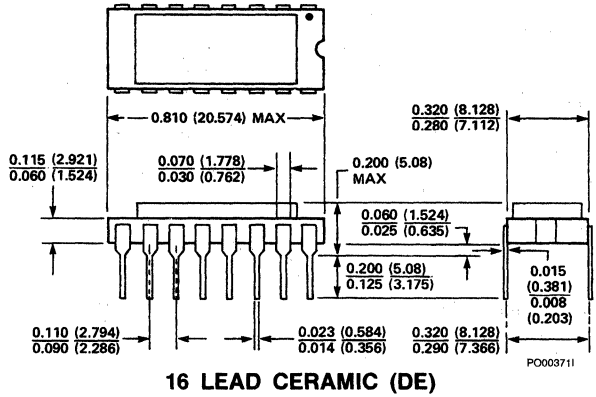
14 LEAD FLATPACK (FD)

10

PACKAGE OUTLINES All dimensions given in inches and (millimeters).

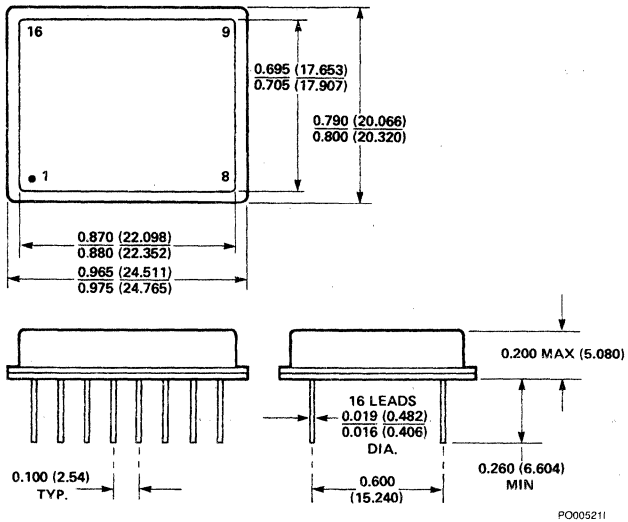


14 LEAD PLASTIC

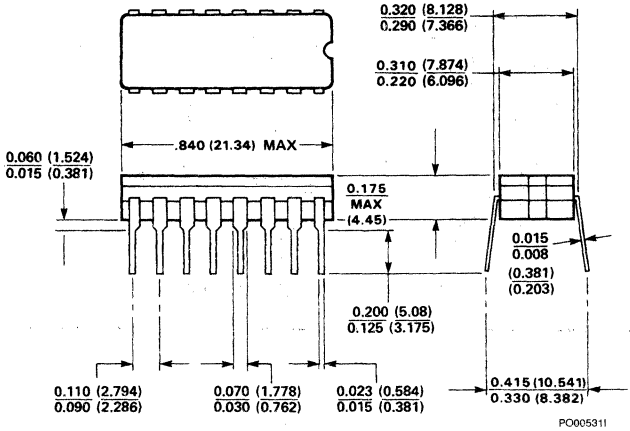


16 LEAD CERAMIC (DE)

PACKAGE OUTLINES All dimensions given in inches and (millimeters).

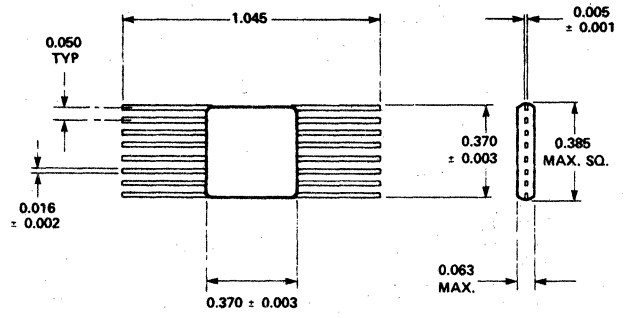


16 LEAD CERAMIC (IE)

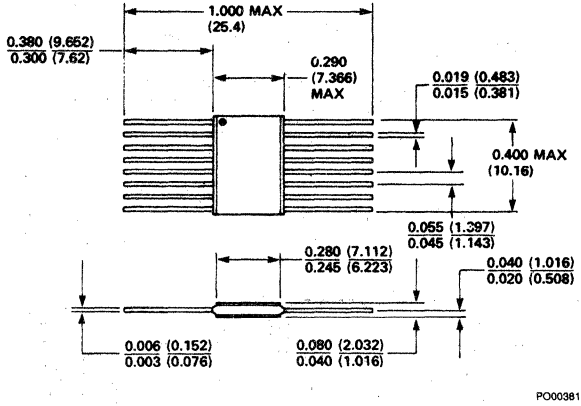


16 LEAD CERDIP (JE)

PACKAGE OUTLINES All dimensions given in inches and (millimeters).

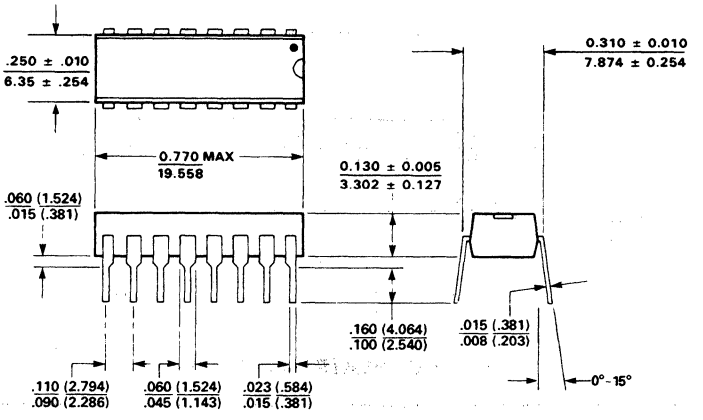


16 LEAD FLATPACK (FE-2)

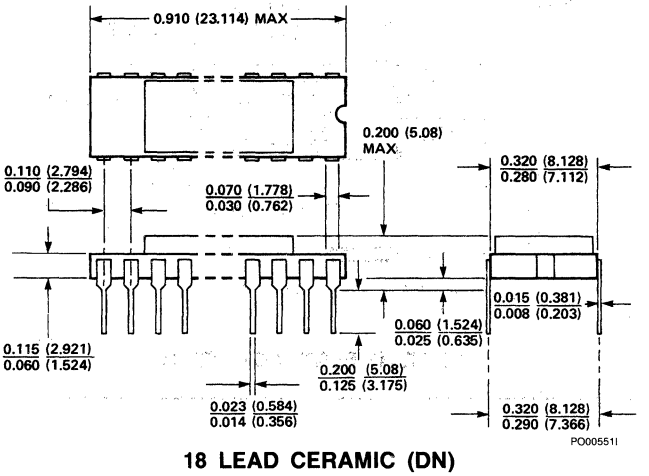


16 LEAD FLATPACK (FE-1)

PACKAGE OUTLINES All dimensions given in inches and (millimeters).



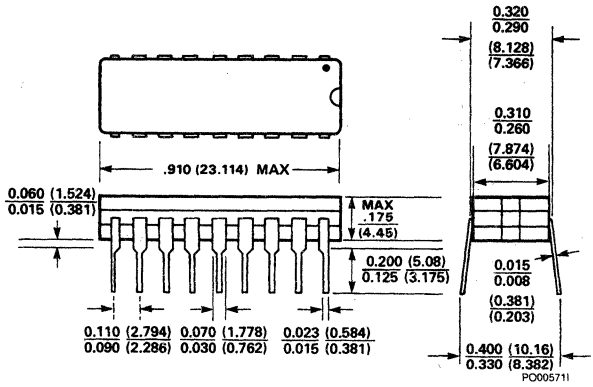
16 LEAD PLASTIC (PE)



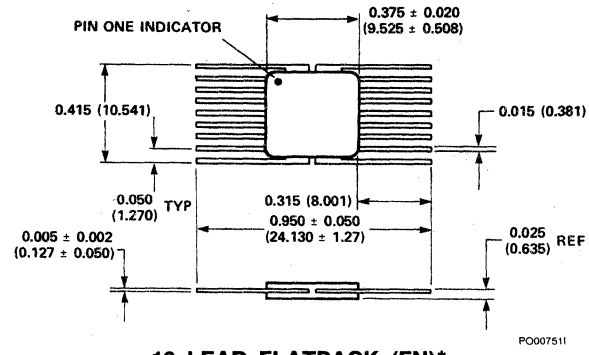
18 LEAD CERAMIC (DN)

10

PACKAGE OUTLINES All dimensions given in inches and (millimeters).

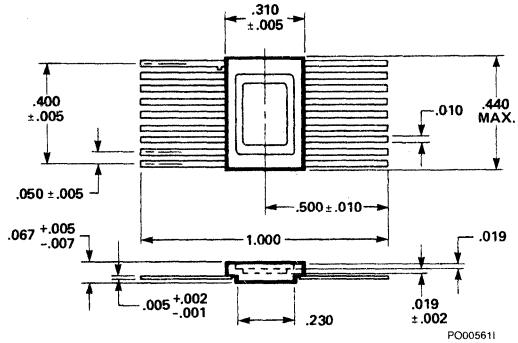


18 LEAD CERDIP (JN)

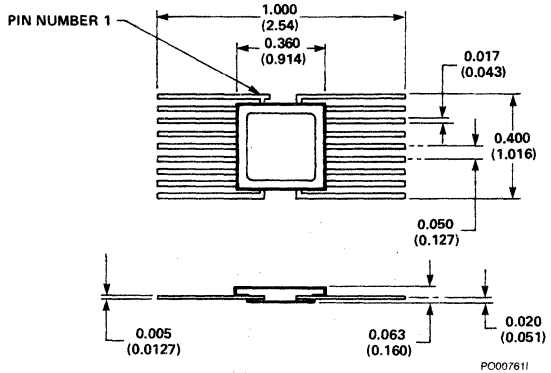


18 LEAD FLATPACK (FN)*

PACKAGE OUTLINES All dimensions given in inches and (millimeters).

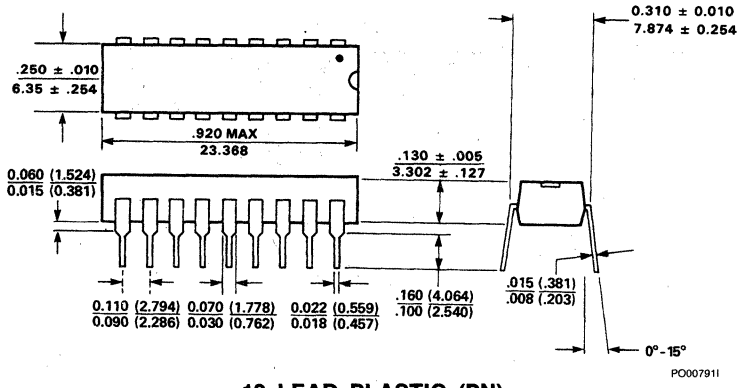


18 LEAD FLATPACK (FN-2)

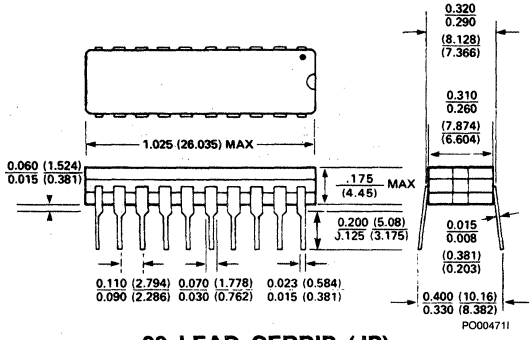


18 LEAD FLATPACK (FN-3)

PACKAGE OUTLINES All dimensions given in inches and (millimeters).

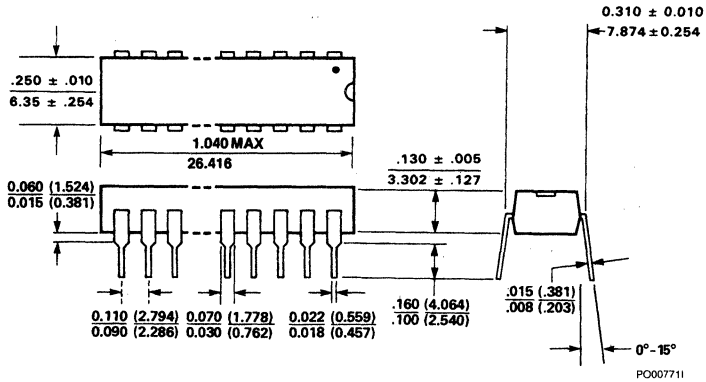


18 LEAD PLASTIC (PN)

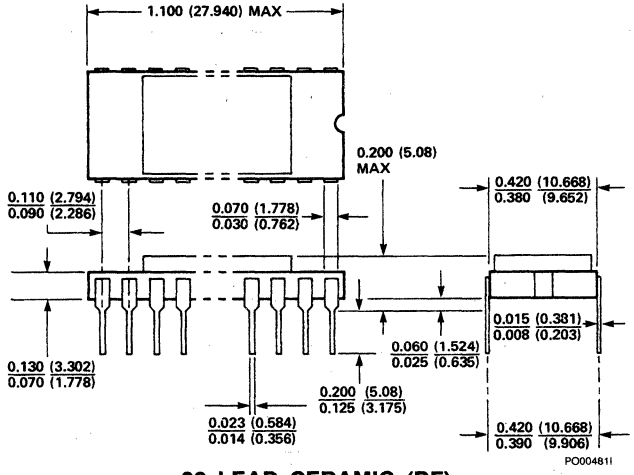


20 LEAD CERDIP (JP)

PACKAGE OUTLINES All dimensions given in inches and (millimeters).



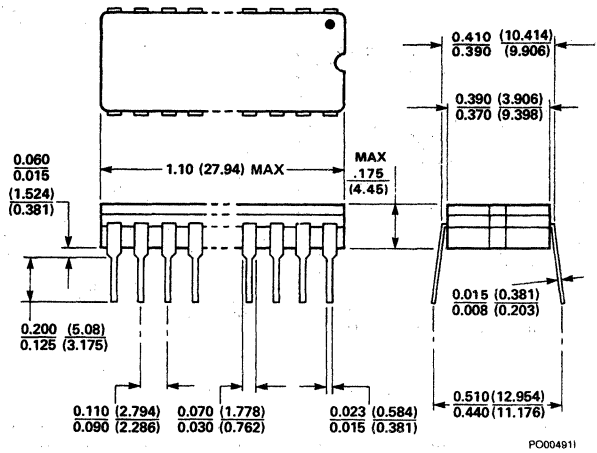
20 LEAD PLASTIC (PP)



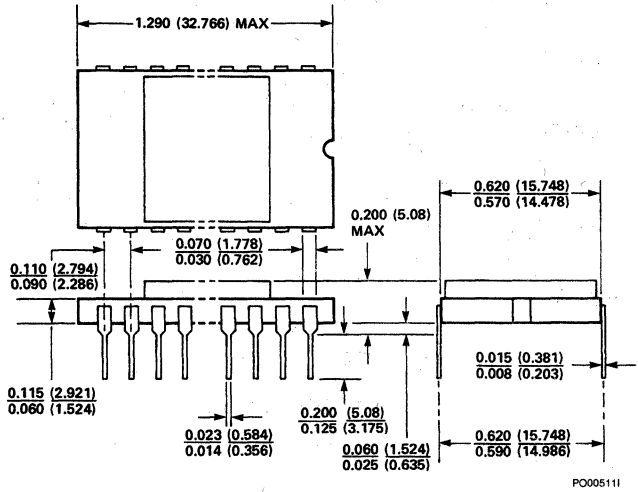
22 LEAD CERAMIC (DF)

10

PACKAGE OUTLINES All dimensions given in inches and (millimeters).

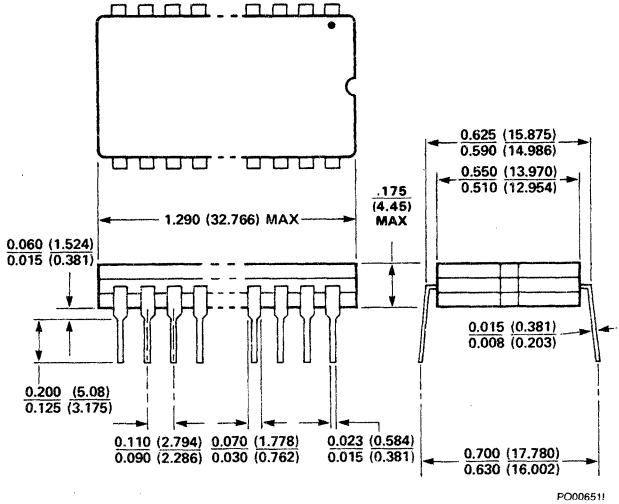


22 LEAD CERDIP (JF)

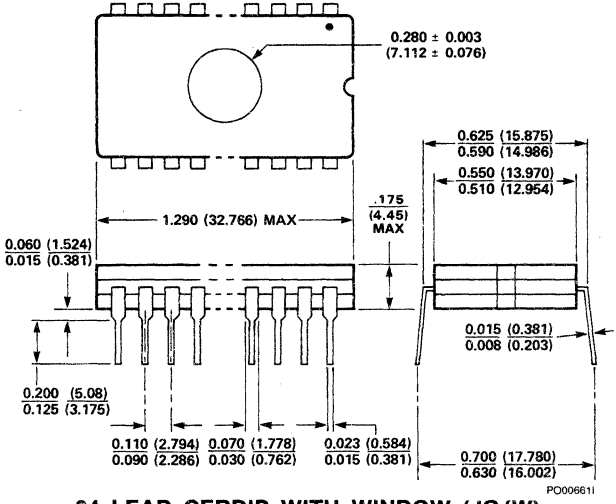


24 LEAD CERAMIC (DG)

PACKAGE OUTLINES All dimensions given in inches and (millimeters).



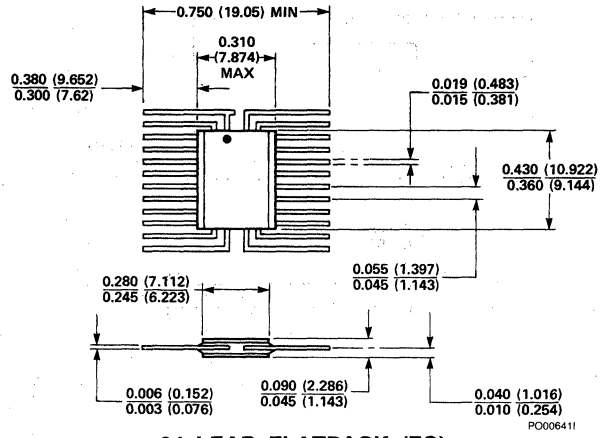
24 LEAD CERDIP (JG)



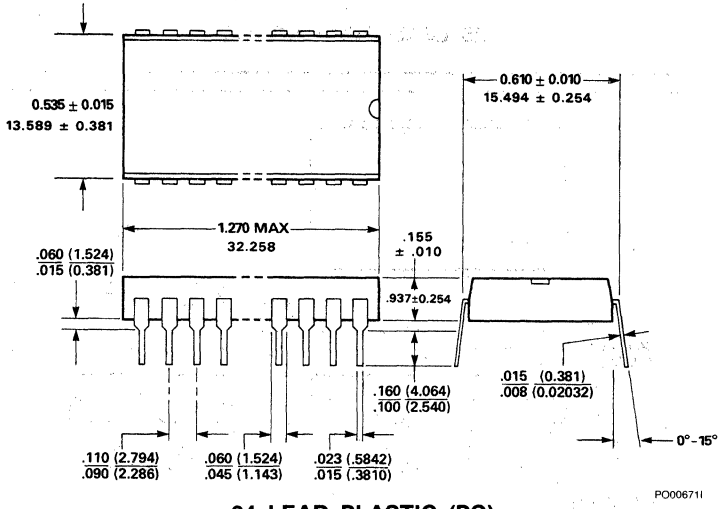
24 LEAD CERDIP WITH WINDOW (JG/W)

10

PACKAGE OUTLINES All dimensions given in inches and (millimeters).

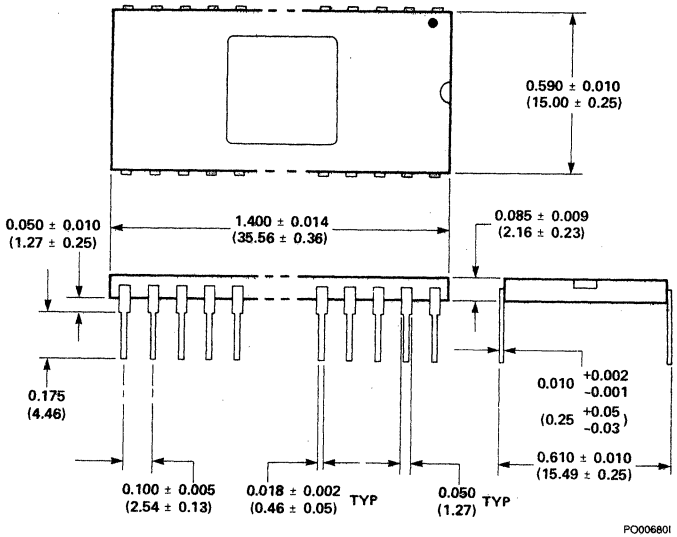


24 LEAD FLATPACK (FG)

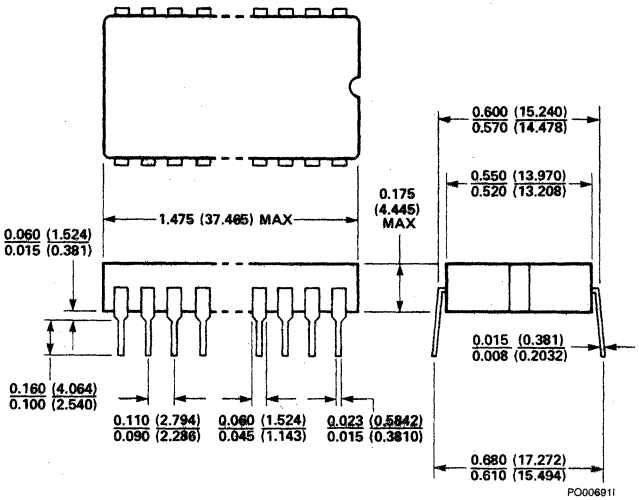


24 LEAD PLASTIC (PG)

PACKAGE OUTLINES All dimensions given in inches and (millimeters).

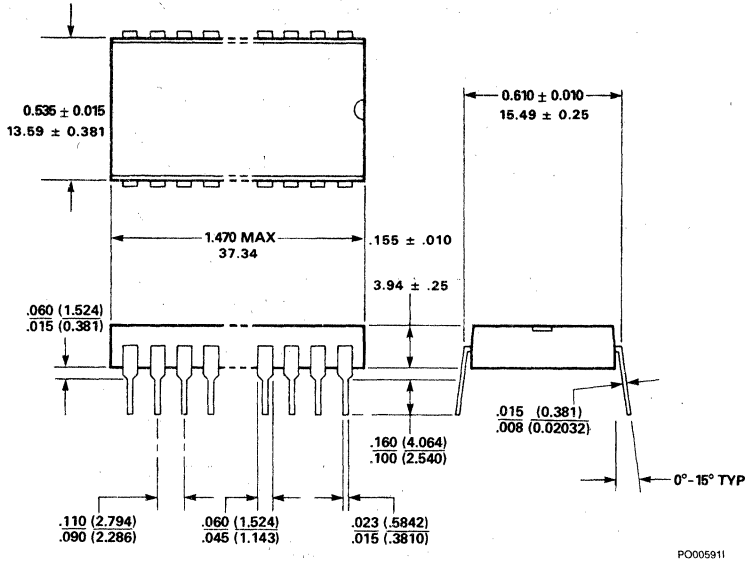


28 LEAD CERAMIC (DI)

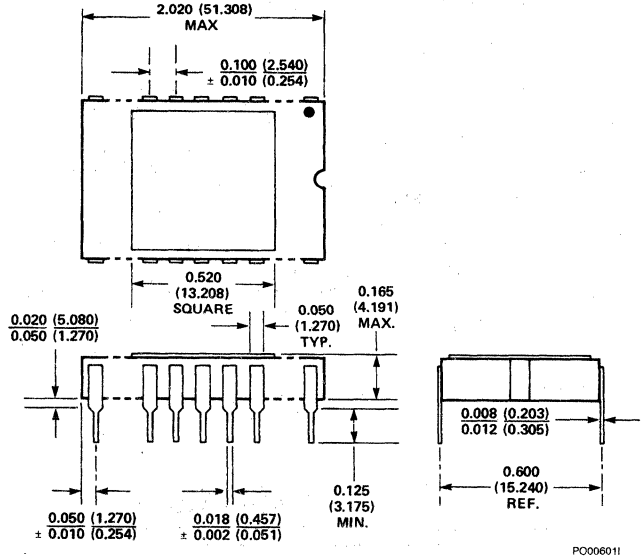


28 LEAD CERDIP (JI)

PACKAGE OUTLINES All dimensions given in inches and (millimeters).

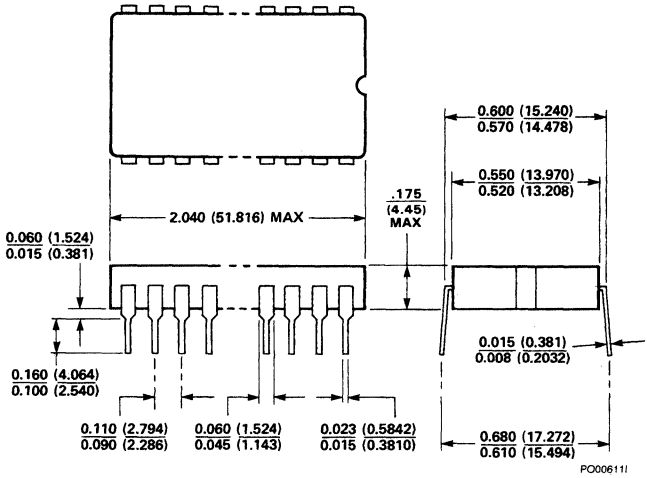


28 LEAD PLASTIC (PI)

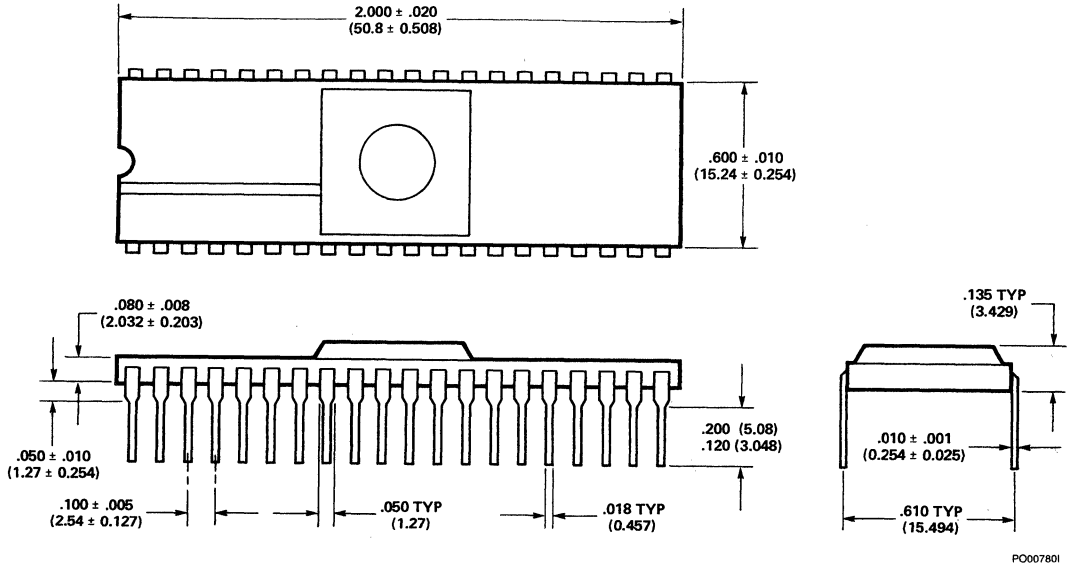


40 LEAD CERAMIC DUAL-IN-LINE (DL)

PACKAGE OUTLINES All dimensions given in inches and (millimeters).



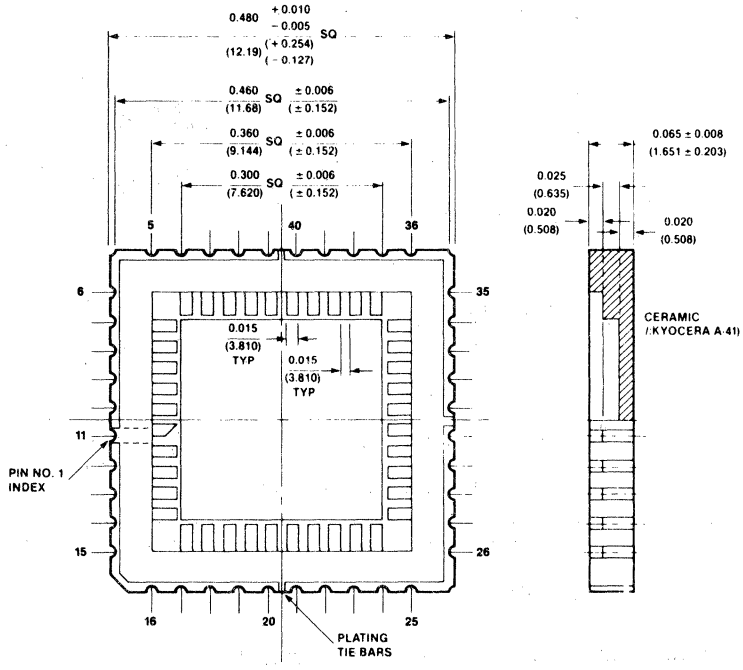
40 LEAD CERDIP (JL)

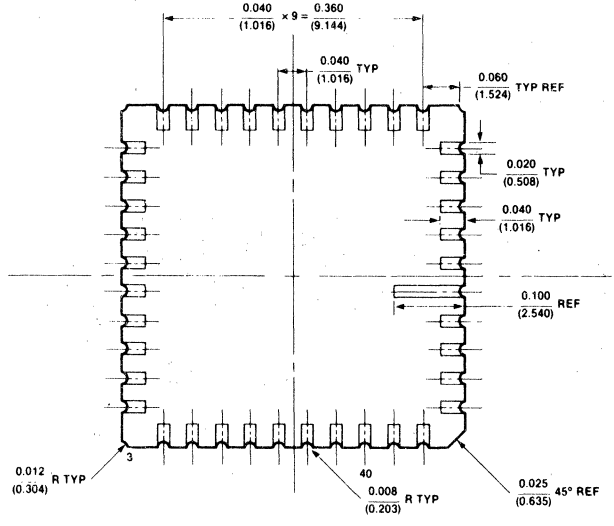


40 LEAD CERDIP WITH WINDOW

10

PACKAGE OUTLINES All dimensions given in inches and (millimeters).

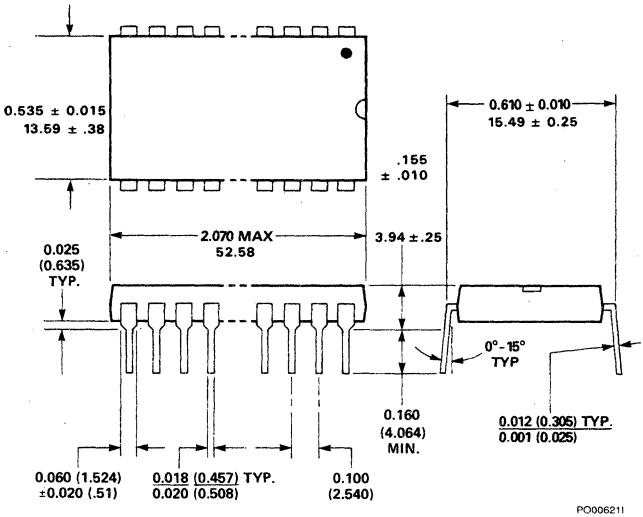




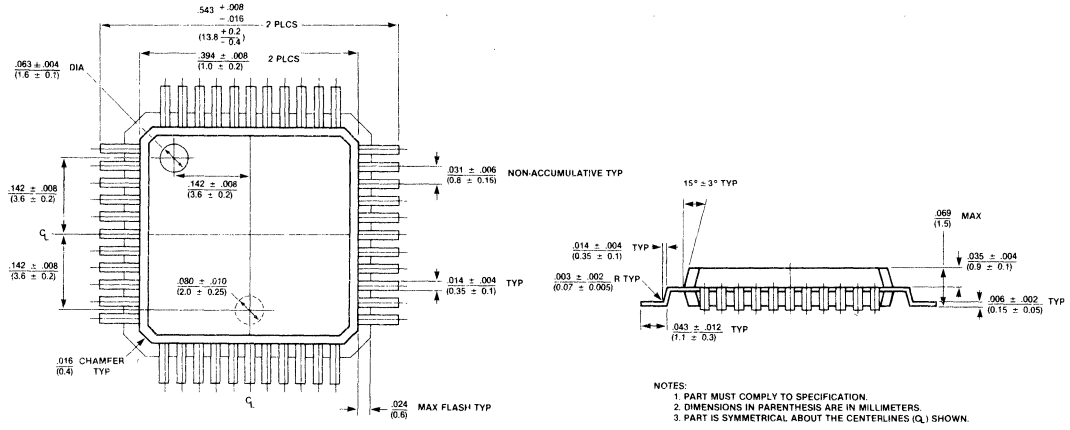
Note 1: Finish: Gold plated 60 micro inches minimum thickness over nickel plated.
Note 2: Pin number 1 connected to die attach pad ground

40 PIN LEADLESS CHIP CARRIER (LL)

PACKAGE OUTLINES All dimensions given in inches and (millimeters).



40 LEAD PLASTIC (PL)

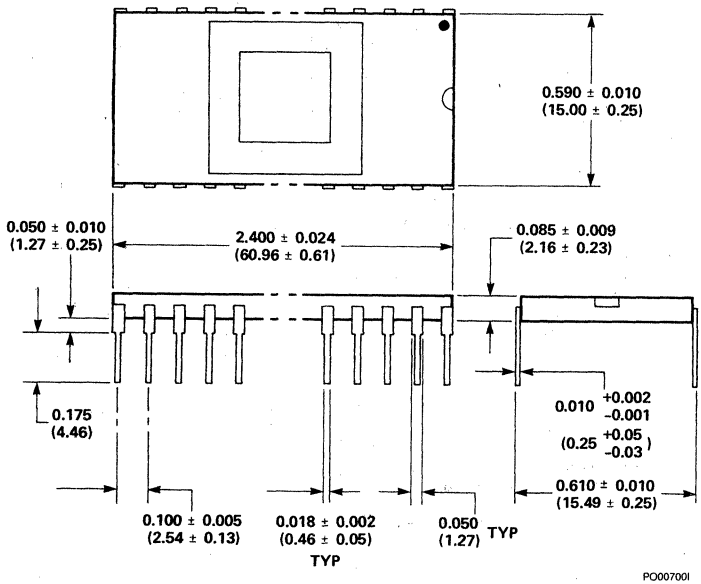


NOTES:
1. PART MUST COMPLY TO SPECIFICATION.
2. DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.
3. PART IS SYMMETRICAL ABOUT THE CENTERLINES ($\mathcal{L}$) SHOWN.

44 LEAD PLASTIC FLATPACK

10

PACKAGE OUTLINES All dimensions given in inches and (millimeters).



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2816 21st Street N.E.,
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Canada L4V 1R2
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Canada K2E 7L5
Tel: (613) 226-1700
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Canada H45 1P8
Tel: (514) 335-1000

Hamilton Avnet Electronics
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Suite 115
Burnaby, B.C.
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Tel: (604) 437-6667

Zentronics
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Tel: (416) 451-9600
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Tel: (403) 272-1021

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General Electric International Operations
Semiconductor Business Division
Chaussee de la Hulpe, 150—Bte. 5
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Belgium
Tel: (2) 673 81 59/660 20 16
TLX: 22004 GEIO B
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Chaussee de la Hulpe, 150—Bte. 5
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Belgium
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FRANCE

General Electric Semiconductor—France
337, Bureaux de la Colline—D8
8 Etage
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France
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General Electric Semiconductor
Via Dei Missaglia, 113/A1
20142 Milano
Italy
Tel: 8229709/10/11 or 8264364
TLX: 331438 CGEHQ1

SPAIN

General Electric Technical Services Co., Inc.
Apartado 700
Juan Bravo 3 C, 4th Floor
Madrid 6
Spain
Tel: 276-7062
TLX: 27650

SWEDEN

International G.E. AB.
Semiconductor Business Division
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S-163 13 Spanga
Sweden
Tel: 8-7939500
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Bavariaring 8, Concordiahaus
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West Germany
Tel: 089-514900
TLX: 5218295 GES M
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FAX: 03-779-1658
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Hong Kong
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GENERAL ELECTRIC (USA) SEMICONDUCTOR K.K.
Meji Seimei Gotanda Bldg., 3rd Fl
2-27-4 Nishi Gotanda
Shinagawa-Ku, Tokyo 141
Japan
Tel: (03) 779-0401
FAX: 03-779-1658
TLX: 2468205 DACADC J

KOREA

G.E. (U.S.A.) Korea Company
10th Floor Hanmi Bldg.
No. 1, Kongpyong-Dong, Chongro-Gu
Seoul 110
Korea
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Turkey
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TLX: 55147 FEC G

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WEST GERMANY

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Dingolfinger Strasse 6
8000 Muenchen 80
West Germany
Tel: 0 89/49/60/01
TLX: 5212931 BIT D

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West Germany
Tel: 0 71 56/2 40 51
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Bitronic GmbH
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West Germany
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TLX: 822 664 BIT D

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Bitronic GmbH
Hanauer Str. 39
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Frankfurt
West Germany
Tel: 06031/9047
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West Germany
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Kreuzbreite 14
3062 Bueckeburg
West Germany
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TLX: 971624 SPEZ D

Spezial-Electronic KG
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7090 Ellwangen
West Germany
Tel: (07) 961 4047
TLX: 74712 SPEZ D

Spezial-Electronic KG
Hanauer Str. 4
6360 Friedberg
West Germany
Tel: (06) 031 4634
TLX: 4184025 SPEZ D

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Intersil, Inc.
10600 Ridgeview Court
Cupertino, CA 95014

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