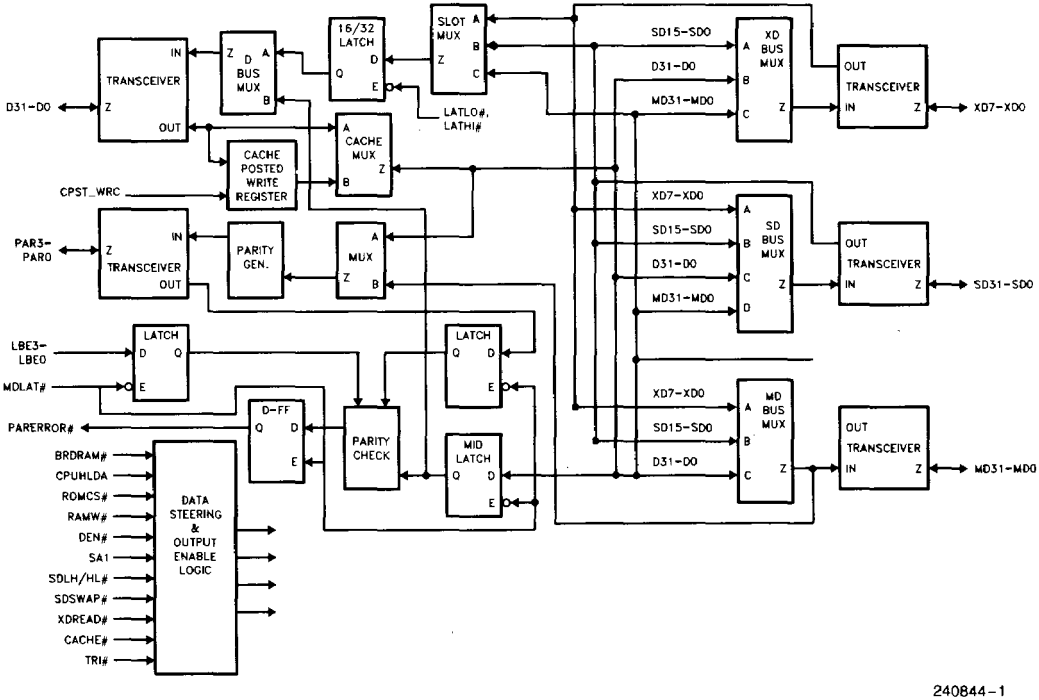
82345
DATA BUFFER

The 82345 Data Buffer is part of a custom, three chip set which allows extremely high performance and integration in 386™ DX processor based, *PC/AT-compatible, personal computer designs. When used with the 82346 System Controller and the 82344 ISA Bus Controller, the set is called the 82340DX chip set.

The 82345 performs all of the data buffering functions required for a 386™ DX-based PC/AT-type system. Under the control of the CPU, the data buffer chip routes data to and from the CPU bus, the MD bus, the XD bus, and the slots (SD bus). For an on-board DRAM read, the data is latched in the MD latch allowing the 82346 System Controller to be programmed for early CAS terminations. The parity is checked for MD bus read operations and any errors are reported during the next read cycle. When reading from ROM, the XD bus or the SD bus, the data can be converted from 8-bits wide to 16-, 24- or 32-bits wide or from 16 bits to 32 bits at the 16/32 latch. The data is latched with LATLO# and LATHI# for synchronization with the CPU. The data conversion is accomplished without the use of the bus size 16 (BS16#) input to the 386DX allowing it to remain in pipelined mode.

CPU writes to any of the three buses are accomplished in several different ways. The 82345 supports posted writes from a cache controller or non-posted writes to the MD bus. Parity is generated for all data written to the MD bus. The 82345 provides the data conversion necessary for 32- or 16-bit writes to 16- or 8-bit devices on the XD or SD buses.



240844-1

Block Diagram

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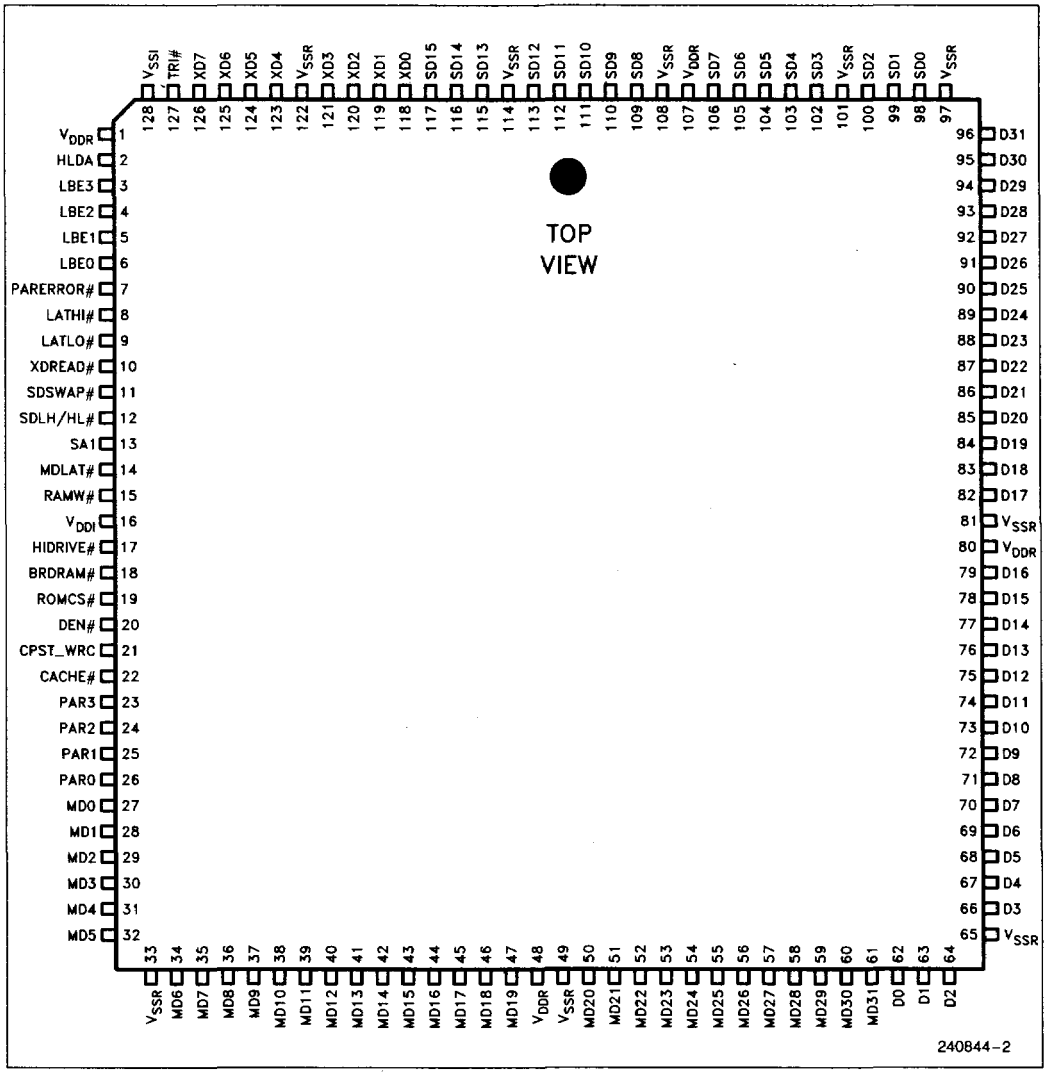
In non-cached systems, system board DRAM can be placed on either the MD bus or the CPU's D bus. In slower systems ($\leq$ 16 MHz) true zero wait state operation is possible with available 60 ns DRAMs when the D bus is used. This is due to the extra timing margin available when the MD bus delay through the 82345 is removed from the critical path. Faster non-cached systems can come close to zero wait state performance using 80 ns to 100 ns DRAMs and page mode interleaving. This requires an even number of DRAM banks.

Under the control of DMA or a bus master, the 82345 will allow 8- or 16-bit data to be routed to and from the XD and the MD buses. The chip also is capable of performing high to low and low to high byte swaps on the SD bus. For transfers between two peripherals on the slot bus, the outputs of the 82345 will be disabled. The chip also provides the feature of a single input, TRI#, to disable all of its outputs for board level testability.

PIN DIAGRAM



SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
CPU INTERFACE			
HLDA	2	I-TTL	**CPU HOLD ACKNOWLEDGE, ACTIVE HIGH:** This is the hold acknowledge pin directly from the CPU. It indicates the CPU has given up the bus for either a DMA master or a slot bus master. It is used in the steering logic to determine data routing.
D31-D0	96-82, 79-66, 64-62	I/O-TTL	**CPU DATA BUS:** This is the data bus directly connected to the CPU. It is also referred to as the local data bus. This bus is output enabled by the DEN# signal.
CACHE INTERFACE			
CPST_WRC	21	I-TPU	**POSTED CACHE WRITE CLOCK:** This clock signal is driven by the cache controller and is needed to latch the write data during a posted cache write cycle. The data is latched on the rising edge of this signal. The latch inside of the Data Buffer is bypassed if the CACHE# input is high. Also, when CACHE# is high, the state of CPST_WRC determines on which bus (D or MD) system DRAM is accessed. When high, DRAM is accessed on the D bus. When low, DRAM is accessed on the MD bus. This pin is pulled up internally.
CACHE#	22	I-TPU	**CACHE ENABLE, ACTIVE LOW:** This signal is used to enable the cache posted write register. When there is not a cache in the system, data bypasses the register. When CACHE# is inactive (high) the state of the CPST_WRC pin determines whether the system DRAM is on the CPU's D bus or on the MD bus. This pin is pulled up internally.
SYSTEM CONTROLLER INTERFACE			
MDLAT#	14	I-TTL	**MEMORY DATA LATCH:** This latching signal serves two purposes simultaneously and is only activated during on-board memory read and write cycles. As a memory data latch, this transparent low signal allows read data to flow through to the CPU's local bus. It follows CAS# on early CAS# high read cycles and on the positive going edge, latches the memory data and holds it for the CPU to sample. As a parity clock, it clocks out PARERROR# on its falling edge an on the rising edge it latches the parity bits (PAR3-PAR0), the byte enables (LBE3-LBE0) and the memory data for parity error processing. Any parity errors will be reported on the next read cycle. It is the negative NOR of all CAS# signals gated by W/R#.
RAMW#	15	I-TTL	**RAM WRITE, ACTIVE LOW:** This signal is supplied by the System Controller to indicate to the Bus Controller that an on-board memory write cycle is occurring. It is used internally to direct the parity logic and to enable the MD bus outputs.
ROMCS#	19	I-TTL	**ROM CHIP SELECT:** This signal tells the Data Buffer when the ROM is to be accessed so that it can latch the data and convert it from 16 or 8 bits to 32 bits. This signal is driven by the System Controller.
BRDRAM#	18	I-TTL	**BOARD MEMORY SELECTED, ACTIVE LOW:** This signal is driven by the System Controller and indicates when on-board DRAM is being accessed.

SIGNAL DESCRIPTIONS (Continued)

Signal Name	Pin Number	Signal Type	Signal Description
SYSTEM CONTROLLER INTERFACE (Continued)			
DEN#	20	I-TTL	**DATA ENABLE, ACTIVE LOW:** This is a control signal generated by the System Controller. It is used to enable data transfers on the local data bus and as an output enable for the D bus.
LBE3–LBE0	3–6	I-TTL	**LATCH BYTE ENABLES 3 THROUGH 0:** These signals are driven by the System Controller. They are used internally to enable the appropriate bytes (in a 4 byte wide memory configuration) for parity generation and checking.
PARERROR#	7	O	**PARITY ERROR, ACTIVE LOW:** This signal is the result of a parity check on the appropriate bytes being read from memory. It is generated on the falling edge of MDLAT#.
BUS CONTROLLER INTERFACE			
SA1	13	I-TTL	**SYSTEM ADDRESS BUS BIT 1:** This input will be driven by the Bus Controller or by the Controlling DMA or bus master. This signal is used for 16- to 32-bit conversion. When low, this signal indicates the low word is to be used.
SDLH/HL#	12	I-TTL	**SYSTEM DATA BUS LOW TO HIGH/HIGH TO LOW SWAP:** This signal is driven by the Bus Controller. It is used to establish the direction of byte swaps. (Similar to DIR245 in the existing PC/AT-type chip sets).
SDSWAP#	11	I-TTL	**SYSTEM DATA BUS BYTE SWAP ENABLE, ACTIVE LOW:** This signal is driven by the Bus Controller. It is the qualifying signal needed for SDLH/HL#. (It was formerly named GATE245 on the existing PC/AT-type chip sets).
XDREAD#	10	I-TTL	**PERIPHERAL DATA BUS (XD BUS) READ, ACTIVE LOW:** This signal is driven by the Bus Controller and it determines the direction of the XD bus data flow. (It is analogous to the XDATADIR control pin on the existing PC/AT-type chip sets). When this signal is high, the XD Bus is output enabled.
LATHI#	8	I-TTL	**SD BUS HIGH BYTE LATCH:** This signal is needed to latch the SD bus' high byte to the local data bus until the CPU is ready to sample the bus. When SA1 is low, the high byte is latched into both the one byte and the three byte of the 16/32 latch. When SA1 is high, the high byte is only latched into the three byte. This signal is driven by the Bus Controller.
LATLO#	9	I-TTL	**SD BUS LOW BYTE LATCH:** This signal is needed to latch the SD bus' low byte to the local data bus until the CPU is ready to sample the bus. When SA1 is low, the low byte is latched into both the zero byte and the two byte of the 16/32 latch. When SA1 is high, the high byte is only latched into the two byte. This signal is driven by the Bus Controller.
BUFFER INTERFACE			
MD31–MD0	61–50, 47–34, 32–27	I/O-TTL	**MEMORY DATA BUS:** This bus connects to the on-board DRAM and BIOS ROM. It is used to transfer data to/from memory during memory write/read bus cycles.
SD15–SD0	117–115, 103–109, 106–102, 100–98	I/O-TTL	**SYSTEM DATA BUS:** This bus connects directly to the slots. It is used to transfer data to/from local and system devices.

SIGNAL DESCRIPTIONS (Continued)

Signal Name	Pin Number	Signal Type	Signal Description
BUFFER INTERFACE (Continued)			
XD7–XD0	126–123 121–118	I/O-TTL	**PERIPHERAL DATA BUS:** This bus is connected to the Bus Controller and the System Controller. These I/O's are used to read and write to on-board 8-bit peripherals.
PAR3–PAR0	23–26	I/O-TTL	**PARITY BIT BYTES 3 THROUGH 0:** These bits are generated by the parity generation circuitry located on the Data Buffer chip. They are written to memory along with their corresponding bytes during memory write operations. During memory read operations, these bits become inputs and are used along with their respective data bytes to determine if a parity error has occurred. The generation and check of each bit is enabled only when their respective LBE3–LBE0 bits are active.
HIDRIVE#	17	I-TPU	**HIGH DRIVE ENABLE:** This pin is intended to be a wire option. When this pin is low, all bus drivers defined with an I_{OL} of 24 mA will sink the full 24 mA of current. When the input is high, all pins defined as 24 mA will have the output low drive capability cut in half to 12 mA. Note that al A.C. specifications are done with the outputs in the high drive mode and a 200 pF capacitive load. HIDRIVE# has an internal pull-up and can be left unconnected in 12 mA drive if desired. It should be tied low if 24 mA drive is desired.
TEST MODE PIN			
TRI#	127	I-TPU	**THREE-STATE:** This pin is used to drive all outputs to a high impedance state. When TRI# is low, all outputs and bidirectional pins are three-stated. This pin should be pulled up via a 10 kΩ pull-up resistor in a standard system configuration.
POWER BUS CONNECTION The power connections are split into an internal supply for the core-logic, and a pad-ring supply for the I/O drivers. Each supply should be individually bypassed with decoupling capacitors.			
V_{DDR}	1, 48, 80, 107	PWR	**PAD-RING POWER CONNECTION NOMINALLY +5V:** These pins along with the V_{SSR} pins should be separately bypassed.
V_{SSR}	33, 49, 65, 81, 97, 101, 108, 114, 122	GND	**PAD-RING GROUND CONNECTION, NOMINALLY 0V:** These pins along with the V_{DDR} pins should be separately bypassed.
V_{DDI}	16	PWR	**INTERNAL CORE-LOGIC POWER CONNECTION, NOMINALLY +5V:** This pin along with the V_{SSI} pin should be separately bypassed.
V_{SSI}	128	GND	**INTERNAL CORE-LOGIC GROUND CONNECTION, NOMINALLY 0V:** This pin along with the V_{DDI} pin should be separately bypassed.

SIGNAL TYPE LEGEND

Signal Code	Signal Type
I-TTL	TTL Level Input
I-TPD	Input with 30 kΩ Pull-Down Resistor
I-TPU	Input with 30 kΩ Pull-Up Resistor
I-TSPU	Schmitt-Trigger Input with 30 kΩ Pull-Up Resistor
I-CMOS	CMOS Level Input
I/O-TTL	TTL Level Input/Output
IT-OD	TTL Level Input/Open Drain Output
I/O-OD	Input or Open Drain, Slow Turn On
O	CMOS and TTL Level Compatible Output
O-TTL	TTL Level Output
O-TS	Three-State Level Output
I1	Input Used for Testing Purposes
GND	Ground
PWR	Power