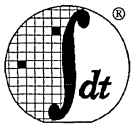
1991 DATABOOK

Update 1

Integrated Device Technology, Inc.



Integrated Device Technology, Inc.

1991
DATA BOOK UPDATE 1

2975 Stender Way, Santa Clara, California 95054
Telephone: (408) 727-6116 • FAX: (408) 492-8674
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CONTENTS OVERVIEW

Historically, Integrated Device Technology has presented its product offerings entirely under one cover. In an effort to simplify this information for our customers, it has been divided into four separate data books — Logic, Specialized Memory, RISC and Static RAM.

This 1991 Update offers new and revised information from each of the four 1991 Data Books. Also included is a current, complete packaging section for all IDT product groups. This section will be updated in each subsequent data book.

The Table of Contents contains a listing of the products in the Update. All data sheets are designated by their corresponding Data Book (A = Logic, B = Specialized Memories, C = RISC, and D = Static RAM) and page numbered individually. For example, *Updated 1 C*, centered at the bottom of the page, refers to the 1991 RISC Data Book. The corresponding page number is shown in the lower right corner. New data sheets and application notes follow the partial and complete data sheets in the section with the data book that they will appear in when next published.

A header bar at the top of each change to a partial or complete data sheet indicates which 1990-91 data book the original data sheet can be found in. The reference is organized by data book, section and page number.

IDT, a recognized leader in high-speed CMOS technology, produces a broad line of products. This enables us to provide a complete CMOS solution to designers of high performance digital systems. Not only do our product lines include industry standard devices, they also feature products with faster speed, lower power, and package and/or architectural benefits that allow the designer to achieve significantly improved system performance.

To find ordering information: Start with the Ordering Information chart at the back of each **new** data sheet. Updated data sheets — for which only the updated information has been included — should be used in reference with the complete data sheet in the appropriate 1991 Data Book.

To find product data: Start with the Table of Contents, organized by data book (data books are organized with partially updated data sheets at the front, followed by updated full data sheets, then new data sheets) or with the numeric Table of Contents organized across all product lines. These indexes will direct you to the page(s) of the partial, full or new data sheet. Included in the update sections is a header bar above the change which has a reference for locating the complete data sheet in the appropriate 1991 Data Book. Data sheets may be of the following type:

ADVANCE INFORMATION — contain initial descriptions, subject to change, for products that are in development, including features and block diagrams.

PRELIMINARY — contain descriptions for products soon to be, or recently, released to production, including features, pinouts and block diagrams. Timing data are based on simulation or initial characterization and are subject to change upon full characterization.

FINAL — contain minimum and maximum limits specified over the complete supply and temperature range for full production devices.

New products, product performance enhancements, additional package types and new product families are being introduced frequently. Although this update is published in an effort to keep our customers informed of new and changing data, it is impossible for it to remain current. Please contact your local IDT sales representative to determine the latest device specifications, package types and product availability.

LIFE SUPPORT POLICY

Integrated Device Technology's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the manufacturer and an officer of IDT.

1. **Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.**
2. **A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.**

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TABLE OF CONTENTS

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1990/91 SPECIALIZED MEMORIES DATA BOOK UPDATES (Continued)

NEW DATA SHEETS AND APPLICATION NOTES

NUMERICAL TABLE OF CONTENTS

Please refer to your 1990/91 data book for current information. This section has not changed.

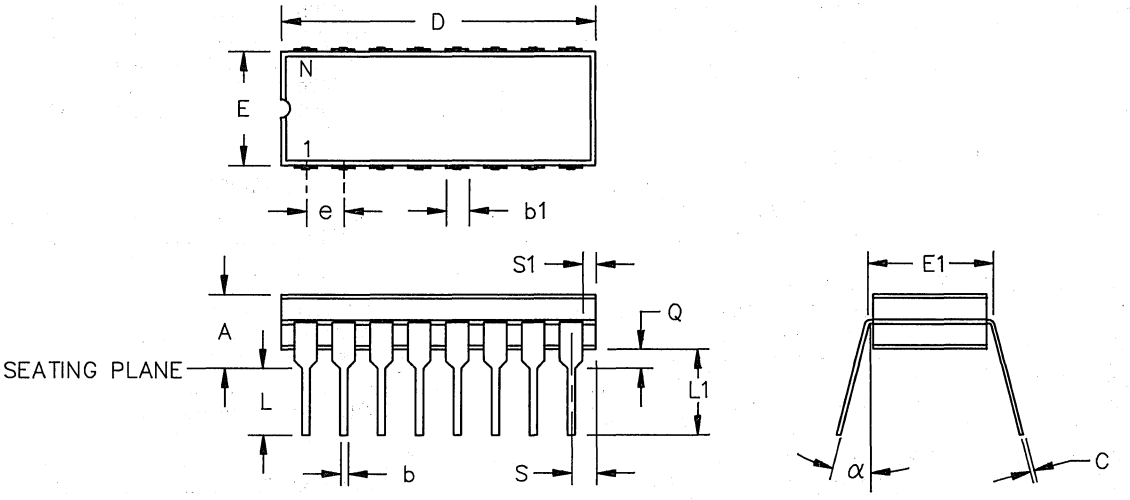
Please refer to your 1990/91 data book for current information. This section has not changed.

PACKAGE DIAGRAM OUTLINE INDEX

Integrated Device Technology, Inc.

PACKAGE DIAGRAM OUTLINES

DUAL IN-LINE PACKAGES



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. THE MINIMUM LIMIT FOR DIMENSION b1 MAY BE .023 FOR CORNER LEADS.

16-28 LEAD CERDIP (300 MIL)

DWG #	D16-1		D18-1		D20-1		D22-1		D24-1		D28-3	
# OF LDS (N)	16		18		20		22		24		28	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.200	.140	.200	.140	.200	.140	.200	.140	.200	.140	.200
b	.015	.021	.015	.021	.015	.021	.015	.021	.015	.021	.015	.021
b1	.038	.060	.038	.060	.038	.060	.045	.060	.045	.065	.045	.065
C	.009	.012	.009	.012	.009	.012	.009	.012	.009	.014	.009	.014
D	.750	.830	.880	.930	.935	1.060	1.050	1.080	1.240	1.280	1.440	1.485
E	.285	.310	.285	.310	.285	.310	.285	.310	.285	.310	.285	.310
E1	.290	.320	.290	.320	.290	.320	.300	.320	.300	.320	.300	.320
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC	
L	.125	.175	.125	.175	.125	.175	.125	.175	.125	.175	.125	.175
L1	.150	–	.150	–	.150	–	.150	–	.150	–	.150	–
Q	.015	.055	.015	.055	.015	.060	.015	.060	.015	.060	.015	.060
S	.020	.080	.020	.080	.020	.080	.020	.080	.030	.080	.030	.080
S1	.005	–	.005	–	.005	–	.005	–	.005	–	.005	–
α	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°

DUAL IN-LINE PACKAGES (Continued)

24-40 LEAD CERDIP (400 & 600 MIL)

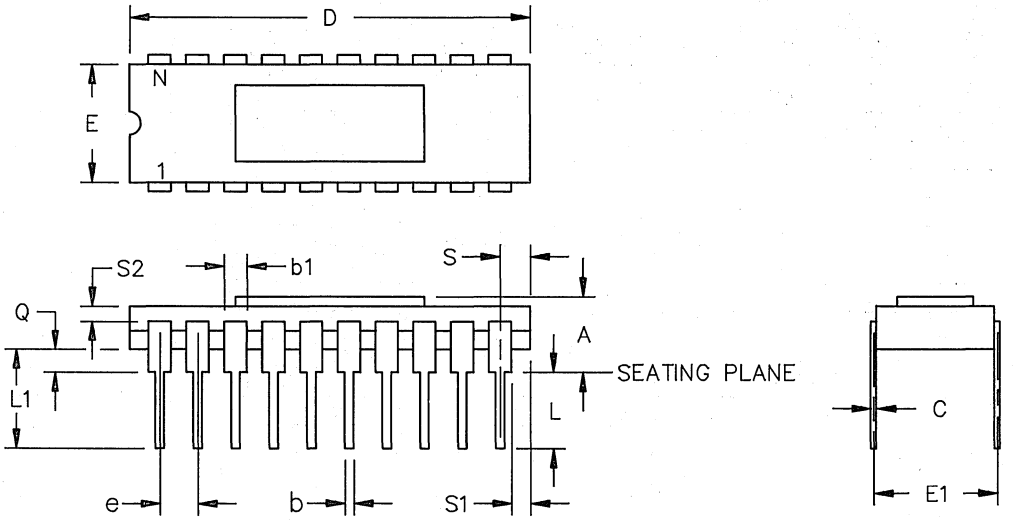
DWG #	D24-3		D24-2		D28-1		D40-1	
# OF LDS (N)	24		24		28		40	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.130	.175	.090	.190	.090	.200	.160	.220
b	.015	.021	.014	.023	.014	.023	.014	.023
b1	.045	.065	.038	.060	.038	.065	.038	.065
C	.009	.014	.008	.012	.008	.014	.008	.014
D	1.180	1.250	1.230	1.290	1.440	1.490	2.020	2.070
E	.350	.410	.500	.610	.510	.545	.510	.545
E1	.380	.420	.590	.620	.590	.620	.590	.620
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC	
L	.125	.175	.125	.200	.125	.200	.125	.200
L1	.150	–	.150	–	.150	–	.150	–
Q	.015	.060	.015	.060	.020	.060	.020	.060
S	.030	.070	.030	.080	.030	.080	.030	.080
S1	.005	–	.005	–	.005	–	.005	–
α	0°	15°	0°	15°	0°	15°	0°	15°

28-40 LEAD CERDIP (WIDE BODY)

DWG #	D28-2		D32-1		D40-2	
# OF LDS (N)	28		32		40	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.120	.210	.160	.220
b	.014	.023	.014	.023	.014	.023
b1	.038	.065	.038	.065	.038	.065
C	.008	.014	.008	.014	.008	.014
D	1.440	1.490	1.625	1.675	2.020	2.070
E	.570	.600	.570	.600	.570	.600
E1	.590	.620	.590	.620	.590	.620
e	.100 BSC		.100 BSC		.100 BSC	
L	.125	.200	.125	.200	.125	.200
L1	.150	–	.150	–	.150	–
Q	.020	.060	.020	.060	.020	.060
S	.030	.080	.030	.080	.030	.080
S1	.005	–	.005	–	.005	–
α	0°	15°	0°	15°	0°	15°

DUAL IN–LINE PACKAGES (Continued)

20–32 LEAD SIDE BRAZE (300 MIL)

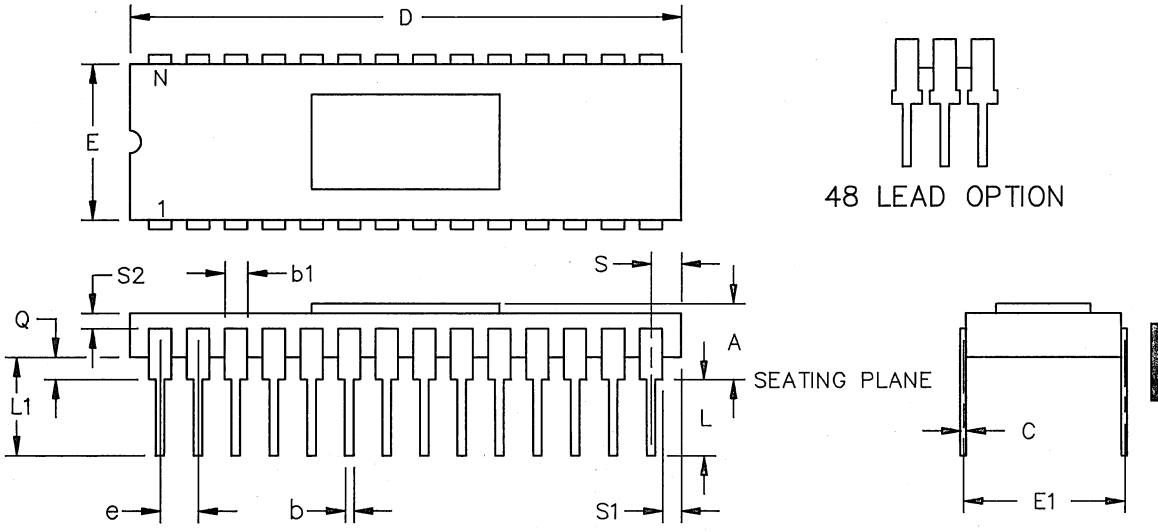


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C20–1		C22–1		C24–1		C28–1		C32–3	
# OF LDS (N)	20		22		24		28		32	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.100	.200	.090	.200	.090	.200	.090	.200
b	.014	.023	.014	.023	.015	.023	.014	.023	.014	.023
b1	.040	.060	.038	.060	.040	.060	.040	.060	.040	.060
C	.008	.015	.008	.015	.008	.015	.008	.015	.008	.014
D	.970	1.060	1.040	1.120	1.180	1.230	1.380	1.420	1.580	1.640
E	.260	.310	.260	.310	.220	.310	.220	.310	.280	.310
E1	.290	.320	.290	.320	.290	.320	.290	.320	.290	.320
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC	
L	.125	.200	.125	.200	.125	.200	.125	.200	.100	.175
L1	.150	–	.150	–	.150	–	.150	–	.150	–
Q	.015	.060	.015	.060	.015	.060	.015	.060	.030	.060
S	.030	.065	.030	.065	.030	.065	.030	.065	.030	.065
S1	.005	–	.005	–	.005	–	.005	–	.005	–
S2	.005	–	.005	–	.005	–	.005	–	.005	–

DUAL IN-LINE PACKAGES (Continued)

28-48 LEAD SIDE BRAZE (400 MIL)

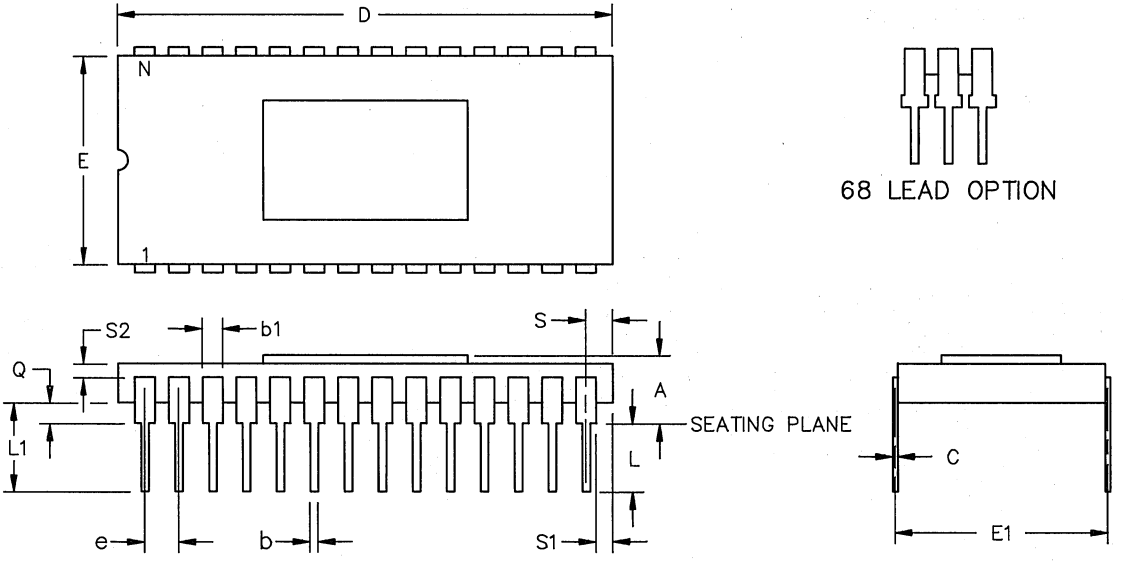


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C28-2		C32-2		C48-1	
# OF LDS (N)	28		32		48	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.090	.200	.085	.190
b	.014	.023	.014	.023	.014	.023
b1	.040	.060	.040	.060	.040	.060
C	.008	.014	.008	.014	.008	.014
D	1.380	1.420	1.580	1.640	1.690	1.730
E	.380	.420	.380	.410	.380	.410
E1	.390	.420	.390	.420	.390	.420
e	.100 BSC		.100 BSC		.070 BSC	
L	.100	.175	.100	.175	.125	.175
L1	.150	–	.150	–	.150	–
Q	.030	.060	.030	.060	.020	.070
S	.030	.065	.030	.065	.030	.065
S1	.005	–	.005	–	.005	–
S2	.005	–	.005	–	.005	–

DUAL IN-LINE PACKAGES (Continued)

24-68 LEAD SIDE BRAZE (600 MIL)

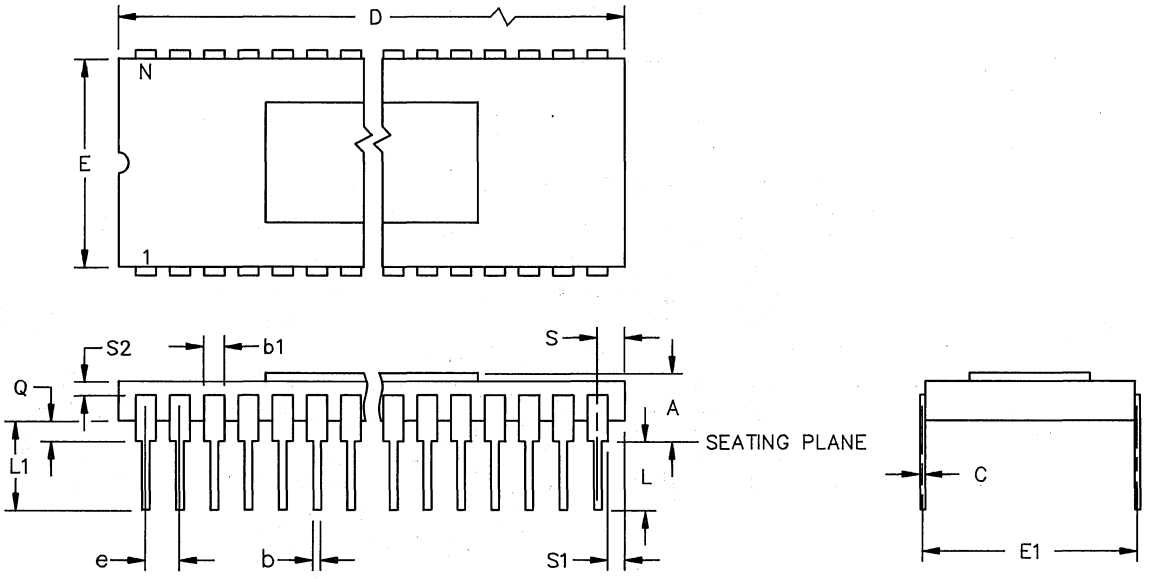


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C24-2		C28-3		C32-1		C40-1		C48-2		C68-1	
# OF LDS (N)	24		28		32		40		48		68	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.190	.085	.190	.100	.190	.085	.190	.100	.190	.085	.190
b	.015	.023	.015	.022	.015	.023	.015	.023	.015	.023	.015	.023
b1	.040	.060	.038	.060	.040	.060	.038	.060	.040	.060	.040	.060
C	.008	.012	.008	.012	.008	.014	.008	.012	.008	.012	.008	.012
D	1.180	1.220	1.380	1.430	1.580	1.640	1.980	2.030	2.370	2.430	2.380	2.440
E	.575	.610	.580	.610	.580	.610	.580	.610	.550	.610	.580	.610
E1	.595	.620	.595	.620	.590	.620	.595	.620	.595	.620	.590	.620
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC		.070 BSC	
L	.125	.175	.125	.175	.100	.175	.125	.175	.125	.175	.125	.175
L1	.150	–	.150	–	.150	–	.150	–	.150	–	.150	–
Q	.020	.060	.020	.060	.020	.060	.020	.060	.020	.060	.020	.070
S	.030	.065	.030	.065	.030	.065	.030	.065	.030	.065	.030	.065
S1	.005	–	.005	–	.005	–	.005	–	.005	–	.005	–
S2	.005	–	.005	–	.005	–	.005	–	.005	–	.005	–

DUAL IN-LINE PACKAGES (Continued)

64 LEAD SIDE BRAZE (900 MIL)

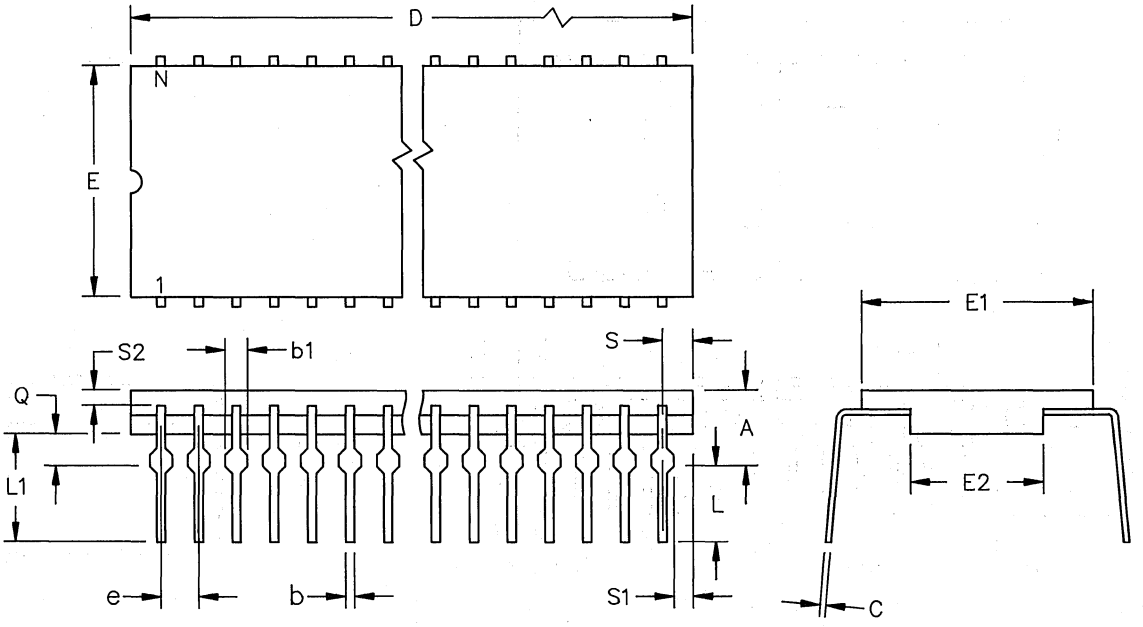


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C64-1	
# OF LDS (N)	64	
SYMBOL	MIN	MAX
A	.110	.190
b	.014	.023
b1	.040	.060
C	.008	.015
D	3.160	3.240
E	.884	.915
E1	.890	.920
e	.100 BSC	
L	.125	.200
L1	.150	–
Q	.015	.070
S	.030	.065
S1	.005	–
S2	.005	–

DUAL IN-LINE PACKAGES (Continued)

64 LEAD TOP BRAZE (900 MIL)

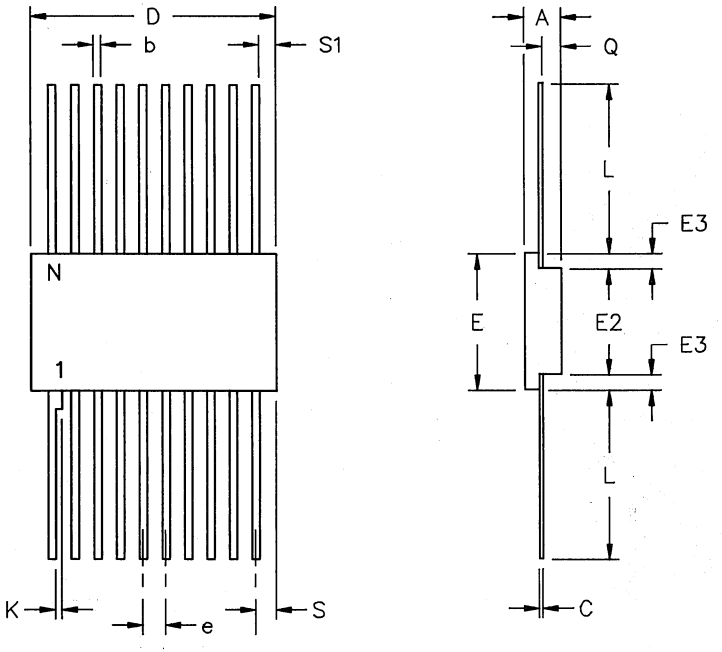


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C64-2	
# OF LDS (N)	64	
SYMBOL	MIN	MAX
A	.120	.180
b	.015	.021
b1	.040	.060
C	.009	.012
D	3.170	3.240
E	.790	.810
E1	.880	.915
E2	.640	.660
e	.100 BSC	
L	.125	.160
L1	.150	–
Q	.020	.100
S	.030	.065
S1	.005	–
S2	.005	–

FLATPACKS

20–28 LEAD FLATPACK

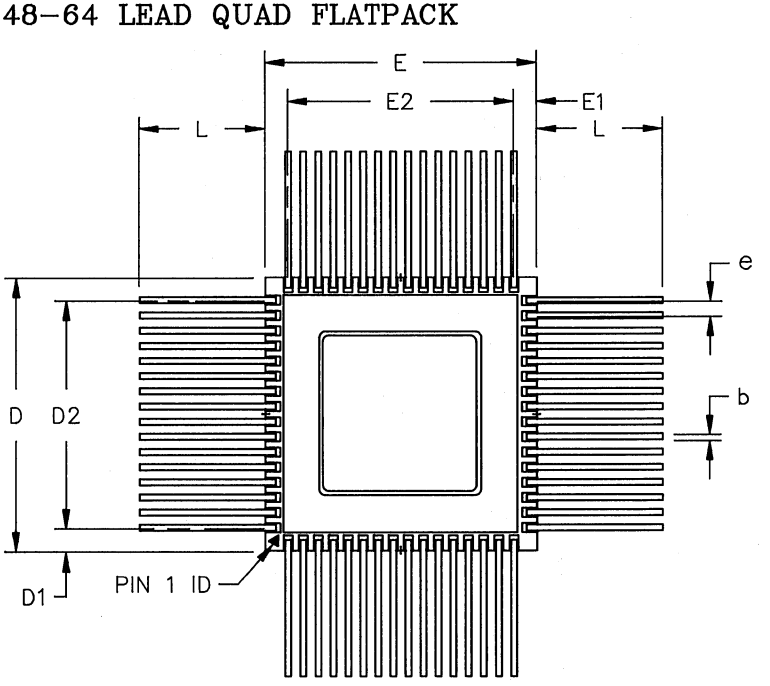


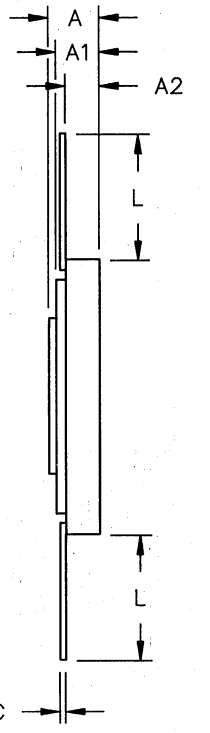
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	F20–1		F20–2		F24–1		F28–1		F28–2	
# OF LDS (N)	20		20 (.295 BODY)		24		28		28	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.045	.092	.045	.092	.045	.090	.045	.090	.045	.115
b	.015	.019	.015	.019	.015	.019	.015	.019	.015	.019
C	.003	.006	.003	.006	.003	.006	.004	.007	.003	.007
D	–	.540	–	.540	–	.640	.710	.740	.710	.740
E	.340	.360	.245	.303	.360	.420	.480	.520	.480	.520
E2	.130	–	.130	–	.180	–	.180	–	.180	–
E3	.030	–	.030	–	.030	–	.040	–	.040	–
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
K	.006	.015	.008	.015	–	–	–	–	–	–
L	.250	.370	.250	.370	.250	.370	.250	.370	.250	.370
Q	.010	.040	.010	.040	.010	.040	.010	.045	.026	.045
S	–	.045	–	.045	–	.045	–	.045	–	.045
S1	.000	–	.005	–	.005	–	.005	–	.005	–

FLATPACKS (Continued)

48–64 LEAD QUAD FLATPACK



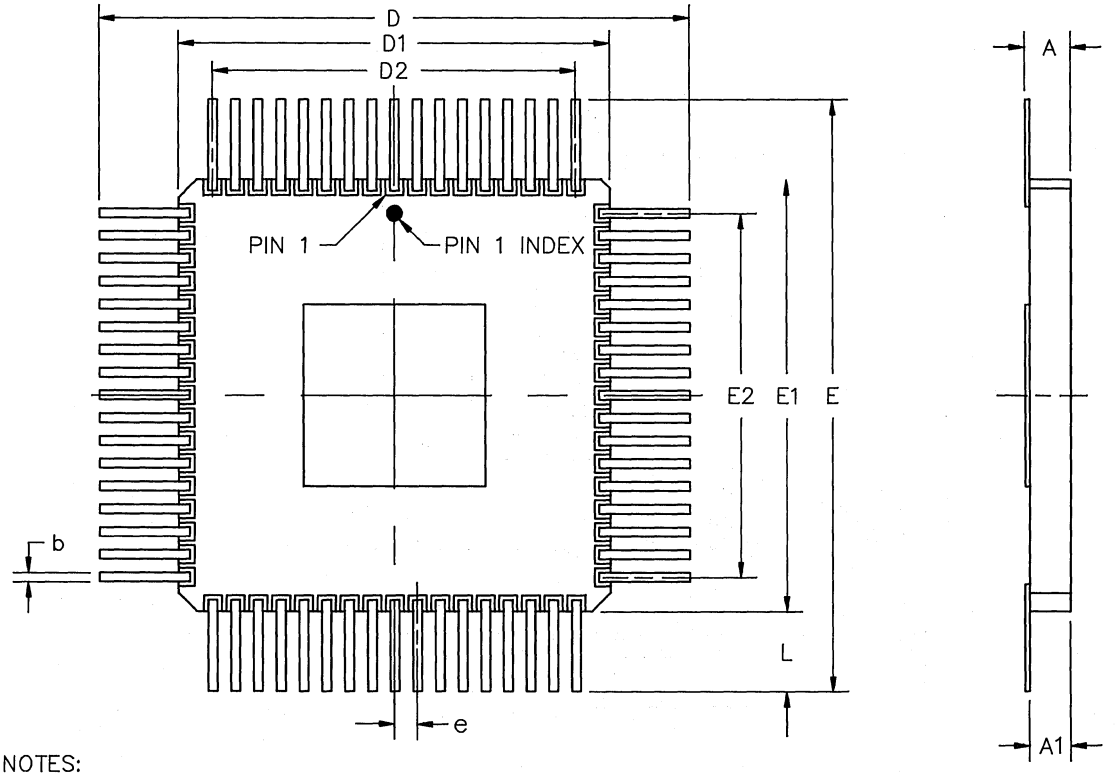


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	F48–1		F64–1	
# OF LDS (N)	48		64	
SYMBOL	MIN	MAX	MIN	MAX
A	.089	.108	.070	.090
A1	.079	.096	.060	.078
A2	.058	.073	.030	.045
b	.018	.022	.016	.020
C	.008	.010	.009	.012
D/E	–	.750	.885	.915
D1/E1	.100 REF		.075 REF	
D2/E2	.550 BSC		.750 BSC	
e	.050 BSC		.050 BSC	
L	.350	.450	.350	.450
ND/NE	12		16	

FLATPACKS (Continued)

68 LEAD QUAD FLATPACK

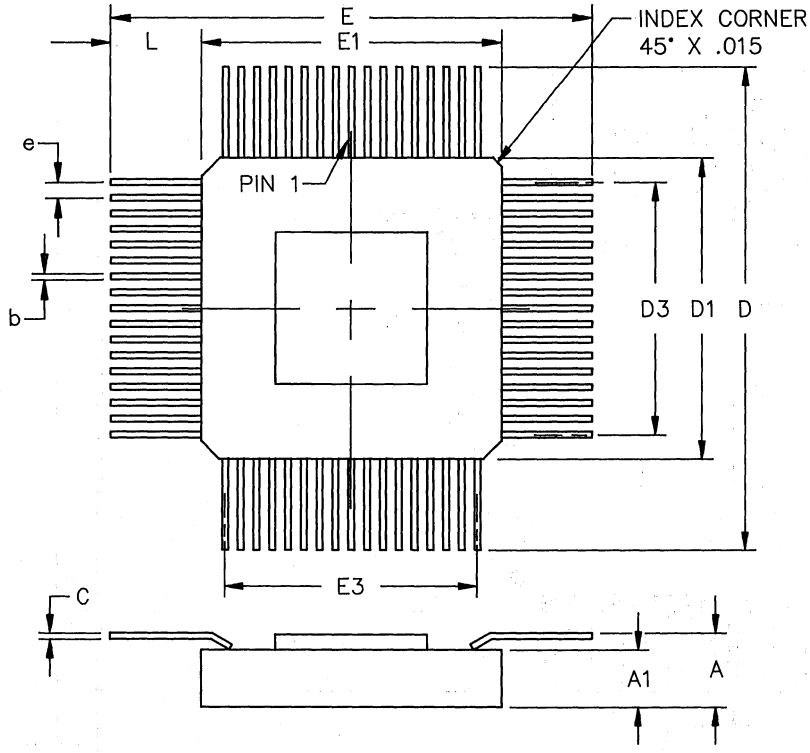


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	F68–1	
# OF LDS (N)	68	
SYMBOL	MIN	MAX
A	.080	.145
A1	.070	.090
b	.014	.021
C	.008	.012
D/E	1.640	1.870
D1/E1	.926	.970
D2/E2	.800 BSC	
e	.050 BSC	
L	.350	.450
ND/NE	17	

FLATPACKS (Continued)

68 LEAD QUAD FLATPACK (FINE PITCH)

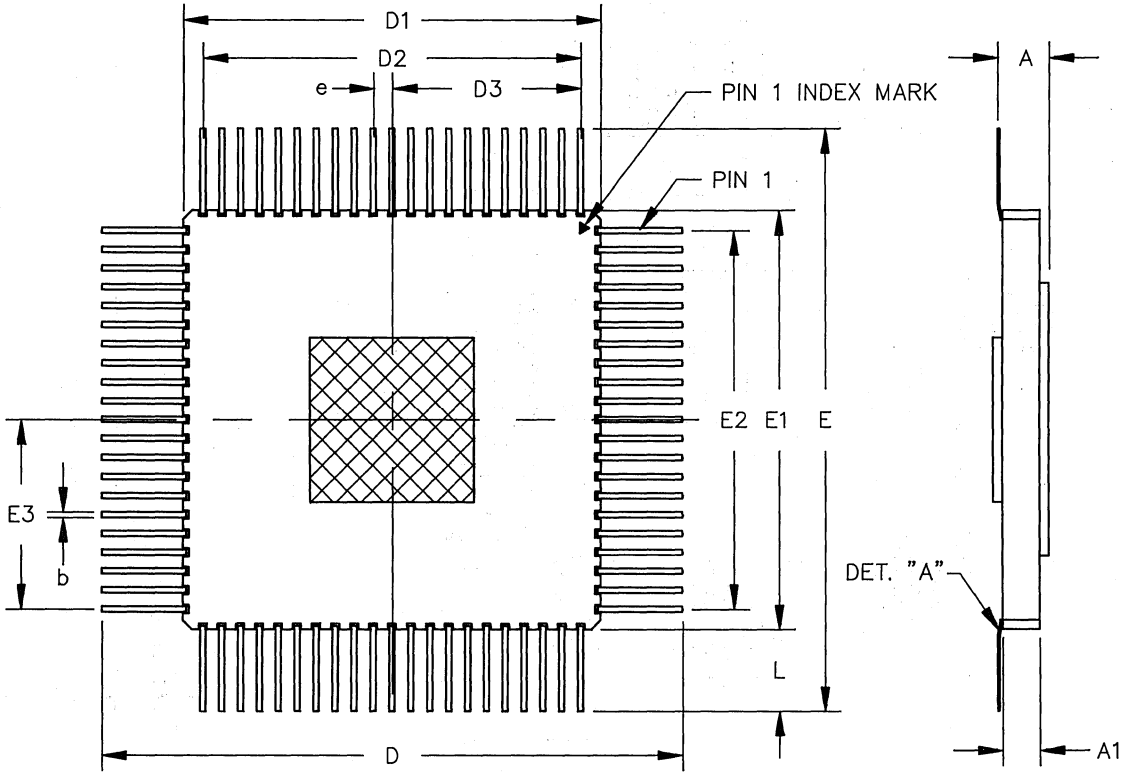


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	F68–2	
# OF LDS (N)	68	
SYMBOL	MIN	MAX
A	.064	.084
A1	.054	.070
b	.008	.013
C	.0045	.008
D/E	.860	1.100
D1/E1	.460	.500
D2/E2	.400 REF	
e	.025 BSC	
L	.200	.300
ND/NE	17	

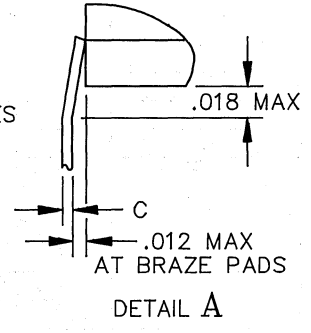
FLATPACKS (Continued)

84 LEAD QUAD FLATPACK (CAVITY DOWN)



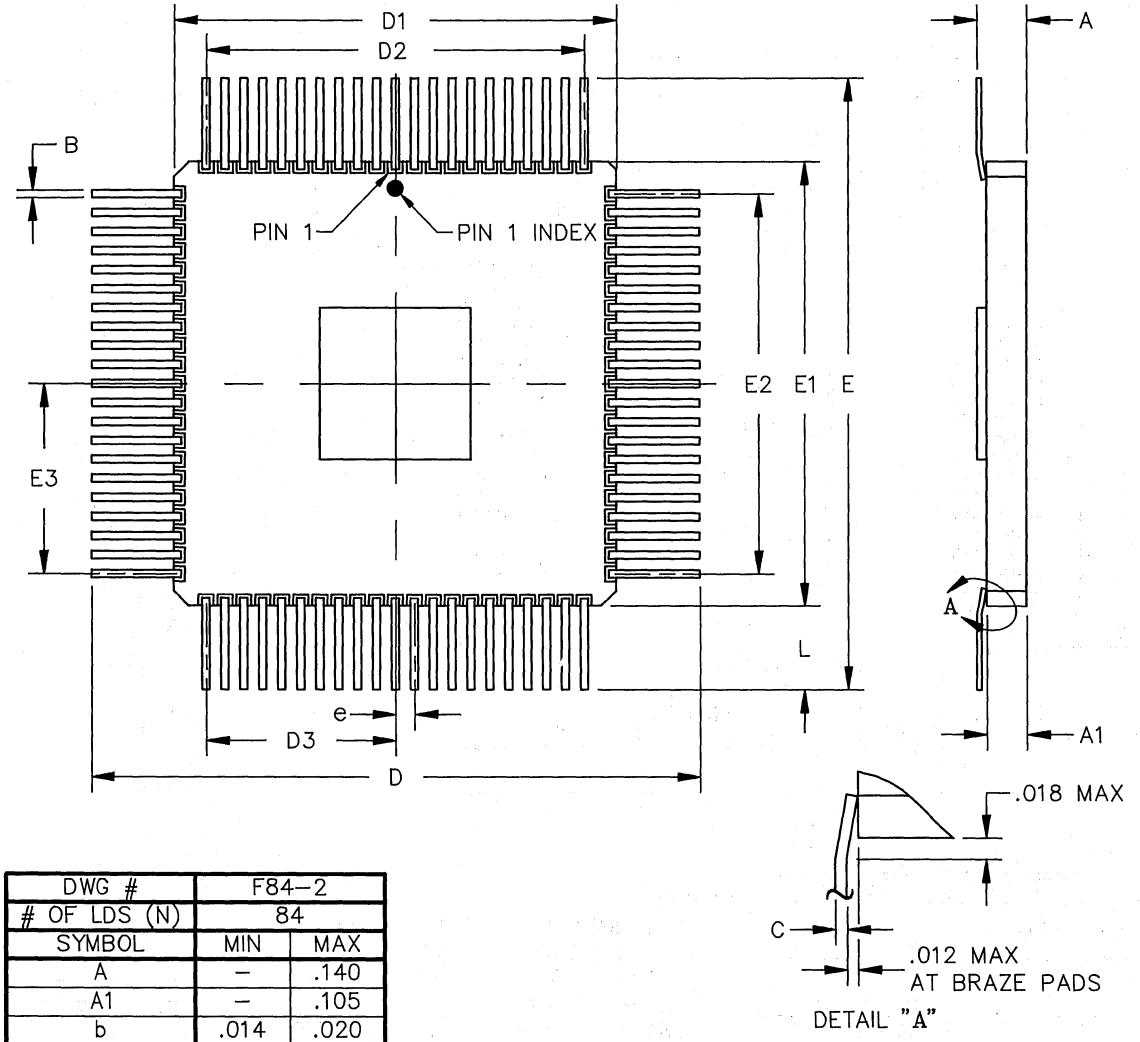
DWG #	F84-1	
# OF LDS (N)	84	
SYMBOL	MIN	MAX
A	–	.140
A1	–	.105
b	.014	.020
C	.007	.013
D/E	1.485	1.615
D1/E1	1.130	1.170
D2/E2	1.000 BSC	
D3/E3	.500 BSC	
e	.050 BSC	
L	.350	.450
ND/NE	21	

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. CROSS HATCHED AREA INDICATES INTEGRAL METALLIC HEAT SINK.



FLATPACKS (Continued)

84 LEAD QUAD FLATPACK (CAVITY UP)

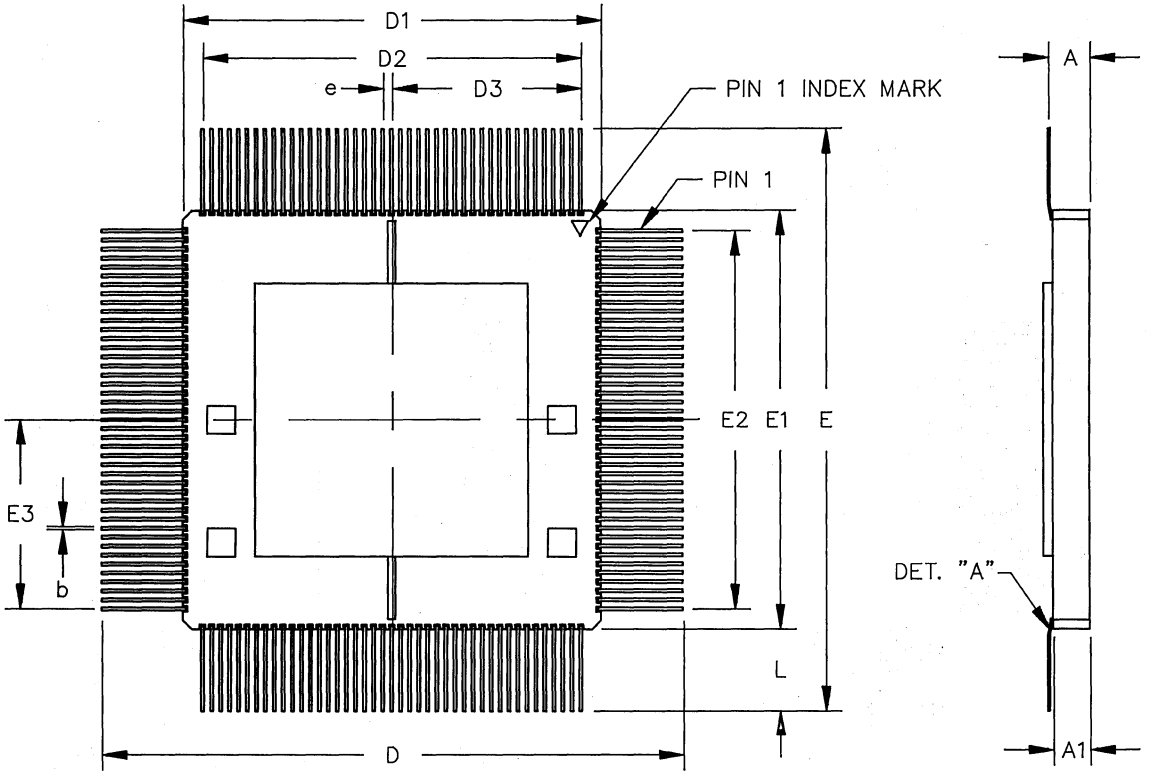


DWG #	F84-2	
# OF LDS (N)	84	
SYMBOL	MIN	MAX
A	–	.140
A1	–	.105
b	.014	.020
C	.007	.013
D/E	1.485	1.615
D1/E1	1.130	1.170
D2/E2	1.000 BSC	
D3/E3	.500 BSC	
e	.050 BSC	
L	.350	.450
ND/NE	21	

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

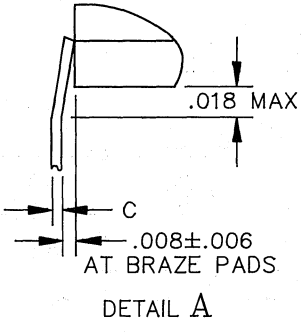
FLATPACKS (Continued)

172 LEAD QUAD FLATPACK (CAVITY UP – R3001)



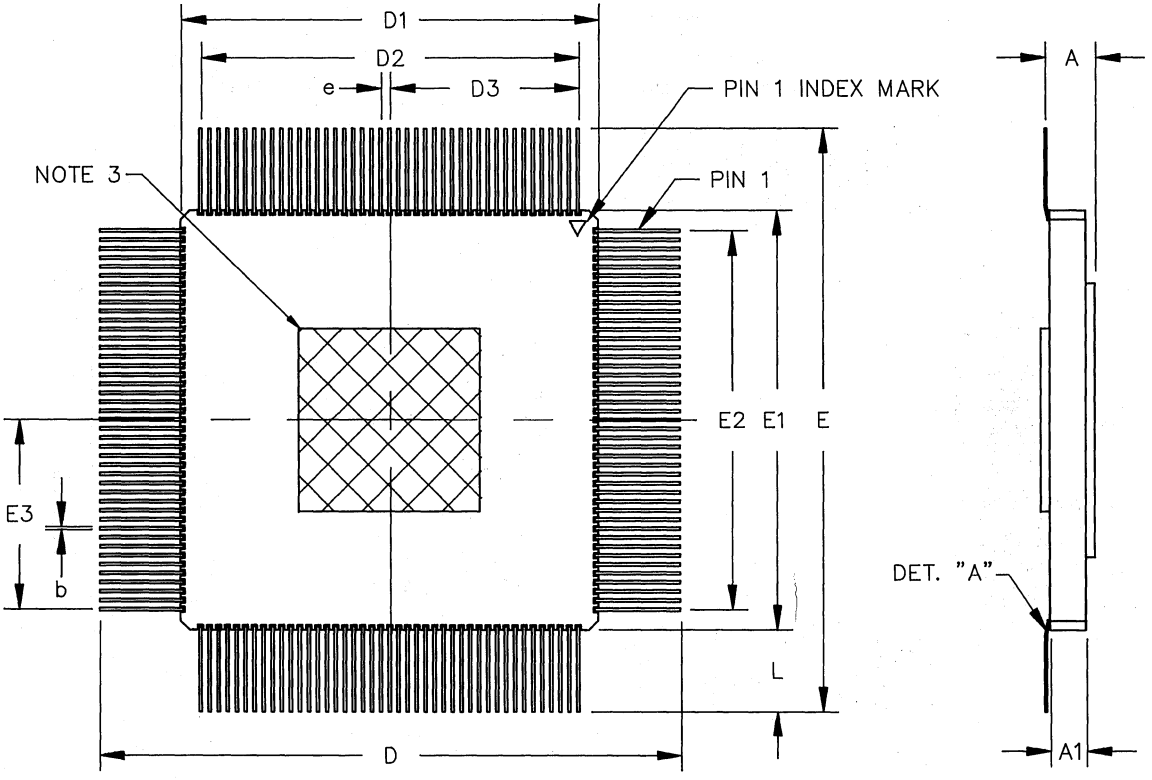
DWG #	F172-1	
# OF LDS (N)	172	
SYMBOL	MIN	MAX
A	–	.130
A1	–	.105
b	.006	.010
C	.004	.008
D/E	1.580	1.620
D1/E1	1.135	1.165
D2/E2	1.050 BSC	
D3/E3	.525 BSC	
e	.025 BSC	
L	.220	.230
ND/NE	43	

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.



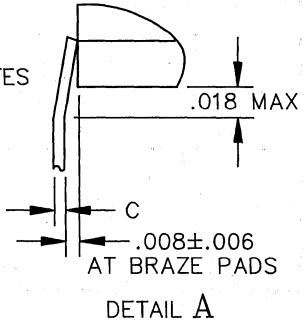
FLATPACKS (Continued)

172 LEAD QUAD FLATPACK (CAVITY DOWN – R3000A)



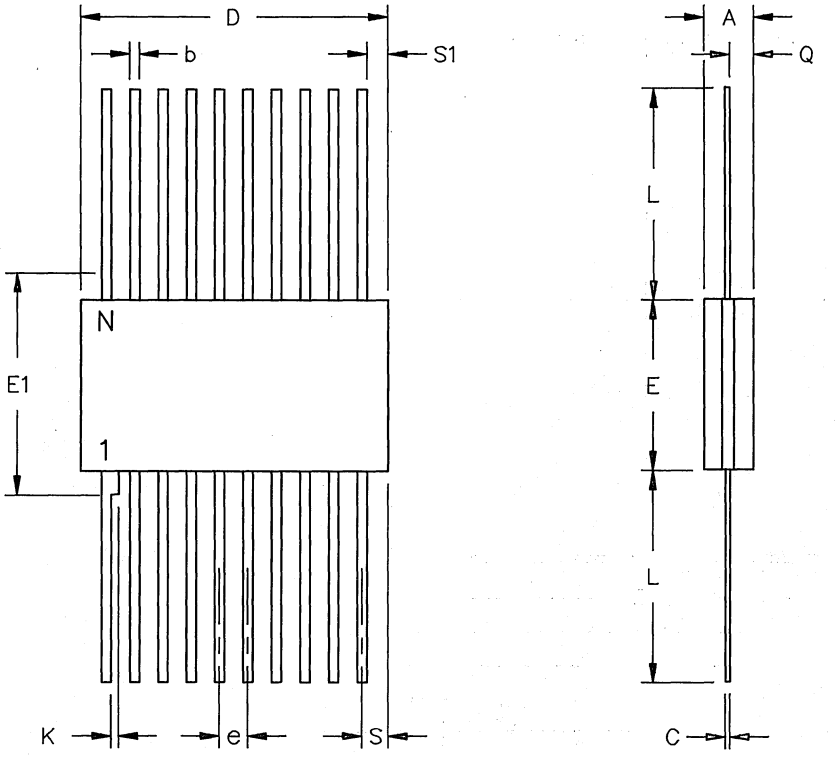
DWG #	F172-2	
# OF LDS (N)	172	
SYMBOL	MIN	MAX
A	–	.140
A1	–	.105
b	.006	.010
C	.004	.008
D/E	1.580	1.620
D1/E1	1.135	1.165
D2/E2	1.050 BSC	
D3/E3	.525 BSC	
e	.025 BSC	
L	.220	.230
ND/NE	43	

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. CROSS HATCHED AREA INDICATES METALLIC HEAT SINK.



CERPACKS

16–28 LEAD CERPACK

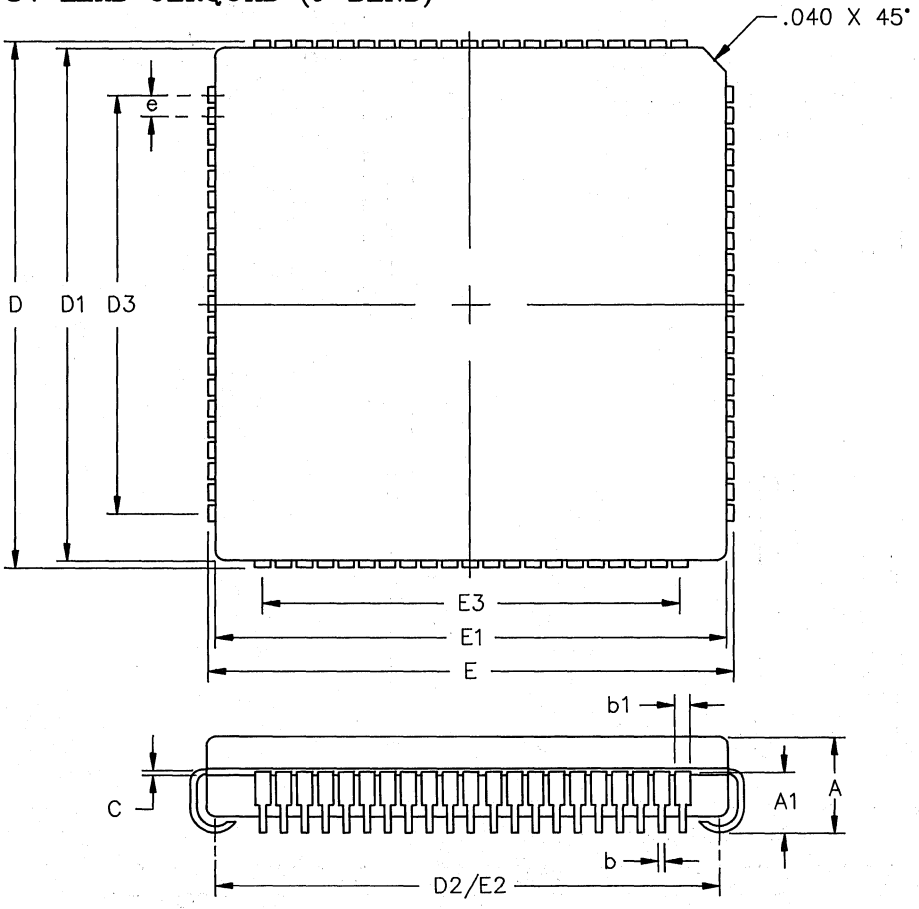


NOTES:
1. ALL DIMENSION ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	E16–1		E20–1		E24–1		E28–1		E28–2	
# OF LDS (N)	16		20		24		28		28	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.055	.085	.045	.092	.045	.090	.045	.115	.045	.090
b	.015	.019	.015	.019	.015	.019	.015	.019	.015	.019
C	.0045	.006	.0045	.006	.0045	.006	.0045	.006	.0045	.006
D	.370	.430	–	.540	–	.640	–	.740	–	.740
E	.245	.285	.245	.300	.300	.420	.460	.520	.340	.380
E1	–	.305	–	.305	–	.440	–	.550	–	.400
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
K	.008	.015	.008	.015	.008	.015	.008	.015	.008	.015
L	.250	.370	.250	.370	.250	.370	.250	.370	.250	.370
Q	.026	.040	.026	.040	.026	.040	.026	.045	.026	.045
S	–	.045	–	.045	–	.045	–	.045	–	.045
S1	.005	–	.005	–	.005	–	.000	–	.005	–

CERQUADS

84 LEAD CERQUAD (J-BEND)

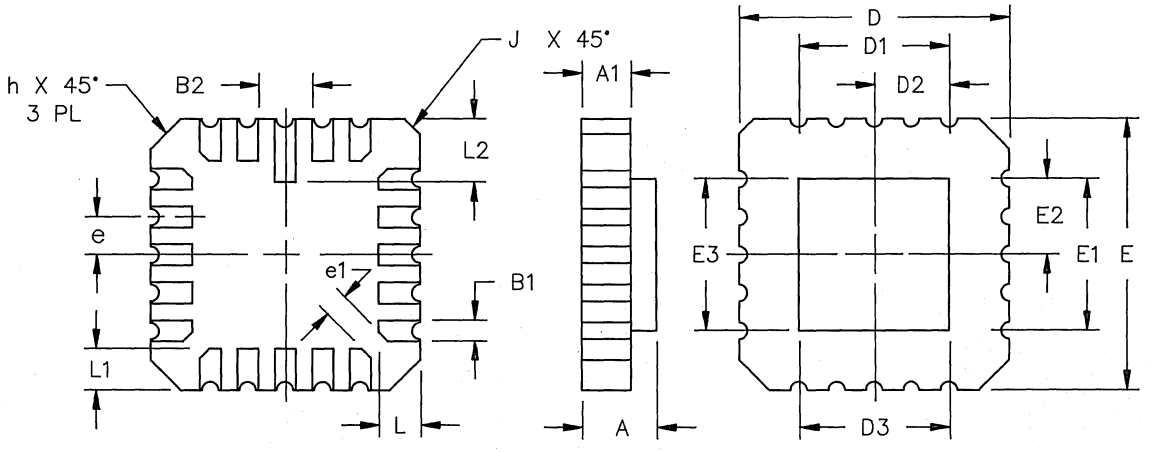


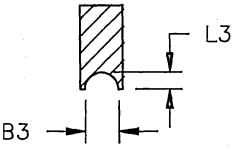
DWG #	CQ84-1	
# OF LDS (N)	84	
SYMBOL	MIN	MAX
A	.155	.200
A1	.090	.120
b1	.022	.032
b	.013	.023
C	.006	.013
D/E	1.170	1.190
D1/E1	1.138	1.162
D2/E2	1.100	.1.150
D3/.E3	1.000 BSC	
e	.050 BSC	
ND/NE	21	

NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

LEADLESS CHIP CARRIERS





NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

20–48 LEAD LCC (SQUARE)

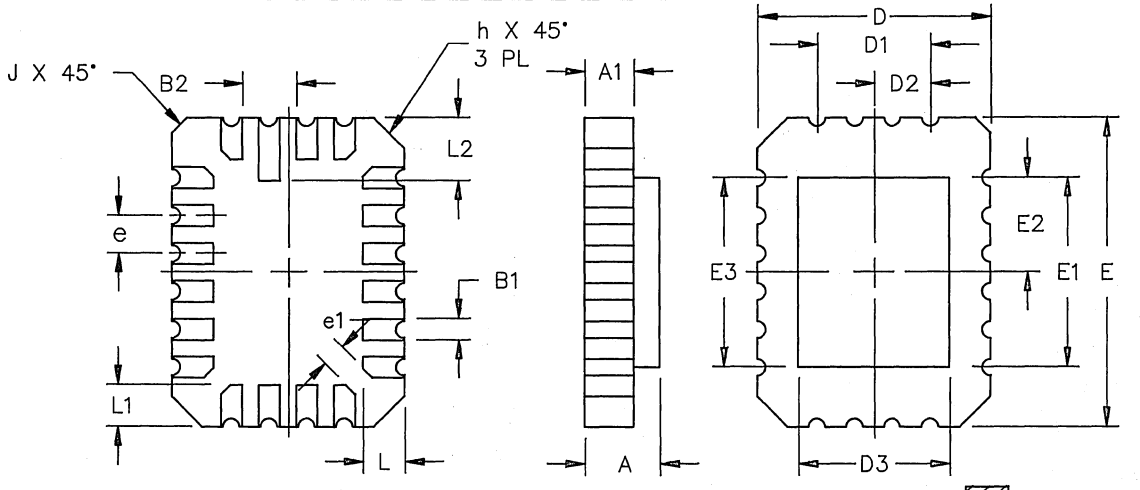
DWG #	L20–2		L28–1		L44–1		L48–1	
# OF LDS (N)	20		28		44		48	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.064	.100	.064	.100	.064	.120	.055	.120
A1	.054	.066	.050	.088	.054	.088	.045	.090
B1	.022	.028	.022	.028	.022	.028	.017	.023
B2	.072 REF		.072 REF		.072 REF		.072 REF	
B3	.006	.022	.006	.022	.006	.022	.006	.022
D/E	.342	.358	.442	.460	.640	.660	.554	.572
D1/E1	.200 BSC		.300 BSC		.500 BSC		.440 BSC	
D2/E2	.100 BSC		.150 BSC		.250 BSC		.220 BSC	
D3/E3	–	.358	–	.460	–	.560	.500	.535
e	.050 BSC		.050 BSC		.050 BSC		.040 BSC	
e1	.015	–	.015	–	.015	–	.015	–
h	.040 REF		.040 REF		.040 REF		.012 RADIUS	
J	.020 REF		.020 REF		.020 REF		.020 REF	
L	.045	.055	.045	.055	.045	.055	.033	.047
L1	.045	.055	.045	.055	.045	.055	.033	.047
L2	.077	.093	.077	.093	.077	.093	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015
ND/NE	5		7		11		12	

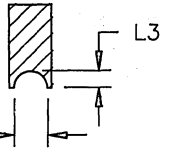
LEADLESS CHIP CARRIERS (Continued)

52–68 LEAD LCC (SQUARE)

DWG #	L52–1		L52–2		L68–2		L68–1	
# OF LDS (N)	52		52		68		68	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.061	.087	.082	.120	.082	.120	.065	.120
A1	.051	.077	.072	.088	.072	.088	.055	.075
B1	.022	.028	.022	.028	.022	.028	.008	.014
B2	.072 REF		.072 REF		.072 REF		.072 REF	
B3	.006	.022	.006	.022	.006	.022	.006	.022
D/E	.739	.761	.739	.761	.938	.962	.554	.566
D1/E1	.600 BSC		.600 BSC		.800 BSC		.400 BSC	
D2/E2	.300 BSC		.300 BSC		.400 BSC		.200 BSC	
D3/E3	–	.661	–	.661	–	.862	–	.535
e	.050 BSC		.050 BSC		.050 BSC		.025 BSC	
e1	.015	–	.015	–	.015	–	.015	–
h	.040 REF		.040 REF		.040 REF		.040 REF	
J	.020 REF		.020 REF		.020 REF		.020 REF	
L	.045	.055	.045	.055	.045	.055	.045	.055
L1	.045	.055	.045	.055	.045	.055	.045	.055
L2	.077	.093	.075	.093	.075	.095	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015
ND/NE	13		13		17		17	

LEADLESS CHIP CARRIERS (Continued)





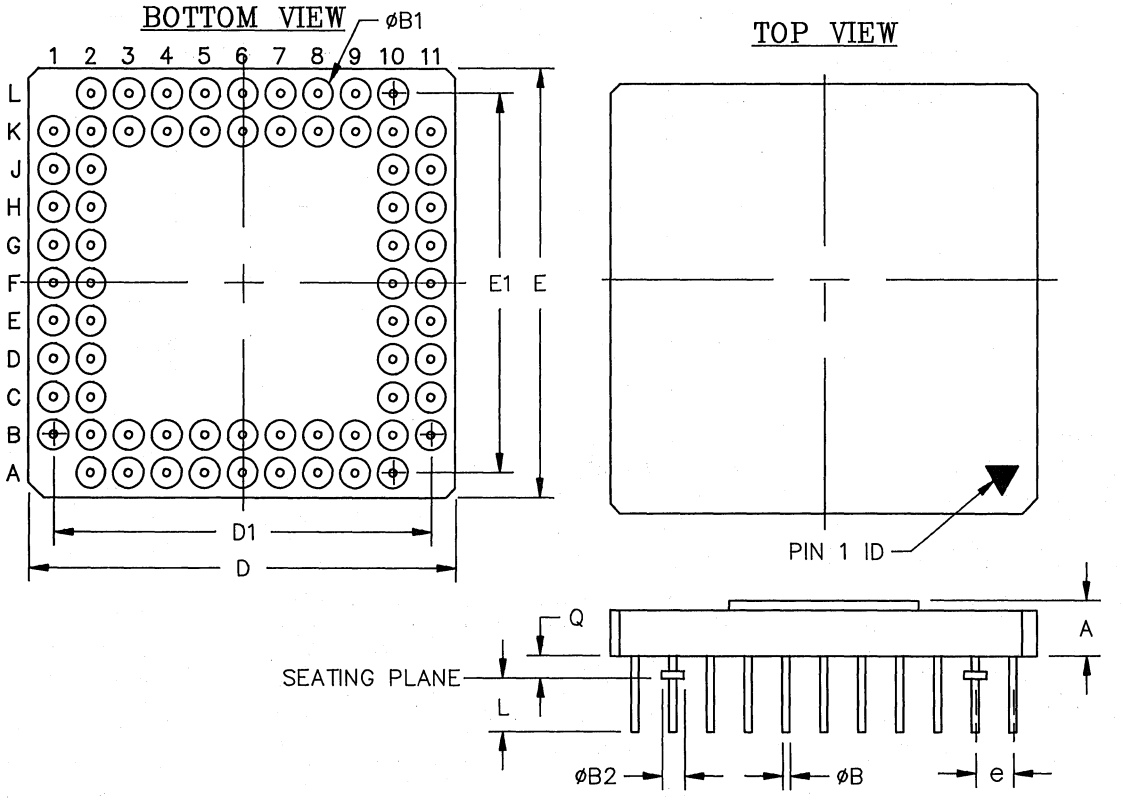
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

20–32 LEAD LCC (RECTANGULAR)

DWG #	L20–1		L22–1		L24–1		L28–2		L32–1	
# OF LDS (N)	20		22		24		28		32	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.060	.075	.064	.100	.064	.120	.060	.120	.060	.120
A1	.050	.065	.054	.063	.054	.066	.050	.088	.050	.088
B1	.022	.028	.022	.028	.022	.028	.022	.028	.022	.028
B2	.072 REF		.072 REF		.072 REF		.072 REF		.072 REF	
B3	.006	.022	.006	.022	.006	.022	.006	.022	.006	.022
D	.284	.296	.284	.296	.292	.308	.342	.358	.442	.458
D1	.150 BSC		.150 BSC		.200 BSC		.200 BSC		.300 BSC	
D2	.075 BSC		.075 BSC		.100 BSC		.100 BSC		.150 BSC	
D3	–	.280	–	.280	–	.308	–	.358	–	.458
E	.420	.435	.480	.496	.392	.408	.540	.560	.540	.560
E1	.250 BSC		.300 BSC		.300 BSC		.400 BSC		.400 BSC	
E2	.125 BSC		.150 BSC		.150 BSC		.200 BSC		.200 BSC	
E3	–	.410	–	.480	–	.408	–	.558	–	.558
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
e1	.015	–	.015	–	.015	–	.015	–	.015	–
h	.040 REF		.012 RADIUS		.025 REF		.040 REF		.040 REF	
J	.020 REF		.012 RADIUS		.015 REF		.020 REF		.020 REF	
L	.045	.055	.039	.051	.040	.050	.045	.055	.045	.055
L1	.045	.055	.039	.051	.040	.050	.045	.055	.045	.055
L2	.080	.095	.083	.097	.077	.093	.077	.093	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015	.003	.015
ND	4		4		5		5		7	
NE	6		7		7		9		9	

PIN GRID ARRAYS

68 PIN PGA (CAVITY UP)

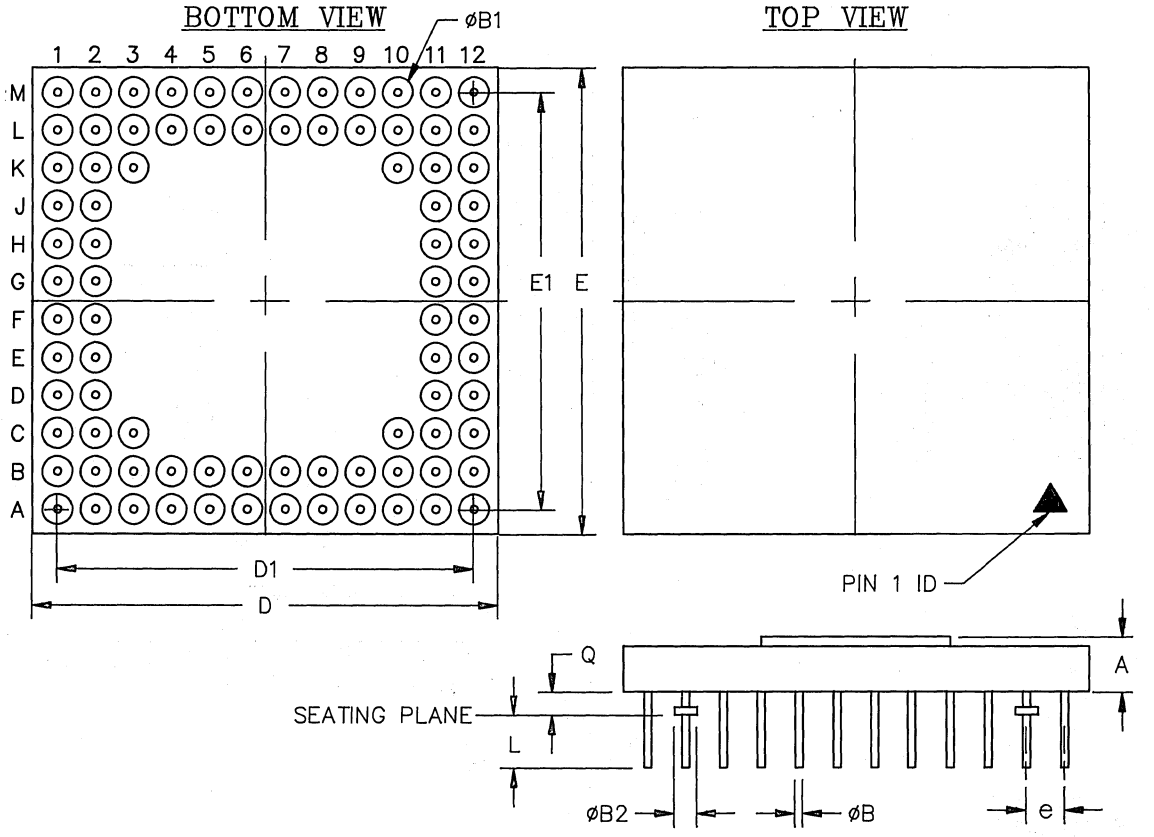


DWG #	G68-1	
# OF PINS (N)	68	
SYMBOL	MIN	MAX
A	.070	.145
øB	.016	.020
øB1	–	.080
øB2	.040	.060
D/E	1.140	1.180
D1/E1	1.000 BSC	
e	.100 BSC	
L	.120	.140
M	11	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

84 PIN PGA (CAVITY UP – 12 X 12 GRID)

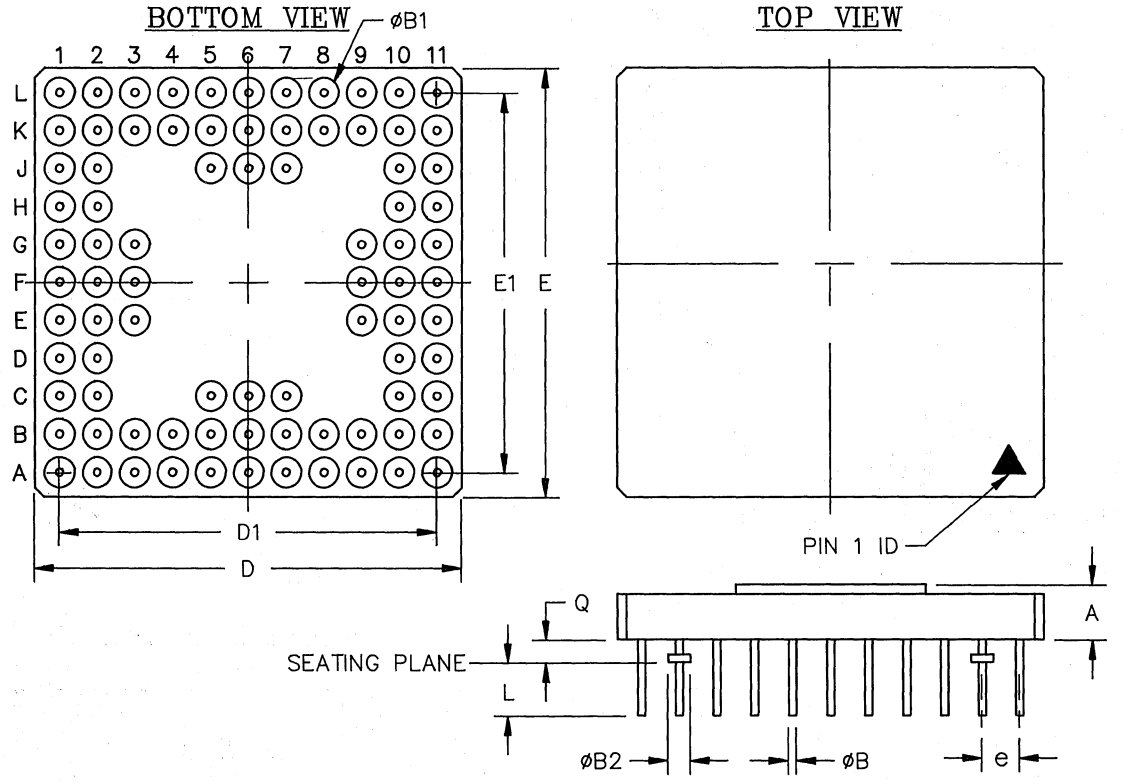


DWG #	G84–1	
# OF PINS (N)	84	
SYMBOL	MIN	MAX
A	.077	.145
ØB	.016	.020
ØB1	.060	.080
ØB2	.040	.060
D/E	1.180	1.235
D1/E1	1.100 BSC	
e	.100 BSC	
L	.120	.140
M	12	
Q	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

84 PIN PGA (CAVITY UP – 11 X 11 GRID)

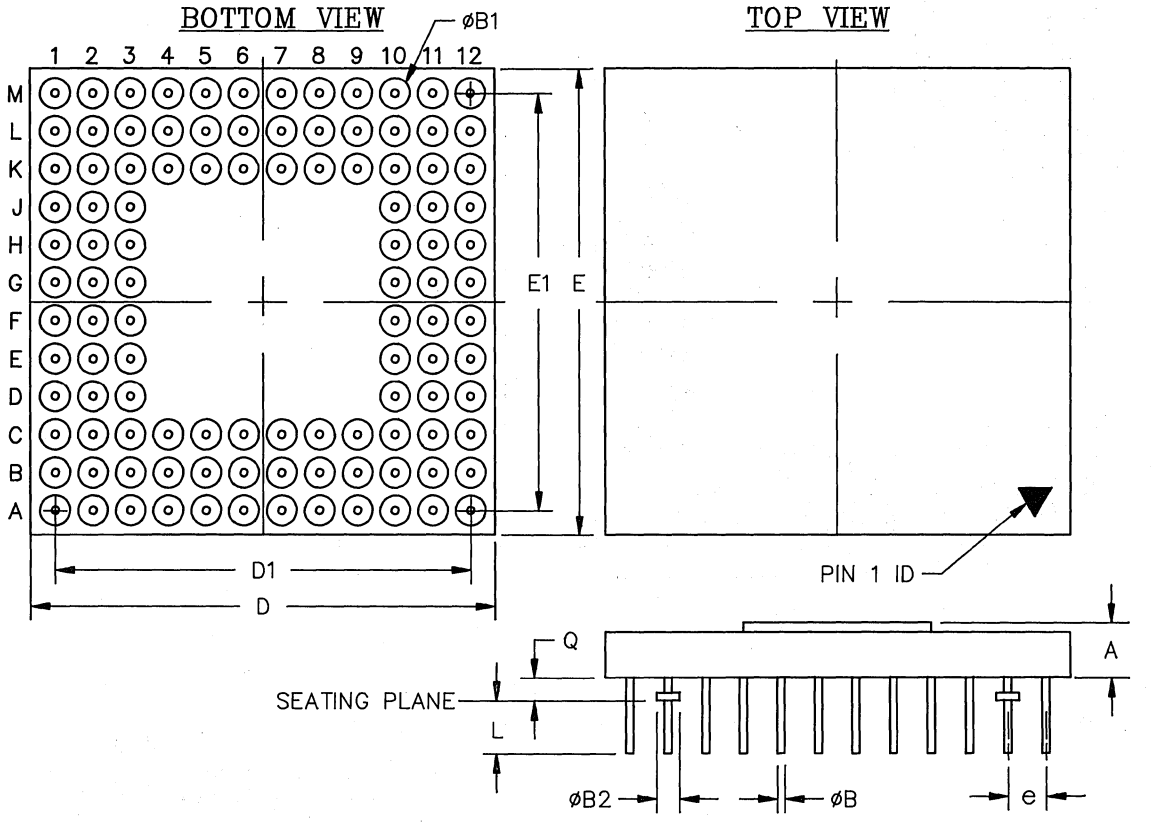


DWG #	G84–3	
# OF PINS (N)	84	
SYMBOL	MIN	MAX
A	.070	.145
øB	.016	.020
øB1	–	.080
øB2	.040	.060
D/E	1.080	1.120
D1/E1	1.000 BSC	
e	.100 BSC	
L	.120	.140
M	11	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

108 PIN PGA (CAVITY UP)

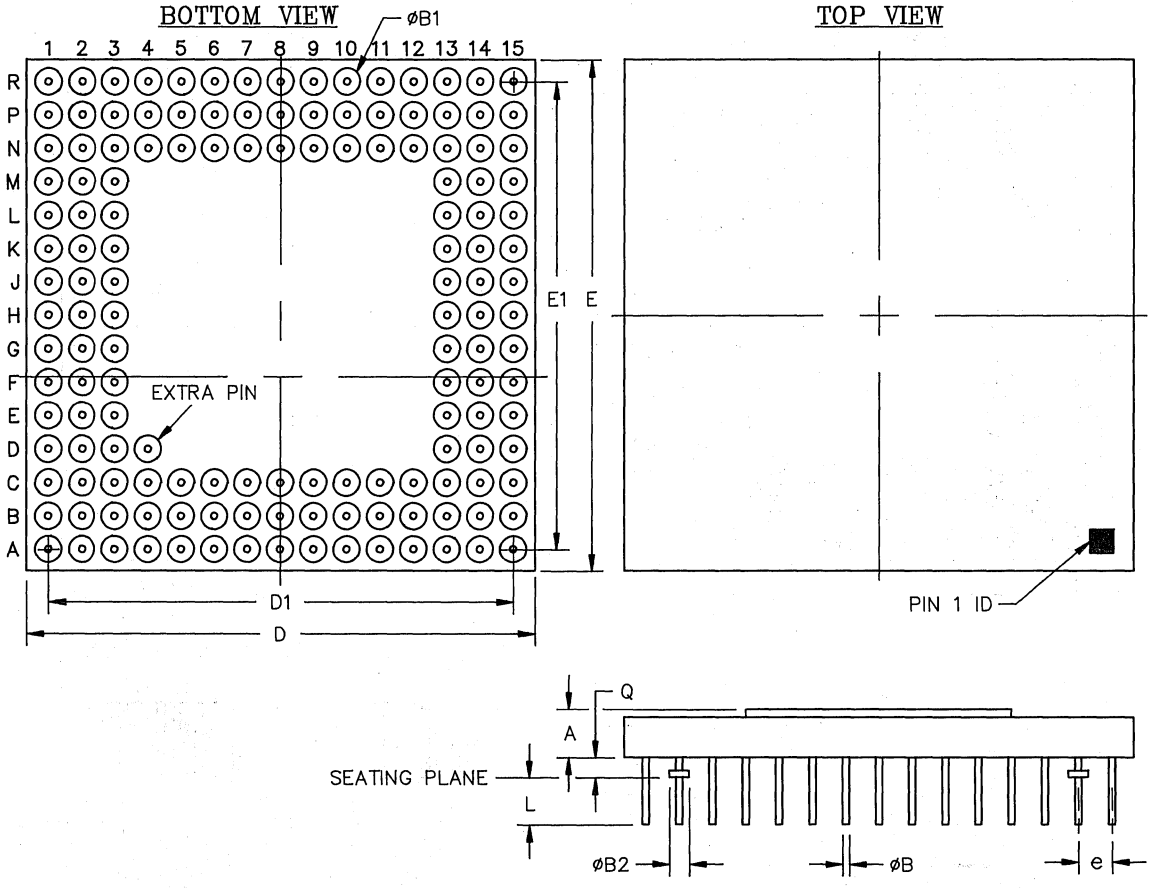


DWG #	G108-1	
# OF PINS (N)	108	
SYMBOL	MIN	MAX
A	.070	.145
ØB	.016	.020
ØB1	–	.080
ØB2	.040	.060
D/E	1.188	1.212
D1/E1	1.100 BSC	
e	.100 BSC	
L	.120	.140
M	12	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

144 PIN PGA (CAVITY UP – R3001)

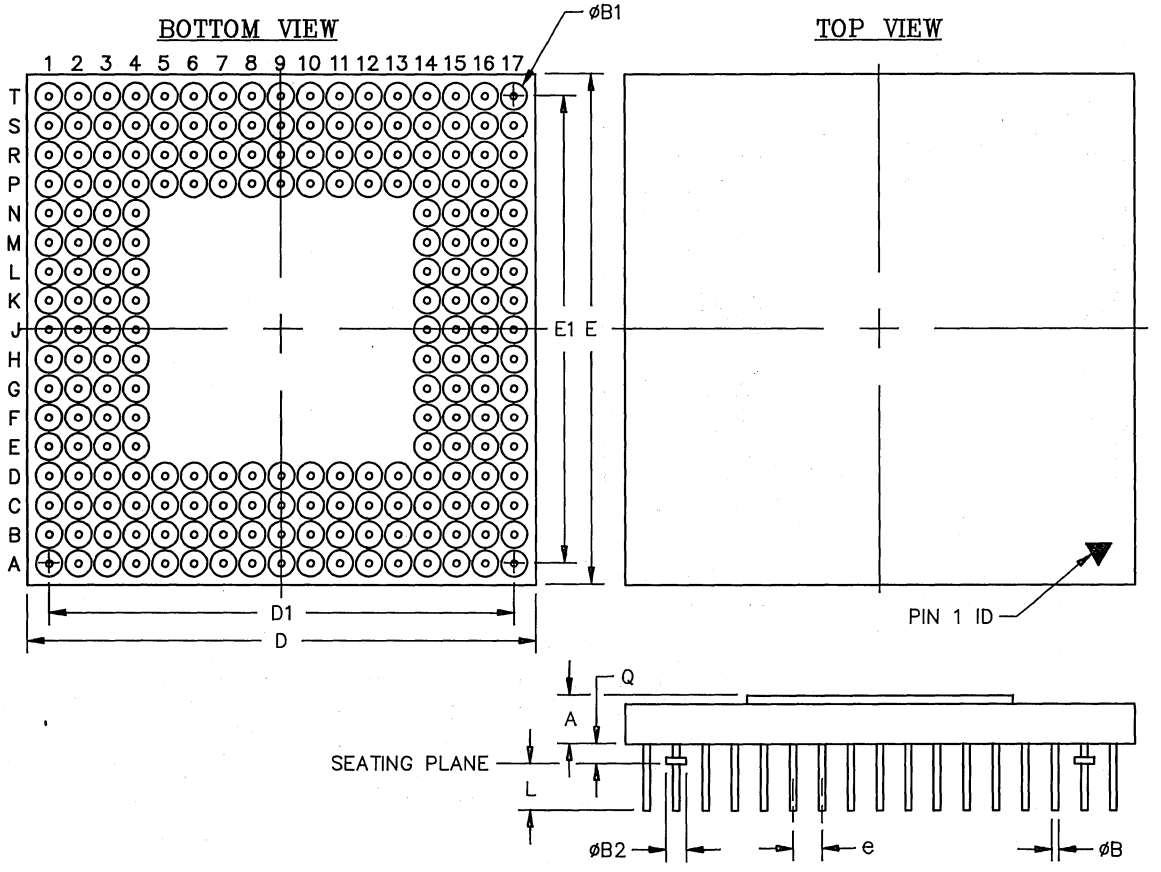


DWG #	G144–2	
# OF PINS (N)	145	
SYMBOL	MIN	MAX
A	.082	.125
ØB	.016	.020
ØB1	.060	.080
ØB2	.040	.060
D/E	1.559	1.590
D1/E1	1.400 BSC	
e	.100 BSC	
L	.120	.140
M	15	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.
6. EXTRA PIN (D–4) ELECTRICALLY CONNECTED TO D–3.

PIN GRID ARRAYS (Continued)

208 PIN PGA (CAVITY UP)

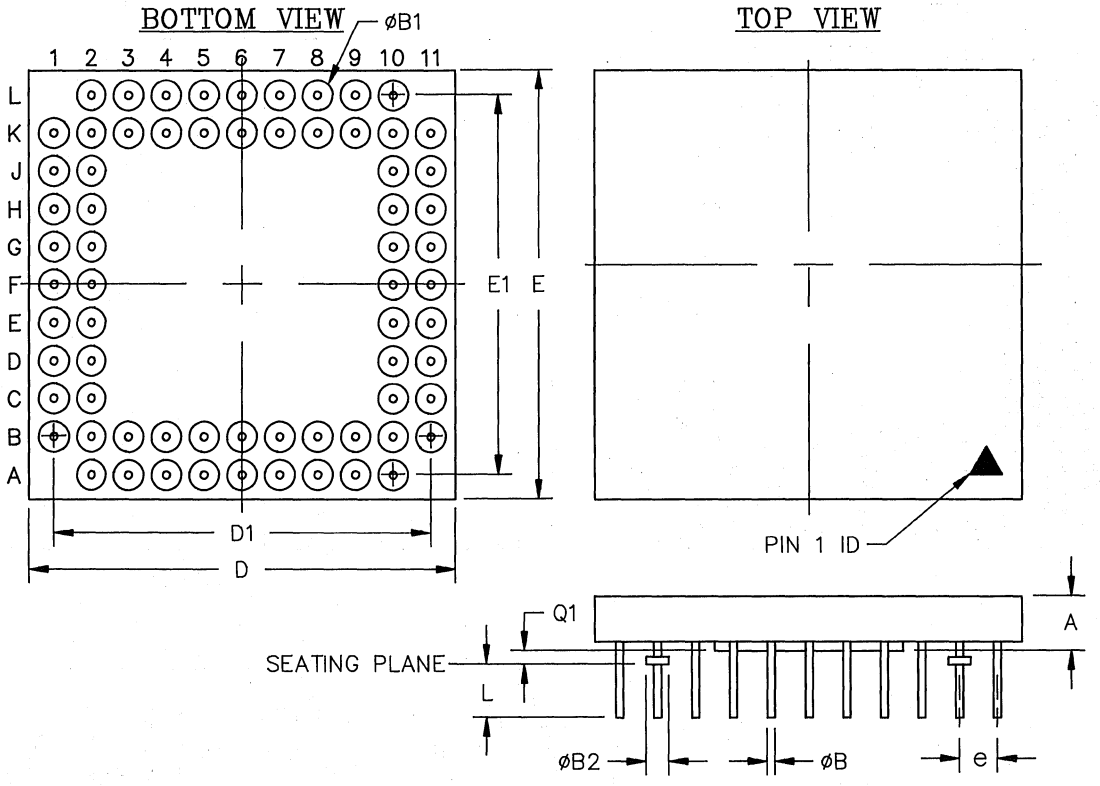


DWG #	G208-1	
# OF PINS (N)	208	
SYMBOL	MIN	MAX
A	.070	.145
øB	.016	.020
øB1	–	.080
øB2	.040	.060
D/E	1.732	1.780
D1/E1	1.600 BSC	
e	.100 BSC	
L	.125	.140
M	17	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

68 PIN PGA (CAVITY DOWN)

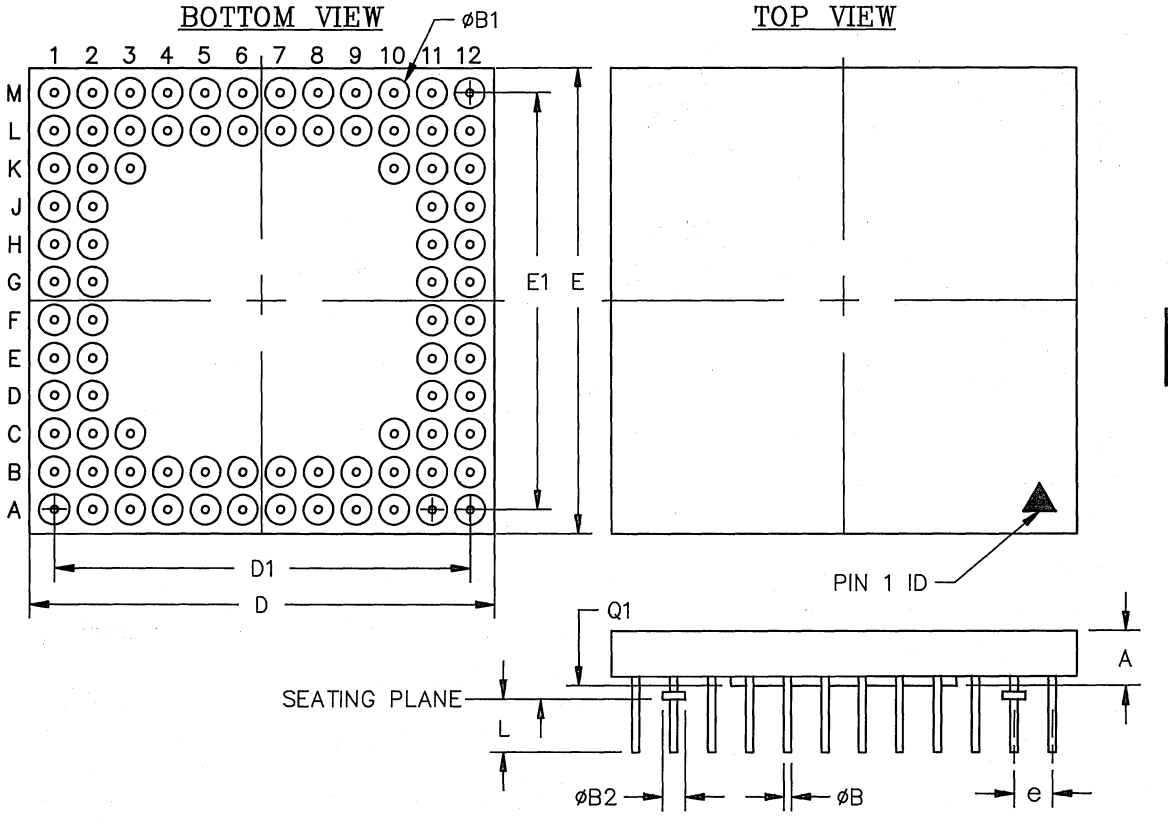


DWG #	GU68-2	
# OF PINS (N)	68	
SYMBOL	MIN	MAX
A	.077	.095
ØB	.016	.020
ØB1	.060	.080
ØB2	.040	.060
D/E	1.098	1.122
D1/E1	1.000 BSC	
e	.100 BSC	
L	.120	.140
M	11	
Q1	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

84 PIN PGA (CAVITY DOWN)

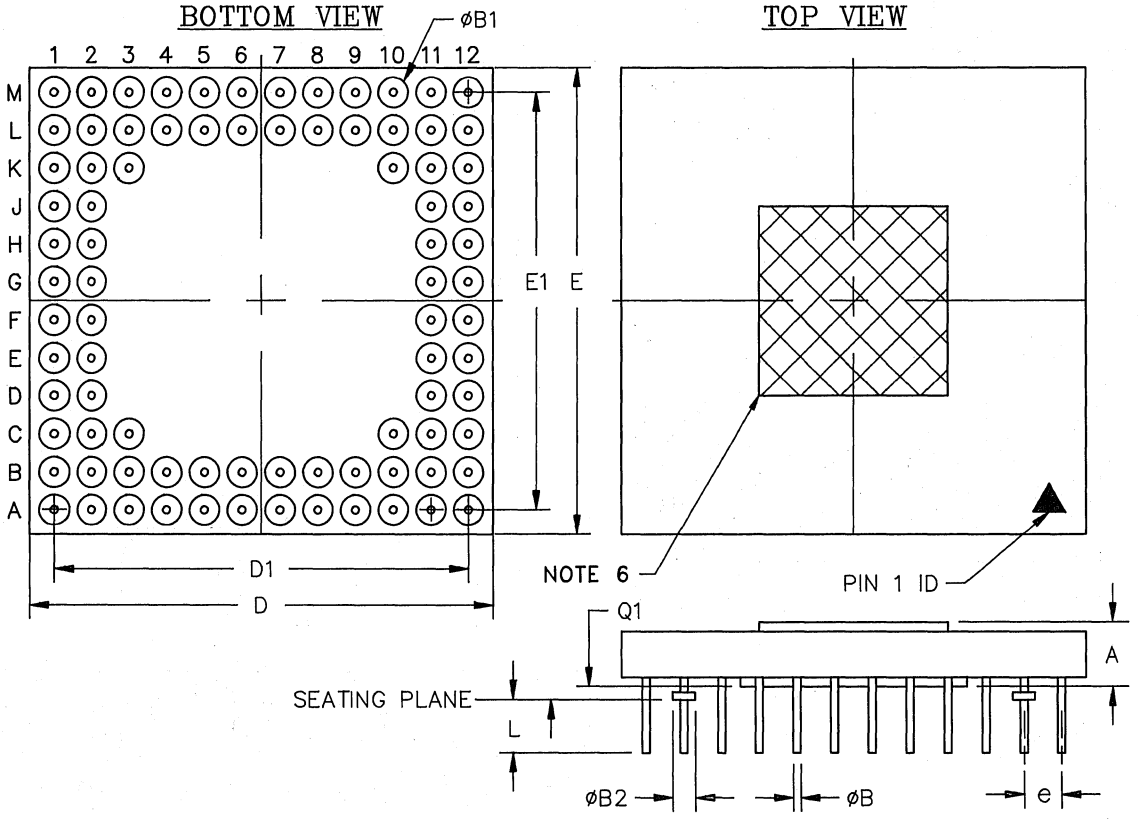


DWG #	G84-2	
# OF PINS (N)	84	
SYMBOL	MIN	MAX
A	.077	.145
øB	.016	.020
øB1	.060	.080
øB2	.040	.060
D/E	1.180	1.235
D1/E1	1.100 BSC	
e	.100 BSC	
L	.100	.120
M	12	
Q1	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

84 PIN PGA (CAVITY DOWN – R3010A)

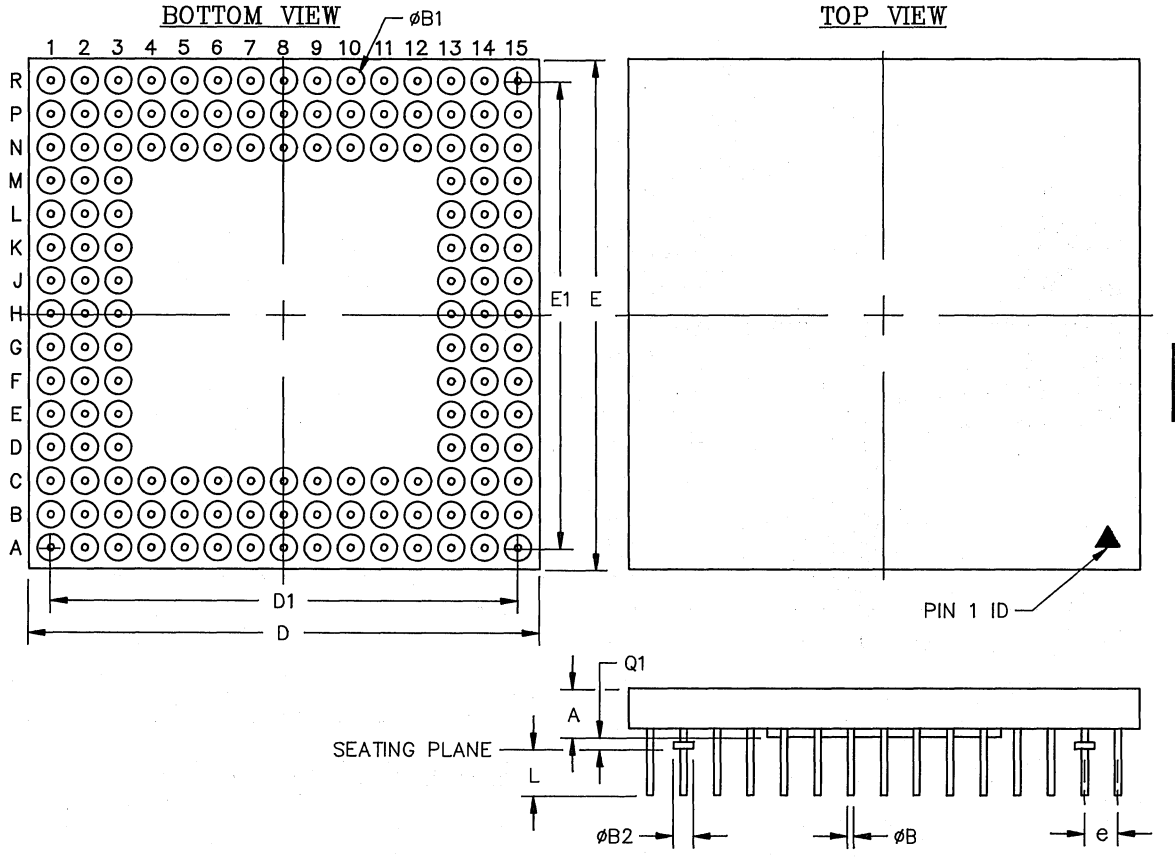


DWG #	G84–4	
# OF PINS (N)	84	
SYMBOL	MIN	MAX
A	.077	.145
øB	.016	.020
øB1	.060	.080
øB2	.040	.060
D/E	1.180	1.235
D1/E1	1.100 BSC	
e	.100 BSC	
L	.120	.140
M	12	
Q1	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.
6. CROSS HATCHED AREA INDICATES INTEGRAL METALLIC HEAT SINK.

PIN GRID ARRAYS (Continued)

144 PIN PGA (CAVITY DOWN)

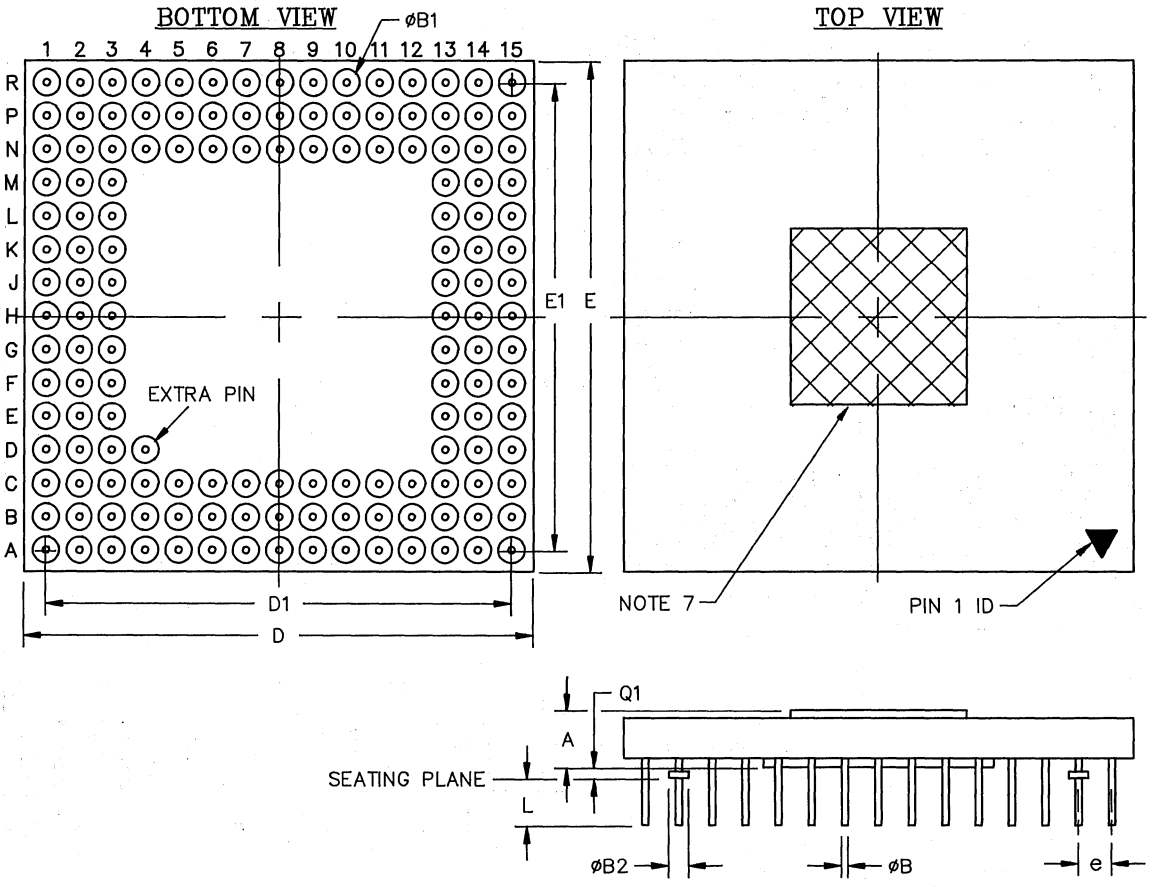


DWG #	G144-1	
# OF PINS (N)	144	
SYMBOL	MIN	MAX
A	.082	.100
ØB	.016	.020
ØB1	.060	.080
ØB2	.040	.060
D/E	1.559	1.590
D1/E1	1.400 BSC	
e	.100 BSC	
L	.120	.140
M	15	
Q1	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

144 PIN PGA (CAVITY DOWN – R3000A)

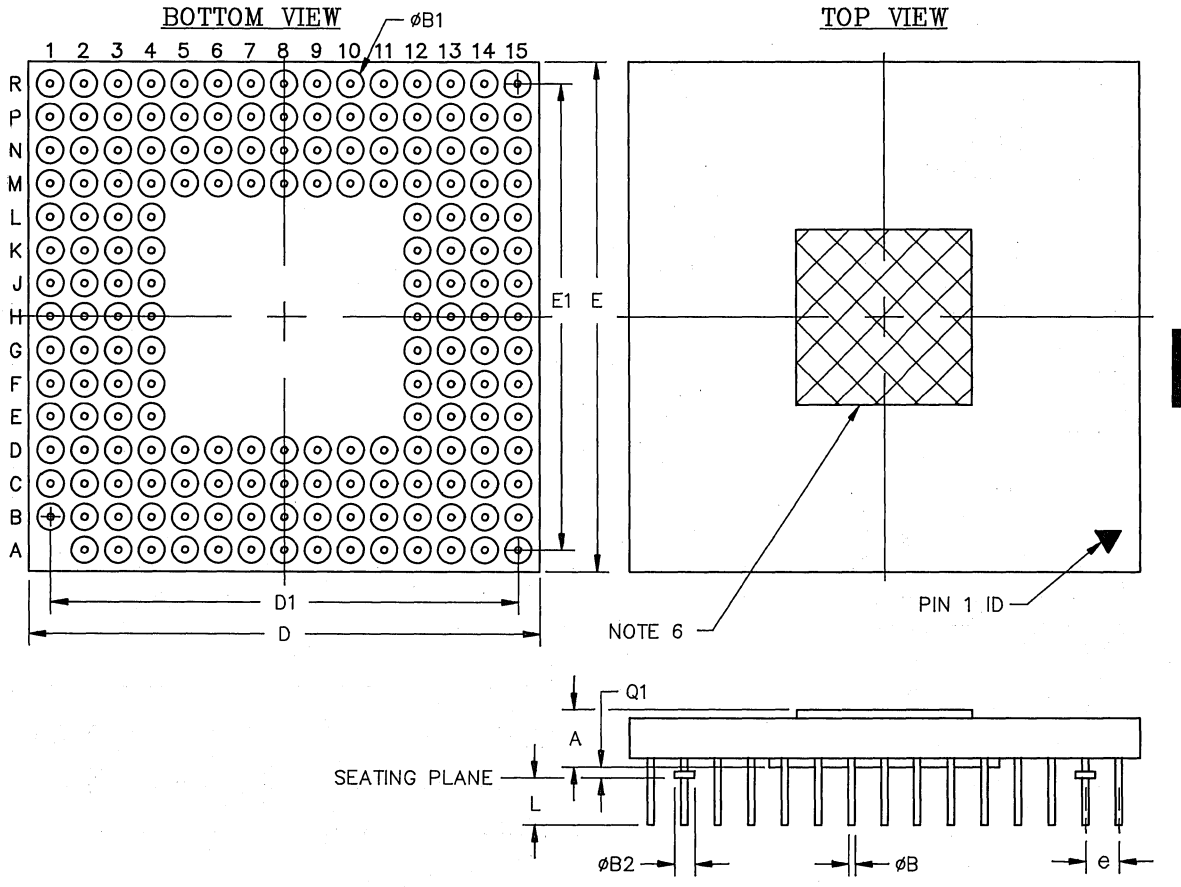


DWG #	G144-3	
# OF PINS (N)	145	
SYMBOL	MIN	MAX
A	.082	.130
ØB	.016	.020
ØB1	.060	.080
ØB2	.040	.060
D/E	1.559	1.590
D1/E1	1.400 BSC	
e	.100 BSC	
L	.120	.140
M	15	
Q1	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.
6. EXTRA PIN (D–4) ELECTRICALLY CONNECTED TO D–3.
7. CROSS HATCHED AREA INDICATES INTEGRAL METALLIC HEAT SINK.

PIN GRID ARRAYS (Continued)

175 PIN PGA (CAVITY DOWN – R3000A)

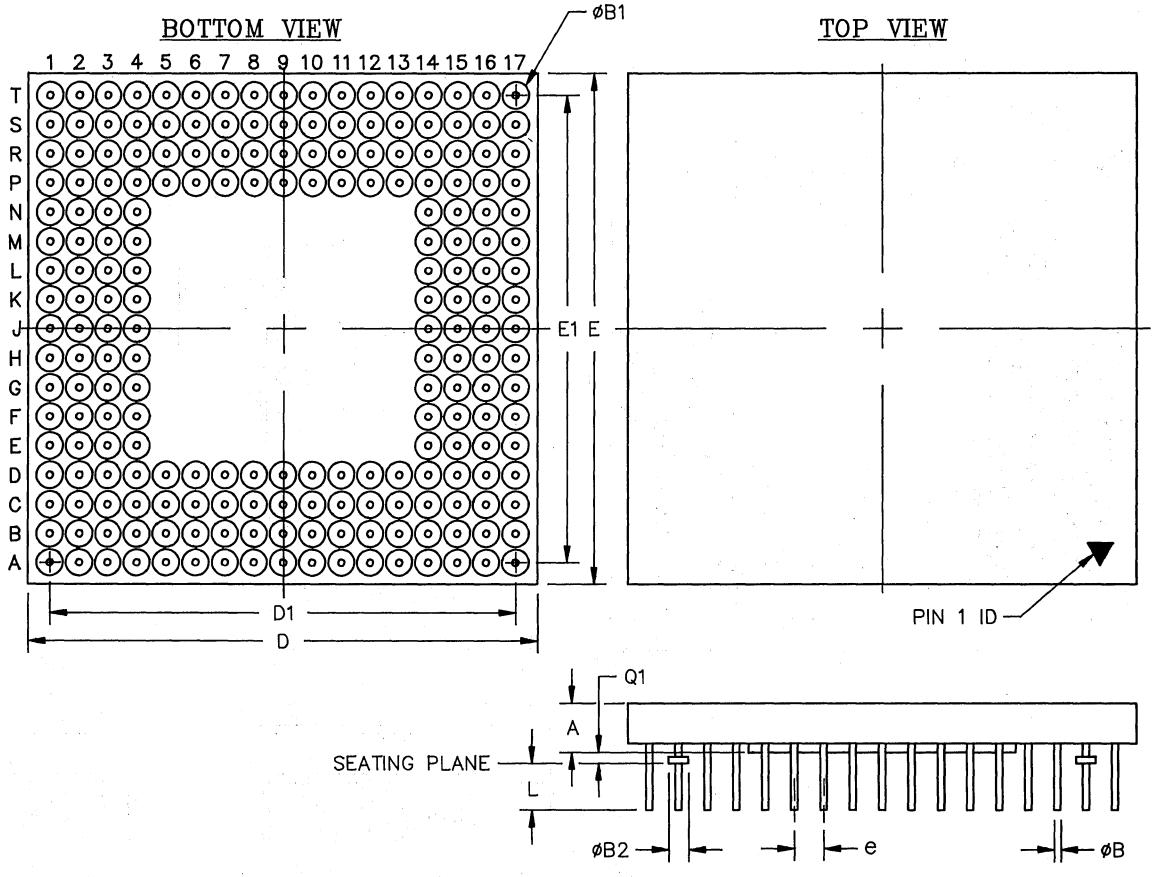


DWG #	G175–1	
# OF PINS (N)	175	
SYMBOL	MIN	MAX
A	.082	.130
øB	.016	.020
øB1	.060	.080
øB2	.040	.060
D/E	1.559	1.590
D1/E1	1.400 BSC	
e	.100 BSC	
L	.120	.140
M	15	
Q1	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.
6. CROSS HATCHED AREA INDICATES INTEGRAL METALLIC HEAT SINK.

PIN GRID ARRAYS (Continued)

208 PIN PGA (CAVITY DOWN)

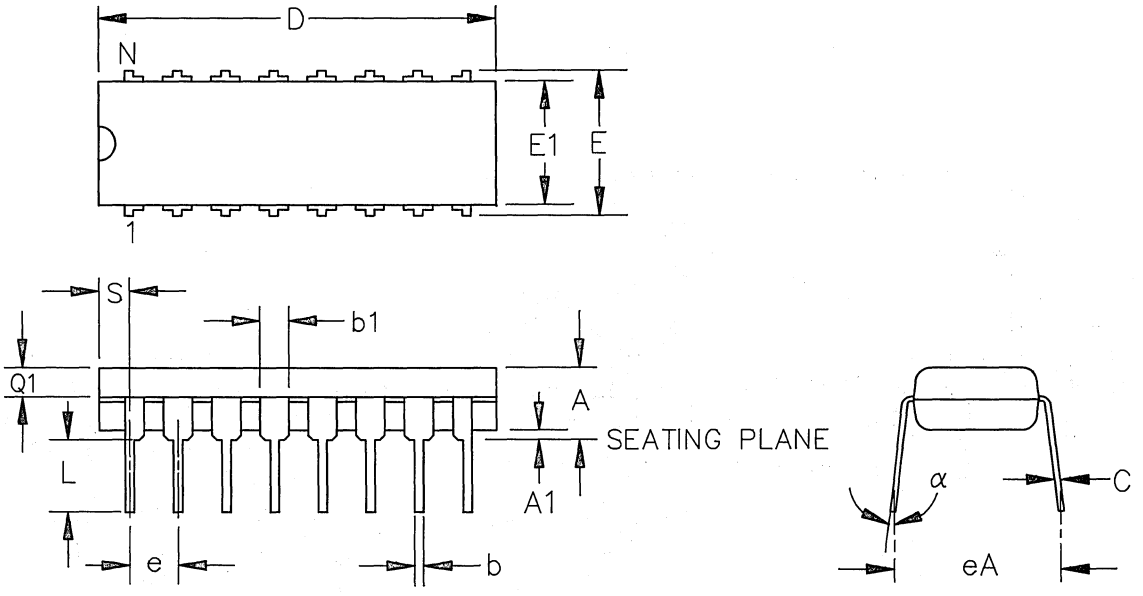


DWG #	G208-2	
# OF PINS (N)	208	
SYMBOL	MIN	MAX
A	.070	.145
øB	.016	.020
øB1	–	.080
øB2	.040	.060
D/E	1.732	1.780
D1/E1	1.600 BSC	
e	.100 BSC	
L	.120	.140
M	17	
Q1	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PLASTIC DUAL IN-LINE PACKAGES

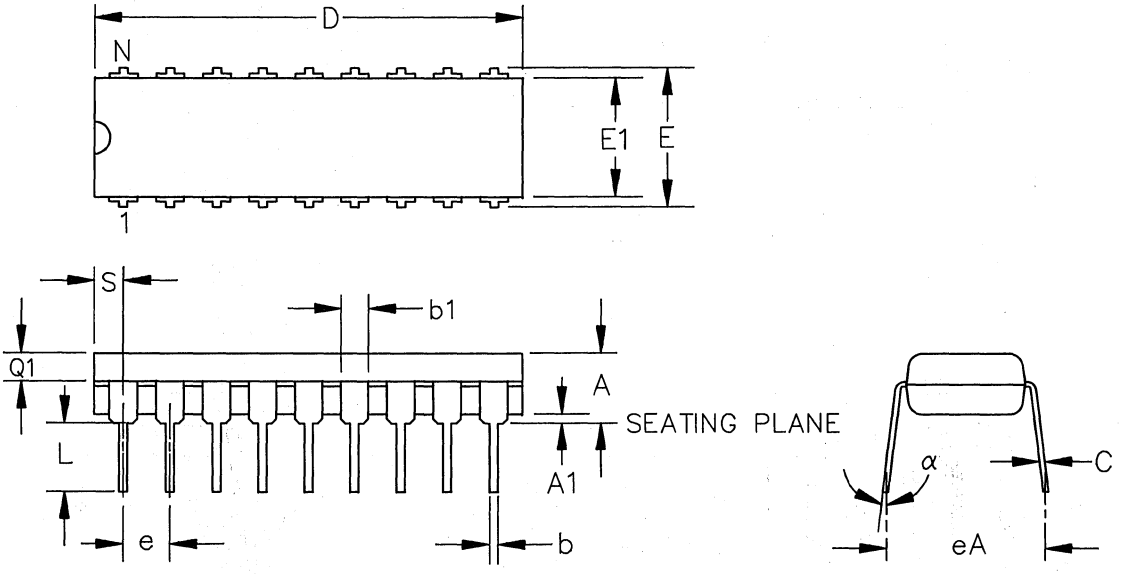
16-32 LEAD PLASTIC DIP (300 MIL)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DWG #	P16-1		P22-1		P28-2		P32-2	
# OF LDS (N)	16		22		28		32	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.165	.145	.165	.145	.180	.145	.180
A1	.015	.035	.015	.035	.015	.030	.015	.030
b	.015	.022	.015	.022	.015	.022	.016	.022
b1	.050	.070	.050	.065	.045	.065	.045	.060
C	.008	.012	.008	.012	.008	.015	.008	.015
D	.745	.760	1.050	1.060	1.345	1.375	1.545	1.585
E	.300	.325	.300	.320	.300	.325	.300	.325
E1	.247	.260	.240	.270	.270	.295	.275	.295
e	.090	.110	.090	.110	.090	.110	.090	.110
eA	.310	.370	.310	.370	.310	.400	.310	.400
L	.120	.150	.120	.150	.120	.150	.120	.150
α	0°	15°	0°	15°	0°	15°	0°	15°
S	.015	.035	.020	.040	.020	.042	.020	.060
Q1	.050	.070	.055	.075	.055	.065	.055	.065

PLASTIC DUAL IN-LINE PACKAGES (Continued)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

18-24 LEAD PLASTIC DIP (300 MIL - FULL LEAD)

DWG #	P18-1		P20-1		P24-1	
# OF LDS (N)	18		20		24	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.165	.145	.165	.145	.165
A1	.015	.035	.015	.035	.015	.035
b	.015	.020	.015	.020	.015	.020
b1	.050	.070	.050	.070	.050	.065
C	.008	.012	.008	.012	.008	.012
D	.885	.910	1.022	1.040	1.240	1.255
E	.300	.325	.300	.325	.300	.320
E1	.247	.260	.240	.280	.250	.275
e	.090	.110	.090	.110	.090	.110
eA	.310	.370	.310	.370	.310	.370
L	.120	.150	.120	.150	.120	.150
α	0°	15°	0°	15°	0°	15°
S	.040	.060	.025	.070	.055	.075
Q1	.050	.070	.055	.075	.055	.070

PLASTIC DUAL IN-LINE PACKAGES (Continued)

24-48 LEAD PLASTIC DIP (600 MIL)

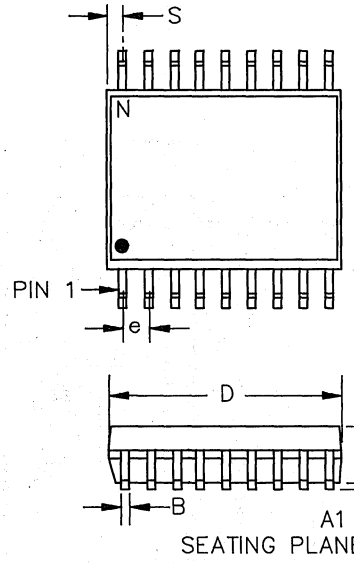
DWG #	P24-2		P28-1		P32-1		P40-1		P48-1	
# OF LEADS (N)	24		28		32		40		48	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.160	.185	.160	.185	.170	.190	.160	.185	.170	.200
A1	.015	.035	.015	.035	.015	.050	.015	.035	.015	.035
b	.015	.020	.015	.020	.016	.020	.015	.020	.015	.020
b1	.050	.065	.050	.065	.045	.055	.050	.065	.050	.065
C	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012
D	1.240	1.260	1.420	1.460	1.645	1.655	2.050	2.070	2.420	2.450
E	.600	.620	.600	.620	.600	.625	.600	.620	.600	.620
E1	.530	.550	.530	.550	.530	.550	.530	.550	.530	.560
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
eA	.610	.670	.610	.670	.610	.670	.610	.670	.610	.670
L	.120	.150	.120	.150	.125	.135	.120	.150	.120	.150
α	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°
S	.060	.080	.055	.080	.070	.080	.070	.085	.060	.075
Q1	.060	.080	.060	.080	.065	.075	.060	.080	.060	.080

4

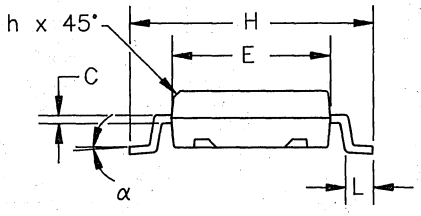
64 LEAD PLASTIC DIP (900 MIL)

DWG #	P64-1	
# OF LEADS (N)	64	
SYMBOLS	MIN	MAX
A	.180	.230
A1	.015	.040
b	.015	.020
b1	.050	.065
C	.008	.012
D	3.200	3.220
E	.900	.925
E1	.790	.810
e	.090	.110
eA	.910	1.000
L	.120	.150
α	0°	15°
S	.045	.065
Q1	.080	.090

SMALL OUTLINE IC



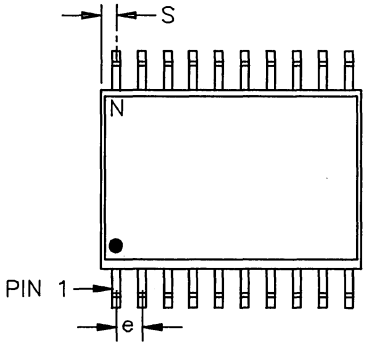
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND TO BE MEASURED FROM THE BOTTOM OF PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.



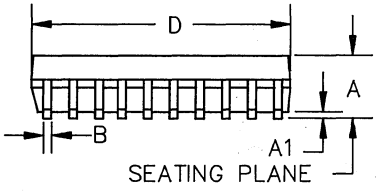
16–24 LEAD SMALL OUTLINE (GULL WING)

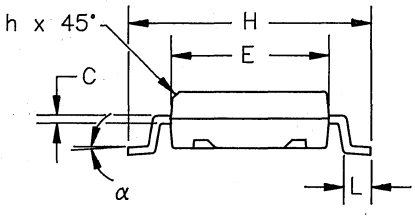
DWG #	SO16–1		SO18–1		SO20–2		SO24–2	
# OF LDS (N)	16 (.300)		18 (.300)		20 (.300")		24 (.300")	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.095	.1043	.095	.1043	.095	.1043	.095	.1043
A1	.005	.0118	.005	.0118	.005	.0118	.005	.0118
B	.014	.020	.014	.020	.014	.020	.014	.020
C	.0091	.0125	.0091	.0125	.0091	0125	.0091	.0125
D	.403	.413	.447	.462	.497	.511	.600	.614
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC	
E	.292	.2992	.292	.2992	.292	.2992	.292	.2992
h	.010	.020	.010	.020	.010	.020	.010	.020
H	.400	.419	.400	.419	.400	.419	.400	.419
L	.018	.045	.018	.045	.018	.045	.018	.045
α	0°	8°	0°	8°	0°	8°	0°	8°
S	.023	.035	.023	.035	.023	.035	.023	.035

SMALL OUTLINE IC (Continued)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.

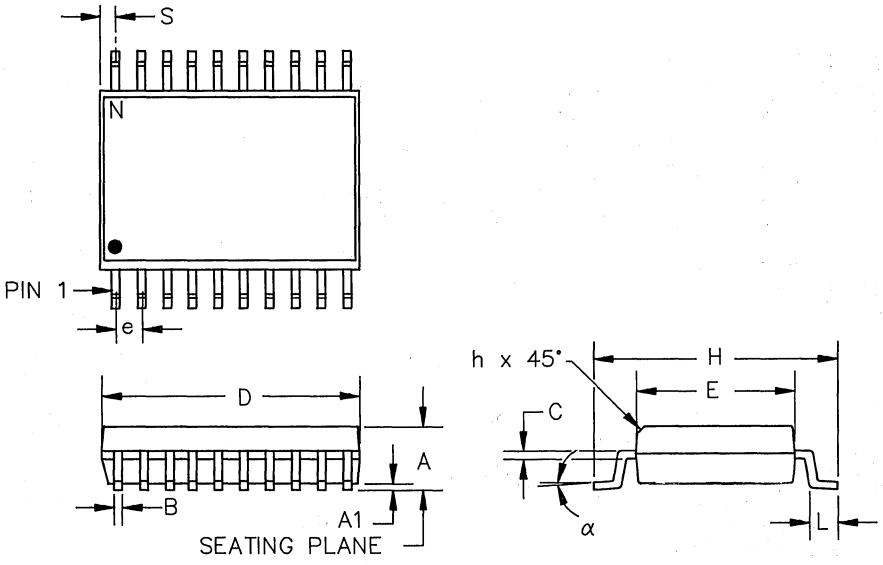




28 LEAD SMALL OUTLINE (GULL WING)

DWG #	SO28–2		SO28–3	
# OF LDS (N)	28 (.300")		28 (.330")	
SYMBOL	MIN	MAX	MIN	MAX
A	.095	.1043	.110	.120
A1	.005	.0118	.005	.014
B	.014	.020	.014	.019
C	.0091	.0125	.006	.010
D	.700	.712	.718	.728
e	.050 BSC		.050 BSC	
E	.292	.2992	.340	.350
h	.010	.020	.012	.020
H	.400	.419	.462	.478
L	.018	.045	.028	.045
α	0°	8°	0°	8°
S	.023	.035	.023	.035

SMALL OUTLINE IC (Continued)

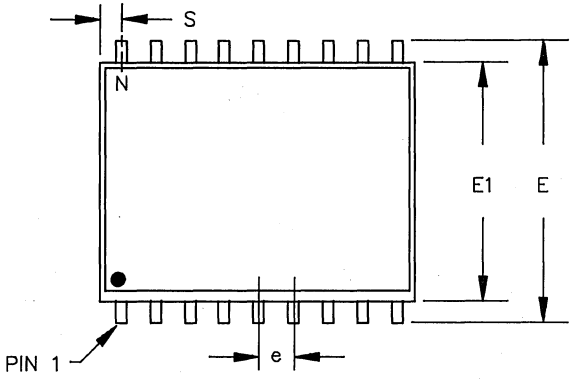


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.

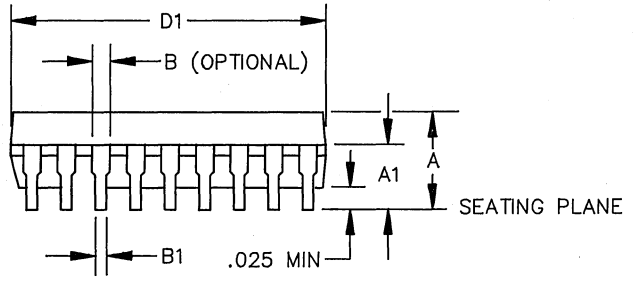
16–28 LEAD SMALL OUTLINE (EIAJ – .050 PITCH)

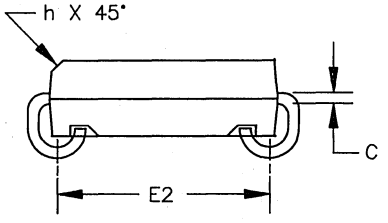
DWG #	SO16–6		SO20–6		SO24–6	
# OF LDS (N)	16		20		24	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX
A	.067	.083	.069	.083	.069	.083
A1	.003	–	.002 TYP		.002 TYP	
B	.014	.018	.012	.020	.012	.020
C	.005	.007	.006	.010	.006	.010
D	.398	.406	.480	.504	.580	.603
E	.197	.220	.205	.220	.205	.220
e	.050 BSC		.050 BSC		.050 BSC	
H	.299	.315	.300	.319	.300	.319
L	.026	.034	.010	–	.010	–
α	12° REF		0°	8°	0°	8°

SMALL OUTLINE IC (Continued)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSION AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE



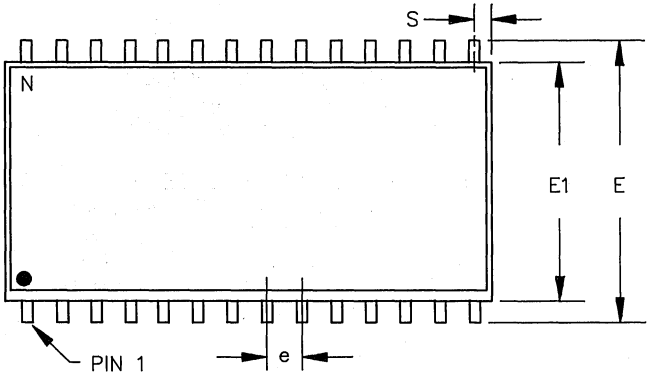


4

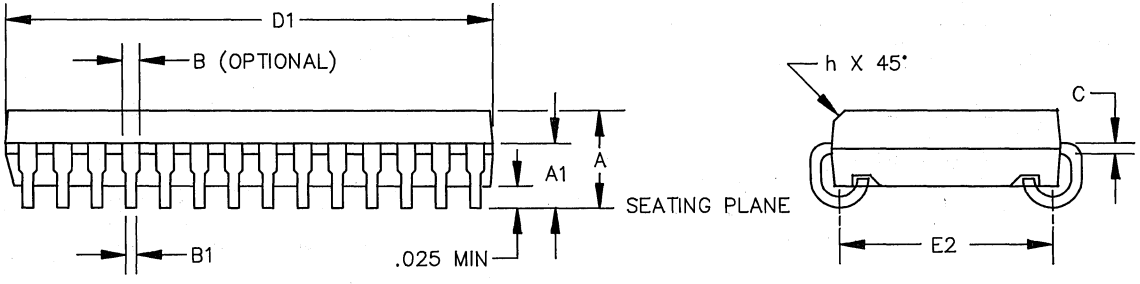
16–24 LEAD SMALL OUTLINE (J–BEND)

DWG #	SO16–2		SO20–1		SO24–4		SO24–8	
# OF LDS (N)	16 LD (.300")		20 LD (.300")		24 LD (.300")		24 LD (.300")	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.120	.140	.120	.140	.130	.148	.120	.140
A1	.078	.095	.078	.095	.082	.095	.078	.091
B	.020	.024	.020	.024	.026	.032	.026	.032
B1	.014	.020	.014	.020	.015	.020	.014	.019
C	.008	.013	.008	.013	.007	.011	.0091	.0125
D1	.400	.412	.500	.512	.620	.630	.602	.612
E	.335	.347	.335	.347	.335	.345	.335	.347
E1	.292	.300	.292	.300	.295	.305	.292	.299
E2	.262	.272	.262	.272	.260	.280	.262	.272
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC	
h	.010	.020	.010	.020	.010	.020	.010	.016
S	.023	.035	.023	.035	.032	.043	.032	.043

SMALL OUTLINE IC (Continued)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSION AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.

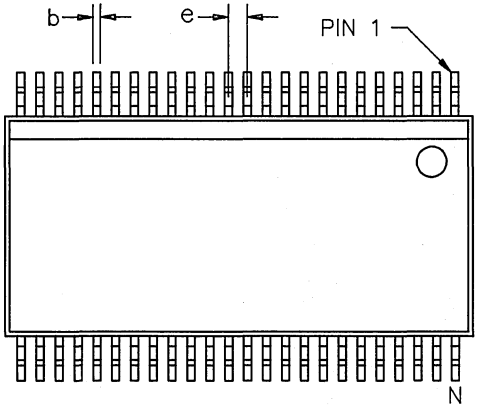


28–32 LEAD SMALL OUTLINE (J–BEND)

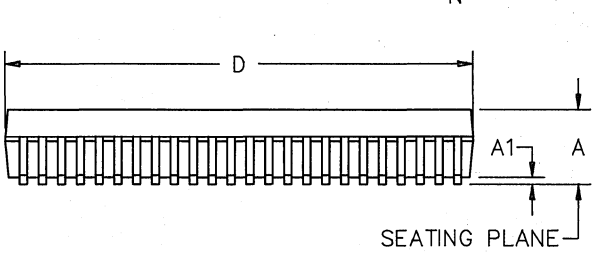
DWG #	SO28–5		SO28–4		SO32–2		SO32–3	
# OF LDS (N)	28 LD (.300")		28 LD (.350")		32 LD (.300")		32 LD (.400")	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.120	.140	.130	.148	.130	.148	.131	.145
A1	.078	.095	.082	.095	.082	.095	.045	.055
B	.020	.024	.026	.032	.026	.032	.026	.032
B1	.014	.020	.016	.020	.016	.020	.015	.020
C	.008	.013	.007	.011	.008	.013	.006	.0125
D1	.700	.712	.720	.730	.820	.830	.820	.830
E	.335	.347	.380	.390	.330	.340	.435	.445
E1	.292	.300	.345	.355	.295	.305	.395	.405
E2	.262	.272	.310	.330	.260	.275	.360	.380
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC	
h	.012	.020	.012	.020	.012	.020	–	–
S	.023	.035	.023	.035	.032	.043	.032	.043

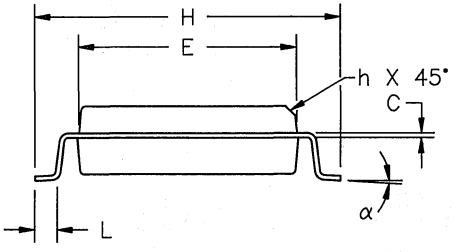
SMALL OUTLINE IC (Continued)

48 & 56 LEAD SMALL OUTLINE (SSOP – JEDEC)



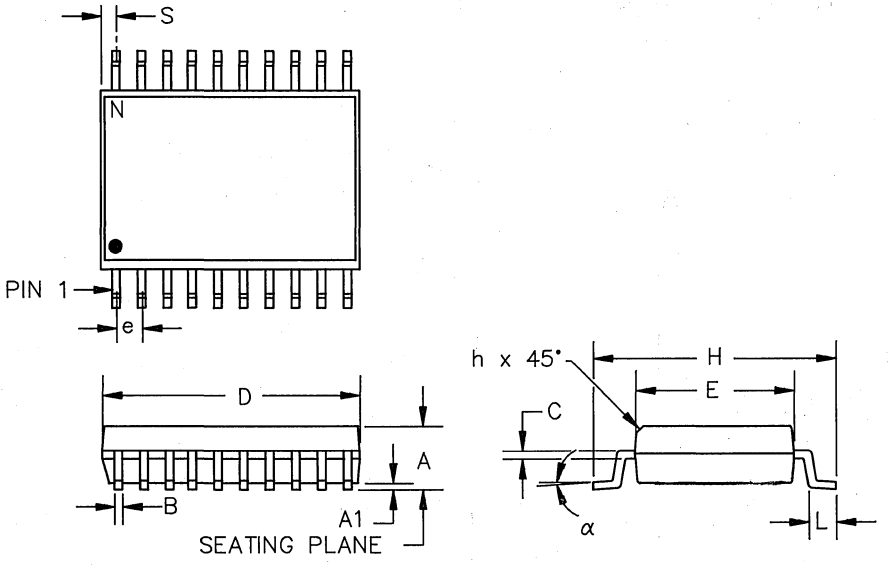
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.





DWG #	SO48–1		SO56–1	
# OF LDS (N)	48 (.300")		56 (.300")	
SYMBOL	MIN	MAX	MIN	MAX
A	.095	.110	.095	.110
A1	.008	.016	.008	.016
b	.008	.012	.008	.012
C	.005	.009	.005	.009
D	.620	.630	.720	.730
E	.291	.299	.291	.299
e	.025 BSC		.025 BSC	
H	.395	.420	.395	.420
h	.015	.025	.015	.025
L	.020	.040	.020	.040
α	0°	8°	0°	8°

SMALL OUTLINE IC (Continued)



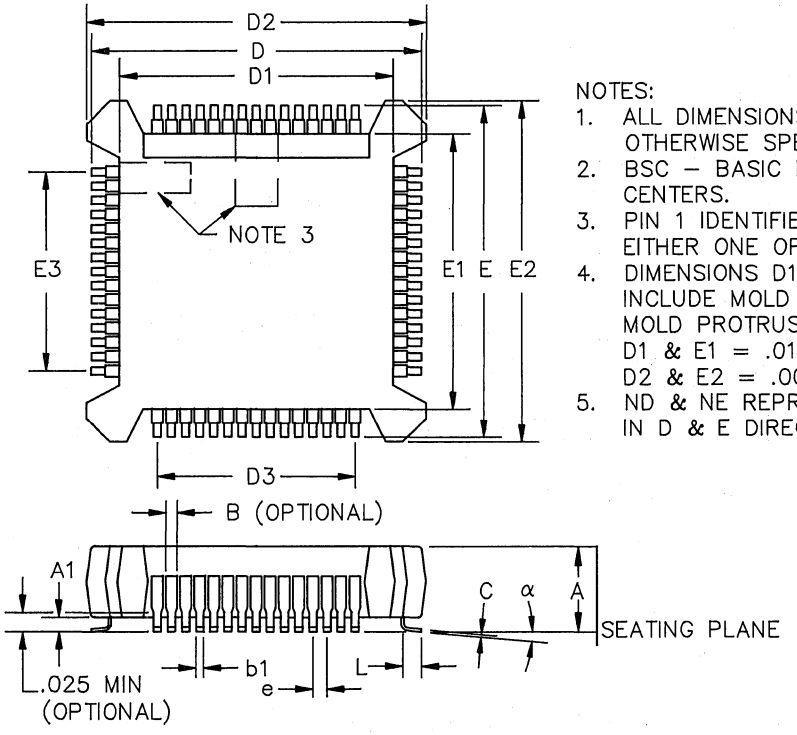
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.

20 & 24 LEAD SMALL OUTLINE (SSOP – EIAJ)

DWG #	SO20-7		SO24-7	
# OF LDS (N)	20		24	
SYMBOLS	MIN	MAX	MIN	MAX
A	.068	.078	.068	.078
A1	.002	.008	.002	.008
B	.010	.015	.010	.015
C	.005	.009	.005	.009
D	.278	.289	.318	.328
E	.205	.212	.205	.212
e	.025 BSC		.025 BSC	
H	.301	.311	.301	.311
L	.022	.037	.022	.037
α	0°	8°	0°	8°

PLASTIC QUAD FLATPACKS

100–132 LEAD PLASTIC QUAD FLATPACK (JEDEC)

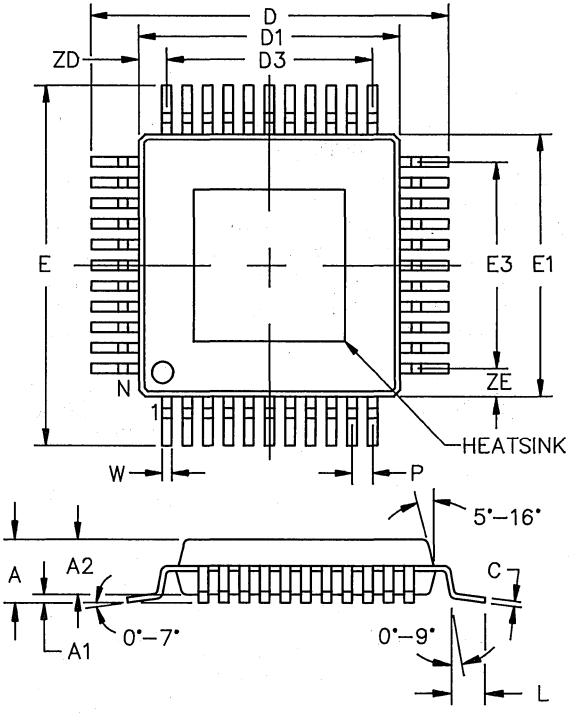


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. PIN 1 IDENTIFIER CAN BE POSITIONED AT EITHER ONE OF THESE TWO LOCATIONS.
4. DIMENSIONS D1, D2, E1, AND E2 DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE MOLD PROTRUSIONS ARE AS FOLLOWS:
   D1 & E1 = .010 MAX.
   D2 & E2 = .007 MAX.
5. ND & NE REPRESENT NUMBERS OF LEADS IN D & E DIRECTIONS RESPECTIVELY.

DWG #	PQ100–1		PQ132–1	
# OF LDS (N)	100		132	
SYMBOLS	MIN	MAX	MIN	MAX
A	.160	.180	.160	.180
A1	.020	.040	.020	.040
B	.008	.016	.008	.016
b1	.008	.012	.008	.012
C	.0055	.008	.0055	.008
D	.875	.885	1.075	1.085
D1	.747	.753	.947	.953
D2	.897	.903	1.097	1.103
D3	.600 REF		.800 REF	
e	.025 BSC		.025 BSC	
E	.875	.885	1.075	1.085
E1	.747	.753	.947	.953
E2	.897	.903	1.097	1.103
E3	.600 REF		.800 REF	
L	.020	.030	.020	.030
α	0°	8°	0°	8°
ND/NE	25/25		33/33	

PLASTIC QUAD FLATPACKS (Continued)

80–128 LEAD PLASTIC QUAD FLATPACK (EIAJ)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .010 PER SIDE.
4. ND & NE REPRESENT NUMBERS OF LEADS IN D & E DIRECTIONS RESPECTIVELY.

DWG #	PQ80–2		PQ100–2		PQ120–2		PQ128–2	
# OF LDS (N)	80		100		120		128	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.110	.124	.110	.124	.136	.156	.136	.156
A1	.010	–	.010	–	.010	–	.010	–
A2	.100	.120	.100	.120	.125	.144	.125	.144
C	.005	.008	.005	.008	.005	.008	.005	.008
D	.937	.945	.937	.945	1.252	1.260	1.252	1.260
D1	.783	.791	.783	.791	1.098	1.106	1.098	1.106
D3	.724 REF		.742 REF		.913 REF		.976 REF	
E	.701	.709	.701	.709	1.252	1.260	1.252	1.260
E1	.547	.555	.547	.555	1.098	1.106	1.098	1.106
E3	.472 REF		.486 REF		.913 REF		.976 REF	
L	.026	.037	.026	.037	.026	.037	.026	.037
ND/NE	16/24		20/30		30/30		32/32	
P	.0315 BSC		.026 BSC		.026 BSC		.0315 BSC	
W	.012	.018	.012	.018	.012	.018	.012	.018
ZD	.032		.023		.094		.063	
ZE	.039		.032		.094		.063	

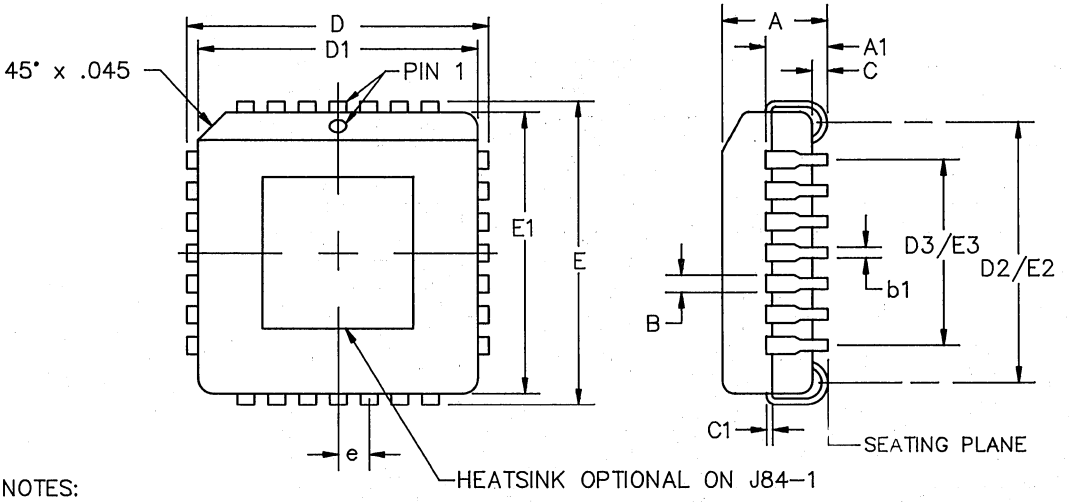
PLASTIC QUAD FLATPACKS (Continued)

144–208 LEAD PLASTIC QUAD FLATPACK (EIAJ)

DWG #	PQ144–2		PQ160–2		PQ184–2		PQ208–2	
# OF LDS (N)	144		160		184		208	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.136	.156	.136	.156	.136	.156	.136	.156
A1	.010	–	.010	–	.010	–	.010	–
A2	.125	.144	.125	.144	.125	.144	.125	.144
C	.005	.008	.005	.008	.005	.008	.005	.008
D	1.252	1.260	1.252	1.260	1.252	1.260	1.252	1.260
D1	1.098	1.106	1.098	1.106	1.098	1.106	1.098	1.106
D3	.896 REF		.998 REF		.886 REF		1.004 REF	
E	1.252	1.260	1.252	1.260	1.252	1.260	1.252	1.260
E1	1.098	1.106	1.098	1.106	1.098	1.106	1.098	1.106
E3	.896 REF		.998 REF		.886 REF		1.004 REF	
L	.026	.037	.026	.037	.026	.037	.026	.037
ND/NE	36/36		40/40		46/46		52/52	
P	.026 BSC		.026 BSC		.020 BSC		.020 BSC	
W	.009	.014	.009	.014	.009	.014	.009	.014
ZD	.103		.052		.108		.049	
ZE	.103		.052		.108		.049	

PLASTIC LEADED CHIP CARRIERS

20–84 LEAD PLCC (SQUARE)



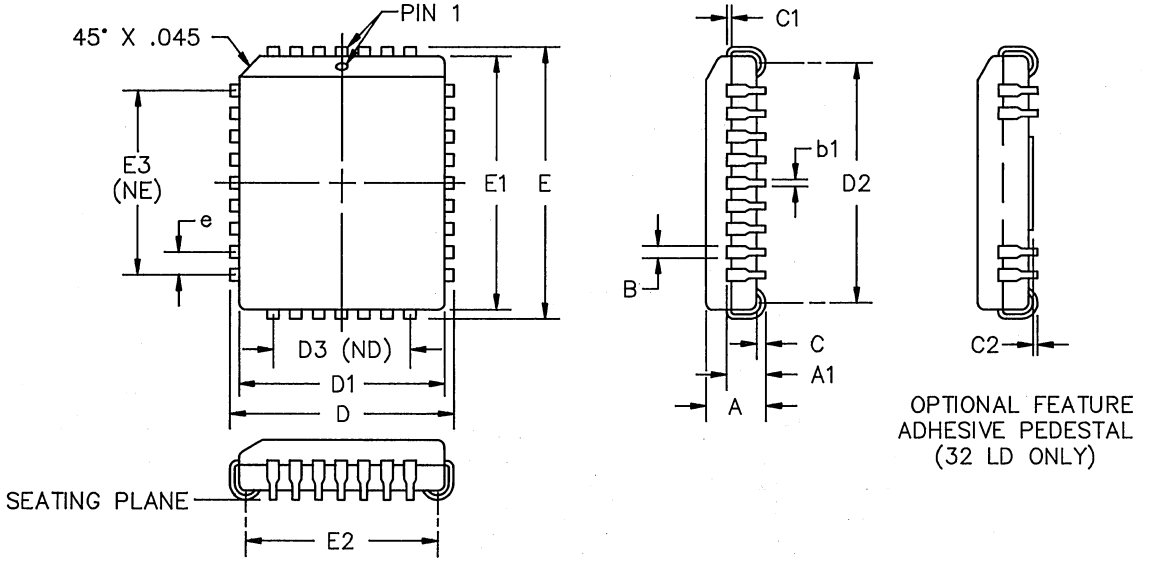
NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.
5. ND & NE REPRESENT NUMBER OF LEADS IN D & E DIRECTIONS RESPECTIVELY.
6. D1 & E1 SHOULD BE MEASURED FROM THE BOTTOM OF THE PKG.

DWG #	J20–1		J28–1		J44–1		J52–1		J68–1		J84–1	
# OF LDS	20		28		44		52		68		84	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.165	.180	.165	.180	.165	.180	.165	.180	.165	.180	.165	.180
A1	.095	.115	.095	.115	.095	.115	.095	.115	.095	.115	.095	.115
B	.026	.032	.026	.032	.026	.032	.026	.032	.026	.032	.026	.032
b1	.013	.021	.013	.021	.013	.021	.013	.021	.013	.021	.013	.021
C	.020	.040	.020	.040	.020	.040	.020	.040	.020	.040	.020	.040
C1	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012
D	.385	.395	.485	.495	.685	.695	.785	.795	.985	.995	1.185	1.195
D1	.350	.356	.450	.456	.650	.656	.750	.756	.950	.956	1.150	1.156
D2/E2	.290	.330	.390	.430	.590	.630	.690	.730	.890	.930	1.090	1.130
D3/E3	.200 REF		.300 REF		.500 REF		.600 REF		.800 REF		1.000 REF	
E	.385	.395	.485	.495	.685	.695	.785	.795	.985	.995	1.185	1.195
E1	.350	.356	.450	.456	.650	.656	.750	.756	.950	.956	1.150	1.156
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
ND/NE	5		7		11		13		17		21	

PLASTIC LEADED CHIP CARRIERS (Continued)

18–32 LEAD PLCC (RECTANGULAR)

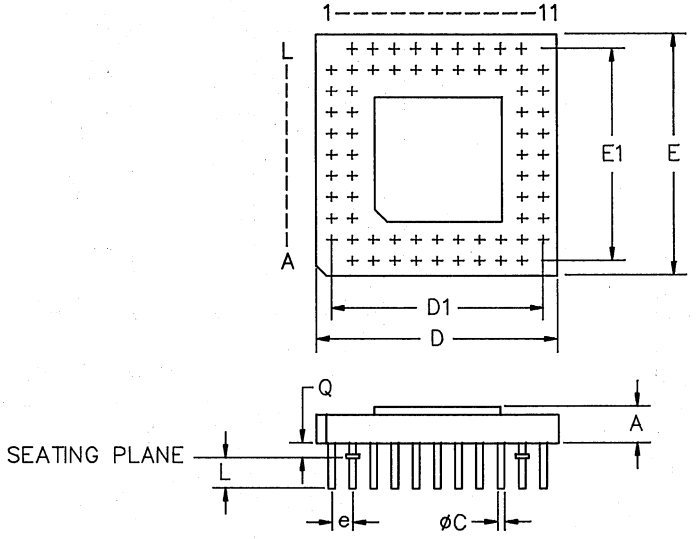


DWG #	J18–1		J32–1	
# OF LDS	18		32	
SYMBOL	MIN	MAX	MIN	MAX
A	.120	.140	.120	.140
A1	.075	.095	.075	.095
B	.026	.032	.026	.032
b1	.013	.021	.013	.021
C	.015	.040	.015	.040
C1	.008	.012	.008	.012
C2	–	–	.005	.015
D	.320	.335	.485	.495
D1	.289	.293	.449	.453
D2	.225	.265	.390	.430
D3	.150 REF		.300 REF	
E	.520	.535	.585	.595
E1	.489	.493	.549	.553
E2	.422	.465	.490	.530
E3	.200 REF		.400 REF	
e	.050 BSC		.050 BSC	
ND/NE	4 / 5		7 / 9	

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.
5. ND & NE REPRESENT NUMBERS OF LEADS IN D & E DIRECTIONS RESPECTIVELY.
6. D1 & E1 SHOULD BE MEASURED FROM THE BOTTOM OF THE PACKAGE.

PLASTIC PIN GRID ARRAYS

68–208 PIN PGA (CAVITY UP)



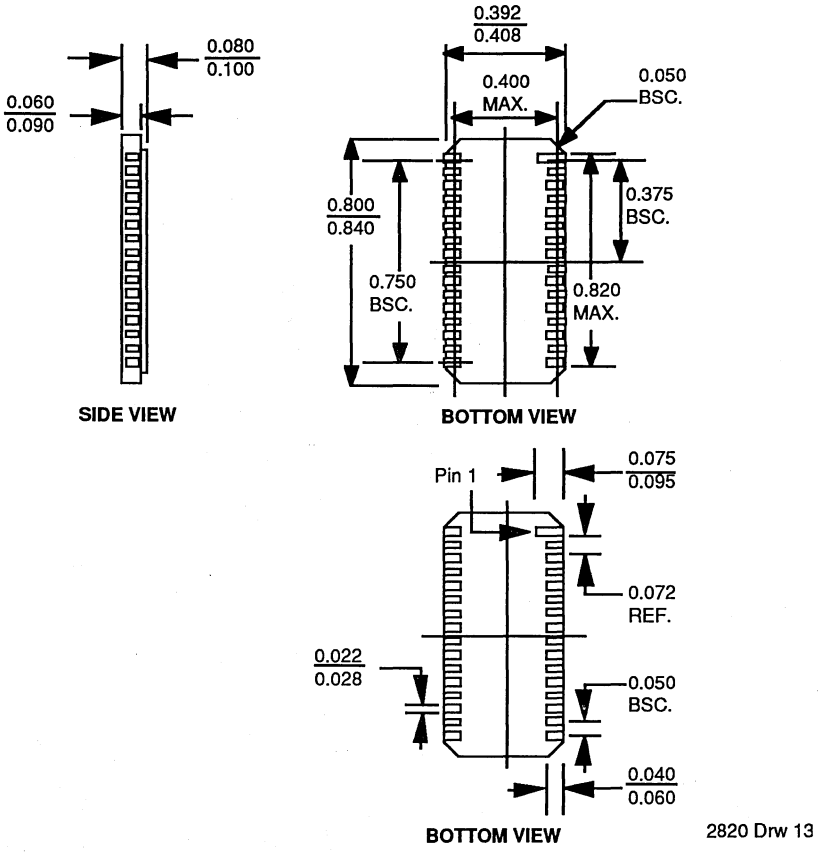
NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC PIN SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS.
5. DIM. "A" INCLUDES BOTH THE PKG BODY & THE LID. IT DOES NOT INCLUDE HEATSINK OR OTHER ATTACHED FEATURES.
6. PIN DIAMETER "C" EXCLUDES SOLDER DIP OR OTHER LEAD FINISH.
7. PIN TIPS MAY HAVE RADIUS OR CHAMFER.

DWG No.	PG 68–2		PG 84–2		PG 208–2	
# OF PINS (N)	68 PIN		84 PIN		208 PIN	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX
A	.115	.160	.115	.160	.115	.160
C	.016	.020	.016	.020	.016	.020
D	1.140	1.180	1.140	1.180	1.740	1.780
D1	1.000 BSC		1.000 BSC		1.600 BSC	
E	1.140	1.180	1.140	1.180	1.740	1.780
E1	1.000 BSC		1.000 BSC		1.600 BSC	
e	.100 BSC		.100 BSC		.100 BSC	
L	.100	.160	.100	.160	.100	.160
M	11		11		17	
Q	.040	.070	.040	.070	.040	.070

LEADLESS CHIP CARRIER PACKAGES

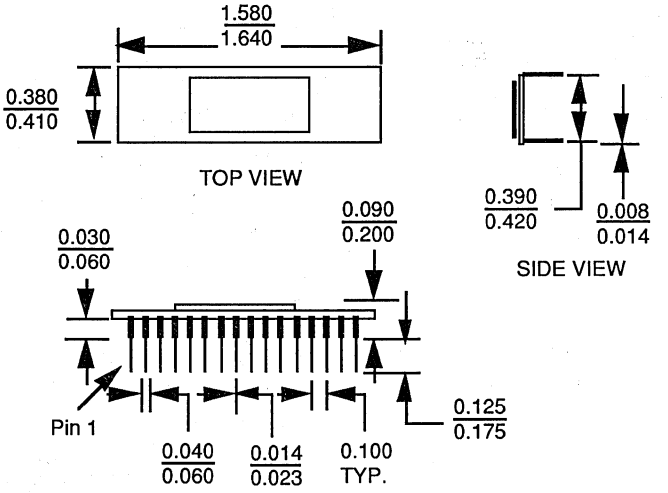
32Pin 0.400mil x 0.820mil LCC – M1



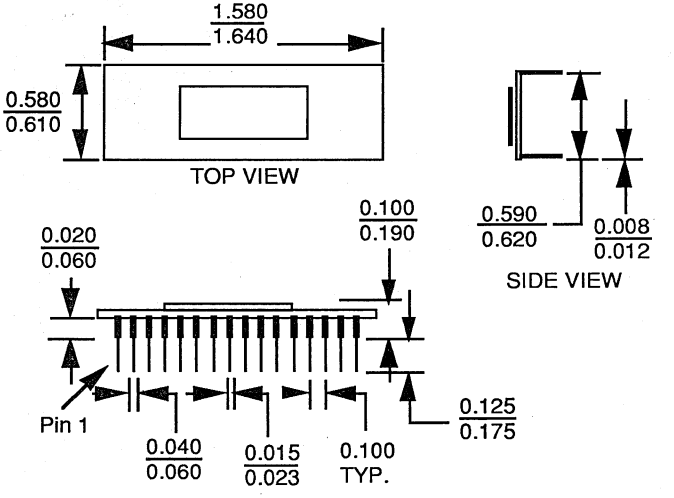
2820 Drw 13

DUAL IN-LINE PACKAGES

32-Pin 400mil Ceramic Sidebraze DIP – M2

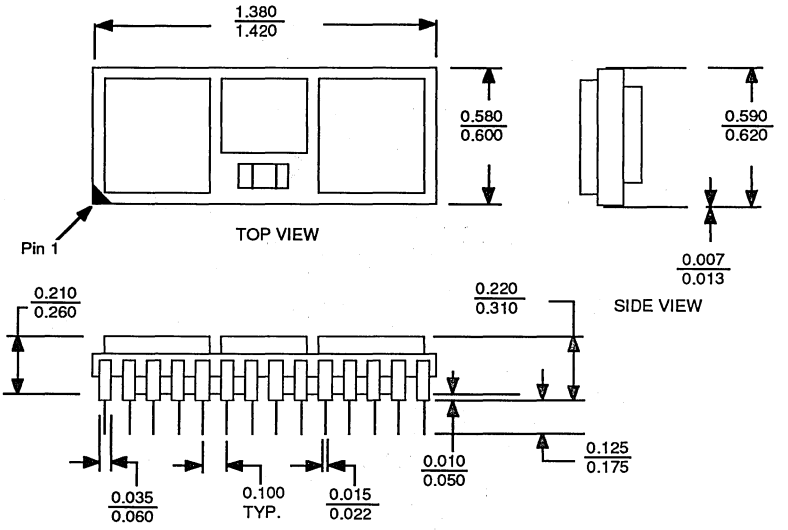


32-Pin 600mil Ceramic Sidebraze DIP – M3

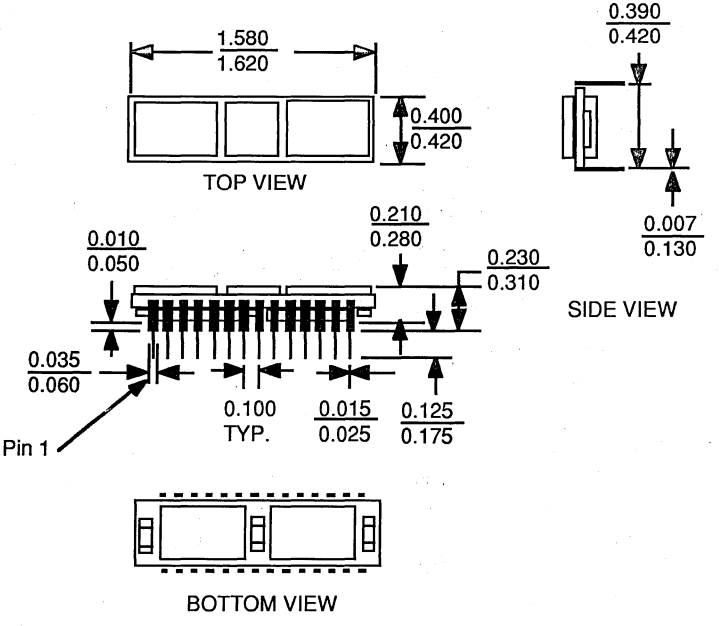


DUAL IN-LINE PACKAGES

28-Pin Ceramic Sidebraze DIP – M4

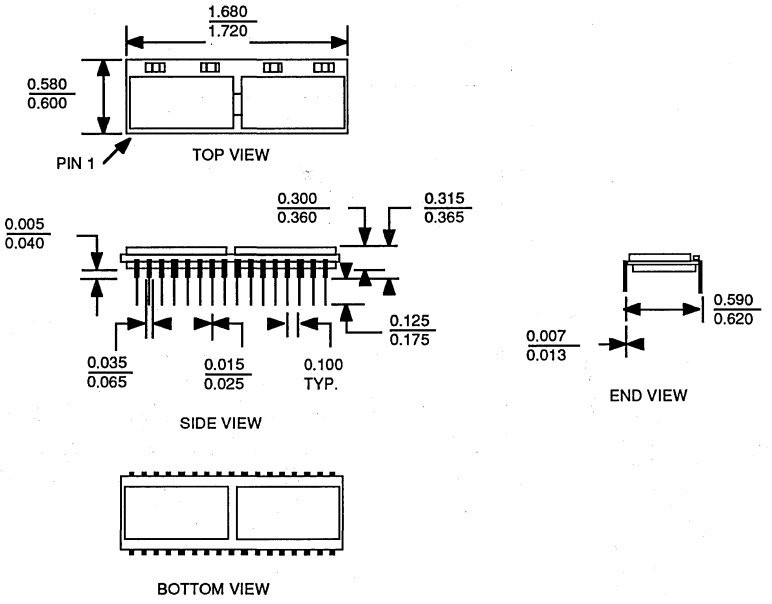


28-Pin Ceramic Sidebraze DIP – M5

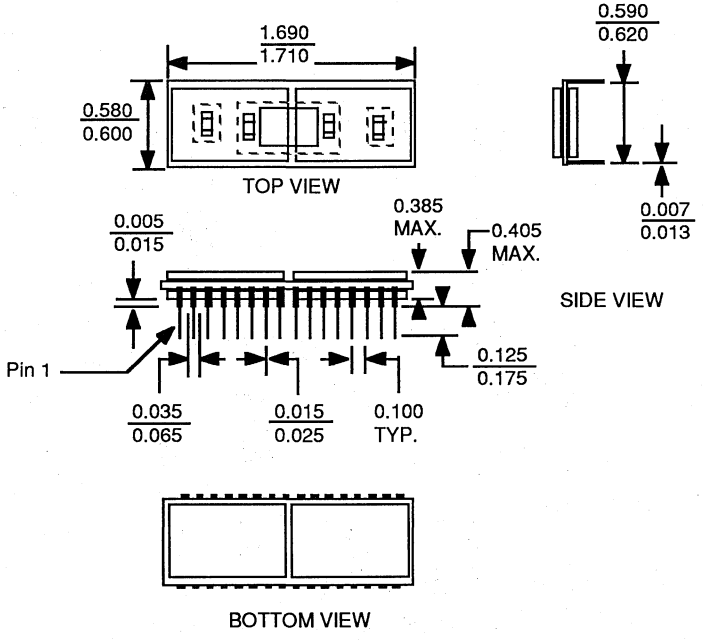


DUAL IN-LINE PACKAGES (Continued)

32-Pin Ceramic Sidebraze DIP – M6

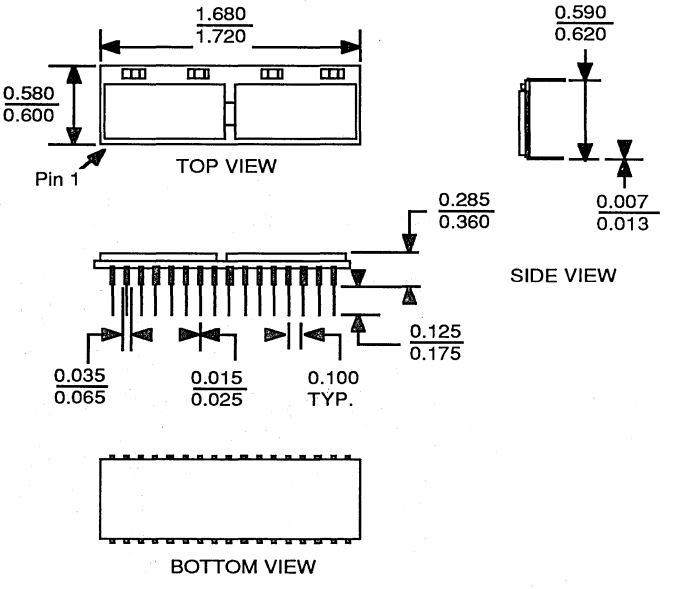


32-Pin Ceramic Sidebraze DIP – M7

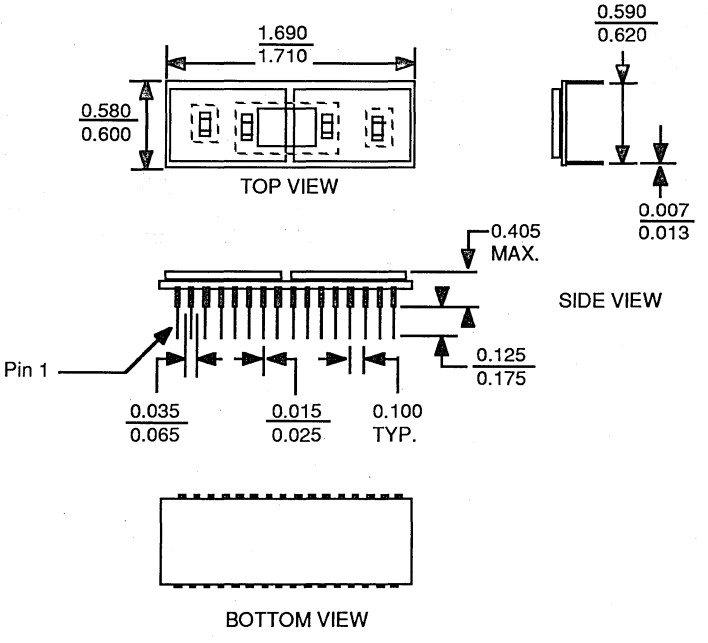


DUAL IN-LINE PACKAGES (Continued)

32-Pin Ceramic Sidebraze DIP – M8

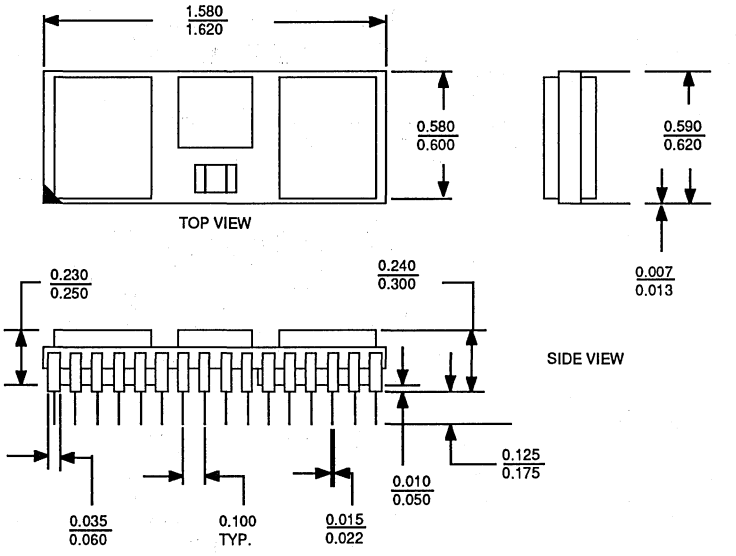


32-Pin Ceramic Sidebraze DIP – M9

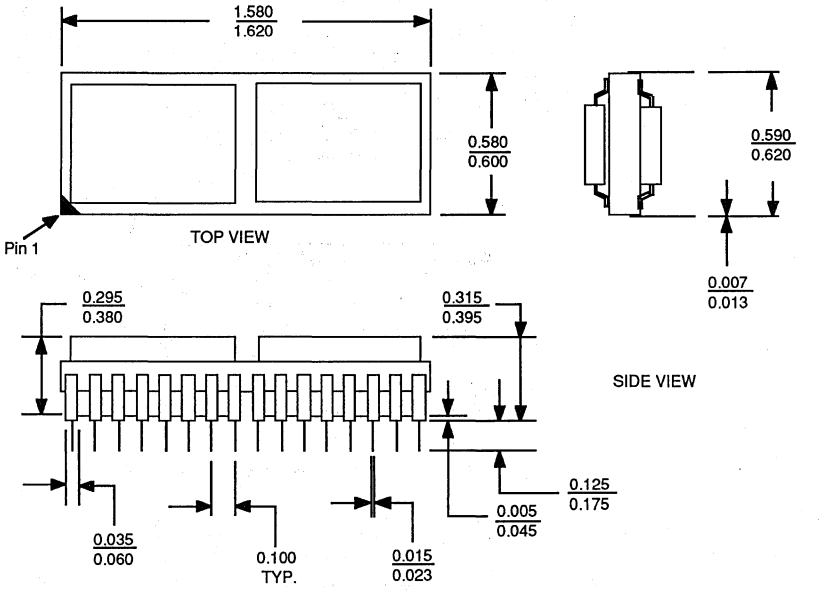


DUAL IN-LINE PACKAGES (Continued)

32-Pin Ceramic Sidebraze DIP – M10

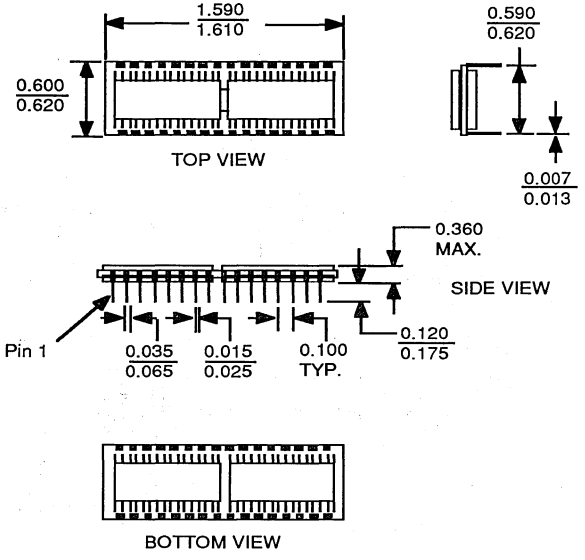


32-Pin Ceramic Sidebraze DIP – M11

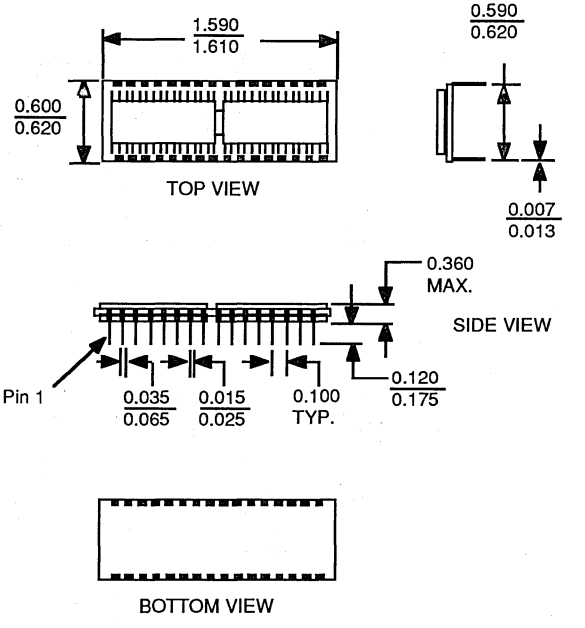


DUAL IN-LINE PACKAGES (Continued)

32-Pin FR-4 Plastic DIP – M12

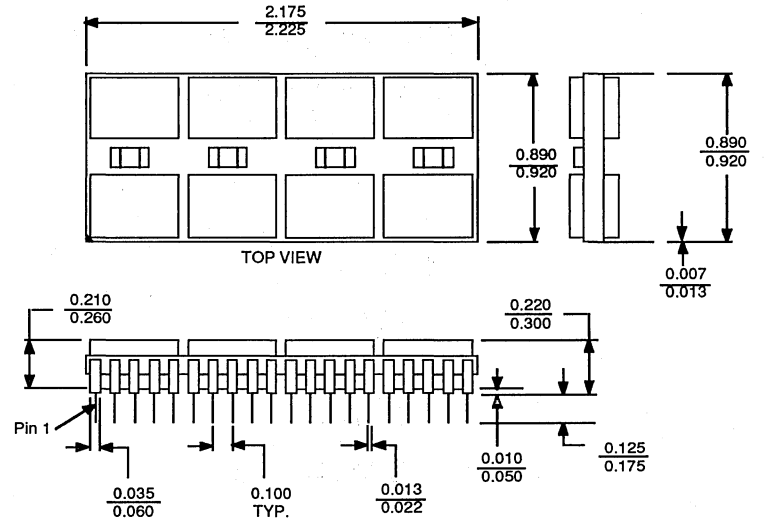


32-Pin FR-4 Plastic DIP – M13

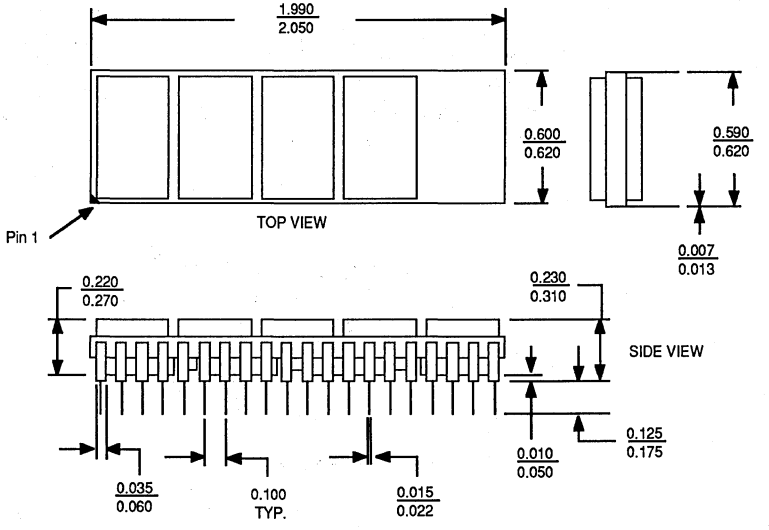


DUAL IN-LINE PACKAGES (Continued)

40-Pin Ceramic Sidebraze DIP – M14

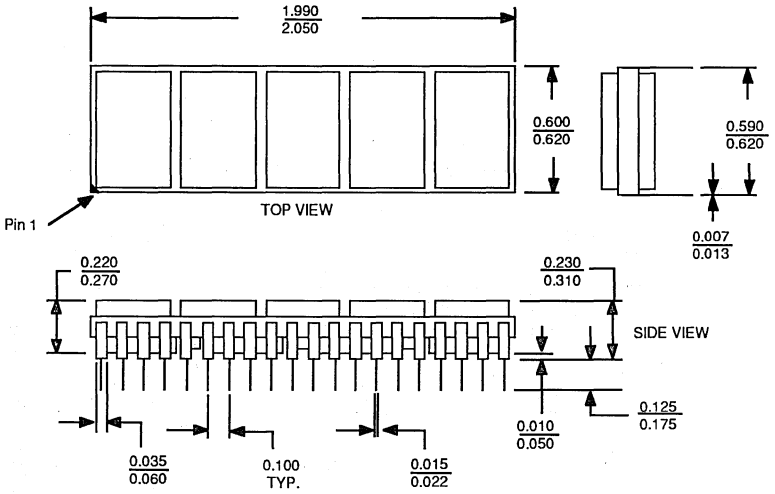


40-Pin Ceramic Sidebraze DIP – M15

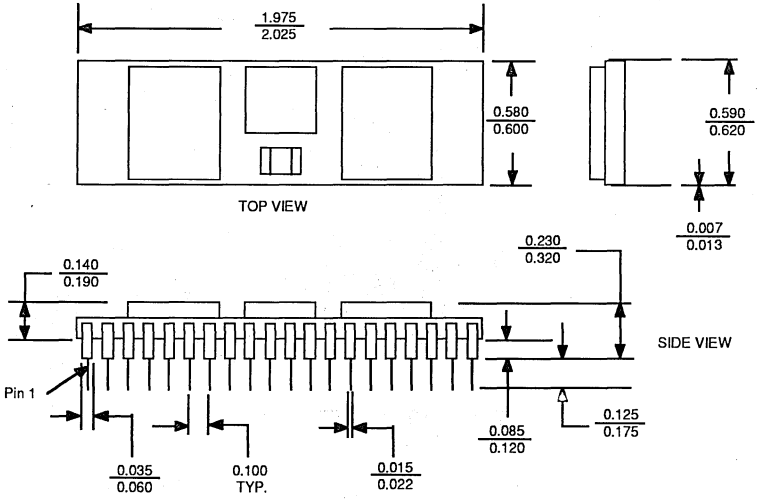


DUAL IN-LINE PACKAGES (Continued)

40-Pin Ceramic Sidebraze DIP – M16

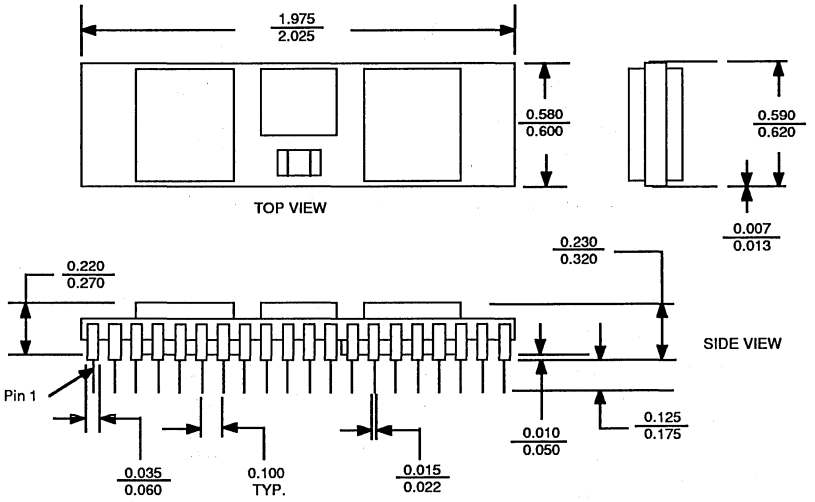


40-Pin Ceramic Sidebraze DIP – M17

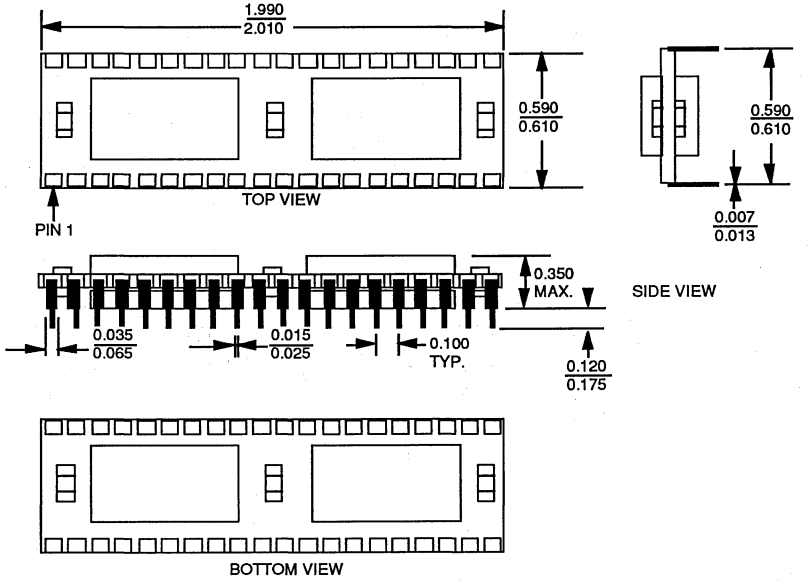


DUAL IN-LINE PACKAGES (Continued)

40-Pin Ceramic Sidebraze DIP – M18

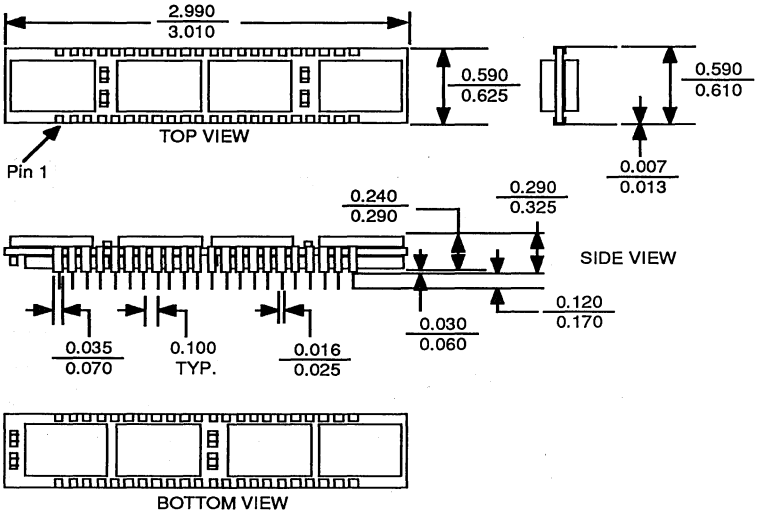


40-Pin FR-4 Plastic DIP – M19

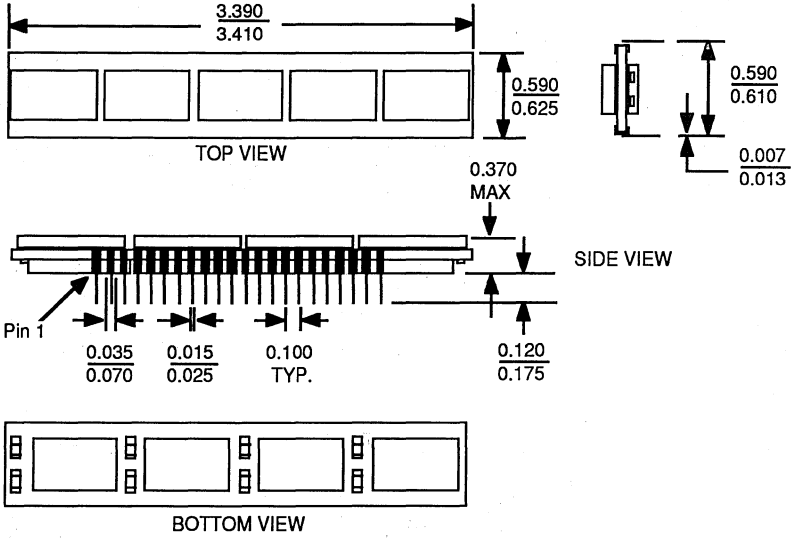


DUAL IN-LINE PACKAGES (Continued)

44-Pin FR-4 Plastic DIP – M20

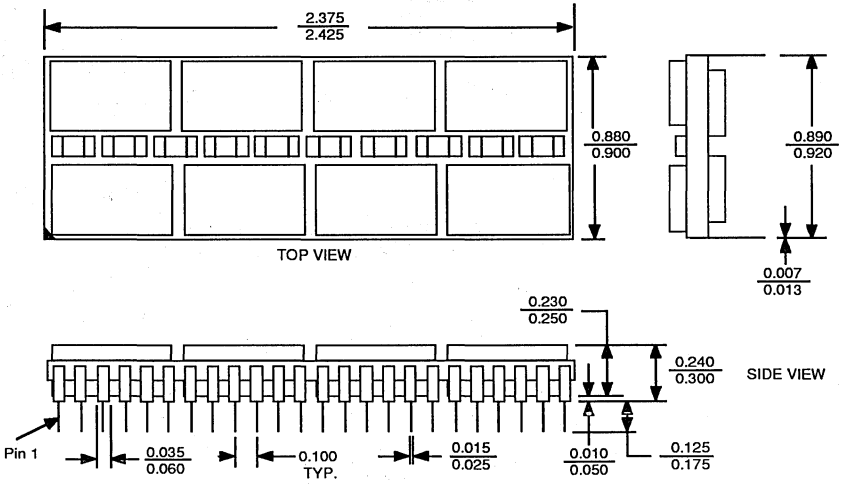


44-Pin FR-4 Plastic DIP – M21

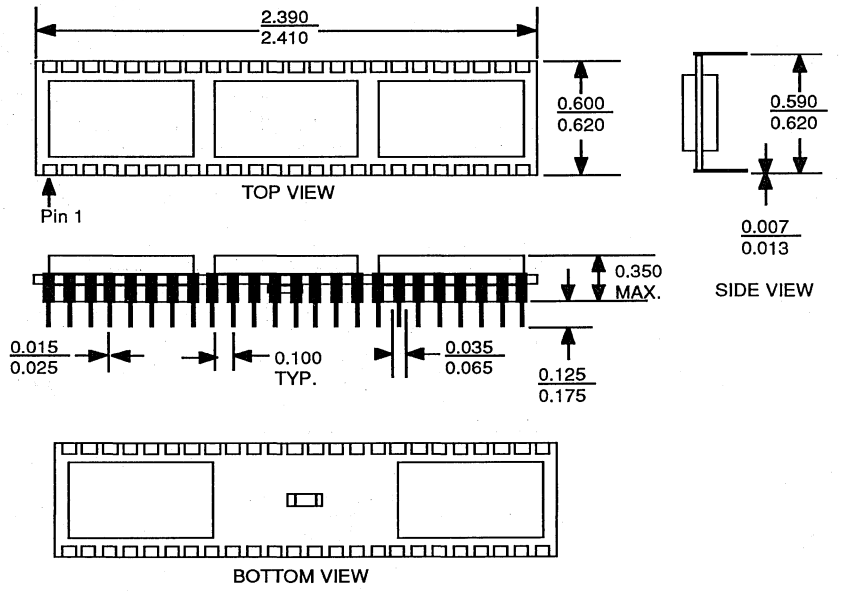


DUAL IN-LINE PACKAGES (Continued)

48-Pin Ceramic Sidebraze DIP – M22

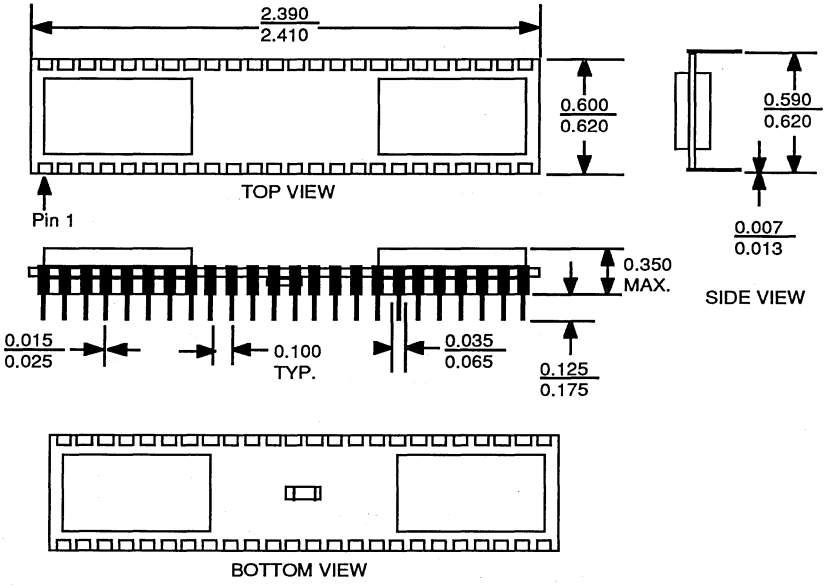


48-Pin FR-4 Plastic DIP – M23

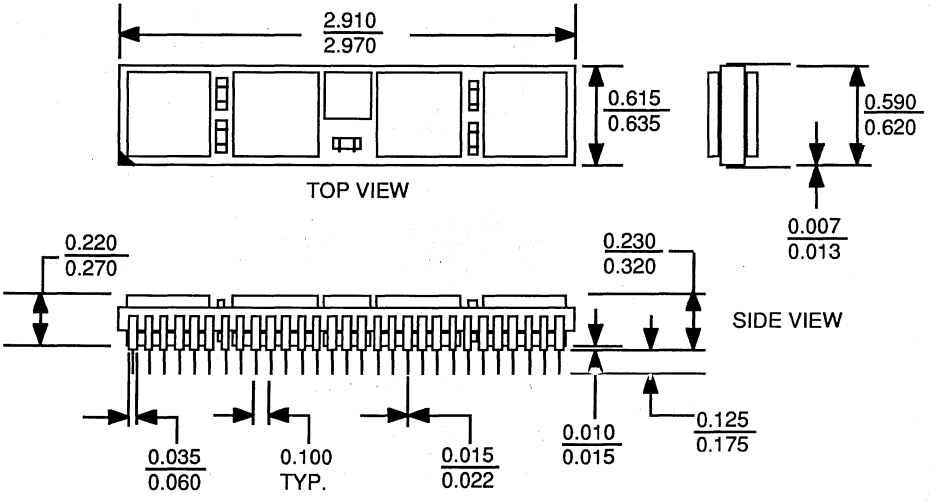


DUAL IN-LINE PACKAGES (Continued)

48-Pin FR-4 Plastic DIP – M24

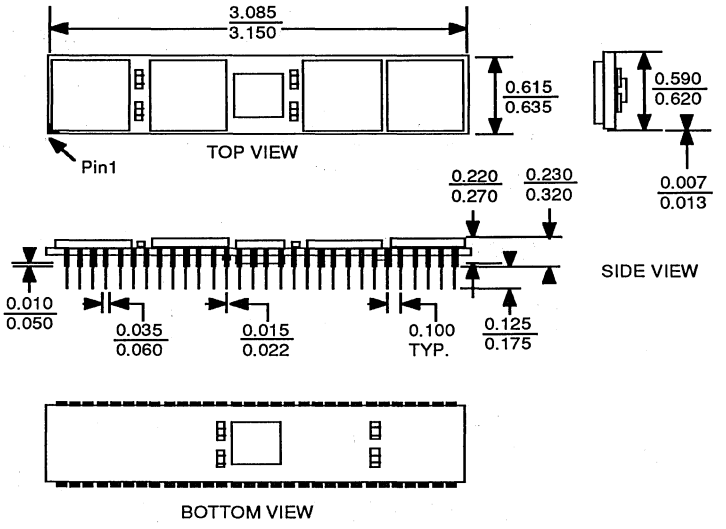


58-Pin Ceramic Sidebraze DIP – M25

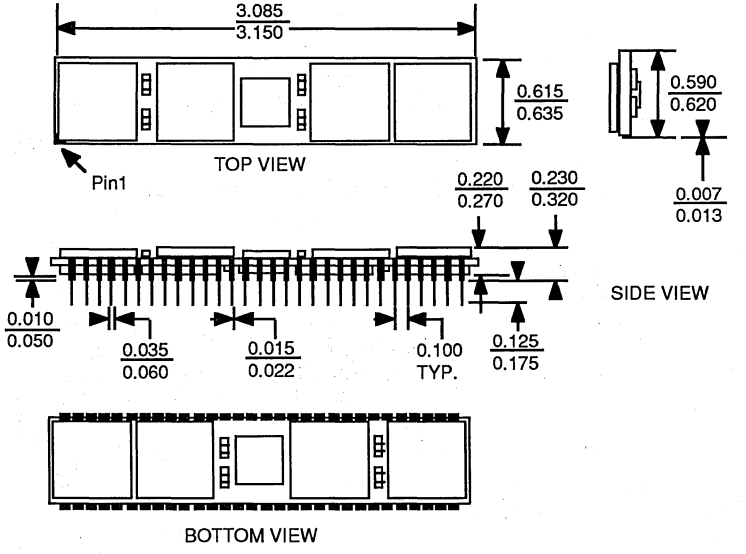


DUAL IN-LINE PACKAGES (Continued)

60-Pin Ceramic Sidebraze DIP – M26

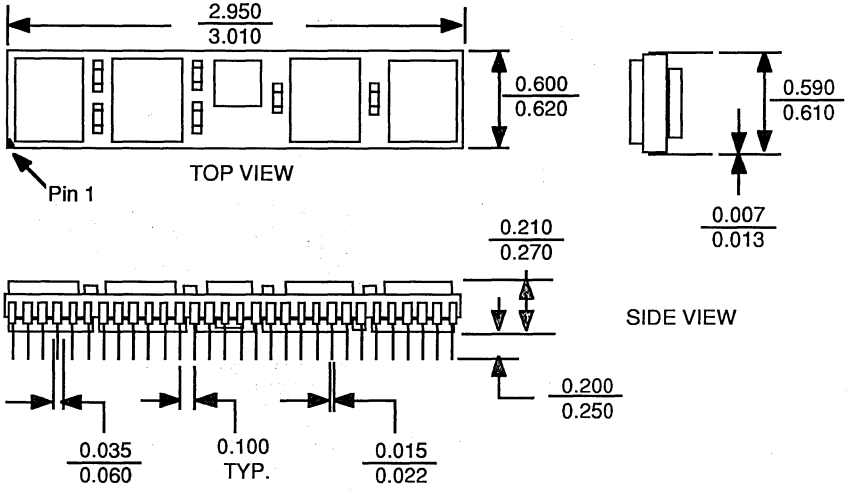


60-Pin Ceramic Sidebraze DIP – M27

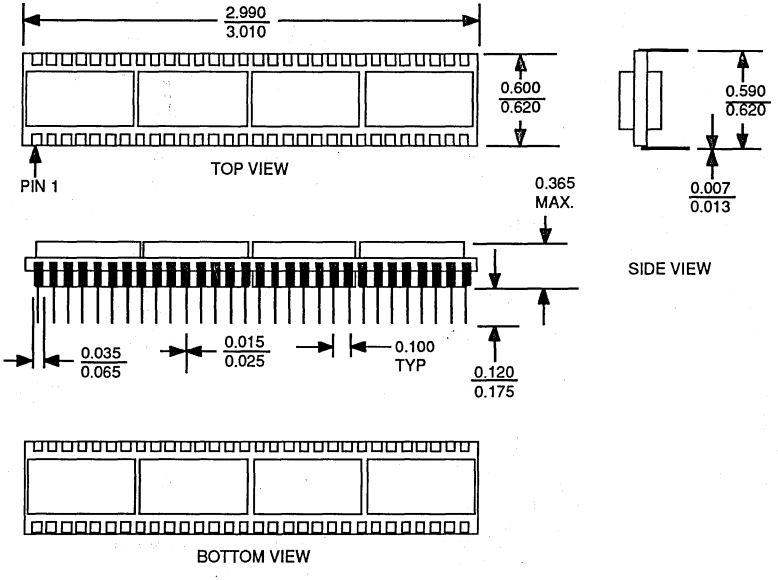


DUAL IN-LINE PACKAGES (Continued)

60-Pin Ceramic Sidebraze DIP – M28

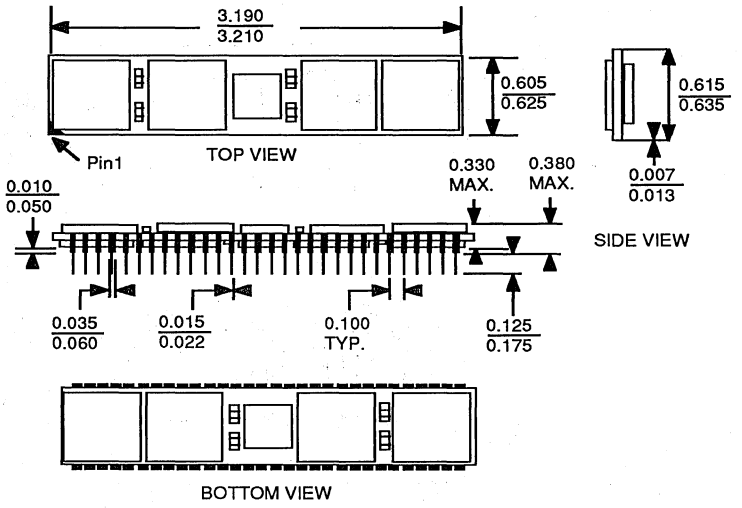


60-Pin FR-4 Plastic DIP – M29

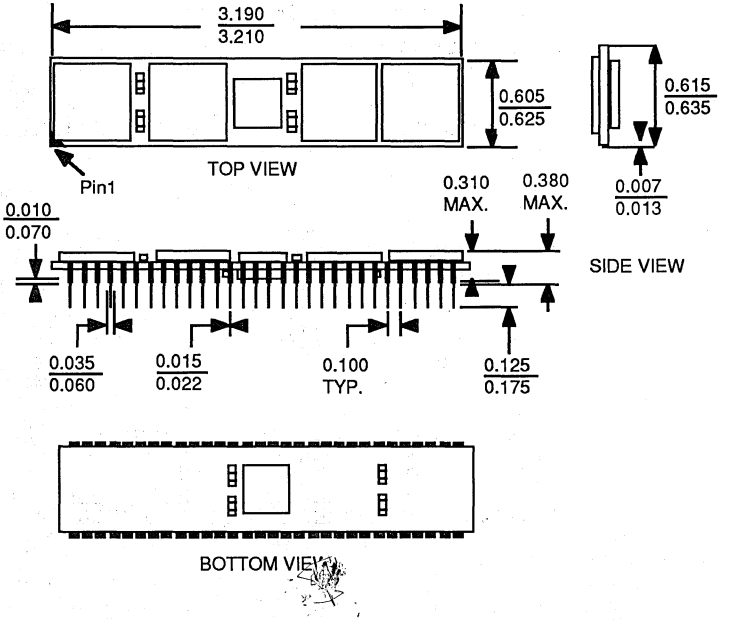


DUAL IN-LINE PACKAGES (Continued)

64-Pin Ceramic Sidebraze DIP – M30

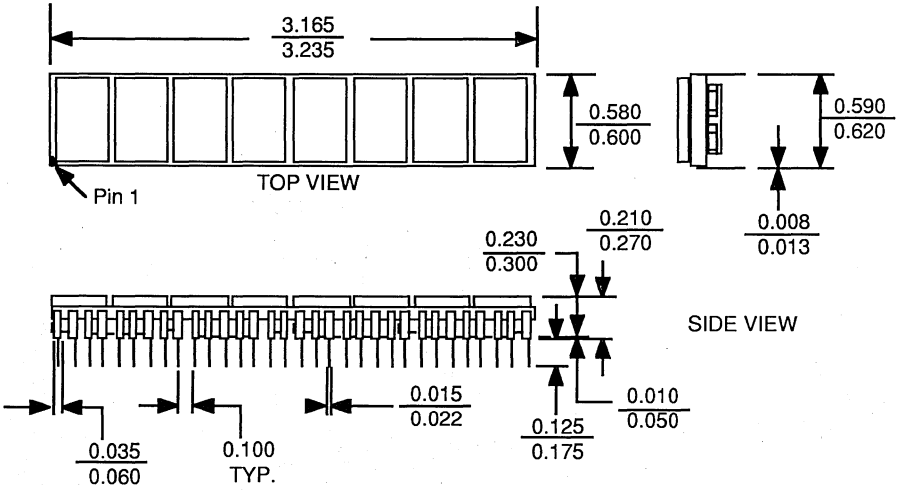


64-Pin Ceramic Sidebraze DIP – M31



DUAL IN-LINE PACKAGES (Continued)

64-Pin Ceramic Sidebraze DIP – M32



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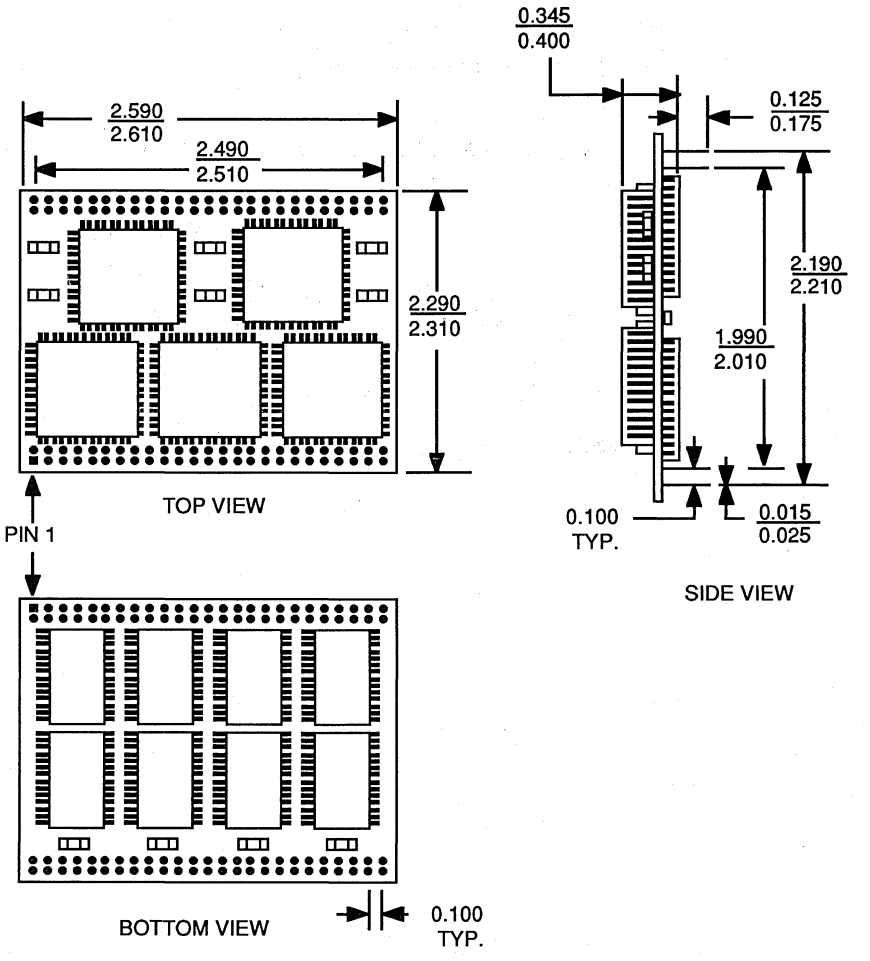
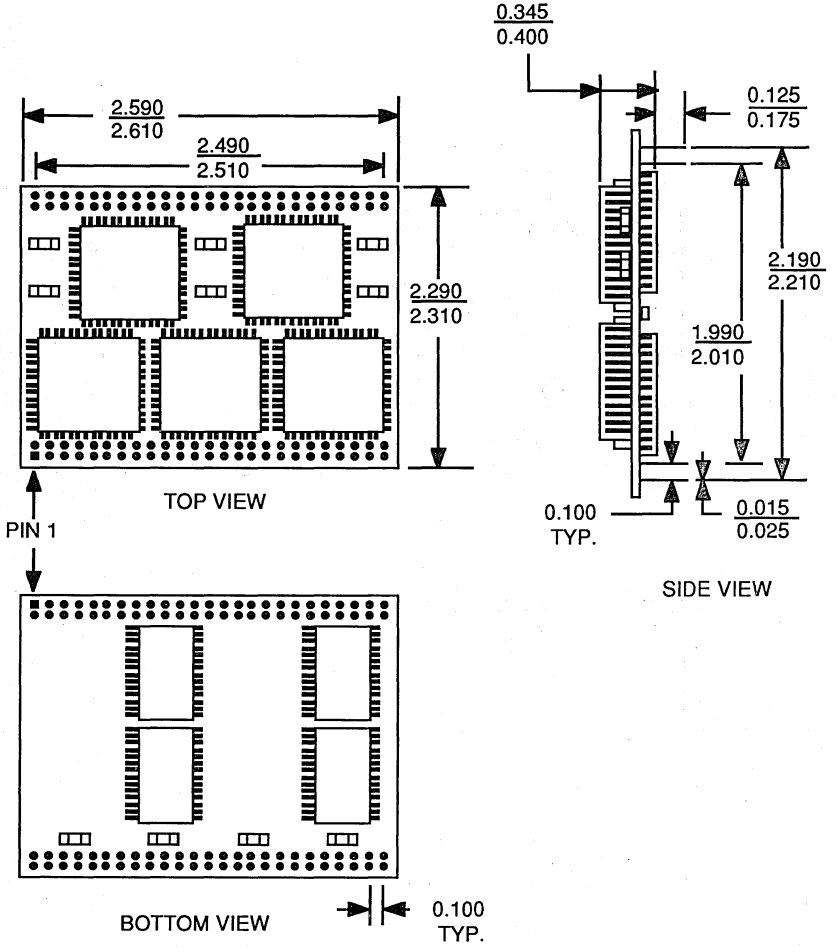
QUAD IN-LINE PACKAGES

100-Pin FR-4 Plastic QIP – M33



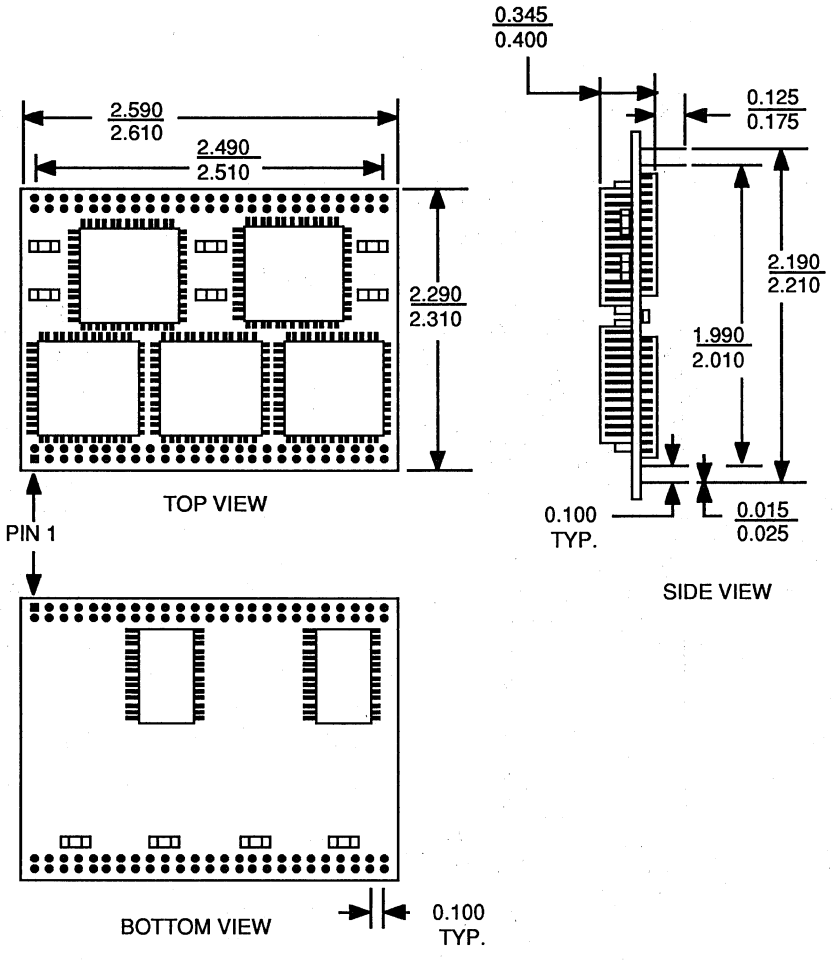
QUAD IN-LINE PACKAGES (Continued)

100-Pin FR-4 Plastic QIP – M34



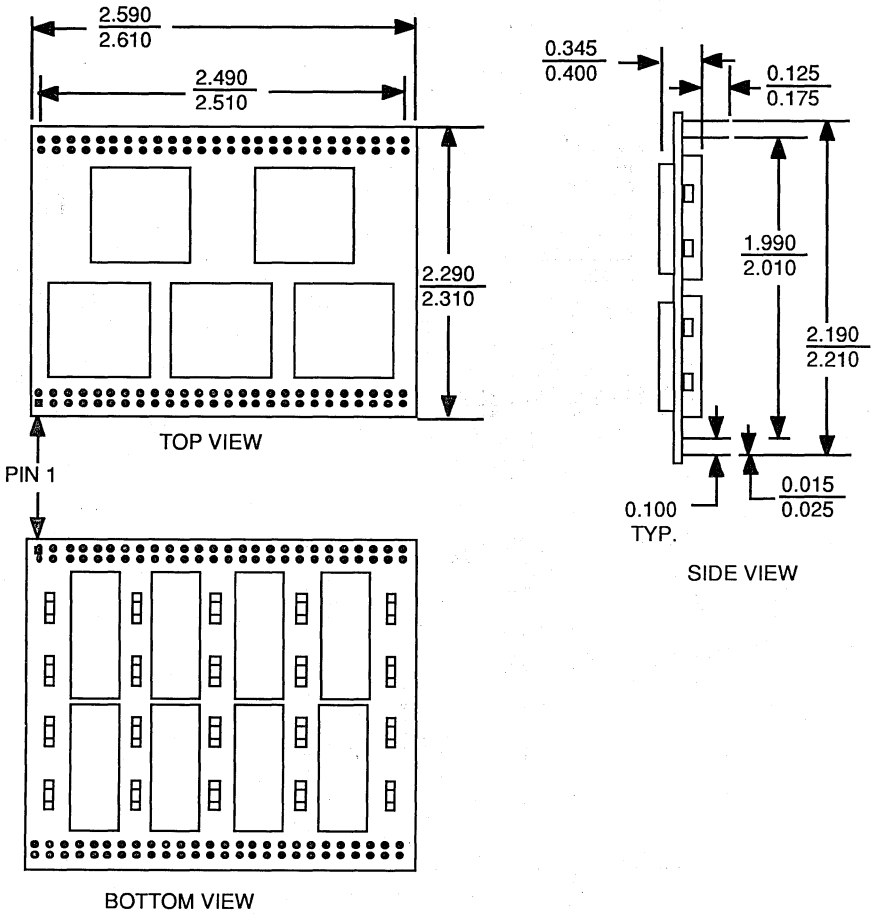
QUAD IN-LINE PACKAGES (Continued)

100-Pin FR-4 Plastic QIP – M35



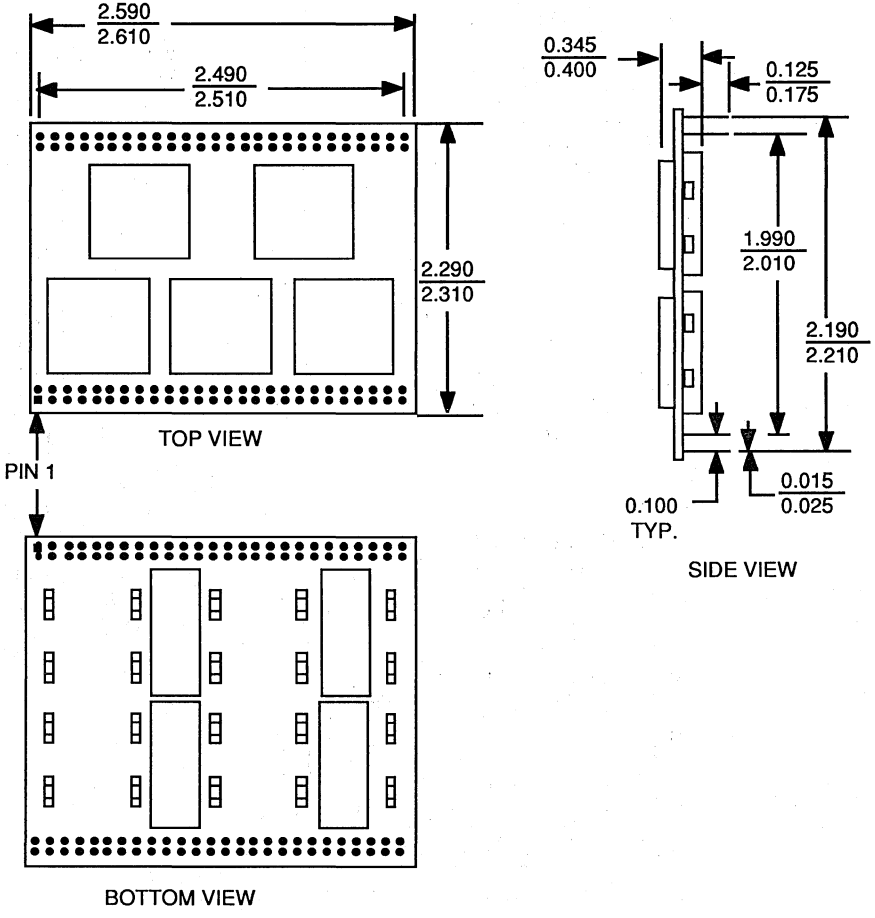
QUAD IN-LINE PACKAGES (Continued)

104-Pin FR-4 Plastic QIP – M36



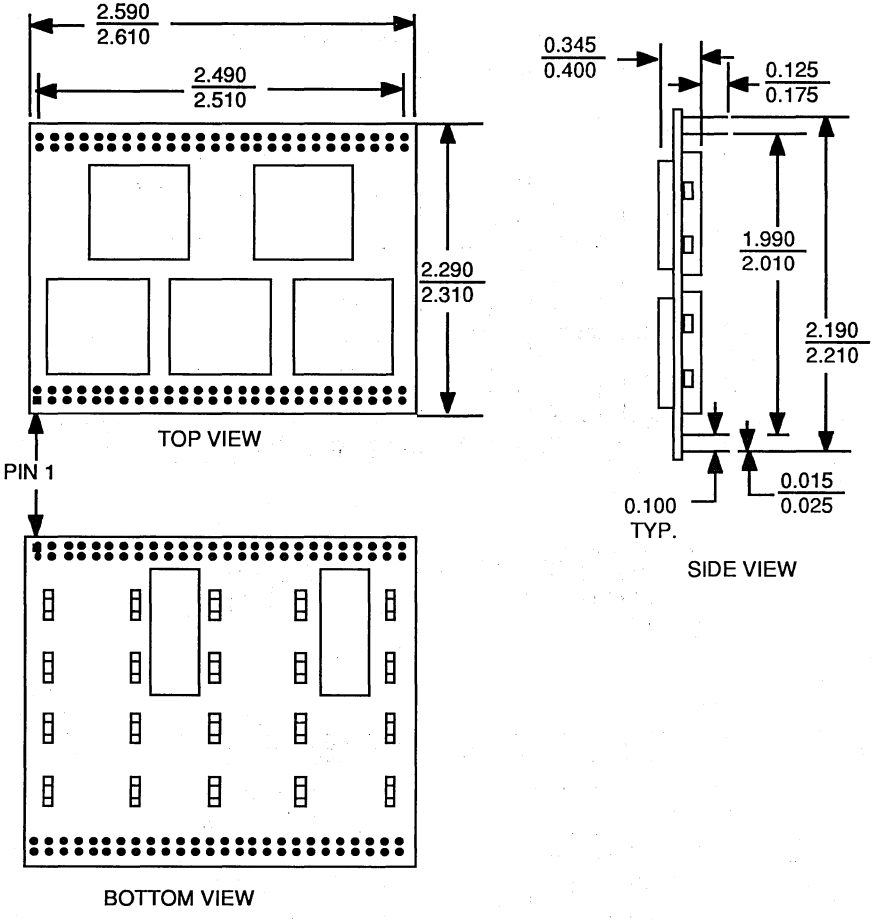
QUAD IN-LINE PACKAGES (Continued)

104-Pin FR-4 Plastic QIP – M37



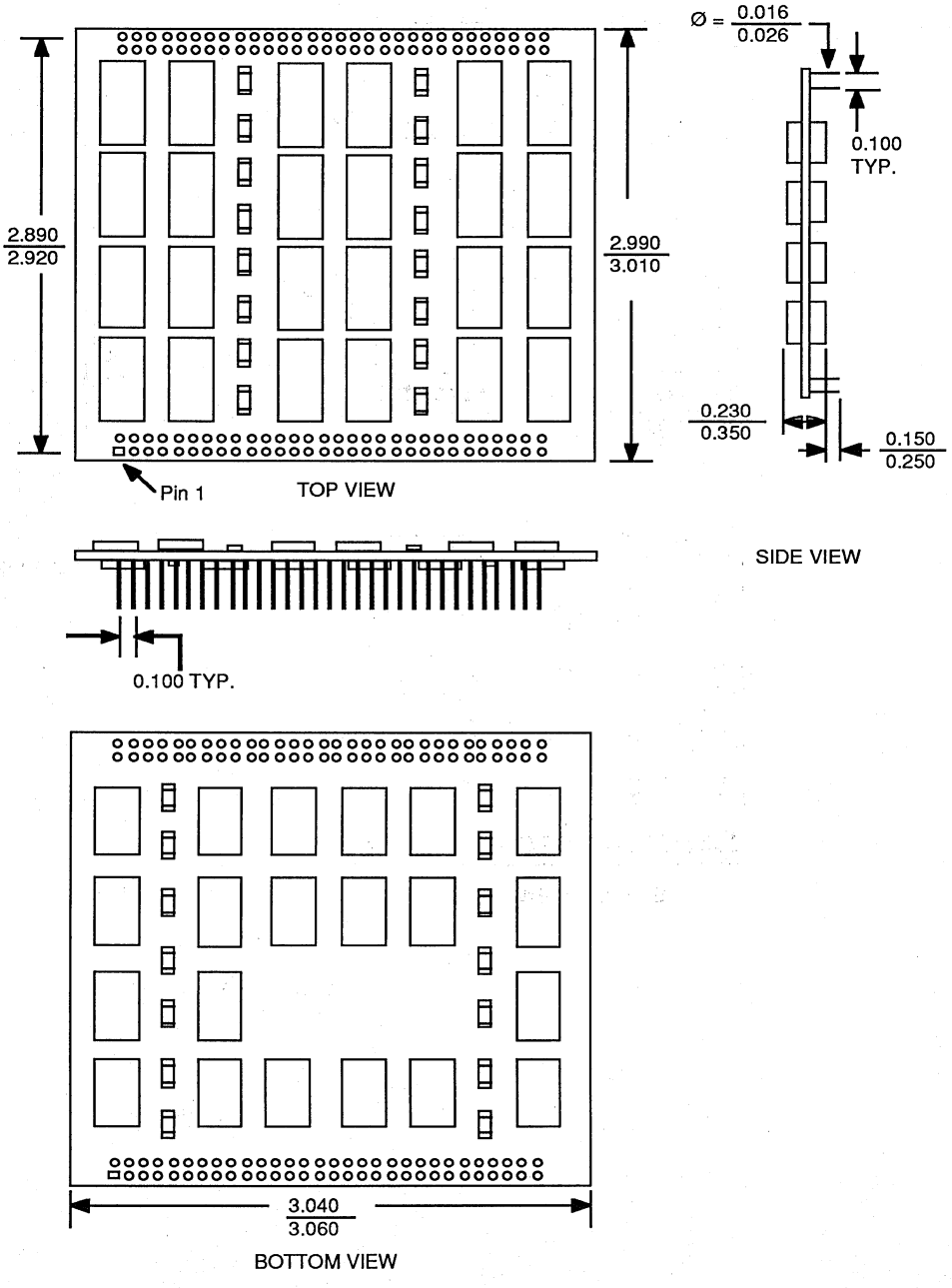
QUAD IN-LINE PACKAGES (Continued)

104-Pin FR-4 Plastic QIP – M38



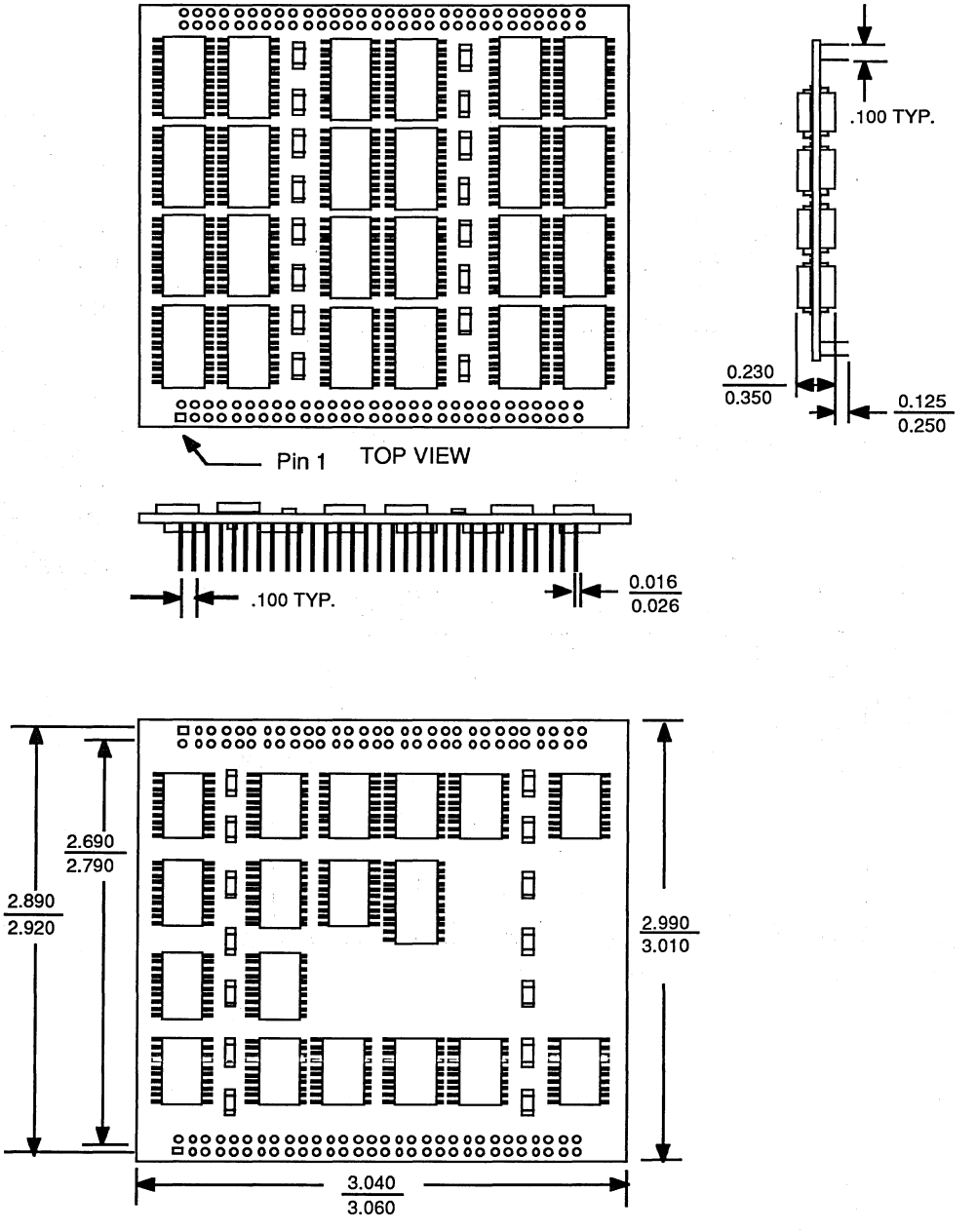
QUAD IN-LINE PACKAGES (Continued)

120-Pin FR-4 Plastic QIP – M39



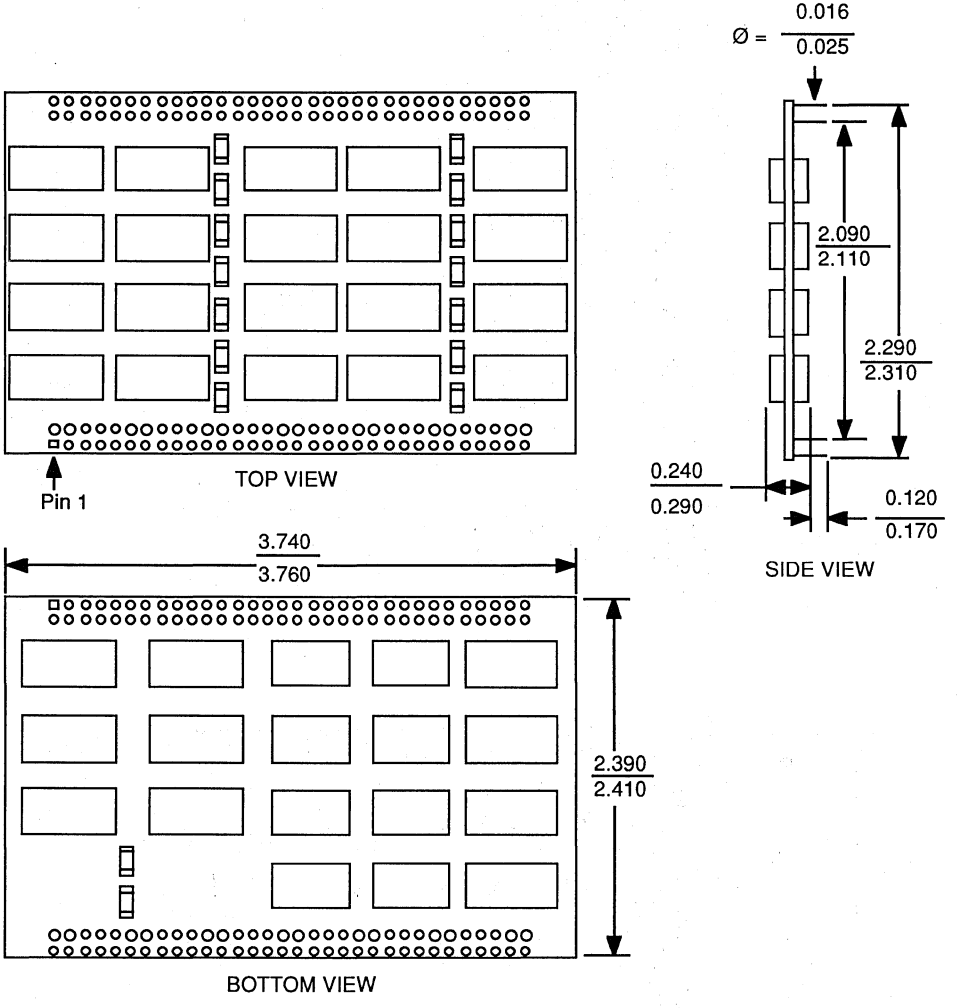
QUAD IN-LINE PACKAGES (Continued)

120-Pin FR-4 Plastic QIP – M40



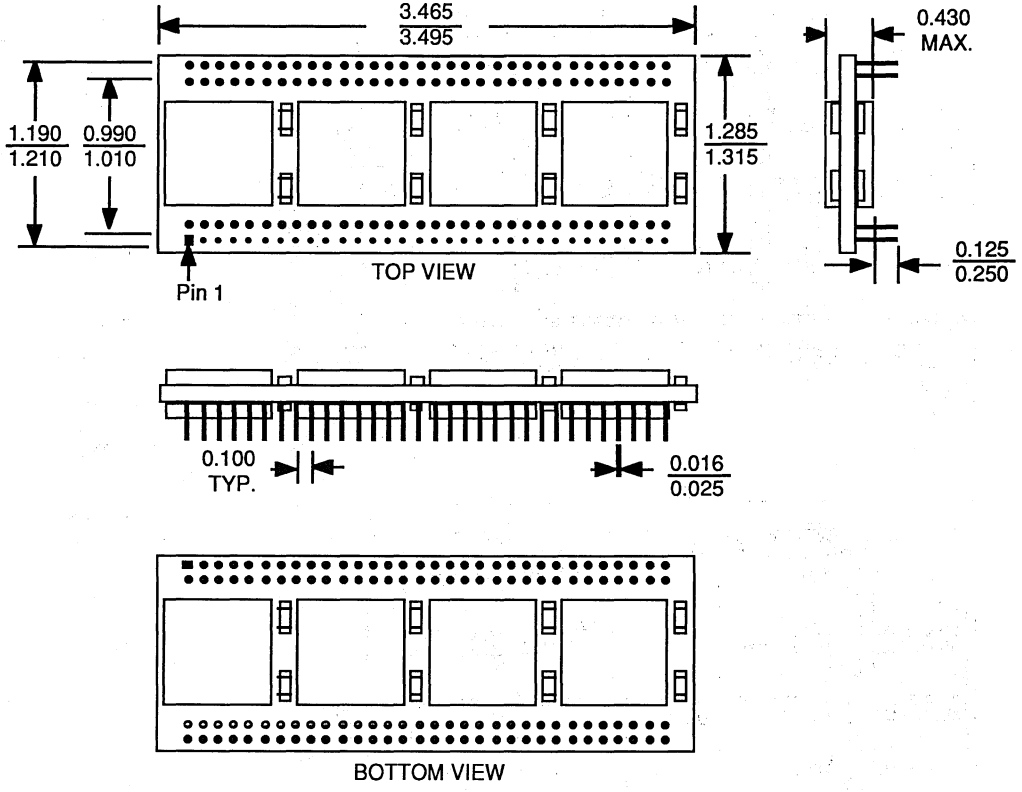
QUAD IN-LINE PACKAGES (Continued)

128-Pin FR-4 Plastic QIP – M41



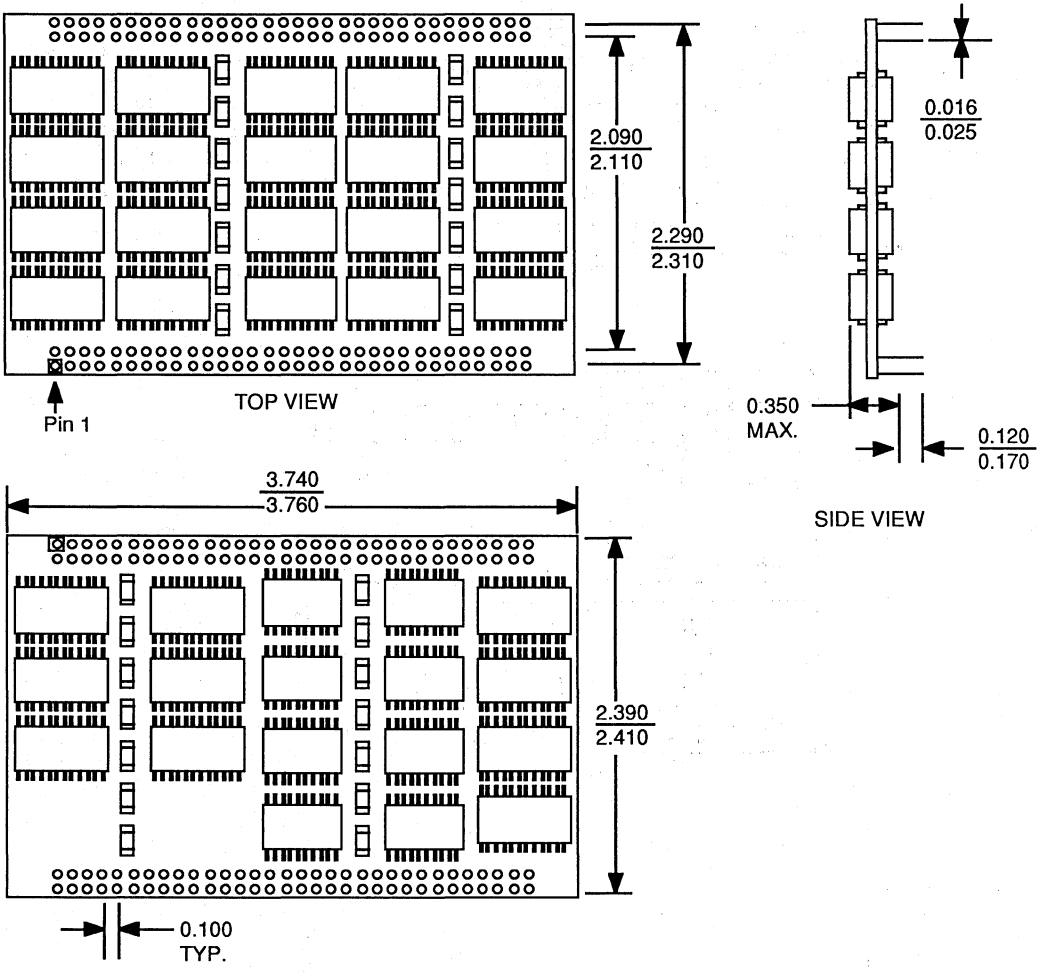
QUAD IN-LINE PACKAGES (Continued)

128-Pin FR-4 Plastic QIP – M42



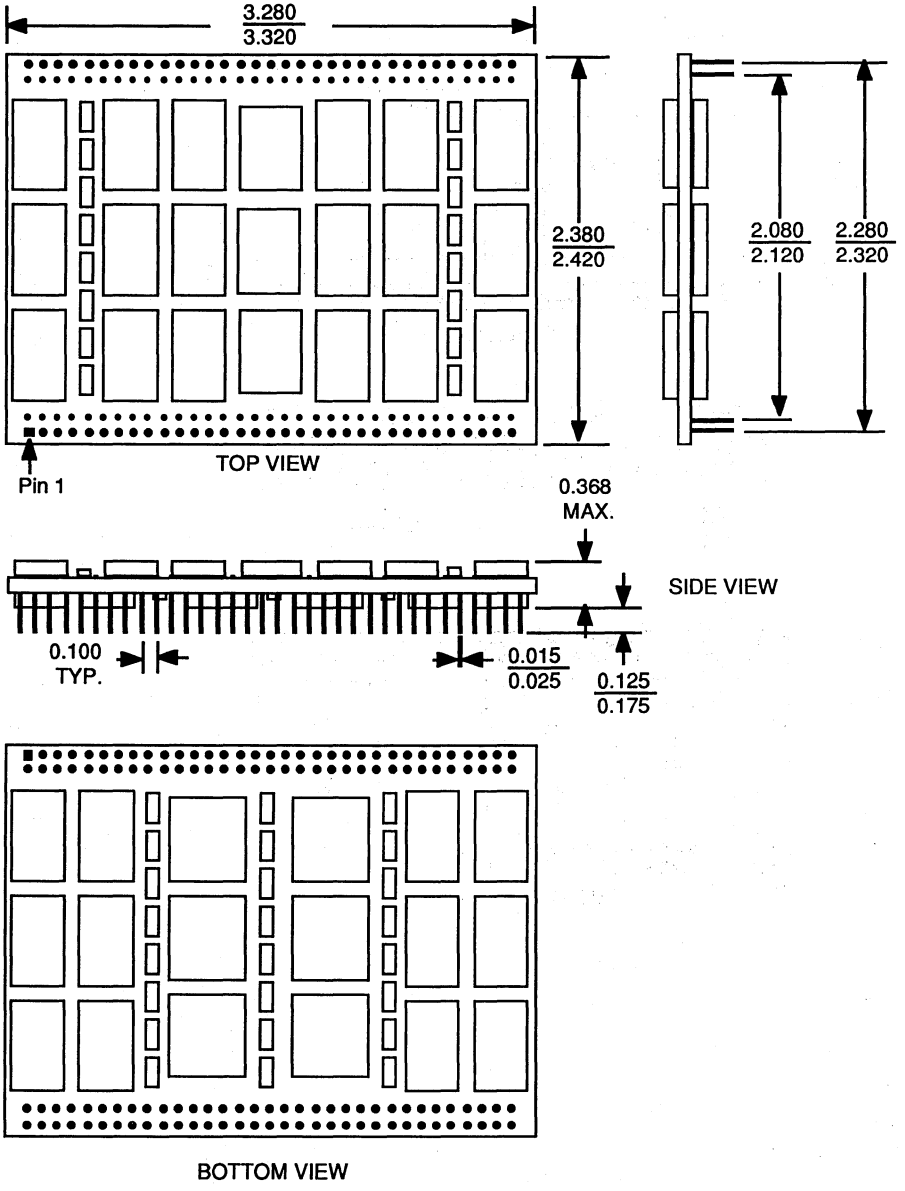
QUAD IN-LINE PACKAGES (Continued)

128-Pin FR-4 Plastic QIP – M43



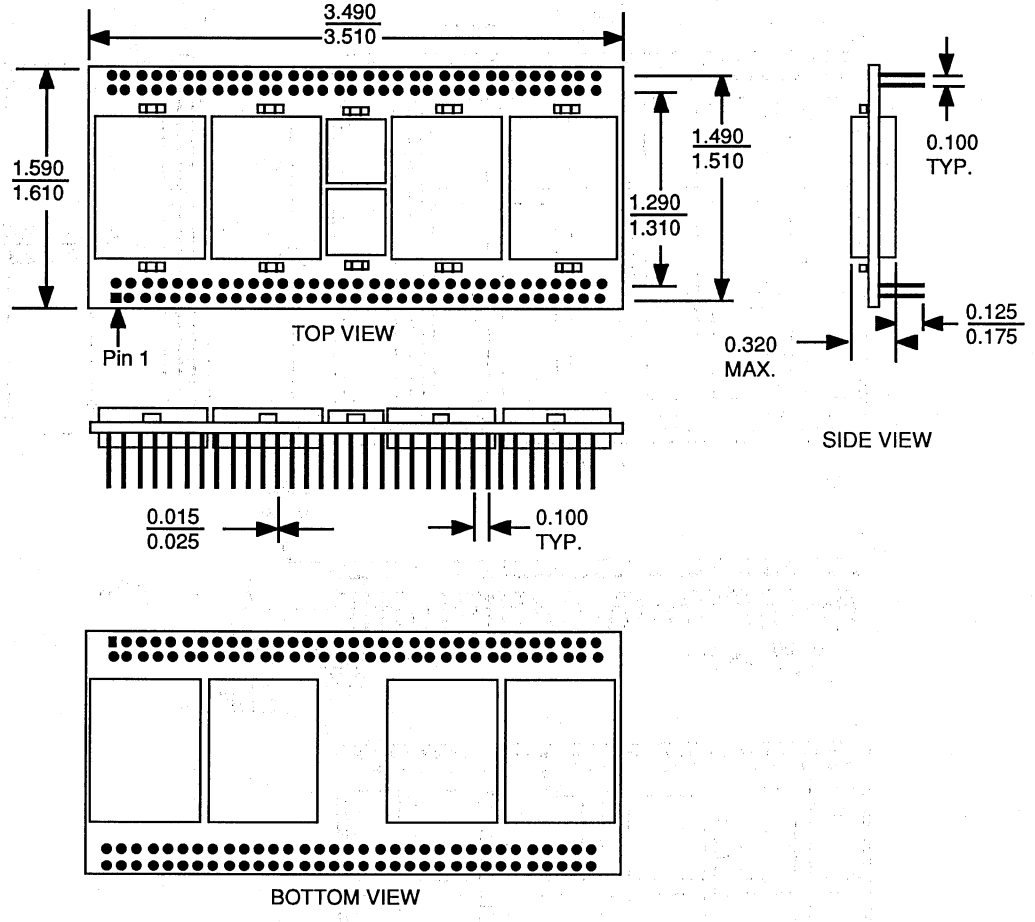
QUAD IN-LINE PACKAGES (Continued)

132-Pin FR-4 Plastic QIP – M44



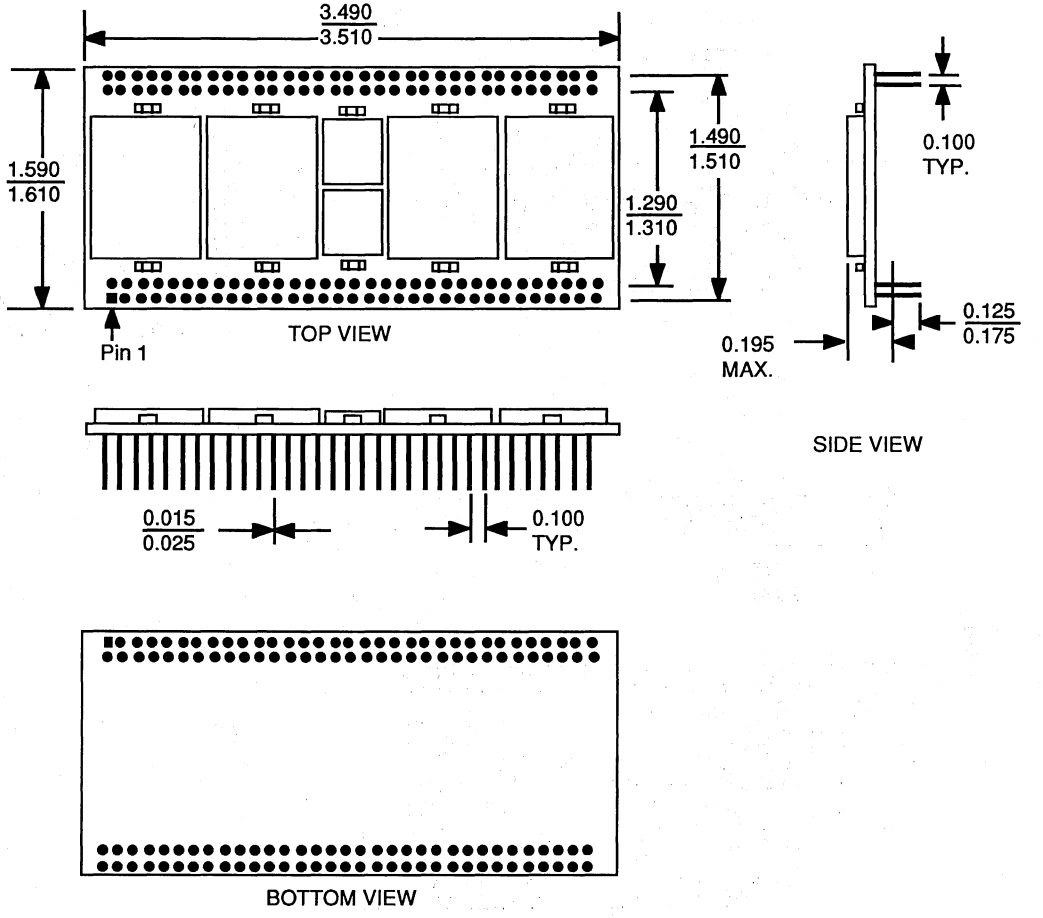
QUAD IN-LINE PACKAGES (Continued)

132-Pin FR-4 Plastic QIP – M45



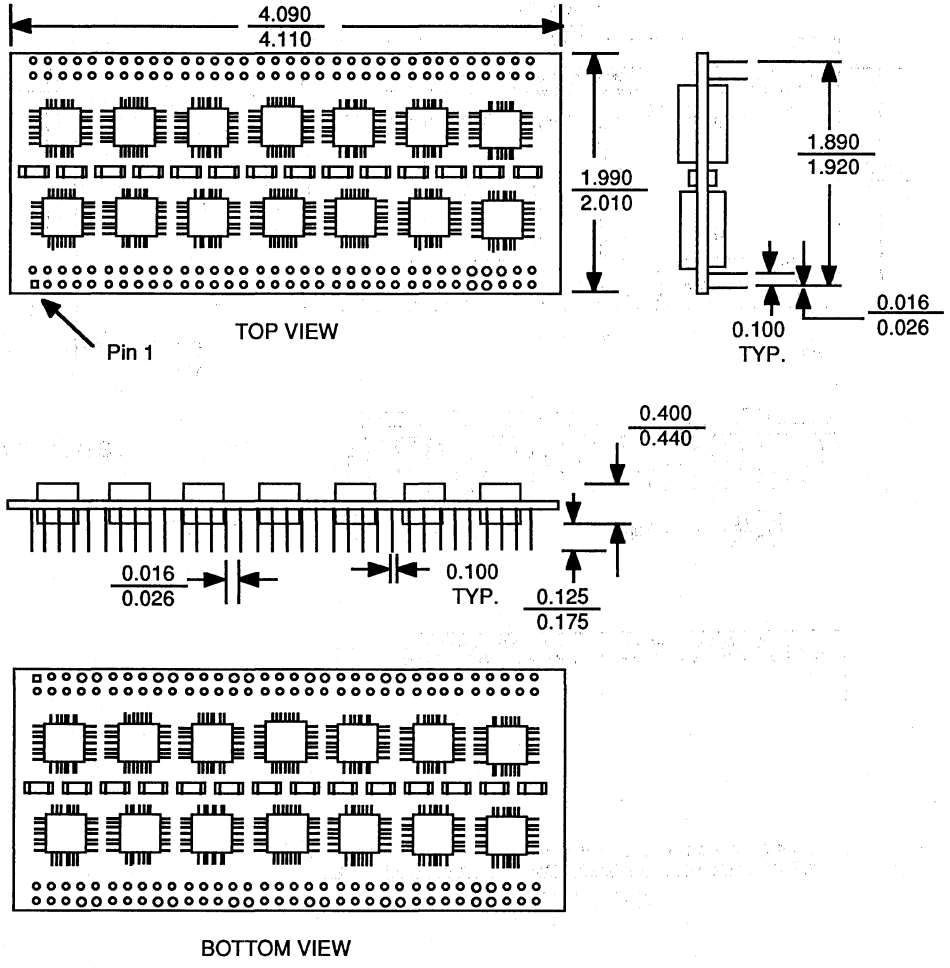
QUAD IN-LINE PACKAGES (Continued)

132-Pin FR-4 Plastic QIP – M46



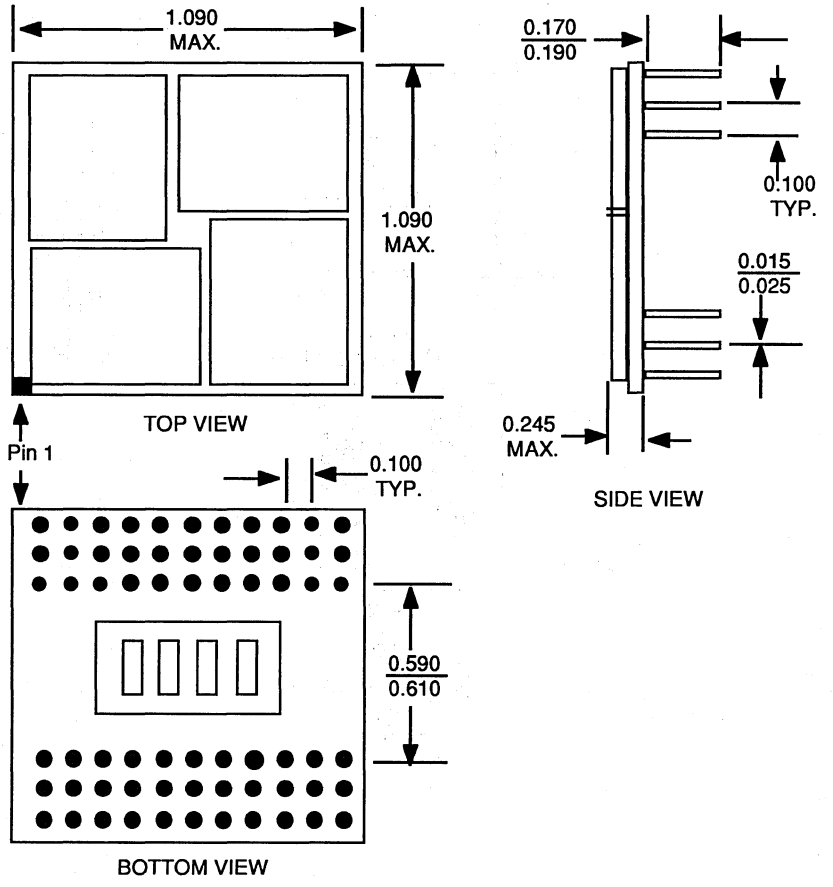
QUAD IN-LINE PACKAGES (Continued)

164-Pin FR-4 Plastic QIP – M47



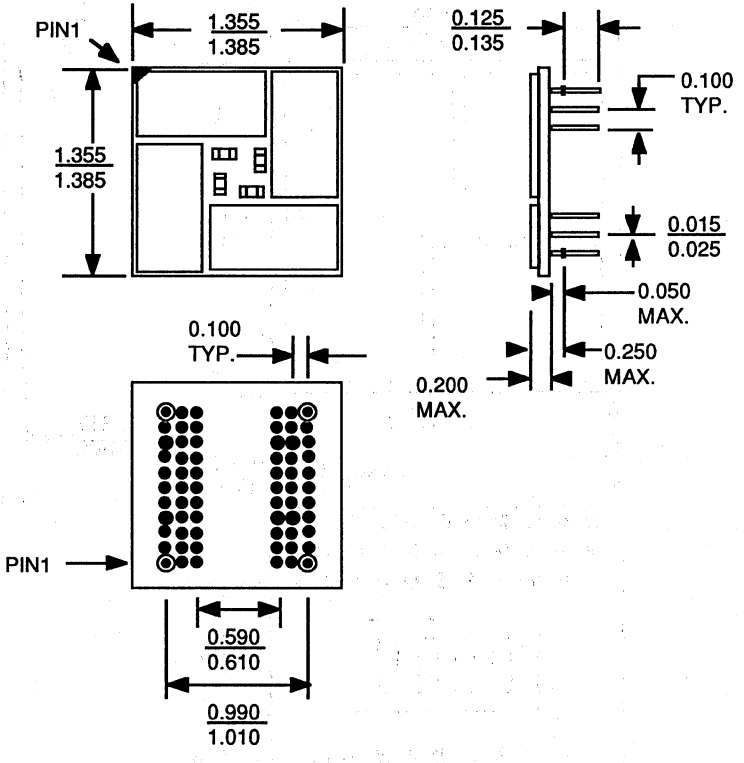
HEX IN-LINE PACKAGES

66-Pin Ceramic Sidebraze HIP – M48



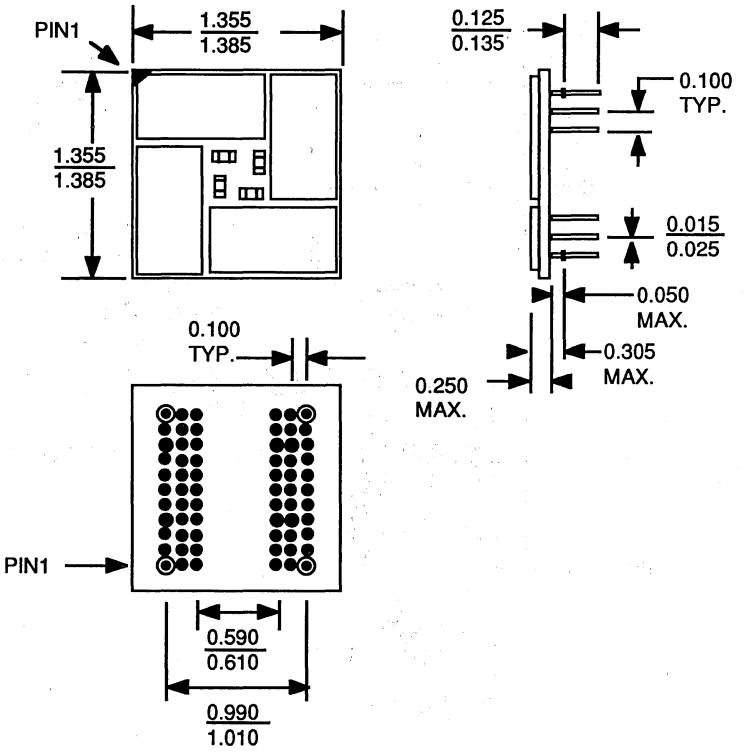
HEX IN-LINE PACKAGES (Continued)

66-Pin Ceramic Sidebraze HIP – M49



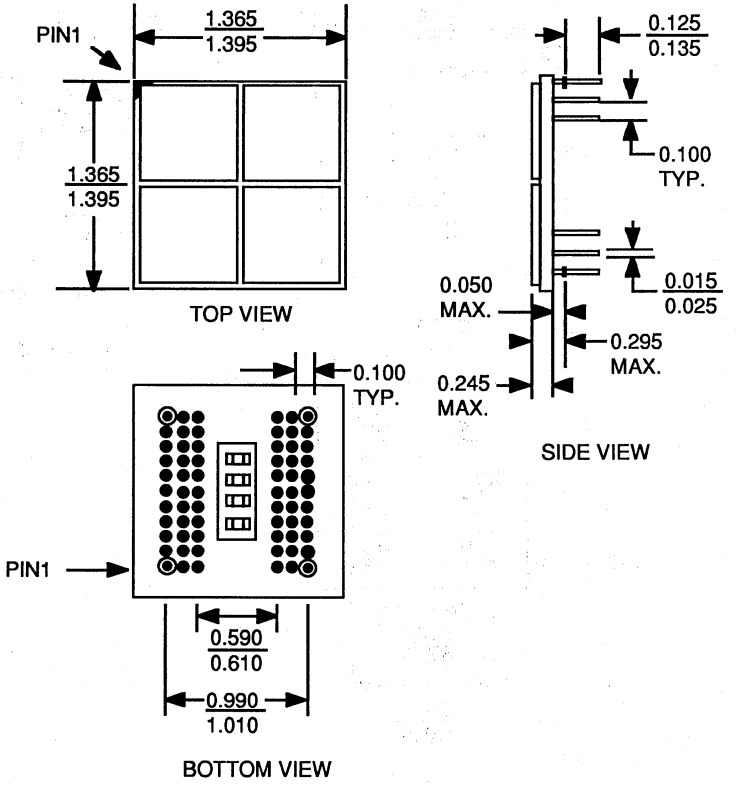
HEX IN-LINE PACKAGES (Continued)

66-Pin Ceramic Sidebraze HIP – M50



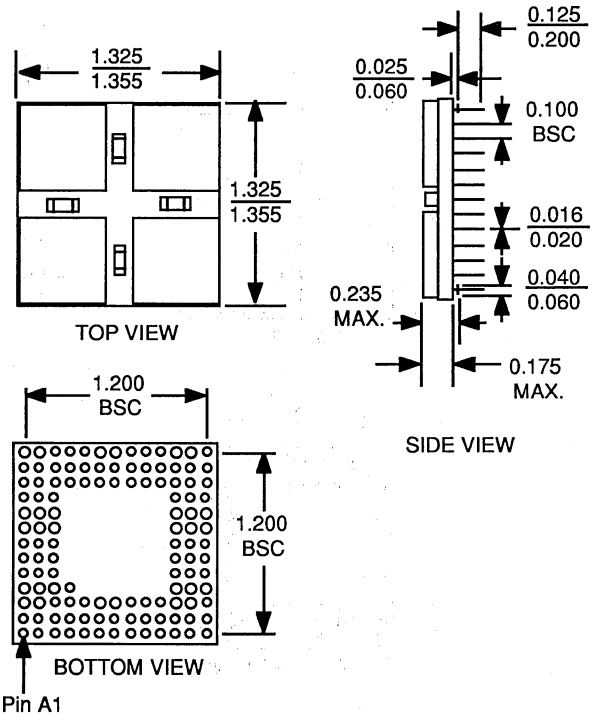
HEX IN-LINE PACKAGES (Continued)

66-Pin Ceramic Sidebraze HIP – M51



PIN GRID ARRAY PACKAGES

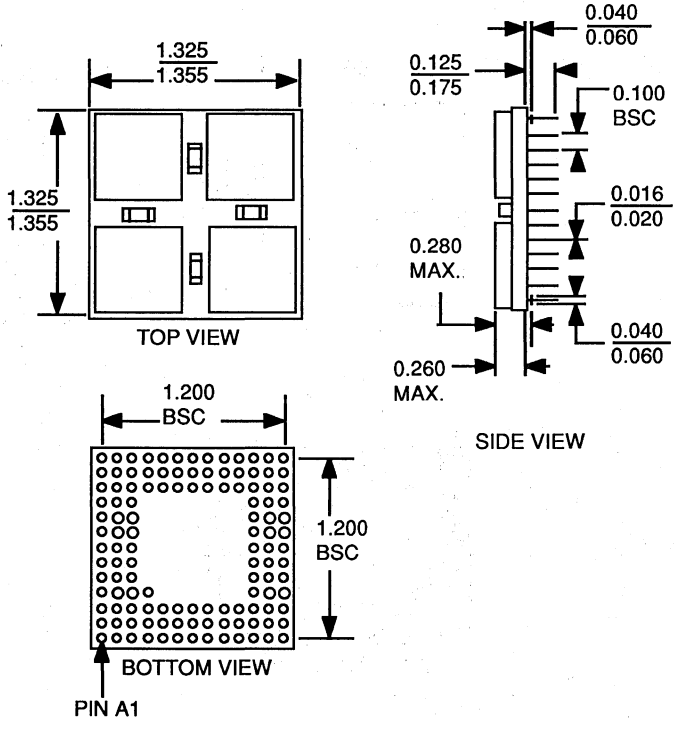
121-Pin Ceramic Sidebraze PGA – M52



4

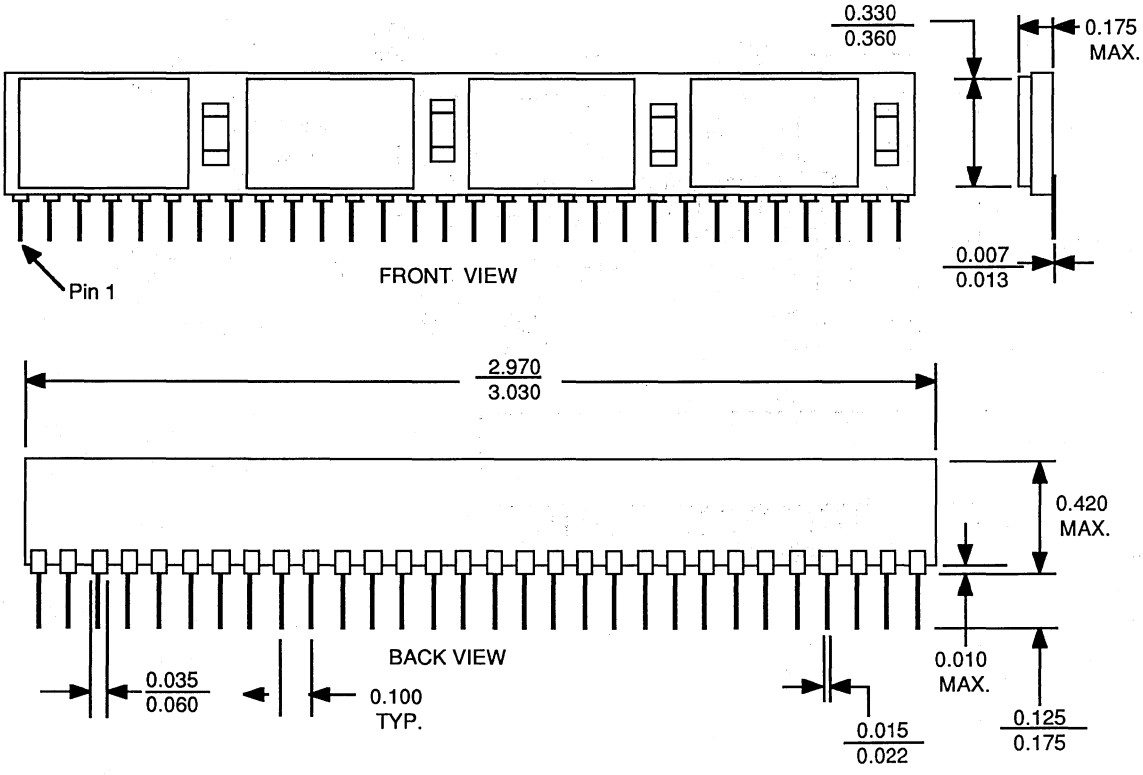
PIN GRID ARRAY PACKAGES (Continued)

121-Pin Ceramic Sidebraze PGA – M53



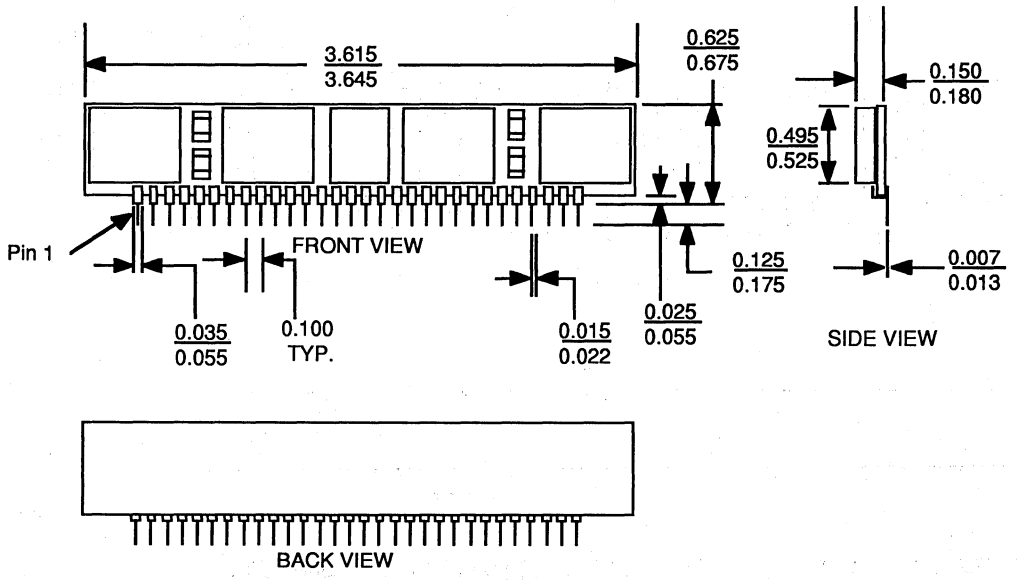
SINGLE IN-LINE PACKAGES

30-Pin Ceramic Sidebraze SIP – M54



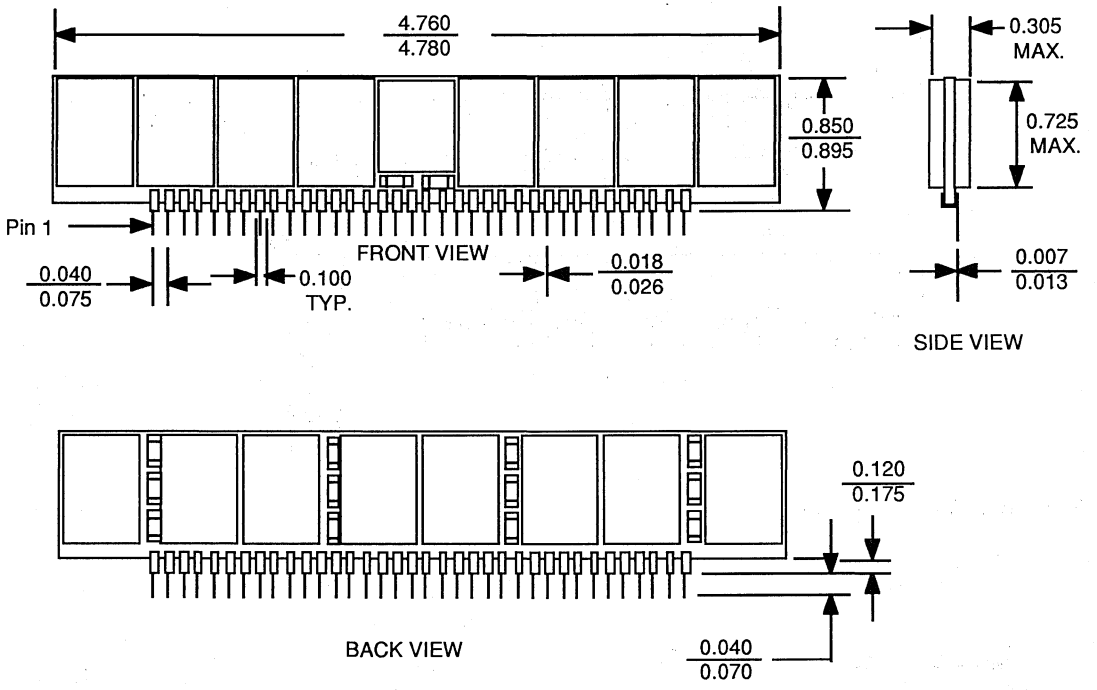
SINGLE IN-LINE PACKAGES (CONTINUED)

30-Pin FR-4 Plastic SIP – M55



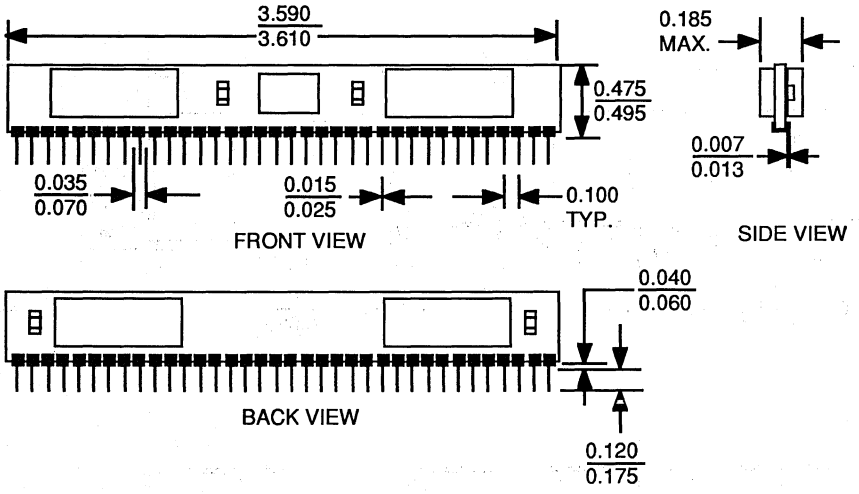
SINGLE IN-LINE PACKAGES (Continued)

36-Pin FR-4 Plastic SIP – M56

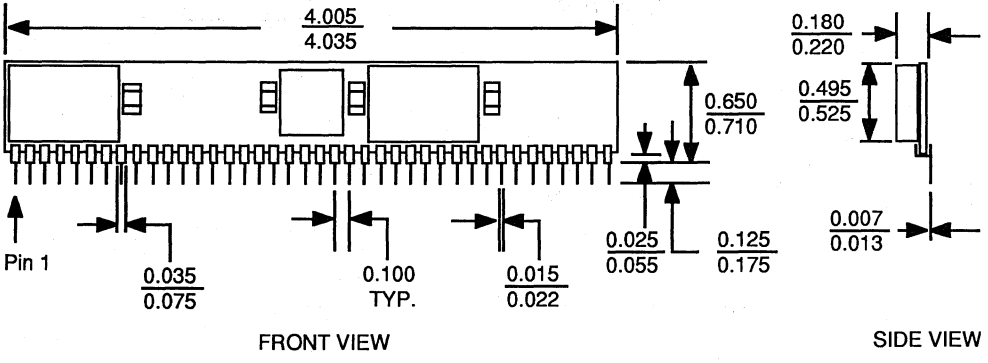


SINGLE IN-LINE PACKAGES (Continued)

36-Pin FR-4 Plastic SIP – M57

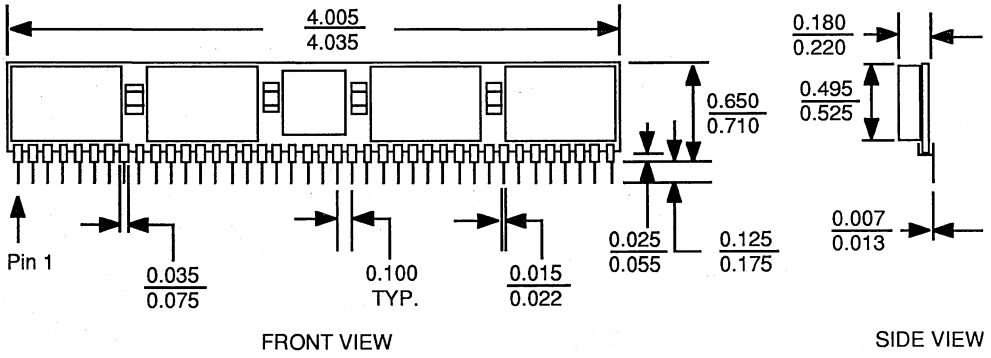


40-Pin FR-4 Plastic SIP – M58



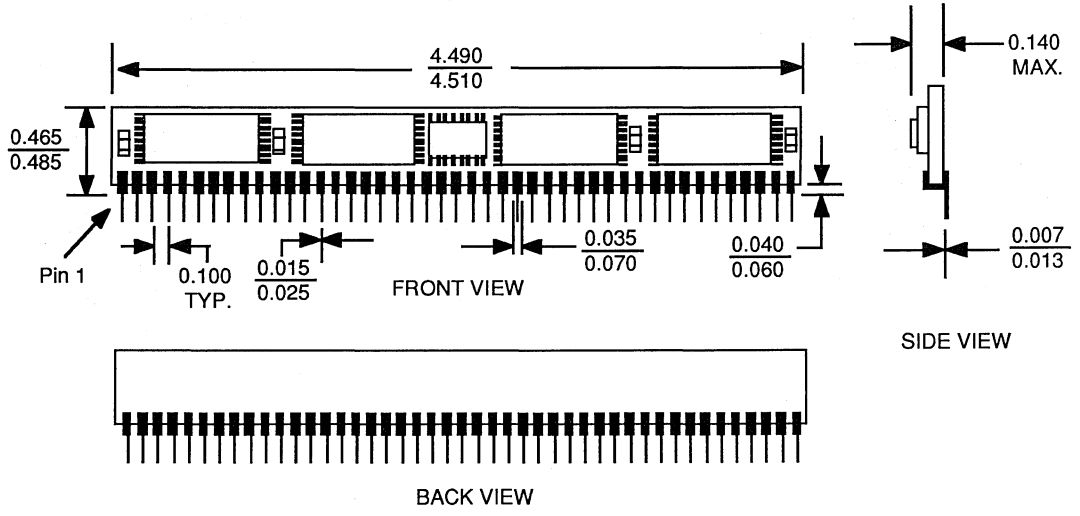
SINGLE IN-LINE PACKAGES (Continued)

40-Pin FR-4 Plastic SIP – M59



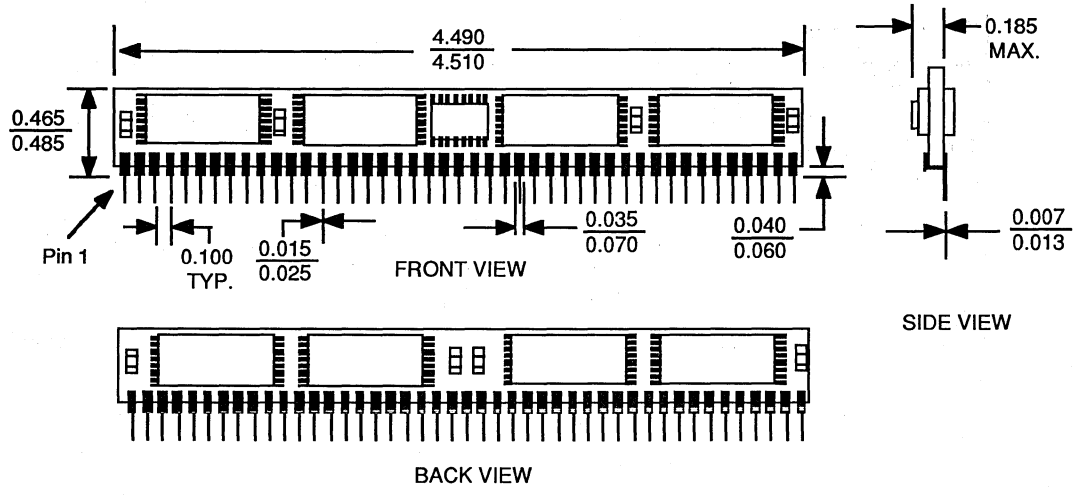
4

45-Pin FR-4 Plastic SIP – M60



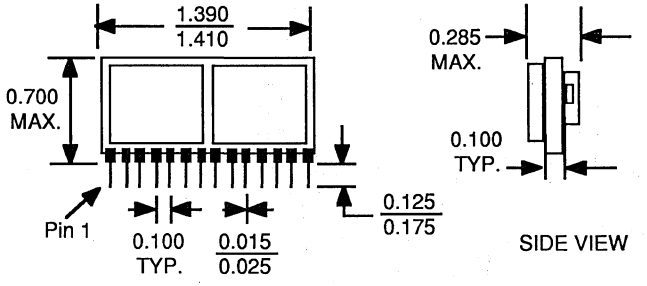
SINGLE IN-LINE PACKAGES (Continued)

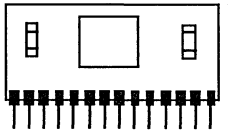
45-Pin FR-4 Plastic SIP – M61



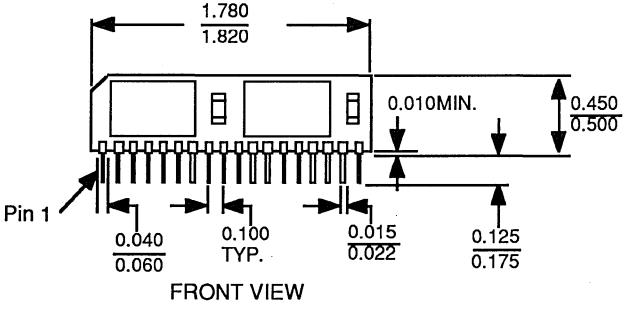
DUAL SINGLE IN-LINE PACKAGES

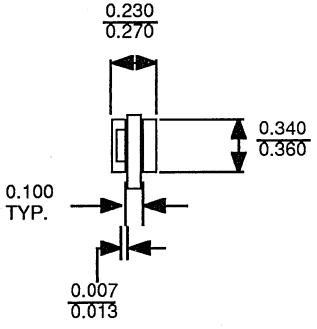
28-Pin FR-4 Plastic DSIP – M62





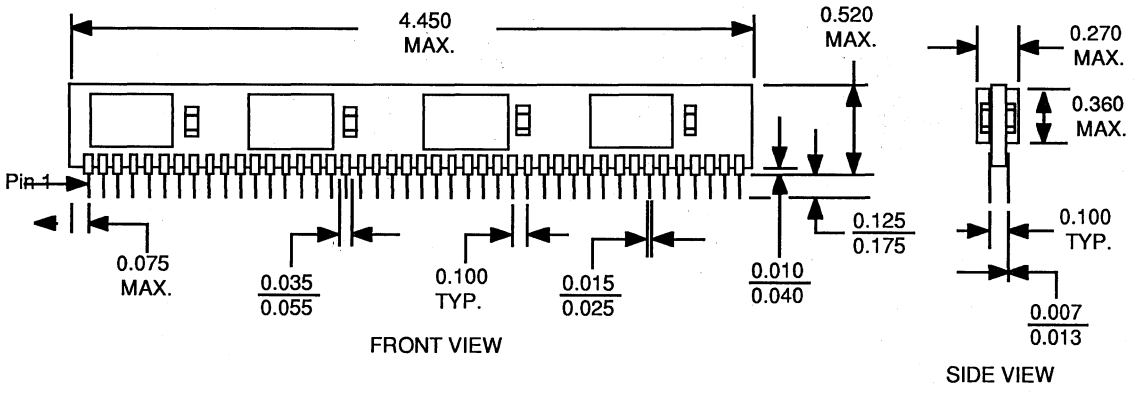
36-Pin Ceramic Sidebraze DSIP – M63





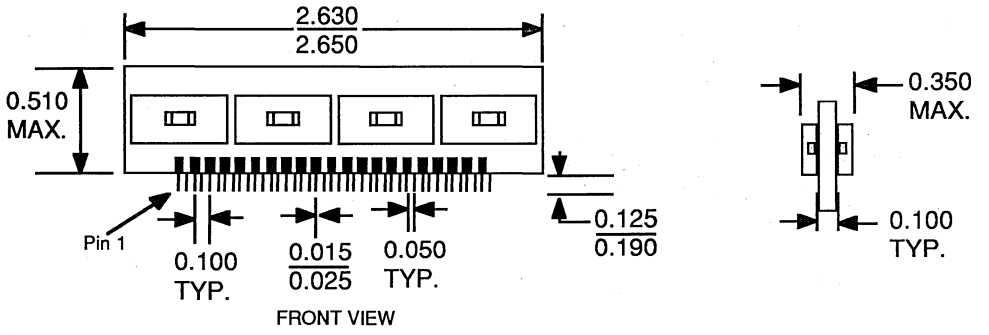
DUAL SINGLE IN-LINE PACKAGES (Continued)

88-Pin Ceramic Sidebraze DSIP – M64

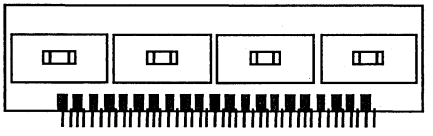


ZIG-ZAG IN-LINE PACKAGES

42-Pin FR-4 Plastic ZIP – M65

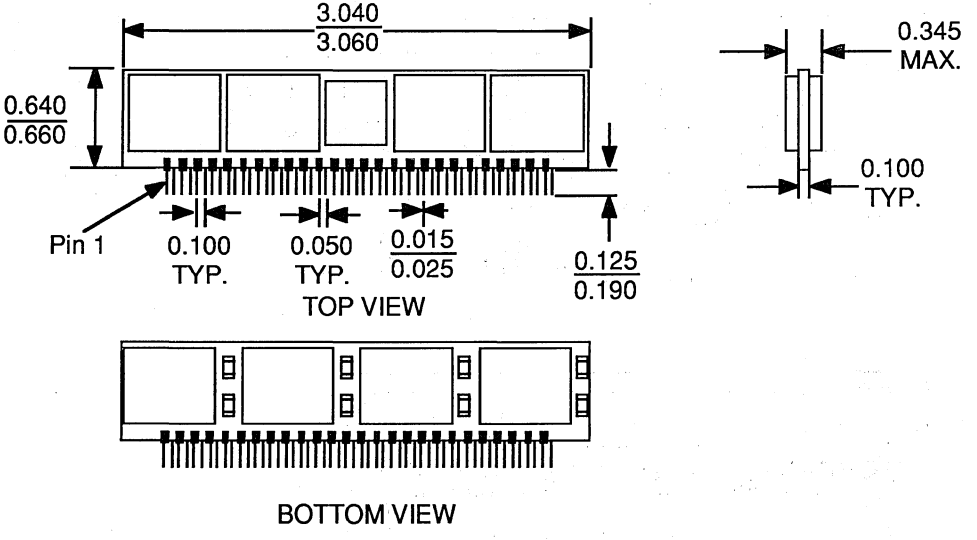


FRONT VIEW



BACK VIEW

52-Pin FR-4 Plastic ZIP – M66

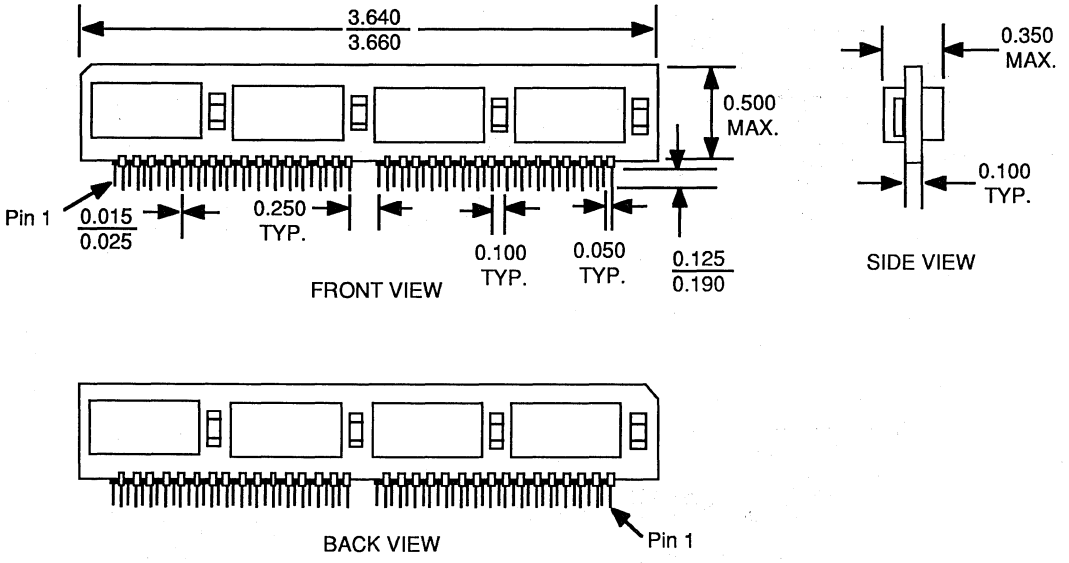


TOP VIEW

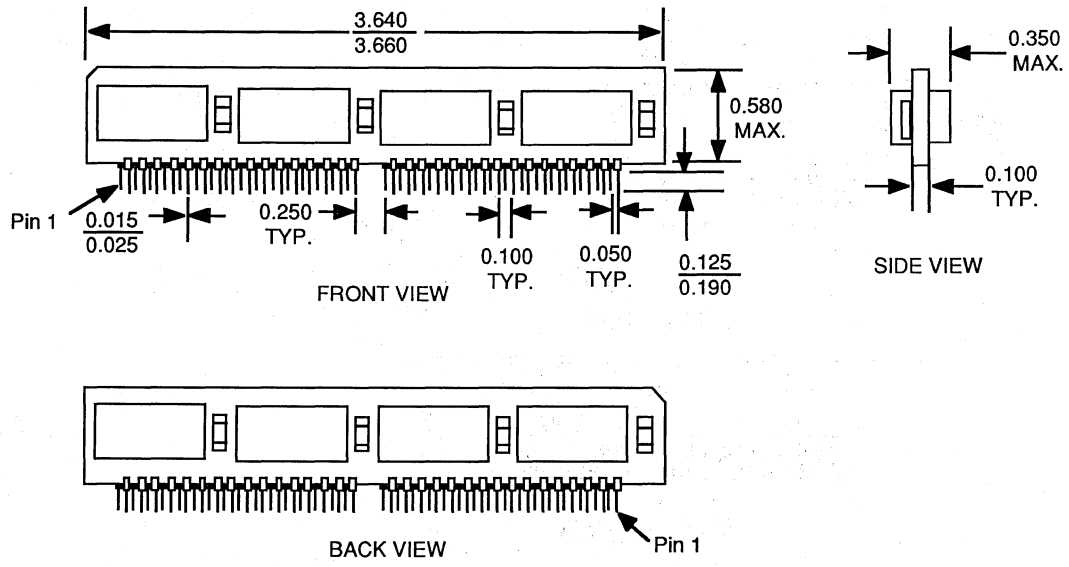
BOTTOM VIEW

ZIG-ZAG IN-LINE PACKAGES (Continued)

64-Pin FR-4 Plastic ZIP – M67

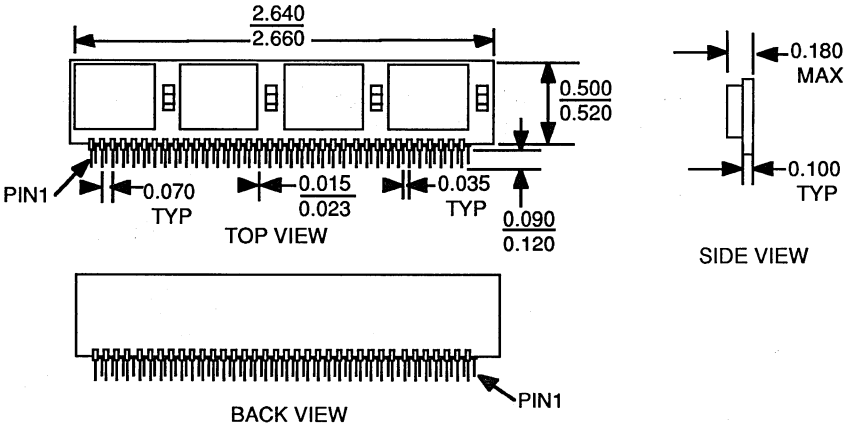


64-Pin FR-4 Plastic ZIP – M68



ZIG-ZAG IN-LINE PACKAGES (Continued)

75-Pin FR-4 Plastic ZIP – M69



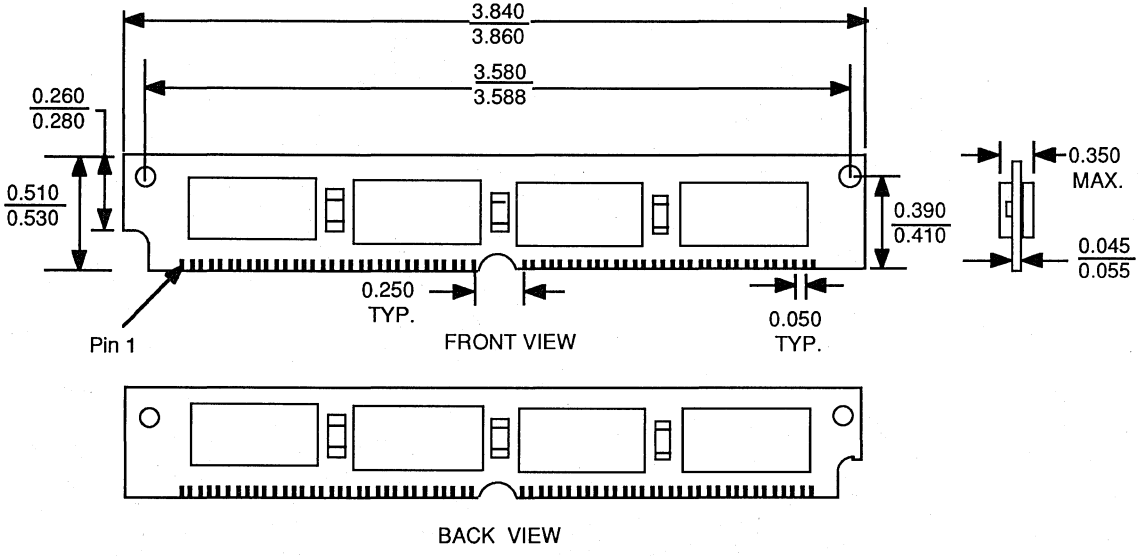
4

SINGLE IN-LINE MEMORY MODULES

64-Pin FR-4 Plastic SIMM – M70

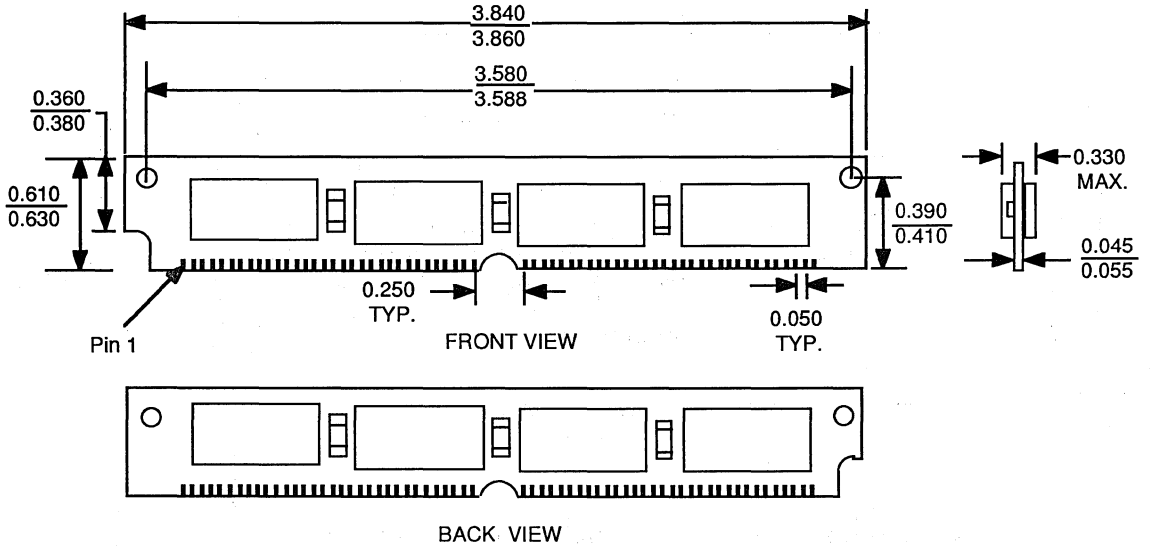
Module Dimensions for Package M70 are not yet finalized.
Please consult the factory for further details.

64-Pin FR-4 Plastic SIMM – M71

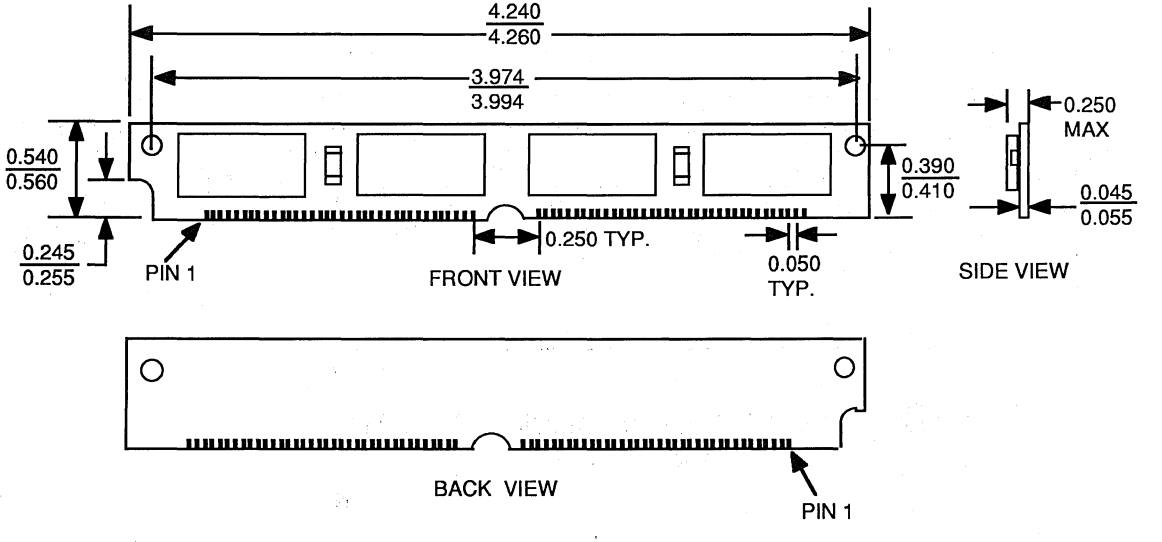


SINGLE IN-LINE MEMORY MODULES (Continued)

64-Pin FR-4 Plastic SIMM – M72

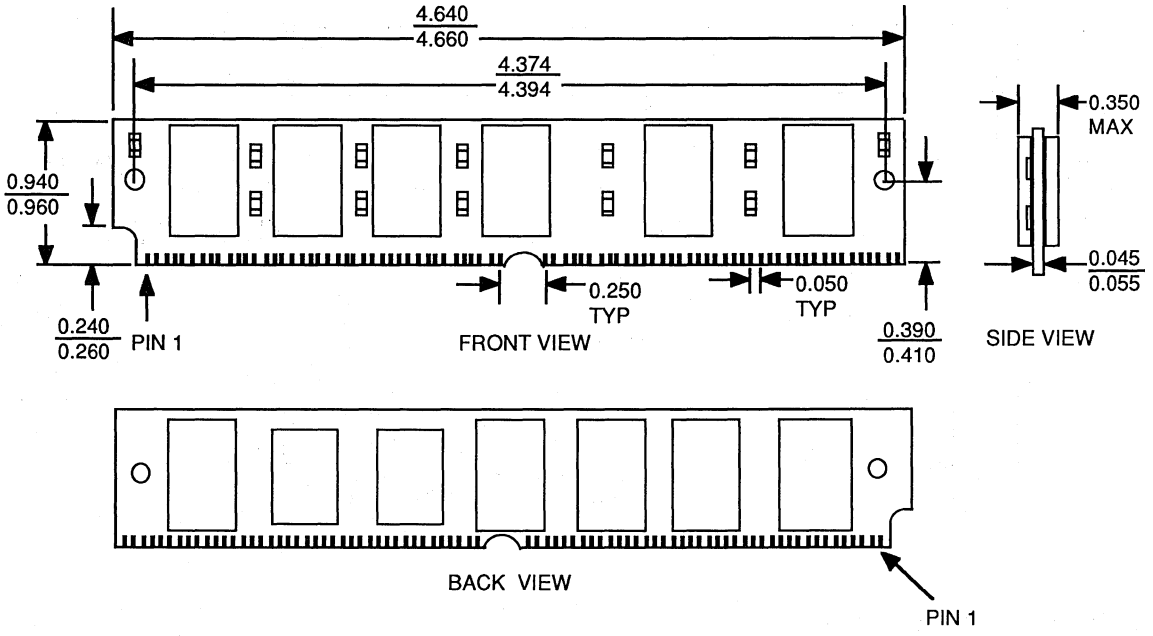


72-Pin FR-4 Plastic SIMM – M73

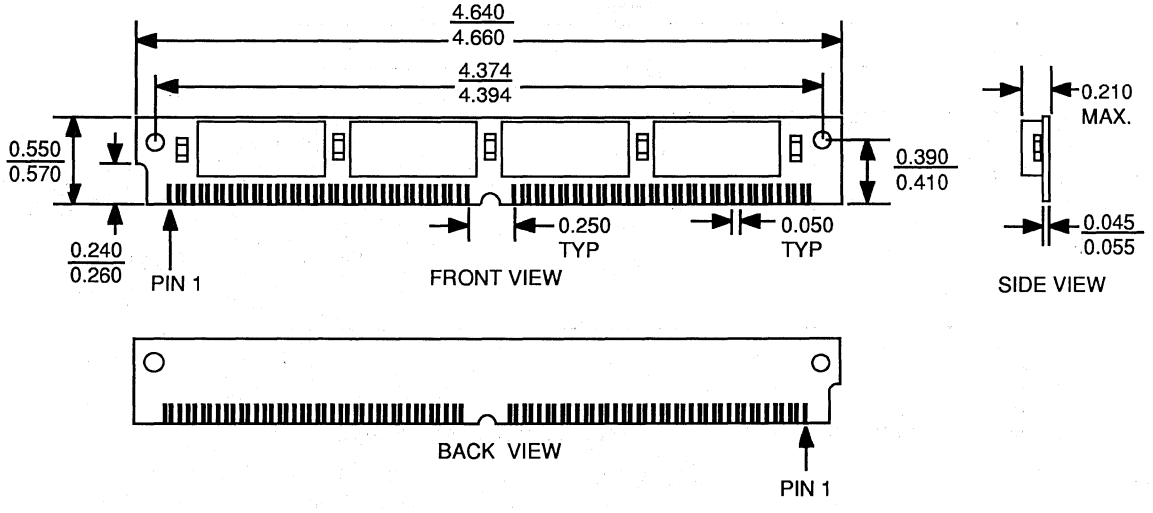


SINGLE IN-LINE MEMORY MODULES (Continued)

80-Pin FR-4 Plastic SIMM – M74

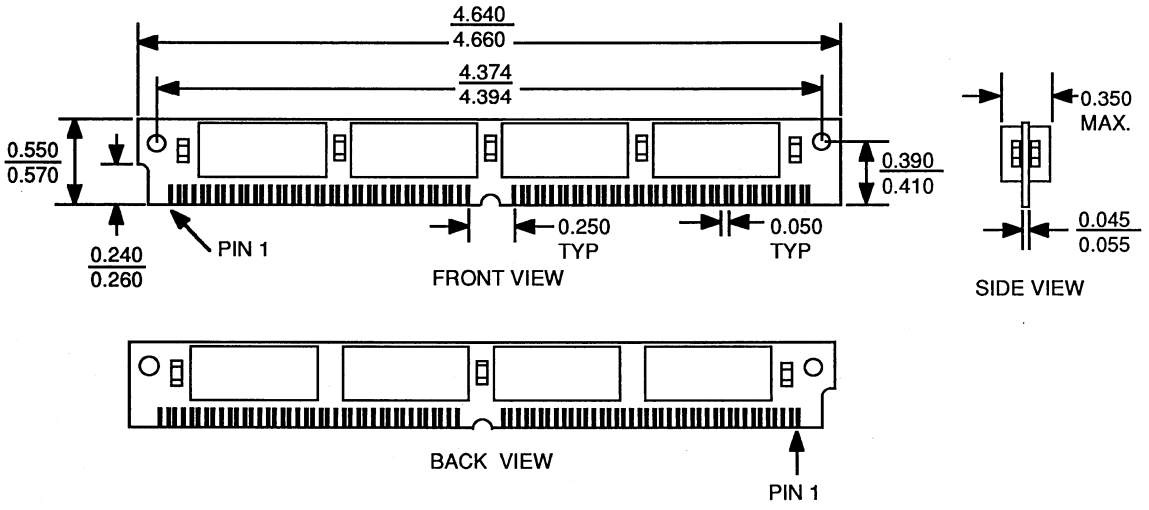


80-Pin FR-4 Plastic SIMM – M75



SINGLE IN-LINE MEMORY MODULES (Continued)

80-Pin FR-4 Plastic SIMM – M76

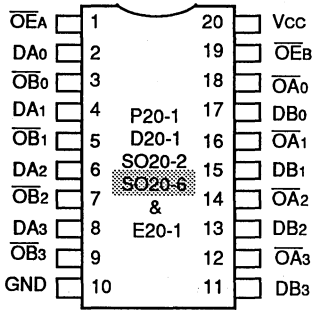


1991 DATA BOOK UPDATE 1
TABLE OF CONTENTS

The following section contains partial data sheets that appeared in the 1991 LOGIC Data Book. These data sheets had changes to less than 50% of the overall contents. Refer to the bars above changes to see where that section can be found in the 1991 LOGIC Data Book.

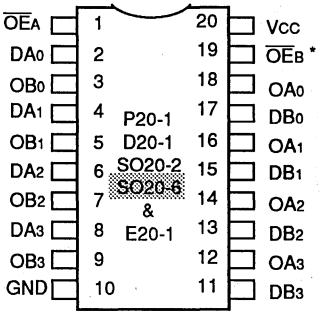
PIN CONFIGURATIONS

IDT54/74FCT240T



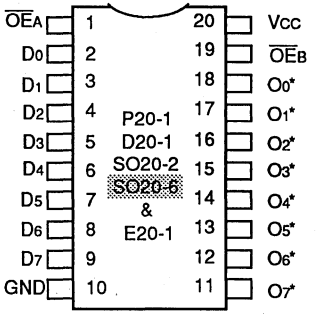
DIP/SOIC/EIAJ/CERPACK
TOP VIEW

IDT54/74FCT241T/244T



DIP/SOIC/EIAJ/CERPACK
TOP VIEW

IDT54/74FCT540T/541T

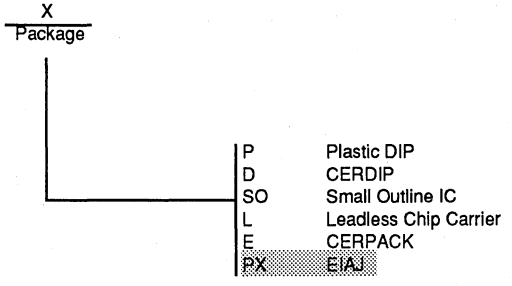


DIP/SOIC/EIAJ/CERPACK
TOP VIEW

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT240T

Symbol	Parameter	Condition[1]	54/74FCT240T				54/74FCT240AT				54/74FCT240CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay DN to $\overline{ON}$	CL = 50pF RL = 500Ω	1.5	8.0	1.5	9.0	1.5	4.8	1.5	5.1	1.5	4.3	1.5	4.7	ns
tPZH tPZL	Output Enable Time		1.5	10.0	1.5	10.5	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time		1.5	9.5	1.5	10.0	1.5	5.6	1.5	5.9	1.5	5.2	1.5	5.7	ns

ORDERING INFORMATION



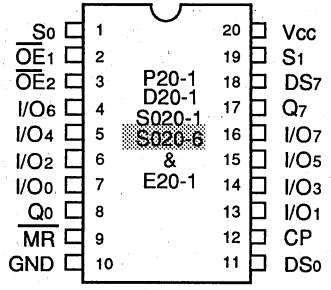
FEATURES:

- IDT54/74FCT299T equivalent to FAST™ speed
- IDT54/74FCT299AT 25% faster than FAST™
- IDT54/74FCT299CT 35% faster than FAST™

DESCRIPTION:

The IDT54/74FCT299T and IDT54/74FCT299AT/CT are built using advanced CEMOS™, a dual-metal CMOS technology.

PIN CONFIGURATIONS



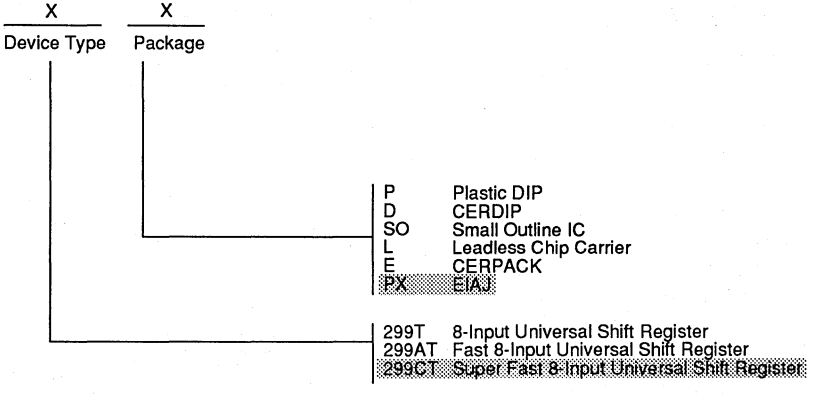
DIP/SOIC/EIAJ/CERPACK
TOP VIEW

A

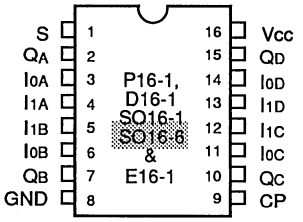
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT299T				IDT54/74FCT299AT				IDT54/74FCT299CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CP to Q0 or Q7	CL = 50pF RL = 500Ω	2.0	10.0	2.0	14.0	2.0	7.2	2.0	9.5	2.0	6.5	2.0	7.5	ns
tPLH tPHL	Propagation Delay CP to I/On		2.0	12.0	2.0	12.0	2.0	7.2	2.0	9.5	2.0	6.5	2.0	7.5	ns
tPHL	Propagation Delay $\overline{MR}$ to Q0 or Q7		2.0	10.0	2.0	10.5	2.0	7.2	2.0	9.5	2.0	6.5	2.0	7.5	ns
tPHL	Propagation Delay $\overline{MR}$ to I/On		2.0	15.0	2.0	15.0	2.0	8.7	2.0	11.5	2.0	6.5	2.0	7.5	ns
tPZH tPZL	Output Enable Time $\overline{OE}$n to I/On		1.5	11.0	1.5	15.0	1.5	6.5	1.5	7.5	1.5	6.5	1.5	7.5	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$n to I/On		1.5	7.0	1.5	9.0	1.5	6.0	1.5	6.5	1.5	6.0	1.5	6.5	ns
tSU	Set-up Time HIGH or LOW S0 or S1 to CP		7.5	—	7.5	—	3.5	—	4.0	—	3.5	—	4.0	—	ns
tSU	Set-up Time HIGH or LOW I/On, DS0 or DS7 to CP		5.5	—	5.5	—	4.0	—	4.5	—	4.0	—	4.5	—	ns
tH	Hold Time HIGH or LOW S0 or S1 to CP		1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns
tH	Hold Time HIGH or LOW I/On, DS0 or DS7 to CP		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tW	CP Pulse Width HIGH or LOW		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns
tw	$\overline{MR}$ Pulse Width LOW		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns
tREM	Recovery Time $\overline{MR}$ to I/On		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

ORDERING INFORMATION

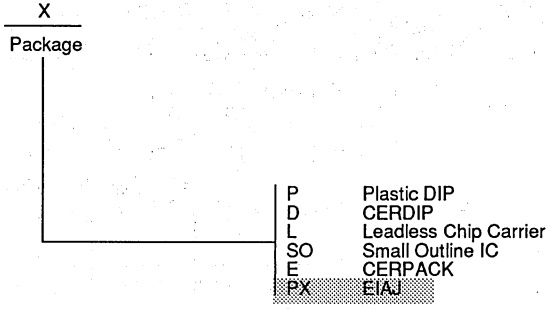


PIN CONFIGURATION



DIP/SOIC/EIAJ/CERPACK
TOP VIEW

ORDERING INFORMATION

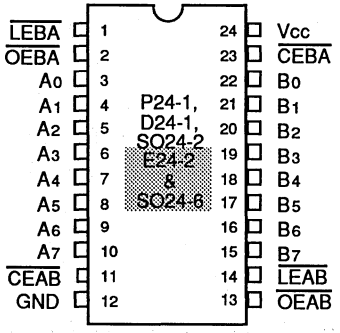


A

FEATURES:

- IDT54/74FCT543T equivalent to FAST™ speed
- **IDT54/74FCT543AT 25% faster than FAST™**
- **IDT54/74FCT543CT 40% faster than FAST™**

PIN CONFIGURATIONS



DIP/SOIC/CERPACK/EIAJ
TOP VIEW

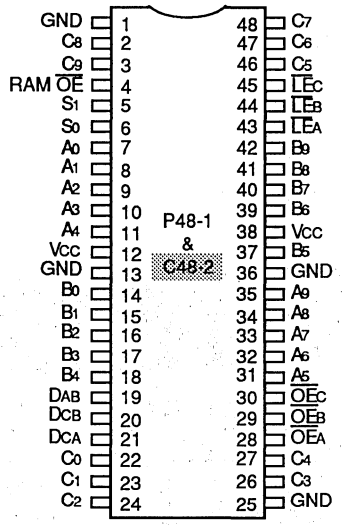
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT543T				IDT54/74FCT543AT				IDT54/74FCT543CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Transparent Mode An to Bn or Bn to An	CL = 50pF RL = 500Ω	2.5	8.5	2.5	10.0	2.5	6.5	2.5	7.5	2.5	5.3	2.5	6.1	ns
tPLH tPHL	Propagation Delay LEBA to An, LEAB to Bn		2.5	12.5	2.5	14.0	2.5	8.0	2.5	9.0	2.5	7.0	2.5	8.0	ns
tPZH tPZL	Output Enable Time OEBA or OEAB to An or Bn CEBA or CEAB to An or Bn		2.0	12.0	2.0	14.0	2.0	9.0	2.0	10.0	2.0	8.0	2.0	9.0	ns
tPHZ tPLZ	Output Disable Time OEBA or OEAB to An or Bn CEBA or CEAB to An or Bn		2.0	9.0	2.0	13.0	2.0	7.5	2.0	8.5	2.0	6.5	2.0	7.5	ns
tSU	Set-up Time, HIGH or LOW An or Bn to LEBA or LEAB		3.0	—	3.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time, HIGH or LOW An or Bn to LEBA or LEAB		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tW	LEBA or LEAB Pulse Width LOW		5.0	—	5.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns

FEATURES:

- Available in plastic and sidebraze DIPs, and PLCC

PIN CONFIGURATION



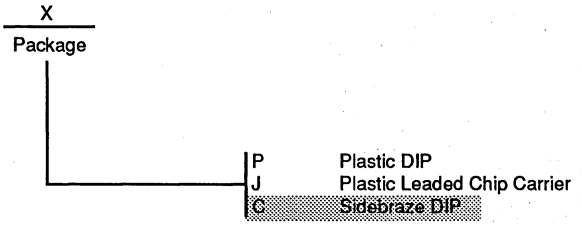
DIP
TOP VIEW

A

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			IDT49FCT804				IDT49FCT804A				IDT49FCT804C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
tPHL tPLH	Propagation Delay Port to Port	CL = 50pF RL = 500Ω	1.5	10.8	1.5	11.8	1.5	9.0	1.5	10.0	1.5	7.2	1.5	8.2	ns
tPHL tPLH	Propagation Delay $\overline{LE}$x to Port		1.5	14.4	1.5	15.8	1.5	12.0	1.5	13.0	1.5	8.7	1.5	10.2	ns
tPHL tPLH	Propagation Delay S0 or S1 to port		1.5	13.2	1.5	14.8	1.5	11.0	1.5	12.0	1.5	8.2	1.5	9.2	ns
tPHL tPLH	Propagation Delay S0 or S1 to RAM $\overline{OE}$		1.5	14.4	1.5	15.8	1.5	12.0	1.5	13.0	1.5	9.2	1.5	10.2	ns
tPHL tPLH	Propagation Delay Dxx to RAM $\overline{OE}$		1.5	10.8	1.5	11.8	1.5	9.0	1.5	10.0	1.5	7.2	1.5	8.2	ns
tPZL tPZH	Output Enable Time Dxx or $\overline{OE}$x to Port[3]		1.5	13.0	1.5	14.0	1.5	11.5	1.5	12.5	1.5	8.0	1.5	9.5	ns
tPLZ tPHZ	Output Disable Time Dxx or $\overline{OE}$x to Port[3]		1.5	10.0	1.5	11.0	1.5	9.0	1.5	10.0	1.5	7.7	1.5	9.2	ns

ORDERING INFORMATION



SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT240[1,2]

Symbol	Parameter	Condition	54/74FCT240				54/74FCT240A				54/74FCT240C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay DN to $\overline{ON}$	CL = 50pF RL = 500Ω	1.5	8.0	1.5	9.0	1.5	4.8	1.5	5.1	1.5	4.3	1.5	4.7	ns
tPZH tPZL	Output Enable Time		1.5	10.0	1.5	10.5	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time		1.5	9.5	1.5	10.0	1.5	5.6	1.5	5.9	1.5	5.2	1.5	5.7	ns

FEATURES:

- IDT54/74FCT299 equivalent to FAST™ speed
- **IDT54/74FCT299A 25% faster than FAST™**
- **IDT54/74FCT299C 35% faster than FAST™**

DESCRIPTION:

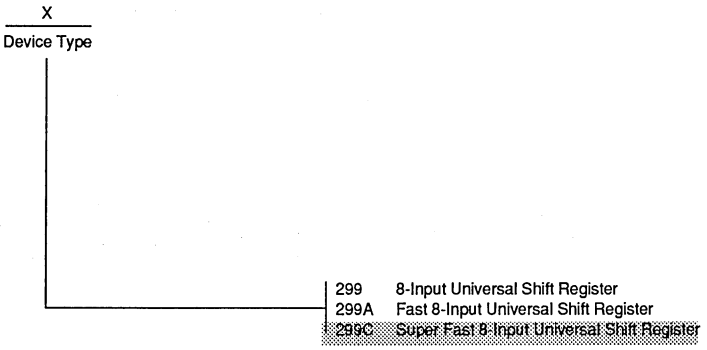
The IDT54/74FCT299 and IDT54/74FCT299A/C are built using advanced CEMOS™, a dual-metal CMOS technology. The IDT54/74FCT299 and IDT54/74FCT299A/C are 8-input universal shift/storage registers with 3-state outputs.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT299				IDT54/74FCT299A				IDT54/74FCT299C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CP to Q0 or Q7	CL = 50pF RL = 500Ω	2.0	10.0	2.0	14.0	2.0	7.2	2.0	9.5	2.0	6.5	2.0	7.5	ns
tPLH tPHL	Propagation Delay CP to I/On		2.0	12.0	2.0	12.0	2.0	7.2	2.0	9.5	2.0	6.5	2.0	7.5	ns
tPHL	Propagation Delay $\overline{MR}$ to Q0 or Q7		2.0	10.0	2.0	10.5	2.0	7.2	2.0	9.5	2.0	6.5	2.0	7.5	ns
tPHL	Propagation Delay $\overline{MR}$ to I/On		2.0	15.0	2.0	15.0	2.0	8.7	2.0	11.5	2.0	6.5	2.0	7.5	ns
tPZH tPZL	Output Enable Time $\overline{OE}$n to I/On		1.5	11.0	1.5	15.0	1.5	6.5	1.5	7.5	1.5	6.5	1.5	7.5	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$n to I/On		1.5	7.0	1.5	9.0	1.5	6.0	1.5	6.5	1.5	6.0	1.5	6.5	ns
tSU	Set-up Time HIGH or LOW S0 or S1 to CP		7.5	—	7.5	—	3.5	—	4.0	—	3.5	—	4.0	—	ns
tH	Hold Time HIGH or LOW S0 or S1 to CP		1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns
tSU	Set-up Time HIGH or LOW I/On, DS0 or DS7 to CP		5.5	—	5.5	—	4.0	—	4.5	—	4.0	—	4.5	—	ns
tH	Hold Time HIGH or LOW I/On, DS0 or DS7 to CP		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tW	CP Pulse width HIGH or LOW		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns
tW	$\overline{MR}$ Pulse Width LOW		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns
tREM	Recovery Time $\overline{MR}$ to CP		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

A

ORDERING INFORMATION



FEATURES:

- IDT54/74FCT399 equivalent to FAST™ speed
- **IDT54/74FCT399A 30% faster than FAST™**
- **IDT54/74FCT399C 45% faster than FAST™**

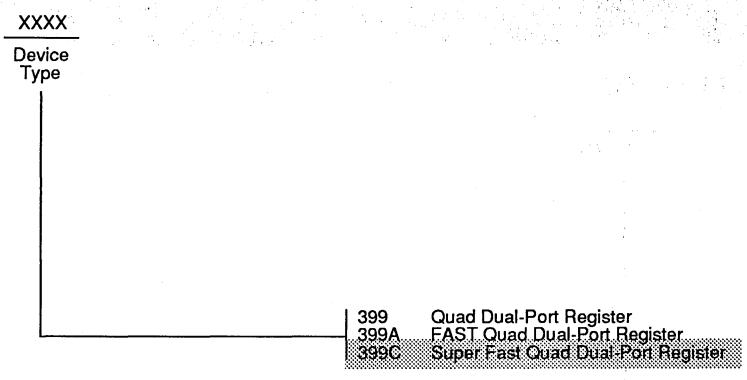
DESCRIPTION:

The IDT54/74FCT399/A/C are high-speed quad dual-port registers.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT399				IDT54/74FCT399A				IDT54/74FCT399C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	C_L = 50pF R_L = 500Ω	3.0	10.0	3.0	11.5	2.5	7.0	2.5	7.5	2.5	6.1	2.5	6.6	ns
t_{SU}	Set-up Time HIGH or LOW I_n to CP		4.0	—	4.5	—	3.5	—	4.0	—	3.5	—	4.0	—	ns
t_H	Hold Time HIGH or LOW I_n to CP		1.0	—	1.5	—	1.0	—	1.0	—	1.0	—	1.0	—	ns
t_{SU}	Set-up Time HIGH or LOW S to CP		9.0	—	9.5	—	8.5	—	9.0	—	8.5	—	9.0	—	ns
t_H	Hold Time HIGH or LOW S to CP		0	—	0	—	0	—	0	—	0	—	0	—	ns
t_W	CP Pulse Width HIGH or LOW		5.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

ORDERING INFORMATION



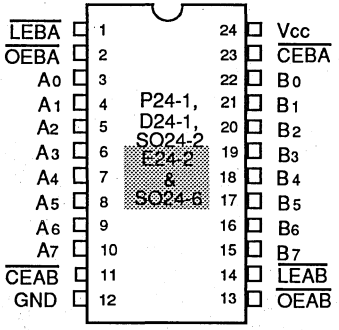
FEATURES:

- IDT54/74FCT543 equivalent to FAST™ speed
- **IDT54/74FCT543A 25% faster than FAST™**
- **IDT54/74FCT543C 40% faster than FAST™**

DESCRIPTION:

The IDT54/74FCT543/A/C is a non-inverting octal transceiver built using advanced CEMOS™, a dual metal CMOS technology.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK/EIAJ
TOP VIEW

A

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

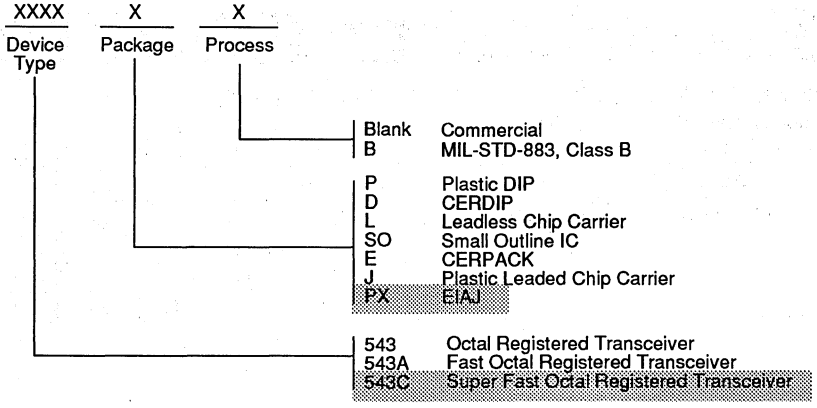
Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min.	I_{OH} = -300µA	V_{HC}[4]	V_{CC}	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT543				IDT54/74FCT543A				IDT54/74FCT543C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Transparent Mode An to Bn or Bn to An	CL = 50pF RL = 500Ω	2.5	8.5	2.5	10.0	2.5	6.5	2.5	7.5	2.5	5.3	2.5	6.1	ns
tPLH tPHL	Propagation Delay $\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn		2.5	12.5	2.5	14.0	2.5	8.0	2.5	9.0	2.5	7.0	2.5	8.0	ns
tPZH tPZL	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn $\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn		2.0	12.0	2.0	14.0	2.0	9.0	2.0	10.0	2.0	8.0	2.0	9.0	ns
tPHZ tPLZ	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn $\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn		2.0	9.0	2.0	13.0	2.0	7.5	2.0	8.5	2.0	6.5	2.0	7.5	ns
tSU	Set-up Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$		3.0	—	3.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tW	$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW		5.0	—	5.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns

ORDERING INFORMATION



The following section contains full data sheets that appeared in the 1991 LOGIC Data Book. These data sheets had changes to 50% or more of the overall contents and are now considered new. Refer to the bar at the top of each page to see where that page can be found in the 1991 LOGIC Data Book.

Integrated Device Technology, Inc.

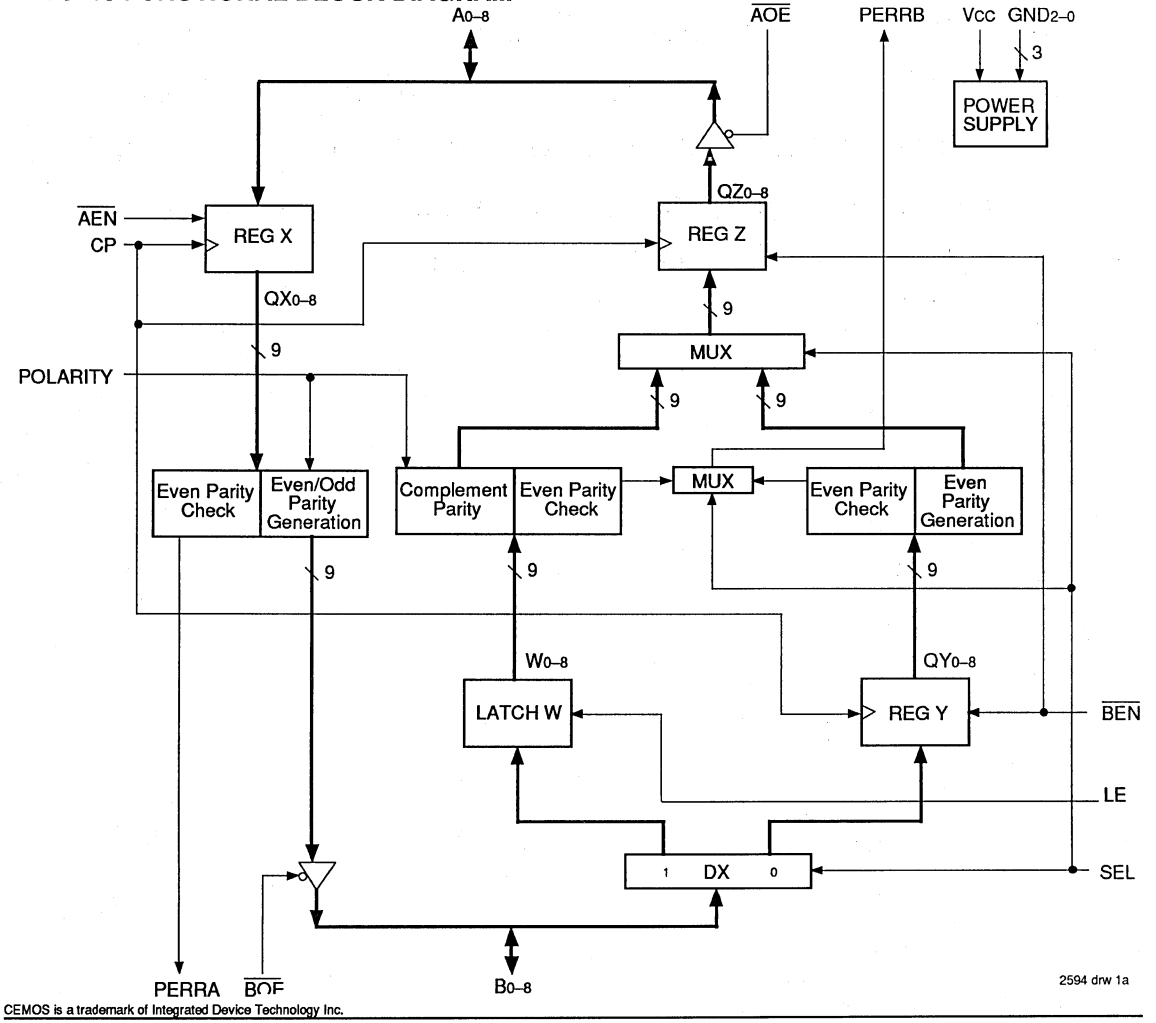
FAST CMOS OCTAL REGISTER TRANSCEIVER WITH PARITY

PRELIMINARY
IDT73210/A
IDT73211/A

FEATURES

- Two bidirectional interfacing ports
- Single-level pipeline register for one port and one-level (73211) or two-level (73210) pipeline register for the other port
- 8-bit wide interface ports plus parity bit
- Even parity checking in both directions
- Even/odd parity generation from Port A to Port B
- Even parity generation from Port B to Port A
- Parity polarity control
- High output drive capability: 64/48mA (commercial/ military)
- Available in 32-pin sidebraze DIP and surface mount 32-pin SOJ packages
- High-speed, low-power, CEMOS™ process technology
- Military product compliant to MIL-STD-883, Class B

IDT73210 FUNCTIONAL BLOCK DIAGRAM



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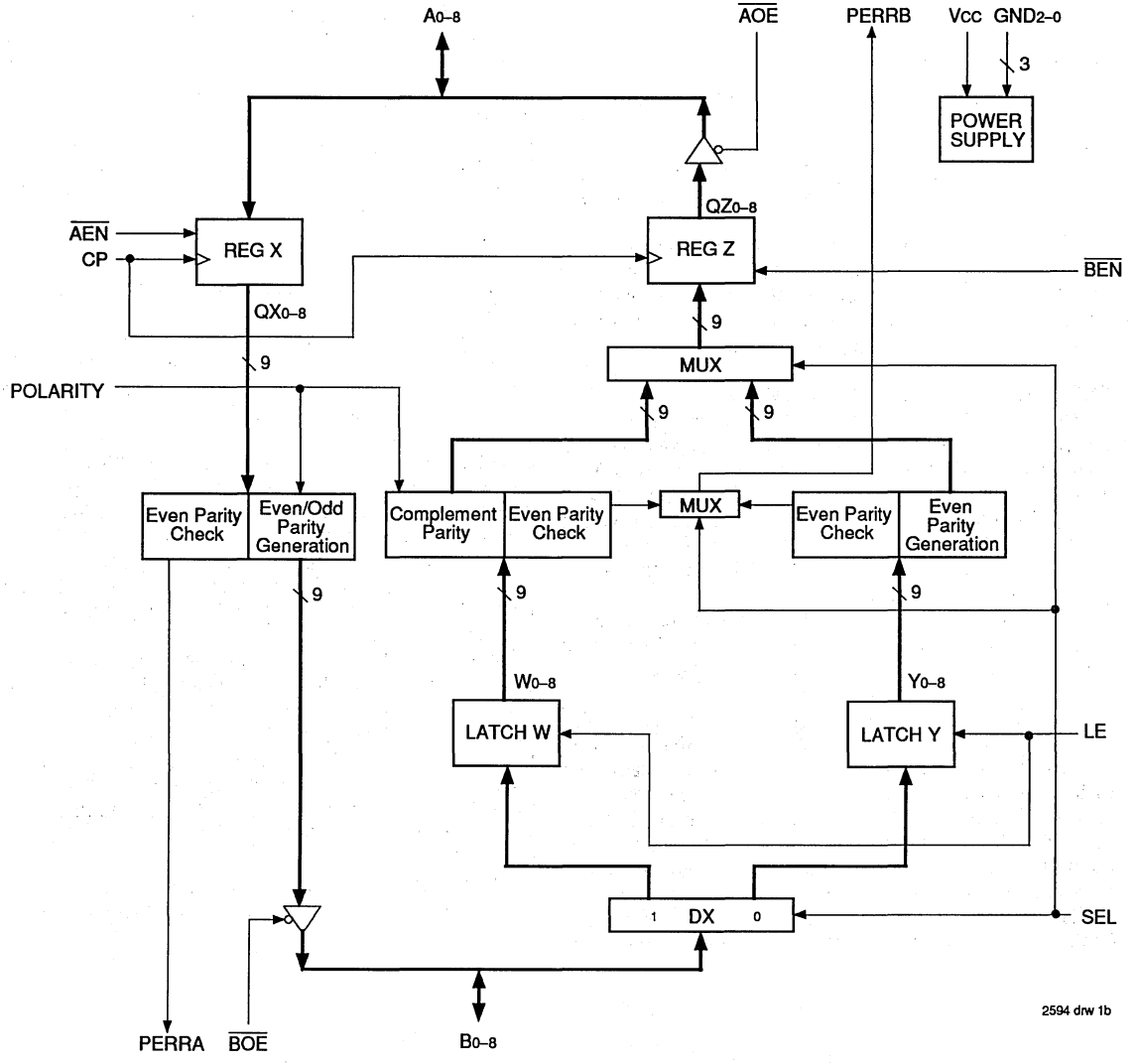
IDT73211 FUNCTIONAL BLOCK DIAGRAM



A

APPLICATIONS

- Cache memory bus interface
- Read and write buffers for RISC microprocessor system
- Registered transceiver with parity

FUNCTIONAL DESCRIPTION

The IDT73210/1 Octal Register Transceivers are high-speed, low-power data interface with data integrity checking capability.

They are designed for high-performance systems requiring bidirectional data transfer between two buses and maintaining error checking via parity.

In any RISC or CISC microprocessor system, the IDT73210/1 can be used to interface cache memory with main memory. Data integrity is ensured through parity checking. Control features allow dynamic reconfiguration of check/generate and odd/even parity options.

DETAILED FUNCTIONAL DESCRIPTION

Port A to Port B Path (IDT73210 and IDT73211) is comprised of a register (X), an even/odd parity generator and an even parity checker. The input data is on the A_{0-8} lines. When $\overline{AEN}$ is low, A_{0-8} is latched into Register X on the low-to-high CP transition. Even parity of the latched data is checked. If PERRA goes high, a parity error has occurred. A new parity bit, B_8, is generated. The output data bus is B_{0-8} and is enabled when $\overline{BOE}$ is low.

Port B to Port A Path (IDT73210) is comprised of a latch (W), two registers (Y and Z), an even parity generator/checker and a parity bit latch complementor. The input data bus is on the B_{0-8} lines.

When SEL is high, the incoming data is latched into Latch W. When LE is high, Latch W is transparent; when LE is low, Latch W is closed. The parity bit, B_8, can be complemented by the POLARITY pin. If POLARITY is low, the parity sense remains the same. If POLARITY is high, the parity sense is complemented. Parity is not generated in this path. Even parity of latched data is checked. If PERRB goes high, a parity error has occurred. When $\overline{BEN}$ is low, W_{0-8} is latched into Register Z on the low-to-high CP transition. The previous contents are held in Register Z if $\overline{BEN}$ is high or if there is no low-to-high CP transition. The output data bus is A_{0-8} and is enabled when $\overline{AOE}$ is low. When SEL is high, there is only a one clock cycle latency.

When SEL is low, the incoming data is latched into Register Y on the low-to-high CP transition, when $\overline{BEN}$ is low. Even parity of the registered data is checked. If PERRB goes high, a parity error has occurred. Even parity (QY_8) is generated on the contents in Register Y. When $\overline{BEN}$ is low, the contents of register Y are transferred to Register Z on the low-to-high CP transition. When $\overline{BOE}$ is low, the content of Register Z is made available at output Port A. When SEL is low, there is a two clock cycle latency.

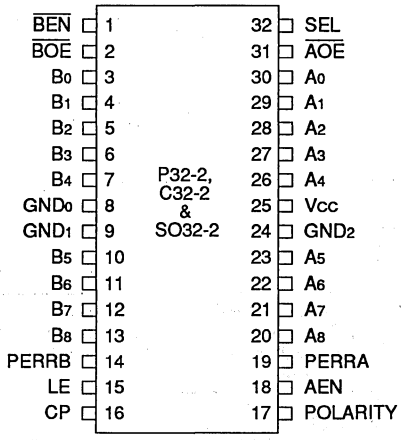
Port B to Port A Path (IDT73211) is comprised of latch (W),latch (Y), register (Z), an even parity generator/checker and a parity bit latch complementor. The input data bus is on the B_{0-8} lines.

When SEL is high, the incoming data is latched into Latch W. When LE is high, Latch W is transparent; when LE is low, Latch W is closed. The parity bit, B_8, can be complemented by the POLARITY pin. If POLARITY is low, the parity sense remains the same. If POLARITY is high, the parity sense is complemented. Parity is not generated in this path. Even parity of latched data is checked. If PERRB goes high, a parity error has occurred. When $\overline{BEN}$ is low, W_{0-8} is latched into Register Z on the low-to-high CP transition. The previous contents are held in Register Z if $\overline{BEN}$ is high or if there is no low-to-high CP transition. The output data bus is A_{0-8} and is enabled when $\overline{AOE}$ is low. When SEL is high, there is only a one clock cycle latency.

When SEL is low, the incoming data is latched into Latch Y when LE is high. Latch Y is closed when LE is low. Even parity of latched data is checked. If PERRB goes high, a parity error has occurred. Even parity (Y_8) is generated on the contents in Latch Y. When $\overline{BEN}$ is low, the contents of Latch Y are transferred to Register Z on the low-to-high CP transition. When $\overline{BOE}$ is low, the content of Register Z is made available at output Port A. When SEL is low, there is a one clock cycle latency.

The power pins are Vcc and GND_{0-2}. GND_0 is internal quiet ground, GND_1 is Port B ground and GND_2 is Port A ground.

PIN CONFIGURATIONS[1]



DIP/SOJ
TOP VIEW

NOTE:
1. GND_0 is internal quiet ground
   GND_1 is B Port ground
   GND_2 is A Port ground

A

PIN DESCRIPTIONS

Pin Name	I/O	Description
A_{0-8}	I/O	Data Port A.
$\overline{AEN}$	I	Clock enable (active low) for the register X.
$\overline{AOE}$	I	3-state output enable for Port A.
B_{0-8}	I/O	Data Port B.
$\overline{BEN}$	I	Clock enable (active low) for the registers Y and Z.
$\overline{BOE}$	I	3-state output enable for Port B.
LE	I	Latch enable input for Latch Y/Latch W of Port B. The Latch Y/Latch W is open when LE is high. Data is latched on the high-to-low transition of LE.
SEL	I	Input selection for Port B. SEL = 0 Register Y (73210); SEL = 1 Latch W SEL = 0 Latch Y (73211);
POLARITY	I	Polarity selection input. **Polarity** / **A to B Direction** / **B to A Direction** 0 / EVEN / Pass Parity 1 / ODD / Complement Parity
PERRA	O	Parity output error for Port A.
PERRB	O	Parity output error for Port B.
CP	I	Input clock.
VCC		+5 volts.
GND_{0-2}		Ground.

2594 tbl 01

OPERATING MODES SUMMARY

IDT73210/1 A TO B DIRECTION

Input	Reg. X	PERRA	Output (B8)	Output B0–8
A0–8	A0–8 → QX0–8 (CP = Lo to Hi) ($\overline{AEN}$ = 0)	Result of even parity check	Even/odd parity bit B8 = POLARITY XOR Even parity generate from QX0–7	QX0–8 → B0–8 ($\overline{BOE}$ = 0)

2594 tbl 02

IDT73210/1 B TO A DIRECTION WHEN SEL = 1

Input	Latch W	PERRB	Reg. Z (QZ8)	Reg. Z QZ0–8	Output (A8)	Output A0–8
B0–8	B0–8 → W0–8 (LE = 1)	Result of even parity check	Bit complemented by POLARITY (Even/odd parity translation)	W0–8 → QZ0–8 (CP = Lo to Hi) ($\overline{BEN}$ = 0)	A8 = POLARITY XOR W8	QZ0–8 → A0–8 ($\overline{AOE}$ = 0)

2594 tbl 03

IDT73210 B TO A DIRECTION WHEN SEL = 0

Input	Reg. Y	PERRB	Reg. Z (QZ8)	Reg. Z QZ0–8	Output (A8)	Output A0–8
B0–8	B0–8 → QY0–8 (CP = Lo to Hi) ($\overline{BEN}$ = 0)	Result of even parity check	Even parity generated bit	QY0–8 → QZ0–8 (CP = Lo to Hi) ($\overline{BEN}$ = 0)	A8 = Even parity generated from QY0–7	QZ0–8 → A0–8 ($\overline{BOE}$ = 0)

2594 tbl 04

IDT73211 B TO A DIRECTION WHEN SEL = 0

Input	Latch Y	PERRB	Reg. Z (QZ8)	Reg. Z QZ0–8	Output (A8)	Output A0–8
B0–8	B0–8 → Y0–8 (LE = 1)	Result of even parity check	Even parity generated bit	Y0–8 → QZ0–8 (CP = Lo to Hi) ($\overline{BEN}$ = 0)	A8 = Even parity generated from Y0–7	QZ0–8 → A0–8 ($\overline{BOE}$ = 0)

2594 tbl 05

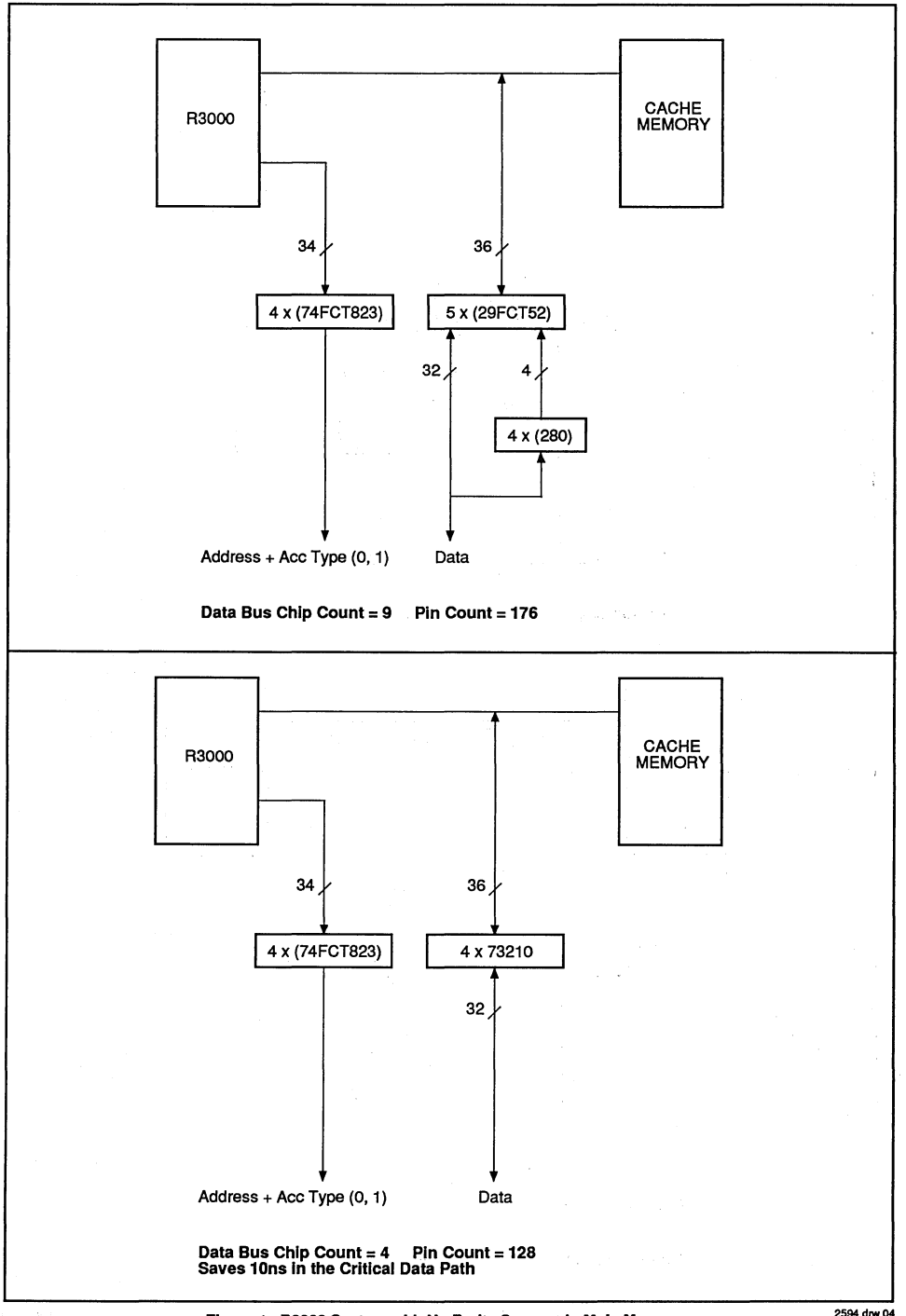


Figure 1. R3000 System with No Parity Support in Main Memory

2594 drw 04

A

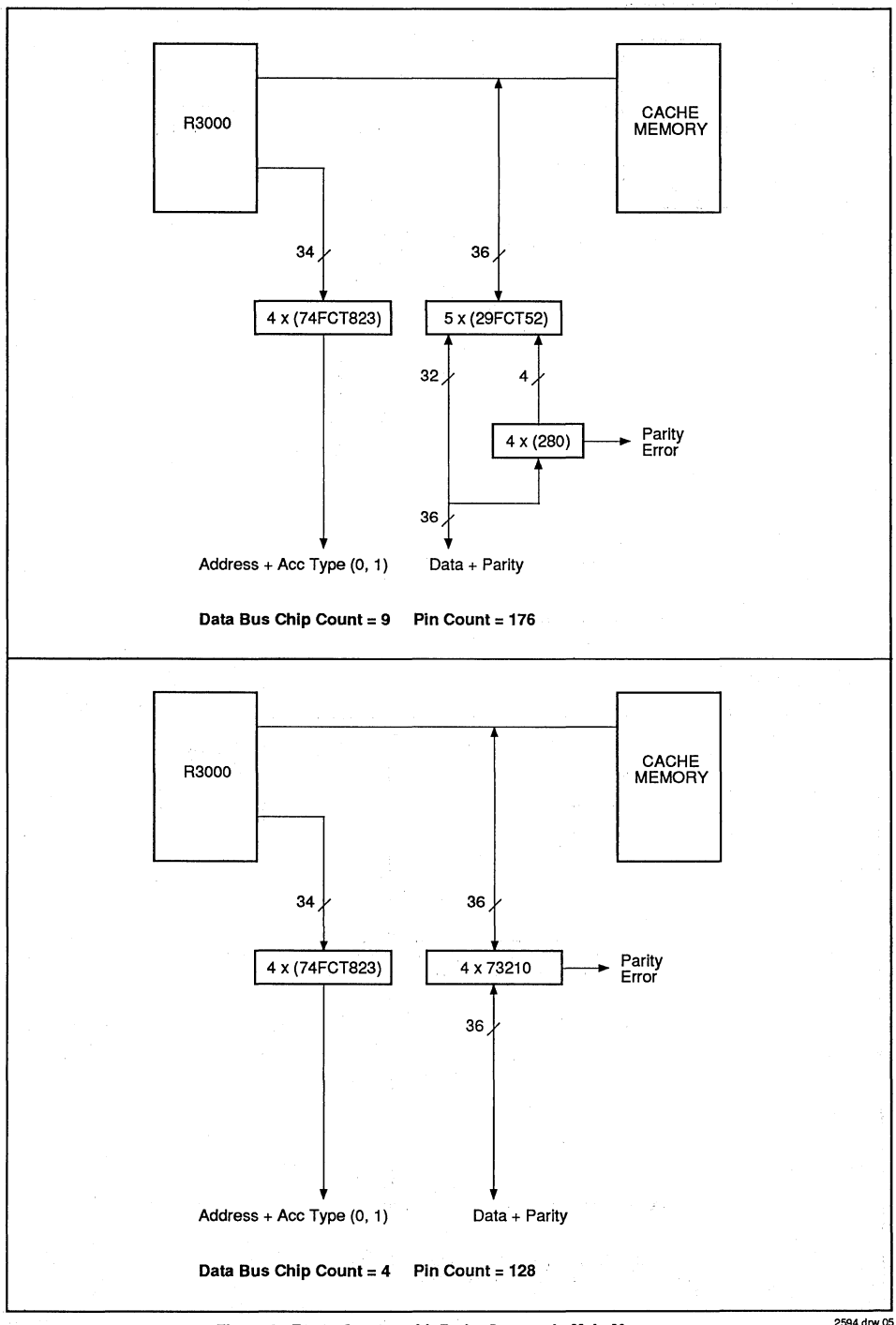


Figure 2. R3000 System with Parity Support in Main Memory

2594 drw 05

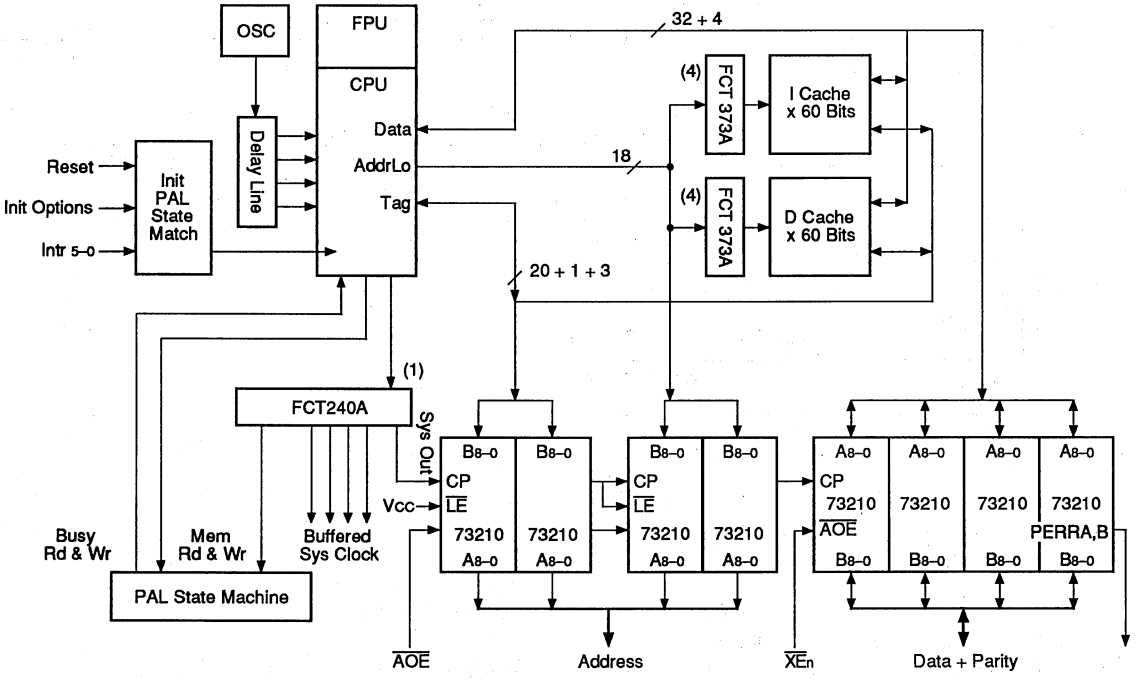


Figure 3. Read and Write Buffers Using Eight IDT73210/1

A

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
V_{CC}	Power Supply Voltage	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.2	1.5	W
I_{OUT}	Total Output Current	200	250	mA

NOTE: 2594 tbl 06

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF
$C_{I/O}$	Input – Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2594 tbl 07

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

The following conditions apply unless otherwise specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]			Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level			2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level			—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.		Except I/O	—	—	10	µA
		V_I = 2.7V		I/O pins	—	—	20	
I_{IL}	Input LOW Current	V_{CC} = Max.		Except I/O	—	—	-10	µA
		V_I = 0.5V		I/O pins	—	—	-20	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA			—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		PERRA, PERRB	-30	—	-150	mA
				A_{0-8}, B_{0-8}	-20	—	-75	
V_{OH}	Output HIGH Voltage	V_{CC} = Min.		I_{OH} = –12mA MIL.	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}		I_{OH} = –15mA COM'L.				
V_{OL}	Output LOW Voltage	V_{CC} = Min.	A_{0-8}	I_{OL} = 48mA MIL.	—	0.3	0.5	V
		V_{IN} = V_{IH} or V_{IL}	B_{0-8}	I_{OL} = 64mA COM'L.				
		V_{CC} = Min.	PERRA	I_{OL} = 20mA MIL.				
		V_{IN} = V_{IH} or V_{IL}	PERRB	I_{OL} = 24mA COM'L.				
V_H	Input Hysteresis for CP only	V_{CC} = 5V			—	200	—	mV

NOTES: 2594 tbl 09

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient, not production tested.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed 100 millisecond.

POWER SUPPLY CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CCQC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4[3]	COM'L.	—	0.3	1.0	mA/
			MIL.	—	0.3	1.5	Input
I_{CCD1}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Disabled f_{CP} = 10MHz 50% Duty Cycle f_i = 5MHz	V_{IN} = V_{CC} or GND	—	6.0	15	mA
I_{CCD2}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Disabled f_{CP} = 40MHz 50% Duty Cycle f_i = 20MHz	V_{IN} = V_{CC} or GND	—	24	60	mA

NOTES:

2594 tbl 08

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading, not production tested.
3. This parameter is not directly testable but is derived for use in the total power supply calculation.
4. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CCQC} + I_{CCQT} D_H N_T + I_{CCD}$
   I_{CCQC} = Quiescent Current
   I_{CCQT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at DH
   I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
   All currents are in milliamps and all frequencies are in megahertz.

A

IDT73210A, IDT73211A AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance) T_A = 0°C to +70°C; V_{CC} = 5V ± 5%
C_L = 50pF; R_L = 500Ω

Parameter	Description	Min.	Typ.(1)	Max.	Unit
t_{PHL} t_{PLH}	Propagation Delay Clock to A_{0-8} ($\overline{AOE}$ = Low)	—	—	7.2	ns
t_{PHL} t_{PLH}	Propagation Delay Clock to B_{0-8} ($\overline{BOE}$ = Low)	—	—	9.0	ns
t_{PHL} t_{PLH}	Propagation Delay CP to PERRA, PERRB	—	—	9.0	ns
t_{PHL} t_{PLH}	Propagation Delay POLARITY to B_8	—	—	8.5	ns
t_{PHL} t_{PLH}	Propagation Delay B_{0-8} to PERRB LE = High	—	—	9	ns
t_S	Set-up Time A_{0-8}, B_{0-8} (Reg Y-73210 only), POLARITY, SEL to CP	3.0	—	—	ns
t_H	Hold Time to CP — A_{0-8}, B_{0-8} (Reg Y-73210 only)	1.0	—	—	ns
	Hold Time to CP — POLARITY, SEL	1.5	—	—	ns
t_S	Set-up Time $\overline{AEN}$, $\overline{BEN}$ to CP	3.0	—	—	ns
t_H	Hold Time $\overline{AEN}$, $\overline{BEN}$ to CP	1.5	—	—	ns
t_S	Set-up Time B_{0-8} to LE	3.0	—	—	ns
t_H	Hold Time B_{0-8} to LE	1.5	—	—	ns
t_S	Set-up Time B_{0-8} to CP (Reg Z); LE = High	3.5	—	—	ns
t_H	Hold Time B_{0-8} to CP (Reg Z); LE = High	1.5	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{AOE}$ to A_{0-8}, $\overline{BOE}$ to B_{0-8}	—	—	7.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{AOE}$ to A_{0-8}, $\overline{BOE}$ to B_{0-8}	—	—	6.0	ns
t_{PWH}	Clock Pulse Width High	7.0	5.0	—	ns
t_{PWL}	Clock Pulse Width Low	7.0	5.0	—	ns

NOTE:
1. Typical values are at V_{CC} = 5.0V and +25°C ambient, not production tested.

2594 tbl 10

IDT73210A, IDT73211A AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance) T_A = -55°C to +125°C; V_{CC} = 5V ± 10%
C_L = 50pF; R_L = 500Ω

Parameter	Description		Min.	Typ.[1]	Max.	Unit
tPHL tPLH	Propagation Delay Clock to A_{0-8} ($\overline{AOE}$ = Low)		—	—	9	ns
tPHL tPLH	Propagation Delay Clock to B_{0-8} ($\overline{BOE}$ = Low)		—	—	10.5	ns
tPHL tPLH	Propagation Delay CP to PERRA, PERRB		—	—	10.5	ns
tPHL tPLH	Propagation Delay POLARITY to B_8		—	—	9.5	ns
tPHL tPLH	Propagation Delay B_{0-8} to PERRB LE = High		—	—	10	ns
tS	Set-up Time A_{0-8}, B_{0-8} (Reg Y-73210 only), POLARITY, SEL to CP		3.5	—	—	ns
tH	Hold Time to CP	A_{0-8}, B_{0-8} (Reg Y-73210 only)	1.5	—	—	ns
		POLARITY, SEL	2.0	—	—	ns
tS	Set-up Time $\overline{AEN}$, $\overline{BEN}$ to CP		3.5	—	—	ns
tH	Hold Time $\overline{AEN}$, $\overline{BEN}$ to CP		1.5	—	—	ns
tS	Set-up Time B_{0-8} to LE		3.5	—	—	ns
tH	Hold Time B_{0-8} to LE		1.5	—	—	ns
tS	Set-up Time B_{0-8} to CP (Reg Z); LE = High		4.5	—	—	ns
tH	Hold Time B_{0-8} to CP (Reg Z); LE = High		2.5	—	—	ns
tPZH tPZL	Output Enable Time $\overline{AOE}$ to A_{0-8}, $\overline{BOE}$ to B_{0-8}		—	—	8.0	ns
tPHZ tPLZ	Output Disable Time $\overline{AOE}$ to A_{0-8}, $\overline{BOE}$ to B_{0-8}		—	—	7.5	ns
tPWH	Clock Pulse Width High		8	6	—	ns
tPWL	Clock Pulse Width Low		8	6	—	ns

NOTE:
1. Typical values are at Vcc = 5.0V and +25°C ambient, not production tested.

2594 tbl 11

A

IDT73210, IDT73211 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance) T_A = 0°C to +70°C; V_{CC} = 5V ± 5%
C_L = 50pF; R_L = 500Ω

Parameter	Description	Min.	Typ.(1)	Max.	Unit
t_{PHL} t_{PLH}	Propagation Delay Clock to A_{0-8} ($\overline{AOE}$ = Low)	—	—	9	ns
t_{PHL} t_{PLH}	Propagation Delay Clock to B_{0-8} ($\overline{BOE}$ = Low)	—	—	10.5	ns
t_{PHL} t_{PLH}	Propagation Delay CP to PERRA, PERRB	—	—	10.5	ns
t_{PHL} t_{PLH}	Propagation Delay POLARITY to B_8	—	—	9.5	ns
t_{PHL} t_{PLH}	Propagation Delay B_{0-8} to PERRB LE = High	—	—	10	ns
t_S	Set-up Time A_{0-8}, B_{0-8} (Reg Y-73210 only), POLARITY, SEL to CP	3.5	—	—	ns
t_H	Hold Time to CP — A_{0-8}, B_{0-8} (Reg Y-73210 only)	1.0	—	—	ns
	Hold Time to CP — POLARITY, SEL	1.5	—	—	ns
t_S	Set-up Time $\overline{AEN}$, $\overline{BEN}$ to CP	3.5	—	—	ns
t_H	Hold Time $\overline{AEN}$, $\overline{BEN}$ to CP	1.5	—	—	ns
t_S	Set-up Time B_{0-8} to LE	3.5	—	—	ns
t_H	Hold Time B_{0-8} to LE	1.5	—	—	ns
t_S	Set-up Time B_{0-8} to CP (Reg Z); LE = High	4.5	—	—	ns
t_H	Hold Time B_{0-8} to CP (Reg Z); LE = High	1.5	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{AOE}$ to A_{0-8}, $\overline{BOE}$ to B_{0-8}	—	—	8.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{AOE}$ to A_{0-8}, $\overline{BOE}$ to B_{0-8}	—	—	7.5	ns
t_{PWH}	Clock Pulse Width High	7.0	5.0	—	ns
t_{PWL}	Clock Pulse Width Low	7.0	5.0	—	ns

NOTE:
1. Typical values are at V_{CC} = 5.0V and +25°C ambient, not production tested.

2594 tbl 12

IDT73210, IDT73211 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance) T_A = -55°C to +125°C; V_{CC} = 5V ± 10%
C_L = 50pF; R_L = 500Ω

Parameter	Description	Min.	Typ.[1]	Max.	Unit
t_{PHL} t_{PLH}	Propagation Delay Clock to A_{0-8} ($\overline{AOE}$ = Low)	—	—	11	ns
t_{PHL} t_{PLH}	Propagation Delay Clock to B_{0-8} ($\overline{BOE}$ = Low)	—	—	12	ns
t_{PHL} t_{PLH}	Propagation Delay CP to PERRA, PERRB	—	—	12	ns
t_{PHL} t_{PLH}	Propagation Delay POLARITY to B_8	—	—	11	ns
t_{PHL} t_{PLH}	Propagation Delay B_{0-8} to PERRB LE = High	—	—	11.5	ns
t_S	Set-up Time A_{0-8}, B_{0-8} (Reg Y-73210 only), POLARITY, SEL to CP	3.5	—	—	ns
t_H	Hold Time to CP — A_{0-8}, B_{0-8} (Reg Y-73210 only)	1.5	—	—	ns
	Hold Time to CP — POLARITY, SEL	2.0	—	—	ns
t_S	Set-up Time $\overline{AEN}$, $\overline{BEN}$ to CP	3.5	—	—	ns
t_H	Hold Time $\overline{AEN}$, $\overline{BEN}$ to CP	2	—	—	ns
t_S	Set-up Time B_{0-8} to LE	3.5	—	—	ns
t_H	Hold Time B_{0-8} to LE	2	—	—	ns
t_S	Set-up Time B_{0-8} to CP (Reg Z); LE = High	5	—	—	ns
t_H	Hold Time B_{0-8} to CP (Reg Z); LE = High	3	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{AOE}$ to A_{0-8}, $\overline{BOE}$ to B_{0-8}	—	—	10	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{AOE}$ to A_{0-8}, $\overline{BOE}$ to B_{0-8}	—	—	9	ns
t_{PWH}	Clock Pulse Width High	8	6	—	ns
t_{PWL}	Clock Pulse Width Low	8	6	—	ns

NOTE:
1. Typical values are at Vcc = 5.0V and +25°C ambient, not production tested.

2594 tbl 13

A

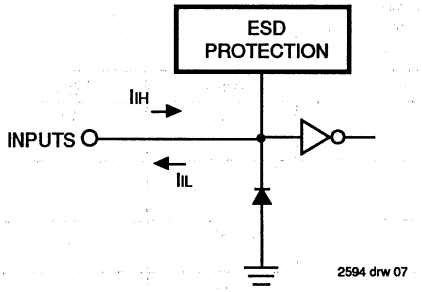


Figure 4. Input Interface Circuit

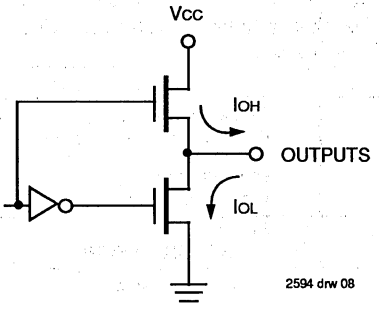
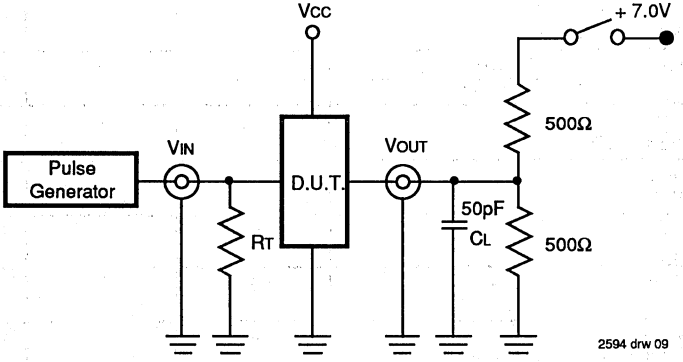


Figure 5. Output Interface Circuit



DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance
R_L = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

Figure 6. AC Test Load Circuit

AC TEST CONDITIONS

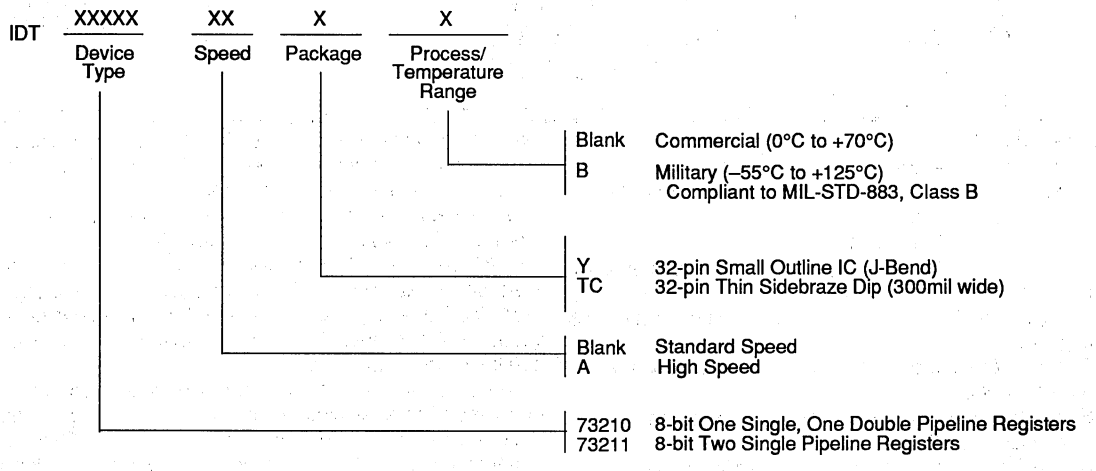
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 6

2594 tbl 12

Test	Switch
Open Drain Disable Low Enable Low	Closed
All other Tests	Open

2594 tbl 13

ORDERING INFORMATION



A

Integrated Device Technology, Inc.

64-BIT FLOW-THRU ERROR DETECTION AND CORRECTION UNIT

PRELIMINARY
IDT49C466

FEATURES:

- 64-bit wide Flow-thruEDC™
- Separate System and Memory Data Input/Output Buses
- — Error Detect Time: 15ns
  — Error Correct Time: 20ns
- Corrects all single bit errors; Detects all double bit errors and some multiple bit errors
- Configurable 16-deep system bus read/write buffer with flag indicators
- Simultaneous check bit generation and data correction of memory data
- Supports partial word writes on byte boundaries
- Low noise output
- Sophisticated error diagnostics and error logging
- Parity generation on system data bus
- 208-pin Pin Grid Array and Plastic Quad Flatpack

DESCRIPTION:

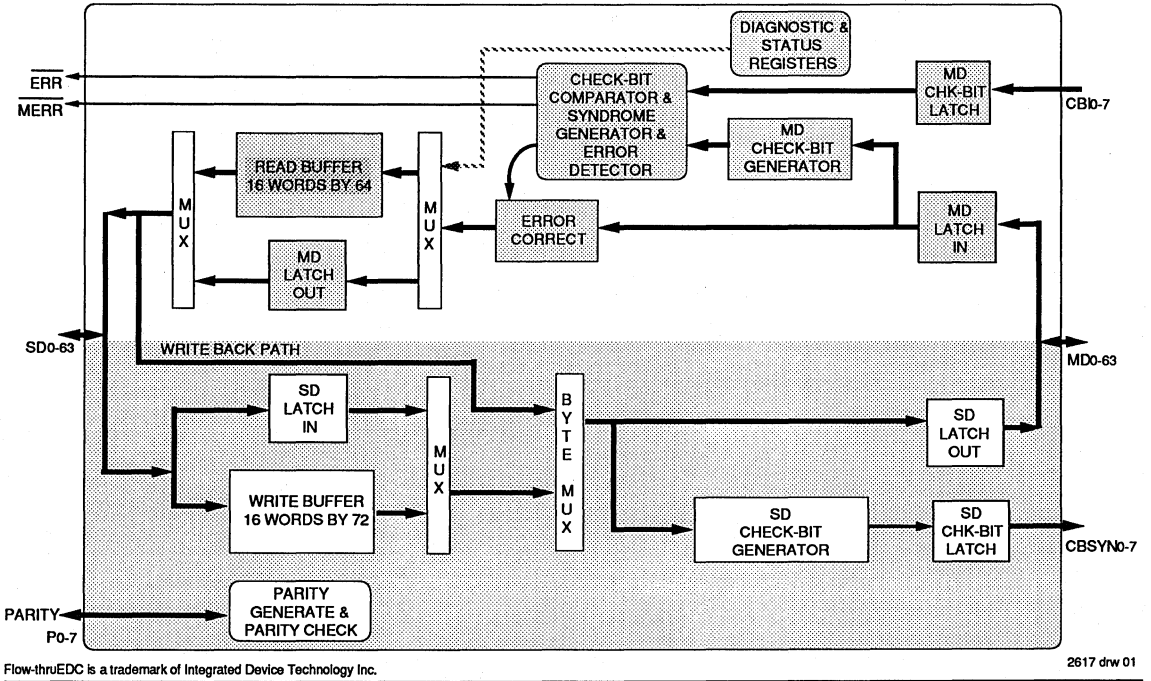
The IDT49C466 64-bit Flow-thruEDC™ is a high-speed error detection and correction unit to ensure data integrity in high reliability memory systems. The flow-thru architecture, with separate system and memory data buses, is ideally suited for pipelined memory systems.

Implementing a Hamming code in the 8-bit wide check bit bus, the IDT49C466 corrects all single bit hard and soft errors, and detects all double bit errors. The read/write buffers can store up to sixteen 64/72-bit words until the system bus is ready (during reads) or until the system bus is released (during writes). Full and empty flags indicate whether additional data can be written to the EDC.

The simultaneous check bit generation and data correction of memory data eliminates the separate correction and generation modes found on other EDC units. Check bit generation for partial word writes on byte boundaries is supported on the IDT49C466.

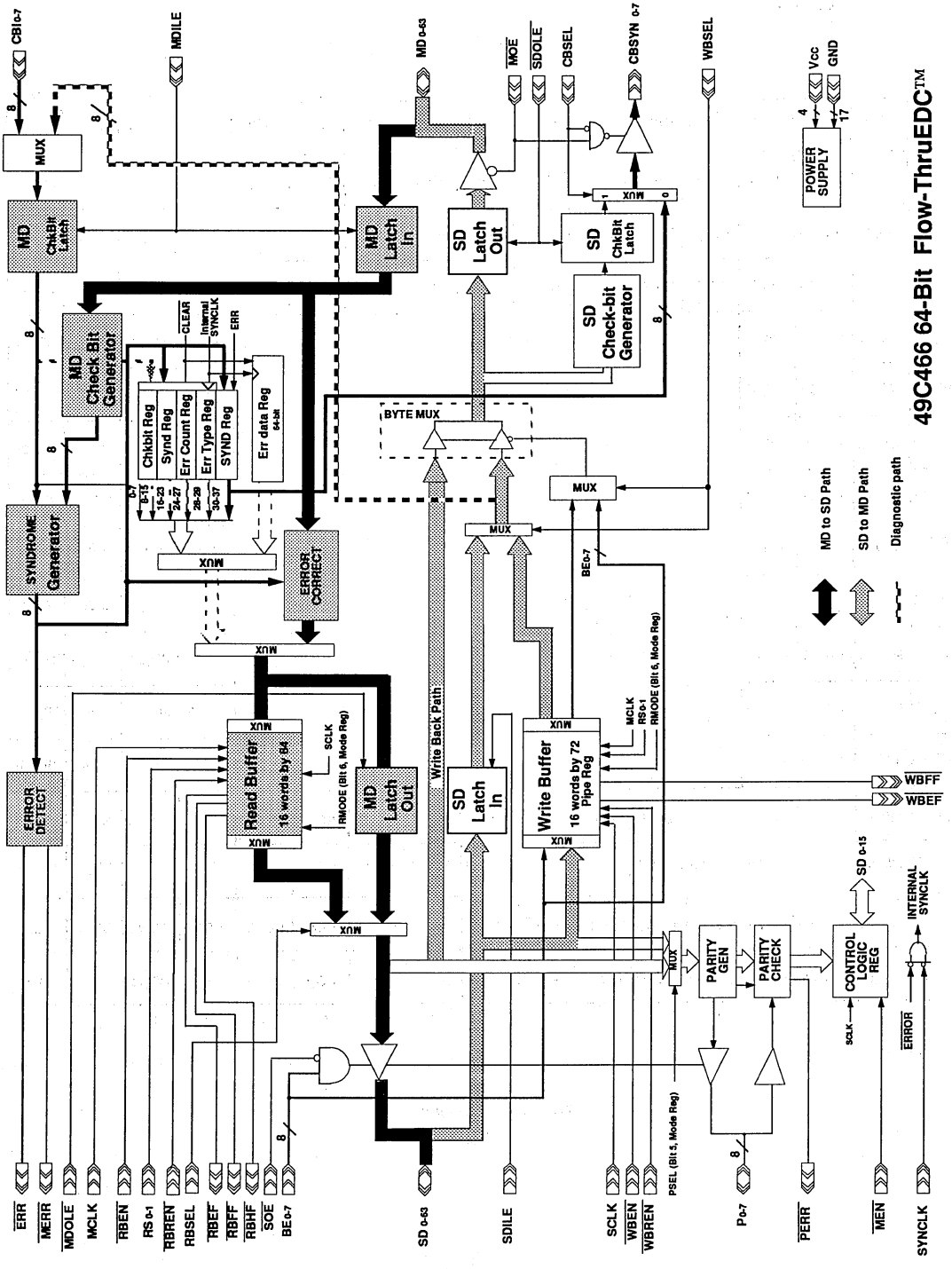
Diagnostics features include a syndrome latch from which the error bit can be located, a four bit error counter which logs up to 15 errors, and an error data latch which stores the complete error data word. Parity can be generated and checked on the system bus by the IDT49C466.

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM



Flow-thruEDC is a trademark of Integrated Device Technology Inc.

2617 drw 01


49C466 64-Bit Flow-ThruEDC™
MD to SD Path
SD to MD Path
Diagnostic path
CBI0-7
MDILE
MD 0-63
MOE
SDOLE
CBSEL
CBSYN 0-7
WBSEL
Vcc
GND
POWER SUPPLY
MUX
MD ChkBit Latch
MD Latch In
SD Latch Out
SD ChkBit Latch
SD Check-bit Generator
MD Check Bit Generator
CLEAR
Internal SYNCLK
ERR
Chkbit Reg
Synd Reg
Err Count Reg
Err Type Reg
SYND Reg
Err data Reg 64-bit
BYTE MUX
SYNDROME Generator
ERROR CORRECT
ERROR DETECT
Read Buffer 16 words by 64
Write Buffer 16 words by 72 Pipe Reg
MD Latch Out
SD Latch In
Write Back Path
SCLK
RMODE (Bit 6, Mode Reg)
MCLK
RS0-1
RMODE (Bit 6, Mode Reg)
BE0-7
WBFF
WBEF
PARITY GEN
PARITY CHECK
CONTROL LOGIC REG
SD 0-15
INTERNAL SYNCLK
PSEL (Bit 5, Mode Reg)
ERR
MERR
MDOLE
MCLK
RBEN
RS 0-1
RBREN
RBSEL
RBEF
RBFF
RBHF
SOE
BE0-7
SD 0-63
SDILE
SCLK
WBEN
WBREN
P0-7
PERR
MEN
SYNCLK

A

PIN CONFIGURATION

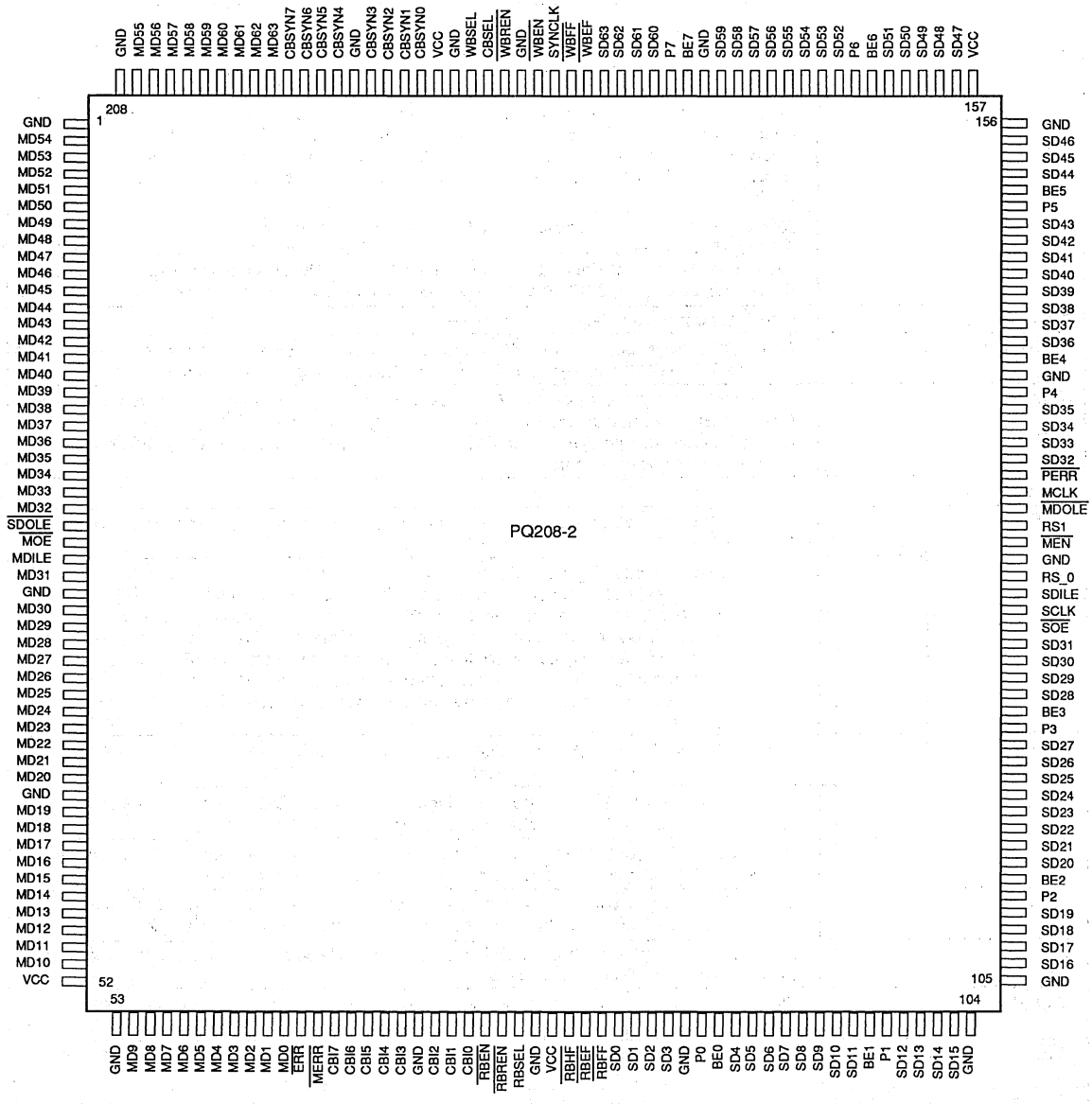
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	
17	MD_10	MD_8	MD_2	MD_1	$\overline{\text{MERR}}$	CBI_6	CBI_1	$\overline{\text{RBEN}}$	RBSEL	$\overline{\text{RBHF}}$	SD_2	SD_3	BE0	SD_9	SD_10	SD_12	SD_15	17
16	MD_13	MD_9	MD_6	MD_3	$\overline{\text{ERR}}$	CBI_3	CBI_2	$\overline{\text{RBREN}}$	$\overline{\text{RBEF}}$	$\overline{\text{RBFF}}$	SD_1	SD_4	SD_6	SD_8	SD_13	SD_16	SD_17	16
15	MD_17	MD_12	MD_11	MD_5	MD_4	CBI_7	CBI_4	CBI_0	GND	SD_0	P0	SD_7	P1	BE1	SD_14	SD_19	SD_21	15
14	MD_18	MD_19	MD_15	GND	MD_7	MD_0	CBI_5	GND	Vcc	GND	SD_5	SD_11	GND	GND	P2	BE2	SD_20	14
13	MD_23	MD_20	MD_14	Vcc										SD_18	SD_22	SD_24	SD_25	13
12	MD_25	MD_22	MD_21	MD_16										SD_23	SD_26	SD_28	SD_27	12
11	MD_27	MD_28	MD_24	GND										P3	BE3	SD_30	SD_29	11
10	MD_31	MD_30	MD_29	MD_26										SD_31	$\overline{\text{SOE}}$	SDILE	SCLK	10
9	$\overline{\text{SDOLE}}$	$\overline{\text{MOE}}$	MDILE	GND				G208-1						$\overline{\text{MDOLE}}$	GND	$\overline{\text{MEN}}$	RS_0	9
8	MD_33	MD_32	MD_34	MD_35										GND	SD_33	MCLK	RS_1	8
7	MD_37	MD_36	MD_39	MD_40										SD_37	SD_34	SD_32	$\overline{\text{PERR}}$	7
6	MD_41	MD_38	MD_42	MD_45										SD_42	SD_38	P4	SD_35	6
5	MD_43	MD_44	MD_46	MD_52										GND	P5	BE4	SD_36	5
4	MD_48	MD_49	MD_50	GND	GND	MD_61	CBSYN4	Vcc	GND	SD_61	GND	SD_54	SD_49	VCC	SD_43	SD_39	SD_40	4
3	MD_47	MD_51	MD_56	MD_60	MD-59	CBSYN6	GND	GND	$\overline{\text{WBEN}}$	SD_62	SD_59	SD_57	SD_53	SD_51	SD_45	SD_44	SD_41	3
2	MD_53	MD_54	MD_57	CBSYN7	CBSYN5	CBSYN2	CBSYN0	$\overline{\text{WBREN}}$	SYNCLK	$\overline{\text{WBEF}}$	SD_60	BE7	SD_55	BE6	SD_50	SD_47	BE5	2
1	MD_55	MD_58	MD_62	MD_63	CBSYN3	CBSYN1	WBSEL	CBSEL	$\overline{\text{WBFF}}$	SD_63	P7	SD_58	SD_56	P6	SD_52	SD_48	SD_46	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	

Pin 1 reference

2617 drw 03

208-pin PGA Package
Top View

PIN CONFIGURATION



PQFP

Top View

2617 drw 04

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PIN DESCRIPTION

Pin Name	I/O	Description
Data Buses		
SD_{0-63}	I/O	**System Data Bus:** is a bidirectional 64-bit bus interfacing to the system or CPU. When System Output Enable, $\overline{SOE}$, is high or Byte Enable, BE_{0-7}, is low, data is input. The data is latched into the system data (SD) latch when the System Data Input Latch Enable (SDILE) is low. The System Data Bus outputs corrected memory data during a read operation. Corrected data can come from the memory data (MD) output latch or the content of the read buffer. When the Read Buffer Select (RBSEL) pin is low, the MD latch is selected. When RBSEL is high, the read buffer content is selected. When System Output Enable, $\overline{SOE}$, is low and Byte Enable, BE_{0-7}, is high, the SD bus output drivers are enabled.
MD_{0-63}	I/O	**Memory Data Bus:** is a bidirectional 64-bit bus interfacing to the memory. During a read cycle, memory data is input for error detection and correction. Data is latched in the memory data (MD) input latch when Memory Data Input Latch Enable (MDILE) is low. During a memory write cycle, data from the SD output latch (WBSEL=0)or the write buffer (WBSEL=1)is output on the Memory Data Bus.
CBI_{0-7}	I	**Check Bit Inputs:** interface to the check bit memory.
$CBSYN_{0-7}$	O	**Check Bit or Syndrome Output:**. When CBSEL is low and $\overline{MOE}$ is low the generated check bits are selected. When CBSEL is high and $\overline{MOE}$ is high, the syndrome bits are selected.
P_{0-7}	I/O	**Parity Input/output for bytes 0 to 7:** These pins are parity inputs when the corresponding Byte Enable (BE) is low, and are used to generate the parity error signal ($\overline{PERR}$). These pins are outputs when the corresponding Byte Enable (BE) is high. The internal parity select bit (PSEL) of the mode register selects odd or even parity.
Control Inputs		
$\overline{SOE}$	I	**System Output Enable:** enables system data output drivers if the corresponding Byte Enable (BE_{0-7}) is high.
BE_{0-7}	I	**Byte Enable:** is used along with $\overline{SOE}$, to enable the System Data outputs for a particular byte. For example, if BE_1 is high, the System data outputs for byte 1 (SD_{8-15}) are enabled. The BE_{0-7} pins also control the data byte mux. If a particular BE is high during a memory read cycle, data is fed back to the memory data bus and used for check bit generation of that byte. This is used during partial word write operations and rewriting corrected data to the memory. If a particular BE is low, data from the system data latch and write buffer is directed to the memory data bus and used for check bit generation of that byte, used in writing new data during a partial word write operation. BE is buffered with the data in the write buffer.
$\overline{MOE}$	I	**Memory Output Enable:** when low, enables the output buffers of the memory data bus (MD). It also controls the check bit output buffer enable.
MDILE	I	**Memory Data Input Latch Enable:** on the high to low transition latches data at the MD inputs and the checkbits at the CBI inputs. The latch is transparent when MDILE is high.
$\overline{MDOLE}$	I	**Memory Data Output Latch Enable:** latches data into the MD output latch during the low to high transition of $\overline{MDOLE}$. When $\overline{MDOLE}$ is low, the MD output latch is transparent.
$\overline{SDOLE}$	I	**System Data Output Latch Enable:** latches data in the SD output latch and the SD checkbit latch on the low to high transition of $\overline{SDOLE}$. The latch is transparent when $\overline{SDOLE}$ is low.
SDILE	I	**System Data Input Latch Enable:** latches in the SD input latch on the high to low transition. When SDILE is high, the SD input latch is transparent.
WBSEL	I	**Write Buffer Select:** when high, the output of the write buffer is selected. When the WBSEL is low, output from the SD input latch is selected.
$\overline{WBEN}$	I	**Write Buffer Enable:** allows system data (SD) input to be written to the write buffer on the SCLK rising edge.
$\overline{WBREN}$	I	**Write Buffer Read Enable:** when low, allows data to be read from the the write buffer on MCLK rising edge.
RS_{0-1}	I	**Reset and Select pins** (read and write buffer FIFOs) RS_1 RS_0 Function 0 0 Reset 16-deep FIFO or first 8-deep FIFO 0 1 Reset second 8-deep FIFO 1 0 Select 16-deep FIFO or first 8-deep FIFO 1 1 Select second 8-deep FIFO

2617 tbl 01

PIN DESCRIPTION (Continued)

Pin Name	I/O	Description
RBSEL	I	**Read Buffer Select:** when high the output of the read buffer is selected. When low, data from the MD output latch is selected.
$\overline{\text{RBEN}}$	I	**Read Buffer Enable:** when low allows data to be written into the read buffer on the low to high transition of the memory clock.
$\overline{\text{RBREN}}$	I	**Read Buffer Enable:** when low, allows data to be read from the read buffer on the low-to-high transition of SCLK
CBSEL	I	**Checkbit Select:** when high, selects the syndrome bits at the CBSYN0-7 output. When CBSEL is low, the checkbits are selected.
$\overline{\text{MEN}}$	I	**Mode Enable Input:** When low, data on the SD bus is loaded into the EDC mode register on the low-to-high transition of the SCLK. The mode register is used to determine the modes of the EDC.
Clock Inputs		
MCLK	I	**Memory Clock:** On the low to high transition of MCLK, memory data is written to the read buffer when $\overline{\text{RBEN}}$ is low. Data is read from the write buffer when $\overline{\text{WBREN}}$ is low on the low to high transition of MCLK.
SCLK	I	**System Clock:** On the low to high transition of the SYSCLK, data is read from the read buffer when $\overline{\text{RBREN}}$ is low. Data on the system data bus is written into the write buffer when $\overline{\text{WBEN}}$ is low on the low to high transition of SCLK.
SYNCLK	I	**SYNdrome CLocK:** If $\overline{\text{ERR}}$ is high, and the Error Counter indicates zero errors, syndrome bits are clocked into the Syndrome Register and data from the outputs of the Memory Data input latch are clocked into the Error-Data Register on the low-to-high edge of SYNCLK. If $\overline{\text{ERR}}$ is low, the Error Counter will increment on the low-to-high edge of SYNCLK, unless the Error Counter indicates fifteen errors.
Status Outputs		
$\overline{\text{WBEF}}$	O	**Write Buffer Empty Flag:** when low, indicates that the last data word in the write buffer has just been output. Further read operations are then inhibited. At reset, the $\overline{\text{WBEF}}$ is low.
$\overline{\text{WBFF}}$	O	**Write Buffer Full Flag:** when low, inhibits further write operations to the buffer and indicates that the write buffer is full. After a reset, $\overline{\text{WBFF}}$ goes high.
$\overline{\text{RBEF}}$	O	**Read Buffer Empty Flag:** when low, indicates that the last data word in the read buffer has just been output. Further read operations are then inhibited. At reset, the $\overline{\text{RBEF}}$ is low.
$\overline{\text{RBHF}}$	O	**Read Buffer Half-full Flag:** when low, indicates that there are eight or more data words (in the 16-deep configuration) or four or more data words (in the dual 8-deep configuration) in the read buffer. The flag will return high when less than eight (or four) data words are in the buffer.
$\overline{\text{RBFF}}$	O	**Read Buffer Full Flag:** when low, inhibits further write operations to the buffer and indicates that the read buffer is full. After a reset, $\overline{\text{RBFF}}$ goes high.
$\overline{\text{ERR}}$	O	**Error Flag:** In normal mode (Mode 3), when $\overline{\text{ERR}}$ is low, a data error is indicated. The $\overline{\text{ERR}}$ is not latched internally.
$\overline{\text{MERR}}$	O	**Multiple Error Flag:** In normal mode (Mode 3), when $\overline{\text{MERR}}$ is low, a multiple data error is indicated. The $\overline{\text{MERR}}$ is not latched internally.
$\overline{\text{PERR}}$	O	**Parity Error Flag:** when low, indicates a parity error on the system data bus input.
Power Supply		
Vcc	P	Power Supply Voltage, +5 volts.
GND	P	Ground.

2617 tbl 02

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DETAILED DESCRIPTION —

64-BIT MODIFIED HAMMING CODE - CHECKBIT ENCODING CHART(1, 2)

Generated Checkbits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB0	Even (XOR)		X	X	X		X			X	X		X			X	
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)	X	X	X	X	X	X	X	X								
CB7	Even (XOR)	X	X	X	X	X	X	X	X								

2617 tbl 03

Generated Checkbits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CB0	Even (XOR)		X	X	X		X			X	X		X			X	
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)									X	X	X	X	X	X	X	X
CB7	Even (XOR)									X	X	X	X	X	X	X	X

2617 tbl 04

Generated Checkbits	Parity	Participating Data Bits															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
CB0	Even (XOR)	X				X		X	X			X		X	X		X
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)	X	X	X	X	X	X	X	X								
CB7	Even (XOR)									X	X	X	X	X	X	X	X

2617 tbl 05

Generated Checkbits	Parity	Participating Data Bits															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CB0	Even (XOR)	X				X		X	X			X		X	X		X
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)									X	X	X	X	X	X	X	X
CB7	Even (XOR)	X	X	X	X	X	X	X	X								

2617 tbl 06

NOTES:

1. The table indicates the data bits participating in the checkbit generation. For example, checkbit CB0 is the Exclusive-OR function of the 64 data input bits marked with an X.
2. The checkbit is generated as either an XOR or an XNOR of the 64 data bits noted by an "X" in the table.

DETAILED DESCRIPTION —

64-BIT SYNDROME DECODE TO BIT-IN-ERROR(1)

				HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
				S7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
				S6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
				S5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
				S4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
HEX	S3	S2	S1	S0																
0	0	0	0	0	*	C4	C5	T	C6	T	T	62	C7	T	T	46	T	M	M	T
1	0	0	0	1	C0	T	T	14	T	M	M	T	T	M	M	T	M	T	T	30
2	0	0	1	0	C1	T	T	M	T	34	56	T	T	50	40	T	M	T	T	M
3	0	0	1	1	T	18	8	T	M	T	T	M	M	T	T	M	T	2	24	T
4	0	1	0	0	C2	T	T	15	T	35	57	T	T	51	41	T	M	T	T	31
5	0	1	0	1	T	19	9	T	M	T	T	63	M	T	T	47	T	3	25	T
6	0	1	1	0	T	20	10	T	M	T	T	M	M	T	T	M	T	4	26	T
7	0	1	1	1	M	T	T	M	T	36	58	T	T	52	42	T	M	T	T	M
8	1	0	0	0	C3	T	T	M	T	37	59	T	T	53	43	T	M	T	T	M
9	1	0	0	1	T	21	11	T	M	T	T	M	M	T	T	M	T	5	27	T
A	1	0	1	0	T	22	12	T	33	T	T	M	49	T	T	M	T	6	28	T
B	1	0	1	1	17	T	T	M	T	38	60	T	T	54	44	T	1	T	T	M
C	1	1	0	0	T	23	13	T	M	T	T	M	M	T	T	M	T	7	29	T
D	1	1	0	1	M	T	T	M	T	39	61	T	T	55	45	T	M	T	T	M
E	1	1	1	0	16	T	T	M	T	M	M	T	T	M	M	T	0	T	T	M
F	1	1	1	1	T	M	M	T	32	T	T	M	48	T	T	M	T	M	M	T

2617 tbl 07

NOTES:

1. The table indicates the decoding of the seven syndrome bits to identify the bit-in-error for a single-bit error, or whether a double or triple-bit error was detected. The all-zero case indicates no error detected.
   * = No errors detected
   # = The number of the single data bit-in-error
   T = Two errors detected
   M = Three or more detected
   C# = The number of the single checkbits in error

49C466 OPERATION

The EDC is concerned with two types of operation — memory reads and memory writes. In the 466 both these can be accomplished by utilizing either of two possible data paths — one incorporating the buffer and the other without the buffer. These operations are treated separately below.

Memory Write

The interference of the EDC in this type of operation is relatively minimal since it does not involve any error checking. The only overhead introduced by the EDC into the write cycle is that of generating the check bits associated with each 64-bit wide data word.

While a write operation is performed, it must be insured that the output buffer (enabled by $\overline{SOE}$ and BE_{0-7}) is disabled so that no attempt is made to simultaneously transfer read data onto the System Data (SD) Bus at the same time. This can be done by pulling $\overline{SOE}$ high.

When the write buffer is bypassed (WBSEL low), data passes through the SD Latch In. To latch data, the SDILE signal should be asserted. The special case of a partial word write or byte merge is discussed later. Hence, here it is assumed that all 64 bits are being written. Consequently, BE_{0-7} must all be low.

The data is fed to the SD Checkbit generator where appropriate checkbits are generated. Both system data and the generated checkbits can be latched before they are output by asserting the $\overline{SDOLE}$ signal. Asserting $\overline{MOE}$ enables the output buffer and data is output onto the Memory Data (MD) bus. CBSEL and $\overline{MOE}$ need to be asserted to enable the generated checkbit output buffer and output the checkbits onto $CBSYN_{0-7}$.

When the write buffer is incorporated into the write cycle, instead of asserting SDILE, $\overline{WBEN}$ is asserted and data is clocked into the write buffer on the rising edge of SCLK. The WBFF is asserted when the buffer is full and a write undertaken under this condition will fail. When $\overline{WBREN}$ is asserted, data can be clocked out of the write buffer on the rising edge of MCLK. Again, an attempt to read data from an empty write buffer (when empty, $\overline{WBEF}$ is asserted) will fail.

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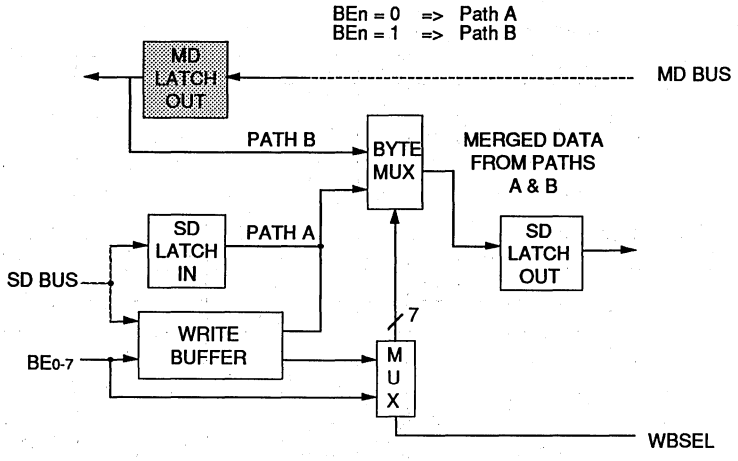

Figure 1. Byte Merge

2617 drw 05

Memory Read

During a memory read, data and the corresponding input checkbits are read from the MD bus and CBI$_{0-7}$, respectively. The memory data and CBI may both be latched as they come in (MD Latch In and MD Checkbit latch) by the MDILE signal. Memory data is sent to the MD checkbit generator (where checkbits corresponding to the input data are generated) and to the error correct circuitry. The generated checkbits are X-ORed with the input checkbits to produce the syndrome word. This is sent to the error correction circuitry which generates the corrected data (normal mode). The corrected data is output to the SD bus via either of two data paths. If the user chooses not to use the read buffer (RBSEL low), data flows through MD Latch Out. Asserting $\overline{\text{MDOLE}}$ latches this data. The output buffer is enabled by asserting $\overline{\text{SOE}}$ and BE$_{0-7}$. In order to also write this corrected data back to memory, the output buffer needs to be disabled by pulling $\overline{\text{SOE}}$ high, followed by the usual write procedure.

If the read buffer is selected (RBSEL high), data is clocked into the buffer (Read-Buffer Write) when $\overline{\text{RBEN}}$ is low, on the rising edge of MCLK. Data is clocked out of the buffer (Read_Buffer Read) when $\overline{\text{RBREN}}$ is low on the rising edge of SCLK. An appropriate skew between the buffer read and write clocks (MCLK and SCLK) is essential to avoid any flag contention on read/write boundaries (simultaneous read and write when buffer is either empty or full).

Partial Word Write/Byte Merge

Writing a word shorter than 64 bits to memory is treated as a special case. The checkbits generated for a data word shorter than 64 bits and written to a particular memory location differ from the checkbit word that would be generated by the entire 64-bit data word at the same location. Hence, the byte merge operation is required to carry out the following tasks: read the contents of the memory location to be written to, merge the byte/bytes being written (from SD side) with the other component bytes previously at that memory location (from MD side), generate a checkbit word for this composite word and write both the generated checkbits and the composite data word to memory. The BEn bits supplied by the user determine the bytes that come from SD and those that come from MD, as illustrated in Figure 1.

EDC Modes

The IDT49C466 has 5 modes of operation (very similar to those of the IDT49C465 32-bit Flow-Thru EDC) which are described in the Operating Mode section. The Error Data Output mode is useful for memory initialization. On issuing a clear, the Error Data register becomes an 'all-zero-data' source. All diagnostic registers can be cleared in this manner. In Checkbit Injection mode, the MD Checkbit Latch is loaded with data from the System Bus. This serves to verify the functioning of the EDC. Any discrepancy between the injected checkbits and generated checkbits should result in assertion of the $\overline{\text{ERR}}$ or $\overline{\text{MERR}}$ signals. These modes, and certain other features such as clear, buffer configuration, etc., can be controlled by appropriately loading the Mode Register. The Mode Register can be written to by asserting $\overline{\text{MEN}}$. Then SD$_{0-15}$ is clocked into the register on the rising edge of SCLK.

Diagnostics

The diagnostic ability of the 466 rests on a set of 6 registers that provide error logging information. They include the checkbit register, error count register, error type register, 2 syndrome registers and the error data register. Data is clocked into each of these registers on the rising edge of SYNCLK. The checkbit register, error count register, error type register and one of the syndrome registers are reloaded only in the case of an error. The other syndrome register and the error data register are reloaded on every new read cycle. The contents of the Error Data register can be read only in Error Data mode. The contents of the other diagnostic registers can be read in Diagnostic mode.

Parity

The 466 provides a parity check & generation facility. On a memory read the EDC generates parity bits for each data word and outputs the parity byte on the parity bus, P0-7. During a memory write, parity is checked by comparing the parity bits input on P0-7 and the parity bits generated from the input data word. A discrepancy between these two would cause the $\overline{PERR}$ pin to be asserted.

OPERATING MODE CHARTS

15 7	6	5	4	3	2 0
UNUSED	RMODE	PSEL	RWBD	CLEAR	EDCM0-2

EDCM2	EDCM1	EDCM0	OPERATION
0	0	0	ERRO-DATA OUTPUT MODE
0	0	1	DIAGNOSTIC-OUTPUT MODE
0	1	0	GENERATE-DETECT MODE
0	1	1	NORMAL MODE (DEFAULT)
1	X	X	CHECKBIT-INJECTION MODE

RMODE	OPERATION
0	NOP
1	READ MODE REGISTER ON SD BUS

RWBD	OPERATION
0	DUAL BUFFERS (8), DEFAULT
1	SINGLE BUFFER (16)

CLEAR	OPERATION
0	NORMAL
1	CLEAR ALL DIAG. REGISTERS

PSEL	OPERATION
0	EVEN
1	ODD

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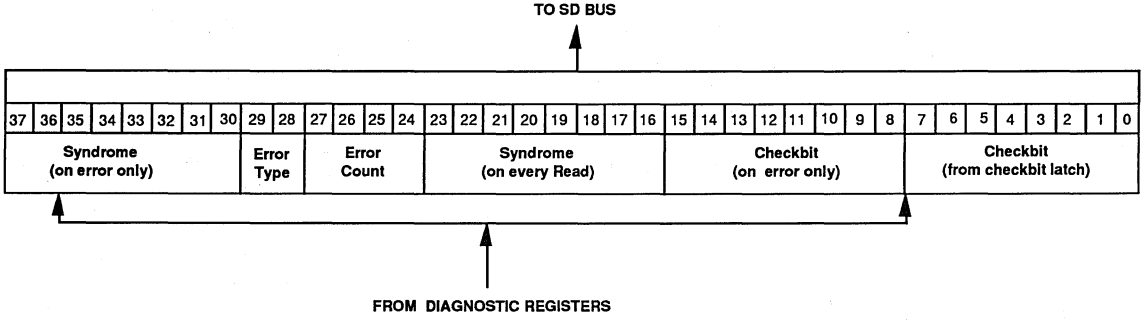
DIAGNOSTIC OUTPUT DATA FORMAT



2617 drw 07

OPERATING MODE DESCRIPTION

MODE	DESCRIPTION
MODE 0	**Error-Data Output Mode:** This mode allows the uncorrected data captured from an error event by the Error-Data Register to be read by the system for diagnostic purposes. The Error-Data Register is cleared by setting the mode register 'clear-bit'.
MODE 1	**Diagnostic-Output Mode:** In this mode, one external source and four internal registers are read by the system bus for diagnostic and error logging purpose. Internal data paths allow output from the CBI_{0-7} LATCH to be read directly by the system bus for diagnostic purpose. The contents of the internal diagnostic checkbit register, syndrome register, error count register and error-type register are also output on the SD bus.
MODE 2	**Generate-Detect Mode:** (Detect-Only) The EDC performs checkbit generation during a memory write, and performs error detection only during memory reads.
MODE 3	**Normal Mode:** The EDC performs checkbit generation during memory writes and error detection and correction during memory reads.
MODE 4	**Checkbit-Injection Mode:** In this mode, the checkbit latch is loaded with a desired 8-bit data from the SD bus when MDILE is strobed. By inserting various checkbit values, correct functioning of the EDC can be verified "on-board". The rest of the operation is similar to regular memory read. The EDC compares the injected checkbits against the internally generated checkbits. Any discrepancy in the injected checkbit and the internally generated checkbit will cause the $\overline{ERR}$ or $\overline{MERR}$ to go low.

2617 tbl 08

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Unit
V_{CC}	Power Supply Voltage	–0.5 to +7.0	V
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to VCC + 0.5	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	30	mA

NOTE: 2617 tbl 09

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Ratings for extended periods of time may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	PGA	5	pF
			PQFP	—	
C_{OUT}	Output Capacitance	V_{OUT} = 0V	PGA	7	pF
			PQFP	—	

NOTE: 2617 tbl 10

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

The following conditions apply unless otherwise specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%;

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input High Level[4]	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input Low Level[4]	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input High Current	V_{CC} = Max., V_{IN} = 2.7V		—	0.1	5.0	µA
I_{IL}	Input Low Current	V_{CC} = Max., V_{IN} = 0.5V		—	-0.1	–5.0	µA
I_{OZ}	Off State (Hi-Z)	V_{CC} = Max.	V_O = 0V	—	-0.1	–10	µA
	Output Current		V_O = V_{CC} (Max.)	—	0.1	10	
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_{OUT}= 0V		—	—	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –2mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8mA	—	0.3	0.5	V
V_H	Input Hysteresis on input control lines			—	200	—	mV

NOTES:
2617 tbl 11

1. For conditions shown as min. or max., use appropriate value specified above for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient temperature and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

A

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Con't)

The following conditions apply unless otherwise specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions[1]	Min.	Typ.[2]	Max.	Unit
I_{CCQC}	Quiescent Power Supply Current	V_{IN} = V_{CC}, or V_{IN} = GND V_{CC} = Max.	—	3.0	5	mA
I_{CCQT}	Quiescent Power Supply Current TTL Input Levels	V_{IN} = 3.4V V_{CC} = Max.	—	0.3	1	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{IN} = V_{CC}, or V_{IN} = GND V_{CC} = Max. f = 10MHz Correct Mode	—	—	—	mA

NOTES:
2617 tbl 12

1. For conditions shown as Min. or Max., use appropriate value specified above for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient temperature, and maximum loading.

AC PARAMETERS
PROPAGATION DELAY TIMES (PRELIMINARY)

Number	Parameter	Description		Max.	Unit	Refer to Timing Diagram Figure
		From Input	To Output			
GENERATE (WRITE) PARAMETERS						
Without Write Buffer:						
1	tBC	BEn	CBSYN (chkbit)	20	ns	
2	tBM	BEn	MDOUT	20	ns	
3	tPPE	Pxin	PERR	9	ns	
4	tSC	SDin	CBSYN (chkbit)	15	ns	
5	**tSM**	SDin	MDout	15	ns	
6	tSPE	SDin	$\overline{\text{PERR}}$	13	ns	
With Write Buffer:						
7	tMCb	MCLK (Lo-Hi)	CBSYN (chkbit)	25	ns	
8	tMMD	MCLK (Lo-Hi)	MDout	20	ns	
9	tWBSEL	WBSEL	MDout	17	ns	
DETECT (READ) PARAMETERS						
Without Read Buffer:						
10	tWYC	SYNCLK (Lo-Hi)	CBSYN (syndr)	15	ns	
11	**tME**	MDin	$\overline{\text{ERR}}$	15	ns	
12	tMME	MDin	$\overline{\text{MERR}}$	20	ns	
13	tCE	CBI	$\overline{\text{ERR}}$	15	ns	
14	tCME	CBI	$\overline{\text{MERR}}$	20	ns	
With Read Buffer:						
15	tSSD	SCLK (Lo-Hi)	SDout	22	ns	
16	tRBSEL	RBSEL	SDout	10	ns	
CORRECT (READ) PARAMETERS						
Without Read Buffer:						
17	tCS	CBI	SDout	20	ns	
18	tMP	MDin	Pxout	24	ns	
19	**tMS**	MDin	SDout	23	ns	
With Read Buffer:						
20	tSPb	SCLK (Lo-Hi)	Pxout	25	ns	

NOTES:
1. Bold indicates critical system parameters.
2. (Lo-Hi) indicates Low-to-High transition and vice versa.

2617 tbl 13

PROPAGATION DELAY TIMES FROM LATCH ENABLES (PRELIMINARY)

Number	Parameter	Description		Max.	Unit	Refer to Timing Diagram Figure
		From Input	To Output			
21	tMLE	MDILE (Lo-Hi)	$\overline{ERR}$	18	ns	
22	tMLME	MDILE (Lo-Hi)	$\overline{MERR}$	21	ns	
23	tMLP	MDILE (Lo-Hi)	Px	25	ns	
24	tMLS	MDILE (Lo-Hi)	SDout	22	ns	
25	tMOLS	$\overline{MDOLE}$ (Hi-Lo)	SDout	15	ns	
26	tMOLP	$\overline{MDOLE}$ (Hi-Lo)	Px	18	ns	
27	tSLC	SDILE (Lo-Hi)	CBSYN (chkbit)	20	ns	
28	tSLM	SDILE (Lo-Hi)	MDout	16	ns	
29	tSOLC	$\overline{SDOLE}$ (Hi-Lo)	CBSYN (chkbit)	12	ns	
30	tSOLM	$\overline{SDOLE}$ (Hi-Lo)	MDout	12	ns	

NOTE:
1. (Lo-Hi) indicates Low-to-High transition and vice versa.

2617 tbl 14

R/W BUFFER TIMES (PRELIMINARY)

Number	Parameter	Description		Min.	Max.	Unit	Refer to Timing Diagram Figure
		From Input	To Output				
31	tRSF	RS1 (Hi-Lo)	$\overline{EF}$ (Hi-Lo)/$\overline{FF}$ (Lo-Hi)	—	15	ns	7
32	tSKEW1	RCLK (Lo-Hi) (SCLK or MCLK)	WCLK (Lo-Hi) (SCLK or MCLK)	20	—	ns	3, 5
33	tSKEW2	WCLK (Lo-Hi) (SCLK or MCLK)	RCLK (Lo-Hi) (SCLK or MCLK)	20	—	ns	4, 6
34	tEF	R/WCLK (Lo-Hi) (SCLK or MCLK)	$\overline{EF}$	—	16	ns	4, 6
35	tFF	R/WCLK (Lo-Hi) (SCLK or MCLK)	$\overline{FF}$	—	16	ns	3, 5

NOTE:
1. (Lo-Hi) indicates Low-to-High transition and vice versa.

2617 tbl 15

A

BYTE MERGE TIMES (PRELIMINARY)

Number	Parameter	Description		Max.	Unit	Refer to Timing Diagram Figure
		From	To			
36	tSCM	SCLK (Lo-Hi)	MDout	22	ns	
37	tMDM	$\overline{\text{MDOLE}}$ (Hi-Lo)	MDout	18	ns	
38	tRBM	RBSEL	MDout	18	ns	
39	tSDM	SDILE (Lo-Hi))	MDout	16	ns	
40	tSOE	MDin	SOE (Hi-Lo)	TBD	ns	

NOTES:
1. (Lo-Hi) indicates Low-to-High transition and vice versa.

2617 tbl 16

ENABLE AND DISABLE TIMES (PRELIMINARY)

Number	Parameter	Description				Min.	Max.	Unit	Refer to Timing Diagram Figure
		From Input		To Output					
41	tBESZx	BEN =	High	SDout	*	—	15	ns	6
42	tBESxZ		Low		Hi-Z	—	15		
43	tBEPZx	BEN =	High	Pout	*	—	15	ns	6
44	tBEPxZ		Low		Hi-Z	—	15		
45	tCECZx	$\overline{\text{MOE}}$ =	Low	CBSYN	*	—	15	ns	4
46	tCECxZ		High		Hi-Z	—	15		
47	tMEMZx	$\overline{\text{MOE}}$ =	Low	MDout	*	—	18	ns	4, 9
48	tMEMxZ		High		Hi-Z	—	18		
49	tSESZx	$\overline{\text{SOE}}$ =	Low	SDout	*	—	15	ns	6
50	tSESxZ		High		Hi-Z	—	15		

NOTES:
1. (Z) indicates high impedence.
2. (Lo-Hi) indicates Low-to-High transition and vice versa.
3. * indicates delay to both edges.

2617 tbl 17

SET-UP AND HOLD TIMES (PRELIMINARY)

Number	Parameter	Description			Min.	Unit	Refer to Timing Diagram Figure
		From Input	To Input	(edge)			
51	tCMLS	CBI Set-up	before MDILE =	Hi-Lo	2	ns	5
52	tCMLH	CBI Hold	after MDILE =	Hi-Lo	6	ns	5
53	tMMLS	MDIN Set-up	before MDILE =	Hi-Lo	2	ns	5
54	tMMLH	MDIN Hold	after MDILE =	Hi-Lo	6	ns	5
55	tCMOLS	CBI Set-up	before $\overline{\text{MDOLE}}$ =	Lo-Hi	10	ns	
56	tCMOLH	CBI Hold	after $\overline{\text{MDOLE}}$ =	Lo-Hi	2	ns	
57	tMMOLS	MDIN Set-up	before $\overline{\text{MDOLE}}$ =	Lo-Hi	10	ns	
58	tMMOLH	MDIN Hold	after $\overline{\text{MDOLE}}$ =	Lo-Hi	2	ns	
59	tMMCS	MDIN Set-up	before MCLK =	Lo-Hi	6	ns	
60	tMMCH	MDIN Hold	after MCLK =	Lo-Hi	6	ns	
61	tSSLS	SDIN Set-up	before SDILE =	Hi-Lo	4	ns	
62	tSSLH	SDIN Hold	after SDILE =	Hi-Lo	4	ns	
63	tSSCS	SDIN Set-up	before SCLK	Lo-Hi	4	ns	
64	tSSCH	SDIN Hold	after SCLK	Lo-Hi	4	ns	
65	tSDOLE	MCLK (Lo-Hi)	before $\overline{\text{SDOLE}}$ =	Lo-Hi	8	ns	
66	tENS	R/W Buffer Enable Set-up	before S/M CLK =	Lo-Hi	4	ns	3, 4, 5, 6
67	tENH	R/W Buffer Enable Hold	after S/M CLK =	Lo-Hi	4	ns	3, 4, 5, 6
68	tDS	R/W Buffer Data In Set-up	before S/M CLK =	Lo-Hi	2	ns	3
69	tDH	R/W Buffer Data In Hold	after S/M CLK =	Lo-Hi	6	ns	3
70	tRSS	RS1 (Hi-Lo)	R/WBEN =	Hi-Lo	12	ns	7
71	tMODS	Mode Data Set-up	before SCLK =	Lo-Hi	5	ns	8
72	tMODH	Mode Data Hold	after SCLK =	Lo-Hi	1	ns	8
73	tMENS	Mode Enable Set-up	before SCLK =	Lo-Hi	2	ns	8
74	tMENH	Mode Enable Hold	after SCLK =	Lo-Hi	6	ns	8
DIAGNOSTIC SET-UP AND HOLD TIMES							
75	tCSCS	CBI Set-up	before SYNCLK =	High	25	ns	
76	tMSCS	MDIN Set-up			25	ns	
77	tMLSCS	MDILE Set-up = High			25	ns	

NOTES:
1. (Lo-Hi) indicates L0w-to-=High transition and vice sersa.

2617 tbl 18

MINIMUM PULSE WIDTH (PRELIMINARY)

Number	Parameter	Description			Min.	Unit	Refer to Timing Diagram Figure
		From Input		Condition			
78	tRS	Min. RS1 low time	to reset buffers	—	6	ns	
79	tMLE	Min. MDILE high time	to strobe new data	MD, CBI = Valid	6	ns	
80	tMDOLE	Min. $\overline{\text{MDOLE}}$ low time	to strobe new data	SD = Valid	6	ns	
81	tSLE	Min. SDILE high time	to strobe new data	SD = Valid	6	ns	
82	tCLK	Min. S/MCLK high time	to clock in new data	EN signal low	6	ns	
83	tSYNCLK	Min. SYNCLK high time	to clock in new data	—	6	ns	

2617 tbl 19

A

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Out Load	See Figure 13

2617 tbl 21

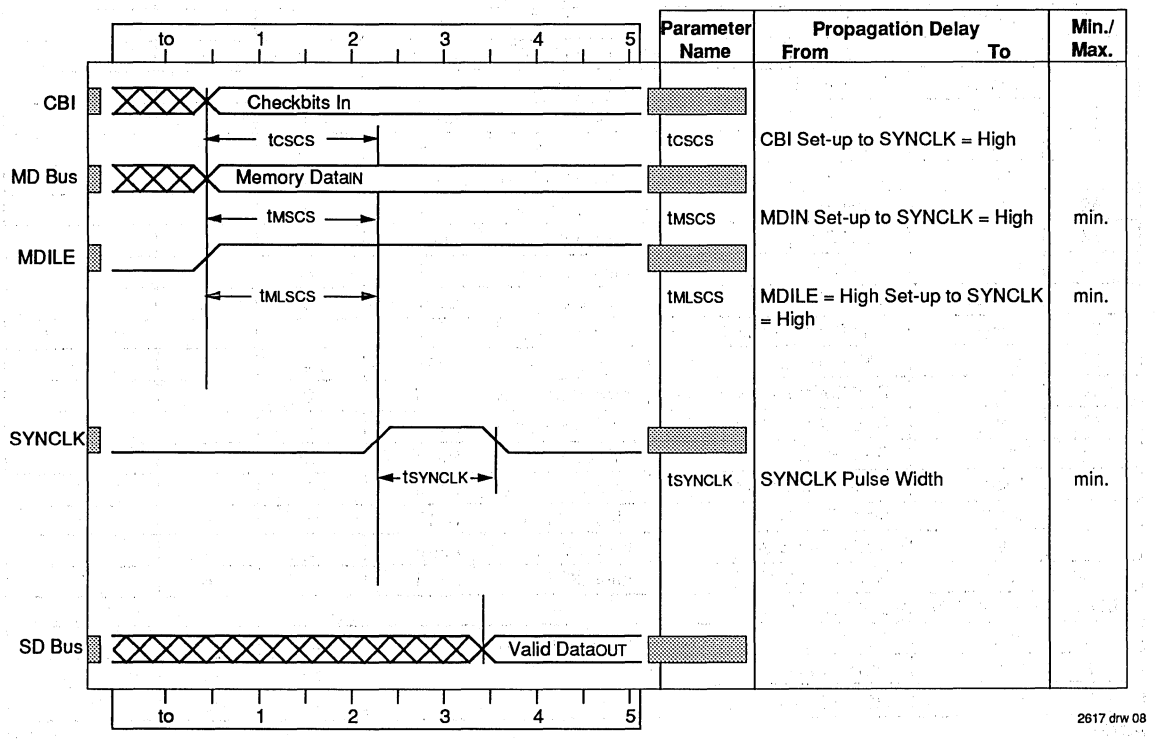


Figure 2. Diagnostic Timing

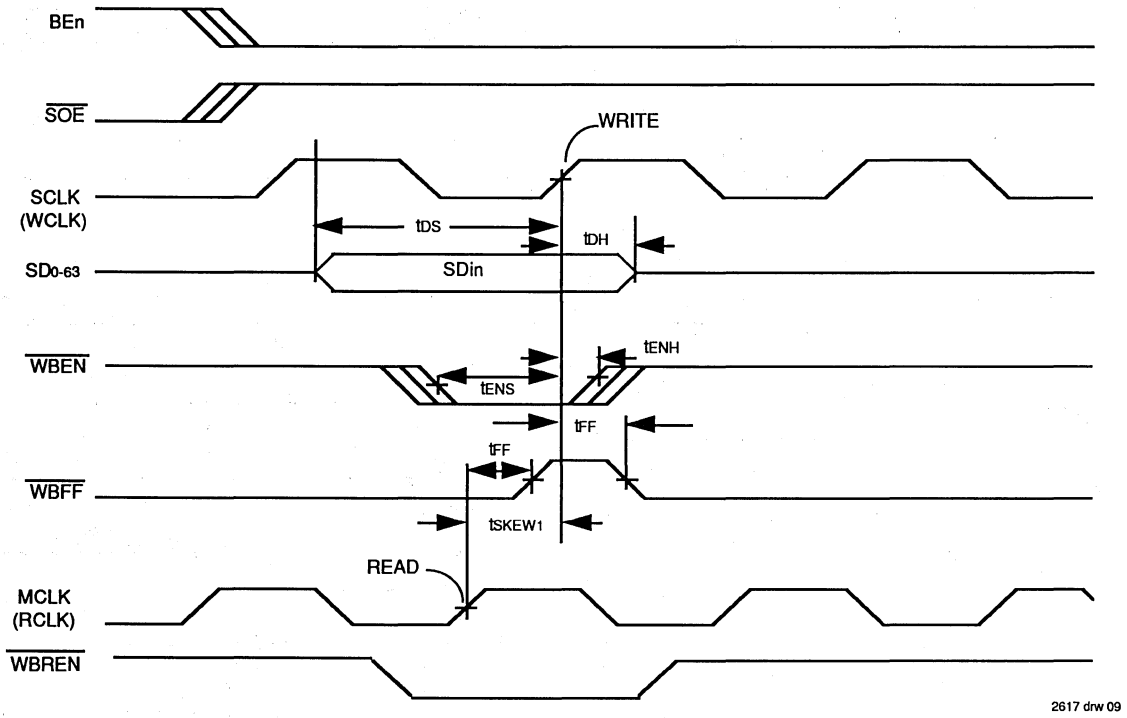


Figure 3. Write Buffer Write Timing (Write Cycle)

A

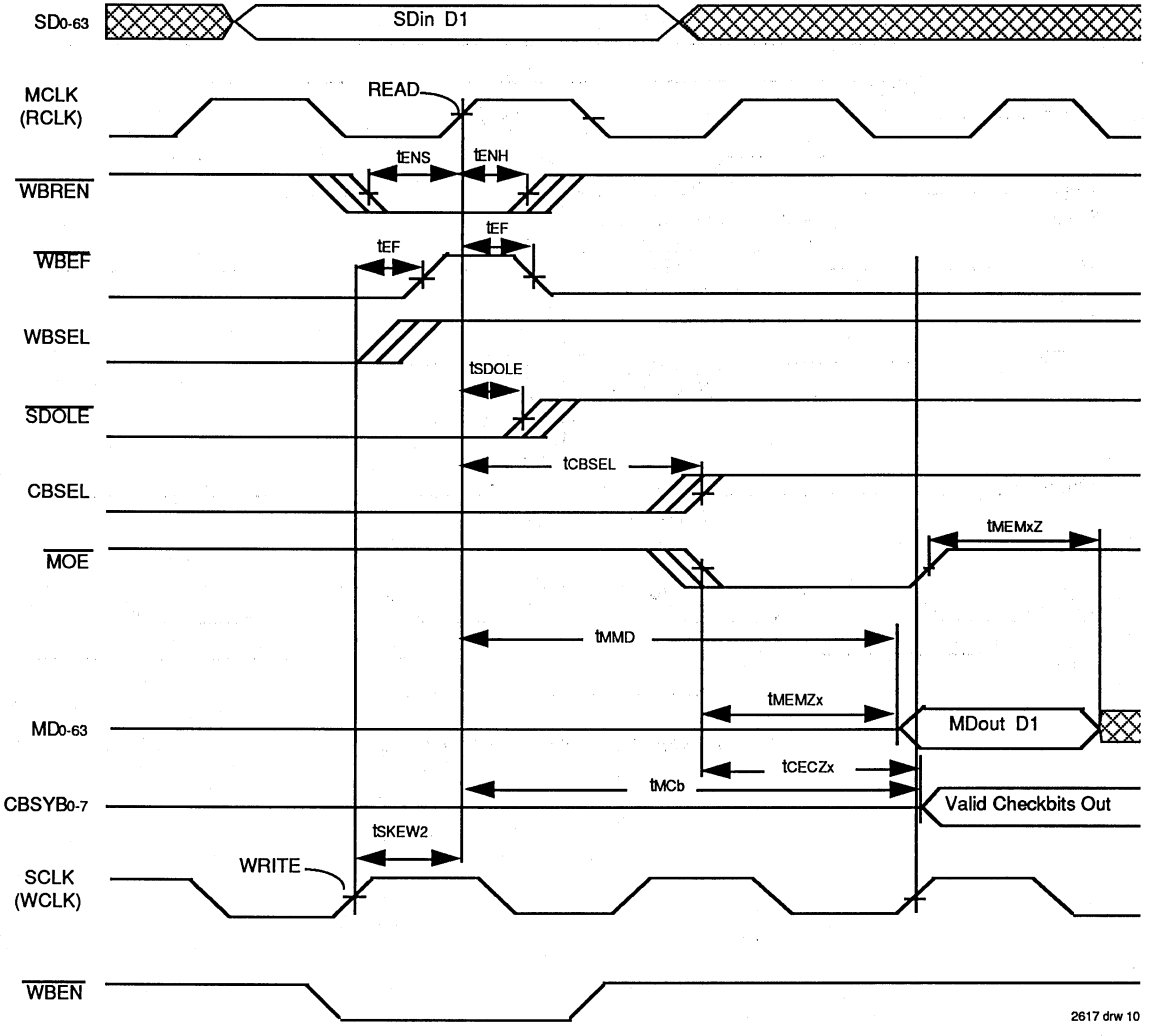


Figure 4. Write Buffer Read and Checkbit Generate Timing (Write Cycle)

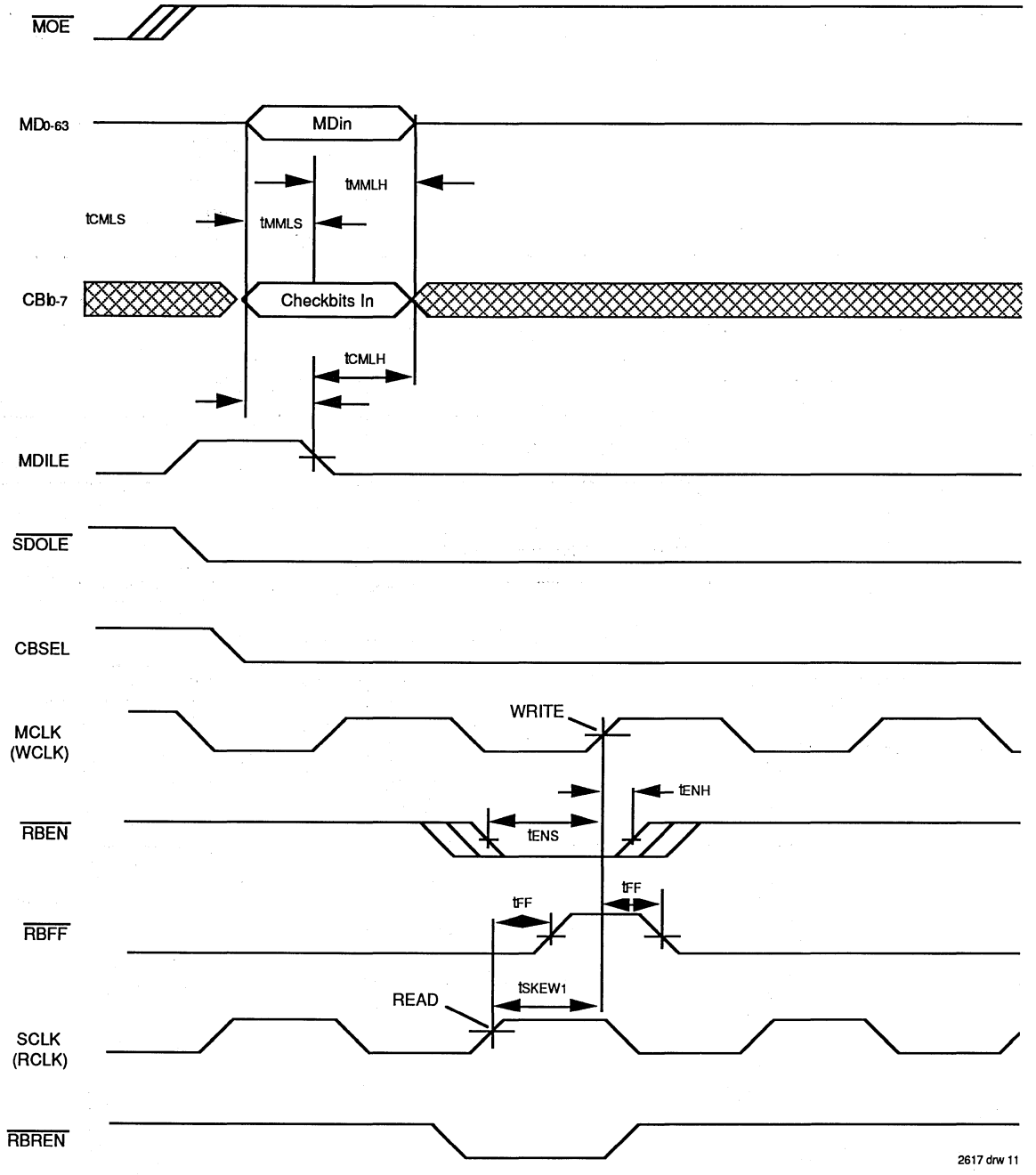


Figure 5. Read Buffer Write and Syndrome Generate Timing (Read Cycle)

A

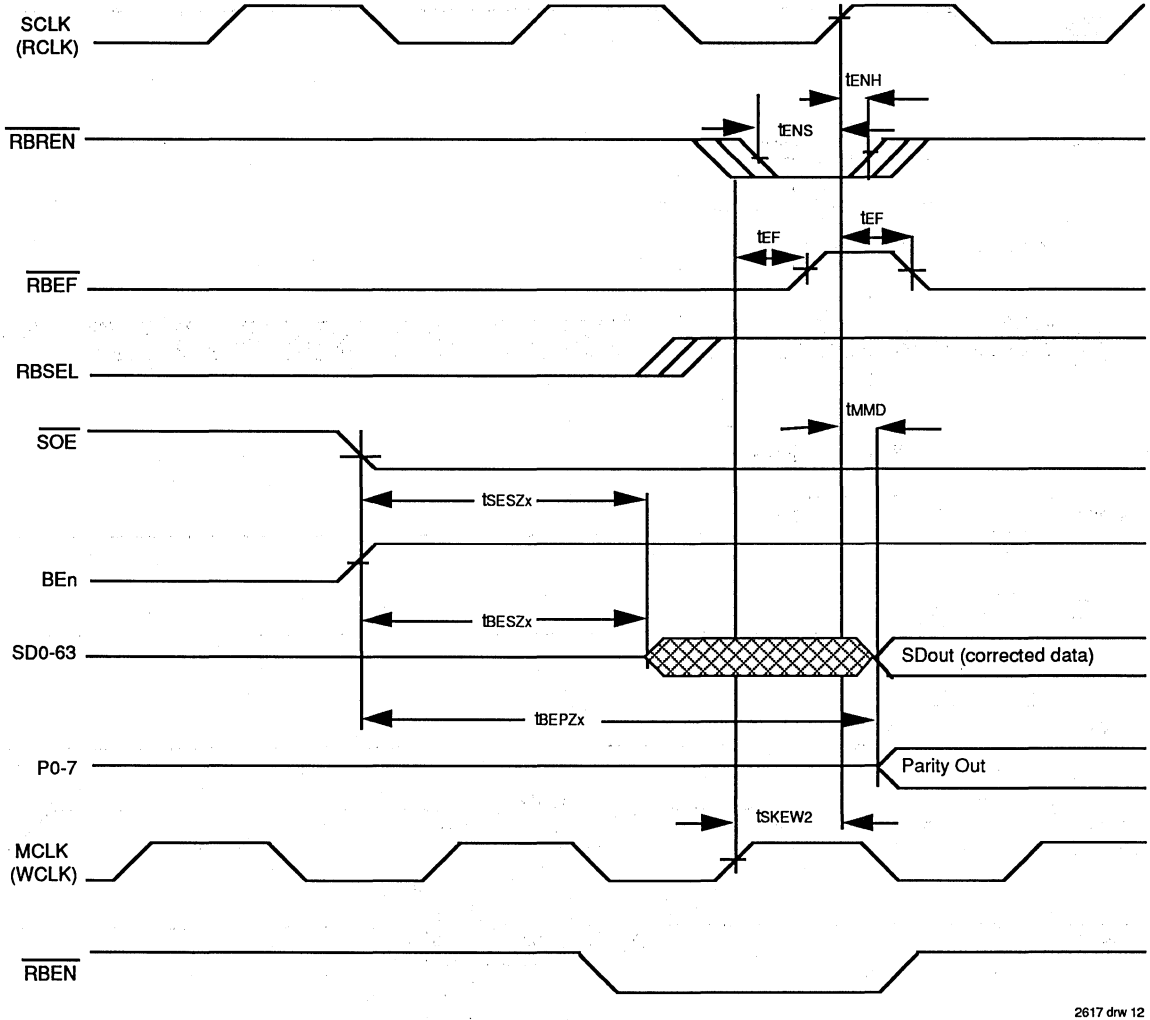
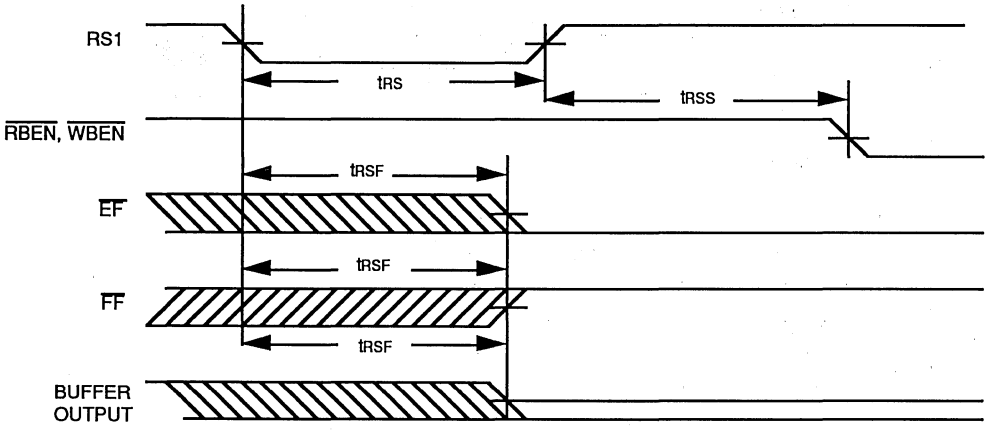


Figure 6. Read Buffer Read Timing (Read Cycle)

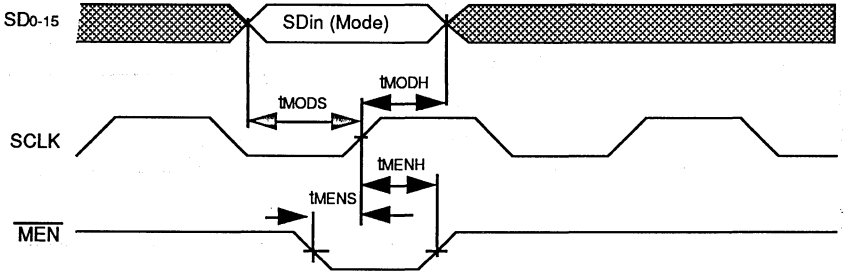


2617 drw 13

NOTES:
1. The clocks SCLK and MCLK can be free-running during reset.

Figure 7. Buffer Reset Timing

A



2617 drw 14

Figure 8. Mode Enable Timing

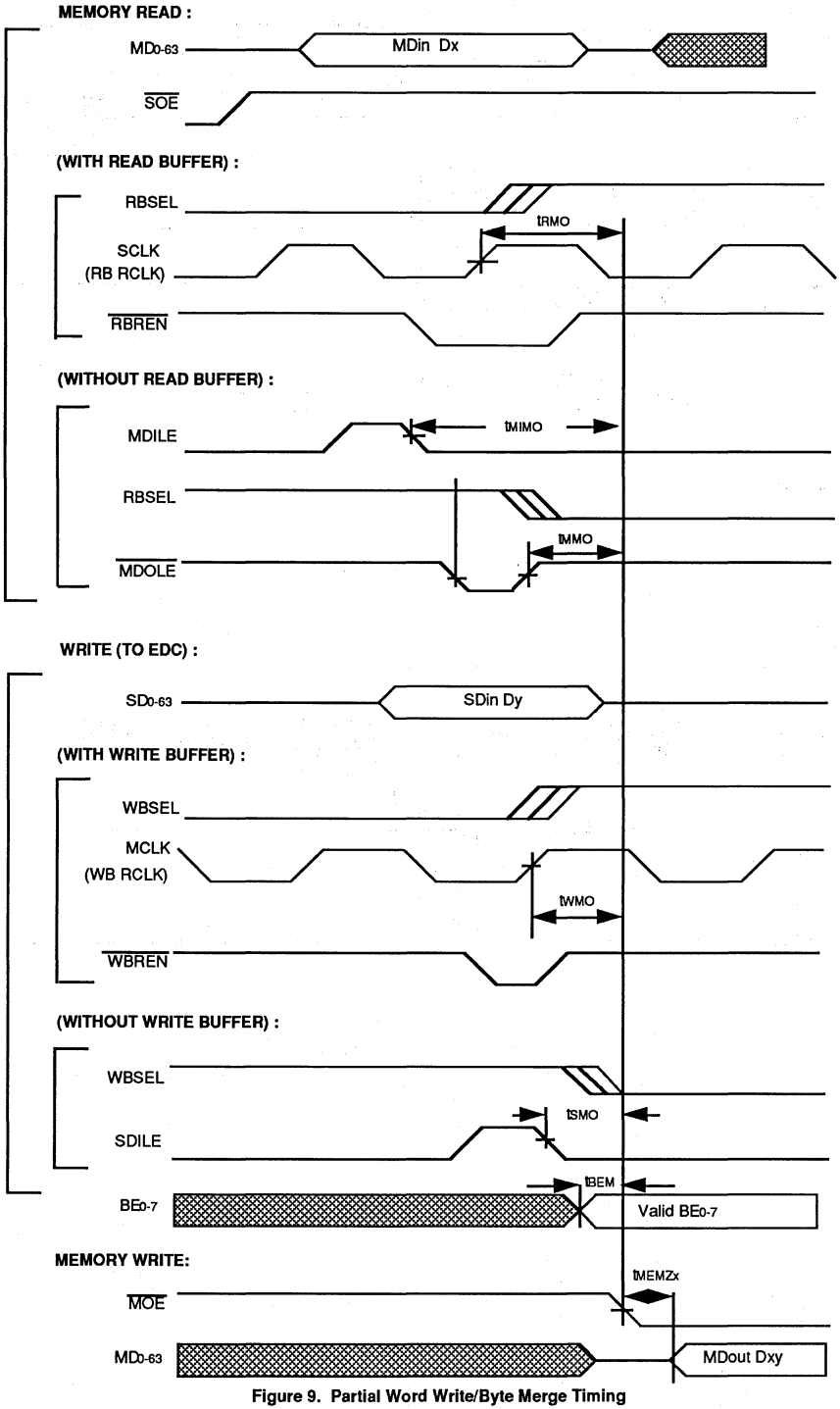


Figure 9. Partial Word Write/Byte Merge Timing

2617 drw 15

INPUT/OUTPUT INTERFACE CIRCUITS

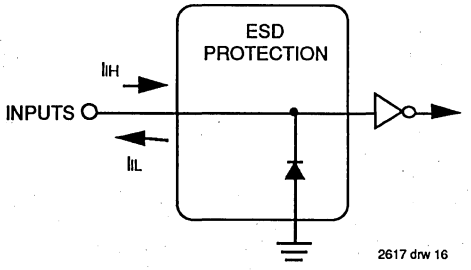


Figure 10. Input Structure (All Inputs)

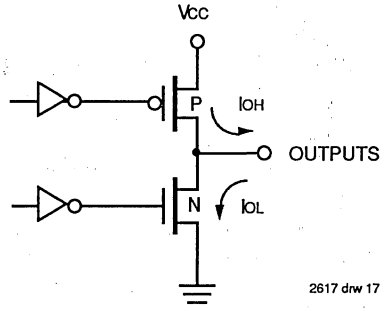
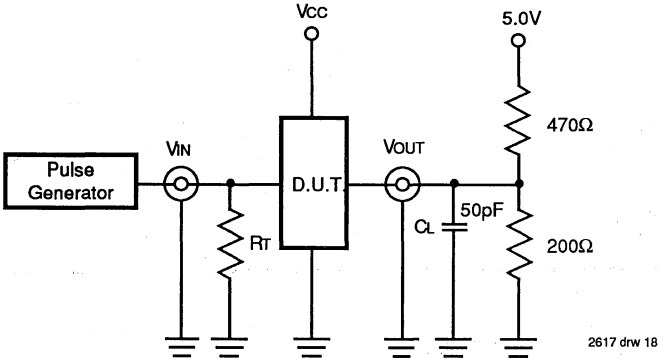


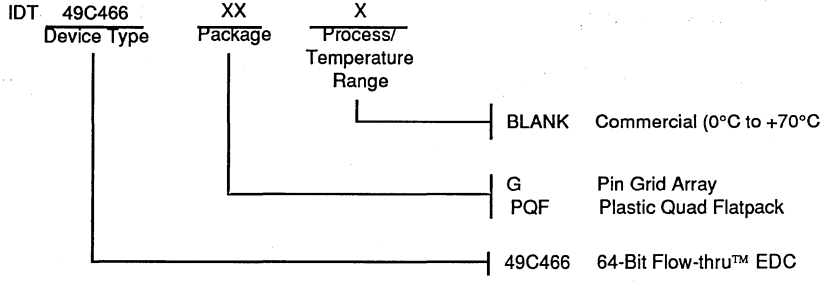
Figure 11. Output Structure



DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

Figure 12. AC Test Circuit

ORDERING INFORMATION



Integrated Device Technology, Inc.

FAST CMOS BUFFER/CLOCK DRIVER

IDT49FCT805/A
IDT49FCT806/A

FEATURES:

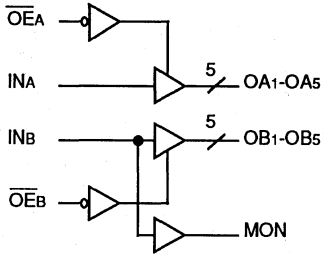
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Two independent groups of buffers with 3-state control
- 5:1 fanout (1 in - 5 out) per group
- True and inverting options
- 'Heartbeat' monitor output
- Guaranteed low skew
- Pinout designed for minimum skew and ground bounce
- Clock busing with 3-state control
- 20 pin DIP, SOIC, CERPACK and LCC
- Meets or exceeds JEDEC Standard 18 specifications
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT49FCT805/A and IDT49FCT806/A are clock drivers built using advanced CEMOS™, a dual metal CMOS technology. The IDT49FCT805A is a non-inverting clock driver and the IDT49FCT806A is an inverting clock driver. Each clock driver consists of two banks of drivers. Each bank drives five output buffers from a standard TTL compatible CMOS input.

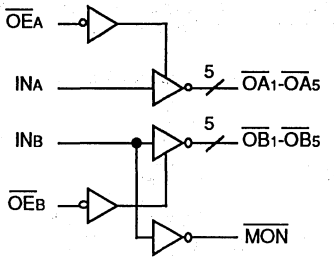
FUNCTIONAL BLOCK DIAGRAMS

IDT49FCT805



2574 drw 03

IDT49FCT806



2574 drw 06

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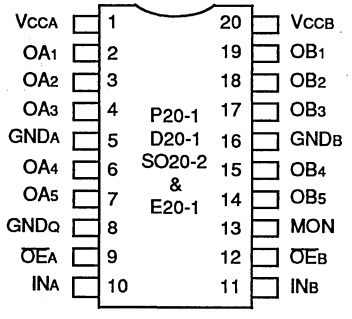
FAST is a trademark of National Semiconductor Co.

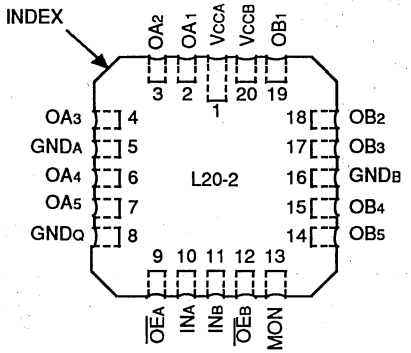
PIN CONFIGURATIONS

IDT49FCT805



DIP/SOIC/CERPACK
TOP VIEW

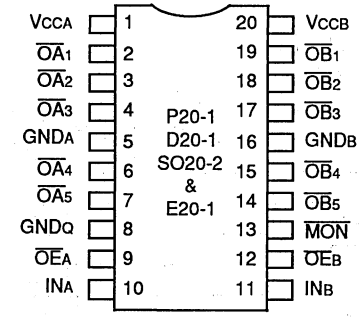
2574 drw 01



LCC
TOP VIEW

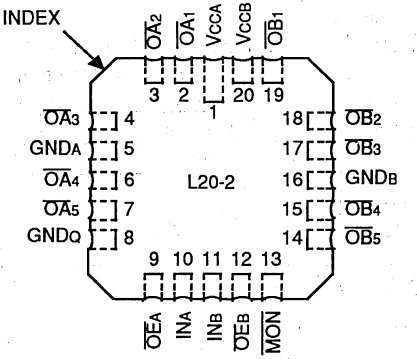
2574 drw 02

IDT49FCT806



DIP/SOIC/CERPACK
TOP VIEW

2574 drw 04



LCC
TOP VIEW

2574 drw 05

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
IN_A, IN_B	Clock Inputs
O_An, O_Bn	Clock Outputs
MON	Monitor Output

2574 tbl 05

FUNCTION TABLE[1]

Inputs		Outputs			
		49FCT805		49FCT806	
$\overline{OE}_A$, $\overline{OE}_B$	IN_A, IN_B	O_An, O_Bn	MON	$\overline{O_An}$, $\overline{O_Bn}$	$\overline{MON}$
L	L	L	L	H	H
L	H	H	H	L	L
H	L	Z	L	Z	H
H	H	Z	H	Z	L

NOTE:
1. H = HIGH, L = LOW, Z = High Impedance

2574 tbl 06

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE: 2574tbl01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals.
3. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2574 tbl 02

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = Vcc – 0.2V
Commercial: TA = 0°C to +70°C; VCC = 5.0V ± 5%, Military: TA = –55°C to +125°C; VCC = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IIH}	Input HIGH Current	Vcc = Max.	V_I = Vcc	—	—	5	µA
I_{IL}	Input LOW Current	Vcc = Max.	V_I = GND	—	—	–5	µA
I_{OZH}	Off State (HIGH Z)	Vcc = Max.	V_O = Vcc	—	—	10	µA
I_{OZL}	Output Current		V_O = GND	—	—	–10	µA
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_{IN}= –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	Vcc = Max.(3), V_O = GND		–60	–120	–250	mA
V_{OH}	Output HIGH Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	Vcc	—	V
		Vcc = Min.	I_{OH} = –300µA	V_{HC}(4)	Vcc	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	3.6	4.3	—	
			I_{OH} = -24mA MIL. I_{OH} = -24mA COM'L.	2.4	3.8	—	
V_{OL}	Output LOW Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL}= 300µA		—	GND	V_{LC}	V
		Vcc = Min.	I_{OL}= 300µA	—	GND	V_{LC}(4)	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.3	0.55	
V_H	Input Hysteresis for all inputs	—		—	200	—	mV

NOTES: 2574 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	1.0	2.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND Per Output Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND Mon. Output Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	5.3	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND Eleven Outputs Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	4.3	8.4[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.3	10.9[5]	

2574 tbl 04

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_O)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_O = Number of Outputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

A

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

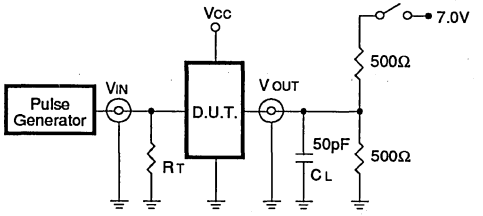
Symbol	Parameter	Condition[1]	IDT49FCT805/806				IDT49FCT805A/806A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay IN_A to OA_n, IN_B to OB_n	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	7.5	1.5	5.8	1.5	6.8	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}_A$ to OA_n, $\overline{OE}_B$ to OB_n		1.5	8.0	1.5	8.5	1.5	8.0	1.5	8.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{OE}_A$ to OA_n, $\overline{OE}_B$ to OB_n		1.5	7.0	1.5	7.5	1.5	7.0	1.5	7.5	ns
$t_{SK(o)}$[3]	Skew between two outputs of same package (same transition)		—	0.7	—	0.9	—	0.7	—	0.9	ns
$t_{SK(p)}$[3]	Skew between opposite transitions (t_{PHL}-t_{PLH}) of same output		—	1.0	—	1.1	—	1.0	—	1.1	ns
$t_{SK(t)}$[3]	Skew between two outputs of different package at same power supply voltage and temperature (same transition)		—	1.5	—	1.5	—	1.5	—	1.5	ns

2574 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew guaranteed across temperature range but measured at maximum temperature only. Skew parameters apply to propagation delays only.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



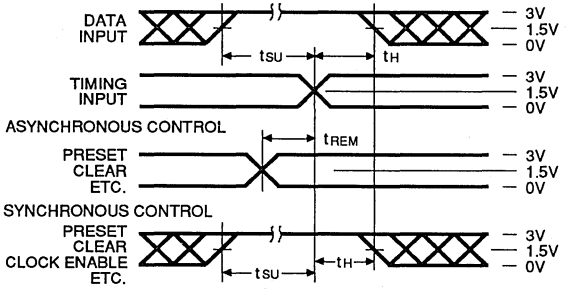
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

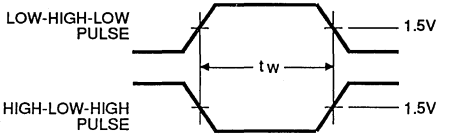
DEFINITIONS: 2574 tbl 09

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

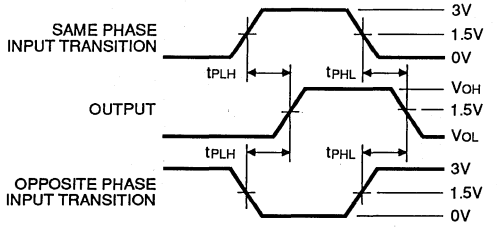
SET-UP, HOLD AND RELEASE TIMES



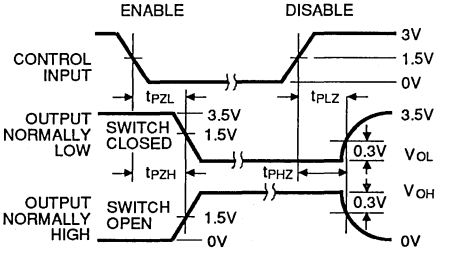
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

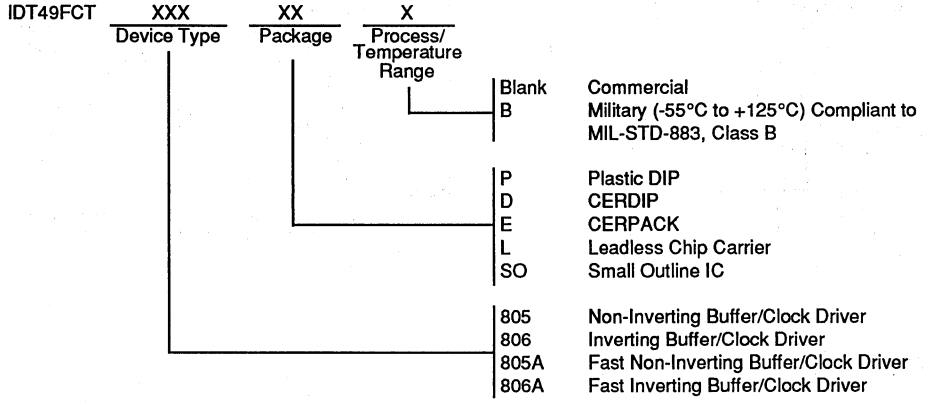


NOTES 2574 drw 05

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; $Z_O \leq 50\Omega$; $t_F \leq 2.5$ns; $t_R \leq 2.5$ns.

A

ORDERING INFORMATION



Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS MEMORY DRIVERS

ADVANCE INFORMATION
IDT54/74FBT2240
IDT54/74FBT2240A

FEATURES:

- IDT54/74FBT2240 equivalent to the 54/74BCT2240
- **IDT54/74FBT2240A 25% faster than the 2240**
- 25Ω output resistors reduce overshoot and undershoot when driving MOS RAMs
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Higher static VOH for improved noise immunity and reduced system power dissipation
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

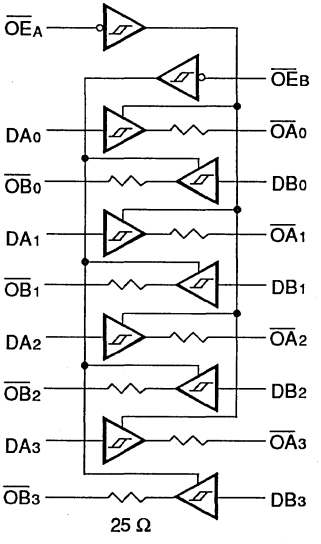
DESCRIPTION:

The FBT series of BiCMOS Memory Drivers is built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT2240 series are octal buffers/line drivers where each output is terminated with a 25Ω series resistor.

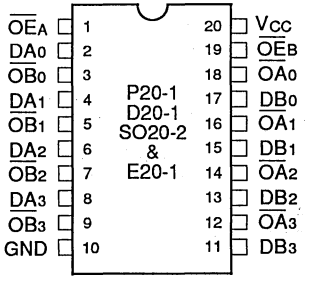
The FBT series of bus interface devices are ideal for use in designs needing to drive large capacitive loads with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection. The output buffers are designed to guarantee a static VOH of 2.7V. This higher output level in the high state results in a significant reduction in overall system power dissipation and improved noise immunity when driving DRAMS and SRAMS.

FUNCTIONAL BLOCK DIAGRAM

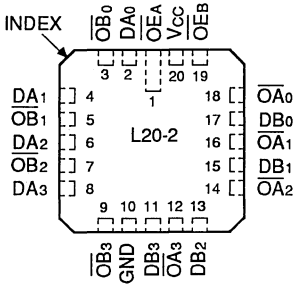


2642 drw 01

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

2642 drw 02

BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
Dxx	Inputs
$\overline{O}$xx	Outputs

2642 tbl 01

FUNCTION TABLE[1]

Inputs		Output
$\overline{OE}_A$, $\overline{OE}_B$	Dxx	Oxx
L	L	H
L	H	L
H	X	Z

NOTE: 2642 tbl 02

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE: 2642 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Type	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2642 tbl 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V		—	—	-10	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	-50	
I_I	Input HIGH Current	V_{CC} = Max., V_{CC} (Max.)		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{ODH}	Output Drive Current	V_{CC} = Min., V_O = 2.25V		-35	—	—	mA
I_{ODL}	Output Drive Current	V_{CC} = Min., V_O = 2.25V		50	—	—	mA
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		-75	—	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = -1mA	2.7	3.8	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = - 8mA	2.4	3.3	—	
			I_{OH} = -12mA	2.0	3.2	—	
V_{OL}	Output LOW Voltage		I_{OL} = 1mA	—	0.1	0.5	V
			I_{OL} = 12mA	—	0.35	0.8	
V_H	Input Hysteresis	V_{CC} = 5V		—	200	—	mV
I_{CCH} I_{CCZ} I_{CCL}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2642 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE_A}$ = $\overline{OE_B}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.3	0.40	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.2	5.5	mA
		$\overline{OE_A}$ = $\overline{OE_B}$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	3.5	6.5	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	6.2	9.5[5]	
		$\overline{OE_A}$ = $\overline{OE_B}$ = GND Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	8.2	17.5[5]	

NOTES:

2642 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL HIgh Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			IDT54/74FBT2240				IDT54/74FBT2240A				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Dxx to $\overline{O}$xx	C_L = 50pF R_L = 500Ω	1.5	5.7	1.5	6.3	1.5	4.8	1.5	5.1	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	8.0	1.5	8.5	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.0	1.5	7.5	1.5	5.6	1.5	5.9	ns

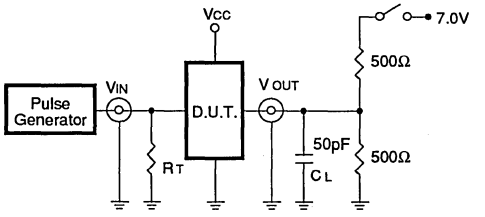
NOTES:

2642 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

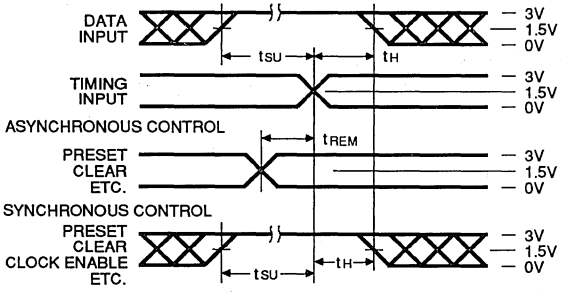
2642 tbl 08

DEFINITIONS:

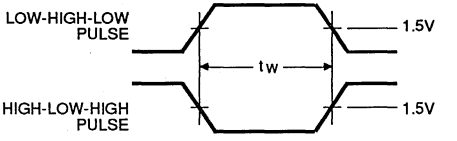
C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

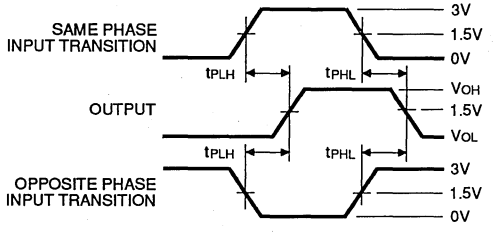
SET-UP, HOLD AND RELEASE TIMES



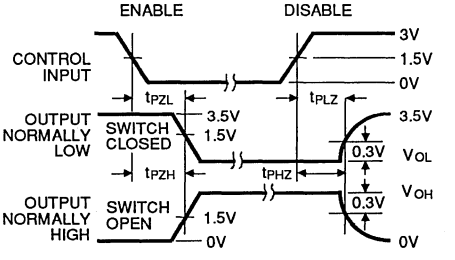
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



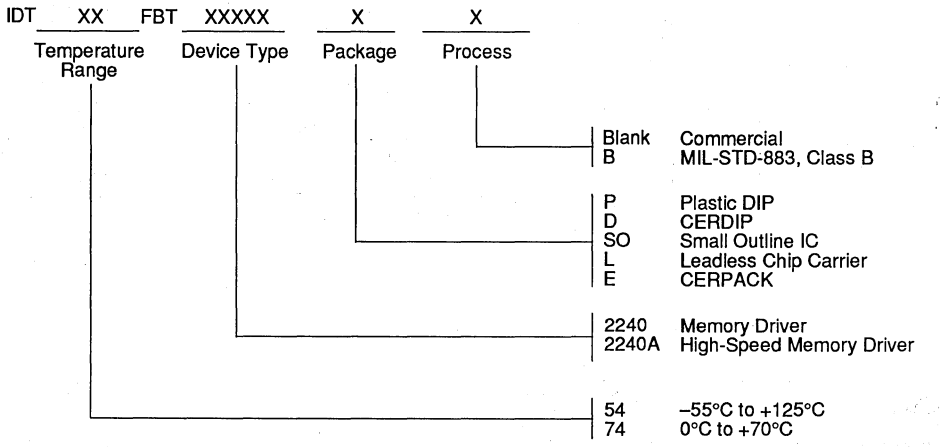
2642 drw 05

NOTES

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

A

ORDERING INFORMATION



Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS MEMORY DRIVERS

PRELIMINARY
IDT54/74FBT2244
IDT54/74FBT2244A

FEATURES:

- IDT54/74FBT2244 equivalent to the 54/74BCT2244
- **IDT54/74FBT2244A 25% faster than the 2244**
- 25Ω output resistors reduce overshoot and undershoot when driving MOS RAMs
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Higher static VOH for improved noise immunity and reduced system power dissipation.
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

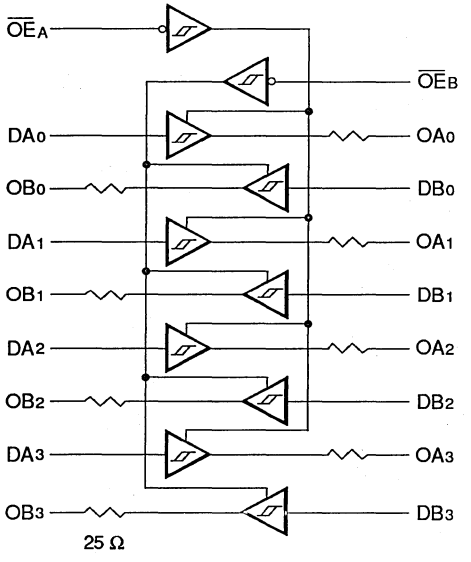
DESCRIPTION:

The FBT series of BiCMOS Memory Drivers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT2244 series are octal buffers/line drivers where each output is terminated with a 25Ω series resistor.

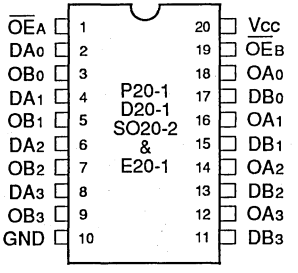
The FBT series of bus interface devices are ideal for use in designs needing to drive large capacitive loads with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection. The output buffers are designed to guarantee a static VOH of 2.7V. This higher output level in the high state results in a significant reduction in overall system power dissipation and in improved noise immunity when driving DRAMS and SRAMS.

FUNCTIONAL BLOCK DIAGRAM

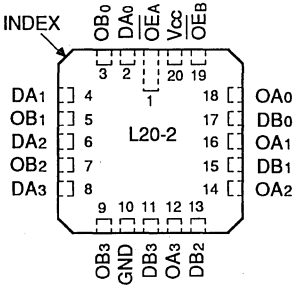


2641 drw 01

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



2641 drw 02

LCC
TOP VIEW

BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Inputs
Dxx	Inputs
Oxx	Outputs

2641 tbl 01

FUNCTION TABLE[1]

Inputs		Outputs
$\overline{OE}_A$, $\overline{OE}_B$	Dxx	Oxx
L	L	L
L	H	H
H	X	Z

NOTE: 2641 tbl 02

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	-0.5 to Vcc	-0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2641 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Type	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2641 tbl 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V		—	—	-10	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	-50	
I_I	Input HIGH Current	V_{CC} = Max., V_{CC} (Max.)		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{ODH}	Output Drive Current	V_{CC} = Min., V_O = 2.25V		-35	—	—	mA
I_{ODL}	Output Drive Current	V_{CC} = Min., V_O = 2.25V		50	—	—	mA
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		-75	—	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = -1mA	2.7	3.8	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = - 8mA	2.4	3.3	—	
			I_{OH} = -12mA	2.0	3.2	—	
V_{OL}	Output LOW Voltage		I_{OL} = 1mA	—	0.1	0.5	V
			I_{OL} = 12mA	—	0.35	0.8	
V_H	Input Hysteresis	V_{CC} = 5V		—	200	—	mV
I_{CCH} I_{CCZ} I_{CCL}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2641 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.3	0.40	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.2	5.5	mA
		$\overline{OE}_A$ = $\overline{OE}_B$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	3.5	6.5	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	6.2	9.5[5]	
		$\overline{OE}_A$ = $\overline{OE}_B$ = GND Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	8.2	17.5[5]	

NOTES:

2641 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			IDT54/74FBT2244				IDT54/74FBT2244A				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Dxx to Oxx	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	7.0	1.5	4.8	1.5	5.1	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	8.0	1.5	8.5	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.0	1.5	7.5	1.5	5.6	1.5	5.9	ns

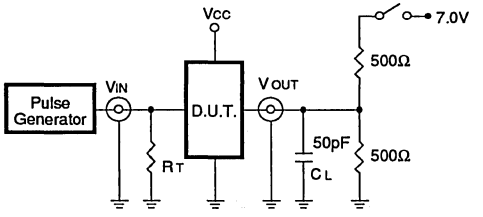
NOTES:

2641 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



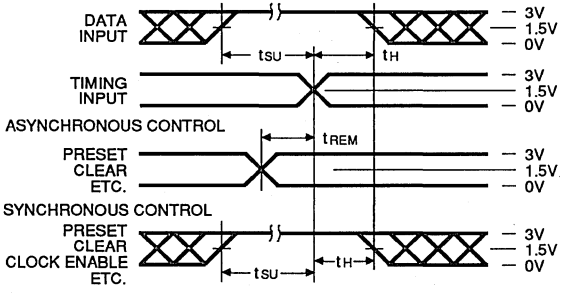
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

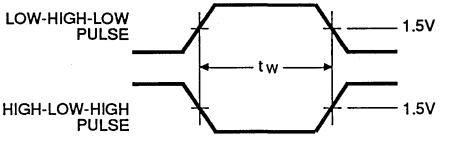
DEFINITIONS: 2641 tbl 08

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

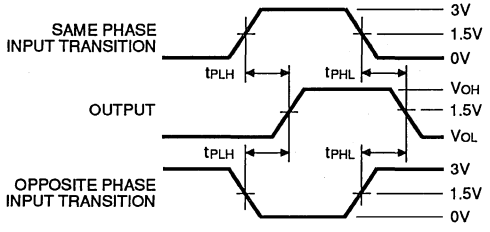
SET-UP, HOLD AND RELEASE TIMES



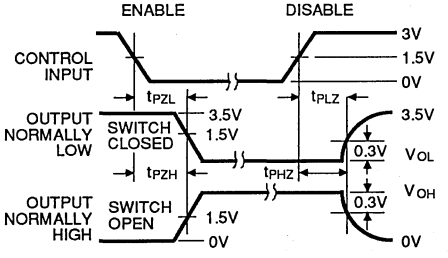
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

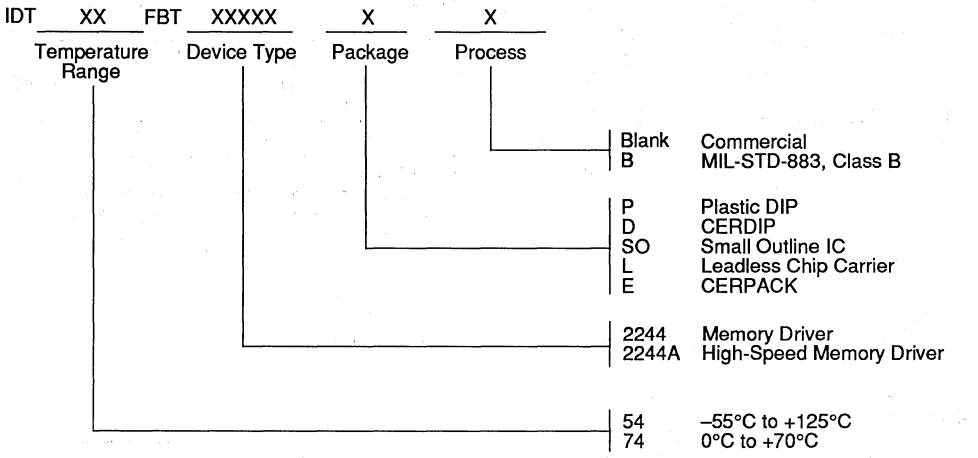


NOTES 2641 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

A

ORDERING INFORMATION



Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS OCTAL TRANSPARENT LATCH DRIVERS

ADVANCE INFORMATION
IDT54/74FBT2373
IDT54/74FBT2373A

FEATURES:

- 25Ω output resistors reduce overshoot and undershoot when driving MOS RAMs
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Higher static V_{OH} for improved noise immunity and reduced power dissipation.
- Low power in all three states
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

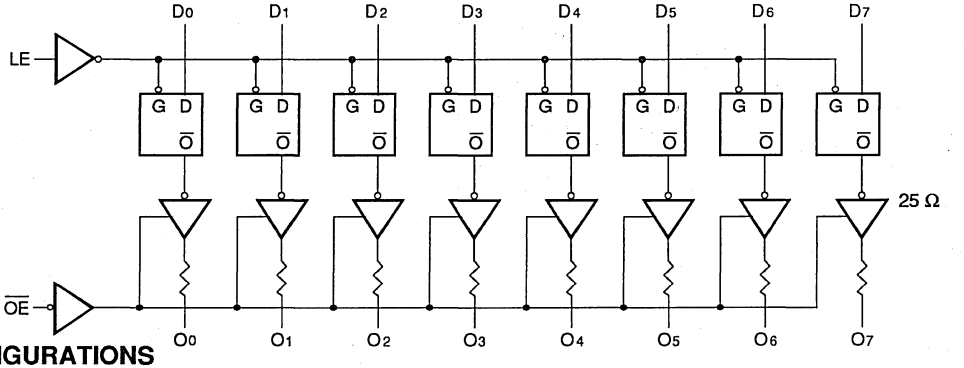
The FBT series of BiCMOS Latch Drivers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT2373 series are 3-state, 8-bit latches where each output is terminated with a 25Ω series resistor. The latches appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

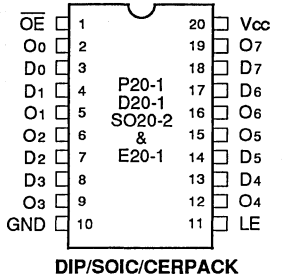
The FBT series of bus interface devices are ideal for driving large capacitive loads with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection. The output buffers are designed to guarantee a static V_{OH} of 2.7V. This higher output level in the high state will result in a significant reduction in overall system power dissipation and in improved noise immunity when driving DRAMS and SRAMS.

A

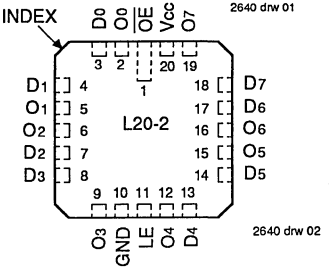
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN DESCRIPTION

Pin Names	Description
$D_0 - D_7$	Data Inputs
LE	Latch Enables Input (Active HIGH)
$\overline{OE}$	Output Enables Input (Active LOW)
$O_0 - O_7$	3-State Latch Outputs

2640 tbl 05

FUNCTION TABLE[1]

Inputs			Outputs
D_n	LE	$\overline{OE}$	O_n
H	H	L	H
L	H	L	L
X	L	L	NC
X	X	H	Z

NOTE: 2640 tbl 06

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   NC = No Change

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2640 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Type	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2640 tbl 02

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V		—	—	-10	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	-50	
I_I	Input HIGH Current	V_{CC} = Max., V_{CC} (Max.)		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{ODH}	Output Drive Current	V_{CC} = Min., V_O = 2.25V		-35	—	—	mA
I_{ODL}	Output Drive Current	V_{CC} = Min., V_O = 2.25V		50	—	—	mA
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		-75	—	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = -1mA	2.7	3.8	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = - 8mA	2.4	3.3	—	
			I_{OH} = -12mA	2.0	3.2	—	
V_{OL}	Output LOW Voltage		I_{OL} = 1mA	—	0.1	0.5	V
			I_{OL} = 12mA	—	0.35	0.8	
V_H	Input Hysteresis	V_{CC} = 5V		—	200	—	mV
I_{CCH} I_{CCZ} I_{CCL}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2640 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

A

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}$ = GND, LE = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.3	0.4	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.2	5.5	mA
		$\overline{OE}$ = GND, LE = V_{CC} One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	3.5	6.5	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	6.2	9.5[5]	
		$\overline{OE}$ = GND, LE = V_{CC} Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	8.2	17.5[5]	

2640 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTLI inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FBT2373				IDT54/74FBT2373A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	8.5	1.5	5.2	1.5	5.6	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_n		2.0	9.3	2.0	10.1	2.0	8.5	2.0	9.8	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	12.0	1.5	12.5	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.4	1.5	8.1	1.5	5.5	1.5	6.5	ns
t_{SU}	Set-up Time HIGH or LOW D_n to LE		2.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW D_n to LE		1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	LE Pulse Width HIGH or LOW		6.0	—	6.0	—	5.0	—	6.0	—	ns

NOTES:

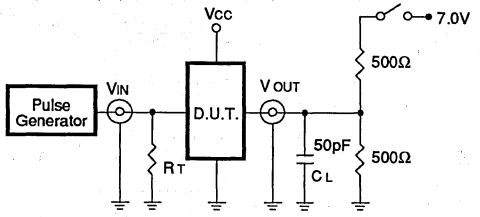
2640 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

A

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

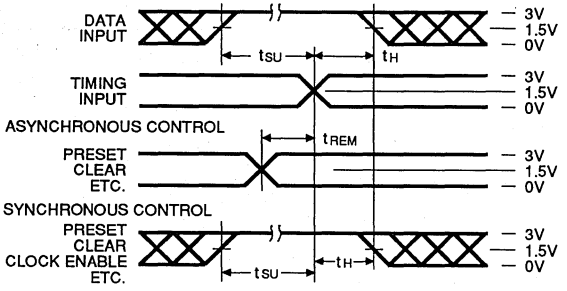
2640 tbl 08

DEFINITIONS:

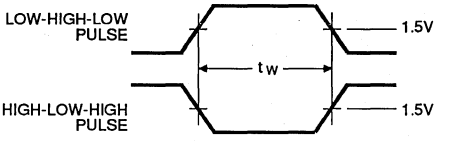
C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

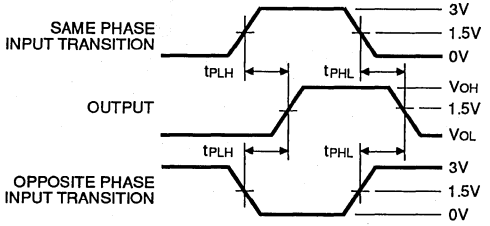
SET-UP, HOLD AND RELEASE TIMES



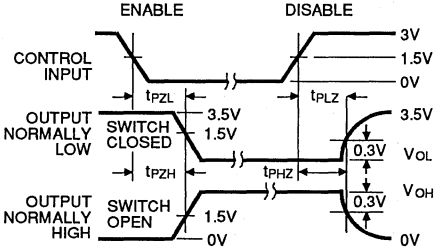
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

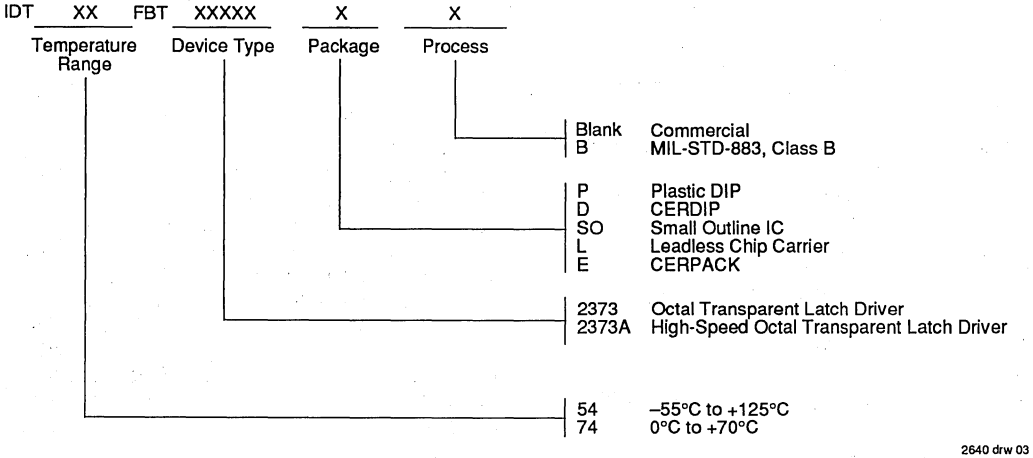


2640 drw 04

NOTES

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



2640 drw 03

A

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS 10-BIT MEMORY LATCHES

IDT54/74FBT2841A
IDT54/74FBT2841B

FEATURES:

- 25Ω output resistors reduce overshoot and undershoot when driving MOS RAMs
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Low power in all three states
- ± 10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

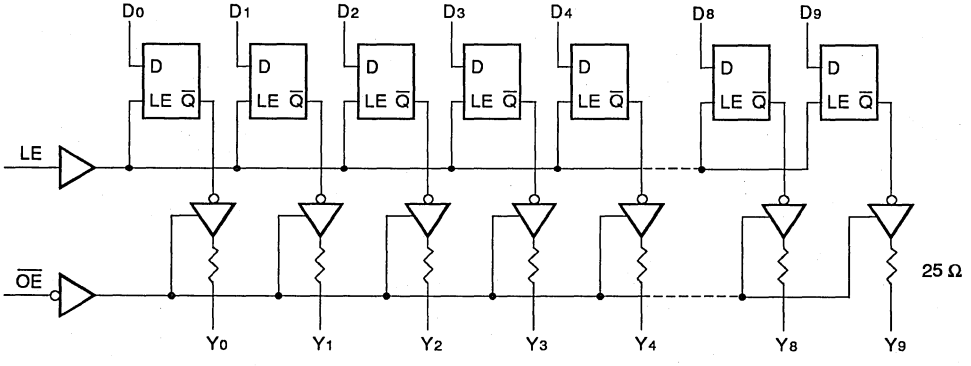
DESCRIPTION:

The FBT series of BiCMOS Memory Drivers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT2841 series are 3-state, 10-bit latches where each output is terminated with a 25Ω series resistor.

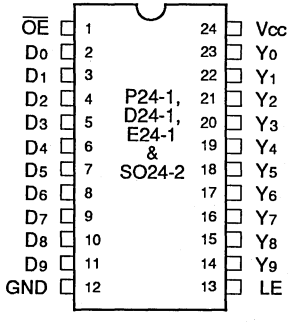
The FBT series of memory line drivers are ideal for use in designs needed to drive large capacitive loads with low static (DC) current loading. They are also designed for rail-to-rail output switching. This higher output level in the high state will result in a significant reduction in overall system power dissipation.

FUNCTIONAL BLOCK DIAGRAM

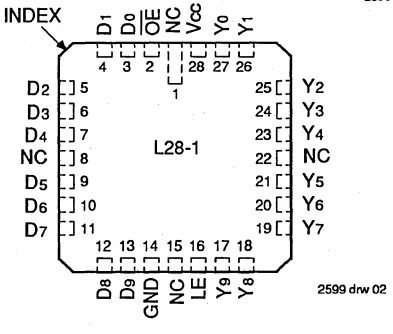


PIN CONFIGURATIONS

2599 drw 01



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

BiCEMOS is a trademark of Integrated Device Techology, Inc.

PIN DESCRIPTION

Name	I/O	Description
$D_0 - D_9$	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
$Y_0 - Y_9$	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is high, the outputs Y_I are in the high-impedance (off) state.

2599 tbl 05

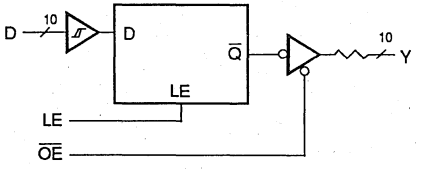
FUNCTION TABLE[1]

Inputs			Internal	Outputs	
$\overline{OE}$	LE	D_I	Q_I	Y_I	Function
H	X	X	X	Z	High Z
H	H	L	L	Z	High Z
H	H	H	H	Z	High Z
H	L	X	NC	Z	Latched (High Z)
L	H	L	L	L	Transparent
L	H	H	H	H	Transparent
L	L	X	NC	NC	Latched

NOTE: 2599 tbl 06

1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, Z = High Impedance

LOGIC SYMBOL



2599 drw 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2599 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Inputs and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2599 tbl 02

1. This parameter is measured at characterization but not tested.

A

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V		—	—	-10	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	-50	
I_I	Input HIGH Current	V_{CC} = Max., V_{CC} (Max.)		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{ODH}	Output Drive Current	V_{CC} = Min., V_O = 2.25V		-35	—	—	mA
I_{ODL}	Output Drive Current	V_{CC} = Min., V_O = 2.25V		50	—	—	mA
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		-75	—	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = -1mA	2.7	3.8	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = - 8mA	2.4	3.3	—	
			I_{OH} = -12mA	2.0	3.2	—	
V_{OL}	Output LOW Voltage		I_{OL} = 1mA	—	0.1	0.5	V
			I_{OL} = 12mA	—	0.35	0.8	
V_H	Input Hysteresis	V_{CC} = 5V		—	200	—	mV
I_{CCH} I_{CCZ} I_{CCL}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES:
2599 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}$ = GND One Input Toggling LE = V_{CC} 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.3	0.4	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.2	5.5	mA
		$\overline{OE}$ = GND, LE = V_{CC} One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	3.5	6.5	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	7.7	11.5[5]	
		$\overline{OE}$ = GND, LE = V_{CC} Ten Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	10.2	21.5[5]	

2599 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

A

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

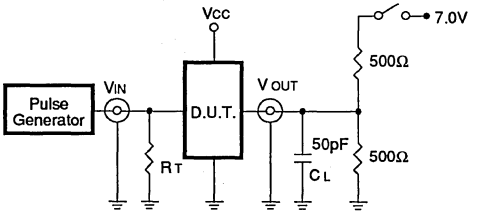
Symbol	Parameter	Condition[1]	54/74FBT2841A				54/74FBT2841B				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay DI to YI (LE = HIGH)	CL = 50pF RL = 500Ω	—	9.0	—	10.0	—	6.5	—	7.5	ns
tSU	Data to LE Set-up Time		2.5	—	2.5	—	2.5	—	2.5	—	ns
tH	Data to LE Hold Time		2.5	—	3.0	—	2.5	—	2.5	—	ns
tPLH tPHL	Propagation Delay LE to YI		—	12.0	—	13.0	—	8.0	—	10.5	ns
tW	LE Pulse Width[3] HIGH		4.0	—	5.0	—	4.0	—	4.0	—	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to YI		—	11.5	—	13.0	—	8.0	—	8.5	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to YI		—	8.0	—	10.0	—	7.0	—	7.5	ns

2599 tbl 07

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed, but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



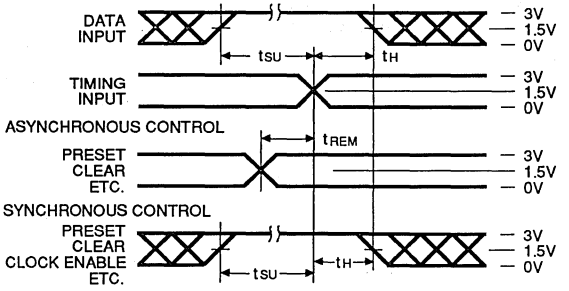
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

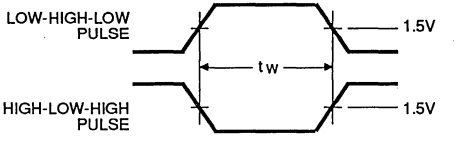
DEFINITIONS: 2599 tbl 08

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

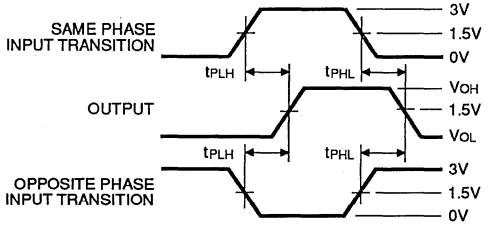
SET-UP, HOLD AND RELEASE TIMES



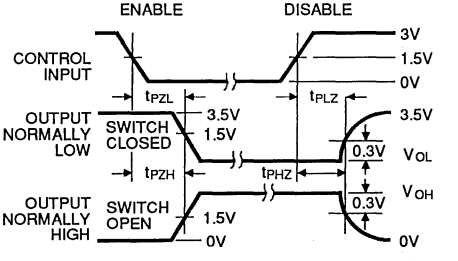
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

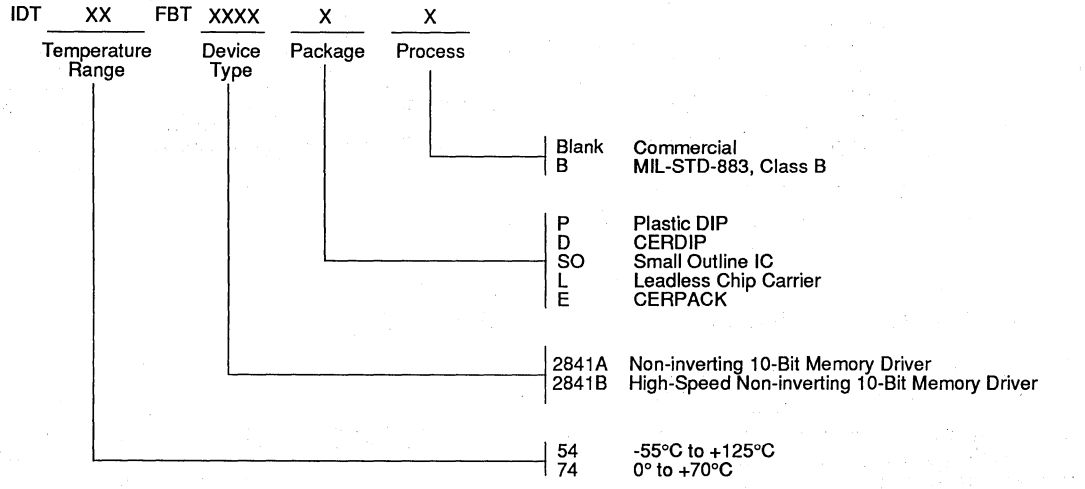


NOTES 2599 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; tF ≤ 2.5ns; tR ≤ 2.5ns.

A

ORDERING INFORMATION



2599 drw 04

The following section contains important new data sheets and application notes that were not included in the 1991 LOGIC Data Book.

Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS INTERFACE REGISTERS

PRELIMINARY
IDT54/74FCT826AT
IDT54/74FCT826BT
IDT54/74FCT826CT

FEATURES:

- IDT54/74FCT826AT equivalent to FAST™ speed and drive
- IDT54/74FCT826BT up to 30% faster than FAST™
- IDT54/74FCT826CT up to 50% faster than FAST™
- Equivalent to AMD's Am29826 bipolar registers in pinout/function, speeds and output drive over full temperature and voltage supply extremes
- High-speed parallel registers with positive edge-triggered D-type flip-flops
- Buffered common Clock Enable ($\overline{EN}$) and asynchronous Clear input ($\overline{CLR}$)
- I_{OL} = 48mA (commercial) and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- Substantially lower input current levels (5μA max.) than AMD's bipolar Am29800 series
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Meet or exceed JEDEC Standard 18 specifications

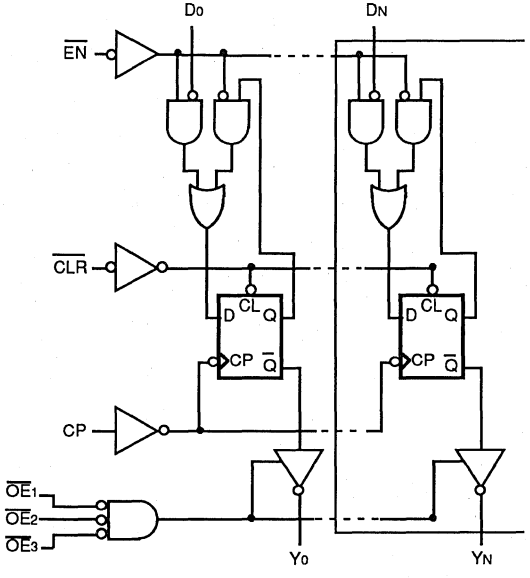
DESCRIPTION:

The IDT54/74FCT800AT/BT/CT series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT826 series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity.The IDT54/74FCT826AT/BT/CT are 8-bit inverting buffered registers with all the '823 controls plus multiple enables ($\overline{OE_1}$, $\overline{OE_2}$, $\overline{OE_3}$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the IDT54/74FCT8XX high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state.

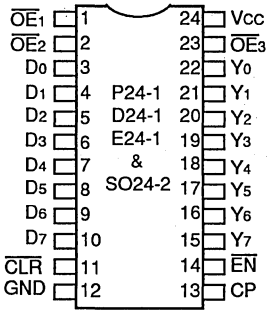
FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor.

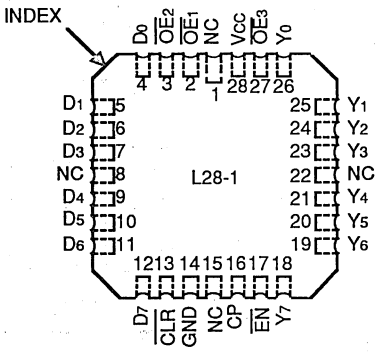
2522 drw 01

PIN CONFIGURATION



2522 drw 02

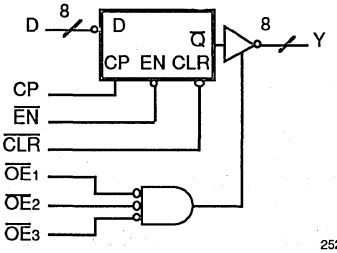
DIP/SOIC/CERPACK TOP VIEW



2522 drw 03

LCC TOP VIEW

LOGIC SYMBOL



2522 drw 04

FUNCTION TABLES(1)

Inputs					Internal/ Outputs		
OE(2)	CLR	EN	DI	CP	QI	YI	Function
L	H	L	L	↑	H	Z	High Z
L	H	L	H	↑	L	Z	
L	L	X	X	X	L	Z	Clear
H	L	X	X	X	L	L	
L	H	H	X	X	NC	Z	Hold
H	H	H	X	X	NC	NC	
L	H	L	L	↑	H	Z	Load
L	H	L	H	↑	L	Z	
H	H	L	L	↑	H	H	
H	H	L	H	↑	L	L	

2522 tbl 05

NOTE:
1. H=HIGH
   L=LOW
   X=Don't Care
   NC= No change
   ↑= LOW-to-HIGH Transition
   Z = High Impedance
2. OE is an Active-High internal signal produced as follows:

OE1	OE2	OE3	OE
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

2522 tbl 05a

PIN DESCRIPTION

Names	I/O	Description
DI	I	The D flip-flop data inputs.
CLR	I	When the clear input is LOW and OE is LOW, the QI outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
YI	O	The register three-state outputs.
EN	I	Clock Enable. When the clock enable is LOW, data on the DI input is transferred to the QI output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the QI outputs do not change state, regardless of the data or clock input transitions.
OEn	I	Output Control. When any OEn input is HIGH, the YI outputs are in the high impedance state. When all OEn inputs are LOW, the TRUE register data is present at the YI outputs.

2522 tbl 04

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE: 2522 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2522 tbl 02

1. This parameter is measured at characterization, but is not production tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: T_A = -55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	Vcc = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	Vcc = Max.	V_I = 0.5V	—	—	–5	µA
I_{OZH}	High Impedance Output Current	Vcc = Max.	V_O = 2.7V	—	—	10	µA
I_{OZL}			V_O = 0.5V	—	—	–10	
I_I	Input HIGH Current	Vcc = Max., V_I = Vcc (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	Vcc = Max.(3), V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	Vcc = Max. V_{IN} = GND or Vcc		—	0.2	1.5	mA

NOTES: 2522 tbl 03

1. For conditions shown as Max. or Min. use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = $\overline{EN}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle $\overline{OE}$ = $\overline{EN}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle $\overline{OE}$ = $\overline{EN}$= GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	4.0	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.2	16.8[5]	

NOTES:

2522 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

A

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

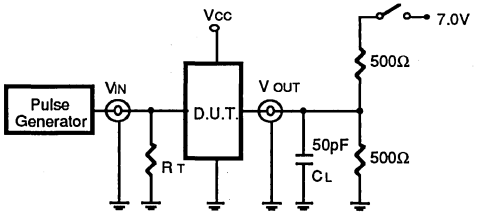
Symbol	Parameter	Test Conditions[1]	IDT54/74FCT826AT				IDT54/74FCT826BT				IDT54/74FCT826CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CP to Y i ($\overline{OE}$ = LOW)	CL = 50pF RL = 500Ω	—	10.0	—	11.5	—	7.5	—	8.5	—	6.0	—	7.0	ns
		CL = 300pF[3] RL = 500Ω	—	20.0	—	20.0	—	15.0	—	16.0	—	12.5	—	13.5	
tSU	Set-up Time HIGH or LOW D i to CP	CL = 50pF RL = 500Ω	4.0	—	4.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW D i to CP		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tSU	Set-up Time HIGH or LOW $\overline{EN}$ to CP		4.0	—	4.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW $\overline{EN}$ to CP		2.0	—	2.0	—	0	—	0	—	0	—	0	—	ns
tPHL	Propagation Delay, $\overline{CLR}$ to Yi		—	14.0	—	15.0	—	9.0	—	9.5	—	8.0	—	8.5	ns
tREM	Recovery Time $\overline{CLR}$ to CP		6.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tW	Clock Pulse Width HIGH or LOW		7.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tW	$\overline{CLR}$ Pulse Width LOW		6.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to Yi	CL = 50pF RL = 500Ω	—	12.0	—	13.0	—	8.0	—	9.0	—	7.0	—	8.0	ns
		CL = 300pF[3] RL = 500Ω	—	23.0	—	25.0	—	15.0	—	16.0	—	12.5	—	13.5	
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to Yi	CL = 5pF[3] RL = 500Ω	—	7.0	—	8.0	—	6.5	—	7.0	—	6.0	—	6.0	ns
		CL = 50pF RL = 500Ω	—	8.0	—	9.0	—	7.5	—	8.0	—	7.0	—	7.0	

NOTES:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

2522 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS

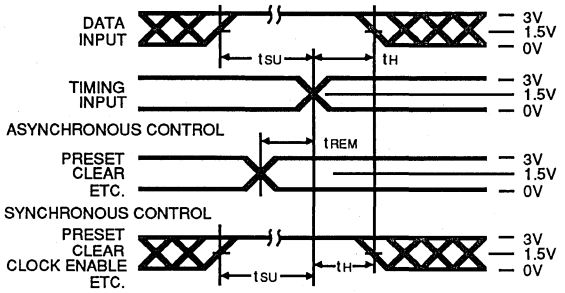


SWITCH POSITION

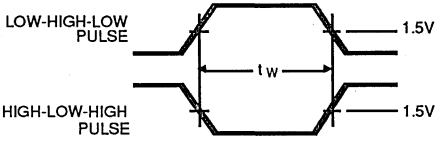
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

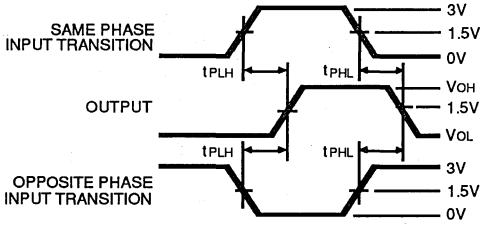
SET-UP, HOLD AND RELEASE TIMES



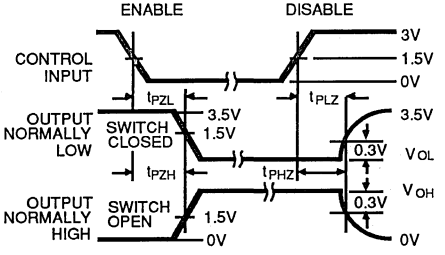
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



NOTES
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Z_O ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

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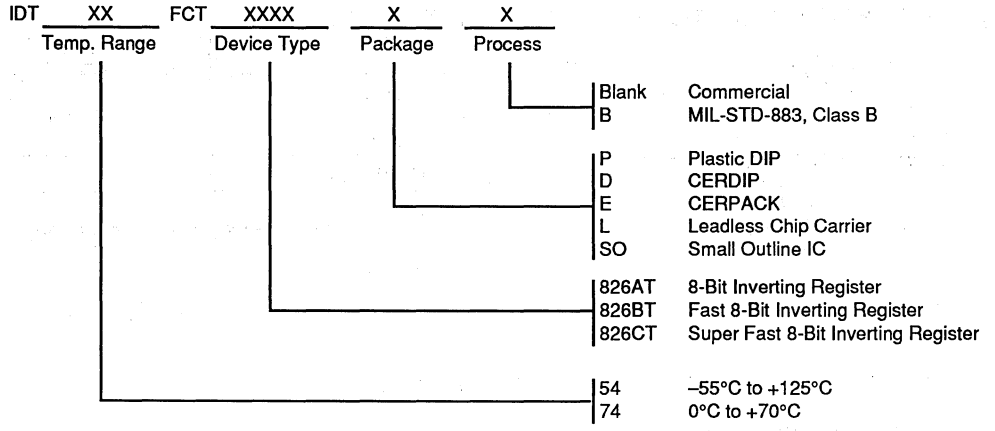
ORDERING INFORMATION



2522 drw 05

Integrated Device Technology, Inc.

CLOCK DISTRIBUTION SIMPLIFIED WITH IDT GUARANTEED SKEW CLOCK DRIVERS

APPLICATION NOTE AN-82

By Michel Conrad

INTRODUCTION

In today's world of RISC or CISC microprocessor based systems there is an endless quest for cost effective solutions which offer the best system performance. Faster processors, increased integration and innovations in architecture have resulted in high performance systems which can be packed into smaller and smaller boxes. With processor clock frequencies migrating towards 33, 40 and 50Mhz, clock signals are becoming more and more critical. As the clock period gets shorter, the uncertainty or skew in the clock distribution system becomes more of a problem. Since clocks are used to drive the processors and to synchronize the transfer of data between system components the clock distribution system is an essential part of the system design. A clock distribution system design that does not take skew into consideration may result in a system with degraded performance and reliability.

Designing a clock distribution system which minimizes skew is not a trivial problem. To address this problem IDT has developed the IDT49FCT805 and IDT49FCT806 guaranteed skew clock drivers. These high-speed clock drivers have been designed to minimize skew, thus simplifying the problem of designing a reliable, minimum skew clock distribution system. This application note discusses the issues surrounding clock skew, clock drivers, and clock distribution. It will show how the IDT49FCT805 and IDT49FCT806 can be used to simplify the design of minimum skew clock distribution systems.

WHAT IS CLOCK SKEW ?

The term clock skew is used to describe the timing differences between signals in a clock distribution system. The non-ideal characteristics of system components and their connecting circuitry result in uncertainties as to when clock signals trigger their loads. Figure 1 shows a generalized, multiple output clock driver and its associated timing for the low-to-high transition. A common signal drives each input resulting in "n" copies of that signal on the clock driver outputs. The clock skew is the difference in propagation delay between the driver's slowest output and its fastest output. Since output "n" has the minimum propagation delay and output "1" has the maximum propagation delay, the clock skew is the difference or $t_{PLH1} - t_{PLHn}$.

In a typical system clock skew has two distinct sources. The first source of skew is the clock driver device itself. The clock driver is a piece of interface logic used to drive clock signal lines. With any given technology the clock driver is an inherent source of skew. In an ideal clock driver all the internal circuit elements of the device are perfectly matched so that propagation delays through equivalent paths are identical. In a practical clock driver there are many variables which can effect the propagation delay through equivalent paths and therefore contribute to skew. The layout and electrical characteristics of the circuit elements, the location of those elements relative to ground and Vcc, as well as the parasitics of the

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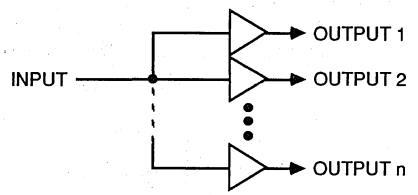
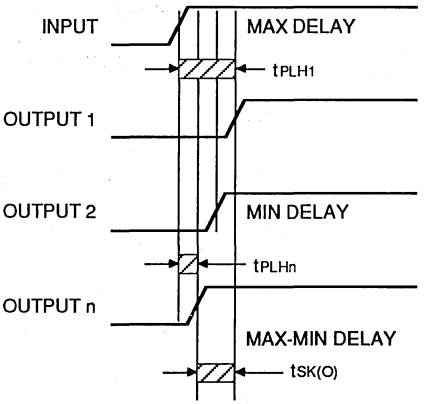


Output Skew, $t_{SK(O)}$ =
$t_{P(max)} - t_{P(min)} = t_{PLH1} - t_{PLHn}$
(same package, same transition)



2521 drw 01

Output Skew is the difference in propagation delay between the fastest and the slowest outputs of a single chip for the same input and output transition.

Figure 1. Output Skew $t_{SK(O)}$ Schematic and Timing Diagram

package can all have an effect on propagation delay. Many of these variables are dependant on manufacturing process parameters, which adds many more variables that can effect the skew characteristics of the device.

The second source of clock skew is the clock distribution system. How the clock driver device is incorporated into the clock distribution system is critical. The issues include the layout of signal lines, device loading, power supply connections and power supply decoupling. Operating conditions such as the power supply voltage and the ambient temperature also play a significant role. Because of the fast edge rates found in today's high speed logic, most PCB traces should be treated as transmission lines. If the design does not address the transmission line effects caused by the fast edge rates, the design may never work as intended.

THE CLOCK SKEW PROBLEM

Clock skew problems arise when the timing requirements of a system component are violated. Many of the common clocking bottlenecks can be categorized into two types of clock skew problems. The first is the synchronization problem caused by skew between multiple copies of a system clock. The second problem is that of meeting the duty cycle requirements of system components which require a controlled duty cycle.

A simple pipeline register can be used to illustrate the synchronization problem (Figure 2). The pipeline is composed of two registers and some clock circuitry. The clock circuit begins with a Master Clock which is buffered into two clock signals, CLK1 and CLK2. CLK1 drives Register X and CLK2 drives Register Y. The registers are configured to pass sequential data on each clock cycle so that the current output of Register Y is the previous cycle's output of Register X. The circuit's timing is shown in Figure 3.

In Figure 3-a the data sample "N" is the input to Register X and data "N-1" is the input to Register Y. For correct operation the input to each register must satisfy the setup and hold time requirements with respect to its clock. Since the output of Register X is the input to Register Y, the hold time t_{Hy} should not be greater than $t_{PDx(min)}$. In Figure 3-a CLK1 and CLK2 switch at the same time so that the output of Register X satisfies the setup and hold time requirements of the input to Register Y.

In Figure 3-b CLK2 is delayed relative to CLK1 resulting in a t_{SKEW} between the two clocks. Now, for correct operation the hold time t_{Hy} should not be greater than $t_{PDx(min)}$-t_{SKEW}. As shown, the skew in CLK2 causes a violation of either the hold time requirement of data "N-1" or the setup time requirement of data "N" as input to Register Y. For correct operation data "N-1" must be clocked into Register Y and in Figure 3-b it is unclear whether data "N" or "N-1" is clocked into Register Y. If the timing margin $t_{PDx(min)}$-t_{Hy} is about 2.5ns then a clock skew of 2.5ns or greater is a threat to the reliability of the system

Many microprocessor systems require that the clock have a controlled duty cycle. Guaranteeing a fixed duty-cycle at fast clock rates is difficult because propagation delays for opposite transitions in standard interface logic used for clock distribution are seldom identical. Also, timing differences between transitions do not scale with frequency. If a driver has 3.0ns of pulse skew (see definitions below) the tolerance of a 25ns cycle time (40Mhz) is ±12%. If the clock is pushed to 50Mhz, the tolerance grows to ±15%. A rule-of-thumb is that no more than 10% of the clock cycle be used for clock distribution. It is clear that if standard components are used the rule is easily violated at higher clock frequencies.

CLOCK SKEW DEFINITIONS

With the objective of minimizing skew inherent to the clock driver device, IDT has designed the IDT49FCT805 and IDT49FCT806 clock drivers. These clock drivers are designed to meet very tight skew specifications. The critical parameters are output skew, pulse skew, and package or part-to-part skew.

Output skew $t_{SK(O)}$ is the difference in propagation delay between any two outputs of the same device going through the same transition. This is the type of skew illustrated in Figure 1. If the propagation delay of the slowest output (t_{PLH1})

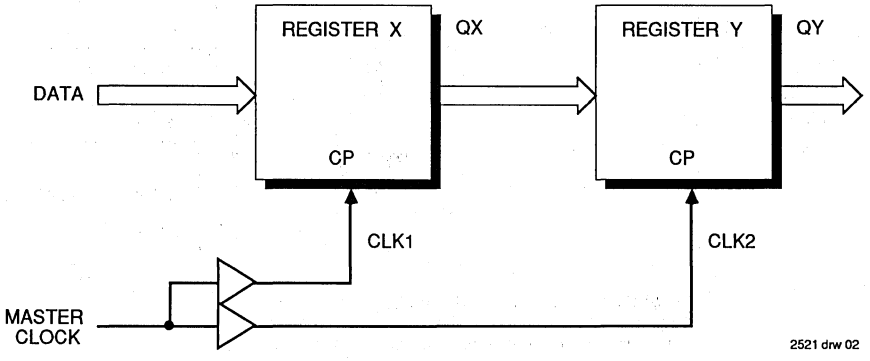
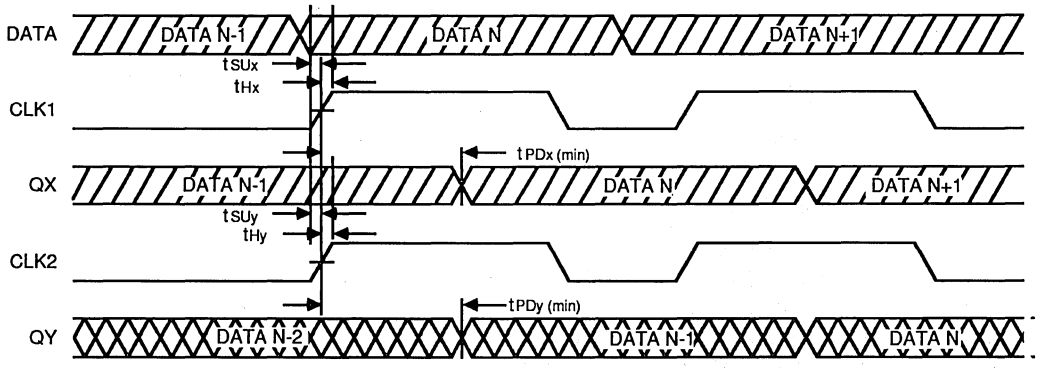
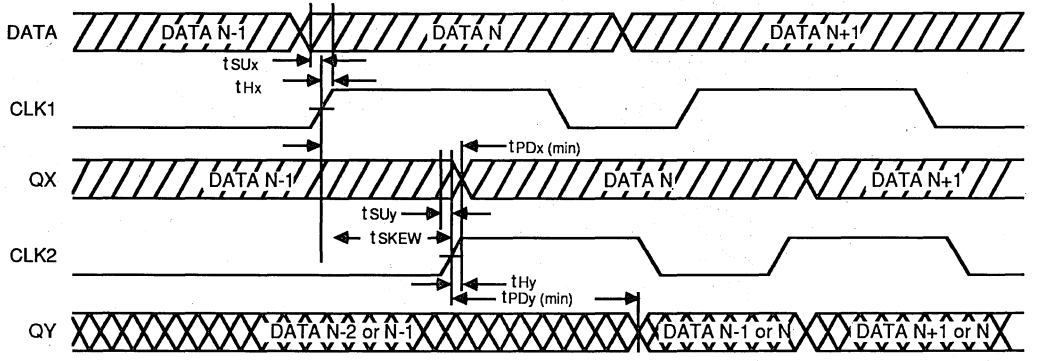


Figure 2. Schematic for a Two Register Pipeline



(a) Pipeline timing without skew between CLK1 and CLK2.



(b) Pipeline timing with skew between CLK1 and CLK2.

Figure 3. Timing Diagrams for Pipeline Register Example

is 5.0ns and the fastest output (t_{PLHn}) is 3.0ns then the output skew is 2.0ns. The $t_{SK(O)}$ parameter applies to all the outputs of a single clock driver chip. It is measured separately for the high-to-low and low-to-high transitions. Figure 4 shows the measured output skew of several IDT49FCT805As for low-to-high and high-to-low transitions. Under typical conditions (V_{CC}=5.0V, TEMP=25°C) the maximum skew is less than 450 picoseconds for both the low-to-high and high-to-low conditions. In the IDT49FCT805/806 data sheet this value is guaranteed to be less than 700 picoseconds over the commercial operating range.

Pulse skew $t_{SK(P)}$ is the difference in propagation delay for low-to-high and high-to-low transitions and is measured on a single output pin. In Figure 5, if t_{PLH1} is 5.5ns and t_{PHL1} is 4.0

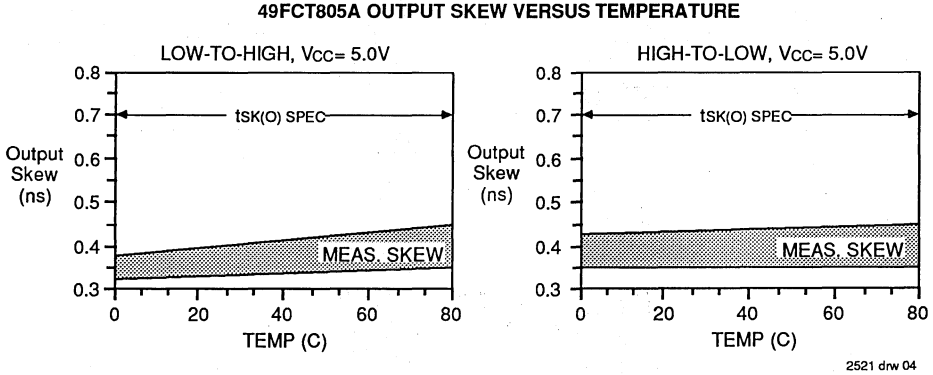


Figure 4. Measured Output Skew $t_{SK(O)}$ of Several IDT49FCT805As

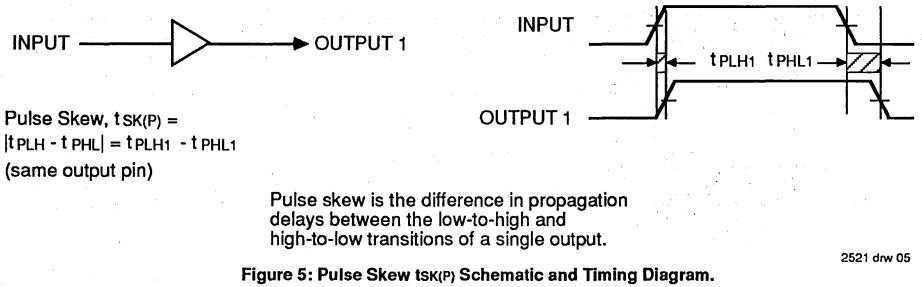


Figure 5: Pulse Skew tSK(P) Schematic and Timing Diagram.

ns, tSK(P) will be the the difference, or 1.5ns. Pulse skew is also a measure of the duty cycle distortion that the clock driver will contribute to an incoming clock signal. This is an important parameter for applications that use both edges of the clock and where a controlled duty cycle is required. Figure 6 shows the pulse skew measured on several IDT49FCT805As. Under typical conditions the measured pulse skew was less than 825 picoseconds. In the data sheet this value is guaranteed to be less than 1.0 nanosecond over the commercial operating range. For a 40Mhz clock with a period of 25ns, the IDT49FCT805/806 guarantees a maximum of 4% duty cycle distortion.

Part-to-part or package skew tSK(T) is similar to output skew. The difference is that it applies to outputs of two or more devices. The timing diagram in Figure 7 illustrates the case

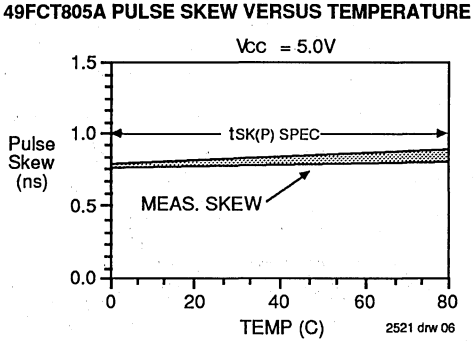


Figure 6. Measured Pulse Skew tSK(P) on Several IDT49FCT805As

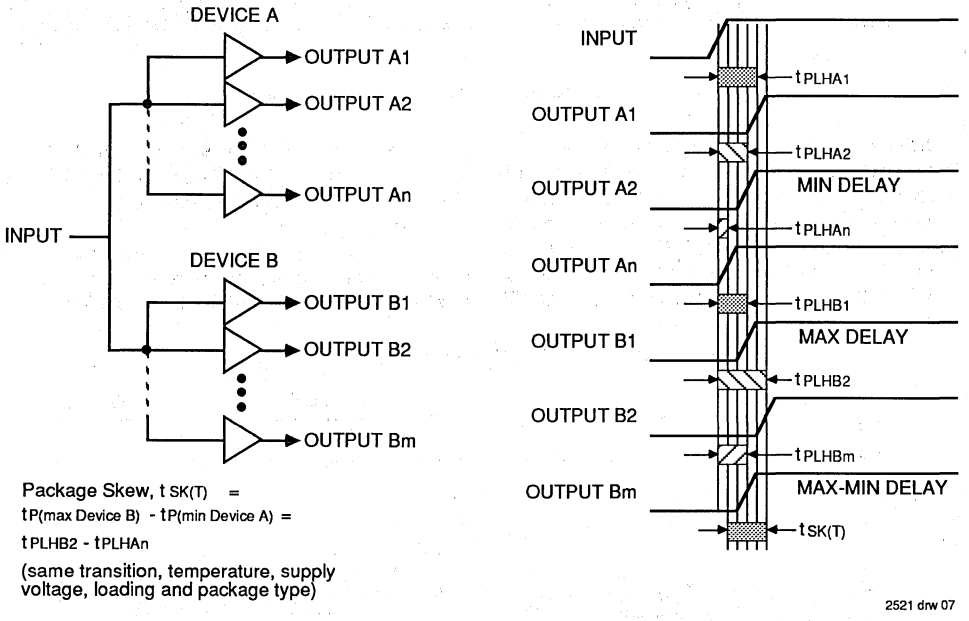


Figure 7. Package Skew tSK(T) Schematic and Timing Diagram

where two generalized clock drivers are driven by a common input. The result is "n" outputs from device A and "m" outputs from device B making the same transition. The package skew is the difference in propagation delay between the slowest output of one device and the fastest output of the other device for the same transition. In this case the output An is the fastest output and the output B2 is the slowest If t_{PLHAn} is 4.0ns and t_{PLHB2} is 6.0ns the package skew is 2.0ns. Certain conditions must be satisfied for the package skew specification to apply. The devices must have the same Vcc, ambient temperature and be assembled in the same package type. Also each device must have equivalent loading and be of the same speed grade.

Part-to-part skew is difficult to specify because it implies that the characteristics every part ever sold will operate within a window of operation. The window of operation ensures that parts that run too fast or too slow do not get sold. Figure 8 shows the measured values of package skew on several IDT49FCT805As under typical conditions. The maximum measured package skew from this sample is 525 picoseconds. In the IDT49FCT805/806 data sheet this value is guaranteed to be less than 1.5 nanoseconds over the commercial operating range.

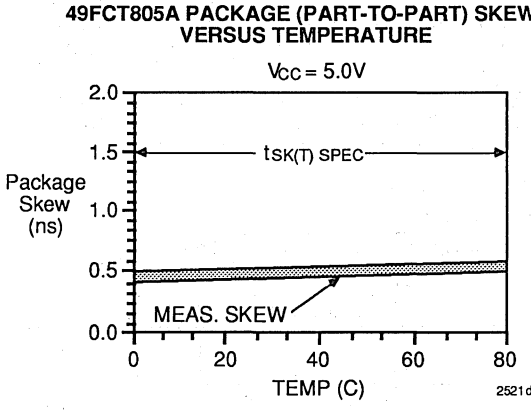


Figure 8. Measured Package Skew $t_{SK(T)}$ for Several IDT49FCT805As

THE IDT49FCT805 & IDT49FCT806 CLOCK DRIVERS

The IDT49FCT805 and 49FCT806 are high-speed guaranteed skew clock driver chips specifically designed to meet the clocking requirements of today's high-performance systems. The logic diagram and pin configuration of the IDT49FCT805 are given in Figure 9. The IDT49FCT806 is the inverting option of IDT49FCT805.

Skew in the IDT49FCT805/806 is minimized throughout the design process. Careful circuit design and layout in silicon have resulted in a pin configuration that is specifically designed for very low output and pulse skew. Independent power and ground pins reduce the amount of ground bounce and dynamic threshold shift caused by multiple outputs switching. The 1:5 input to output ratio reduces the amount of capacitive loading on the previous stage which simplifies termination and reduces component count when compared to conventional solutions. The devices are optimized for both PDIP and SOIC packages.

The IDT49FCT805/806 clock drivers consist of two independent banks of drivers. Each bank drives five output buffers from a single standard TTL compatible CMOS input. The input has 200mV of hysteresis for increased immunity to system noise. Independent active low output enable pins ($\overline{OEA}$ and $\overline{OEB}$) control each of the banks, allowing for independent control of the outputs. This feature may be used in applications where clock bussing or a power savings mode is required. The input INB drives the B bank as well as an output called MON (Monitor). The MON output is not controlled by $\overline{OEB}$ and therefore runs continuously. The MON signal can be used for priming phase locked loops or driving diagnostic hardware.

Each IDT49FCT805/806 has 3 ground pins and 2 VCC pins. The ground pins, GNDA and GNDB, are located in the middle of the package to minimize inductance in the ground return path. The two grounds are returns for the A and B bank output buffer and pre-driver currents. The third ground pin, GNDQ (Quiet Ground), provides a ground return for the remaining circuitry. The ground pin arrangement reduces ground bounce on the outputs and noise on the thresholds of the internal logic. Since GNDA and GNDB are completely

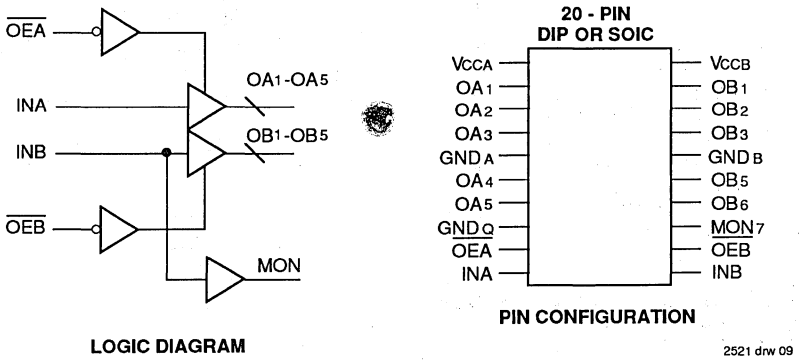


Figure 9. Logic Diagram and Pinout of the IDT49FCT805

isolated from each other on the die, switching effects on one bank will have minimal effects on the other bank. The independent V_{CC} pins, V_{CCA} and V_{CCB}, supply power to the two banks.

Each output of the IDT49FCT805/806 clock driver features a high current drive output buffer. These outputs can be used to drive both TTL and CMOS loads. With a typical V_{OL} of 0.3 volts the buffer can sink 64mA. For a typical V_{OH} of 3.8 volts the output buffer can source 24mA. These output buffers are optimized around the 1.5 volts switching threshold which is the standard for TTL compatible logic. These output buffers can easily meet the edge rate requirements of today's microprocessors and peripheral components. Typical edge rates for the IDT49FCT805A are 1.0 volt/nanosecond for risetime and 2.0 volt/nanosecond for falltime

WORKING WITH THE DATA SHEET

In the past, designers have used the minimum and maximum limits of a clock driver's propagation delay specifications to determine skew in their designs. With the IDT74FCT244A ($t_{PHL\ min}$=1.5ns and $t_{PHL\ max}$=4.8 ns) the difference between the two limits results in a 3.3ns window. With the IDT49FCT805/806, subtracting the minimum from the maximum limit is no longer necessary because the skew is specified in the data sheet. However, because the IDT49FCT805/806 data sheet still specifies a 1.5ns minimum for propagation delay there may be some confusion as to whether or not the skew specifications are real. In the following discussion it will be shown that meeting the skew specifications is not a problem for IDT49FCT805.

The Switching Characteristics (Table 1) for the FCT805A/806A show the maximum propagation delay ($t_{PLH/HL}$) to be 5.8 ns and the minimum propagation delay to be 1.5ns. If the skew is calculated by subtracting the minimum delay from the maximum delay the result is a number much larger than the $t_{SK(O)}$ spec of 700ps. How can IDT guarantee a 700ps output skew number and still have such a wide range of minimum and maximum propagation delay values?

The range of values between the minimum and maximum propagation delay reflects the wide range of conditions under which the part must operate and the range of manufacturing process parameters. Consider a part that under typical conditions has a median propagation delay of 5.0ns. According to the $t_{SK(O)}$ specification of 700ps, each output of that driver will switch within a 5.0±0.35 ns window. If the median propagation delay drops to 4.0ns, due to variations in V_{CC} or temperature, the specification guarantees that each output will then switch within a 4.0±0.35ns window. In the unlikely event that the operating conditions cause the median delay to drop to 1.85ns, then all outputs will switch within a 1.85±0.35ns window. It is important to recognize that all the devices are assumed to be operating under the same conditions. If one part is running fast because of cold temperature and high V_{CC}, all the other parts will be running fast as well. The following data is provided to show that the IDT49FCT805A does indeed meet its skew specifications over the commercial operating range.

Figure 10 shows the range of output skew measurements for low-to-high and high-to-low transitions with V_{CC}s of 4.75 and 5.25 volts. For both low-to-high and high-to-low transitions,

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions[1]	IDT49FCT805/806 Com'l. Min.[2]	IDT49FCT805/806 Com'l. Max.	IDT49FCT805A/806A Com'l. Min.[2]	IDT49FCT805A/806A Com'l. Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay IN_A to OA_n, IN_B to OB_n	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	5.8	ns
t_{PZL} t_{PZH}	Output Enable Time OE_A to OA_n, OE_B to OB_n		1.5	8.0	1.5	8.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time OE_A to OA_n, OE_B to OB_n		1.5	7.0	1.5	7.0	ns
$t_{SK(O)}$[3]	Skew between two outputs of same package (same transition)		—	0.7	—	0.7	ns
$t_{SK(P)}$[3]	Skew between opposite transitions (t_{PHL}-t_{PLH}) of same output		—	1.0	—	1.0	ns
$t_{SK(T)}$[3]	Skew between two outputs of different package at same power supply voltage and temperature (same transition)		—	1.5	—	1.5	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays
3. Skew guaranteed across temperature range but measured at maximum temparature only. Skew parameters apply to propagation delays only.

Table 1. IDT49FCT805/806 Switching Characteristics

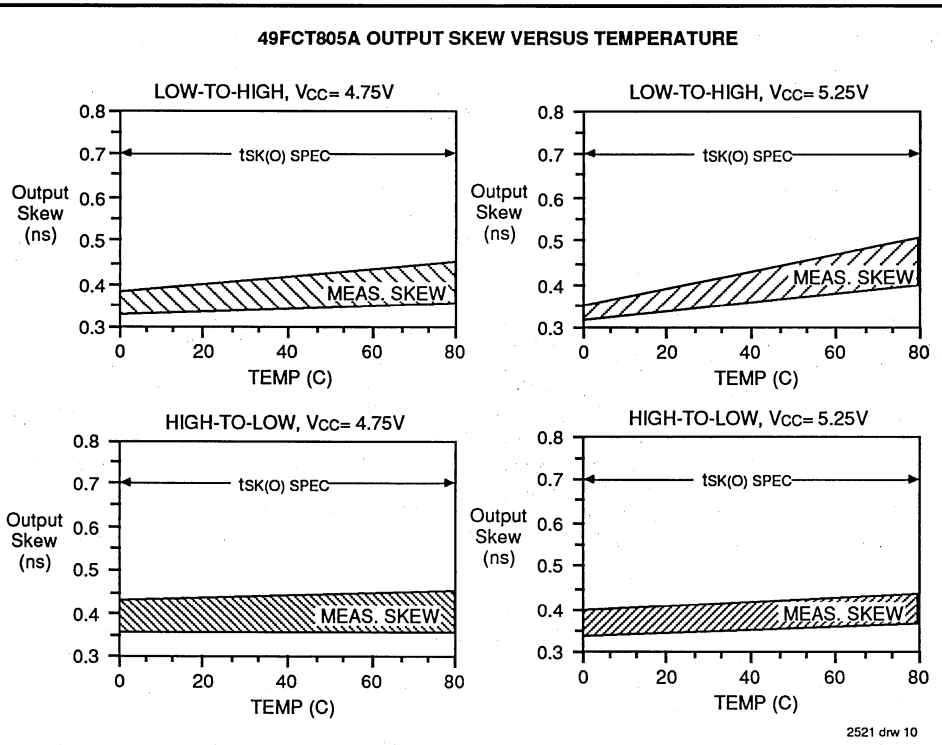


Figure 10. Measured Output Skew $t_{SK(O)}$ for Several IDT49FCT805As over the Operating Range

the graphs show that output skew is maximum at hot temperature (70°C). In each case the skew is well below the data sheet specification of 700ps.

Figure 11 shows the range of pulse skew measurements with Vccs of 4.75 and 5.25 volts. The measured pulse skew peaks at hot temperature and is slightly greater for a Vcc of 4.75V. The measured performance is safely within the data sheet specification of 1.0ns.

Figure 12 shows the range of package skew measurements for low-to-high and high-to-low transitions with Vccs of 4.75 and 5.25 volts. For both low-to-high and high-to-low transitions the skew peaks at hot temperature with minimal differences between low and high Vcc. Again the measured performance easily meets the data sheet specification of 1.5ns.

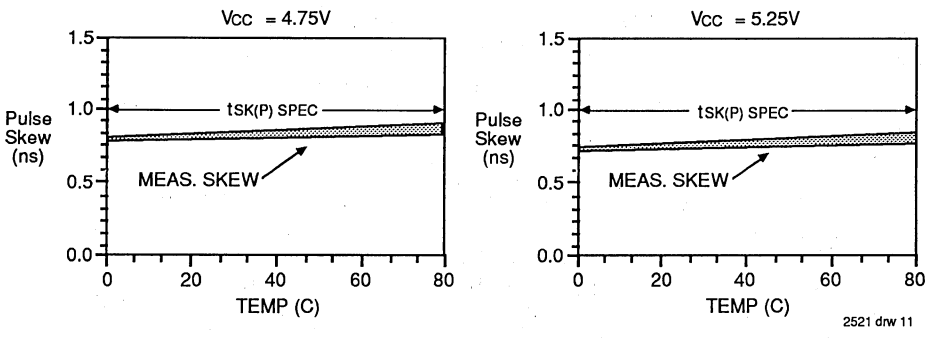


Figure 11. Measured Pulse Skew $t_{SK(P)}$ for Several IDT49FCT805As over the Operating Range

CLOCK DISTRIBUTION SIMPLIFIED

To show how easy it is to design with the IDT49FCT805, consider a hypothetical clock distribution system. The system has a 50Mhz clock source and must drive 75 loads. Each load is a CMOS input connected by 70Ω micro-strip trace at a density of 1 load every 0.5 inches. Assume that all the inputs are positive edge triggered and the objective is to minimize skew.

One approach would be to drive all 75 inputs with a single clock driver output (Figure 13). There are many problems with this approach. The first problem is the large amount capacitance associated with 75 CMOS inputs. Assuming 10pF maximum of capacitance per CMOS input, the total capacitive load is 750pF. A standard clock driver such as the IDT74FCT244A has Δt_{PLH} of 2ns/100pF for loads above 50pF. If the IDT74FCT244A is used the capacitance alone adds up to 14ns of additional propagation delay. If 75 loads are distributed along a single trace, the trace length is 38 inches (75 X 0.5 inputs/inch). If the PCB trace has an intrinsic delay of 0.15ns/inch (1), the delay from point B to point C is 5.7ns (38" X 0.15 ns/inch). Using a loaded trace delay of 0.37ns/inch (1), the skew between the ends of the trace approaches 15ns (38" X 0.37ns/inch). Given a 20ns cycle time (40 MHz), 14ns of clock skew implies that 70% of the clock cycle is given to clock distribution.

A second approach is the clock tree shown in Figure 14. By adding a level of buffers between the clock source and the 75 loads, the capacitive loading on the buffer outputs is reduced from 750pF to 50pF and the amount of PCB trace associated with each driver is reduced to 2.5". If IDT74FCT244As are used at least three packages (8 drivers per package) will be required. Since the 244's do not specify skew the designer might assume that each device output will switch within a 3.3ns window (t_{PHLmax}-t_{PHLmin}= 4.8ns -1.5ns). If the output transitions at points B, C, and D occur within a 3.3ns window, then the outputs of the second level (point E) may occur within a 6.6ns window. Assuming a 20ns cycle time (50Mhz) the designer has lost 33% of the cycle time to clock distribution without even considering transmission line effects.

A third approach is to use IDT49FCT805As as shown in Figure 15. Since each group of six buffers in Figure 14 can be replaced by 1/2 of an IDT49FCT805, only two devices are

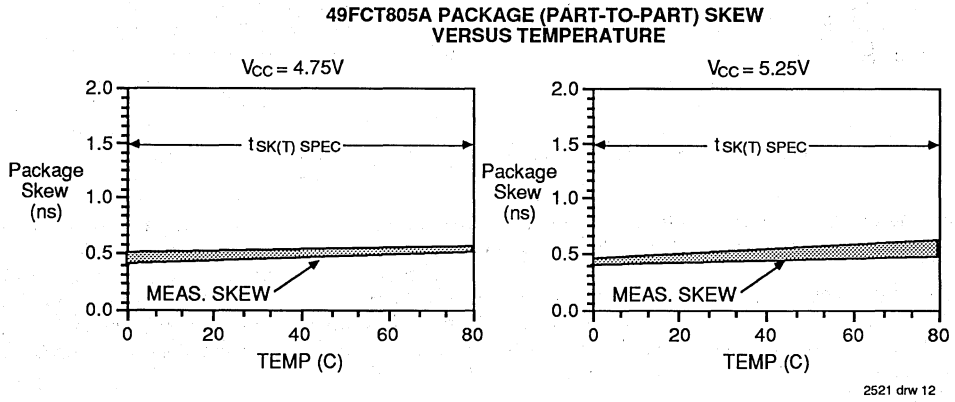


Figure 12. Measured Output Skew $t_{SK(T)}$ for Several IDT49FCT805As over the Operating Range

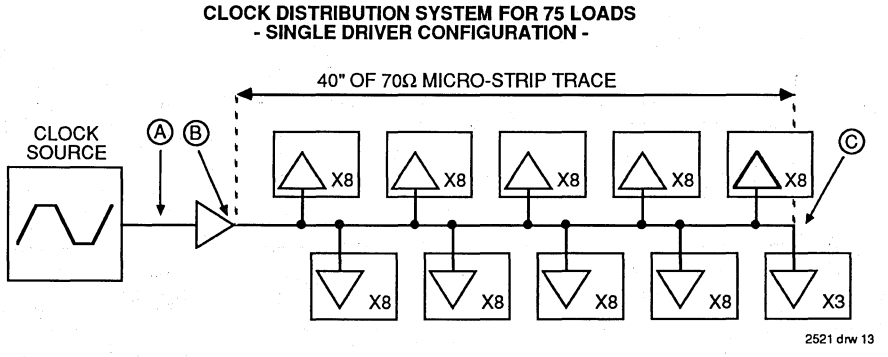


Figure 13. Single Driver Clock Distribution System

CLOCK DISTRIBUTION SYSTEM FOR 75 LOADS
- CLOCK DRIVER TREE CONFIGURATION -

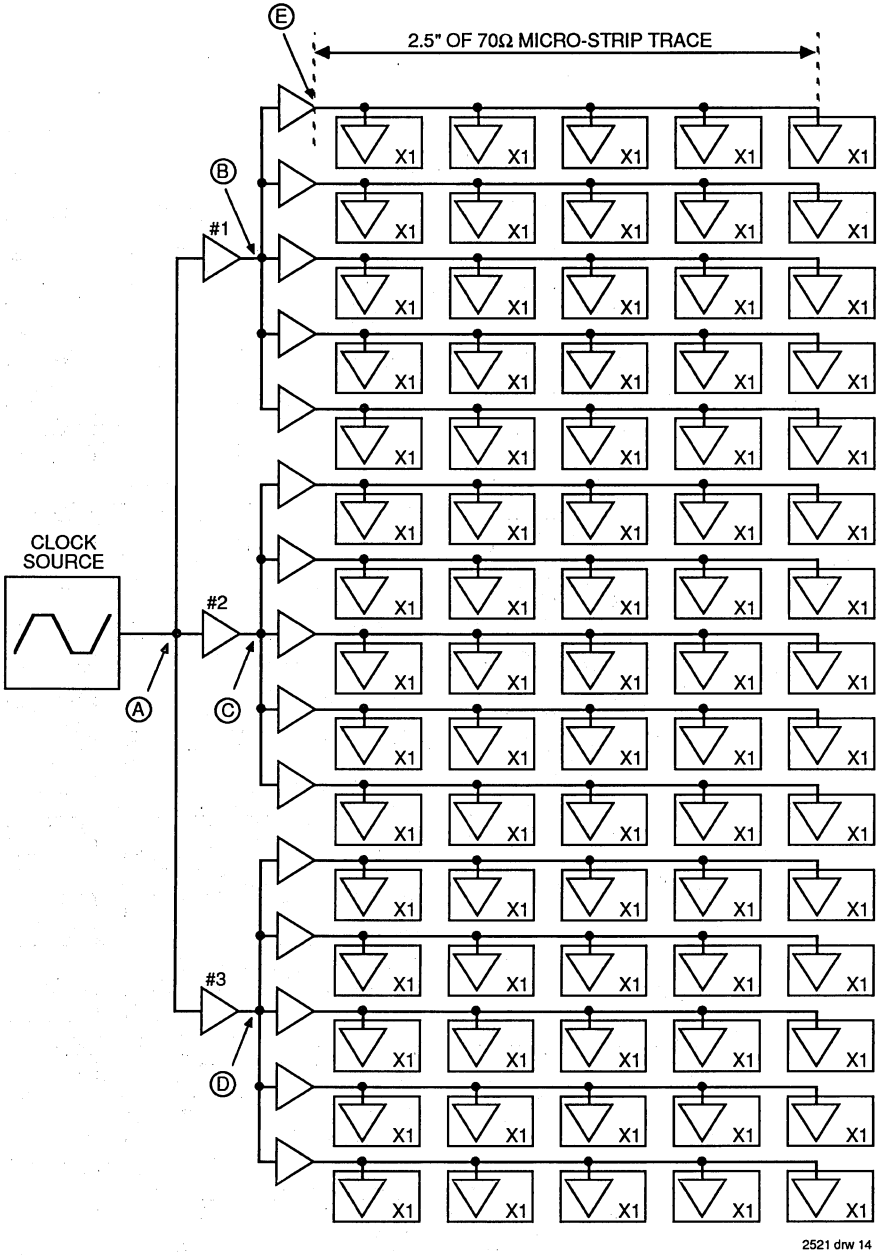


Figure 14. Clock Tree Distribution System Using 244's

CLOCK DISTRIBUTION SYSTEM FOR 75 LOADS
- CLOCK DRIVER TREE CONFIGURATION -

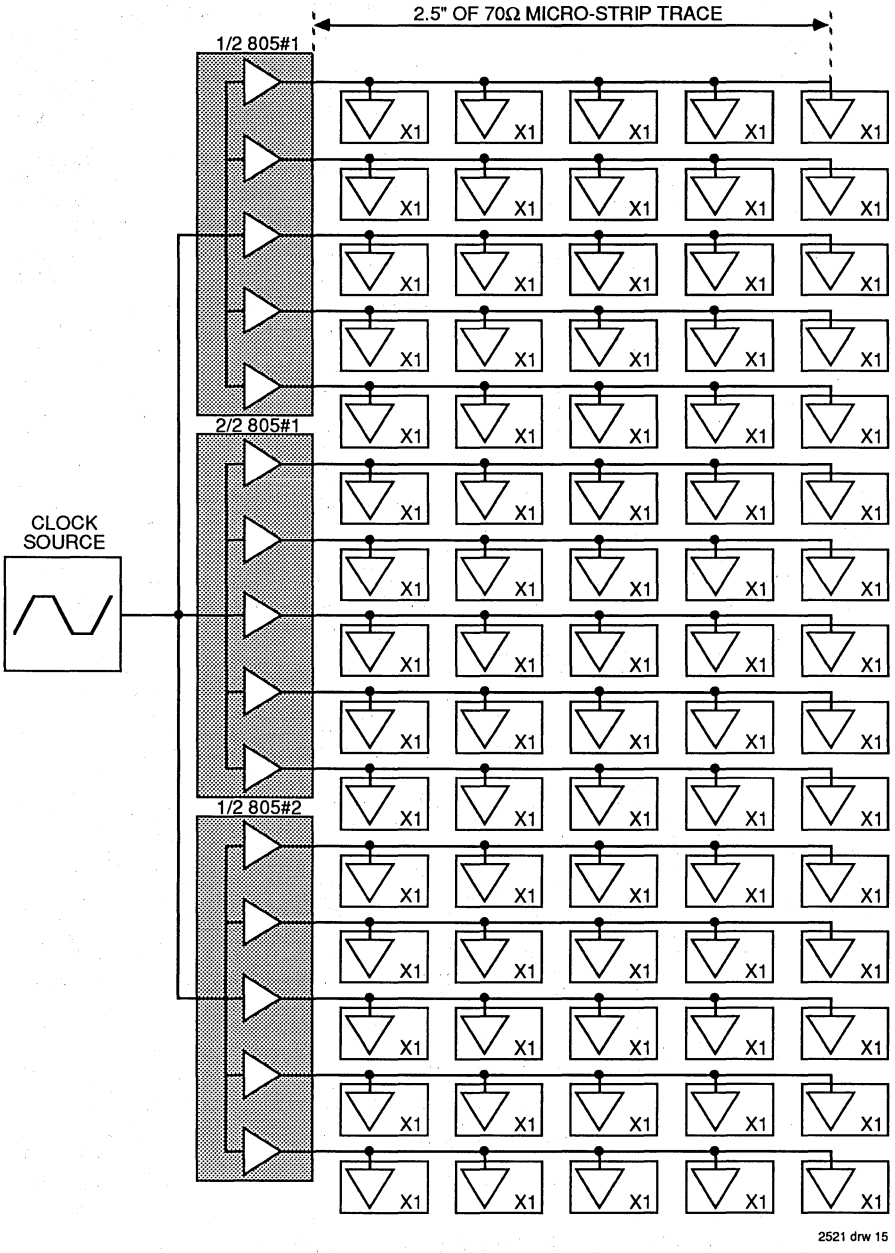


Figure 15. Clock Tree Distribution System Using IDT49FCT805's

required to implement the design. Using the 1.5ns package skew specification reduces the 6.6ns skew window to a 1.5ns skew window. If 0.925ns of loaded trace delay (2.5" X 0.37 ns/inch) is considered the maximum skew is 2.425ns including a 1st order treatment of transmission line effects. For a 20ns cycle time, the penalty imposed by the clock distribution system is reduced to 12% of the cycle time including transmission line effects. Besides reducing the size of the skew window of the second approach by 77%, the IDT49FCT805 increases the level of integration associated with the clock distribution tree. A significant benefit is the reduced loading on previous stages. Reduced loading helps minimize skew and makes the termination of clock lines clean and simple. The reduced chip count also saves valuable board space and simplifies the layout of the board.

SUMMARY

The following features of the IDT49FCT805/806 address clock driver skew and clock distribution problems:

- Circuit design, chip layout, and pin configuration specifically designed for very low output, pulse and package skew.
- Independent power and ground pins for reduced ground bounce and dynamic threshold shift.
- High current drive capability for driving heavily loaded/terminated PCB traces.
- 1:5 input/output ratio for reduced loading on previous stages.
- 11 outputs reduce the need for additional drivers—saves board space and simplifies PCB layout.
- Multiple grounds and Vccs to minimize ground bounce effects on propagation delay and skew.
- Input Hysteresis for increased immunity to system noise.
- Available in SOICs for increased packing density and reduced lead inductance.

RECOMMENDATIONS

To realize the performance benefits offered by the IDT49FCT805/806 clock drivers, IDT recommends the following high speed design practices:

- Use low impedance power and ground planes.
- Keep loading balanced and light.
- Keep trace lengths short, avoiding sharp bends and discontinuities (eg. use two 45° bends vs one 90° bend).
- Decouple both Vcc pins with a combination of capacitors (0.1μF and 0.01μF or 0.005μF) for effective high frequency filtering.
- Use termination for signal lines longer than 3 inches.
- Only use parts of same speed grade (non-A or A speed).

CONCLUSIONS

Clock skew is an important design consideration in today's high-speed systems. For successful and reliable operation, the clock skew must be kept within an acceptably small fraction of the system clock period. The IDT49FCT805 and IDT49FCT806 simplify the design of minimum skew clock distribution networks by specifying guaranteed low-skew performance. The skew specifications allow system designers to control the clock skew at each stage of the design which simplifies the problem of meeting global system requirements. With the IDT49FCT805/806 clock driver and a design methodology that pays close attention to high-speed design issues, maximum system performance can be achieved without risking reliability.

REFERENCES

(1) "Application Note AN-49", High-Speed CMOS Logic Design Guide, Integrated Device Technology Corp., November 1989.

A

Integrated Device Technology, Inc.

IDT49FCT804 TRI-PORT BUS MULTIPLEXER (BUSMUX™)

APPLICATION NOTE AN-84

by Kiran Kapshikar

INTRODUCTION

There is an obvious trend to push the performance of microprocessor-based systems by operating the processors at faster clock rates. Clock speeds of 33MHz are now becoming common-place with 40MHz and 50MHz CPUs just around the corner. To build efficient systems around these processors, the designer needs high performance interface logic, which combines both the speed (propagation delay) and intelligent integration to eliminate speed bottlenecks.

One example of such a requirement is the processor-to-DRAM interface. A DRAM has multiplexed address lines. The processor address must be latched and then multiplexed on the DRAM address bus. The propagation delays involved in this interface determine the overall access time and therefore the maximum rate of data transfer. By integrating the components used in the processor-to-DRAM interface, one can achieve improved performance as well as space savings. The IDT49FCT804 Bus Multiplexer is an interface element that provides an efficient solution for the processor-to-DRAM interface.

This introductory application note describes the features of the IDT49FCT804 Bus Multiplexer and its use in several practical applications.

IDT49FCT804 FEATURES

The IDT49FCT804 is a high speed, three port, Bus Multiplexer (BUSMUX™). The block diagram of the device is shown in Figure 1.

Each port is 10-bits wide which provides 25% extra addressing capability when compared to byte-oriented components. Bidirectional data transfer is possible between any two ports under the control of path selection logic (S0, S1) and direction control logic (Dxx). The latch inputs ($\overline{LE}x$) facilitate asynchronous storage of the incoming data. Each port has a separate tri-state control ($\overline{OE}x$). The BUSMUX is offered in three different speed grades to meet the diverse needs of the design community. All the outputs have 48/-15mA I_{OL}/I_{OH} capability to drive large capacitive loads without significant performance degradation.

The BUSMUX offers significant space savings and speed performance benefit over a discrete implementation of the same function. To implement the BUSMUX functionality we need at least three 10-bit latched transceivers plus control logic. If an 8-bit version of the BUSMUX is built using FCT543T (SOIC package), it will occupy at least 22% more space (IDT49FCT804 in PLCC) and will be 40% slower (port to port delay) compared to the IDT49FCT804. The device is ideal for inter-bus communication in a multiple bus environment as shown in the some of the typical applications.

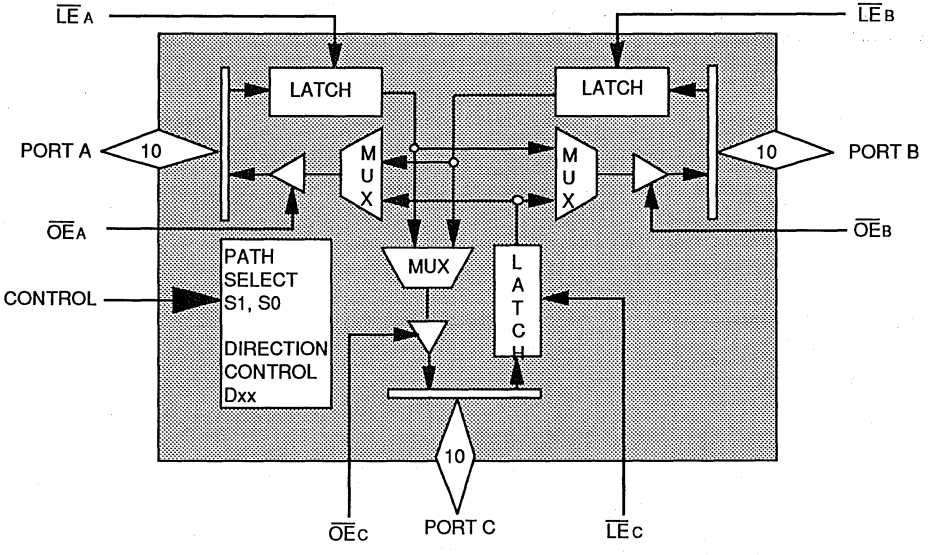


Figure 1. Block Diagram of the IDT49FCT804

IDT49FCT804 APPLICATIONS

In this section, we describe some of the typical applications using the IDT49FCT804. These applications show a variety of processor-to-memory interface configurations.

SHARED RAM APPLICATION

Figure 2A shows the block diagram of two processors P1 and P2 sharing a common memory bank. Figure 2B shows the detailed implementation using the BUSMUX. One set of IDT49FCT804 Bus Multiplexers is used for multiplexing addresses from P1 and P2. The address buses from the two processors are connected to A and C ports, respectively. The B port serves as the memory address bus. Address from A or C ports is routed to B port under the control of SO, which receives its input from an external arbiter/decoder PAL (S1 = 0 and DAB = DCB = 1).

The other set of IDT49FCT804 multiplexers route data between the processor data buses connected to A and C ports and the memory data bus connected to the B port. Again, the control input S0 selects the proper data bus. Inputs DAB and DCB provide direction control for READ and WRITE operations. This scheme uses less components and control logic as compared to an implementation using discrete latches and transceivers.

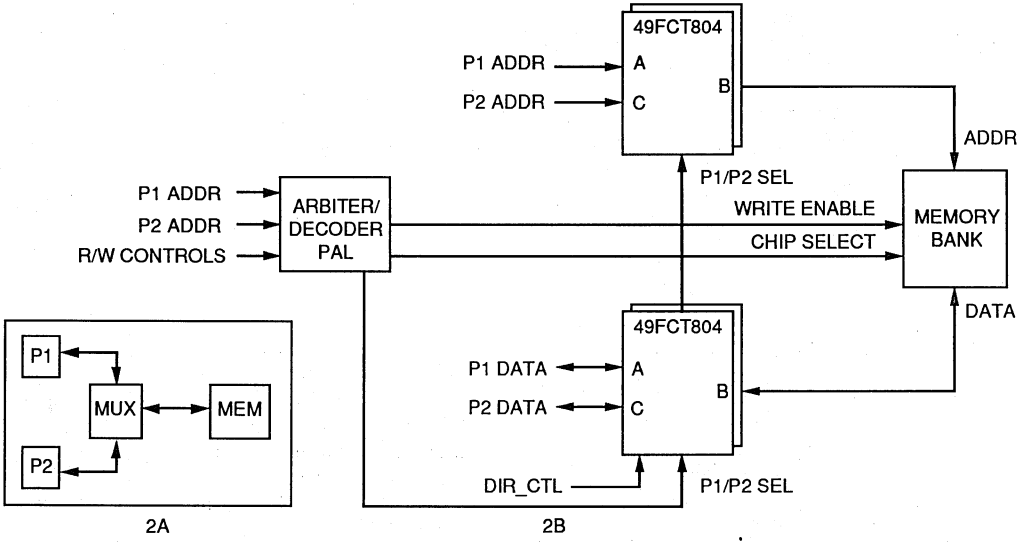


Figure 2. Shared RAM Application

A

DRAM ADDRESS MULTIPLEXER APPLICATION

Figure 3A shows the block diagram of the DRAM address path with multiplexed row and column addressing. Figure 3B shows the details of this scheme using the BUSMUX.

The IDT49FCT804 is well suited for latching the address and passing it to the DRAM. The row address lines of the processor are connected to the A port and the column address lines are connected to the C port. All address signals are latched simultaneously in the A and C port input latches. Under the control of path selection input S0 (S1 = LOW), the row and column addresses are sent sequentially to the DRAM array. The key advantages of this implementation are the reduced component count and fast operation.

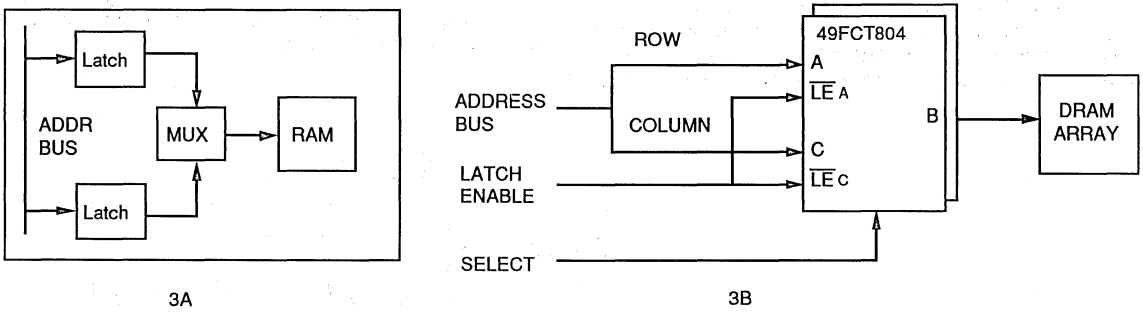


Figure 3. DRAM Address Multiplexing

INTERLEAVED DRAM DATA PATH APPLICATION

Figure 4A shows the block diagram of the data path for an interleaved memory using the BUSMUX. Figure 4B shows the details of the scheme. Two DRAM banks are organized as an even bank and an odd bank. The outputs of these two banks are multiplexed through the IDT49FCT804 on the system data bus. The data pins of the even bank and odd bank are connected to A and C ports, respectively. The B port is connected to the system data bus.

Under the control of the path selection input S0 (S1 = LOW) and the direction control signals, DAB and DCB, data is transferred between the processor data bus and the two memory banks. This implementation uses less components and control logic than a discrete implementation using transceivers.

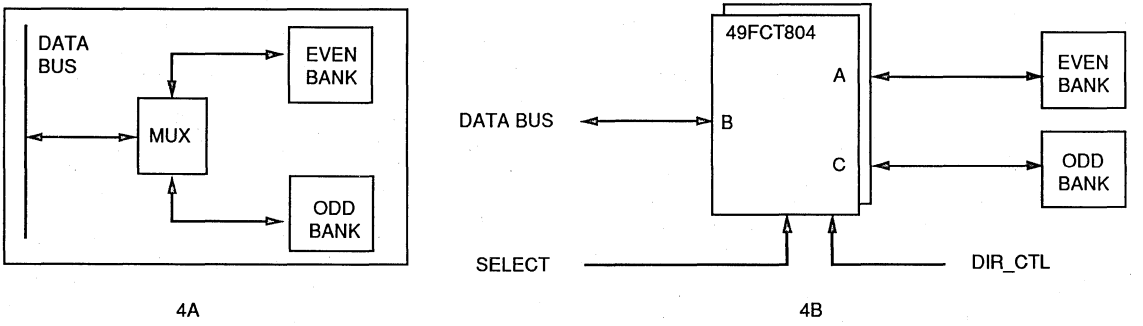


Figure 4. Interleaved Memory Data Path Application

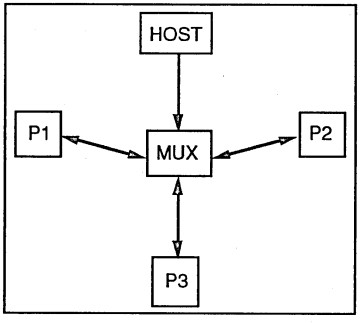
MULTIPROCESSOR SYSTEM DATA COMMUNICATION APPLICATION

Figure 5A shows the block diagram of a multiprocessor (P1, P2 and P3) system coupled through the BUSMUX. The scheme is explained in detail in Figure 5B. The three processors are operating in parallel. There is a central host processor which divides the problem into parallel segments and allocates the code and data among the three processors. Eventually, the three processors need to communicate with each other to pass and update the results. The BUSMUX is used as the communication channel.

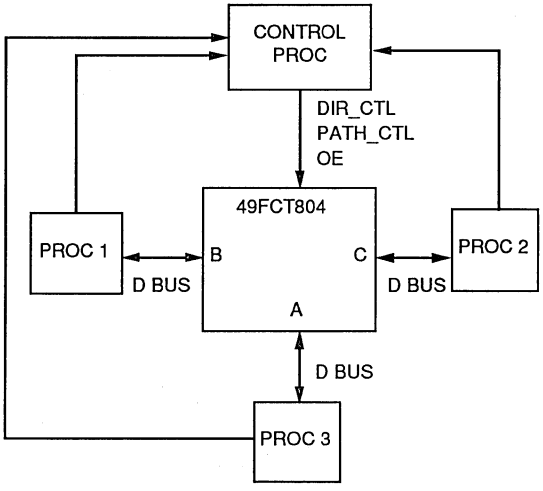
The host processor controls the arbitration between the three processor requests and achieves transfer of the data by applying the proper signals to the BUSMUX. The key advantages of this scheme are reduced component count leading to a compact layout and fast operation.

CONCLUSION

The IDT49FCT804 three-port BUSMUX is ideally suited for applications involving inter-bus communication. The key benefits of using the BUSMUX are simplified system design, ease of control, savings in space and power dissipation and an overall improvement in the system performance.



5A



5B

Figure 5. Multiprocessor System Application

A

1991 DATA BOOK UPDATE 1
TABLE OF CONTENTS

The following section contains partial data sheets that appeared in the 1991 SPECIALIZED MEMORIES Data Book. These data sheets had changes to less than 50% of the overall contents. Refer to the bars above changes to see where that section can be found in the 1991 SPECIALIZED MEMORIES Data Book.

IDT10/100/101484 — Data Book B, Section 5.1, Page 8

AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10484S7 100484S7 101484S7		10484S8 100484S8 101484S8		10484S10 100484S10 101484S10		10484S15 100484S15 101484S15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle											
tW	Write Pulse Width	tWSA = minimum	6	–	7	–	8	–	10	–	ns

IDT10/100/101A484 — Data Book B, Section 5.2, Page 7

AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10A484S5 100A484S5 101A484S5		10A484S7 100A484S7 101A484S7		10A484S8 100A484S8 101A484S8		10A484S10 100A484S10 101A484S10		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle											
tACS	Chip Select Access Time	–	–	2.5	–	3	–	5	–	5	ns
tRCS	Chip Select Recovery Time	–	–	2.5	–	3	–	5	–	5	ns

IDT10/100/101A484 — Data Book B, Section 5.2, Page 8

AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10A484S5 100A484S5 101A484S5		10A484S7 100A484S7 101A484S7		10A484S8 100A484S8 101A484S8		10A484S10 100A484S10 101A484S10		Unit
			Mlin.	Max.	Mlin.	Max.	Mlin.	Max.	Mlin.	Max.	
Write Cycle											
tW	Write Pulse Width	tWSA= minimum	4	–	6	–	7	–	8	–	ns

IDT10/100/101490 — Data Book B, Section 5.3, Page 8

AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10490S8 100490S8 101490S8		10490S10 100490S10 101490S10		10490S12 100490S12 101490S12		10490S15 100490S15 101490S15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle											
tW	Write Pulse Width	tWSA = minimum	7	–	9	–	10	–	10	–	ns
tWHD	Data Hold Time	–	1	–	1	–	2	–	3	–	ns
tWHA	Address Hold Time	–	1	–	1	–	2	–	3	–	ns
tWHCS	Chip Select Hold Time	–	1	–	1	–	2	–	3	–	ns

IDT10/100/101496RL · Data Book B, Section 5.6, Page 8

AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10496RL10 100496RL10 101496RL10		10496RL12 100496RL12 101496RL12		10496RL15 100496RL15 101496RL15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle									
tWL	Clock Low Pulse Width	–	5	–	5	–	6	–	ns
tWH	Clock High Pulse Width	–	5	–	5	–	6	–	ns

IDT10/100/101496RL Data Book B, Section 5.6, Page 9

AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10496RL10 100496RL10 101496RL10		10496RL12 100496RL12 101496RL12		10496RL15 100496RL15 101496RL15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle[2]									
tHWE	Hold Time for Write Enable	–	2.5	–	2.5	–	2.5	–	ns
tHD	Hold Time for Data In	–	2.5	–	2.5	–	2.5	–	ns

IDT10/100/101506RL Data Book B, Section 5.11, Page 8

AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10506RLA12		10506RLA15		Unit
			Min.	Max.	Min.	Max.	
Read Cycle							
tSA	Setup Time for Address	—	2.5	—	2.5	—	ns
tHCS	Hold Time for Chip Select	—	2	—	2	—	ns
tHA	Hold Time for Address	—	2	—	2	—	ns
tDR	Data Ready from Clock Low	—	0	4	0	4	ns

B

IDT7251/7252/72510/72520 Data Book B, Section 6.19, Page 15

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	IDT7251L IDT7252L IDT72510L IDT72520L Commercial t_A = 35, 40, 50, 80ns			IDT7251L IDT7252L IDT72510L IDT72520L Military t_A = 40, 50, 80ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{CC2}[3]	Average Standby Current ($\overline{FB}$ = $\overline{WB}$ = $\overline{DSA}$ = V_{IH})	—	15	30	—	24	50	mA

NOTES:

1. Measurements with 0.4V ≤ V_{IN} ≤ V_{CC}, $\overline{DSA}$ = $\overline{DSB}$ ≥ V_{IH}. 2. Measurements with 0.4V ≤ V_{OUT} ≤ V_{CC}, $\overline{DSA}$ = $\overline{DSB}$ ≥ V_{IH}. 3. Masurements are made with outputs open. Tested at f = 20 MHz

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V±10%, T_A = -55°C to +125°C)

		Commercial		Commercial and Military							
		IDT7251L35 IDT7252L35 IDT72510L35 IDT72520L35		IDT7251L40 IDT7252L40 IDT72510L40 IDT72520L40		IDT7251L50 IDT7252L50 IDT72510L50 IDT72520L50		IDT7251L80 IDT7252L80 IDT72510L80 IDT72520L80			Timing
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Figure
t_{aDH} [1]	Data hold time	0	—	5	—	5	—	10	—	ns	11, 12, 14, 15

NOTE:

1. The minimum data hold time is 5ns (10ns for the 80ns speed grade) when writing to the Command or Configuration registers.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V±10%, T_A = -55°C to +125°C)

		Commercial		Commercial and Military							
		IDT7251L35 IDT7252L35 IDT72510L35 IDT72520L35		IDT7251L40 IDT7252L40 IDT72510L40 IDT72520L40		IDT7251L50 IDT7252L50 IDT72510L50 IDT72520L50		IDT7251L80 IDT7252L80 IDT72510L80 IDT72520L80			Timing
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Figure
t_{bDH1}	Data hold time with no parity	0	—	5	—	5	—	10	—	ns	13, 14, 15
t_{bDH2}	Data hold time with parity	0	—	5	—	5	—	10	—	ns	13, 14, 15
t_{bA1}	Port B access time with no parity	—	40	—	45	—	55	—	85	ns	17
t_{bA2}	Port B access time with parity	—	42	—	48	—	60	—	90	ns	17

AC ELECTRICAL CHARACTERISTICS

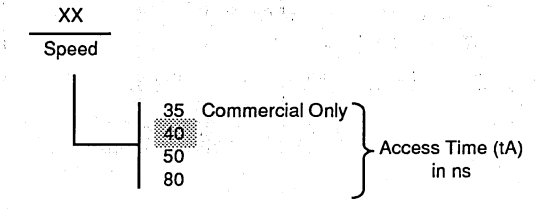
(Commercial: Vcc = 5V±10%, TA = 0°C to +70°C; Military: Vcc = 5V±10%, TA = -55°C to +125°C)

Symbol	Parameter	Commercial		Commercial and Military						Unit	Timing Figure
		IDT7251L35 IDT7252L35 IDT72510L35 IDT72520L35		IDT7251L40 IDT7252L40 IDT72510L40 IDT72520L40		IDT7251L50 IDT7252L50 IDT72510L50 IDT72520L50		IDT7251L80 IDT7252L80 IDT72510L80 IDT72520L80			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
BYPASS TIMING											
tBYD	Bypass delay	—	15	—	20	—	20	—	30	ns	16
taBYDV	Bypass data valid time from $\overline{DS_A}$	15	—	15	—	15	—	15	—	ns	16
tbBYDV (3)	Bypass data valid time from $\overline{DS_B}$	3	—	3	—	3	—	3	—	ns	16
FLAG TIMING											
tREF	Read clock edge to Empty Flag asserted	—	35	—	40	—	45	—	60	ns	14, 15, 20, 22
tWEF	Write clock edge to Empty Flag not asserted	—	35	—	40	—	45	—	60	ns	14, 15, 20, 22
tRFF	Read clock edge to Full Flag not asserted	—	35	—	40	—	45	—	60	ns	14, 15, 21, 23
tWFF	Write clock edge to Full Flag asserted	—	35	—	40	—	45	—	60	ns	14, 15, 21, 23
tRAEF	Read clock edge to Almost-Empty Flag asserted	—	50	—	55	—	60	—	75	ns	20, 22
tWAEF	Write clock edge to Almost-Empty Flag not asserted	—	50	—	55	—	60	—	75	ns	20, 22
tRAFF	Read clock edge to Almost-Full Flag not asserted	—	50	—	55	—	60	—	75	ns	21, 23
tWAFF	Write clock edge to Almost-Full Flag asserted	—	50	—	55	—	60	—	75	ns	21, 23

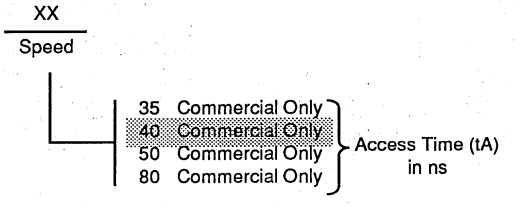
B

ORDERING INFORMATION

IDT7251/7252



IDT72510/72520



PIN DISCRIPTION

Symbol	Name	I/O	Description
R/$\overline{W}$A	Read/Write A	I	This pin controls the read or write direction of Port A. When $\overline{CS}$A is LOW and R/$\overline{W}$A is HIGH, data is read from Port A on the falling edge of $\overline{DS}$A. When $\overline{CS}$A is LOW and R/$\overline{W}$A is LOW, data is written into Port A on the rising edge of $\overline{DS}$A.

DC ELECTRICAL CHARACTERISTICS

(Commercial: VCC = 5V ± 10%, TA = 0°C to +70°C; Military: VCC = 5V ± 10%, TA = -55°C to +125°C)

Symbol	Parameter	IDT72511L IDT72521L Commercial tA = 35, 40, 50, 80ns			IDT72511L IDT72521L Military tA = 40, 50, 80ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
ICC2(3)	Average Standby Current ($\overline{R}$B = $\overline{W}$B = $\overline{DS}$A = VIH)	—	16	30	—	24	50	mA

NOTES:

3. Measurements are made with outputs open. Tested at f = 20 MHz.

AC ELECTRICAL CHARACTERISTICS

(Commercial: VCC = 5V ± 10%, TA = 0°C to + 70°C; Military: VCC = 5V ± 10%, TA = -55°C to + 125°C)

Symbol	Parameter	Commercial IDT72511L35 IDT72521L35		Commercial and Military IDT72511L40 IDT72521L40		IDT72511L50 IDT72521L50		IDT72511L80 IDT72521L80		Unit	Timing Figure
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
taDH(1)	Data hold time	2	—	5	—	5	—	10	—	ns	11, 12, 14, 15

NOTE:

1. The minimum data hold time is 5ns (10ns for the 80ns speed grade) when writing to the Command or Configuration registers.

AC ELECTRICAL CHARACTERISTICS

(Commercial: VCC = 5V ± 10%, TA = 0°C to + 70°C; Military: VCC = 5V ± 10%, TA = -55°C to + 125°C)

Symbol	Parameter	Commercial IDT72511L35 IDT72521L35		Commercial and Military IDT72511L40 IDT72521L40		IDT72511L50 IDT72521L50		IDT72511L80 IDT72521L80		Unit	Timing Figure
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
tbDH	Data hold time	2	—	5	—	5	—	10	—	ns	13, 14, 15
tbA	Port B access time	—	40	—	45	—	55	—	85	ns	17

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to + 70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to + 125°C)

		Commercial		Commercial and Military							
		IDT72511L35 IDT72521L35		IDT72511L40 IDT72521L40		IDT72511L50 IDT72521L50		IDT72511L80 IDT72521L80			Timing
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Figure
PROGRAMMABLE I/O TIMING											
t_{PIOS}	Programmable I/O set-up time	10	—	10	—	15	—	15	—	ns	19
t_{PIOH}	Programmable I/O hold time	10	—	10	—	15	—	15	—	ns	19
BYPASS TIMING											
t_{BYD}	Bypass delay	—	15	—	20	—	20	—	30	ns	16
t_{aBYDV}	Bypass data valid time from $\overline{DS_A}$	15	—	15	—	15	—	15	—	ns	16
t_{bBYDV} [3]	Bypass data valid time from $\overline{DS_B}$	3	—	3	—	3	—	3	—	ns	16
FLAG TIMING											
t_{REF}	Read clock edge to Empty Flag asserted	—	35	—	40	—	45	—	60	ns	14, 15, 20, 22
t_{WEF}	Write clock edge to Empty Flag not asserted	—	35	—	40	—	45	—	60	ns	14, 15, 20, 22
t_{RFF}	Read clock edge to Full Flag not asserted	—	35	—	40	—	45	—	60	ns	14, 15, 21, 23
t_{WFF}	Write clock edge to Full Flag asserted	—	35	—	40	—	45	—	60	ns	14, 15, 21, 23
t_{RAEF}	Read clock edge to Almost-Empty Flag asserted	—	50	—	55	—	60	—	75	ns	20, 22
t_{WAEF}	Write clock edge to Almost-Empty Flag not asserted	—	50	—	55	—	60	—	75	ns	20, 22
t_{RAFF}	Read clock edge to Almost-Full Flag not asserted	—	50	—	55	—	60	—	75	ns	21, 23
t_{WAFF}	Write clock edge to Almost-Full Flag asserted	—	50	—	55	—	60	—	75	ns	21, 23

B

ORDERING INFORMATION

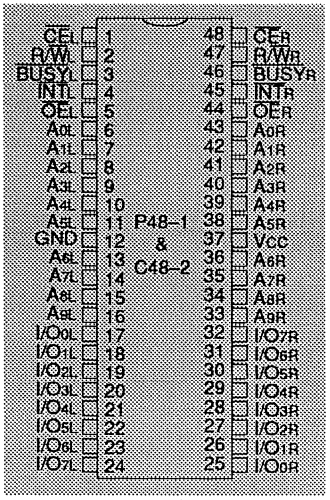
XX

Speed

35 Commercial Only
40
50
80

} Access Time (tA) in ns

PIN CONFIGURATIONS



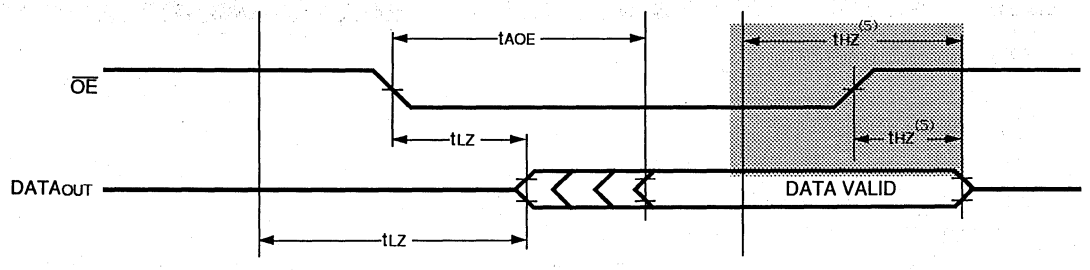
DIP
TOP VIEW

2690 drw 02

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7030 x 20[2] 7040 x 20[2] Typ.	Max.	7030 x 25 7040 x 25 Typ.	Max.	7030 x 35 7040 x 35 Typ.	Max.	7030 x 45[3] 7040 x 45[3] Typ.	Max.	Unit
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs, f = 0[5])	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open, f=f_{MAX}[4]	Mil.	SA	—	—	50	170	45	150	40	140	mA
				LA	—	—	46	135	42	115	35	105	
			Com'l.	SA	50	160	50	150	45	135	—	—	
				LA	46	125	46	115	42	105	—	—	

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE[1,3]



5. Specified for OE at high (refer to "Timing Waveform of Write Cycle", Note 7).

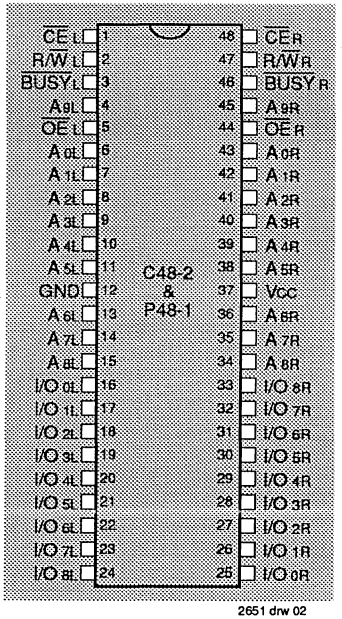
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[8]

Symbol	Parameter	7030 x 20[1,10] 7040 x 20[1,10] Min.	Max.	7030 x 25 7040 x 25 Min.	Max.	7030 x 35 7040 x 35 Min.	Max.	7030 x 45[2] 7040 x 45[2] Min.	Max.	Unit
Busy Timing (For Master IDT7030 Only)										
tDDD	Write Data Valid to Read Data Delay[3]	—	35	—	35	—	45	—	55	ns
Busy Timing (For Slave IDT7040 Only)										
tDDD	Write Data Valid to Read Data Delay[9]	—	35	—	35	—	45	—	55	ns

TABLE II – ARBITRATION[1,2]

Left Port		Right Port		Flags[1]		Function
$\overline{CE}_L$	A_{0L}-A_{9L}	$\overline{CE}_R$	A_{0R}-A_{9R}	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
LL5R	=A0R-A9R	LL5R	=A0L-A9L	H	L	L-Port Wins

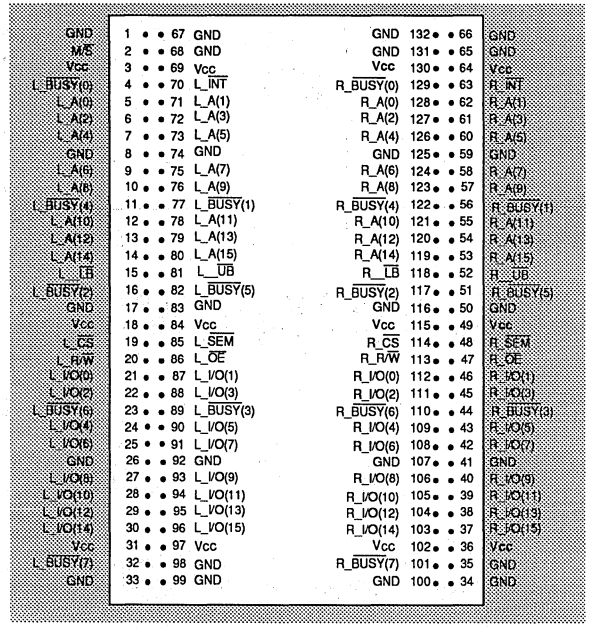
PIN CONFIGURATIONS



2651 drw 02

B

PIN CONFIGURATION (1, 2)



DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7MB1006 Min.	IDT7MB1006 Max.	IDT7MB1008 Min.	IDT7MB1008 Max.	Unit
V_{OL}	Output Low Voltage	V_{CC} = Min. I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min. I_{OH} = -4mA	2.4	—	2.4	—	V

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	IDT7MB1006SxxK or IDT7MB1008SxxK								Unit
		-25[5]		-30[5]		-35		-40		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	25	—	30	—	35	—	40	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	—	40	ns
t_{ACS}[2]	Chip Select Access Time	—	25	—	30	—	35	—	40	ns
t_{OE}	Output Enable Access Time	—	13	—	15	—	20	—	25	ns
t_{OH}	Output Hold From Address Change	3	—	3	—	3	—	3	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	3	—	3	—	3	—	3	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	18	—	20	—	20	—	20	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	3	—	3	—	3	—	3	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	18	—	20	—	20	—	20	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Disable to Power Down Time	—	50	—	50	—	50	—	50	ns
t_{SOP}	$\overline{SEM}$ Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	12	—	12	—	15	—	15	—	ns
t_{WC}	Write Cycle Time	25	—	30	—	35	—	40	—	ns
t_{CW}[2]	Chip Select to End of Write	20	—	25	—	30	—	35	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	30	—	35	—	ns
t_{AS1}[3]	Address Set-up to Write Pulse Time	5	—	5	—	5	—	5	—	ns
t_{AS2}	Address Set-up to $\overline{CS}$ Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	30	—	35	—	ns
t_{WR}[4]	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	15	—	20	—	25	—	30	—	ns
t_{DH}[4]	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	18	—	20	—	20	—	20	ns
t_{WHZ}[1]	Write Disable to Output in High Z	—	18	—	20	—	20	—	20	ns
t_{OW}[1, 4]	Output Active from End of Write	0	—	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	10	—	13	—	15	—	15	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	10	—	13	—	15	—	15	—	ns

B

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	IDT7MB1006SxxK or IDT7MB1008SxxK -50 Min.	-50 Max.	-65 Min.	-65 Max.	-80 Min.	-80 Max.	Unit
Read Cycle								
t_{RC}	Read Cycle Time	50	—	65	—	80	—	ns
t_{AA}	Address Access Time	—	50	—	65	—	80	ns
t_{ACS}[2]	Chip Select Access Time	—	50	—	65	—	80	ns
t_{OE}	Output Enable Access Time	—	30	—	35	—	40	ns
t_{OH}	Output Hold From Address Change	3	—	3	—	3	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	3	—	3	—	3	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	25	—	30	—	35	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	3	—	3	—	3	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	25	—	30	—	35	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Disable to Power Down Time	—	50	—	50	—	50	ns
t_{SOP}	$\overline{SEM}$ Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	20	—	20	—	ns
Write Cycle								
t_{WC}	Write Cycle Time	50	—	65	—	80	—	ns
t_{CW}[2]	Chip Select to End of Write	40	—	50	—	55	—	ns
t_{AW}	Address Valid to End of Write	40	—	50	—	55	—	ns
t_{AS1}[3]	Address Set-up to Write Pulse Time	5	—	5	—	5	—	ns
t_{AS2}	Address Set-up to $\overline{CS}$ Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	40	—	45	—	50	—	ns
t_{WR}[4]	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	35	—	40	—	45	—	ns
t_{DH}[4]	Data Hold Time	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	25	—	30	—	35	ns
t_{WHZ}[1]	Write Disable to Output in High Z	—	25	—	30	—	35	ns
t_{OW}[1,4]	Output Active from End of Write	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	15	—	15	—	15	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	15	—	15	—	15	—	ns

NOTES:

2903 tbl 10

1. This parameter is guaranteed by design but not tested.
2. To access RAM $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
3. t_{AS1} = 0 if R/$\overline{W}$ is asserted low simultaneously with or after the $\overline{CS}$ low transition.
4. For $\overline{CS}$ controlled write cycles, t_{WR} = 5ns, t_{DH} = 5ns, t_{OW} = 5ns.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameters	IDT7MB1006SxxK or IDT7MB1008SxxK								Unit
		-25[11]		-30[11]		-35		-40		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{BUSY}$ Cycle - MASTER MODE[3]										
t_{BAA}	$\overline{BUSY}$ Access Time from Address	—	25	—	30	—	35	—	40	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address	—	20	—	25	—	30	—	35	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Select	—	20	—	25	—	30	—	35	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Select	—	20	—	25	—	30	—	30	ns
t_{APS}[6]	Arbitration Priority Set-up Time	5	—	5	—	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Time	—	Note 9	—	Note 9	—	Note 9	—	Note 9	ns
$\overline{BUSY}$ Cycle - Slave Mode[4]										
t_{WB}[7]	Write to $\overline{BUSY}$ Input	0	—	0	—	0	—	0	—	ns
t_{WH}[8]	Write Hold After $\overline{BUSY}$	15	—	20	—	25	—	25	—	ns
Port-to-Port Delay Timing										
t_{WDD}[5]	Write Pulse to Data Delay	—	50	—	55	—	60	—	65	ns
t_{DDD}[5]	Write Data Valid to Read Data Valid	—	35	—	40	—	45	—	50	ns
Interrupt Timing										
t_{AS}[10]	Address Set-up Time	5	—	5	—	5	—	5	—	ns
t_{WR}[10]	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	20	—	25	—	30	—	35	ns
t_{INR}	Interrupt Reset Time	—	20	—	25	—	30	—	35	ns

NOTES:

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1. This parameter is guaranteed by design but not tested.
2. To access RAM, $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
3. When the module is being used in the Master Mode ($M/\overline{S} \geq V_{IH}$).
4. When the module is being used in the Slave Mode ($M/\overline{S} \leq V_{IL}$).
5. Port-to-Port delay through the RAM cells from the writing port to the reading port.
6. To ensure that the earlier of the two ports wins.
7. To ensure that the write cycle is inhibited during contention.
8. To ensure that a write cycle is completed after contention.
9. t_{BDD} is a calculated parameter and is the greater of 0, t_{WDD} - t_{WP} (actual), or t_{DDD} - t_{WP} (actual).
10. If $\overline{CS}$ is used to control interrput, then t_{AS}=0 and t_{WR}= 5ns.
11. Preliminary specifications only.

B

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameters	IDT7MB1006SxxK or IDT7MB1008SxxK -50 Min.	-50 Max.	-65 Min.	-65 Max.	-80 Min.	-80 Max.	Unit
$\overline{BUSY}$ Cycle - MASTER MODE[3]								
t_{BAA}	$\overline{BUSY}$ Access Time from Address	—	50	—	55	—	55	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address	—	45	—	45	—	45	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Select	—	45	—	50	—	55	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Select	—	40	—	45	—	45	ns
t_{APS}[6]	Arbitration Priority Set-up Time	5	—	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Time	—	Note 9	—	Note 9	—	Note 9	ns
$\overline{BUSY}$ Cycle - Slave Mode[4]								
t_{WB}[7]	Write to $\overline{BUSY}$ Input	0	—	0	—	0	—	ns
t_{WH}[8]	Write Hold After $\overline{BUSY}$	25	—	30	—	30	—	ns
Port-to-Port Delay Timing								
t_{WDD}[5]	Write Pulse to Data Delay	—	70	—	85	—	95	ns
t_{DDD}[5]	Write Data Valid to Read Data Valid	—	55	—	70	—	80	ns
Interrupt Timing								
t_{AS}[10]	Address Set-up Time	5	—	5	—	5	—	ns
t_{WR}[10]	Write Recovery Time	0	—	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	45	—	45	—	55	ns
t_{INR}	Interrupt Reset Time	—	45	—	45	—	55	ns

2803 tbl 11

NOTES:

1. This parameter is guaranteed by design but not tested.
2. To access RAM, $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
3. When the module is being used in the Master Mode ($M/\overline{S} \geq V_{IH}$).
4. When the module is being used in the Slave Mode ($M/\overline{S} \leq V_{IL}$).
5. Port-to-Port delay through the RAM cells from the writing port to the reading port.
6. To ensure that the earlier of the two ports wins.
7. To ensure that the write cycle is inhibited during contention.
8. To ensure that a write cycle is completed after contention.
9. t_{BDD} is a calculated parameter and is the greater of 0, t_{WDD} - t_{WP} (actual), or t_{DDD} - t_{WP} (actual).
10. If $\overline{CS}$ is used to control interrput, then t_{AS}=0 and t_{WR}= 5ns.

PIN CONFIGURATION [1]

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	L_I/O(24)	L_I/O(26)	L_I/O(28)	L_I/O(30)	L_CS	L_OE	L_R/W(3)	R_OE	R_CS	R_I/O(30)	R_I/O(28)	R_I/O(26)	R_I/O(24)
B	L_I/O(23)	L_I/O(25)	L_I/O(27)	L_I/O(29)	L_I/O(31)	L_A(0)	L_R/W(4)	R_A(0)	R_I/O(31)	R_I/O(29)	R_I/O(27)	R_I/O(25)	R_I/O(23)
C	L_I/O(21)	L_I/O(22)	VCC	L_A(3)	L_A(2)	L_A(1)	GND	R_A(1)	R_A(2)	R_A(3)	GND	R_I/O(22)	R_I/O(21)
D	L_I/O(19)	L_I/O(20)	L_A(4)	GND							R_A(4)	R_I/O(20)	R_I/O(19)
E	L_I/O(17)	L_I/O(18)	L_A(5)								R_A(5)	R_I/O(18)	R_I/O(17)
F	L_SEM	L_I/O(16)	L_A(6)								R_A(6)	R_I/O(16)	R_SEM
G	L_BUSY	L_INT	GND				PGA TOP VIEW				GND	R_INT	R_BUSY
H	L_R/W(1)	L_R/W(2)	L_A(7)								R_A(7)	R_R/W(2)	R_R/W(1)
I	L_I/O(15)	L_I/O(14)	L_A(8)								R_A(8)	R_I/O(14)	R_I/O(15)
J	L_I/O(13)	L_I/O(12)	L_A(9)								R_A(9)	R_I/O(12)	R_I/O(13)
K	L_I/O(11)	M/S	GND	L_A(10)	L_A(11)	L_A(12)	GND	R_A(12)	R_A(11)	R_A(10)	VCC	GND	R_I/O(11)
L	L_I/O(10)	L_I/O(8)	L_I/O(6)	L_I/O(4)	L_I/O(2)	L_A(13)	R_R/W(4)	R_A(13)	R_I/O(2)	R_I/O(4)	R_I/O(6)	R_I/O(8)	R_I/O(10)
M	L_I/O(9)	L_I/O(7)	L_I/O(5)	L_I/O(3)	L_I/O(1)	L_I/O(0)	R_R/W(3)	R_I/O(0)	R_I/O(1)	R_I/O(3)	R_I/O(5)	R_I/O(7)	R_I/O(9)

NOTE:
1. For module dimensions, please refer to the module drawings in the packaging section.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

		-30[10]		-35[10]		-40		-45		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	30	—	35	—	40	—	45	—	ns
t_{AA}	Address Access Time	—	30	—	35	—	40	—	45	ns
t_{ACS}[2]	Chip Select Access Time	—	30	—	35	—	40	—	45	ns
t_{OE}	Output Enable Access Time	—	13	—	20	—	20	—	25	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	3	—	3	—	3	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	15	—	15	—	15	—	20	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	3	—	3	—	3	—	5	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	15	—	15	—	15	—	20	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Up Time	—	50	—	50	—	50	—	50	ns
t_{SOP}	Sem. Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	15	—	15	—	ns
Write Cycle										
t_{WC}	Write Cycle Time	30	—	35	—	40	—	45	—	ns
t_{CW}[2]	Chip Select to End of Write	25	—	30	—	35	—	40	—	ns
t_{AW}	Address Valid to End of Write	25	—	30	—	35	—	40	—	ns
t_{AS}	Address Set-Up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	30	—	35	—	35	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns

B

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	-30[10]		-35[10]		-40		-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle (continued)										
tDW	Data Valid to End of Write	20	—	25	—	25	—	25	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tOHZ[1]	Output Disable to Output in High Z	—	15	—	15	—	15	—	20	ns
tWHZ[1]	Write Disable to Output in High Z	—	15	—	15	—	15	—	20	ns
tOW[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	10	—	10	—	10	—	10	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	10	—	10	—	10	—	10	—	ns
Busy Cycle-Master Mode[3]										
tBAA	$\overline{BUSY}$ Access Time to Address	—	30	—	35	—	30	—	35	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	25	—	30	—	30	—	30	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Select	—	25	—	30	—	30	—	30	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Deselect	—	20	—	25	—	25	—	25	ns
tWDD[5]	Write Pulse to Data Delay	—	55	—	60	—	60	—	70	ns
tDDD	Write Data Valid to Read Data Delay	—	40	—	45	—	40	—	50	ns
tAPS[6]	Arbitration Priority Set-Up Time	5	—	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Time	—	NOTE 9	—	NOTE 9	—	NOTE 9	—	NOTE 9	ns
Busy Cycle-Slave Mode[4]										
tWB[7]	Write to BUSY Input	0	—	0	—	0	—	0	—	ns
tWH[8]	Write Hold after BUSY	20	—	25	—	25	—	25	—	ns
tWDD[5]	Write Pulse to Data Delay	—	55	—	60	—	60	—	70	ns
tDDD[5]	Write Data Valid to Read Data Valid	—	40	—	45	—	45	—	50	ns
Interrupt Timing										
tAS	Address Set-Up Time	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	25	—	30	—	30	—	35	ns
tINR	Interrupt Reset Time	—	25	—	30	—	30	—	35	ns

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 55°C to +125°C or 0°C to +70°C)

NOTE:
1. This parameter is guaranteed by design but not tested.
2. To access RAM, $\overline{CS} \le V_{IL}$ and $\overline{SEM} \ge V_{IH}$. To access semaphore, $\overline{CS} \ge V_{IH}$ and $\overline{SEM} \le V_{IL}$.
3. When the module is being used in the Master Mode ($M/\overline{S} \ge V_{IH}$).
4. When the module is being used in the Slave Mode ($M/\overline{S} \le V_{IL}$).
5. Port-to-Port delay through the RAM cells from the writing port to the reading port.
6. To ensure that the earlier of the two ports wins.
7. To ensure that the write cycle is inhibited during contention.
8. To ensure that a write cycle is completed after contention.
9. tBDD is a calculated parameter and is the greater of 0, tWDD - tWP (actual), or tDDD - tWP (actual).

DESCRIPTION:

The memory configuration results in a package 2.65 inches long and 0.35 inches wide. At only 0.5 inches high, this low profile package is ideal for high performance systems with minimum board spacing.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

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AC ELECTRICAL CHARACTERISTICS(2)

(VCC = 5.0V ± 10%, TA = 0°C to +70°C)

		7MP4034SxxZ												
		-15		-17		-20		-25		-35		-45		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
READ CYCLE														
tRC	Read Cycle Time	15	—	17	—	20	—	25	—	35	—	45	—	ns
tAA	Address Access Time	—	15	—	17	—	20	—	25	—	35	—	45	ns
tACS	Chip Select Access Time	—	15	—	17	—	20	—	25	—	35	—	45	ns
tCLZ (1)	Chip Select to Output in Low Z	3	—	3	—	3	—	5	—	5	—	5	—	ns
tCHZ (1)	Chip Deselect to Output in High Z	—	10	—	10	—	10	—	13	—	20	—	25	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	3	—	ns
tPU (1)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tPD (1)	Chip Deselect to Power Down Time	—	15	—	17	—	20	—	25	—	35	—	45	ns
WRITE CYCLE														
tWC	Write Cycle Time	15	—	17	—	20	—	25	—	35	—	45	—	ns
tCW	Chip Select to End of Write	12	—	15	—	17	—	22	—	30	—	40	—	ns
tAW	Address Valid to End of Write	13	—	15	—	17	—	22	—	30	—	40	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	13	—	15	—	17	—	22	—	30	—	40	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWHZ (1)	Write Enable to Output in High Z	—	8	—	9	—	10	—	13	—	20	—	25	ns
tDW	Data to Write Time Overlap	10	—	11	—	13	—	15	—	20	—	25	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tOW (1)	Output Active from End of Write	0	—	0	—	0	—	5	—	5	—	5	—	ns

B

AC ELECTRICAL CHARACTERISTICS[2] (V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameters	7MB4040SxxP -15 Min.	-15 Max.	-17 Min.	-17 Max.	-20 Min.	-20 Max.	-25 Min.	-25 Max.	-35 Min.	-35 Max.	Unit
Read Cycle												
t_{RC}	Read Cycle Time	15	—	17	—	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	15	—	17	—	20	—	25	—	35	ns
t_{ACS}	Chip Select Access Time	—	15	—	17	—	20	—	25	—	35	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	3	—	3	—	3	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	10	—	10	—	10	—	13	—	20	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Down Time	—	15	—	17	—	20	—	25	—	35	ns
Write Cycle												
t_{WC}	Write Cycle Time	15	—	17	—	20	—	25	—	35	—	ns
t_{CW}	Chip Selection to End of Write	12	—	15	—	17	—	22	—	30	—	ns
t_{AW}	Address Valid to End of Write	12	—	15	—	17	—	22	—	30	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	15	—	17	—	22	—	30	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	3	—	3	—	ns
t_{WHZ}[1]	Write Enable to Ouput in High Z	—	8	—	9	—	10	—	13	—	20	ns
t_{DW}	Data to Write Time Overlap	10	—	11	—	13	—	15	—	20	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	5	—	5	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. 15ns, 17ns are preliminary specifications.

2700 tbl 10

PIN CONFIGURATION[1]

NOTE:
1. For module dimension, please refer to the module drawings in the packaging section.

AC ELECTRICAL CHARACTERISTICS (Continued)

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameters	7MC4032S30		7MC4032S40		7MC4032S50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	30	—	40	—	50	—	ns
t_{AA}	Address Access Time	—	30	—	40	—	50	ns
t_{ACS}	Chip Select Access Time	—	30	—	40	—	50	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	20	—	22	—	30	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	13	—	17	—	18	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	17	—	17	—	18	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Down Time	—	30	—	40	—	50	ns
Write Cycle								
t_{WC}	Write Cycle Time	25	—	35	—	45	—	ns
t_{CW}	Chip Selection to End of Write	25	—	28	—	38	—	ns
t_{AW}	Address Valid to End of Write	25	—	30	—	40	—	ns
t_{AS}	Address Set-up Time	0	—	2	—	2	—	ns
t_{WP}	Write Pulse Width	25	—	28	—	38	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Ouput in High Z	—	10	—	12	—	17	ns
t_{DW}	Data to Write Time Overlap	15	—	17	—	23	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	5	—	ns

B

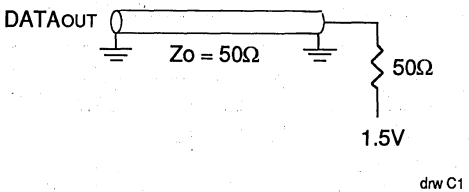


Figure 3. BiCMOS Output Load

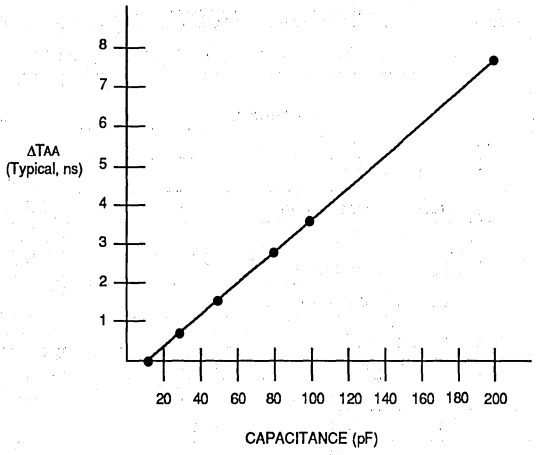


Figure 4. Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS

(VCC = 5V ± 10%, TA = 0°C TO +70°C)

Symbol	Parameter	7MP4031BxxZ -8[2] Min.	-8[2] Max.	-10[2] Min.	-10[2] Max.	-12 Min.	-12 Max.	Unit
Read Cycle								
tRC	Read Cycle Time	8	—	10	—	12	—	ns
tAA	Address Access Time	—	8	—	10	—	12	ns
tACS	Chip Select Access Time	—	8	—	10	—	12	ns
tCLZ1, 2[1]	Chip Select to Output in Low Z	3	—	3	—	3	—	ns
tOE	Output Enable to Output Valid	—	4	—	5	—	6	ns
tOLZ[1]	Output Enable to Output in Low Z	3	—	3	—	3	—	ns
tCHZ[1]	Chip Deselect to Output in High Z	—	6	—	6	—	7	ns
tOHZ[1]	Output Disable to Output in High Z	—	3	—	3	—	3	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
Write Cycle								
tWC	Write Cycle Time	8	—	10	—	12	—	ns
tCW	Chip Select to End of Write	8	—	8	—	9	—	ns
tAW	Address Valid to End of Write	8	—	10	—	12	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width	8	—	8	—	9	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tWHZ[1]	Write Enable to Output in High Z	—	3	—	3	—	3	ns
tDW	Data to Write Time Overlap	5	—	5	—	6	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	ns
tOW[1]	Output Active from End of Write	3	—	3	—	3	—	ns

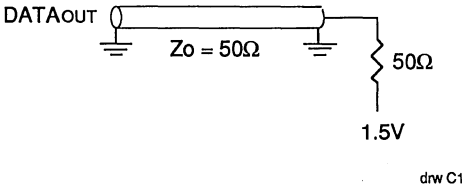


Figure 3. BiCMOS Output Load

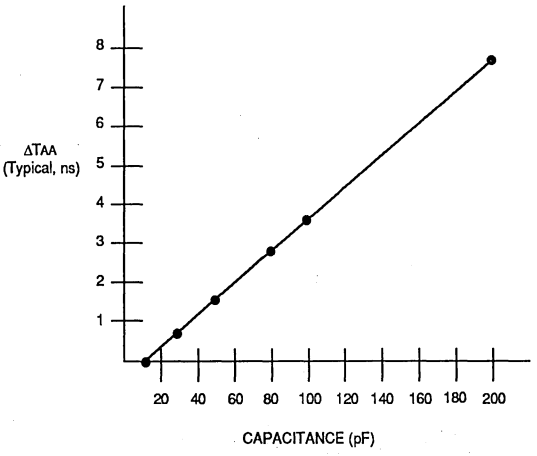


Figure 4. Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS

(VCC = 5V ±10%, TA = 0°C TO +70°C)

Symbol	Parameter	7MP4036BxxZ, 7MP4036BxxM								Unit
		-10[2]		-12[2]		-15		-17		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tRC	Read Cycle Time	10	—	12	—	15	—	17	—	ns
tAA	Address Access Time	—	10	—	12	—	15	—	17	ns
tACS	Chip Select Access Time	—	4	—	7	—	8	—	9	ns
tCLZ[1]	Chip Select to Output in Low Z	2	—	2	—	2	—	2	—	ns
tOE	Output Enable to Output Valid	—	4	—	5	—	6	—	8	ns
tOLZ[1]	Output Enable to Output in Low Z	2	—	2	—	2	—	2	—	ns
tCHZ[1]	Chip Deselect to Output in High Z	—	6	—	7	—	8	—	10	ns
tOHZ[1]	Output Disable to Output in High Z	—	3	—	4	—	5	—	6	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
Write Cycle										
tWC	Write Cycle Time	10	—	12	—	15	—	17	—	ns
tCW	Chip Select to End of Write	7	—	8	—	9	—	10	—	ns
tAW	Address Valid to End of Write	8	—	9	—	10	—	12	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	8	—	9	—	10	—	12	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tWHZ[1]	Write Enable to Output in High Z	—	4	—	5	—	6	—	7	ns
tDW	Data to Write Time Overlap	4	—	5	—	6	—	8	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
tOW[1]	Output Active from End of Write	2	—	2	—	2	—	2	—	ns

B

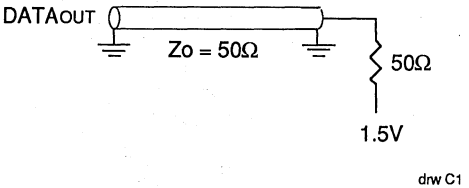


Figure 3. BiCMOS Output Load

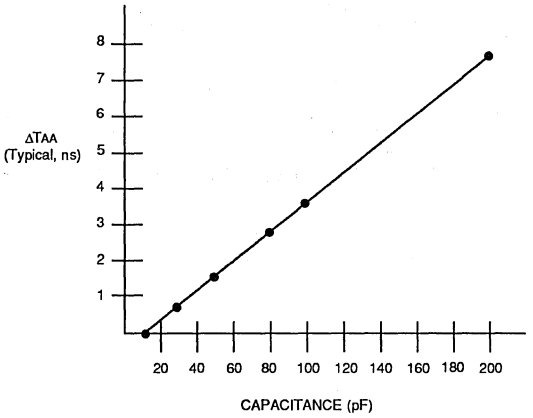


Figure 4. Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS

(VCC = 5V ±10%, TA = 0°C TO +70°C)

Symbol	Parameter	7MP4045BxxZ, 7MP4045BxxM						Unit
		-12[2]		-15[2]		-17[2]		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
tRC	Read Cycle Time	12	—	15	—	17	—	ns
tAA	Address Access Time	—	12	—	15	—	17	ns
tACS	Chip Select Access Time	—	7	—	8	—	9	ns
tCLZ[1]	Chip Select to Output in Low Z	2	—	2	—	2	—	ns
tOE	Output Enable to Output Valid	—	5	—	6	—	8	ns
tOLZ[1]	Output Enable to Output in Low Z	2	—	2	—	2	—	ns
tCHZ[1]	Chip Deselect to Output in High Z	—	7	—	8	—	10	ns
tOHZ[1]	Output Disable to Output in High Z	—	4	—	5	—	6	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	ns
Write Cycle								
tWC	Write Cycle Time	12	—	15	—	17	—	ns
tCW	Chip Select to End of Write	8	—	9	—	10	—	ns
tAW	Address Valid to End of Write	9	—	10	—	12	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width	9	—	10	—	12	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tWHZ[1]	Write Enable to Output in High Z	—	5	—	6	—	7	ns
tDW	Data to Write Time Overlap	5	—	6	—	8	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	ns
tOW[1]	Output Active from End of Write	2	—	2	—	2	—	ns

NOTES:

2703 tbl 09

1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

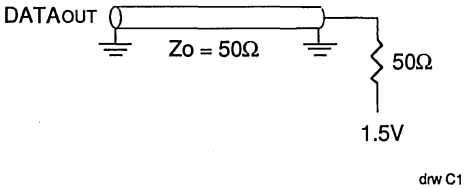


Figure 3. BICMOS Output Load

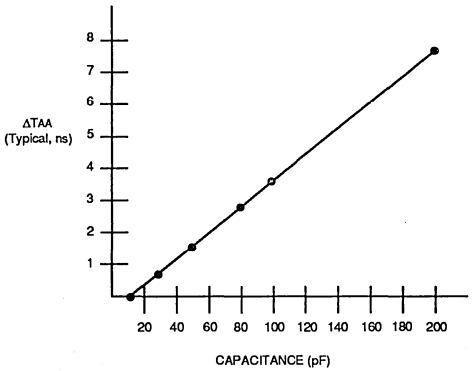


Figure 4. Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS

(VCC = 5V ±10%, TA = 0°C TO +70°C)

		7MP4045SxxZ, 7MP4045SxxM										
		-20[2]		-25		-30		-35		-45		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
tAA	Address Access Time	—	20	—	25	—	30	—	35	—	45	ns
tACS	Chip Select Access Time	—	20	—	25	—	30	—	35	—	45	ns
tCLZ[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	10	—	12	—	15	—	18	—	23	ns
tOLZ[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	0	—	ns
tCHZ[1]	Chip Deselect to Output in High Z	—	10	—	12	—	15	—	18	—	20	ns
tOHZ[1]	Output Disable to Output in High Z	—	10	—	10	—	10	—	10	—	10	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	5	—	5	—	ns
tPU[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
tPD[1]	Chip Deselect to Power-Down Time	—	20	—	25	—	30	—	35	—	45	ns
Write Cycle												
tWC	Write Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
tCW	Chip Select to End of Write	15	—	20	—	25	—	30	—	40	—	ns
tAW	Address Valid to End of Write	15	—	20	—	25	—	30	—	40	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	15	—	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tWHZ[1]	Write Enable to Output in High Z	—	13	—	15	—	18	—	20	—	23	ns
tDW	Data to Write Time Overlap	12	—	15	—	17	—	20	—	25	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	ns
tOW[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns

NOTES:

2703 tbl 09

1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

B

The following section contains full data sheets that appeared in the 1991 SPECIALIZED MEMORIES Data Book. These data sheets had changes to 50% or more of the overall contents and are now considered new. Refer to the bar at the top of each page to see where that page can be found in the 1991 SPECIALIZED MEMORIES Data Book.

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 64K (16K x 4-BIT) SRAM

IDT10494
IDT100494
IDT101494

FEATURES:

- 16,384-words x 4-bit organization
- Address access time: 5/6/7/8/10/15
- Low power dissipation: 700mW (typ.)
- Guaranteed Output Hold time
- Fully compatible with ECL logic levels
- Separate data input and output
- JEDEC standard through-hole and surface mount packages

DESCRIPTION:

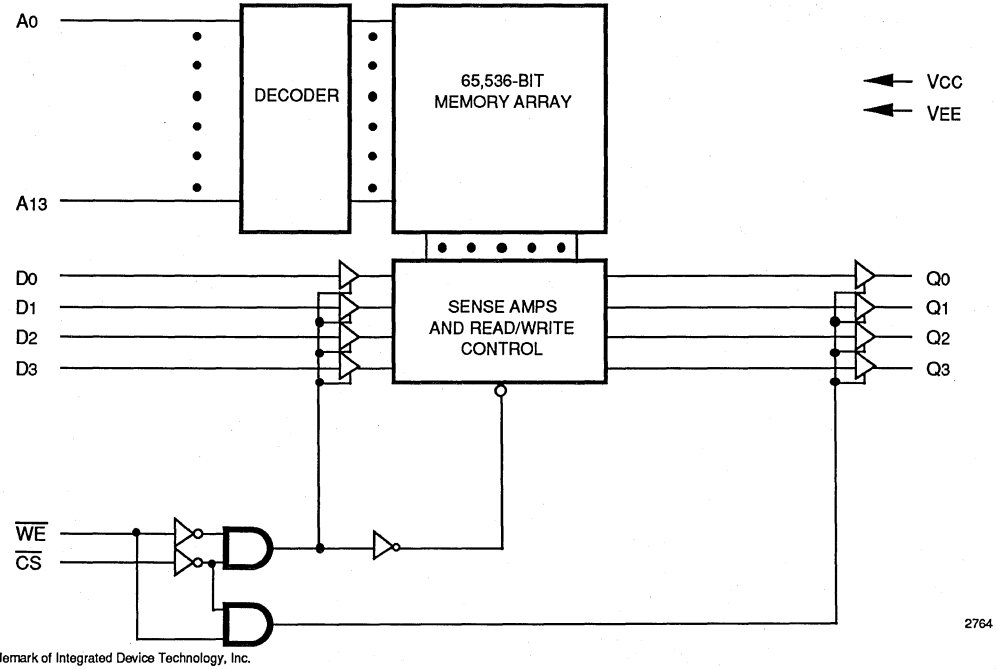
The IDT10494, IDT100494 and 101494 are 65,536-bit high-speed BiCEMOS™ ECL static random access memories organized as 16K x 4, with separate data inputs and outputs. All I/Os are fully compatible with ECL levels.

These devices are part of a family of asynchronous four-bit-wide ECL SRAMs. The devices have been configured to follow the standard ECL SRAM JEDEC pinout. Because they are manufactured in BiCEMOS™ technology, however, power dissipation is greatly reduced over equivalent bipolar devices.

The asynchronous SRAMs are the most straightforward to use because no additional clocks or controls are required: $Data_{OUT}$ is available an access time after the last change of address. To write data into the device requires the creation of a Write Pulse, and the write cycle disables the output pins in conventional fashion.

The fast access time and guaranteed Output Hold time allow greater margin for system timing variation. $Data_{IN}$ setup time specified with respect to the trailing edge of Write Pulse eases write timing allowing balanced Read and Write cycle times.

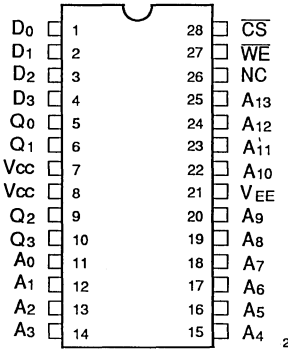
FUNCTIONAL BLOCK DIAGRAM



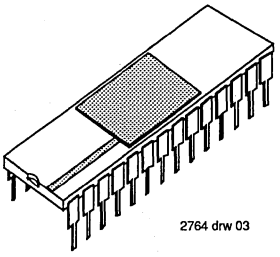
2764 drw 01

BiCEMOS is a trademark of Integrated Device Technology, Inc.

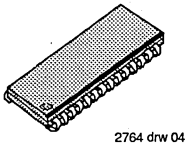
PIN CONFIGURATION



DIP/SOJ
TOP VIEW



400-Mil-Wide
CERAMIC PACKAGE
C28



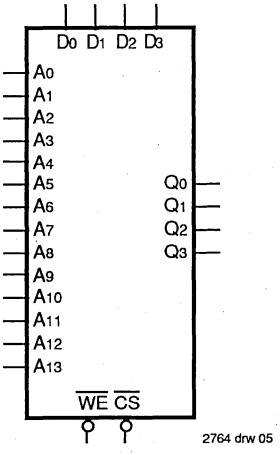
300-Mil-Wide
PLASTIC SOJ PACKAGE
Y28

PIN DESCRIPTIONS

Symbol	Pin Name
A0 through A13	Address Inputs
D0 through D3	Data Inputs
Q0 through Q3	Data Outputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input (Internal pull down)
VEE	More Negative Supply Voltage
VCC	Less Negative Supply Voltage

2764 tbl 01

LOGIC SYMBOL



16K x 4
SRAM

AC OPERATING RANGES(1)

I/O	VEE	Temperature
10K	-5.2V ±5%	0 TO 75°C, air flow exceeding 2 m/sec
100K	-4.5V ±5%	0 TO 85°C, air flow exceeding 2 m/sec
101K	-4.75V to -5.46V	0 TO 75°C, air flow exceeding 2 m/sec

2764 tbl 02

NOTE:
1. Referenced to Vcc

CAPACITANCE (TA=+25°C, f=1.0MHz)

Symbol	Parameter	DIP Typ.	DIP Max.	SOJ Typ.	SOJ Max.	Unit
CIN	Input Capacitance	4	–	3	–	pF
COUT	Output Capacitance	6	–	3	–	pF

2764 tbl 03

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	DataOUT	Function
H	X	L	Deselected
L	H	RAM Data	Read
L	L	L	Write

2764 tbl 04

NOTE:
1. H=High, L=Low, X=Don't Care

B

ECL-10K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2764 tbl 05

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-10K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L =50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit	T_A
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	V_{IN} = V_{IHB} or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	V_{IN} = V_{IHB} or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	V_{IN} = V_{IHA}	$\overline{CS}$	–	–	220	µA	–
			Others	–	–	110	µA	–
I_{IL}	Input LOW Current	V_{IN} = V_{ILB}	$\overline{CS}$	0.5	–	170	µA	–
			Others	-50	–	90	µA	–
I_{EE}	Supply Current	All Inputs and Outputs Open		-190	-130	–	mA	–

2764 tbl 06

NOTE:

1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

ECL-100K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +85	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Out mput Current (Output High)		-50	mA

2762 tbl 07

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-100K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.5V, R_L =50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-170	-110	–	mA

2762 tbl 08

NOTE:

1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.

B

ECL-101K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Out mput Current (Output High)		-50	mA

2763 tbl 09

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-101K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L=50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

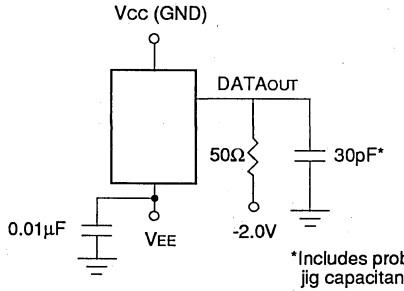
Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	V_{IN} = V_{IHB} or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	V_{IN} = V_{IHB} or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	V_{IN} = V_{IHA}	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	V_{IN} = V_{ILB}	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-190	-130	–	mA

2763 tbl 10

NOTE:

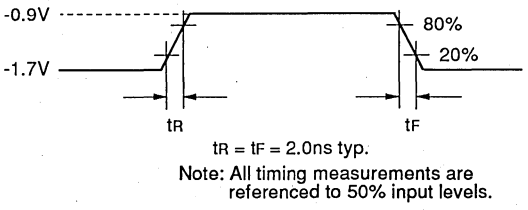
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

AC TEST LOAD CONDITION



2764 drw 06

AC TEST INPUT PULSE



2764 drw 07

RISE/FALL TIME

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
tR	Output Rise Time	–	–	2	–	ns
tF	Output Fall Time	–	–	2	–	ns

2764 tbl 11

FUNCTIONAL DESCRIPTION

The IDT10494, IDT100494 and IDT101494 BiCMOS ECL static RAMs (SRAM) provide high speed with low power dissipation typical of BiCMOS ECL. These devices follow the conventional pinout and functionality for 16K x 4 ECL SRAMs. The ECL-101K meets electrical specifications that combine the ECL-100K temperature and voltage compensated output levels with the high-speed of ECL-10K VEE compatibility (-5.2V).

READ TIMING

The read timing on these asynchronous devices is straightforward. DataOUT is held low until the device is selected by Chip Select ($\overline{CS}$). Then Address (ADDR) settles and data appears on the output after time tAA. Note that DataOUT is held for a short time (tOH) after the address begins to change for the next access, then ambiguous data is on the bus until a new time tAA.

WRITE TIMING

To write data to the device, a Write Pulse need be formed on the Write Enable input ($\overline{WE}$) to control the write to the SRAM array. While $\overline{CS}$ and ADDR must be set-up when $\overline{WE}$ goes low, DataIN can settle *after* the falling edge of $\overline{WE}$, giving the datapath extra margin. Data is written to the memory cell at the end of the Write Pulse, and addresses and Chip Select must be held after the rising edge of the Write Pulse to ensure satisfactory completion of the cycle.

DataOUT is disabled (held low) during the Write Cycle. If $\overline{CS}$ is held low (active) and addresses remain unchanged, the DataOUT pins will output the written data after "Write Recovery Time" (tWR).

Because of the very short Write Pulse requirement, these devices can be cycled as quickly for Writes as for Reads. Balanced cycles mean simpler timing in cache applications.

B

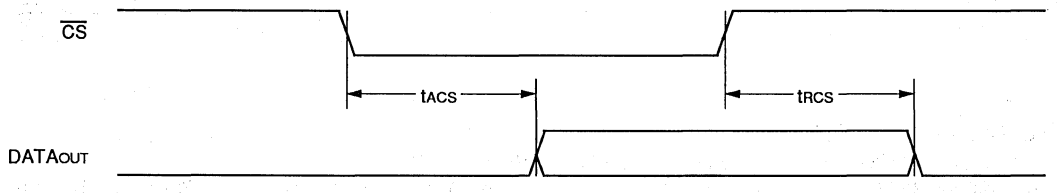
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10494S5 100494S5 101494S5		10494S6 100494S6 101494S6		10494S7 100494S7 101494S7		10494S8 100494S8 101494S8		10494S10 100494S10 101494S10		10494S15 100494S15 101494S15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE															
tACS	Chip Select Access Time	—	—	2.5	—	3	—	3	—	5	—	5	—	5	ns
tRCS	Chip Select Recovery Time	—	—	2.5	—	3	—	3	—	5	—	5	—	5	ns
tAA	Address Access Time	—	—	5	—	6	—	7	—	8	—	10	—	15	ns
tOH	Data Hold from Address Change	—	2	—	3	—	3	—	3	—	3	—	3	—	ns

NOTE:
1. Input and Output reference level is 50% point of waveform.

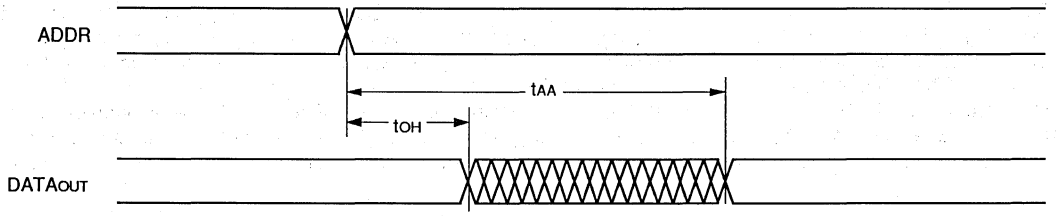
2764 tbl 12

READ CYCLE GATED BY CHIP SELECT



2764 drw 08

READ CYCLE GATED BY ADDRESS



2764 drw 09

AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

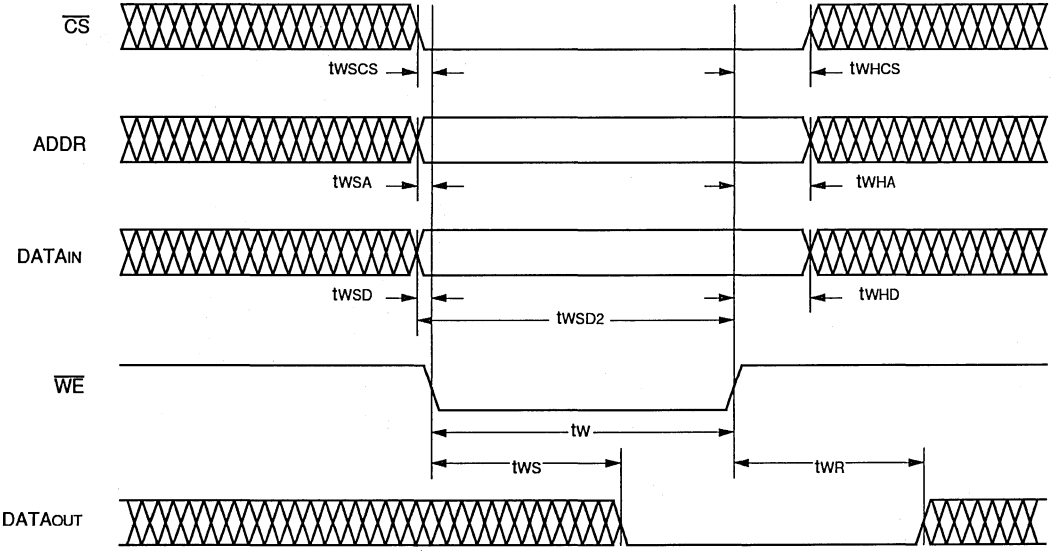
Symbol	Parameter[1]	Test Condition	10494S5 100494S5 101494S5		10494S6 100494S6 101494S6		10494S7 100494S7 101494S7		10494S8 100494S8 101494S8		10494S10 100494S10 101494S10		10494S15 100494S15 101494S15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE															
tW	Write Pulse Width	tWSA=min.	4	—	5	—	6	—	7	—	8	—	10	—	ns
tWSD	Data Set-up Time	—	0	—	0	—	0	—	0	—	0	—	2	—	ns
tWSD2[2]	Data Set-up Time to $\overline{WE}$ High	—	4	—	5	—	5	—	5	—	5	—	5	—	ns
tWSA	Address Set-up Time	tWSA-min.	0	—	0	—	0	—	0	—	0	—	2	—	ns
tWSCS	Chip Select Set-up Time	—	0	—	0	—	0	—	0	—	0	—	2	—	ns
tWHD	Data Hold Time	—	1	—	1	—	1	—	1	—	2	—	3	—	ns
tWHA	Address Hold Time	—	1	—	1	—	1	—	1	—	2	—	3	—	ns
tWHCS	Chip Select Hold Time	—	1	—	1	—	1	—	1	—	2	—	3	—	ns
tWS	Write Disable Time	—	—	3	—	4	—	5	—	5	—	5	—	5	ns
tWR[3]	Write Recovery Time	—	—	3	—	4	—	5	—	5	—	5	—	5	ns

NOTES:

2764 tbl 13

1. Input and Output reference level is 50% point of waveform.
2. tWSD is specified with respect to the falling edge of $\overline{WE}$ for compatibility with bipolar part specifications, but this device actually only requires tWSD2 with respect to rising edge of $\overline{WE}$.
3. tWR is defined as the time to reflect the newly written data on the Data Outputs (Q_0 to Q_3) when no new Address Transition occurs.

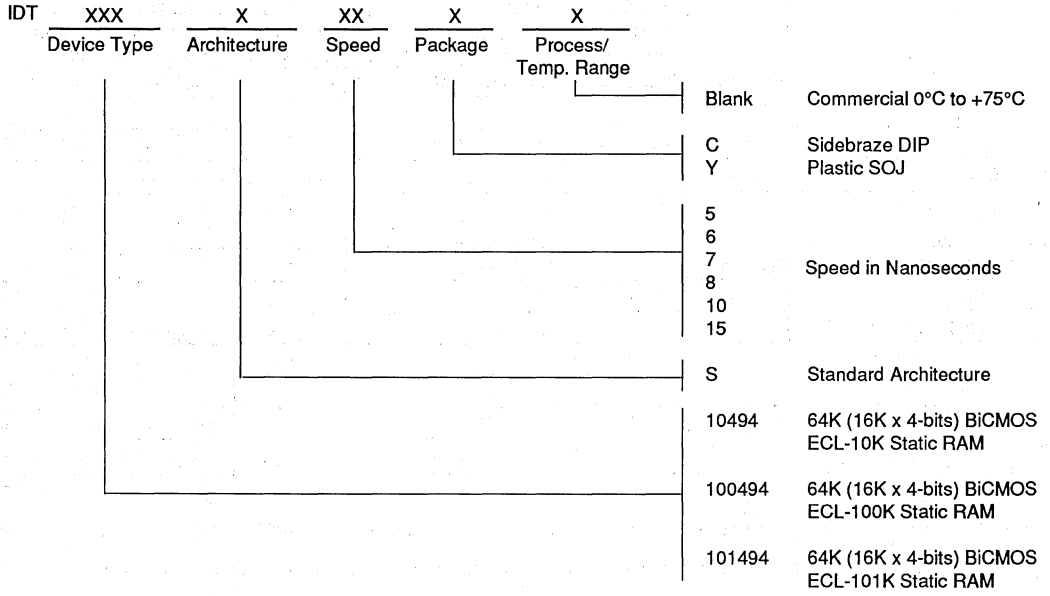
WRITE CYCLE TIMING DIAGRAM



2764 drw 10

B

ORDERING INFORMATION



2764 drw 11

Integrated Device Technology, Inc.

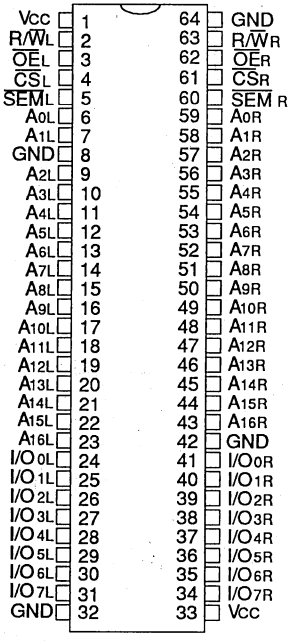
128K x 8
64K x 8
CMOS DUAL-PORT
STATIC RAM MODULE

PRELIMINARY
IDT7M1001
IDT7M1003

FEATURES

- High density 1M/512K CMOS dual-port static RAM module
- Fast access times:
  - — commercial - 25, 30, 35, 40, 50, 65ns
  - — military - 35, 40, 50, 65, 80ns
- Fully asynchronous read/write operation from either port
- Full on-chip hardware support of semaphore signaling between ports
- Surface mounted LCC (leadless chip carriers) components on a 64-pin sidebraze DIP (Dual In-line Package)
- Multiple Vcc and GND pins for maximum noise immunity
- Single 5V (±10%) power supply
- Input/outputs directly TTL compatible

PIN CONFIGURATION[1, 2]



DIP
TOP VIEW

2803 drw 01

DESCRIPTION:

The IDT7M1001/IDT7M1003 is a 128K x 8 /64K x 8 high-speed CMOS dual-port static RAM module constructed on a multilayer ceramic substrate using eight IDT7006 (16K x 8) dual-port RAMs and two IDT FCT138 decoders or depopulated using only four IDT7006s and two decoders.

This module provides two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory. System performance is enhanced by facilitating port-to-port communication via semaphore ($\overline{SEM}$) "handshake" signaling. The IDT7M1001/1003 module is designed to be used as stand-alone dual-port RAM where on-chip hardware port arbitration is not needed. It is the users responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports.

The IDT7M1001/1003 module is packaged on a multilayer co-fired ceramic 64-pin DIP (Dual In-line Package) with dimensions of only 3.2" x 0.62" x 0.38". Maximum access times as fast as 25ns over the commercial temperature range and 35ns over the military temperature range are available.

All inputs and outputs of the IDT7M1001/1003 are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation of the module.

All IDT military module semiconductor components are manufacured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

B

PIN NAMES

Left Port	Right Port	Description
A (0–16)L	A (0–16)R	Address Inputs
I/O (0–7)L	I/O (0–7)R	Data Inputs/Outputs
R/$\overline{W}$L	R/$\overline{W}$R	Read/Write Enables
$\overline{CS}$L	$\overline{CS}$R	Chip Select
$\overline{OE}$L	$\overline{OE}$R	Output Enable
$\overline{SEM}$L	$\overline{SEM}$R	Semaphore Control
Vcc		Power
GND		Ground

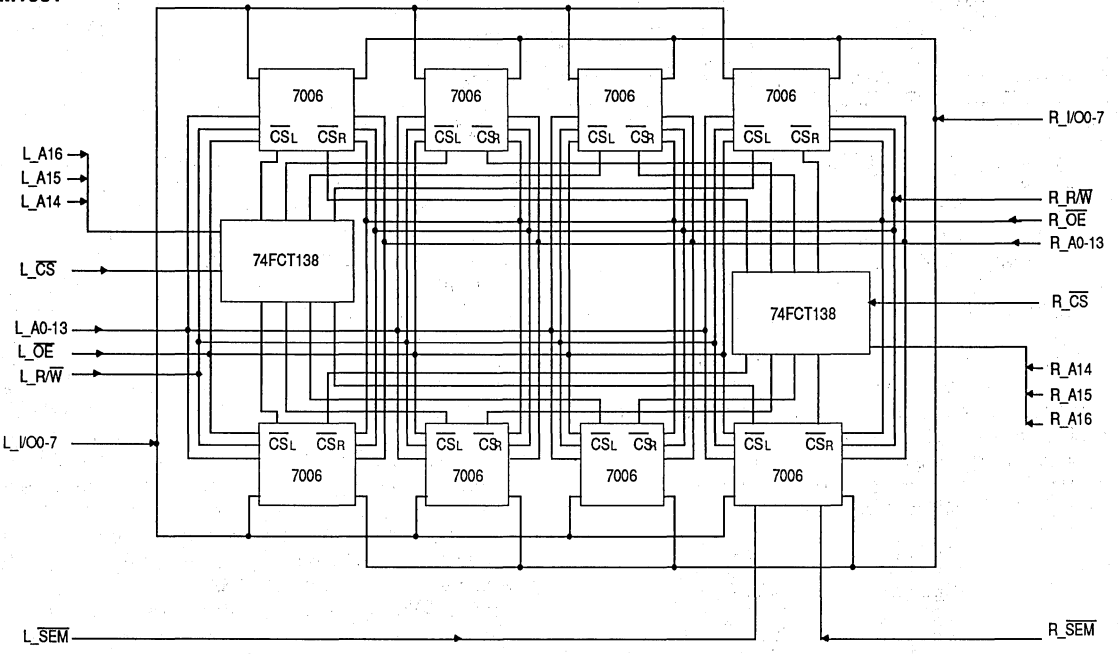
2803 tbl 01

NOTE:
1. For module dimensions, please refer to the module drawings in the packaging section.
2. For the IDT7M1003 (64K x 8) version, Pins 23 & 43 must be connected to GND for proper operation of the module.

CEMOS is a trademark of Integrated Device Technology, Inc.

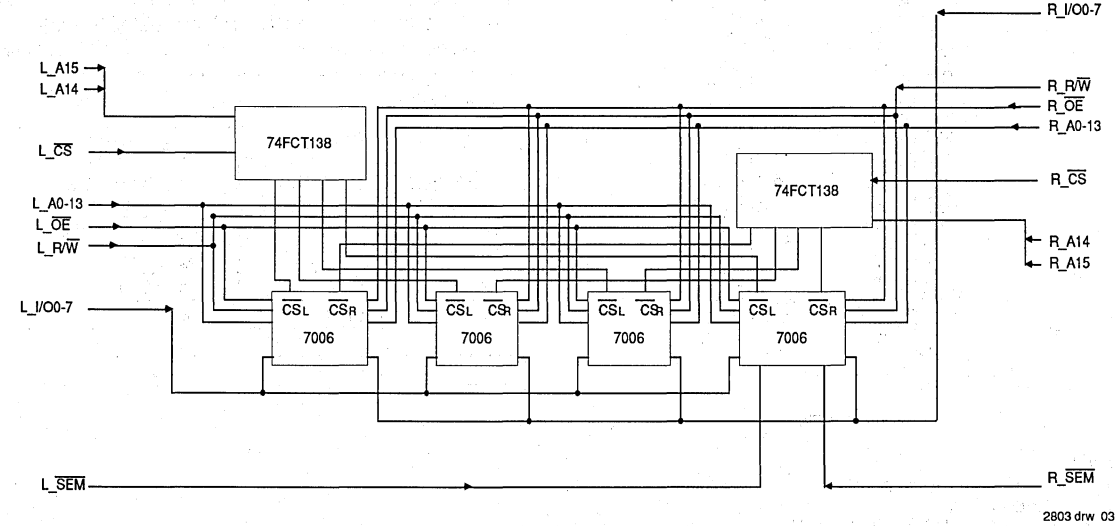
FUNCTIONAL BLOCK DIAGRAM

7M1001



2803 drw 02

7M1003



2803 drw 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2803 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Test Conditions	Max.	Unit
C_{IN1}	Input Capacitance ($\overline{CS}$ or $\overline{SEM}$)	V_{IN} = 0V	15	pF
C_{IN2}	Input Capacitance (Data, Address, All Other Controls)	V_{IN} = 0V	100	pF
C_{OUT}	Output Capacitance (Data)	V_{OUT} = 0V	100	pF

2803 tbl 05

NOTE:
1. This parameter is guaranteed by design but not tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2803 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	-	0.8	V

2803 tbl 04

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

B

DC ELECTRICAL CHARACTERISTICS

(Vcc = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7M1001/1003 Commercial Min.	Commercial Max.[1]	Commercial Max.[2]	Military Min.	Military Max.[1]	Military Max.[2]	Unit
I_{CC2}	Dynamic Operating Current (Both Ports Active)	Vcc = Max., $\overline{CS} \le V_{IL}$, $\overline{SEM} \ge V_{IH}$ Outputs Open, f = f_{MAX}	—	940	660	—	1130	790	mA
I_{CC1}	Standby Supply Current (One Port Active)	Vcc = Max., L_$\overline{CS}$ or R_$\overline{CS} \ge V_{IH}$ Outputs Open, f = f_{MAX}	—	750	470	—	905	565	mA
I_{SB1}	Standby Supply Current (TTL Levels)	Vcc = Max., L_$\overline{CS}$ and R_$\overline{CS} \ge V_{IH}$ Outputs Open, f = f_{MAX} L_$\overline{SEM}$ and R_$\overline{SEM} \ge$ Vcc –0.2V	—	565	285	—	685	345	mA
I_{SB2}	Full Standby Supply Current (CMOS Levels)	L_$\overline{CS}$ and R_$\overline{CS} \ge$ Vcc –0.2V $V_{IN} >$ Vcc 0.2V or < 0.2V L_$\overline{SEM}$ and R_$\overline{SEM} \ge$ Vcc –0.2V	—	125	65	—	245	125	mA

2803 tbl 06

NOTES:
1. For IDT7M1001 (128K x 8) version only.
2. For IDT7M1003 (64K x 8) version only.

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7M1001 Min.	IDT7M1001 Max.	IDT7M1003 Min.	IDT7M1003 Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address, Data & Other Controls)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	80	—	40	µA
$\|I_{LI}\|$	Input Leakage ($\overline{CS}$ and $\overline{SEM}$)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	10	—	10	µA
$\|I_{LO}\|$	Output Leakage (Data)	V_{CC} = Max. $\overline{CS} \geq V_{IH}$, V_{OUT} = GND to V_{CC}	—	80	—	40	µA
V_{OL}	Output Low Voltage	V_{CC} = Min. I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min. I_{OH} = -4mA	2.4	—	2.4	—	V

2803 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2803 tbl 08

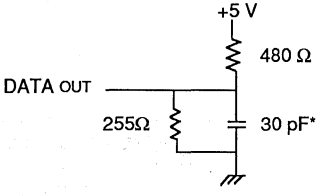


Figure 1. Output Load

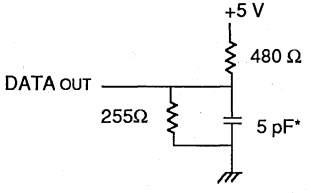


Figure 2. Output Load
(for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{WHZ}, t_{OW})

*Including scope and jig.

2803 drw 04

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	IDT7M1001Sxx / IDT7M1003Sxx								Unit
		-25[5]		-30[5]		-35[5]		-40		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	25	—	30	—	35	—	40	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	—	40	ns
t_{ACS}[2]	Chip Select Access Time	—	25	—	30	—	35	—	40	ns
t_{OE}	Output Enable Access Time	—	13	—	15	—	20	—	25	ns
t_{OH}	Output Hold From Address Change	3	—	3	—	3	—	3	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	3	—	3	—	3	—	3	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	18	—	20	—	20	—	20	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	3	—	3	—	3	—	3	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	18	—	20	—	20	—	20	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Disable to Power Down Time	—	50	—	50	—	50	—	50	ns
t_{SOP}	$\overline{SEM}$ Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	12	—	12	—	15	—	15	—	ns
Write Cycle										
t_{WC}	Write Cycle Time	25	—	30	—	35	—	40	—	ns
t_{CW}[2]	Chip Select to End of Write	20	—	25	—	30	—	35	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	30	—	35	—	ns
t_{AS1}[3]	Address Set-up to Write Pulse Time	5	—	5	—	5	—	5	—	ns
t_{AS2}	Address Set-up to $\overline{CS}$ Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	30	—	35	—	ns
t_{WR}[4]	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	15	—	20	—	25	—	30	—	ns
t_{DH}[4]	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	18	—	20	—	20	—	20	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	18	—	20	—	20	—	20	ns
t_{OW}[1, 4]	Output Active from End of Write	0	—	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	10	—	13	—	15	—	15	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	10	—	13	—	15	—	15	—	ns
Port-to-Port Delay Timing										
t_{WDD}[6]	Write Pulse to Data Delay	—	50	—	55	—	60	—	65	ns
t_{DDD}[6]	Write Data Valid to Read Data Valid	—	35	—	40	—	45	—	50	ns

NOTES:

1. This parameter is guaranteed by design but not tested.
2. To access RAM $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
3. t_{AS1}= 0 if R/$\overline{W}$ is asserted low simultaneously with or after the $\overline{CS}$ low transition.
4. For $\overline{CS}$ controlled write cycles, t_{WR}= 5ns, t_{DH}= 5ns, t_{OW}= 5ns.
5. Preliminary specifications only.
6. Port-to-Port delay through the RAM cells from the writing port to the reading port.

2803 tbl 09

AC ELECTRICAL CHARACTERISTICS

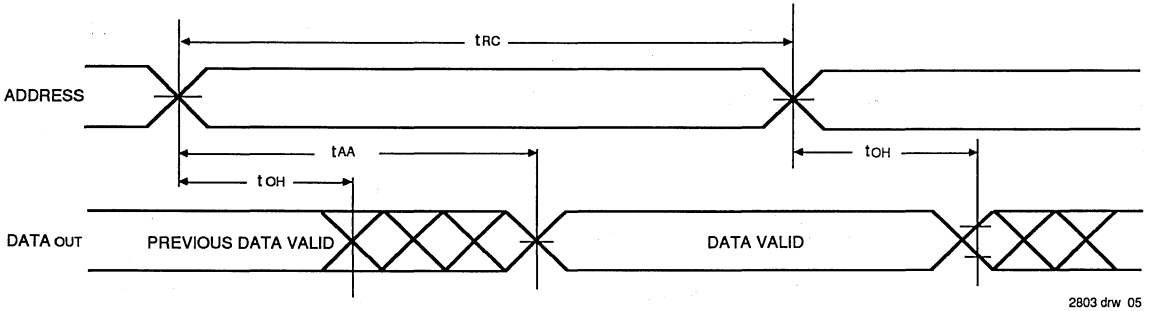
(Vcc = 5.0V ± 10%, TA = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	IDT7M1001Sxx / IDT7M1003Sxx -50 Min.	-50 Max.	-65 Min.	-65 Max.	-80 Min.	-80 Max.	Unit
Read Cycle								
t_{RC}	Read Cycle Time	50	—	65	—	80	—	ns
t_{AA}	Address Access Time	—	50	—	65	—	80	ns
t_{ACS}[2]	Chip Select Access Time	—	50	—	65	—	80	ns
t_{OE}	Output Enable Access Time	—	30	—	35	—	40	ns
t_{OH}	Output Hold From Address Change	3	—	3	—	3	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	3	—	3	—	3	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	25	—	30	—	35	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	3	—	3	—	3	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	25	—	30	—	35	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Disable to Power Down Time	—	50	—	50	—	50	ns
t_{SOP}	$\overline{SEM}$ Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	20	—	20	—	ns
Write Cycle								
t_{WC}	Write Cycle Time	50	—	65	—	80	—	ns
t_{CW}[2]	Chip Select to End of Write	40	—	50	—	55	—	ns
t_{AW}	Address Valid to End of Write	40	—	50	—	55	—	ns
t_{AS1}[3]	Address Set-up to Write Pulse Time	5	—	5	—	5	—	ns
t_{AS2}	Address Set-up to $\overline{CS}$ Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	40	—	45	—	50	—	ns
t_{WR}[4]	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	35	—	40	—	45	—	ns
t_{DH}[4]	Data Hold Time	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	25	—	30	—	35	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	25	—	30	—	35	ns
t_{OW}[1, 4]	Output Active from End of Write	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	15	—	15	—	15	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	15	—	15	—	15	—	ns
Port-to-Port Delay Timing								
t_{WDD}[5]	Write Pulse to Data Delay	—	70	—	85	—	95	ns
t_{DDD}[5]	Write Data Valid to Read Data Valid	—	55	—	70	—	80	ns

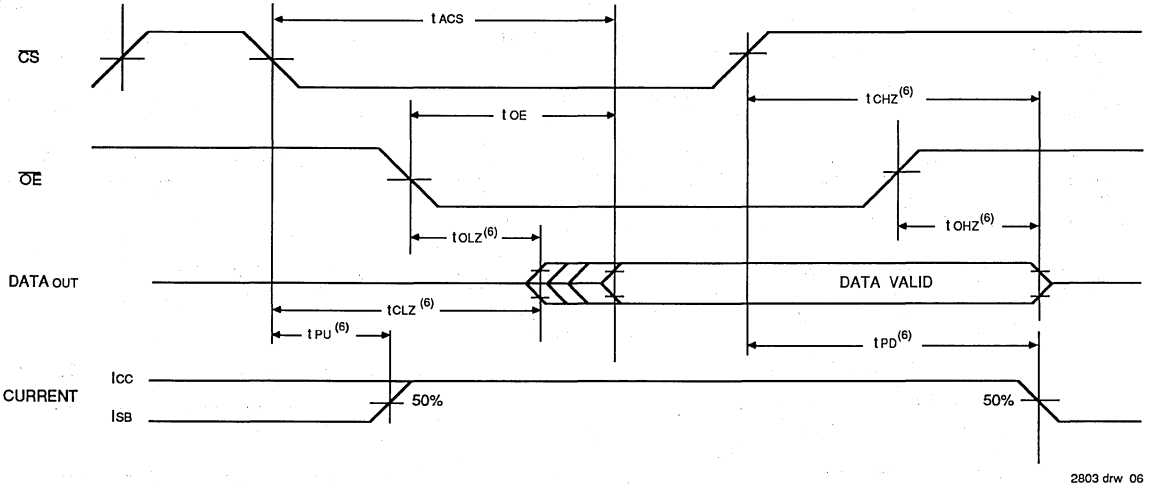
NOTES:

1. This parameter is guaranteed by design but not tested.
2. To access RAM $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
3. $t_{AS1} = 0$ if R/$\overline{W}$ is asserted low simultaneously with or after the $\overline{CS}$ low transition.
4. For $\overline{CS}$ controlled write cycles, $t_{WR} = 5ns$, $t_{DH} = 5ns$, $t_{OW} = 5ns$.
5. Port-to-Port delay through the RAM cells from the writing port to the reading port.

TIMING WAVEFORM OF READ CYCLE NO. 1 (EITHER SIDE)(1,2,4)



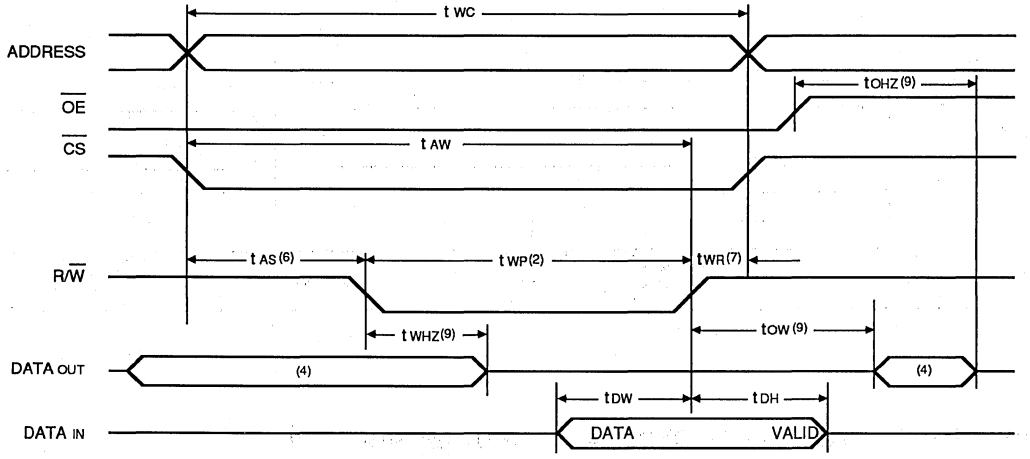
TIMING WAVEFORM OF READ CYCLE NO. 2 (EITHER SIDE)(1,3,5)



B

NOTES:
1. R/$\overline{W}$ is High for Read Cycles
2. Device is continuously enabled. $\overline{CS}$ = Low. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = Low.
5. To access RAM, $\overline{CS}$ = Low, $\overline{SEM}$ = H. To access semaphore, $\overline{CS}$ = H and $\overline{SEM}$ = Low.
6. This parameter is guaranteed by design but not tested.

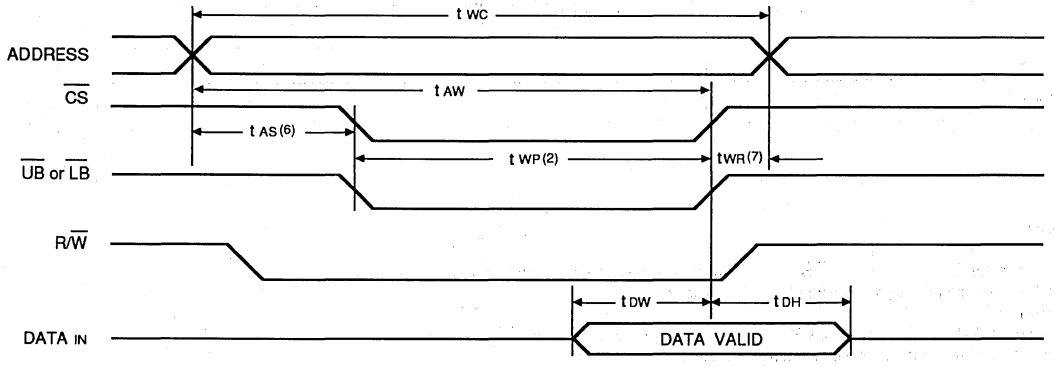
TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING)(1,3,5,8)



2803 drw 08

NOTES:
1. R/$\overline{W}$ is High for Read Cycles
2. Device is continuously enabled. $\overline{CS}$ = Low. $\overline{UB}$ or $\overline{LB}$ = Low. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = Low.
5. To access RAM, $\overline{CS}$ = Low, $\overline{UB}$ or $\overline{LB}$ = Low, $\overline{SEM}$ = H. To access semaphore, $\overline{CS}$ = H and $\overline{SEM}$ = Low.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is Low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be larger of twp or (twz + tdw) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is High during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse width be as short as the specified twp.
9. This parameter is guaranteed by design but not tested.

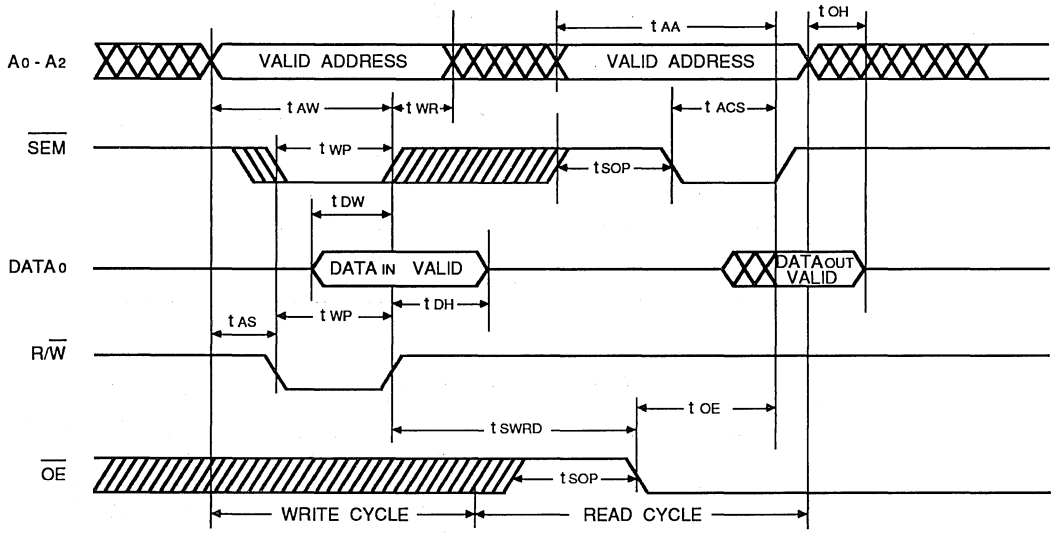
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1,3,5,8)



2803 drw 09

NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (twp) of a Low $\overline{UB}$ or $\overline{LB}$ and a Low $\overline{CS}$ and a Low R/$\overline{W}$ for memory array writing cycle.
3. twr is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CS}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of twp or (twz + tdw) to allow the I/O drivers to turn off and data to be placed on the bus for the required tdw. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified twp.
9. This parameter is guaranteed by design but not tested.

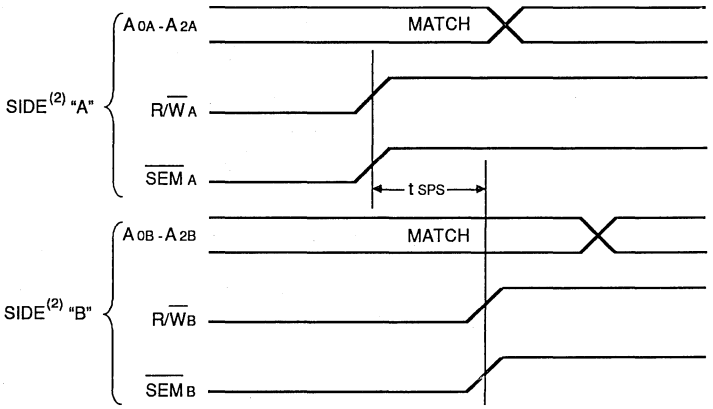
TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING (EITHER SIDE)(1)



2803 drw 10

NOTE:
1. $\overline{CS}$ = High for the duration of the above timing (both write and read cycle).

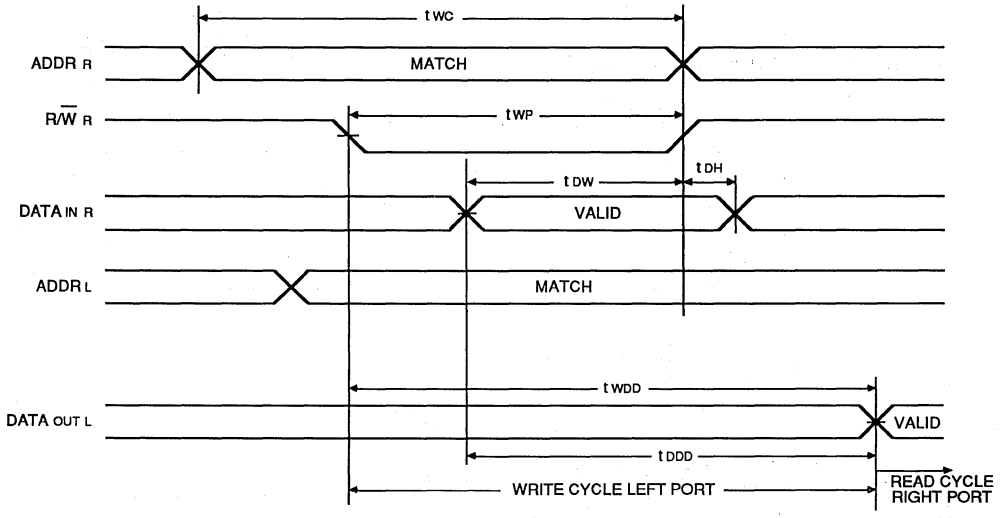
TIMING WAVEFORM OF SEMAPHORE CONTENTION(1,3,4)



2803 drw 11

NOTES:
1. $D_{OR} = D_{OL}$ = Low, $L\_\overline{CS} = R\_\overline{CS}$ = High. Semaphore Flag is released form both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from $R/\overline{W}_A$ or $\overline{SEM}_A$ going High to $R/\overline{W}_B$ or $\overline{SEM}_B$ going High.
4. If t_{SPS} is violated, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY(1)



NOTE:
1. L_$\overline{CS}$ = R_$\overline{CS}$ = Low

2803 drw 13

TRUTH TABLES

TABLE I: NON-CONTENTION READ/WRITE CONTROL[1]

Inputs[1]				Outputs	
$\overline{CS}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0 - I/O7	Mode
H	X	X	H	Hi-Z	Deselected: Power Down
L	L	X	H	DATAIN	Write to Both Bytes
L	H	L	H	DATAOUT	Read Both Bytes
X	X	H	X	Hi-Z	Outputs Disabled

NOTE:
1. $A_{0L} - A_{12} \neq A_{0R} - A_{12R}$

2803 tbl 12

TABLE II: SEMAPHORE READ/WRITE CONTROL[1]

Inputs				Outputs	
$\overline{CS}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0 - I/O7	Mode
H	H	L	L	DATAOUT	Read Data in Semaphore Flag
X	↑	X	L	DATAIN	Write DIN0 into Semaphore Flag
L	X	X	L	—	Not Allowed

NOTE:
1. $A_{0L} - A_{12} \neq A_{0R} - A_{12R}$

2803 tbl 13

TABLE III: EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE

Function	D0 - D7 Left	D0 - D7 Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains sempahore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to SEmaphore	0	1	Left port obtains sempahore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has sempahore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

NOTE:
1. This table denotes a sequence of events for only one of the eight semaphores available on the IDT7M1001/1003.

2803 tbl 16

B

FUNCTIONAL DESCRIPTIONAL

The IDT7M1001/1003 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. TheIDT7M1001/1003 has an automatic power down feature controlled by $\overline{CS}$. The $\overline{CS}$ controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{CS}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-Contention READ/WRITE conditions are illustrated in the Truth Tables.

SEMAPHORES

The IDT7M1001/1003 is an extremely fast dual-port 128K/64K x 8 CMOS static RAM module with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the dual-port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the dual-port RAM or any shared resource.

The dual-port RAM module features a fast access time, both ports completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS static RAM modules and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultanious READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non- semaphore portion of the dual-port RAM. These devices have an automatic power-down feature controlled by $\overline{CS}$ the dual-port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CS}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table where $\overline{CS}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT7M1001/1003 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT7M1001/1003's hardware semaphores which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT7M1001/1003 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW SEMPAHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the dual-port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that a shared resource is inuse. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor had set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side had relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT7M1001/1003 in a separate memory space from the dual-port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A_0 - A_2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D_0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other (Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that flag this is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go active or the output will never change.

A sequence of WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the samaphore flag will appear as a one, a fact which the processor will verify by the subsequent read. (see Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same samaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during a subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 1. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore latch have been written to a zero in the meantime, the samaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critcal case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is especially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a recource secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen. Code integrity is of the utmost importance when semaphores are used instead of slower, more restrictive hardware intensive schemes.

Initialization of the samaphores is not automatic and must be handled via the initialization program at power-up. Since any sempahore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES — SOME EXAMPLES

Perhaps the simplest application of semaphores is their application as resource markers for the IDT7M1001/1003's dual-port RAM module. Say that a 16K x 8 RAM block was to be divided into two 4K x 8 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 4K of dual-port RAM, the processor on the left port could write and then read a zero into Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 4K. Meanwhile the right processor would attempt to perform the same function. Since this processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 4K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 4K blocks of dual-port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the dual-port RAM or other shared resources into eight parts. Semaphore can even assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interface where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices had determined which memory area was "off limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available to one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application, one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor

arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

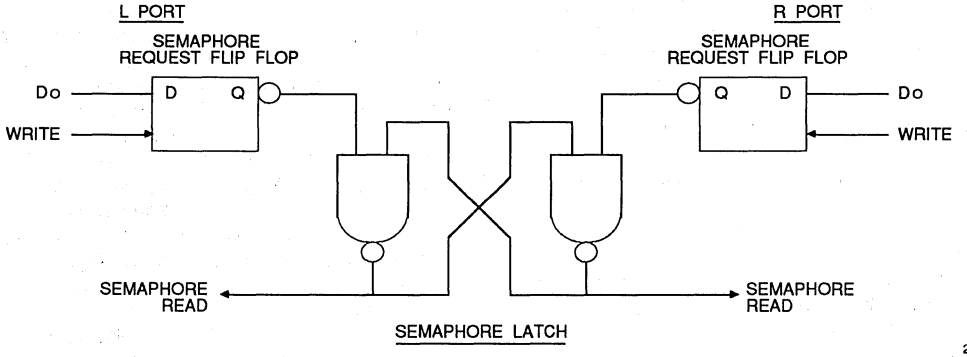
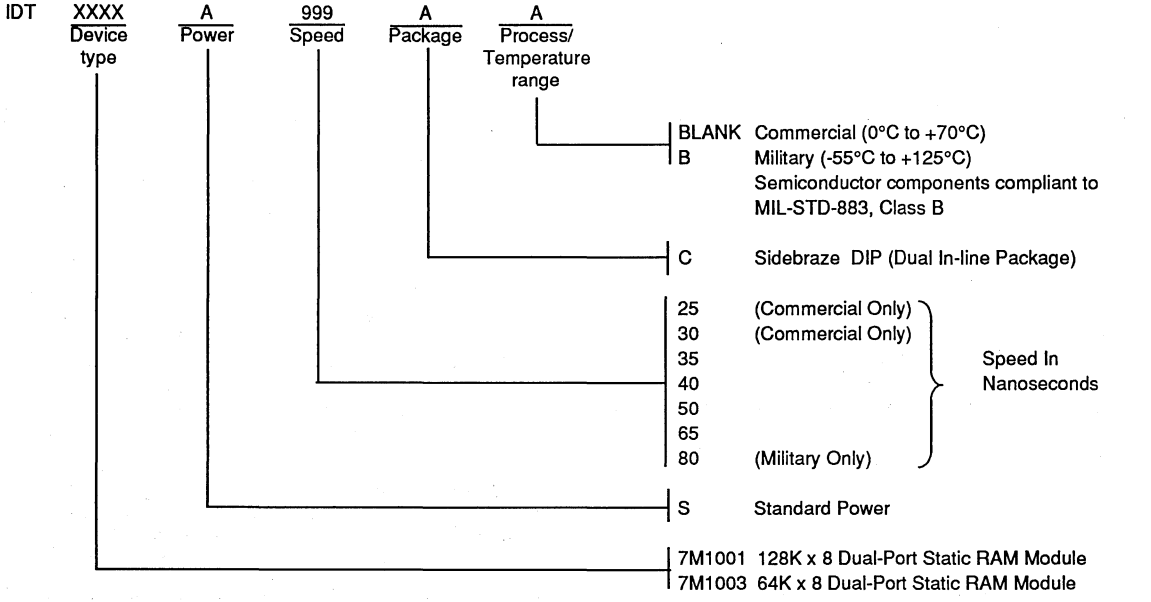


Figure 1. IDT7M1001/1003 Semaphore Logic

ORDERING INFORMATION



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B

Integrated Device Technology, Inc.

512K x 16 CMOS STATIC RAM MODULE

IDT7MP4047

FEATURES:

- High-speed 8 megabit CMOS static RAM module
- Fast access time: 70ns (max.)
- Low power consumption
  - — Active: 220mA max.
  - — CMOS Standby: 800µA max.
  - — Data retention: 450µA max. (Vcc= 2V)
- Surface mounted small outline plastic packages on a 45 pin FR-4 SIP (Single In-line Package)
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum immunity
- Inputs/outputs directly TTL compatible

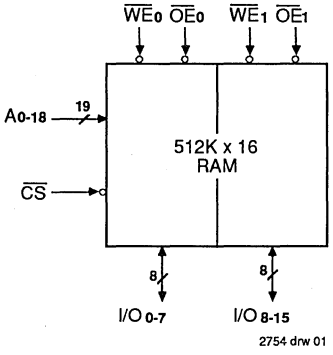
DESCRIPTION:

The IDT7MP4047 is a 512K x 16 CMOS static RAM module constructed on a multilayer epoxy laminate (FR-4) substrate using 8 128K x 8 static RAMs in small outline plastic packages and a one-of-four decoder. Availability of two Write Enables and two Output Enables provides byte access and output control flexibility. The IDT7MP4047 is available with access times as fast as 70ns with a maximum operating current of 220mA. For battery backup applications, a very low data retention current is available.

The IDT7MP4047 is packaged in a 45 pin FR-4 SIP (Single In-line Package). This results is a package 4.6 inches in length and 0.3 inches in thickness.

All inputs and outputs of the IDT7MP4047 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



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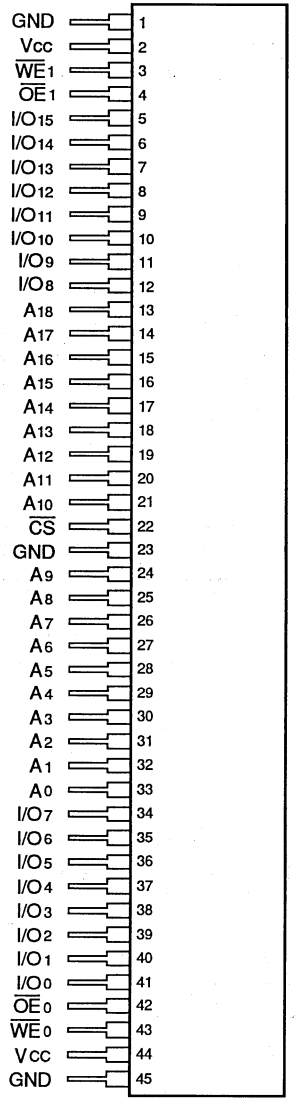
PIN CONFIGURATION[1]



2754 drw 02

SIP
FRONT VIEW

NOTE:
1. For module dimensions, please refer to the module drawings in the packaging section.

PIN NAMES

I/O0–I/O15	Data Inputs/Outputs
A0–A18	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}_{0-1}$	Write Enables
$\overline{OE}_{0-1}$	Output Enables
Vcc	Power
GND	Ground

2754 tbl 01

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	-10 to +85	°C
TSTG	Storage Temperature	-55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE: 2754 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

B

CAPACITANCE[1] (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	35	pF
CIN(C)	Input Capacitance($\overline{CS}$)	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	35	pF

NOTE: 2754 tbl 04
1. This parameter is guaranteed by design, but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2754 tbl 05
1. VIL = -3.0V for pulse width less than 20ns.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	$DATA_{OUT}$	Active
Write	L	L	High Z	Active

2754 tbl 02

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2754 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	8	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	8	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 2mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -1mA	2.4	—	V
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ = V_{IL}, f = f_{MAX}, Output Open	—	220	mA
I_{SB}	Standby Supply Current (TTL Levels)	$\overline{CS} \geq V_{IH}$, V_{CC} = Max., f = f_{MAX}, Ouput Open	—	24	mA
I_{SB}	Full Standby Supply Current (CMOS Levels)	$\overline{CS} \geq V_{HC}$, $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$ V_{CC} = Max., Output Open	—	800	µA

2754 tbl 07

DATA RETENTION CHARACTERISTICS (1)

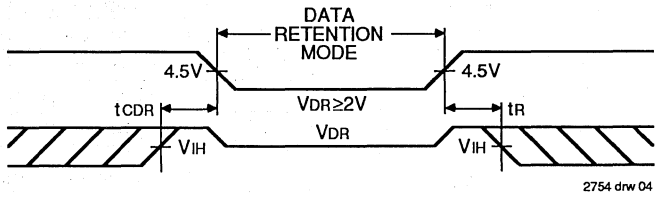
(T_A = 0°C to +70°C)

Symbol	Parameter	Test Condition	Min.	Max. cc @ 2.0V	Unit
V_{DR}	V_{CC} for Data Retention	—	2.0	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ - 0.2V	—	450	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time	$V_{IN} \leq V_{CC}$ - 0.2V	0	—	ns
t_R(3)	Operation Recovery Time	$V_{IN} \geq$ - 0.2V	t_{RC}(2)	—	ns

2754 tbl 10

NOTES:
1. V_{CC} = 2V, T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by design, but not tested.

DATA RETENTION WAVEFORM



2754 drw 04

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2754 tbl 08

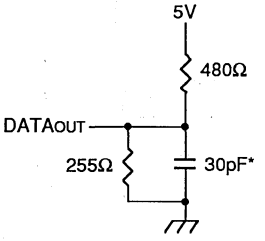


Figure 1. Output Load

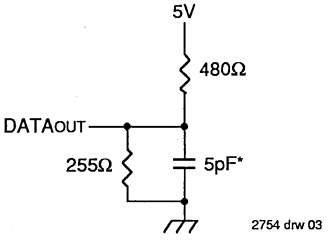


Figure 2. Output Load
(for tCLZ, tOLZ, tCHZ, tOHZ, tOW, and tWHZ)

*Including scope and jig

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

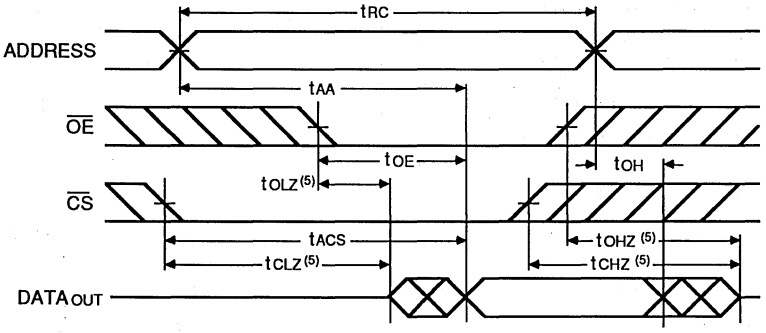
		7MP4047L xxS								
		-70		-85		-100		-120		
Symbol	Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
READ CYCLE										
tRC	Read Cycle Time	70	—	85	—	100	—	120	—	ns
tAA	Address Access Time	—	70	—	85	—	100	—	120	ns
tACS	Chip Select Access Time	—	70	—	85	—	100	—	120	ns
tOE	Output Enable to Output Valid	—	45	—	48	—	50	—	60	ns
tOHZ(1)	Output Disable to Output in High Z	—	30	—	33	—	35	—	40	ns
tOLZ(1)	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	ns
tCLZ(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	ns
tCHZ(1)	Chip Deselect to Output in High Z	—	40	—	43	—	45	—	50	ns
tOH	Output Hold from Address Change	10	—	10	—	10	—	10	—	ns
WRITE CYCLE										
tWC	Write Cycle Time	70	—	85	—	100	—	120	—	ns
tWP	Write Pulse Width	55	—	65	—	75	—	90	—	ns
tAS	Address Set-up Time	0	—	2	—	5	—	5	—	ns
tAW	Address Valid to End of Write	65	—	82	—	90	—	100	—	ns
tCW	Chip Selection to End of Write	65	—	80	—	85	—	100	—	ns
tDS	Data Set-up Time	35	—	38	—	40	—	45	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tWHZ(1)	Write Enable to Ouput in High Z	—	30	—	33	—	35	—	40	ns
tOW(1)	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

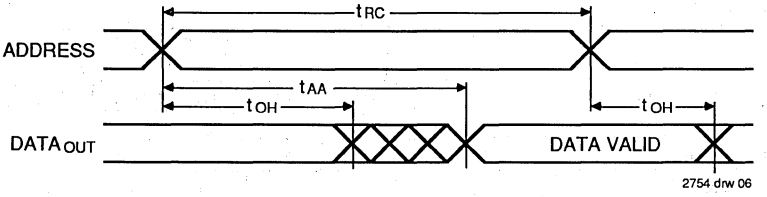
2754 tbl 09

B

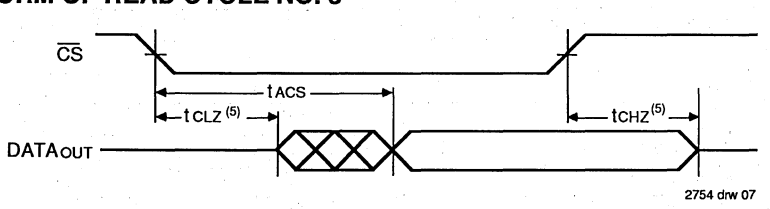
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)

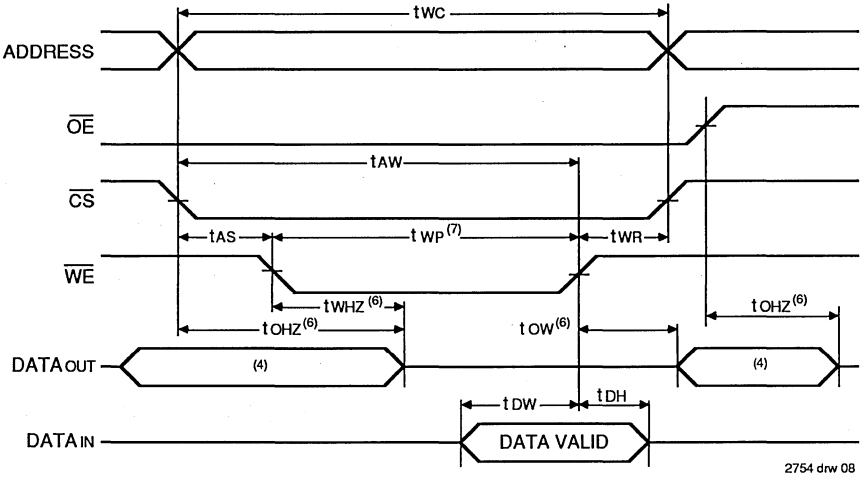


TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)

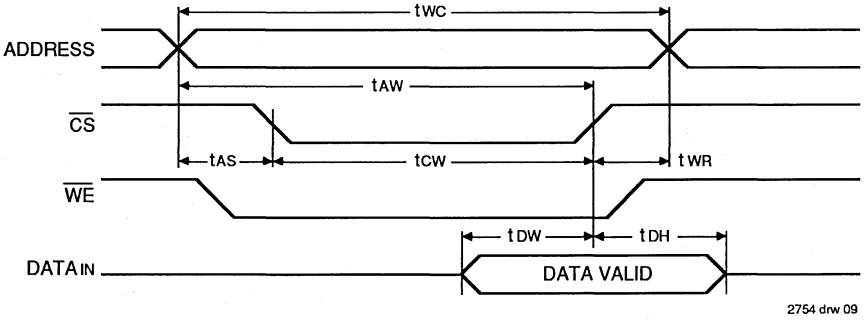


NOTES:
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



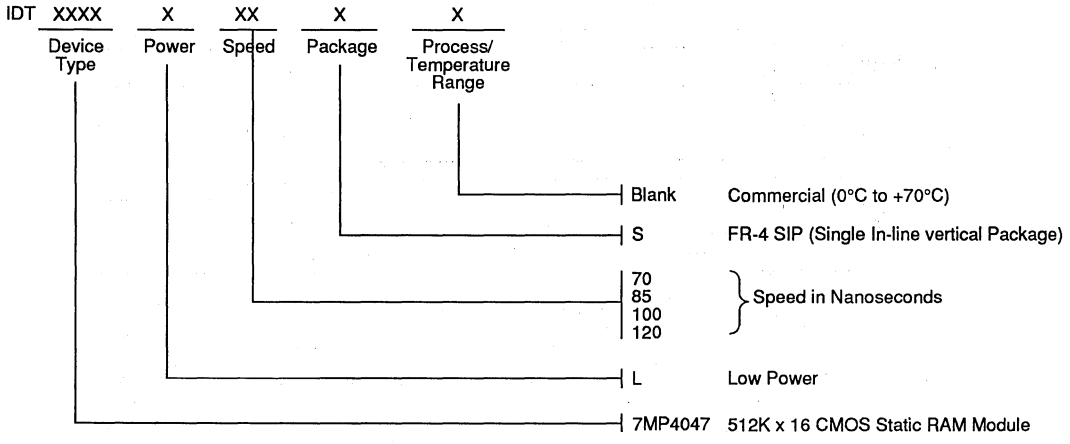
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



B

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going High to the end of write cycle.
4. During this period, I/O pins are in the output state and inputs signals must not be applied.
5. If the $\overline{CS}$ Low transition occurs simultaneously with or after the $\overline{WE}$ Low transitions, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).. This parameter is graranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse ((tWP) > tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tWD. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

ORDERING INFORMATION



The following section contains important new data sheets and application notes that were not included in the 1991 SPECIALIZED MEMORIES Data Book.

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 4K (1K x 4-BIT) SRAM

PRELIMINARY
IDT10474
IDT100474
IDT101474

FEATURES:

- 1024-words x 4-bit organization
- Address access time: 7/8/10/15 ns
- Low power dissipation: 600mW (typ.)
- Guaranteed Output Hold time
- Fully compatible with ECL logic levels
- Separate data input and output
- Traditional corner-power pinout
- Standard through-hole and surface mount packages

DESCRIPTION:

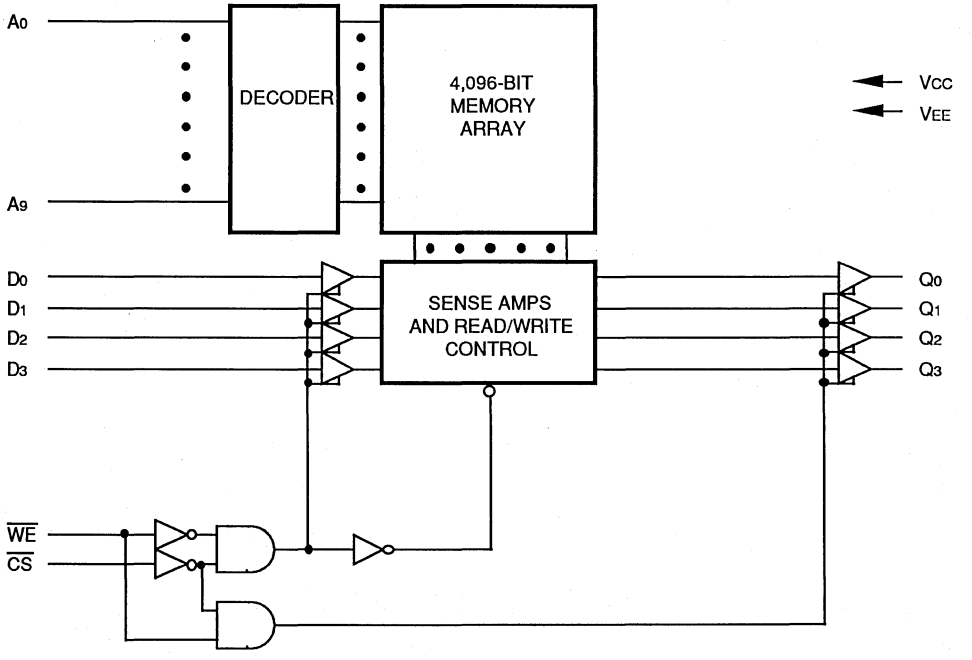
The IDT10474, IDT100474 and 101474 are 4,096-bit high-speed BiCEMOS™ ECL static random access memories organized as 1Kx4, with separate data inputs and outputs. All I/Os are fully compatible with ECL levels.

These devices are part of a family of asynchronous four-bit-wide ECL SRAMs. This device have been configured to follow the traditional corner-power pinout. Because they are manufactured in BiCEMOS™ technology, however, power dissipation is greatly reduced over equivalent bipolar devices.

The asynchronous SRAMs are the most straightforward to use because no additional clocks or controls are required: DataOUT is available an access time after the last change of address. To write data into the device requires the creation of a Write Pulse, and the write cycle disables the output pins in conventional fashion.

The fast access time and guaranteed Output Hold time allow greater margin for system timing variation. DataIN setup time specified with respect to the trailing edge of Write Pulse eases write timing allowing balanced Read and Write cycle times.

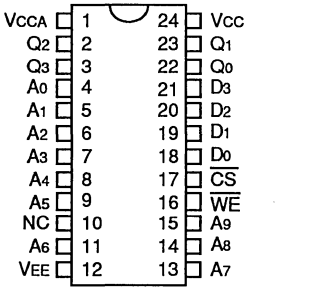
FUCNTIONAL BLOCK DIAGRAM



2758 drw 01

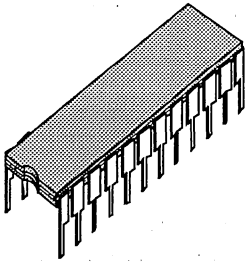
BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



2758 drw 02

TOP VIEW



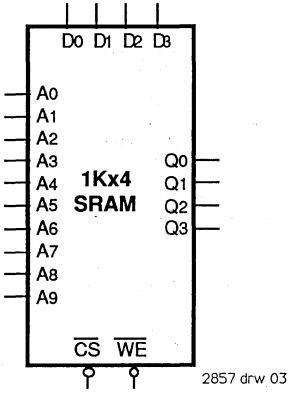
400-Mil-Wide
CERDIP PACKAGE
D24

PIN DESCRIPTIONS

Symbol	Pin Name
A0 through A9	Address Inputs
D0 through D3	Data Inputs
Q0 through Q3	Data Outputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select Input (Internal pull down)
VEE	More Negative Supply Voltage
VCC	Less Negative Supply Voltage

2758 tbl 01

LOGIC SYMBOL



2857 drw 03

AC OPERATING RANGES(1)

I/O	VEE	Temperature
10K	-5.2V ± 5%	0 to 75°C, air flow exceeding 2 m/sed
100K	-4.5V ± 5%	0 to 85°C, air flow exceeding 2 m/sed
101K	-4.75V ± -5.46V	0 to 75°C, air flow exceeding 2 m/sed

2758 tbl 02

NOTE:
1. Referenced to VCC.

CAPACITANCE (TA=+25°C, f=1.0MHz)

Symbol	Parameter	DIP		Unit
		Typ.	Max.	
CIN	Input Capacitance	4	—	pF
COUT	Output Capacitance	6	—	pF

2758 tbl 03

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	DATAOUT	FUNCTION
H	X	L	Deselected
L	H	RAM Data	Read
L	L	L	Write

NOTE:
1. H=High, L=Low, X=Don't Care

2758 tbl 04

B

ECL-10K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2758 tbl 05

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-10K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L=50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit	T_A
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	V_{IN} = V_{IHB} or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	V_{IN} = V_{IHB} or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	V_{IN} = V_{IHA}	$\overline{CS}$	–	–	220	µA	–
			Others	–	–	110	µA	–
I_{IL}	Input LOW Current	V_{IN} = V_{ILB}	$\overline{CS}$	0.5	–	170	µA	–
			Others	-50	–	90	µA	–
I_{EE}	Supply Current	All Inputs and Outputs Open		-190	-130	–	mA	–

2758 tbl 06

NOTE:

1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

ECL-100K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +85	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2758 tbl 07

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-100K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.5V, R_L = 50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-170	-110	–	mA

2758 tbl 08

NOTE:
1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.

B

ECL-101K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2758 tbl 09

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

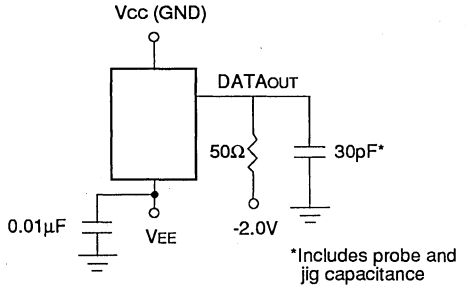
ECL-101K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L = 50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

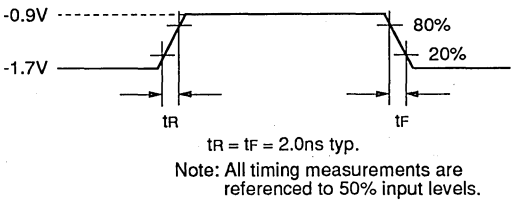
Symbol	Parameter	Test Condition		Min. (B)	Typ.[1]	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-190	-130	–	mA

2758 tbl 10

AC TEST LOAD CONDITION



AC TEST INPUT PULSE



Note: All timing measurements are referenced to 50% input levels.

RISE/FALL TIME

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
tR	Output Rise Time	–	–	2	–	ns
tF	Output Fall Time	–	–	2	–	ns

2758 tbl 11

FUNCTIONAL DESCRIPTION

The IDT10474, IDT100474, and IDT101474 BiCMOS ECL static RAMs (SRAM) provide high speed with low power dissipation typical of BiCMOS ECL. These devices follow the traditional corner-power pinout and functionality for 1Kx4 ECL SRAMs. (For center-power pinouts, please see the IDT10A474, IDT100A474, and IDT101A474, respectively.)

READ TIMING

The read timing on these asynchronous devices is straightforward. DataOUT is held low until the device is selected by Chip Select ($\overline{CS}$). Then Address (ADDR) settles and data appears on the output after time tAA. Note that DataOUT is held for a short time (tOH) after the address begins to change for the next access, then ambiguous data is on the bus until a new time tAA.

WRITE TIMING

To write data to the device, a Write Pulse need be formed on the Write Enable input ($\overline{WE}$) to control the write to the SRAM array. While $\overline{CS}$ and ADDR must be set-up when $\overline{WE}$ goes low, DataIN can settle after the falling edge of $\overline{WE}$, giving the data path extra margin. Data is written to the memory cell at the end of the Write Pulse, and addresses and Chip Select must be held after the rising edge of the Write Pulse to ensure satisfactory completion of the cycle.

DataOUT is disabled (held low) during the Write Cycle. If $\overline{CS}$ is held low (active) and addresses remain unchanged, the DataOUT pins will output the written data after "Write Recovery Time" (tWR).

Because of the very short Write Pulse requirement, these devices can be cycled as quickly for Writes as for Reads. Balanced cycles mean simpler timing in cache applications.

B

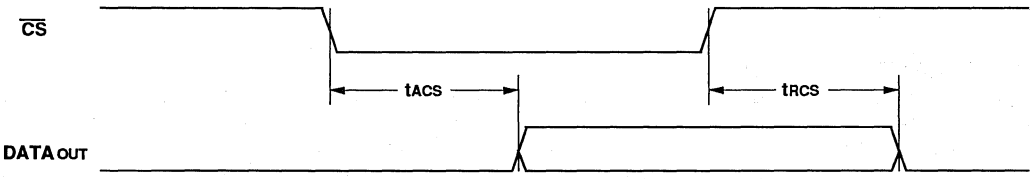
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10474S7 100474S7 101474S7		10474S8 100474S8 101474S8		10474S10 100474S10 101474S10		10474S15 100474S15 101474S15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle											
tACS	Chip Select Access Time	–	–	3	–	5	–	5	–	5	ns
tRCS	Chip Select Recovery Time	–	–	3	–	5	–	5	–	5	ns
tAA	Address Access Time	–	–	7	–	8	–	10	–	15	ns
tOH	Data Hold from Address Change	–	3	–	3	–	3	–	3	–	ns

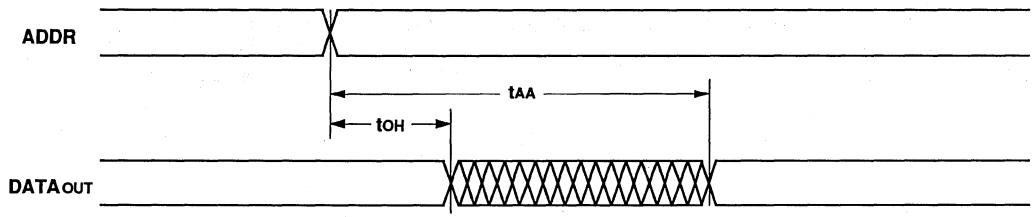
2758 tbl 12

NOTE:
1. Input and Output reference level is 50% point of waveform.

READ CYCLE GATED BY CHIP SELECT



READ CYCLE GATED BY ADDRESS



2758 drw 04

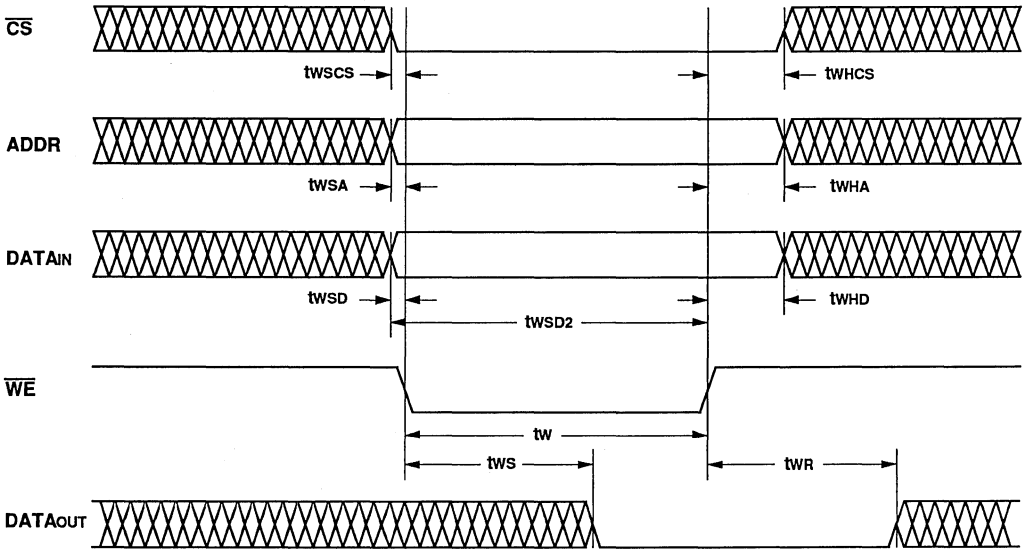
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10474S7 100474S7 101474S7		10474S8 100474S8 101474S8		10474S10 100474S10 101474S10		10474S15 100474S15 101474S15		Unit
			Mlin.	Max.	Mlin.	Max.	Mlin.	Max.	Mlin.	Max.	
Write Cycle											
tW	Write Pulse Width	tWSA= minimum	6	–	7	–	8	–	10	–	ns
tWSD	Data Set-up Time	–	0	–	0	–	0	–	2	–	ns
tWSD2[2]	Data Set-up Time to $\overline{WE}$ High	–	5	–	5	–	5	–	5	–	ns
tWSA	Address Set-up Time	tWSA= minimum	0	–	0	–	0	–	2	–	ns
tWSCS	Chip Select Set-up Time	–	0	–	0	–	0	–	2	–	ns
tWHD	Data Hold Time	–	1	–	1	–	1	–	2	–	ns
tWHA	Address Hold Time	–	1	–	1	–	1	–	2	–	ns
tWHCS	Chip Select Hold Time	–	1	–	1	–	1	–	2	–	ns
tWS	Write Disable Time	–	–	5	–	5	–	5	–	5	ns
tWR[3]	Write Recovery Time	–	–	5	–	5	–	5	–	5	ns

2758 tbl 13

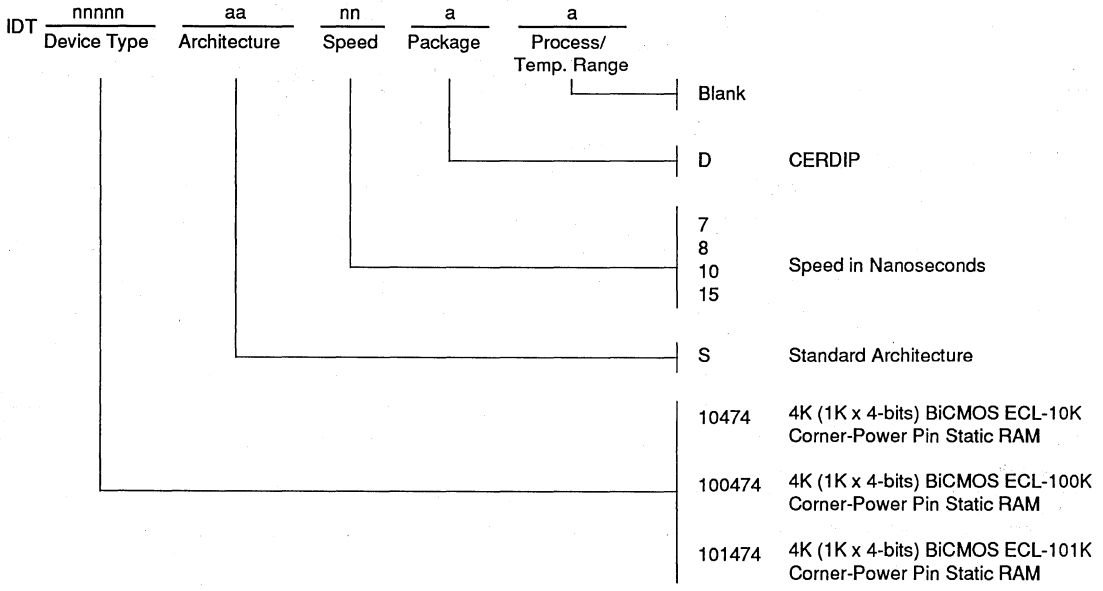
NOTES:
1. Input and Output reference level is 50% point of waveform.
2. tWSD is specified with respect to the falling edge of $\overline{WE}$ for compatibility with bipolar part specifications, but this device actually only requires tWSD2 with respect to rising edge of $\overline{WE}$.
3. tWR is defined as the time to reflect the newly written data on the Data Outputs (Q0 to Q3) when no new Address Transition occurs.

WRITE CYCLE TIMING DIAGRAM



2758 drw 05

ORDERING INFORMATION



2758 drw 06

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 4K (1K x 4-BIT) SRAM

PRELIMINARY
IDT10A474
IDT100A474
IDT101A474

FEATURES:

- 1024-words x 4-bit organization
- Address access time: 5/7/8/10/15 ns
- Low power dissipation: 600mW (typ.)
- Guaranteed Output Hold time
- Fully compatible with ECL logic levels
- Separate data input and output
- Center-power pin pinout for reduced noise
- Standard through-hole and surface mount packages

DESCRIPTION:

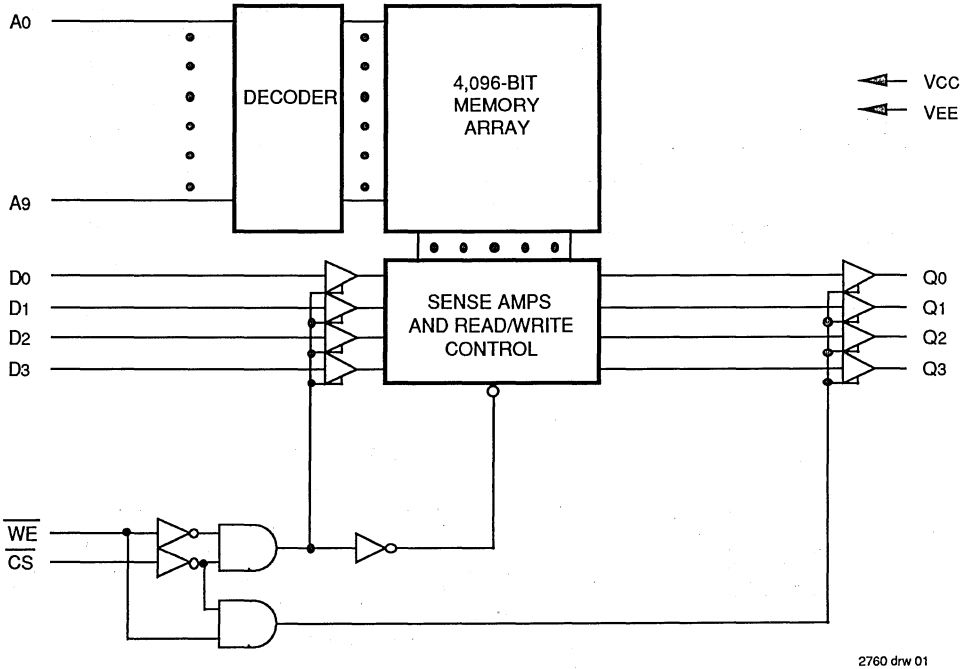
The IDT10A474, IDT100A474 and 101A474 are 4,096-bit high-speed BiCEMOS™ ECL static random access memories organized as 1Kx4, with separate data inputs and outputs. All I/Os are fully compatible with ECL levels.

These devices are part of a family of asynchronous four-bit-wide ECL SRAMs. This device have been configured to follow the center-power pinout for reduced noise allowing higher speed operation. Because they are manufactured in BiCEMOS™ technology, however, power dissipation is greatly reduced over equivalent bipolar devices.

The asynchronous SRAMs are the most straightforward to use because no additional clocks or controls are required: DataOUT is available an access time after the last change of address. To write data into the device requires the creation of a Write Pulse, and the write cycle disables the output pins in conventional fashion.

The fast access time and guaranteed Output Hold time allow greater margin for system timing variation. DataIN setup time specified with respect to the trailing edge of Write Pulse eases write timing allowing balanced Read and Write cycle times.

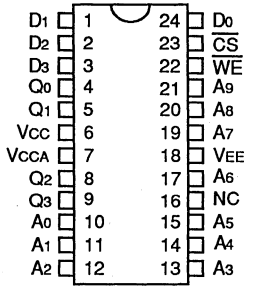
FUNCTIONAL BLOCK DIAGRAM



2760 drw 01

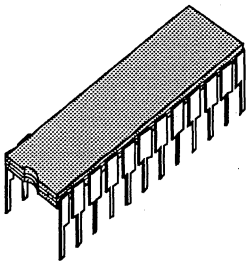
BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



2760 drw 02

TOP VIEW



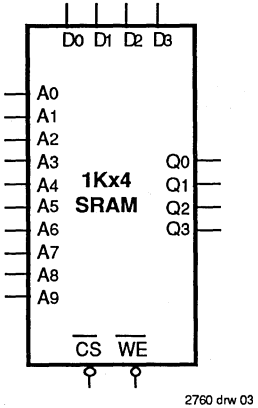
400-Mil-Wide
CERDIP PACKAGE
D24

PIN DESCRIPTIONS

Symbol	Pin Name
A0 through A9	Address Inputs
D0 through D3	Data Inputs
Q0 through Q3	Data Outputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select Input (Internal pull down)
VEE	More Negative Supply Voltage
VCC	Less Negative Supply Voltage

2760 tbl 01

LOGIC SYMBOL



2760 drw 03

AC OPERATING RANGES(1)

I/O	VEE	Temperature
10K	-5.2V ± 5%	0 to 75°C, air flow exceeding 2 m/sed
100K	-4.5V ± 5%	0 to 85°C, air flow exceeding 2 m/sed
101K	-4.75V ± -5.46V	0 to 75°C, air flow exceeding 2 m/sed

NOTE:
1. Referenced to VCC.

2760 tbl 02

CAPACITANCE (TA=+25°C, f=1.0MHz)

Symbol	Parameter	DIP Typ.	DIP Max.	Unit
CIN	Input Capacitance	4	—	pF
COUT	Output Capacitance	6	—	pF

2760 tbl 03

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	DATAOUT	FUNCTION
H	X	L	Deselected
L	H	RAM Data	Read
L	L	L	Write

NOTE:
1. H=High, L=Low, X=Don't Care

2760 tbl 04

ECL-10K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2760 tbl 05

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-10K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L=50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit	T_A
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	V_{IN} = V_{IHB} or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	V_{IN} = V_{IHB} or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	V_{IN} = V_{IHA}	$\overline{CS}$	–	–	220	µA	–
			Others	–	–	110	µA	–
I_{IL}	Input LOW Current	V_{IN} = V_{ILB}	$\overline{CS}$	0.5	–	170	µA	–
			Others	-50	–	90	µA	–
I_{EE}	Supply Current	All Inputs and Outputs Open		-190	-130	–	mA	–

2760 tbl 06

NOTE:
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

B

ECL-100K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +85	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2760 tbl 07

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-100K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.5V, R_L = 50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-170	-110	–	mA

2760 tbl 08

NOTE:
1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.

ECL-101K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2760 tbl 09

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-101K DC ELECTRICAL CHARACTERISTICS

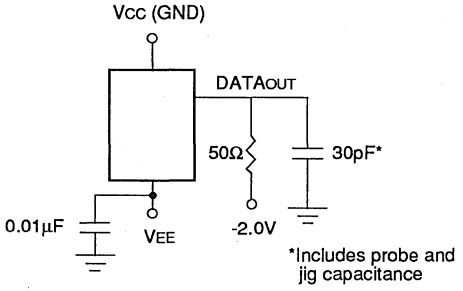
(V_{EE} = -5.2V, R_L = 50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Condition		Min. (B)	Typ.[1]	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-190	-130	–	mA

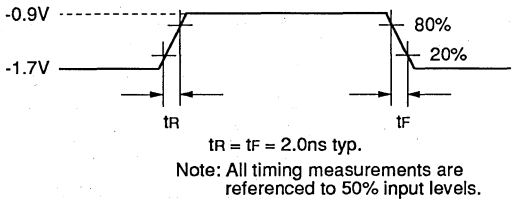
2760 tbl 10

B

AC TEST LOAD CONDITION



AC TEST INPUT PULSE



tR = tF = 2.0ns typ.

Note: All timing measurements are referenced to 50% input levels.

RISE/FALL TIME

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
tR	Output Rise Time	–	–	2	–	ns
tF	Output Fall Time	–	–	2	–	ns

2760 tbl 11

FUNCTIONAL DESCRIPTION

The IDT10A474, IDT100A474, and IDT101A474 BiCMOS ECL static RAMs (SRAM) provide high speed with low power dissipation typical of BiCMOS ECL. These devices follow the center-power pinout and functionality for 1Kx4 ECL SRAMs, reducing noise over corner-power versions allowing for improved system performance. (For corner-power pinouts, please see the IDT10474, IDT100474, and IDT101474, respectively.)

READ TIMING

The read timing on these asynchronous devices is straightforward. DataOUT is held low until the device is selected by Chip Select ($\overline{CS}$). Then Address (ADDR) settles and data appears on the output after time tAA. Note that DataOUT is held for a short time (tOH) after the address begins to change for the next access, then ambiguous data is on the bus until a new time tAA.

WRITE TIMING

To write data to the device, a Write Pulse need be formed on the Write Enable input ($\overline{WE}$) to control the write to the SRAM array. While $\overline{CS}$ and ADDR must be set-up when $\overline{WE}$ goes low, DataIN can settle after the falling edge of $\overline{WE}$, giving the data path extra margin. Data is written to the memory cell at the end of the Write Pulse, and addresses and Chip Select must be held after the rising edge of the Write Pulse to ensure satisfactory completion of the cycle.

DataOUT is disabled (held low) during the Write Cycle. If $\overline{CS}$ is held low (active) and addresses remain unchanged, the DataOUT pins will output the written data after "Write Recovery Time" (tWR).

Because of the very short Write Pulse requirement, these devices can be cycled as quickly for Writes as for Reads. Balanced cycles mean simpler timing in cache applications.

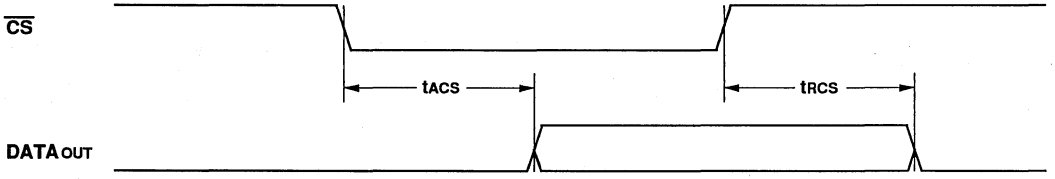
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10A474S5 100A474S5 101A474S5		10A474S7 100A474S7 101A474S7		10A474S8 100A474S8 101A474S8		10A474S10 100A474S10 101A474S10		10A474S15 100A474S15 101A474S15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle													
tACS	Chip Select Access Time	–	–	2.5	–	3	–	5	–	5	–	5	ns
tRCS	Chip Select Recovery Time	–	–	2.5	–	3	–	5	–	5	–	5	ns
tAA	Address Access Time	–	–	5	–	7	–	8	–	10	–	15	ns
tOH	Data Hold from Address Change	–	2	–	3	–	3	–	3	–	3	–	ns

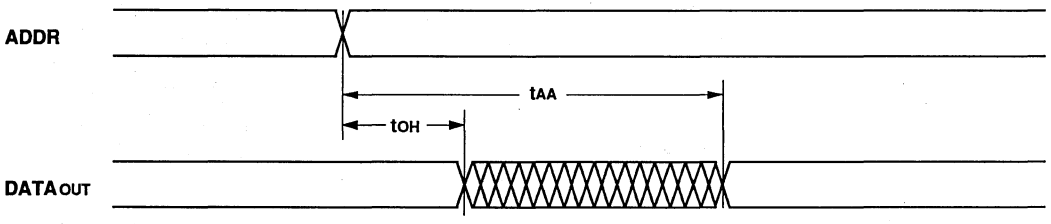
2760 tbl 12

NOTE:
1. Input and Output reference level is 50% point of waveform.

READ CYCLE GATED BY CHIP SELECT



READ CYCLE GATED BY ADDRESS



2760 drw 04

B

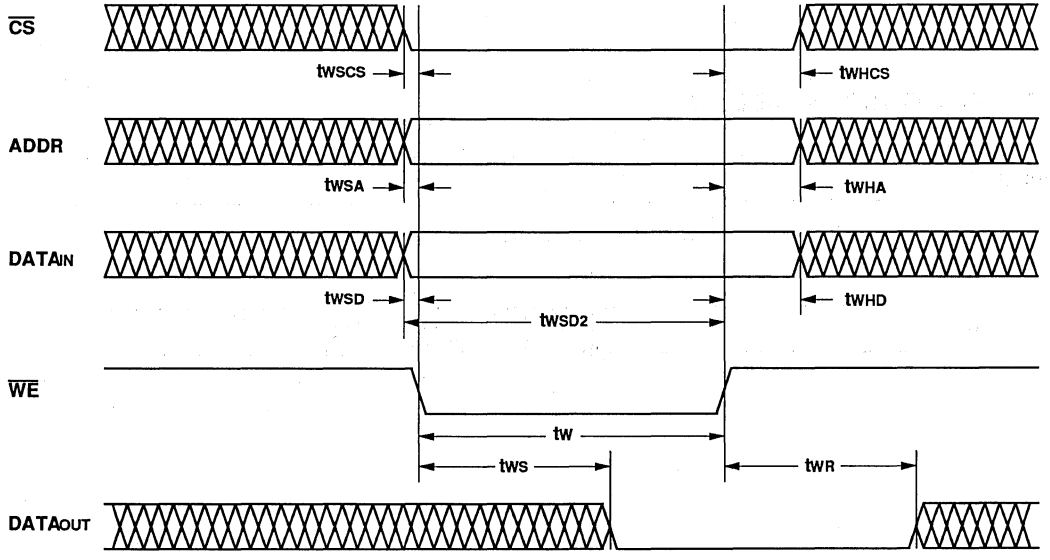
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10A474S5 100A474S5 101A474S5		10A474S7 100A474S7 101A474S7		10A474S8 100A474S8 101A474S8		10A474S10 100A474S10 101A474S10		10A474S15 100A474S15 101A474S15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle													
tW	Write Pulse Width	tWSA= minimum	4	–	6	–	7	–	8	–	10	–	ns
tWSD	Data Set-up Time	–	0	–	0	–	0	–	0	–	2	–	ns
tWSD2[2]	Data Set-up Time to $\overline{WE}$ High	–	3	–	5	–	5	–	5	–	5	–	ns
tWSA	Address Set-up Time	tWSA= minimum	0	–	0	–	0	–	0	–	2	–	ns
tWSCS	Chip Select Set-up Time	–	0	–	0	–	0	–	0	–	2	–	ns
tWHD	Data Hold Time	–	1	–	1	–	1	–	1	–	2	–	ns
tWHA	Address Hold Time	–	1	–	1	–	1	–	1	–	2	–	ns
tWHCS	Chip Select Hold Time	–	1	–	1	–	1	–	1	–	2	–	ns
tWS	Write Disable Time	–	–	3	–	5	–	5	–	5	–	5	ns
tWR[3]	Write Recovery Time	–	–	3	–	5	–	5	–	5	–	5	ns

2760 tbl 13

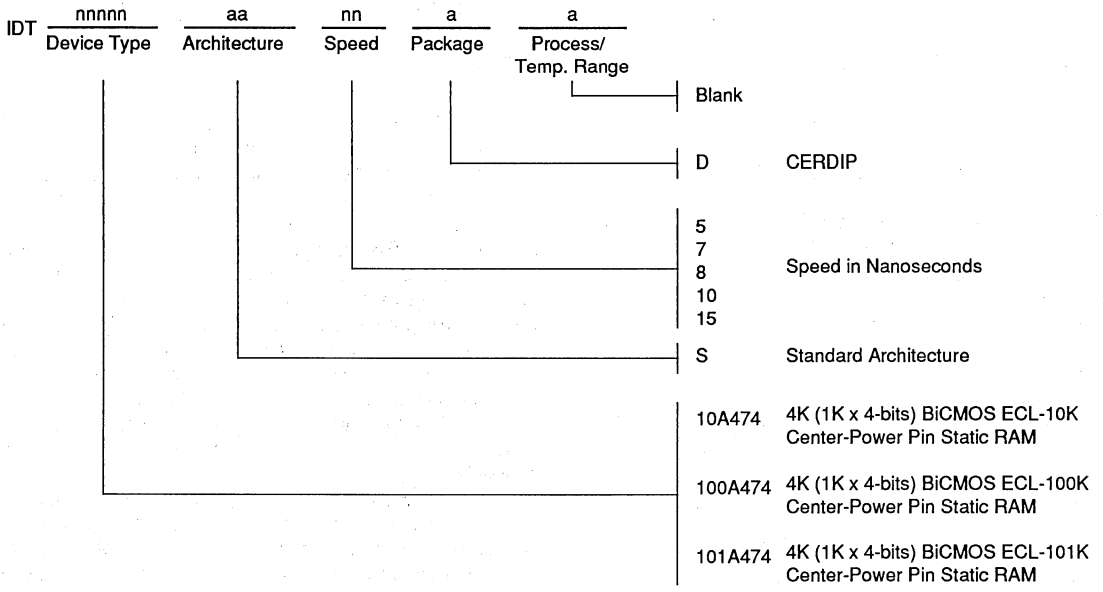
NOTES:
1. Input and Output reference level is 50% point of waveform.
2. tWSD is specified with respect to the falling edge of $\overline{WE}$ for compatibility with bipolar part specifications, but this device actually only requires tWSD2 with respect to rising edge of $\overline{WE}$.
3. tWR is defined as the time to reflect the newly written data on the Data Outputs (Q_0 to Q_3) when no new Address Transition occurs.

WRITE CYCLE TIMING DIAGRAM



2760 drw 05

ORDERING INFORMATION



2760 drw 06

B

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 16K (16K x 1-BIT) SRAM

IDT10480
IDT100480
IDT101480

FEATURES:

- 16,384-words x 1-bit organization
- Address access time: 8/10/12/15
- Low power dissipation: 420mW (typ.)
- Guaranteed Output Hold time
- Fully compatible with ECL logic levels
- Separate data input and output
- JEDEC standard through-hole and surface mount packages

DESCRIPTION:

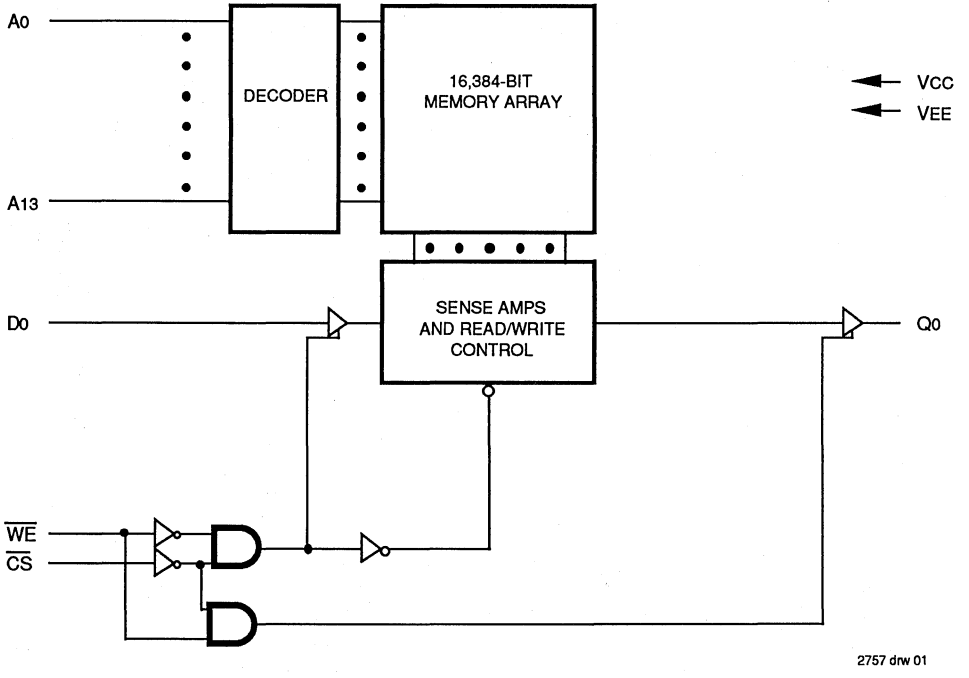
The IDT10480, IDT100480 and IDT101480 are 16,384-bit high-speed BiCEMOS™ ECL static random access memories organized as 16K x 1, with separate data inputs and outputs. All I/Os are fully compatible with ECL levels.

These devices are part of a family of asynchronous one-bit-wide ECL SRAMs. The devices have been configured to follow the standard ECL SRAM JEDEC pinout. Because they are manufactured in BiCEMOS™ technology, however, power dissipation is greatly reduced over equivalent bipolar devices.

The asynchronous SRAMs are the most straightforward to use because no additional clocks or controls are required: $Data_{OUT}$ is available an access time after the last change of address. To write data into the device requires the creation of a Write Pulse, and the write cycle disables the output pins in conventional fashion.

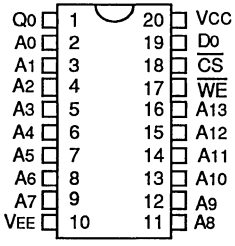
The fast access time and guaranteed Output Hold time allow greater margin for system timing variation. $Data_{IN}$ setup time specified with respect to the trailing edge of Write Pulse eases write timing allowing balanced Read and Write cycle times.

FUNCTIONAL BLOCK DIAGRAM



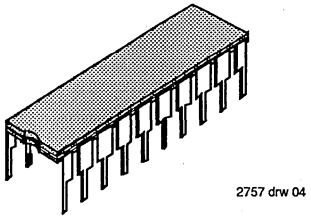
BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



2757 drw 02

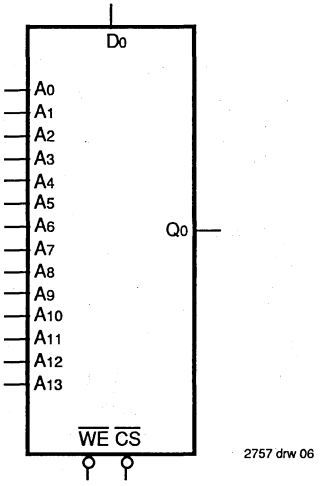
CERDIP
TOP VIEW



2757 drw 04

300-Mil-Wide
CERDIP PACKAGE
D20

LOGIC SYMBOL



2757 drw 06

64Kx1
SRAM

PIN DESCRIPTIONS

Symbol	Pin Name
A0 through A13	Address Inputs
D0	Data Input
Q0	Data Output
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input (Internal pull down)
VEE	More Negative Supply Voltage
VCC	Less Negative Supply Voltage

2757 tbl 01

CAPACITANCE (TA =+25°C, f=1.0MHz)

Symbol	Parameter	DIP Typ.	DIP Max.	FP Typ.	FP Max.	Unit
CIN	Input Capacitance	4	–	TBD	–	pF
COUT	Output Capacitance	6	–	TBD	–	pF

2757 tbl 03

AC OPERATING RANGES(1)

I/O	VEE	Temperature
10K	-5.2V ±5%	0 TO 75°C, air flow exceeding 2 m/sed
100K	-4.5V ±5%	0 TO 85°C, air flow exceeding 2 m/sed
101K	-4.75V to -5.46V	0 TO 75°C, air flow exceeding 2 m/sed

2757 tbl 02

NOTE:
1. Referenced to Vcc

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	Data OUT	Function
H	X	L	Deselected
L	H	RAM Data	Read
L	L	L	Write

2757 tbl 04

NOTE:
1. H=High, L=Low, X=Don't Care

ECL-10K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
VTERM	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
TA	Operating Temperature		0 to +75	°C
TBIAS	Temperature Under Bias		-55 to +125	°C
TSTG	Storage Temperature	Ceramic Plastic	-65 to +150 -55 to +125	°C
PT	Power Dissipation		1.5	W
IOUT	DC Output Current (Output High)		-50	mA

2757 tbl 05

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-10K DC ELECTRICAL CHARACTERISTICS

(VEE = -5.2V, RL =50Ω to -2.0V, TA = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit	TA
VOH	Output HIGH Voltage	VIN = VIHA or VILB		-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
VOL	Output LOW Voltage	VIN = VIHA or VILB		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
VOHC	Output Threshold HIGH Voltage	VIN = VIHB or VILA		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
VOLC	Output Threshold LOW Voltage	VIN = VIHB or VILA		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
VIH	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
VIL	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I IH	Input HIGH Current	VIN = VIHA	$\overline{CS}$	–	–	220	µA	–
			Others	–	–	110	µA	–
I IL	Input LOW Current	VIN = VILB	$\overline{CS}$	0.5	–	170	µA	–
			Others	-50	–	90	µA	–
IEE	Supply Current	All Inputs and Outputs Open		-170	-80	–	mA	–

2757 tbl 06

NOTE:

1. Typical parameters are specified at VEE = -5.2V, TA = +25°C and maximum loading.

ECL-100K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +85	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Out mput Current (Output High)		-50	mA

2757 tbl 07

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-100K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.5V, R_L =50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-150	-70	–	mA

2757 tbl 08

NOTE:
1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.

B

ECL-101K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.0	W
I_{OUT}	DC Out mput Current (Output High)		-50	mA

2757 tbl 09

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-101K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L=50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

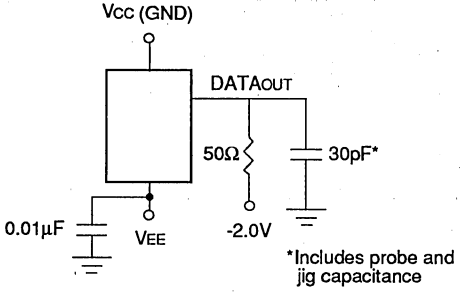
Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-170	-80	–	mA

2757 tbl 10

NOTE:

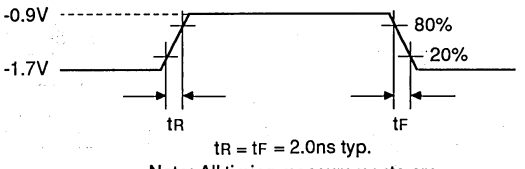
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

AC TEST LOAD CONDITION



2757 drw 07

AC TEST INPUT PULSE



Note: All timing measurements are referenced to 50% input levels.

2757 drw 08

RISE/FALL TIME

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
tR	Output Rise Time	–	–	2	–	ns
tF	Output Fall Time	–	–	2	–	ns

2757 tbl 11

FUNCTIONAL DESCRIPTION

The IDT10480, IDT100480 and IDT101480 BiCMOS ECL static RAMs (SRAM) provide high speed with low power dissipation typical of BiCMOS ECL. These devices follow the conventional pinout and functionality for 16Kx1 SRAMs. The ECL -101K meets electrical specifications that combine the ECL-100K temperature and voltage compensated output levels with the high-speed of ECL-10K VEE compatibility (-5.2V).

READ TIMING

The read timing on these asynchronous devices is straightforward. DataOUT is held low until the device is selected by Chip Select ($\overline{CS}$). Then Address (ADDR) settles and data appears on the output after time tAA. Note that DataOUT is held for a short time (tOH) after the address begins to change for the next access, then ambiguous data is on the bus until a new time tAA.

WRITE TIMING

To write data to the device, a Write Pulse need be formed on the Write Enable input ($\overline{WE}$) to control the write to the SRAM array. While $\overline{CS}$ and ADDR must be set-up when $\overline{WE}$ goes low, DataIN can settle after the falling edge of $\overline{WE}$, giving the data path extra margin. Data is written to the memory cell at the end of the Write Pulse, and addresses and Chip Select must be held after the rising edge of the Write Pulse to ensure satisfactory completion of the cycle.

DataOUT is disabled (held low) during the Write Cycle. If $\overline{CS}$ is held low (active) and addresses remain unchanged, the DataOUT pins will output the written data after "Write Recovery Time" (tWR).

Because of the very short Write Pulse requirement, these devices can be cycled as quickly for Writes as for Reads. Balanced cycles mean simpler timing in cache applications.

B

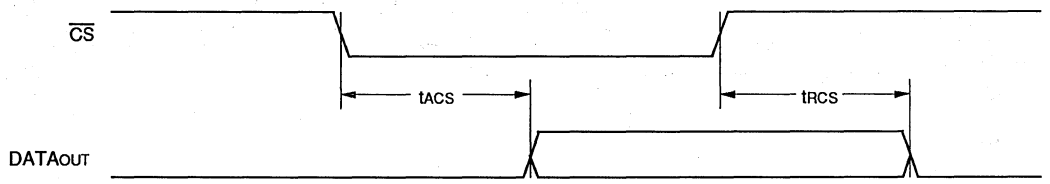
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10480S8 100480S8 101480S8		10480S10 100480S10 101480S10		10480S12 100480S12 101480S12		10480S15 100480S15 101480S15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle											
tACS	Chip Select Access Time	–	–	3	–	5	–	5	–	5	ns
tRCS	Chip Select Recovery Time	–	–	3	–	5	–	5	–	5	ns
tAA	Address Access Time	–	–	8	–	10	–	12	–	15	ns
tOH	Data Hold from Address Change	–	3	–	3.5	–	3.5	–	3.5	–	ns

NOTES:
1. Input and Output reference level is 50% point of waveform.

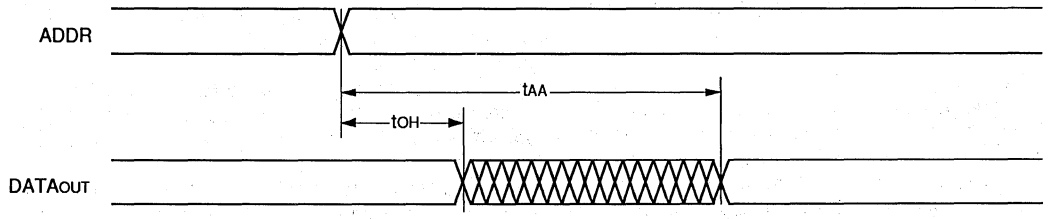
2757 tbl 12

READ CYCLE GATED BY CHIP SELECT



2757 drw 09

READ CYCLE GATED BY ADDRESS



2757 drw 10

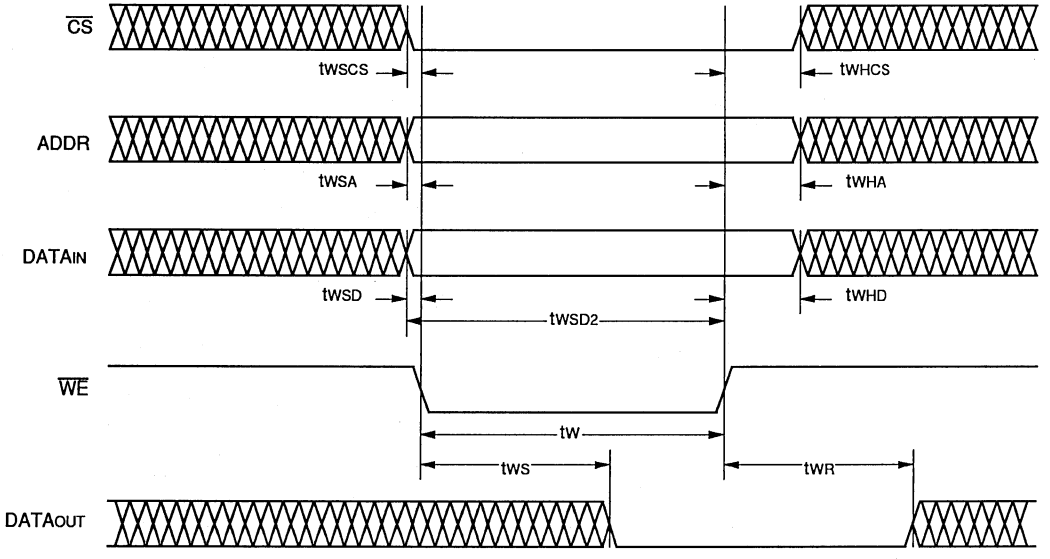
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10480S8 100480S8 101480S8		10480S10 100480S10 101480S10		10480S12 100480S12 101480S12		10480S15 100480S15 101480S15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle											
tW	Write Pulse Width	tWSA = minimum	7	–	9	–	10	–	10	–	ns
tWSD	Data Set-up Time	–	0	–	0	–	0	–	2	–	ns
tWSD2[2]	Data Set-up Time to $\overline{WE}$ High	–	5	–	5	–	5	–	5	–	ns
tWSA	Address Set-up Time	tWSA = minimum	0	–	0	–	0	–	2	–	ns
tWSCS	Chip Select Set-up Time	–	0	–	0	–	0	–	2	–	ns
tWHD	Data Hold Time	–	1	–	1	–	2	–	3	–	ns
tWHA	Address Hold Time	–	1	–	1	–	2	–	3	–	ns
tWHCS	Chip Select Hold Time	–	1	–	1	–	2	–	3	–	ns
tWS	Write Disable Time	–	–	5	–	5	–	5	–	10	ns
tWR[3]	Write Recovery Time	–	–	10	–	12	–	14	–	18	ns

2757 tbl 13

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. tWSD is specified with respect to the falling edge of $\overline{WE}$ for compatibility with bipolar part specifications, but this device actually only requires tWSD2 with respect to rising edge of $\overline{WE}$.
3. tWR=tWHA + tAA and thus can include a full access time if addresses change while Chip Select is still low.

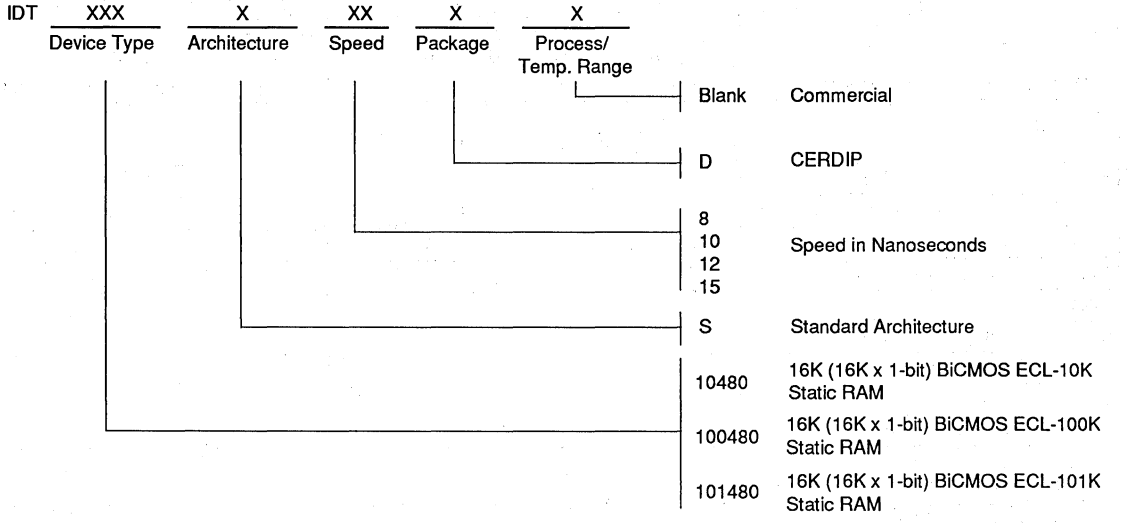
WRITE CYCLE TIMING DIAGRAM



2757 drw 11

B

ORDERING INFORMATION



2757 drw 12

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 1M (256K x 4-BIT) SRAM

PRELIMINARY
IDT10514
IDT100514
IDT101514

FEATURES:

- 262,144-words x 4-bit organization
- Address access time: 10/12/15
- Low power dissipation: 900mW (typ.)
- Guaranteed Output Hold time
- Fully compatible with ECL logic levels
- Separate data input and output
- JEDEC standard through-hole and surface mount packages

DESCRIPTION:

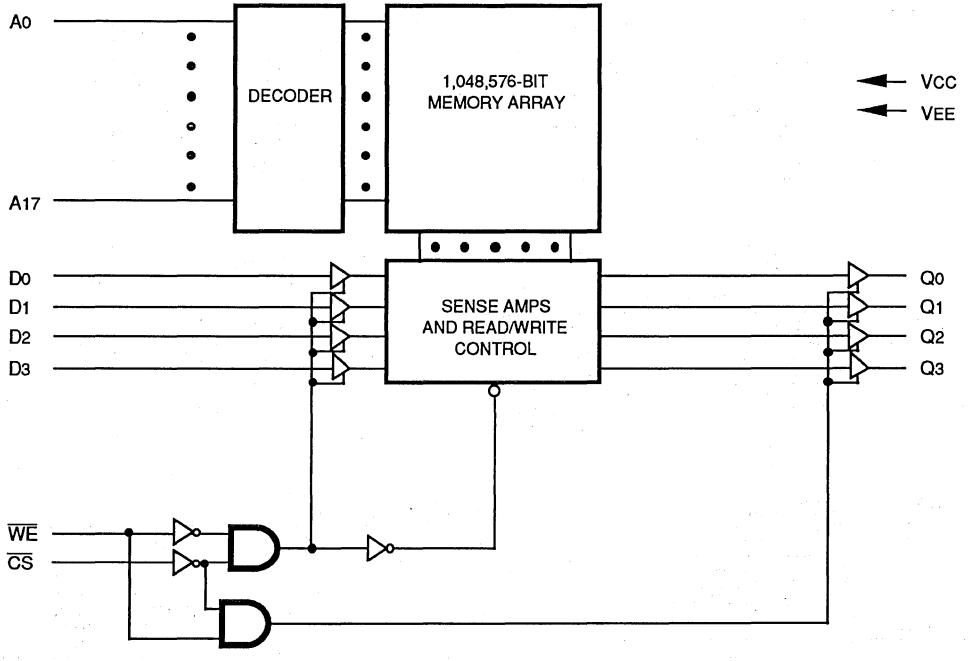
The IDT10514, IDT100514 and IDT101514 are 1,048,576-bit high-speed BiCEMOS™ ECL static random access memories organized as 256Kx4, with separate data inputs and outputs. All I/Os are fully compatible with ECL levels.

These devices are part of a family of asynchronous four-bit-wide ECL SRAMs. The devices have been configured to follow the standard ECL SRAM family pinout. Because they are manufactured in BiCEMOS™ technology, however, power dissipation is greatly reduced over equivalent bipolar devices.

The asynchronous SRAMs are the most straightforward to use because no additional clocks or controls are required: $Data_{OUT}$ is available an access time after the last change of address. To write data into the device requires the creation of a Write Pulse, and the write cycle disables the output pins in conventional fashion.

The fast access time and guaranteed Output Hold time allow greater margin for system timing variation. $Data_{IN}$ setup time specified with respect to the trailing edge of Write Pulse eases write timing allowing balanced Read and Write cycle times.

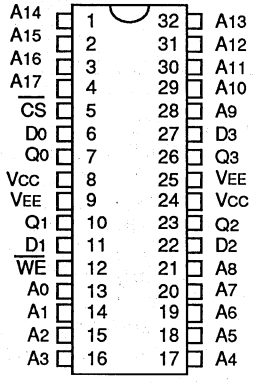
FUNCTIONAL BLOCK DIAGRAM



2780 drw 01

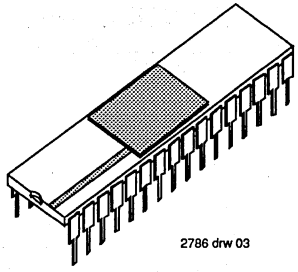
BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



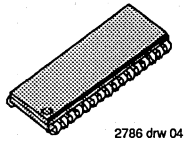
2786 drw 02

TOP VIEW



2786 drw 03

400-Mil-Wide
CERAMIC PACKAGE
C32



2786 drw 04

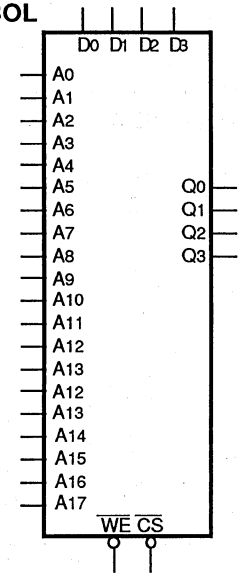
400-Mil-Wide
PLASTIC SOJ PACKAGE
Y32

PIN DESCRIPTION

Symbol	Pin Name
A0 through A17	Address Inputs
D0 through D3	Data Inputs
Q0 through Q3	Data Outputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input (Internal pull down)
VEE	More Negative Supply Voltage
VCC	Less Negative Supply Voltage
NC	No Connect (Not Internally Connected

2786 tbl 01

LOGIC SYMBOL



2786 drw 05

256Kx4
SRAM

AC OPERATING RANGES(1)

I/O	VEE	Temperature
10K	-5.2V ±5%	0 TO 75°C, air flow exceeding 2 m/sec
100K	-4.5V ±5%	0 TO 85°C, air flow exceeding 2 m/sec
101K	-4.75V to -5.46V	0 TO 75°C, air flow exceeding 2 m/sec

2786 tbl 02

NOTE:
1. Referenced to Vcc

CAPACITANCE (TA=+25°C, f=1.0MHz)

Symbol	Parameter	DIP Typ.	DIP Max.	SOJ Typ.	SOJ Max.	Unit
CIN	Input Capacitance	4	–	3	–	pF
COUT	Output Capacitance	6	–	3	–	pF

2786 tbl 03

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	DATAOUT	Function
H	X	L	Deselected
L	H	RAM Data	Read
L	L	L	Write

NOTE:
1. H=High, L=Low, X=Don't Care

2786 tbl 04

ECL-10K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic Plastic	-65 to +150 -55 to +125	°C
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Output Current (Output High)		-50	mA

NOTE: 2786 tbl 05

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-10K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, RL=50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit	T_A
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA	–
			Others	–	–	110	µA	–
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA	–
			Others	-50	–	90	µA	–
I_{EE}	Supply Current	All Inputs and Outputs Open		-260	-180	–	mA	–

NOTE: 2786 tbl 06

1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

B

ECL-100K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +85	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Output Current (Output High)		-50	mA

NOTE: 2786 tbl 07

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-100K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.5V, RL=50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-240	-160	–	mA

NOTES: 2786 tbl 08

1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.

ECL-101K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Out mput Current (Output High)		-50	mA

NOTE: 2786 tbl 09

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-101K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, RL=50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

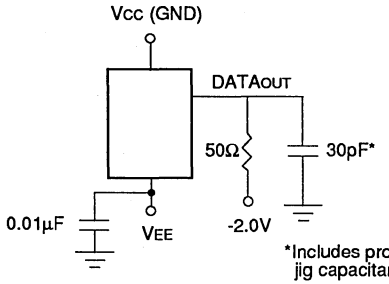
Symbol	Parameter	Test Condition		Min. (B)	Typ.(1)	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-260	-180	–	mA

NOTES: 2786 tbl 10

1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

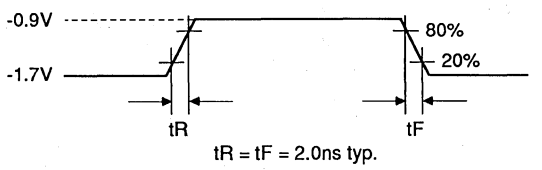
B

AC TEST LOAD CONDITION



2786 drw 06

AC TEST INPUT PULSE



Note: All timing measurements are referenced to 50% input levels.

2786 drw 07

RISE/FALL TIME

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
tR	Output Rise Time	–	–	2	–	ns
tF	Output Fall Time	–	–	2	–	ns

2786 tbl 11

FUNCTIONAL DESCRIPTION

The IDT10514, IDT100514 and IDT101514 BiCMOS ECL static RAMs (SRAM) provide high speed with low power dissipation typical of BiCMOS ECL. These devices follow the JEDEC standard revolutionary pinout. The ECL-101K meets electrical specifications that combine the ECL-100K temperature and voltage compensated output levels with the high-speed of ECL-10K VEE compatibility (-5.2V).

READ TIMING

The read timing on these asynchronous devices is straightforward. DataOUT is held low until the device is selected by Chip Select ($\overline{CS}$). Then Address (ADDR) settles and data appears on the output after time tAA. Note that DataOUT is held for a short time (tOH) after the address begins to change for the next access, then ambiguous data is on the bus until a new time tAA.

WRITE TIMING

To write data to the device, a Write Pulse need be formed on the Write Enable input ($\overline{WE}$) to control the write to the SRAM array. While $\overline{CS}$ and ADDR must be set-up when $\overline{WE}$ goes low, DataIN can settle after the falling edge of $\overline{WE}$, giving the data path extra margin. Data is written to the memory cell at the end of the Write Pulse, and addresses and Chip Select must be held after the rising edge of the Write Pulse to ensure satisfactory completion of the cycle.

DataOUT is disabled (held low) during the Write Cycle. If $\overline{CS}$ is held low (active) and addresses remain unchanged, the DataOUT pins will output the written data after "Write Recovery Time" (tWR).

Because of the very short Write Pulse requirement, these devices can be cycled as quickly for Writes as for Reads. Balanced cycles mean simpler timing in cache applications.

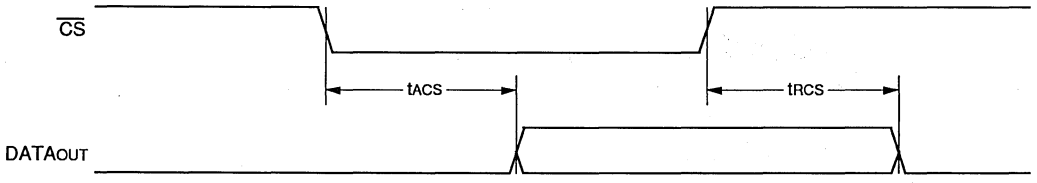
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10514S10 100514S10 101514S10		10514S12 100514S12 101514S12		10514S15 100514S15 101514S15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle									
t_{ACS}	Chip Select Access Time	—	—	5	—	5	—	5	ns
t_{RCS}	Chip Select Recovery Time	—	—	5	—	5	—	5	ns
t_{AA}	Address Access Time	—	—	10	—	12	—	15	ns
t_{OH}	Data Hold from Address Change	—	3	—	3	—	3	—	ns

NOTE:
1. Input and Output reference level is 50% point of waveform.

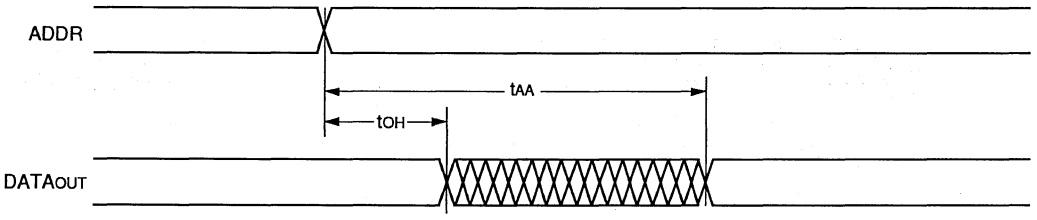
2786 tbl 12

READ CYCLE GATED BY CHIP SELECT



2786 drw 08

READ CYCLE GATED BY ADDRESS



2786 drw 09

B

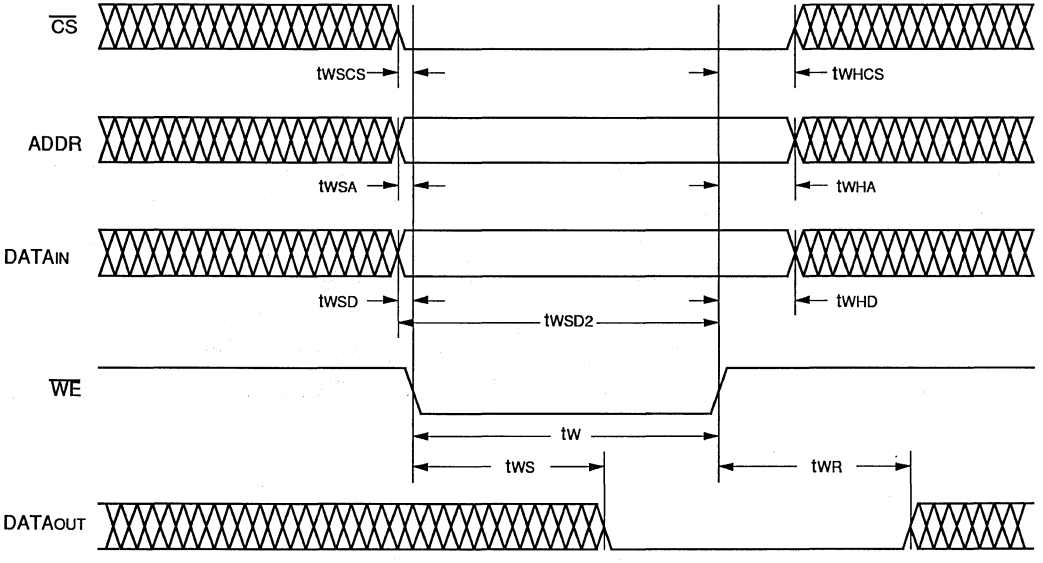
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10514S10 100514S10 101514S10		10514S12 100514S12 101514S12		10514S15 100514S15 101514S15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle									
tW	Write Pulse Width	tWSA = min.	8	—	10	—	10	—	ns
tWSD	Data Set-up Time	—	0	—	0	—	2	—	ns
tWSD2[2]	Data Set-up Time to $\overline{WE}$ High	—	6	—	8	—	8	—	ns
tWSA	Address Set-up Time	tWSA = min.	0	—	0	—	1	—	ns
tWSCS	Chip Select Set-up Time	—	0	—	0	—	1	—	ns
tWHD	Data Hold Time	—	2	—	2	—	2	—	ns
tWHA	Address Hold Time	—	2	—	2	—	2	—	ns
tWHCS	Chip Select Hold Time	—	2	—	2	—	2	—	ns
tWHS	Write Disable Time	—	—	5	—	5	—	5	ns
tWR[3]	Write Recovery Time	—	—	5	—	5	—	5	ns

NOTES:
2786 tbl 13

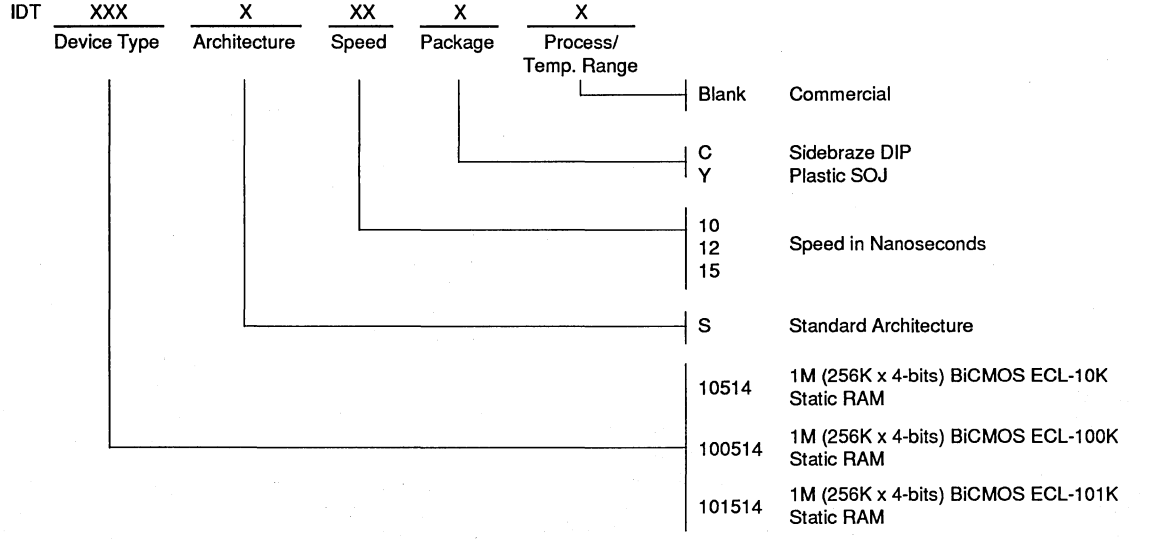
1. Input and Output reference level is 50% point of waveform.
2. tWSD is specified with respect to the falling edge of $\overline{WE}$ for compatibility with bipolar part specifications, but this device actually only requires tWSD2 with respect to rising edge of $\overline{WE}$.
3. tWR is defined as the time to reflect the newly written data on the Data Outputs (Q_0 to Q_3) when no new Address Transition occurs.

WRITE CYCLE TIMING DIAGRAM



2786 drw 10

ORDERING INFORMATION



2786 drw 11

B

Integrated Device Technology, Inc.

SELF-TIMED BiCMOS ECL STATIC RAM 256K (32K x 9-BIT) SRAM

ADVANCE INFORMATION
IDT10596RR
IDT100596RR
IDT101596RR

FEATURES:

- 32,768-words x 9-bit organization
- Self-Timed Write, with registers on inputs and outputs
- Balanced Read/Write cycle time: 10/12/15 ns
- Wide word for reduced address loading
- Differential clock input
- Fully compatible with ECL logic levels
- Separate data input and output
- JEDEC standard pinouts

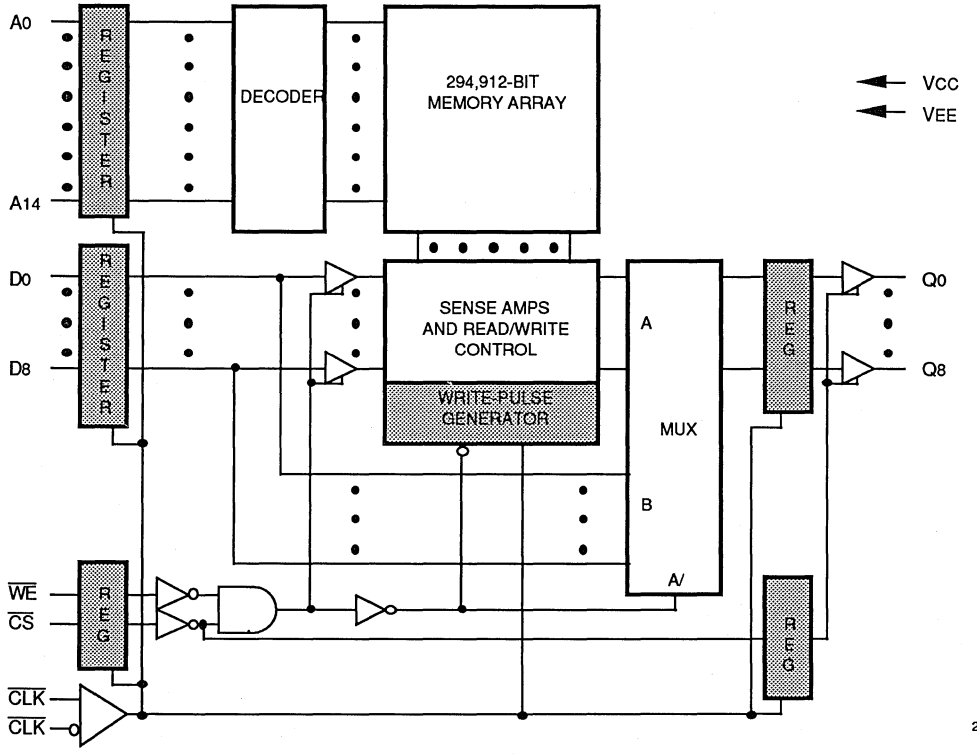
DESCRIPTION:

The IDT10596RR, IDT100596RR, and IDT101596RR are 294,912-bit high-speed BiCEMOS™ ECL self-timed static random access memories (STRAM) organized as 32Kx9, with inputs and outputs fully compatible with ECL levels. Clocked registers on inputs and outputs, and the self-timed write operation, provide enhanced system performance over conventional RAMs, providing easier design and improved system level cycle times.

These devices are part of a family of nine-bit-wide ECL SRAMs. The devices have been configured to follow the proposed ECL SRAM JEDEC pinout. Because they are manufactured in BiCEMOS™ technology, however, power dissipation is similar to CMOS devices of equivalent density. Inputs are captured and outputs gated by the rising edge of an externally supplied differential clock. The small input valid window required means more margin for system skews. Logic-to-memory propagation delay is included in device cycle time calculation, allowing this device to deliver better system performance than asynchronous SRAMs and glue logic.

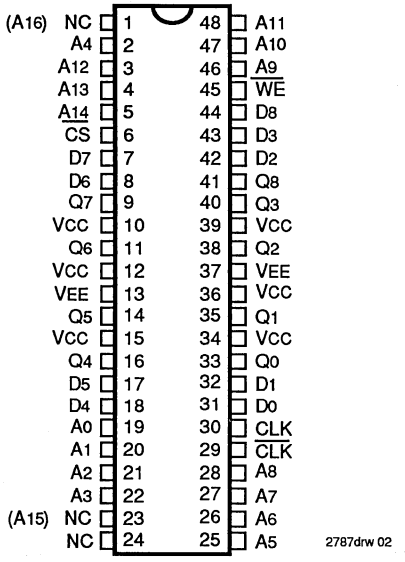
Write timing is controlled internally based on the clock. Write Enable has no special requirements. The device allows balanced read and write cycle times, and reads and writes can be inserted in any order.

FUNCTIONAL BLOCK DIAGRAM

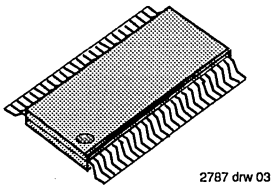


BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION

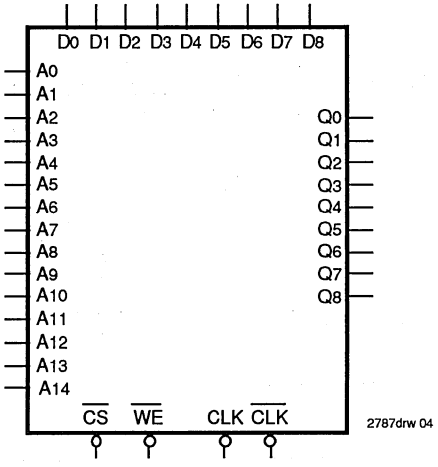


TOP VIEW



300-Mil-Wide
Plastic SSOP Package
48

LOGIC SYMBOL



32Kx9
SRAM

PIN DESCRIPTIONS

Symbol	Pin Name
A0 through A14	Address Inputs
D0 through D8	Data Inputs
Q0 through Q8	Data Outputs
$\overline{CS}$	Chip Select Input (Internal pull down)
$\overline{WE}$	Write Enable Input
CLK, $\overline{CLK}$	Differential Clock Imputs
VEE	More Negative Supply Voltage
VCC	Less Negative Supply Voltage
VCCA	Less Negative Supply Voltage for Output
NC	No Connect (Not internally bonded)

2787 tbl 01

AC OPERATING RANGES(1)

I/O	VEE	Temperature
10K	-5.2V ±5%	0 TO 75°C, air flow exceeding 2 m/sec
100K	-4.5V ±5%	0 TO 85°C, air flow exceeding 2 m/sec
101K	-4.75V to -5.46V	0 TO 75°C, air flow exceeding 2 m/sec

NOTE:
1. Referenced to Vcc

2787 tbl 02

CAPACITANCE (TA=+25°C, f=1.0MHz)

Symbol	Parameter	SSOP Typ.	SSOP Max.	Unit
CIN	Input Capacitance	TBD	–	pF
COUT	Output Capacitance	TBD	–	pF

2787tbl 03

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	CLK	DATAOUT(2)	Function
H	X	↑	L	Deselected
L	H	↑	RAM Data	Read
L	L	↑	WRITE Data	Write

NOTES:
1. H=High, L=Low, X=Don't Care.
2. DATAOUT initiated by next rising CLK.

2787 tbl 04

B

ECL-10K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2787 tbl 05

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this

ECL-10K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L = 50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit	T_A
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA	–
			Others	–	–	110	µA	–
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA	–
			Others	-50	–	90	µA	–
I_{EE}	Supply Current	All Inputs and Outputs Open		-280	-220	–	mA	–

2787 tbl 06

NOTE:
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

ECL-100K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
VTERM	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
TA	Operating Temperature		0 to +85	°C
TBIAS	Temperature Under Bias		-55 to +125	°C
TSTG	Storage Temperature	Ceramic	-65 to +150	°C
PT	Power Dissipation		2.0	W
IOUT	DC Output Current (Output High)		-50	mA

2787 tbl 07

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-100K DC ELECTRICAL CHARACTERISTICS

(VEE = -4.5V, RL = 50Ω to -2.0V, TA = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit
VOH	Output HIGH Voltage	V IN = V IHA or V ILB		-1025	-955	-880	mV
VOL	Output LOW Voltage	V IN = V IHA or V ILB		-1810	-1715	-1620	mV
VOHC	Output Threshold HIGH Voltage	V IN = V IHB or V ILA		-1035	–	–	mV
VOLC	Output Threshold LOW Voltage	V IN = V IHB or V ILA		–	–	-1610	mV
VIH	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
VIL	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I IH	Input HIGH Current	V IN = V IHA	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I IL	Input LOW Current	V IN = V ILB	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
IEE	Supply Current	All Inputs and Outputs Open		-260	-200	–	mA

2787 tbl 08

NOTE:
1. Typical parameters are specified at VEE = -4.5V, TA = +25°C and maximum loading.

B

ECL-101K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2787 tbl 09

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-101K DC ELECTRICAL CHARACTERISTICS

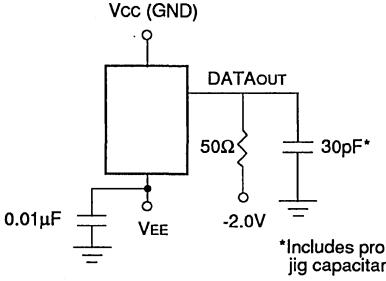
(V_{EE} = -5.2V, R_L = 50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Condition		Min. (B)	Typ.(1)	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-280	-220	–	mA

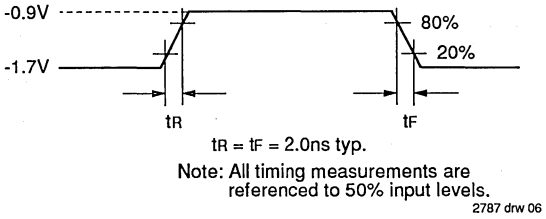
2787 tbl 10

NOTE:
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

AC TEST LOAD CONDITION



AC TEST INPUT PULSE



RISE/FALL TIME

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
tR	Output Rise Time	–	–	2	–	ns
tF	Output Fall Time	–	–	2	–	ns

2787 tbl 11

FUNCTIONAL DESCRIPTION

The IDT10596RR, IDT100596RR, and IDT101596RR Self-Timed BiCMOS ECL static RAMs (STRAM) provide high speed with low power dissipation typical of BiCMOS ECL. On-chip logic additionally helps improve system performance.

As can be seen in the Functional Block Diagram on the title page, this device contains clocked input registers to sample and hold addresses, input data, and control status. Inputs are sampled on the rising edge of the clock (CLK) input (falling edge of $\overline{CLK}$). In the case of a write cycle, the memory cell is written by an internal timer initiated by the rising edge of CLK, and write data conducted to the outputs. Output data is clocked out the output register and is held through the next cycle.

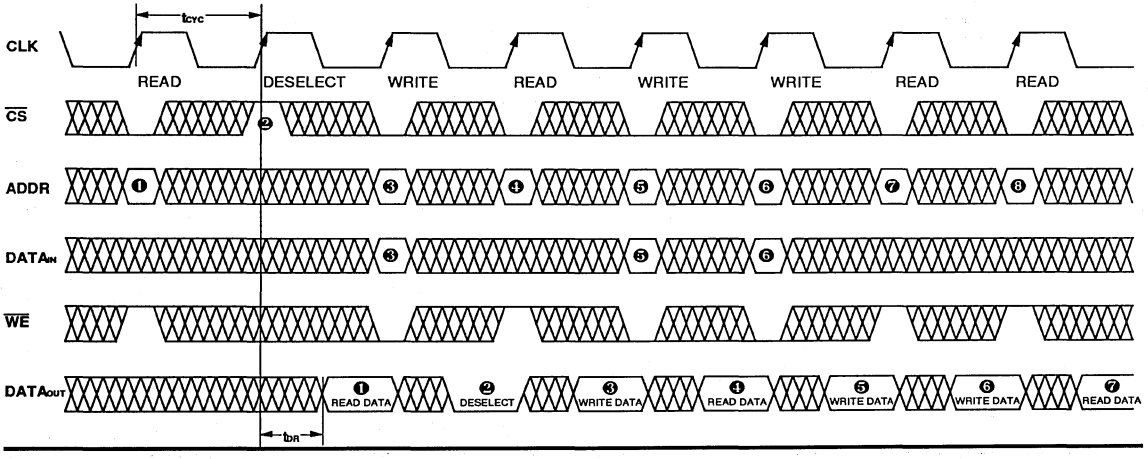
READ TIMING

In a typical read cycle, the read address is captured by the rising edge of clock, as at ❶ below. Then, after access occurs internally, the read data for the read address clocked in at ❶ is clocked through the output register to the output pins by the next rising edge of clock (for this example, at ❷). There is a short delay from rising clock to output ready, called tDR (see Read Cycle Timing).

The output register takes some time to change state for the next output, but this time is very short. Therefore, data hold time from clock high (tDH) is specified as zero minimum hold time.

B

FUNCTIONAL DESCRIPTION TIMING EXAMPLE



DESELECT TIMING

Because the outputs are registered, they will continue to drive the output pins until a disable state is clocked through the device. The deselected state is achieved by de-asserting chip select ($\overline{CS}$ high) at rising edge of clock. This case occurs at ❷ below. Outputs then attain the disable state (low) after the next rising clock edge. Status of other inputs do not effect the disabling of the device when chip select is de-asserted with the proper relation to clock.

WRITE TIMING

Write cycles are identical to read cycles, except that write enable and write data need also be supplied, with the appropriate setup and hold timing. The device has on-chip timing that handles all aspects of writing data into the addressed RAM cell without the need for external write-pulse generation. The timing logic uses an internal timer as the write pulse, and thus only one edge of clock need be determined (de-skewed) exactly.

In addition to writing to the RAM cell, the write data is fed to the output register by a multiplexer, so that write data is available on the output pins in the appropriate time slot (i.e. after the next clock high edge). This function is sometimes called "Transparent Write," and is useful for write-through cache applications. Thus the input data sampled at ❸ is available on the output in the next cycle.

There are no restrictions on the order of read cycles and write cycles.

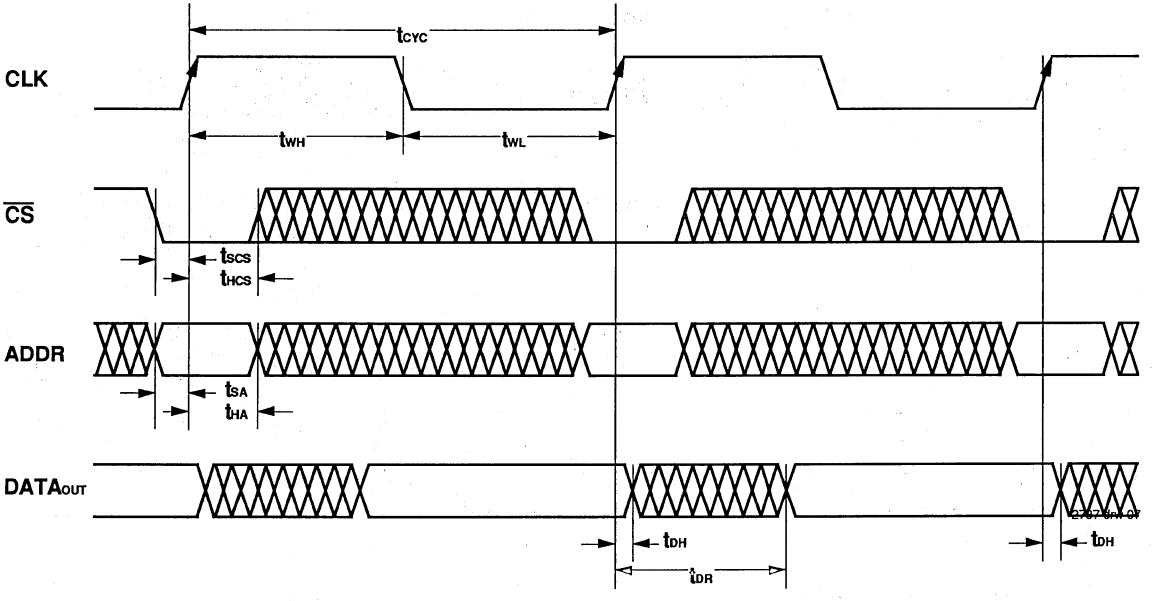
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10596RR10 100596RR10 101596RR10		10596RR12 100596RR12 101596RR12		10596RR15 100596RR15 101596RR15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE									
tCYC	Cycle Time	—	10	—	12	—	15	—	ns
tWL	Clock Low Pulse Width	—	4	—	5	—	6	—	ns
tWH	Clock High Pulse Width	—	4	—	5	—	6	—	ns
tSCS	Setup Time for Chip Select	—	1	—	1	—	1	—	ns
tSA	Setup Time for Address	—	1	—	1	—	1	—	ns
tHCS	Hold Time for Chip Select	—	2	—	2	—	2	—	ns
tHA	Hold Time for Address	—	2	—	2	—	2	—	ns
tDH	Data Hold from Clock High	—	0	—	0	—	0	—	ns
tDR	Data Ready from Clock High	—	0	4	0	4	0	4	ns

NOTE:
1. Input and Output reference level is 50% point of waveform.

2787 tbl 12

READ CYCLE TIMING DIAGRAM



B

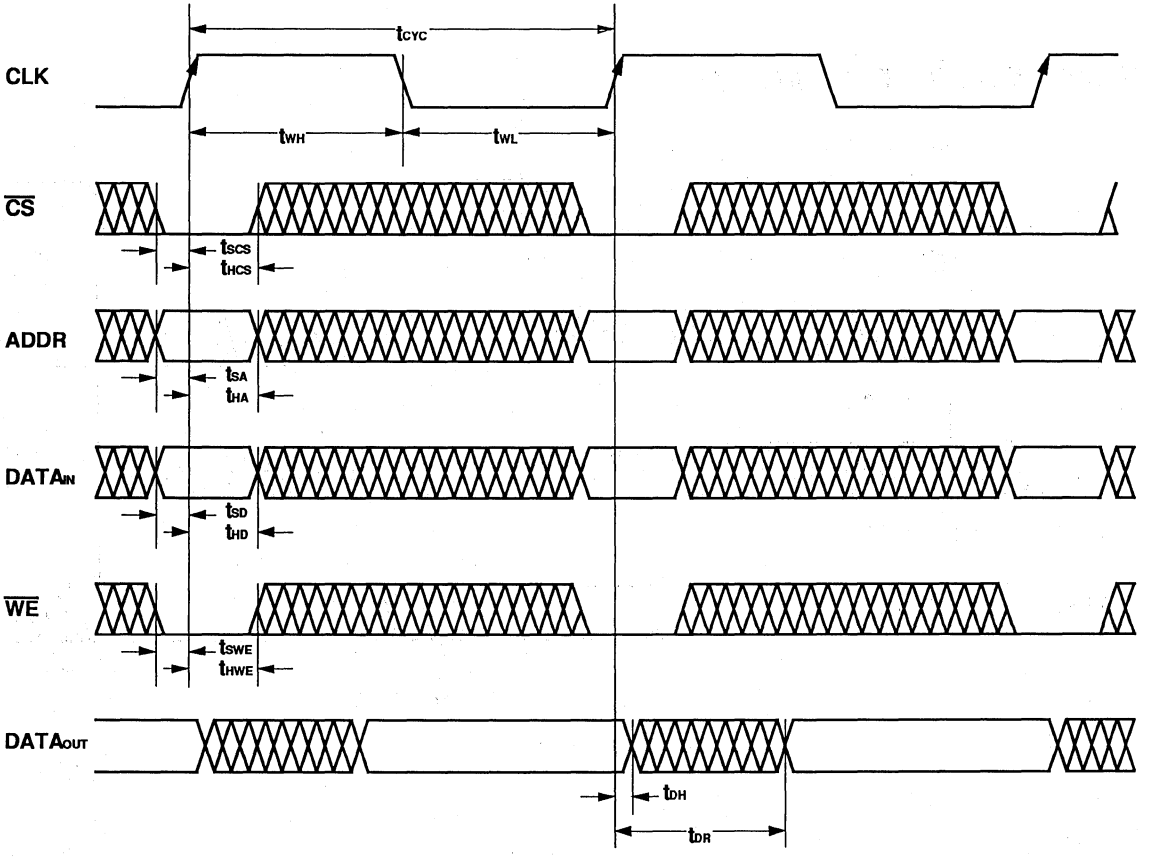
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10596RR10 100596RR10 101596RR10		10596RR12 100596RR12 101596RR12		10596RR15 100596RR15 101596RR15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE									
tSWE	Setup Time for Write Enable	—	1	—	1	—	1	—	ns
tSD	Setup Time for Data In	—	1	—	1	—	1	—	ns
tHWE	Hold Time for Write Enable	—	2	—	2	—	2	—	ns
tHD	Hold Time for Data In	—	2	—	2	—	2	—	ns

NOTES:
2787 tbl 12

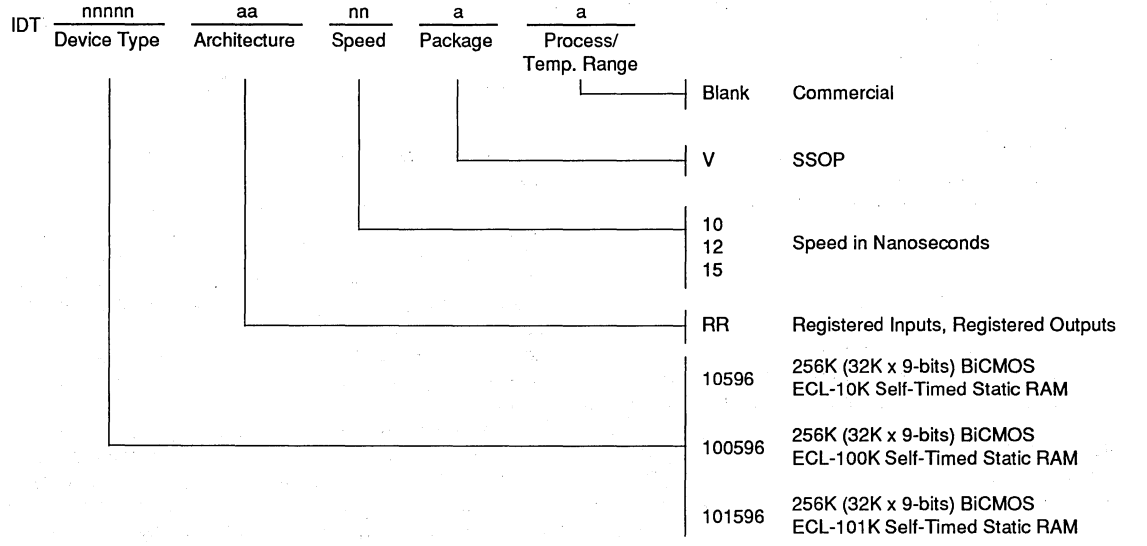
1. Input and Output reference level is 50% point of waveform.
2. All Setup, Hold, and access timing is the same as the Read Cycle with the addition of the above requirements. Write Data appears on the output pins after the next rising edge of CLK.

WRITE CYCLE TIMING DIAGRAM



2787 drw 08

ORDERING INFORMATION



2787 drw 09

B

Integrated Device Technology, Inc.

HIGH-SPEED 36K (4K x 9-BIT) SYNCHRONOUS DUAL-PORT RAM

ADVANCE INFORMATION
IDT7099S

FEATURES:

- High-speed clock-to-data output times
  - — Military: 20/25/30ns (max.)
  - — Commercial: 15/20/25ns (max.)
- Low-power operation
  - — IDT7099S
    Active: 900 mW (typ.)
    Standby: 50 mW (typ.)
- 4K X 9 bits
- Architecture based on dual-port RAM cells
  - — Allows full simultaneous access from both ports
  - — Independent bit/byte read and write inputs for control functions
- IDT's BiCEMOS™ process technology
- Synchronous operation
  - — 4ns setup to clock, 1ns hold on all control, data, and address inputs
  - — Data input, address, and control registers
  - — Fast 15ns clock to data out
  - — Self-timed write allows fast write cycle
  - — 20ns cycle times, 50MHz operation
- Clock enable feature
- Guaranteed data output hold times
- Available in 68-pin PGA and PLCC
- Military product compliant to MIL-STD-883, Class B

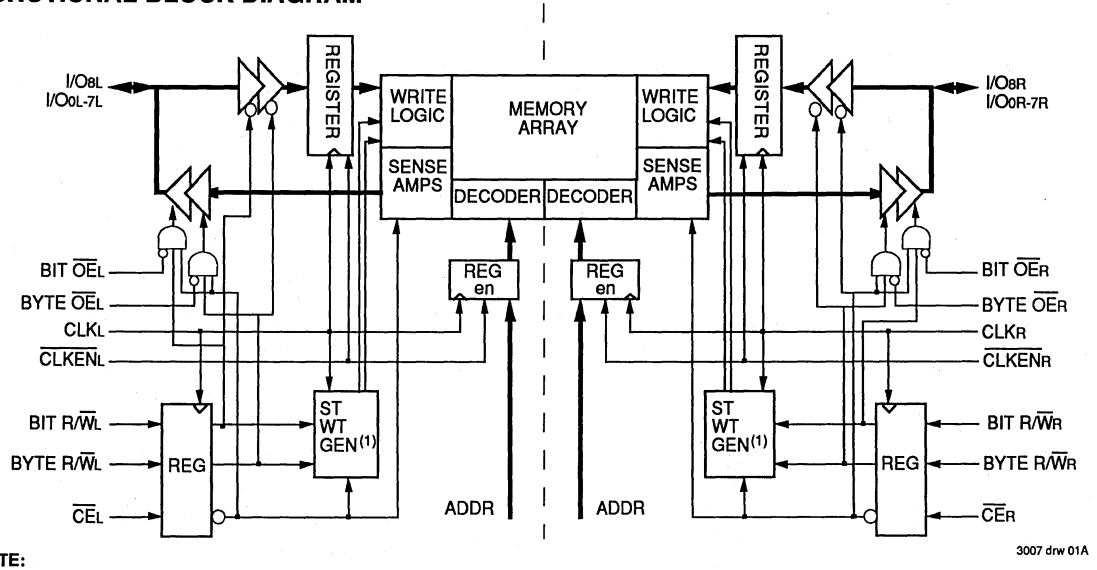
DESCRIPTION:

The IDT7099 is a high-speed 4K X 9 bit synchronous dual-port RAM. The memory array is based on dual-port memory cells to allow simultaneous access from both ports. Registers on control, data and address inputs provide low set-up and hold times. The timing latitude provided by this approach allow systems to be designed with very short realized cycle times. With an input data register, this device has been optimized for applications having unidirectional data flow or bi-directional data flow in bursts. Changing data direction from reading to writing normally requires one dead cycle.

Fabricated using IDT's BiCEMOS™ high-performance technology, these dual-ports typically operate on only 900mW of power at maximum high-speed clock-to-data output times as fast as 15ns. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT7099 is packaged in a 68-pin PGA or 68-pin PLCC. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Method 5004.

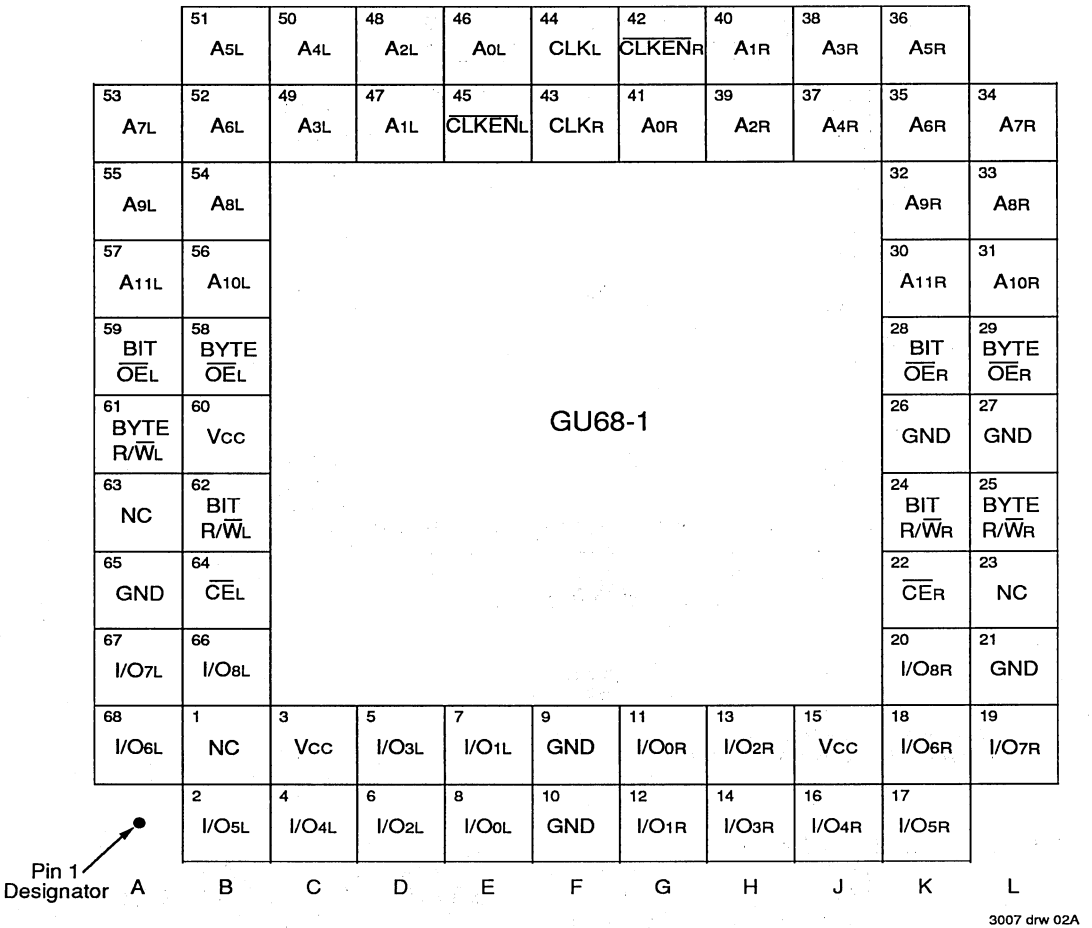
FUNCTIONAL BLOCK DIAGRAM



NOTE:
1. Self-timed write generator.

BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



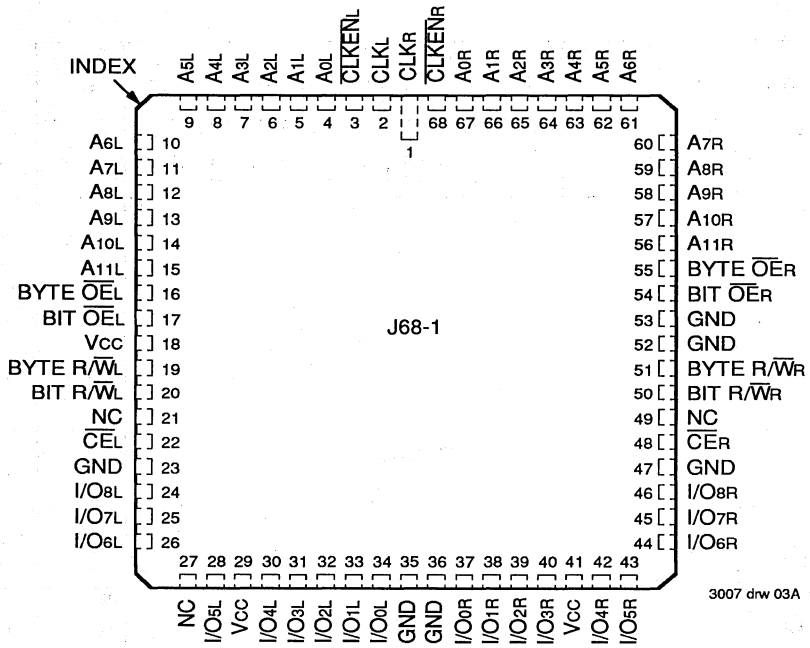
3007 drw 02A

68-Pin PGA
Top View

NOTES:
1. All VCC pins must be connected to power supply.
2. All ground pins must be connected to ground supply.

B

PIN CONFIGURATIONS (CONTINUED)



68-Pin PLCC
Top View

NOTES:

1. All VCC pins must be connected to power supply.
2. All ground pins must be connected to ground supply.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage	-0.5 to Vcc	-0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

3007 tbl 01

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Inputs and Vcc terminals only.
3. I/O terminals only.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

3007 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

3007 tbl 03

NOTE:

1. V_{IL} = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	IDT7099S Min.	IDT7099S Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4	—	V

3007 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Version	IDT7099S15(1) Typ.	IDT7099S15(1) Max.	IDT7099S20 Typ.	IDT7099S20 Max.	IDT7099S25 Typ.	IDT7099S25 Max.	IDT7099S30(2) Typ.	IDT7099S30(2) Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \le V_{IL}$ Outputs Open f = f_{MAX}(3)	Mil.	—	—	—	260	—	250	—	240	mA
			Com'l.	—	240	—	220	—	210	—	—	
I_{SB1}	Standby Current (Both Ports—TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \ge V_{IH}$ f = f_{MAX}(3)	Mil.	—	—	—	80	—	80	—	80	mA
			Com'l.	—	60	—	60	—	60	—	—	
I_{SB2}	Standby Current (One Port—TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \ge V_{IH}$ Active Port Outputs Open, f = f_{MAX}(3)	Mil.	—	—	—	210	—	210	—	210	mA
			Com'l.	—	180	—	170	—	170	—	—	
I_{SB3}	Full Standby Current (Both Ports—CMOS Level Inputs)	Both Ports $\overline{CE}_R$ and $\overline{CE}_L \ge V_{CC}$ – 0.2V $V_{IN} \ge V_{CC}$ – 0.2V or $V_{IN} \le$ 0.2V, f = 0(4)	Mil.	—	—	—	20	—	20	—	20	mA
			Com'l.	—	10	—	10	—	10	—	—	
I_{SB4}	Full Standby Current (One Port—CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ – 0.2V, $V_{IN} \ge V_{CC}$ – 0.2V or $V_{IN} \le$ 0.2V, Active Port Outputs Open, f = f_{MAX}(3)	Mil.	—	—	—	160	—	160	—	160	mA
			Com'l.	—	140	—	130	—	130	—	—	

3007 tbl 05

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. At f = fMAX, address and data inputs (except Output Enable) are cycling at the maximum frequency of clock cycle of 1/tCLK, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
4. f = 0 means no address, clock, or control lines change. Applies only to inputs at CMOS level standby.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

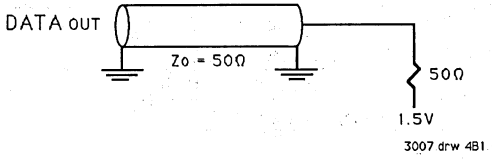


Figure 1. Output load.

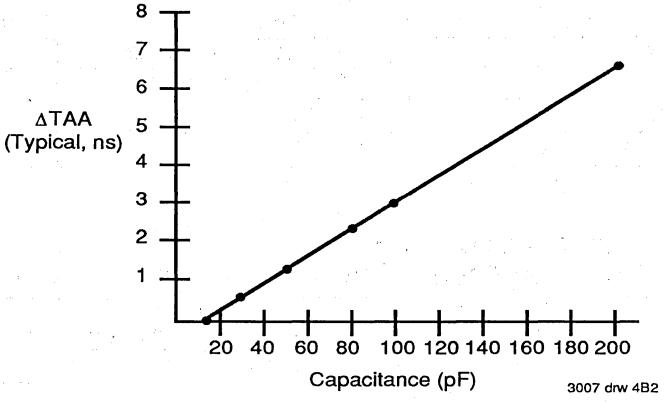


Figure 2. Lumped Capacitive Load, Typical Derating.

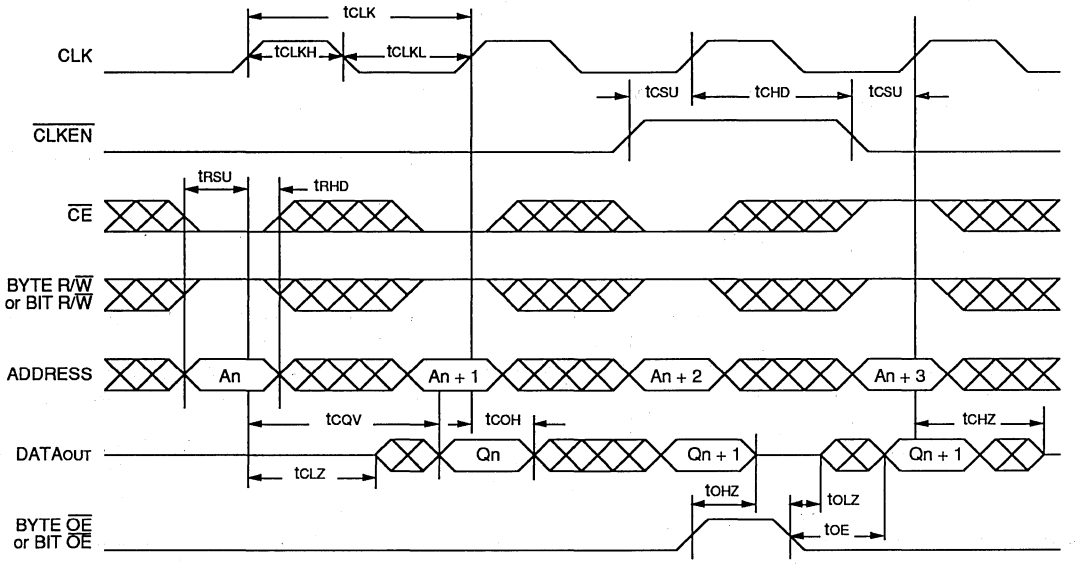
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGE — (READ AND WRITE CYCLE TIMING)

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

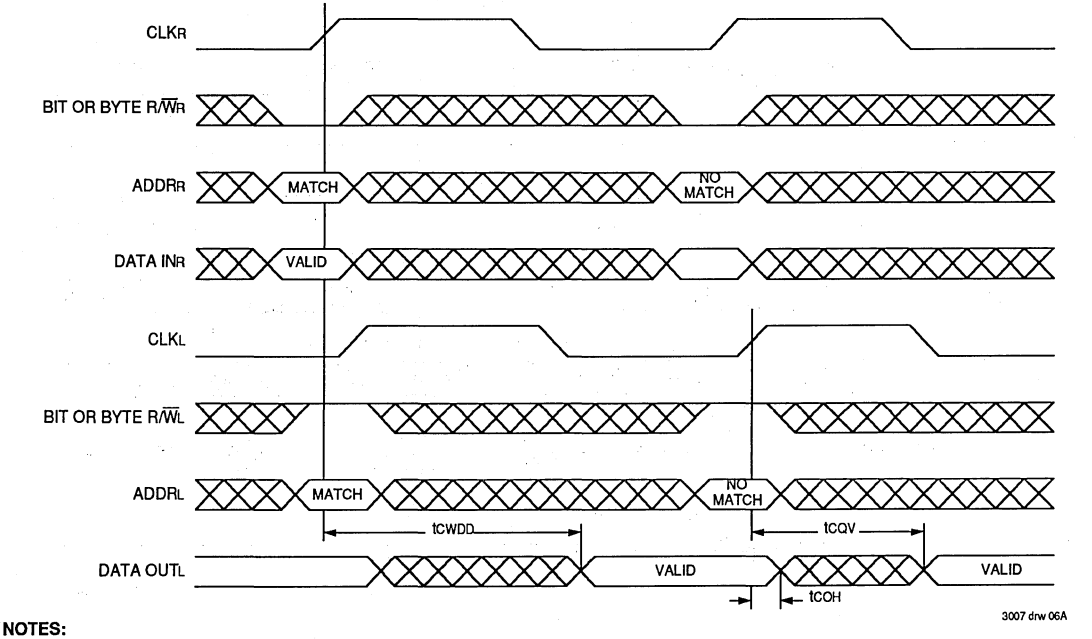
		Commercial						Military						
		7099S15		7099S20		7099S25		7099S20		7099S25		7099S30		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{CLK}	Clock Cycle Time	20	—	20	—	25	—	20	—	25	—	30	—	ns
t_{CLKH}	Clock High Time	6	—	8	—	10	—	8	—	10	—	12	—	ns
t_{CLKL}	Clock Low Time	6	—	8	—	10	—	8	—	10	—	12	—	ns
t_{CQV}	Clock High to Output Valid	—	15	—	20	—	25	—	20	—	25	—	30	ns
t_{RSU}	Registered Signal Set-up Time	4	—	5	—	6	—	5	—	6	—	7	—	ns
t_{RHD}	Registered Signal Hold Time	1	—	1	—	1	—	2	—	2	—	2	—	ns
t_{COH}	Data Output Hold After Clock High	3	—	3	—	3	—	3	—	3	—	3	—	ns
t_{CLZ}	Clock High to Output Low Z	2	—	2	—	2	—	2	—	2	—	2	—	ns
t_{CHZ}	Clock High to Output High Z	2	7	2	9	2	12	2	9	2	12	2	15	ns
t_{OE}	Output Enable to Output Valid	—	8	—	10	—	12	—	10	—	12	—	15	ns
t_{OLZ}	Output Enable to Output Low Z	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{OHZ}	Output Disable to Output High Z	—	7	—	9	—	11	—	9	—	11	—	14	ns
t_{CSU}	Clock Enable, Disable Set-up Time	4	—	5	—	6	—	5	—	6	—	7	—	ns
t_{CHD}	Clock Enable, Disable Hold Time	2	—	2	—	2	—	3	—	3	—	3	—	ns
Port-to-Port Delay														
t_{CWDD}	Write Port Clock High to Read Data Delay	—	30	—	35	—	45	—	35	—	45	—	55	ns

3007 tbl 06

TIMING WAVEFORM OF READ CYCLE, EITHER SIDE[2]

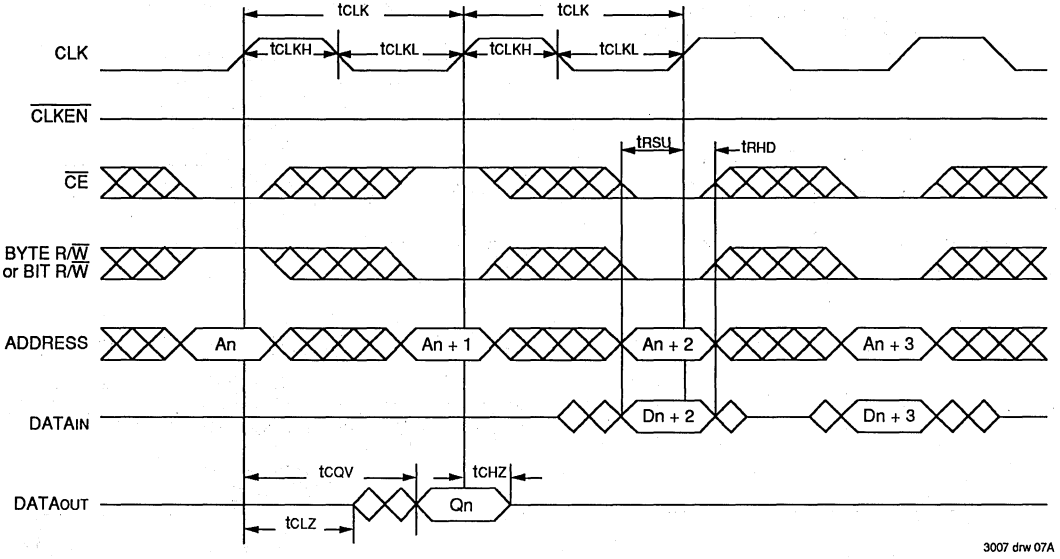


TIMING WAVEFORM OF READ CYCLE WITH PORT-TO-PORT DELAY[1, 2]



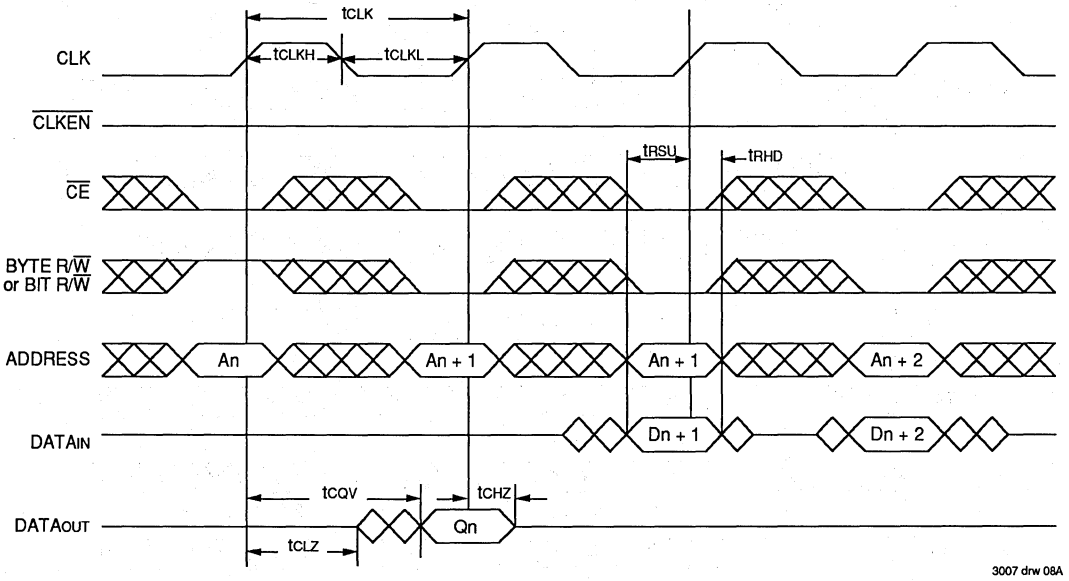
NOTES:
1. $\overline{CE}_L = \overline{CE}_R = L$, $\overline{CLKEN}_L = \overline{CLKEN}_R = L$
2. $\overline{OE} = L$ for the reading port.

TIMING WAVEFORM OF READ-TO-WRITE CYCLE NO. 1, $\overline{CE}$ HIGH (1)



NOTE:
1. $\overline{OE}$ low throughout.

TIMING WAVEFORM OF READ-TO-WRITE CYCLE NO. 1, $\overline{CE}$ LOW (1,2)



NOTES:
1. During dead cycle, if $\overline{CE}$ is low, data will be written into array.
2. $\overline{OE}$ low throughout.

FUNCTIONAL DESCRIPTION

The IDT7099 provides a true synchronous dual-port static RAM interface. Registered inputs provide very short set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal. An asynchronous output enable is provided to ease asynchronous bus interfacing.

The internal write pulse width is independent of the high and low periods of the clock. This allows the shortest possible realized cycle times. Clock enable inputs are provided to stall the operation of the address and data input registers without introducing clock skew for very fast interleaved memory applications.

The data inputs are gated to control on-chip noise in bussed applications. The user must guarantee that the BYTE R/$\overline{W}$ and BIT R/$\overline{W}$ pins are low for at least one clock cycle before any write is attempted. A high on the $\overline{CE}$ input for one clock cycle will power down the internal circuitry to reduce static power consumption.

The device has independent bit write, byte write, bit enable, and byte enable pins to allow for independent control.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

3007 tbl 07

TRUTH TABLES

TRUTH TABLE I: READ/WRITE CONTROL[1]

Inputs						Outputs		
Synchronous				Asynchronous				
Clk	$\overline{CE}$	Byte R/$\overline{W}$	Bit R/$\overline{W}$	Byte $\overline{OE}$	Bit $\overline{OE}$	I/O0-7	I/O8	Mode
↑	h	h	h	X	X	Hi-Z	Hi-Z	Deselected, Power Down, Data I/O Disabled
↑	h	l	h	X	X	DATAIN	Hi-Z	Deselected, Power Down, Byte Data Input Enabled
↑	h	h	l	X	X	Hi-Z	DATAIN	Deselected, Power Down, Bit Data Input Enabled
↑	h	l	l	X	X	DATAIN	DATAIN	Deselected, Power Down, Data Input Enabled
↑	l	l	h	X	L	DATAIN	DATAOUT	Write Byte, Read Bit
↑	l	l	h	X	H	DATAIN	Hi-Z	Write Byte Only
↑	l	h	l	L	X	DATAOUT	DATAIN	Read Byte, Write Bit
↑	l	h	l	H	X	Hi-Z	DATAIN	Write Bit Only
↑	l	l	l	X	X	DATAIN	DATAIN	Write Byte, Write Bit
↑	l	h	h	L	L	DATAOUT	DATAOUT	Read Byte, Read Bit
↑	l	h	h	H	L	Hi-Z	DATAOUT	Read Bit Only
↑	l	h	h	L	H	DATAOUT	Hi-Z	Read Byte Only
↑	l	h	h	H	H	Hi-Z	Hi-Z	Data I/O Disabled

3007 tbl 08

TRUTH TABLE II: CLOCK ENABLE FUNCTION TABLE[1]

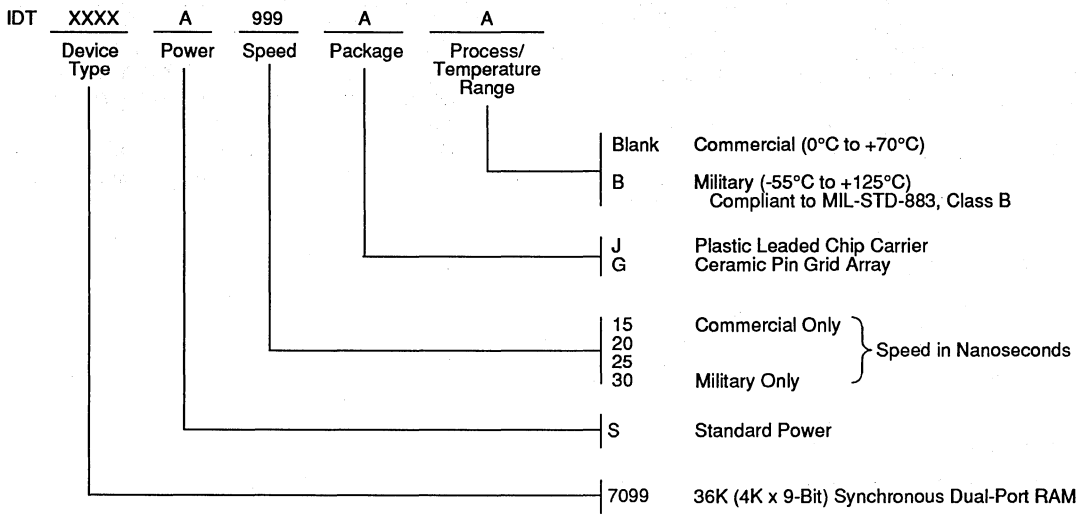
	Inputs		Register Inputs		Register Outputs	
Operating Mode	Clk	$\overline{CLKEN}$	ADDR	DATAIN	ADDR	DATAIN
Load "1"	↑	l	h	h	H	H
Load "0"	↑	l	l	l	L	L
Hold (do nothing)	↑	h	X	X	N/C	N/C
	X	H	X	X	N/C	N/C

3007 tbl 09

NOTE:
1. H = High voltage level steady state, h = High voltage level one set-up time prior to the low-to-high clock transition, L = Low voltage level steady state
l = Low voltage level one set-up time prior to the low-to-high clock transition, X = Don't care, N/C = No change

B

ORDERING INFORMATION



3007 drw 09

Integrated Device Technology, Inc.

IDT SUBSYSTEMS CUSTOM MODULE CAPABILITIES

INTRODUCTION

IDT Subsystems is available for design and manufacturing of a wide range of custom products. From dense memory modules to sophisticated multi-processor subsystems, we are the leading supplier of custom modules to commercial and military customers. This experience provides the basis of our professional approach to meet your needs. Custom module solutions can provide significant benefits to you:

- **Application Specific**

Encompassing all of your design criteria (electrical, mechanical, environmental), a custom solution is specially tailored to perform in your application.

- **Faster Time to Market**

Acting as an extension of your design team, we can provide the additional resources you need to bring your product out in time to meet *your* window of opportunity.

- **Manufacturing Ease/Guaranteed Performance**

100% of IDT Subsystem products are tested over guardbanded temperature and supply voltage to ensure datasheet conformance. This guaranteed performance reduces time-consuming debugging and provides you with confidence that your system will perform well at your customer's installation.

- **Density**

More capability into smaller space is what it takes to stay competitive. IDT Subsystems can help you using the packaging technology appropriate for your needs. Double-sided surface mounted components on FR-4 substrates offer quick-turn solutions. TAB mounted die and other approaches on a wide variety of substrates can offer substantial density advantages, especially for high pincount devices such as processors and ASICs. We can help you evaluate and compare alternatives to make the best selection for your application.

CUSTOM MODULE DEVELOPMENT FLOW

Figure 1 illustrates our custom module development flow, from initial concept through manufacturing and delivery. The initial concept is the starting point for discussions with the customer and Subsystems Engineering. Specifications, mechanical requirements, and other needs are reviewed and discussed to select the best components and assembly technology for the application.

All specifications are reviewed with you prior to substrate fabrication to ensure adherence to your requirements.

PACKAGING FLEXIBILITY

Packaging options provide you with the flexibility to fit your function within the available space. Military and hostile environments typically require the use of ceramic substrates while FR-4 is most often used in commercial and industrial temperature applications. Newer die packaging technologies such as TAB, flip-chip and others offer density and performance advantages not attainable by conventional through-hole or surface mount assemblies.

IDT Subsystems can provide you with the technology to fit your needs through prototype/beta testing, pilot production, and volume manufacturing. Contact the factory for more details.

CUSTOM PRODUCT DEVELOPMENT OVERVIEW

Customer requirements gathered and understood to prepare proposal which fits electrical, mechanical, and business needs.

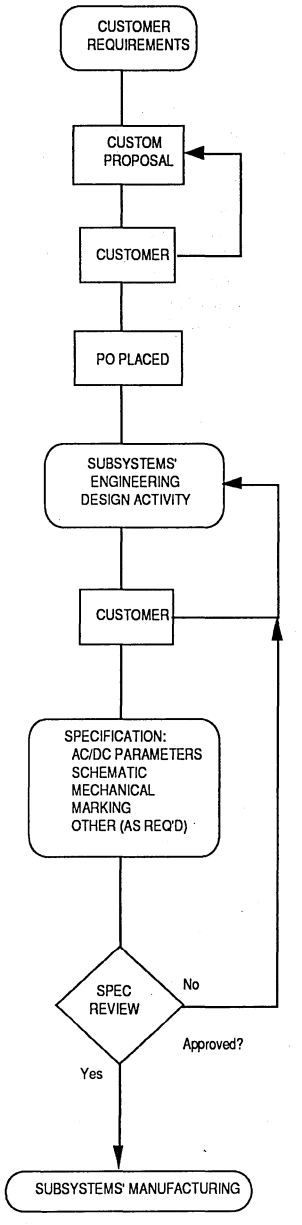
Custom development proposal written and presented to customer for evaluation and feedback. Changes are made as required to ensure customer will receive desired end product.

Subsystems' Engineering begins design. This process often involves communication with customer engineering group.

Subsystems' Engineering finshes design, and obtains approval within Subsystems' Marketing, Production, Assembly, and Test groups.

Complete custom specification delivered to customer for review and approval prior to ordering motherboard fabrication.

Custom module approval received; motherboard and other parts ordered for assembly kitting.



B

Integrated Device Technology, Inc.

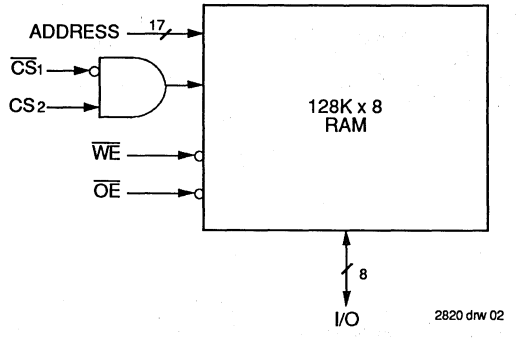
128K x 8 CMOS STATIC RAM

PRELIMINARY
IDT71M024
IDT71M025

FEATURES:

- High density 1 megabit (128K x 8) static RAM
- Dual Chip Select Version (IDT71M024)
  Single Chip Select Version (IDT71M025)
- Fast access time:
  - commercial: 55ns (max.)
  - military: 60ns (max.)
- Low power consumption
  - active: 100mA (max.)
  - CMOS standby: 2mA (max.)
- Very low power version
  - data retention: 50µA (max.) Vcc = 3V
  - CMOS standby: 100µA (max.)
- 32-pin ceramic sidebrazed DIP or ceramic leadless chip carrier (LCC)
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible

FUNCTIONAL BLOCK DIAGRAM(1)



NOTE:
1. For the IDT71M024 version Pin 30=CS_2. For the IDT71M025 version Pin 30=N.C.

PIN NAMES

I/O_{0-7}	Data Inputs/Outputs
A_{0-18}	Addresses
$\overline{CS_1}$, CS_2	Chip Selects
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
N.C.	No Connect
Vcc	Power
GND	Ground

2820 tbl 01

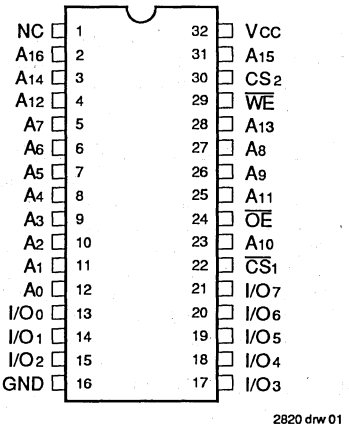
DESCRIPTION:

The IDT71M024/71M025 is a 1 megabit (128K x 8) static RAM packaged in a sidebrazed ceramic dual in-line package (DIP) and a ceramic leadless chip carrier (LCC). The IDT71M024/71M025 is available with access times as fast as 55ns. For battery backup applications, a very low power version is available, offering a commercial temperature data retention current of 50µA with Vcc = 3V.

The IDT71M024/71M025 is packaged in a 400 mil and a 600 mil 32-pin ceramic DIP as well as a 400 mil by 820 mil LCC. The 600 mil DIP conforms to the JEDEC standard, while the 400 mil DIP offers the same solution in 30% less space. For surface mount applications, the proposed JEDEC standard 400 mil by 820 mil LCC is ideal.

All inputs and outputs of the IDT71M024/71M025 are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use. All IDT military semiconductor components are manufactured in compliance to the latest revision of MIL-STD-883 Class B, making them ideally suited for applications demanding the highest level of performance and reliability.

PIN CONFIGURATION(1, 2)



DIP, LCC
TOP VIEW

NOTES:
1. For package dimensions, please refer to the drawings in the packaging section.
2. For the IDT71M024 version Pin 30=CS_2. For the IDT71M025 version Pin 30=N.C.

TRUTH TABLE

Mode	$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	X	High-Z	Standby
Standby	X	L	X	X	High-Z	Standby
Read	L	H	L	H	DOUT	Active
Read	L	H	L	H	High-Z	Active
Write	L	H	X	L	DIN	Active

tbl 09

CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	6	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE: 2820 tbl 10
1. This parameter is guaranteed by design, but not tested.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2820 tbl 02
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2820 tbl 03
1. VIL = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Commercial	0°C to +70°C	0V	5V ± 10%
Military	-55°C to +125°C	0V	5V ±10%

2820 tbl 04

B

DC ELECTRICAL CHARACTERISTICS

(VCC = 5V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameter	Test Conditions	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
|ILI|	Input Leakage	VCC = Max., VIN = GND to VCC	—	2.5	—	5	µA
|ILO|	Output Leakage	VCC = Max., $\overline{CS_1}$ = VIH and CS_2= VIL, VOUT = GND to VCC	—	2.5	—	5	µA
VOL	Output Low Voltage	VCC = Min., IOL = 2mA	—	0.4	—	0.4	V
VOH	Output High Voltage	VCC = Min., IOH = -1mA,	2.4	—	2.4	—	V
ICC	Dynamic Operating Current	VCC = Max., $\overline{CS}_1 \leq$ VIL and $CS_2 \geq$ VIH, f = fMAX, Outputs Open	—	100	—	100	mA
ISB	Standby Supply Current (TTL Levels)	$\overline{CS_1} \geq$ VIH and $CS_2 \leq$ VIL, VCC = Max., f = fMAX, Outputs Open	—	2.5	—	2.5	mA
ISB1	Full Standby Supply Current (CMOS Levels)	$\overline{CS_1} \geq$ VCC - 0.2V and $CS_2 \leq$ 0.2V VIN ≥ VCC - 0.2V or ≤ 0.2V	—	2	—	2	mA
		Very Low Power Version[1]	—	100	—	350	µA

NOTE: 2820 tbl 05
1. For data retention version, please specify L power when ordering.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2820 tbl 07

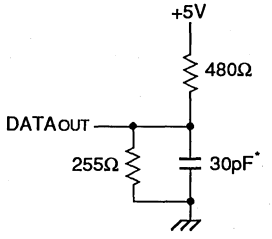


Figure 1. Output Load

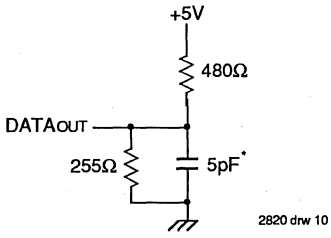


Figure 2. Output Load
(for tOLZ, tCHZ, tOHZ, tWHZ, tOW and tCLZ)

* Including scope and jig

DATA RETENTION CHARACTERISTICS(1)

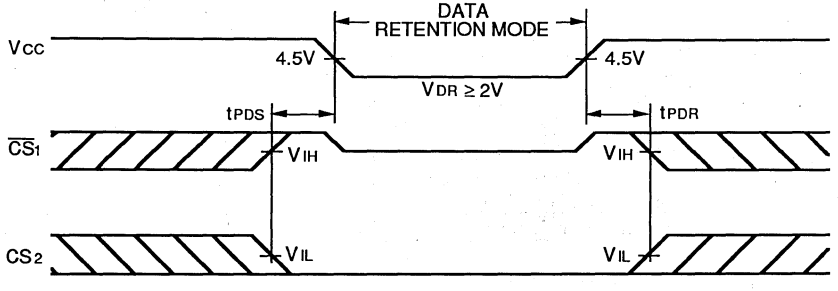
(TA = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameter	Test Condition	Min.	Comm. Max.	Military Max.	Unit
V_{DR}	V_{CC} for Data Retention	—	2.0	—	—	V
$V_{\overline{CS}1}$	$\overline{CS}_1$ Input Voltage	$V_{DR} \geq 2.2V$	2.2	—	—	V
V_{CS2}	CS_2 Input Voltage	$V_{DR} \geq 4.5V$	—	0.8	0.8	V
		$V_{DR} < 4.5V$	—	0.2	0.2	V
I_{CCDR1}	Data Retention Current	V_{CC} = 3.0V, $CS_2 \leq 0.2V$ or $\overline{CS}_1$, $CS_2 \geq V_{CC}$ - 0.2V, $V_{IN} \leq V_{CC}$ - 0.2V or $V_{IN} \geq 0.2V$	—	50	300	µA
I_{CCDR2}	Data Retention Current	V_{CC} = 2.0V, $CS_2 \leq 0.2V$ or $\overline{CS}_1$, $CS_2 \geq V_{CC}$ - 0.2V, $V_{IN} \leq V_{CC}$ - 0.2V or $V_{IN} \geq 0.2V$	—	50	200	µA
t_{PDS}(2)	Power Down Set Up Time		0	—	—	ns
t_{PDR}(2)	Power Down Recovery Time		t_{RC}(3)	—	—	ns

NOTES:
1. This option is only offered when ordering L power version.
2.. This parameter is guaranteed by design, but not tested.
3. t_{RC} = Read Cycle Time.

2820 tbl 09

DATA RETENTION WAVEFORM



2820 drw 03

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameter	71M024 or 71M025								Unit
		-55[2,3]		-60[2]		-65[2]		-70		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	60	—	65	—	70	—	70	—	ns
t_{AA}	Address Access Time	—	55	—	60	—	65	—	70	ns
t_{ACS1}	Chip Select ($\overline{CS_1}$) Access Time	—	55	—	60	—	65	—	70	ns
t_{ACS2}	Chip Select (CS_2) Access Time	—	60	—	65	—	70	—	70	ns
t_{OE}	Output Enable to Output Valid	—	25	—	30	—	35	—	35	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	20	—	25	—	25	—	25	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	3	—	3	—	5	—	5	—	ns
$t_{CLZ1,2}$[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	ns
$t_{CHZ1,2}$[1]	Chip Deselect to Output in High Z	—	20	—	25	—	25	—	25	ns
t_{OH}	Output Hold from Address Change	10	—	10	—	10	—	10	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	60	—	65	—	70	—	70	ns
Write Cycle										
t_{WC}	Write Cycle Time	60	—	65	—	70	—	70	—	ns
t_{WP}	Write Pulse Width	45	—	50	—	55	—	55	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{AW}	Address Valid to End of Write	55	—	60	—	65	—	65	—	ns
t_{CW1}	Chip Select ($\overline{CS_1}$) to End of Write	55	—	60	—	65	—	65	—	ns
t_{CW2}	Chip Select (CS_2) to End of Write	55	—	60	—	65	—	65	—	ns
t_{DW}	Data to Write Time Overlap	25		30	—	30	—	30	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	20	—	25	—	25	—	25	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specification only.
3 Commercial temperature only.

2820 tbl 06

B

AC ELECTRICAL CHARACTERISTICS

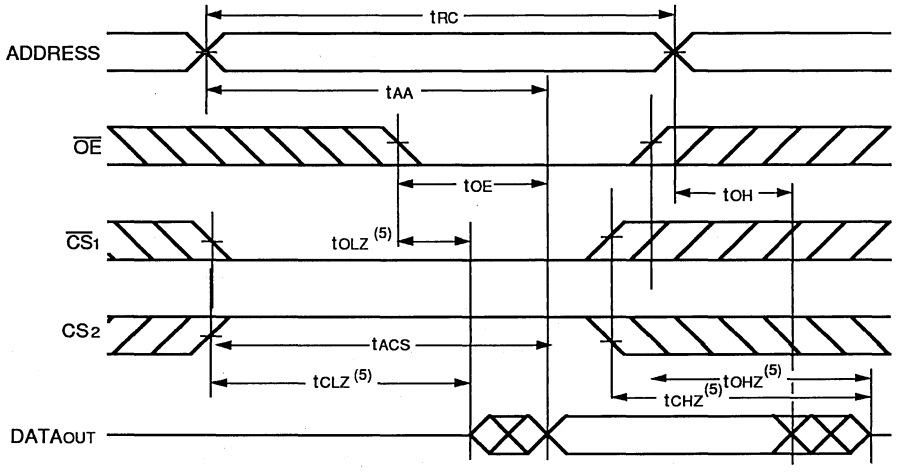
(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

		71M024 or 71M025						
		-85		-100		-120		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle								
t_{RC}	Read Cycle Time	85	—	100	—	120	—	ns
t_{AA}	Address Access Time	—	85	—	100	—	120	ns
t_{ACS1}	Chip Select ($\overline{CS_1}$) Access Time	—	85	—	100	—	120	ns
t_{ACS2}	Chip Select (CS_2) Access Time	—	85	—	100	—	120	ns
t_{OE}	Output Enable to Output Valid	—	40	—	45	—	45	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	30	—	35	—	35	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	5	—	ns
$t_{CLZ1,2}$[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	ns
$t_{CHZ1,2}$[1]	Chip Deselect to Output in High Z	—	30	—	35	—	35	ns
t_{OH}	Output Hold from Address Change	10	—	10	—	10	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	85	—	100	—	120	ns
Write Cycle								
t_{WC}	Write Cycle Time	85	—	100	—	120	—	ns
t_{WP}	Write Pulse Width	60	—	65	—	65	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{AW}	Address Valid to End of Write	70	—	75	—	75	—	ns
t_{CW1}	Chip Select ($\overline{CS_1}$) to End of Write	70	—	75	—	75	—	ns
t_{CW2}	Chip Select (CS_2) to End of Write	70	—	75	—	75	—	ns
t_{DW}	Data to Write Time Overlap	35	—	40	—	40	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	30	—	35	—	35	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

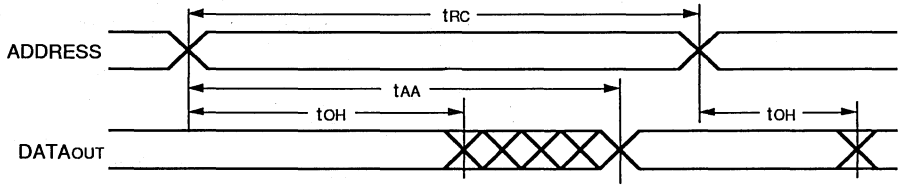
2820 tbl 06

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



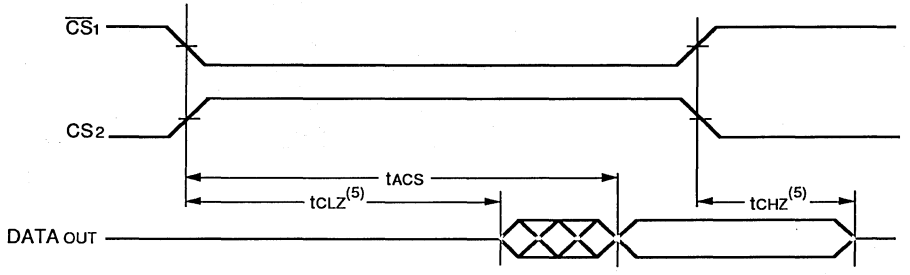
2820 drw 04

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2820 drw 05

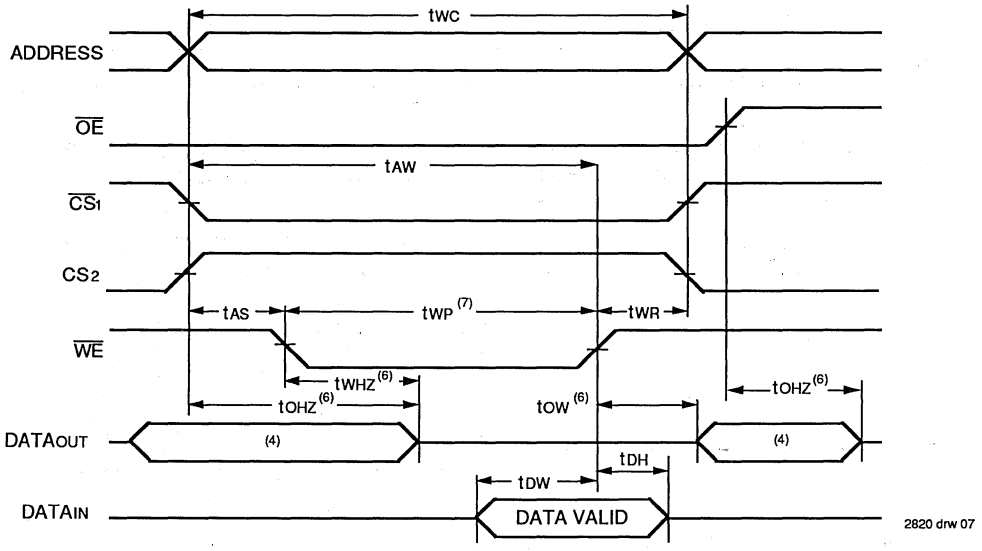
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



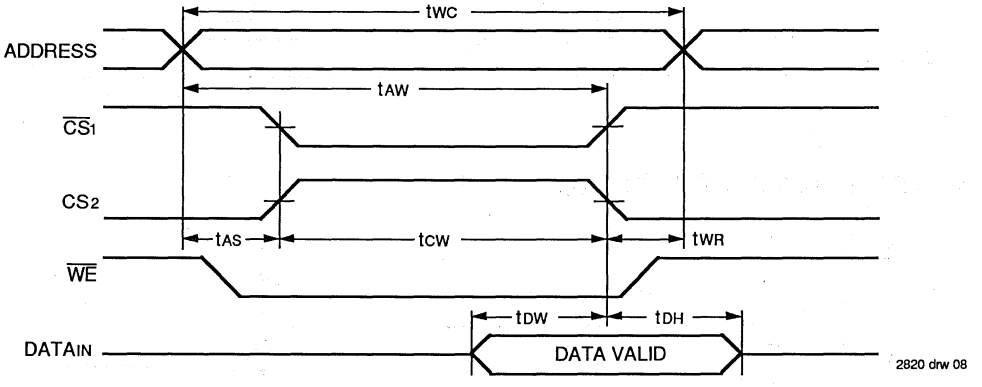
2820 drw 06

NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH} .
3. Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)

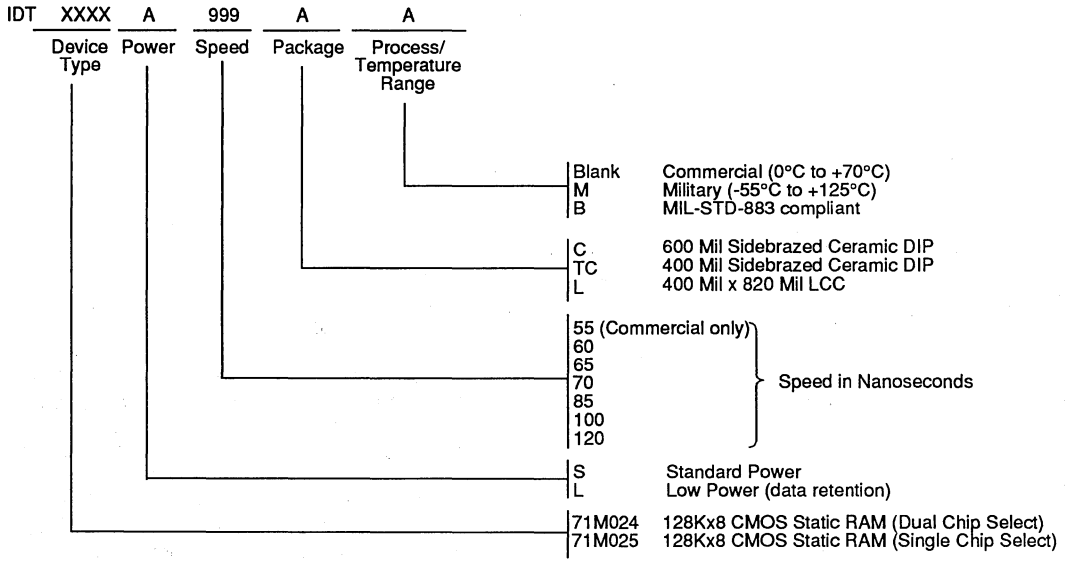


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS_1}$, CS_2 CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS_1}$ must be high, or CS_2 must be low during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS_1}$, high CS_2, and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS_1}$ or $\overline{WE}$ going high or CS_2 going low to the end of the write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS_1}$ low transition, CS_2 high transition occur simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

ORDERING INFORMATION



2820 drw 09

B

Integrated Device Technology, Inc.

1K x 36
2K x 36
CMOS DUAL-PORT STATIC RAM MODULE

PRELIMINARY
IDT7M1011
IDT7M1012

FEATURES

- High density 1K/2K x 36 CMOS Dual-Port Static RAM modules
- Fast access times
  - — Commercial: 25, 30, 40, 50, 60ns
  - — Military: 30, 40, 50, 60, 70ns
- Fully asynchronous read/write operation from either port
- Surface mounted LCC packages allow through-hole module to fit on a 121-pin PGA footprint
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible

DESCRIPTION

The IDT7M1011/1012 are 1K/2K x 36 high speed CMOS Dual-Port static RAM modules constructed on a co-fired ceramic substrate using 4 IDT7010 (1K x 9) Dual-Port RAMs or 4 IDT7012 (2K x 9) Dual-Port RAMs. The IDT7M1011/1012 modules are designed to be used as stand alone 36-bit dual-port RAM.

This module provides two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory.

The IDT7M1011/1012 modules are packaged in a 121-pin ceramic PGA (Pin Grid Array), resulting in package dimensions of only 1.36" x 1.36" x 0.28". Maximum access times as fast as 25ns/30ns are available over the commercial/military temperature range.

All IDT military modules are constructed with semiconductor components manufactured in compliance with the latest revision of MIL-STD-883, Class B making them ideally suited to applications demanding the highest level of performance and reliability.

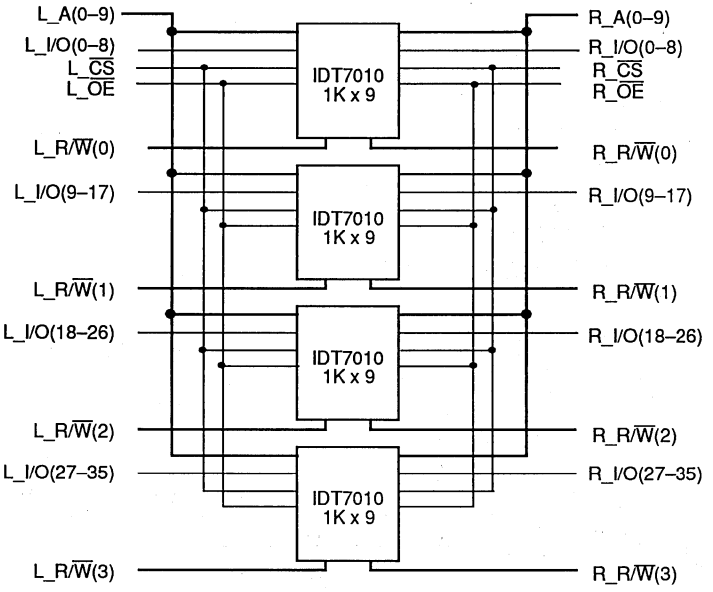
PIN CONFIGURATION[1, 2]

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	GND	L_R/$\overline{W}$(3)	R_R/$\overline{W}$(3)	R_I/O(20)	R_I/O(22)	R_I/O(25)	L_I/O(27)	L_I/O(28)	L_I/O(30)	L_I/O(32)	L_R/$\overline{W}$(4)	R_R/$\overline{W}$(4)	R_I/O(35)	A
B	L_I/O(18)	R_I/O(18)	R_I/O(19)	R_I/O(21)	R_I/O(23)	R_I/O(24)	R_I/O(26)	L_I/O(29)	L_I/O(31)	L_I/O(33)	VCC	L_I/O(34)	R_I/O(34)	B
C	L_I/O(19)	L_I/O(23)	VCC	L_A(0)	L_A(9)	L_A(10)	GND	R_A(10)	R_A(9)	R_A(0)	GND	L_I/O(35)	R_I/O(33)	C
D	L_I/O(20)	L_I/O(24)	L_A(1)	GND							R_A(1)	R_I/O(27)	R_I/O(32)	D
E	L_I/O(21)	L_I/O(25)	L_A(2)								R_A(2)	R_I/O(28)	R_I/O(31)	E
F	L_I/O(22)	L_I/O(26)	L_A(3)								R_A(3)	R_I/O(29)	R_I/O(30)	F
G	GND	L_$\overline{CS}$	GND				PGA Top View				GND	R_$\overline{CS}$	GND	G
H	L_R/$\overline{W}$(1)	L_$\overline{OE}$	R_R/$\overline{W}$(1)								L_R/$\overline{W}$(2)	R_$\overline{OE}$	R_R/$\overline{W}$(2)	H
J	L_I/O(0)	R_I/O(3)	L_A(4)								R_A(4)	L_I/O(15)	R_I/O(17)	J
K	L_I/O(1)	R_I/O(2)	L_A(5)								R_A(5)	L_I/O(16)	R_I/O(16)	K
L	L_I/O(2)	R_I/O(1)	GND	L_A(6)	L_A(7)	L_A(8)	GND	R_A(8)	R_A(7)	R_A(6)	VCC	GND	R_I/O(15)	L
M	L_I/O(3)	R_I/O(0)	VCC	R_I/O(4)	R_I/O(5)	R_I/O(7)	R_I/O(8)	L_I/O(11)	L_I/O(12)	L_I/O(13)	L_I/O(14)	L_I/O(17)	R_I/O(14)	M
N	L_I/O(4)	L_I/O(5)	L_I/O(6)	L_I/O(7)	L_I/O(8)	R_I/O(6)	L_I/O(9)	L_I/O(10)	R_I/O(9)	R_I/O(10)	R_I/O(11)	R_I/O(12)	R_I/O(13)	N
	1	2	3	4	5	6	7	8	9	10	11	12	13	

NOTES:
1. For module dimensions, please refer to the module drawings in the packaging section.
2. For the IDT7M1011 (1K x 36 version), Pins C6 and C8 (L_A(10) and R_A(10) respectively) must be connected to VCC for proper operation of the module.

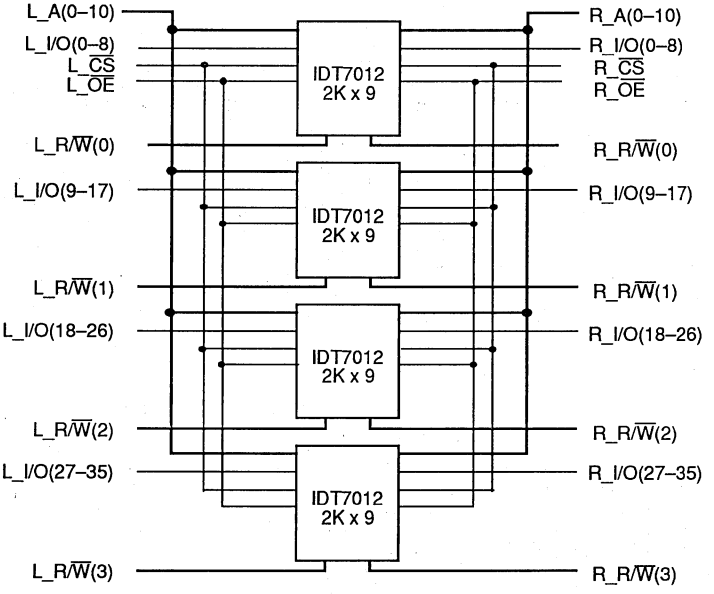
FUNCTIONAL BLOCK DIAGRAMS

7M1011



2821 drw 02

7M1012



2821 drw 03

B

PIN NAMES

Left Port	Right Port	Names
L_$\overline{CS}$	R_$\overline{CS}$	Chip Selects
L_R/$\overline{W}$(1-4)	R_R/$\overline{W}$(1-4)	Read/Write Enables
L_$\overline{OE}$	R_$\overline{OE}$	Output Enables
L_A (0–10)	R_A (0–10)	Address Inputs
L_I/O (0–35)	R_I/O (0–35)	Data Input/Outputs
Vcc		Power
GND		Ground

2821 tbl 01

NOTE:
1. On the IDT7M1011 (1K x 36 version), Pins C6 and C8 (L_A10 and R_A10 respectively) need to be connected to VCC for proper operation of the module.

CAPACITANCE TABLE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	IDT7M1011 Max.	IDT7M1012 Max.	Unit
C_IN(1)	Input Capacitance (Address, $\overline{CS}$, $\overline{OE}$)	V_IN = 0V	50	50	pF
C_IN(2)	Input Capacitance (Data, R/$\overline{W}$)	V_IN = 0V	15	15	pF
COUT	Output Capacitance (Data)	V_OUT = 0V	15	15	pF

2821 tbl 05

NOTE:
1. This parameter is guaranteed by design but not tested.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

2821 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	–0.5(1)	—	0.8	V

2821 tbl 03

NOTE:
1. VIL ≥ –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2821 tbl 04

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7M1011		IDT7M1012		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	40	—	40	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS} \geq V_{IH}$, V_{OUT} = GND to V_{CC}	—	40	—	40	µA
V_{OL}	Output Low Voltage	V_{CC} = Min. I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min. I_{OH} = -4mA	2.4	—	2.4	—	V

2821 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7M1011			IDT7M1012			Unit
			Min.	Max.(1)	Max.(2)	Min.	Max.(1)	Max.(2)	
I_{CC}	Dynamic Operating Current (Both Ports Active)	V_{CC} = Max., $\overline{CS} \leq V_{IL}$, Outputs Open, f = f_{MAX}	—	1040	1240	—	1040	1240	mA
I_{SB}	Standby Supply Current (Both Ports Inactive)	V_{CC} = Max., $\overline{CS}\_L$ and $\overline{CS}\_R \geq V_{IH}$ Outputs Open, f = f_{MAX}	—	260	320	—	260	320	mA
I_{SB1}	Standby Supply Current (One Port Inactive)	V_{CC} = Max., $\overline{CS}\_L$ o $\overline{CS} \geq V_{IH}$ Outputs Open, f = f_{MAX}	—	700	800	—	700	800	mA
I_{SB2}	Full Standby Supply Current (Both Ports Inactive)	$\overline{CS}\_L$ and $\overline{CS}\_R \geq V_{CC}$ –0.2V $V_{IN} > V_{CC}$ 0.2V or < 0.2V	—	60	120	—	60	120	mA

NOTES:
1. For commercial grade (0°C to +70°C) versions only.
2. For military grade (-55°C to +125°C) versions only.

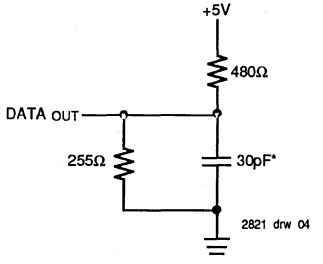
2821 tbl 07

B

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2821 tbl 08



*Including scope and jig.

Figure 1. Output Load

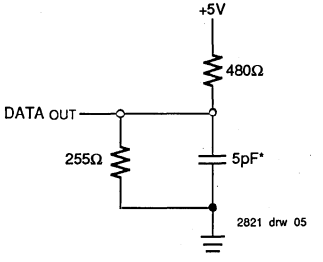


Figure 2. Output Load (For tCHZ, tCLZ, tOHZ, tOLZ, tWHZ, tOW)

AC ELECTRICAL CHARACTERISTICS

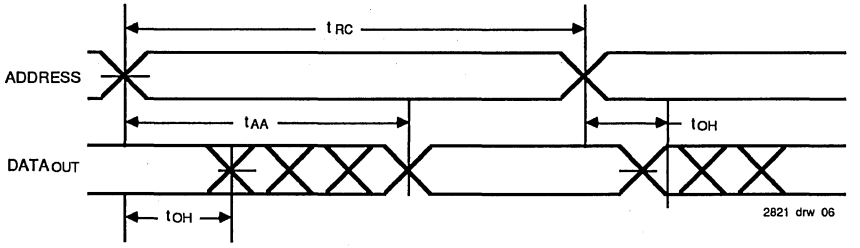
(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

		7M1011Sxx or 7M1012Sxx												
		-25[9]		-30		-40		-50		-60		-70		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle														
t_{RC}	Read Cycle Time	25	—	30	—	40	—	50	—	60	—	70	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	40	—	50	—	60	—	70	ns
t_{ACS} [2]	Chip Select Access Time	—	25	—	30	—	40	—	50	—	60	—	70	ns
t_{OE}	Output Enable Access Time	—	12	—	15	—	25	—	30	—	35	—	40	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	10	—	12	—	15	—	20	—	30	—	35	ns
t_{OLZ} [1]	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{OHZ} [1]	Output Disable to Output in High Z	—	10	—	12	—	15	—	20	—	30	—	35	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Down Time	—	50	—	50	—	50	—	50	—	50	—	50	ns
Write Cycle														
t_{WC}	Write Cycle Time	25	—	30	—	40	—	50	—	60	—	70	—	ns
t_{CW}[2]	Chip Select to End of Write	20	—	25	—	30	—	35	—	40	—	50	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	30	—	35	—	40	—	50	—	ns
t_{AS}	Address Set-Up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	30	—	35	—	40	—	50	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	12	—	15	—	20	—	20	—	20	—	30	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	10	—	12	—	15	—	20	—	30	—	35	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	10	—	12	—	15	—	20	—	30	—	35	ns
t_{OW}[1]	Output Active from End of Write	0	——	0	—	0	—	0	—	0	—	0	—	ns

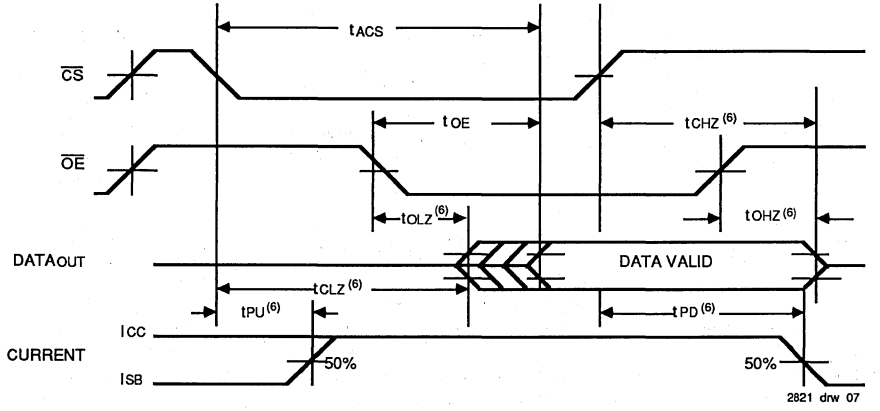
2821 tbl 09

NOTES:
1. This parameter is guaranteed by design but not tested.
2. To access RAM array, $\overline{CS} \leq V_{IL}$.
3. Master mode is not available on this module.
4. The module is always in the Slave Mode.
5. Port-to-Port delay through the RAM cells from the writing port to the reading port.
6. To ensure that the earlier of the two ports wins.
7. To ensure that the write cycle is inhibited during contention.
8. To ensure that a write cycle is completed after contention.
9. Preliminary specification only.

TIMING WAVEFORM OF READ CYCLE NO. 1 (EITHER SIDE) (1, 2, 4)



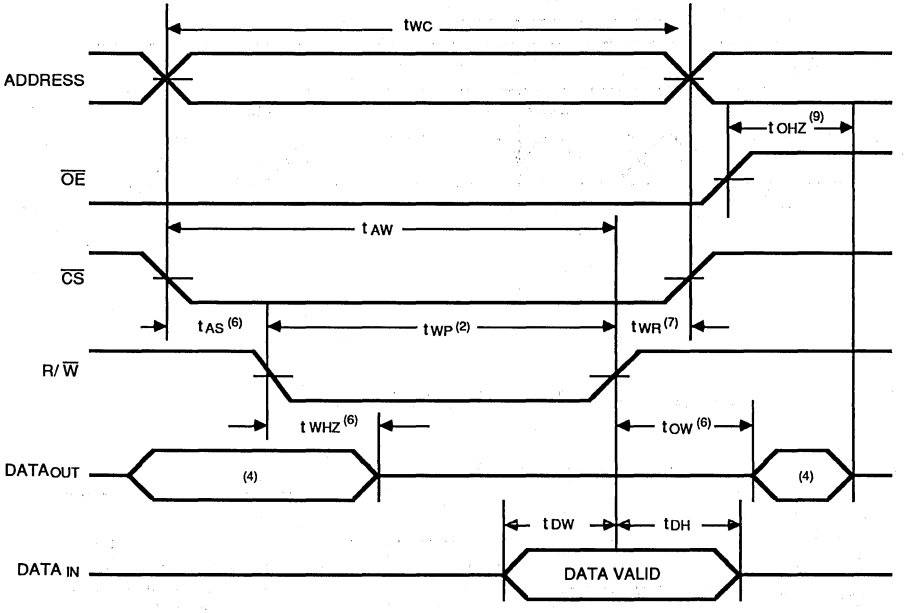
TIMING WAVEFORM OF READ CYCLE NO. 2 (EITHER SIDE) (1, 3, 5)



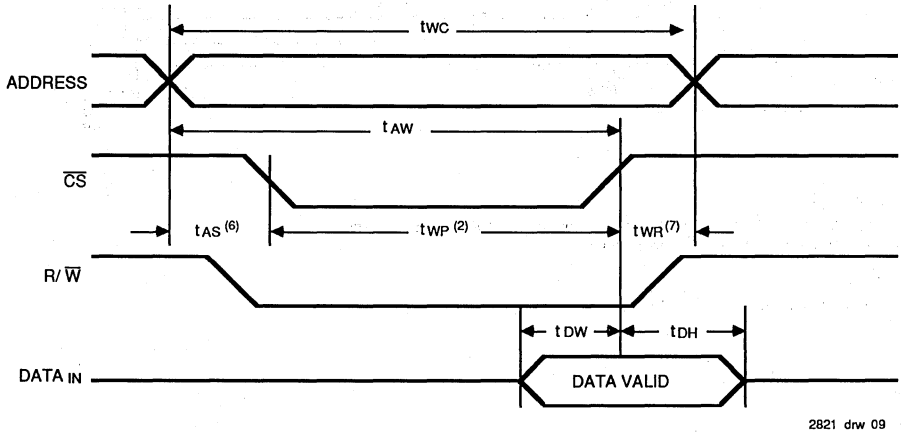
NOTES:
1. R/$\overline{W}$ is high for Read Cycles
2. Device is continuously enabled, $\overline{CS}$ = L. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low
4. $\overline{OE}$ = L
5. To access RAM, $\overline{CS}$ = L.
6. This parameter is guaranteed by design but not tested.

B

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING) (1, 3, 5, 8)

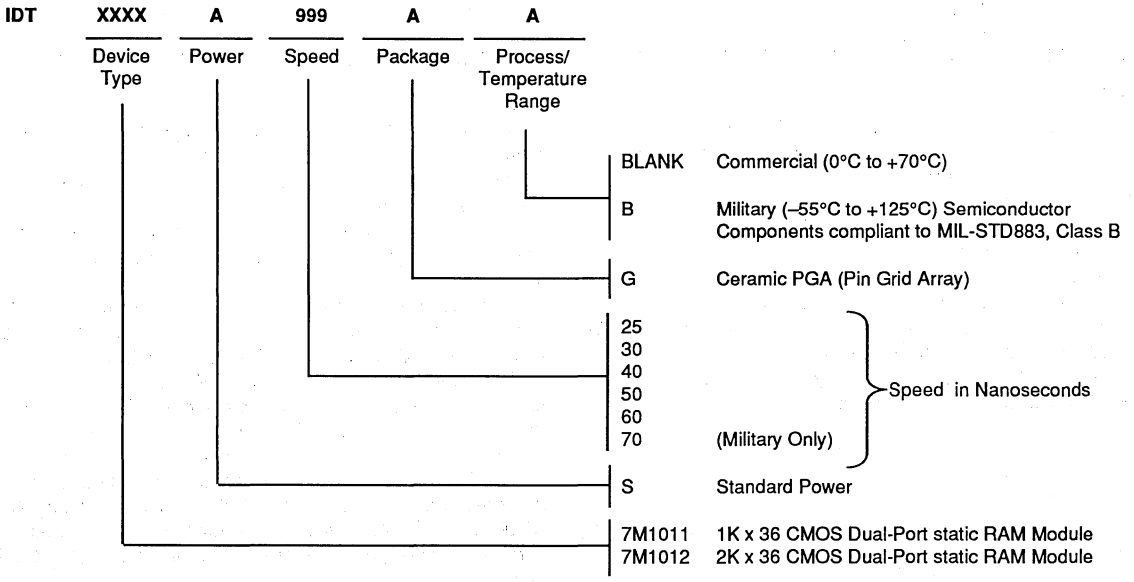


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING) (1, 3, 5, 8)



NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply. and the write pulse can be as short as the specified tWP.
9. This parameter is guaranteed by design but not tested.

ORDERING INFORMATION



B

Integrated Device Technology, Inc.

512K x 8 CMOS STATIC RAM MODULE

PRELIMINARY
IDT7M4048

FEATURES:

- High density 4 megabit CMOS static RAM module
- Equivalent to the JEDEC standard for future monolithic 512K x 8 static RAMs
- Fast access time: 17ns (max.)
- Low power consumption (L version)
  - — Active: 110mA (max.)
  - — CMOS Standby: 1.4mA (max.)
  - — Data Retention: 800µA (max.) Vcc = 2V
- Surface mounted LCCs (leadless chip carriers) on a 32-pin, 600 mil ceramic DIP substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible

DESCRIPTION:

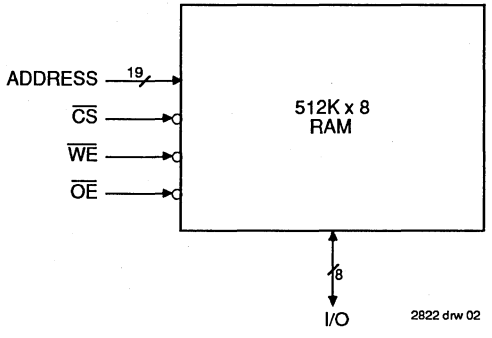
The IDT7M4048 is a 4 megabit (512K x 8) CMOS static RAM module constructed on a co-fired ceramic substrate using four 1 Megabit static RAMs and a decoder. The IDT7M4048 is available with access times as fast as 17ns. For low power applications, the IDT7M4048 version offers a data retention current of 800µA and a standby current of 1.4mA.

The IDT7M4048 is packaged in a 32-pin ceramic DIP. This results in a package 1.7 inches long and 0.6 inches wide, packing 4 megabits into the JEDEC DIP footprint.

All inputs and outputs of the IDT7M4048 are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

All IDT military module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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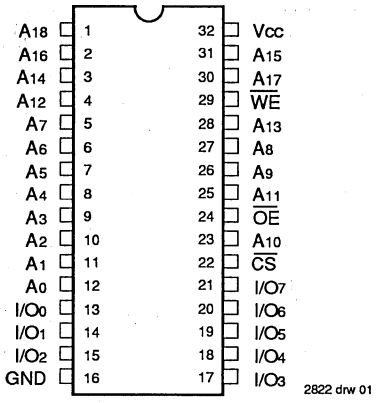
MILITARY TEMPERATURE RANGE **MAY 1991**

PIN CONFIGURATION[1]



2822 drw 01

DIP
TOP VIEW

NOTE:
1. For module dimensions, please refer to the module drawings in the packaging section.

PIN NAMES

I/O0-7	Data Inputs/Outputs
A0-18	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power
GND	Ground

2822 tbl 01

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	DOUT	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	DIN	Active

2822 tbl 09

CAPACITANCE[1] (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	50	pF
CIN(C)	Input Capacitance ($\overline{CS}$)	VIN = 0V	10	pF
COUT	Output Capacitance	VOUT = 0V	40	pF

NOTE: 2822 tbl 10
1. This parameter is guaranteed by design, but not tested.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	-55 to +125	°C
TBIAS	Temperature Under Bias	–65 to +135	°C
TSTG	Storage Temperature	–65 to +160	°C
IOUT	DC Output Current	50	mA

NOTE: 2822 tbl 02
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2822 tbl 03
1. VIL = -2.0V for pulse width less than 10ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%

2822 tbl 04

B

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	Test Conditions	7M4048SxxCB, 7M4048LxxCB				Unit
			17ns-55ns		60ns-120ns		
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	20	—	20	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	20	—	20	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 2mA(1), I_{OL} = 8mA(2)	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -1mA(1), I_{OH} = –4mA(2)	2.4	—	2.4	—	V
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS} \leq V_{IL}$; f = f_{MAX}, Outputs Open	—	240	—	110	mA
I_{SB}	Standby Supply Current (TTL Levels)	$\overline{CS} \geq V_{IH}$, V_{CC} = Max., f = f_{MAX}, Outputs Open	—	120	—	12	mA
I_{SB1}	Full Standby Supply Current (CMOS Levels)	$\overline{CS} \geq V_{CC}$ - 0.2V, $V_{IN} \geq V_{CC}$ - 0.2V or ≤ 0.2V	—	60	—	4	mA
		Very Low Power Version(3)	—	60	—	1.4	mA

NOTES:
1. For 60ns-120ns versions only.
2. For 17ns-55ns versions only.
3. L version only.

2822 tbl 05

DATA RETENTION CHARACTERISTICS(5)

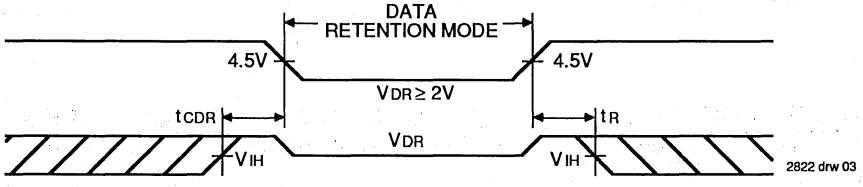
(T_A = -55°C to +125°C)

Symbol	Parameter	Test Condition	Min.	Max. V_{CC} @ 2.0V	Unit
V_{DR}	V_{CC} for Data Retention	—	2.0	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ - 0.2V	—	2(4)	mA
t_{CDR}(3)	Chip Deselect to Data Retention Time	$V_{IN} \leq V_{CC}$ - 0.2V or	0	—	ns
t_R(3)	Operation Recovery Time	$V_{IN} \geq$ 0.2V	t_{RC}(2)	—	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by design, but not tested.
4. For 60ns-120ns versions, ICCDR=800µA.
5. L version only.

2822 tbl 09

DATA RETENTION WAVEFORM



2822 drw 03

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2822 tbl 07

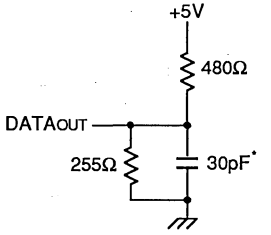


Figure 1. Output Load

* Including scope and jig

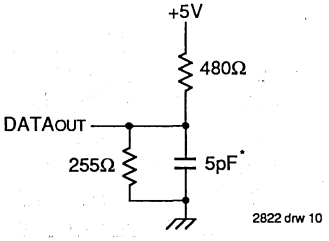


Figure 2. Output Load
(for t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, t_{OW} and t_{CLZ})

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

		7M4048SxxCB, 7M4048LxxCB										
		-17(3)		-20(3)		-25		-30		-35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle												
t_{RC}	Read Cycle Time	17	—	20	—	25	—	30	—	35	—	ns
t_{AA}	Address Access Time	—	17	—	20	—	25	—	30	—	35	ns
t_{ACS}	Chip Select Access Time	—	17	—	20	—	25	—	30	—	35	ns
t_{OE}	Output Enable to Output Valid	—	8	—	10	—	12	—	15	—	15	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	7	—	8	—	12	—	12	—	15	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	0	—	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	—	12	—	13	—	14	—	16	—	20	ns
t_{OH}	Output Hold from Address Change	1	—	3	—	3	—	3	—	3	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	17	—	20	—	25	—	30	—	35	ns
Write Cycle												
t_{WC}	Write Cycle Time	17	—	20	—	25	—	30	—	35	—	ns
t_{WP}	Write Pulse Width	14	—	15	—	17	—	20	—	25	—	ns
t_{AS}(2)	Address Set-up Time	3	—	3	—	3	—	0	—	0	—	ns
t_{AW}	Address Valid to End of Write	17(4)	—	18	—	20	—	25	—	30	—	ns
t_{CW}	Chip Select to End of Write	17	—	18	—	20	—	25	—	30	—	ns
t_{DW}	Data to Write Time Overlap	10	—	12	—	15	—	17	—	20	—	ns
t_{DH}(2)	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WR}(2)	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}(1)	Write Enable to Output in High Z	—	10	—	13	—	15	—	15	—	15	ns
t_{OW}(1)	Output Active from End of Write	2	—	2	—	2	—	5	—	5	—	ns

2822 tbl 06

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. t_{AS}=0ns for $\overline{CS}$ controlled write cycles. t_{DH}, t_{WR}= 3ns for $\overline{WE}$ controlled write cycles.
3. Preliminary specifications only.
4. t_{AW}=14ns for $\overline{CS}$ controlled write cycles.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	7M4048SxxCB, 7M4048LxxCB										Unit
		-45		-55		-60[3]		-65[3]		-70		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t_{RC}	Read Cycle Time	45	—	55	—	65	—	65	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	60	—	65	—	70	ns
t_{ACS}	Chip Select Access Time	—	45	—	55	—	60	—	65	—	70	ns
t_{OE}	Output Enable to Output Valid	—	25	—	30	—	30	—	35	—	45	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	20	—	20	—	25	—	25	—	30	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	3	—	5	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	20	—	20	—	25	—	25	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	10	—	10	—	—	10	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	45	—	55	—	65	—	65	—	70	ns
Write Cycle												
t_{WC}	Write Cycle Time	45	—	55	—	65	—	65	—	70	—	ns
t_{WP}	Write Pulse Width	35	—	45	—	50	—	55	—	55	—	ns
t_{AS}	Address Set-up Time	5	—	5	—	0	—	0	—	0	—	ns
t_{AW}	Address Valid to End of Write	40	—	50	—	60	—	65	—	65	—	ns
t_{CW}	Chip Select to End of Write	40	—	50	—	60	—	65	—	65	—	ns
t_{DW}	Data to Write Time Overlap	20	—	20	—	30	—	30	—	35	—	ns
t_{DH}	Data Hold Time	0[2]	—	0[2]	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0[2]	—	0[2]	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	15	—	20	—	25	—	25	—	30	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	0	—	0	—	0	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. t_{AS}=0ns for $\overline{CS}$ controlled write cycles. t_{DH}, t_{WR}= 5ns for $\overline{WE}$ controlled write cycles.
3. Preliminary specifications only.

2822 tbl 06

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

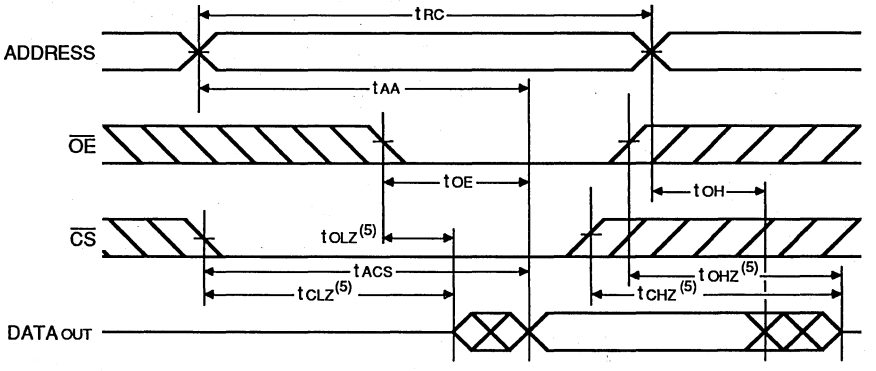
Symbol	Parameter	7M4048SxxCB, 7M4048LxxCB						Unit
		-85		-100		-120		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	85	—	100	—	120	—	ns
t_{AA}	Address Access Time	—	85	—	100	—	120	ns
t_{ACS}	Chip Select Access Time	—	85	—	100	—	120	ns
t_{OE}	Output Enable to Output Valid	—	48	—	50	—	60	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	33	—	35	—	40	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	0	—	0	—	0	—	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	—	43	—	45	—	50	ns
t_{OH}	Output Hold from Address Change	10	—	10	—	10	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	85	—	100	—	120	ns
Write Cycle								
t_{WC}	Write Cycle Time	85	—	100	—	120	—	ns
t_{WP}	Write Pulse Width	65	—	75	—	90	—	ns
t_{AS}	Address Set-up Time	2	—	5	—	5	—	ns
t_{AW}	Address Valid to End of Write	82	—	90	—	100	—	ns
t_{CW}	Chip Select to End of Write	80	—	85	—	100	—	ns
t_{DW}	Data to Write Time Overlap	38	—	40	—	45	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}(1)	Write Enable to Output in High Z	—	33	—	35	—	40	ns
t_{OW}(1)	Output Active from End of Write	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

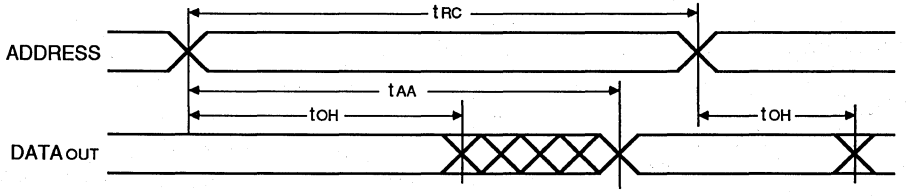
2822 tbl 08

B

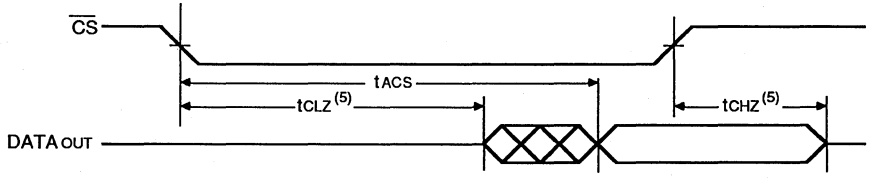
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)

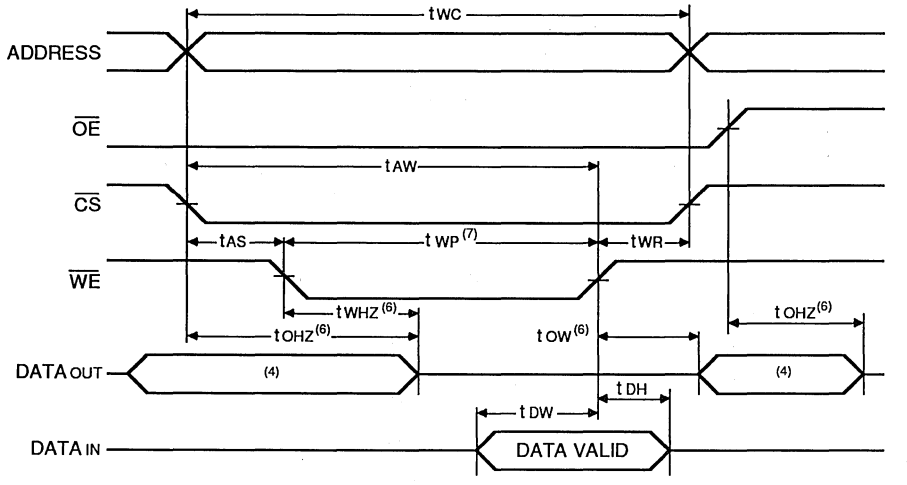


TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)

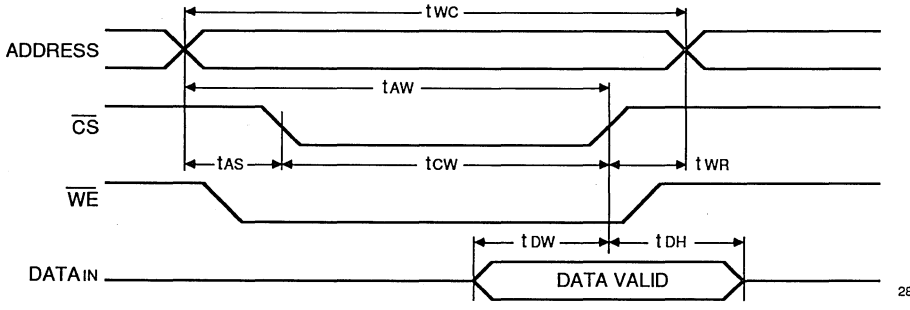


NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)

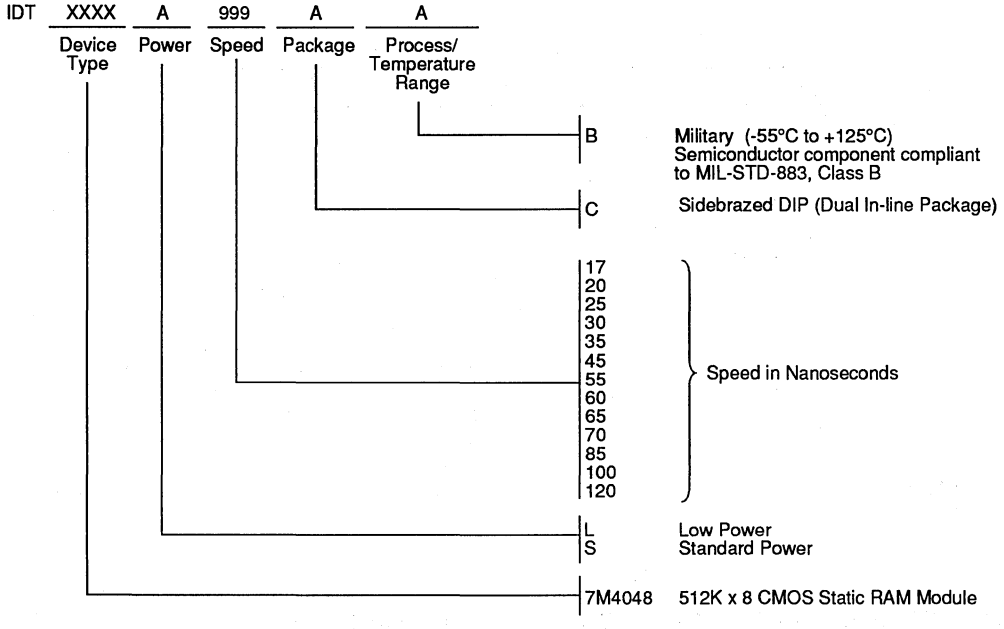


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse ((tWP) > tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

ORDERING INFORMATION



2822 drw 09

Integrated Device Technology, Inc.

512K x 8 CMOS STATIC RAM MODULE

PRELIMINARY
IDT7M4048
IDT7MB4048

FEATURES:

- High density 4 megabit (512K x 8) static RAM module
- Equivalent to the JEDEC standard for future monolithic 512K x 8 static RAMs
- Fast access time: 17ns (max.)
- Low power consumption (L version)
  - — Active: 110mA (max.)
  - — CMOS Standby: 400µA (max.)
  - — Data Retention: 200µA (max.) Vcc = 2V
- Surface mounted plastic packages on a 32-pin, 600 mil ceramic or FR-4 DIP substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible

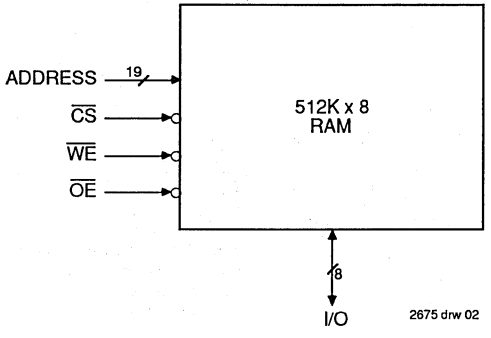
DESCRIPTION:

The IDT7M4048/7MB4048 is a 4 megabit (512K x 8) static RAM module constructed on a co-fired ceramic or multilayer epoxy laminate (FR-4) substrate using four 1 megabit static RAMs and a decoder. The IDT7MB4048 is available with access times as fast as 17ns. For low power applications, the IDT7M4048 version offers a data retention current of 200µA and a standby current of 400µA.

The IDT7M4048 is packaged in a 32-pin ceramic DIP. This results in a package 1.7 inches long and 0.6 inches wide, packing 4 megabits into the JEDEC DIP footprint. The IDT7MB4048 likewise is packaged in a 32-pin FR-4 DIP resulting in the same JEDEC footprint in a package 1.6 inches long and 0.6 inches wide.

All inputs and outputs of the IDT7M4048 and 7MB4048 are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



B

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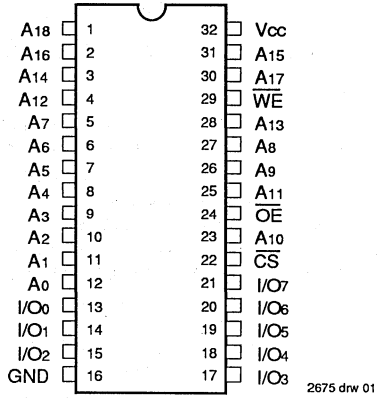
PIN CONFIGURATION[1]



DIP
TOP VIEW

NOTE:
1. For module dimensions, please refer to the module drawings in the packaging section.

PIN NAMES

I/O_{0-7}	Data Inputs/Outputs
A_{0-18}	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power
GND	Ground

2675 tbl 01

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	DOUT	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	DIN	Active

2675 tbl 09

CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	35	pF
CIN(C)	Input Capacitance ($\overline{CS}$)	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	35	pF

NOTE:
1. This parameter is guaranteed by design, but not tested.

2675 tbl 10

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	–10 to +85	°C
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2675 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE:
1. VIL = -2.0V for pulse width less than 10ns.

2675 tbl 03

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%

2675 tbl 04

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	7M4048LxxN		7MB4048SxxP		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	4	—	8	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	4	—	8	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 2mA[1], I_{OL} = 8mA[2]	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -1mA[1], I_{OH} = –4mA[2]	2.4	—	2.4	—	V
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS} \leq V_{IL}$; f = f_{MAX}, Outputs Open	—	110	—	480	mA
I_{SB}	Standby Supply Current (TTL Levels)	$\overline{CS} \geq V_{IH}$, V_{CC} = Max., f = f_{MAX}, Outputs Open	—	12	—	250	mA
I_{SB1}	Full Standby Supply Current (CMOS Levels)	$\overline{CS} \geq V_{CC}$ - 0.2V, $V_{IN} \geq V_{CC}$ - 0.2V or ≤ 0.2V	—	0.4	—	50	mA

NOTES:
1. For 7M4048LxxN version only.
2. For 7MB4048SxxP version only.

2675 tbl 05

DATA RETENTION CHARACTERISTICS[1, 4]

(T_A = 0°C to +70°C)

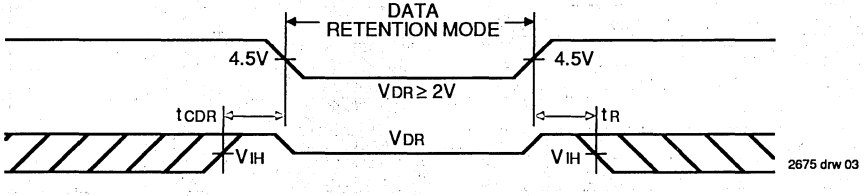
Symbol	Parameter	Test Condition	Min.	Max. Vcc @ 2.0V	Unit
V_{DR}	Vcc for Data Retention	—	2.0	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ - 0.2V	—	200	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time	$V_{IN} \leq V_{CC}$ - 0.2V or	0	—	ns
t_R[3]	Operation Recovery Time	$V_{IN} \geq$ 0.2V	t_{RC}[2]	—	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by design, but not tested.
4. For 7M4048LxxN version only.

2675 tbl 09

B

DATA RETENTION WAVEFORM



2675 drw 03

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2675 tbl 07

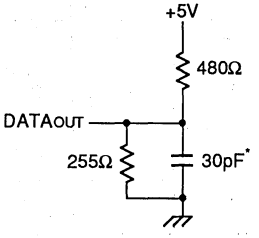


Figure 1. Output Load

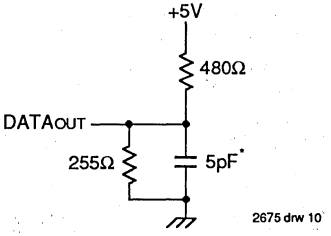


Figure 2. Output Load
(for t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, t_{OW} and t_{CLZ})

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

		7MB4048SxxP										
		-17[3]		-20[3]		-25		-30P		-35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle												
t_{RC}	Read Cycle Time	17	—	20	—	25	—	30	—	35	—	ns
t_{AA}	Address Access Time	—	17	—	20	—	25	—	30	—	35	ns
t_{ACS}	Chip Select Access Time	—	17	—	20	—	25	—	30	—	35	ns
t_{OE}	Output Enable to Output Valid	—	8	—	10	—	12	—	15	—	15	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	7	—	8	—	12	—	12	—	15	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	12	—	13	—	14	—	16	—	20	ns
t_{OH}	Output Hold from Address Change	1	—	3	—	3	—	3	—	3	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	17	—	20	—	25	—	30	—	35	ns
Write Cycle												
t_{WC}	Write Cycle Time	17	—	20	—	25	—	30	—	35	—	ns
t_{WP}	Write Pulse Width	14	—	15	—	17	—	20	—	25	—	ns
t_{AS}[2]	Address Set-up Time	3	—	3	—	3	—	0	—	0	—	ns
t_{AW}	Address Valid to End of Write	17[4]	—	18	—	20	—	25	—	30	—	ns
t_{CW}	Chip Select to End of Write	17	—	18	—	20	—	25	—	30	—	ns
t_{DW}	Data to Write Time Overlap	10	—	12	—	15	—	17	—	20	—	ns
t_{DH}[2]	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WR}[2]	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	10	—	13	—	15	—	15	—	15	ns
t_{OW}[1]	Output Active from End of Write	2	—	2	—	2	—	5	—	5	—	ns

2675 tbl 06

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. tAS=0ns for $\overline{CS}$ controlled write cycles. tDH, tWR= 3ns for $\overline{WE}$ controlled write cycles.
3. Preliminary specifications only.
4. tAW=14ns for $\overline{CS}$ controlled write cycles.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MB4048SxxP				7M4048LxxN						Unit
		-45		-55		-60[3]		-65[3]		-70		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t_{RC}	Read Cycle Time	45	—	55	—	65	—	65	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	60	—	65	—	70	ns
t_{ACS}	Chip Select Access Time	—	45	—	55	—	60	—	65	—	70	ns
t_{OE}	Output Enable to Output Valid	—	25	—	30	—	30	—	35	—	45	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	20	—	20	—	25	—	25	—	30	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	3	—	5	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	20	—	20	—	25	—	25	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	10	—	10	—	—	10	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	45	—	55	—	65	—	65	—	70	ns
Write Cycle												
t_{WC}	Write Cycle Time	45	—	55	—	65	—	65	—	70	—	ns
t_{WP}	Write Pulse Width	35	—	45	—	50	—	55	—	55	—	ns
t_{AS}	Address Set-up Time	5	—	5	—	0	—	0	—	0	—	ns
t_{AW}	Address Valid to End of Write	40	—	50	—	60	—	65	—	65	—	ns
t_{CW}	Chip Select to End of Write	40	—	50	—	60	—	65	—	65	—	ns
t_{DW}	Data to Write Time Overlap	20	—	20	—	30	—	30	—	35	—	ns
t_{DH}	Data Hold Time	0[2]	—	0[2]	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0[2]	—	0[2]	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	15	—	20	—	25	—	25	—	30	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	0	—	0	—	0	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. t_{AS}=0ns for $\overline{CS}$ controlled write cycles. t_{DH}, t_{WR}= 5ns for $\overline{WE}$ controlled write cycles.
3. Preliminary specifications only.

2675 tbl 06

B

AC ELECTRICAL CHARACTERISTICS

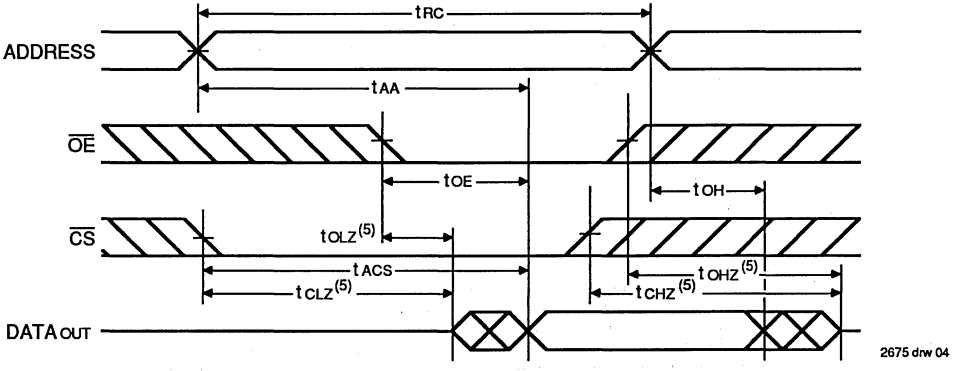
(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7M4048LxxN						Unit
		-85		-100		-120		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	85	—	100	—	120	—	ns
t_{AA}	Address Access Time	—	85	—	100	—	120	ns
t_{ACS}	Chip Select Access Time	—	85	—	100	—	120	ns
t_{OE}	Output Enable to Output Valid	—	48	—	50	—	60	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	33	—	35	—	40	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	0	—	0	—	0	—	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	—	43	—	45	—	50	ns
t_{OH}	Output Hold from Address Change	10	—	10	—	10	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	85	—	100	—	120	ns
Write Cycle								
t_{WC}	Write Cycle Time	85	—	100	—	120	—	ns
t_{WP}	Write Pulse Width	65	—	75	—	90	—	ns
t_{AS}	Address Set-up Time	2	—	5	—	5	—	ns
t_{AW}	Address Valid to End of Write	82	—	90	—	100	—	ns
t_{CW}	Chip Select to End of Write	80	—	85	—	100	—	ns
t_{DW}	Data to Write Time Overlap	38	—	40	—	45	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}(1)	Write Enable to Output in High Z	—	33	—	35	—	40	ns
t_{OW}(1)	Output Active from End of Write	0	—	0	—	0	—	ns

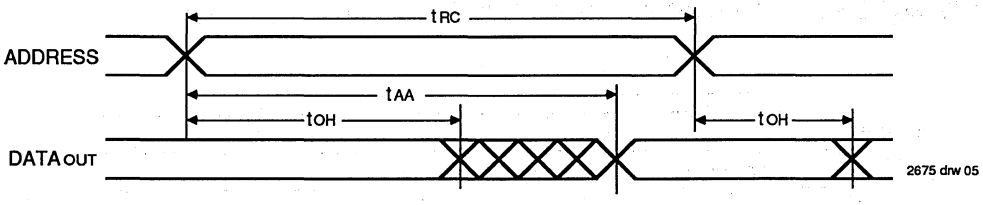
NOTE:
1. This parameter is guaranteed by design, but not tested.

2675 tbl 08

TIMING WAVEFORM OF READ CYCLE NO. 1(1)

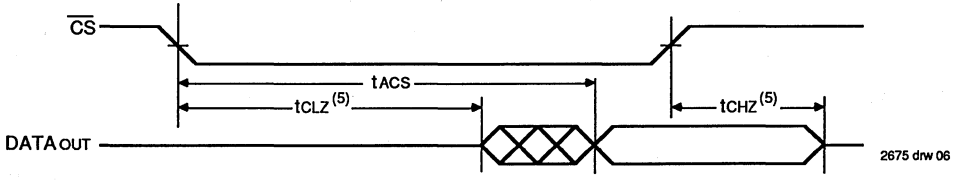


TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



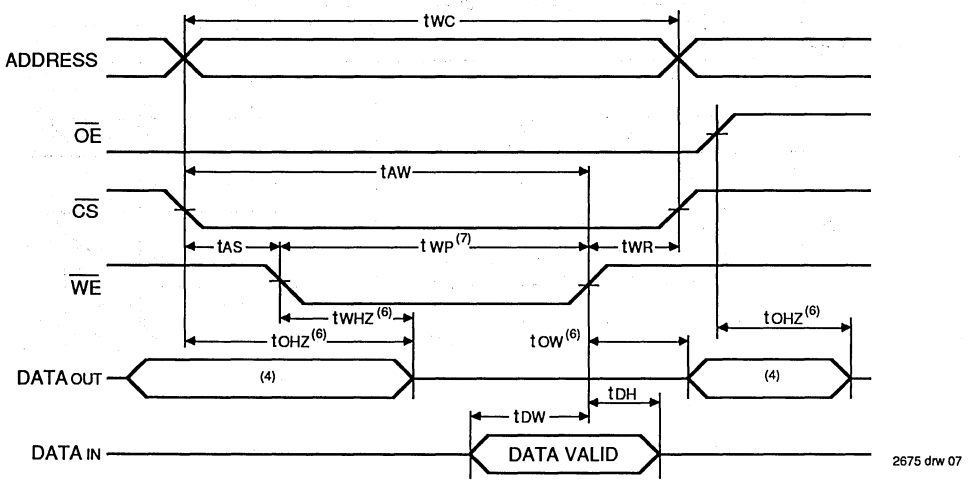
B

TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)

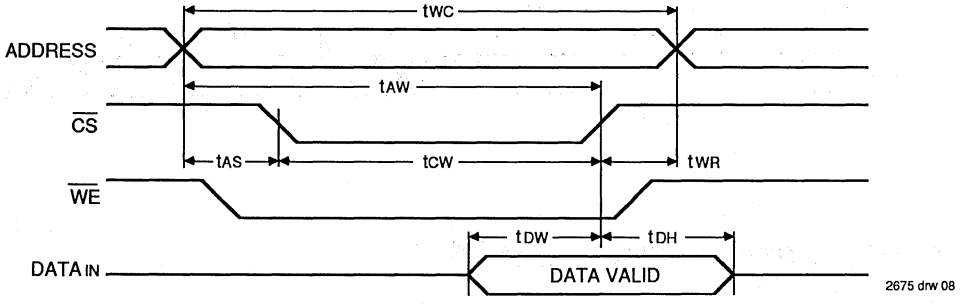


NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)

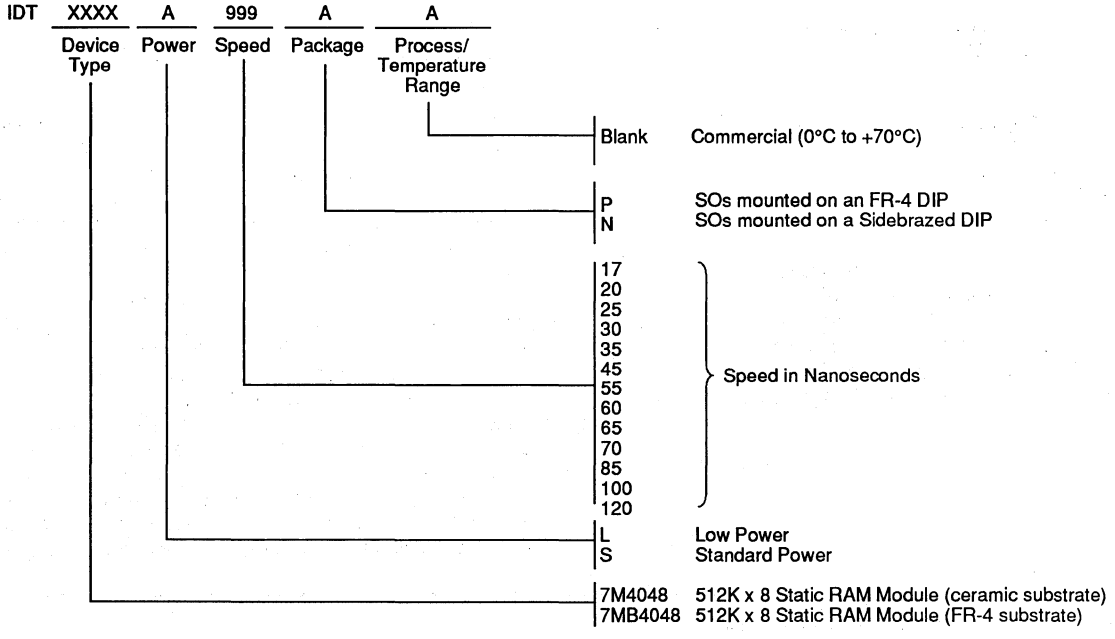


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse ((tWP) > tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

ORDERING INFORMATION



2675 drw 09

B

Integrated Device Technology, Inc.

256K x 8
CMOS STATIC RAM MODULE

PRELIMINARY
IDT7M4068

FEATURES:

- High density 2 megabit CMOS static RAM module
- Equivalent to the JEDEC standard for future monolithic 256K x 8 static RAMs
- Fast access time: 17ns (max.)
- Low power consumption (L version)
  - — Active: 110mA (max.)
  - — CMOS Standby: 700µA (max.)
  - — Data Retention: 400µA (max.) Vcc = 2V
- Surface mounted LCCs (leadless chip carriers) on a 32-pin, 600 mil ceramic DIP substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible

DESCRIPTION:

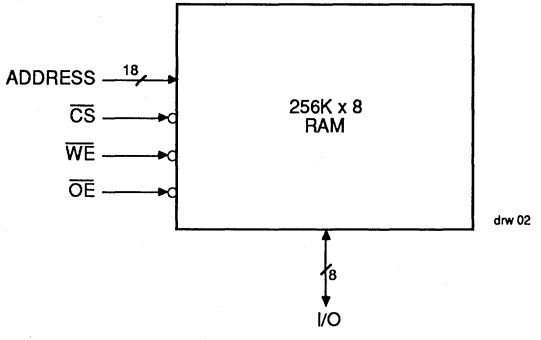
The IDT7M4068 is a 2 megabit (256K x 8) CMOS static RAM module constructed on a co-fired ceramic substrate using two 1 Megabit static RAMs and a decoder. The IDT7M4068 is available with access times as fast as 17ns. For low power applications, the IDT7M4068 version offers a data retention current of 400µA and a standby current of 700µA.

The IDT7M4068 is packaged in a 32-pin ceramic DIP. This results in a package 1.7 inches long and 0.6 inches wide, packing 2 megabits into the JEDEC DIP footprint.

All inputs and outputs of the IDT7M4068 are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

All IDT military module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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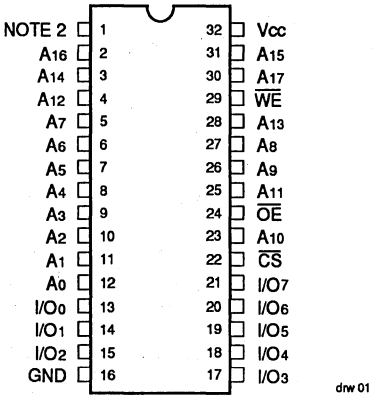
MILITARY TEMPERATURE RANGE **MAY 1991**

PIN CONFIGURATION[1]



drw 01

DIP
TOP VIEW

NOTE:
1. For module dimensions, please refer to the module drawings in the packaging section.
2. For proper operation of the module, Pin 1 must be connected to GND.

PIN NAMES

I/O0-7	Data Inputs/Outputs
A0-17	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power
GND	Ground

2675 tbl 01

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	DOUT	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	DIN	Active

2675 tbl 11

CAPACITANCE[1] (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	25	pF
CIN(C)	Input Capacitance ($\overline{CS}$)	VIN = 0V	10	pF
COUT	Output Capacitance	VOUT = 0V	25	pF

NOTE:
1. This parameter is guaranteed by design, but not tested.

2675 tbl 10

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	-55 to +125	°C
TBIAS	Temperature Under Bias	–65 to +135	°C
TSTG	Storage Temperature	–65 to +160	°C
IOUT	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2675 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE:
1. VIL = -2.0V for pulse width less than 10ns.

2675 tbl 03

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%

2675 tbl 04

B

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	Test Conditions	7M4068SxxCB, 7M4068LxxCB				Unit
			17ns-55ns		60ns-120ns		
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	—	10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 2mA(1), I_{OL} = 8mA(2)	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -1mA(1), I_{OH} = –4mA(2)	2.4	—	2.4	—	V
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS} \le V_{IL}$; f = f_{MAX}, Outputs Open	—	240	—	110	mA
I_{SB}	Standby Supply Current (TTL Levels)	$\overline{CS} \ge V_{IH}$, V_{CC} = Max., f = f_{MAX}, Outputs Open	—	60	—	6	mA
I_{SB1}	Full Standby Supply Current (CMOS Levels)	$\overline{CS} \ge V_{CC}$ - 0.2V, $V_{IN} \ge V_{CC}$ - 0.2V or ≤ 0.2V	—	30	—	2	mA
		Very Low Power Version(3)	—	30	—	0.7	mA

NOTES:
1. For 60ns-120ns versions only.
2. For 17ns-55ns versions only.
3. L version only.

2675 tbl 05

DATA RETENTION CHARACTERISTICS(5)

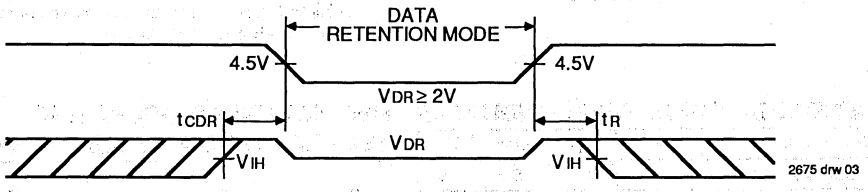
(T_A = -55°C to +125°C)

Symbol	Parameter	Test Condition	Min.	Max. V_{CC} @ 2.0V	Unit
V_{DR}	V_{CC} for Data Retention	—	2.0	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \ge V_{CC}$ - 0.2V	—	1(4)	mA
t_{CDR}(3)	Chip Deselect to Data Retention Time	$V_{IN} \le V_{CC}$ - 0.2V or	0	—	ns
t_R(3)	Operation Recovery Time	$V_{IN} \ge$ 0.2V	t_{RC}(2)	—	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by design, but not tested.
4. For 60ns-120ns versions, ICCDR=400µA.
5. L version only.

2675 tbl 09

DATA RETENTION WAVEFORM



2675 drw 03

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2675 tbl 07

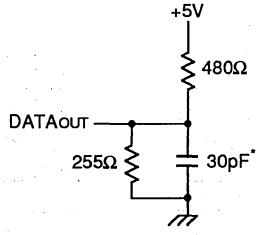


Figure 1. Output Load

* Including scope and jig

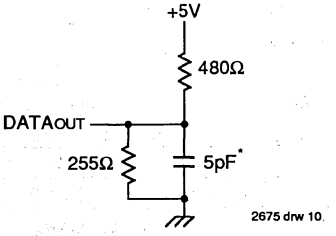


Figure 2. Output Load
(for tOLZ, tCHZ, tOHZ, tWHZ, tOW and tCLZ)

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

		7M4068SxxCB, 7M4068LxxCB										
		-17(3)		-20(3)		-25		-30		-35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	17	—	20	—	25	—	30	—	35	—	ns
tAA	Address Access Time	—	17	—	20	—	25	—	30	—	35	ns
tACS	Chip Select Access Time	—	17	—	20	—	25	—	30	—	35	ns
tOE	Output Enable to Output Valid	—	8	—	10	—	12	—	15	—	15	ns
tOHZ(1)	Output Disable to Output in High Z	—	7	—	8	—	12	—	12	—	15	ns
tOLZ(1)	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	0	—	ns
tCLZ(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
tCHZ(1)	Chip Deselect to Output in High Z	—	12	—	13	—	14	—	16	—	20	ns
tOH	Output Hold from Address Change	1	—	3	—	3	—	3	—	3	—	ns
tPU(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
tPD(1)	Chip Deselect to Power-Down Time	—	17	—	20	—	25	—	30	—	35	ns
Write Cycle												
tWC	Write Cycle Time	17	—	20	—	25	—	30	—	35	—	ns
tWP	Write Pulse Width	14	—	15	—	17	—	20	—	25	—	ns
tAS(2)	Address Set-up Time	3	—	3	—	3	—	0	—	0	—	ns
tAW	Address Valid to End of Write	17(4)	—	18	—	20	—	25	—	30	—	ns
tCW	Chip Select to End of Write	17	—	18	—	20	—	25	—	30	—	ns
tDW	Data to Write Time Overlap	10	—	12	—	15	—	17	—	20	—	ns
tDH(2)	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWR(2)	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tWHZ(1)	Write Enable to Output in High Z	—	10	—	13	—	15	—	15	—	15	ns
tOW(1)	Output Active from End of Write	2	—	2	—	2	—	5	—	5	—	ns

NOTES:
2675 tbl 06

1. This parameter is guaranteed by design, but not tested.
2. tAS=0ns for $\overline{CS}$ controlled write cycles. tDH, tWR= 3ns for $\overline{WE}$ controlled write cycles.
3. Preliminary specifications only.
4. tAW=14ns for $\overline{CS}$ controlled write cycles.

B

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	7M4068SxxCB, 7M4068LxxCB										Unit
		-45		-55		-60[3]		-65[3]		-70		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t_{RC}	Read Cycle Time	45	—	55	—	65	—	65	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	60	—	65	—	70	ns
t_{ACS}	Chip Select Access Time	—	45	—	55	—	60	—	65	—	70	ns
t_{OE}	Output Enable to Output Valid	—	25	—	30	—	30	—	35	—	45	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	20	—	20	—	25	—	25	—	30	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	3	—	5	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	20	—	20	—	25	—	25	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	10	—	10	—	—	10	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	45	—	55	—	65	—	65	—	70	ns
Write Cycle												
t_{WC}	Write Cycle Time	45	—	55	—	65	—	65	—	70	—	ns
t_{WP}	Write Pulse Width	35	—	45	—	50	—	55	—	55	—	ns
t_{AS}	Address Set-up Time	5	—	5	—	0	—	0	—	0	—	ns
t_{AW}	Address Valid to End of Write	40	—	50	—	60	—	65	—	65	—	ns
t_{CW}	Chip Select to End of Write	40	—	50	—	60	—	65	—	65	—	ns
t_{DW}	Data to Write Time Overlap	20	—	20	—	30	—	30	—	35	—	ns
t_{DH}	Data Hold Time	0[2]	—	0[2]	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0[2]	—	0[2]	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	15	—	20	—	25	—	25	—	30	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	0	—	0	—	0	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. t_{AS}=0ns for $\overline{CS}$ controlled write cycles. t_{DH}, t_{WR}= 5ns for $\overline{WE}$ controlled write cycles.
3. Preliminary specifications only.

2675 tbl 12

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

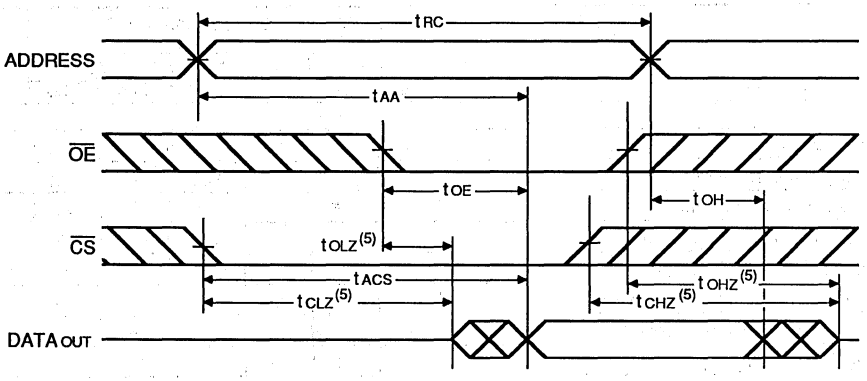
Symbol	Parameter	7M4068SxxCB, 7M4068LxxCB						Unit
		-85		-100		-120		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	85	—	100	—	120	—	ns
t_{AA}	Address Access Time	—	85	—	100	—	120	ns
t_{ACS}	Chip Select Access Time	—	85	—	100	—	120	ns
t_{OE}	Output Enable to Output Valid	—	48	—	50	—	60	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	33	—	35	—	40	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	43	—	45	—	50	ns
t_{OH}	Output Hold from Address Change	10	—	10	—	10	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	85	—	100	—	120	ns
Write Cycle								
t_{WC}	Write Cycle Time	85	—	100	—	120	—	ns
t_{WP}	Write Pulse Width	65	—	75	—	90	—	ns
t_{AS}	Address Set-up Time	2	—	5	—	5	—	ns
t_{AW}	Address Valid to End of Write	82	—	90	—	100	—	ns
t_{CW}	Chip Select to End of Write	80	—	85	—	100	—	ns
t_{DW}	Data to Write Time Overlap	38	—	40	—	45	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	33	—	35	—	40	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

2675 tbl 13

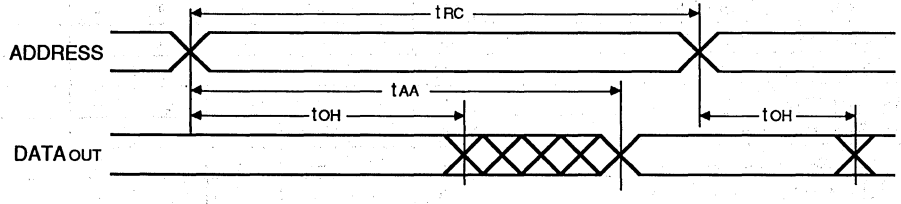
B

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



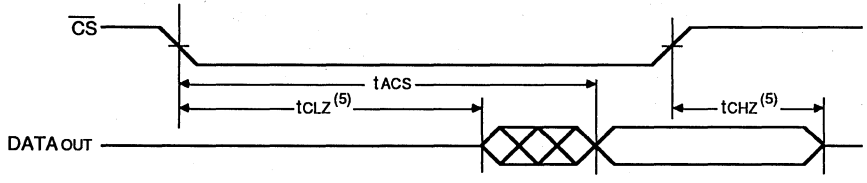
2675 drw 04

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2675 drw 05

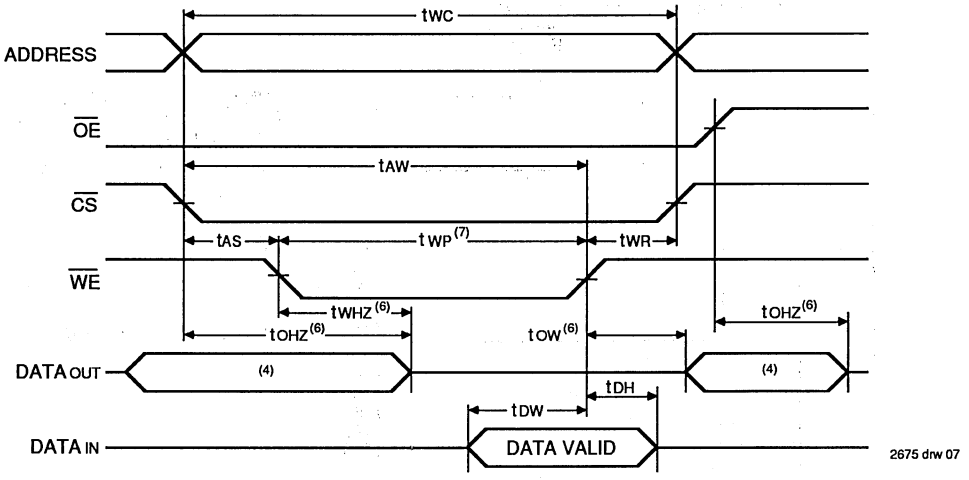
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



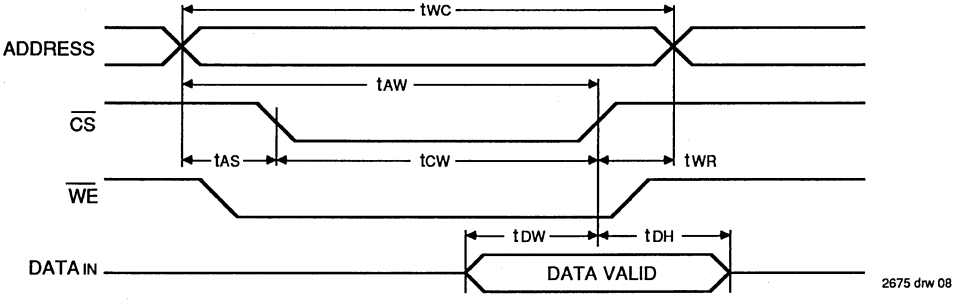
2675 drw 06

NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



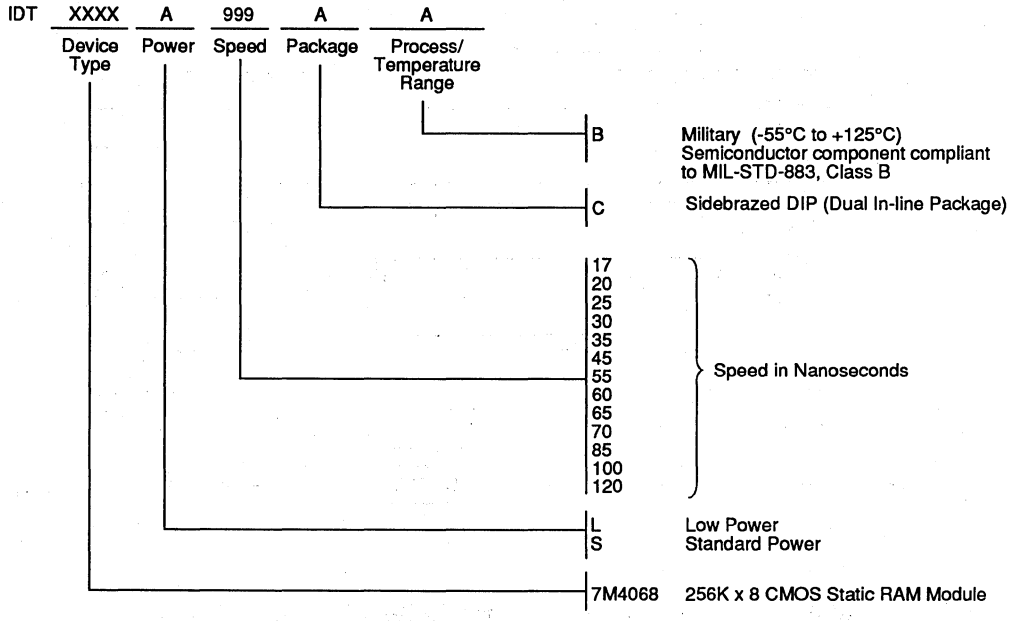
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



B

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse ((tWP) > tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

ORDERING INFORMATION



Integrated Device Technology, Inc.

256K x 8 CMOS STATIC RAM MODULE

PRELIMINARY
IDT7M4068
IDT7MB4068

FEATURES:

- High density 2 megabit CMOS static RAM module
- Equivalent to the JEDEC standard for future monolithic 256K x 8 static RAMs
- Fast access time: 17ns (max.)
- Low power consumption (L version)
  - — Active: 110mA (max.)
  - — CMOS Standby: 200µA (max.)
  - — Data Retention: 100µA (max.) Vcc = 2V
- Surface mounted plastic packages on a 32-pin, 600 mil ceramic or FR-4 DIP (Dual In-line Package) substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible

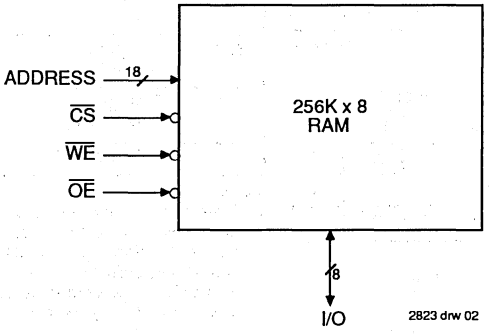
DESCRIPTION:

The IDT7M4068/7MB4068 is a 2 megabit (256K x 8) static RAM module constructed on a co-fired ceramic or multilayer epoxy laminate (FR-4) substrate using two 1 Megabit static RAMs and a decoder. The IDT7MB4068 is available with access times as fast as 17ns. For low power applications, the IDT7M4068 version offers a data retention current of 100µA and a standby current of 200µA.

The IDT7M4068 is packaged in a 32-pin ceramic DIP. This results in a package 1.7 inches long and 0.6 inches wide, packing 2 megabits into the JEDEC DIP footprint. The IDT7MB4068 likewise is packaged in a 32-pin FR-4 DIP resulting in the same JEDEC footprint in a package 1.6 inches long and 0.6 inches wide.

All inputs and outputs of the IDT7M4068 and 7MB4068 are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

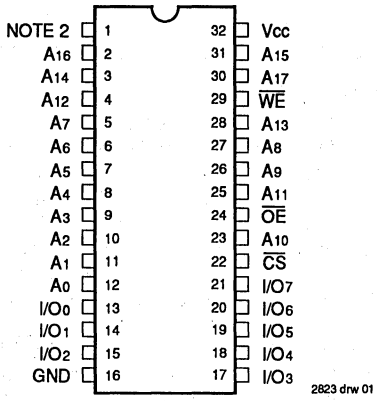
FUNCTIONAL BLOCK DIAGRAM



B

CEMOS is a trademark of Integrated Device Technology Inc.

PIN CONFIGURATION[1]



2823 drw 01

DIP
TOP VIEW

NOTES:
1. For module dimensions, please refer to the module drawings in the packaging section.
2. For proper operation of the 7M4068LxxN module, Pin 1 must be connected to GND. For 7MB4068xxP module, Pin 1 is a no connect.

PIN NAMES

I/O0-7	Data Inputs/Outputs
A0-17	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power
GND	Ground

2823 tbl 01

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	DOUT	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	DIN	Active

2823 tbl 09

CAPACITANCE[1] (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	25	pF
CIN(C)	Input Capacitance ($\overline{CS}$)	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	25	pF

NOTE:
1. This parameter is guaranteed by design, but not tested.

2823 tbl 10

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	–10 to +85	°C
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2823 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE:
1. VIL = -2.0V for pulse width less than 10ns.

2823 tbl 03

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%

2823 tbl 04

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	7M4068LxxN		7MB4068SxxP		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	2	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	2	—	10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 2mA[1], I_{OL} = 8mA[2]	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -1mA[1], I_{OH} = –4mA[2]	2.4	—	2.4	—	V
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ ≤ V_{IL}; f = f_{MAX}, Outputs Open	—	110	—	300	mA
I_{SB}	Standby Supply Current (TTL Levels)	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., f = f_{MAX}, Outputs Open	—	6	—	120	mA
I_{SB1}	Full Standby Supply Current (CMOS Levels)	$\overline{CS}$ ≥ V_{CC} - 0.2V, V_{IN} ≥ V_{CC} - 0.2V or ≤ 0.2V	—	0.2	—	20	mA

NOTES:
1. For 7M4068LxxN version only.
2. For 7MB4068SxxP version only.

2823 tbl 05

DATA RETENTION CHARACTERISTICS[1, 4]

(T_A = 0°C to +70°C)

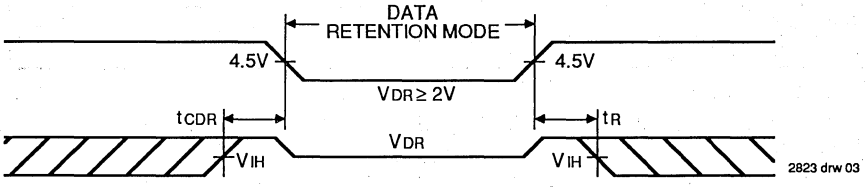
Symbol	Parameter	Test Condition	Min.	Max. V_{CC} @ 2.0V	Unit
V_{DR}	V_{CC} for Data Retention	—	2.0	—	V
I_{CCDR}	Data Retention Current	$\overline{CS}$ ≥ V_{CC} - 0.2V	—	100	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time	V_{IN} ≤ V_{CC} - 0.2V or	0	—	ns
t_R[3]	Operation Recovery Time	V_{IN} ≥ 0.2V	t_{RC}[2]	—	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by design, but not tested.
4. For 7M4068LxxN version only.

2823 tbl 09

B

DATA RETENTION WAVEFORM



2823 drw 03

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2823 tbl 07

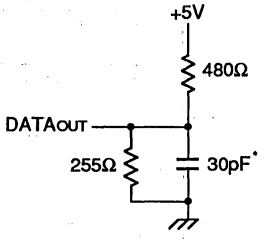


Figure 1. Output Load

* Including scope and jig

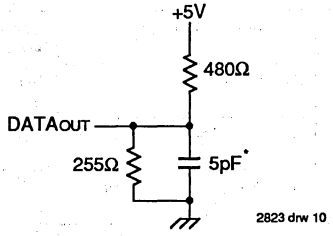


Figure 2. Output Load
(for tOLZ, tCHZ, tOHZ, tWHZ, tOW and tCLZ)

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

		7MB4068SxxP										
		-17[2]		-20[2]		-25		-30		-35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	17	—	20	—	25	—	30	—	35	—	ns
tAA	Address Access Time	—	17	—	20	—	25	—	30	—	35	ns
tACS	Chip Select Access Time	—	17	—	20	—	25	—	30	—	35	ns
tOE	Output Enable to Output Valid	—	8	—	10	—	12	—	15	—	15	ns
tOHZ[1]	Output Disable to Output in High Z	—	7	—	10	—	12	—	12	—	15	ns
tOLZ[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	0	—	ns
tCLZ[1]	Chip Select to Output in Low Z	2	—	5	—	5	—	5	—	5	—	ns
tCHZ[1]	Chip Deselect to Output in High Z	—	10	—	10	—	14	—	16	—	20	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
tPU[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
tPD[1]	Chip Deselect to Power-Down Time	—	12	—	12	—	25	—	30	—	35	ns
Write Cycle												
tWC	Write Cycle Time	17	—	20	—	25	—	30	—	35	—	ns
tWP	Write Pulse Width	14	—	15	—	17	—	20	—	25	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tAW	Address Valid to End of Write	14	—	16	—	20	—	25	—	30	—	ns
tCW	Chip Select to End of Write	14	—	15	—	20	—	25	—	30	—	ns
tDW	Data to Write Time Overlap	10	—	12	—	15	—	17	—	20	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tWHZ[1]	Write Enable to Output in High Z	—	10	—	13	—	15	—	18	—	20	ns
tOW[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

2823 tbl 06

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MB4068SxxP				7M4068LxxN						Unit
		-45		-55		-60[2]		-65[2]		-70		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t_{RC}	Read Cycle Time	45	—	55	—	65	—	65	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	60	—	65	—	70	ns
t_{ACS}	Chip Select Access Time	—	45	—	55	—	60	—	65	—	70	ns
t_{OE}	Output Enable to Output Valid	—	25	—	30	—	30	—	35	—	45	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	20	—	20	—	25	—	25	—	30	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	0	—	0	—	3	—	5	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	20	—	25	—	25	—	25	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	10	—	10	—	—	10	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	45	—	55	—	65	—	65	—	70	ns
Write Cycle												
t_{WC}	Write Cycle Time	45	—	55	—	65	—	65	—	70	—	ns
t_{WP}	Write Pulse Width	35	—	45	—	50	—	55	—	55	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{AW}	Address Valid to End of Write	40	—	50	—	60	—	65	—	65	—	ns
t_{CW}	Chip Select to End of Write	40	—	50	—	60	—	65	—	65	—	ns
t_{DW}	Data to Write Time Overlap	25	—	25	—	30	—	30	—	35	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	25	—	25	—	25	—	25	—	30	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns

2823 tbl 06

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

B

AC ELECTRICAL CHARACTERISTICS

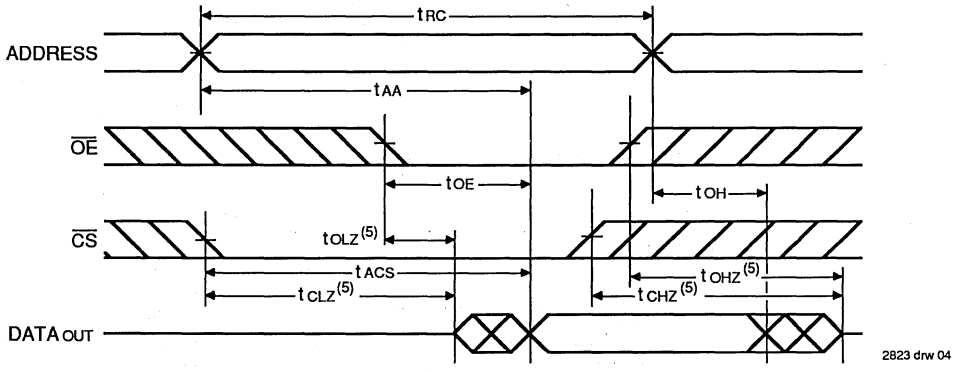
(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7M4068LxxN						Unit
		-85		-100		-120		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	85	—	100	—	120	—	ns
t_{AA}	Address Access Time	—	85	—	100	—	120	ns
t_{ACS}	Chip Select Access Time	—	85	—	100	—	120	ns
t_{OE}	Output Enable to Output Valid	—	48	—	50	—	60	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	33	—	35	—	40	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	0	—	0	—	0	—	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	—	43	—	45	—	50	ns
t_{OH}	Output Hold from Address Change	10	—	10	—	10	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	85	—	100	—	120	ns
Write Cycle								
t_{WC}	Write Cycle Time	85	—	100	—	120	—	ns
t_{WP}	Write Pulse Width	65	—	75	—	90	—	ns
t_{AS}	Address Set-up Time	2	—	5	—	5	—	ns
t_{AW}	Address Valid to End of Write	82	—	90	—	100	—	ns
t_{CW}	Chip Select to End of Write	80	—	85	—	100	—	ns
t_{DW}	Data to Write Time Overlap	38	—	40	—	45	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}(1)	Write Enable to Output in High Z	—	33	—	35	—	40	ns
t_{OW}(1)	Output Active from End of Write	0	—	0	—	0	—	ns

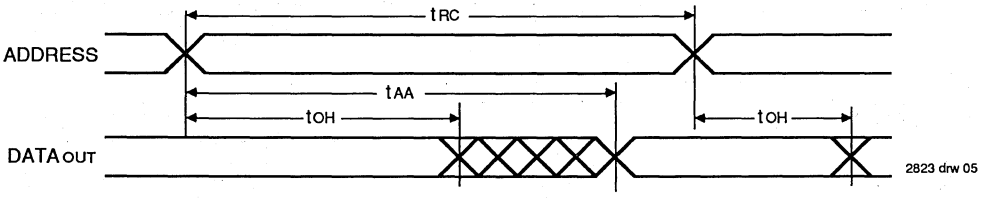
NOTE:
1. This parameter is guaranteed by design, but not tested.

2823 tbl 08

TIMING WAVEFORM OF READ CYCLE NO. 1(1)

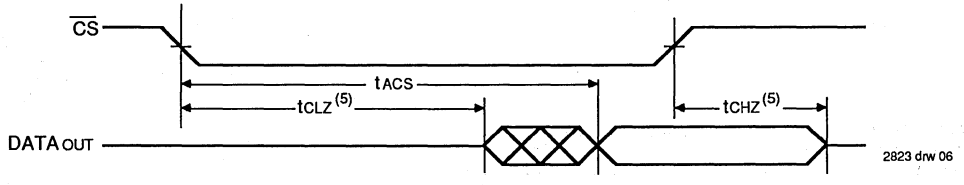


TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



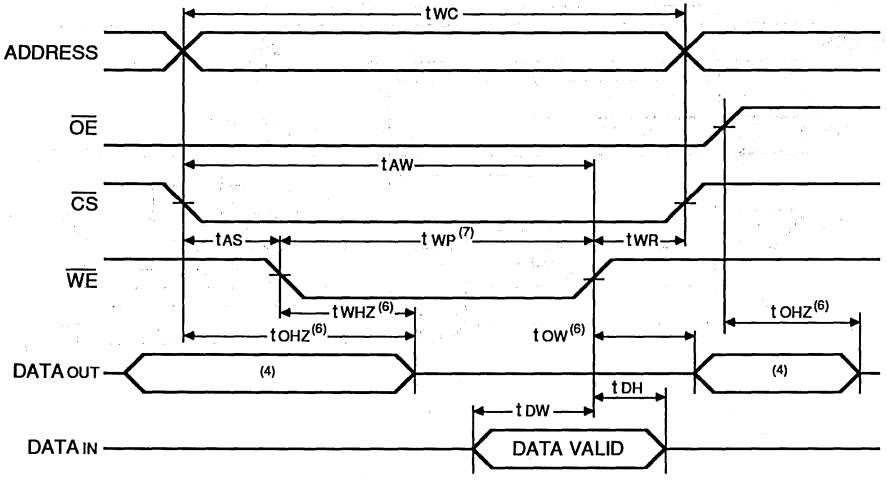
B

TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)

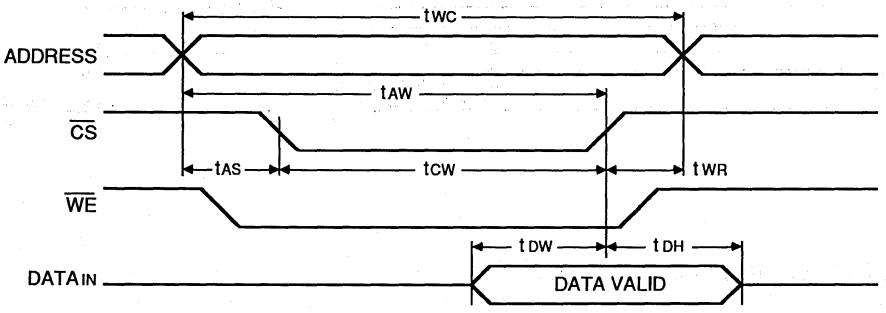


NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)

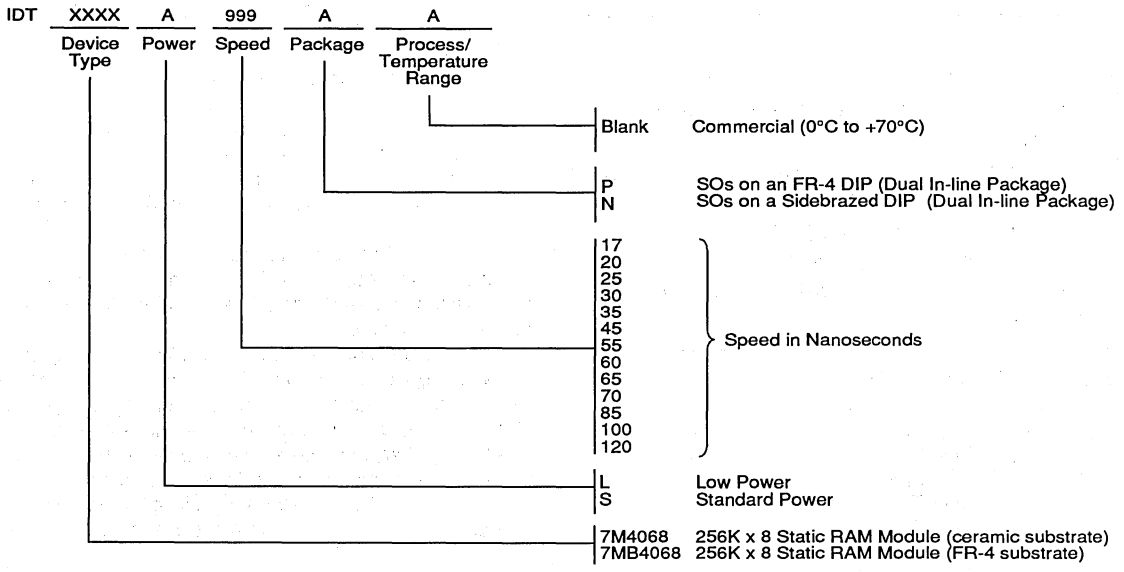


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse ((tWP) > tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

ORDERING INFORMATION



drw 09

B

Integrated Device Technology, Inc.

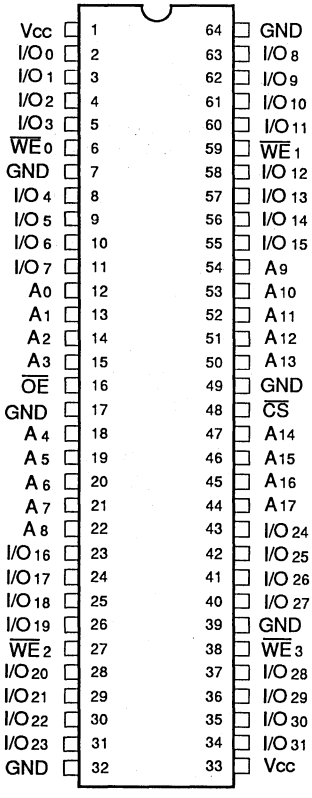
256K x 32 BiCMOS/CMOS STATIC RAM MODULE

PRELIMINARY
IDT7M4077

FEATURES:

- High density 8 megabit static RAM module
- Low profile 64 pin sidebraze DIP (Dual In-line Package)
- Very fast access time: 15ns (max.)
- Surface mounted leadless chip carrier (LCC) components on an multilayer ceramic substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible
- Multiple GND pins and decoupling capacitors for maximum noise immunity

PIN CONFIGURATION[1]



2814 drw 02

DIP
TOP VIEW

NOTES:

1. For module dimensions, please refer to module drawing in the packaging section.

DESCRIPTION:

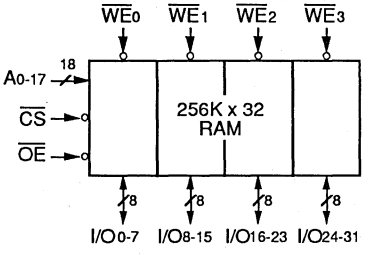
The IDT7M4077 is a 256K x 32 static RAM module constructed on an a multilayer ceramic substrate using 8 1 megabit static RAMs in leadless chip carrier (LCC) packages. Availability of four write enable lines (one for each group of two RAMs) provides byte write capability. The IDT7M4077 is available with access time as fast as 15ns with minimal power consumption.

The IDT7M4077 is packaged in a 64 pin sidebraze DIP (Dual In-line Package). The DIP configuration allows 64 pins to be placed on a package 3.2 inches long, 0.6 inches wide and 0.31 inches tall.

All inputs and outputs of the IDT7M4077 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

All IDT military modules are constructed with semiconductor components manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



2814 drw 01

PIN NAMES

I/O0–31	Data Inputs/Outputs
A0–17	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$0–3	Write Enables
$\overline{OE}$	Output Enable
Vcc	Power
GND	Ground

2814 tbl 01

BiCEMOS and CEMOS are trademarks of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–10 to +85	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTES: 2814 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	DATAOUT	Active
Write	L	X	L	DATAIN	Active
Read	L	H	H	High-Z	Active

2814 tbl 02

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CI/O	I/O Capacitance (Data)	V(IN) = 0V	15	pF
CIN1	Input Capacitance (Address & Control)	V(IN) = 0V	90	pF
CIN2	Input Capacitance ($\overline{WE}$)	V(IN) = 0V	35	pF

NOTE: 2814 tbl 04

1. This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2814 tbl 05

1. VIL (min) = –1.5V for pulse width less than 10ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2814 tbl 06

DC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V ±10%, TA = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Military Max.	Comm. Max.	Unit
|ILI|	Input Leakage (Address and Control)	VCC = Max.; VIN = GND to VCC	—	120	80	µA
|ILI|	Input Leakage (Data)	VCC = Max.; VIN = GND to VCC	—	15	10	µA
|ILI|	Input Leakage ($\overline{WE}$)	VCC = Max.; VIN = GND to VCC	—	30	20	µA
|ILO|	Output Leakage	VCC = Max.; $\overline{CS}$ = VIH, VOUT = GND to VCC	—	15	10	µA
VOL	Output Low	VCC = Min., IOL = 8mA	—	0.4	0.4	V
VOH	Output High	VCC = Min., IOH = –4mA	2.4	—	—	V

Symbol	Parameter	Test Conditions	7M4077B(1) Max.	7M4077S(1) Military Max.	7M4077S Comm. Max.	Unit
ICC	Dynamic Operating Current	f = fMAX; $\overline{CS}$ = VIL VCC = Max.; Output Open	1600	1540	1200	mA
ISB	Standby Supply Current	$\overline{CS}$ ≥ VIH, VCC = Max. Outputs Open, f = fMAX	—	800	480	mA
ISB1	Full Standby Supply Current	$\overline{CS}$ ≥ VCC – 0.2V; f = 0 VIN > VCC – 0.2V or < 0.2V	—	640	80	mA

NOTE: 2814 tbl 09

1. Preliminary specifications only.

B

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1-4

2814 tbl 08

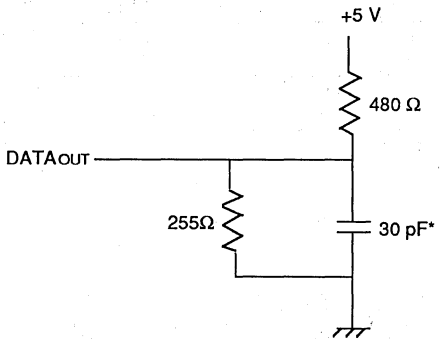
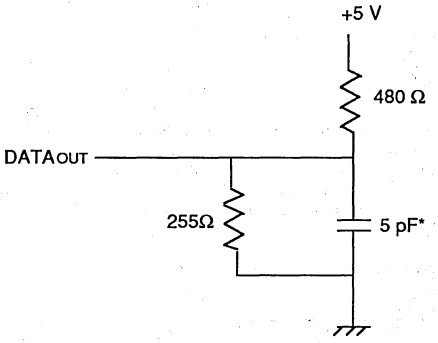


Figure 1. Output Load



2814 drw 03

Figure 2. Output Load
(for tOLZ, tOHZ, tCH Z, tCLZ, tWHZ, tOW)

* Includes scope and jig.

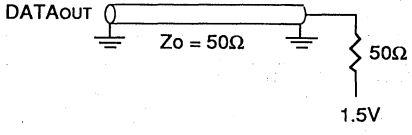
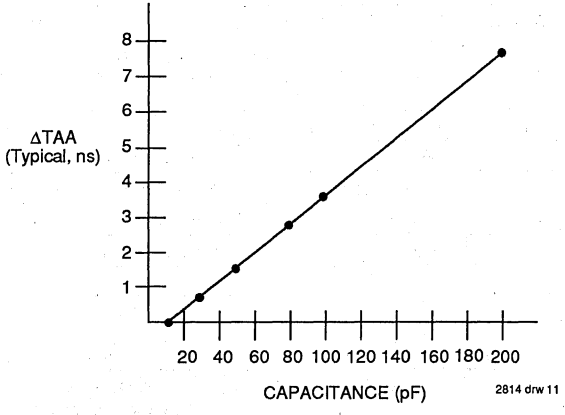


Figure 3. BiCMOS Output Load



2814 drw 11

Figure 4. BiCMOS Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

		7M4077Bxx						
		-15[2]		-17[2]		-20[2]		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle								
t_{RC}	Read Cycle Time	15	—	17	—	20	—	ns
t_{AA}	Address Access Time	—	15	—	17	—	20	ns
t_{ACS}	Chip Select Access Time	—	8	—	9	—	20	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	2	—	2	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	6	—	8	—	10	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	2	—	2	—	0	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	8	—	10	—	10	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	5	—	6	—	10	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	ns
Write Cycle								
t_{WC}	Write Cycle Time	15	—	17	—	20	—	ns
t_{CW}	Chip Select to End of Write	9	—	10	—	15	—	ns
t_{AW}	Address Valid to End of Write	10	—	12	—	16	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	10	—	12	—	15	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	6	—	7	—	13	ns
t_{DW}	Data to Write Time Overlap	6	—	8	—	12	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	2	—	2	—	0	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

2814 tbl 09

B

AC ELECTRICAL CHARACTERISTICS

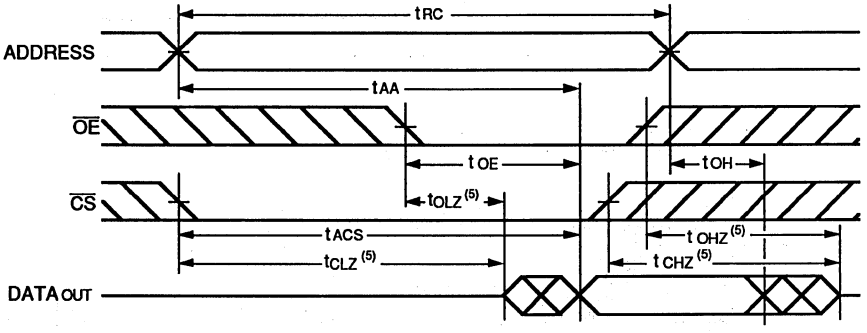
(V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

		7M4077Sxx										
		-25		-30		-35		-45		-55		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle												
t_{RC}	Read Cycle Time	25	—	30	—	35	—	45	—	55	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	—	45	—	55	ns
t_{ACS}	Chip Select Access Time	—	25	—	30	—	35	—	45	—	55	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	12	—	15	—	18	—	23	—	25	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	0	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	15	—	18	—	20	—	25	—	25	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	10	—	10	—	10	—	10	—	10	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	25	—	30	—	35	—	45	—	55	ns
Write Cycle												
t_{WC}	Write Cycle Time	25	—	30	—	35	—	45	—	55	—	ns
t_{CW}	Chip Select to End of Write	20	—	25	—	30	—	40	—	50	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	30	—	40	—	50	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	30	—	35	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	15	—	18	—	20	—	23	—	25	ns
t_{DW}	Data to Write Time Overlap	15	—	17	—	20	—	25	—	30	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

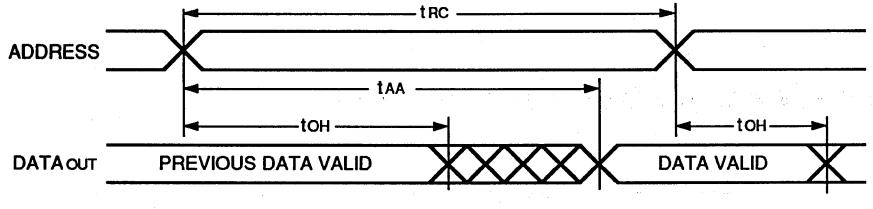
2814 tbl 09

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



2814 drw 04

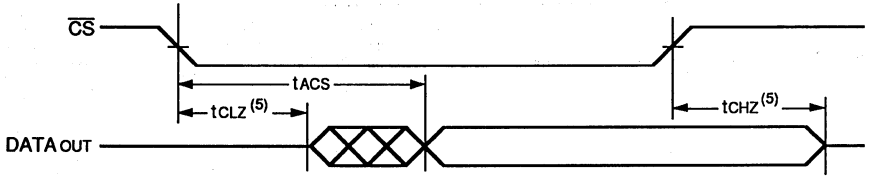
TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



2814 drw 05

B

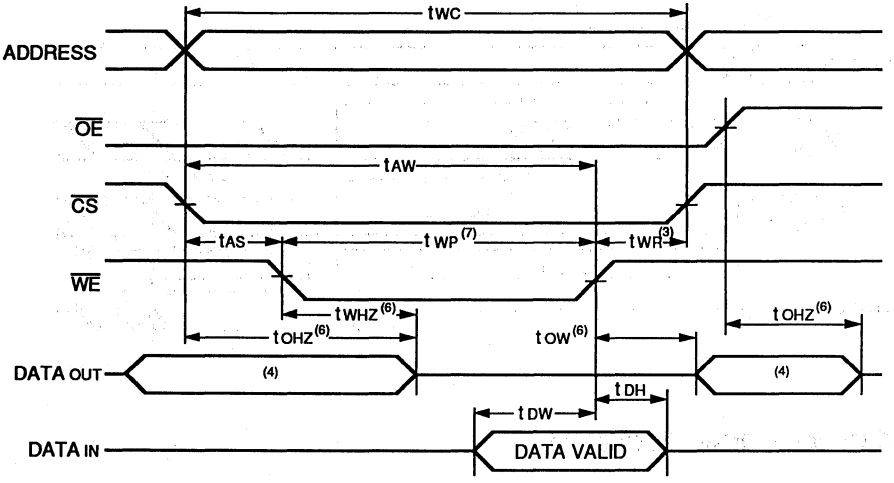
TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)



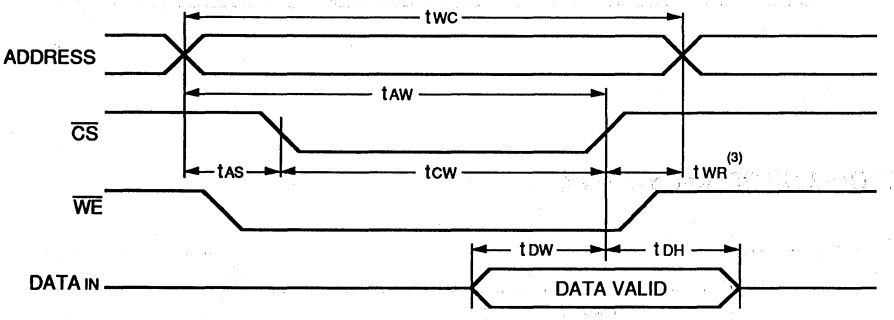
2814 drw 06

NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1,2,3,7)

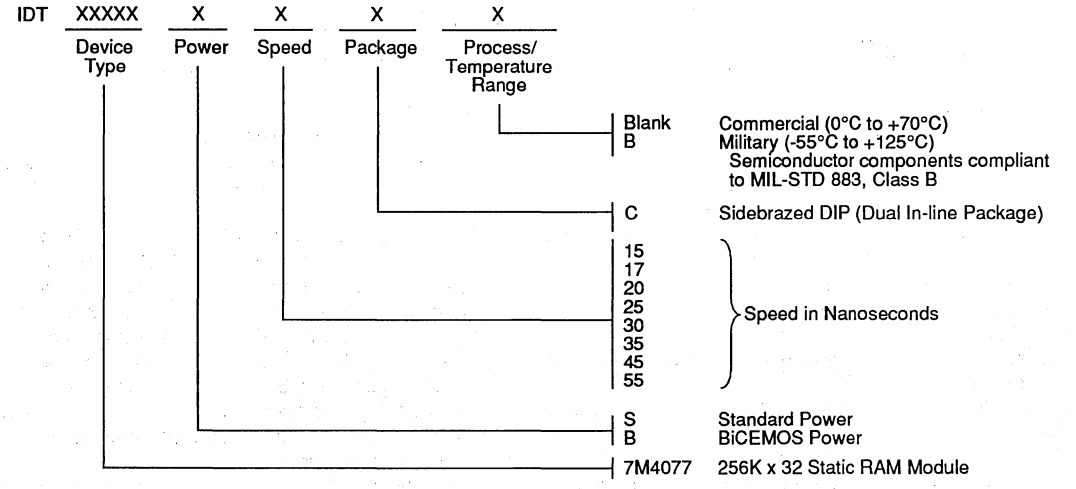


TIMING WAVEFORM OF WRITE CYCLE NO. 2(1,2,3,5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

ORDERING INFORMATION



2814 drw 10

B

Integrated Device Technology, Inc.

SUBSYSTEMS "FLEXI-PAK™" FAMILY
32K x 32
CMOS EEPROM MODULE

PRELIMINARY
IDT7M7004

FEATURES:

- High-density 1 megabit CMOS EEPROM modules
- Member of the Subsystems "Flexi-Pak" Family of interchangeable modules, with equivalent pin-outs, supporting a wide range of applications.
- Footprint compatible module upgrades to the next higher density with relative ease
- Fast access time:
  - — 75ns (max.) 7M7004 commercial
  - — 95ns (max.) 7M7004 military
- Surface mounted LCC components mounted on a co-fired ceramic substrate
- Offered in a 66-pin HIP (Hex In-line Package), occupying only 1 sq. inch of board space
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Please consult the factory regarding the number of Erase/ Write Cycles per Byte Minimum available on the module

DESCRIPTION:

The IDT7M7004 is a high-speed, high-density 1 megabit CMOS EEPROM module constructed on a multi-layer, co-fired ceramic substrate using 4 32K x 8 EEPROM components in leadlesss chip carriers.

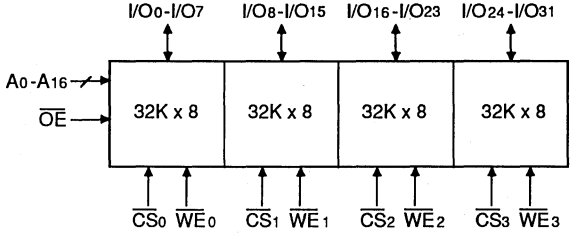
This module is part of the IDT Subsystems "Flexi-Pak" Family. This family of SRAM/EEPROM/EPROM memory modules support applications requiring stand alone static or programmmable memory or those applications needing a combination of both. All of these module configurations have equivalent pin-outs, making these "plug-in compatible" (i.e. inter-changeable), suitable for a wide range of applications.

The IDT7M7004 is available with access times as fast as 75ns over the commercial temperature range and 95ns over the military temperature range.

This family of IDT modules are offered in a 66-pin, ceramic HIP (Hex In-line Package). This HIP package is similar to a PGA and fits 1 megabit of memory into 1 sq. inch of board space.

All military IDT modules are assembled with semiconductor components compliant with the latest revision of MIL-STD-883 Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



2825 drw 01

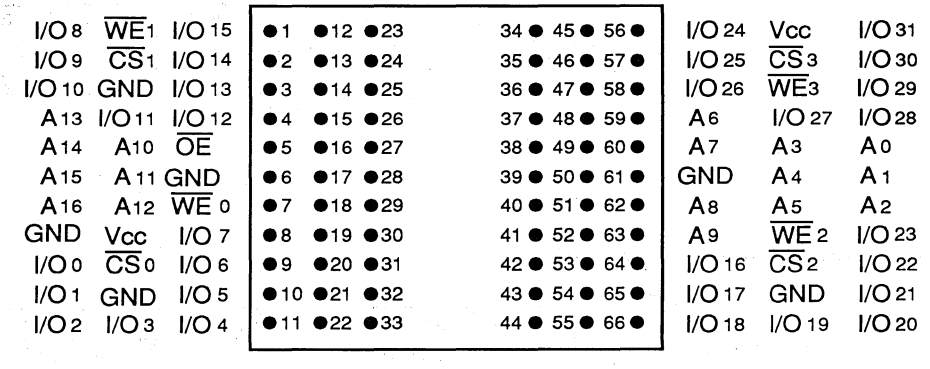
Flexi-Pak is a trademark of Integrated Device Technology, Inc.

PIN NAMES

Name	Description
I/O 0-31	Data Inputs/Outputs
A 0-16	Address Inputs
$\overline{WE}$ 0-3	Write Enables
$\overline{CS}$ 0-3	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground

Tbl 01

PIN CONFIGURATIONS (1, 2)



HIP
TOP VIEW

Drw 02

NOTES:
1. For module dimensions, please refer to the module drawings in the packaging section.
2. For the IDT7M7004 (32K x 32 version), pins 6 and 7 are no connects.

B

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to Ground	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–10 to +85	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

Tbl 04

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE (1)

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	DOUT	Active
Write	L	H	L	DIN	Active
Read	L	H	H	High Z	Active

Tbl 02

NOTE:
1. For the proper operation of the module, $\overline{OE}$ must be High for all Write Cycles.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

Tbl 05

NOTE:
1. VIL (min.) = –3.0V for pulse width less than 20ns.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN (1)	Input Capacitance (Data, $\overline{CS}$, $\overline{WE}$)	VIN = 0V	12	pF
CIN (2)	Input Capacitance (Address, $\overline{OE}$)	VIN = 0V	50	pF
COUT	Output Capacitance	VOUT = 0V	15	pF

Tbl 03

NOTE:
1. This parameter is guaranteed by design but not tested.

RECOMMENDED OPERATING TEMPERATURE AND VOLTAGE SUPPLY

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%
Military	-55°C to +125°C	0V	5.0V ± 10%

Tbl 06

DC ELECTRICAL CHARACTERISTICS

(VCC = 5V ± 10%, TA =-55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
|ILI|	Input Leakage Current (Address, $\overline{OE}$)	VCC = Max., VIN = GND to VCC	—	40	µA
|ILI|	Input Leakage (Data, $\overline{WE}$, $\overline{CS}$)	VCC = Max., VIN = GND to VCC	—	10	µA
|ILO|	Output Leakage	VCC = Max. $\overline{CS}$ = VIH, VOUT = GND to VCC	—	10	µA
VOL	Output Low Voltage	VCC = Min., IOL = 6mA	—	0.45	V
VOH	Output High Voltage	VCC = Min., IOH = –4mA	2.4	—	V
ICC	Dynamic Operating Current	f = 5 MHz, IOUT = 0 mA VCC = Max.	—	320	mA
ISB	Standby Supply Current (TTL)	$\overline{CS}$ ≥ 2V to VCC + 1V	—	12	mA

Tbl 07

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

Tbl 08

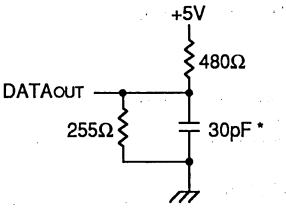


Figure 1. Output Load

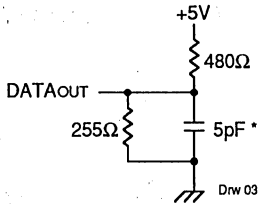


Figure 2. Output Load (for tCHZ)

* Including scope and jig

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C or 0°C to +70°C)

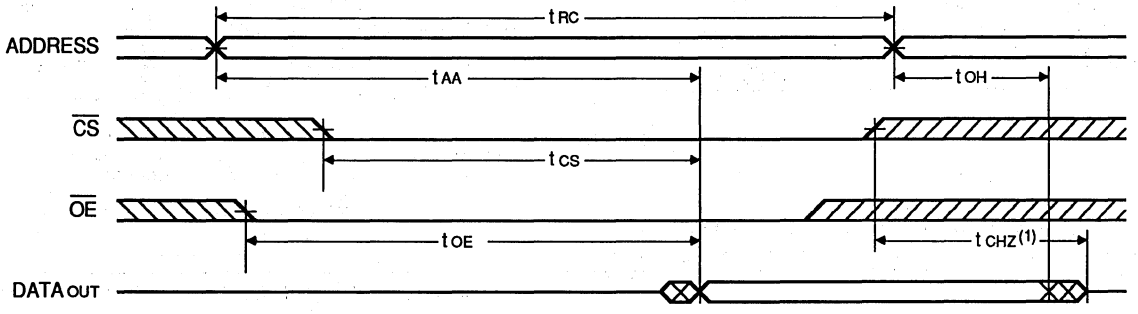
Symbol	Parameters	7M7004SxxCH or 7M7004SxxCHB										Unit
		-75		-95		-125		-150		-200		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
tRC	Read Cycle Time	75	—	95	—	125	—	150	—	200	—	ns
tAA	Address Access Time	—	75	—	95	—	125	—	150	—	200	ns
tACS	Chip Select Access Time	—	75	—	95	—	125	—	150	—	200	ns
tOE	Output Enable to Output Valid	—	40	—	50	—	55	—	70	—	80	ns
tCHZ (1)	Chip Select to Output in High Z	0	40	0	50	0	55	0	55	0	60	ns
tOH	Output Hold from Address Change	0	—	0	—	0	—	0	—	0	—	ns
WRITE CYCLE												
tWC	Write Cycle Time	0.4	10	0.4	10	0.4	10	0.4	10	0.4	10	ms
tAH	Address Hold Time	50	—	50	—	50	—	50	—	50	—	ns
tAS	Address Setup Time	2	—	2	—	2	—	2	—	2	—	ns
tWP	Write Pulse Width	105	—	105	—	105	—	105	—	105	—	ns
tCS	$\overline{CS}$ Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tCH	$\overline{CS}$ Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tDS	Data Set-up Time	55	—	55	—	55	—	55	—	55	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
PAGE MODE WRITE CYCLE												
tWC	Write Cycle Time	0.4	10	0.4	10	0.4	10	0.4	10	0.4	10	ms
tAH	Address Hold Time	50	—	50	—	50	—	50	—	50	—	ns
tAS	Address Setup Time	2	—	2	—	2	—	2	—	2	—	ns
tDS	Data Set-up Time	55	—	55	—	55	—	55	—	55	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	105	—	105	—	105	—	105	—	105	—	ns
tBLC	Byte Load Cycle Time	0.2	200	0.2	200	0.2	200	0.2	200	0.2	200	µs
tWPH	Write Pulse Width High	55	—	55	—	55	—	55	—	55	—	ns
DATA POLLING CYCLE												
tDH (1)	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ms
tOEH (1)	Output Enable Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tOE (1)	Output Enable to Output Delay	—	100	—	100	—	100	—	100	—	100	ns
tWR (1)	Write Recovery Time	2	—	2	—	2	—	2	—	2	—	ns

Tbl 09

NOTE:
1. This parameter is guaranteed by design but not tested.

B

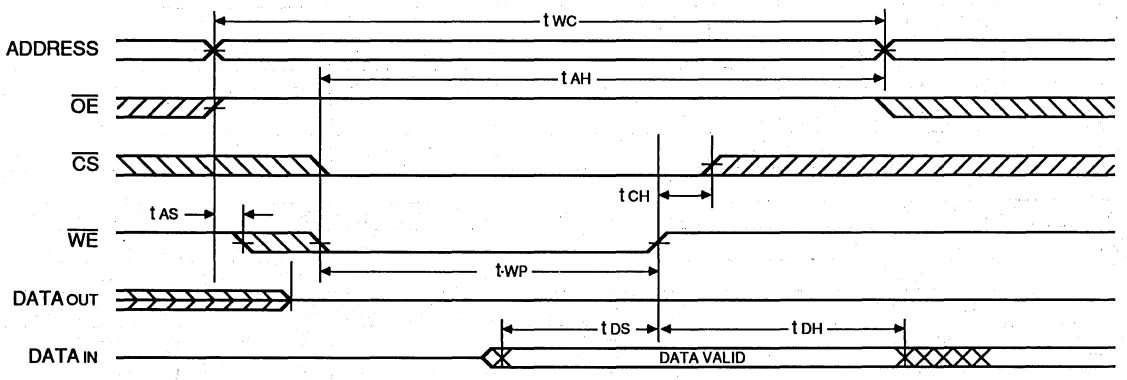
TIMING WAVEFORM OF READ CYCLE[1]



NOTES:
1. This parameter is guaranteed by design but not tested.

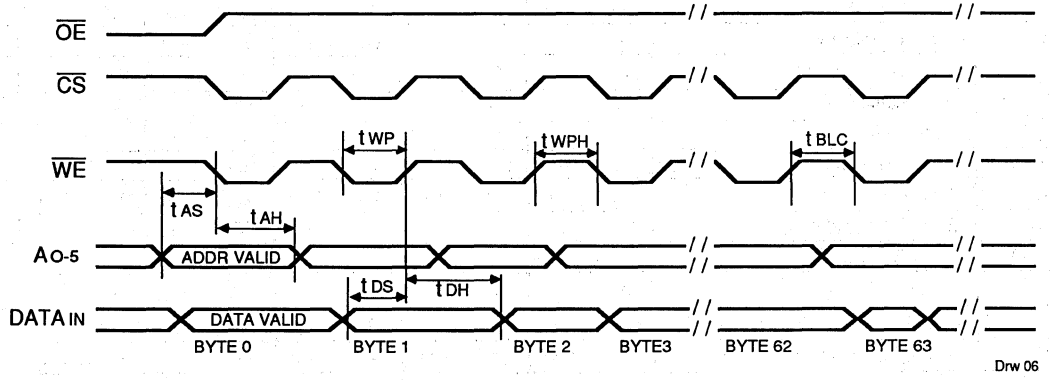
Drw 04

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)



Drw 05

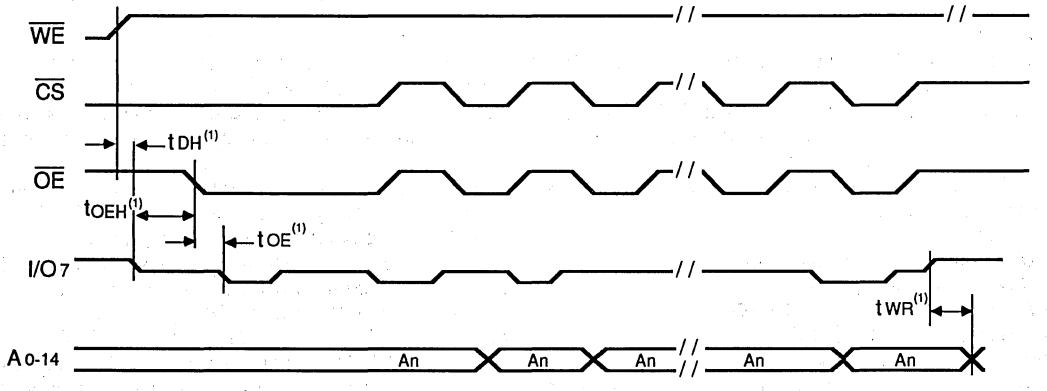
TIMING WAVEFORM OF PAGE MODE WRITE CYCLE [1]



Drw 06

NOTES:
1. A6 through A14 must specify the page address during each High to Low transitions of $\overline{WE}$ (or $\overline{CS}$). $\overline{OE}$ must be High only when $\overline{WE}$ and $\overline{CS}$ are both Low.

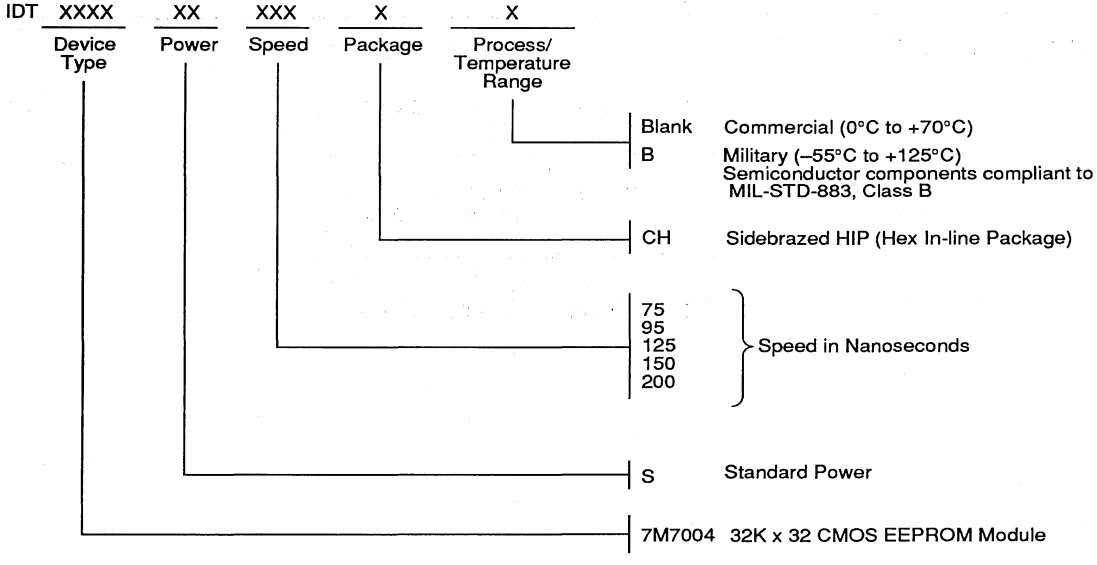
TIMING WAVEFORM OF $\overline{DATA}$ POLLING CYCLE



Drw 07

NOTES:
1. This parameter is guaranteed by design but not tested.
2. A6 through A14 must specify the page address during each High to Low transitions of $\overline{WE}$ (or $\overline{CS}$). $\overline{OE}$ must be High only when $\overline{WE}$ and $\overline{CS}$ are both Low.

ORDERING INFORMATION



2825 drw 08

B

Integrated Device Technology, Inc.

SUBSYSTEMS "FLEXI-PAK™" FAMILY

32K x 16/32K x 16 CMOS SRAM/EEPROM MODULE

PRELIMINARY
IDT7M7005

FEATURES:

- High-density CMOS module with SRAM and EEPROM memory on-board
- Member of the Subsystems "Flexi-Pak" Family of interchangeable modules, with equivalent pin-outs, supporting a wide range of applications.
- Footprint compatible module upgrades to the next higher density with relative ease
- Fast access times:
  - — 25ns (max.) commercial SRAM
  - — 30ns (max.) military SRAM
  - — 75ns (max.) commercial EEPROM
  - — 95ns (max.) military EEPROM
- Low power CMOS operation
- Surface mounted LCC components mounted on a co-fired ceramic substrate
- Offered in a 66-pin HIP (Hex In-line Package), occupying only 1 sq. inch of board space
- Single 5V (±10%) power supply
- Multiple ground pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Please consult the factory regarding the number of Erase/ Write Cycles per Byte Minimum available on the module

DESCRIPTION:

The IDT7M7005 is a high-speed, high-density CMOS module with both SRAM & EEPROM memory on-board. It is constructed on a multi-layer, co-fired ceramic substrate using 32K x 8 SRAM or EEPROM components in leadlesss chip carriers.

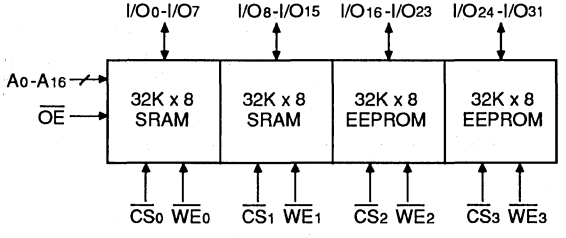
These modules are part of the IDT Subsystems "Flexi-Pak" Family. This family of SRAM/EEPROM/EPROM memory modules support applications requiring stand alone static or programmmable memory or those applications needing a combination of both. All of these module configurations have equivalent pin-outs, making them "plug-in compatible" with each other, suitable for a wide range of applications.

The IDT7M7005 is available with SRAM access times as fast as 25ns over the commercial temperature range and 30ns over the military temperature range and EEPROM access times as fast as 75ns over the commercial temperature range and 95ns over the military temperature range.

These modules are offered in a 66-pin, ceramic HIP (Hex In-line Package). This HIP package is similar to a PGA and fits the SRAM/EEPROM memory into 1 sq. inch of board space.

All military IDT military modules are assembled with semiconductor components compliant with the latest revision of MIL-STD-883 Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

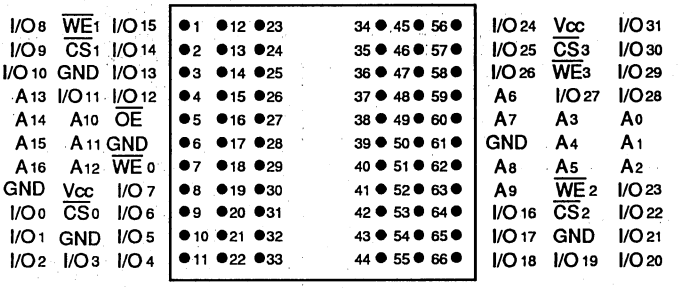
FUNCTIONAL BLOCK DIAGRAM



2826 drw 01

Flexi-Pak is a Trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS [1, 2]



2826 drw 02

HIP
TOP VIEW

NOTES:
1. For module dimensions, please refer to the module drawings in the packaging section.
2. For the IDT7M7005 (32K x 16/32K x 16) version, pins 6 and 7 are no connects.

PIN NAMES

Name	Description
I/O 0-31	Data Inputs/Outputs
A 0-16	Address Inputs
$\overline{WE}$ 0-1	RAM Write Enables
$\overline{WE}$ 2-3	EEPROM Write Enables
$\overline{CS}$ 0-1	RAM Chip Selects
$\overline{CS}$ 2-3	EEPROM Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground

2826 tbl 01

RECOMMENDED OPERATING TEMPERATURE AND VOLTAGE SUPPLY

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%
Military	-55°C to +125°C	0V	5.0V ± 10%

2826 tbl 06

TRUTH TABLE [1]

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	DOUT	Active
Write	L	note 1	L	DIN	Active
Read	L	H	H	High Z	Active

2826 tbl 02

NOTE:
1. For the SRAM array $\overline{OE}$ = X (don't care); however, for the EEPROM array $\overline{OE}$ = H (high).

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN (1)	Input Capacitance (Data, $\overline{CS}$, $\overline{WE}$)	VIN = 0V	12	pF
CIN (2)	Input Capacitance (Address, $\overline{OE}$)	VIN = 0V	50	pF
COUT	Output Capacitance	VOUT = 0V	15	pF

2826 tbl 03

NOTE:
1. This parameter is guaranteed by design but not tested.

B

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

2826 tbl 05

NOTE:
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns.

ABSOLUTE MAXIMUM RATINGS [1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2826 tbl 04

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS (EEPROM)

(V_{CC} = 5V ± 10%, T_A =-55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current (Address, $\overline{OE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	20	µA
$\|I_{LI}\|$	Input Leakage (Data, $\overline{CS}$, $\overline{WE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
I_{CC}	Dynamic Operating Current	f = 5 MHz, I_{OUT} = 0 mA V_{CC} = Max.	—	160	mA
I_{SB}	Standby Supply Current (TTL)	$\overline{CS}$ ≥ 2V to V_{CC} + 1V	—	6	mA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 6mA	—	0.45	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V

2826 tbl 07

DC ELECTRICAL CHARACTERISTICS (SRAM)

Symbol	Parameter	Test Conditions	Min.	Max.[1]	Max.[2]	Unit
$\|I_{LI}\|$	Input Leakage Current (Address, $\overline{OE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	10	µA
$\|I_{LI}\|$	Input Leakage Current (Data, $\overline{CS}$, $\overline{WE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	20	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	10	µA
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ ≤ V_{IL} f = f_{MAX}, Output Open	—	400	440	mA
I_{SB}	Standby Supply Curent	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH} f = f_{MAX}, Output Open	—	40	140	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} -0.2V V_{IN} > V_{CC} -0.2V or < 0.2V	—	40	40	mA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	—	—	V

NOTES:
1. For T_A = 0°C to +70°C versions only.
2. For T_A = -55°C to +125°C versions only.

2826 tbl 06

AC TEST CONDITIONS (EEPROM)

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2826 tbl 08

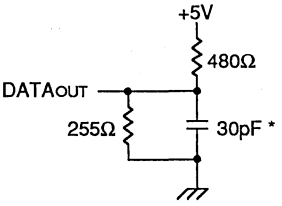
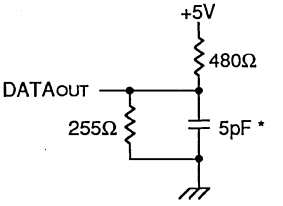


Figure 1. Output Load



2826 drw 03

Figure 2. Output Load (for tCHZ)

* Including scope and jig

AC ELECTRICAL CHARACTERISTICS (EEPROM)

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C or 0°C to +70°C)

Symbol	Parameters	7M7005Sxx/xxCH 7M7005Sxx/xxCHB -75 Min.	-75 Max.	-95 Min.	-95 Max.	-125 Min.	-125 Max.	-150 Min.	-150 Max.	-200 Min.	-200 Max.	Unit
READ CYCLE												
tRC	Read Cycle Time	75	—	95	—	125	—	150	—	200	—	ns
tAA	Address Access Time	—	75	—	95	—	125	—	150	—	200	ns
tACS	Chip Select Access Time	—	75	—	95	—	125	—	150	—	200	ns
tOE	Output Enable to Output Valid	—	40	—	50	—	55	—	70	—	80	ns
tCHZ (1)	Chip Select to Output in High Z	0	40	0	50	0	55	0	55	0	60	ns
tOH	Output Hold from Address Change	0	—	0	—	0	—	0	—	0	—	ns
WRITE CYCLE												
tWC	Write Cycle Time	0.4	10	0.4	10	0.4	10	0.4	10	0.4	10	ms
tAH	Address Hold Time	50	—	50	—	50	—	50	—	50	—	ns
tAS	Address Setup Time	2	—	2	—	2	—	2	—	2	—	ns
tWP	Write Pulse Width	105	—	105	—	105	—	105	—	105	—	ns
tCS	$\overline{CS}$ Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tCH	$\overline{CS}$ Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tDS	Data Set-up Time	55	—	55	—	55	—	55	—	55	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
PAGE MODE WRITE CYCLE												
tWC	Write Cycle Time	0.4	10	0.4	10	0.4	10	0.4	10	0.4	10	ms
tAH	Address Hold Time	50	—	50	—	50	—	50	—	50	—	ns
tAS	Address Setup Time	2	—	2	—	2	—	2	—	2	—	ns
tDS	Data Set-up Time	55	—	55	—	55	—	55	—	55	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	105	—	105	—	105	—	105	—	105	—	ns
tBLC	Byte Load Cycle Time	0.2	200	0.2	200	0.2	200	0.2	200	0.2	200	µs
tWPH	Write Pulse Width High	55	—	55	—	55	—	55	—	55	—	ns
DATA POLLING CYCLE												
tDH (1)	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ms
tOEH (1)	Output Enable Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tOE (1)	Output Enable to Output Delay	—	100	—	100	—	100	—	100	—	100	ns
tWR (1)	Write Recovery Time	2	—	2	—	2	—	2	—	2	—	ns

2826 tbl 09

NOTE:
1. This parameter is guaranteed by design but not tested.

B

AC TEST CONDITIONS (SRAM)

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2826 tbl 08

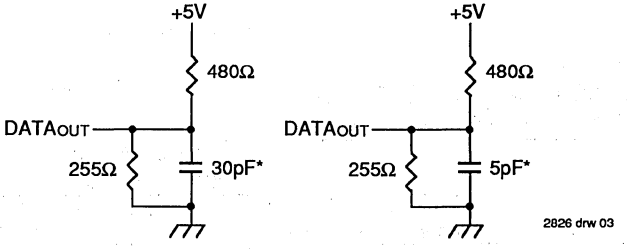


Figure 1. Output Load

Figure 2. Output Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig

AC ELECTRICAL CHARACTERISTICS (SRAM)

(V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameters	7M7005Sxx/xxCH 7M7005Sxx/xxCHB										Unit
		-25		-30		-35		-40		-45		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	—	40	—	45	ns
t_{ACS}	Chip Select Access Time	—	25	—	30	—	35	—	40	—	45	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	12	—	13	—	15	—	20	—	25	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	2	—	2	—	2	—	5	—	5	—	ns
t_{CHZ}(1)	Chip Select to Output in High Z	—	12	—	15	—	17	—	20	—	20	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	12	—	13	—	15	—	20	—	20	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	5	—	5	—	5	—	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_{CW}	Chip Select to End of Write	20	—	25	—	30	—	35	—	40	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	30	—	35	—	40	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	2	—	2	—	ns
t_{WP}	Write Pulse Width	20	—	23	—	25	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}(1)	Write Enable to Ouput in High Z	—	12	—	13	—	17	—	20	—	20	ns
t_{DW}	Data to Write Time Overlap	13	—	15	—	16	—	16	—	20	—	ns
t_{DH}	Data Hold from Write Time	3	—	3	—	3	—	3	—	5	—	ns
t_{OW}(1)	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

2826 tbl 08

AC ELECTRICAL CHARACTERISTICS (SRAM CONTINUED)

(V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameters	7M7005Sxx/xxCH 7M7005Sxx/xxCHB										Unit
		-50		-60		-70		-85		-100		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	50	—	60	—	70	—	85	—	100	—	ns
t_{AA}	Address Access Time	—	50	—	60	—	70	—	85	—	100	ns
t_{ACS}	Chip Select Access Time	—	50	—	60	—	70	—	85	—	100	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	30	—	30	—	35	—	40	—	45	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Select to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	50	—	60	—	70	—	85	—	100	—	ns
t_{CW}	Chip Select to End of Write	45	—	55	—	65	—	80	—	90	—	ns
t_{AW}	Address Valid to End of Write	45	—	55	—	65	—	80	—	90	—	ns
t_{AS}	Address Set-up Time	2	—	2	—	5	—	5	—	5	—	ns
t_{WP}	Write Pulse Width	40	—	45	—	45	—	50	—	55	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Ouput in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{DW}	Data to Write Time Overlap	25	—	30	—	30	—	35	—	40	—	ns
t_{DH}	Data Hold from Write Time	5	—	5	—	5	—	5	—	5	—	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

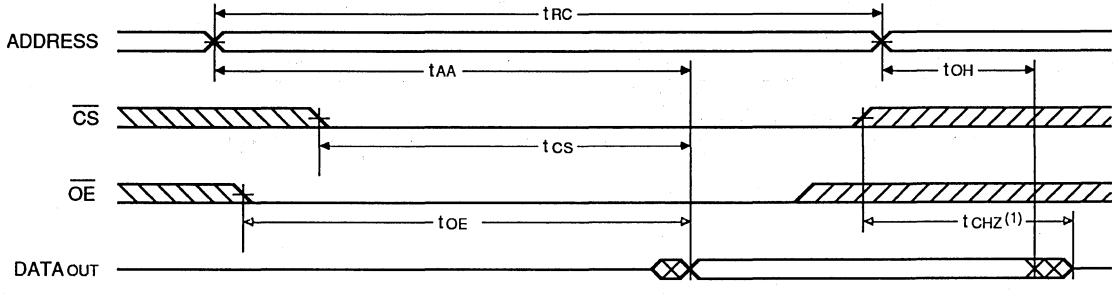
NOTE:
1. This parameter is guaranteed by design, but not tested.

2826 tbl 09

B

EEPROM TIMING WAVEFORMS

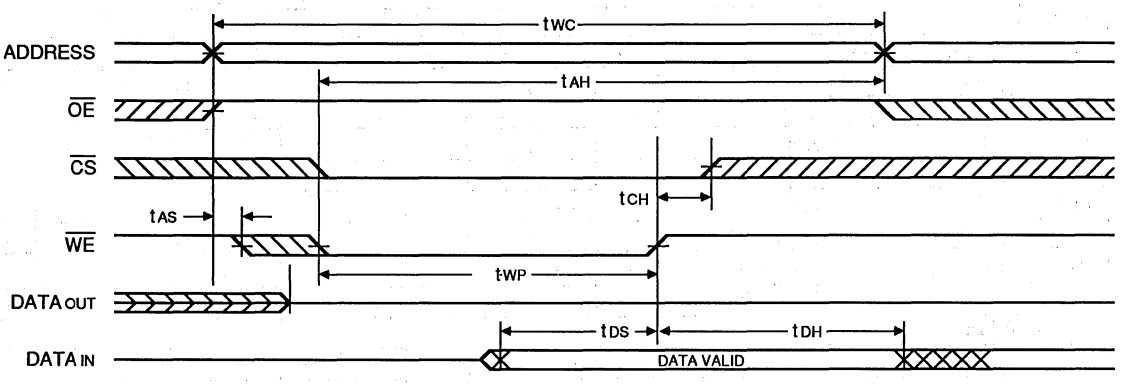
TIMING WAVEFORM OF READ CYCLE[1]



2826 drw 04

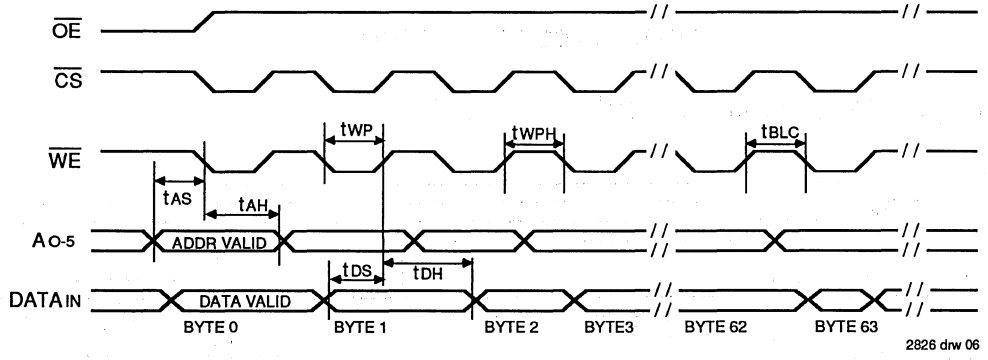
NOTES:
1. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)



2826 drw 05

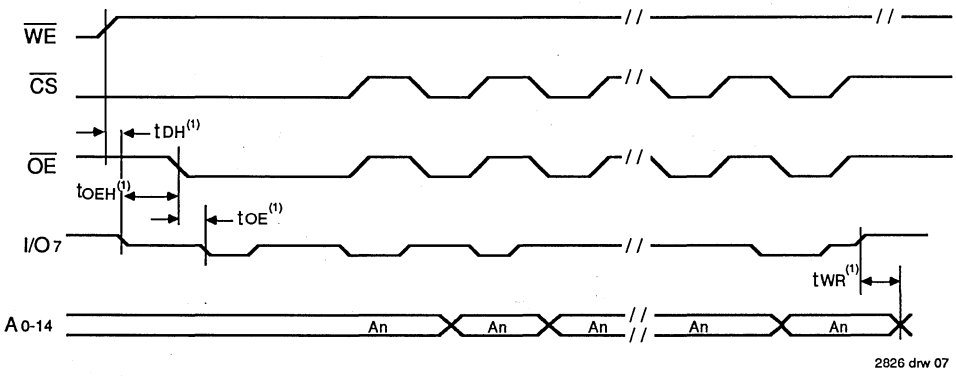
TIMING WAVEFORM OF PAGE MODE WRITE CYCLE (1)



2826 drw 06

NOTES:
1. A6 through A14 must specify the page address during each High to Low transitions of $\overline{WE}$ (or $\overline{CS}$). $\overline{OE}$ must be High only when $\overline{WE}$ and $\overline{CS}$ are both Low.

TIMING WAVEFORM OF $\overline{DATA}$ POLLING CYCLE

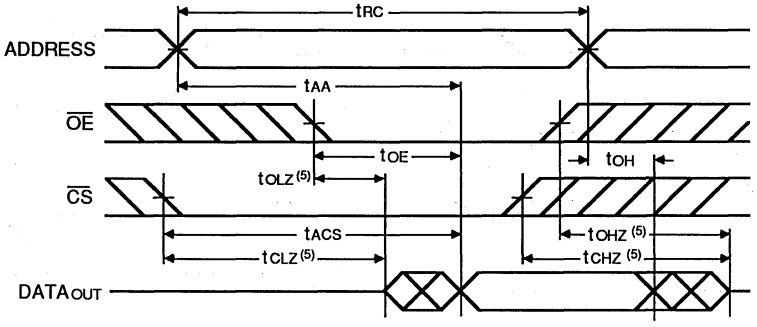


NOTES:
1. This parameter is guaranteed by design but not tested.
2. A6 through A14 must specify the page address during each High to Low transitions of $\overline{WE}$ (or $\overline{CS}$). $\overline{OE}$ must be High only when $\overline{WE}$ and $\overline{CS}$ are both Low.

B

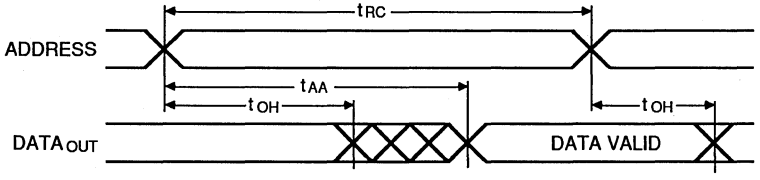
SRAM TIMING WAVEFORMS

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



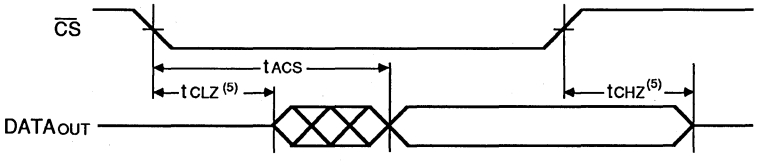
2826 drw 04

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2826 drw 05

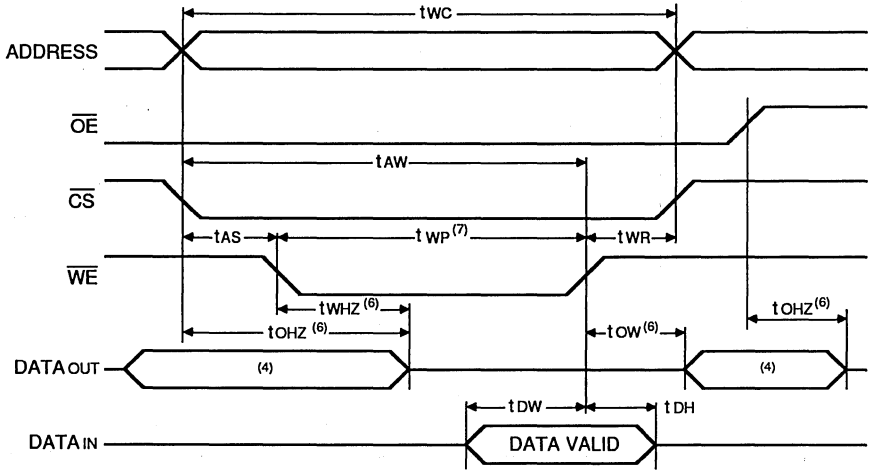
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



2826 drw 06

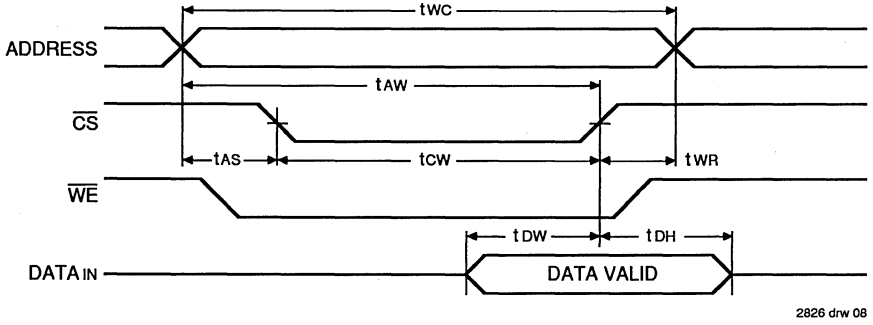
NOTES:
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1, 2, 3, 7)



2826 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1, 2, 3, 5)

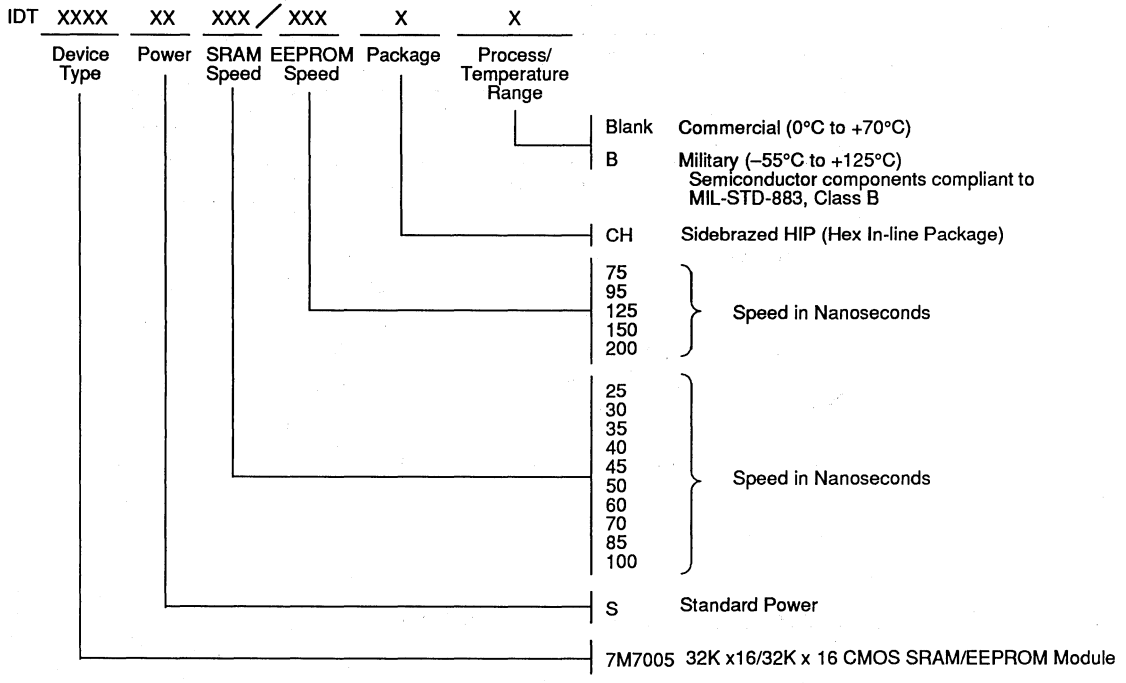


2826 drw 08

B

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going High to the end of write cycle.
4. During this period, I/O pins are in the output state, input signals must not be applied.
5. If the $\overline{CS}$ Low transition occurs simultaneously with or after the $\overline{WE}$ Low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse (tWP > tWHZ + tDW) to allow the I/O drivers to turn off data and to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP .

ORDERING INFORMATION



2826 drw 08

Integrated Device Technology, Inc.

64K x 16 BiCMOS STATIC RAM MODULE

PRELIMINARY
IDT7MB4064

FEATURES:

- High density 1 megabit BiCMOS static RAM module
- Low profile 40-pin DIP (Dual In-line Package)
- Ultra fast access time: 10ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible
- Multiple GND pins for maximum noise immunity

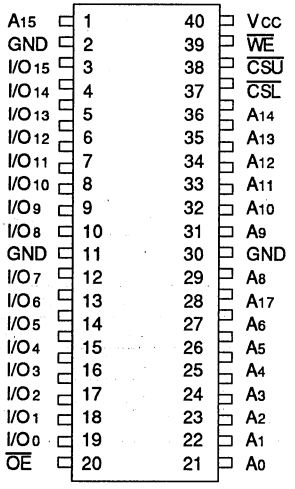
DESCRIPTION:

The IDT7MB4064 is a 64K x 16 BiCMOS static RAM module constructed on an epoxy laminate (FR-4) substrate using 4 64K x 4 static RAMs in plastic SOJ packages. Availability of two chip select lines (one for each group of two RAMs) provides byte access. Extremely fast speeds can be achieved due to the use of 256K static RAMs fabricated in IDT's high performance, high reliability BiCEMOS™ technology. The IDT7MB4064 is available with access time as fast as 10ns with minimal power consumption.

The IDT7MB4064 is packaged in a 40 pin FR-4 DIP (Dual In-line Package). The DIP configuration allows 40 pins to be placed on a package 2.0 inches long and 0.60 inches wide and 0.36 inches tall.

All inputs and outputs of the IDT7MB4064 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

PIN CONFIGURATION[1]

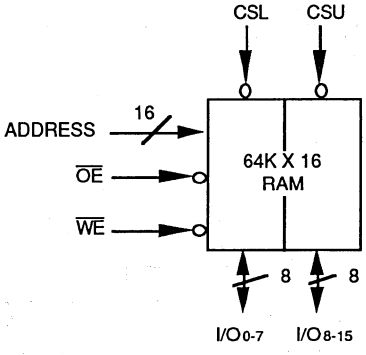


DIP TOP VIEW

2827 drw 02

NOTE:
1. For module dimensions, please refer to the module drawings in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



2827 drw 01

PIN NAMES

I/O0–15	Data Inputs/Outputs
A0–15	Addresses
$\overline{CSL}$, $\overline{CSU}$	Chip Selects Lower, Upper
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
VCC	Power
GND	Ground

2827 tbl 01

B

BiCEMOS is trademark of Integrated Device Technology, Inc.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 2827 tbl 05

1. V_{IL} (min) = –1.5V for pulse width less than 10ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commerical	0°C to +70°C	0V	5.0V ± 10%

2827 tbl 06

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	$V_{(IN)}$ = 0V	10	pF
$C_{IN(A)}$	Input Capacitance (Address & Control)	$V_{(IN)}$ = 0V	40	pF
C_{OUT}	Output Capacitance	$V_{(OUT)}$ = 0V	14	pF

NOTE: 2827 tbl 04

1. This parameter is guaranteed by design but not tested.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Read	L	L	H	$DATA_{OUT}$	Active
Write	L	X	L	$DATA_{IN}$	Active
Read	L	H	H	High-Z	Active

2827 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2827 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

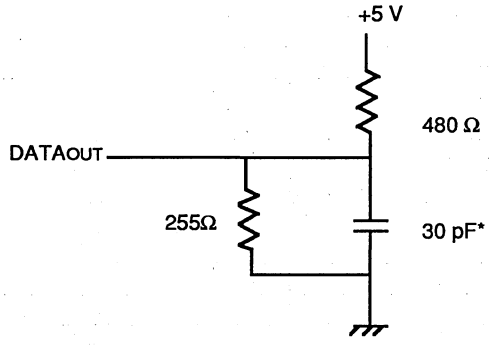
Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	40	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max.; $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V
I_{CC}	Operating Current	V_{CC} = Max,CS ≤ V_{IL}; f = f_{MAX}, Outputs Open	—	720	mA

2827 tbl 07

AC TEST CONDITIONS

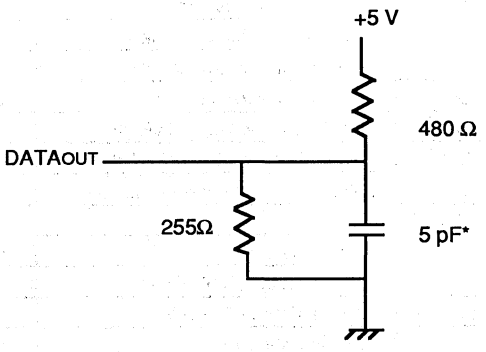
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1-4

2827 tbl 08



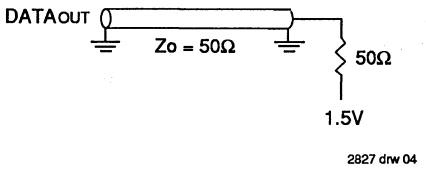
* includes scope and jig.

Figure 1. Output Load



2827 drw 03

Figure 2. Output Load
(for tOLZ, tOHZ, tCHZ, tCLZ, tWHZ, tOW)



2827 drw 04

Figure 3. BICMOS Output Load

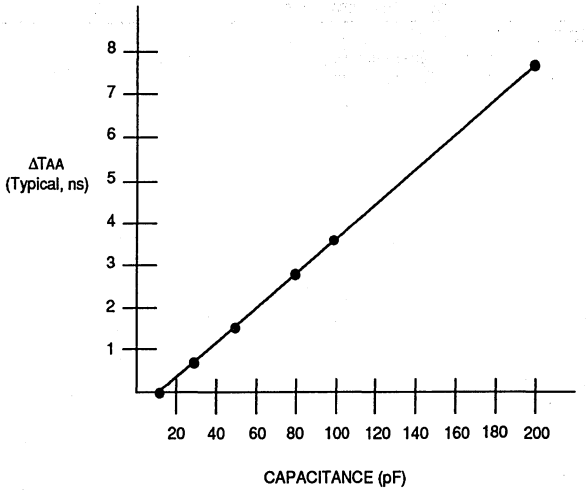


Figure 4. Lumped Capacitive Load, Typical Derating

B

AC ELECTRICAL CHARACTERISTICS

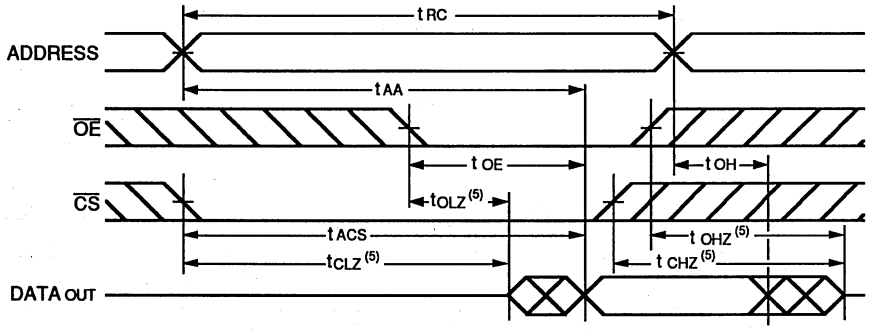
(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

		7MB4064BxxP								
		-10[2]		-12[2]		-15		-17		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	10	—	12	—	15	—	17	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	—	17	ns
t_{ACS}	Chip Select Access Time	—	4	—	5	—	6	—	7	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	2	—	2	—	2	—	2	—	ns
t_{OE}	Output Enable to Output Valid	—	4	—	5	—	6	—	7	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	2	—	2	—	2	—	2	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	6	—	7	—	8	—	9	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	3	—	4	—	5	—	6	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
Write Cycle										
t_{WC}	Write Cycle Time	10	—	12	—	15	—	17	—	ns
t_{CW}	Chip Select to End of Write	7	—	8	—	9	—	10	—	ns
t_{AW}	Address Valid to End of Write	8	—	9	—	10	—	11	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	9	—	10	—	11	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	4	—	5	—	6	—	7	ns
t_{DW}	Data to Write Time Overlap	4	—	5	—	6	—	8	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	2	—	2	—	2	—	2	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

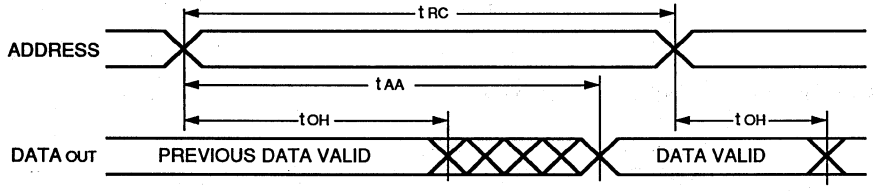
2827 tbl 09

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



2827 drw 05

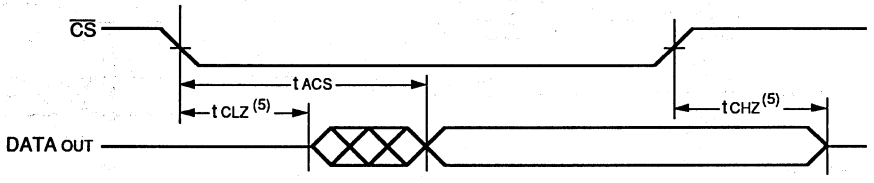
TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



2827 drw 06

B

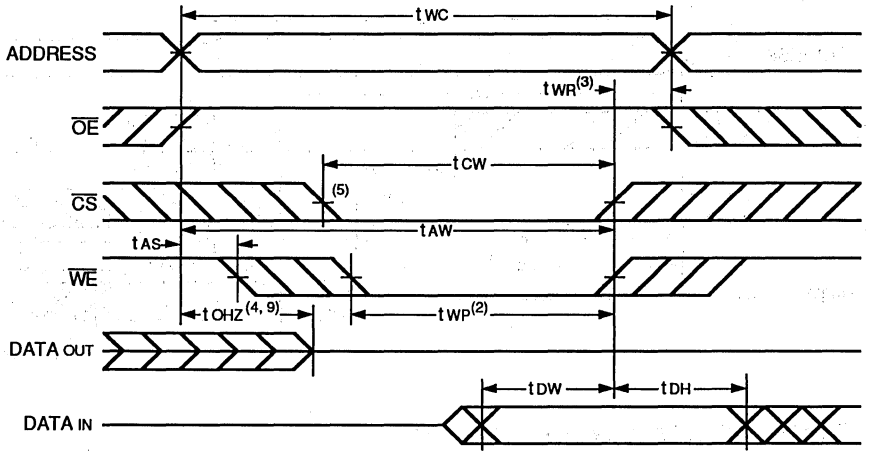
TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)



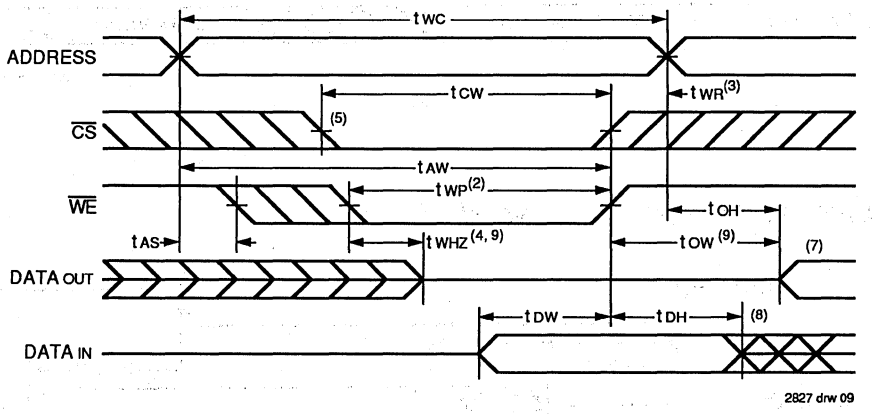
2827 drw 07

NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1)

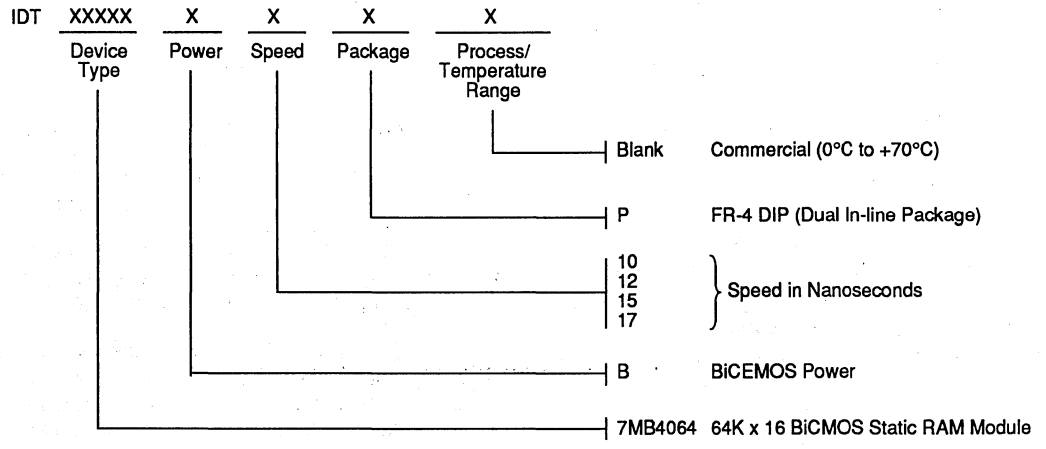


TIMING WAVEFORM OF WRITE CYCLE NO. 2(1,6)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$.
3. tWP is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = VIL).
7. DOUT is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

ORDERING INFORMATION



2827 drw 11

B

Integrated Device Technology, Inc.

256K x 20 BiCMOS/CMOS STATIC RAM MODULE

PRELIMINARY
IDT7MB4065

FEATURES:

- High density 256K x 20 BiCMOS/CMOS static RAM module
- Low profile 48-pin FR-4 DIP (Dual In-line Package)
- Fast access time: 12ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible
- Multiple GND pins for maximum noise immunity

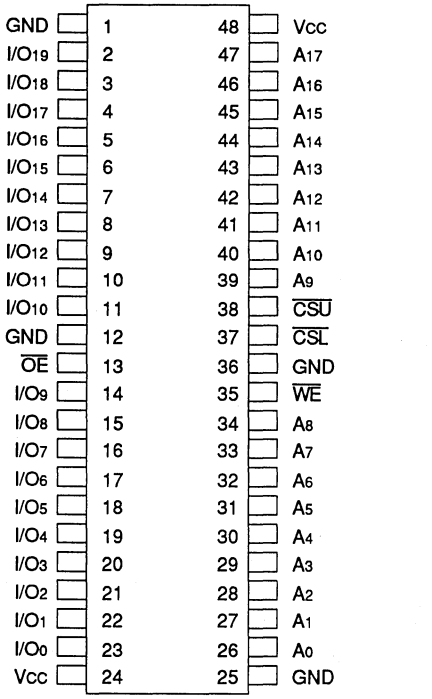
DESCRIPTION:

The IDT7MB4065 is a 256K x 20 BiCMOS/CMOS static RAM module constructed on an epoxy laminate (FR-4) substrate using 5 256K x 4 static RAMs in plastic SOJ packages. The IDT7MB4065 is available with access time as fast as 12ns with minimal power consumption.

The IDT7MB4065 is packaged in a 48 pin FR-4 DIP (Dual In-line Package). The dual row configuration allows 48 pins to be placed on a package 2.4 inches long, 600 mils wide and 0.35 inches tall.

All inputs and outputs of the IDT7MB4065 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

PIN CONFIGURATION[1]

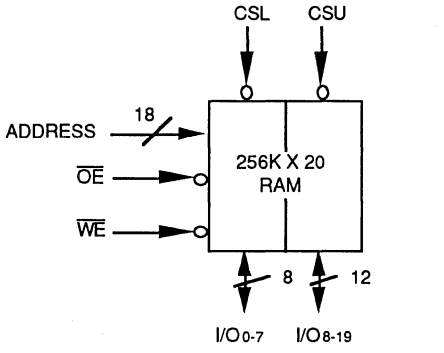


2828 drw 01

DIP
TOP VIEW

NOTE:
1. For module packaging dimensions, please refer to the module drawings in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



2828 drw 02

PIN NAMES

I/O0-19	Data Inputs/Outputs
A0-17	Address
$\overline{CSL}$	Chip Selects - Lower Byte
$\overline{CSU}$	Chip Selects - Upper Byte
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power
GND	Ground

2828 tbl 01

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Comm.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

2828 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	Hi-Z	Standby
Read	L	L	H	Dout	Active
Write	L	X	L	Din	Active
Read	L	H	H	Hi-Z	Active

2828 tbl 08

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6	V
V_{IL}	Input Low Voltage	-0.5 (1)	—	0.8	V

2828 tbl 03

NOTE:
1. V_{IL} = -2.0V for pulse width less than 10ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2828 tbl 04

CAPACITANCE

(T_A = +25°C, F = 1.0MHz)

Symbol	Parameter (1)	Conditions	Max.	Unit
$C_{IN(D)}$	Input Capacitance	V_{IN} = 0V	12	pF
$C_{IN(A)}$	Input Capacitance (Address and Control)	V_{IN} = 0V	42	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
1. This parameter is guaranteed by design but not tested.

2828 tbl 09

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	50	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max.; CS = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V

Symbol	Parameter	Test Conditions	7MB4065B(1) Max.	7MB4065S Max.	Unit
I_{CC}	Dymanic Operating Current	f = f_{MAX}(2); CS = V_{IL} V_{CC} = Max.; Output Open	1000	750	mA
I_{SB}	Standby Supply Current	CS ≥ V_{IH}, V_{CC} = Max. Outputs Open, f = f_{MAX}(2)	—	300	mA
I_{SB1}	Full Standby Supply Current	CS ≥ V_{CC} – 0.2V; F = 0 V_{IN} > V_{CC} – 0.2V or < 0.2V	—	10	mA

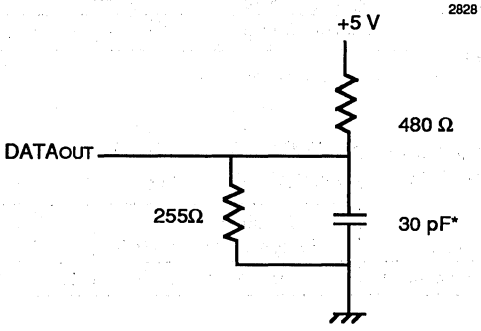
2828 tbl 09

NOTES:
1. Preliminary specifications only.
2. f_{MAX} = 1/t_{RC}

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1-4

2828 tbl 06



* includes scope and jig.

Figure 1. Output Load

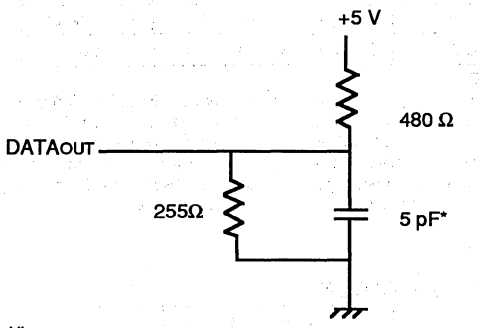


Figure 2. Output Load
(for tOLZ, tOHZ, tCHZ, tCLZ, tWHZ, tOW)

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

		7MB4065BxxP						
		-12(2)		-15(2)		-17(2)		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle								
tRC	Read Cycle Time	12	—	15	—	17	—	ns
tAA	Address Access Time	—	12	—	15	—	17	ns
tACS	Chip Select Access Time	—	7	—	8	—	9	ns
tCLZ(1)	Chip Select to Output in Low Z	2	—	2	—	2	—	ns
tOE	Output Enable to Output Valid	—	5	—	6	—	8	ns
tOLZ(1)	Output Enable to Output in Low Z	2	—	2	—	2	—	ns
tCHZ(1)	Chip Deselect to Output in High Z	—	7	—	8	—	10	ns
tOHZ(1)	Output Disable to Output in High Z	—	4	—	5	—	6	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	ns
Write Cycle								
tWC	Write Cycle Time	12	—	15	—	17	—	ns
tCW	Chip Select to End of Write	8	—	9	—	10	—	ns
tAW	Address Valid to End of Write	9	—	10	—	12	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width	9	—	10	—	12	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tWHZ(1)	Write Enable to Output in High Z	—	5	—	6	—	7	ns
tDW	Data to Write Time Overlap	5	—	6	—	8	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	ns
tOW(1)	Output Active from End of Write	2	—	2	—	2	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

2828 tbl 09

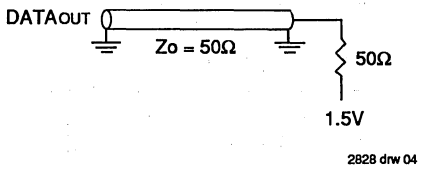


Figure 3. BICMOS Output Load

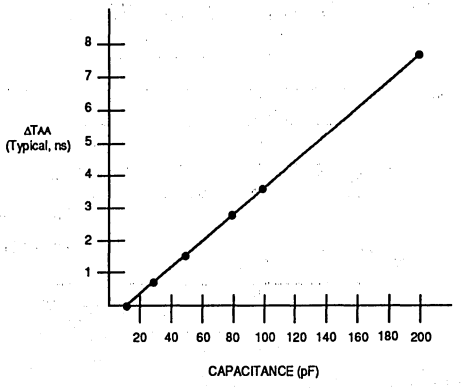


Figure 4. BiCMOS Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V ± 10%, TA = 0°C to +70°C)

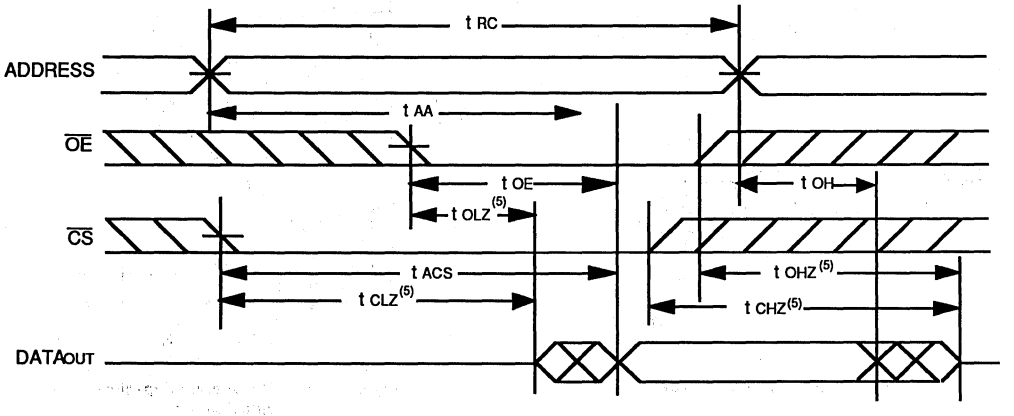
Symbol	Parameters	7MB4065SxxP										
		-20[2]		-25		-30		-35		-45		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
tAA	Address Access Time	—	20	—	25	—	30	—	35	—	45	ns
tACS	Chip Select Access Time	—	20	—	25	—	30	—	35	—	45	ns
tCLZ[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	10	—	12	—	15	—	18	—	23	ns
tOLZ[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	0	—	ns
tCHZ[1]	Chip Deselect to Output in High Z	—	10	—	12	—	15	—	18	—	20	ns
tOHZ[1]	Output Disable to Output in High Z	—	10	—	10	—	10	—	10	—	10	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	5	—	5	—	ns
tPU[1]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
tPD[1]	Chip Deselect to Power Down Time	—	20	—	25	—	30	—	35	—	45	ns
Write Cycle												
tWC	Write Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
tCW	Chip Selection to End of Write	15	—	20	—	25	—	30	—	40	—	ns
tAW	Address Valid to End of Write	15	—	20	—	25	—	30	—	40	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	15	—	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tWHZ[1]	Write Enable to Output in High Z	—	13	—	15	—	18	—	20	—	23	ns
tDW	Data to Write Time Overlap	12	—	15	—	17	—	20	—	25	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	ns
tOW[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns

2828 tbl 07

NOTES:
1. This parameter is guaranteed by design but not tested.
2. Preliminary specifications only.

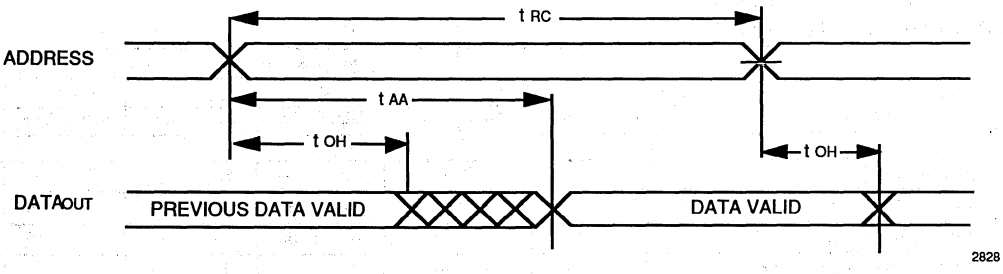
B

TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



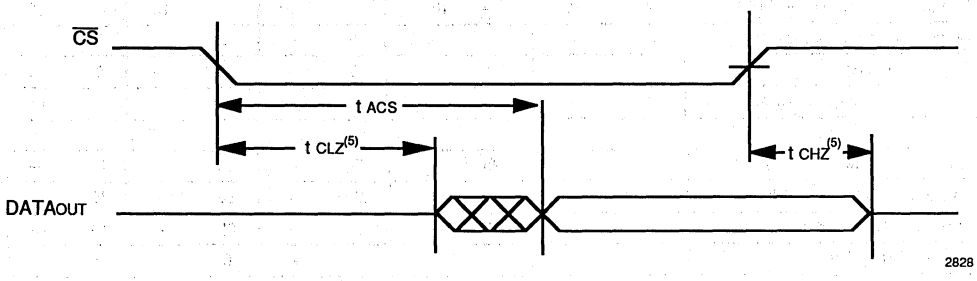
2828 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 2 (1,2,4)



2828 drw 06

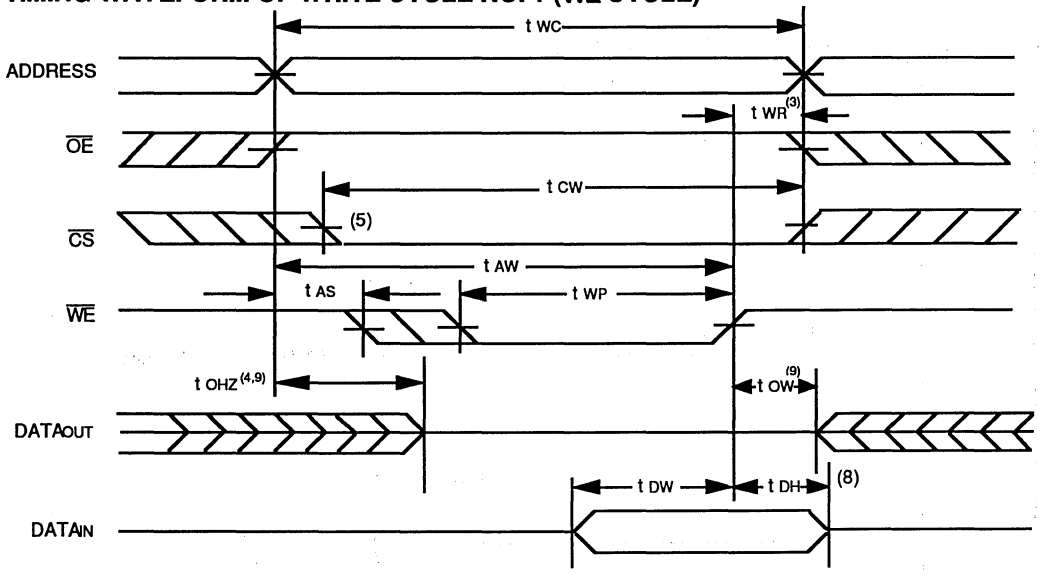
TIMING WAVEFORM OF READ CYCLE NO. 2 (1,3,4)



2828 drw 07

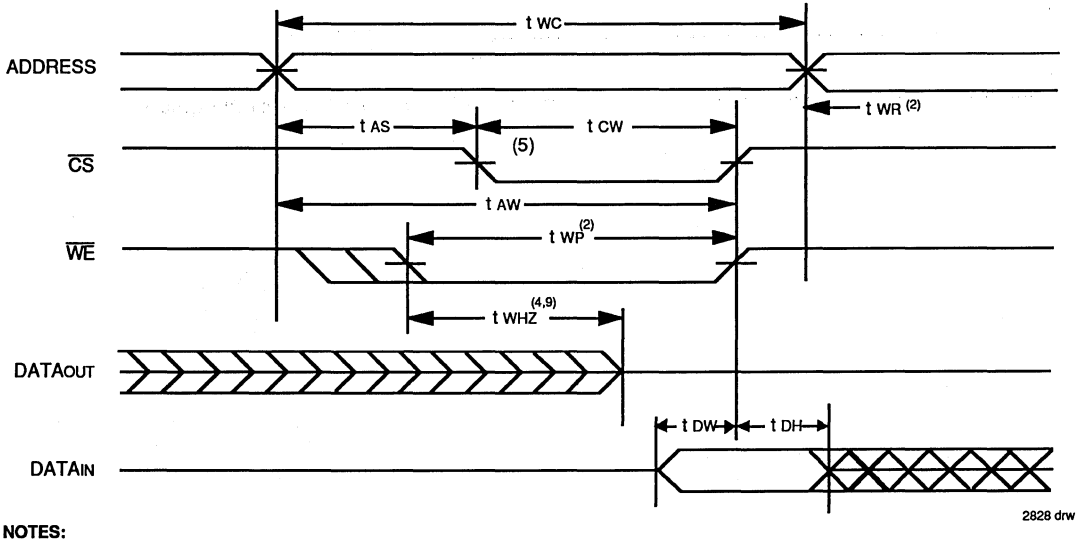
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = V_{IL}.
3. Address valid prior to $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200 mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CYCLE)(1)



2828 drw 08

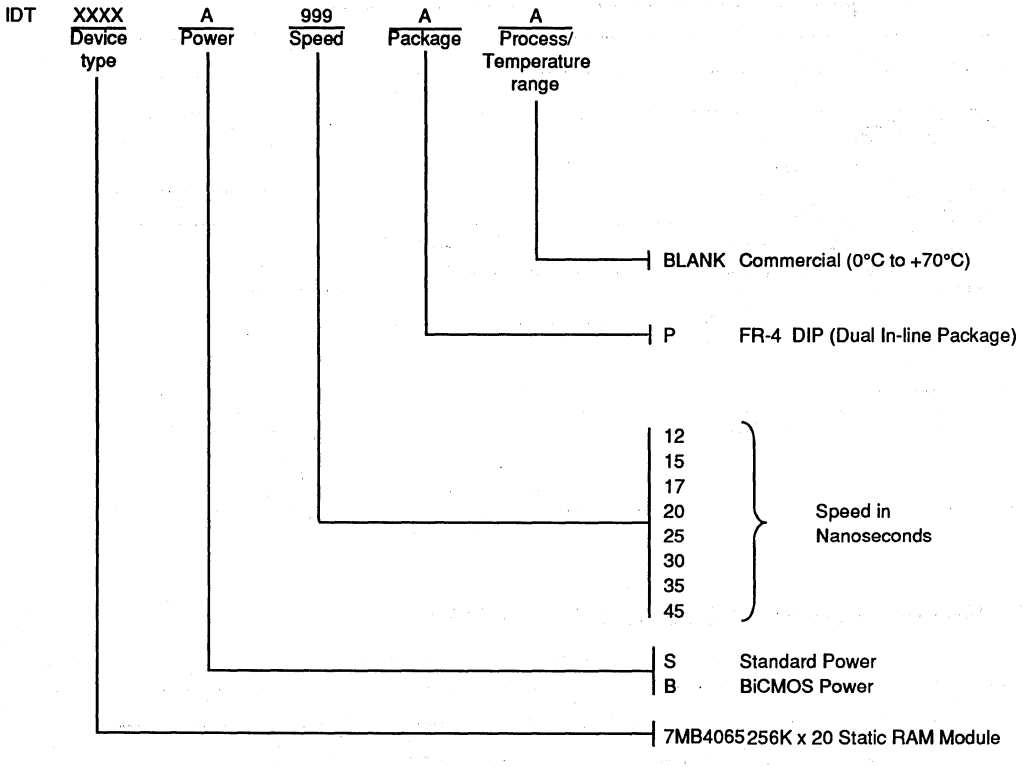
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CYCLE) (1,5,6)



2828 drw 09

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must High during all address transitions.
2. A write occurs during the overlap (twp) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. twp is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, so input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = VIL).
7. DOUT is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state, and input signals must not be applied.
9. Transition is measured ±200 mV from steady state. This parameter is guaranteed by design, but not tested.

ORDERING INFORMATION



Integrated Device Technology, Inc.

256K X 16 BiCMOS/CMOS STATIC RAM MODULE

PRELIMINARY
IDT7MB4066

FEATURES:

- High density 4 megabit BiCMOS/CMOS static RAM module
- Low profile 48-pin FR-4 DIP (Dual In-line Package)
- Fast access time: 12ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible
- Multiple GND pins for maximum noise immunity

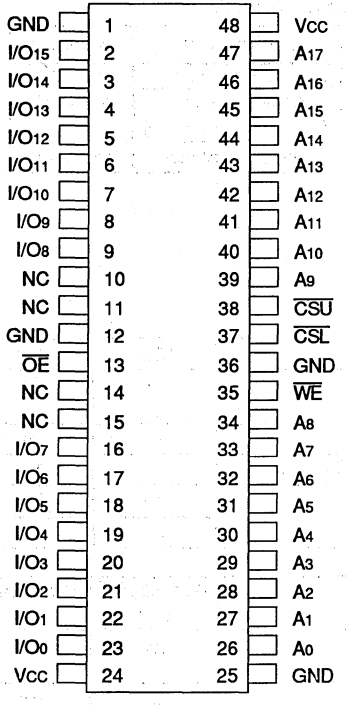
DESCRIPTION:

The IDT7MB4066 is a 256K x 16 CMOS static RAM module constructed on an epoxy laminate (FR-4) substrate using 4 256K x 4 static RAMs in plastic SOJ packages. Availability of two chip select lines (one for each group of two RAMs) provides byte access. The IDT7MB4066 is available with access time as fast as 12ns with minimal power consumption.

The IDT7MB4066 is packaged in a 48 pin FR-4 DIP (Dual In-line Package). The dual row configuration allows 48 pins to be placed on a package 2.4 inches long, 600 mils wide and 0.35 inches tall.

All inputs and outputs of the IDT7MB4066 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

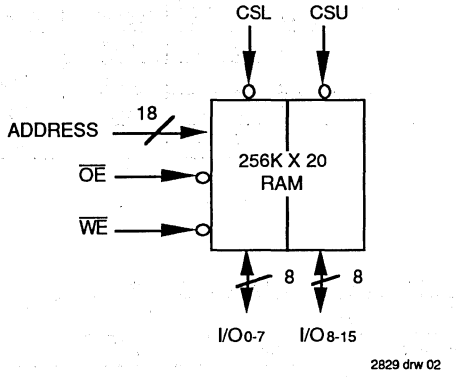
PIN CONFIGURATION (1)



2829 drw 01

DIP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



2829 drw 02

PIN NAMES

I/O0-15	Data Inputs/Outputs
A0-17	Address
$\overline{CSL}$	Chip Select - Lower Byte
$\overline{CSU}$	Chip Select - Upper Byte
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
NC	No Connect
Vcc	Power
GND	Ground

2829 tbl 01

NOTE:
1. For module dimensions, please refer to the module drawings in the packaging section.

B

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Comm.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2829 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6	V
V_{IL}	Input Low Voltage	-0.5 (1)	—	0.8	V

NOTE: 2829 tbl 03

1. V_{IL} = -2.0V for pulse width less than 10ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2829 tbl 04

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	Hi-Z	Standby
Read	L	L	H	Dout	Active
Write	L	X	L	Din	Active
Read	L	H	H	Hi-Z	Active

2829 tbl 08

CAPACITANCE

(T_A = +25°C, F = 1.0MHz)

Symbol	Parameter (1)	Conditions	Max.	Unit
$C_{IN(D)}$	Input Capacitance	V_{IN} = 0V	12	pF
$C_{IN(A)}$	Input Capacitance (Address and Control)	V_{IN} = 0V	36	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

2829 tbl 09

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	40	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max.; CS = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V

Symbol	Parameter	Test Conditions	7MB4066B(1) Max.	7MB4066S Max.	Unit
I_{CC}	Dymanic Operating Current	f = f_{MAX}(2); CS = V_{IL} V_{CC} = Max.; Output Open	800	600	mA
I_{SB}	Standby Supply Current	CS ≥ V_{IH}, V_{CC} = Max. Outputs Open, f = f_{MAX}(2)	—	240	mA
I_{SB1}	Full Standby Supply Current	CS ≥ V_{CC} – 0.2V; F = 0 V_{IN} > V_{CC} – 0.2V or < 0.2V	—	8	mA

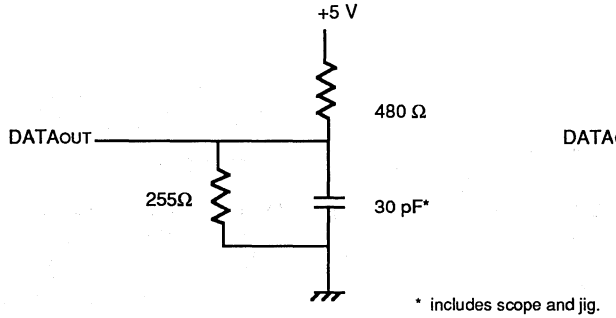
NOTES: 2829 tbl 09

1. Preliminary specifications only.
2. f_{MAX} = 1/t_{RC}

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1-4

2829 tbl 06



* includes scope and jig.

Figure 1. Output Load

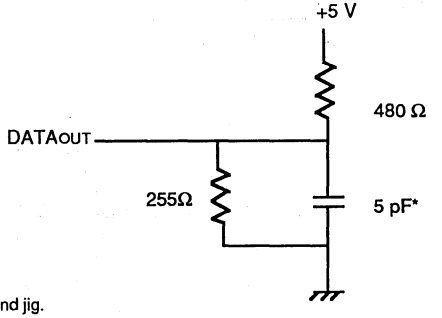


Figure 2. Output Load (for tOLZ, tOHZ, tCHZ, tCLZ, tWHZ, tOW) 2829 drw 03

AC ELECTRICAL CHARACTERISTICS

(VCC = 5V ±10%, TA = 0°C to +70°C)

		7MB4066BxxP						
		-12(2)		-15(2)		-17(2)		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle								
tRC	Read Cycle Time	12	—	15	—	17	—	ns
tAA	Address Access Time	—	12	—	15	—	17	ns
tACS	Chip Select Access Time	—	7	—	8	—	9	ns
tCLZ(1)	Chip Select to Output in Low Z	2	—	2	—	2	—	ns
tOE	Output Enable to Output Valid	—	5	—	6	—	8	ns
tOLZ(1)	Output Enable to Output in Low Z	2	—	2	—	2	—	ns
tCHZ(1)	Chip Deselect to Output in High Z	—	7	—	8	—	10	ns
tOHZ(1)	Output Disable to Output in High Z	—	4	—	5	—	6	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	ns
Write Cycle								
tWC	Write Cycle Time	12	—	15	—	17	—	ns
tCW	Chip Select to End of Write	8	—	9	—	10	—	ns
tAW	Address Valid to End of Write	9	—	10	—	12	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width	9	—	10	—	12	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tWHZ(1)	Write Enable to Output in High Z	—	5	—	6	—	7	ns
tDW	Data to Write Time Overlap	5	—	6	—	8	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	ns
tOW(1)	Output Active from End of Write	2	—	2	—	2	—	ns

NOTES:

1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

2829 tbl 09

B

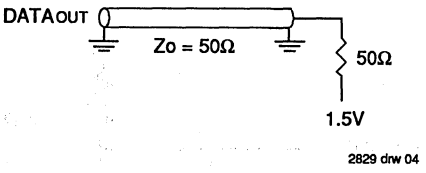


Figure 3. BICMOS Output Load

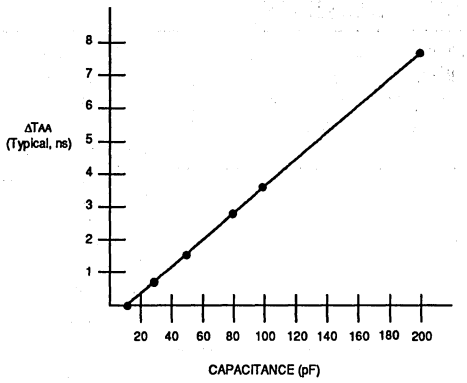


Figure 4. BiCMOS Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS

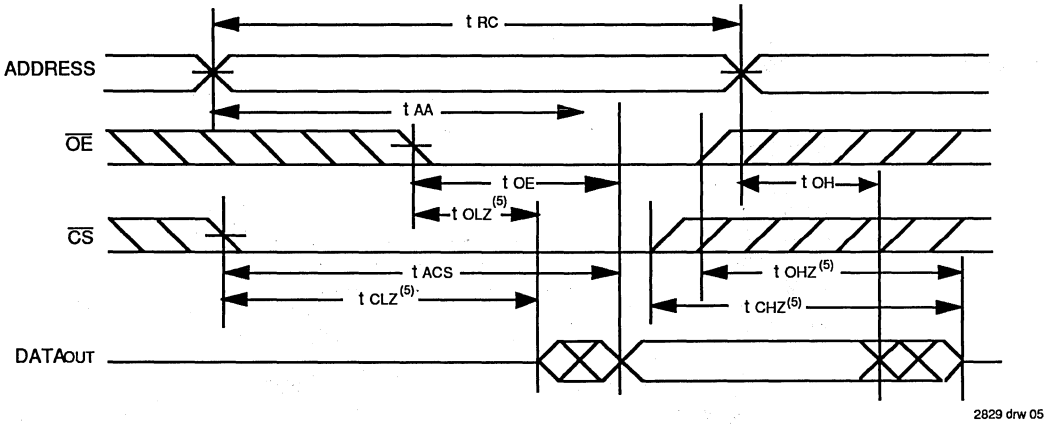
(VCC = 5.0V ± 10%, TA = 0°C to +70°C)

Symbol	Parameters	7MB4066SxxP										
		-20[2]		-25		-30		-35		-45		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
tAA	Address Access Time	—	20	—	25	—	30	—	35	—	45	ns
tACS	Chip Select Access Time	—	20	—	25	—	30	—	35	—	45	ns
tCLZ[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	10	—	12	—	15	—	18	—	23	ns
tOLZ[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	0	—	ns
tCHZ[1]	Chip Deselect to Output in High Z	—	10	—	12	—	15	—	18	—	20	ns
tOHZ[1]	Output Disable to Output in High Z	—	10	—	10	—	10	—	10	—	10	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	5	—	5	—	ns
tPU[1]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
tPD[1]	Chip Deselect to Power Down Time	—	20	—	25	—	30	—	35	—	45	ns
Write Cycle												
tWC	Write Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
tCW	Chip Selection to End of Write	15	—	20	—	25	—	30	—	40	—	ns
tAW	Address Valid to End of Write	15	—	20	—	25	—	30	—	40	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	15	—	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tWHZ[1]	Write Enable to Output in High Z	—	13	—	15	—	18	—	20	—	23	ns
tDW	Data to Write Time Overlap	12	—	15	—	17	—	20	—	25	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	ns
tOW[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns

2829 tbl 07

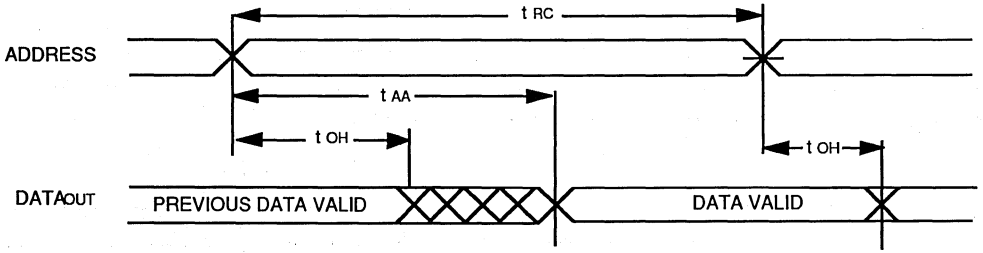
NOTES:
1. This parameter is guaranteed by design but not tested.
2. Preliminary specifications only.

TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



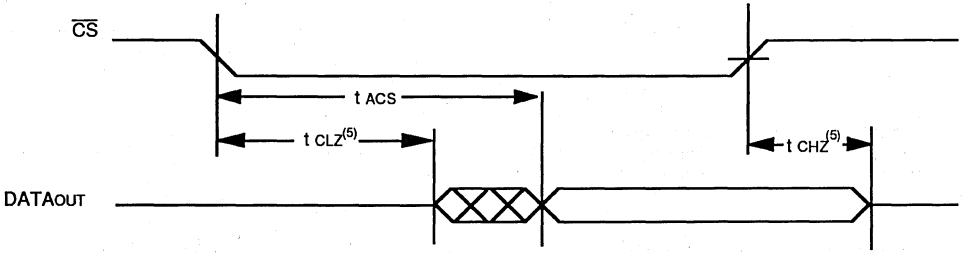
2829 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 2 (1,2,4)



2829 drw 06

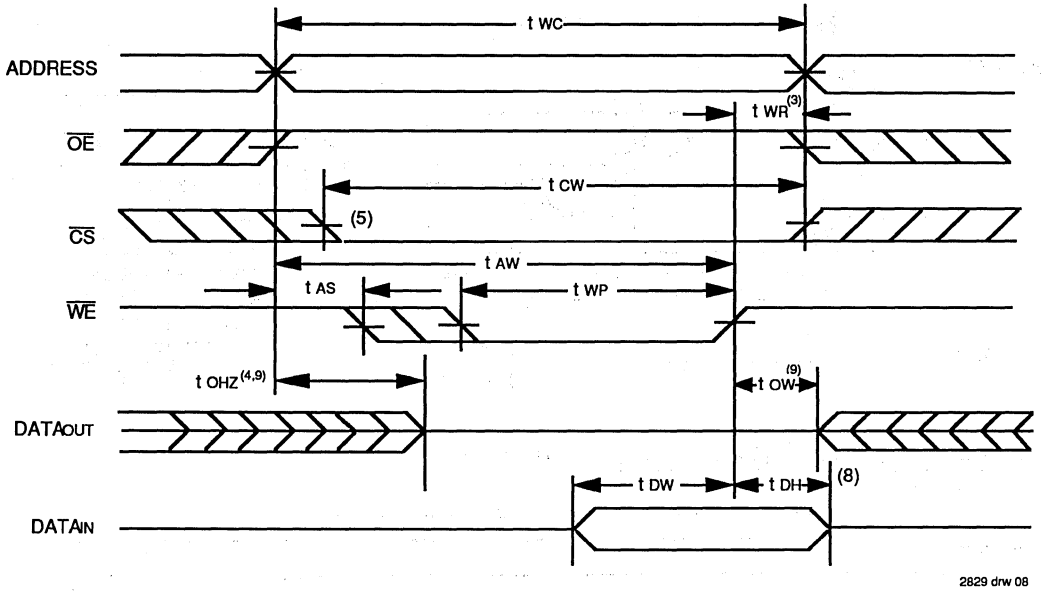
TIMING WAVEFORM OF READ CYCLE NO. 2 (1,3,4)



2829 drw 07

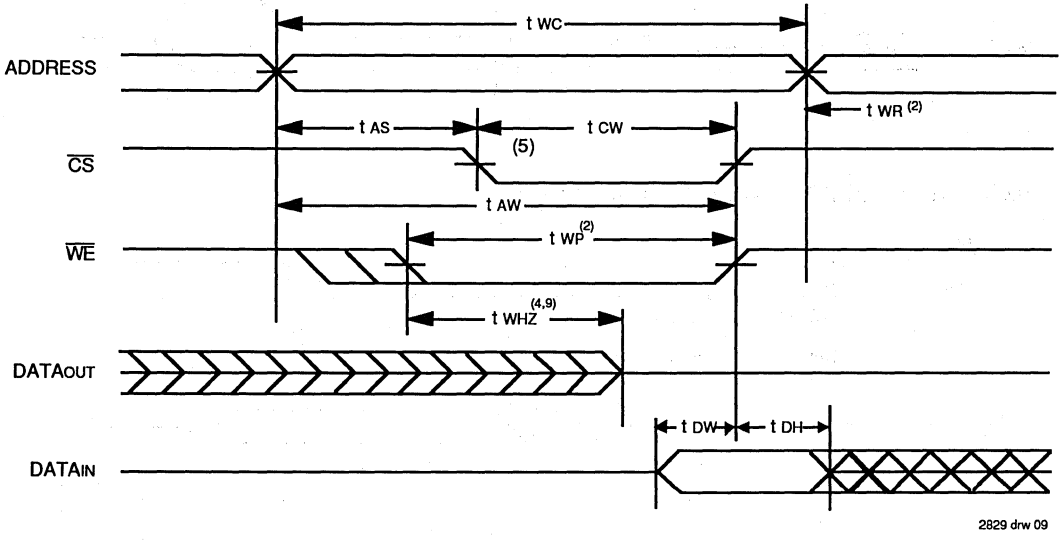
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = VIL.
3. Address valid prior to $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200 mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CYCLE) (1)



2829 drw 08

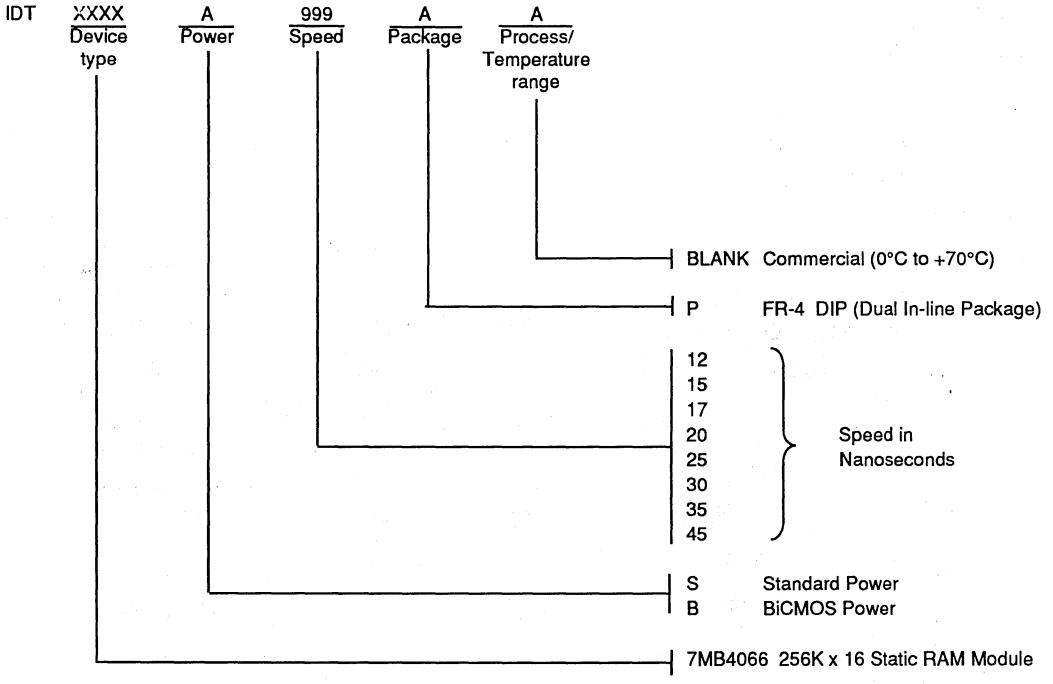
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CYCLE) (1,5,6)



2829 drw 09

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must High during all address transitions.
2. A write occurs during the overlap (twp) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. twp is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, so input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = VIL).
7. DOUT is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state, and input signals must not be applied.
9. Transition is measured ±200 mV from steady state. This parameter is guaranteed by design, but not tested.

ORDERING INFORMATION



B

Integrated Device Technology, Inc.

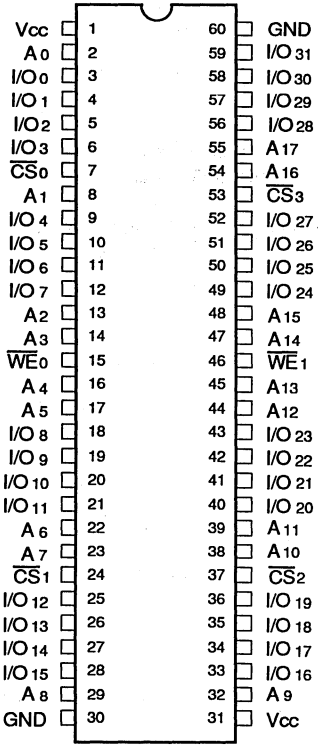
256K x 32 CMOS STATIC RAM MODULE

PRELIMINARY
IDT7MB4067

FEATURES:

- High density 8 megabit static RAM module
- Low profile 60 pin DIP (Dual In-line Package)
- Very fast access time: 20ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible
- Multiple GND pins and decoupling capacitors for maximum noise immunity

PIN CONFIGURATION[1]



2830 drw 01

DIP
TOP VIEW

NOTE:
1. For package dimensions, please refer to the module drawings in the packaging section.

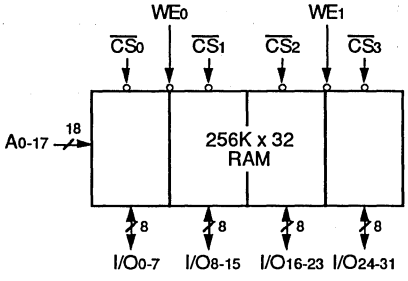
DESCRIPTION:

The IDT7MB4067 is a 256K x 32 static RAM module constructed on an epoxy laminate (FR-4) substrate using 8 256K x 4 static RAMs in plastic SOJ packages. Availability of four chip select lines (one for each group of two RAMs) provides byte access. The IDT7MB4067 is available with access time as fast as 20ns with minimal power consumption.

The IDT7MB4067 is packaged in a 60 pin DIP (Dual In-line Package). The DIP configuration allows 60 pins to be placed on a package 3.0 inches long and 0.6 inches wide and 0.365 inches tall.

All inputs and outputs of the IDT7MB4067 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



2830 drw 02

PIN NAMES

A0-A17	Addresses
I/O0-31	Data Inputs/Outputs
$\overline{CS}_0$	Chip Select for I/O0-7
$\overline{CS}_1$	Chip Select for I/O8-15
$\overline{CS}_2$	Chip Select for I/O16-23
$\overline{CS}_3$	Chip Select for I/O24-31
$\overline{WE}_0$	Write Enable for I/O0-15
$\overline{WE}_1$	Write Enable for I/O16-31
GND	Ground
Vcc	Power

2830 tbl 01

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
$C_{I/O}$	Data I/O Capacitance	$V_{(IN)}$ = 0V	15	pF
$C_{IN(W)}$	Input Capacitance ($\overline{WE}$)	$V_{(IN)}$ = 0V	35	pF
$C_{IN(C)}$	Input Capacitance ($\overline{CS}$)	$V_{(IN)}$ = 0V	18	pF
$C_{IN(A)}$	Input Capacitance (Address)	$V_{(IN)}$ = 0V	60	pF

NOTE: 2830 tbl 04
1. This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 2830 tbl 05
1. V_{IL} (min) = –1.5V for pulse width less than 10ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

2830 tbl 06

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	Hi-Z	Standby
Read	L	H	Dout	Active
Write	L	L	Din	Active

2830 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTES: 2830 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

B

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	7MB4067 Min.	7MB4067 Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	80	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max.; $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V

Symbol	Parameter	Test Conditions	7MB4067 Min.	7MB4067 Max.	Unit
I_{CC}	Dynamic Operating Current	f = f_{MAX}; $\overline{CS}$ = V_{IL} V_{CC} = Max.; Output Open	—	1200	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max. Outputs Open, f = f_{MAX}	—	480	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} – 0.2V; f = 0 V_{IN} > V_{CC} – 0.2V or < 0.2V	—	80	mA

2830 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1 & 2

2830 tbl 08

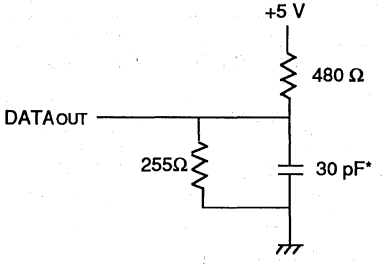


Figure 1. Output Load

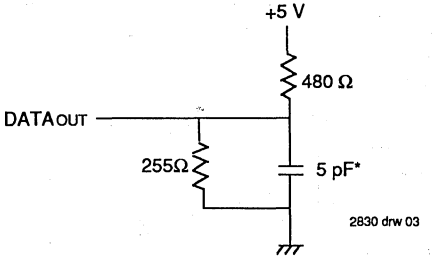


Figure 2. Output Load
(for tCH Z, tCLZ, tWHZ, tOW)

* Includes scope and jig.

AC ELECTRICAL CHARACTERISTICS

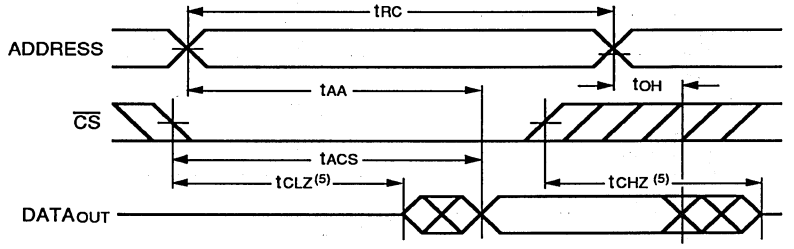
(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

		7MB4067SxxP										
		-20[2]		-25		-30		-35		-45		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
tAA	Address Access Time	—	20	—	25	—	30	—	35	—	45	ns
tACS	Chip Select Access Time	—	20	—	25	—	30	—	35	—	45	ns
tCLZ[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
tCHZ[1]	Chip Deselect to Output in High Z	—	10	—	12	—	15	—	18	—	20	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	5	—	5	—	ns
tPU[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
tPD[1]	Chip Deselect to Power-Down Time	—	20	—	25	—	30	—	35	—	45	ns
Write Cycle												
tWC	Write Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
tCW	Chip Select to End of Write	15	—	20	—	25	—	30	—	40	—	ns
tAW	Address Valid to End of Write	15	—	20	—	25	—	30	—	40	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	15	—	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tWHZ[1]	Write Enable to Output in High Z	—	13	—	15	—	18	—	20	—	23	ns
tDW	Data to Write Time Overlap	12	—	15	—	17	—	20	—	25	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	ns
tOW[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

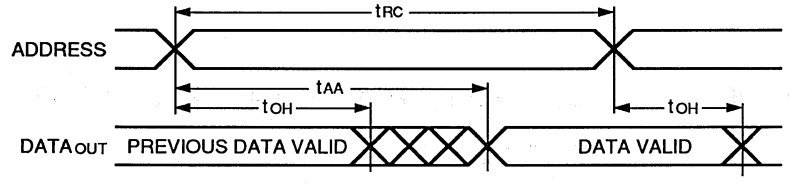
2830 tbl 09

TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



2830 drw 04

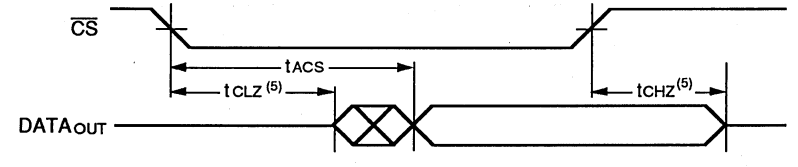
TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



2830 drw 05

B

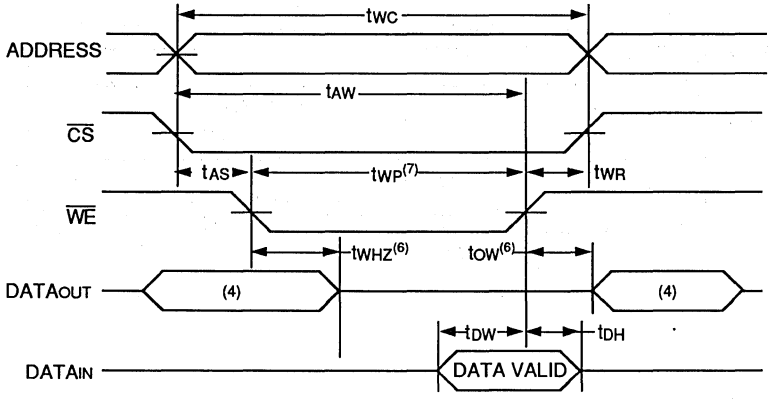
TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



2830 drw 06

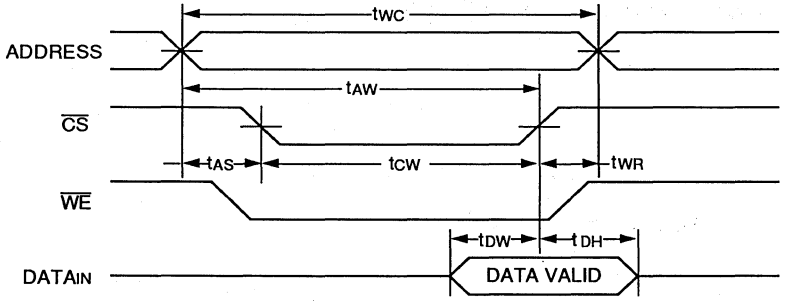
NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected. $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING) (1, 2, 3, 7)



2830 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING) (1, 2, 3, 5)

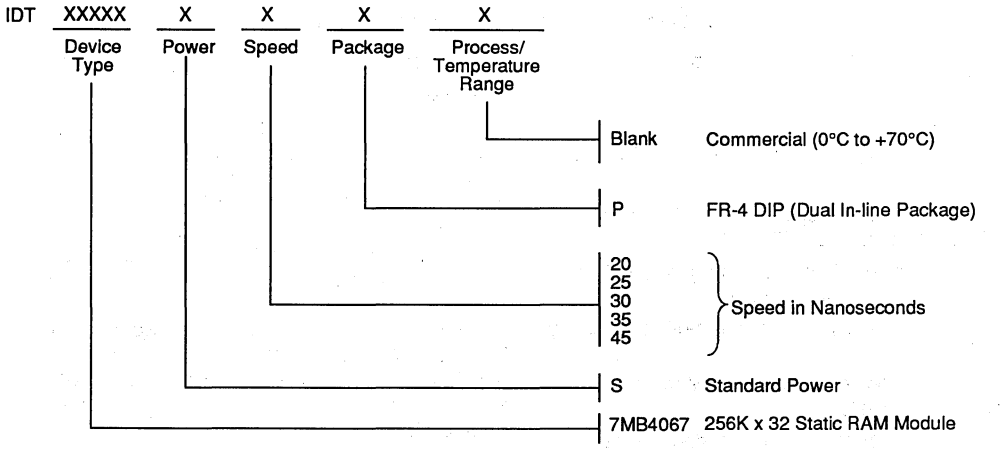


2830 drw 08

NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design but not tested.
7. During a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW.

ORDERING INFORMATION



2830 drw 010

B

Integrated Device Technology, Inc.

DUAL (16K x 60) DATA/INSTRUCTION CACHE MODULE FOR IDT79R3000 CPU

PRELIMINARY
IDT7MB6139

FEATURES:

- High-speed CMOS static RAM module constructed to support the IDT79R3000 RISC CPU as a complete data and instruction cache
- Operating frequencies to support 12MHz, 16.7MHz, 20MHz, 25MHz and 33MHz IDT79R3000
- Available in high-density, low profile 128-pin QIP (Quad In-line Package) with special stand-off
- Surface mounted SO components on a multi-layer epoxy substrate (FR-4)
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- On-board address latches for direct interface to the IDT79R3000 CPU
- TTL compatible I/Os
- Single 5V (± 10%) power supply

PIN CONFIGURATION

GND	1	65	GND	Vcc	128	64	Vcc
D0	2	66	D1	N.C.	127(1)	63	N.C.
D2	3	67	D3	N.C.	126(1)	62	N.C.
D4	4	68	D5	D58	125	61	D59
D6	5	69	D7	D56	124	60	D57
D8	6	70	D9	GND	123	59	D55
$\overline{WE}_1$	7	71	$\overline{OE}_1$	$\overline{WE}_4$	122	58	$\overline{OE}_4$
$\overline{CS1}_1$	8	72	GND	D54	121	57	$\overline{CS1}_4$
$\overline{CS1}_5$	9	73	D10	D53	120	56	$\overline{CS1}_8$
$\overline{WE}_5$	10	74	$\overline{OE}_5$	$\overline{WE}_8$	119	55	$\overline{OE}_8$
D11	11	75	D12	D51	118	54	D52
D13	12	76	Vcc	GND	117	53	D50
A0	13	77	A1	A12	116	52	A13
A2	14	78	A3	A10	115	51	A11
A4	15	79	A5	A8	114	50	A9
D14	16	80	GND	A6	113	49	A7
GND	17	81	LE1	LE2	112	48	GND
GND	18	82	LE3	LE4	111	47	GND
D15	19	83	D16	GND	110	46	D49
D17	20	84	Vcc	D47	109	45	D48
D18	21	85	D19	D45	108	44	D46
D20	22	86	D21	D43	107	43	D44
$\overline{WE}_2$	23	87	$\overline{OE}_2$	$\overline{WE}_7$	106	42	$\overline{OE}_7$
$\overline{CS1}_2$	24	88	GND	GND	105	41	$\overline{CS1}_7$
$\overline{CS1}_6$	25	89	D22	D42	104	40	$\overline{CS1}_3$
$\overline{WE}_6$	26	90	$\overline{OE}_6$	$\overline{WE}_3$	103	39	$\overline{OE}_3$
D23	27	91	D24	D40	102	38	D41
D25	28	92	D26	Vcc	101	37	D39
D27	29	93	D28	D37	100	36	D38
D29	30	94	D30	D35	99	35	D36
D31	31	95	D32	D33	98	34	D34
Vcc	32	96	Vcc	GND	97	33	GND

QIP
TOP VIEW

2800 drw 01

NOTES:

1. Pins 62, 63, 126, and 127 must be connected to GND for proper operation of this module.
2. For module dimensions, please refer to module drawings in the packaging section.

DESCRIPTION:

The IDT7MP6139 is a 240K-byte high-speed CMOS static RAM cache module constructed on a multilayer epoxy substrate (FR-4) using 28 (16K X 4) SRAMs, 8 IDT74FCT373 latches, and a IDT74FCTT244 buffer.

The construction and specifications of this module have been optimized to support its use as a complete 16K deep Instruction and Data cache for the IDT79R3000 MIPs™ microprocessor.

The IDT7MB6139 is organized as two separate banks of 16K x 60 with the IDT74FCT373s being used as address latches. The two banks of RAM with their associated address latches share a common 14-bit ADDRESS bus and a common 60-bit DATA bus. The chip select, write enable, RAM output enable and latch enable controls for the two banks are brought out separately to support interleaving access to the two banks of RAM. Each bank of address latches reduces the capacitance loading on the outputs of the latches; thereby, enhancing CPU performance.

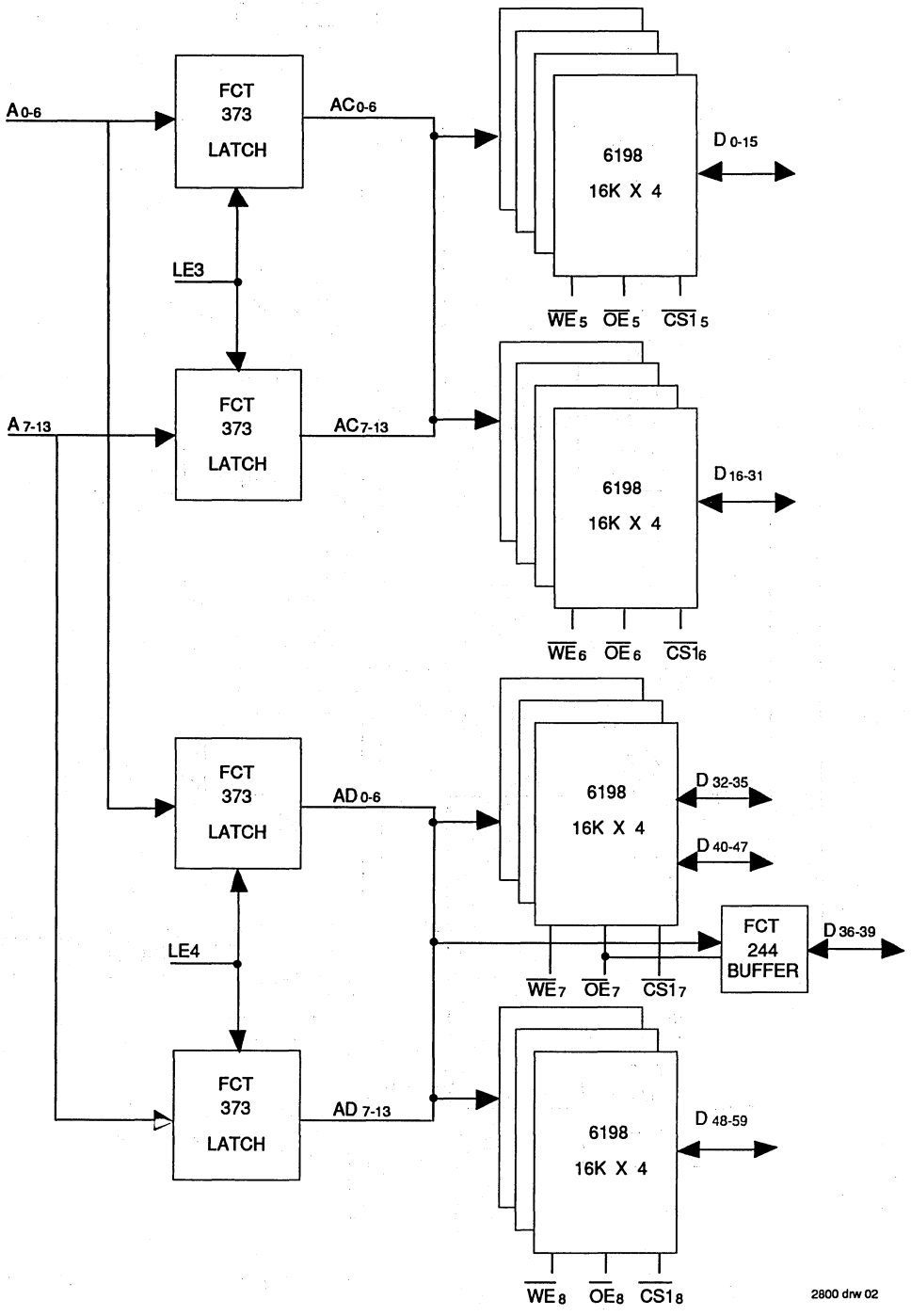
All inputs and outputs of the IDT7MB6139 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

PIN NAMES

D0 - D59	Data Inputs/Outputs
A0 - A13	Address Inputs
LE1 - LE4	Latch Enables
$\overline{CS1}_1$ - $\overline{CS1}_8$	RAM Selects
$\overline{WE}_1$ - $\overline{WE}_8$	Write Enables
$\overline{OE}_1$ - $\overline{OE}_8$	Output Enables
GND	Ground
Vcc	Power Supply
N.C.	No connection (1)

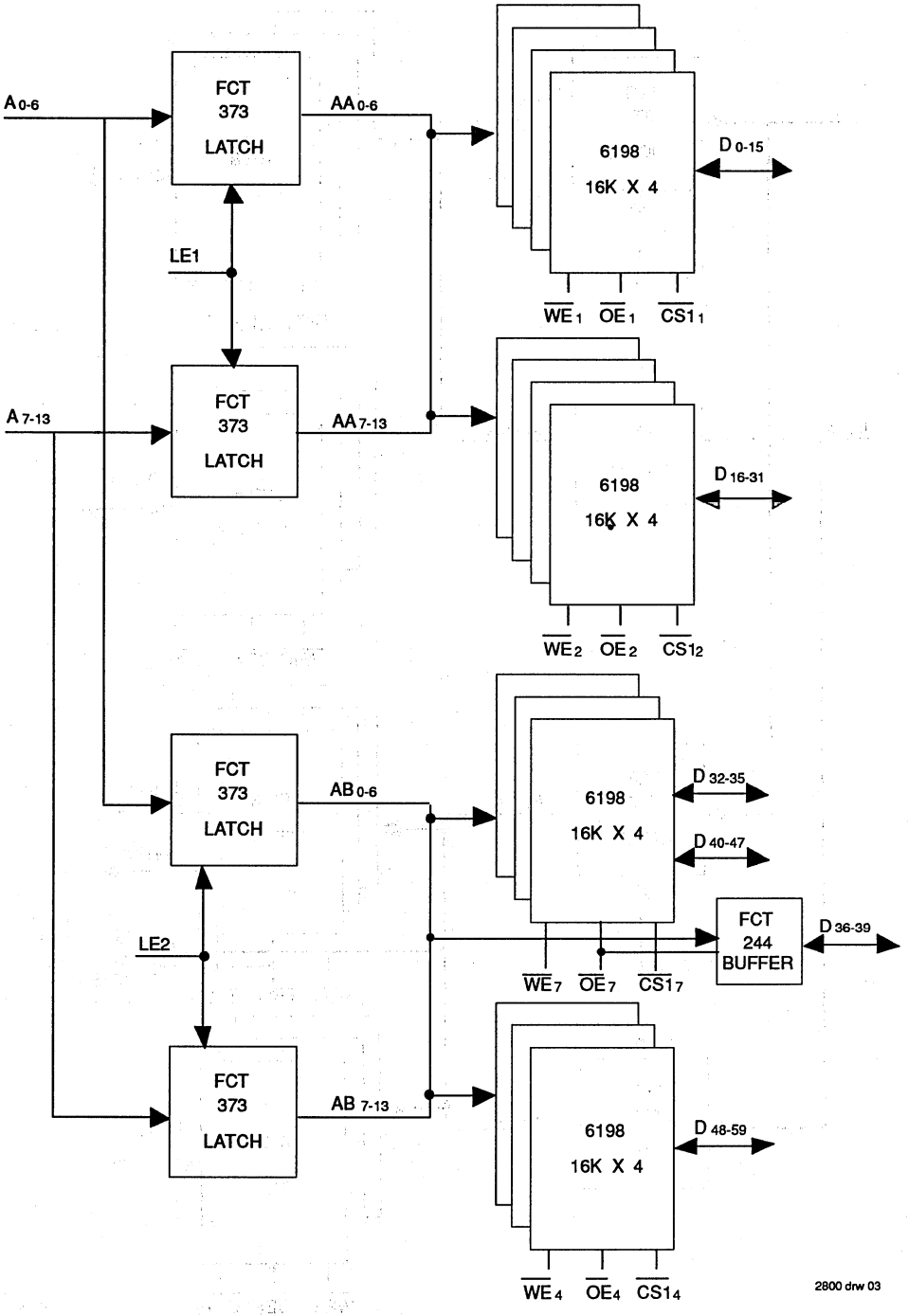
2800 tbl 01

CACHE - BANK "A"



B

CACHE - BANK "B"


A0-6
FCT 373 LATCH
AA0-6
6198 16K X 4
D0-15
LE1
WE1 OE1 CS11
A7-13
FCT 373 LATCH
AA7-13
6198 16K X 4
D16-31
WE2 OE2 CS12
FCT 373 LATCH
AB0-6
6198 16K X 4
D32-35
D40-47
LE2
FCT 244 BUFFER
D36-39
WE7 OE7 CS17
FCT 373 LATCH
AB7-13
6198 16K X 4
D48-59
WE4 OE4 CS14
2800 drw 03

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Comm.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperture	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

2800 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

Mode	$\overline{CS1}$	$\overline{CS2}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	X	High Z	Standby
Standby	X	H	X	X	High Z	Standby
Read	L	L	L	H	Dout	Active
Read	L	L	H	H	High Z	Active
Write	L	L	X	L	DIN	Active

2800 tbl 07

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6	V
V_{IL}	Input Low Voltage	-0.5 (1)	—	0.8	V

2800 tbl 03

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

2800 tbl 04

CAPACITANCE (1) (T_A = +25°C, F = 1.0 MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	30	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	18	pF

2800 tbl 08

NOTE:
1. This parameter is guaranteed by design but not tested.

B

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5.0V ± 10%, T_A = 0°C to +70°C)

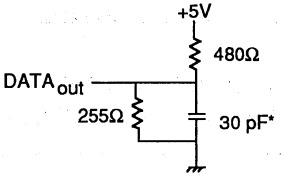
Symbol	Parameter	Test Conditions	12 MHz		16.7 MHz		20 MHz		25 MHz		33 MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I_{LI}	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	-20	20	-20	20	-20	20	-20	20	-20	20	µA
I_{LO}	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	-10	10	-10	10	-10	10	-10	10	-10	10	µA
I_{CC1}	Operating Current	$\overline{CS}$ = V_{IL}, V_{CC} = Max. Outputs Open, f = 0	—	3000	—	3000	—	3000	—	3500	—	3750	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ = V_{IL}, f = f_{MAX}, Outputs Open	—	3750	—	3750	—	4050	—	4500	—	4750	mA
I_{SB1}	Full Standby Operating Current	$\overline{CS}$ ≥ V_{CC} - 0.2V, V_{IN} > V_{CC} - 0.2V or < 0.2V	—	450	—	450	—	450	—	600	—	750	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}	—	1500	—	1500	—	1650	—	1800	—	2000	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = 4mA	2.4	—	2.4	—	2.4	—	2.4	—	2.4	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min. I_{OL} = 8mA	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	V

2800 tbl 05

AC TEST CONDITIONS

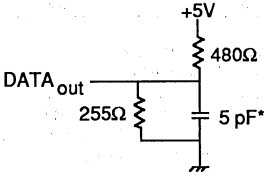
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2800 tbl 06



* Including scope and jig.

Figure 1. Output Load



2800 drw 04

Figure 2. Output Load (for tOLZ, tOHZ)

AC ELECTRICAL CHARACTERISTICS

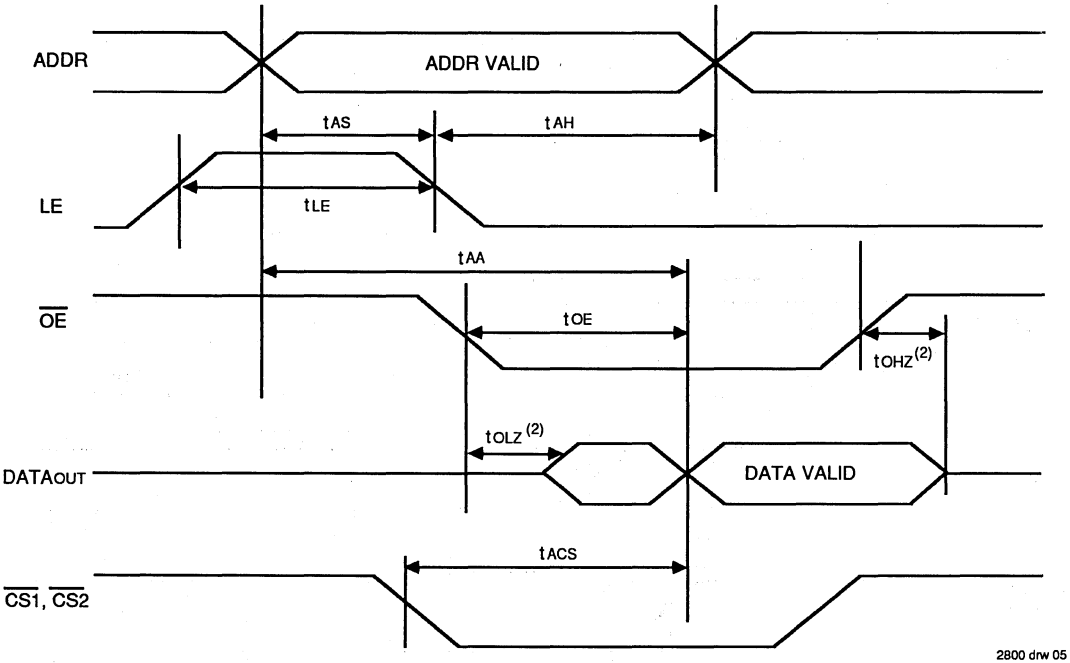
(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameters	12MHz		16.7 MHz		20 MHz		25 MHz		33 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
tLE	Latch Enable Width	8	—	6	—	6	—	6	—	6	—	ns
tAS	Address Setup Time to LE	4	—	2	—	2	—	4	—	4	—	ns
tAH	Address Hold Time from LE	3	—	1.5	—	1.5	—	3.5	—	3.5	—	ns
tAA(2)	Address Access Time	—	45	—	35	—	30	—	25	—	20	ns
tACS	Chip Select Time	—	40	—	30	—	25	—	20	—	15	ns
tOE	Output Enable Time	—	22	—	17	—	13	—	8	—	5	ns
tOHZ(1)	Output Disable to Output in High Z	2	16	2	14	2	10	2	8	2	6	ns
tOHZ(1)	Output Disable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
Write Cycle												
tLE	Latch Enable Width	8	—	6	—	6	—	6	—	6	—	ns
tAS	Address Setup Time to LE	4	—	2	—	2	—	4	—	4	—	ns
tAH	Address Hold Time from LE	3	—	1.5	—	1.5	—	3.5	—	3.5	—	ns
tAW	Address Valid to End of Write	40	—	30	—	25	—	23	—	20	—	ns
tCW	Chip Select to End of Write	35	—	25	—	20	—	18	—	15	—	ns
tWP	Write Pulse Width	30	—	25	—	20	—	17	—	12	—	ns
tDW	Data Valid to End of Write	20	—	13	—	13	—	11	—	8	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns

NOTES:
1. This parameter is guaranteed by design but not tested.
2. LE already asserted.

2800 tbl 07

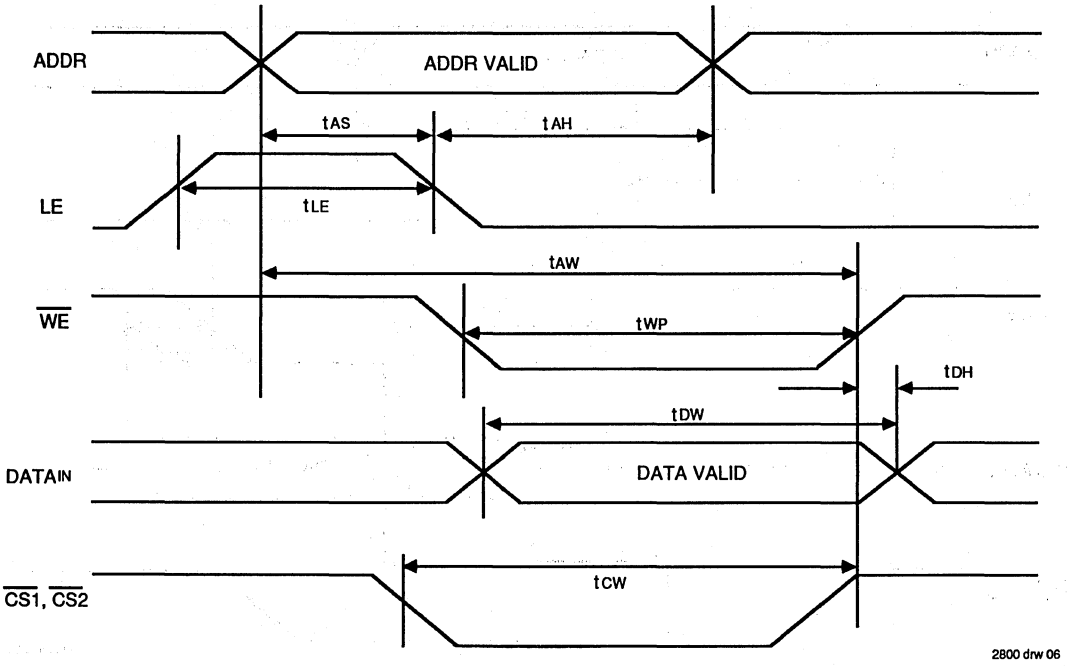
TIMING WAVEFORM OF READ CYCLE[1]



NOTES:
1. $\overline{WE}$ and $\overline{CS}$ must be High for all address transitions.
2. This parameter is guaranteed by design but not tested.

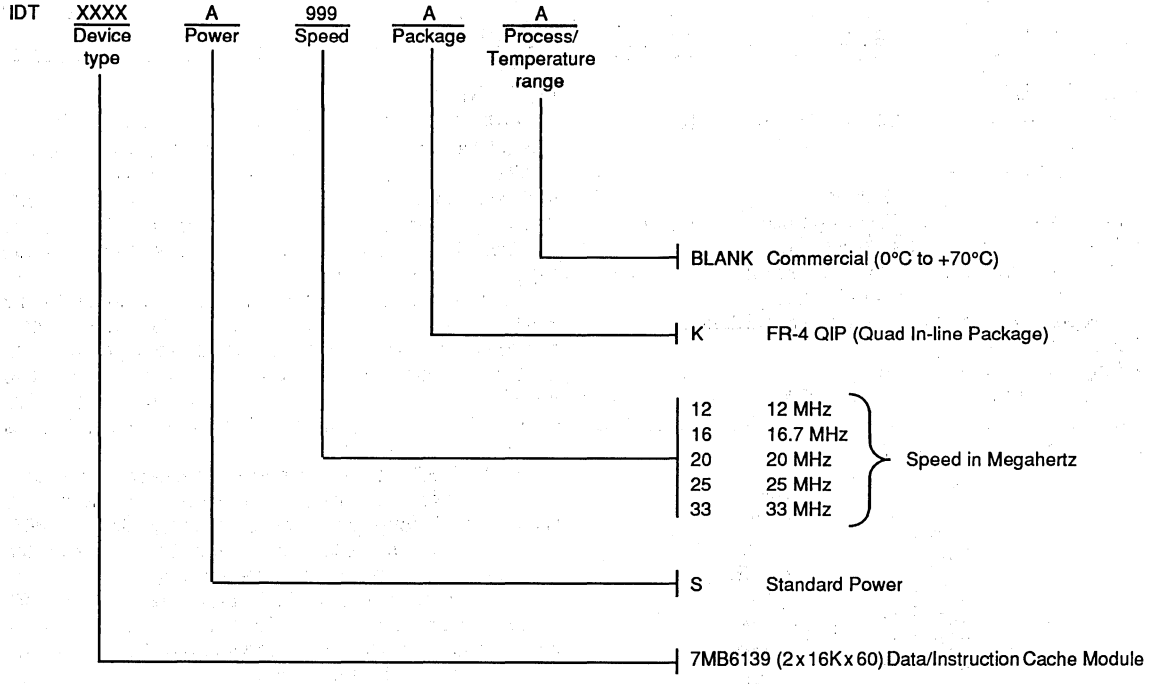
B

TIMING WAVEFORM OF WRITE CYCLE[1]



NOTE:
1. A write occurs (t_{WP}) during the overlap of a Low $\overline{CS}$ and $\overline{WE}$ and a High LE.

ORDERING INFORMATION



B

Integrated Device Technology, Inc.

128K x 8
64K x 8
CMOS DUAL-PORT STATIC RAM MODULE

ADVANCE INFORMATION
IDT7MP1021
IDT7MP1023

FEATURES

- High density 1M/512K CMOS dual-port static RAM module
- Fast access times:
  - 25, 30, 35, 40, 50, 65ns
- Fully asynchronous read/write operation from either port
- On-board semaphore ($\overline{SEM}$) controls
- Surface mounted plastic components on a 64-pin FR-4 SIMM (Single In-line Memory Module)
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Single 5V (±10%) power supply
- Input/outputs directly TTL compatible

PIN CONFIGURATION

VCC	1	2	GND
L_$\overline{OE}$	3	4	R_$\overline{OE}$
L_R/$\overline{W}$	5	6	R_R/$\overline{W}$
L_$\overline{SEM}$	7	8	R_$\overline{SEM}$
L_$\overline{CS}$	9	10	R_$\overline{CS}$
L_I/O(0)	11	12	R_I/O(0)
L_I/O(1)	13	14	R_I/O(1)
GND	15	16	R_I/O(2)
L_I/O(2)	17	18	R_I/O(3)
L_I/O(3)	19	20	R_I/O(4)
L_I/O(4)	21	22	R_I/O(5)
L_I/O(5)	23	24	R_I/O(6)
L_I/O(6)	25	26	R_I/O(7)
L_I/O(7)	27	28	R_A(0)
L_A(0)	29	30	R_A(1)
L_A(1)	31	32	R_A(2)
L_A(2)	33	34	R_A(3)
L_A(3)	35	36	R_A(4)
L_A(4)	37	38	R_A(5)
L_A(5)	39	40	R_A(6)
L_A(6)	41	42	R_A(7)
L_A(7)	43	44	R_A(8)
L_A(8)	45	46	GND
L_A(9)	47	48	R_A(9)
L_A(10)	49	50	R_A(10)
L_A(11)	51	52	R_A(11)
L_A(12)	53	54	R_A(12)
L_A(13)	55	56	R_A(13)
L_A(14)	57	58	R_A(14)
L_A(15)	59	60	R_A(15)
L_A(16)	61	62	R_A(16)
GND	63	64	VCC

SIMM
TOP VIEW

DESCRIPTION:

The IDT7MP1021/IDT7MP1023 is a 128K x 8/64K x 8 high-speed CMOS dual-port static RAM module constructed on a multilayer glass epoxy laminate (FR-4) substrate using eight IDT7006 (16K x 8) dual-port RAMs and two IDT 74FCT138 decoders or depopulated using only four IDT7006s and two decoders.This module provides two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory. The $\overline{SEM}$ controls can be used to facilitate port-to-port communication via "handshake" signaling. The $\overline{SEM}$ controls are logic latches which are part of the IDT7006 but independent of the dual-port RAM memory array. This control allows the signalling of information to easily pass through the dual-port module.

The IDT7MP1021/1023 module is packaged on a multilayer glass expoxy laminate (FR-4) 64-pin SIMM (Single In-line Memory Module) with dimensions of only 3.85" x 0.305" x 1.12". Maximum access times as fast as 25ns over the commercial temperature range are available.

All inputs and outputs of the IDT7MP1021/1023 are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation of the module.

PIN NAMES

Left Port	Right Port	Description
L_A (0–16)	R_A (0–16)	Address Inputs
L_I/O (0–7)	R_I/O (0–7)	Data Inputs/Outputs
L_R/$\overline{W}$	R_R/$\overline{W}$	Read/Write Enables
L_$\overline{CS}$	R_$\overline{CS}$	Chip Select
L_$\overline{OE}$	R_$\overline{OE}$	Output Enable
L_$\overline{SEM}$	R_$\overline{SEM}$	Semaphore Control
Vcc		Power
GND		Ground

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Integrated Device Technology, Inc.

256K x 16 CMOS STATIC RAM MODULE

IDT7MP4046

FEATURES:

- High-speed 4 megabit CMOS static RAM module
- Fast access time: 70ns (max.)
- Low power consumption
  - — Active: 220mA max.
  - — CMOS Standby: 450µA max.
  - — Data retention: 250µA max. (Vcc= 2V)
- Surface mounted small outline plastic packages on a 45 pin FR-4 SIP (Single In-line Package)
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible

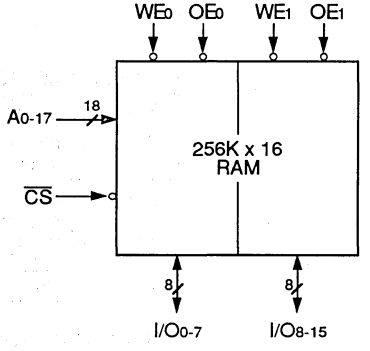
DESCRIPTION:

The IDT7MP4046 is a 256K x 16 CMOS static RAM module constructed on a multilayer epoxy laminate (FR-4) substrate using 4 128K x 8 static RAMs in small outline plastic packages and a one-of-four decoder. Availability of two Write Enables and two Output Enables provides byte access and output control flexibility. The IDT7MP4046 is available with access times as fast as 70ns with a maximum operating current of 220mA. For battery backup applications, there is a very low data retention current.

The IDT7MP4046 is packaged in a 45 pin FR-4 SIP (Single In-line Package). This results is a package 4.5 inches in length and 0.14 inches in thickness.

All inputs and outputs of the IDT7MP4046 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



B

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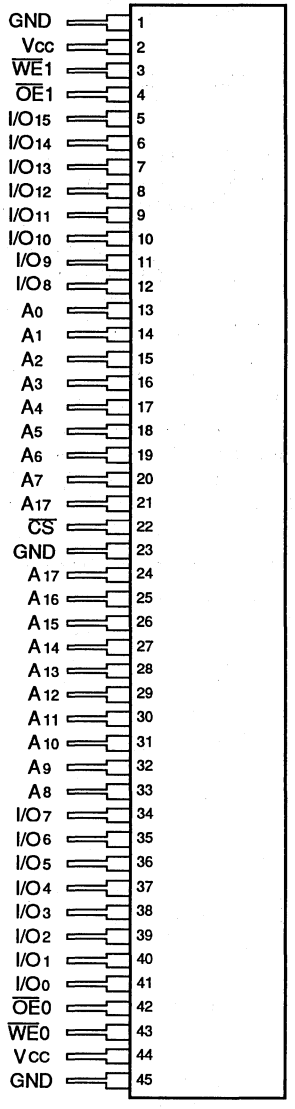
PIN CONFIGURATION[1, 2]



SIP 2832 drw 02
FRONT VIEW

NOTES:
1. For module dimensions, please refer to the module drawings in the packaging section.
2. Pins 21 and 24 must be tied together.

PIN NAMES

I/O0–I/O15	Data Inputs/Outputs
A0–A17	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}_{0-1}$	Write Enables
$\overline{OE}_{0-1}$	Output Enables
Vcc	Power
GND	Ground

2832 tbl 01

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	-10 to +85	°C
TSTG	Storage Temperature	-55 to +125	°C
IOUT	DC Output Current	50	mA

2832 tbl 03

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE[1] (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
CIN(A)	Input Capacitance (Address)	VIN = 0V	30	pF
CIN(D)	Input Capacitance (Data, $\overline{WE}$, $\overline{OE}$)	VIN = 0V	15	pF
CIN(C)	Input Capacitance($\overline{CS}$)	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	20	pF

2832 tbl 04

NOTE:
1. This parameter is guaranteed by design, but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

2832 tbl 05

NOTE:
1. VIL = -3.0V for pulse width less than 20ns.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	DATAOUT	Active
Write	L	L	High Z	Active

2832 tbl 02

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2832 tbl 06

DC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V ± 10%, TA = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
|ILI|	Input Leakage	VCC = Max., VIN = GND to VCC	—	4	µA
|ILO|	Output Leakage	VCC = Max. $\overline{CS}$ = VIH, VOUT = GND to VCC	—	4	µA
VOL	Output Low Voltage	VCC = Min., IOL = 2mA	—	0.4	V
VOH	Output High Voltage	VCC = Min., IOH = -1mA	2.4	—	V
ICC	Dynamic Operating Current	VCC = Max., $\overline{CS}$ = VIL, f = fMAX, Output Open	—	220	mA
ISB	Standby Supply Current (TTL Levels)	$\overline{CS}$ ≥ VIH, VCC = Max., f = fMAX, Ouput Open	—	12	mA
ISB1	Full Standby Supply Current (CMOS Levels)	$\overline{CS}$ ≥ VHC, VIN ≥ VHC or ≤ VLC VCC = Max., Output Open	—	450	µA

2832 tbl 07

DATA RETENTION CHARACTERISTICS (1)

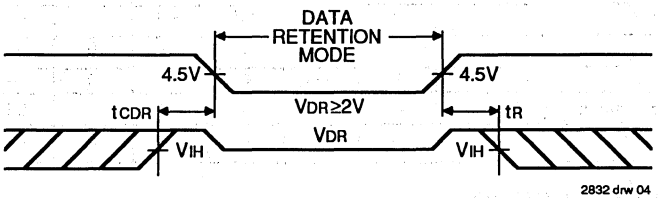
(TA = 0°C to +70°C)

Symbol	Parameter	Test Condition	Min.	Max. cc @ 2.0V	Unit
VDR	Vcc for Data Retention	—	2.0	—	V
ICCDR	Data Retention Current	$\overline{CS}$ ≥ VCC - 0.2V	—	250	µA
tCDR(3)	Chip Deselect to Data Retention Time	VIN ≤ VCC - 0.2V	0	—	ns
tR(3)	Operation Recovery Time	VIN ≥ - 0.2V	tRC(2)	—	ns

2832 tbl 10

NOTES:
1. VCC = 2V, TA = +25°C.
2. tRC = Read Cycle Time.
3. This parameter is guaranteed by design, but not tested.

DATA RETENTION WAVEFORM



2832 drw 04

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2832 tbl 08

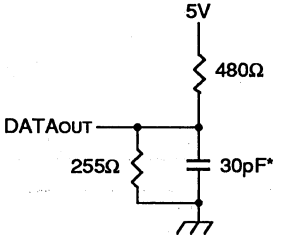


Figure 1. Output Load

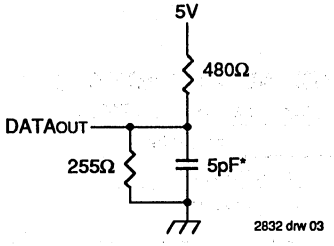


Figure 2. Output Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

*Including scope and jig

AC ELECTRICAL CHARACTERISTICS

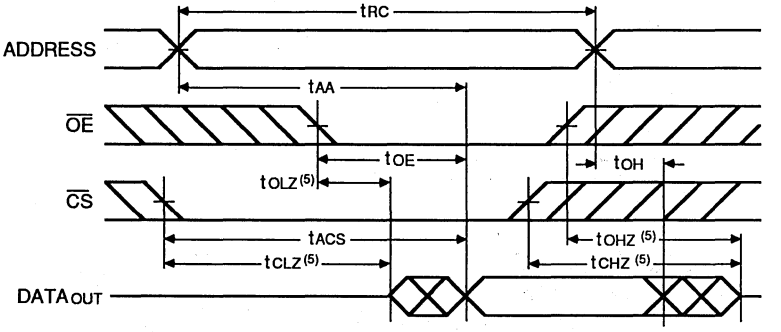
(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

		7MP4046LxxS								
		-70		-85		-100		-120		
Symbol	Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
READ CYCLE										
t_{RC}	Read Cycle Time	70	—	85	—	100	—	120	—	ns
t_{AA}	Address Access Time	—	70	—	85	—	100	—	120	ns
t_{ACS}	Chip Select Access Time	—	70	—	85	—	100	—	120	ns
t_{OE}	Output Enable to Output Valid	—	45	—	48	—	50	—	60	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	30	—	33	—	35	—	40	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	—	40	—	43	—	45	—	50	ns
t_{OH}	Output Hold from Address Change	10	—	10	—	10	—	10	—	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	70	—	85	—	100	—	120	—	ns
t_{WP}	Write Pulse Width	55	—	65	—	75	—	90	—	ns
t_{AS}	Address Set-up Time	0	—	2	—	5	—	5	—	ns
t_{AW}	Address Valid to End of Write	65	—	82	—	90	—	100	—	ns
t_{CW}	Chip Selection to End of Write	65	—	80	—	85	—	100	—	ns
t_{DS}	Data Set-up Time	35	—	38	—	40	—	45	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}(1)	Write Enable to Ouput in High Z	—	30	—	33	—	35	—	40	ns
t_{OW}(1)	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

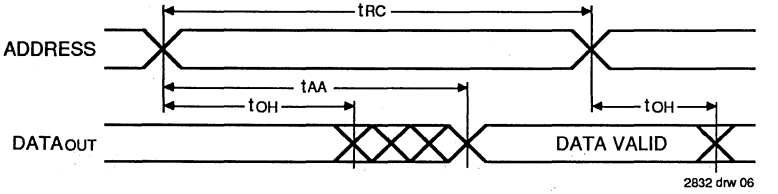
2832 tbl 09

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



2832 drw 05

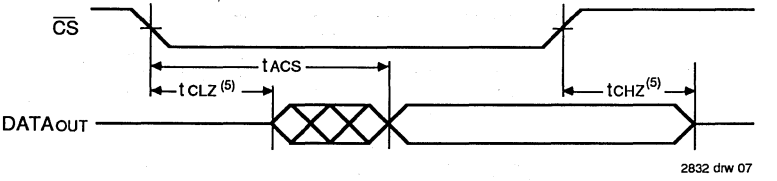
TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2832 drw 06

B

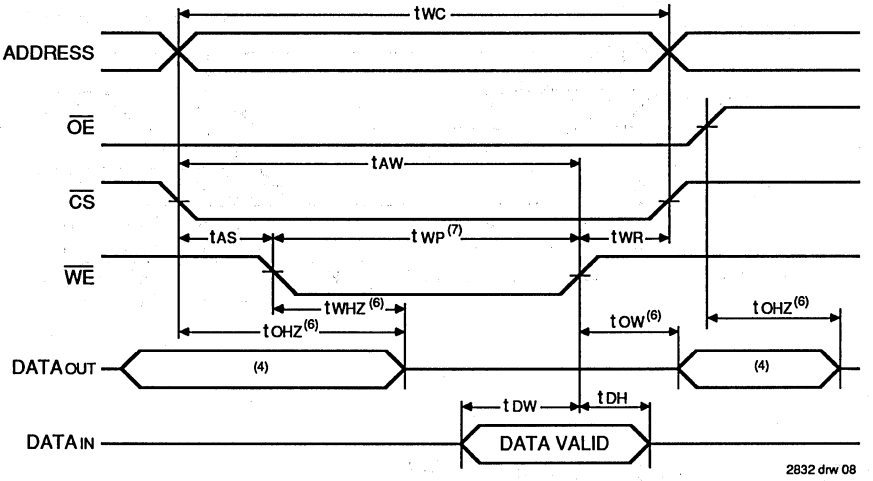
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



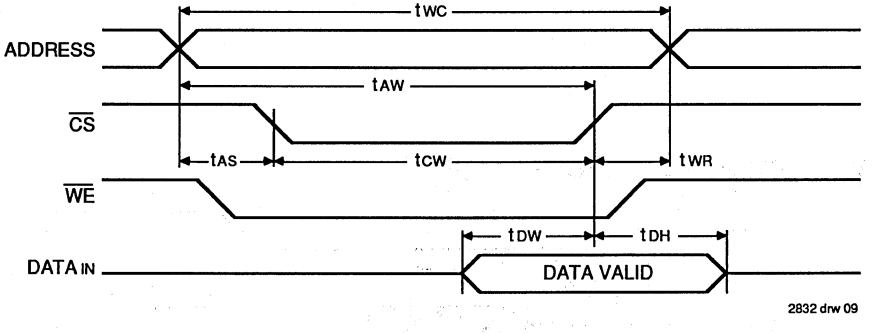
2832 drw 07

NOTES:
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)

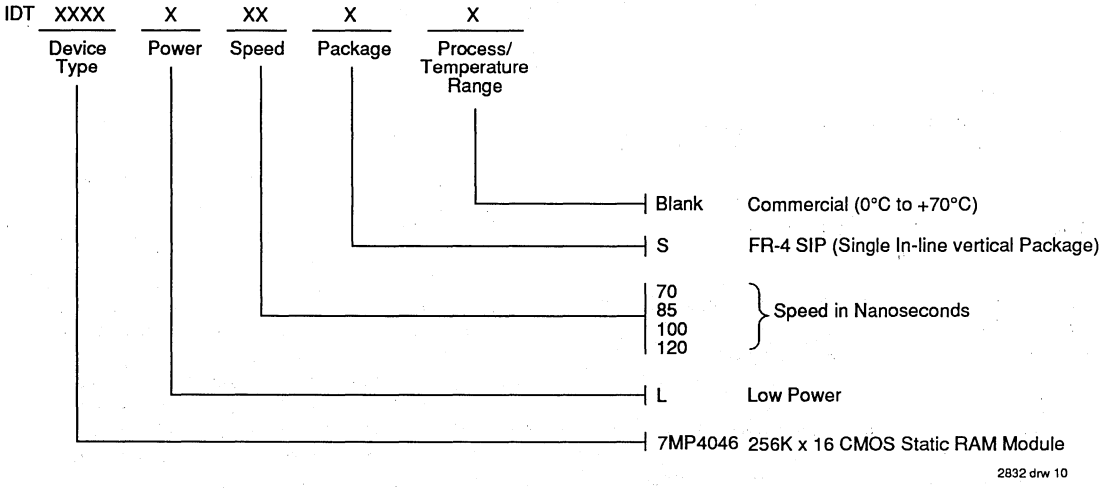


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going High to the end of write cycle.
4. During this period, I/O pins are in the output state and inputs signals must not be applied.
5. If the $\overline{CS}$ Low transition occurs simultaneously with or after the $\overline{WE}$ Low transitions, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).. This parameter is graranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse ((t_{WP}) > t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{WD}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

ORDERING INFORMATION



B

Integrated Device Technology, Inc.

256KB/ 1MB/ 4MB IDT79R4000 SECONDARY CACHE MODULE BLOCK FAMILY

PRELIMINARY
IDT7MP6074
IDT7MP6084
IDT7MP6094

FEATURES:

- High-speed BiCEMOS™/CEMOS™ secondary cache module block constructed to support the IDT79R4000 CPU
- Available as a pin compatible family to build 256 kilobyte, 1 megabyte and 4 megabyte secondary caches
- Zero wait-state operation
- Four word line size
- Operating frequencies to support 50MHz and 75MHz IDT79R4000
- Available as a set of four identical high density 80 lead (gold-plated fingers) SIMMs (Single In-Line Memory Modules)
- Surface mounted plastic components on a multilayer epoxy laminate (FR-4) substrate
- Multiple ground pins and decoupling capacitors for maximum noise immunity
- TTL compatible I/Os
- Single 5V (±10%) power supply

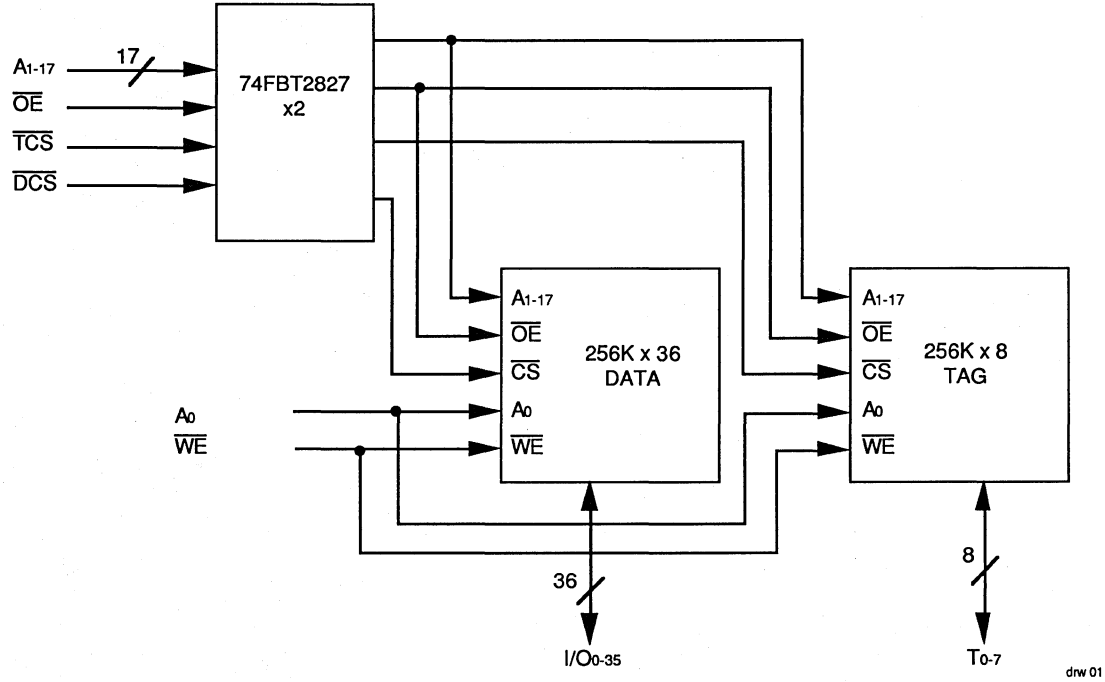
DESCRIPTION:

The IDT7MP6074 is a 256 kilobyte IDT79R4000 secondary cache module block constructed on a multilayer epoxy laminate substrate (FR-4), using 11 16K x 4 static RAMs and 2 IDT74FBT2827 drivers. The IDT7MP6084 is a 1 megabyte IDT79R4000 secondary cache module block using 11 64K x 4 static RAMs, and the IDT7MP6094 is a 4 megabyte IDT79R4000 secondary cache module block using 11 256K x 4 static RAMs. The IDT74FBT2827 has internal 25Ω series resistors and BiCEMOS™ I/Os resulting in the fastest propagation times with minimal overshoot and ringing. Four identical cache module blocks comprise a full secondary cache.

The IDT7MP6074/84/94 support use in an IDT79R4000-based system at speeds of 50MHz and 75MHz with zero wait-state operation. Module supports a four word line size. For other line sizes, please consult factory.

All inputs and outputs of the IDT7MP6074/84/94 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refresh for operation.

FUNCTIONAL BLOCK DIAGRAM



BiCEMOS and CEMOS are trademarks of Integrated Device Technology Inc.

PIN CONFIGURATION[1, 2]

GND	1	2	VCC
I/O0	3	4	I/O1
I/O2	5	6	I/O3
I/O4	7	8	I/O5
I/O6	9	10	GND
I/O7	11	12	I/O8
I/O9	13	14	I/O10
I/O11	15	16	I/O12
I/O13	17	18	I/O14
GND	19	20	I/O15
I/O16	21	22	I/O17
I/O18	23	24	I/O19
I/O20	25	26	I/O21
I/O22	27	28	GND
VCC	29	30	I/O23
I/O24	31	32	I/O25
I/O26	33	34	I/O27
I/O28	35	36	I/O29
GND	37	38	I/O30
I/O31	39	40	I/O32
I/O33	41	42	I/O34
I/O35	43	44	GND
$\overline{WE}$	45	46	A0
A1	47	48	A2
A3	49	50	A4
A5	51	52	A6
GND	53	54	VCC
$\overline{DCS}$	55	56	$\overline{OE}$
A7	57	58	A8
A9	59	60	A10
A11	61	62	GND
A12	63	64	A13
A14	65	66	A15
A16	67	68	A17
$\overline{TCS}$	69	70	T0
GND	71	72	T1
T2	73	74	T3
T4	75	76	T5
T6	77	78	T7
VCC	79	80	GND

drw 02

SIMM
TOP VIEW

NOTES:
1. For the IDT7MP6084 (1MB version), pins 67 and 68 are no connects for proper operation of the module. For the IDT7MP6074 (256KB version), pins 65, 66, 67 and 68 are no connects for proper operation of the module.
2. For package dimensions, please refer to the module drawings in the packaging section.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Commercial	0°C to +70°C	0V	5V ± 10%

tbl 05

PIN NAMES

I/O0-35	Data Inputs/Outputs
T0-7	Tag Inputs/Outputs
A0-17	Address Inputs
$\overline{DCS}$	Data Chip Select
$\overline{TCS}$	Tag Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground

tbl 01

CAPACITANCE

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN(D)	Input Capacitance (Data)	VIN = 0V	10	pF
CIN(A)	Input Capacitance (A_{1-15}, $\overline{OE}$, $\overline{TCS}$, $\overline{DCS}$)	VIN = 0V	10	pF
CIN(B)	Input Capacitance (A0, $\overline{WE}$)	VIN = 0V	100	pF
COUT	Output Capacitance	VOUT = 0V	10	pF

NOTE: tbl 03
1. This parameter is guaranteed by design, but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: tbl 04
1. VIL = -1.5V for pulse width less than 10ns.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating[1]	Value	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	–10 to +85	°C
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE: tbl 02
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

B

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	50MHz		75MHz		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI1}\|$	Input Leakage (except A0, $\overline{WE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	—	10	µA
$\|I_{LI2}\|$	Input Leakage (A0, $\overline{WE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	110	—	110	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	—	10	µA
I_{CC}	Operating Current	$\overline{CS}$ = V_{IL}; V_{CC} = Max., Outputs Open	—	2200	—	TBD	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	—	2.4	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	—	0.4	V

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

tbl 06

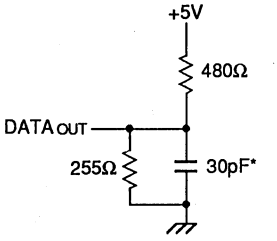


Figure 1. Output Load

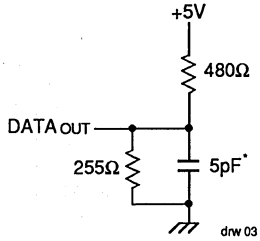


Figure 2. Output Load (for t_{OLZ} and t_{OHZ})

* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

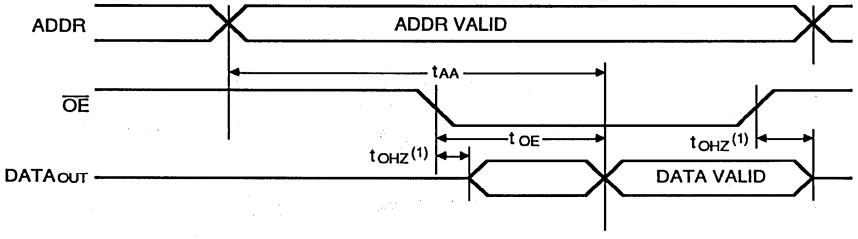
(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP6074S50 7MP6084S50 7MP6094S50		7MP6074S75 7MP6084S75 7MP6094S75		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{AA}	Address Access Time	—	25	—	15	ns
t_{OE}	Output Enable to Output Valid	—	25	—	15	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	20	—	13	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	0	—	0	—	ns
WRITE CYCLE						
t_{AW}	Address Valid to End of Write	25	—	15	—	ns
t_{WP}	Write Pulse Width	20	—	10	—	ns
t_{DW}	Data Valid to End of Write	17	—	8	—	ns
t_{DH}	Data Hold Time	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design but not tested.

tbl 09

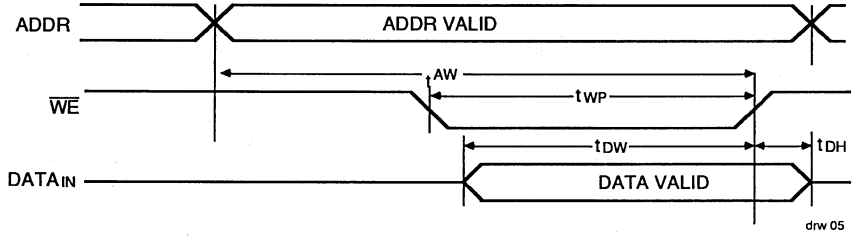
TIMING WAVEFORM OF READ CYCLE(1)



drw 04

NOTES:
1. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE

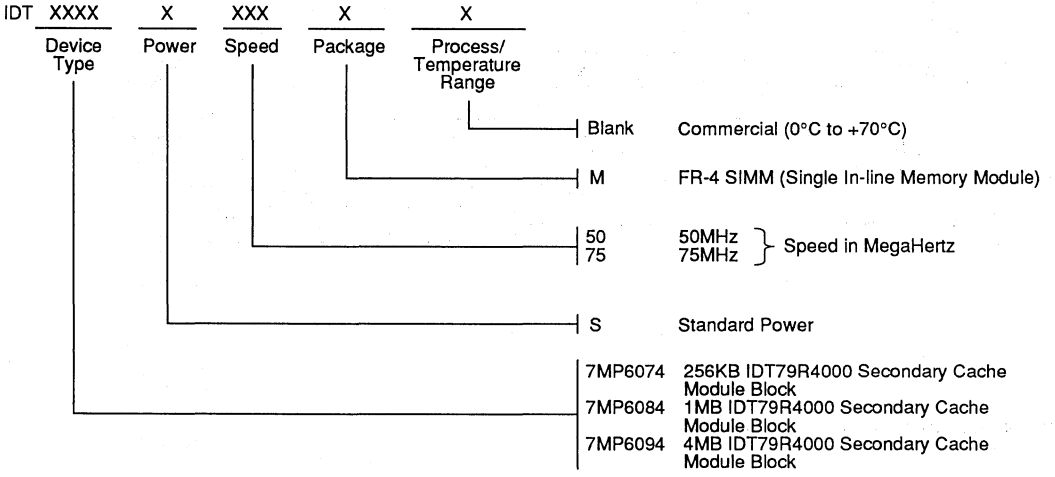


drw 05

B

drw 07

ORDERING INFORMATION



drw 08

Integrated Device Technology, Inc.

128K/ 256K BYTE CMOS SECONDARY CACHE MODULE FOR THE INTEL™ i486™

PRELIMINARY
IDT7MP6085
IDT7MP6087

FEATURES:

- 128K/ 256K byte pin compatible secondary cache modules
- Ideal for use with Chips and Technologies M/PAX™ multiprocessor chipset
- Uses the IDT71589 32K x 9 CacheRAM™ with burst counter and self-timed write
- Matches all timing and signals of the i486 processor
- Operates with i486 speeds of up to 50MHz
- 80 lead FR-4 SIMM (Single-in-Line Memory Module)
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible

DESCRIPTION:

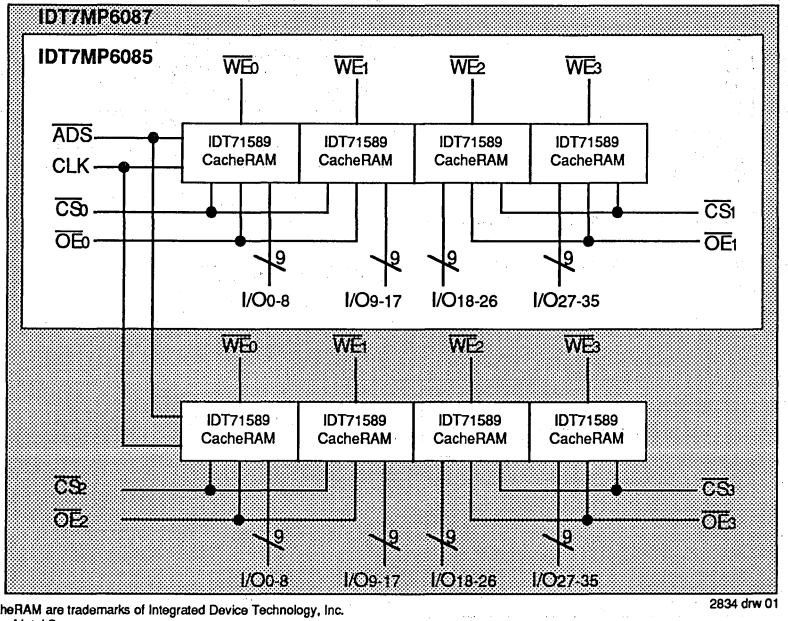
The IDT7MP6085 and the IDT7MP6087 are pin compatible secondary cache modules. The IDT7MP6085 is a 128K byte cache and the IDT7MP6087 is a 256K byte cache. The IDT7MP6087 uses eight IDT71589 32K x 9 CacheRAMs in plastic surface mount packages mounted on both sides of a multilayer epoxy laminate (FR-4) substrate with gold-plated lead fingers while the IDT7MP6085 uses four IDT71589s on one side of the same substrate. Extremely high speeds are achieved using IDT's high performance, high reliability CEMOS™ technology. This module is designed to facilitate the implementation of the highest performance secondary caches for the i486 and is ideal for designs with Chips and Technologies M/PAX™ multiprocessor chipset.

The IDT7MP6085 and IDT7MP6087 RAMs contain a full set of write data and address registers. These registers are combined with the internal write abort logic to allow the processor to generate a self-timed write based upon a decision which can be left until the end of the write cycle.

An internal burst address counter accepts the first cycle address from the processor and then cycles through the adjacent four locations using the i486's burst refill sequence on appropriate rising edges of the system clock.

The SIMM package configuration allows 80 leads to be placed on a package 4.65 inches long by 0.56 inches tall. The IDT7MP6085 is 0.21 inches thick, and the IDT7MP6087 is 0.35 inches thick. The IDT7MP6085 and IDT7MP6087 are available to interface with a 50MHz i486. All inputs and outputs of the IDT7MP6085 and IDT7MP6087 are TTL compatible and operate from a single 5V power supply.

FUNCTIONAL BLOCK DIAGRAM



2834 drw 01

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Intel and i486 are trademarks of Intel Corp.
M/PAX is a trademark of Chips and Technologies, Inc.

PIN CONFIGURATION[1, 2]

GND	1	2	GND
Vcc	3	4	I/O0
I/O1	5	6	I/O2
I/O3	7	8	I/O4
I/O5	9	10	I/O6
I/O7	11	12	I/O8
$\overline{WE_0}$	13	14	GND
$\overline{WE_1}$	15	16	I/O9
I/O10	17	18	I/O11
I/O12	19	20	I/O13
I/O14	21	22	I/O15
I/O16	23	24	I/O17
GND	25	26	$\overline{CS_0}$
$\overline{CS_2}$	27	28	$\overline{OE_0}$
$\overline{OE_2}$	29	30	A0
A1	31	32	A2
A3	33	34	A4
A5	35	36	A6
A7	37	38	$\overline{ADS}$
GND	39	40	Vcc
Vcc	41	42	GND
CLK	43	44	A8
A9	45	46	A10
A11	47	48	A12
A13	49	50	A14
Vcc	51	52	$\overline{CS_1}$
$\overline{CS_3}$	53	54	$\overline{OE_1}$
$\overline{OE_3}$	55	56	GND
I/O18	57	58	I/O19
I/O20	59	60	I/O21
I/O22	61	62	I/O23
I/O24	63	64	I/O25
I/O26	65	66	$\overline{WE_2}$
GND	67	68	$\overline{WE_3}$
I/O27	69	70	I/O28
I/O29	71	72	I/O30
I/O31	73	74	I/O32
I/O33	75	76	I/O34
I/O35	77	78	Vcc
GND	79	80	GND

2834 drw 02

SIMM
TOP VIEW

NOTES:

1. For the IDT7MP6085 (128K byte) version, pins 27, 29, 53, 55 are no connects.
2. For module dimensions, please refer to the module drawings in the packaging section.

PIN NAMES

A0–A14	Address Inputs
I/O0–I/O35	Data Input/Output
$\overline{CS_{0\text{-}3}}$	Word Chip Select/Count Enable
$\overline{WE_{0\text{-}3}}$	Byte Write Enables
$\overline{OE_{0\text{-}3}}$	Word Output Enables
$\overline{ADS}$	Address Status
CLK	System Clock
GND	Ground
Vcc	Power

2834 tbl 01

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Value	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	–10 to +85	°C
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE: 2834 tbl 03

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2834 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0.0	V
VIH	Input High Votage	2.2	—	6.0	V
VIL	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 2834 tbl 05

1. VIL = –3.0V for pulse width less than 5ns.

CAPACITANCE[1]

(TA = +25°C, f = 1.0 MHz)

Symbol	Parameter[1]	Condition	Max.	Unit
CIN	Input Capacitance ($\overline{CS}$, $\overline{OE}$, $\overline{WE}$)	VIN = 0V	20	pF
CIN	Input Capacitance (Address, CLK, $\overline{ADS}$)	VIN = 0V	70[2]	pF
CI/O	I/O Capacitance	VOUT = 0V	20[3]	pF

NOTE: 2834 tbl 09

1. This parameter is determined by device characterization but is not production tested and applies to both the IDT7MP6085 and IDT7MP6087 unless otherwise noted.
2. Specification for IDT7MP6085 is 42 pF.
3. Specification for IDT7MP6085 is 13pF.

TRUTH TABLE[1]

CLK	Previous $\overline{ADS}$	$\overline{ADS}$	Address	$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O	Function
↑	H	L	Valid Input	X	X	—	—	Preset Address Counter
↑	X	H	—	—	—	—	—	Ignore External Address Pins
↑	L	X	—	—	—	—	—	Ignore External Address Pins
↑	X	H	—	—	L	—	—	Sequence Address Counter
↑	L	X	—	—	L	—	—	Sequence Address Counter
↑	X	H	—	—	H	—	—	Suspend Address Sequencing
↑	L	X	—	—	H	—	—	Suspend Address Sequencing
—	—	—	—	—	—	H	Hi-Z	Outputs Disabled
—	—	—	—	H	—	L	$DATA_{OUT}$	Read
↑	X	H	—	L	L	H	$DATA_{IN}$	Write
↑	L	X	—	L	L	H	$DATA_{IN}$	Write
—	—	—	—	L	L	L	—	Not Allowed

NOTE:
1. H = HIGH, L = LOW, X = Don't Care, "–" = Unrelated, Hi-Z = High Impedance.

2834 tbl 11

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to 70°C)

Symbol	Parameter	Test Condition	Min.	Max.[1]	Unit
$\|I_{LI}\|$	Input Leakage Current (Address, CLK, $\overline{ADS}$)	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	80[2]	µA
$\|I_{LI}\|$	Input Leakage Current ($\overline{CS}$, $\overline{OE}$)	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	20	µA
$\|I_{LI}\|$	Input Leakage Current (Data, $\overline{WE}$)	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	20[3]	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	—	20[3]	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

NOTES:
1. Specifications apply to both the IDT7MP6085 and IDT7MP6087 unless otherwise noted.
2. Specification for IDT7MP6085 is 40µA.
3. Specification for IDT7MP6085 is 10µA.

B

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, T_A = 0°C to 70°C)

Symbol	Parameter	Test Condition	IDT7MP6085		IDT7MP6087		Unit
			50MHz[1]	25,33,40MHz	50MHz[1]	25,33,40MHz	
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ ≤ V_{IL} Outputs Open V_{CC} = Max., f = 0[2]	—	520	—	1040	mA
I_{CC2}	Dynamic Operating Current	CS ≤ V_{IL} Outputs Open V_{CC} = Max., f = f_{MAX}[2]	1050	960	2100	1920	mA

NOTES:
1. Preliminary specification only.
2. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.

2834 tbl 07

FUNCTIONAL DESCRIPTION

The IDT7MP6085 and the IDT7MP6087 are based on the IDT71589 CacheRAM with internal edge-triggered registers dedicated to support the Intel i486 CPU. These registers support the fastest system designs and allow a 128K byte or larger cache to be designed to consume the smallest number of chips, the lowest power and board space, and allow the designer to avoid the use of expensive high-speed cache-tag RAMs and PLDs.

The internal registers are designed to support two high speed functions: Burst read cycles and a late-abort self-timed write cycle.

Burst read cycles are accomplished through the assertion of the $\overline{ADS}$ signal with a valid address input during the rising edge of the clock input. This address will be used to access the data in the CacheRAM module during the next clock cycle, and data will be output during the following three cycles in accordance with the i486's burst refill sequence (i.e., during the next cycle the address LSB is inverted, then the second LSB is inverted as the LSB is restored to its original value, etc.). Since the CacheRAM contains this counter internally, the critical clock-to-data time of even the fastest CPU speeds can be met by using a slower RAM module speed grade without resorting to chip-intensive interleaving schemes. Should the $\overline{ADS}$ signal be sampled as valid after having been sampled as invalid, any bursting in process will be reinitialized to the new address, and a new burst cycle will be started. The burst counter wraps around at the end of the sequence and continues to count until stopped by the $\overline{ADS}$ or $\overline{CS}$ inputs. A fast copy-back scheme can harness this capability by reading, then writing the four burst addresses within a single burst cycle.

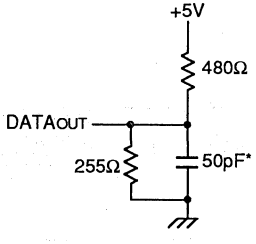
The self-timed write cycle significantly eases the timing of the address and data inputs during a write cycle, and allows the write/don't write decision to be postponed until the very end of the second cycle of a write cycle. During a write cycle, the address will be strobed into the address register during the first rising edge of the clock after the $\overline{ADS}$ input becomes valid. Data is sampled into the data input register during the next cycle's rising edge, as is the write enable input. If a write has been enabled the data will be written from the address and input data registers into the CacheRAM module during the second (low) phase of the clock of that cycle.

A chip select pin is provided to give control over interruption of write cycles and burst read cycles. When the $\overline{CS}$ input is used to interrupt a burst cycle, it operates as a synchronous input to the burst counter. A low level must be present on the chip select input and must satisfy data set-up and hold times in order for the counter to progress to its next state. To stop the counter at its current state, the chip select input must be taken high, and must stay high long enough to satisfy the CacheRAM module's data set-up and hold times. The $\overline{CS}$ pin also is used as an auxiliary to the $\overline{WE}$ inputs. Writes can only be accomplished if both $\overline{CS}$ and $\overline{WE}$ are simultaneously sampled active.

AC TEST CONDITIONS

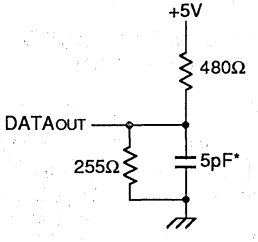
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2834 tbl 08



2834 drw 03

Figure 1. Output Load



2834 drw 04

Figure 1. Output Load (for t_{OHZ}, t_{CHZ}, t_{OLZ} and t_{CLZ})

*including scope and jig

AC ELECTRICAL CHARACTERISTICS

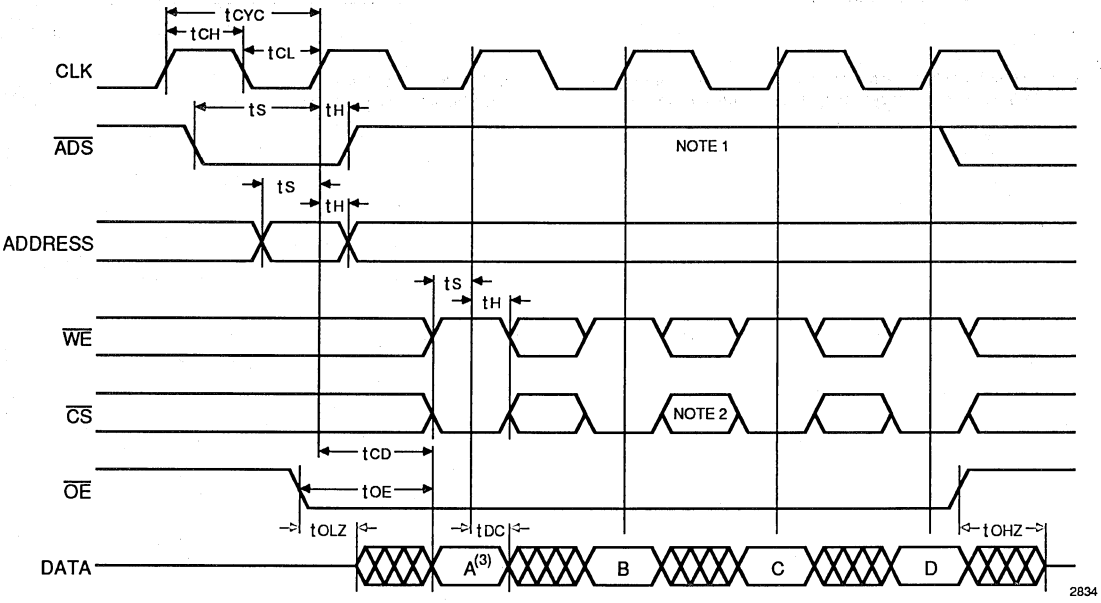
(V_{CC} = 5.0V ± 10%, T_A = 0° to +70°C)

Symbol	Name	50MHz[1]		40MHz		33MHz		25MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	20	—	25	—	30	—	40	—	ns
t_{CH}	Clock Pulse High	8	—	10	—	11	—	14	—	ns
t_{CL}	Clock Pulse Low	8	—	10	—	11	—	14	—	ns
t_{S1}	Set-up Time ($\overline{ADS}$, $\overline{WE}$, $\overline{CS}$)	4	—	4	—	4	—	5	—	ns
t_{S2}	Set-up Time (Address, Input Data)	5	—	5	—	5	—	6	—	ns
t_{H1}	Hold Time ($\overline{CS}\downarrow$ Input Data)	1	—	1	—	1	—	1	—	ns
t_{H2}	Hold Time ($\overline{CS}\uparrow$, $\overline{WE}$, Address)	2	—	2	—	2	—	2	—	ns
t_{ADSH}	Hold Time ($\overline{ADS}$)	3	—	3	—	3	—	3	—	ns
t_{CD}	Clock to Data Valid	—	14	—	19	—	24	—	34	ns
t_{DC}	Data Valid After Clock	3	—	4	—	4	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	7	—	8	—	9	—	10	ns
t_{OLZ}	Output Enable to Output in Lo-Z[2,3]	2	—	2	—	2	—	2	—	ns
t_{OHZ}	Output Disable to Output in Hi-Z[2,3]	—	7	—	8	—	9	—	10	ns

NOTES:
2834 tbl 10

1. Preliminary specifications only.
2. Transition is measured ±200mV from low or high impedance voltage with load (See AC Test Conditions, Figure 2).
3. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF BURST READ CYCLE



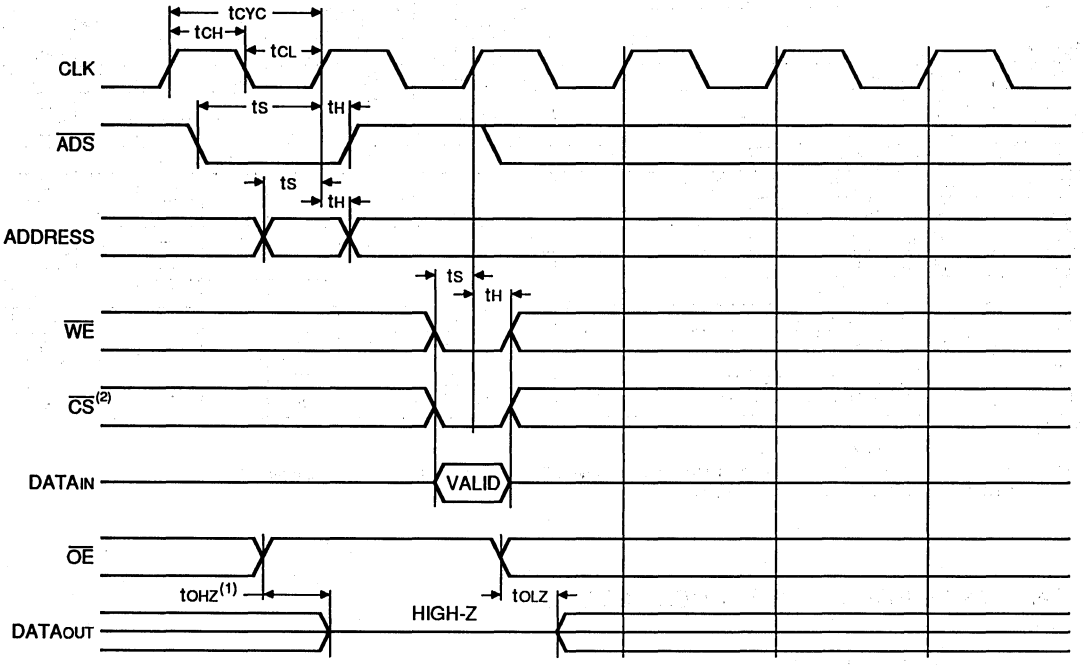
2834 drw 05

NOTES:

1. If $\overline{ADS}$ goes low during a burst cycle, a new address will be loaded and another burst cycle will be started.
2. If $\overline{CS}$ is taken inactive during a burst read cycle, the burst counter will discontinue counting until $\overline{CS}$ input again goes active. The timing of the $\overline{CS}$ input for this control of the burst counter must satisfy setup and hold parameters t_S and t_H.
3. A-Data from input address
   B-Data from input address except A_0 is now $\overline{A}_0$.
   C-Data from input address except A_1 is now $\overline{A}_1$.
   D-Data from input address except A_0 and A_1 are now $\overline{A}_0$ and $\overline{A}_1$.

B

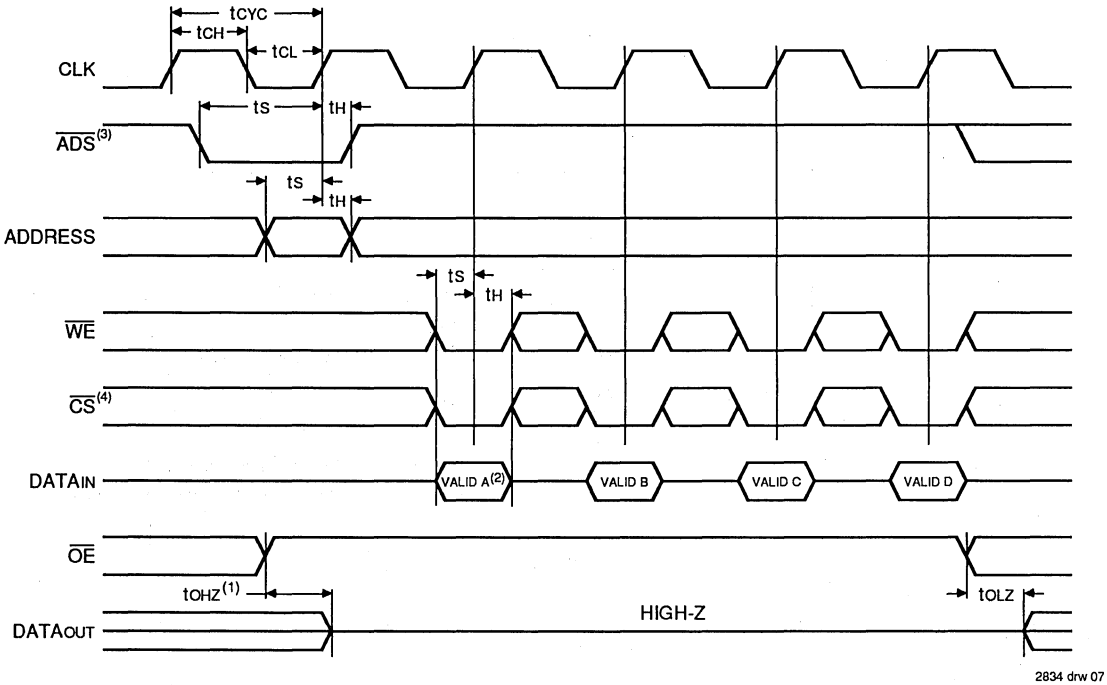
TIMING WAVEFORM OF WRITE CYCLE



2834 drw 06

NOTES:
1. $\overline{OE}$ Must be taken inactive at least as long as tOHZ + ts before the second rising clock edge of write cycle.
2. $\overline{CS}$ timing is the same as any synchronous signal when used to block writes or to stop the burst count sequence.

TIMING WAVEFORM OF BURST WRITE CYCLE

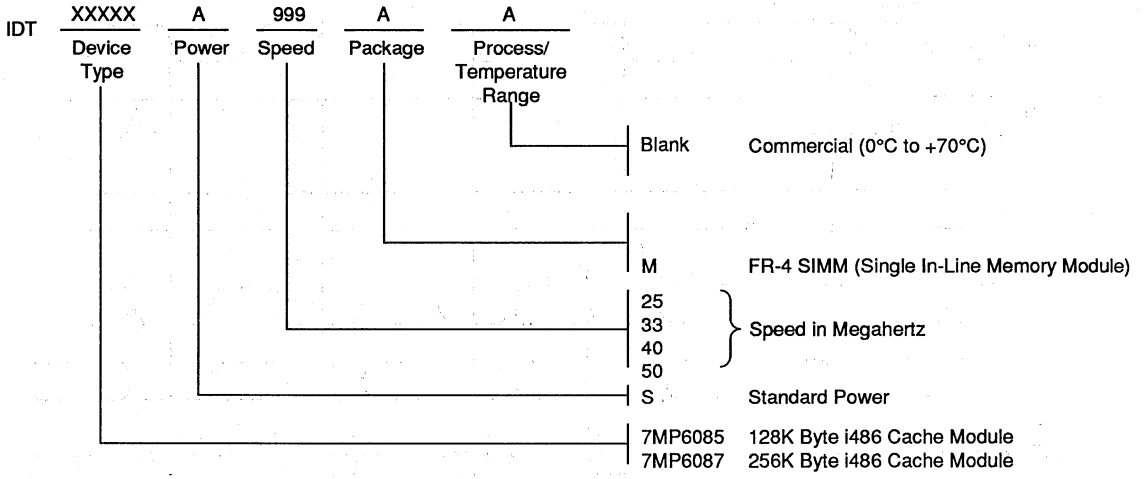


2834 drw 07

NOTES:
1. $\overline{OE}$ Must be taken inactive at least as long as t_{OHZ} + ts before the second rising clock edge of write cycle.
2. A-Data to be written to original input address.
   B-Data to be written to original input address except A_0 is now $\overline{A}_0$.
   C-Data to be written to original input address except A_1 is now $\overline{A}_1$.
   D-Data to be written to original input address except A_0 and A_1 are now $\overline{A}_0$ and $\overline{A}_1$.
3. If $\overline{ADS}$ goes low during a burst cycle, a new address will be loaded, and another burst cycle will be started.
4. If $\overline{CS}$ is taken inactive during a burst write cycle the burst counter will discontinue counting until the $\overline{CS}$ input again goes active. The timing of the $\overline{CS}$ input for this control of the burst counter must satisfy setup and hold parameters ts and t_H. $\overline{CS}$ timing is the same as any synchronous signal when used to block writes or to stop the burst count sequence.

B

ORDERING INFORMATION



2834 drw 11

Integrated Device Technology, Inc.

128K BYTE CMOS SECONDARY CACHE MODULE FOR THE INTEL™ i486™

PRELIMINARY
IDT7MP6086

FEATURES:

- 128K byte direct mapped secondary cache module
- Uses the IDT71589 32K x 9 CacheRAM™ with burst counter and self-timed write
- Matches all timing and signals of the i486 processor
- Operates with i486 speeds of up to 50MHz
- 72 lead FR-4 SIMM (Single-in-Line Memory Module)
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible

DESCRIPTION:

The IDT7MP6086, a 128K byte direct mapped secondary cache module, uses 4 IDT71589 32K x 9 CacheRAMs in plastic surface mount packages mounted on a multilayer epoxy laminate (FR-4) substrate with gold-plated leads. Extremely high speeds are achieved using IDT's high performance, high reliability CEMOS™ technology. This module is designed to facilitate the implementation of the highest performance secondary caches for the i486 architecture while using low speed logic devices and consuming the minimum board space.

The IDT7MP6086 data RAMs contain a full set of write data and address registers. These registers are combined with the internal write abort logic to allow the processor to generate a self-timed write based upon a decision which can be left until the end of the write cycle.

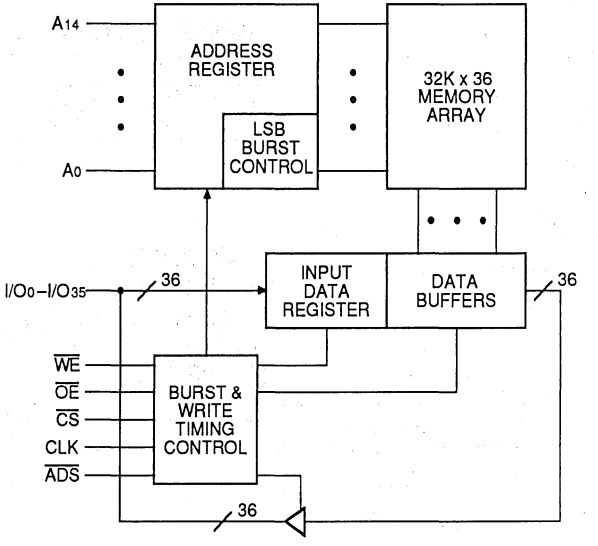
An internal burst address counter accepts the first cycle address from the processor and then cycles through the adjacent four locations using the i486's burst refill sequence on appropriate rising edges of the system clock.

Three program identification pins are provided so that the system can uniquely identify the IDT7MP6086.

Note that individual parity bits are grouped with their respective bytes, not all at the end.

The SIMM package configuration allows 72 leads to be placed on a package 4.25 inches long, 0.55 inches tall and 0.25 inches thick. The IDT7MP6086 is available to interface with a 50MHz i486. All inputs and outputs of the IDT7MP6086 are TTL compatible and operate from a single 5V power supply.

FUNCTIONAL BLOCK DIAGRAM



B

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Intel and i486 are trademarks of Intel Corp.

PIN CONFIGURATION[1, 2]

		1	GND
GND	2	3	VCC
I/O0	4	5	I/O1
I/O2	6	7	I/O3
I/O4	8	9	I/O5
I/O6	10	11	I/O7
I/O8	12	13	$\overline{WE0}$
$\overline{WE1}$	14	15	I/O9
I/O10	16	17	I/O11
GND	18	19	I/O12
I/O13	20	21	I/O14
I/O15	22	23	I/O16
I/O17	24	25	A0
A1	26	27	A2
A3	28	29	A4
A5	30	31	A6
A7	32	33	A8
$\overline{ADS}$	34	35	CLK
VCC	36		
$\overline{CS}$	38	37	GND
A9	40	39	$\overline{OE}$
A11	42	41	A10
A13	44	43	A12
I/O18	46	45	A14
I/O20	48	47	I/O19
I/O22	50	49	I/O21
I/O24	52	51	I/O23
I/O26	54	53	I/O25
$\overline{WE2}$	56	55	GND
I/O27	58	57	$\overline{WE3}$
I/O29	60	59	I/O28
I/O31	62	61	I/O30
I/O33	64	63	I/O32
I/O35	66	65	I/O34
PD1	68	67	PD0
VCC	70	69	PD2
GND	72	71	GND

drw 02

SIMM
TOP VIEW

NOTE:

1. For module dimensions, please refer to the module drawings in the packaging section.
2. Please consult the factory regarding program identification pins.

PIN NAMES

A0–A14	Address Inputs
I/O0–I/O35	Data Input/Output
$\overline{CS}$	Chip Select/Count Enable
$\overline{WE0-3}$	Byte Write Enables
$\overline{OE}$	Output Enable
$\overline{ADS}$	Address Status
CLK	System Clock
PD0-2	Program Identification
GND	Ground
VCC	Power

tbl 01

CAPACITANCE

(T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter[1]	Condition	Max.	Unit
C_{IN}	Input Capacitance (Data)	V_{IN} = 0V	13	pF
C_{IN}	Input Capacitance (Address & Control)	V_{IN} = 0V	42	pF
$C_{I/O}$	Output Capacitance	V_{OUT} = 0V	13	pF

NOTE:

1. This parameter is guaranteed by design but not tested.

tbl 09

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:

tbl 03

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0.0	V
V_{IH}	Input High Votage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE:

1. V_{IL} = –3.0V for pulse width less than 5ns.

tbl 05

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, T_A = 0°c TO + 70°c)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current (Address & Contol)	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	40	µA
$\|I_{LI}\|$	Input Leakage Current (Data)	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

tbl 06

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, T_A = 0°c to +70°c)

			7MP6086xxM				
Symbol	Parameter	Test Condition	50 MHz (1)	40 MHz	33 MHz	25 MHz	Unit
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0(2)	—	520	520	520	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	1150	960	880	800	mA

tbl 07

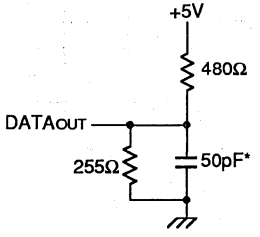
NOTES:
1. Preliminary specification only.
2. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.

B

AC TEST CONDITIONS

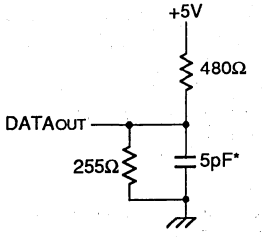
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

Tbl 08



drw 03

Figure 1. Output Load



drw 04

Figure 1. Output Load (for t_{OHZ}, t_{CHZ}, t_{OLZ} and t_{CLZ})

*including scope and jig

FUNCTIONAL DESCRIPTION

The IDT7MP6086 is an extremely fast 128K byte CMOS static CacheRAM module with internal edge-triggered registers dedicated to the support of the Intel i486 CPU. These registers support the fastest systems and allow a 128K byte or larger cache to be designed to consume the smallest number of chips, the lowest power and board space, and allow the designer to avoid the use of expensive high-speed cache-tag RAMs and PLDs.

The internal registers are designed to support two high speed functions: Burst read cycles, and a late-abort self-timed write cycle.

Burst read cycles are accomplished through the assertion of the $\overline{ADS}$ signal with a valid address input during the rising edge of the clock input. This address will be used to access the data in the CacheRAM module during the next clock cycle, and data will be output during the following three cycles in accordance with the i486's burst refill sequence (i.e., during the next cycle the address' LSB is inverted, then the second LSB is inverted as the LSB is restored to its original value, etc.). Since the CacheRAM contains this counter internally, the critical clock-to-data time of even the fastest CPU speeds can be met by using a slower RAM module speed grade without resorting to chip-intensive interleaving schemes. Should the $\overline{ADS}$ signal be sampled as valid after having been sampled as invalid, any bursting in process will be reinitialized to the new address, and a new burst cycle will be started. The burst counter wraps around at the end of the sequence and continues to count until stopped by the $\overline{ADS}$ or $\overline{CS}$ inputs. A fast copy-back scheme can harness this capability by reading, then writing the four burst addresses within a single burst cycle.

The self-timed write cycle significantly eases the timing of the address and data inputs during a write cycle, and allows the write/don't write decision to be postponed until the very end of the second cycle of a write cycle. During a write cycle, the address will be strobed into the address register during the first rising edge of the clock after the $\overline{ADS}$ input becomes valid. Data is sampled into the data input register during the next cycle's rising edge, as is the write enable input. If a write has been enabled the data will be written from the address and input data registers into the CacheRAM module during the second (low) phase of the clock of that cycle.

A chip select pin is provided to give control over interruption of write cycles and burst read cycles. When the $\overline{CS}$ input is used to interrupt a burst cycle, it operates as a synchronous input to the burst counter. A low level must be present on the chip select input and must satisfy data set-up and hold times in order for the counter to progress to its next state. To stop the counter at its current state, the chip select input must be taken high, and must stay high long enough to satisfy the CacheRAM module's data set-up and hold times. The $\overline{CS}$ pin also is used as an auxiliary to the $\overline{WE}$ inputs. Writes can only be accomplished if both $\overline{CS}$ and $\overline{WE}$ are simultaneously sampled active.

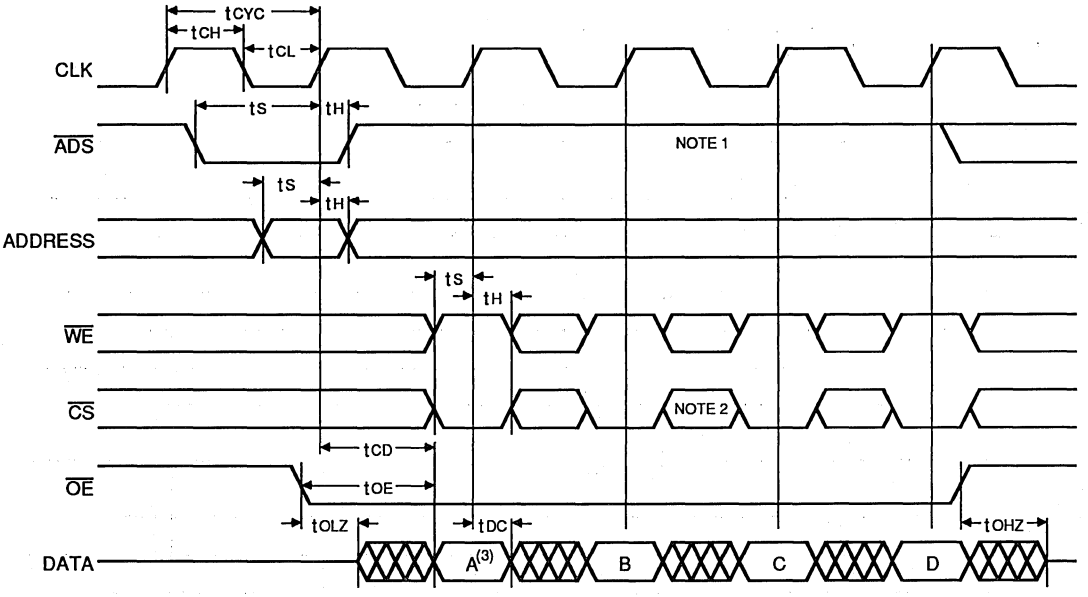
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, T_A = 0° to +70°C)

		7MP6086xxM								
		50 MHz[1]		40 MHz		33 MHz		25 MHz		
Symbol	Name	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{CYC}	Clock Cycle Time	20	—	25	—	30	—	40	—	ns
t_{CH}	Clock Pulse High	8	—	10	—	11	—	14	—	ns
t_{CL}	Clock Pulse Low	8	—	10	—	11	—	14	—	ns
t_{S1}	Set-up Time ($\overline{ADS}$, $\overline{WE}$, $\overline{CS}$)	4	—	4	—	4	—	5	—	ns
t_{S2}	Set-up Time (Address, Input Data)	5	—	5	—	5	—	6	—	ns
t_{H1}	Hold Time ($\overline{CS}\downarrow$ Input Data)	1	—	1	—	1	—	1	—	ns
t_{H2}	Hold Time ($\overline{CS}\uparrow$, $\overline{WE}$, Address)	2	—	2	—	2	—	2	—	ns
t_{ADSH}	Hold Time ($\overline{ADS}$)	3	—	3	—	3	—	3	—	ns
t_{CD}	Clock to Data Valid	—	14	—	19	—	24	—	34	ns
t_{DC}	Data Valid After Clock	3	—	4	—	4	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	7	—	8	—	9	—	10	ns
t_{OLZ}	Output Enable to Output in Lo-Z[2,3]	2	—	2	—	2	—	2	—	ns
t_{OHZ}	Output Disable to Output in Hi-Z[2,3]	—	7	—	8	—	9	—	10	ns

NOTES: tbl 10

1. Preliminary specifications only.
2. Transition is measured ±200mV from low or high impedance voltage with load (Figure 2).
3. This parameter is guaranteed, but not tested.

TIMING WAVEFORM OF BURST READ CYCLE

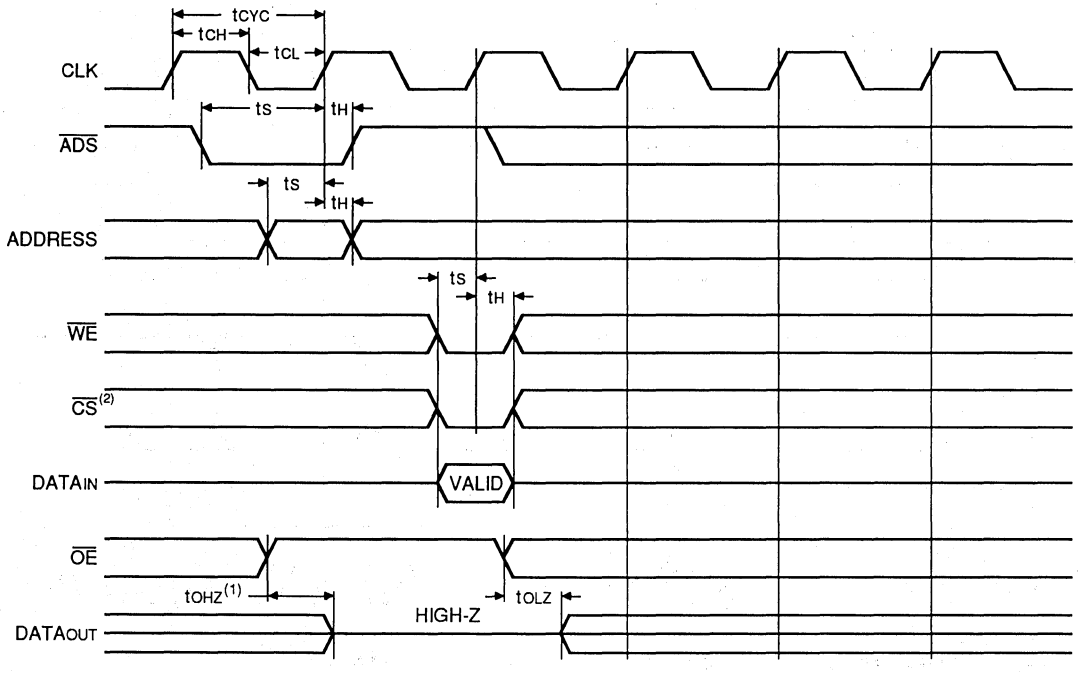


drw 05

NOTES:
1. If $\overline{ADS}$ goes low during a burst cycle, a new address will be loaded and another burst cycle will be started.
2. If $\overline{CS}$ is taken inactive during a burst read cycle, the burst counter will discontinue counting untll $\overline{CS}$ input again goes active. The timing of the $\overline{CS}$ input for this control of the burst counter must satisfy setup and hold parameters ts and tH.
3. A-Data from input address
   B-Data from input address except A_0 is now $\overline{A}_0$.
   C-Data from input address except A_1 is now $\overline{A}_1$.
   D-Data from input address except A_0 and A_1 are now $\overline{A}_0$ and $\overline{A}_1$.

B

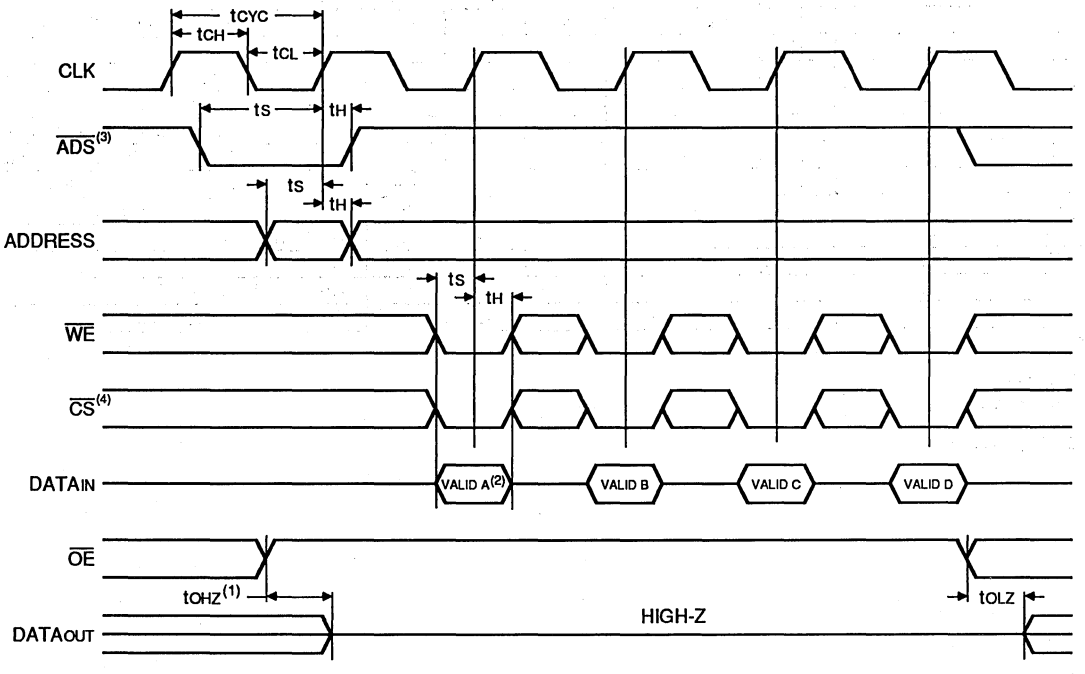
TIMING WAVEFORM OF WRITE CYCLE



drw 06

NOTES:
1. $\overline{OE}$ Must be taken inactive at least as long as t_{OHZ} + ts before the second rising clock edge of write cycle.
2. $\overline{CS}$ timing is the same as any synchronous signal when used to block writes or to stop the burst count sequence.

TIMING WAVEFORM OF BURST WRITE CYCLE



drw 07

NOTES:
1. $\overline{OE}$ Must be taken inactive at least as long as $t_{OHZ} + t_S$ before the second rising clock edge of write cycle.
2. A-Data to be written to original input address.
   B-Data to be written to original input address except A_0 is now $\overline{A}_0$.
   C-Data to be written to original input address except A_1 is now $\overline{A}_1$.
   D-Data to be written to original input address except A_0 and A_1 are now $\overline{A}_0$ and $\overline{A}_1$.
3. If $\overline{ADS}$ goes low during a burst cycle, a new address will be loaded, and another burst cycle will be started.
4. If $\overline{CS}$ is taken inactive during a burst write cycle the burst counter will discontinue counting until the $\overline{CS}$ input again goes active. The timing of the $\overline{CS}$ input for this control of the burst counter must satisfy setup and hold parameters t_S and t_H. $\overline{CS}$ timing is the same as any synchronous signal when used to block writes or to stop the burst count sequence.

B

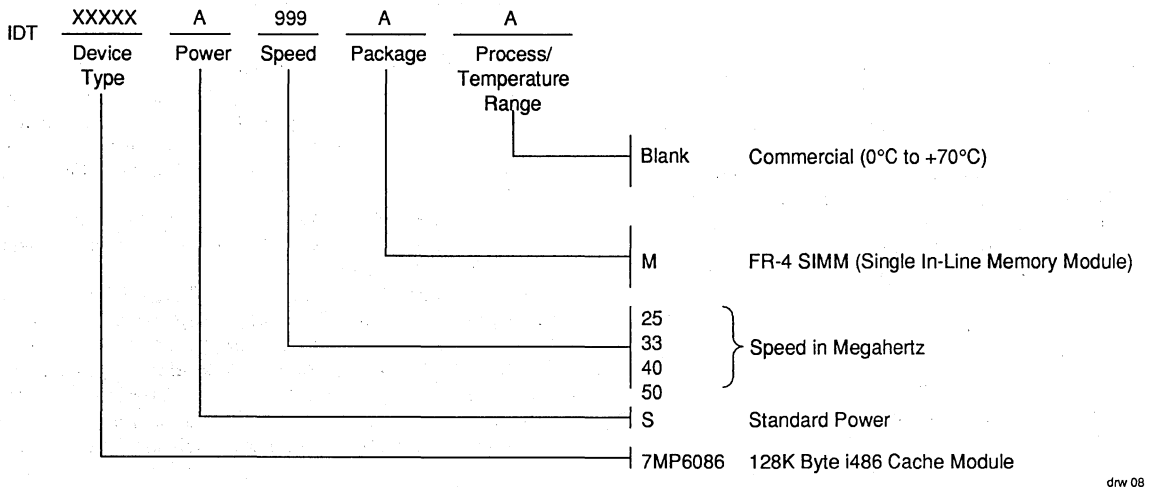
TRUTH TABLE

CLK	Previous $\overline{ADS}$	$\overline{ADS}$	Address	$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O	Function
↑	H	L	Valid Input	X	X	—	—	Preset Address Counter
↑	X	H	—	—	—	—	—	Ignore External Address Pins
↑	L	X	—	—	—	—	—	Ignore External Address Pins
↑	X	H	—	—	L	—	—	Sequence Address Counter
↑	L	X	—	—	L	—	—	Sequence Address Counter
↑	X	H	—	—	H	—	—	Suspend Address Sequencing
↑	L	X	—	—	H	—	—	Suspend Address Sequencing
—	—	—	—	—	—	H	Hi-Z	Outputs Disabled
—	—	—	—	H	—	L	$DATA_{OUT}$	Read
↑	X	H	—	L	L	H	$DATA_{IN}$	Write
↑	L	X	—	L	L	H	$DATA_{IN}$	Write
—	—	—	—	L	L	L	—	Not Allowed

tbl 11

NOTE:
H = HIGH
L = LOW
X = Don't Care
– = Unrelated
Hi-Z = High Impedance

ORDERING INFORMATION



drw 08

B

Integrated Device Technology, Inc.

FAST CMOS 32-BIT BUFFER/LINE DRIVER AND BIDIRECTIONAL TRANSCEIVER MODULES

PRELIMINARY
IDT7MP9244T/AT/CTZ
IDT7MP9245T/AT/CTZ

FEATURES:

- High density 32-bit FCT Logic modules
- Equivalent to FAST™ speed and drive
- Low profile module 75-pin ZIP (Zig-zag In-line vertical Package)
- Uses 70 mil pitch leads for maximum density
- Surface mount components on a multilayer epoxy laminate (FR-4) substrate
- True TTL input and output compatible
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
  - — I_{OL} = 64mA
- CMOS power levels (10mW typ. static)
- Single 5V (±5%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity

DESCRIPTION:

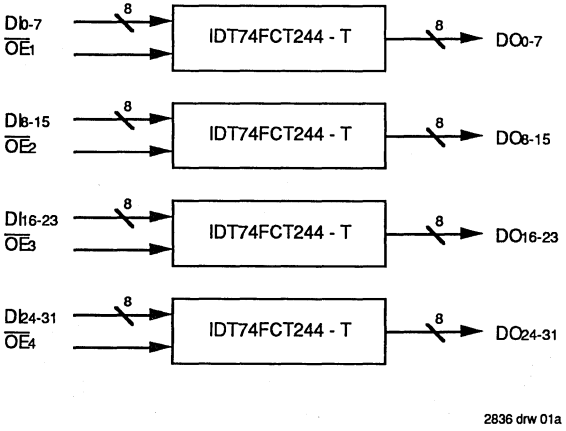
The IDT7MP9244T/AT/CTand IDT7MP9245T/AT/CT logic modules are designed to be employed as 32-bit memory and address drivers, clock drivers and bus-oriented transmitter/receivers which require maximum board packing density. The IDT FCT logic components are built using advanced CEMOS™, a dual metal CMOS technology.

The IDT7MP9244T/AT/CT has byte output enable control and the IDT7MP9245T/AT/CT has word output enable and transmit/receive control.

The IDT7MP9244T/AT/CT and IDT7MP9245T/AT/CT are packaged in a 75 pin ZIP (Zig-zag In-line vertical Package) module offering the optimum in packing density. The dual row (70 mil lead pitch) vertical configuration allows 75 pins to be placed on a package 2.65 inches long, 510 mils tall and only 180 mils thick, resulting in a three-fold density improvement over an equivalent monolithic though-hole implementation.

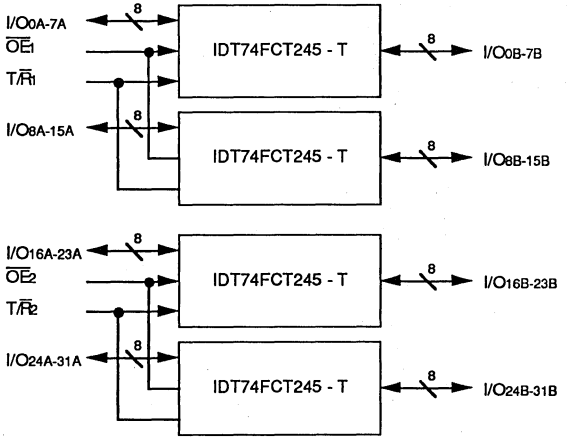
FUNCTIONAL BLOCK DIAGRAMS

IDT7MP9244



2836 drw 01a

IDT7MP9245



2836 drw 01b

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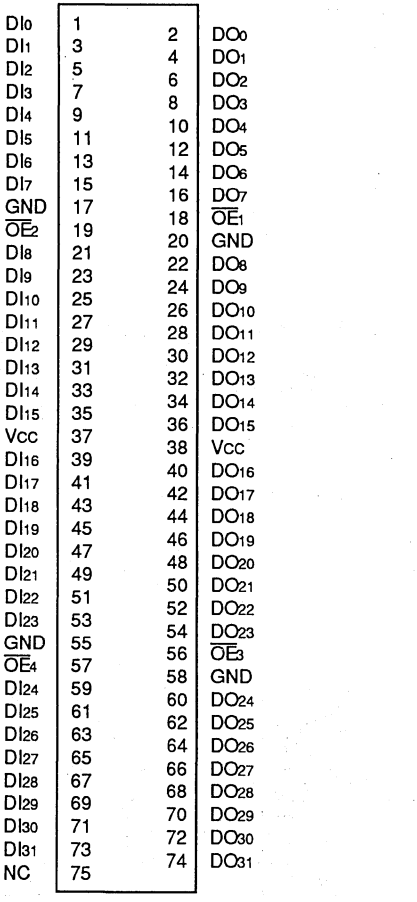
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATION[1]

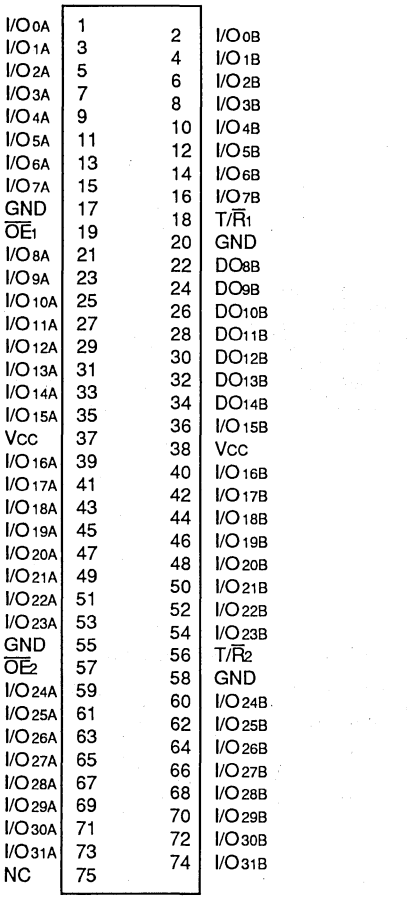
IDT7MP9244



ZIP
TOP VIEW

2836 drw 02a

IDT7MP9245



ZIP
TOP VIEW

2836 drw 02b

NOTE:
1. For package dimensions, please refer to the module drawings in the packaging section.

PIN DESCRIPTION - 7MP9244

Pin Names	Description
$\overline{OE}_1$- $\overline{OE}_4$	3–State Output Enable Inputs (Active LOW)
DI0-31	Inputs
DO0-31	Outputs

2836 tbl 04a

PIN DESCRIPTION - 7MP9245

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	3–State Output Enable Inputs (Active LOW)
T/$\overline{R}_1$, T/$\overline{R}_2$	Transmit/Receive Inputs
I/O0A-31A	Side A Inputs or 3-State Outputs
I/O0B-31B	Side BInputs or 3-State Outputs

2836 tbl 04b

B

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	-0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTES: 2836 tbl 01
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

FUNCTION TABLE[1]

7MP9244			7MP9245		
Inputs		Outputs	Inputs		
$\overline{OE}$	D	O	$\overline{OE}$	T/$\overline{R}$	Outputs
L	L	L	L	L	Bus I/OB Data to Bus I/OA
L	H	H	L	H	Bus I/OB Data to Bus I/OA
H	X	Z	H	X	High-Z State

NOTE: 2836 tbl 05
1. H = High Voltage Level
   X = Don't Care
   L = Low Voltage Level
   Z = High Impedance

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
$C_{I/O}$	Input Capacitance (I/O)	V_{IN} = 0V	15	pF
C_{CTRL}	Input Capacitance ($\overline{OE}$, T/$\overline{R}$)	V_{IN} = 0V	30	pF

NOTE: 2836 tbl 02
1. This parameter is guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS[4]

(T_A = 0°C to +70°C, Vcc = 5.0V ± 5%)

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	Vcc = Max.	Except I/O Pins	—	—	5	µA
		V_I = 2.7V	I/O Pins	—	—	15	
I_{IL}	Input LOW Current	Vcc = Max.	Except I/O Pins	—	—	–5	µA
		V_I = 0.5V	I/O Pins	—	—	-15	
I_{OZH}	High Impedance Output Current	Vcc = Max.	V_O= 2.7V	—	—	10	µA
I_{OZL}			V_O = 0.5V	—	—	–10	µA
I_I	Input HIGH Current	Vcc = Max., V_I = Vcc (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	Vcc = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	Vcc = Min.	I_{OH} = –8mA	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –15mA	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	—	0.3	0.55	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	Vcc = Max., V_{IN} = GND or Vcc		—	2.0	6.0	mA

NOTES: 2836 tbl 03
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Gross functional testing is performed on the IDT modules; power supply characteristics of the IDT modules are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS[7]

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = T/$\overline{R}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[5, 6]	V_{CC} = Max. Outputs Open fi =10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	3.5	8.5	mA
		50% Duty Cycle $\overline{OE}$ = T/$\overline{R}$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	3.8	9.5	
		V_{CC} = Max. Outputs Open fi = 2.5MHz	V_{IN} = V_{CC} V_{IN} = GND	—	12.8	26.0	
		50% Duty Cycle $\overline{OE}$ = T/$\overline{R}$ = GND 32 Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	20.8	58.0	

2836 tbl 06

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.
7. Gross functional testing is performed on the IDT modules; power supply characteristics of the IDT modules are guaranteed by design but not tested.

B

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR IDT7MP9244[1]

Symbol	Parameter	Condition[2]	7MP9244T		7MP9244AT		7MP9244CT		Unit
			Min.[3]	Max.	Min.[3]	Max.	Min.[3]	Max.	
tPLH tPHL	Propagation Delay DN to ON	CL = 50pF RL = 500Ω	1.5	6.5	1.5	4.8	1.5	4.1	ns
tPZH tPZL	Output Enable Time		1.5	8.0	1.5	6.2	1.5	5.8	ns
tPHZ tPLZ	Output Disable Time		1.5	7.0	1.5	5.6	1.5	5.2	ns

2836 tbl 07

NOTES:
1. Specifications are for the IDT74FCT244-T components used on the IDT7MP9244. Gross functional testing is performed on the IDT modules; switching characteristics of the IDT modules are guaranteed by design but not tested.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR IDT7MP9245[1]

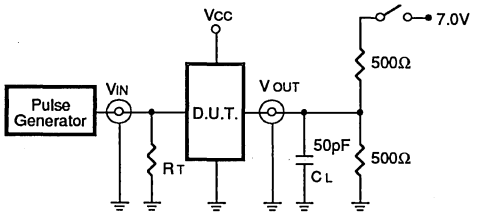
2836 tbl 07

Symbol	Parameter	Condition[2]	7MP9245T		7MP9245AT		7MP9245CT		Unit
			Min.[3]	Max.	Min.[3]	Max.	Min.[3]	Max.	
tPLH tPHL	Propagation Delay I/OA to I/OB, I/OB to I/OA	CL = 50pF RL = 500Ω	1.5	7.0	1.5	4.6	1.5	4.1	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to I/OA or I/OB		1.5	9.5	1.5	6.2	1.5	5.8	ns
tPZH tPZL	Output Disable Time $\overline{OE}$ to I/OA or I/OB		1.5	7.5	1.5	5.0	1.5	4.8	ns
tPZH tPZL	Output Enable Time T/$\overline{R}$ to I/OA or I/OB		1.5	9.5	1.5	6.2	1.5	5.8	ns
tPHZ tPLZ	Output Disable Time T/$\overline{R}$ to I/OA or I/OB		1.5	7.5	1.5	5.0	1.5	4.8	ns

2836 tbl 08

NOTES:
1. Specifications are for the IDT74FCT245-T components used on the IDT7MP9245. Gross functional testing is performed on the IDT modules; switching characteristics of the IDT modules are guaranteed by design but not tested.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS (FOR ALL OUTPUTS)



SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

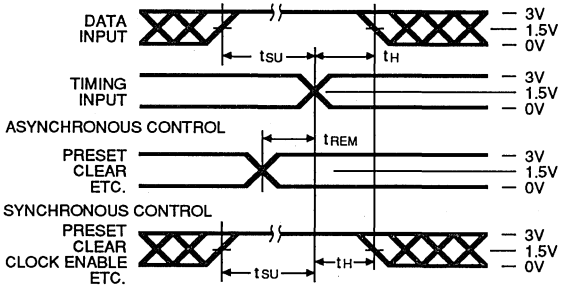
2836 tbl 09

DEFINITIONS:

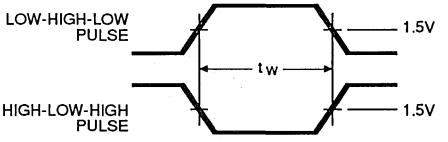
C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

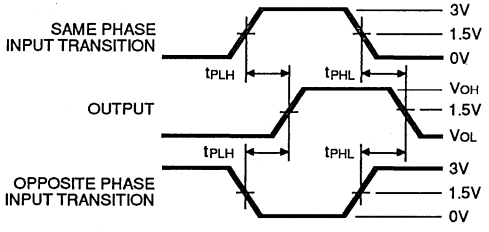
SET-UP, HOLD AND RELEASE TIMES



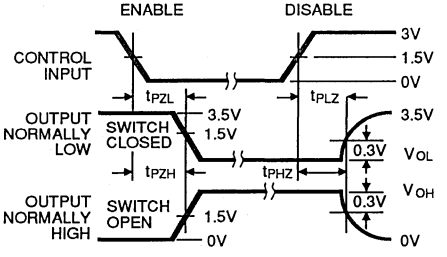
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

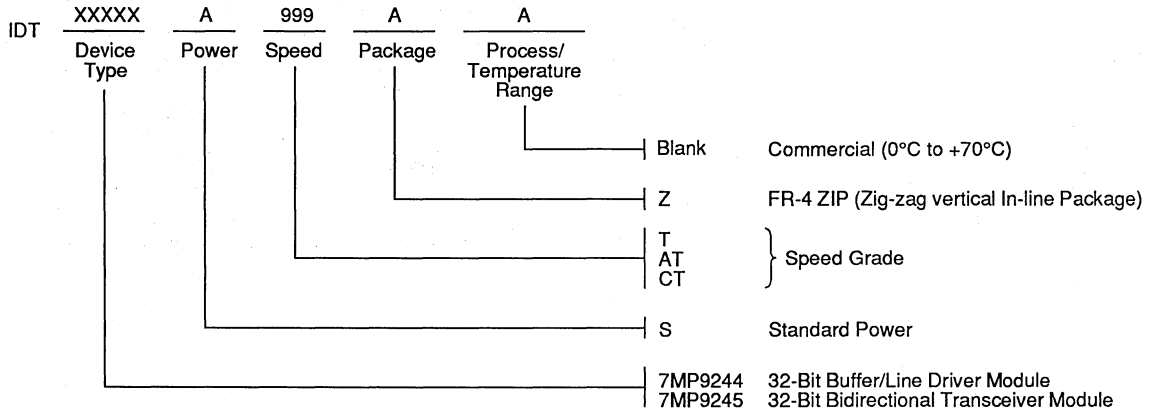


NOTES 2836 drw 10

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

B

ORDERING INFORMATION



2836 drw 11

FEATURES:

- High-density modules using high-speed CMOS SRAM, EPROM, and EEPROM components.
- Inter-changeable modules, with equivalent footprints, support a wide range of applications
- Fast access times:

SRAM:	30ns (max.) - military
	25ns (max.) - commercial
EEPROM:	95ns (max.) - military
	75ns (max.) - commercial
EPROM:	95ns (max.) - military
	40ns (max.) - commercial

- Low power CMOS operation
- Surface mounted LCC components on a co-fired ceramic substrate
- Offered in a 66-pin, ceramic HIP (Hex In-line Package) occupying only 1 sq. inch of board space
- Single 5V (± 10%) power supply
- Multiple ground pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

The Flexi-Pak family of modules are high-speed, high-density CMOS memory modules constructed on a multilayer co-fired ceramic substrate using either SRAM, EPROM, or EEPROM components in leadless chip carriers.

This family of IDT modules supports applications requiring stand alone static or programmable memory or those applications needing a combination of both. All module configurations in this family have equivalent footprints, allowing "plug-in compatibility" with each other (i.e. interchangeable), ideal for a wide range of prototype and debugging applications.

The Flexi-Pak family utilizes the fastest commercial grade and MIL-STD-883 Class B military grade components, giving you the highest performance available anywhere. CMOS technology offers a low-cost, low-power alternative to bipolar and fast NMOS memories.

All versions of the Flexi-Pak Module Family are offered in a 66-pin, ceramic HIP (Hex In-line Package). This HIP package is similar to a PGA and allows the designer to fit into 1 sq. inch of board space.

All IDT military modules are assembled with semiconductor components compliant with the latest revision of MIL-STD-883 Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

ORGANIZATIONS

SRAM: IDT7M4003 - 128K x 8, 64K x 16, 32K x 32
IDT7M4013 - 512K x 8, 256K x 16, 128K x 32

SRAM / EEPROM:

IDT7M7005 -	64K x 8 / 64K x 8
	64K x 8 / 32K x 16
	32K x 16 / 64K x 8
	32K x 16 / 32K x 16
IDT7M7025* -	64K x 8 / 256K x 8
	64K x 8 / 128K x 16
	32K x 16 / 256K x 8
	32K x 16 / 128K x 16
IDT7M7035* -	256K x 8 / 256K x 8
	256K x 8 / 128K x 16
	128K x 16 / 256K x 8
	128K x 16 / 128K x 16
IDT7M7045* -	256K x 8 / 64K x 8
	256K x 8 / 32K x 16
	128K x 16 / 64K x 8
	128K x 16 / 32K x 16

EEPROM: IDT7M7004 - 128K x 8, 64K x 16, 32K x 32
IDT7M7014*- 512K x 8, 256K x 16, 128K x 32

SRAM / EPROM:

IDT7M7012 -	64K x 8 / 64K x 8
	64K x 8 / 32K x 16
	32K x 16 / 64K x 8
	32K x 16 / 32K x 16
IDT7M7002 -	64K x 8 / 256K x 8
	64K x 8 / 128K x 16
	32K x 16 / 256K x 8
	32K x 16 / 128K x 16
IDT7M7022* -	256K x 8 / 256K x 8
	256K x 8 / 128K x 16
	128K x 16 / 256K x 8
	128K x 16 / 128K x 16
IDT7M7032* -	256K x 8 / 64K x 8
	256K x 8 / 32K x 16
	128K x 16 / 64K x 8
	128K x 16 / 32K x 16

*Please consult the factory for availability of these versions.

B

Integrated Device Technology, Inc.

WIDTH EXPANSION OF SyncFIFOs™ (CLOCKED FIFOS)

APPLICATION NOTE AN-83

by Rob De Voto

INTRODUCTION

The performance requirements of today's systems are continually reaching to new heights. In response to needs for higher performance, IDT has introduced a family of First-In-First-Out (FIFO) buffers which are ideally suited for system speeds of 25MHz or greater. The synchronous interface of this family of Clocked FIFOs offers several advantages over the traditional IDT720X Series of FIFOs:

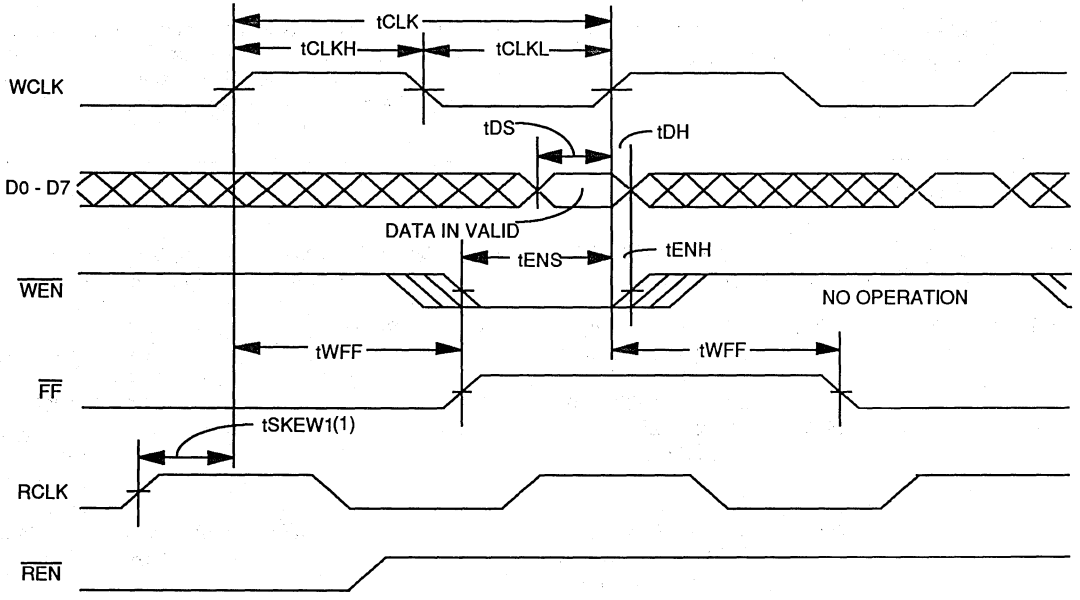
a) speed (data transfer rates of up to 67MHz);
b) free running clock control simplifies system design.

The Clocked FIFO family includes x8-bit, x9-bit, and x18-bit parts in a wide range of densities. To accommodate system requirements beyond this product family, the FIFOs can be easily expanded in width and depth. The purpose of this Application Note is to discuss design considerations and recommendations when designing with SyncFIFOs (Clocked FIFOs) in Width Expansion.

SKEW TIMING

The inherent advantage of FIFO buffers is the ability to buffer data between two mismatched systems or subsystems. Inherent to an interface between two asynchronous systems is the issue of synchronizing events on one side with respect to events on the other.

For the Clocked FIFOs, internal logic is used to synchronize the status flags to either the Write Clock (WCLK) or the Read Clock (RCLK). A skew time is specified which determines if sufficient time has been allowed for the flag to be updated in the current clock cycle. If the skew timing is not met, an extra cycle is required to update the flag.



NOTE:

1. tSKEW1 is the minimum time between a rising RCLK edge and a rising WCLK edge for FF to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than tSKEW1, then FF may not change state until the next WCLK edge.

Figure 1. Skew Timing

SyncFIFO is a trademark of Integrated Device Technology, Inc.

WIDTH EXPANSION

When using the Clocked FIFOs in Width Expansion, the control signals of all parallel FIFOs should be connected together to maintain concurrent operations on all devices. The recommended flag output circuitry is shown in the following section.

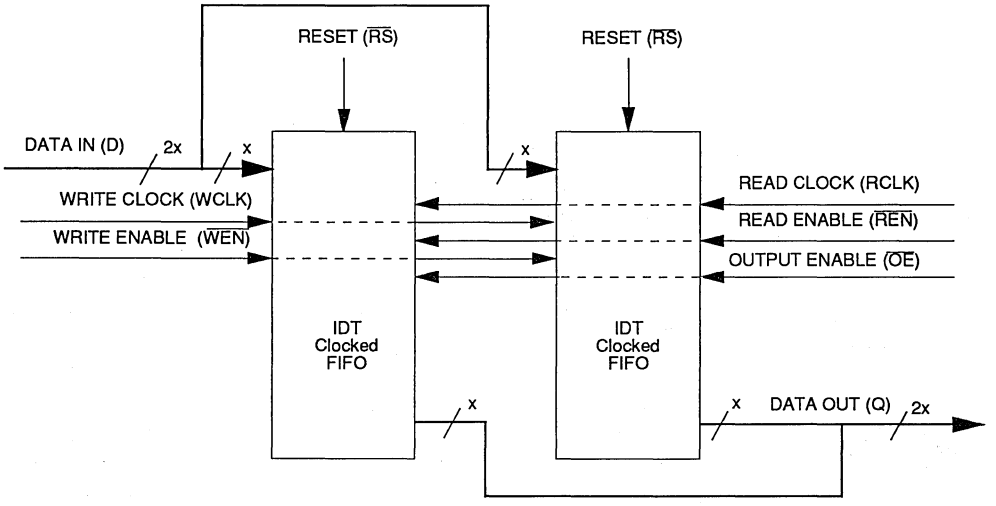


Figure 2. Block Diagram Showing the Control Signals of a SyncFIFO (Clocked FIFO) in a Width Expansion Configuration

B

DESIGN CONSIDERATIONS

Inherent to all Clocked FIFOs is the concept of skew timing. In reality, the skew timing of individual devices may vary by a small amount. For example, the t_{SKEW1} minimum spec for the 20 ns speed grade of the IDT72211 (512 x 9-Bit) equals 8ns. For two devices in width expansion, the actual t_{SKEW1} of FIFO#1 may equal 7.2ns and the actual t_{SKEW1} of FIFO#2 may equal 7.4ns.

This small variation in the actual timing of the devices may cause the flags of the parallel devices to be de-asserted in different cycles. For example, if the t_{SKEW1} timing of the system happens to be 7.3ns on the edge which is de-asserting the $\overline{EF}$, then the $\overline{EF}$ of the two FIFOs will be de-asserted on different clock cycles.

In this situation, if $\overline{REN}$ is asserted to begin read operations when the $\overline{EF}$ of FIFO#1 is de-asserted but the $\overline{EF}$ of FIFO#2 is not de-asserted, then data on the outputs (Q) of the two devices will not be aligned. In other words, data from FIFO#2 will have a one location lag behind data from FIFO#1.

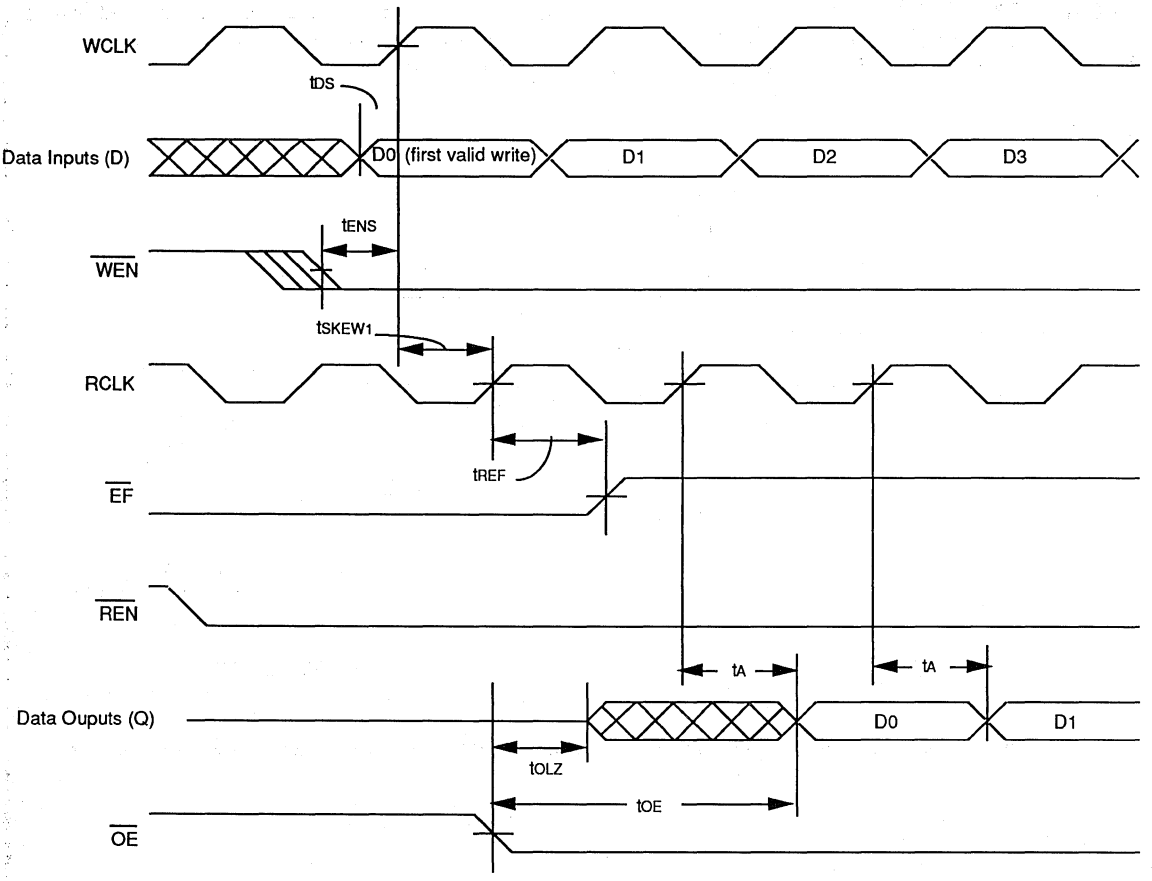


Figure 3. Skew Timing for FIFO#1

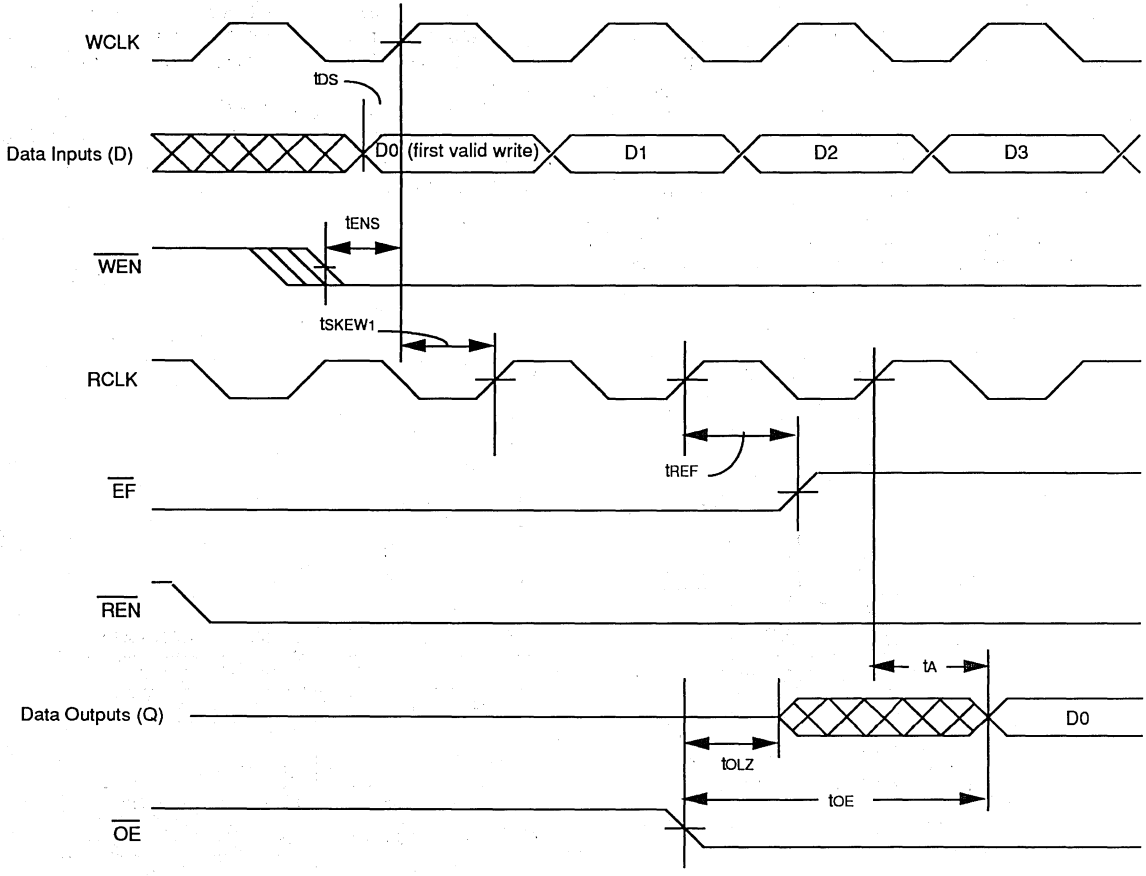


Figure 4. Skew Timing for FIFO#2

SOLUTION AND RECOMMENDATION

There are three solutions to the situation described.

1. Composite Flag. Monitor the $\overline{EF}$ from all FIFOs in Width Expansion. A read operation ($\overline{REN}$ = low) can begin only when the $\overline{EF}$ from all devices have been de-asserted. This is the recommended solution.

2. Wait two clock cycles after $\overline{EF}$ de-assertion of any one device to begin a read operation. A read operation can begin ($\overline{REN}$ = low) once two cycles of the RCLK have occurred after de-assertion of the $\overline{EF}$ of any one of the parallel FIFOs. This will ensure that the $\overline{EF}$ on all devices has been de-asserted.

In a system where the Enable signals are generated by logic based on the state of the FIFO flags, the occurence of two clock cycles after $\overline{EF}$ de-assertion is already designed into the system.

3. Use the Almost Empty Flag ($\overline{AE}$) to begin read operations. De-assertion of $\overline{AE}$ may exhibit the same skew affect as the $\overline{EF}$ (see next section), however, using $\overline{AE}$ does not jeopardize data integrity.

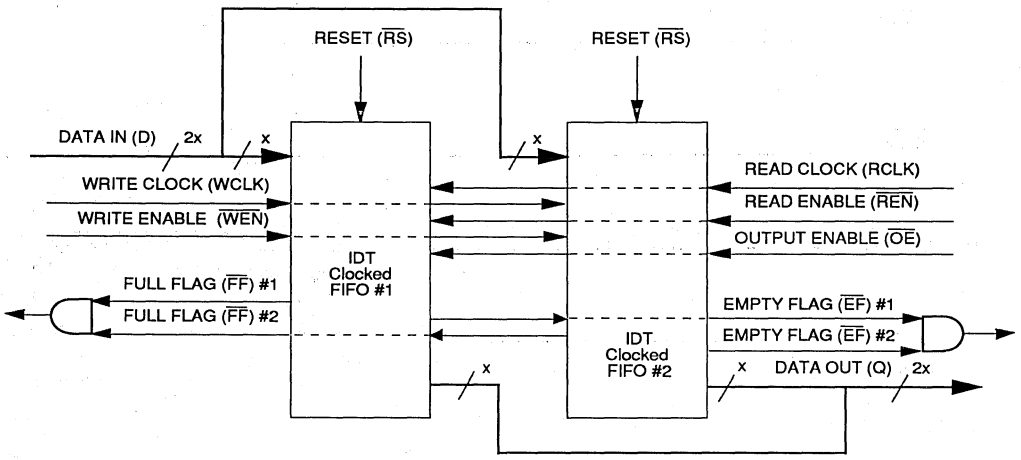


Figure 5. Recommended Block Diagram of Width Expansion using Composite Flags

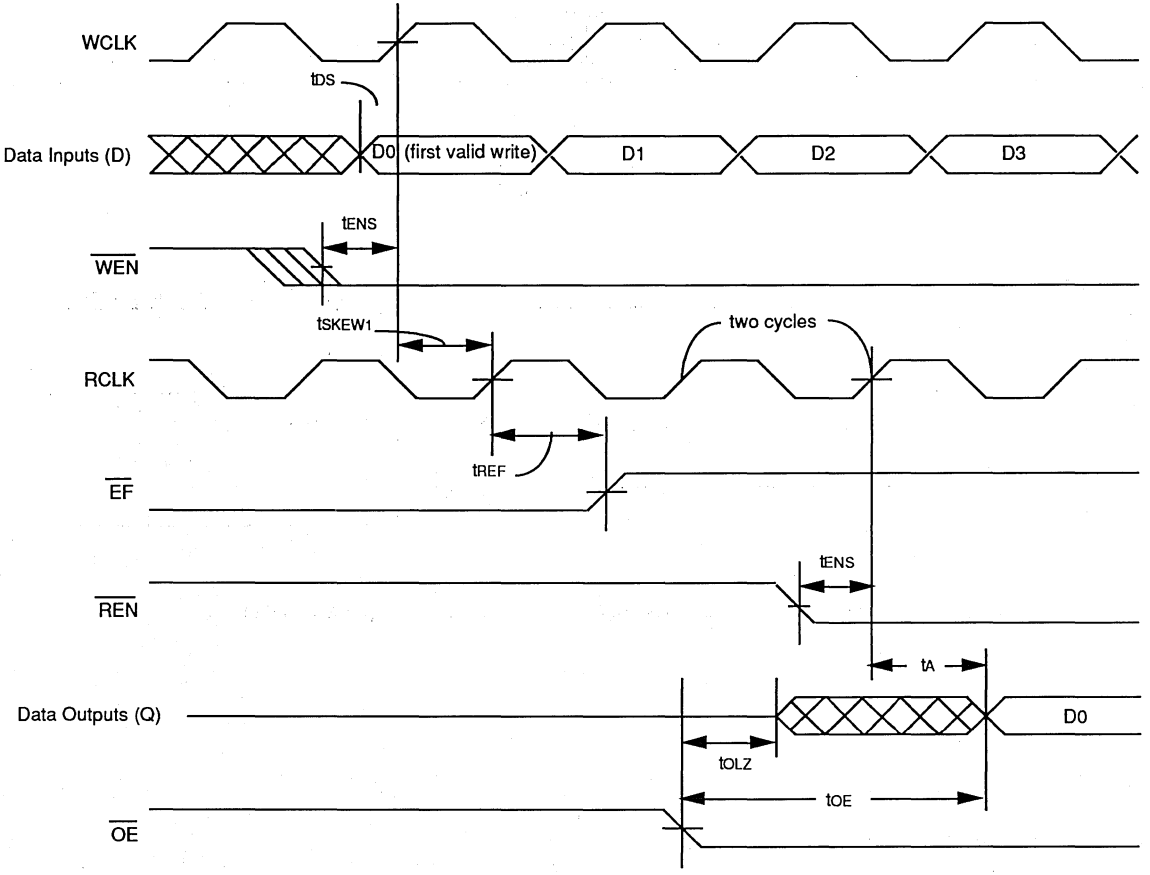


Figure 6. Waiting Two Clock Cycles after Flag Assertion

OTHER FLAGS

This skew affect also applies to the Full Flags ($\overline{FF}$) of all the Clocked FIFOs (x8, x9 and x18 SyncFIFOs), the Almost-Empty Flag ($\overline{AE}$) and Almost-Full Flag ($\overline{AF}$) for the IDT72XX0 family (x8 SyncFIFOs), and the Programmable Almost-Empty Flag ($\overline{PAE}$) and Programmable Almost-Full Flag ($\overline{PAF}$) for the IDT72XX1 family (x9 SyncFIFOs). The solution for these flags is identical to those outlined above. In summary:

1. Composite Flag. Monitor the flags from all devices.
2. Wait two clock cycles after de-assertion of the flag of any one device.

EXCEPTION

The exception to the skew affect is the Programmable Almost-Empty Flag ($\overline{PAE}$), the Programmable Almost-Full Flag ($\overline{PAF}$), and the Half-Full Flag ($\overline{HF}$) on the IDT722X5 family (x18 SyncFIFOs). These flags are not synchronized with respect to any one clock. In other words, they are asserted and de-asserted with respect to different clocks. In this case, there is no skew timing (t_{SKEW1}). The monitoring of only one device in Width Expansion is adequate for these flags.

B

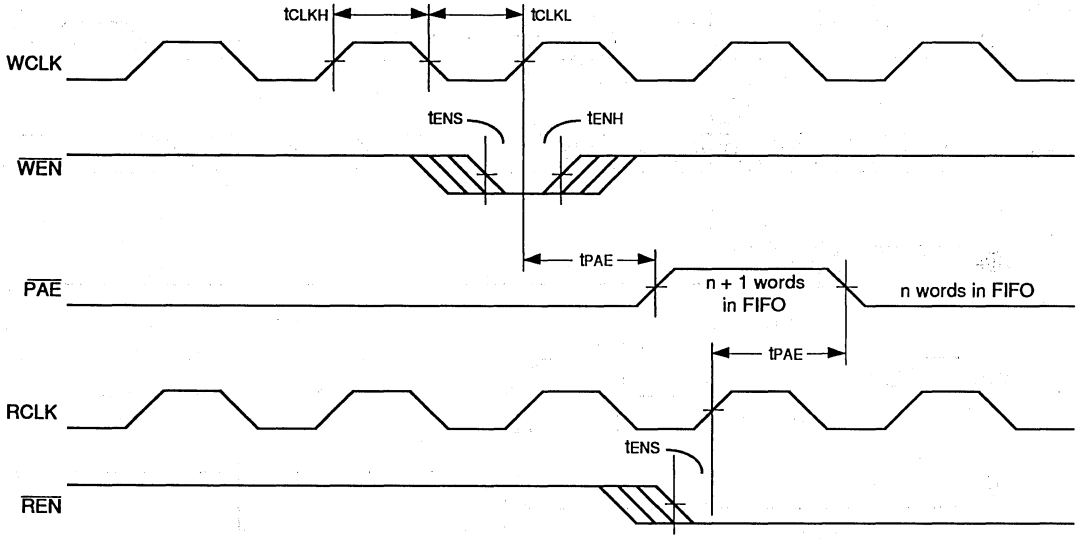


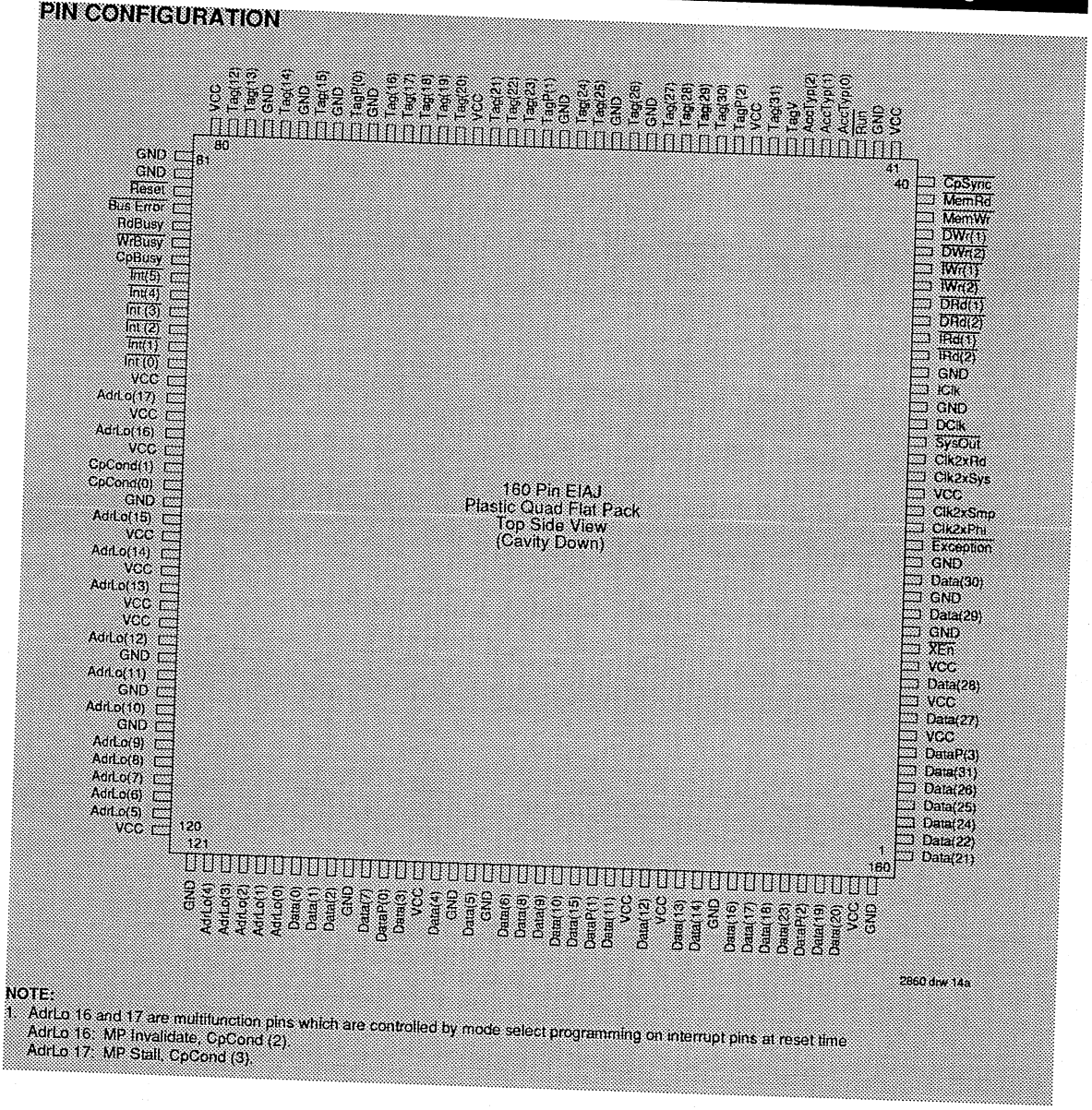
Figure 7. Programmable Flag Timing for the IDT722X5 Family (x18 SyncFIFOs)

1991 DATA BOOK UPDATE 1
TABLE OF CONTENTS

The following section contains partial data sheets that appeared in the 1991 RISC Data Book. These data sheets had changes to less than 50% of the overall contents. Refer to the bars above changes to see where that section can be found in the 1991 RISC Data Book.

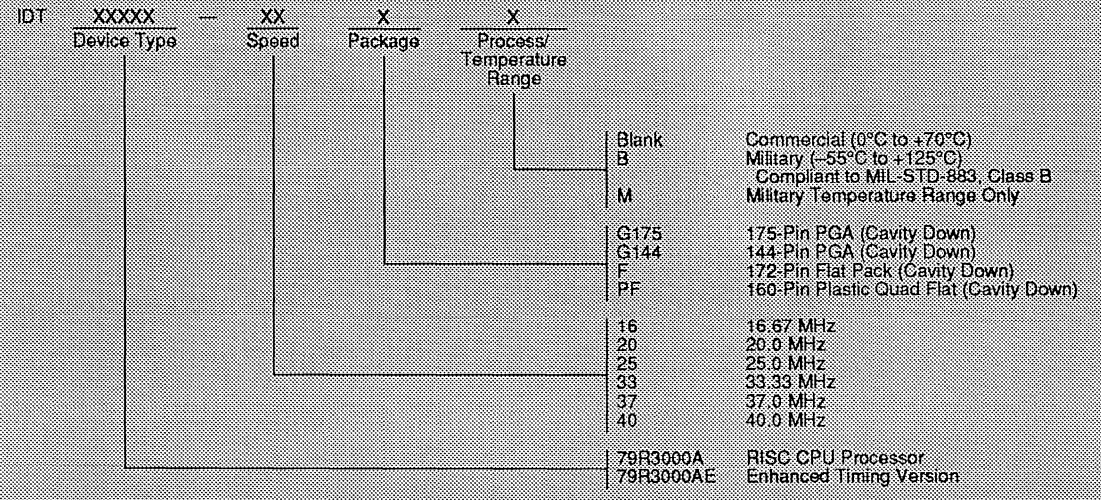
C

PIN CONFIGURATION



NOTE:
1. AdrLo 16 and 17 are multifunction pins which are controlled by mode select programming on interrupt pins at reset time.
   AdrLo 16: MP Invalidate, CpCond (2).
   AdrLo 17: MP Stall, CpCond (3).

ORDERING INFORMATION



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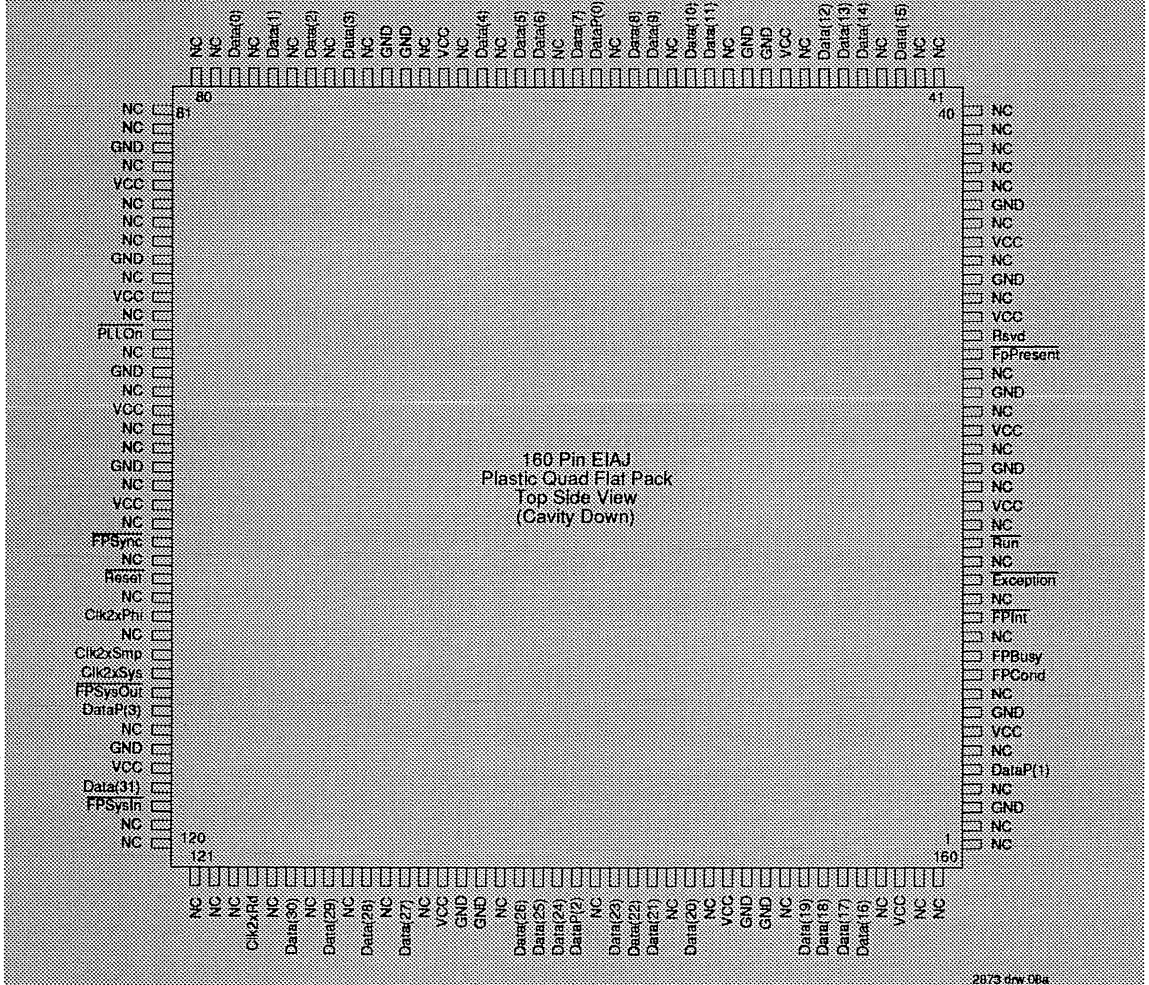
VALID COMBINATIONS

IDT	79R3000A - 16, 20	All packages
	79R3000A - 16, 20B, M	G144, G175, F
	79R3000AE - 25, 33 B, M	G144, G175, F
	79R3000AE - 25, 33, 37, 40	All Packages

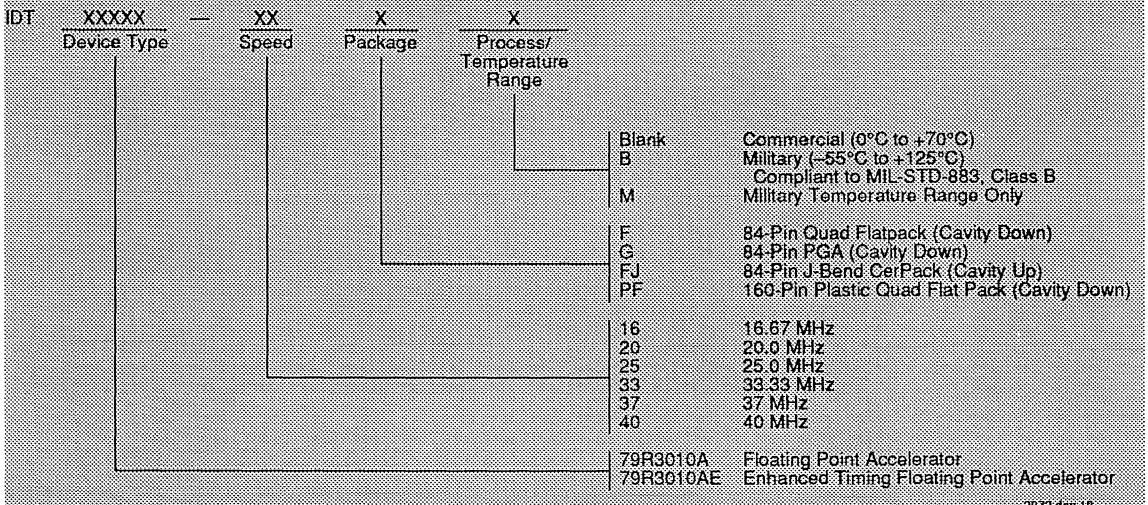
C

PIN CONFIGURATION[1]
160–PIN PLASTIC QUAD FLATPACK (CAVITY DOWN)
TOP VIEW



NOTE:
1. Reserved pins must not be connected.
2. NC are no connects and must not be connected.

ORDERING INFORMATION



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VALID COMBINATIONS

IDT	79R3010A - 16, 20	All packages
	79R3010A - 16, 20B, M	G, F
	79R3010AE - 25, 33 B, M	G, F
	79R3010AE - 25, 33, 37, 40	All Packages

C

External R3000 Condition Code Pin

The R3000 input CPC0 is available as a pin on the module. During run cycles, this pin acts as a Condition Code test pin, so the R3000 can do a Test and Branch in a single cycle based on its state.

SPECIFICATIONS

CPU
R3000

Floating Point
R3010 optional in either configuration. If present, connected to INT2.

Cache Ram
64 KB I-cache (16K words)
64 KB D-cache (16K words)

Cacheable Address Space
4 GBytes

MP Support
Cache invalidate supported

Block Refill
8 word (or single word)

Endianess
Big Endian

Read/Write Buffers
1 - Word Read Buffer
4 - Word Write Buffer

Interrupts
6 User Interrupts, synchronized with SYSOUTA:D in an on-board register.

I/O characteristics
TTL levels from FCT logic devices, PALs and R3000

Power Supply
4.5 amps (typical) at 5.0 V, 25°C, at33MHz.

Environmental Conditions
Ambient temperature 0°C to +50°C.
Relative Humidity 5% to 95%

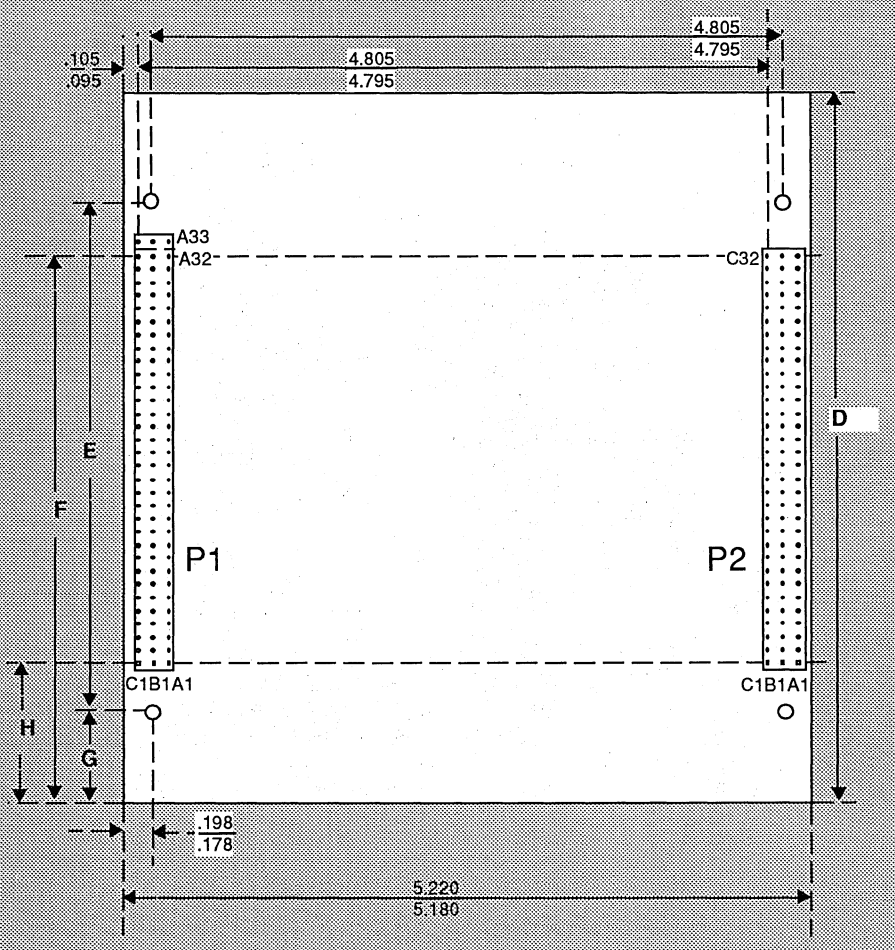
Clock Frequencies
20, 25 and 33 MHz

Interconnection
195 18-mil round pins on 100-mil centers
Mating connector: Samtec SS-1 series socket strips or equivalent.

User Selectable Options via jumpers:
Streaming/No Streaming
Store Partial On/Off

MECHANICAL OUTLINE

7RS107 TOP VIEW



	7RS107-66		7RS108-88		7RS109-66	
	Min.	Max.	Min.	Max.	Min.	Max.
D	5.180	5.220	5.380	5.420	5.180	5.220
E	3.545	3.555	3.545	3.555	3.545	3.555
F	4.145	4.155	4.245	4.255	4.145	4.155
G	0.815	0.835	0.915	0.935	0.815	0.835
H	1.045	1.055	1.145	1.155	1.045	1.055
K		0.30		0.30		0.30
L		0.20		0.15		0.20

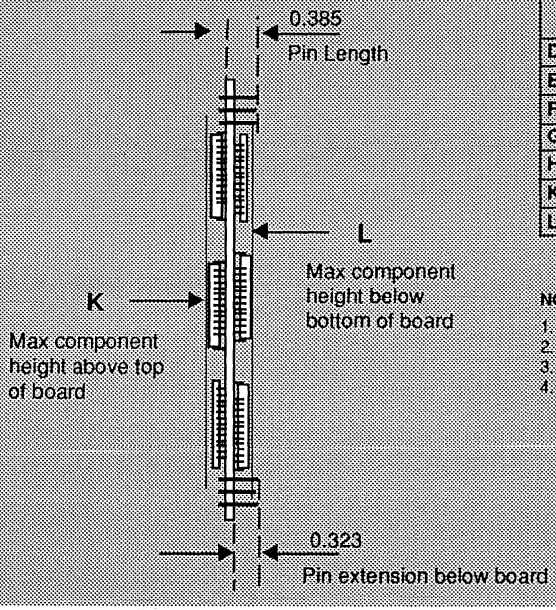
NOTES:

1. All dimensions in inches unless otherwise noted.
2. The 7RS107, 108 and 109 are a family of modules. Dimensions for all three are listed here, so that you can add flexibility by accepting all three modules.
3. P1 on the 7RS107 has three rows of 33 pins, while P1 on the 7RS108/9 has three rows of 32 pins.
4. Mounting holes are 0.109 ± .002. Note that mounting holes are offset from center line of connector.
5. Holes take #2 mounting hardware.
6. Pins are 0.018 diameter on 0.100 spacing on both axis.
7. To connect the modules use strip connectors Rob. Nug. SBE-32-S-TG for 32 pins, Rob. Nug. SBE-33-S-TG for 33 pins or equivalent.

C

MECHANICAL OUTLINE

7RS107 SIDE VIEW



	7RS107-66 Min.	7RS107-66 Max.	7RS108-88 Min.	7RS108-88 Max.	7RS109-66 Min.	7RS109-66 Max.
D	5.180	5.220	5.380	5.420	5.180	5.220
E	3.545	3.555	3.545	3.555	3.545	3.555
F	4.145	4.155	4.245	4.255	4.145	4.155
G	0.815	0.835	0.915	0.935	0.815	0.835
H	1.045	1.055	1.145	1.155	1.045	1.055
K		0.30		0.30		0.30
L		0.20		0.15		0.20

NOTES:
1. All dimensions in inches unless otherwise noted.
2. Pins are 0.018 diameter on 0.100 spacing on both axis.
3. Board thickness 0.062 ± .007.
4. To connect the modules use strip connectors Rob. Nug. SBE-32-S-TG for 32 pins, Rob. Nug. SBE-33-S-TG for 33 pins or equivalent.

CUSTOM OPTIONS

Some features of the 7RS107 can be modified by special order. Contact your IDT sales office for details. Examples of possible modifications include: initialization mode for the R3000, endian option, size of block refill, pin length, style, and plating; special marking; additional burn-in, and socketing of the CPU and/or FPA.

FOR DETAILED DESIGN INFORMATION, CONTACT IDT AND ASK FOR THE 7RS107 DESIGNER'S GUIDE.

R3000 MODULE FOR HIGH PERFORMANCE CPUS:

The module is constructed using surface mount devices on a 5.2" by 5.4" epoxy laminate board, and is connected to the user's system via 192 pins located in two pin row regions on the board.

7RS108 Module. Actual Size 5.2" x 5.4"

SIGNALS PROVIDED ON MODULE PINS

Signal Name	Type	Description
EXTOSC	I	Optional input for external oscillator.

SPECIFICATIONS

CPU
R3000

Floating Point
R3010 optional in either configuration. If present, connected to INT2.

Cache Ram
256 KB I-cache (64K words)
256 KB D-cache (64K words)

Cacheable Address Space
4 GBytes

MP Support
Cache invalidate supported

Block Refill
8 or 16 - word (or single word)

Endianess
Big Endian

Read/Write Buffers
1 - Word Read Buffer
4 - Word Write Buffer

Interrupts
6 User Interrupts, synchronized with SYSOUTA.D in an on-board register.

I/O characteristics
TTL levels from FCT logic devices, PALs and R3000

Power Supply
3.5 amps (typical) at 5.0 V, 25°C, at 25MHz.

Environmental Conditions
Ambient temperature 0°C to +50°C
Relative Humidity 5% to 95%

Clock Frequencies
20 and 25 MHz

Interconnection
192 18-mil round pins on 100-mil centers
Mating connector: Samtec SS-1 series socket strips or equivalent.

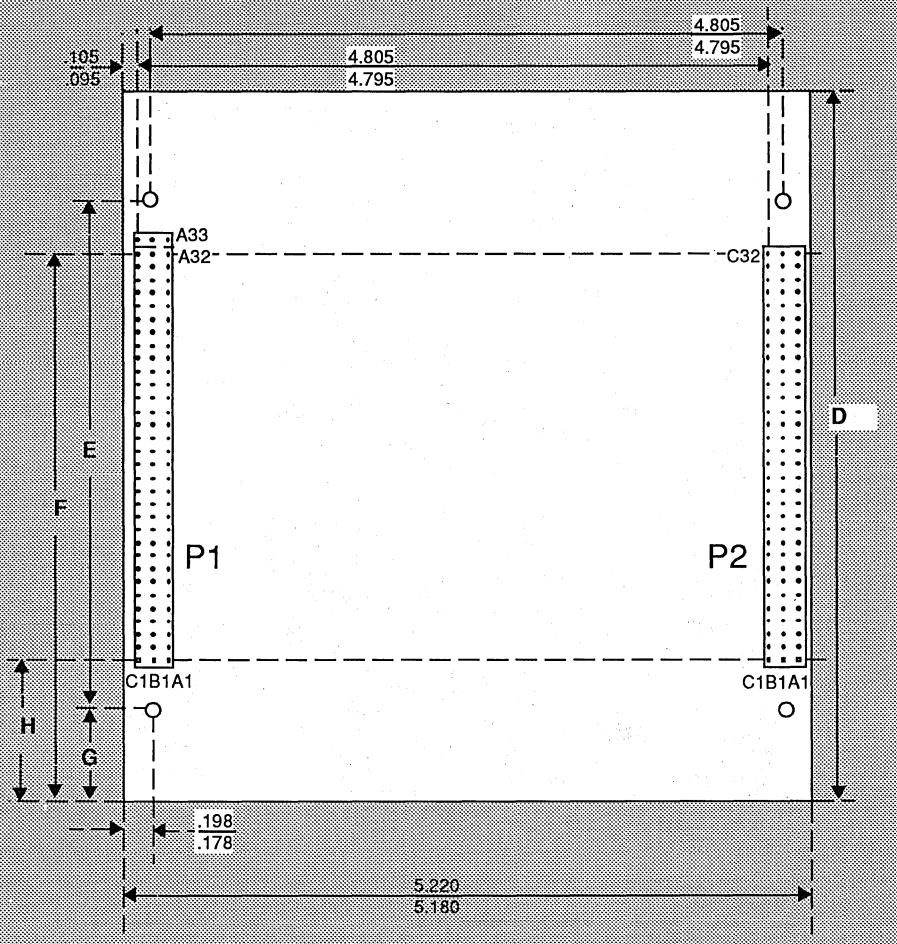
User Selectable Options via jumpers:
8 word or 16 word block refill
Streaming/No Streaming
Store Partial On/Off

Other Options:
The 7RS108 may be factory programmed with different initialization options or altered in other ways for special needs. Please contact your IDT sales office if you are interested in a variation of the standard 7RS108 module.

C

MECHANICAL OUTLINE

7RS108 TOP VIEW

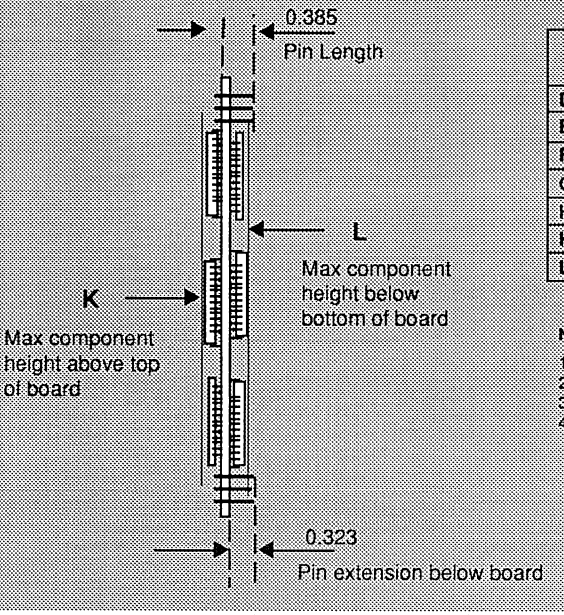


	7RS107-66		7RS108-88		7RS109-66	
	Min.	Max.	Min.	Max.	Min.	Max.
D	5.180	5.220	5.380	5.420	5.180	5.220
E	3.545	3.555	3.545	3.555	3.545	3.555
F	4.145	4.155	4.245	4.255	4.145	4.155
G	0.815	0.835	0.915	0.935	0.815	0.835
H	1.045	1.055	1.145	1.155	1.045	1.055
K		0.30		0.30		0.30
L		0.20		0.15		0.20

NOTES:

1. All dimensions in inches unless otherwise noted.
2. The 7RS107, 108, and 109 are a family of modules. Dimensions for all three are listed here, so that you can add flexibility by accepting all three modules.
3. P1 on the 7RS107 has three rows of 33 pins, while P1 on the 7RS108/9 has three rows of 32 pins.
4. Mounting holes are 0.109 ± .002. Note that mounting holes are offset from center line of connector.
5. Holes take #2 mounting hardware.
6. Pins are 0.018 diameter on 0.100 spacing on both axis.
7. To connect the modules use strip connectors Rob. Nug. SBE-32-S-TG for 32 pins, Rob. Nug. SBE-33-S-TG for 33 pins or equivalent.

MECHANICAL OUTLINE



	7RS107-66		7RS108-88		7RS109-66	
	Min.	Max.	Min.	Max.	Min.	Max.
D	5.180	5.220	5.380	5.420	5.180	5.220
E	3.545	3.555	3.545	3.555	3.545	3.555
F	4.145	4.155	4.245	4.255	4.145	4.155
G	0.815	0.835	0.915	0.935	0.815	0.835
H	1.045	1.055	1.145	1.155	1.045	1.055
K		0.30		0.30		0.30
L		0.20		0.15		0.20

NOTES:
1. All dimensions in inches unless otherwise noted.
2. Pins are 0.018 diameter on 0.100 spacing on both axis.
3. Board thickness 0.062 ± .007.
4. To connect the modules use strip connectors Rob. Nug. SBE-32-S-TG for 32 pins, Rob. Nug. SBE-33-S-TG for 33 pins or equivalent.

CUSTOM OPTIONS

Some features of the 7RS108 can be modified by special order. Contact your IDT sales office for details. Possible modifications include: initialization mode for the R3000, endian option, size of block refill, instruction streaming, pin length, style, and plating; special marking; additional burn-in, and socketing of the CPU and/or FPA.

ADDITIONAL INFORMATION

For detailed design information, contact IDT and ask for the 7RS108 Designer's Guide.

C

FEATURES:

- Small size: 3.3" x 4.1"

7RS110 Module. Actual Size 3.3" x 4.1"

SIGNALS PROVIDED ON MODULE PINS

Signal Name	Type	Description
WPERR# **	OUT	Negative-true output used to indicate data parity error while write to memory operation.
RPERR# **	OUT	Negative-true output used to indicate data parity error while read from memory operation.

SPECIFICATIONS

CPU
R3000 in 7RS110-55; R3001 in 7RS110-54

Floating Point
R3010 optional in either configuration. If present, connected to INT1.

Cache Ram
7RS110-55:
32 KB each I and D-cache. (8K words)
7RS110-54
32 KB I-cache (8K words)
16 KB D-cache (4K words)

Cacheable Address Space
7RS110-55
4 GBytes
7RS110-54
0.5 GBytes

MP Support
7RS110-55
Cache invalidate supported
7RS110-54
Not supported

Block Refill
8 or 16 word (or single word)

Endianess
User programmable via module pin.

Read/Write Buffers
Both are one word deep.

Interrupts
6 User Interrupts, synchronized with SYSOUTA:D in an on-board register.

I/O characteristics
TTL levels from FCT logic devices, PALs and R3000

Power Supply
2.5 amps (typical) at 5.0 V, 25°C, at rated speed.

Environmental Conditions
Ambient temperature 0°C to +50°C.
Relative Humidity 5% to 95%

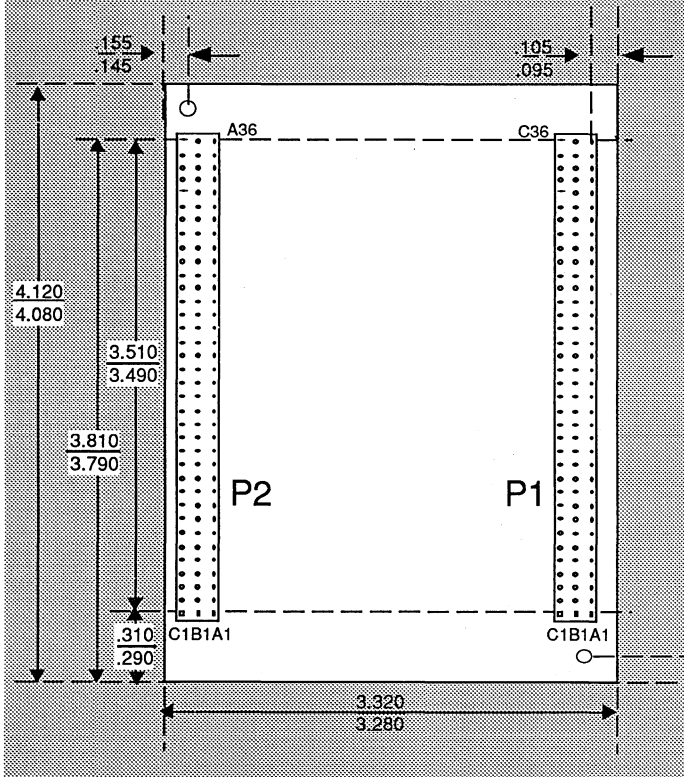
Clock Frequencies
7RS110-55
20, 25, and 33 MHz
7RS110-54
20 and 25 MHz

Interconnection
216 18-mil round pins on 100-mil centers
Mating connector: Samtec SS-1 series socket strips or equivalent.

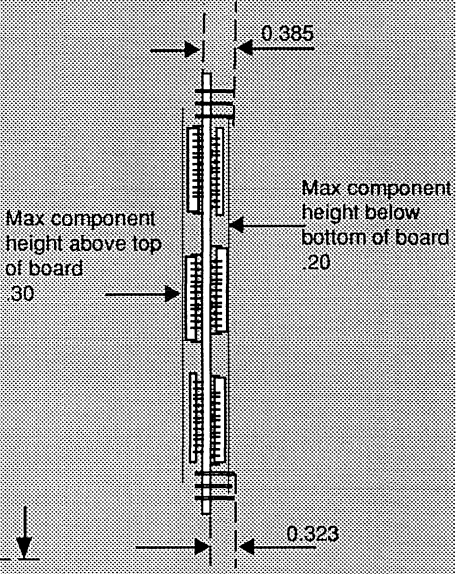
User Selectable Options

MECHANICAL OUTLINE

7RS110 TOP VIEW



7RS110 SIDE VIEW



NOTES:

1. Mounting holes are 0.090± .002. Note that the mounting holes are offset from the center line of connector.
2. All dimensions in inches unless otherwise noted.
3. Pins are 0.018 diameter on 0.100 spacing on both axis.
4. Pin length = .385" (Extension below board = .323").
5. Board thickness 0.062 ± .007.
6. To connect the modules use strip connectors Rob. Nug. SBQ-50P-D-100-TG for 36 pins or equivalent.

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ADDITIONAL INFORMATION

For detailed design information, contact IDT and ask for the 7RS110 Designer's Guide.

OTHER OPTIONS

The 7RS110 may be factory programmed with different initialization options or altered in other ways for special needs. Please contact your IDT sales office if you are interested in a variation on the standard 7RS110 module.

The following section contains full data sheets that appeared in the 1991 RISC Data Book. These data sheets had changes to 50% or more of the overall contents and are now considered new. Refer to the bar at the top of each page to see where that page can be found in the 1991 RISC Data Book.

Integrated Device Technology, Inc.

IDT79R3051 FAMILY OF INTEGRATED RISControllers™

PRELIMINARY
IDT 79R3051™, 79R3051E
IDT 79R3052™, 79R3052E

FEATURES:

- Instruction set compatible with IDT79R3000A and IDT79R3001 MIPS RISC CPUs
- High level of integration minimizes system cost, power consumption
  - 79R3000A /79R3001 RISC Integer CPU
  - R3051 features 4kB of Instruction Cache
  - R3052 features 8kB of Instruction Cache
  - All devices feature 2kB of Data Cache
  - "E" Versions (Extended Architecture) feature full function Memory Management Unit, including 64-entry Translation Lookaside Buffer (TLB)
  - 4-deep write buffer eliminates memory write stalls
  - 4-deep read buffer supports burst refill from slow memory devices
  - On-chip DMA arbiter
  - Bus Interface Minimizes Design Complexity
- Single clock input with 40%-60% duty cycle
- Direct interface to R3720/21/22 RISChipset™
- 35 MIPS, over 64,000 Dhrystones at 40 MHz
- Low cost 84-pin PLCC packaging with optional thermal slug
- Flexible bus interface allows simple, low cost designs
- 20, 25, 33, and 40 MHz operation
- Complete software support
  - Optimizing compilers
  - Real-time operating systems
  - Monitors/debuggers
  - Floating Point Software
  - Page Description Languages

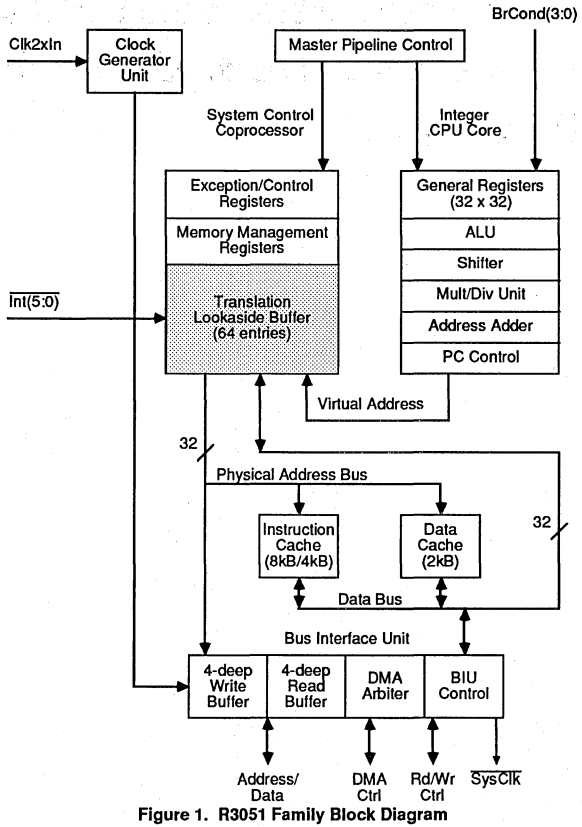

Figure 1. R3051 Family Block Diagram

RISController, R305x, R3051, R3052 are trademarks of Integrated Device Technology, Inc.

INTRODUCTION

The IDT R3051 Family is a series of high-performance 32-bit microprocessors featuring a high level of integration, and targeted to high-performance but cost sensitive embedded processing applications. The R3051 family is designed to bring the high-performance inherent in the MIPS RISC architecture into low-cost, simplified, power sensitive applications.

Functional units were integrated onto the CPU core in order to reduce the total system cost, without significantly degrading system performance. Thus, the R3051 family is able to offer 35 MIPS of integer performance at 40 MHz without requiring external SRAM or caches.

Further, the R3051 family brings dramatic power reduction to these embedded applications, allowing the use of low-cost packaging for devices up to 25 MHz. The R3051 family allows customer applications to bring maximum performance at minimum cost.

Figure 1 shows a block level representation of the functional units within the R3051 family. The R3051 family could be viewed as the embodiment of a discrete solution built around the IDT 79R3000A or 79R3001. However, by integrating this functionality on a single chip, dramatic cost and power reductions are achieved.

Currently, there are four members of the R3051 family family. All devices are pin and software compatible: the differences lie in the amount of instruction cache, and in the memory management capabilities of the processor:

- The R3052"E" incorporates 8kB of Instruction Cache, and features a full function memory management unit (MMU) including a 64-entry fully-associative Translation Lookaside Buffer (TLB). This is the same memory management unit incorporated in the IDT 79R3000A and 79R3001.
- The R3052 also incorporates 8kB of Instruction Cache. However, the memory management unit is a much simpler subset of the capabilities of the enhanced versions of the architecture, and in fact does not use a TLB.
- The R3051"E" incorporates 4kB of Instruction Cache. Additionally, this device features the same full function MMU (including TLB file) as the R3052"E", and R3000A.
- The R3051 incorporates 4kB of Instruction Cache, and uses the simpler memory management model of the R3052.

An overview of the functional blocks incorporated in these devices follows.

CPU Core

The CPU core is a full 32-bit RISC integer execution engine, capable of sustaining close to single cycle execution rate. The CPU core contains a five stage pipeline, and 32 orthogonal 32-bit registers. The R3051 family implements the MIPS ISA. In fact, the execution engine of the R3051 family is the same as the execution engine of the R3000A (and R3001). Thus, the R3051 family is binary compatible with those CPU engines.

The execution engine of the R3051 family uses a five-stage pipeline to achieve close to single cycle execution. A new instruction can be started in every clock cycle; the execution engine actually processes five instructions concurrently (in various pipeline stages). Figure 2 shows the concurrency achieved by the R3051 family pipeline.

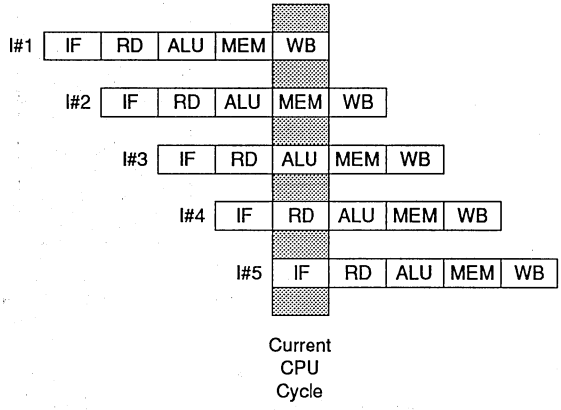

Figure 2. R3051 Family 5-Stage Pipeline

System Control Co-Processor

The R3051 family also integrates on-chip the System Control Co-processor, CP0. CP0 manages both the exception handling capability of the R3051 family, as well as the virtual to physical mapping of the R3051 family.

There are two versions of the R3051 family architecture: the Extended Architecture Versions (the R3051E and R3052E) contain a fully associative 64-entry TLB which maps 4kB virtual pages into the physical address space. The virtual to physical mapping thus includes kernel segments which are hard mapped to physical addresses, and kernel and user segments which are mapped on a page basis by the TLB into anywhere within the 4GB physical address space. In this TLB, 8 page translations can be "locked" by the kernel to insure deterministic response in real-time applications. These versions thus use the same MMU structure as that found in the IDT 79R3000A and 79R3001. Figure 3 shows the virtual to physical address mapping found in the Extended Architecture versions of the processor family.

The Extended Architecture devices allow the system designer to implement kernel software to dynamically manage User task utilization of memory resources, and also allow the Kernel to effectively "protect" certain resources from user tasks. These capabilities are important in a number of embedded applications, from process control (where resource protection may be extremely important) to X-Window display systems (where virtual memory management is extremely important), and can also be used to simplify system debugging.

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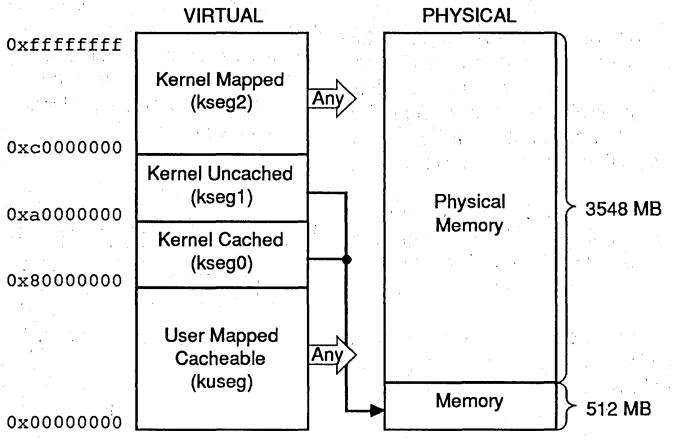

Figure 3. Virtual to Physical Mapping of Extended Architecture Versions

The base versions of the architecture (the R3051 and R3052) remove the TLB and institute a fixed address mapping for the various segments of the virtual address space. The base processors support distinct kernel and user mode operation without requiring page management software, leading to a simpler software model. The memory mapping used by these devices is illustrated in figure 4. Note that the reserved address spaces shown are for compatibility with future family members; in the current family members, references to these addresses are translated in the same fashion as their respective segments, with no traps or exceptions taken.

When using the base versions of the architecture, the system designer can implement a distinction between the user tasks and the kernel tasks, without having to execute page management software. This distinction can take the form of physical memory protection, accomplished by address decoding, or in other forms. In systems which do not wish to implement memory protection, and wish to have the kernel and user tasks operate out of a single unified memory space, upper address lines can be ignored by the address decoder, and thus all references will be seen in the lower gigabyte of the physical address space.

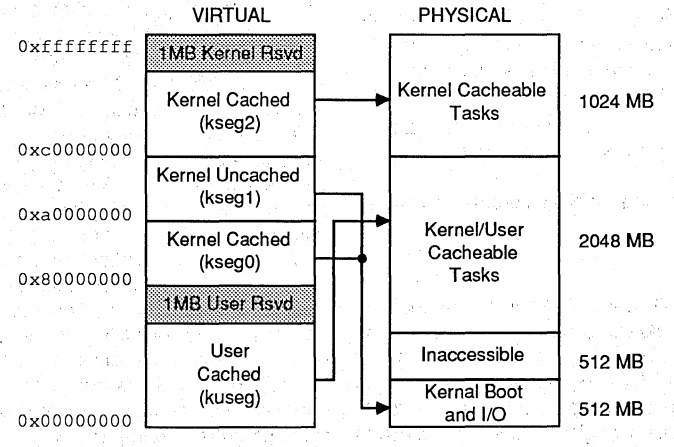

Figure 4. Virtual to Physical Mapping of Base Architecture Versions

Clock Generation Unit

The R3051 family is driven from a single input clock, capable of operating in a range of 40%-60% duty cycle. On-chip, the clock generator unit is responsible for managing the interaction of the CPU core, caches, and bus interface. The clock generator unit replaces the external delay line required in R3000A and R3001 based applications.

Instruction Cache

The current family includes two different instruction cache sizes: the R3051 family (the R3051 and R3051E) feature 4kB of instruction cache, and the R3052 and R3052E each incorporate 8kB of Instruction Cache. For all four devices, the instruction cache is organized as a line size of 16 bytes (four words). This relatively large cache achieves a hit rate well in excess of 95% in most applications, and substantially contributes to the performance inherent in the R3051 family. The cache is implemented as a direct mapped cache, and is capable of caching instructions from anywhere within the 4GB physical address space. The cache is implemented using physical addresses (rather than virtual addresses), and thus does not require flushing on context switch.

Data Cache

All four devices incorporate an on-chip data cache of 2kB, organized as a line size of 4 bytes (one word). This relatively large data cache achieves hit rates well in excess of 90% in most applications, and contributes substantially to the performance inherent in the R3051 family. As with the instruction cache, the data cache is implemented as a direct mapped physical address cache. The cache is capable of mapping any word within the 4GB physical address space.

The data cache is implemented as a write through cache, to insure that main memory is always consistent with the internal cache. In order to minimize processor stalls due to data write operations, the bus interface unit incorporates a 4-deep write buffer which captures address and data at the processor execution rate, allowing it to be retired to main memory at a much slower rate without impacting system performance.

Bus Interface Unit

The R3051 family uses its large internal caches to provide the majority of the bandwidth requirements of the execution engine, and thus can utilize a simple bus interface connected to slow memory devices.

The R3051 family bus interface utilizes a 32-bit address and data bus multiplexed onto a single set of pins. The bus interface unit also provides an ALE signal to de-multiplex the A/D bus, and simple handshake signals to process processor read and write requests. In addition to the read and write interface, the R3051 family incorporates a DMA arbiter, to allow an external master to control the external bus.

The R3051 family incorporates a 4-deep write buffer to decouple the speed of the execution engine from the speed of the memory system. The write buffers capture and FIFO processor address and data information in store operations, and presents it to the bus interface as write transactions at the rate the memory system can accommodate.

The R3051/52 read interface performs both single word reads and quad word reads. Single word reads work with a simple handshake, and quad word reads can either utilize the simple handshake (in lower performance, simple systems) or utilize a tighter timing mode when the memory system can burst data at the processor clock rate. Thus, the system designer can choose to utilize page or nibble mode DRAMs (and possibly use interleaving), if desired, in high-performance systems, or use simpler techniques to reduce complexity.

In order to accommodate slower quad word reads, the R3051 family incorporates a 4-deep read buffer FIFO, so that the external interface can queue up data within the processor before releasing it to perform a burst fill of the internal caches. Depending on the cost vs. performance tradeoffs appropriate to a given application, the system design engineer could include true burst support from the DRAM to provide for high-performance cache miss processing, or utilize the read buffer to process quad word reads from slower memory systems.

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SYSTEM USAGE

The IDT R3051 family has been specifically designed to easily connect to low-cost memory systems. Typical low-cost memory systems utilize slow EPROMs, DRAMs, and application specific peripherals. These systems may also typically contain large, slow static RAMs, although the IDT R3051 family has been designed to not specifically require the use of external SRAMs.

Figure 5 shows a typical system block diagram. Transparent latches are used to de-multiplex the R3051/52 address and data busses from the A/D bus. The data paths between the memory system elements and the R3051 family A/D bus is managed by simple octal devices. A small set of simple PALs can be used to control the various data path elements, and to control the handshake between the memory devices and the CPU.

Alternately, the memory interface can be constructed using the IDT R3051 family RISChipset, which includes DRAM control, data path control for interleaved memories, and other general memory and system interface control functions. These devices are described in separate data sheets. Figure 6 illustrates a simple system constructed using the R3051 RISChipset.

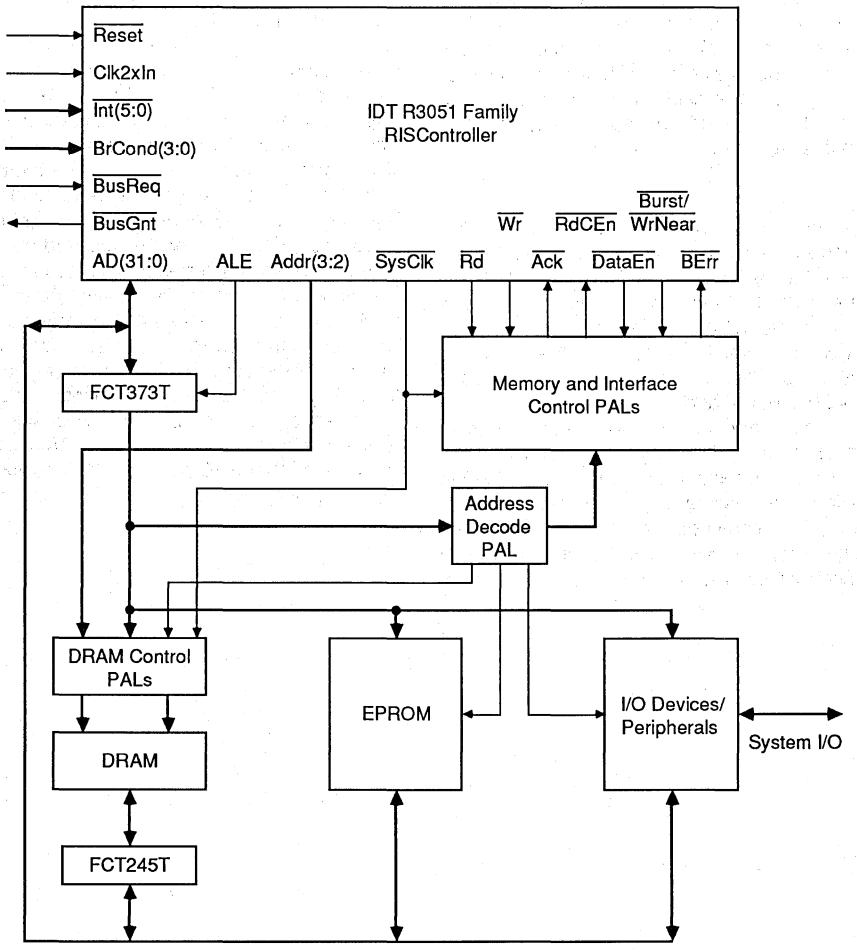

Figure 5. Typical R3051 Family Based System

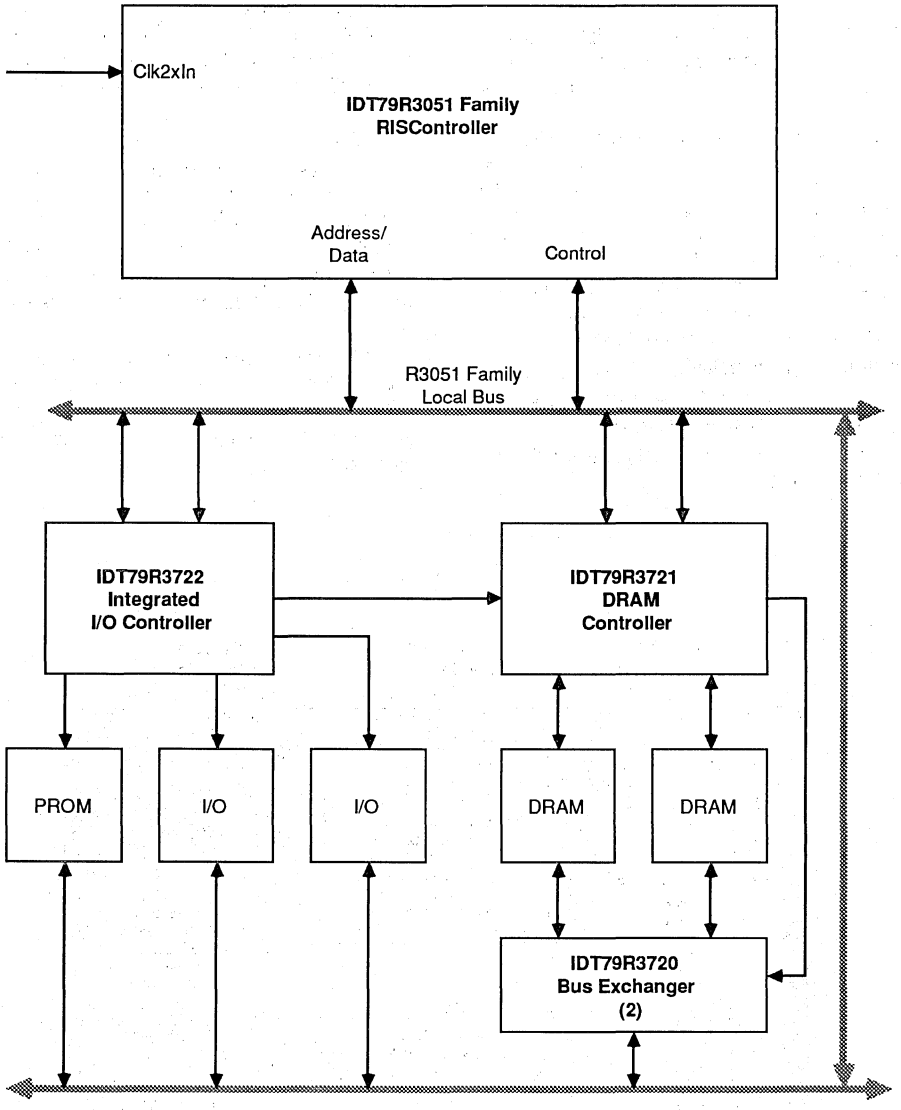

Figure 6. R3051 Family Chip Set Based System

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DEVELOPMENT SUPPORT

The IDT R3051 family is supported by a rich set of development tools, ranging from system simulation tools through prom monitor support, logic analysis tools, and sub-system modules.

Figure 7 is an overview of the system development process typically used when developing R3051 family-based applications. The R3051 family is supported by powerful tools through all phases of project development. These tools allow timely, parallel development of hardware and software for R3051/52 based applications, and include tools such as:

- A program, Cache-3051, which allows the performance of an R3051 family based system to be modeled and understood without requiring actual hardware.
- Sable, an instruction set simulator.
- Optimizing compilers from MIPS, the acknowledged leader in optimizing compiler technology.
- IDT Cross development tools, available in a variety of development environments.
- The high-performance IDT floating point library software, which has been integrated into the compiler toolchain to allow software floating point to replace hardware floating point without modifying the original source code.
- The IDT Evaluation Board, which includes RAM, EPROM, I/O, and the IDT Prom Monitor.
- The IDT Laser Printer System board, which directly drives a low-cost print engine, and runs Microsoft TrueImage™ Page Description Language on top of PeerlessPage™ Advanced Printer Controller BIOS.
- Adobe PostScript™ Page Description Language, ported to the R3000 instruction set, runs on the IDT R3051 family.
- The IDT Prom Monitor, which implements a full prom monitor (diagnostics, remote debug support, peek/poke, etc.).
- An In-Circuit Emulator, developed and sold by Embedded Performance, Inc.

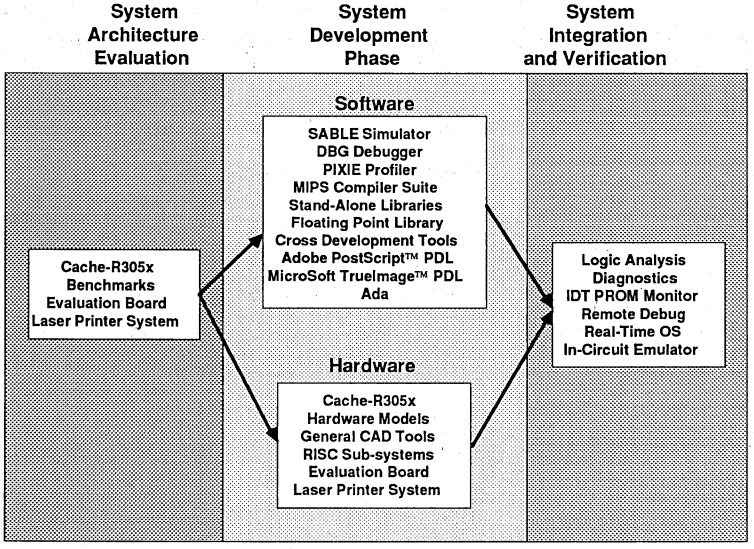

Figure 7. R3051 Family Development Toolchain

PERFORMANCE OVERVIEW

The R3051 family achieves a very high-level of performance. This performance is based on:

- **An efficient execution engine.** The CPU performs ALU operations and store operations at a single cycle rate, and has an effective load time of 1.3 cycles, and branch execution rate of 1.5 cycles (based on the ability of the compilers to avoid software interlocks). Thus, the execution engine achieves over 35 MIPS performance when operating out of cache.
- **Large on-chip caches.** The R3051 family contains caches which are substantially larger than those on the majority of today's embedded microprocessors. These large caches minimize the number of bus transactions required, and allow the R3051 family to achieve actual sustained performance very close to its peak execution rate.
- **Autonomous multiply and divide operations.** The R3051 family features an on-chip integer multiplier/divide unit which is separate from the other ALU. This allows the R3051 family to perform multiply or divide operations in parallel with other integer operations, using a single multiply or divide instruction rather than "step" operations.
- **Integrated write buffer.** The R3051 family features a four deep write buffer, which captures store target addresses and data at the processor execution rate and retires it to main memory at the slower main memory access rate. Use of on-chip write buffers eliminates the need for the processor to stall when performing store operations.
- **Burst read support.** The R3051 family enables the system designer to utilize page mode or nibble mode RAMs when performing read operations to minimize the main memory read penalty and increase the effective cache hit rates.

These techniques combine to allow the processor to achieve 35 MIPS integer performance, and over 64,000 dhrystones at 40 MHz without the use of external caches or zero wait-state memory devices.

SELECTABLE FEATURES

The R3051 family allows the system designer to configure some aspects of operation. These aspects are established when the device is reset, and include:

- BigEndian vs. LittleEndian operation: The part can be configured to operate with either byte ordering convention, and in fact may also be dynamically switched between the two conventions. This facilitates the porting of applications from other processor architectures, and also permits inter-communications between various types of processors and databases.
- Data cache refill of one or four words: The memory system must be capable of performing 4 word transfers to satisfy cache misses. This option allows the system designer to choose between one and four word refill on data cache misses, depending on the performance each option brings to his application.

THERMAL CONSIDERATIONS

The R3051 family utilizes special packaging techniques to improve the thermal properties of high-speed processors. Thus, all versions of the R3051 family are packaged in cavity down packaging.

The lowest cost members of the family use a standard cavity down, injection molded PLCC package (the "J" package). This package, coupled with the power reduction techniques employed in the design of the R3051 family, allows operation at speeds to 25MHz. However, at higher speeds, additional thermal care must be taken.

Thus, the R3051 family is also available in the "PH" package, which is basically a cavity down PLCC with an embedded exposed thermal slug. The thermal slug makes direct contact with the back of the die, allowing efficient thermal transfer between the die and the case of the part. Even nominal amounts of airflow will dramatically reduce the junction temperature of the die, resulting in cooler operation. The PH package is available at all frequencies, and is pin and form compatible with the PLCC package. Thus, designers can choose to utilize this package without changing their PCB.

Finally, the R3051 family is also available in a cavity down PGA with integral thermal slug. As with the PH package, this package is highly thermally efficient, and is appropriate for use in more extreme temperature conditions, such as military applications.

The members of the R3051 family are guaranteed in a case temperature range of 0°C to +85°C. The type of package, speed (power) of the device, and airflow conditions, affect the equivalent ambient conditions which meet this specification.

The equivalent allowable ambient temperature, T_A, can be calculated using the thermal resistance from case to ambient ($\emptyset_{CA}$) of the given package. The following equation relates ambient and case temperature:

$$T_A = T_C - P * \emptyset_{CA}$$

where P is the maximum power consumption at hot temperature, calculated by using the maximum Icc specification for the device.

Typical values for $\emptyset_{CA}$ at various airflows are shown in Table 1 for the various packages.

	Airflow (ft/min)					
$\emptyset_{CA}$	0	200	400	600	800	1000
"J" Package	29	26	21	18	16	15
"PH" Package*	22	8	3	2	1.5	1
PGA Package	22	8	3	2	1.5	1

Table 1. Thermal Resistance ($\emptyset_{CA}$) at Various Airflows (*estimated: final values tbd)

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PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
A/D(31:0)	I/O	**Address/Data:** A 32-bit time multiplexed bus which indicates the desired address for a bus transaction in one phase, and which is used to transmit data between the CPU and external memory resources during the rest of the transfer. Bus transactions on this bus are logically separated into two phases: during the first phase, information about the transfer is presented to the memory system to be captured using the ALE output. This information consists of: **Address(31:4):** The high-order address for the transfer is presented on A/D(31:4). **$\overline{BE}$(3:0):** These strobes indicate which bytes of the 32-bit bus will be involved in the transfer, and are presented on A/D(3:0). During write cycles, the bus contains the data to be stored and is driven from the internal write buffer. On read cycles, the bus receives the data from the external resource, in either a single data transaction or in a burst of four words, and places it into the on-chip read buffer.
Addr(3:2)	O	**Low Address (3:2)** A 2-bit bus which indicates which word is currently expected by the processor. Specifically, this two bit bus presents either the address bits for the single word to be transferred (writes or single datum reads) or functions as a two bit counter starting at '00' for burst read operations.
Diag(1)	O	**Diagnostic Pin 1.** This output indicates whether the current bus read transaction is due to an on-chip cache miss, and also presents part of the miss address. The value output on this pin is time multiplexed: **Cached:** During the phase in which the A/D bus presents address information, this pin is an active high output which indicates whether the current read is a result of a cache miss.The value of this pin at this time in other than read cycles is undefined. **Miss Address (3):** During the remainder of the read operation, this output presents address bit (3) of the address the processor was attempting to reference when the cache miss occurred. Regardless of whether a cache miss is being processed, this pin reports the transfer address during this time.
Diag(0)	O	**Diagnostic Pin 0.** This output distinguishes cache misses due to instruction references from those due to data references, and presents the remaining bit of the miss address. The value output on this pin is also time multiplexed: **I/$\overline{D}$:** If the "Cached" Pin indicates a cache miss, then a high on this pin at this time indicates an instruction reference, and a low indicates a data reference. If the read is not due to a cache miss but rather an uncached reference, then this pin is undefined during this phase. **Miss Address (2):** During the remainder of the read operation, this output presents address bit (2) of the address the processor was attempting to reference when the cache miss occurred. Regardless of whether a cache miss is being processed, this pin reports the transfer address during this time.
ALE	O	**Address Latch Enable:** Used to indicate that the A/D bus contains valid address information for the bus transaction. This signal is used by external logic to capture the address for the transfer, typically using transparent latches.
$\overline{DataEn}$	O	**External Data Enable:** This signal indicates that the A/D bus is no longer being driven by the processor during read cycles, and thus the external memory system may enable the drivers of the memory system onto this bus without having a bus conflict occur. During write cycles, or when no bus transaction is occurring, this signal is negated, thus disabling the external memory drivers

PIN DESCRIPTION (Continued):

PIN NAME	I/O	DESCRIPTION
Burst/ WrNear	O	**Burst Transfer/Write Near:** On read transactions, the Burst signal indicates that the current bus read is requesting a block of four contiguous words from memory. This signal is asserted only in read cycles due to cache misses; it is asserted for all I-Cache miss read cycles, and for D-Cache miss read cycles if selected at device reset time. On write transactions, the WrNear output tells the external memory system that the bus interface unit is performing back-to-back write transactions to an address within the same 256 word page as the prior write transaction. This signal is useful in memory systems which employ page mode or static column DRAMs, and allows near writes to be retired quickly.
Rd	O	**Read:** An output which indicates that the current bus transaction is a read.
Wr	O	**Write:** An output which indicates that the current bus transaction is a write.
Ack	I	**Acknowledge:** An input which indicates to the device that the memory system has sufficiently processed the bus transaction, and that the CPU may either terminate the write cycle or process the read data from this read transfer.
RdCEn	I	**Read Buffer Clock Enable:** An input which indicates to the device that the memory system has placed valid data on the A/D bus, and that the processor may move the data into the on-chip Read Buffer.
SysClk	O	**System Reference Clock:** An output from the CPU which reflects the timing of the internal processor "Sys" clock. This clock is used to control state transitions in the read buffer, write buffer, memory controller, and bus interface unit.
BusReq	I	**DMA Arbiter Bus Request:** An input to the device which requests that the CPU tri-state its bus interface signals so that they may be driven by an external master.
BusGnt	O	**DMA Arbiter Bus Grant.** An output from the CPU used to acknowledge that a BusReq has been detected, and that the bus is relinquished to the external master.
SBrCond(3:2) BrCond(1:0)	I	**Branch Condition Port:** These external signals are internally connected to the CPU signals CpCond(3:0). These signals can be used by the branch on co-processor condition instructions as input ports. There are two types of Branch Condition inputs: the SBrCond inputs have special internal logic to synchronize the inputs, and thus may be driven by asynchronous agents. The direct Branch Condition inputs must be driven synchronously.
BErr	I	**Bus Error:** Input to the bus interface unit to terminate a bus transaction due to an external bus error. This signal is only sampled during read and write operations. If the bus transaction is a read operation, then the CPU will take a bus error exception.
Int(5:3) SInt(2:0)	I	**Processor Interrupt:** During normal operation, these signals are logically the same as the Int(5:0) signals of the R3000. During processor reset, these signals perform mode initialization of the CPU, but in a different (simpler) fashion than the interrupt signals of the R3000. There are two types of interrupt inputs: the SInt inputs are internally synchronized by the processor, and may be driven by an asynchronous external agent. The direct interrupt inputs are not internally synchronized, and thus must be externally synchronized to the CPU. The direct interrupt inputs have one cycle lower latency than the synchronized interrupts.
Clk2xIn	I	**Master Clock Input:** This is a double frequency input used to control the timing of the CPU.
Reset	I	**Master Processor Reset:** This signal initializes the CPU. Mode selection is performed during the last cycle of Reset.
Rsvd(4:0)	I/O	**Reserved:** These five signal pins are reserved for testing and for future revisions of this device. Users must not connect these pins.

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ABSOLUTE MAXIMUM RATINGS(1, 3)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TC	Operating Case Temperature	0 to +85	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +155	°C
VIN	Input Voltage	–0.5 to +7.0	–0.5 to +7.0	V

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VIN minimum = -3.0V for pulse width less than 15ns. VIN should not exceed VCC +0.5 Volts.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

AC TEST CONDITIONS

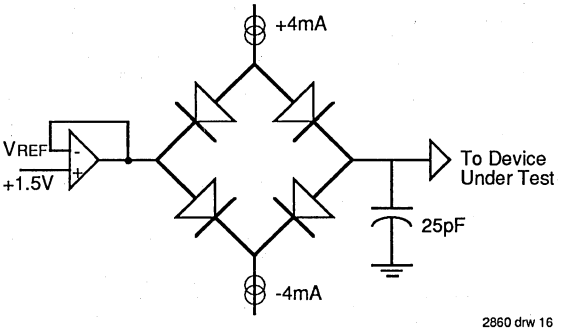
Symbol	Parameter	Min.	Max.	Unit
VIH	Input HIGH Voltage	3.0	—	V
VIL	Input LOW Voltage	—	0.4	V
VIHS	Input HIGH Voltage	3.5	—	V
VILS	Input LOW Voltage	—	0.4	V

2860 tbl 08

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C (Case)	0V	5.0 ±10%
Commercial	0°C to +85°C (Case)	0V	5.0 ±5%

OUTPUT LOADING FOR AC TESTING



2860 drw 16

DC ELECTRICAL CHARACTERISTICS— (T_C = 0°C to +85°C, V_{CC} = +5.0V ±5%)

Symbol	Parameter	Test Conditions	20MHz		25MHz		33.33MHz		40MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4mA	3.5	—	3.5	—	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage(3)	—	2.0	—	2.0	—	2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage(1)	—	—	0.8	—	0.8	—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage(2,3)	—	3.0	—	3.0	—	3.0	—	3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)	—	—	0.4	—	0.4	—	0.4	—	0.4	V
C_{IN}	Input Capacitance(4)	—	—	10	—	10	—	10	—	10	pF
C_{OUT}	Output Capacitance(4)	—	—	10	—	10	—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = 5V, T_A = 70°C	—	350	—	400	—	500	—	600	mA
I_{IH}	Input HIGH Leakage	V_{IH} = VCC	—	100	—	100	—	100	—	100	µA
I_{IL}	Input LOW Leakage	V_{IL} = GND	-100	—	-100	—	-100	—	-100	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	-100	100	-100	100	-100	100	-100	100	µA

2860 tbl 10

NOTES:

1. V_{IL} Min. = -3.0V for pulse width less than 15ns. V_{IL} should not fall below -0.5 Volts for larger periods.
2. V_{IHS} and V_{ILS} apply to Clk2xIn and $\overline{\text{Reset}}$.
3. V_{IH} should not be held above V_{CC} + 0.5 volts.
4. Guaranteed by design.

C

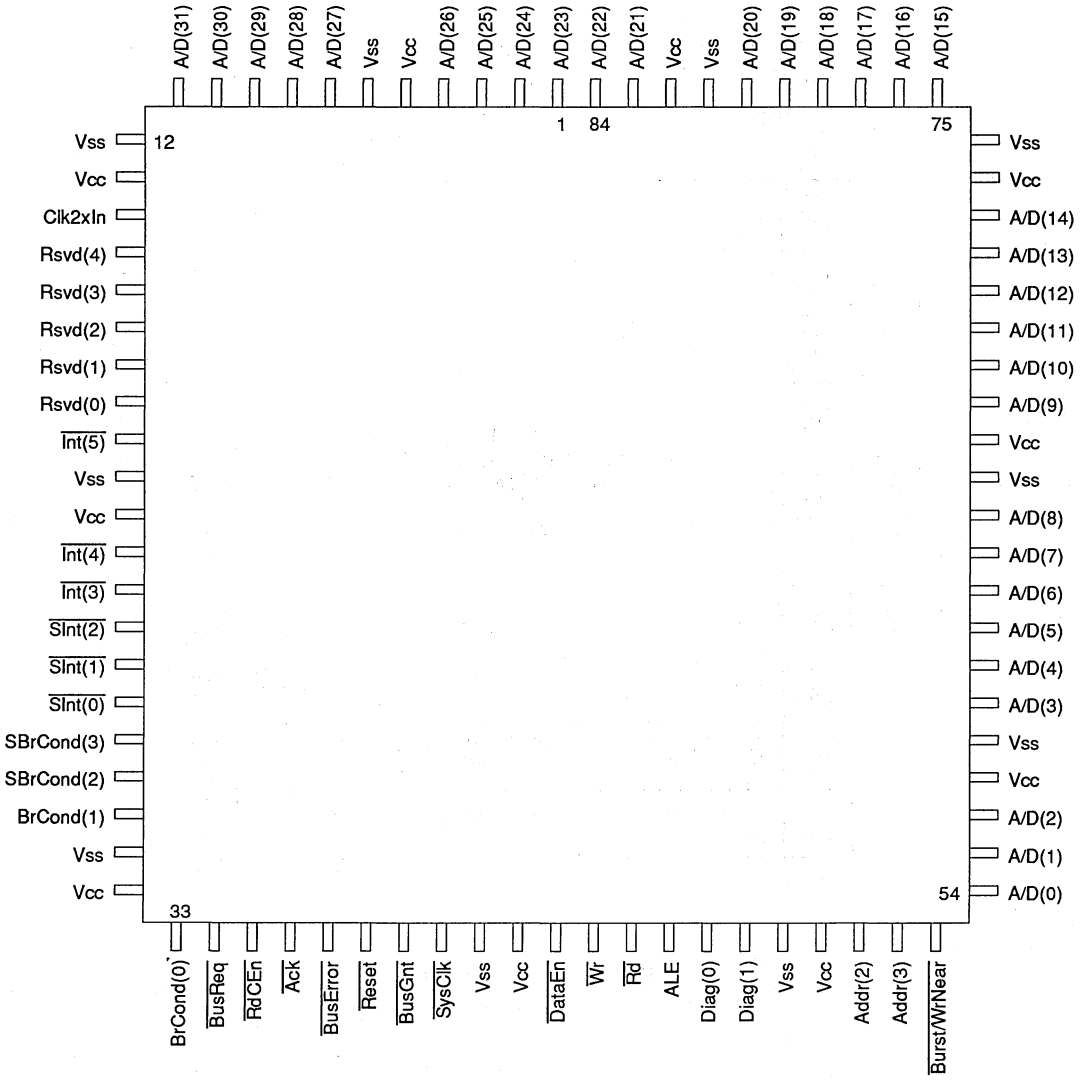
AC ELECTRICAL CHARACTERISTICS (1, 2, 3) — (Tc = 0°C to +85°C, Vcc = +5.0V ±5%)

Symbol	Signals	Description	20MHz		25MHz		33.33MHz		40MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t1	BusReq, Ack, BusError, SInt, RdCEn, Int, BrCond, SBrCond	Set-up to SysClk rising	6	—	5	—	4	—	3	—	ns
t1a	A/D	Set-up to SysClk falling	7	—	6	—	5	—	4	—	ns
t2	BusReq, Ack, BusError, SInt, RdCEn, Int, BrCond, SBrCond	Hold from SysClk rising	4	—	4	—	3	—	3	—	ns
t2a	A/D	Hold from SysClk falling	2	—	2	—	1	—	1	—	
t3	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Tri-state from SysClk rising	—	10	—	10	—	10	—	10	ns
t4	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Driven from SysClk falling	—	10	—	10	—	10	—	10	ns
t5	BusGnt	Asserted from SysClk rising	—	8	—	7	—	6	—	5	ns
t6	BusGnt	Negated from SysClk falling	—	8	—	7	—	6	—	5	ns
t7	Wr, Rd, Burst/WrNear, A/D	Valid from SysClk rising	—	5	—	5	—	4	—	3	ns
t8	ALE	Asserted from SysClk rising	—	4	—	4	—	3	—	2	ns
t9	ALE	Negated from SysClk falling	—	4	—	4	—	3	—	2	ns
t10	A/D	Hold from ALE negated(4)	2	—	2	—	1.5	—	1.5	—	ns
t11	DataEn	Asserted from SysClk falling	—	15	—	15	—	13	—	12	ns
t12	DataEn	Asserted from A/D tri-state(4)	0	—	0	—	0	—	0	—	ns
t14	A/D	Driven from SysClk rising(4)	0	—	0	—	0	—	0	—	ns
t15	Wr, Rd, DataEn, Burst/WrNear	Negated from SysClk falling	—	7	—	6	—	5	—	4	ns
t16	Addr(3:2)	Valid from SysClk	—	6	—	6	—	5	—	4	ns
t17	Diag	Valid from SysClk	—	7	—	7	—	6	—	5	ns
t18	A/D	Tri-state from SysClk falling	—	10	—	10	—	9	—	8	ns
t19	A/D	SysClk falling to data out	—	10	—	10	—	9	—	8	ns
t20	Clk2xIn	Pulse Width High	10	—	8	—	6.5	—	5	—	ns
t21	Clk2xIn	Pulse Width Low	10	—	8	—	6.5	—	5	—	ns
t22	Clk2xIn	Clock Period	25	—	20	—	15	—	12.5	—	ns
t23	Reset	Pulse Width from Vcc valid	200	—	200	—	200	—	200	—	µs
t24	Reset	Minimum Pulse Width	32	—	32	—	32	—	32	—	tsys
t25	Reset	Set-up to SysClk falling	6	—	5	—	4	—	3	—	ns
t26	Int	Mode set-up to Reset rising	6	—	5	—	4	—	3	—	ns
t27	Int	Mode hold from Reset rising	2	—	2	—	1	—	1	—	ns
t28	SInt, SBrCond	Set-up to SysClk falling	6	—	5	—	4	—	3	—	ns
t29	SInt, SBrCond	Hold from SysClk falling	2	—	2	—	1	—	1	—	ns
t30	Int, BrCond	Set-up to SysClk falling	6	—	5	—	4	—	3	—	ns
t31	Int, BrCond	Hold from SysClk falling	2	—	2	—	1	—	1	—	ns
tsys	SysClk	Pulse Width	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	
t32	SysClk	Clock High Time	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 1	t22 + 1	t22 - 1	t22 + 1	ns
t33	SysClk	Clock Low Time	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 1	t22 + 1	t22 - 1	t22 + 1	ns
tderate	All outputs	Timing deration for loading over 25pf(4, 5)	—	0.5	—	0.5	—	0.5	—	0.5	ns/ 25pF

NOTES:

1. All timings referenced to 1.5 Volts.
2. All outputs tested with 25 pF loading.
3. The AC values listed here reference timing diagrams contained in the R3051 Family Hardware User's Manual.
4. Guaranteed by design.
5. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25 pF over the specified test load condition.

PIN CONFIGURATIONS



84-Pin PLCC with or without Integral Thermal Slug

Top View

Note:
Reserved Pins must not be connected.

PIN CONFIGURATIONS (CONTINUED)

	1	2	3	4	5	6	7	8	9	10	11	12
M	Vss	Clk2xIn	Rsvd (4)	Rsvd (2)	Rsvd (0)	Vss	$\overline{\text{Int}}$ (4)	$\overline{\text{Int}}$ (3)	$\overline{\text{SInt}}$ (1)	S BrCond (3)	S BrCond (2)	BrCond (0)
L	A/D (28)	A/D (30)	Vcc	Rsvd (3)	Rsvd (1)	$\overline{\text{Int}}$ (5)	Vcc	$\overline{\text{SInt}}$ (2)	$\overline{\text{SInt}}$ (0)	BrCond (1)	Vss	$\overline{\text{RdCEn}}$
K	A/D (27)	A/D (29)	A/D (31)							Vcc	$\overline{\text{BusReq}}$	$\overline{\text{Ack}}$
J	Vcc	Vss									$\overline{\text{Bus Error}}$	$\overline{\text{Reset}}$
H	A/D (25)	A/D (26)									$\overline{\text{BusGnt}}$	$\overline{\text{SysClk}}$
G	A/D (23)	A/D (24)									Vcc	Vss
F	A/D (21)	A/D (22)									$\overline{\text{Wr}}$	$\overline{\text{DataEn}}$
E	Vcc	Vss									$\overline{\text{ALE}}$	$\overline{\text{Rd}}$
D	A/D (20)	A/D (19)									Diag (1)	Diag (0)
C	A/D (18)	A/D (16)	Vss							$\overline{\text{Burst/ WrNear}}$	Addr (2)	Vss
B	A/D (17)	Vcc	A/D (14)	A/D (11)	A/D (9)	A/D (8)	A/D (6)	A/D (4)	Vss	A/D (1)	Addr (3)	Vcc
A	A/D (15)	A/D (13)	A/D (12)	A/D (10)	Vcc	Vss	A/D (7)	A/D (5)	A/D (3)	Vcc	A/D (2)	A/D (0)

R3051
84-Pin Ceramic Pin Grid Array
(Cavity Down)

Bottom View

84-Pin PGA with Integral Thermal Slug
BottomView

Note:
Reserved Pins must not be connected.

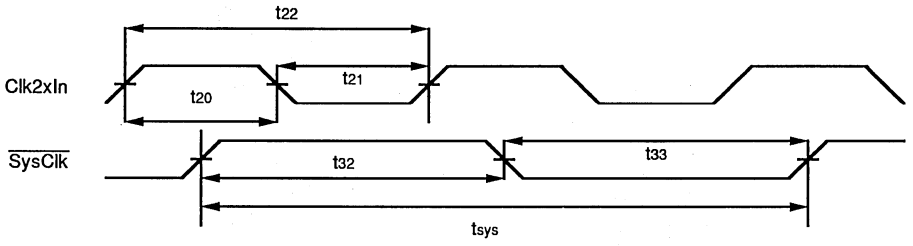


Figure 8. R3051 Family Clocking

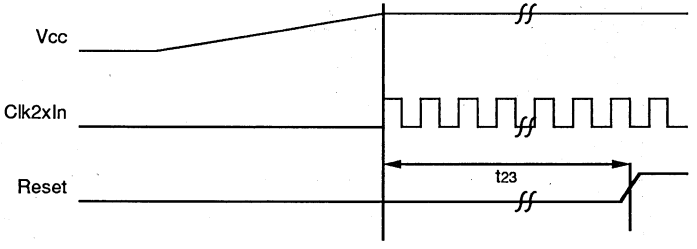


Figure 9. Power-On Reset Sequence

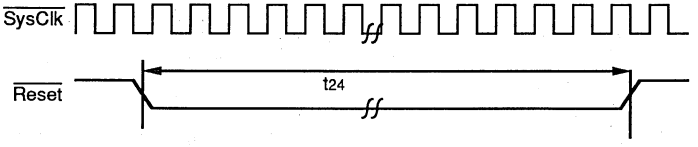


Figure 10. Warm Reset Sequence

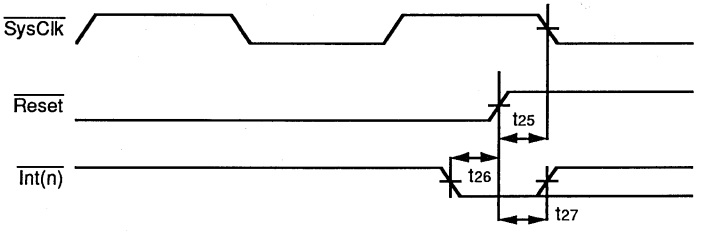


Figure 11. Mode Selection and Negation of Reset

C

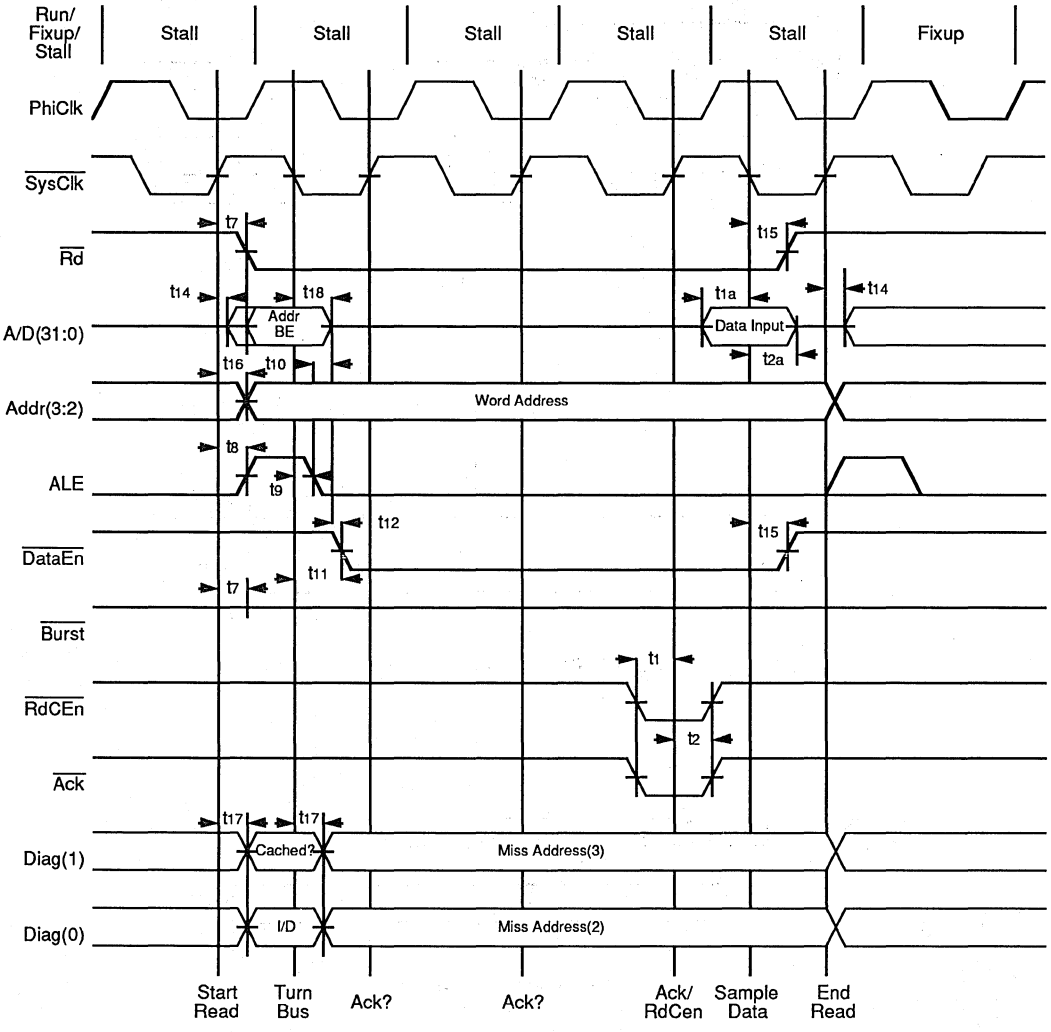


Figure 12. Single Datum Read in R3051 Family

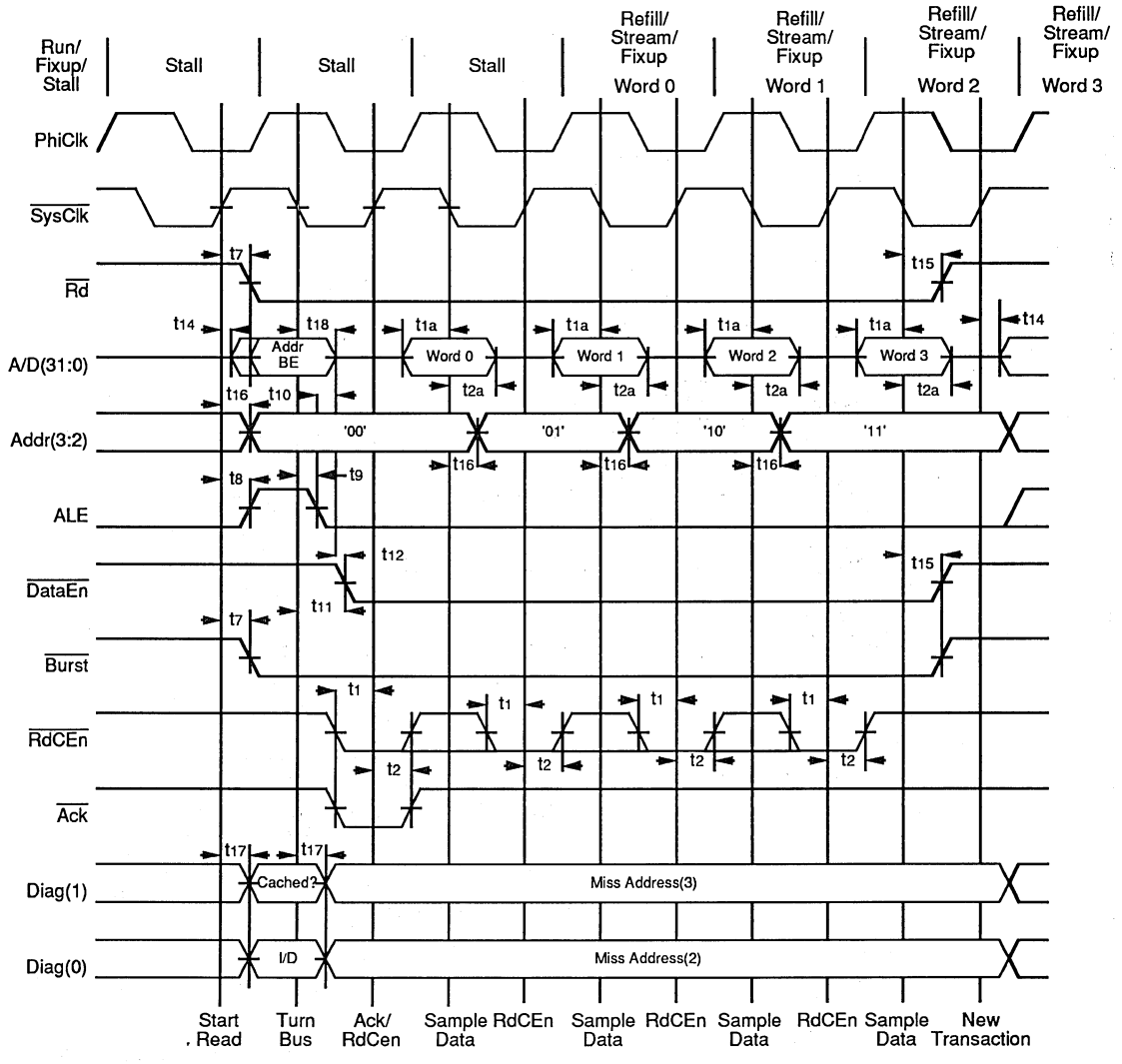


Figure 13. R3051 Family Burst Read

C

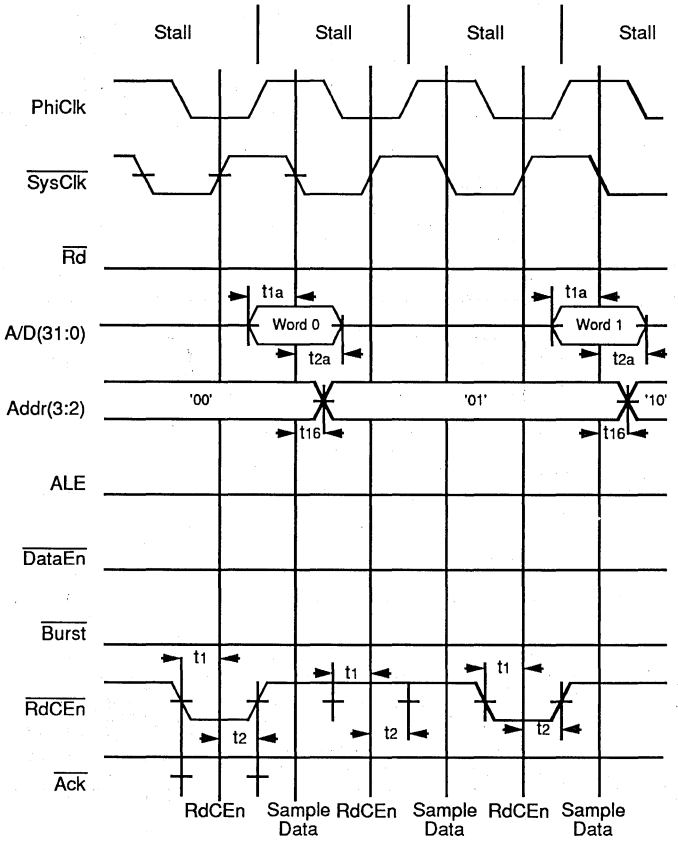


Figure 14 (a). Start of Throttled Quad Read

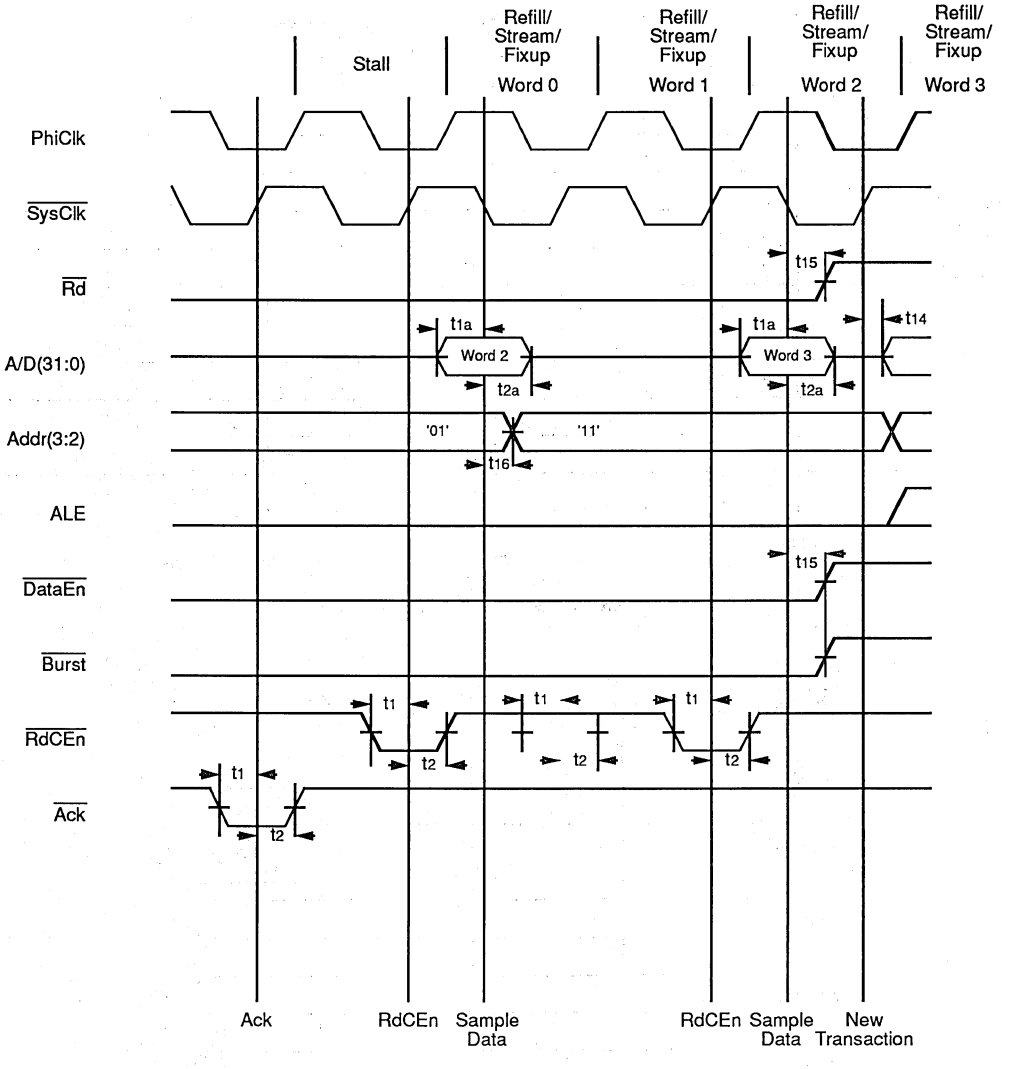


Figure 14 (b). End of Throttled Quad Read

C

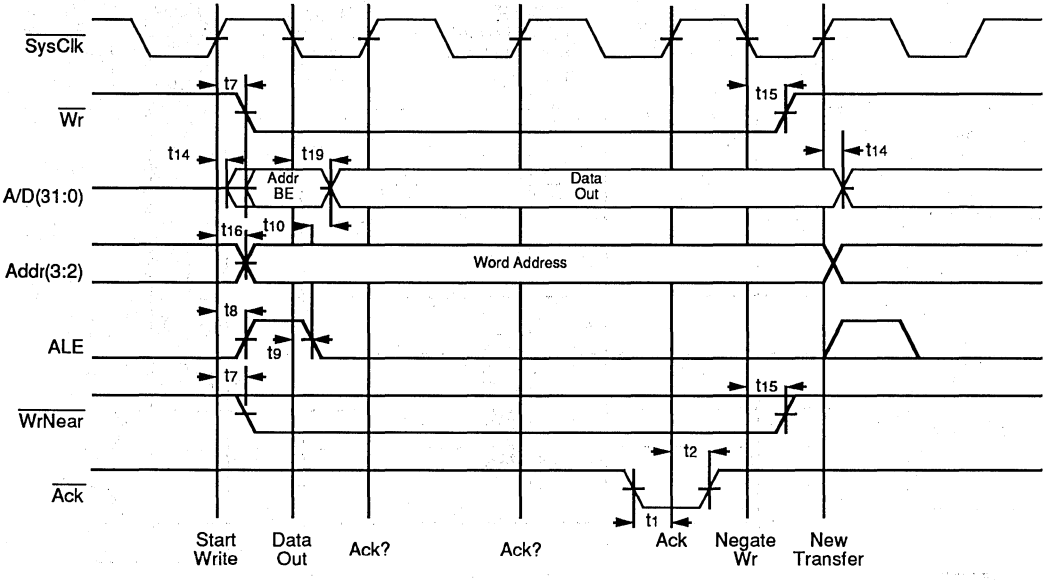


Figure 15. R3051 Family Write Cycle

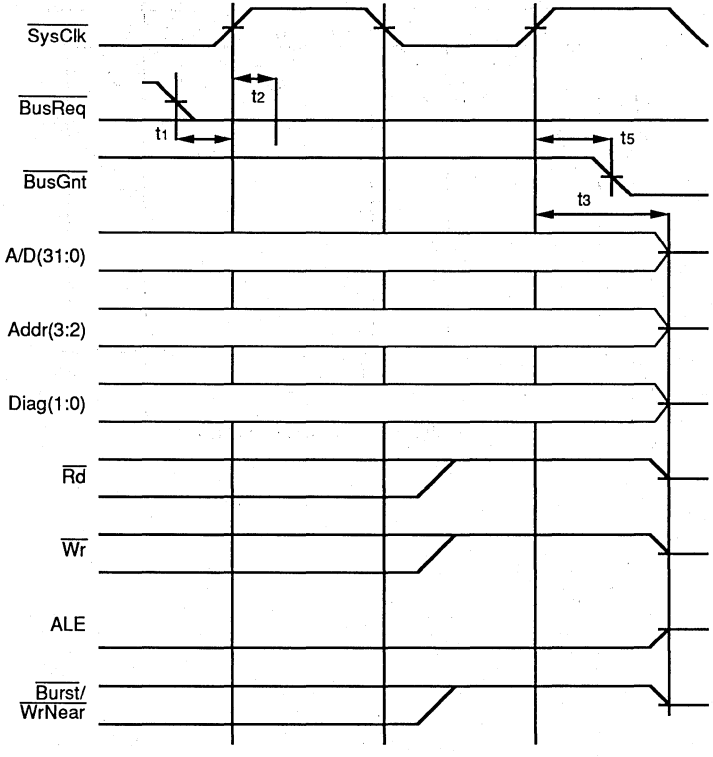


Figure 16. Request and Relinquish of R3051 Family Bus to External Master

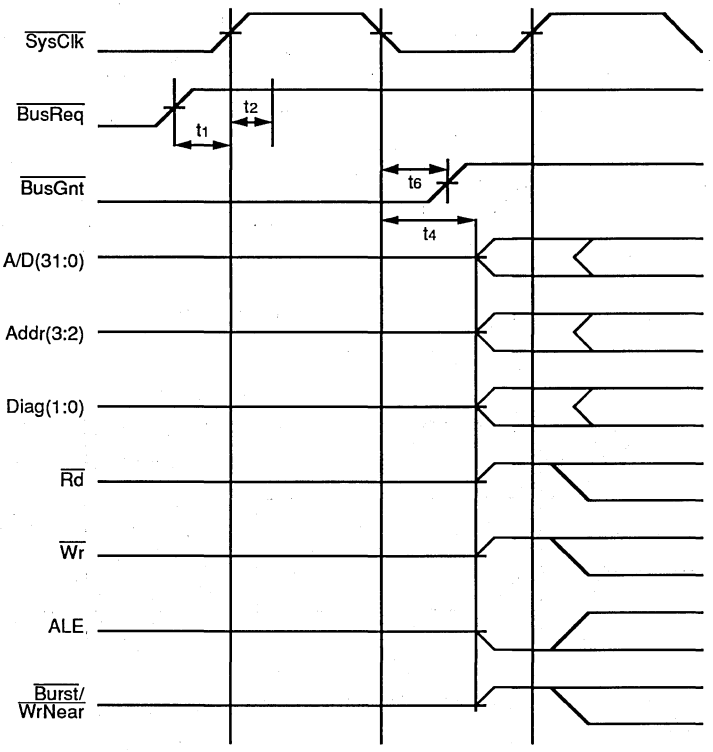


Figure 17. R3051 Family Regaining Bus Mastership

C

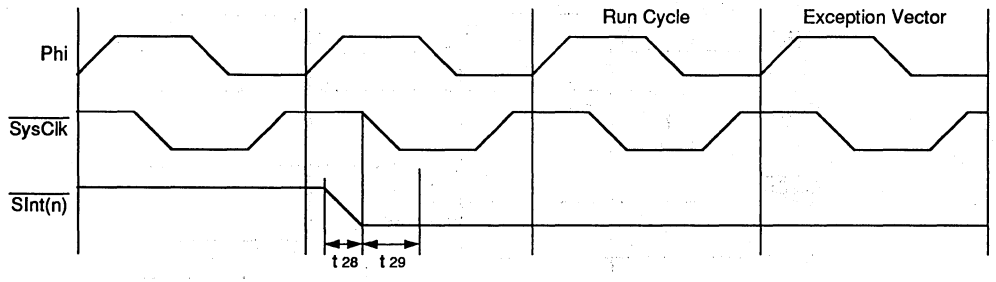


Figure 18. Synchronized Interrupt Input Timing

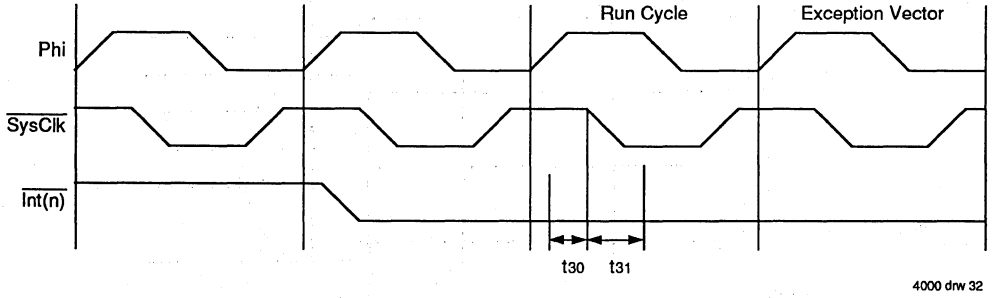


Figure 19. Direct Interrupt Input Timing

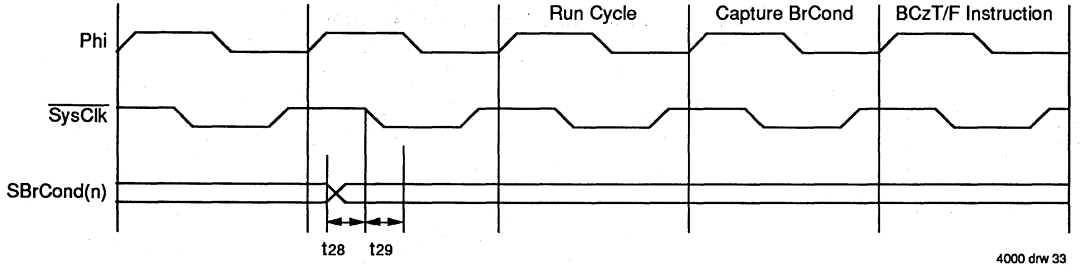


Figure 20. Synchronized Branch Condition Input Timing

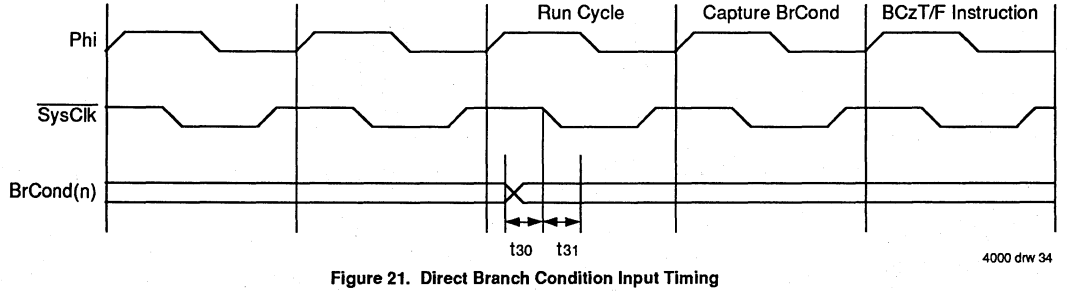
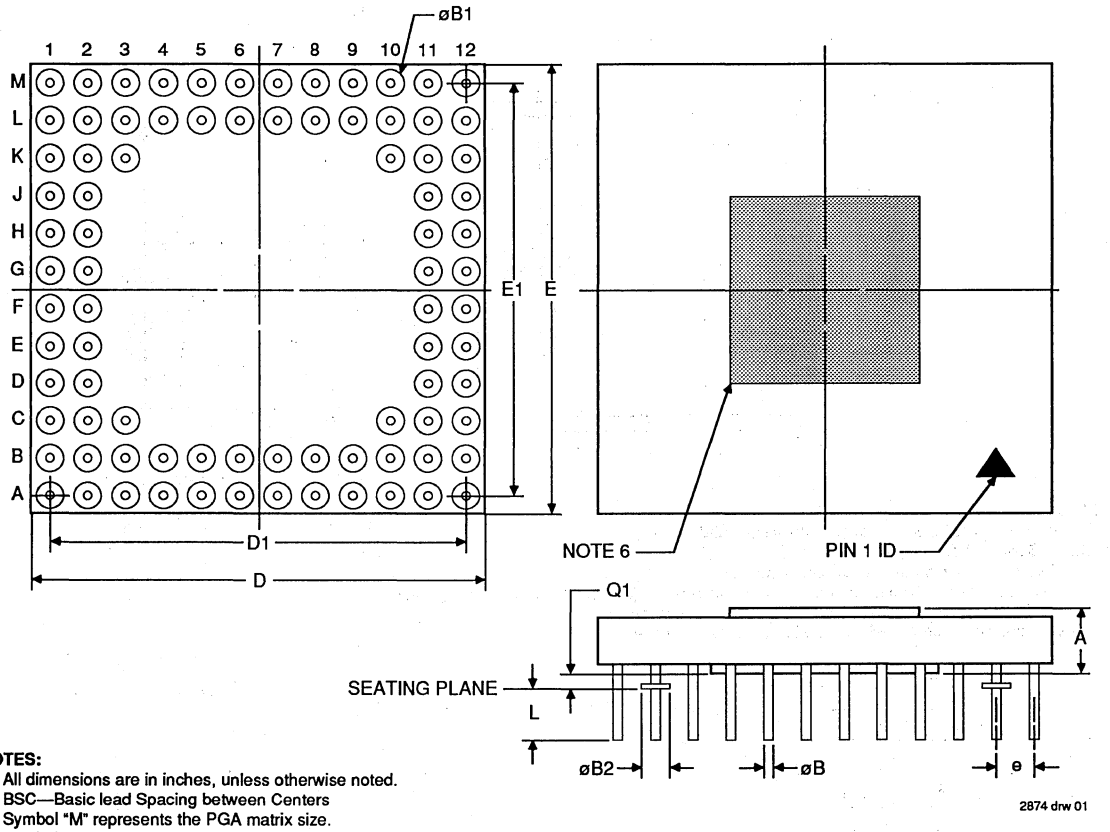


Figure 21. Direct Branch Condition Input Timing

84-PIN PGA (CAVITY DOWN)

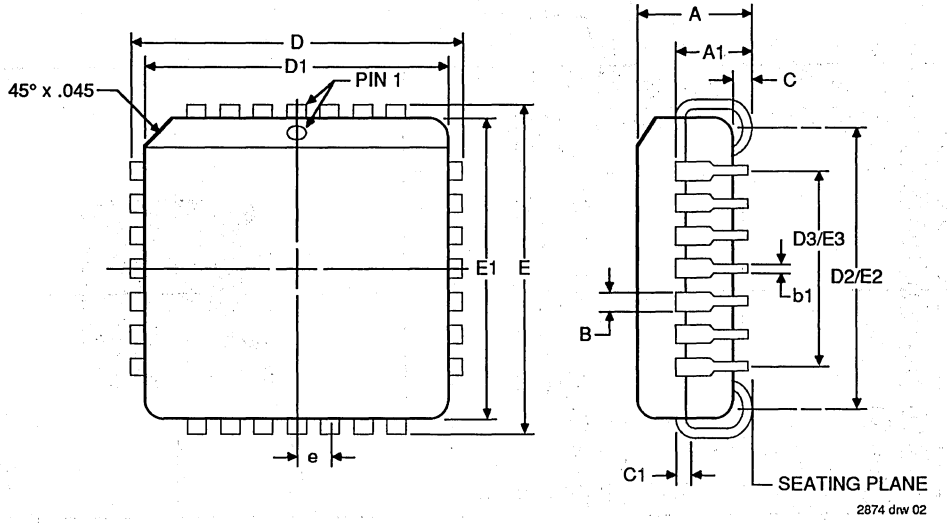


NOTES:
1. All dimensions are in inches, unless otherwise noted.
2. BSC—Basic lead Spacing between Centers
3. Symbol "M" represents the PGA matrix size.
4. Symbol "N" represents the number of pins.
5. Chamfered corners are IDT's option.
6. Shaded area indicates integral metallic heat sink.

Drawing #	G84-4	
Symbol	Min	Max
A	.077	.145
øB	.016	.020
øB1	.060	.080
øB2	.040	.060
D/E	1.180	1.235
D1/E1	1.100 BSC	
e	.100 BSC	
L	.120	.140
M	12	
N	84	
Q1	.025	.060

C

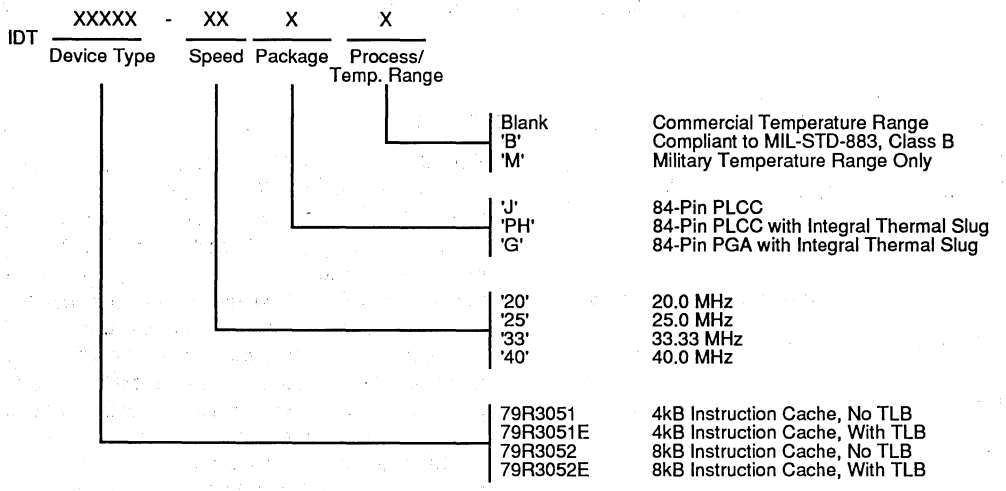
84 LEAD PLCC (SQUARE)



NOTES:
1. All dimensions are in inches, unless otherwise noted.
2. BSC—Basic lead Spacing between Centers.
3. D & E do not include mold flash or protutions.
4. Formed leads shall be planar with respect to one another and within .004" at the seating plane.
5. ND & NE represent the number of leads in the D & E directions respectively.
6. D1 & E1 should be measured from the bottom of the package.

DWG #	J84-1	
# of Leads	84	
Symbol	Min.	Max.
A	165	.180
A1	.095	.115
B	.026	.032
b1	.013	.021
C	.020	.040
Cl	.008	.012
D	1.185	1.195
D1	1.150	1.156
D2/E2	1.090	1.130
D3/E3	1.000 REF	
E	1.185	1.195
E1	1.150	1.156
e	.050 BSC	
ND/NE	21	

ORDERING INFORMATION



VALID COMBINATIONS

IDT	79R3051 - 20, 25	All packages
	79R3051E - 20, 25	All packages
	79R3052 - 20, 25	All packages
	79R3052E - 20, 25	All packages
	79R3051 - 33, 40	PGA, PH Packages Only
	79R3051E - 33, 40	PGA, PH Packages Only
	79R3052 - 33, 40	PGA, PH Packages Only
	79R3052E - 33, 40	PGA, PH Packages Only

C

Integrated Device Technology, Inc.

R3000 CPU MODULES

IDT7RS109

FEATURES:

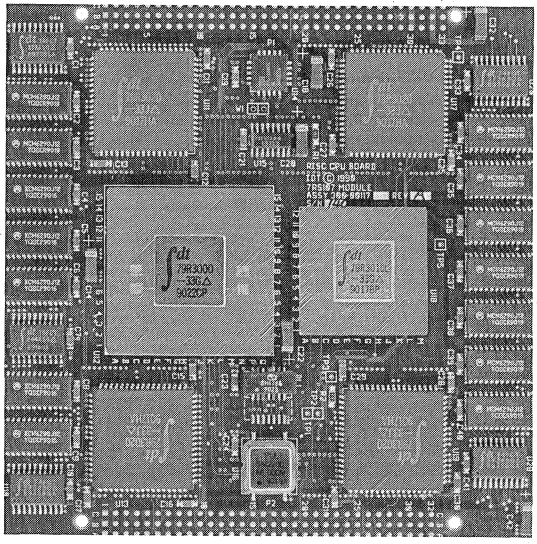
- Cache Size: 64K Instruction, 64K Data
- Processor Speeds up to 33 MHz
- Includes R3010 Floating Point Accelerator
- 1-word Read Buffer; 4-word Write Buffer
- Supports R3000 Multiprocessor Features
- On-Board Parity Check and Generate
- Four or Eight-word block refills
- On-board oscillator, delay line, and reset circuitry
- 100% burn-in and functional test at rated speed

R3000 MODULE FOR HIGH PERFORMANCE CPUs AND MULTIPROCESSOR SYSTEMS:

The IDT7RS109 is a complete reduced instruction set computer (RISC) CPU, based on the MIPS R3000 RISC processor, and supplied on a small fully-tested high-density plug-in module. The module includes the R3000 CPU, the R3010 Floating Point Accelerator, 64 Kbytes each of data and instruction cache memory, a single word read buffer and a four-word write buffer. Clock generation, reset, control, parity, and interrupt functions are included on the module to simplify the remainder of the system design.

The 109 module includes a latch to hold an external address for snooping in the D-cache and is designed to support the R3000's multiprocessor features.

The module is constructed using surface mount devices on a 5.2" by 5.2" epoxy laminate board, and is connected to the user's system via 192 pins located in two pin row regions on the board.



7RS109 Module. Actual Size 5.2" x 5.2 "

ARCHITECTURAL HIGHLIGHTS

Uses R3020 Write Buffers

R3020 chips are used on the module to provide a "smart" four-deep write buffer between the CPU and external memory. These devices store data and addresses for up to four write requests to main memory, and handle the hand-shaking with the memory controller. The R3020s support features such as byte gathering (combining multiple byte writes to the same address in the buffer into a single write) and address matching (a read or write to an address already in the write buffer will be detected so the user software can take appropriate action). The R3020's Match signals are OR'ed on the module to produce a single output, labeled CONFLICT.

Four or Eight-Word Block Refill

The module refills both the instruction and data caches from memory in either four or eight-word blocks. The block refill size is set by a jumper on the module. Following a cache miss, the processor will request a memory read at the missed address and wait for a data ready acknowledgement. When an acknowledge is received, the processor will load four or eight words into cache on four or eight successive clock cycles. The memory interface must supply the correct four or eight words (address A4A3A2 = 0 to 7) at the processor's speed, 40 ns intervals for a 25 MHz system. Interleaved memory is usually the best way to support this requirement. The processor's CPC0 pin, available as a pin on the module, can be used to over-ride the block refill. The processor performs instruction streaming during the refill.

On-board Oscillator and Delay Line

All the clock generation circuitry required by the R3000 system is on the module. A jumper can be used to select between the on-board crystal oscillator or an external oscillator input. A delay line on the module is used to set the timing for register strobes and other critical signals relative to the R3000 clock. The R3000 clock output "SYSOUT" is made available to the user system through eight pins on the module, each independently buffered.

R3000 Reset and Initialization Logic

The initialization logic for the R3000 CPU is contained on the module. A "Cold Reset" pin on the module starts the required 15 ms reset signal to the CPU, and then provides the initialization vectors during the last few cycles. A second reset pin is provided to reinitialize the CPU without repeating the 15 ms delay. The R3000 is initialized to "Big-Endian" operation.

Five User Interrupt Lines

Five pins on the module are used for user interrupt inputs. The user interrupts are synchronized in registers on the module before being sent to the R3000. Interrupt 2 is used for the Floating Point Accelerator, if present.

External R3000 Condition Code Pin

The R3000 input CPC0 is available as a pin on the module. During run cycles, this pin acts as a Condition Code test pin, so the R3000 can do a Test and Branch in a single cycle based on its state. During read stalls, the pin determines whether a single word or 8 words will be read. Reads into the instruction cache must always be block refills.

Internal Parity Check and Generate

The 7RS109 uses IDT 73211 registers for the data read buffer. This device provides the ability to generate parity on incoming data, if it is not already present, or to check parity on outgoing data to detect parity errors occuring on the module.

TYPICAL APPLICATIONS

The 7RS109 module is designed for applications that run complex operating systems, such as UNIX™, or that need the maximum possible performance. The module contains the maximum possible cache sizes (64K each) that can be supported by the R3000 in Multiprocessor configurations.

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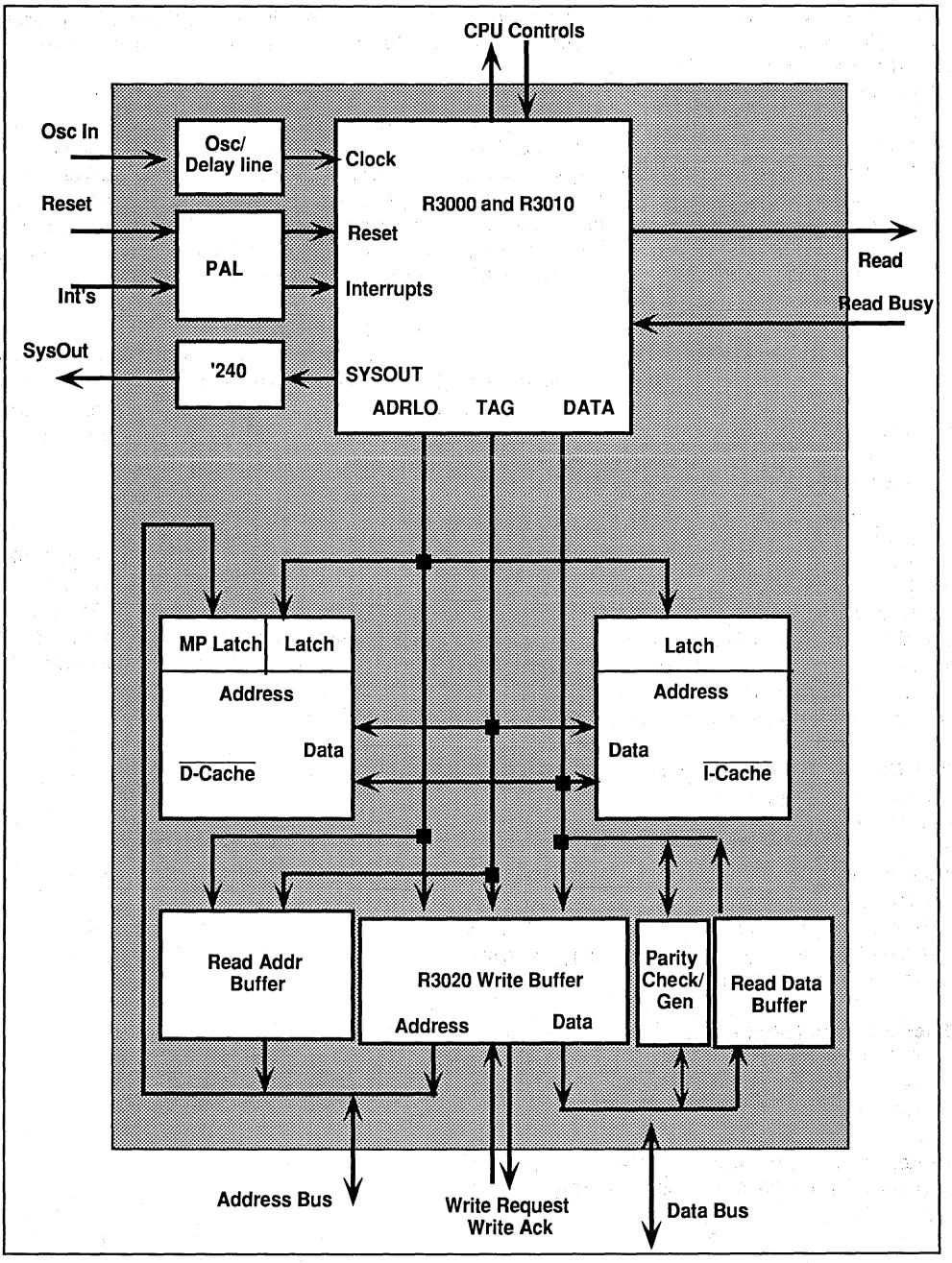
FUNCTIONAL BLOCK DIAGRAM



SIGNALS PROVIDED ON MODULE PINS

Signal Name	Type	Description
MA0...MA31	I/O	32-bit address from the module to external memory. This is an output from the 3020 Write Buffer except during the MP Invalidate function, when it is the input to the MP cache address latch.
MD0...MD31	I/O	32-bit data bus between the module and external memory. Driven from the 3020 Write Buffer during writes; input to the Read Data Buffer during reads.
BACT0,1,2	O	The three R3000 AccType status signals, driven from the 3020 Write Buffer during writes and from a latch during reads.
MDP0...MDP3	I/O	The four parity bits for the MD data. Output during writes and input during reads.
CP_CpCond0, 2, 3	I	The three flag inputs to the R3000 CPU. CPC0 is used during read stalls to control block refill of the data cache. (The instruction cache must always be block refilled.) CPC2 and CPC3 are the MP stall and invalidate controls.
ALOE	I	Data Cache Address Latch Output Enable When LOW, enables the output of the latch holding the data cache address supplied by the R3000. It should be LOW at all times except when the MP Latch is being used to invalidate a cache address.
BSYSOUT2...9	O	Eight buffered inverted copies of the R3000 signal "SYSOUT" for use in the user's system.
UINT0,1,3,4,5	I	Interrupt inputs to the R3000. These signals are synchronized to SYSOUT on the module. R3000 interrupt 2 is used for the Floating Point Accelerator.
BRESET	O	Buffered copy of the reset signal created on the module to reset the CPU. LOW during Reset.
WB_WbFull	O	Write Busy. Status signal created by the R3020 write buffer. Goes LOW to indicate the buffer is full.
CPU_BusError	I	Input to the R3000 indicating a bus error has occurred.
RESETC	I	Cold Reset to the module. The module creates a 15 ms long reset to the R3000 and executes the R3000 initialization sequence when this pin goes LOW.
FP_FpPresent	O	This signal can be used to detect the presence of an FPA on the module. To be used, it must be connected to a 4.7K pullup resistor. The pin will be LOW if the FPA is present.
WB_OutEn	I	Write Buffer Output Enable. When LOW, turns on the outputs of the R3020 write buffers.
WB_Request	O	Output from the R3020 to indicate that there is data in the buffer to be written to memory. Active LOW
WB_Acknowledge	I	Input to the R3020 to indicate data has been written into memory.
CONFLICT	O	The OR of all the R3020 Match signals; indicates the address on the R3020 inputs matches one of the addresses currently in the write buffer.
RABOE	I	Read Address Buffer Output Enable. When LOW, turns on outputs of the buffers containing the read address.
RDBCE	I	Read Data Buffer Clock Enable. When LOW, enables the clock (SYSOUT) to the Read Data Buffers.
READ	O	Status signal output. LOW during reads.
RABLE	I	Read Address Buffer Latch Enable. When HIGH, enables the Read Address Buffer latches.
WB_LatchErrAddr	I	Latch Error Address input to the R3020.
WB_EnErrAddr	I	Enable Error Address input to R3020.
CP_MemRd	O	R3000 output signal. When LOW, there is a request for a read from external memory.
CP_RdBusy	I	Read Busy. Input to the R3000 to indicate acknowledgment of the MEMRD request.
EXTOSC	I	Optional Input from External Oscillator

RELATED PRODUCTS

Prototyping System

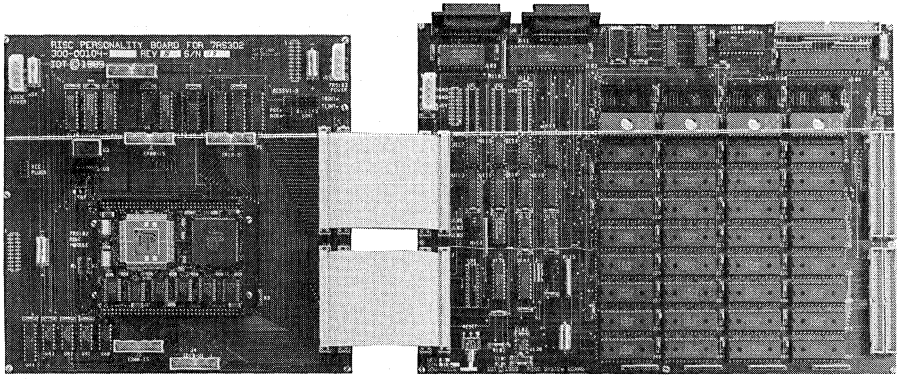
The 7RS109 module can be placed into immediate service using our flexible 7RS309 Prototyping Platform. The system includes two boards: a general purpose CPU board, and a personality card that interfaces the module to the CPU board.

The CPU board contains 1Mb of main memory, 256K of EPROM, two RS232 serial ports, an 8254 counter/timer, and an 8-bit parallel port accessible through a dual port RAM. Four 50-pin connectors provide access to all the address, data, and control signals for external connection to additional hardware on, for example, a wire-wrap board.

The system includes IDT's Software Integration Manager, which provides facilities for downloading code, examining memory, and stepping through programs.

The personality card is on a separate board, and provides a bed for the module, necessary control signals, and connectors for an HP 16500 Logic Analyzer.

Code for the R3000 can be created on a MIPS development system, on IDT's MacStation™ system, or using IDT's PC-based cross assembler and compiler products. Assembled code can be downloaded into the Prototyping System for execution and debug.



A Module Prototyping Platform.
The card on the left is the personality card with a module; the card on the right is the general purpose CPU.

SPECIFICATIONS

CPU
R3000

Floating Point
R3010 optional in either configuration. If present, connected to INT2.

Cache Ram
64 KB I-cache (16K words)
64 KB D-cache (16K words)

Cacheable Address Space
4 GBytes

MP Support
Cache invalidate supported

Block Refill
4 or 8 word (or single word)

Endianess
User programmable via module pin.

Read/Write Buffers
1 - Word Read Buffer
4 - Word Write Buffer

Interrupts
6 User Interrupts, synchronized with SYSOUTA:D in an on-board register.

I/O characteristics
TTL levels from FCT logic devices, PALs and R3000

Power Supply
4.5 amps (typical) at 5.0 V, 25°C, at 33MHz.

Environmental Conditions
Ambient temperature 0°C to +50°C.
Relative Humidity 5% to 95%

Clock Frequencies
20, 25 and 33 MHz

Interconnection
192 18-mil round pins on 100-mil centers
Mating connector: Samtec SS-1 series socket strips or equivalent.

User Selectable Options via jumpers:
4 word or 8 word block refill
Big or Little Endian
Streaming/No Streaming
Store Partial On/Off

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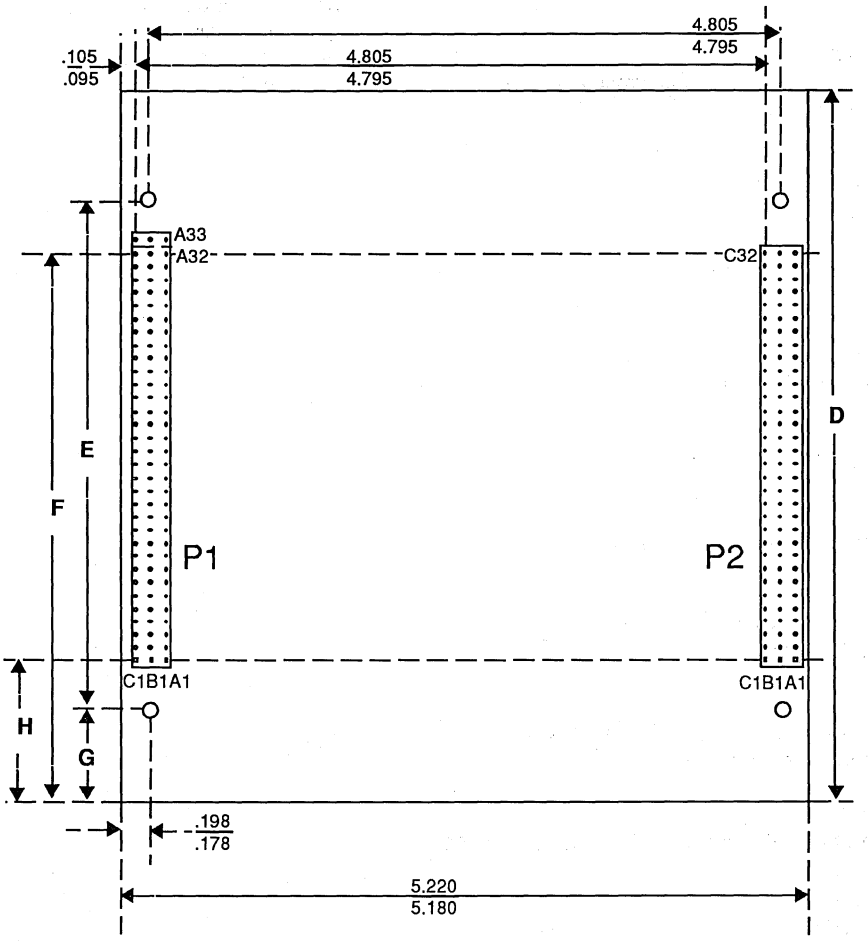
MECHANICAL OUTLINE

7RS109 TOP VIEW



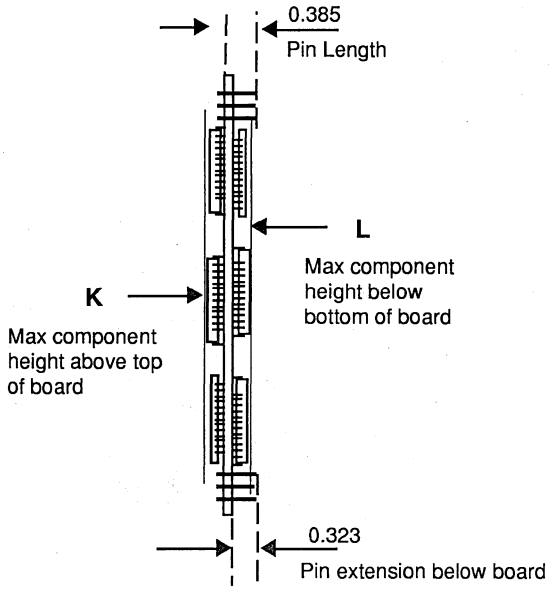
	7RS107-66		7RS108-88		7RS109-66	
	Min.	Max.	Min.	Max.	Min.	Max.
D	5.180	5.220	5.380	5.420	5.180	5.220
E	3.545	3.555	3.545	3.555	3.545	3.555
F	4.145	4.155	4.245	4.255	4.145	4.155
G	0.815	0.835	0.915	0.935	0.815	0.835
H	1.045	1.055	1.145	1.155	1.045	1.055
K		0.30		0.30		0.30
L		0.20		0.15		0.20

NOTES:

1. All dimensions in inches unless otherwise noted.
2. The 7RS107, 108 and 109 are a family of modules. Dimensions for all three are listed here, so that you can add flexibility by accepting all three modules.
3. P1 on the 7RS107 has three rows of 33 pins, while P1 on the 7RS108/9 has three rows of 32 pins.
4. Mounting holes are 0.109 ± .002. Note that mounting holes are offset from center line of connector.
5. Holes take #2 mounting hardware.
6. Pins are 0.018 diameter on 0.100 spacing on both axis.
7. To connect the modules use strip connectors Rob. Nug. SBE-32-S-TG for 32 pins, Rob. Nug. SBE-33-S-TG for 33 pins or equivalent.

MECHANICAL OUTLINE

7RS109 SIDE VIEW



	7RS107-66		7RS108-88		7RS109-66	
	Min.	Max.	Min.	Max.	Min.	Max.
D	5.180	5.220	5.380	5.420	5.180	5.220
E	3.545	3.555	3.545	3.555	3.545	3.555
F	4.145	4.155	4.245	4.255	4.145	4.155
G	0.815	0.835	0.915	0.935	0.815	0.835
H	1.045	1.055	1.145	1.155	1.045	1.055
K		0.30		0.30		0.30
L		0.20		0.15		0.20

NOTES:

1. All dimensions in inches unless otherwise noted.
2. Pins are 0.018 diameter on 0.100 spacing on both axis.
3. Board thickness 0.062 ± .007.
4. To connect the modules use strip connectors Rob. Nug. SBQ-32-S-TG for 32 pins, Rob. Nug. SBE-33-S-TG for 33 pins or equivalent.

ORDERING INFORMATION

Ordering Part Number	CPU	FPA	I-cache	D-cache	Speed	Other
7RS109N66A16A	R3000A	NONE	64K	64K	16 MHz	
7RS109N66A20A	R3000A	NONE	64K	64K	20 MHz	
7RS107N66A25A	R3000A	NONE	64K	64K	25 MHz	
7RS107N66A33A	R3000A	NONE	64K	64K	33 MHz	
7RS109F66A16A	R3000A	R3010A	64K	64K	16 MHz	
7RS109F66A20A	R3000A	R3010A	64K	64K	20 MHz	
7RS109F66A25A	R3000A	R3010A	64K	64K	25 MHz	
7RS109F66A33A	R3000A	R3010A	64K	64K	33 MHz	

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CUSTOM OPTIONS

Some features of the 7RS109 can be modified by special order. Contact your IDT sales office for details. Possible modifications include: initialization mode for the R3000, endian option, size of block refill, instruction streaming, pin length, style, and plating; special marking; additional burn-in, and socketing of the CPU and/or FPA.

ADDITIONAL INFORMATION

For Detailed design information, contact IDT and ask for the 7RS109 Designer's guide.

Integrated Device Technology, Inc.

NEW! Version 3.0

IDT/sim
SYSTEM INTEGRATION MANAGER
ROMable DEBUGGING KERNEL

IDT7RS901

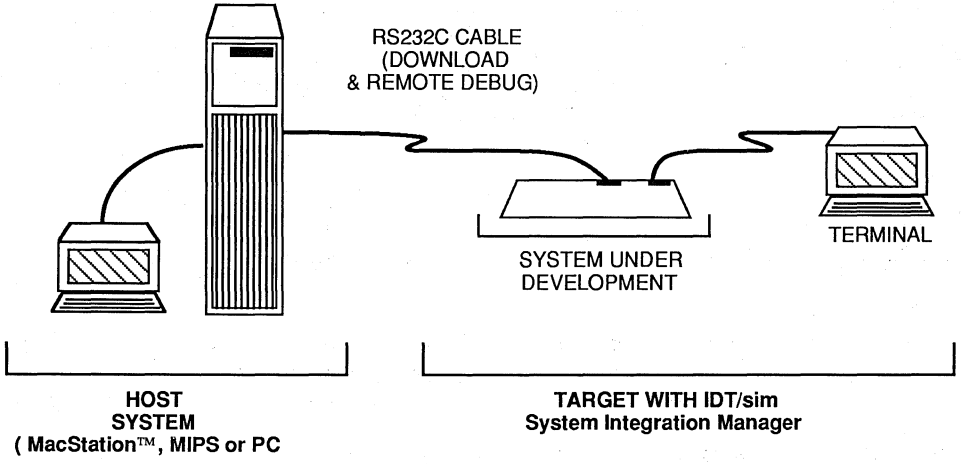
FEATURES:

- **Provides complete control over hardware and software for system integration**
- **Fits in 96Kb of EPROM space, plus 18Kb of RAM**
- **Provides CPU control for register and memory manipulation, cache access, and TLB management**
- **Includes Diagnostic tests for Memory, Cache, MMU, FPU, and System**
- **Easy to add new commands and new I/O drivers**
- **Complete support for MIPS symbolic debugger**
- **In-line assembly and disassembly**

POWERFUL TOOL FOR R3000 SOFTWARE/ HARDWARE INTEGRATION:

The IDT7RS901 System Integration Manager (IDT/sim) is a ROMable software product that permits convenient control and debug of RISC systems built around the MIPS R3000 architecture. It permits users to quickly develop and debug stand-alone systems. Facilities are included to operate the CPU under controlled conditions, examining and altering the contents of memory, manipulating and controlling R3000 resources (such as cache, TLB and coprocessors), loading programs from host machines, and controlling the path of execution of loaded programs. Remote (source/symbolic) debugging is also supported.

IDT/sim requires 96Kb of EPROM space for code and data and 18Kb of ram space for uninitialized variable data and stack.



IDT/SIM FEATURES

IDT/sim is a software tool to help system designers debug hardware designs and port software to systems based on one of the MIPS Instruction Set Architecture CPUs. The software is supplied in EPROMs on most IDT RISC SubSystem Development products, and may be purchased in source code form so it can be compiled and installed on any R3000 compatible hardware.

IDT/sim provides all the basic functions needed to get a new hardware design debugged and to port and debug software on it. Typically, the monitor is compiled and burned into EPROMs that are plugged into the target system. Approximately 96KB of EPROM are needed for the binary code, and 18KB of RAM are needed for storing variables. Once installed, the designer communicates with the monitor via a simple terminal connected to an RS-232 port on the target system. Source code is included to support a variety of UARTs for this port. On start-up, the monitor will determine the cache and main memory sizes automatically.

DIAGNOSTICS

The monitor includes a set of diagnostic routines for testing the integrity of the hardware.

Main Memory Test: Finds opens, shorts, and stuck-at faults on data and address lines. A cache memory test runs memory tests on both caches, checks tag memory, and verifies that instructions can be executed from cache.

System Test: Checks the ability to read and store full words, half words, and bytes. Checks cache operation for valid, hit/miss, and invalidation.

MMU Test: Checks operation of TLB inside the R3000.

Floating Point Test: Tests the functionality of the R3010 FPU, including exception interrupts.

DOWNLOAD SUPPORT

Object code created on a software development system can be downloaded in either ASCII S-records or binary formats to the target system's memory. The code can be produced with the MIPS development tools or with IDT/c on any of a number of development platforms, including a 286 or 386 PC or SUN SparcStation.

IDT/sim includes utilities to convert object code from the MIPS compiler to S-records, to convert the S-records to a binary format (which is more compressed and downloads faster), and to download the binary records to the target. Similar utilities for use with the IDT/c multi-host C compiler are supplied with IDT/c.

A terminal emulation feature allows the terminal being used as the IDT/sim console to be used also as a terminal to a software development system accessed through a second serial port.

DEBUG COMMANDS

There are a variety of commands included in IDT/sim to support software/hardware debug.

Execution Control: Breakpoint, call, gotill, step, etc.

Memory Commands: Assemble, disassemble, dump, flush cache, etc.

TLB Commands: Dump, flush, map, etc.

Remote Debug: Turns on remote debug with DBX on a MIPS RISC/os system.

RUN-TIME SUPPORT

IDT/sim includes over 40 functions that can be called by user's programs to perform common I/O and R3000 control operations. A complete list of the commands is listed later in this document.

NEW FEATURES IN VERSION 3.0

Interactive Assembler. A command has been added that allows the user to enter R3000 instructions into memory using assembly language mnemonics.

Floating Point R3010 support. Floating point data can be entered and displayed in floating point notation. R3010 registers can be dumped in either single or double precision.

Terminal Emulation Mode. For targets having two serial ports, there is a terminal emulation mode that supports connecting to a remote host through the second port.

Display Cache Tags and Data. Allows display of the contents of either cache, the valid bit, and the cache tag value. Includes a check for cache/main memory inconsistencies.

Diagnostics. All the diagnostics have been rewritten and are now supplied in source form.

Memory Sizes. IDT/sim determines the sizes of main memory and both caches at start-up. New entry points have been added to allow user programs to access this information.

Configuration Control. IDT/sim can be configured for I and D-caches from zero to max size; for little or big endian; for R3001 cache configurations; and for FPU present or missing.

Multiple Host Support. IDT/sim can now be compiled by IDT/c (version 3.5) on a 386 system running MS-DOS or XENIX; on a SUN SparcStation; on a MIPS workstation; or on IDT's MacStation.

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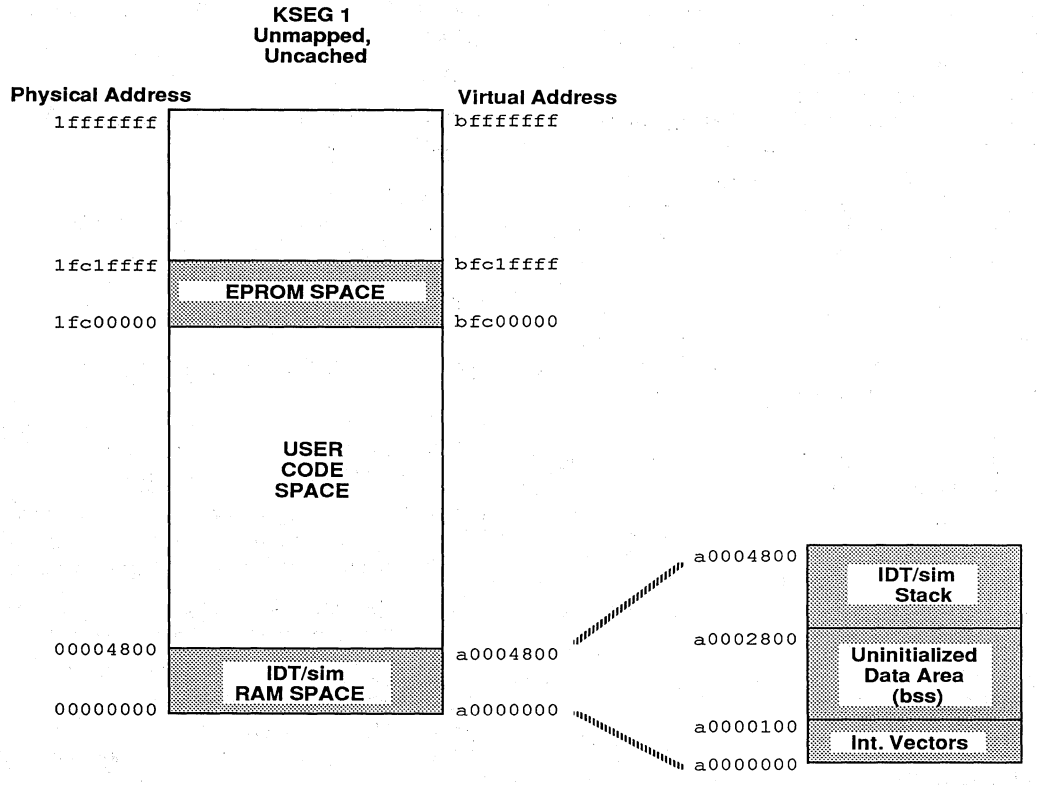

IDT/sim Memory Map

The figure above shows the memory utilized by IDT/sim. The EPROM space starts at virtual address bfc00000, which is the R3000's start-up address. The compiled version of IDT/sim with all features included occupies about 96 KB of EPROM space, and is normally placed in 128 KB of EPROM. IDT/sim uses main memory to store interrupt vectors, variables, and a stack. Eighteen KB of RAM space is reserved for this data.

IDT/SIM COMMANDS

asm <addr> This command allows the user to examine and change memory interactively using standard assembler mnemonics.

brk|b [addresslist] This command will display all of the currently set breakpoints if no address list is supplied. If an address list is supplied, breakpoints are set at each of the addresses in the list.

cacheflush/cf [-i|-d] This command will flush both the i-cache and the d-cache if no option is specified. If the user wants to just flush one or the other, the optional argument may be entered.

call|ca <address> [arg1 arg2 ... arg8] This command invokes a subprocedure under the monitor environment. It will do a jump and link to *address* passing any arguments, up to 8, while still in monitor mode.

checksum|cs [start_addr num_bytes] Display the checksums for each of the 'eproms'.

compare|cp [-w|-b|-h] <RANGE> <destination> Compare the block of memory specified by *RANGE* to the block of memory that starts at *destination*.

cont|c This command continues execution of the client process from where it last halted execution.

dbgint|di [<-e|-d DEV>] Debug interrupt enable/disable - allows 'break key' to gen extr. int.

debug|db [DEV] Enter remote debug mode.

dis <RANGE> Disassemble the contents of memory specified by range. If *RANGE* consists only of a beginning address, enough locations following the beginning address are disassembled to fill one page.

disptag|dt [-i] RANGE This command displays the instruction or data cache contents and the tag values if the cache location is valid.

dr [reg#|name\reg_group] This command will print out the current contents of register(s).

dump|d [-w|-h] <RANGE> Dump the memory specified by *RANGE* to the display .

fill|f [-w|-h|-b|-l|-r] <RANGE> [value_list] Fills memory specified by range with *value_list*..

fr [-s|-d] <reg#|name> <value> Put <value> into the register specified by <reg#|name>.

go|g [-n] <address> This command will begin execution at address <address>.

gotill|gt <address> This command will continue execution from the current value of the test program register. The program will stop execution just prior to the execution of the instruction pointed to by *address*.

help|? [commandlist] This command will print out a list of the commands available in the monitor. If a command list is supplied, only the syntax for the commands in the list is displayed.

history|h This command will display the last 16 commands entered with identifying numbers so the user may re-execute the command by entering !#. This is a circular list such that at any one time the latest 16 commands are available.

init|i Initialize prom monitor (warm reset)

load|l [options] DEV This command will input from the device specified by *_DEV* records of the format specified by options.

move|m [-w|-b|-h] <RANGE> <destination> Move the block of memory specified by *RANGE* to the address specified by *destination*.

next|n [count] This command is like the 'step' command except that when a **jal** or **bal** instruction is encountered, all of the instructions of the subprocedure are executed until the subprocedure returns to the instruction following the jump or branch and link.

rad [-o|-d|-h] Set the default radix to the requested base.

rc [-i] [-w|-b|-h] <RANGE> Addresses are automatically set to Kseq0 and the caches are isolated. Read cache memory specified by *RANGE*.

regsel|rs [-c|-h] Select either the compiler names or the hardware names for registers.

search|sr [-w|-b|-h] <RANGE> <value> [mask] This command will search the area of memory specified by *RANGE* for the value specified by *value*.

seg [-0|-1|-2|-u] Set the default segment to the requested k-segment.

setbaud|sb DEV This command allows the user to select the baud rate for the device specified by *DEV* . *DEV* may be either *tty0 or tty1*.

step|s [count] This command will execute a single step or if <count> is supplied then 'count' number of single steps will be executed.

sub [-w|-h|-b|-l|-r] <address> This command allows the user to examine and change memory interactively.

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te [DEV] This command puts IDT/sim in a transparent mode and connects the console port straight through to an outer serial port.

tlbdump|td [RANGE] This command dumps the contents of the translation buffer. If a range is specified, just the range is dumped, otherwise the entire buffer is dumped.

tlbflush|tf [RANGE] This command flushes the contents of the translation buffer. If a range is specified, just the range is flushed, otherwise the entire buffer is flushed.

tlbmap|tm [-i index] [-ndgv] <vaddress> <paddress> This command establishes a virtual to physical mapping in the translation buffer.

tlbpid|tl [pid] This command, without arguments, displays the current process identifier in the system co-processor register 'tlbhi'. If an argument is supplied then the current process identifier in 'tlbhi' is set to < pid >.

tlbptov|tp <physaddr> This command searches the translation buffer looking for translations which map to <physaddr>. Any translations found, valid or invalid, are displayed. The default segment is not applied to <physaddr>.

unbrk|ub <bpnumlist> This command will unset all of the breakpoints listed in <bpnumlist>. These are the ordinal numbers of the breakpoints and can be obtained by doing a 'brk' command.

wc [-i] [-w|-b|-h] <RANGE> [value_list] Addresses are automatically set to Kseq0 and the selected cache is isolated. This command will fill the selected cache memory specified by *RANGE* with the pattern specified by *value_list*.

LIST OF RUN TIME SUPPORT ENTRY POINTS

reset
restart
reinit
open
read
write
ioctl
close
getchar
putchar
showcar
gets
puts
printf
_exit
flush_cache
clear_cache
setjmp
longjmp
exc_utlb_code
atob
strcmp
strlen
strcpy
strcat
cli
get_range
tokenize
get_mem_conf
set_mem-conf
install_command
install_new_dev
install_immediate_int
Install_normal_int

ORDERING INFORMATION

To order EPROMs to upgrade an IDT board level product, see the order codes below. To order IDT/sim in source code, order the Developmental Use License AND order the software on the appropriate source media. The license will be shipped to you for signature; on return the software will be shipped. You may also order binary distribution rights for the run-time version of the monitor. Ask your IDT sales office for information.

Licenses

Developmental Use License **7RS901SLV**
Permits purchase of up to six copies of source code (any media combination) and use of source code to develop run-time binaries on up to six machines at a time, but does not permit inclusion of the run time code in an end product.

Binary Distribution Rights **7RS901BLP-L**
Extension to Developmental Use License to permit inclusion of binary code into end product. Development Use License must be referenced on order or ordered simultaneously. This license permits up to 100 copies to be distributed royalty-free. Additional copies are subject to the royalty below, or a one-time buyout.

Binary Distribution Sublicense **7RS901BLC-L**
Per Copy Royalty or one-time buyout for distribution of run-times developed using the System Integration Manager beyond the first 100.

Maintenance Agreement **7RS901SSY**
One year free updates. We supply a direct telephone contact for support.

Source Media

IDT/sim source code can be compiled with either the MIPS C compiler or with IDT/c version 3.5 or later. Earlier versions of IDT/c cannot compile this code. IDT/sim cannot be compiled on the 286 versions of IDT/c due to insufficient memory. The products listed below are media only and must be purchased with license 7RS901SLV above.

Source for 386, MS-DOS **7RS901SBF-L**
Compile with IDT/c C-Compiler. Shipped with both 1.2 MB 5.25" and 1.44 MB 3.5" diskettes.

Source for 386 PC, SCO Xenix **7RS901SXX-L**
Use with IDT/c C-Compiler.

Source for IDT MacStation, on Mac Disc **7RS901SMD-L**
Use with MIPS C Compiler supplied with MacStation or with IDT/c.

Source for MIPS machine, QIC-24 TAR Tape **7RS901SUU-L**
Use with MIPS C Compiler or with IDT/c.

Source for SUN SparcStation, QIC-24 TAR Tape **7RS901SWU-L**
Use with IDT/c.

EPROM Versions

The following versions of IDT/sim are supplied in EPROMs for the indicated hardware. These versions are for updating the hardware to the latest version of the monitor.

For Any 7RS30x Prototyping System **7RS901BAP**
For the MacStation 1 (7RS501) **7RS901BBP**
or the MacStation 2 (7RS502) **7RS901BCP**
For 7RS382 Evaluation Board **7RS901BDP**
For 7RS383 Evaluation board **7RS901BEP**
For 7RS388 Real8™ Laser Printer Controller **7RS901BFP**

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Integrated Device Technology, Inc.

New! Version 3.5

IDT/c Multi-Host C-Compiler System

IDT7RS903

FEATURES:

- **Includes C-compiler, Optimizing Scheduler, Assembler, Linker, Librarian, and ANSI Libraries**
- **Optional Floating Point Emulation Software**
- **Meets Plum Hall 2.00 ANSI C validation suite**
- **Runs on 80286 and 80386 machines under MS-DOS™ or XENIX™, on MIPS machines and MacStation under RISC/os, and on Sun SparcStation**
- **Supports entire IDT family of MIPS ISA Processors: R3000, R3001, R3051, and R3052**
- **Supports Big- and Little-Endian Compilations**
- **Provides control over multiple memory segments**
- **Produces disassembled link listings to simplify debug**

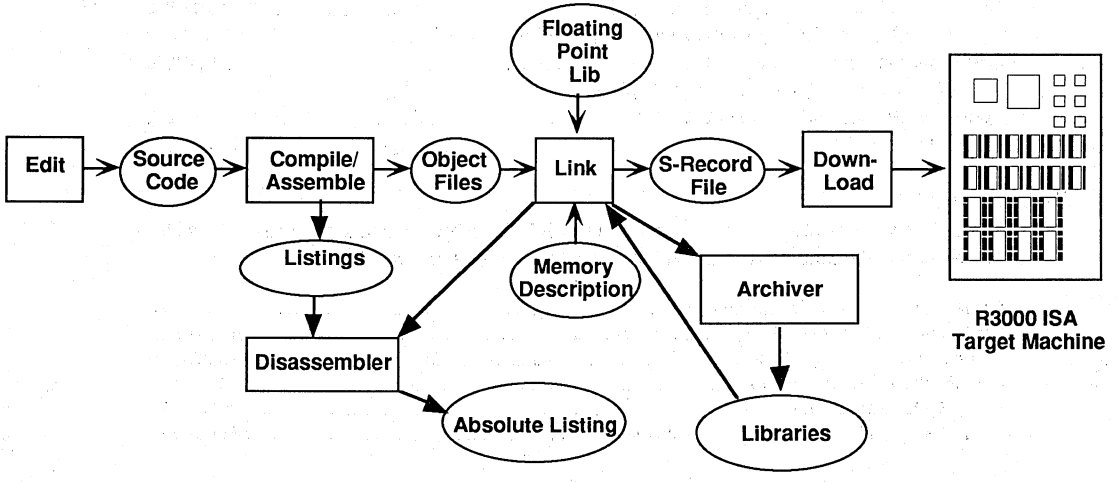
OPTIMIZING C-COMPILER SYSTEM:

IDT/c consists of a set of software products that run on a variety of platforms, and which together produce highly efficient code for R3000 CPUs and derivatives. The compiled code can be downloaded in several formats to a target machine for execution. On the target machine, the code can be controlled with IDT's System Integration Manager (IDT/sim). The compiler is based on the popular GNU C compiler, and is fully compliant with ANSI C.

New features in release 3.5 of IDT/c include a library archiving program, ANSI C libraries, and a utility for moving initialized variables into EPROM space.

The IDT/c package is available for execution on 286 or 386 machines under MS-DOS or XENIX, as well as the MIPS and SUN workstations, and IDT's MacStation single user workstation.

For any platform, IDT/c can be ordered with or without a software floating point library. A switch in the compiler determines if floating point instructions will result in R3010 instructions in the object code or whether calls to the floating point library will be made instead.



IDT/c System Flow

DESCRIPTION

The IDT/c C-Compiler System is a complete development package for CPUs based on the R3000 architecture. It contains an optimizing cross compiler, optimizing scheduler, assembler, linker, and a downloader. The 'C' compiler is compliant with ANSI 'C' standard and performs the optimizations available in state-o-the-art 'C' compilers. The assembler supports the R3000 machine instructions and architecture described in the book by Gerry Kane, "MIPS RISC Architecture", including both native and synthetic instructions. The complete IDT/c package runs on a variety of host machines and operating systems and is part of IDT's cross development system tools which include other packages such as debug monitors and libraries.

Compiler

The C pre-processor is GNU cpp and the compiler itself is based on GNU C. All C-preprocessing features are supported. The combination of the compiler and assembler included in IDT/c has been tested for compliance to the ANSI 'C' standard using the Plum Hall test suite and is compliant. Some compiler syntax and directives are different than those in the MIPS C-compiler, but it is possible to write C programs which may be compiled using either compiler.

The C compiler performs extensive optimization in multiple passes through the code. Each of the many optimization techniques can be individually switched on or off with compiler directives.

Optimizing Scheduler and Assembler

The IDT cross assembler input is compatible with source code written for the MIPS assembler. It implements the R3000 native instruction set as well as the augmented synthetic instructions defined in the "MIPS RISC ARCHITECTURE" book by Gerry Kane. There are some extensions in the IDT cross assembler that provide the programmer with more control over code generation, such as 'laiu' - load address upper and 'oria' - load address lower, enabling direct programming in pure assembly language. The assembler produces .o files which are later linked together with other files to produce an executable file.

The scheduler first expands the synthetic instructions into the native instruction set. It then rearranges code to allow for and take advantage of R3000 pipeline architecture. At the same time the scheduler analyzes loads of static constants and makes use of previously loaded constants that are close in value.

Memory description file

The memory description file is used to instruct the linker where to place object modules in the R3000 memory map. It tells the linker what address classes are legal, what addresses exist within those classes, and what addresses should be written to output files. The file consists of a sequence of class specifications (CODE, DATA, etc.) and associated address ranges.

Linker

The linker combines separately assembled program files into one object module. Command line switches may be used to override the memory description file.

The format of object code produced by the assembler in IDT/c is *not* compatible with the format produced by the MIPS assembler, so modules compiled by the MIPS software cannot be linked directly with modules compiled by IDT/c. Recompilation under IDT/c is required. Files produced by IDT/c can be run and debugged under the IDT/sim monitor.

There are three types of output file formats supported: S-Records, hex, and binary image. The S-Record files are useful in down-loading to target boards. The hex format file is useful for EPROM programming because the code can be divided into multiple files under this format.

The linker output can be disassembled back into a listing file and map that includes all object modules at their correct final locations in memory.

Endianess

IDT/c includes a switch so that code may be compiled in either Big-endian or Little-endian format.

Floating Point Library

IDT/c may be ordered with a floating point library. A switch in the compiler is set at compile time to determine how the compiler should handle floating point instructions. In the normal mode, it will produce R3010 Floating Point Accelerator instructions in the object code. If the switch is set the other way, the compiler will insert calls to the floating point library instead, and the floating point library must be available at link time. Because the compiler knows about the library during compile time, it can perform optimizations not otherwise possible and keep the execution penalty for using software instead of hardware to about a factor of 4 in very floating point intensive code.

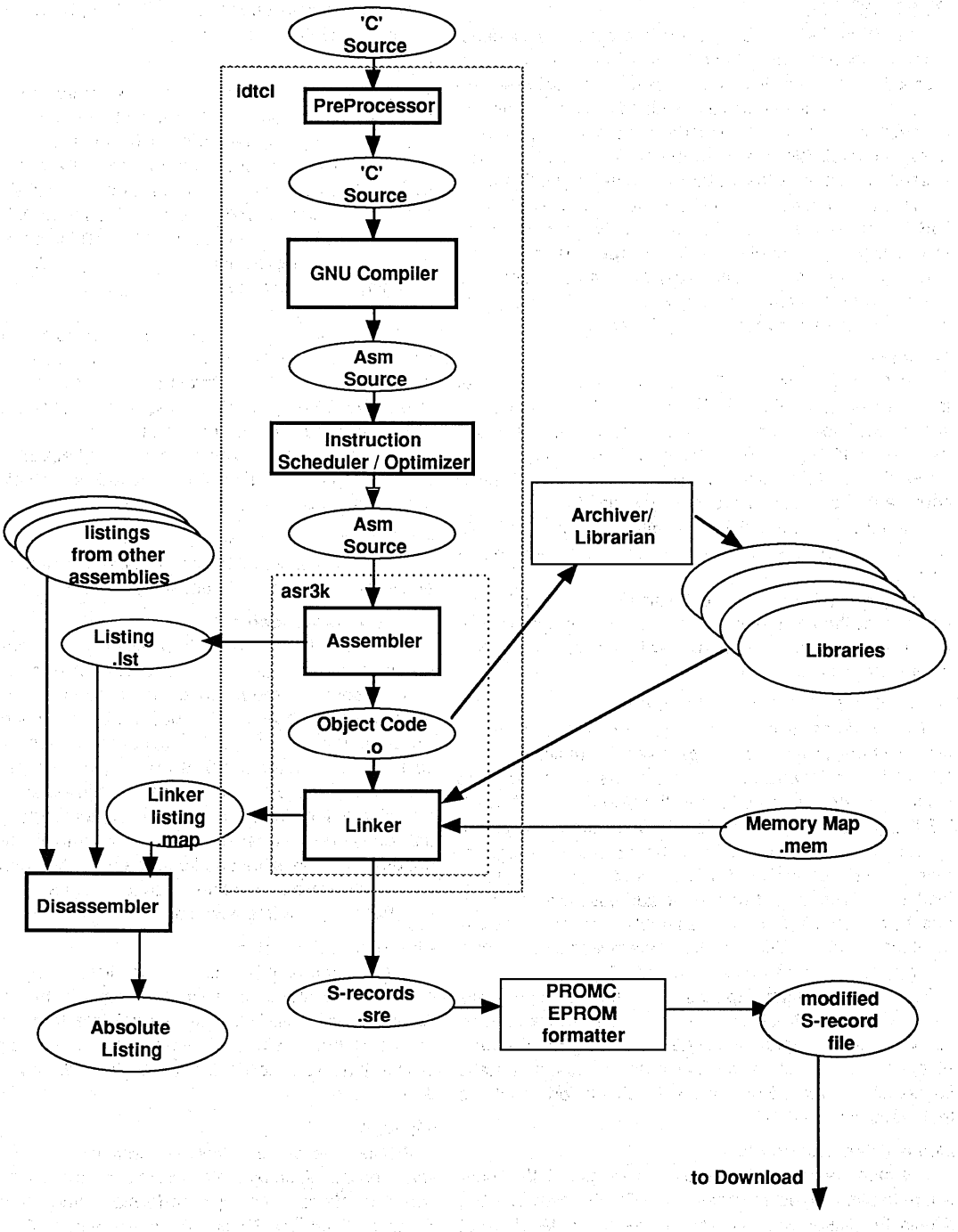
Librarian and Archiver

IDT/c supports object code library files. Many compiled routines may stored in a single library file by using the Archiver utility. At link time, the linker extracts only the routines actually used. This technique reduces the number of files that must be dealt with explicitly during program development.

PROM-C

PROM-C is a utility included with IDT/c that permits variables initialized by the program to be moved from their normal locations in the object code into designated memory space destined for EPROM. The user program can execute a simple routine at start-up to move the variables from EPROM back into RAM space at the appropriate locations.

C


'C' Source
idtcl
PreProcessor
'C' Source
GNU Compiler
Asm Source
Instruction Scheduler / Optimizer
Asm Source
asr3k
Assembler
Object Code .o
Linker
listings from other assemblies
Listing .lst
Linker listing .map
Disassembler
Absolute Listing
Archiver/ Librarian
Libraries
Memory Map .mem
S-records .sre
PROMC EPROM formatter
modified S-record file
to Download

IDT/c Flow

OPTIMIZATION PASSES

Multiple optimization passes are performed by the GCC compiler. Below is a brief description of what takes place on each pass. Note that switches can be used in the compiler to turn individual optimization choices off or on, providing the programmer with a great deal of control over how the compiler modifies the code.

Jump optimization

Simplifies jumps to the following instruction, jumps across jumps, and jumps to jumps. Deleties unreferenced labels and unreachable code.

Register Scan and common subexpression elimination

Finds first and last use of each register for purposes of subexpression elimination while performing constant propagation.

Loop optimization and strength reduction

Moves constant expression code outside of dynamic loop.

Data flow analysis

Divides the program into basic blocks and identifies the life of values in registers. Code producing unused results and unreachable loops are eliminated.

Local register allocation

Allocates registers to be used inside each basic block.

Global register allocation

Assigns registers for values which live across basic block boundaries.

Final Pass

The final pass is to generate assembler code. At this point, peephole optimizations are performed as well as generation and optimization of the function entry and exit code sequences.

PERFORMANCE COMPARISONS

Execution

To obtain a measure of the efficiency of the IDT/c compiler, a set of benchmark programs was compiled under both IDT/c and the MIPS compiler, and the size and execution time of the resulting binaries were compared.

Execution Time Comparison

	Code Size	Exec. Time
Compiled with MIPS C	1.0	1.0
Compiled with IDT/c	1.20	1.19

Compile Time

The time required to compile a program under IDT/c depends on the machine speed, type, and configuration. For comparative purposes, the Stanford benchmark was compiled under a variety of hosts and the results are shown below. For reference, the same program was also compiled using the MIPS compiler.

Compile Time Comparisons

Host	Compile Time
MIPS C on MIPS Machine	24 sec.
IDT/c on MIPS Machine	25 sec.
IDT/c on 10 MHz 286, MS-DOS	695 sec.
IDT/c on 25 MHz 386, Xenix	70 sec.

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COMMAND LINE SWITCHES

-E : Pre-process only. .S file is expected. Pre-processed file is written to the standard output.

-O : Optimize (GNU cc -O option).

-O1: Optimize even more (GNU cc options: -fstrength-reduce -fforce-addr -fforce-mem -fcombine-regs -finline-functions).

-c : Assemble only, do not link. Expected are filenames with .s or .S suffixes. Output files (in absence of -o) will have .o suffix.

-ZA: Produce assembly listing.

-o xxx: Name output file. The default output name is 'out.sre'.

-ZL: Produce link map.

-Fxxx.xxx: Use xxx.xxx as memory layout description file. In absence of -F option the default is to use file idt.mem in default library directory.

-ZThhhhhhhh: Specify text loading address; hhhhhhhh is address in hex, up to 8 hex digits. This will override .mem file definitions.

-ZDhhhhhhhh: Specify data loading address; hhhhhhhh is address in hex, up to 8 hex digits. This will override .mem file definitions.

-e name: Use global 'name' as program start address.

-noenv: Do not include default library modules which define the order of program sections and global symbols that point to beginning and end of text, data and bss.

-nostdlib: Do not include library for linking with IDT/sim monitor.

ASSEMBLER DIRECTIVES

.align n Align so that n least significant bits of address are 0.

.ascii "string" Assemble string.

.bss Store following into bss section.

.byte arg,...,arg Assemble arguments into consecutive bytes.

.data Store following into data section.

.end name Included for MIPS asm compatibility but ignored.

.ent name Included for MIPS asm compatibility but ignored.

.extern name Import symbol 'name' that refers to n bytes of storage . (included for MIPS asm compatibility and ignored).

.globl name Export defined symbol.

.half arg Assemble arguments into consecutive halfwords.

.set argument Argument can be :

at - error flag every use of $1.

noat - disable errors due to user's usage of $1 (at).

reorder - enable scheduling to resolve pipeline conflicts.

noreorder - disable scheduling.

.space n Skip next n bytes, advancing location counter by n.

.text Store following into text section.

.word arg Assemble arguments into consecutive words.

SEGMENT The SEGMENT directive selects the address segment where the following code or data will be stored. It is used to implement '.text', '.data' and '.bss' which are MIPS compatible segments. Using this directive the user can create other custom segments.

FLOATING POINT EMULATION

The floating point emulation library provides routines to perform the functions listed below.

Single and Double Precision Add
Single and Double Precision Subtract
Single and Double Precision Multiply
Single and Double Precision Divide
Single and Double Precision Compare
Single and Double Precision Float to Integer Conversion
Integer to Single and Double Precision Float Conversion
Single to Double Precision Conversion
Double to Single Precision Conversion
ASCII to Single and Double Precision Binary
Single and Double Precision Binary to ASCII

ORDERING INFORMATION

The IDT/c C-Compiler is an efficient R3000 C-compiler system based on the popular GNU C and hosted on a variety of computers. The IDT/c system includes the compiler, assembler, scheduler and linker. All PC versions of the software are shipped with both 1.2 MB floppy discs and 1.44MB 3.5" diskettes. A "boxtop" single user license is included with the product. Contact your IDT sales office for multiple user licensing.

Media, without Floating Point

The software listed below does not include the floating point library.

For 286 machine, MS-DOS 7RS903BAF-N
Not recommended for large, complex programs. At least 2MB RAM recommended. Requires DOS version 3.3 or greater.

For 386 machine, MS-DOS 7RS903BBF-N
This product uses extended memory space on the 386. 4 MB recommended.

For 286 machine, SCO Xenix 7RS903BYX-N

For 386 machine, SCO Xenix 7RS903BXX-N

For MIPS machine RISC/os, on QIC-24 TAR Tape 7RS903BUU-N

For MacStation, on Macintosh Disc 7RS903BMD-N
Runs on MacStation R3000 board under IDT/ux.

For SUN Sparcstation, on QIC-24 TAR tape 7RS903BWU-N

Media, with Floating Point Library

The software listed below includes the floating point library.

For 286 machine, MS-DOS 7RS903FBAF-N
Not recommended for large, complex programs. At least 2MB RAM recommended. Requires DOS version 3.3 or greater.

For 386 machine, MS-DOS 7RS903FBBF-N
This product uses extended memory space on the 386. 4 MB recommended.

For 286 machine, SCO Xenix 7RS903FBYX-N

For 386 machine, SCO Xenix 7RS903FBXX-N

For MIPS machine RISC/os, on QIC-24 TAR Tape 7RS903FBUU-N

For MacStation, on Macintosh Disc 7RS903FBMD-N
Runs on MacStation R3000 board under IDT/ux.

For SUN Sparcstation, on QIC-24 TAR tape 7RS903FBWU-N

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Floating Point Upgrade

The version of the compiler without floating point may be upgraded to the version with the floating point library. To upgrade, contact your IDT sales office and give them the order code and serial number of your original software.

Maintenance

Maintenance 7RS903BSY
Includes free upgrades for one year and direct telephone contact for support

Integrated Device Technology, Inc.

IDT/fp FLOATING POINT LIBRARY For use with MIPS C-Compiler

IDT7RS905

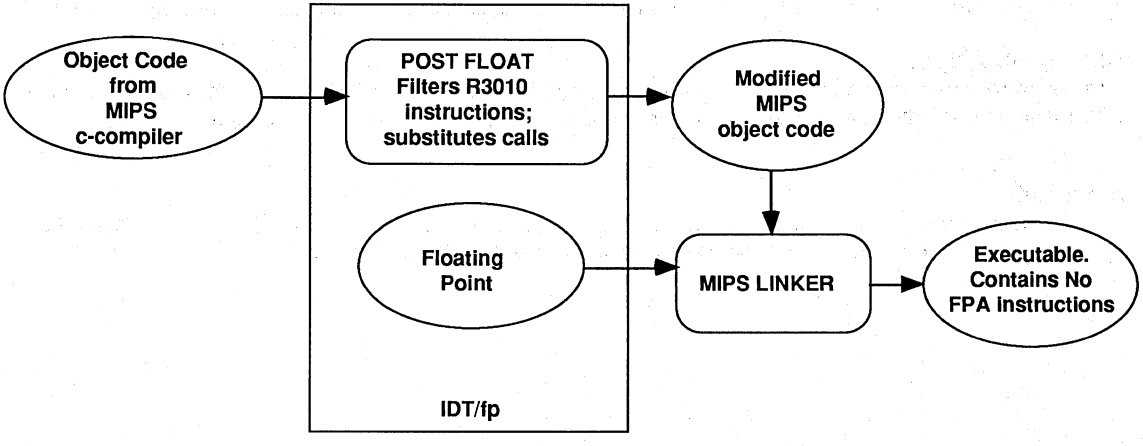
FEATURES:

- **Allows use of floating point operations without requiring a floating point chip in system**
- **Requires no changes to C source code**
- **Floating point code can be linked to application or OS; does not require UNIX™**
- **License includes binary distribution rights**
- **Conforms to IEEE 754 format**

DESCRIPTION:

The IDT7RS905 product is an IEEE-754 compliant floating point arithmetic library for use with the MIPS C-compiler. It is used as a substitute for instructions normally requiring the presence of a floating point accelerator (FPA), and eliminates the need for that device. The software consists of a pre-processor called Post Float, and a library which contains software to duplicate the FPA's floating point instruction set using only integer arithmetic. The Post Float pre-processor reads object code from the MIPS C-compiler, and substitutes calls to the library for each FPA instruction encountered. The library is then linked with the modified object code to produce an executable file that does not require an FPA.

The library includes the basic single and double precision arithmetic functions (add, subtract, multiply and divide) as well as conversion routines between different precisions, integer and ascii formats. The IEEE-754 single precision floating point format represents numbers ranging from ±1.2E-38 to ±3.4E+38 with 24-bit mantissa precision. The double precision format offers a range of ±2.2D-308 to ±1.8D308 with a 53 bit mantissa. The accuracy of the floating point library is within one least significant bit. The IEEE floating point format defines special representations for underflow (result = zero), overflow (result = + INF or - INF), and invalid operation (result = **N**ot **a** **N**umber, NaN). The floating point library adheres to the IEEE-754 error handling procedure in all applicable cases.



SUPPORTED OPERATIONS

Addition	FPADD(a,b) & DPADD(a,b)	FP to Integer	FPINT(sp) & DPINT(dp)
Subtraction	FPSUB(a,b) & DPSUB(a,b)	DP to SP	DPTOSP(dp)
Multiplication	FPMUL(a,b) & DPMUL(a,b)	SP to DP	SPTODP(sp)
Division	FPDIV(a,b) & DPDIV(a,b)	ACSII to FP	FASCBIN() & DASCBIN()
Comparision	FPCMP(a,b) & DPCMP(a,b)	FP to ASCII	FBINASC() & DBINASC()
Integer to FP	FPFLT(int) & DPFLT(int)		

ORDERING INFORMATION:

The IDT/fp package consists of the Post Float filter for the MIPS C-compiler and the floating point library. The product is shipped with a single-user license which permits unlimited distribution of binary applications which have been linked with the floating point library.

For use with MIPS C-compiler 7RS905BUU-N
Maintenance 7RS905BSY
One year free updates

C

The following section contains important new data sheets and application notes that were not included the 1991 RISC Data Book.

Integrated Device Technology, Inc.

SRAM TIMING PARAMETERS FOR 40 MHz R3000A CACHE DESIGN

APPLICATION NOTE AN-85

by Satyanarayana Simha

The IDT79R3000A is a RISC microprocessor which is used in a variety of applications ranging from low-end embedded controllers to high-end workstations. Currently, the R3000A operates at a frequency of up to 40 MHz. This technical note specifies the timing parameters for SRAMs to function as cache for a 40 MHz R300.

Figure 1 shows a block level diagram of the R3000A with its four clock inputs coming from a delay line. Table 1 shows a summary of the delay line settings to be used for a 40 MHz R3000A. **Please note carefully that Clk2xSys is taken as the zero time reference and comes from the first tap of the delay line.** The other 2x clocks lag Clk2xSys in time and follow it with respect to delay line taps.

The design of the cache subsystem for the R3000A is straightforward. Industry standard static RAMs function as cache. The timing equations derived take into account the effect of capacitive loading on the bus. The derating factors are calculated based on certain assumptions. The deratings due to the capacitive loading on the address, data and control signals are assumed to be 2 ns each. Figure 2 shows a typical R3000A based system. The cache comprises of fast 16 K X 4 static RAMs i.e., the IDT7198. The AdrLo bus of the R3000A goes through a latch : the FCT373C.

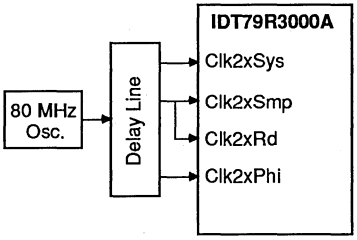


Figure 1. Four-phase clock input to the R3000A

Parameter	40 MHz
Clk2xSys	0
Clk2xSmp	4
Clk2xRd	4
Clk2xPhi	8

Table 1. Delay line settings for a 40 MHz R3000A

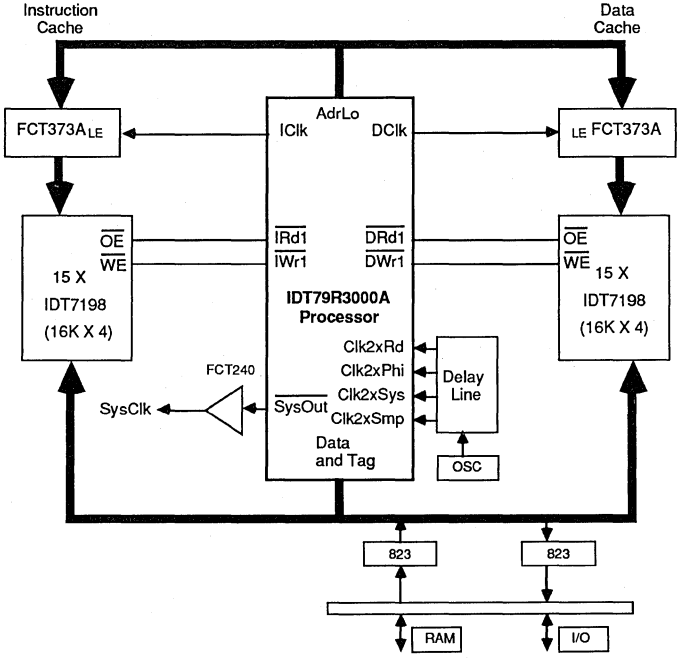


Figure 2. Block level diagram of a cache subsystem with the R3000A using IDT7198 16K X 4 to function as cache. (The R3010 is not shown in this Figure)

The cache format of the R3000A is comprised of 60 bits: 32 bits of data, 4 bits of data parity, 20 bits of tag, a valid bit, and three bits of parity to cover the tag and the valid bit. With this requirement, it is clear that for the instruction cache, 15 IDT7198s (16K X 4 SRAMs) are needed. The same number is also required for the data cache. This means that there are a total of 30 SRAM devices for the cache.

Timing equations for cache design

This section deals with the timing equations that enable us to determine the critical timing requirements of the static RAM that will be used as cache. These equations are based on the use of static RAMs (without built-in latches) as cache RAMs. The superscript 'd' in the following equations denote the deratings to be taken into account. The static RAM chosen for illustration here is a 16K X 4 IDT7198. The board is assumed to be surface mount for the 40 MHz R3000A. All calculations are based on the 40 MHz R3000A specifications.

Figure 3 show the timing diagrams of the R3000A when performing a data store followed by an instruction fetch. This is the worst case example and is chosen to determine the SRAM parameter requirements. The encircled numbers represent the equations presented in section 4.4. The timing diagram in conjunction with the equations are used to determine the timing requirements.

The following equations are used to determine the timing parameters for the static RAM so that they can function as cache for a 40 MHz R3000A. The numbers at the left correspond to the encircled numbers in the timing diagrams. Equations 9 and 10 are not shown in the timing diagram but are included for completeness. The equations also use some R3000A parameters. These are listed in Table 2. The SRAM specifications are given in Table 3.

25ns Cycle Timing

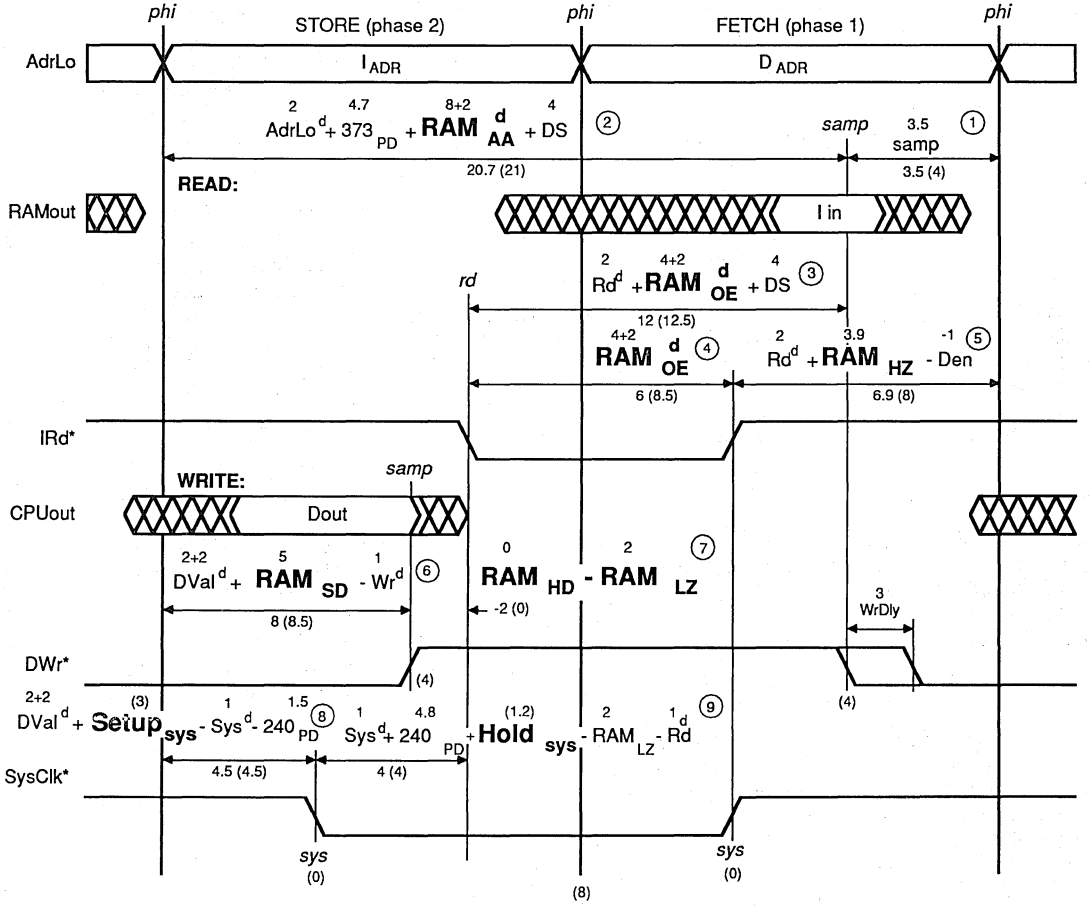


Figure 3. Cache timing diagram for a 40 MHz R3000A

Internal Sample to Phase Delay

This is the time that the processor needs to sample the incoming data. Typically, for the R3000A,

tsmp ≥ 3

RAM Address Access Time

This equation is used to determine the Address Access time parameter requirements of the static RAM. From the timing diagram of Figure 4.9, it is easily calculated. As an example, let us calculate the address access time for a 33 MHz R3000A. The total cycle time for a 33 MHz R3000A is 30 ns. If the processor's sample time requirement is met the time remaining in the cycle is 24 ns in which the data has to be presented to the processor. The processor requires a data setup time of 4 ns. There is also a propagation delay through the latch for the address bus. For the 33 MHz part, a fast FCT373C is used because it has a maximum propagation delay of 4.2 ns. The derating factors due to the capacitance and the trace length have also to be taken into account. Using all these factors, the equation is

$tRAMAA \le tcyc - tsmp - tDS - t373PD - tAdrLo^d - tRAMAA^d$

40 MHz R3000A: $tRAMAA \le 25 - 4 - 4 - 4.2 - 2 - 2$

$tRAMAA \le 8.8$

Cache Enable to Sample

This equation is used to determine the system output enable(tOES) requirements of the cache RAM. This should meet the processor's setup specification. The output enable time (tOE) specifications for the RAM is tested for a voltage change of 200 mV (a fall from 1.732 V to 1.532 V for IDT RAMs). For a system, however, the voltage falls from approximately 3.3 V to 1.5 V. This fall time is usually a nanosecond. **Therefore, the RAM specifications should take this system factor into consideration and specify the output enable time at least one nanosecond lower than the calculated timings.**

$tOES \le tcyc/2 - tRD^d - tDS - tsys\text{-}smp + tsys\text{-}rd - tOES^d$

40 MHz R3000A: $tOES \le 12.5 - 2 - 4 - 4 + 4 - 2$

$tOES \le 4.5$

Minimum Read Pulse Width

This timing requirement guarantees that the read pulse-width generated by the processor is at least as long as the cache RAM output-enable time.

$tOES \le tcyc/2 - tsys\text{-}rd - tOES^d$

40 MHz R3000A: $tOES \le 12.5 - 4 - 2$

$tOES \le 6.5$

Read-Write I-Cache Data Bus Contention

This timing requirement ensures that the RAM output is tristated soon enough after the instruction read signal goes high. In the worst case, when the processor performs a store operation, no data contention occurs.

$tRAMHZ \le tsys - tRd^d + DEn$

40 MHz R3000A: $tRAMHZ \le 8 - 2 + (-1)$

$tRAMHZ \le 5$

Processor Data-SetUp to End of Write

This enables the designer to determine whether the cache RAMs have adequate data setup time when the processor does a store operation. In the equation, the minimum derating is used on the write line i.e., tWr^d as the worst case assumption.

$tRAMDS \le tcyc/2 - tsys\text{-}smp - tDVal - tDVal^d - tWr^d$

40 MHz R3000A: $tRAMDS \le 12.5 - 4 - 2 - 2 - (-1)$

$tRAMDS \le 5.5$

Data Hold from End of Write

This parameter requirement guarantees that the data hold from end of write of the cache RAM is met when the processor or the read buffer is writing to the RAMs.

$tRAMHD \le tsmp\text{-}rd + tRAMLZ$

40 MHz R3000A: $tRAMHD \le 0 + 2$

$tRAMHD \le 2$

Data SetUp to SysClk

This timing parameter ensures that the setup time into an external register (for the main memory interface) is sufficient enough for the case when the processor is doing a store. The data is clocked in the register on the rising edge of the buffered SysOut* (through an inverting FCT240A). In this equation, $tsys(min)^d$ is used to insure worst case calculations.

$tsetupSys \le tcyc/2 - tsys - tDVal - tDVal^d + tsys^d + t240PDmin$

40 MHz R3000A: $tSetUpSys \le 12.5 - 8 - 2 - 2 + 1 + 1.5$

$tSetUpSys \le 3$

Data Hold from SysClk

This timing parameter is to guarantee that the hold time specification for an external register is met on a processor store. In this equation the minimum value of tRD^d is taken to insure worst case numbers.

$tHoldSys \le tsys\text{-}rd - tsys^d - t240PDmax + tRAMLZ + tRd^d$

40 MHz R3000A: $tHoldSys \le 4 - 1 - 4.8 + 2 + 1$

$tHoldSys \le 1.2$

Address SetUp to End of Write

This equation enables us to determine the timing requirement for the RAM so that the address set up time is sufficient before the trailing edge of the write pulse.

$tRAMAW \le tcyc - tsmp\text{-}sys - tAdrLo^d - t373PD + tWr^d$

16 MHz R3000A: $tRAMAW \le 25 - 4 - 2 - 4.2 + 1$

$tRAMAW \le 15.8$

Write Hold Pulse Width

This requirement guarantees that the cache RAMs minimum write pulse width specification is met.

$tRAMPW \le tcyc/2 - tWrDly$

16 MHz R3000A: $tRAMPW \le 12.5 - 2$

$tRAMPW \le 10.5$

Symbol	Parameter	40 MHz		Unit
		Min	Max	
	Clock			
TCkHigh	Input Clock High	5		ns
TCkLow	Input Clock Low	5		ns
TCkP	Input Clock Period	12.5	500	ns
	Clk2xSys to Clk2xSmp	0	tcyc/4	ns
	Clk2xSys to Clk2xRd	0	tcyc/4	ns
	Clk2xSys to Clk2xPhi	3	tcyc/4	ns
	Run Operation			ns
TDen	Data Enable	-	-1.0	ns
TDDis	Data Disable	-	-0.5	ns
TDVal	Data Valid	-	1.5	ns
TWrDly	Write Delay	-	1.5	ns
TDS	Data Set-Up	4	-	ns
TDH	Data Hold	-2	-	ns
TCBS	CpBusy Set-Up	6	-	ns
TCBH	CpBusy Hold	-1.5	-	ns
TAcTy	Access Type[1:0]	-	3	ns
TAT2	Access Type[2]	-	7.5	ns
TMWr	Memory Write	-	9	ns
TExe	Exception	-	3	ns
	Stall Operation			ns
TSAVal	Address Valid	-	12.5	ns
TSAcTy	Access Type Valid	-	9	ns
TMRdI	Memory Read Initiate	-	9	ns
TMRdT	Memory Read Terminate	-	5	ns
TSd	Run Terminate	1.5	7	ns
TRun	Run Initiate	-	2.5	ns
TSMWr	Memory Write	-	9	ns
TSEx	Exception Valid	-	7.5	ns
	Reset Initialization			
TRST	Reset Pulse Width	6	-	TckP
TrstPLL	Reset Timing, PLL on	3000	-	TckP
Trstcp	Reset Timing, PLL off	128	-	TckP
	Capacitive Load Derating			
CLD	Load Derate	0.5	1	ns/25pF

Table 2. R3000A AC Specifications.*PLL: Phase Locked Loops

READ CYCLE TIMING SPECIFICATIONS

Parameter	40 MHz	
	Min	Max
tRC	8	—
tAA	—	8
tACS	—	—
tCLZ	2	—
tOES	—	4
tOLZ	2	—
tCHZ	—	4
tOHZ	—	3.9
tOH	—	—
tPU	0	—
tPD	—	15

WRITE CYCLE TIMING SPECIFICATIONS

Parameter	40 MHz	
	Min	Max
tWC	10	—
tCW1	10	—
tAW	10	—
tAS	0	—
tWP	10	—
tWR1	0	—
tWR2	0	—
tWHZ	—	4
tDW	5	—
tDH	0	—
tOW	5	—

Table 3. Static RAM Read and Write Timings to work as cache with the R3000A.

(1) This assumes that an FCT373C with a T_{PD} = 4.2 ns is used.

Legend:

tRAMAA - RAM Access Time
tRAMOE - RAM Output Enable Time
tRAMHZ - RAM OutPut Low impedance to Output in High impedance
tRAMLZ - RAM Output in High impedance to output in Low impedance
tRAMHD - RAM Data Hold Time
tDS - R3000A Data Setup Time
tsys - Phase Difference between Clk2xSys and Clk2xPhi
trd - Phase Difference between Clk2xPhi and Clk2xRd
tsmp - Phase Difference between Clk2xPhi and Clk2xSmp
tcyc - Cycle time of the R3000A
tsmp-rd = tsmp - trd
t240PD - Propagation delay from Clk to Output of FCT240A

References:

1) IDT RISC R3000A Family Hardware User Manual, October 1988
2) IDT RISC R3000A Family Data Sheets, 1988
3) IDT RISC Data Book, 1991
4) IDT Data Book Supplement, 1989

Integrated Device Technology, Inc.

IDT79R3051™ SYSTEM DESIGN EXAMPLE

APPLICATION NOTE AN-86

by Andrew Ng

INTRODUCTION

This application note describes a memory evaluation board that is an example of many of the design considerations for systems based on an IDT79R3051™ RISController™ family CPU.

The memory board, illustrated in Figure 1, consists of:

- An R3051 CPU
- Reset circuitry
- An address de-multiplexer
- A data transceiver
- Wait-state and memory control logic
- 128K bytes of SRAM
- 128K bytes of EPROM
- A dual channel UART
- A real time counter
- An interrupt controller

In addition, an expansion connector supplies all the CPU signals for the addition of external modules such as DRAM memory systems or other application specific I/O systems. The memory and I/O system on the example board are compatible with the IDT7RS382 R3000 Evaluation Board. Thus 7RS382 software such as the IDT/sim PROM Debug Monitor can run on the example board. The board is typical of an embedded controller core such as for LAN adapters, laser printers, facsimiles, and avionics applications. The differences would appear in which peripherals are used and memory type, size, and speed requirements.

The board was designed as a generic example of the construction of a system using the IDT79R3051 RISController with both low parts count and cost sensitive requirements. However, since many generalities were taken into consideration, many systems can reduce both parts count and cost even further. Although the board is not populated with parts that have the highest performance achievable, its design can be easily modified to do so. In addition, PAL™ support for further experiments with optimizations and trade-offs can be done to accommodate different kinds and speeds of memory and I/O. While the board is designed with SRAM for the simplicity of a design example, the extension to a DRAM system with CAS before RAS refresh is only slightly more complex.

THE R3051 RISCONTROLLER CPU

The IDT79R3051 family is a series of high-performance 32-bit microprocessor RISControllers designed to bring the high-performance inherent in the MIPS™ RISC architecture into low cost, simplified, and power sensitive applications.

The instruction set is compatible with the 79R3000A and 79R3001 RISC CPUs. Features of the R3051 family include:

- 4kB (R3051) to 8kB (R3052) of Instruction Cache on-chip
- 2kB of Data Cache on-chip
- Clocked from a single, double-frequency clock input
- On-chip 4 deep read and write buffer
- On-chip DMA arbiter
- Flexible burst/simple block bus interface
- Multiplexed address and data bus for low cost packaging, simplicity of use
- Base versions use fixed address translation to simplify software
- Extended architecture versions use 64-entry, fully associative Translation Lookaside Buffer (TLB) to support page mapping and virtual memory

The R3051 RISController combines a similarly featured R3000A CPU system consisting of over 50 LSI/MSI parts into a single integrated chip.

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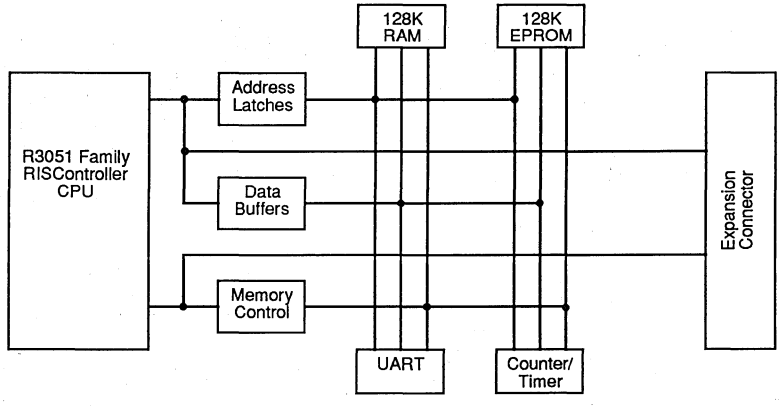

Figure 1. System Block Diagram

DETAILED DESIGN REVIEW

The following sections give a detailed review of how each functional block relates specifically to designing with the R3051 RISController. Particular attention is focused on alternative design strategies that could reduce parts count and improve performance as well as on a description of the original design. The subsystem block designs include:

- Analog reset logic
- A PAL-based memory controller (3x PALs)
- Address de-multiplexer (4x IDT74FCT373T)
- Data transceiver (4x IDT74FCT623T)
- 128kB of SRAM (4x IDT71256 32kx8 45ns SRAM)
- 128kB of EPROM (4x 27256 32kx8 125ns EPROM)
- 68681 DUART
- 8254 Timer
- Interrupt controller (1x PAL)
- Off-card connector

Reset, Reset Vector, and Clock Buffer Circuitry

The $\overline{\text{Reset}}$ signal is based on a linear integrated circuit, a TI TL7705A supply voltage supervisor with a Power-On Reset Generator. A 1 µF capacitor is used to program the reset generator for a 13 ms Reset period.

Note that because the R3051 synchronizes the $\overline{\text{Reset}}$ input signal internally, an RC circuit can be used instead. An example is to pull $\overline{\text{Reset}}$ high with a resistor of about 10K Ohms, tie $\overline{\text{Reset}}$ to a 22 µF capacitor which is tied to ground, and tie $\overline{\text{Reset}}$ to a push button switch that is tied to ground. The example board can be reprogrammed and populated to experiment with $\overline{\text{Reset}}$.

Certain configuration options (the reset vector) are selected in the R3051 by using the interrupt pins at the rising edge of $\overline{\text{Reset}}$. On the example board, the interrupt pins are simply pulled up (or down) since $\overline{\text{SInt}}$(2:0) are not used in this system (software can permanently mask these interrupt inputs in the Status Register). However, if they are used (via the expansion connector) they would need to be multiplexed with the reset function. There are a number of techniques to perform this multiplexing: for example, if the interrupting agent is not capable of tri-stating its interrupt during $\overline{\text{Reset}}$, an external multiplexer such as an IDT74FCT257T can be used, with the enable always tied active and the select tied to $\overline{\text{Reset}}$. If the interrupting agent tri-states its interrupt during Reset, then using simple pull-ups or pull-downs will still operate properly.

The clocks on the board are buffered by an IDT74FCT240C(T) inverting tri-state buffer. This buffer was selected partially to provide a board testability path for injecting a test clock, as well as to buffer the signals to increase their drive. The primary reason for the buffer, however, is to invert $\overline{\text{SysClk}}$ to form SysClk, the signal that is used to clock the state machines on this board. Buffer output pins closest to the ground pin (pins with the lowest pin inductance) were used first to help lessen potential noise and ground bounce problems. The Clk2xIn oscillator is socketed, so that the board may be populated with different speed parts.

In this design, the FCT240C(T) enables are pulled down to be active all of the time. Since $\overline{\text{SysClk}}$ does not tri-state when $\overline{\text{Tri-State}}$ ($\overline{\text{SInt}}$(1)) is active during the reset vector, it is helpful to an ATE programmer to be able to tri-state the inverter.

Memory Controller

The example board's Memory Controller consists of three 22V10 PALs. The first PAL is used for address decoding, the second for wait state and cycle counting, and the third for byte enables. The PALs are functionally described in the following paragraphs. The PAL equations are included in the appendices. The PALs are all placed in sockets, and thus can easily be reprogrammed for various experiments.

Address Decoder

The Address Decoder PAL, MEMDEC.JED, uses Address(31:17) to generate chip selects. The chip selects are decoded according to the 7RS382 address map as described in the 7RS382 Hardware User's Guide. Three spare I/O pins are provided, which could be used to decode additional chip selects. These spare outputs are in place of the 'USER CS1X*' chip selects provided for on the 7RS382 board, but not explicitly supplied by this example board.

The address decoder does not wait for ALE to begin generating the chip-select outputs. It does this so that maximum performance may be achieved, since the Chip Select outputs will be generated earlier in the transfer. However, as a result, the CS outputs may tend to "glitch" as a valid address is driven. Thus, the Read Enable and Write Enable seen in the memory system must be synchronized so that they are valid only within the time that the CPU is attempting a read or write transfer. This combination allows maximum performance: address and chip enables are seen early in the transfer, but the Read and Write signals are generated synchronously to insure proper system operation.

One of the extra I/O pins can be used as a test enable input to tri-state the outputs for board level ATE. Some systems will not need to decode as many address bits or may have a fixed map, and thus may able to use FCT138's or 16V8's to do the address decoding instead of the relatively expensive 22V10 part.

Memory Cycle Controller

The purpose of the Memory Cycle Controller is to provide a wait-state generator which stalls the R3051's Bus Interface Unit, so that various types and speeds of memory can be used. The Memory Cycle Controller is implemented with a 22V10 PAL called MEMCONT.JED. Note that this PAL was selected in order to make the PAL equations more readable. A lower cost solution may implement the state machine in two 16R8 PALs.

The Memory Cycle Controller allows various speeds of memory devices to be used, by using the throttled read supported by the R3051 bus interface. Other kinds of transactions are treated as simplified cases of the throttled read.

The basic state machine looks for the start of a read or write transaction by looking for an asserting edge of $\overline{\text{Rd}}$ or $\overline{\text{Wr}}$. When a transaction is begun, the state machine starts a 5-bit binary up counter, C(4:0). C(4:0) then increments on each SysClk rising edge. C(4:0) is used as the basic timing master for all

of the other control signals generated in the state machine.

In the memory scheme used here, rather than search for the negating edge of $\overline{Rd}$ or $\overline{Wr}$ at the end of the transaction, a $\overline{CycEnd}$ synchronous decoder is used to tell the C counter when the end of the memory cycle occurs. This type of strategy is used because the de-asserting edges of $\overline{Rd}$ and $\overline{Wr}$ occur within the setup and hold times of a buffered/inverted (FCT240C(T)) $\overline{SysClk}$. Typically, the de-asserting edge of $\overline{Rd}$, $\overline{Wr}$, and $\overline{Burst}$ should not be used to control a SysClk based state machine. Similarly, the rapid negation of ALE by the processor makes it difficult to synchronously sample ALE when using a state machine driven by a buffered clock.

$\overline{CycEnd}$ serves to synchronously reset the state machine when a de-asserting $\overline{Rd}$ or $\overline{Wr}$ edge is expected, whether or not the $\overline{Rd}$ or $\overline{Wr}$ de-asserting edge meets the setup and hold times of the state machine. Another output, $\overline{EnStart}$ is used to start the byte enables by waiting a number of cycles before asserting. The amount of time the transfer waits is used to allow drivers used in the previous transfer to tri-state, and may be necessary in systems which employ devices whose output disable time is long relative to the system clock frequency.

Other outputs from the Memory Cycle Controller PAL include the R3051 transfer termination inputs $\overline{RdCEn}$, $\overline{Ack}$, and $\overline{BusError}$. On a read transfer, $\overline{Burst}$ and one of the Chip Enable inputs from the Address Decoder are used to determine the timing and quantity of $\overline{RdCEn}$ signals to be asserted for this transfer (according to the requested transfer size and the memory device speed).

$\overline{Ack}$ is asserted at the end of a write cycle to indicate completion of the transfer, and optionally towards the end of a Quad Word (Burst) read cycle. A description of the various kinds and options of read and write cycles is thoroughly explained in the R3051 Family Hardware User's Guide. The number of cycles before and between the assertion of $\overline{Ack}$ and $\overline{RdCEn}$ is programmable, allowing flexibility for various types of memories.

Finally, the $\overline{BusError}$ output is used to end an undecoded memory cycle. In the R3051, $\overline{Rd}$ is negated one-half cycle after the $\overline{BusError}$ input is asserted.

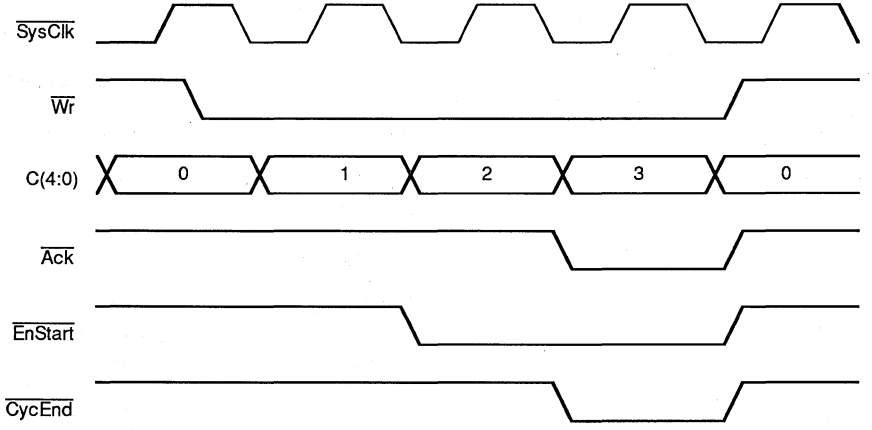

Figure 2. Timing of $\overline{CycEnd}$

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Other Approaches

Of course, alternative methods and techniques to memory interfacing with an R3051 family CPU exist. Four approaches easily implemented in discrete components include:

- using a SysClk based $\overline{CycEnd}$ counter (as used in this example)
- using asynchronously resettable registers for the counter
- using interlocking SysClk and $\overline{SysClk}$ registers
- using an unbuffered $\overline{SysClk}$

All of these methods can be used to design for the clocking scheme of the R3051 Family, which uses both the rising and falling edges to control its outputs. The use of both edges of the clock allows the R3051 to mitigate the 1 clock inter-transaction latency that is associated with most other CPUs that need the extra clock to fixup and start new memory cycles. However,because the R3051 Family asserts and de-asserts its edges the same way on both $\overline{Rd}$ and $\overline{Wr}$ cycles, specific methods can be employed so that the memory system is always clocked from one edge of $\overline{SysClk}$. An example of this is the $\overline{CycEnd}$ method used on this board, which ignores the edges that are not synchronized with the state machine. Although traditional high-performance CPUs require complex state machines to operate efficiently, the beauty of the R3051 family is the simplicity of its interface. Memory control state machines for the R3051 family are really only minor variations on traditional wait-state machines, and can also easily take advantage of the 1/2 clock inter-transaction savings provided by the CPU interface.

Each of the four approaches has advantages as well as drawbacks relative to each other. The following paragraphs will give a brief description of each technique. Each of the methods could be used by themselves or combined with one

or more of the other methods, to achieve the optimal price/performance/parts count for a given application. Systems employing dedicated interface chips (such as the IDT R372x family, or customer specific ASIC or Gate Array devices), may choose to make different trade-offs than those using discrete component based solutions.

Using SysClk and generating a Cycle End indicator

The SysClk based CycEnd approach as described above is straightforward because of its similarity to traditional wait-state machines. As mentioned above, it does not require the terminating edge of Rd or Wr to complete a transaction.

The system implemented in this design example is limited in speed by:

tclk/2 >= t240 + tpalco + t3051setup + tcap + twire

which works out to 28 MHz for a 10 nsec 16V8, over 40 MHz for a 5 nsec 16R8 PAL, and 33 MHz for a 10 nsec 22V10 PAL.

Using Asynchronous Reset to terminate the Cycle Counter

The second potential method, which uses an asynchronous reset to terminate the cycle, requires AND'ing together Rd and Wr into the the reset line of the counter C(4:0) and can be demonstrated by reprogramming the PAL on the example board. The reset-to-valid output, reset width, and the reset recovery time to clock are among the speed limiting paths in this approach when implemented in PALs. Unfortunately, the reset-to-output delay of a PAL is usually less optimized and relatively slow.

tasyncreset <= tclk/2 - trdn - tcap - twire

For example, a 20 MHz system would require a reset-to-output delay of 17ns, which can be found in a 10 nsec 22V10 PAL (with a 15 nsec reset to valid output data time).

Using interlocking PALs clocked on opposite edges

The third potential approach uses a SysClk based register to detect asserting edges and a SysClk based register to detect de-asserting edges. The outputs of each of the PALs interlock by controlling the outputs of the other PALs. This allows the flexibility of seeing all edges and being able to control outputs optimally by using any 1/2 clock edge (such as output enables). Such an approach obviously requires more PALs, and is somewhat speed limited by:

tclk/2 >= t240 + tpalco + tpalsetup + tcap + twire

which works out to 20 MHz for a 10 nsec 16V8 PAL.

In systems using chips designed specifically to interface to the R3051 family (such as the IDT R3721 DRAM controller), this approach is simpler to implement and leads to the highest levels of performance.

Using an unbuffered SysClk

The fourth potential approach uses an unbuffered SysClk based state machine. This leads to the requirement of having 0 hold time on the registers as well as a 2 nsec minimum propagation delay time to meet the R3051 timing requirements (note that using a buffered SysClk instead of the unbuffered version would require negative hold time on the registers). Despite these restrictions, some PALs can be found that meet all of these requirements. This approach leads to a one cycle latency in reacting to R3051 output assertions. An asserting Rd or Wr would be seen a clock too late to bring RdCEn or Ack low during their first possible sampling clock. Using an unbuffered SysClk has a speed advantage over the other techniques:

tclk >= tpalco + t3051setup + tcap + twire

tclk/2 >= t3051prop + tpalsetup + tcap + twire

which can support designs of 35 MHz for a 10 nsec 16V8 PAL and well over 40 MHz with a 7.5 nsec 16R8 PAL.

An additional consideration relative to using an unbuffered SysClk is the amount of loading placed on the clock, and the impact of additional loading on R3051 AC parameters. Of course, when using a single chip memory controller such as the IDT R3721 or a customer designed ASIC, these loading considerations are minimal.

In summary, the R3051 Family uses both edges of the clock to assert control signals in order to reduce inter-transaction delay between external bus cycles. However, by using one or a combination of the above techniques in a design, a traditional wait-state machine can still be used with the addition of only minor variations.

Read and Write Enables

The Read and Write Enables PAL, MEMEN.JED, uses EnStart and CycEnd to control the initiation and length of the output enable and write enable assertions. Rd and Wr are used to select between read and write cycles. Note that it would have been possible to combine individual bank selects with the address decoder PAL, rather than use a distinct PAL to control the timing of the assertion of Write and Read Byte Strobes.

On read cycles, RdEn is asserted as the system's primary output enable signal. RdDataEn is used to enable the FCT623T data transceiver bank. RdDataEn in most systems would simply be 'DataEn' as supplied straight from the processor. This system provides RdDataEn in case other transceiver banks are added to the system.

The byte enables are used to support partial word writes which are used during byte, halfword, and tri-byte operations. Write cycles combine the byte enables, BE(3:0), with Wr, EnStart, and CycEnd to form the write enable outputs WrEn(D:A) which are attached to the byte banks within the memory system. Whether or not the system is Little or Big Endian, WrEn(A) is always attached to the LSB. WrEn(D:A) can also be implemented using an FCT257T multiplexer. WrDataEn is used to control the FCT623T data transceiver bank and must be held extra long to provide memory data hold time.

Finally, the Byte Enable PAL also has a synchronized PowReset output called Reset and a "guarded" GUARTCS. The guarded chip select, GUARTCS is an example of interfacing R3051 signals to a Motorola-type I/O Device as opposed to an Intel-type I/O Device.

Motorola-type devices multiplex their read/write input pin and expect a data strobe pin to validate the data out or to latch the data in, while Intel-type devices have separate read and write strobes. Since the MC68681 DUART is a Motorola device, the data strobe must start late and end early, so that read/write is held throughout that period. Additionally, the MC68681 uses its chip select pin as a data strobe. As a data strobe, it is important not to have decoder glitches on the chip select since reads in I/O devices are often used to update

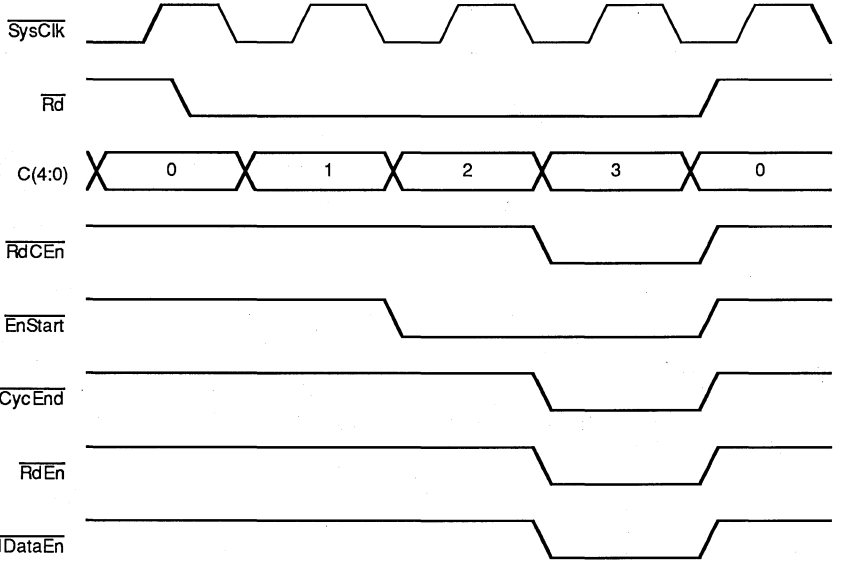

Figure 3. Timing Diagram of RdEn

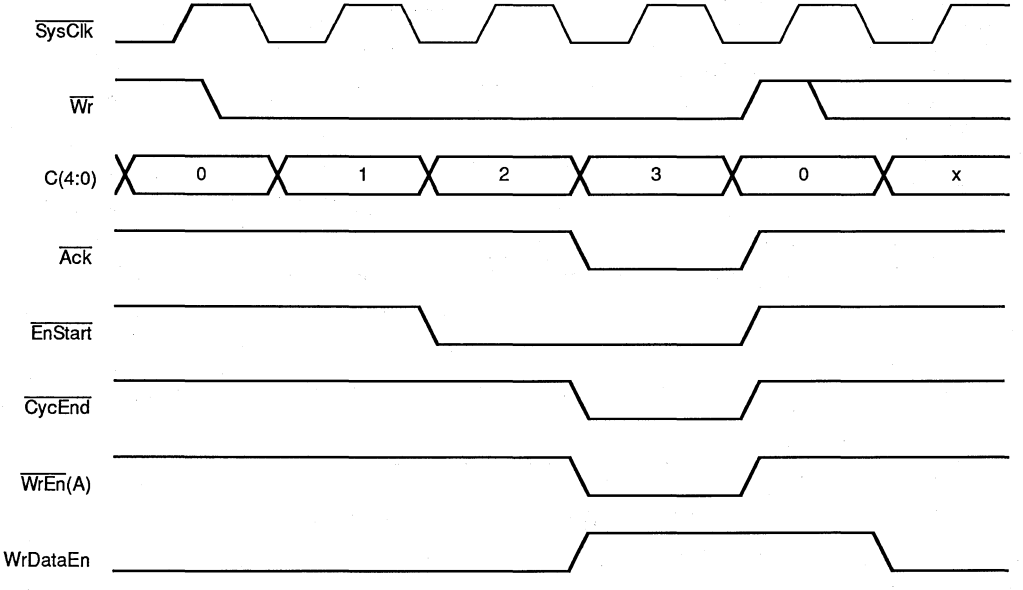

Figure 4. Timing Diagram of WrEn(A)

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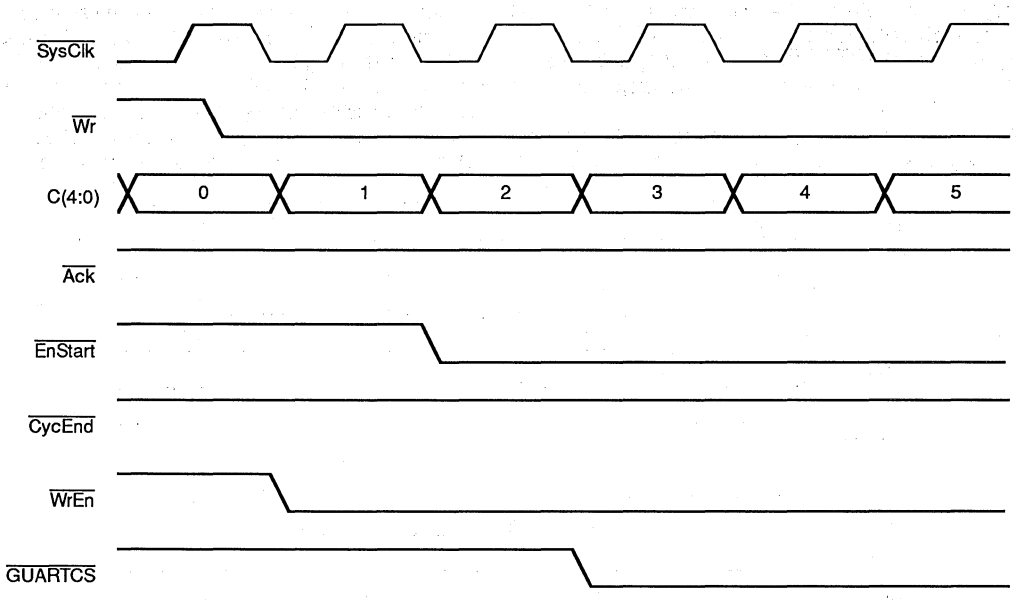

Figure 5. Timing Diagram of Start of GUARTCS

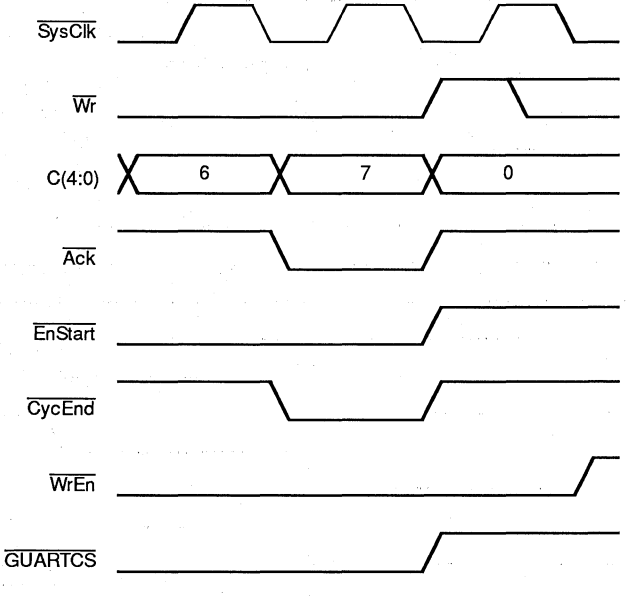

Figure 6. Timing Diagram of End of GUARTCS

FIFO pointers. Thus, the guarded GUARTCS uses EnStart and CycEnd to shorten up UARTCS. Finally, WrEn is provided to extend Wr to allow additional data hold time at the end of the write cycle. WrEn could easily be inserted with another OR term into WrEn(A).

Address Latch and Transceiver De-multiplexer

The address latch bank consists of four FCT373T 8-bit transparent latches. ALE is used for the latch enable on the FCT373T's. The transparent phase allows extra address decoding time during the time that ALE is high; the outputs of the latches are fed directly to the address decode PAL and to the memory devices. In order to insure that address hold time to the latches are met, it is important to take care with the use of the ALE signal. The number and length of the ALE traces is critical and should be kept to a minimum.

Rather than use FCT373's, DRAM systems may want to use FCT821's or FCT823's, which are wider latches. RAS/CAS address multiplexing can be performed by sequencing the output enables of the latches and having the outputs of the latches tied together and driving the DRAM address bus.

The data transceiver bank on the example board uses four FCT623T 8-bit transceivers. FCT623T's were chosen over the similar 10-bit FCT861's and 9-bit FCT863's simply to reduce pin count. The FCT861/3's provide a more conventional interface, since both output enables are active low, instead of one enable active high, and the other active low as in the FCT623T's. However, since this system uses PALs to control the transceivers, the use of FCT623's poses no additional complexity to the design.

FCT623T's were selected instead of FCT245's because of the ease of interfacing to dual output enable pins instead of a direction and enable pins as in the FCT245. Interfacing with FCT245 controls would ideally require that the direction control only be changed when the output enable is disabled. This requires extending a combined (latched) Rd and Wr based signal for an extra cycle at the end of a memory transaction, which may be the beginning of the next memory cycle. Unless the direction pin is controlled with a SysClk based state machine, a signal like EnStart would be necessary to keep the enable pin de-asserted in the subsequent cycle until the direction pin control becomes valid. Some systems with high noise tolerance, e.g., IBM-PC adapter boards, forgo the extra cycle ideal and simply bus contend for a very short time (a few ns) into its memory system by having the read strobe directly control the direction. DataEn, output from the CPU, can be used in such systems to simplify control signal generation.

When there are no pending DMA, read, or write requests, the R3051 tri-states the A/D(31:0) bus during these non-bus clock cycles to reduce power consumption. One can optionally add external pullup or pulldown resistors so that the A/D(31:0) bus is always defined for board level ATE and so that the input pins of the latches and transceivers are stabilized.

Finally, systems that can output disable (oe to Z-state) all memory readable devices within:

tdisable < tclk/2 - t3051dataenn + taddr - tcap - twire

might not require the transceiver bank and thus could reduce the parts count by 4.

EPROM and Static RAM Memory

The memory on the example board is populated with 125 nsec Erasable PROMs (EPROMs) and 45 nsec Static RAMs (SRAMs). Four 27C256 32Kx8 EPROMs are used to form 128K bytes of ROM. The EPROMs are placed in sockets and thus can easily be removed for reprogramming or replacement; alternative designs may wish to add circuitry to allow in-board programming of the EPROMs (e.g. Flash Erase EPROMs).

The EPROMs have a relatively long output disable time (oe to z-state), typical of ROMs and thus require data buffers to prevent contention on the multiplexed AD(31:0) bus, since the following equation is not met:

tclk/2 >= tdisablecontrol + tdisable - taddr + tcap + twire

In addition, the disable time for these EPROMs is long enough that, except for relatively slow systems (under 20 MHz), extra clocks need to be added to the next bus cycle to prevent bus contention with other memory banks. This is determined by:

tclk >= tdisablecontrol + tdisable - tdata + tcap + twire

The SRAM bank is formed using four IDT71256 32Kx8 SRAMs for a total of 128K bytes. The RAM chips have common data I/O pins, separate read and write strobes, and chip selects. RAMs without a separate read strobe (output enable pin) may require more complex address decoding when used in a multiple bank configuration.

DUART, Timer, and Interrupt Controller

An MC68681 DUART and an MAX235 RS232 transceiver are used to form two RS232 serial communication links. The DUART control registers are word addressed, but only D(7:0) are used. The MC68681 is an example of a Motorola-type I/O interface as explained above.

An iP8254 timer/counter chip is used for a real-time clock or timer. The iP8254 is an example of an Intel-type I/O interface. The iP8254's need for separate read and write strobes matches up well with the R3051.

Software control of these chips is best described by their respective data sheets. Typically, most software programs for the 7RS382 have used the DUART in a polling mode and the timer in a square wave mode. Interrupts Int(5:3) are controlled by UARTIntOC, Timer OutB, and Timer OutA respectively from MSB to LSB. The 16R8 PAL, called MEMINT.JED, is used to control these interrupts latches in the assertion transition of the original interrupt lines.

The controller holds the interrupt line to the processor for Timer A and Timer B until they are acknowledged (as required by the R3051). Acknowledgement is indicated by reading the interrupt controller at Virtual Address BF800010 and BF800014 (Physical Address 1F800010 and 1F800014) respectively. This action incidentally reads extraneous data from the Timer chip itself on D(7:0). The DUART interrupt must be acknowledged by using the DUART control registers.

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The output disable to data in z-state time for these I/O peripherals is relatively long, as is typical for I/O devices. This forms the critical timing path for the placement of $\overline{\text{EnStart}}$ in the Memory Controller and Memory Enable PALs.

Expansion Connector

Two 50-pin connectors are provided which bring out the R3051 RISController pins to allow off-board expansion. The $\overline{\text{BusReq}}$ and $\overline{\text{BusGnt}}$ pins are not presently used on this board. If DMA is to be used, the R3051 control outputs $\overline{\text{Rd}}$, $\overline{\text{Wr}}$, $\overline{\text{Burst}}$, $\overline{\text{DataEn}}$, and ALE are pulled high or low so that they remain inactive when tri-stated.

SCHEMATICS AND PAL EQUATIONS

Appendices include the System Design Example Board Schematics and the PAL equations.

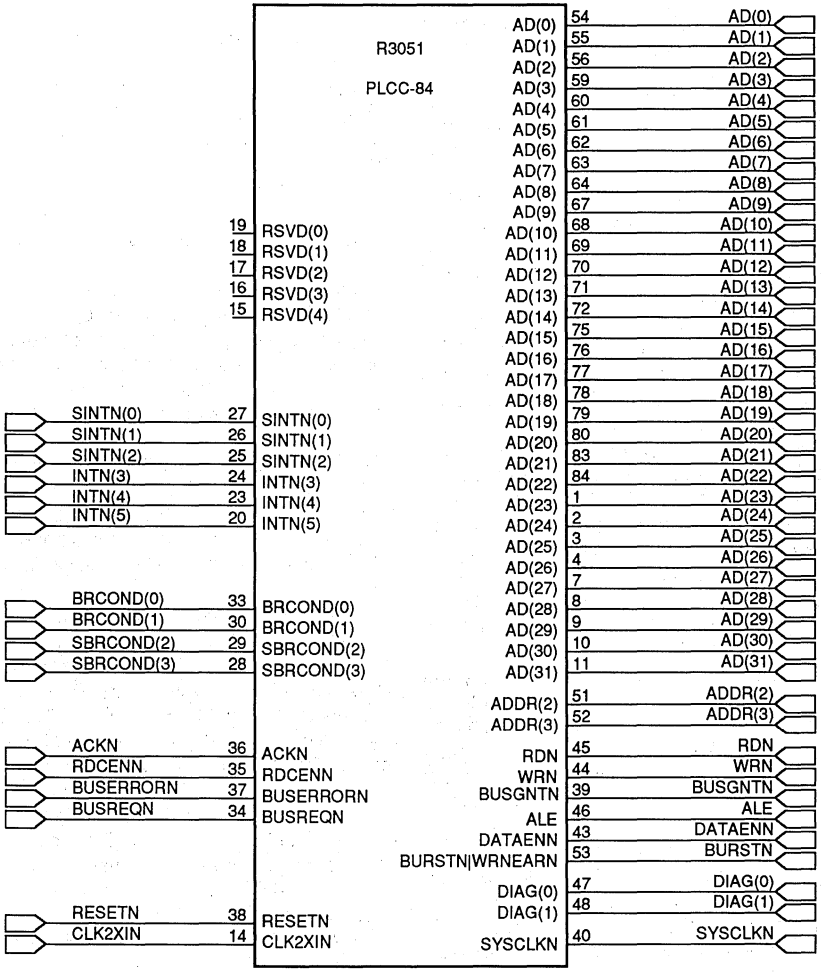


Figure 7. R3051 RISController

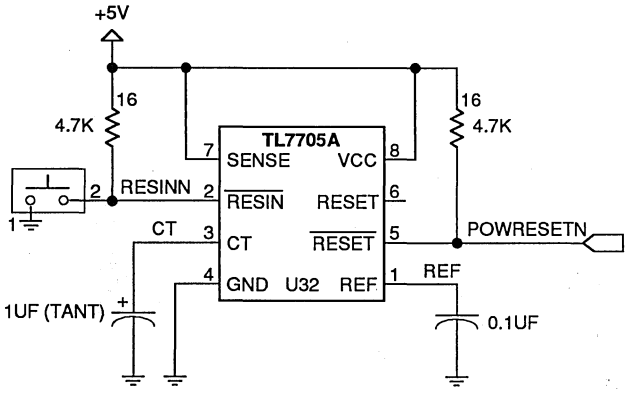


Figure 8. Reset Logic

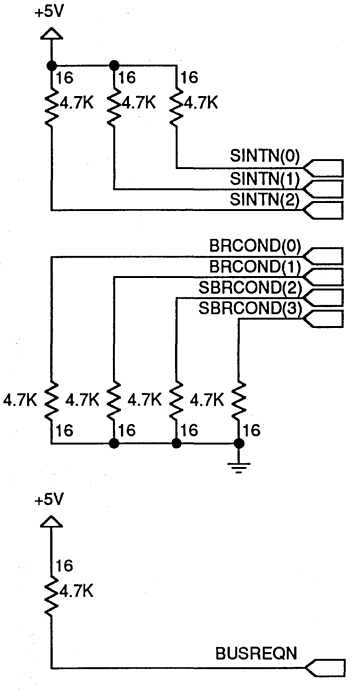


Figure 9. Unused Inputs

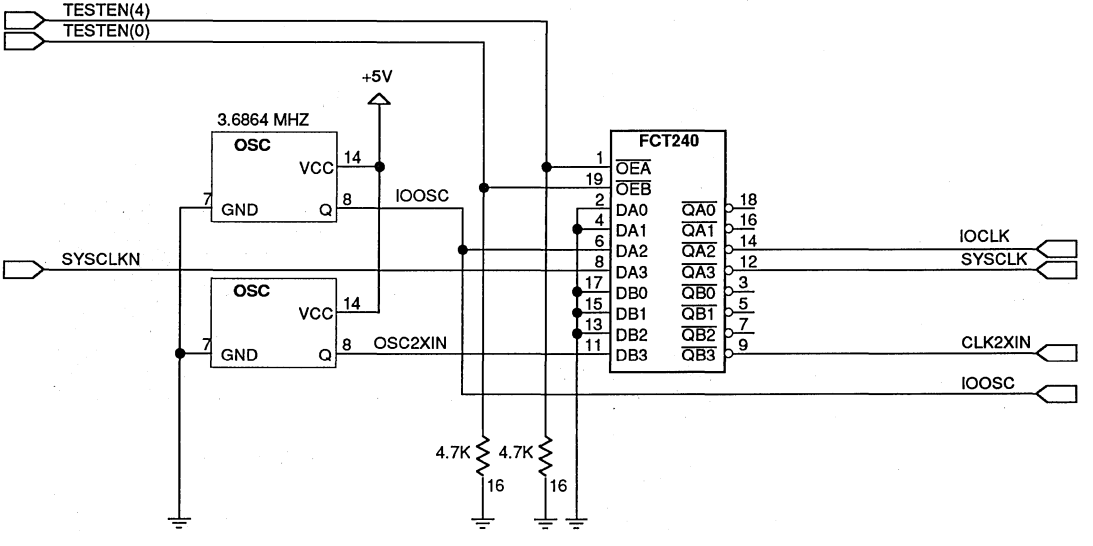


Figure 10. Clock Logic

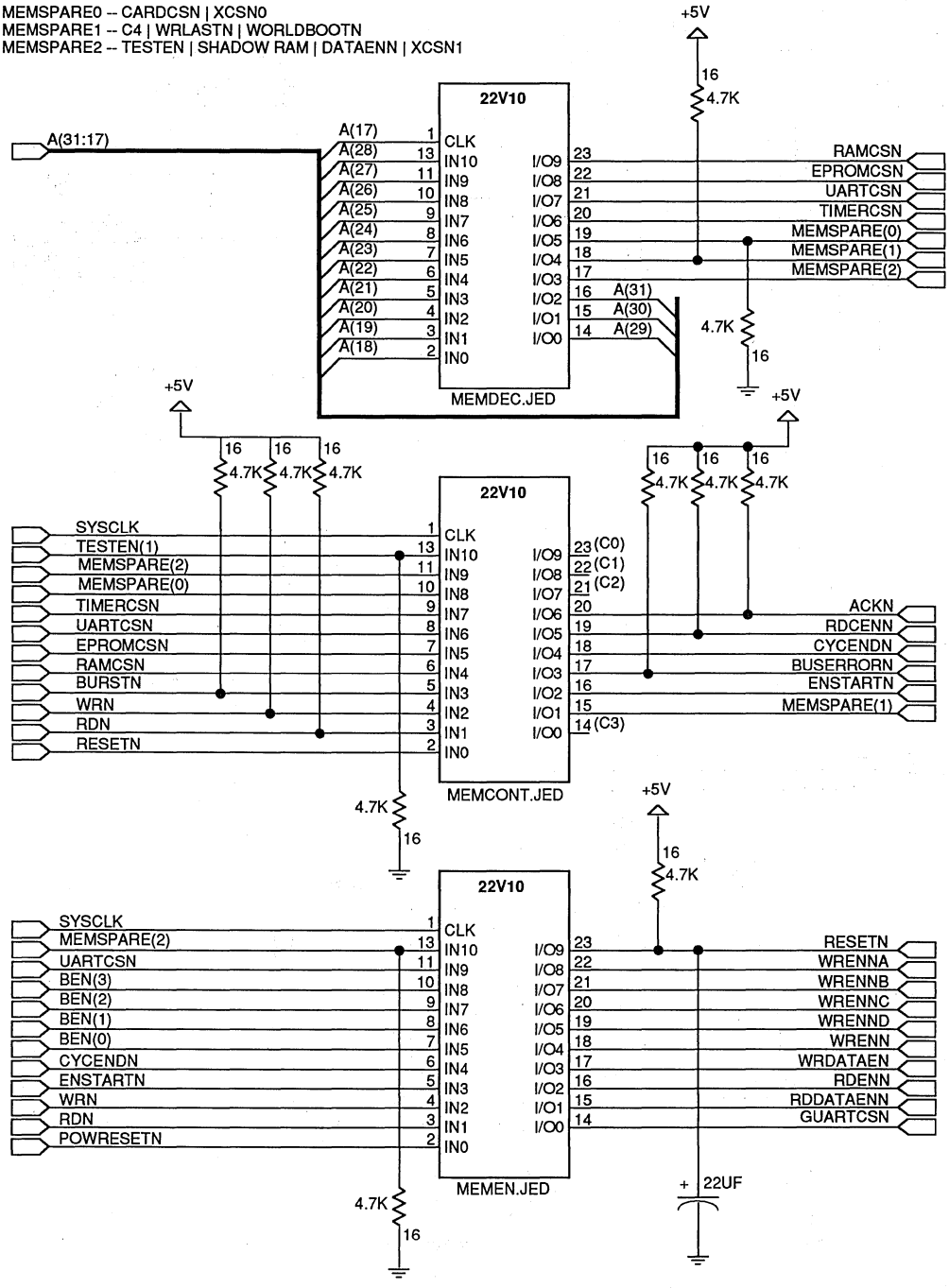


Figure 11. Memory Controller

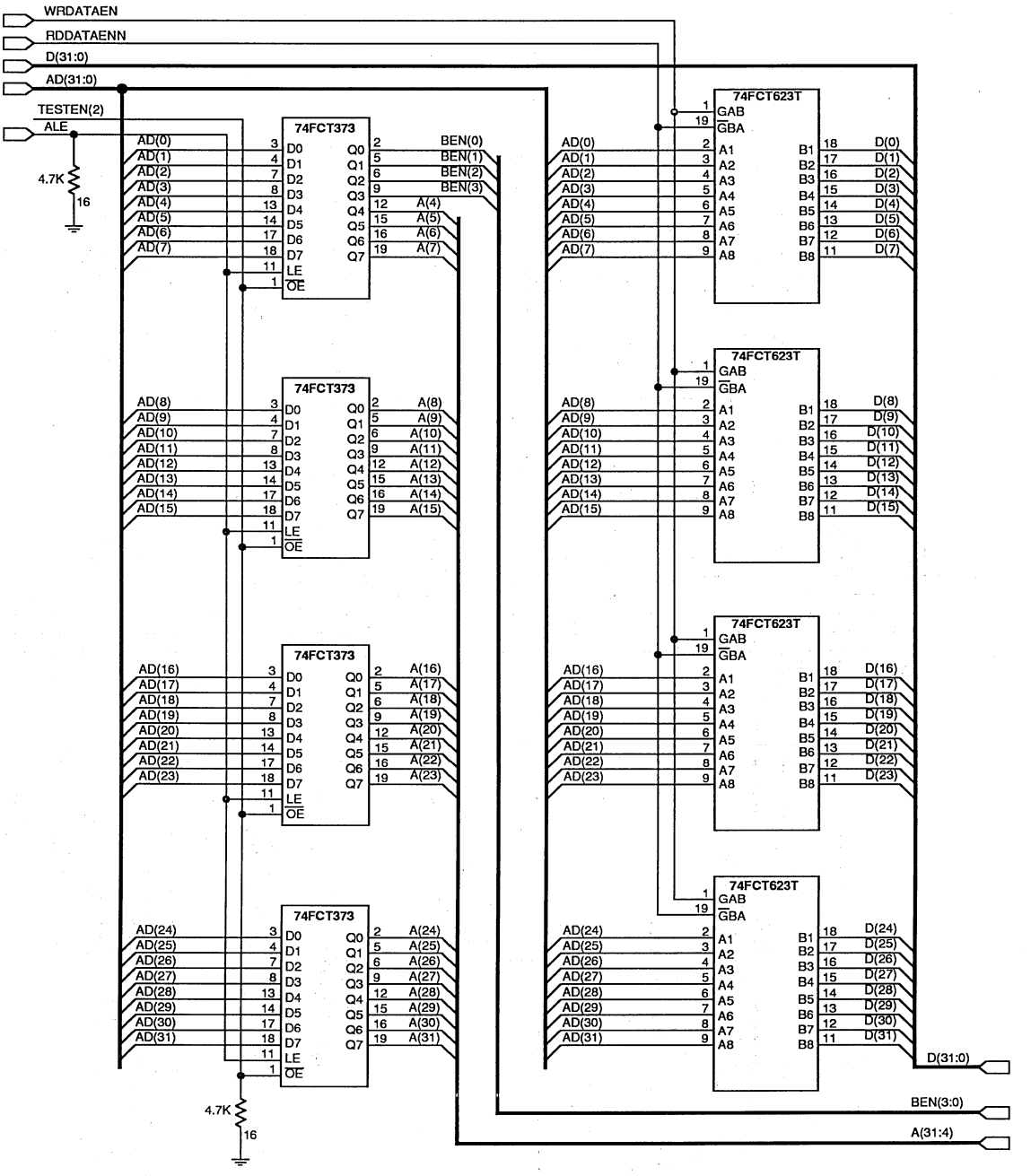
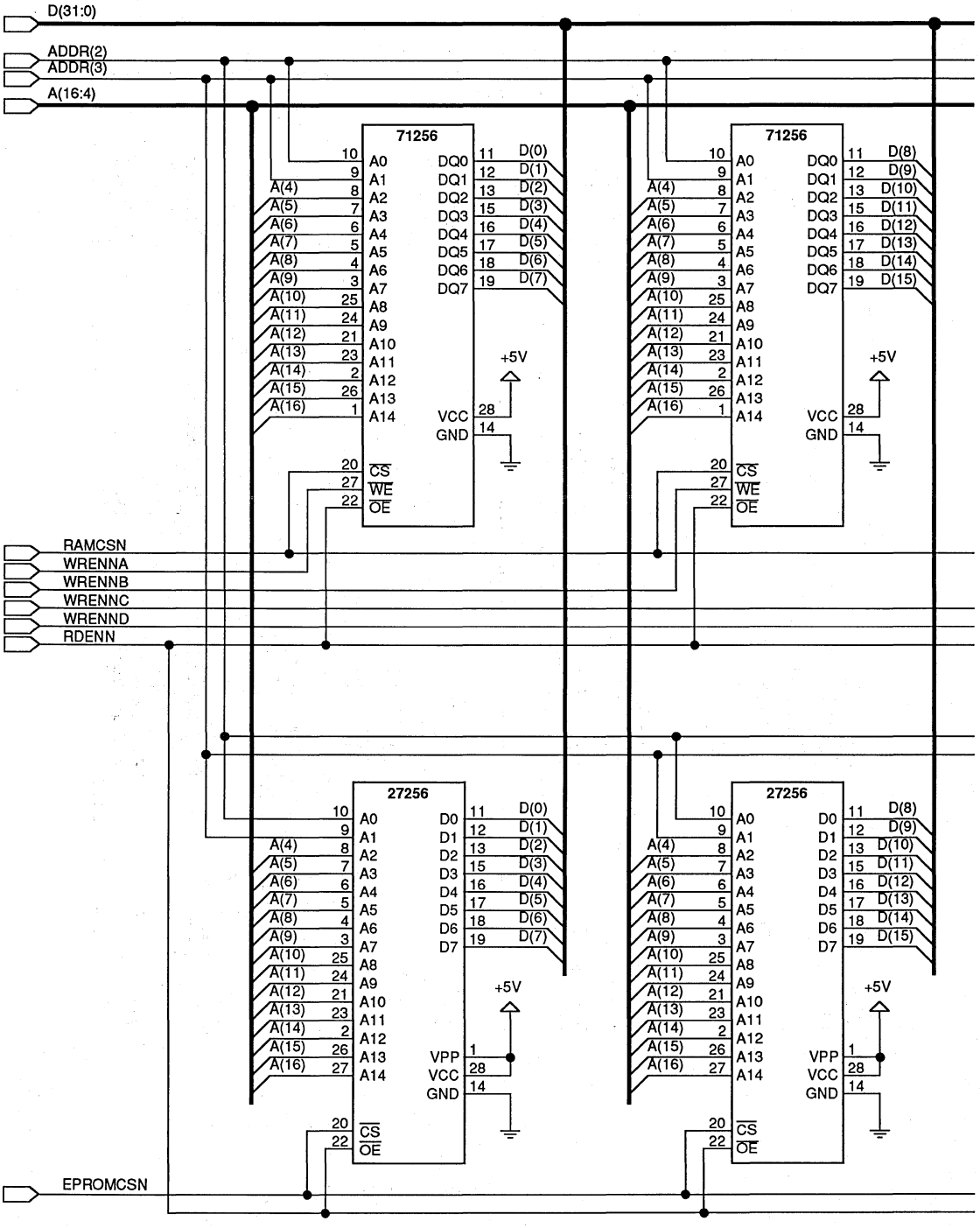


Figure 12. Address Latch Data Transceiver Demultiplexer



NOTE: BANK A -- LITTLE ENDIAN LSB BYTE 0
-- BIG ENDIAN LSB BYTE 3

Figure 13. ROM and Static RAM Memory

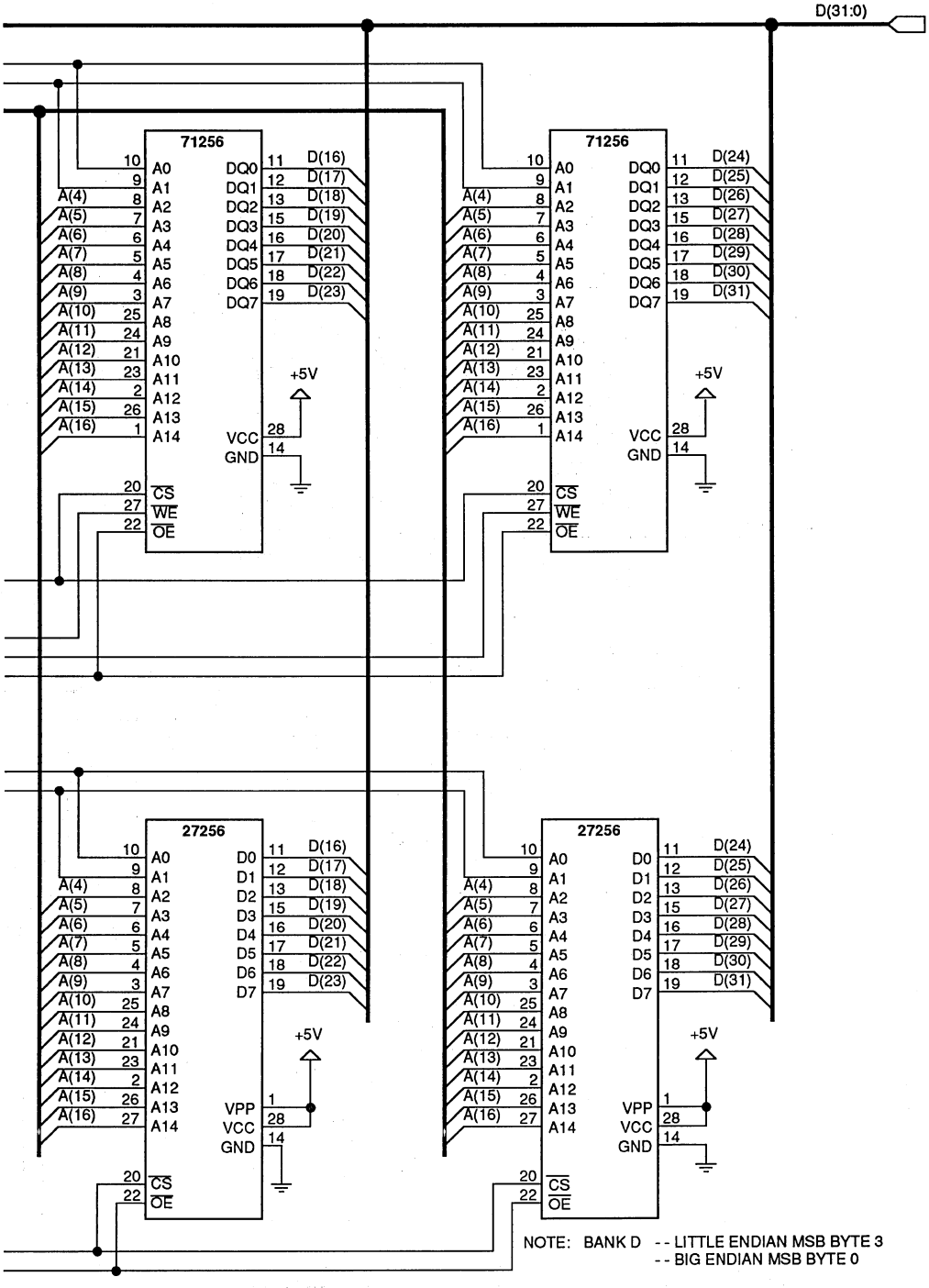


Figure 13. ROM and Static RAM Memory

C

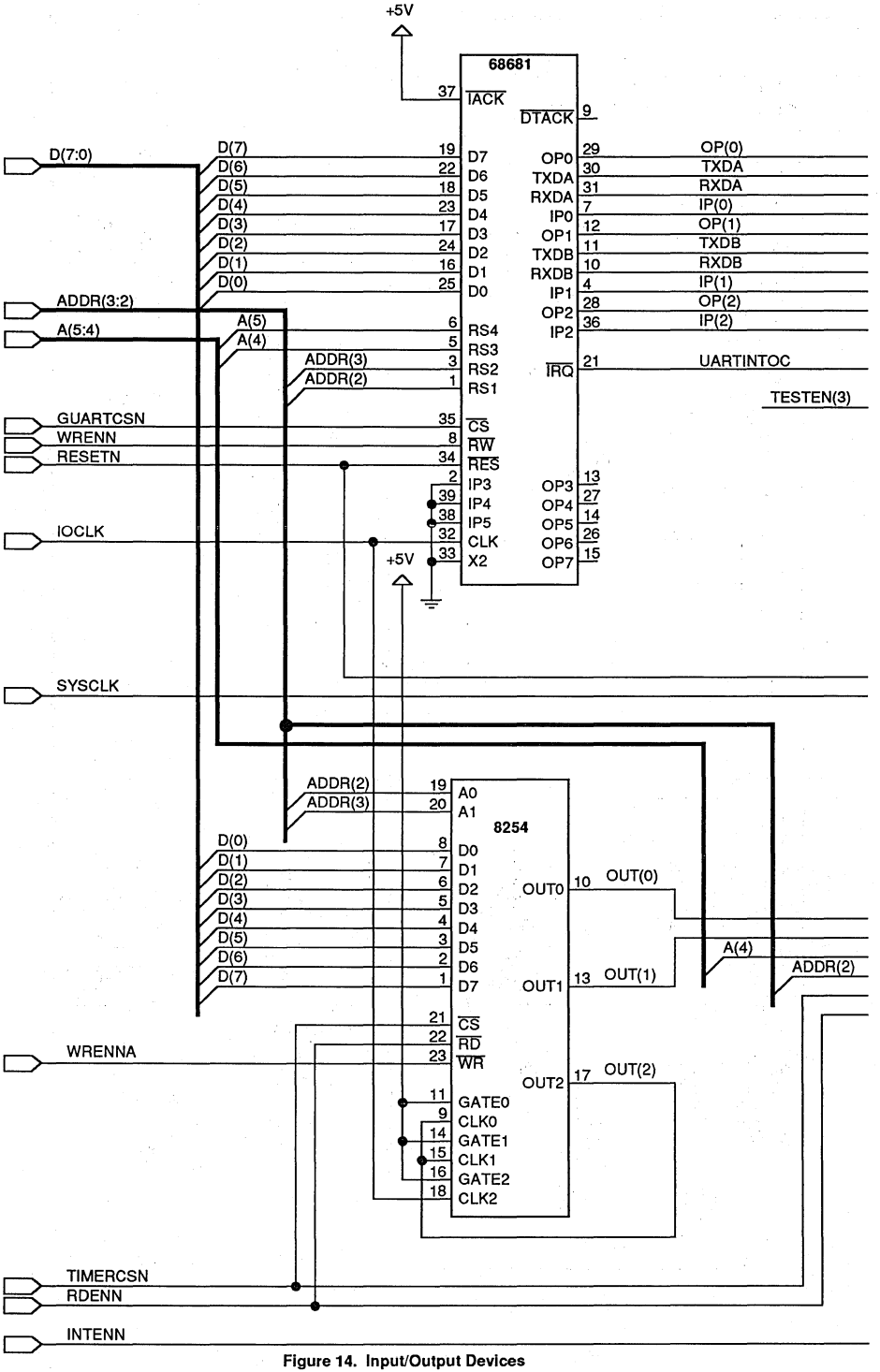


Figure 14. Input/Output Devices

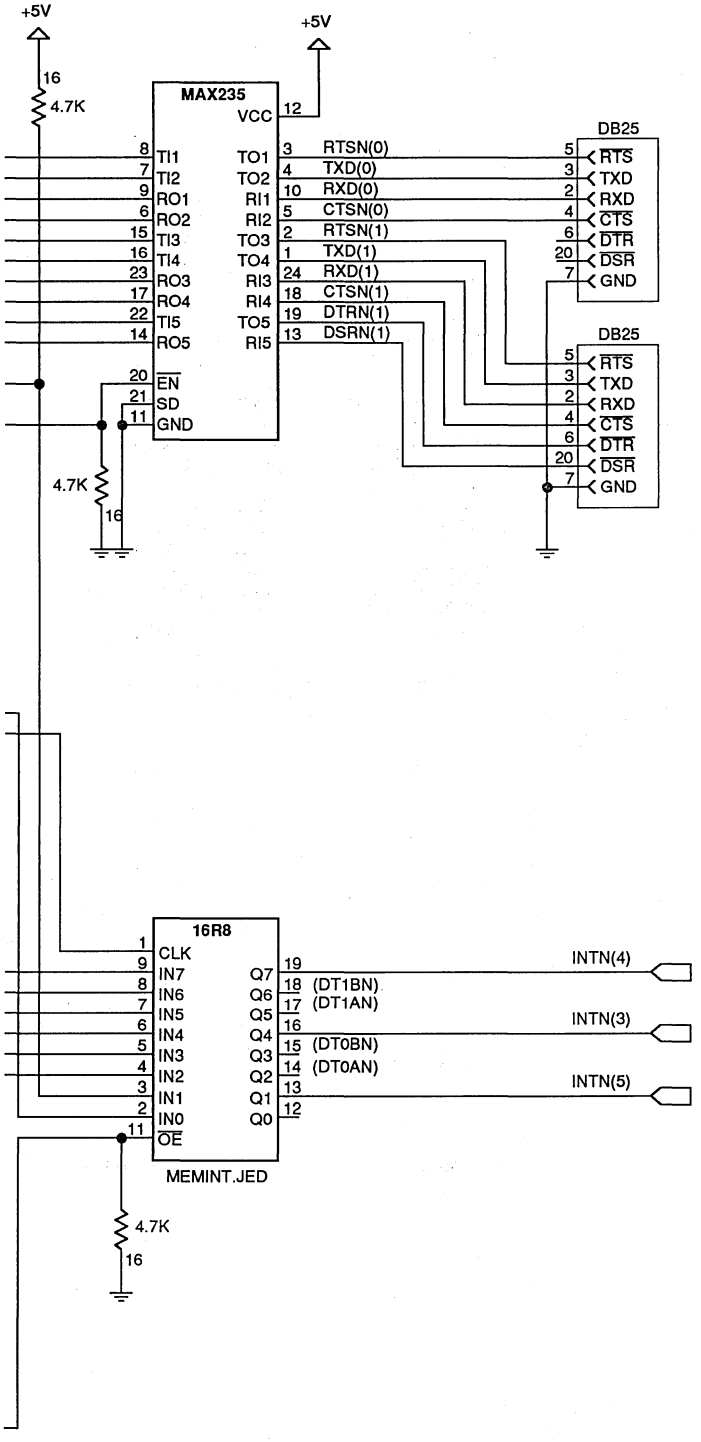


Figure 14. Input/Output Devices

C

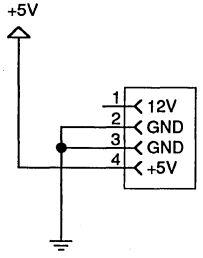


Figure 15. Power Connector

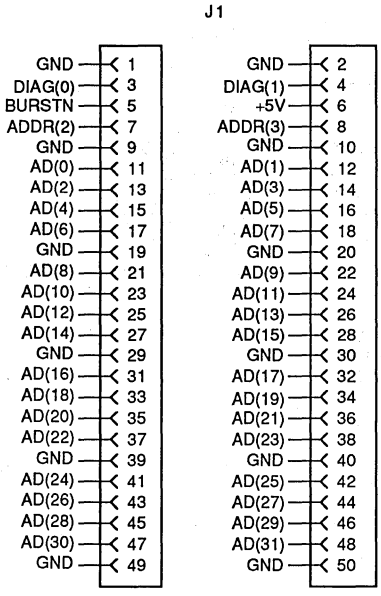


Figure 16. 50-Pin Connector

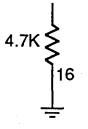


Figure 17. Spares

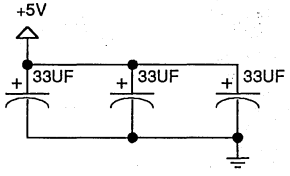


Figure 18. Primary Power Decoupling Capacitors

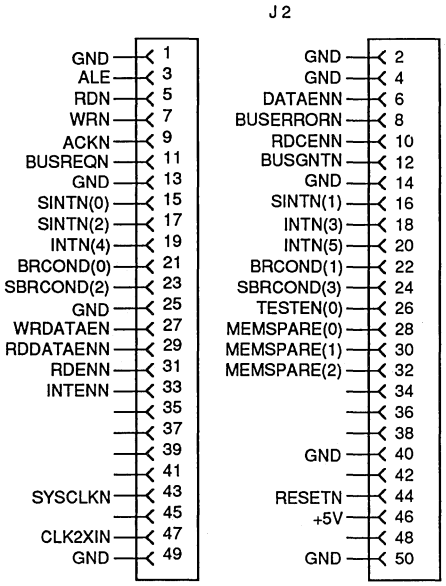


Figure 19. 50-Pin Connector

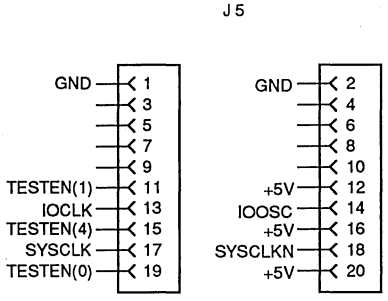


Figure 20. 100 Mil Jumper Headers

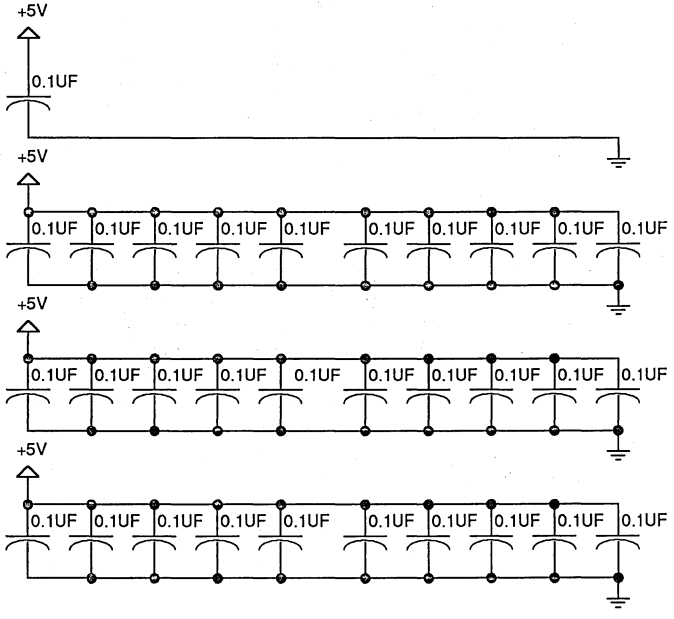


Figure 21. Decoupling Capacitors

C

```
{ TITLE    : MEMDEC.LPLC
             UPAL1 MEMORY AND I/O ADDRESS DECODER PAL FOR THE R305X
             BEHAVIORAL BUS EMULATOR MEMORY EVALUATION BOARD
  PURPOSE  : DECODES DEMULTIPLEXED ADDRESS TO GENERATE CHIP SELECTS.
  LANG     : LPLC - TM OF CAPILANO COMPUTING SYSTEMS
  AUTHOR   : ANDY NG, IDT INC.
  UPDATES  : C2503 03-18-91 AP NOTE FIRST RELEASE
}

MODULE UPAL1      ;
TITLE  UPAL1      ;
TYPE   AMD 22V10 ;

INPUTS ;
        {  DEMULTIPLEXED MEMORY ADDRESS LINES }
        A17             NODE[PIN1]  ;          { MSB ADDRESS LINES 31-17       }
        A18             NODE[PIN2]  ;
        A19             NODE[PIN3]  ;
        A20             NODE[PIN4]  ;
        A21             NODE[PIN5]  ;
        A22             NODE[PIN6]  ;
        A23             NODE[PIN7]  ;
        A24             NODE[PIN8]  ;
        A25             NODE[PIN9]  ;
        A26             NODE[PIN10] ;
        A27             NODE[PIN11] ;
        A28             NODE[PIN13] ;


        { OUTPUT FEEDBACK NODES (NEEDED FOR LPLC'ISM) }
        A29             NODE[PIN16] ;
        A30             NODE[PIN15] ;
        A31             NODE[PIN14] ;
        MEMSPARE0       NODE[PIN19] ;
        MEMSPARE1       NODE[PIN18] ;
        MEMSPARE2       NODE[PIN17] ;

OUTPUTS ; { ATTRIBUTES C - COMBINATIONAL, R - REGISTERED, H - HIGH, L - LOW }

        { CHIP SELECTS }
        RAMCSN          NODE[PIN23] ATTR[CL] ;  { STATIC RAM CHIP SELECT        }
        EPROMCSN        NODE[PIN22] ATTR[CL] ;  { EPROM CHIP SELECT             }
        UARTCSN         NODE[PIN21] ATTR[CL] ;  { UNGATED UART CHIP SELECT      }
        TIMERCSN        NODE[PIN20] ATTR[CL] ;  { TIMER CHIP SELECT             }

        { I/O PINS USED AS INPUTS }
        A29             NODE[PIN14] ATTR[CL] ;  { MSB ADDRESS LINES 31-17       }
        A30             NODE[PIN15] ATTR[CL] ;
        A31             NODE[PIN16] ATTR[CL] ;
        MEMSPARE0       NODE[PIN19] ATTR[CL] ;
        MEMSPARE1       NODE[PIN18] ATTR[CL] ;
        MEMSPARE2       NODE[PIN17] ATTR[CL] ;

        { OUTPUT ENABLES }
        RAMCSNEN        NODE[PIN23EN] ;
        EPROMCSNEN      NODE[PIN22EN] ;
        UARTCSNEN       NODE[PIN21EN] ;
```

```
        TIMERCSNEN      NODE[PIN20EN] ;
        A29EN           NODE[PIN14EN] ;
        A30EN           NODE[PIN15EN] ;
        A31EN           NODE[PIN16EN] ;
        MEMSPARE0EN     NODE[PIN19EN] ;
        MEMSPARE1EN     NODE[PIN18EN] ;
        MEMSPARE2EN     NODE[PIN17EN] ;

        { ASYNCHRONOUS RESET AND SYNCHRONOUS PRESET NODES }
        RESETEN         NODE[RESET]   ;
        PRESETEN        NODE[PRESET]  ;


        { 7RS382 COMPATIBLE PHYSICAL ADDRESS DECODE MAP }
        {    RAM        00000000H - 0001FFFFH    32K    }
        {    EPROM      1FC00000H - 1FC1FFFFH    32K    }
        {    UART       1FE00000H - 1FE0003FH           }
        {    TIMER      1F800000H - 1F80002CH           }


TERMS ; { LPLC "TABLE" ALGORITHM TAKES TOO LONG TO COMPILE }

        { NOTES: MEMSPARE0 IS BEING USED FOR A BOARD CHIP SELECT
                 DRIVABLE BY ANOTHER MEMORY SYSTEM.  WITHOUT IT
                 ASSERTED LOW, THIS BOARD WILL NOT ISSUE ANY MEMORY
                 SIGNALS NOR OUTPUT ENABLE SHARED CONTROL PINS.          }
        { NOTES: MEMSPARE1 IS NOT BEING USED.  IT COULD BE USED AS AN
                 OUTPUT IF IT OR THE UPAL2 OUTPUT IT IS CONNECTED TO IS
                 TRISTATED.                                              }
        { NOTES: MEMSPARE2 IS BEING USED AS A TESTEN INPUT PIN TO
                 TRISTATE THE OUTPUTS DURING BOARD TESTING.  ANOTHER
                 USE WOULD BE FOR A BOARD CHIP SELECT - MEMCSN.
                 MEMSPARE2 IS CONNECTED TO A UPAL3 INPUT PIN.            }

        { I/O PINS USED ONLY AS INPUTS }
        A29EN           = 0 ;
        A30EN           = 0 ;
        A31EN           = 0 ;
        MEMSPARE0EN     = 0 ;
        MEMSPARE1EN     = 0 ;
        MEMSPARE2EN     = 0 ;
        A29         NOT = 0 ;
        A30         NOT = 0 ;
        A31         NOT = 0 ;
        MEMSPARE0   NOT = 0 ;
        MEMSPARE1   NOT = 0 ;
        MEMSPARE2   NOT = 0 ;

        { RESET AND PRESET ARE NOT USED IN THIS PAL. }
        RESETEN  = 0 ;
        PRESETEN = 0 ;


        RAMCSNEN        = !MEMSPARE2 ;
        RAMCSN NOT      = !MEMSPARE0 AND
                                !A31 AND !A30 AND !A29 AND !A28
                            AND !A27 AND !A26 AND !A25 AND !A24
```

```
                        AND !A23 AND !A22 AND !A21 AND !A20
                        AND !A19 AND !A18 AND !A17
    ;


    EPROMCSNEN      = !MEMSPARE2 ;
    EPROMCSN NOT    = !MEMSPARE0 AND
                            !A31 AND !A30 AND !A29 AND  A28
                        AND  A27 AND  A26 AND  A25 AND  A24
                        AND  A23 AND  A22 AND !A21 AND !A20
                        AND !A19 AND !A18 AND !A17
    ;


    UARTCSNEN       = !MEMSPARE2 ;
    UARTCSN NOT     = !MEMSPARE0 AND
                            !A31 AND !A30 AND !A29 AND  A28
                        AND  A27 AND  A26 AND  A25 AND  A24
                        AND  A23 AND  A22 AND  A21 AND !A20
                        AND !A19 AND !A18 AND !A17
    ;


    TIMERCSNEN      = !MEMSPARE2 ;
    TIMERCSN NOT    = !MEMSPARE0 AND
                            !A31 AND !A30 AND !A29 AND  A28
                        AND  A27 AND  A26 AND  A25 AND  A24
                        AND  A23 AND !A22 AND !A21 AND !A20
                        AND !A19 AND !A18 AND !A17
    ;


END;
END UPAL1.
```

```
{ TITLE   : MEMCONT.LPLC
            UPAL2 MEMORY CONTROLLER PAL FOR THE R305X BEHAVIORAL BUS EMULATOR
            MEMORY EVALUATION BOARD
  PURPOSE: PRODUCES READ, WRITE, AND BUS ERROR ACKNOWLEDGE CONTROLS (RDCENN,
            ACKN, BUSERRORN) BASED ON A 4 OR 5 BIT COUNTER AND CYCLE END
            STALL CYCLE (WAIT STATE) EQUATIONS.
  LANG    : LPLC - TM OF CAPILANO COMPUTING SYSTEMS
  AUTHOR : ANDY NG, IDT INC.
  UPDATES: C4B28 03-18-91 AP NOTE FIRST RELEASE
}

MODULE UPAL2      ;
TITLE  UPAL2      ;
TYPE   AMD 22V10 ;

INPUTS ;
        { REGULAR INPUT PINS }
        SYSCLK          NODE[PIN1]  ;          { UN-INVERTED SYSTEM CLOCK      }
        RESETN          NODE[PIN2]  ;          { MASTER RESET                  }
        RDN             NODE[PIN3]  ;          { READ                          }
        WRN             NODE[PIN4]  ;          { WRITE                         }
        BURSTN          NODE[PIN5]  ;          { BURST READ | WRITE NEAR       }
        RAMCSN          NODE[PIN6]  ;          { RAM CHIP SELECT               }
        EPROMCSN        NODE[PIN7]  ;          { EPROM CHIP SELECT             }
        UARTCSN         NODE[PIN8]  ;          { UART CHIP SELECT              }
        TIMERCSN        NODE[PIN9]  ;          { TIMER CHIP SELECT             }
        MEMSPARE0       NODE[PIN10] ;          {                               }
        MEMSPARE2       NODE[PIN11] ;          {                               }
        TESTEN          NODE[PIN13] ;          { TEST PIN TO Z-STATE OUTPUTS   }

        { REGISTER FEEDBACK PINS }
        C WIDTH[5]      NODE[PIN15,PIN14,PIN21,PIN22,PIN23] ;
        ENSTARTN        NODE[PIN16] ;
        CYCENDN         NODE[PIN18] ;
        RDCENN          NODE[PIN19] ;
        ACKN            NODE[PIN20] ;
        BUSERRORN       NODE[PIN17] ;


OUTPUTS ; { ATTRIBUTES C - COMBINATIONAL, R - REGISTERED, H - HIGH, L - LOW  }

        { REGISTERED OUTPUT PINS }
        { BINARY UP COUNTER INPUTS MSB TO LSB C4, C3, C2, C1, C0 }
        C WIDTH[5]      NODE[PIN15,PIN14,PIN21,PIN22,PIN23] ATTR[RL] ;
        ENSTARTN        NODE[PIN16] ATTR[RL] ;  { READ/WRITE OUTPUT ENABLE START }
        CYCENDN         NODE[PIN18] ATTR[RL] ;  { CYCLE END (COMPOSITE ACK)      }
        RDCENN          NODE[PIN19] ATTR[RL] ;  { R305X READ BUFFER CLOCK ENABLE }
        ACKN            NODE[PIN20] ATTR[RL] ;  { R3050X ACKNOWLEDGE             }
        BUSERRORN       NODE[PIN17] ATTR[RL] ;  { R305X BUS ERROR                }

        { OUTPUT ENABLES }
        CEN WIDTH[5]    NODE[PIN15EN,PIN14EN,PIN21EN,PIN22EN,PIN23EN] ;
        ENSTARTNEN      NODE[PIN16EN] ;
        CYCENDNEN       NODE[PIN18EN] ;
        RDCENNEN        NODE[PIN19EN] ;
        ACKNEN          NODE[PIN20EN] ;
        BUSERRORNEN     NODE[PIN17EN] ;
```

C

```
        { ASYNCHRONOUS RESET AND SYNCHRONOUS PRESET NODES }
        RESETEN          NODE[RESET]  ;
        PRESETEN         NODE[PRESET] ;


TABLE ;

        { RESET AND PRESET ARE NOT BEING USED.                                    }
        RESETEN  = 0 ;
        PRESETEN = 0 ;

        { PURPOSE: PROVIDES REGISTERED VERSION OF RDN AND WRN.

          NOTE:    QRDN AND QWRN ARE KEPT LOW ONE EXTRA CLOCK BY CYCENDN.
                   THIS IS BECAUSE THE RISING EDGE OF RDN OR WRN MAY NOT
                   HAVE ENOUGH HOLD TIME FROM THE RISING EDGE OF
                   (BUFFERRED) SYSCLK.
          NOTE:    QRDN AND QWRN DO NOT NECESSARILY TRANSITION BACK HIGH
                   BETWEEN CONSECUTIVE MEMORY CYCLES, E.G., WRITE FOLLOWED
                   BY A WRITE.                                                    }

        { QRDN NOT       :=   RESETN AND (!RDN OR (!QRDN AND !CYCENDN)) ; }
        { QWRN NOT       :=   RESETN AND (!WRN OR (!QWRN AND !CYCENDN)) ; }


        { PURPOSE: C[4]-C[0] PROVIDES A 5-BIT BINARY UP COUNTER.  IT IS RESET
                   ANYTIME RESETN IS ASSERTED AND AT THE END
                   OF EVERY MEMORY CYCLE AFTER CYCENDN IS ASSERTED.
                   IT BEGINS COUNTING UP WHEN A READ OR WRITE CYCLE IS
                   INITIATED.
          NOTE:    CYCENDN IS ASSUMED TO ASSERT WITH THE LAST RDCENN
                   ON READS AND WITH ACKN ON WRITES.  THUS CYCENDN WILL CLEAR
                   THE COUNTER WHETHER OR NOT RDN OR WRN HIGH TRANSITION
                   MEETS THE REGISTER SETUP AND HOLD TIME REQUIREMENTS.           }

        { NOTE:    TO ADD A GENERAL PURPOSE READY (A.K.A. BUSYN AND WAITN)
                   INPUT, CHANGE EACH OF THE COUNTER C[4:0] EQUATIONS SO
                   THAT THEIR VALUE CAN BE HELD WITH AN ADDITIONAL TERM, E.G.:
                   C[0]    :=  RESETN AND CYCENDN AND (!RDN OR !WRN)
                                  AND (    (C[0] XOR 1)
                                        OR (C[0] AND !READY) ) ;
                   A READY INPUT CAN BE USED FOR DUAL-PORT MEMORY INTERFACING,
                   EEPROM WRITE INTERFACING, ETC.
        }

        CEN[0]   =   !TESTEN ;
        CEN[1]   =   !TESTEN ;
        CEN[2]   =   !TESTEN ;
        CEN[3]   =   !TESTEN ;
        CEN[4]   =   !TESTEN ;

        C[0]    :=   RESETN AND CYCENDN AND (!RDN OR !WRN)
                        AND (C[0] XOR 1) ;
        C[1]    :=   RESETN AND CYCENDN AND (!RDN OR !WRN)
                        AND (C[1] XOR C[0]) ;
        C[2]    :=   RESETN AND CYCENDN AND (!RDN OR !WRN)
                        AND (C[2] XOR (C[1] AND C[0])) ;
```

```
C[3]     :=   RESETN AND CYCENDN AND (!RDN OR !WRN)
                 AND (C[3] XOR (C[2] AND C[1] AND C[0])) ;
C[4]     :=   RESETN AND CYCENDN AND (!RDN OR !WRN)
                 AND (C[4] XOR (C[3] AND C[2] AND C[1] AND C[0])) ;


{ PURPOSE: ENSTARTN OUTPUT PROVIDES THE TIMING FOR THE LEADING
           EDGE OF OEN AND WEN STROBES SO THAT 1. THE ADDRESS LINES HAVE
           TIME TO BE DECODED AND 2. OE/DATA PINS HAVE TIME TO Z-STATE
           FROM READS ON THE PRECEDING CYCLE.  THE CYCENDN TERM IS
           NEEDED TO HOLD OFF A CONSECUTIVE MEMORY CYCLE, E.G., WHEN
           WRITE DEASSERTS AND REASSERTS WITHIN THE SAME CLOCK.
           ENSTARTN SHOULD NOT BE USED TO END WRITE TRANSCEIVER
           ENABLES AS IT DEASSERTS WITH THE WRITE LINE INSTEAD OF
           HOLDING FOR ONE MORE 1/2 CLOCK.                              }

ENSTARTNEN     = !TESTEN ;
ENSTARTN  NOT := !MEMSPARE0 AND RESETN AND (C >= 1) AND CYCENDN ;


{ PURPOSE: CYCLE END GOES LOW (SYNCHRONOUSLY) DURING THE LAST RDCENN ON
           READS AND DURING ACKN ON WRITES.  IT RETURNS HIGH
           SYNCHRONOUSLY BY INTERLOCKING ON THE COUNTER OUTPUTS
           WHICH COUNT ONE GREATER THAN THE ASKED FOR VALUE BEFORE
           RESETTING BACK TO ZERO (VIA CYCENDN).  THUS CYCENDN WILL
           DEASSERT ON THE SAME CLOCK AS THE RDN, WRN, OR BURSTN RISING
           EDGES REGARDLESS OF WHETHER OR NOT THOSE RISING EDGES MEET
           THE REGISTER'S SETUP AND HOLD TIMES.                         }
{ NOTE:    TO FIT CYCENDN INTO A 16V8, TWO OUTPUTS MAY BE NEEDED.       }

CYCENDNEN     = !TESTEN ;
CYCENDN NOT := RESETN AND CYCENDN AND (
                   (!RAMCSN    AND (C == 02H) AND !RDN AND  BURSTN)
                OR (!RAMCSN    AND (C == 08H) AND !RDN AND !BURSTN)
                OR (!RAMCSN    AND (C == 03H) AND !WRN            )
                OR (!EPROMCSN AND (C == 03H) AND !RDN AND  BURSTN)
                OR (!EPROMCSN AND (C == 0CH) AND !RDN AND !BURSTN)
                OR (!UARTCSN   AND (C == 06H) AND           BURSTN)
                OR (!TIMERCSN AND (C == 06H) AND           BURSTN)
                OR ( {!BUSERRORN} (C == 1FH)                      )
);


{ NOTE: IN THIS EXPERIMENT MEMSPARE0 IS PULLED LOW AND CAN BE
        USED TO DISABLE THIS CONTROLLER'S RDCENN, ACKN, AND BUSERRORN.
        SINCE MEMSPARE0 IS ATTACHED TO THE MEMDEC.LPLC PAL, THE
        MEMDEC PAL COULD COMBINE THE CSN'S SO THAT THESE SIGNALS
        ARE ONLY DRIVEN WHEN NEEDED.                                    }

{ NOTE: ANOTHER POSSIBILITY IS TO USE MEMSPARE0 AS AN EXTRA CHIP
        SELECT.                                                         }


{ PURPOSE: READ BUFFER CLOCK ENABLE IS USED BY THE R305X TO STROBE
           DATA INTO ITS INTERNAL READ BUFFERS.                         }
{ NOTE:    IT IS ASSUMED THAT THE UART AND TIMER ARE
           IN UNCACHABLE MEMORY SPACE AND WILL NOT BE BURST READ.
           IF THEY ARE BURST READ, THE STATE MACHINE LOOPS 4 TIMES.     }
```

C

```
RDCENNEN      = !MEMSPARE0 ;
RDCENN NOT   := RESETN AND CYCENDN AND (
                  (!RAMCSN AND !RDN
                     AND (                  (C == 02H)
                           OR (!BURSTN AND (C == 04H))
                           OR (!BURSTN AND (C == 06H))
                           OR (!BURSTN AND (C == 08H))
                         )
                  )
               OR (!EPROMCSN AND !RDN
                     AND (                  (C == 03H)
                           OR (!BURSTN AND (C == 06H))
                           OR (!BURSTN AND (C == 09H))
                           OR (!BURSTN AND (C == 0CH))
                         )
                  )
               OR (!UARTCSN AND !RDN
                     AND (                  (C == 06H)
                         )
                  )
               OR (!TIMERCSN AND !RDN
                     AND (                  (C == 06H)
                         )
                  )
);


{ PURPOSE: ACKNOWLEDGE IS PRIMARILY USED TO END WRITE CYCLES.  IT
           SHOULD BE PULSED ONE (HALF) CLOCK CYCLE BEFORE THE WRITE
           STROBE IS NEEDED.  ON READ CYCLES, ACKNOWLEDGE WILL
           IMPLICITLY BE GENERATED BY THE R305X, HOWEVER, IF OPTIMAL
           TIMING IS DESIRED, ACK SHOULD BE DRIVEN NO SOONER THAN 1
           CLOCK BEFORE THE END OF A SINGLE READ AND FOR BURSTS NO
           SOONER THAN 4 CLOCKS BEFORE THE END OF THE LAST READ.        }

ACKNEN        = !MEMSPARE0 ;
ACKN NOT     := RESETN AND CYCENDN AND (
                  (!RAMCSN AND !WRN                          { WRITE CYCLE }
                     AND (                  (C == 03H)
                         )
                  )
                OR (!RAMCSN AND !RDN AND !BURSTN             { READ  CYCLE }
                     AND (                  (C == 05H)
                         )
                  )
                OR (!EPROMCSN AND !RDN AND !BURSTN           { READ  CYCLE }
                     AND (                  (C == 09H)
                         )
                  )
                OR (!UARTCSN AND !WRN AND BURSTN             { WRITE CYCLE }
                     AND (                  (C == 06H)
                         )
                  )
```

```
                    OR (!TIMERCSN AND !WRN                          { WRITE CYCLE }
                          AND (                 (C == 06H)
                              )
                       )
        );


        { PURPOSE: BUSERRORN SIMPLY ENDS A WAYWARD UNDECODED BUS CYCLE.  ON
                   READS IT CAUSES AN EXCEPTION.  ON WRITES IT DOES NOT CAUSE
                   AN EXCEPTION CONDITION FOR THE PROCESSOR.  TO DO THAT, LATCH
                   BUSERRORN AND FEED IT TO AN INTERRUPT PIN OR A BRANCH
                   CONDITION PIN.                                           }

        BUSERRORNEN     = !MEMSPARE0 ;
        BUSERRORN NOT := RESETN AND CYCENDN AND (
                                              (C == 1FH)

        ) ;


END ;
END UPAL2.
```

C

```
{ TITLE    : MEMEN.LPLC
             UPAL3 MEMORY READ AND WRITE ENABLE PAL FOR THE R305X BEHAVIORAL BUS
             EMULATOR MEMORY EVALUATION BOARD
  PURPOSE  : GENERATES READ AND WRITE ENABLES FOR MEMORY CONTROLS.
  LANG     : LPLC – TM OF CAPILANO COMPUTING SYSTEMS
  AUTHOR   : ANDY NG, IDT INC.
  UPDATES  : C7C4F 03-18-91 AP NOTE FIRST RELEASE
}

MODULE UPAL3     ;
TITLE  UPAL3     ;
TYPE   AMD 22V10 ;

INPUTS ;
        {  DEMULTIPLEXED MEMORY ADDRESS LINES }
        SYSCLK          NODE[PIN1]  ;          { INVERTED SYSCLKN              }
        POWRESETN       NODE[PIN2]  ;          { POWER UP RESET                }
        RDN             NODE[PIN3]  ;          { READ LINE                     }
        WRN             NODE[PIN4]  ;          { WRITE LINE                    }
        ENSTARTN        NODE[PIN5]  ;          { ENABLE START                  }
        CYCENDN         NODE[PIN6]  ;          { CYCLE END                     }
        BEN0            NODE[PIN7]  ;          { BYTE ENABLE 0                 }
        BEN1            NODE[PIN8]  ;          { BYTE ENABLE 1                 }
        BEN2            NODE[PIN9]  ;          { BYTE ENABLE 2                 }
        BEN3            NODE[PIN10] ;          { BYTE ENABLE 3                 }
        UARTCSN         NODE[PIN11] ;          { UART CHIP SELECT              }
        MEMSPARE2       NODE[PIN13] ;          { SPARE INPUT                   }

        { OUTPUT FEEDBACK NODES (NEEDED FOR LPLC'ISM) }
        RESETN          NODE[PIN23] ;
        WRENN           NODE[PIN18] ;
        WRDATAEN        NODE[PIN17] ;

OUTPUTS ; { ATTRIBUTES C – COMBINATIONAL, R – REGISTERED, H – HIGH, L – LOW }

        { WRITE ENABLES }
        WRENNA          NODE[PIN22] ATTR[RL] ;  { WRITE ENABLE FOR BYTE 0       }
        WRENNB          NODE[PIN21] ATTR[RL] ;  { WRITE ENABLE FOR BYTE 1       }
        WRENNC          NODE[PIN20] ATTR[RL] ;  { WRITE ENABLE FOR BYTE 2       }
        WRENND          NODE[PIN19] ATTR[RL] ;  { WRITE ENABLE FOR BYTE 3       }
        WRENN           NODE[PIN18] ATTR[RL] ;  { WRITE ENABLE MOTO-TYPE I/O    }
        WRDATAEN        NODE[PIN17] ATTR[RL] ;  { WRITE DATA XCEIVER ENABLE     }

        { READ ENABLES }
        RDENN           NODE[PIN16] ATTR[RL] ;  { READ OUTPUT ENABLE (FOR WORDS)}
        RDDATAENN       NODE[PIN15] ATTR[RL] ;  { READ DATA XCEIVER ENABLE      }

        { MISCELLANEOUS CONTROLS }
        RESETN          NODE[PIN23] ATTR[RL] ;  { SYNCHRONIZED RESET            }
        GUARTCSN        NODE[PIN14] ATTR[RL] ;  { GATED/GUARDED UART CHIP SELECT}

        { I/O PINS USED AS INPUTS }
        { NONE }

        { OUTPUT ENABLES }
        WRENNAEN        NODE[PIN22EN] ;
        WRENNBEN        NODE[PIN21EN] ;
```

```
        WRENNCEN        NODE[PIN20EN] ;
        WRENNDEN        NODE[PIN19EN] ;
        WRENNEN         NODE[PIN18EN] ;
        WRDATAENEN      NODE[PIN17EN] ;
        RDENNEN         NODE[PIN16EN] ;
        RDDATAENNEN     NODE[PIN15EN] ;
        RESETNEN        NODE[PIN23EN] ;
        GUARTCSNEN      NODE[PIN14EN] ;

        { ASYNCHRONOUS RESET AND SYNCHRONOUS PRESET NODES }
        RESETEN         NODE[RESET]   ;
        PRESETEN        NODE[PRESET]  ;

TABLE ;

        { RESET AND PRESET ARE NOT USED IN THIS PAL. }
        RESETEN  = 0 ;
        PRESETEN = 0 ;


        { PURPOSE: WRITE BYTE ENABLES AND WRITE WORD ENABLE ALLOW
                   SUFFICIENT TIME FOR THE ADDRESS TO DECODE AND
                   FOR A VALID CHIP SELECT BEFORE ENABLING THE
                   WRITE STROBE FOR A SPECIFIC BYTE BANK.
          NOTE:    BANK A IS THE BIG ENDIAN'S LSB BYTE3 OR THE LITTLE
                   ENDIAN'S LSB BYTE0.  IT ALWAYS HOLDS D(7:0).
                   BANK D IS THE BIG ENDIAN'S MSB BYTE0 OR THE BIG
                   ENDIAN'S MSB BYTE3.  IT ALWAYS HOLDS D(31:23).
                                                                    }

        WRENNAEN          = !MEMSPARE2 ;
        WRENNA       NOT := RESETN AND (
                               !WRN AND !BEN0 AND !ENSTARTN AND CYCENDN
        );

        WRENNBEN          = !MEMSPARE2 ;
        WRENNB       NOT := RESETN AND (
                               !WRN AND !BEN1 AND !ENSTARTN AND CYCENDN
        );

        WRENNCEN          = !MEMSPARE2 ;
        WRENNC       NOT := RESETN AND (
                               !WRN AND !BEN2 AND !ENSTARTN AND CYCENDN
        );

        WRENNDEN          = !MEMSPARE2 ;
        WRENND       NOT := RESETN AND (
                               !WRN AND !BEN3 AND !ENSTARTN AND CYCENDN
        );

        { PURPOSE: WRENN IS USED TO PROVIDE A WRITE LINE THAT HOLDS
                   LOW FOR AN EXTRA CYCLE, SO THAT IT CAN BE USED FOR
                   MOTOROLA-TYPE I/O DEVICES ON THEIR MULTIPLEXED
                   READ/WRITE LINE.                                 }

        WRENNEN           = !MEMSPARE2 ;
        WRENN        NOT := RESETN AND (
```

C

```
                    (!WRN AND CYCENDN)
                OR (!WRENN AND !CYCENDN)
);

{ PURPOSE: WRDATAEN AND RDDATAENN DRIVE THE OUTPUT ENABLE
           CONTROLS ON A FCT623T TRANSCEIVER BANK FOR THE
           DATA BUS.  THE CONTROLS CAN BE USED FOR ANY
           DUAL-OUTPUT ENABLE TRANSCEIVER (1 FOR EACH
           DIRECTION.  OUTPUT ENABLE/DIRECTION CONTROLLED
           TRANSCEIVERS (FCT245) REQUIRE MORE INTERFACING
           IF OUTPUT CONTENTION IS TO BE AVOIDED BY
           ONLY CHANGING THE DIRECTION WHEN THE OUTPUTS ARE
           DISABLED.                                        }

{ NOTE:    WRITE DATA ENABLE DEASSERTS ONE CLOCK AFTER
           WRN DOES TO PROVIDE SUFFICIENT HOLD TIME FOR THE
           WRITE DATA INTO THE MEMORY (SEE UPAL2 QWRN FOR A
           MORE DETAILED EXPLANATION).
  NOTE:    WRDATAEN IS ACTIVE HIGH FOR THE FCT623T OUTPUT ENABLE
           CONTROL.  FOR THE FCT861 OUTPUT ENABLES, USE ACTIVE
           LOW.
  NOTES:   THE FIRST OR-TERM ASSERTS WRDATAEN WHILE THE SECOND
           OR-TERM DEASSERTS WRDATAEN.                      }

WRDATAENEN       = !MEMSPARE2 ;
WRDATAEN        := RESETN AND (
                       (!WRN AND !ENSTARTN)
                   OR (WRDATAEN AND (!ENSTARTN OR !CYCENDN))
);

RDENNEN          = !MEMSPARE2 ;
RDENN      NOT := RESETN AND (
                       !RDN AND !ENSTARTN AND CYCENDN
);

{ PURPOSE: RDDATAENN IS CONNECTED TO THE MEMORY BOARD'S
           DATA TRANSCEIVER OUTPUT ENABLE (FCT623T OR FCT861)
           AND ONLY ENABLES FOR THIS BOARD'S CHIP SELECTS.
           IF THE MEMORY CONTROLLER IS USED FOR ANOTHER
           BOARD'S MEMORY, THEN THE TRANSCEIVER OUTPUT ENABLE
           SHOULD BE DISABLED FOR THOSE CHIP SELECTS (VIA
           MEMSPARE2.                                       }

{ NOTE:    IN MOST SYSTEMS, R305X'S DATAENN OUTPUT CAN BE
           CONNECTED DIRECTLY TO THE TRANSCEIVER ENABLE PIN
           INSTEAD OF USING A SYNTHESIZED RDDATAENN.        }

RDDATAENNNEN     = !MEMSPARE2 ;
RDDATAENN  NOT := RESETN AND (
                       !RDN AND !ENSTARTN AND CYCENDN
);


{ PURPOSE: RESET SYNCHRONIZES THE POWER UP RESET FOR THE
           MEMORY CONTROLLER STATE MACHINES AND FOR THE R305X.  }

RESETNEN         = !MEMSPARE2 ;
RESETN     NOT := !POWRESETN ;
```

```
        { PURPOSE: GUARDED/GATED UART CHIP SELECT, GUARTCSN GATES
                   UARTCSN BECAUSE THE UART BEING USED HAS A MOTOROLA-
                   TYPE I/O DEVICE INTERFACE WHICH MULTIPLEXES ITS
                   READ/WRITE INPUT PIN SUCH THAT THE CHIP SELECT MUST
                   STROBE IN OR OUT DATA.  THIS IS IN CONTRAST TO AN
                   INTEL-TYPE I/O DEVICE INTERFACE WHICH WOULD HAVE A
                   SEPARATE READ STROBE AND WRITE STROBE AS WELL AS A
                   CHIP SELECT.  IT IS IMPORTANT NOT TO HAVE A
                   GLITCH (FROM ADDRESS DECODING THE CHIP SELECT) ON
                   READS IN ORDER TO ALLOW THE I/O DEVICE TO UPDATE
                   FIFO POINTERS, ETC.  THUS GUARTCSN STARTS LATE AND
                   ENDS EARLY, SO THAT READ/WRITE IS HELD VALID
                   THROUGHOUT THE CHIP SELECT.                          }

        GUARTCSNEN       = !MEMSPARE2 ;
        GUARTCSN     NOT := RESETN AND (
                              !UARTCSN AND !ENSTARTN AND CYCENDN
        );

END;
END UPAL3.
```

C

```
{ TITLE   : MEMINT.LPLC
            UPAL4 MEMORY I/O INTERRUPT CONTROLLER PAL FOR THE R305X BEHAVIORAL
            BUS EMULATOR MEMORY EVALUATION BOARD
  PURPOSE: REPLICATES THE TIMER/UART INTERRUPT CONTROLLER ON THE 7RS382 BOARD.
            ADDITIONAL FUSE BITS ADDED FOR 16V8 COMPATIBILITY.
  LANG    : LPLC - TM OF CAPILANO COMPUTING SYSTEMS
  AUTHOR : IDT INC.
  UPDATES: C3F98 01-04-91 16V8 PCB VERSION FIRST RELEASE A.N.
}


{ U24A_382 INTERRUPT PAL}
{ 1-2-90,12-14-89 }
{JEDEC file's CHECKSUM = 379E } { NOTE: 01-04-91 - NOT APPLICABLE TO 16V8 }

{     CONTROL PAL FOR 8254 TIMER'S AND UART INTERRUPT
      USED FOR EVALUATION BOARD 382 }

MODULE U24A_382;
TITLE U24A_382;
TYPE MMI 16R8;

{ FUSE BITS FOR 16V8 FAMILY ATTRIBUTES USED AS A 16R8 }
FUSE 2048..2079 00000000000000000000000000000000 ;
FUSE 2080..2111 00000000000000000000000000000000 ;
FUSE 2112..2143 00000000000000001111111111111111 ;
FUSE 2144..2175 11111111111111111111111111111111 ;
FUSE 2176..2193 111111111111111101               ;

INPUTS;

MRES/       NODE[PIN2];
UARTINT/    NODE[PIN3];
PMRD/       NODE[PIN4];
CSTIM/      NODE[PIN5];
EA02        NODE[PIN6];
EA04        NODE[PIN7];
OUT1        NODE[PIN8]; {input from Timer output OUT1}
OUT0        NODE[PIN9]; {input from Timer output OUT0}

DT0A/       NODE[PIN14]; {feedback}
DT0B/       NODE[PIN15]; {feedback}
T0INT/      NODE[PIN16]; {feedback}

DT1A/       NODE[PIN17]; {feedback}
DT1B/       NODE[PIN18]; {feedback}
T1INT/      NODE[PIN19]; {feedback}

OUTPUTS;

UINT5/      NODE[PIN13];
DT0A/       NODE[PIN14];
DT0B/       NODE[PIN15];
T0INT/      NODE[PIN16]; { goes to R3000's UINT3}

DT1A/       NODE[PIN17];
DT1B/       NODE[PIN18];
T1INT/      NODE[PIN19]; { goes to R3000's UINT4}
```

```
TABLE;
{     8254 TIMER generates 2 square-wave outputs OUT0 and OUT1.
      When OUT0 goes from high to low, this PAL asserts interrupt
      TOINT/, which will interrupt R3000 through UINT3.
      Same scheme applies to OUT1, T1INT/ and UINT4.
      Reading physical addresses 1F80 0010 and 1F80 0014 (which are
      virtual addresses BF80 0010 and BF80 0014 in this 382 board)
      will clear interrupt UINT3 and UINT4, respectively.

      This PAL also synchronizes UART interrupt signal }


DT0A/       :=     OUT0;        {delay TIMER's OUT0 through a register}
DT0B/       :=     DT0A/;       {delay again}
T0INT/ NOT  :=     MRES/ AND
                   ((NOT DT0A/ AND DT0B/) OR
                   (NOT T0INT/ AND (NOT EA04 OR EA02 OR CSTIM/ OR PMRD/)));

DT1A/       :=     OUT1;
DT1B/       :=     DT1A/;
T1INT/ NOT  :=     MRES/ AND
                   ((NOT DT1A/ AND DT1B/) OR
                   (NOT T1INT/ AND (NOT EA04 OR NOT EA02 OR CSTIM/ OR PMRD/)));

UINT5/      :=     UARTINT/ OR NOT MRES/ ;
                   {put UART's interrupt through a register to synchronize
                   it with R3000 clock }
END;
END U24A_382.
```

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Integrated Device Technology, Inc.

IDT79R3000/R3001 SYSTEM PERFORMANCE ANALYSIS

APPLICATION NOTE AN-87

By Dean M. Smith

INTRODUCTION

Pixstats and *cache2000* are MIPS Computer Systems, Inc. software tools that allow you to evaluate all possible 79R3000 and 79R3001 system designs to determine the optimum price/performance solution. These same tools play a large a role in processor selection. The statistics generated by *pixstats* and *cache2000* allow you to esdtablish the exact performance on various 79R3000/3001-based systems for comparison to other candidate microprocessor systems.

Pixstats projects the number of 79R3000/1 integer unit and 79R3010 floating-point unit pipeline interlock cycles. *Cache2000* models the 79R3000/1 memory subsystem detailed in Figure 1, thereby projecting the penalties incurred for accesses to asynchronous main memory. Cache size, asynchronous-memory access penalties, write-buffer size, cache burst-refill size, TLB miss penalties, cache flushing, and other parameters can be varied and the exact performance impact acertained *Pixstats* and *cache2000* together provide complete analysis of 79R3000/1 compiler and target-system performance.

INTERPRETATION OF STATISTICS

'Synchronous' System

The large allowable cache size for the 79R3000 (512Kb max) and the 79R3001 (32Mb max) permit entire applications to be housed in synchronous memory. Or, if needed, the time-critical portion of a larger task or kernel can be locked in cache segment. The performance of these 79R3000/1 'synchronous' solutions is determined from *pixstats*.

Since *pixstats* assumes a 100% cache hit-rate, the performance statistics generated are those for a 'synchronous' system design. Asynchronous main memory access penalties are not simulated by *pixstats*. *Pixstats* assumes that the application is operating in KSEG0 and KSEG1 virtual address segments. Thus, TLB and uTLB miss penalties are not simulated. Any additional run-time cycles incurred are a result of the 79R3000 integer multiply/divide busy interlock cycles and the 79R3010 floating-point busy interlock cycles.

The 79R3000/1 has a separate multiply and divide unit that takes 12 and 35 cycles, respectively, for integer multiply and divide . Attempts to prematurely read the result of a multiply or divide cause the pipeline to stall (ie. interlock) until the operation has been completed. Also, a new multiply or divide operation can not begin before a previously issued one completes. Such resource conflicts also cause the pipeline to stall. The 79R3010 has separate add, multiply, and divide units and will similarly stall its own pipeline when conflicts occur. The optimizing compiler reduces the number of pipeline stalls by re-scheduling the 79R3000/1 and the 79R3010 pipelines to eliminate as many data and resource conflicts as possible. In the example *pixstats* output in Figure 2, the total number of run-time cycles calculated is 10211. The difference between this number and the 8795 instructions executed is equal to the total number of 79R3000/1 and 79R3010 interlock cycles.

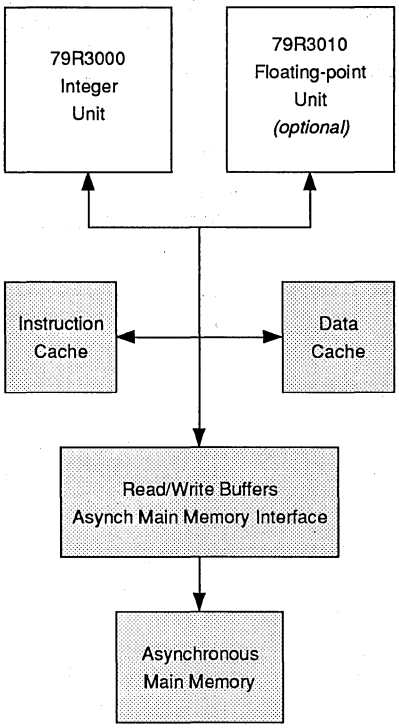


Figure 1. 79R3000/1 Memory Subsystem

All 79R3000/1 cache accesses are on word boundaries. Consequently, Partial Word Store, Store Word Left, and Store Word Right instructions are implemented as two cycle read-modify-write operations. However, *pixstats* was originally written to model the 79R2000, the first implementation of the MIPS architecture. The 79R2000 implemented these special instructions as one-cycle operations, simultaneously updating main memory and invalidating the corresponding cache entry. This is the only shortcoming of *pixstats* in modeling the 79R3000/1 and the 79R3010. Thus, *the total number of run-time cycles for a 'synchronous' system operating out of virtual address segments KSEG0 or KSEG1 is equal to the number of run-time cycles calculated by pixstats plus the number of two cycle store instructions (sb, sh, swl, swr).* The number of two cycle store instructions is obtainable

from the opcode distribution section of the *pixstats* output. For the example in Figure 2 there are 127 sb instructions and 102 sh instructions accounting for a total run-time of 10340 cycles (ie. 129 two cycle stores + 10211 cycles calculated by PIXSTATS).

'Cached' System

A 'cached' 79R3000/1 system is one in which a smaller synchronous memory behaves as a cache to a larger and slower asynchronous memory. Such a target system does not have enough synchronous memory to house the entire application.

Example:

10211 (1.161) cycles (0.000408s @ 25.0MHz)
8795 (1.000) instructions
.
.
.
0 (0.000) multiply/divide interlock cycles (12/35 cycles)
— these are due to R3000/1 Data and Resource Conflicts.
604 (0.069) flops (1.48 mflop/s @ 25.0MHz)
112 (0.013) floating point data interlock cycles
— these are due to R3010 Data Conflicts
336 (0.038) floating point add unit interlock cycles
— these are due to R3010 Resource Conflicts
0 (0.000) floating point multiply unit interlock cycles
— these are due to R3010 Resource Conflicts
0 (0.000) floating point divide unit interlock cycles
— these are due to R3010 Resource Conflicts
968 (0.110) other floating point interlock cycles
— these are due to R3010 ?
112 (0.013) 1 cycle interlocks (2 cycle stalls — not counted)
0 (0.000) overlapped floating point cycles
492 (0.056) interlock cycles due to basic block boundary
.
.

Opcode distribution:

spec	1700	19.33%
bnop	215	2.44%
.		
.		
lwc1	50	1.71%
sb	127	1.44%
jnop	117	1.33%
xori	112	1.27%
fcvtw	112	1.27%
mff	112	1.27%
lbu	110	1.25%
sh	102	1.16%

.
.

Figure 2. Excerpt From a PIXSTATS Output

(18634 cycles) x (40 nS) = 745.36 µS, @ 25MHz
(18634 cycles) x (30 nS) = 559.02 µS, @ 33MHz
(18634 cycles) x (25 nS) = 465.85 µS, @ 40MHz

cache2000:
Thu May 31 15:29:29 1990

17218 cycles (1.958), 0.0s @ 20.0MHz
8795 instructions (0.0M)
0 cache flushes (Infinityms)
.
.

I-cache size = 4096 words, direct-mapped, 4 word refill
D-cache size = 4096 words, direct-mapped, 4 word refill, write-through
Write buffer = 1 deep
TLB size = 56 entries, associative, random replacement, page size = 1024 words

	Per Instr	Per Cycle/Per Other
uTLB misses:	9	(0.10%/ 0.05%)
I-TLB misses:	3	(0.03%/ 0.02%)
D-TLB misses:	3	(0.03%/ 0.02%/ 0.12%)
I-cache misses:	486	(5.53%/ 2.84%)
D-cache misses:	119	(1.35%/ 0.69%/14.27%)
Idle writes:	684	(7.78%/ 3.99%/ 43.4%) (2 memory cycles)
Page mode writes:	882	(10.03%/ 5.15%/ 56.0%) (2 memory cycles)
Non-page writes:	10	(0.11%/ 0.06%/ 0.6%) (2 memory cycles)
Total writes:	1576	(17.92%/ 9.20%)
I-stream branch:	45	(0.51%/ 0.26%/ 9.3%)
I-stream d-miss:	8	(0.09%/ 0.05%/ 1.6%)
I-stream write:	241	(2.74%/ 1.41%/ 49.6%)
I-stream block:	192	(2.18%/ 1.12%/ 39.5%)
I-stream words:		0.1/1.6/2.3
uTLB miss cycles:	9	(0.00%/ 0.00%) (penalty 1)
I-TLB miss cycles:	39	(0.00%/ 0.00%) (penalty 13)
D-TLB miss cycles:	39	(0.00%/ 0.00%) (penalty 13)
I-cache miss cycles:	2916	(33.16%/ 17.02%) (penalty 6)
I-cache streaming:	-771	(-8.77%/ -4.50%)
D-cache miss cycles:	714	(8.12%/ 4.17%) (penalty 6)
2-cycle SB/SH/SWL/ SWR:	229	(2.60%/ 1.34%) (penalty 1)
Write buffer full cycles:	3469	(39.44%/ 20.25%) (average 2.2 per write)
Write wait cycles:	1779	(20.23%/ 10.38%) (average 2.9 per miss)

.
.

Figure 3. Excerpt From A *cache2000* Output

C

Cache2000 must be used to generate the performance statistics of a 'cached' system. Main memory access penalties, uTLB/TLB miss penalties, and two-cycle store penalties are simulated. However, *cache2000* does not simulate 79R3000/1 and 79R3010 interlock cycles. Thus, *the total number of run-time cycles for a 'cached' system is equal to the number of run-time cycles calculated by cache2000 plus the total number of interlock cycles calculated by pixstats.* For the *cache2000* example in Figure 3, the total number of run time cycles for the target cached system is 18634 (ie. 17218 cycles from *cache2000* + 1416 interlock cycles from the corresponding *pixstats* output in Figure 2). *Cache2000* assumes that the cache is initially void of the benchmark. Initial cache misses are incurred as code gets loaded into the cache for the first time. All run times projected by *cache2000* include these initial cache misses. Note that the number of instructions executed is the same for both the *cache2000* output and the corresponding *pixstats* output. These instructions include the jump/branch and load delay slot nops not replaced with useful instructions by the optimizing compiler.

The statistics generated by pixstats and cache2000 can be used to scale target system performance by using a faster (or slower) 79R3000/1 matched with the corresponding speed grades of synchronous and asynchronous memory. For instance, the run times for the example application detailed in Figures 2 & 3 with 25, 33, and 40MHz clocks are:

Size Of Executable

The size of the executable is useful in determining the appropriate amount of target system cache. The executable size also dictates the minimum amount of synchronous memory required for a 'synchronous' target system. The RISC/os UNIX utility size prints the size of the instruction and data sections of the executable.

Size of example:**18736**

Section	Size	Physical Address	Virtual Address
.text	**11360**	4194672	4194672
.init	32	4206032	4206032
.data	16	268435456	268435456
.lit8	144	268435472	268435472
.sdata	2032	268435616	268435616
.sbss	432	268437648	268437648
.bss	4720	268438080	268438080

Figure 4. Output From Unix *size* Utility

The static instruction size of the example executable in Figure 4 is 11360 bytes. The static data size of the example executable is 7376 bytes (ie. 18736 total - 11360 code). Each MIPS RISComputer generated executable has entry/exit code inserted at compile time by RISC/os to transfer control to and from the benchmark.

Dummy routines have been written and compiled to determine the the entry/exit code size for all languages supported by MIPS. These dummy routines are detailed in Figure 5. The corresponding static code sizes are summarized in Table I. The entry/exit code size must be subtracted from the application size to determine the stand-alone application size. For the C application in Figure 4, the stand-alone application code size consists of 7280 bytes of instruction(11360 - 4080) and 2256 bytes of data(7376 - 5120).

Language	I size (bytes)	D size(bytes)	'synchronous' Performance
C	4080	5120	
ADA	30064	23552	
FORTRAN			
PASCAL			
COBOL			
PL/1			
assembly			

NOTE: compiler optimization level 4 used

Table 1. Entry/Exit Code

There is additional overhead when running the entry/exit code. Table 1 summarizes the additional cycles incurred for a 'synchronous' system, as measured by *pixstats*. Unknown, however, is the exact performance degradation for 'cached' systems. Since some of the cache is consumed by the entry/exit code and data, the number of additional cache misses and other penalties associated with the resultant increase in main memory traffic is not known.

Floating-Point Alternatives

The 79R3010 is optional in 79R3000/1 system design and is used in applications that have floating-point requirements. Floating-point emulation handled in software by the 79R3000/1 integer unit offers a less expensive and space saving alternative to the 79R3010. The performance of available emulation routines is often adequate for limited floating-point applications.

MIPS' compilers always assume the presence of the 79R3010 and thus generate 79R3010 instructions. If the Cu1 (79R3010 usability) bit in the 79R3000/1 status register is not set, then a Coprocessor Unusable Exception occurs when a 79R3010 instruction is decoded. The 79R3000/1 jumps to the general exception vector where the exception type is then decoded. Execution then jumps to the floating-point emulation service routine. The service routine initiates the corresponding 79R3010 instruction emulation routine started. To measure the performance of such systems, you must omit the number of 79R3010 interlock cycles calculated by *pixstats* from the total cycle count. The 79R3010 dynamic opcode distribution listed in the *pixstats* output is used to calculate the emulation overhead. The following are the run

cycle counts for the 79R3010 emulation package available from IDT:

	Single Precision	Double Precision
ADD	40 cycles	66 cycles
SUB	52 cycles	90 cycles
MUL	50 cycles	97 cycles
DIV	160 cycles	236 cycles

NOTE: assuming emulation routines present in cache

Higher floating-point emulation can be achieved by using IDT's PostFloat filter to eliminate exception handling overhead. A source program is first compiled at the assembly level. The PostFloat filter is then used to strip away 79R3010 instructions, replacing them with direct calls to the emulation routines. Even higher performance floating-point emulation is achieved with IDT's cross compilers. IDT's multi-hosted compilers inline floating-point emulation routines which then benefit from global optimizations. Details of the IDT PostFloat filter and the IDT7RS903 Multi-Host C-compiler System are available from IDT. Note that these alternatives eliminate floating-point machine code in the executable. There are no 79R3010 pipeline interlock cycles to subtract out from the statistics generated by *pixstats*.

PERFORMANCE ANALYSIS STEPS

Creating The EXECUTable

At compilation, the MIPS compiler system allows you to choose from various options that affect the nature and efficiency of the executable. These compiler options can be turned on or off as appropriate. You can refer to the "IDT R3000 FAMILY LANGUAGE PROGRAMMERS GUIDE" for a complete description of the MIPS compiler system. A few of the compiler system options, as related to performance analysis, are discussed here.

Compiler Optimization Levels:

There are several levels of optimization for the MIPS compilers:

Level	Optimizations
0	none
1	default pipeline scheduling, local optimizations
2	adds global optimizations, register allocation
3	adds inter-procedural register allocation
4	adds procedure merging

Although optimization level O4 typically generates the most efficient code, the target-system performance may not be optimum. Procedure merging (ie. inlining) is an optimization technique intended to increase performance by eliminating jump/branch instructions. However, inlining of

C dummy routine

```
main()
{
}
```

Ada dummy routine

```
procedure TEST is
begin
null;
end TEST;
```

Fortran dummy routine

Pascal dummy routine

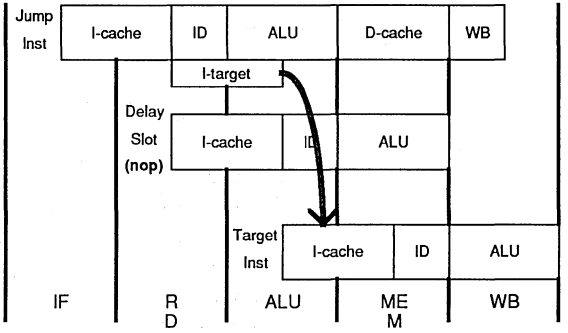
Cobol dummy routine

PL/1 dummy routine

MIPS assembly dummy routine

Figure 5. Dummy Routines

without the -jmpopt compiler option



with the -jmpopt compiler option

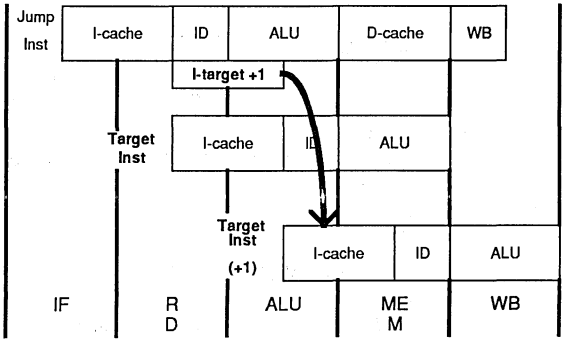


Figure 6. The -jmpopt Lnker Option

C

subroutines also tends to increase the static code size which can have an adverse effect on cache hit-rate. It is advisable to experiment with all compiler optimization levels to determine which results in the highest target performance.

Filling Unconditional Jump Delay Slots:

79R3000/1 jump instructions have a delay of one cycle while they calculate the target address where execution is resumed (refer to Figure 6). The instruction that immediately follows in the pipeline is called the 'delay slot' instruction which the 79R3000/1 always

executes. The compiler is responsible for re-scheduling the pipeline by filling the delay slot with an instruction that is independent of the jump. In this manner the pipeline continues to flow and performance is not degraded. If the compiler can not find a useful instruction, a nop is inserted that results in a 1 cycle performance penalty.

The *-jmpopt* linker option fills any jump delay-slot with the target of the jump and increments the target address to the next instruction. Unlike the compiler, the linker has unlimited scope and can refill the delay slot regardless of where target instruction is.located.

Reducing Cache Conflicts:

Every main memory location maps to exactly one 79R3000/1 cache location. Different sections of code located a multiple of the cache size away from one another compete for the same cache space. The 793000/1 first checks cache for a needed piece of code. If not there, the code is then loaded into cache from main memory - overwriting code previously resident in the corresponding cache locations. Such cache conflicts significantly degrade performance if newly loaded code replaces other code that will be needed right away. A classic example of this activity (known as to 'thrash in cache') is a loop in which a subroutine is called that is located in a multiple of the cache size .

Major cache conflicts can be avoided by using the -cord compiler option that uses statistics generated by the program profiling tools *pixie* and *prof* (refer to Figure 7). The first version of the executable is generated by invoking the corresponding driver with the desired compiler options. *Pixie* is then used to partition the executable into basic blocks. Each basic block has exactly one entry point (ie. target address of a jump/branch instruction) and exactly one exit point (ie. the address of the first jump/branch instruction encountered).

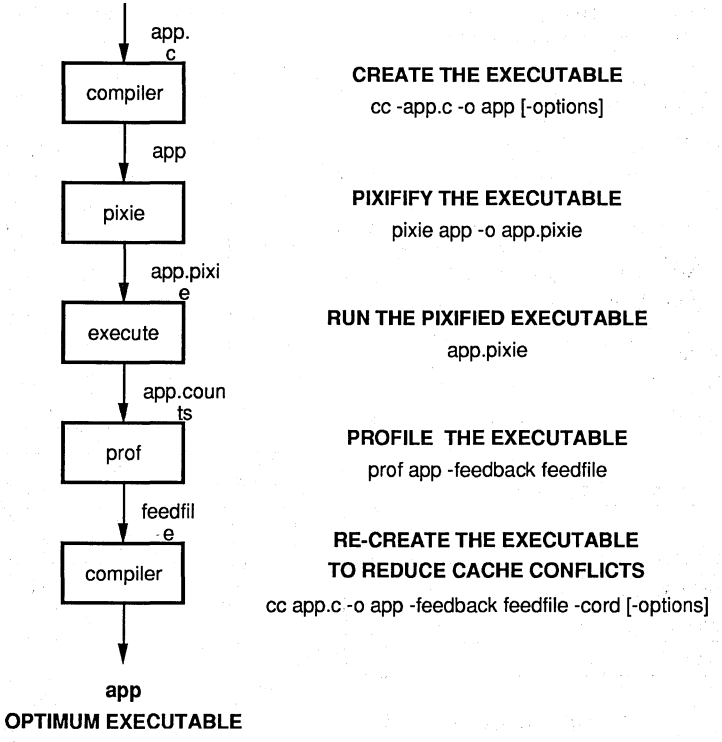


Figure 7: Reducing Cache Conflicts

Additional counting code is inserted by *pixie* at the end of each basic block. The pixified executable generates a file containing the basic block counts (.counts extension). This raw data is used by *prof* to generate profile data for the different procedures within the application. This profile data is stored in a feedback file in a format usable by the compiler. The application is then re-compiled with the *-cord* option. The *-cord* option places the most frequently used loops in main memory locations that do not conflict with one another for the same cache location.

Single or Double-Precision Floating-point:

A significant performance gain can be realized by both the 79R3010 and the floating-point emulation software by doing single-precision arithmetic, vs double-precision. Single-precision often provides adequate dynamic range for an application's floating-point requirements. To ensure that all floating-point operations are done in single-precision, the compiler option *-float* should be used. Even if all floating-point variables are declared as single-precision in the source, the *-float* compiler option is necessary to ensure that intermediate operations are done in single-precision.

Other Concerns:

The most efficient code is not appropriate for all applications/benchmarks. Compiler optimizations can alter the intended nature of a benchmark. This is the case for real-time code in which the precise timing of operations is more important than the execution speed. Loop optimizations that move loop invariant code outside loops so that it is only executed once is one compiler optimization technique that can create havoc with real-time code. The real-time portion of an application should be written in MIPS assembly language and assembled with the *-noreorder* option to prevent pipeline scheduling from altering the execution sequence of instructions . The resultant object code can then be linked with the object code of other compiled modules.

Interprocedural register allocation and procedure merging may not be desired if subroutine calls in a benchmark are intended to simulate interrupts. Also, field serviceability requirements may dictate the use of lower optimization levels. Although compiler optimizations do not alter the flow of control within a program, the sequence of object code may be altered thereby making source-level debug difficult or impossible. It is often useful to look at the dis-assembly of the compiled code to decide on the appropriate optimization level. The RISC/os utility *dis* generates the dis-assembly with source listings interspersed.

Using *pixstats*

(refer to Figure 8)

Pixie is used to partition the executable into basic blocks. Each basic block has only one entry point (ie. target address of a jump/branch instruction) and only one exit point (ie. the address of the first jump/branch instruction encountered). Additional counting code is inserted by *pixie* at the end of each basic block. Also generated is a file containing the basic

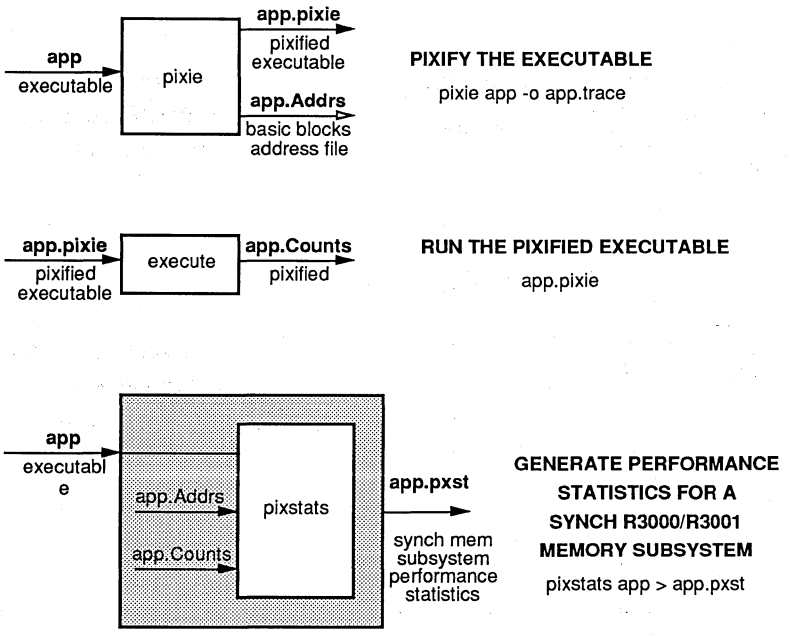


Figure 8. Using *pixstats*

block addresses (.Addrs file). The pixified executable generates a file containing the basic block counts (.counts extension). *Pixstats* uses the .Addrs and .Counts files to generate detailed statistics on pipeline interlocks, opcode frequency, and mini-profile data.

Using *cache2000* (refer to Figure 9)

The size of the executable is useful in determining the appropriate sizes of instruction and data cache to simulate. Pixifying the executable with the *-idtrace* option enables tracing of instruction and data memory references for use by *cache2000*. To model the target system, *cache2000.c* can be modified as shown in Figure 10. Any optimization level may

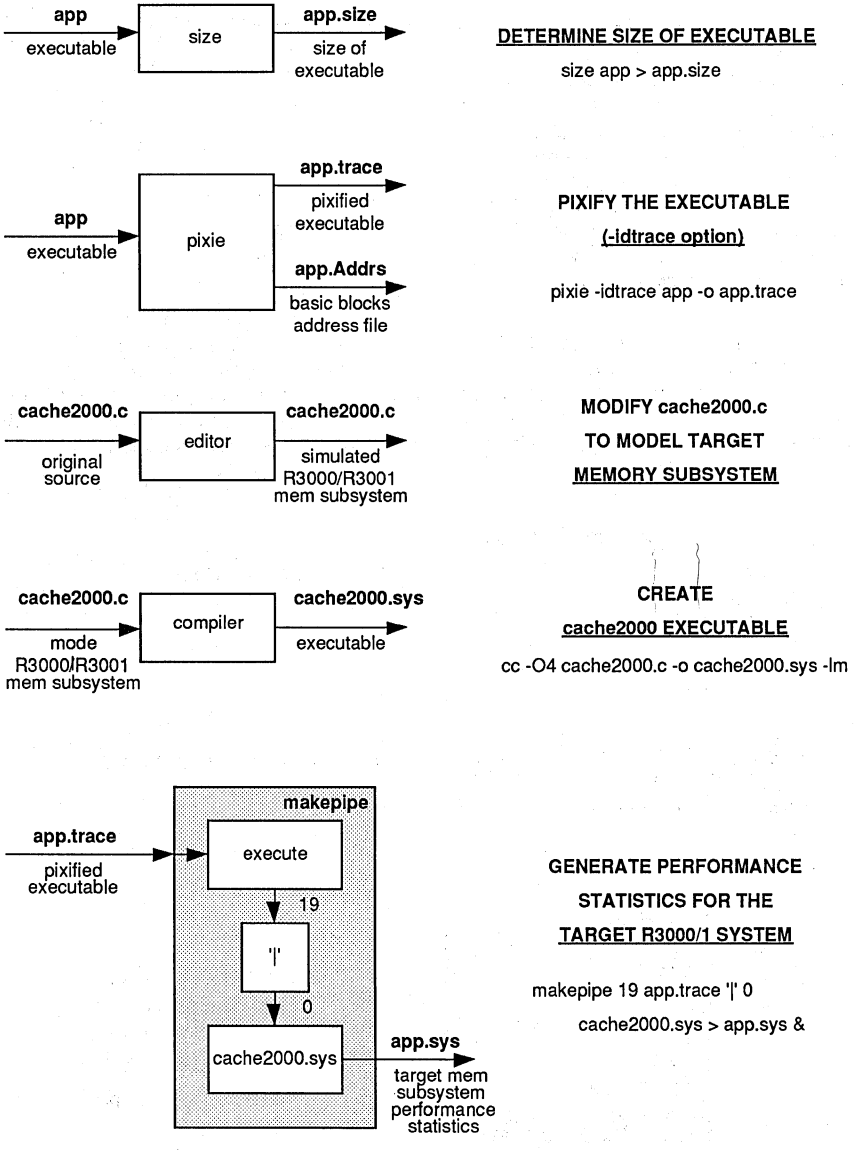


Figure 9: Using *cache2000*

be used to generate the *cache2000* executable. If many simulations are planned, it is advisable to experiment with all of the optimization levels to determine the best tradeoff between *cache2000* compilation and run times. *Trace.h* is an include file that must be resident in the same working directory as *cache2000.c* at the time of compilation. The RISC/os utility *makepipe* is used to run the pixified executable and output the results into the cache2000 standard input file descriptor 19. Cache2000 generates the performance statistics for the 'cached' target system

A TLB miss penalty of 13 cycles is assumed for a random page replacement algorithm. The TLB size is defined as 56 since the lower 8 TLB entries are not accessible by the random register. A non-random replacement algorithm can be simulated by defining the TLB size to be 64. The TLB miss penalty can be changed to the appropriate value.

Embedded applications often do not implement a demand paged virtual memory. Typically, these applications bypass the TLB by running out of virtual address segments KSEG0 and/or KSEG1. This can be simulated with cache2000 by setting the uTLB and TLB miss penalties to 0. The ability to bypass the TLB is important for real-time applications that can not tolerate the non-determinism caused by cache misses.

* A detailed description of setting up the main memory read and write latencies for simulation will be given here. A few examples are shown.

```
.
.
/* cache parameters */

/* instruction refill size, in words */
#ifndef i_refill_log
#       define i_refill_log 2
#endif
#define i_refill_size (1<<i_refill_log)

/* instruction cache size, in words */
#ifndef i_size_log
#       define i_size_log 12
#endif
#define i_size (1<<i_size_log)

/* data refill size, in words */
#ifndef d_refill_log
#       define d_refill_log 2
#endif
#define d_refill_size (1<<d_refill_log)

/* data cache size, in words */
#ifndef d_size_log
#       define d_size_log 12
#endif
#define d_size (1<<d_size_log)

/* TLB */
#ifndef tlbsize
#       define tlbsize 56
#endif

/* byte gathering */
#ifndef byte_gathering
#       define byte_gathering 0
#endif

/* read conflict checking in write buffer */
#ifndef read_conflict_check
#       define read_conflict_check 0
#endif

/* instruction streaming */
#ifndef istreaming
#       define istreaming 1
#endif

/* memory parameters */
private unsigned wbsize =1;
private unsigned read_latency =2;
private unsigned idle_write_time = 2;
private unsigned page_write_time = 2;
private unsigned nonpage_write_time = 2;
private unsigned byte_extra_write_time 0;

#define imiss_penalty (read_latency +
i_refill_size)
#define dmiss_penalty (read_latency +
d_refill_size)

/* random parameters */
#ifndef utlbmiss_penalty
#       define utlbmiss_penalty 0
#endif
#ifndef tlbmiss_penalty
#       define tlbmiss_penalty 0
#endif
#ifndef page_log
#       define page_log 10
#endif
private char *comment = NULL;
private boolean random_flush = false;
private unsigned print_interval =
2000000000000000;
private unsigned flush_interval =
2000000000000000
private double random_flush_parameter;
private double cycletime =50e-9;
.
.
```

Figure 10. *Cache2000.c* Modifiable Parameters

Integrated Device Technology, Inc.

DMA TECHNIQUES WITH IDT'S R3000/R3001 RISC CPU

APPLICATION NOTE AN-88

By Brent Bush

INTRODUCTION

There are many cost sensitive applications today that require high bandwidth data-transfer as well as high compute power. With its efficient pipeline architecture and tightly-coupled flexible memory-controller, the R3000/3001 CPU's from IDT prove to be an extremely effective solution. This application note reveals various DMA (direct memory access) techniques utilized in high bandwidth R3K designs. A general review of the R3K CPU architecture and performance is given and is followed by a detailed description of the R3K system memory-hierarchy and its flexibility. Also, a detailed description of various tightly-coupled DMA approaches is presented.

The MIPS compilers & the R3000 CPU architecture are based on over 35 staff years of research & development; its foundation established with compiler optimizing research at Standford University in the early 1980's. Benchmark comparisons of competitive solutions conducted by IDT customers have shown that the MIPS solution is clearly the best price/performance solution in most applications. As a MIPS semiconductor partner, IDT has produced the R3000 since 1988.and the enhanced version R3000A since 1990.. IDT's agreement with MIPS includes the right to design and sell derivatives of the R3000 architecture. The R3001 RISController™ is IDT's first derivative. Improvements were made to reduce chip-count and increase design flexibility. Bus control and timing is identical to the R3000. The same R3000 (R3K) CPU core is used in all IDT derivative CPU's, guaranteeing binary compatibility and reducing your time-to-market.

ARCHITECTURE OVERVIEW

Both The R3000 and R3001 are available at 16MHz to 40MHz in a 175-pin PGA package. There are also plastic & ceramic surface mount packages available. All common instructions execute in 1 cycle, regardless of instruction sequence. Two exceptions are Loads & Branches. All pipeline CPU architectures potentially incur latency on these instructions. The R3K has a "potential" one-cycle latency. This latency is minimized by always executing, rather than stalling during the cycle following the Load or Branch (the "delay" slot). The compiler's instruction rescheduler is highly successful in filling this delay slot with another instruction, bringing Load's and Branch's close to one cycle.

A dedicated autonomous unit inside the R3K performs multi-cycle integer multiply and divide operations. This unit has dedicated result registers and executes in parallel with other non-multiply/divide instructions. A hardware interlock occurs if the result registers are required prior to completion of the multiply or divide.

Figure 1 shows the functions found in the R3K core. There are two tightly coupled processing units. The first is a full 32-bit integer that executes the MIPS RISC (Reduced Instruction Set Computer) instruction set at 1 cycle per instruction. Integer multiply and divides are included and are multi-cycle operations that execute in an autonomous unit, allowing other instructions to execute in parallel. There are dedicated adders for instruction and data address calculations, eliminating any possible pipeline stalls due to certain instruction sequences. The second processor, Coprocessor 0 (CP0) contains a 64-entry fully associative Translation Lookaside Buffer (TLB) with control registers to support a virtual memory system with dual (instruction & data) caches at full bandwidth. The TLB is part of the Memory Management Unit (MMU). The MMU provides adequate address mapping when the use of the TLB functions is undesirable. Figure 2 shows the Kernel & User as well as cacheable & uncacheable (I/O) memory segments provided. Mapped segments require use of the TLB. Kernel segments 0 & 1 (Kseg0/Kseg1) provide .5 Gbytes of cacheable and uncacheable memory (each) that is "hardwired" to the lower .5 Gbyte of the 4 GB physical address space. All status and exception registers associated with maintaining User and Kernel state and precise exception handling are in CP0.

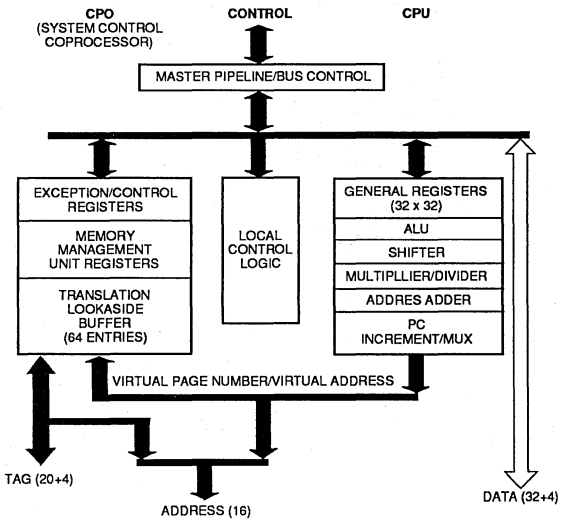


Figure 1. R3000/R3001 Functional Block Diagram

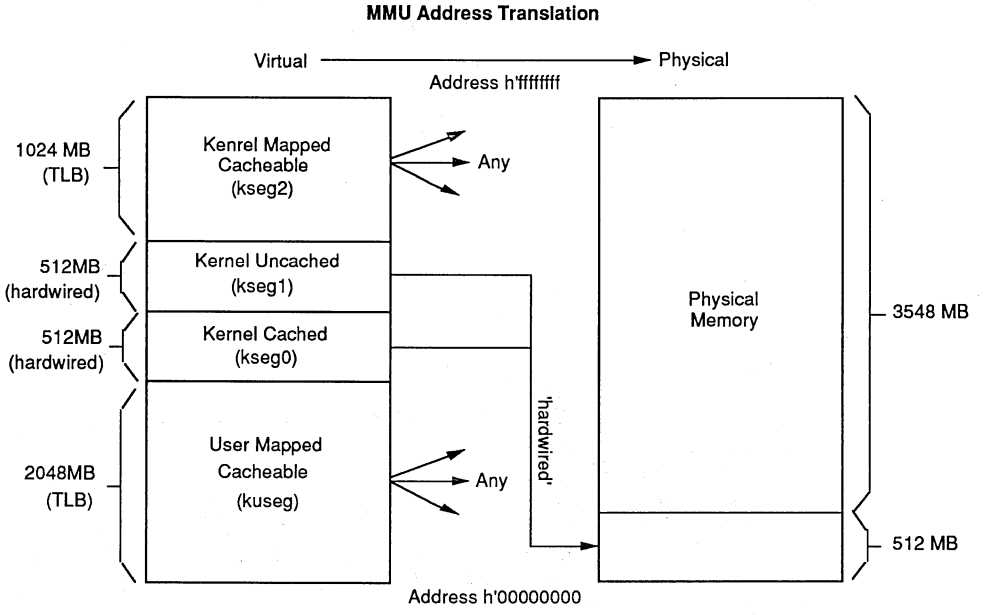


Figure 2. R3000/3001 Memory Mapping

COMPANION CHIPS

IDT provides many companion chips for R3K designs. The R3010 is an optional 84-pin floating point accelerator. The interface to this unit is "seamless". The FPA has it's own register set & can perform Load and Store operations . Therefore floating-point operands, opcodes, and results do not have to be passed to/from the CPU. A high degree of parallelism exists in this 2-chip solution. Integer instructions & multiple floating point instructions can execute simultaneously. The R3020 is a 4-deep write buffer used to decouple the high bandwidth CPU from the slower system bus. This is an effective performance enhancer in data intensive applications. IDT has 7 and 8-deep buffers (IDT73200/201) that provide deep, efficient read and write buffers. IDT's product portfolio includes high-speed logic devices, FIFO's(first in-first out memories), dual-port static RAMs, and generic static RAMs at the speeds required for the highest performance R3K design.

THE R3000 MEMORY HIERARCHY (SYNCHRONOUS VERSUS ASYNCHRONOUS)

Figure 3 shows a typical R3000/R3001 system. The CPU's Synchronous Bus consists of a 24-bit address bus (18-bit for R3000) and a 32-bit data bus coupled to two banks of generic static RAMs, one for Instructions and one for Data. It is important to realize that the SRAMS provide single cycle access (address and data) and can be used as a "Cache" or as a "Local" memory. This bus is decoupled from the slower (multi-cycle) System Bus resources with a registered interface.

A Cache is nothing more than a mirror image of some larger, slower memory, used to hold the most recently acquired data. Properly sized caches will contain ≥ 95% of the instruction and data accesses required. When the required instruction or data is not in the Cache the CPU invokes a multi-cycle access to the slower, larger "main" memory residing on the System Bus. Caches are a cost effective way to greatly increase performance.

When used as a local memory all accesses to the synchronous (cacheable) address space result in accessing the SRAM's on the Synchronous Bus. There is no slower, larger memory that maintains the same data.

It is important to define some terminology at this point:

"Synchronous"	Used when referring to the CPU's tightly coupled, single cycle access bus, independent of SRAM usage; "Cache" or "Local" (Abbreviated "sync.")
"Asynchronous"	Used when referring to the multi-cycle access System Bus. (Abbreviated '-79R3010AE-33G.")
Local Memory	Used when the Synchronous SRAM's are used as a local memory; not as a Cache in a Cache hierarchy.
Cache	Used when the Synchronous SRAM's are used as a Cache in a Cache hierarchy system **or** when referring to the CPU's internal control features for the synchronous bus. (To conform to other documentation.)

C

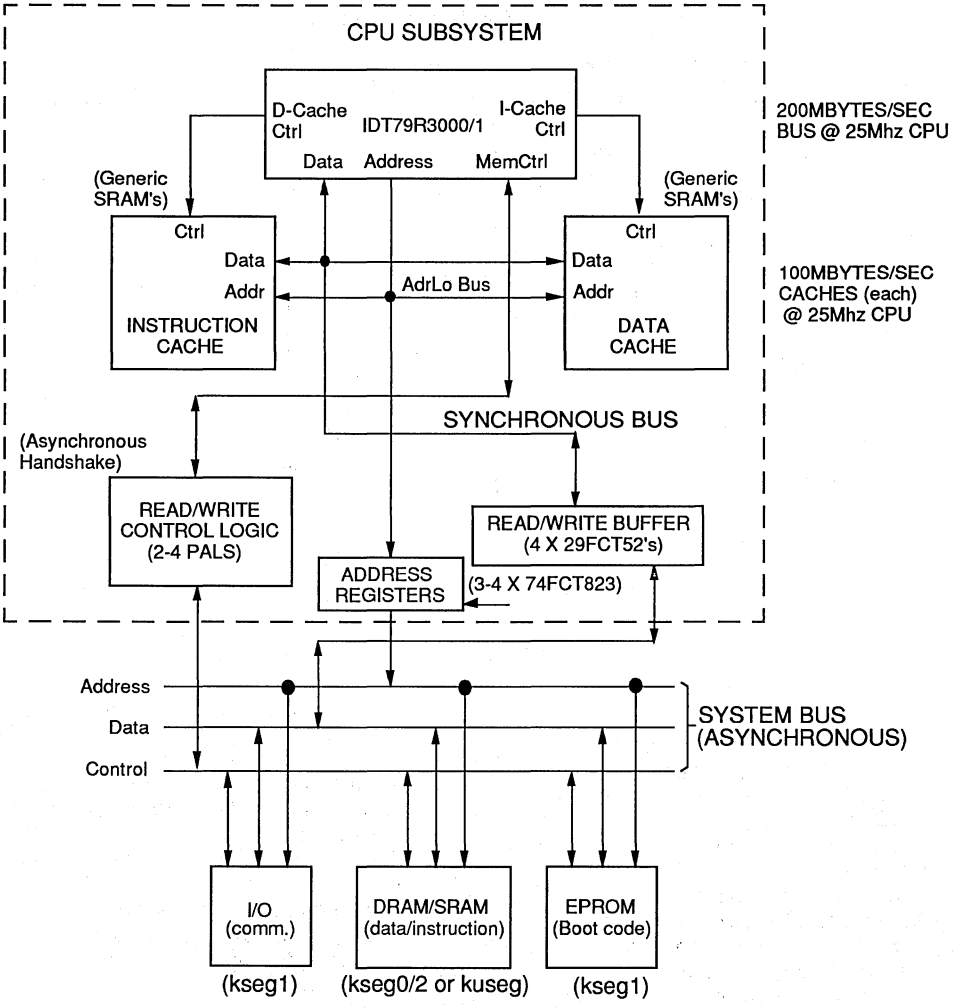


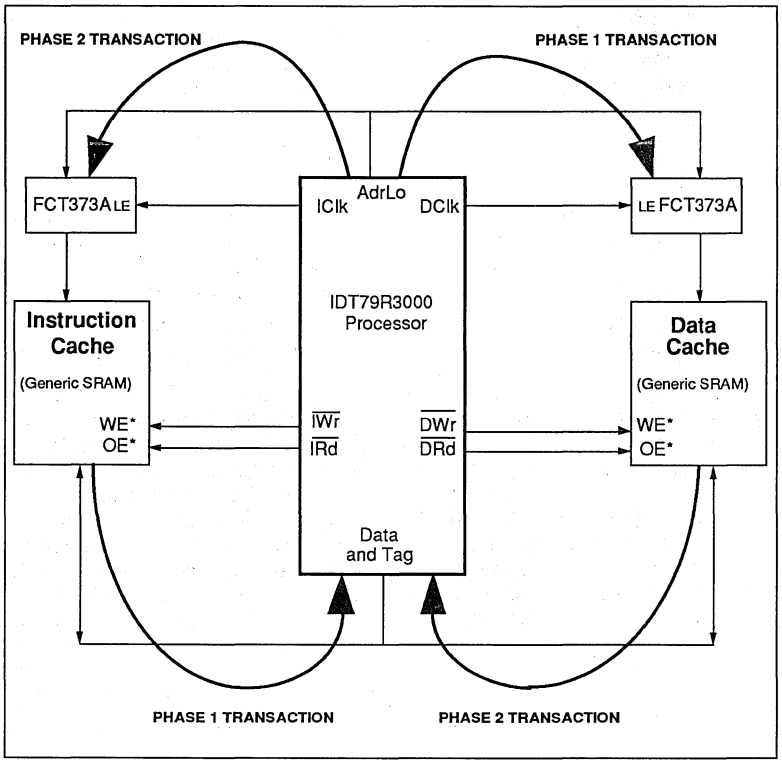
Figure 3. R3000/R3001 System Hierarchy

* Please note that most R3000 documentation uses "Cache" terminology exclusively when referring to the synchronous address space.

A key element integrated into the CPU is the Cache controller. It provides all control lines required to interface to generic static RAMs for instruction fetching and data Loads and Stores on the sync bus. No additional logic is required. Despite the single address and data busses there is no bus conflict between instruction fetching and data loads or stores. The controller "time multiplexes" the address and data busses, providing a true Harvard Architecture in a small package. Figure 4 shows the bus usage for each half-cycle phase. The address and data are acquired during the same cycle. At 25MHz a full 200Mbytes/second is realized regardless of instruction sequence.

During a synchronous read cycle the Cache controller determines if the required data (or instruction) is in the SRAM. If required, on the following cycle, a simple read/read busy handshake is invoked by the controller to perform a multi-cycle (asynchronous) access on the System Bus. The CPU pipeline is "stalled" until data from the asynchronous space is available.

Synchronous Store instructions are always single-cycle events. Fullword (32-bit) Stores always update the sync memory regardless of the hit/miss status of that location. Partial word (byte/halfword) Stores are 2-cycle read/write events. The sync memory is read to determine if the address is in the Cache. If a "hit" occurs the new byte/halfword is merged with the old cached data and then written into the sync memory. When a Store updates the synchronous data memory



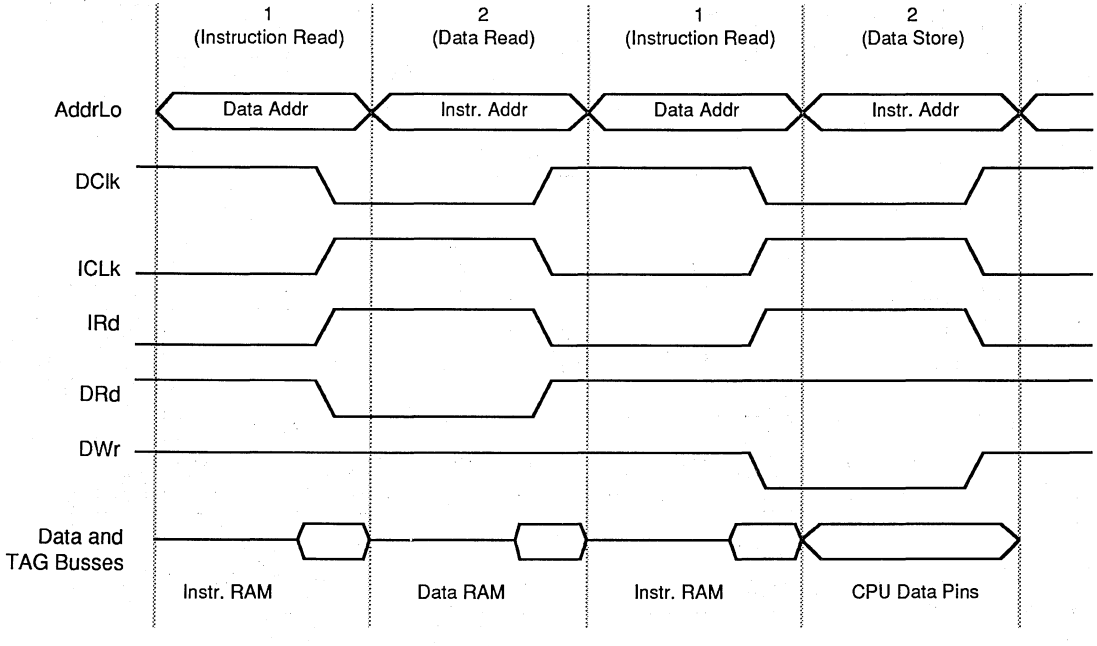


Figure 4. Harvard Architecture of the R3000/R3001 Synchronous Bus

a write request is always "posted" to the System Bus. The data, 32-bit address, and access type controls (i.e. byte, halfword, fullword) are supplied for one cycle and must be held in registers to accommodate the multi-cycle store operation on the System Bus. The CPU continues to execute until the System Bus is required for another access. If the previous Store is not completed, then the CPU will stall until the write buffer can accept the request.

In local memory applications these write requests to the sync space are ignored by the asynchronous handshake logic to avoid undesired bus stalls. Unlike Cache designs there is no larger memory to update in parallel.

THE SYNCHRONOUS MEMORY – CACHE OR LOCAL MEMORY?

A "tag check" is done on all synchronous accesses. (The internal Cache controller has no way to determine that a local memory has been implemented.) "Tag" bits are required (in a Cache hierarchy) to determine whether the requested data resides in the Cache. They are an extension to the SRAM banks. The number of required Tag bits depends on the size of the cacheable memory residing on the System Bus. A "Valid" bit is required to indicate that the addressed location in Cache contains a valid entry. Figure 5 is an R3001 example with 32KB caches supporting a 64MB cacheable main memory.

The main memory to Cache size ratio is 2000:1. Therefore, 11 SRAM Tag bits are required. All unneeded Tag bits are disabled (masked from the address comparison) at Reset with the R3001. A 4K ohm pulldown resistor is required for each disabled Tag. The R3000 does not have this feature so simple buffers are used to supply the addresses required. The buffer's input value is determined by the system memory mapping.

When a local memory is implemented with the R3001, no Tag bits are required since all accesses in the synchronous area are always valid. Therefore all Tag bits and the Valid Bit are disabled (as described above). This eliminates the 4 SRAM's in Figure 5 supporting Tag25:15 and Valid.

INCREASED DMA BANDWIDTH USING THE CACHE BLOCK REFILL MECHANISM

Since the synchronous SRAM is accessed in one cycle it can be viewed as an extension to the CPU's register stack. Once data resides here there is no access latency and routines operating on this data will run very close to 1 cycle per instruction. The R3K, with its internal Cache controller has efficient means to bring data into the synchronous SRAM. It provides support for block refilling of the synchronous SRAM's. Setting the data block size to a large value can greatly improve data throughput. The block size for Instruction and Data is independently configured at Reset, providing 4, 8 16, or 32 word refills per Load instruction.

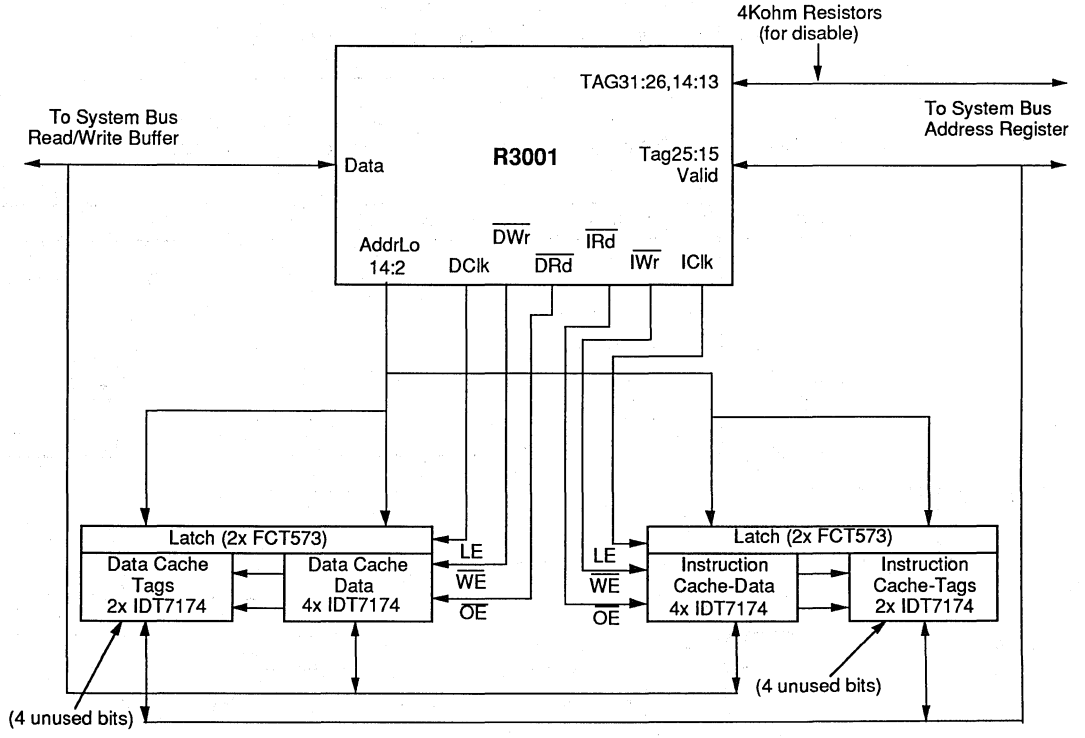


Figure 5. R3001 Cache Design Example

Figure 6 illustrates the timing associated with a 4-word block refill. All signals shown, except RdBusy and CpCond0, are supplied by the CPU. Refilling occurs when an attempt to access data in the synchronous address space results in a "miss". ("D#" means Tag bits did not match or Valid Bit is not set). This decision takes place during the synchronous access cycle (Run). During the first Stall cycle the controller invokes a read protocol (MemRd) to the asynchronous space. The CPU requires that the data be available one word per cycle once the refill starts. This is accommodated by various means; fast memory, dual-banked memory, read pipeline registers, FIFO's, etc. When the data can be delivered at a one word per cycle rate the System Bus state machine releases RdBusy ("read busy") and the internal controller writes the data into the sync memory. (Called "Refill" cycles). The "Fixup" cycle is a repeat of the failed Run cycle and is required to resume the pipeline execution. The address increment required for the sync SRAM is supplied by the CPU. Address increment, if required by the System Bus resource, must be supplied by its state machine.

The block refill can be disabled to accommodate 1 word refills by de-asserting the input CpCond0 during the last RdBusy (read busy) cycle. This is a key attribute when other cacheable resources are accessed in a non-sequential manner.

The block refill mechanism can be utilized in a local memory design as well as a Cache hierarchy. In a local memory design the Valid Bit (and all Tag Bits) are disabled. To facilitate a block refill the Valid Bit is not disabled but is sourced by an I/O mapped register or high order address to force a Cache miss. (More on this later.)

The realized bandwidth when utilizing the block refill mechanism can be easily computed. To follow is an example of generic code used for moving a large block of data and the associated bandwidth with different block refill sizes.

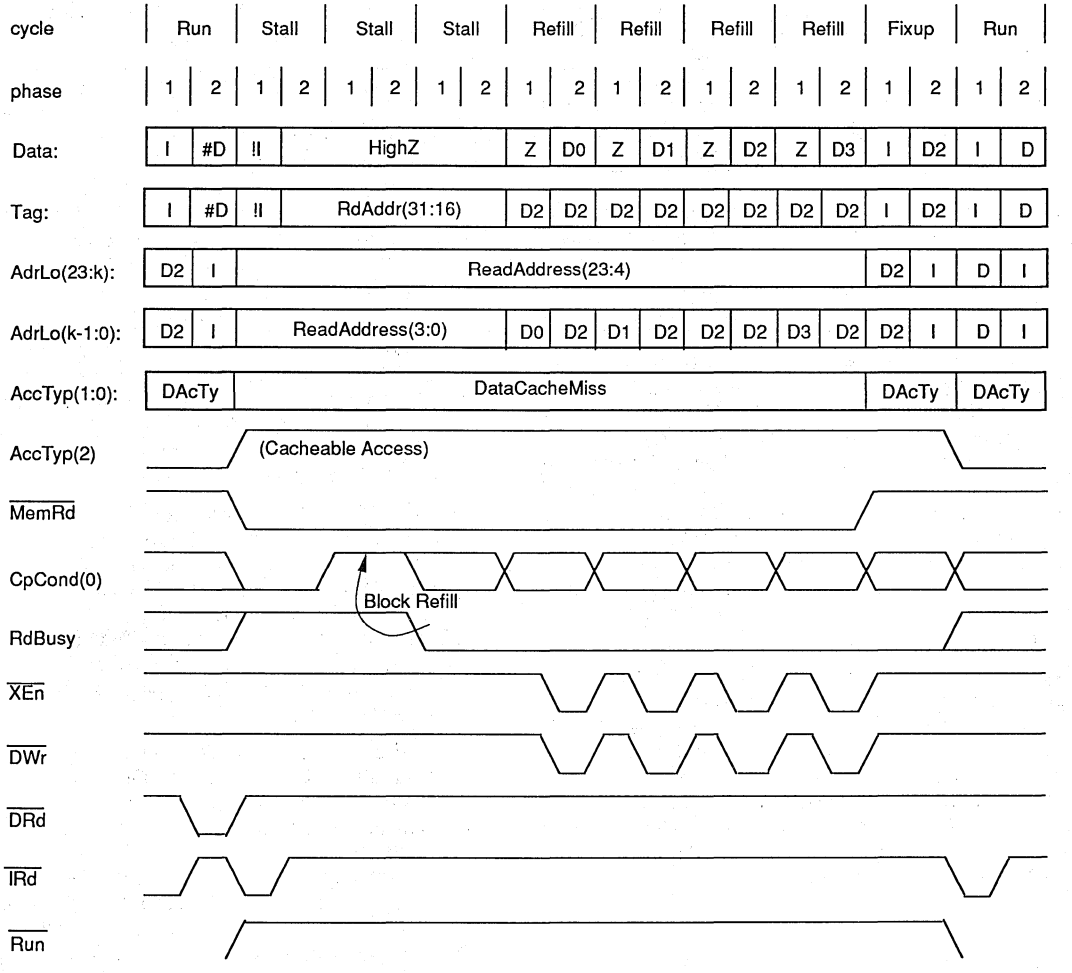


Figure 6. Data Block Refill Timing Sequence (Block of Four Words)

```
DMAloop: Load    ; for synch. memory block refill
                 ; (destination = null)
         Add     ; increment base register by block size.
         Branch  ; to DMAloop if base register not equal to
                 ; maximum value.
```

This simple loop contributes just 2 cycles of latency per block refill. Due to the Branch's delay slot, the Add & Branch must be reversed to avoid an additional cycle. Total cycle count for the loop is:

Load = 1 (instr.) + 2 (Stalls min) + N (Refill size) + 1 (Fixup); N = number of words
Branch = 1 (instr.)
Add = 1 (instr.)

The following table shows the maximum bandwidth achieved in a 25MHz system.

Block Refill Size	Cycle Count	Bandwidth	(% of max.)
4(words)	10(cycles)	40.0 (Mbytes/sec)	40 (%)
8	14	57.1 "	57 "
16	22	72.7 "	73 "
32	38	84.2 "	84 "

The latency incurred will vary based on the code loop required and the speed of the asynchronous resource supplying the data. As seen in the figures above, this latency is greatly minimized by using the larger block refill size.

DMA OBSTACLES IN A CACHE HIERARCHY

Using the Cache controller's block refill capability for DMA type activity is an efficient way to increase bandwidth but does raise a key question. In order to invoke the System Bus protocol for block refilling the sync memory, a Cache "miss" must occur. *How can the required miss occur if the Cache already has a valid entry from a previous DMA transfer?* Furthermore, problems occur in cache hierarchy systems when other bus masters update the cacheable system bus memory. In both scenarios, the data residing in Cache has become "stale". The following are details of various methods to resolve these issues and a discussion of the tradeoffs of each method.

1. Explicit address mapping using two (or more) different address spaces to perform DMA transfers.
   Under program control, a subsequent DMA move can use a different address space to insure the "miss' required to bring the new data into the sync memory. (An "Odd" and "Even" DMA address range could be established.) Data block size can be ≥ Cache size. For clarification, an example flow of events follows. (A 16KByte data Cache is assumed.)
   - Execute "Odd" DMA block transfer: Starting address = b.....x1xx,xxxx,xxxx,xx00
   - Non-DMA code: Data now in sync memory for algorithms, sorting, etc.
   - Execute "Even" DMA block transfer: Starting address = b.....x0xx,xxxx,xxxx,xx00
     Previous data no longer required. Cache miss is guaranteed due to different address range. (Tags don't match.) Starting address is "modulo" Cache size!

   Careful control of address mapping can maximize the usage of the sync memory. It could be partitioned into multiple DMA blocks plus a general usage area. No hardware or software overhead is required to resolve the "stale data" problem.

2. Explicit software Cache invalidation – The R3K caches need to be flushed (Valid Bit set to 0) at Power-up. This is done with a simple software routine. Internal status bits provide means to isolate sync SRAM accesses from the System space. Executing Store Byte instructions at this time sets the Valid Bit to 0 (invalid entry). Since the R3K's Cache line size is 1 word a Store Byte instruction is required for each word to be cleared. This mechanism can be used to resolve stale data problems only when the program has knowledge of the conflicting events and the associated addresses. The program has control and will clear only the required area of Cache, leaving usable data intact. No additional hardware is required to support this mechanism. (See Appendix-D in MIPS' "System Programmers Guide for details.)

3. Explicit hardware Cache invalidation – Some applications cannot accommodate the explicit address control of methods 1 & 2 or the significant software overhead associated with method 2. Described below are several hardware supported methods to control status of the Valid Bit when dealing with the "stale data" obstacles. The tradeoffs of each method is briefly discussed.

   3a. A resettable SRAM supplying the Valid Bit. An I/O mapped register can provide a Reset signal that clears the entire SRAM in 2 cycles. (The 8K x 8 SRAM – IDT7165 is an example.) The other 7 bits of the SRAM would supply Tag Bits if required. One Store instruction plus a fraction of a PAL (programmable logic device) provides a completely cleared Cache. One potential disadvantage is that good data, along with the stale is lost.

   3b. A Valid Bit "disable switch" to force a miss. An I/O mapped register is used to set the CPU's Valid Bit input to 0. When the I/O register is set, all sync Loads result in a miss and subsequent refill, regardless of the Cache status. The SRAM supplying the Valid Bit is not cleared and is updated during the refill. The update is required if the Valid Bit could be previously 0 (due to a real "miss"). This requires minimal hardware and software support, does not delete needed

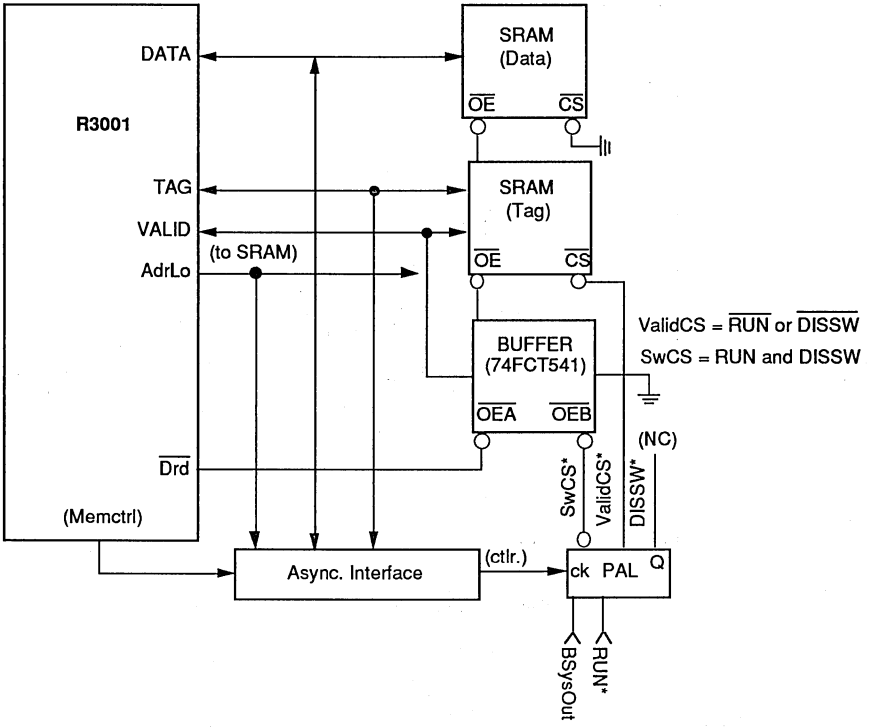


Figure 7. Valid Bit Disable Switch (Using I/0 Mapped Register)

data, and does not require the CPU's knowledge of the sync memory's content. The Valid Bit must be connected through a device that satisfies the strict turn-on/turn-off times of the sync bus; hence the use of an FCT buffer. Figure 7 shows this feature implemented with an R3001 in a Cache hierarchy and gives an example of generic code to execute the operation. (Instruction SRAM is omitted for simplicity.)

```
Generic Code:  Store    ; to I/O mapped register, disabling
                        the Valid
               NOP's    ; cycle count = cycles to retire I/O
                        Store. (Can be any non- data
                        Cache instruction!)
               Load     ; Miss forced, block refill occurs.
                        (Beginning of DMA , etc.)
               "        ; Loop for data block moved into
                        Cache.
               "
               Store    ; to I/O mapped register, restoring
                        Valid Bit to normal. (End of DMA,
                        etc.)
               NOP's    ; cycle count = cycles to retire I/O
                        Store. (Can be any non- data
                        Cache instruction!)
                        ; Resume normal code. DMA data
                        now in Cache
```

An alternate method to control this "miss switch" is to simply use a high-order address bit that is beyond the cacheable address range. This implies that for all normal sync accesses this address bit is not set. The user program, requiring the forced miss, sets this bit in the index or in the base address register used for the block-refill Loads. This requires even less hardware support and offers more code flexibility. When using the I/O mapped register method, (Figure 7), synchronous Stores cannot occur because the Valid Bit SRAM is not enabled during Run cycles. This limitation does not exist when using an address bit for the disable mechanism. Figure 8 illustrates the needed control. (Instruction SRAM is omitted for simplicity.)

In a local memory design (no Cache hierarchy) this circuit is further simplified. Normally, in an R3001 local memory design the Valid Bit (and all Tag Bits) are disabled at Reset and need not be driven. To facilitate a block refill (for DMA, etc.) the Valid Bit is not disabled but is sourced by a register to force the miss. This Valid Bit source must still be output enabled by the CPU controls "IrD" and "Drd" because it is driven during sync Stores and Load Refills by the CPU. The strict timing therefore applies. See Figure 9 for an example implementation.

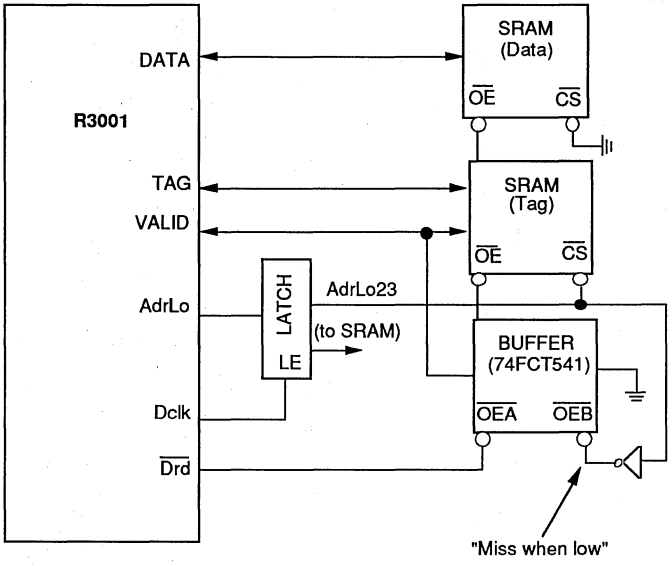


Figure 8. Valid Bit Disable Switch (Using AddrLo bit)

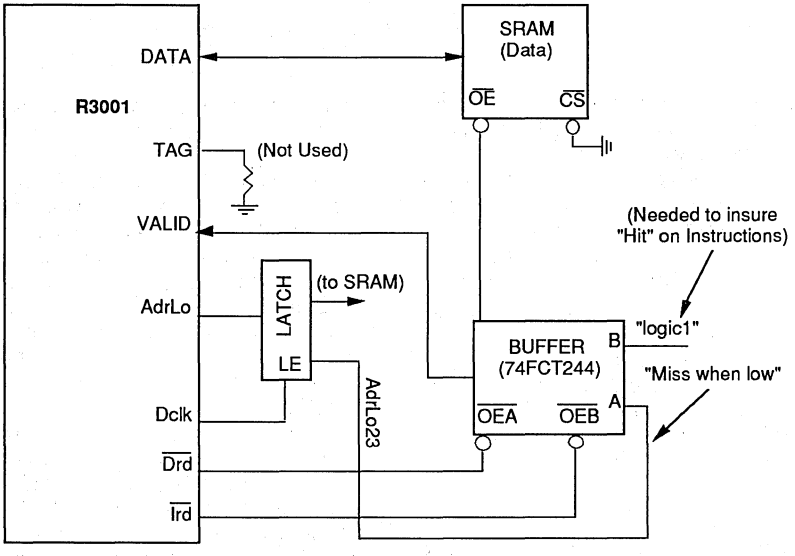


Figure 9. Valid Bit Disable Switch in a Local Memory Design

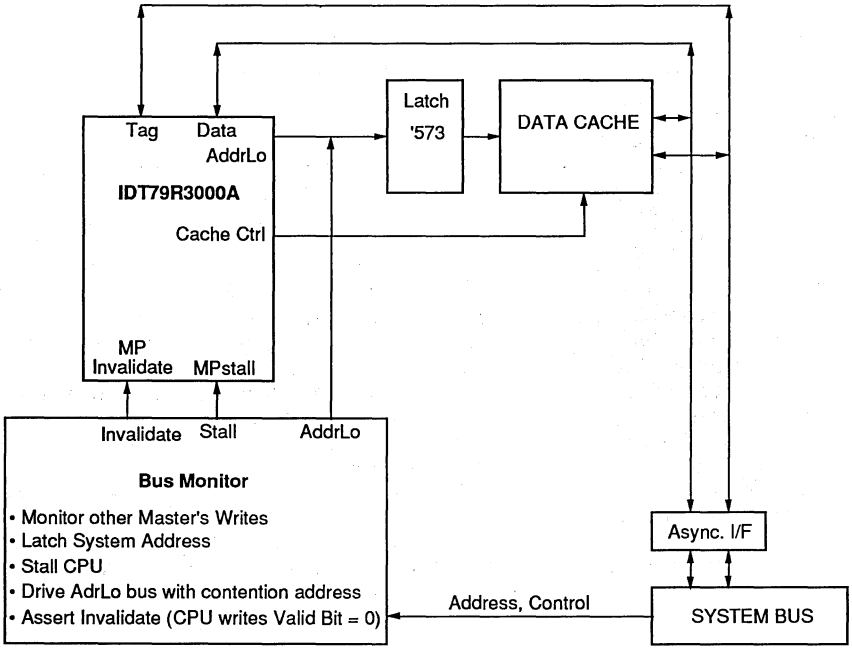


Figure 10. R3000 Multiprocessor Cache Invalidate

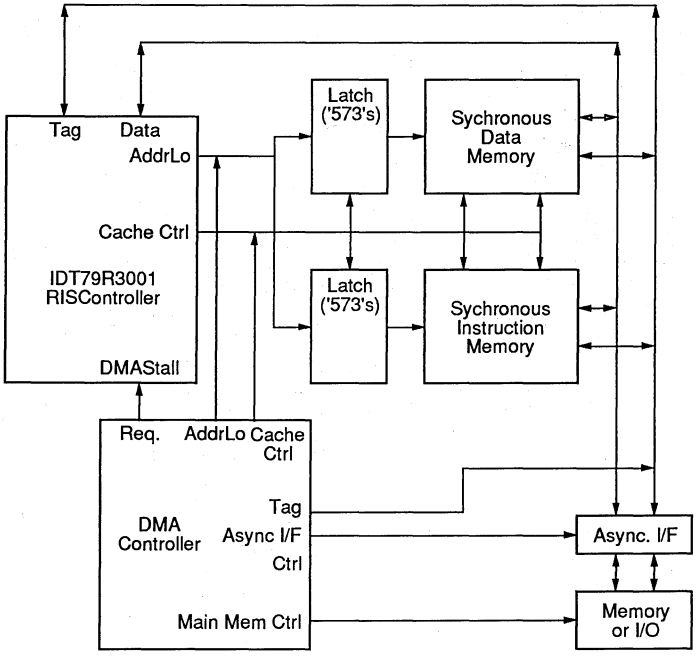


Figure 11. R3001 DMA Interface

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3c. Using the R3000's multiprocessor hooks for Cache invalidation. Solutions to the "stale data" problem discussed require CPU participation. They do not provide support in a Cache hierarchy where an autonomous System Bus master updates the cacheable System memory. (The CPU is unaware of the transaction.) The R3000 has a 2-signal protocol (MPStall,MPInvalidate) to invalidate entries in the data Cache. An independent state machine monitors the System bus for cacheable writes by another bus master. When detected, the address is stored in a register and the MPStall is asserted. The R3000 tri-states its address bus and this System Bus "snooper" supplies the Cache address. When MPInvalidate is asserted, the R3000 clears the Valid Bit at that entry. Figure 10 is a simple block diagram showing the hardware to support this feature.

This example does not compare the cache's tags to the address of the System Bus write. This means that the data in the Cache may have been from a different address (modulo Cache size) and invalidating that location was not required. Invalidating without address comparison may result in reduced Cache hit-rates and loss of performance. The Tag Bits can be read for comparison during MPStall cycles prior to invalidates. This is done with 1 or more Octal comparators (i.e. IDT74FCT521). This extra step will omit any unneeded Cache-entry invalidation.

THE R3001 DMA FEATURE

IDT added hooks to the R3001 providing access to the synchronous memory by an autonomous controller. While the "DMAStall" input is asserted the R3001 stalls and tri-states its outputs allowing complete control by the external master. This is a valuable feature when data transfer under program control is prohibitive or undesirable. Figure 11 illustrates the system connection of an external DMA master to an R3001 system. In this example the CPU's asynchronous interface is utilized to access resources. During DMAStall sourcing the Tag Bus is required to update the Cache tags if a Cache hierarchy exists or to supply high-order address lines during an asynchronous access.

The DMA Controller's bandwidth can exceed the CPU's bandwidth. A 25MHz R3K has a 100MBytes/second data bandwidth and requires 20 nanosecond SRAM. These SRAM's can support cycle times of 20 nanoseconds. Therefore, a carefully designed DMA controller could approach a 200Mbytes/second data bandwidth when using a separate clock source.

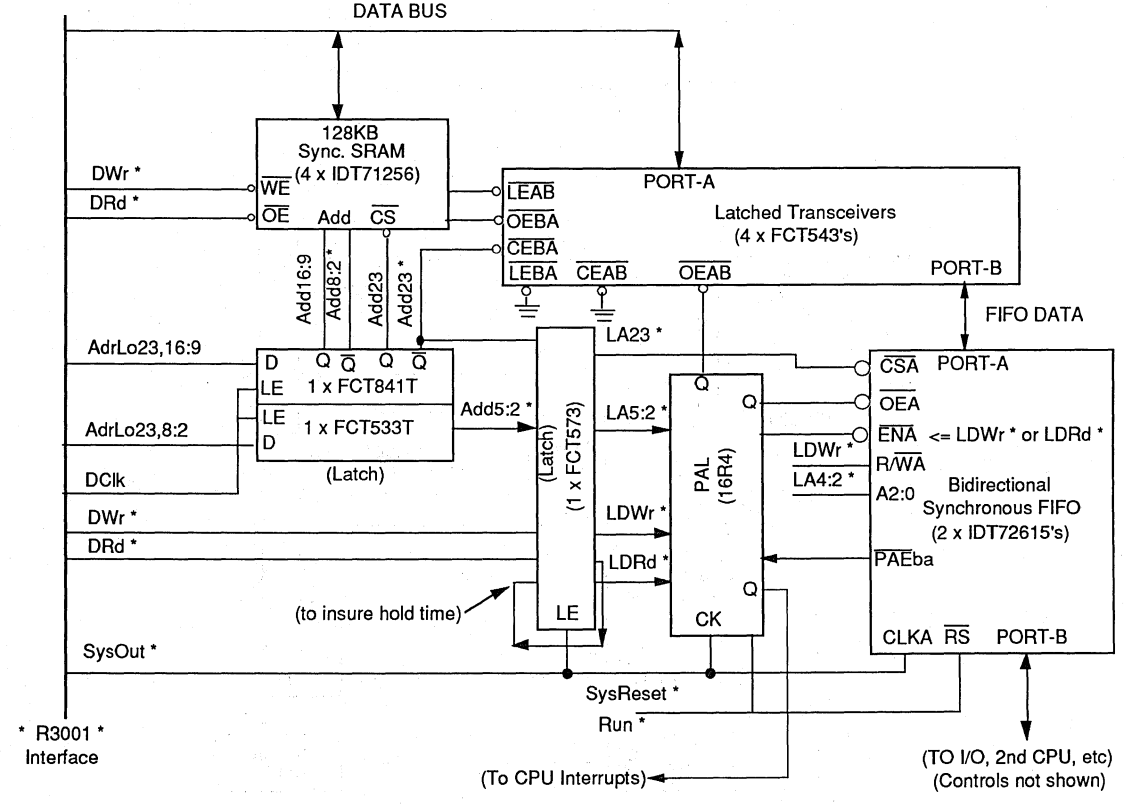

Figure 12. IDT Bidirectional FIFO's on the Synchronous Bus

Another use of the DMAStall feature is preloading the Instruction memory. This might be useful at power-up to bring code from I/O space to local memory or to Cache (to "lock" portions of speed critical code). This preloading is normally done by swapping the data and instruction memories (i.e. special internal control bits) and executing a Load (from I/0 space) Store (to sync memory) routine.

"ZERO LATENCY" DMA USING IDT'S 72605/615 BIDIRECTIONAL FIFO

Most R3K design examples show the synchronous bus with one memory bank to supply data. Because of the split cycle timing required to "ping -pong" between instruction and data resources, timing restrictions apply. However, by using the CPU's control lines and unused sync address lines additional data resources can reside on the synchronous bus. A second data path can be mapped into the synchronous space, providing DMA transfers at the full CPU bandwidth (100 MBytes/sec @ 25MHz) without latency.

Figure 12 illustrates 2 of IDT's 512 x 18 bidirectional synchronous (clocked) FIFO's interfaced to the synchronous bus. This device contains separate ('A to B' and 'B to A') FIFO banks providing a 200MByte/sec. duplex bandwidth in a 25MHz system. The ports are registered and allow free-running clocks. Flags provide buffer depth information that can interface to the CPU's interrupt or status inputs. (For more details on this device refer to Section 6.21 in IDT's "1990/91 Specialized Memories" Databook.)

This example details the described technique in a "Local Memory" approach with the R3001. 32K x 8 SRAM's are used for 128KB of local data and instruction memory each. A high-order address bit beyond the range of the local memory is used to "bank select" between the data SRAM and FIFO operation. (See Figure 13 for a function address map for this example.)

AddrLo23	AddrLo22:7	AddrLo5	AddrLo4:2	Function	Comments
0	x	x	x	implement SRAM or I/O	
0	x	x	x	implement SRAM or I/O	
1	x	x	0	Fifo data write during Store's	
1	x	x	001	Fifo bypass write during Store's	
1	x	x	1xx	Fifo offset reg. write during Store's	
1	x	x	0	Fifo data read during Load's	
1	x	x	001	Fifo bypass read during Load's	
1	x	0	1xx	Fifo offset reg. read	normal offset reads
1	x	1	11x	Fifo offset reg. read	FIFO now drives Bus
1	x	1	10x	Fifo offset reg. read	543 now drives Bus
1	x	1	01x	Reset PAL interrupt	(R3001 requirement)

NOTE: "x" = don't care

Figure 13. Function Address Map

Address mapping of resources on the asynchronous bus must have Address23 = 0 to avoid erroneous FIFO reads. (The control signal "Drd", always goes active during the first ("Run") cycle of any async. access.)

The FIFO's can't connect directly to the sync bus due to strict output enable/disable timing requirements. "Drd" must connect directly to the bus device. Therefore, a "gated" output-enable is required to perform the bank switch. This is accomplished by using the SRAM's chip select (normally tied active) and FCT543's for the FIFO path. The 74FCT543T is a bidirectional transceiver with separate latch and output enables that are gated with a chip select.

A transparent latch (74FCT573) is used to hold the CPU's sync control signals for an additional half cycle. To ease timing at high speeds, the FIFO operation occurs during phase 1 of the following cycle.

FIFO READS

Because of the registered output of the FIFO, a one-cycle latency is incurred for the first word. This occurs only when the buffer status goes from "Empty" to "Not Empty". This design example assumes that the data block sizes are known; therefore, once FIFO reads begin, Empty status will not occur until the last word of the block is read. If Empty was reached before the last word is read the program will load incorrect data into the Load's destination register.

When Empty status is completely deterministic, the 1-cycle latency is always handled by the execution of an initial "dummy" read from the FIFO. If this is undesirable the control PAL could initiate the dummy FIFO read upon deassertion of the EMPTY flag, thereby eliminating the latency.

The PAE (Programmable Almost Empty) output from the FIFO is used to invoke an interrupt, alerting the CPU to present data in the FIFO (when it de-asserts). The offset (from) can be set to any value and can be changed in between transfers to accommodate different block sizes and/or transfer rates. It is set to a value that guarantees Empty will not be reached before the entire data block is read by the CPU. This value can be "fine tuned" to minimize the CPU response time when the data source's rate is known.

The R3001 has inputs (called CpCond3:0) which are used by special conditional branch opcodes. This is an alternate (and faster) way to respond to the FIFO status. If the CPU is waiting for data from the FIFO, it can sit in a 2-instruction loop and branch immediately upon the receipt of the FIFO's flag.

Figure 14 shows example generic code to read a small block of FIFO data into the CPU's general registers to be used for computation.

```
FIFOread:  Load    ;from FIFO, destination = null (1st
                   word pipeline latency)
           Load    ;1st word into general register
           Load's  ; Additional loads equal to number of
                   available registers
           "
           "
           "
Compute:   Add,Sub, etc. ; OR Store to sync data SRAM's
```

Figure 14. Example Synchronous FIFO Read Routine

100% of the maximum bandwidth (100 Mbytes/second at 25MHz) is realized. Obviously, the limitation is based on the number of registers available (maximum of 32). A Load/Store (from FIFO/to local SRAM) routine can accommodate any block size at 50% of the maximum bandwidth. Recall that Loads & Stores execute in 1 cycle on the Synchronous Bus. The local SRAM can be viewed as an extension to the CPU's register stack. Figure 15 illustrates the timing for FIFO reads (including the initial "dummy read").

FIFO WRITES

Bandwidth capability for CPU writes to the FIFO is identical to FIFO reads. Unlike Reads, there is no latency associated with Writing the first word into the FIFO. However, to simplify timing on the FIFO bus, a "dummy" read is done to the FIFO's internal offset register to turn the (FIFO to '543's) bus around. Address bit 5 invokes the operation and Address bit 4 is used to determine direction. (See address function table, Figure 13) The Output Enables of the 543's and the FIFO's are sourced by a registered PAL. Skew between the two outputs represent minimal driving contention at a time the data is not used. No damage to the parts will occur.

Figure 16 shows example generic code to write a small block of data into the FIFO. Timing for the first two FIFO writes is also illustrated.

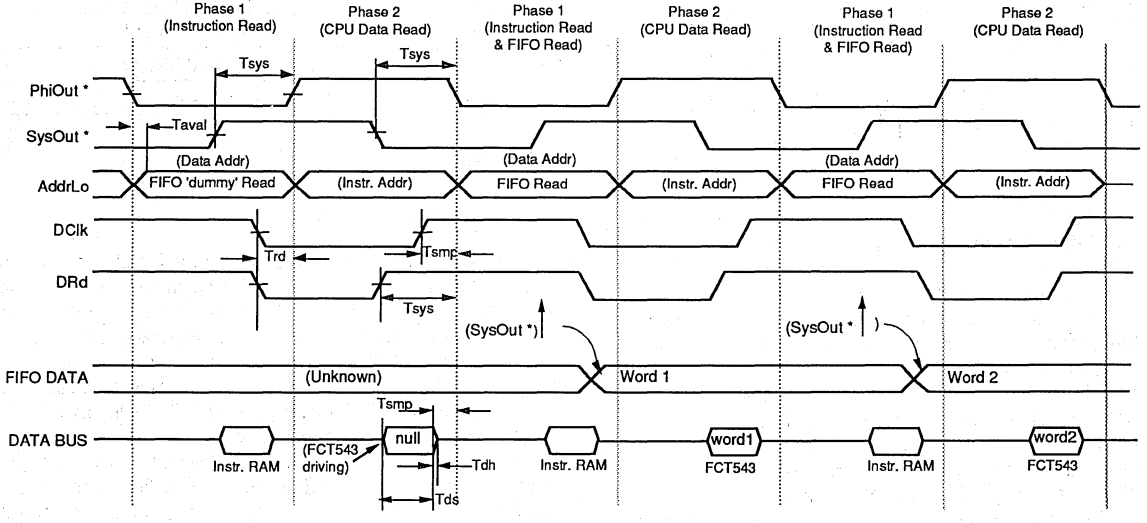

Figure 15. Synchronous FIFO Read Timing

```
FIFOwrite: Load     ; Special to turn FIFO bus around.
                    (543's now driving Bus)
           Store's  ; Number of Stores equal to number of
                    available registers
           "
           "
           "
```

Figure 16. Example Synchronous FIFO Write Routine

This FIFO design can be used in both Cache hierarchy and local memory designs. However, when using the data memory as a Cache (a portion of) the TAG inputs are supplied by SRAM. These Tag inputs must be supplied by a second device (i.e. 541 buffer) to insure the "hit" when the FIFO is read. The 541 inputs are "hardwired" to the address range of the FIFO. The I/O resources, cacheable async. memory, must be mapped so Address23 = 0 to prevent erroneous FIFO reads .

Connecting a second data resource onto the sync bus is a simple way to greatly improve latency and bandwidth in an R3K system. Logic parts like the FCT543T and FCT541T provide the gated output enable necessary to satisfy the bus timing, providing single cycle access to other system resources.

SUMMARY

This article explores various ways to improve data throughput in an R3000/3001 design. Other detailed references (listed below) are available for further study. When the R3K architecture was introduced, it gain immediate popularity as a workstation CPU.. Since introduction, however, IDT has realized many designs in other application areas, such as in embedded systems, that exploit the true potential of the architecture. With the internal cache controller, true Harvard Architecture, simple System Bus protocols, flexibility, speed, and small footprint, the R3000/R3001 fit the needs for a wide variety of systems designs.

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- IDT RISC R3000 Family Assembly Programmer's Guide
- IDT RISC R3000 Family System Programmer's Guide

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Integrated Device Technology, Inc.

R3051™ FAMILY PERFORMANCE IN EMBEDDED APPLICATIONS

APPLICATION NOTE AN-89

By V. S. Ramaprasad

INTRODUCTION

The IDTR3051™ is a family of RISC controllers specially suited for embedded applications. Instruction and data caches are integrated on the chip to yield cache hit rates of over 90% for a wide range of typical embedded applications. These RISC controllers also provide the designer with a simple interface to the rest of the system through built in read/write buffers, a multiplexed address/data bus and a small set of control signals. This simple interface enables the designer to select an optimal price/performance memory and I/O system.

In this application note the performance of a 33 MHz R3051 based system is presented. Standard integer benchmarks are run on the software model of the R3051 DRAM based sytem, and the results obtained are compared with the published results for 33 MHz i960 and 33 MHz 29K RISC processor based systems. The performance of R3051 based systems can be attributed to the raw horse power of R3000A core coupled with the highly desired optimal integration provided on the chip.

SYSTEM DESCRIPTION

The 33 MHz R3051 based system modelled is made up of 80ns DRAMS with a page mode access time of 50ns. The refill sizes for both the caches is four. The processors burst mode of access is utilized for refilling both the caches on cache misses. This implies that after the initial latency cycles the 2-way interleaved main memory is capable of supplying the subsequent instructions or data at the processor speed. The instructions are streamed into the processor along with the on chip cache refill.

The 33 MHz R3051 system is modelled with a software simulation tool called Cache305x. This software is based on the Cache2000, which is part of the Systems Programmers Package developed by MIPS Computer Systems. Cache2000 is used to model R3000/R3001 based systems with more than 98% accuracy of simulation.

To accurately model R3051 based systems, the existing Cache2000 is modified. Besides setting the cache sizes, the block refill sizes, the write buffer depth etc, sections are added to the Cache2000 program to simulate the bus priority scheme adopted by the R3051 family for processing the main memory transactions, and to implement the read/write protocols. Memory transactions are listed here with descending order of priorities. DMA activity is assumed not to be present in these simulations.

1. Current transaction completes without preemption.
2. Instruction cache misses are processed.
3. Data residing in the four deep write buffer is retired to the main memory.
4. Data cache misses are carried out next.

The read/write operations follow the priority scheme. The initiation of either of these transactions depends on the pending memory transaction requests. The built-in bus arbitration logic resolves the conflict for the memory bus following the above mentioned priority scheme. The arbitration unit operates in parallel with the execution core. The core could be executing instructions from the caches, while the bus arbitration unit is retiring the writes currently residing in the write buffer.

For instruction cache misses, in the best case where there is no write in progress, a read signal to the external memory is initiated one cycle after the core missed in the instruction cache. This extra cycle is for the arbitration unit to generate the read signal request. On top of this arbitration cycle, if a write is currently in progress, the processor stalls till the write operation is terminated. In this case, after a write operation a DRAM based system needs to be pre-charged before the read operation. The first instruction is read into the processor after the initial read latency of the memory system. The remaining three instructions are read in three consecutive cycles. After the reads, the DRAM pre-charge cycles are added to the total cycle count.

For data cache misses, there is an extra penalty of flushing the contents of the write buffer besides the extra one cycle for the arbitration. The number of cycles it takes to flush the write buffer depends on the number of words that are resident and also whether they could be retired as idle writes, or page writes, or non page writes. In the current system that is modelled, four words of data is brought in on a cache miss. The first word is read into the processor after the initial read latency of the memory system. The remaining three words are read in the following three consecutive cycles. After the reads, the DRAM pre-charge cycles are added to the total cycle count.

The write buffer interface decouples the core processor from the external slow memory system. Writes are retired in parallel with the processor executing out of the caches. In this state of execution, write operations always win the arbitration, and continuously retires the writes. This parallel mode of operation gets terminated only when the write buffer is full and a store is pending or when the processor can no longer execute out the caches. Keeping in mind that our interest in these simulations is the total cycle count for the complete execution of the program, write operations contribute to the total cycle count only when the processor needs to read from the external memory or when the processor can not proceed with the execution of a store instruction because the write buffer is currently full.

The penalty cycles due to writes delaying the processor external reads on cache misses are accounted for during the read transactions. When the write buffer is full and the

processor is executing a store instruction, penalty cycles that would vacate a single entry in the write buffer is added. This is not the same as retiring a single write, but it is equivalent to four cycles. This is due to the availability of an extra data register that captures the data being vacated from the write buffer. If another store follows in this situation where the four entries of the write buffer are full and the extra data buffer that drives the bus is loaded, the penalty is that of retiring a write to the memory.

DRAM PARAMETERS

The memory system considered in this R3051 design is made up of 80ns DRAMs with page mode access time of 50ns. The other parameters of the DRAM that affect the access time in different modes of DRAM are the initial read latency cycles, number of cycles to perform a write operation when the DRAM is in idle mode, number of cycles to perform a read/write operation when the DRAM is in page mode, number of cycles to perform a write operation when the DRAM is not in page mode. The parameters are set to fixed values to model a DRAM system that works with R3051 running at 33 MHz.

The initial read latency cycles at 33 MHz is the summation of the cycles to win the internal arbitration (1 cycle), cycles for the DRAM controller to generate RAS/CAS signals and perform a random read from the DRAM (6 cycles). The first word of instruction/data is read in the fixup cycle (1 cycle) . The remaining words are read in the three following cycles. It should be noted that the DRAM pre-charge cycles are part of the 6 cycle random read latency mentioned above.

The idle write latency is the number of cycles to retire a write when the DRAM is in idle mode. Using 80ns DRAMS this can be accomplished in 6 cycles. The page mode read or write operations can be completed in 3 cycles, while the non page writes can be carried out in 6 cycles. In the current system that is modelled with Cache305x, DRAM RAS pre-charge cycles are added when a read follows a write operation.

DRAM Parameters @ 33 MHz	
Read Latency	7 Cycles
RAS pre-charge	3 Cycles
Idle write	6 Cycles
Page write	3 Cycles
Non page write	6 Cycles

COMPETITION

In this application note two other RISC systems, namely the i960 and the 29K, are compared with the R3051 DRAM system.

The Intel i960CA system is the ASV960CA board running at 33MHz with 0 wait state memory for instructions and 3 wait state memory for the data. The memory is implemented with 15ns SRAM. Internally the i960CA has 1 KB of instruction cache memory. The benchmarks are compiled with 1.35 GCC/960 (results obtained from Intel).

The 29K system is the YARCs card running at 33 MHz using RevD AM29000. It has a 2 MBytes of instruction memory, and a 512 KBytes of data memory. The memories are implemented with 35ns Static RAMs (results obtained from AMD).

STANDARD INTEGER BENCHMARKS

Several standard integer benchmarks are run on the 33 MHz R3051 based system using the Cache305x. They are Quicksort, Bubblesort, Pi500, Anneal, Matmult, and Dhrystone1.1. (0) The suite was selected by Intel, these benchmarks are selected because of (1) the availability of results for two other RISC procesors, namely the i960 and the 29K, and (2) though being small, they still provide an insight into the capability of the processor in embedded environments.

Quicksort performs sorting of 5000 elements of an integer array using a recursive algorithm.

Bubblesort manipulates and sorts an array of 500 elements after reading a file.

Pi500 computes the value of the mathematical constant 'Pi' upto 500 decimal points. This program does not use any floating point math, but more than 50% of the cycles are spent in integer multiplications and integer divisions.

Anneal program solves the travelling-salesman problem by the method of simulated annealing.

Matmult is a program that loops for 100 times, and in each loop it performs the multiplication of two 8x8 integer arrays. The result is stored in another 8x8 array.

Dhrystone 1.1 benchmark demonstrates the integer number crunching power of the processor, although it is susceptible to compiler optimizations. Dhrystone 1.1 is reported here for the R3051 system instead of Dhrystone 2.0 for lack of data for the i960 and the 29K.

All the above mentioned integer benchmarks are compiled with a C compiler version 2.0 on an M/120 system running RISC/os 4.0. Except for Dhrystone benchmark, all the other benchmarks are compiled with the highest level of optimization O4. This includes optimization techniques such as global register allocation, optimal calling sequences, common subexpression elimination, procedure merging/inlining etc. For Dhrystone, O3 level of optimization is used. This level of optimization does not include procedure merging as it is against the spirit of Dhrystone benchmarking.

The results for R3051 are listed below along with the results published for 33 MHz i960 and 29K. The execution times for above mentioned programs are shown in the table (smaller values are better except for Dhrystone 1.1).

BENCHMARK	IDT R3051-33	i960CA-33	29K-33
QUICKSORT(ms)	**36**	50	46
BUBBLESORT(ms)	**41**	85	59
PI-500(ms)	**1,023**	1,624	1,282
ANNEAL(ms)	**5,056**	8,388	7,205
MATMULT(us)	**19,148**	26,898	44,578
DHRYSTONE 1.1	**55,236**	41,030	50,301

* R3051 system is 80ns DRAM based system.
* i960CA-33 system is ASV960CA with 0 ws for code and 3 ws for data.
* 29K-33 system is YARC card with 35ns SRAMs.

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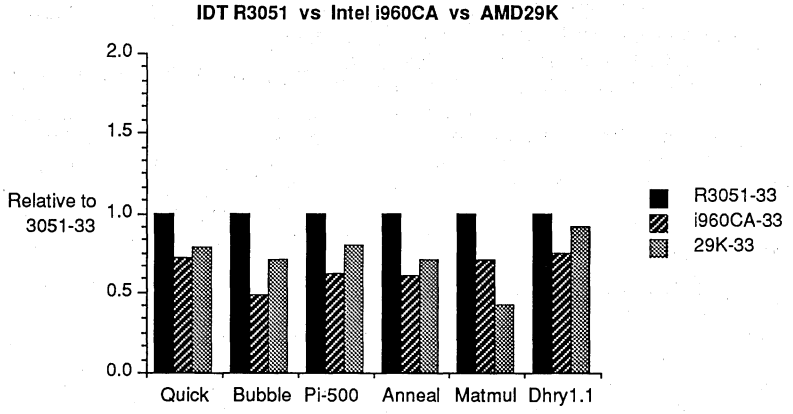

CONCLUSIONS

The standard integer benchmarks, even though they do not represent any real applications, provide an insight into the inherent performance of a processor when running typical embedded applications. The R3051 system considered here is a DRAM based system, and still delivers more performance compared to the fastest i960CA and 29K based designs. It can easily be deduced from the above data that the i960CA 33 MHz system is actually equivalent to a 21.2 MHz R3051 based system, and the 29K 33MHz system is equivalent to a 23.1 MHz R3051 based system. Still faster R305x systems are feasible when designed with Static RAMs and it is reasonable to expect further gains in performance.

1991 DATA BOOK UPDATE 1
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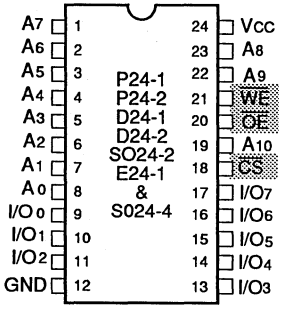
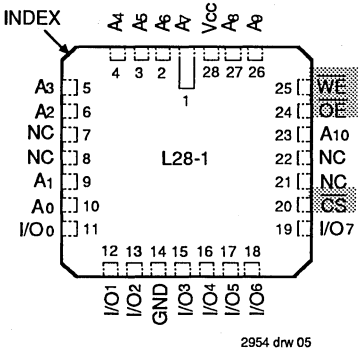
The following section contains partial data sheets that appeared in the 1991 SRAM Data Book. These data sheets had changes to less than 50% of the overall contents. Refer to the bars above changes to see where that section can be found in the 1991 SRAM Data Book.

PIN CONFIGURATIONS



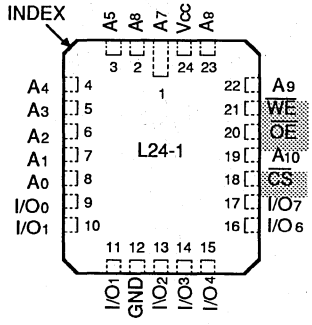
2954 drw 01

DIP/SOIC/CERPACK/SOJ
TOP VIEW



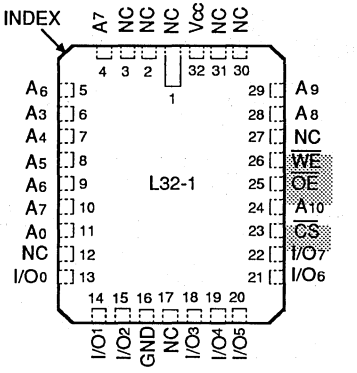
2954 drw 05

28-PIN LCC
TOP VIEW



2954 drw 03

24-PIN LCC
TOP VIEW



2954 drw 04

32-PIN LCC
TOP VIEW

DC ELECTRICAL CHARACTERISTICS (1)

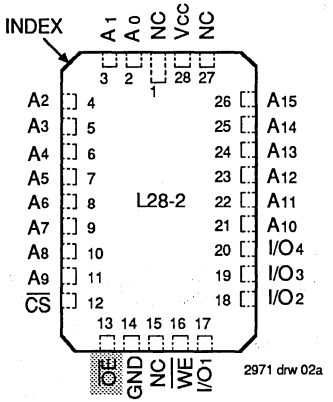
V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Power	6116SA15(2) 6116LA15(2) Com'l.	6116SA15(2) 6116LA15(2) Mil.	6116SA20 6116LA20 Com'l.	6116SA20 6116LA20 Mil.	6116SA25 6116LA25 Com'l.	6116SA25 6116LA25 Mil.	6116SA35 6116LA35 Com'l.	6116SA35 6116LA35 Mil.	Unit
I_{CC1}	Operating Power Supply Current, $\overline{CS}$ = V_{IL}, Outputs Open,	SA	105	—	105	130	100	110	80	90	mA
		LA	95	—	95	120	90	105	75	85	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges)

Symbol	Parameter	6116SA15(1) 6116LA15(1) Min.	6116SA15(1) 6116LA15(1) Max.	6116SA20 6116LA20 Min.	6116SA20 6116LA20 Max.	6116SA25 6116LA25 Min.	6116SA25 6116LA25 Max.	6116SA35 6116LA35 Min.	6116SA35 6116LA35 Max.	Unit
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns

PIN CONFIGURATION



LCC
TOP VIEW

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	61298S20 61298L20		61298S25 61298L25		61298S35 61298L35		61298S45 61298L45		61298S55 61298L55		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, V_{CC} = Max., f = 0(2), $V_{LC} \geq V_{IN} \geq V_{HC}$	S	30	—	30	35	30	35	30	35	—	35	mA
		L	1.5	—	1.5	4.5	1.5	4.5	1.5	4.5	—	4.5	

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{HC} = V_{CC} - 0.2V, V_{LC} = 0.2V

Symbol	Parameter	Test Condition	Min.	Typ.(1) Vcc @		Max. Vcc @		Unit
				2.0v	3.0V	2.0V	3.0V	
t_{CDR}(3)	Chip Deselect to Data Retention Time	$\overline{CS} \geq V_{HC}$ $V_{LC} \geq V_{IN} \geq V_{HC}$	0	—	—	—	—	ns

D

DC ELECTRICAL CHARACTERISTICS(1, 2)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	71256x20		71256x25		71256x30		71256x35		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open V_{CC} = Max., f = f_{MAX}(3)	S	155	—	145	150	140	145	135	140	mA
		L	135	—	115	130	110	125	105	120	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, V_{CC} = Max., f = 0	S	15	—	15	20	15	20	15	20	mA
		L	0.4	—	0.4	1.5	0.4	1.5	0.4	1.5	

Symbol	Parameter	Power	71256x45		71256x55		71256x70		71256x85[5]		71256x100		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
ICC	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open V_{CC} = Max., f = f_{MAX}[3]	S	130	135	—	135	—	135	—	135	—	135	mA
		L	100	115	—	115	—	115	—	115	—	115	
ISB1	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, V_{CC} = Max., f = 0	S	15	20	—	20	—	20	—	20	—	20	mA
		L	0.4	1.5	—	1.5	—	1.5	—	1.5	—	1.5	

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition	Min.	Typ.[1] V_{CC} @ 2.0v	Typ.[1] V_{CC} @ 3.0V	Max. V_{CC} @ 2.0V	Max. V_{CC} @ 3.0V	Unit
tCDR	Chip Deselect to Data	$\overline{CS} \geq V_{HC}$	0	—	—	—	—	ns

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71256S20[1] 71256L20[1]		71256S25 71256L25		71256S30 71256L30		71256S35 71256L35		71256S45 71256L45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tDW	Data to Write Time Overlap	11	—	13	—	14	—	15	—	20	—	ns

2968 tbl 11

NOTES:
1. 0° to +70°C temperature range only.
2. This parameter guaranteed but not tested.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71256S55[1] 71256L55[1]		71256S70[1] 71256L70[1]		71256S85[1] 71256L85[1]		71256S100[1,4] 71256L100[1,4]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	

2968 tbl 11

NOTES:
4. Also available: 120 and 150 ns military devices.

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	7164S15 7164L15 Com'l.	7164S15 7164L15 Mil.	7164S20[4] 7164L20[4] Com'l.	7164S20[4] 7164L20[4] Mil.	7164S25[4] 7164L25[4] Com'l.	7164S25[4] 7164L25[4] Mil.	7164S30 7164L30 Com'l.	7164S30 7164L30 Mil.	Unit
I_{SB1}	Full Standby Power Supply Current (CMOS Level), f = 0[3], V_{CC} = Max. 1. $\overline{CS_1} \geq V_{HC}$ and $CS_2 \geq V_{HC}$, or 2. $CS_2 \leq V_{LC}$	S	15	—	15	20	15	20	15	20	mA
		L	0.2	—	0.2	1	0.2	1	0.2	1	

Symbol	Parameter	Power	7164S35 7164L35 Com'l.	7164S35 7164L35 Mil.	7164S45 7164L45 Com'l.	7164S45 7164L45 Mil.	7164S55 7164L55 Com'l.	7164S55 7164L55 Mil.	7164S70/85[2] 7164L70/85[2] Com'l.	7164S70/85[2] 7164L70/85[2] Mil.	Unit
I_{SB}	Standby Power Supply Current (TTL Level), $\overline{CS_1} \geq V_{IH}$, or $CS_2 \leq V_{IL}$ V_{CC} = Max., Outputs Open, f = f_{MAX}[3]	S	20	20	—	20	—	20	—	20	mA
		L	3	5	—	5	—	5	—	5	
I_{SB1}	Full Standby Power Supply Current (CMOS Level), f = 0[3], V_{CC} = Max. 1. $\overline{CS_1} \geq V_{HC}$ and $CS_2 \geq V_{HC}$, or 2. $CS_2 \leq V_{LC}$	S	15	20	—	20	—	20	—	20	mA
		L	0.2	1	—	1	—	1	—	1	

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition	Min.	Typ.[1] V_{CC} @ 2.0v	Typ.[1] V_{CC} @ 3.0V	Max. V_{CC} @ 2.0V	Max. V_{CC} @ 3.0V	Unit
t_{CDR}[3]	Chip Deselect to Data Retention Time	1. $\overline{CS_1} \geq V_{HC}$ $CS_2 \geq V_{HC}$ or	0	—	—	—	—	ns

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	°C

NOTES:
2. I/O pins must not exceed V_{CC} + 0.5V

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage	2.2	—	6.0[2]	V

NOTES:
2. I/O pins must not exceed V_{CC} + 0.5V

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%)

Symbol	Parameter	61B298S12 Com'l.	61B298S12 Mil.	61B298S15 Com'l.	61B298S15 Mil.	61B298S20 Com'l.	61B298S20 Mil.	Unit
Icc	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	190	—	170	180	150	160	mA

Figure 1B. AC Test Loads
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW} and t_{WHZ})

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	61B298S12(1)		61B298S15		61B298S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tDW	Data Set-up	6	—	7	—	9	—	ns

FEATURES:

- Fast Output Enable
- — Commercial: 4/5/6ns
- — Military: 5/6/7ns
- Single 5V power supply

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM(2)	Operating Temperature	0 to +70	-55 to +125	°C
	61B98S8 Only	0 to +55	N/A	°C

NOTES: 2958 tbl 02
2. I/O pins must not exceed Vcc + 0.5V.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
	61B98S8 Only	4.75	5.0	5.25	V
VIH	Input High Voltage	2.2	—	6.0(2)	V

NOTES: 3000 tbl 04
2. I/O pins must not exceed Vcc + 0.5V.

DC ELECTRICAL CHARACTERISTICS

Vcc = 5.0V ± 10% (61B98S8 Vcc = 5.0V ± 5%)

DC ELECTRICAL CHARACTERISTICS(1)

(Vcc = 5.0V ± 10%) (61B98S8 VCC = 5.0 ± 5%)

Symbol	Parameter	61B98S8(3)		61B98S10		61B98S12		61B98S15		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	

NOTES:
3. Vcc = 5V ± 5%, 0°C ≤ TA ≤ 55°C.

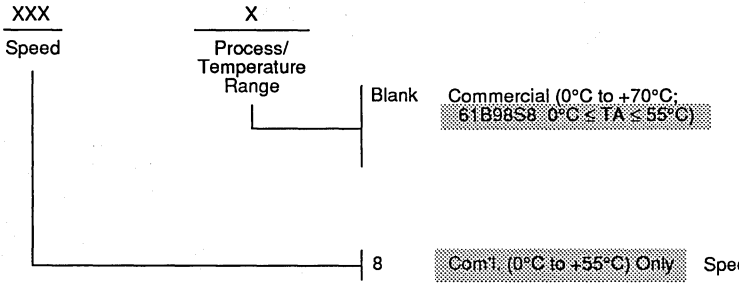
Figure 1B. (for tCLZ, tCHZ, tOLZ, tOHZ, tWHZ, and tOW)

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10% All Temp. Ranges, 61B98S8 Vcc = 5V ± 5%)

Symbol	Parameter	61B98S8(1)		61B98S10		61B98S12		61B98S15(3)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tCLZ(2)	$\overline{CS}$ to Output in Low Z	1	—	1	—	1	—	1	—	ns
tOLZ(2)	$\overline{OE}$ to Output Low Z	1	—	1	—	1	—	1	—	ns
tWHZ(2)	$\overline{WE}$ to Out in High Z	—	3	—	3	—	3	—	4	ns

NOTES: 3000 tbl 08
1. 0° to +55°C temperature range only. Vcc = 5V ± 5%, 0°C ≤ TA ≤ 55°C.

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V

NOTE:
2. I/O pins must not exceed Vcc + 0.5V.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage	2.2	—	6.0(2)	V

NOTE:
2. I/O pins must not exceed Vcc + 0.5V.

DC ELECTRICAL CHARACTERISTICS(1)

(Vcc = 5.0V ± 10%)

Symbol	Parameter	71B256S12		71B256S15		71B256S20		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
Icc	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, Vcc = Max., f = f_{MAX}(2)	220	—	210	—	180	190	mA

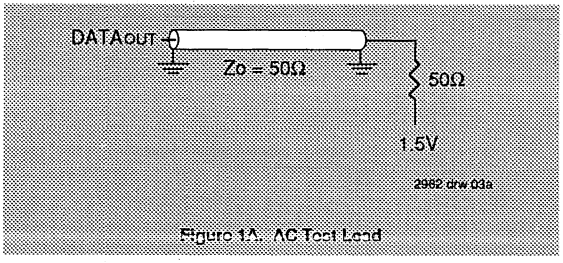
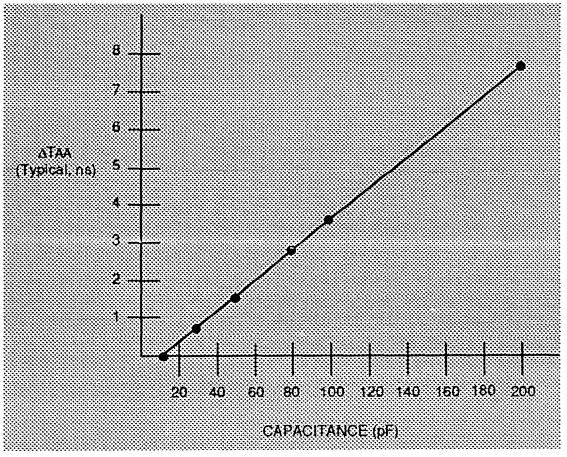


Figure 1A. AC Test Load

Figure 1B. AC Test Load
(for tCLZ, tOLZ, tCHZ, tOHZ, tOW, and tWHZ)

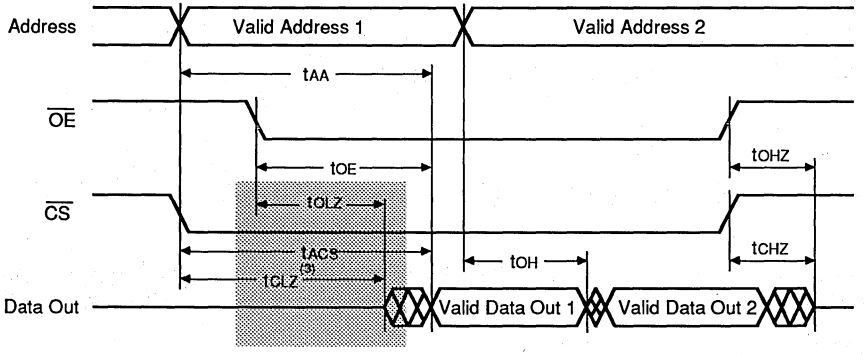


D

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71B256-12[1]		71B256-15[1]		71B256-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tACS	$\overline{CS}$ Access Time	—	7	—	8	—	10	ns
tCLZ[2]	$\overline{CS}$ to Output in Low Z	3	—	3	—	3	—	ns
tOE	$\overline{OE}$ to Output Valid	—	7	—	8	—	10	ns
tOLZ[2]	$\overline{OE}$ to Output Low Z	3	—	3	—	3	—	ns
tOH	Out Hold from Addr Change	5	—	5	—	5	—	ns
tDW	Data Setup	6	—	7	—	9	—	ns
tDH	Data Hold	0	—	0	—	0	—	ns
tOW[2]	Output from End of Write	3	—	3	—	3	—	ns

TIMING WAVEFORM OF READ CYCLE[1,2]



RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIH	Input High Voltage	2.2	—	6.0[2]	V

NOTES:
2. I/O pins must not exceed Vcc + 0.5V.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
VTERM[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V

NOTES:
2. I/O pins must not exceed Vcc + 0.5V.

DC ELECTRICAL CHARACTERISTICS[1]

(Vcc = 5.0V ± 10%)

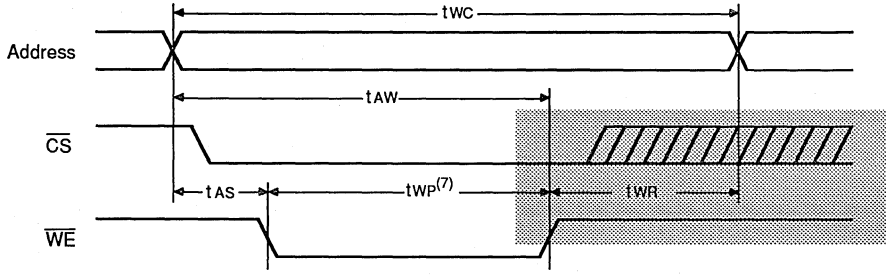
Symbol	Parameter	71B258S12		71B258S15		71B258S20		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
ICC	Dynamic Operating Current $\overline{CS}$ = VIL, Outputs Open, Vcc = Max., f = fMAX[2]	190	—	170	180	150	160	mA

Figure 1B. AC Test Load (for tCLZ, tCHZ, tOW, and tWHZ)

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71B258-12[1]		71B258-15		71B258-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tDW	Data Set-Up Time	6	----	7	----	9	----	ns
tOW[2]	Out Active from End of $\overline{WE}$	2	—	2	—	2	—	ns

TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 5,6]



D

The following section contains full data sheets that appeared in the 1991 SRAM Data Book. These data sheets had changes to 50% or more of the overall contents and are now considered new. Refer to the bar at the top of each page to see where that page can be found in the 1991 SRAM Data Book.

Integrated Device Technology, Inc.

CMOS CacheRAM™ 32K X 9-BIT (288K-BIT) BURST COUNTER & SELF-TIMED WRITE

IDT71589

FEATURES:

- High density 32K x 9 architecture
- Internal write registers (address, data, and control)
- Self-timed write cycle
- Internal burst read and write address counter
  Clock to data times: 14, 19, 24, 34ns
- Chip select for depth expansion
- Matches all timing and signals of Intel™ 486™ processors up to 50MHz
- Packaged in plastic or hermetic 300 mil 32-pin DIP, and plastic 300 mil 32-pin SOJ
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT71589 is an extremely high-speed 32K x 9-bit static RAM with full on-chip hardware support of the Intel i486 CPU interface. This part is designed to facilitate the implementation of the highest-performance secondary caches for the i486 architecture while using low-speed cache-tag RAMs and PALs and consuming the minimum possible board space.

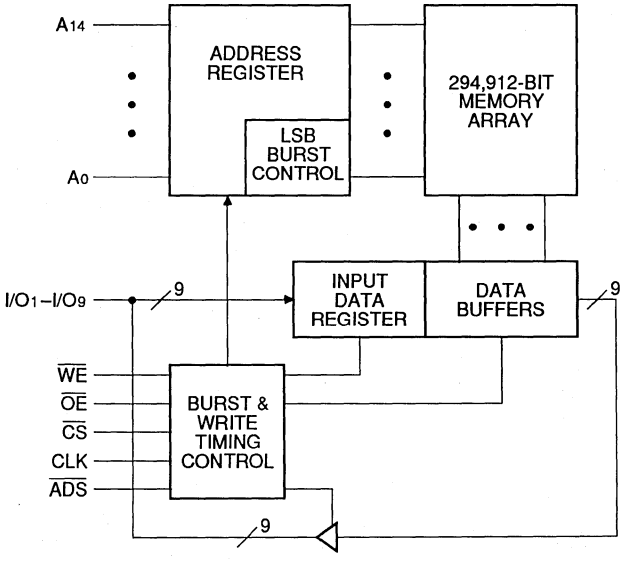
The IDT71589 CacheRAM contains a full set of write data and address registers. Internal logic allows the processor to generate a self-timed write based upon a decision which can be left until the extreme end of the write cycle.

An internal burst address counter accepts the first cycle address from the processor, then cycles through the adjacent four locations using the i486's burst refill sequence on appropriate rising edges of the system clock.

Fabricated using IDT's CEMOS™ high-performance technology, this device operates at a very low power consumption and offers a maximum clock to data access time as fast as 14ns.

The IDT71589 CacheRAMs are packaged in a 32-pin plastic or hermetic DIP, or a plastic J-bend small-outline (SOJ) package. Military grade devices are available 100% processed in compliance to the test methods of MIL-STD-883, Class B, Method 5004.

FUNCTIONAL BLOCK DIAGRAM



2951 drw 01

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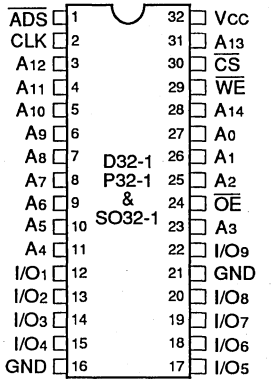
Intel and i486 are trademarks of Intel Corp.

PIN CONFIGURATION



2951 drw 02

DIP/SOJ
TOP VIEW

PIN NAMES

A_0–A_{14}	Address Inputs
I/O_1–I/O_9	Data Input/Output
$\overline{CS}$	Chip Select/Count Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{ADS}$	Address Status
CLK	System Clock
GND	Ground
Vcc	Power

2951 tbl 01

SPEED SELECTION

i486 Speed	Suggested IDT71589
25MHz	IDT71589S35
33MHz	IDT71589S25
40MHz	IDT71589S20
50MHz	IDT71589S14

2951 tbl 02

COUNT SEQUENCE(1) (A_0, A_1 ONLY)

Start	+1	÷2	÷3
0	1	2	3
1	0	3	2
2	3	0	1
3	2	1	0

NOTE: 2951 tbl 12
1. The counter wraps around to its starting value and repeats the same sequence after the last count.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–65 to +135	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation Plastic Hermetic	 1.5 2.0	W
I_{OUT}	DC Output Current	50	mA

NOTE: 2951 tbl 03
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2951 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0.0	V
V_{IH}	Input High Votage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2951 tbl 05
1. V_{IL} = –3.0V for pulse width less than 5ns.

D

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	—	10	µA
V_{OL}	Output Low Voltage (I/O_1–I/O_9)	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

2951 tbl 06

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

			71589S14[3]		71589S20		71589S25		71589S35		
Symbol	Parameter	Test Condition	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Unit
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0[2]	TBD	—	130	—	130	TBD	130	TBD	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	TBD	—	240	—	220	TBD	200	TBD	mA

NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.
3. Preliminary information only.

2951 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2951 Tbl 08

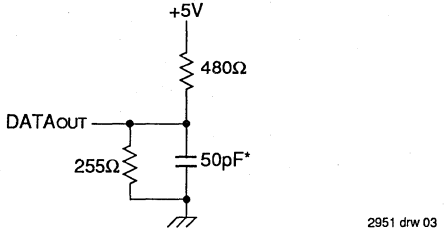
CAPACITANCE

(T_A = +25°C, f = 1.0 MHz, SOJ package only)

Symbol	Parameter[1]	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
$C_{I/O}$	Input/Output Capacitance	V_{OUT} = 0V	7	pF

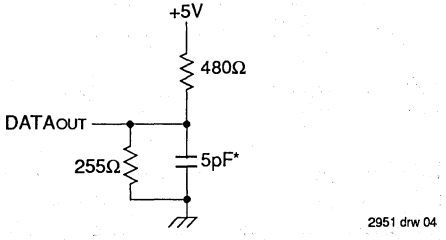
NOTE:
1. This parameter is determined by device characterization but is not production tested.

2951 tbl 09



2951 drw 03

Figure 1. Output Load



2951 drw 04

Figure 1. Output Load (for t_{OHZ}, t_{CHZ}, t_{OLZ} and t_{CLZ})

*including scope and jig

FUNCTIONAL DESCRIPTION

The IDT71589 is an extremely fast 32K x 9 CMOS static CacheRAM with internal edge-triggered registers dedicated to the support of the Intel i486 CPU. These registers support the fastest systems and allow a 128KByte or larger cache to be designed to consume the smallest number of chips, the lowest power and board space, and allow the designer to avoid the use of expensive high-speed cache-tag RAMs and PALs.

The internal registers are designed to support two high speed functions: Burst read cycles, and a late-abort self-timed write cycle.

Burst read cycles are accomplished through the assertion of the $\overline{ADS}$ signal with a valid address input during the rising edge of the clock input. This address will be used to access the data in the CacheRAM during the next clock cycle, and data will be output during the following three cycles in accordance with the i486's burst refill sequence (i.e., during the next cycle the address' LSB is inverted, then the second LSB is inverted as the LSB is restored to its original value, etc.). Since the CacheRAM contains this counter internally, the critical clock-to-data time of even the fastest CPU speeds can be met by using a slower RAM speed grade without resorting to chip-intensive interleaving schemes. Should the $\overline{ADS}$ signal be sampled as valid after having been sampled as invalid, any bursting in process will be reinitialized to the new address, and a new burst cycle will be started. The burst counter wraps around at the end of the sequence and continues to count until stopped by the $\overline{ADS}$ or $\overline{CS}$ inputs. A fast copy-back scheme can harness this capability by reading, then writing the four burst addresses within a single burst cycle.

The self-timed write cycle significantly eases the timing of the address and data inputs during a write cycle, and allows the write/don't write decision to be postponed until the very end of the second cycle of a write cycle. During a write cycle, the address will be strobed into the address register during the first rising edge of the clock after the $\overline{ADS}$ input becomes valid. Data is sampled into the data input register during the next cycle's rising edge, as is the write enable input. If a write has been enabled the data will be written from the address and input data registers into the CacheRAM during the high phase of the clock of that cycle.

A chip select pin is provided to give control over interruption of write cycles and burst read cycles. When the $\overline{CS}$ input is used to interrupt a burst cycle, it operates as a synchronous input to the burst counter. A low level must be present on the chip select input and must satisfy data set-up and hold times in order for the counter to progress to its next state. To stop the counter at its current state, the chip select input must be taken high, and must stay high long enough to satisfy the CacheRAM's data set-up and hold times. The $\overline{CS}$ pin also is used as an auxiliary to the $\overline{WE}$ input. Writes can only be accomplished if both $\overline{CS}$ and $\overline{WE}$ are simultaneously sampled active.

Address set-up times have been reduced on the 50MHz (14ns) part to allow address outputs of the processor to be buffered before being input to the 71589. This dramatically reduces problems stemming from capacitive loading on the processor pins. Longer hold times on these inputs are easily accommodated by the fact that address outputs are always available from the processor for an entire clock cycle.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71589S14[4]		71589S20[1]		71589S25		71589S35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tCYC	Clock Cycle Time	20	—	25	—	30	—	40	—	ns
tCH	Clock Pulse High	8	—	10	—	11	—	14	—	ns
tCL	Clock Pulse Low	8	—	10	—	11	—	14	—	ns
tSD	Set-up Time ($\overline{ADS}$, $\overline{WE}$, $\overline{CS}$, Input Data)	3	—	3	—	4	—	5	—	ns
tSA	Address Set-up Time	0	—	3	—	4	—	5	—	ns
tHD	Hold Time ($\overline{ADS}$, $\overline{WE}$, $\overline{CS}$, Input Data)	1	—	1	—	1	—	1	—	ns
tHA	Address Hold Time	5	—	5	—	5	—	5	—	ns
tCD	Clock to Data Valid	—	14	—	19	—	24	—	34	ns
tDC	Data Valid After Clock	3	—	4	—	4	—	5	—	ns
tOE	Output Enable to Output Valid	—	7	—	8	—	9	—	10	ns
tOLZ	Output Enable to Output in Lo-Z[2,3]	2	—	2	—	2	—	2	—	ns
tOHZ	Output Disable to Output in Hi-Z[2,3]	—	7	—	8	—	9	—	10	ns

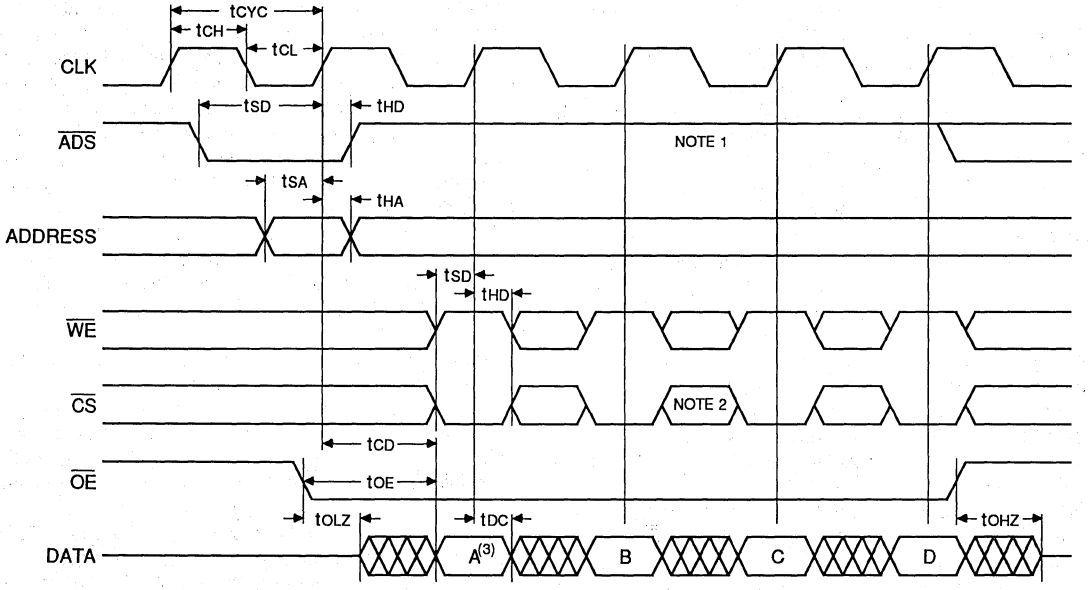
NOTES:

2951 tbl 10

1. 0°C to +70°C Temperature range only.
2. Transition is measured ±200mV from low or high impedence voltage with load (Figure 2).
3. This parameter is guaranteed, but not tested.
4. Preliminary information only.

D

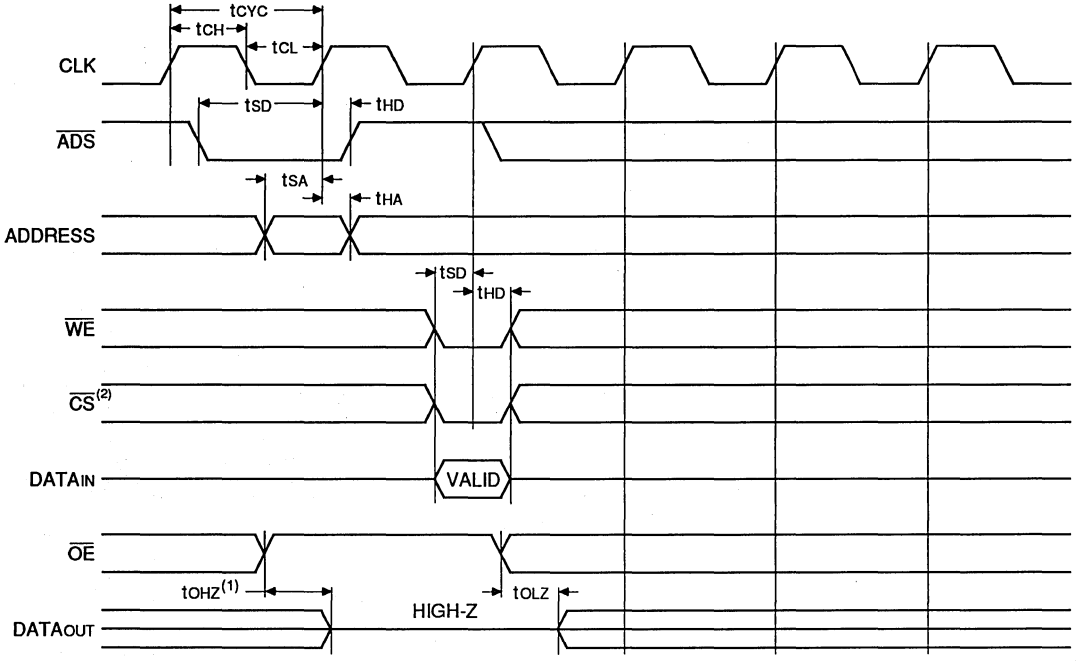
TIMING WAVEFORM OF BURST READ CYCLE



2951 drw 05

NOTES:
1. If $\overline{ADS}$ goes low during a burst cycle, a new address will be loaded and another burst cycle will be started.
2. If $\overline{CS}$ is taken inactive during a burst read cycle, the burst counter will discontinue counting until $\overline{CS}$ input again goes active. The timing of the $\overline{CS}$ input for this control of the burst counter must satisfy setup and hold parameters t_S and t_H.
3. A-Data from input address
   B-Data from input address except A_0 is now $\overline{A}_0$
   C-Data from input address except A_1 is now $\overline{A}_1$
   D-Data from input address except A_0 and A_1 are now $\overline{A}_0$ and $\overline{A}_1$

TIMING WAVEFORM OF WRITE CYCLE

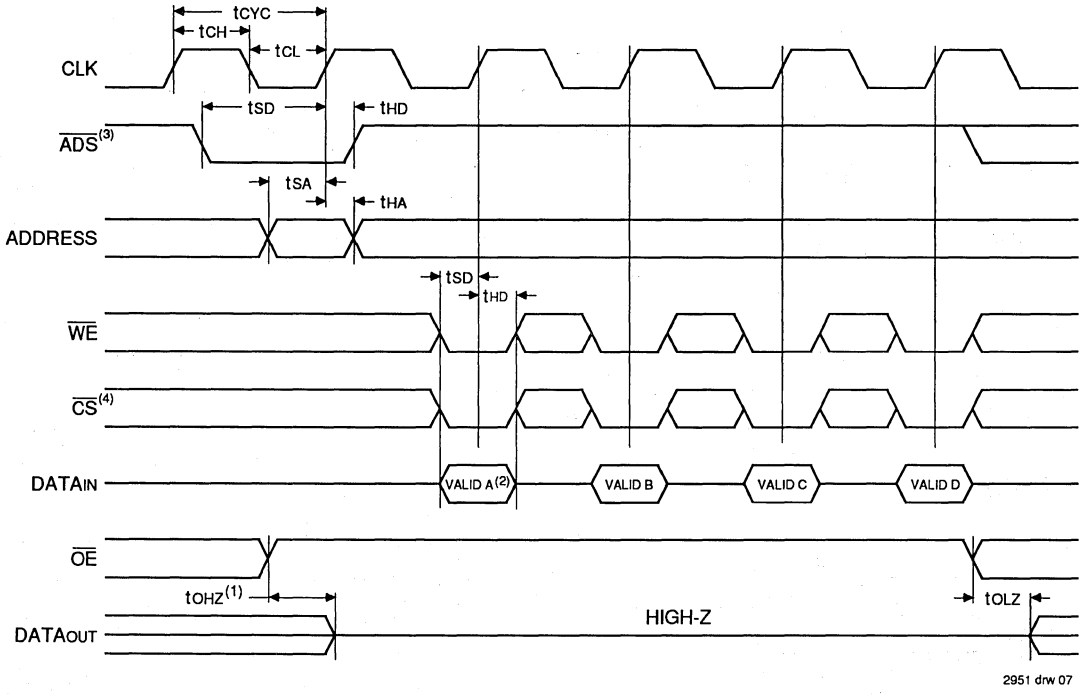


2951 drw 06

NOTES:
1. $\overline{OE}$ Must be taken inactive at least as long as t_{OHZ} + ts before the second rising clock edge of write cycle.
2. $\overline{CS}$ timing is the same as any synchronous signal when used to block writes or to stop the burst count sequence.

D

TIMING WAVEFORM OF BURST WRITE CYCLE



NOTES:

1. $\overline{OE}$ Must be taken inactive at least as long as t_{OHZ} + ts before the second rising clock edge of write cycle.
2. A-Data to be written to original input address.
   B-Data to be written to original input address except A_0 is now $\overline{A}_0$.
   C-Data to be written to original input address except A_1 is now $\overline{A}_1$.
   D-Data to be written to original input address except A_0 and A_1 are now $\overline{A}_0$ and $\overline{A}_1$
3. If $\overline{ADS}$ goes low during a burst cycle, a new address will be loaded, and another burst cycle will be started.
4. If $\overline{CS}$ is taken inactive during a burst write cycle the burst counter will discontinue counting until the $\overline{CS}$ input again goes active. The timing of the $\overline{CS}$ input for this control of the burst counter must satisfy setup and hold parameters ts and t_H. $\overline{CS}$ timing is the same as any synchronous signal when used to block writes or to stop the burst count sequence.

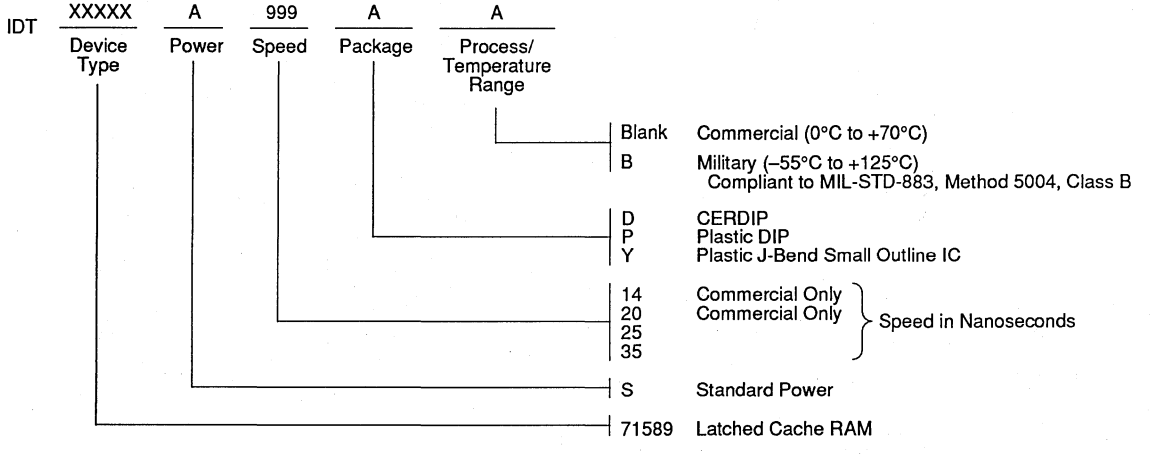
TRUTH TABLE

CLK	Previous $\overline{ADS}$	$\overline{ADS}$	Address	$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O	Function
↑	H	L	Valid Input	X	X	—	—	Preset Address Counter
↑	X	H	—	—	—	—	—	Ignore External Address Pins
↑	L	X	—	—	—	—	—	Ignore External Address Pins
↑	X	H	—	—	L	—	—	Sequence Address Counter
↑	L	X	—	—	L	—	—	Sequence Address Counter
↑	X	H	—	—	H	—	—	Suspend Address Sequencing
↑	L	X	—	—	H	—	—	Suspend Address Sequencing
—	—	—	—	—	—	H	Hi-Z	Outputs Disabled
—	—	—	—	H	—	L	$DATA_{OUT}$	Read
↑	X	H	—	L	L	H	$DATA_{IN}$	Write
↑	L	X	—	L	L	H	$DATA_{IN}$	Write
—	—	—	—	L	L	L	—	Not Allowed

2951 tbl 11

NOTE:
H = HIGH
L = LOW
X = Don't Care
– = Unrelated
Hi-Z = High Impedance

ORDERING INFORMATION



2951 drw 08

D

Integrated Device Technology, Inc.

BiCameral™ CacheRAM™ 288K (16K x 9 x 2) FOR RISC CACHES

ADVANCE INFORMATION IDT71B229S

FEATURES:

- Supports the R3000 and R3001 to 40MHz
- BiCameral organization:
  - — Split instruction/data cache support
  - — No bank-switching timing contention
- Single address bus
- Single data bus
- Separate write enable and output enable for each bank
- Standard read and write control interface
- Internal address latches
- 32-pin 300 mil SOJ package

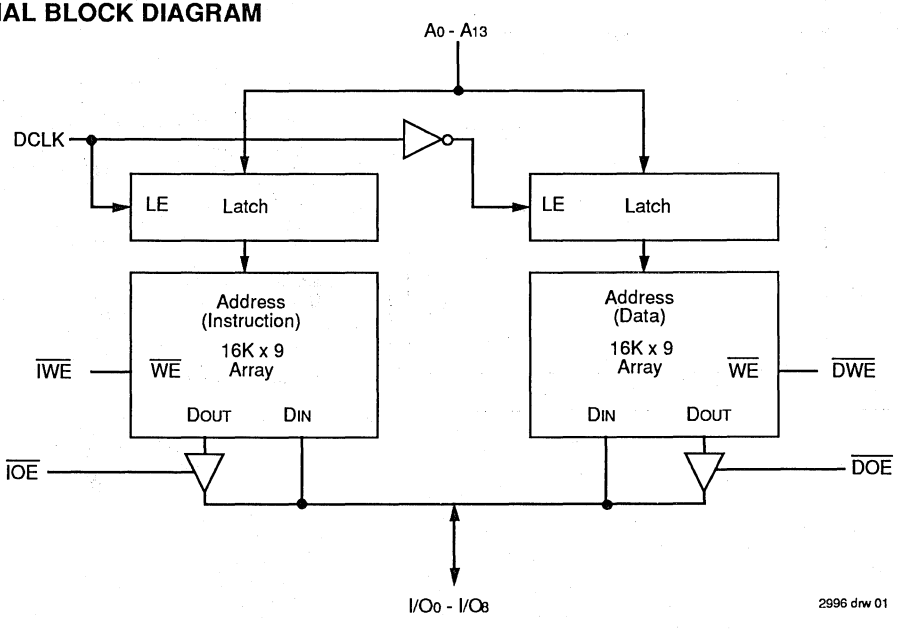
DESCRIPTION:

The IDT71B229 is a BiCameral CacheRAM specifically designed to support the split instruction and data caches of the IDT 79R3000 microprocessor. A complete 128KByte cache for the R3000 can be built with only six to seven IDT71B229s (depending on the main memory size supported by the system), while an R3001 cache can be built with five to six parts. CPU clock frequencies up to 40 MHz are supported. The small 300 mil package allows a 128 KByte cache to fit in a circuit board area of approximately two square inches.

Internal address latches eliminate the need for external latches. The BiCameral (two bank) organization reduces the number of devices required to support the R3000's split-cache architecture and eliminates contention problems encountered when one RAM bank is being enabled while the other is being disabled. All timing parameters have been optimized to support the complete range of R3000 clock speeds, simplifying R3000 cache design.

Made with BiCEMOS™, IDT's advanced high-speed process, the IDT71B229 provides dense caches in low board space while consuming minimum power.

FUNCTIONAL BLOCK DIAGRAM



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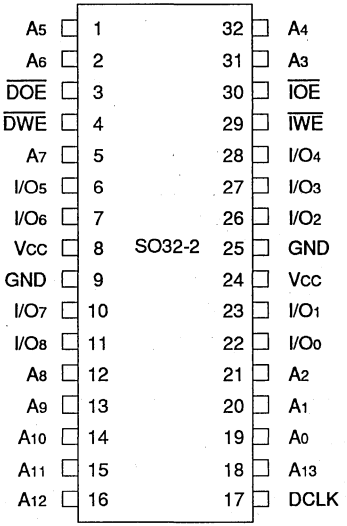
PIN CONFIGURATIONS



SOJ
TOP VIEW

2996 drw 02

TRUTH TABLE 1

$\overline{IOE}$	$\overline{IWE}$	$\overline{DOE}$	$\overline{DWE}$	I/O(0:8)	Function
H	H	L	H	Out, D Bank	Read D Bank data
H	H	H	L	High Z	Write data to D Bank
L	H	H	H	Out, I Bank	Read I Bank data
H	L	H	H	High Z	Write data to I Bank
H	H	H	H	High Z	No Activity
L	L	X	X	High Z	Not Allowed
L	X	L	X	High Z	Not Allowed
L	X	X	L	High Z	Not Allowed
X	L	L	X	High Z	Not Allowed
X	L	X	L	High Z	Not Allowed
X	X	L	L	High Z	Not Allowed

2996 tbl 01

TRUTH TABLE 2(1)

DCLK	I Address Latch	D Address Latch
L	Transparent	Latched
H	Latched	Transparent

2996 tbl 02

NOTE:
1. L = Low, H = High, X = Don't Care, - = Unrelated, High Z = High Impedance

D

PIN DESCRIPTION

Name	Description
DCLK	DCLK, when high, allows the address inputs to flow through the D bank's address latch. Conversely, the address in the I bank's latch is held during a high input on DCLK. Taking DCLK low freezes data in the D bank's address latch and allows addresses to flow through the I bank's address latch.
$\overline{IOE}$	I Output Enable enables the data outputs from the I bank onto the data input/output pins. $\overline{IOE}$ must not be asserted simultaneously with the $\overline{DOE}$, $\overline{DWE}$ or $\overline{IWE}$ pins.
$\overline{DOE}$	This is an input which enables the data outputs from the D bank onto the data input/output pins. $\overline{DOE}$ must not be asserted simultaneously with the $\overline{IOE}$, $\overline{IWE}$ or $\overline{DWE}$ pins.
$\overline{IWE}$	I Write Enable, when low, gates data from the input/output pins into the RAM at the I bank address indicated by the output of the I bank address latch. Neither $\overline{DOE}$ nor $\overline{IOE}$ should be enabled during a write operation.
$\overline{DWE}$	D Write Enable is an input which is taken low to gate data from the input/output pins onto the RAM at the address being output from the D bank address latch. Neither $\overline{DOE}$ or $\overline{IOE}$ should be asserted during a write operation.
Addr(0:13)	The fourteen address inputs are used to access any of the 16,384 locations in either the D or I bank. When an address latch is in the transparent state, these pins are routed directly to that latch's RAM bank. Taking the latch into its latched state causes that RAM bank to ignore subsequent changes on the address input pins.
I/O0:8	The input/output bus comprises nine signals whose functions are determined by the state of the $\overline{IOE}$, $\overline{IWE}$, $\overline{DOE}$ and $\overline{DWE}$ pins. During Output Enables, data is output upon these pins from the selected RAM bank from an address pointed to by the outputs of that bank's address latch. When either Write Enable is asserted, data can be written from these pins into the selected bank's RAM at the address being output by that bank's address latch. When $\overline{IOE}$, $\overline{IWE}$, $\overline{DOE}$ and $\overline{DWE}$ are all inactive, the input/output pins are floated in a high-impedance state.

2996 tbl 03

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2996 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC}+0.5	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTES: 2996 tbl 05

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE: 2996 tbl 06

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS(1, 2)

(V_{CC} = 5.0V ± 5%)

Symbol	Parameter	71B229S12 Com'l.	71B229S16 Com'l.	71B229S22 Com'l.	71B229S28 Com'l	Unit
I_{CC1}	Operating Power Supply Current Outputs Open, V_{CC} = Max., f = 0	135	130	130	130	mA
I_{CC2}	Dynamic Operating Current Outputs Open, V_{CC} = Max., f = f_{MAX}	200	195	190	185	mA

NOTES:

2996 tbl 07

1. All values are maximum guaranteed values.
2. f = MAX. means that address and data are cycling at maximum frequency of read cycles of 1/t_{CYC}.
   f = 0 means no inputs change.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Test Condition	IDT71B229S Min.	IDT71B229S Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	V

2996 tbl 08

ACCESS TIME AND CLOCK FREQUENCY EQUIVALENTS

R3000/1 Clock Frequency	71B229 Access Time
40 MHz	12 ns
33 MHz	16 ns
25 MHz	22 ns
20 MHz	28 ns

2996 tbl 09

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 5%

2996 tbl 10

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1A, 1B, 1C

2996 tbl 11

D

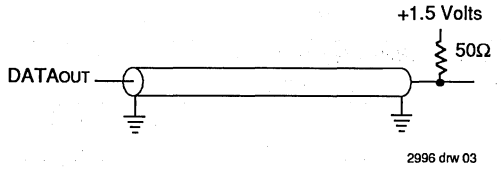
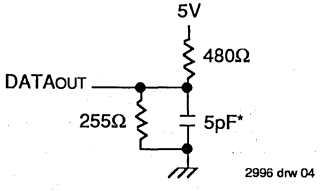


Figure 1A. AC Test Load



*Includes scope and jig.

Figure 1B. AC Test Load (for tOLZ & tOHZ)

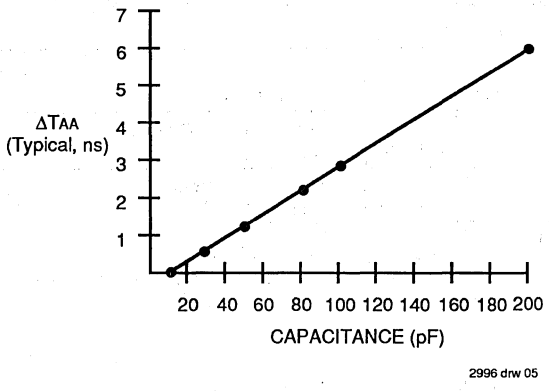
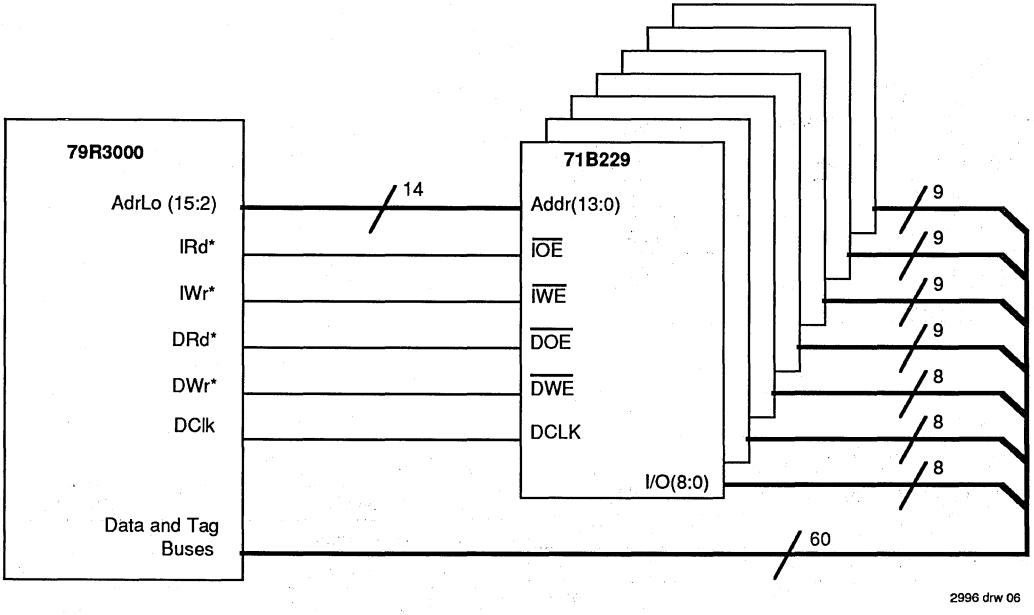


Figure 1C. Lumped Capacitive Load, Typical Derating Curve



NOTE:
1. Loading of the IRd, IWr, DRd and DWr signals should be split evenly between the pair of R3000 pins dedicated to each of these functions.

Figure 2. Example of Cache Memory System Block Diagram

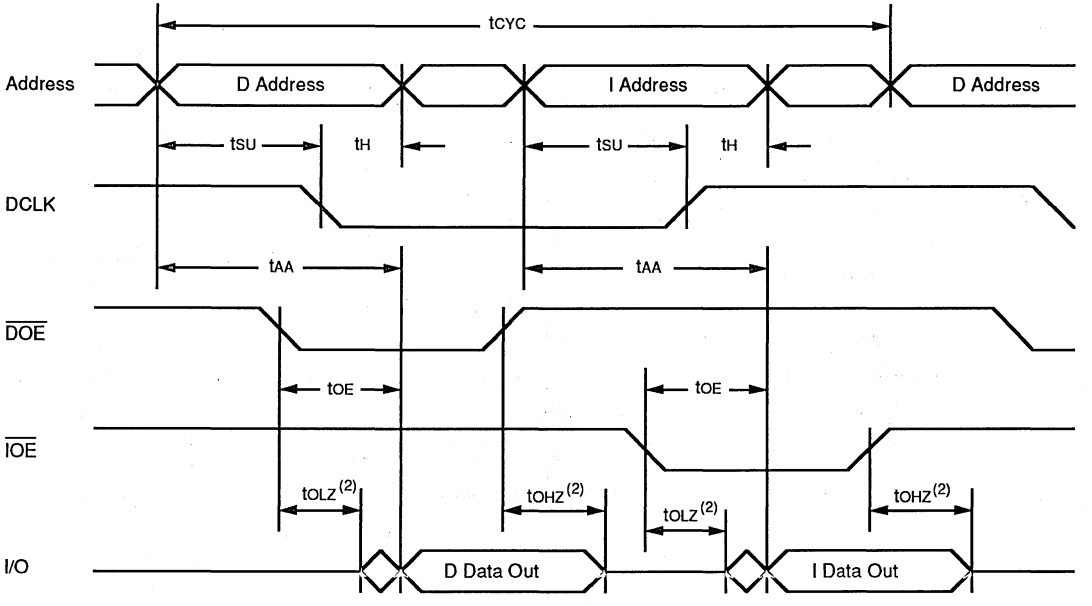
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 5%, All Temperature Ranges)

Symbol	Parameter	71B229S12		71B229S16		71B229S22		71B229S28		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tCYC	Read Cycle Time(1)	25	—	30	—	40	—	50	—	ns
tSU	Address Setup Time	6	—	8	—	11	—	14	—	ns
tH	Address Hold Time	3	—	3	—	4	—	6	—	ns
tAA	Address Access Time	—	12	—	16	—	22	—	28	ns
tOE	Output Enable Time	—	5	—	7	—	10	—	13	ns
tOLZ(2)	Output Enable to Output in Low Z	2	—	2	—	2	—	2	—	ns
tOHZ(2)	Output Disable to Output in High Z	2	5	2	6	2	8	2	10	ns

NOTES:
1. One cycle includes both a D bank read or write and an I bank read or write.
2. This parameter is guaranteed with the AC test load, Figure 1B,due to device characterization, but is not production tested.

2996 tbl 12

TIMING WAVEFORM OF READ CYCLES(1)



2996 drw 07

NOTES:
1. $\overline{DWE}$ and $\overline{IWE}$ must be high during read cycles.
2. The transition is measured ±200mV from steady state with load in Figure 1B.

D

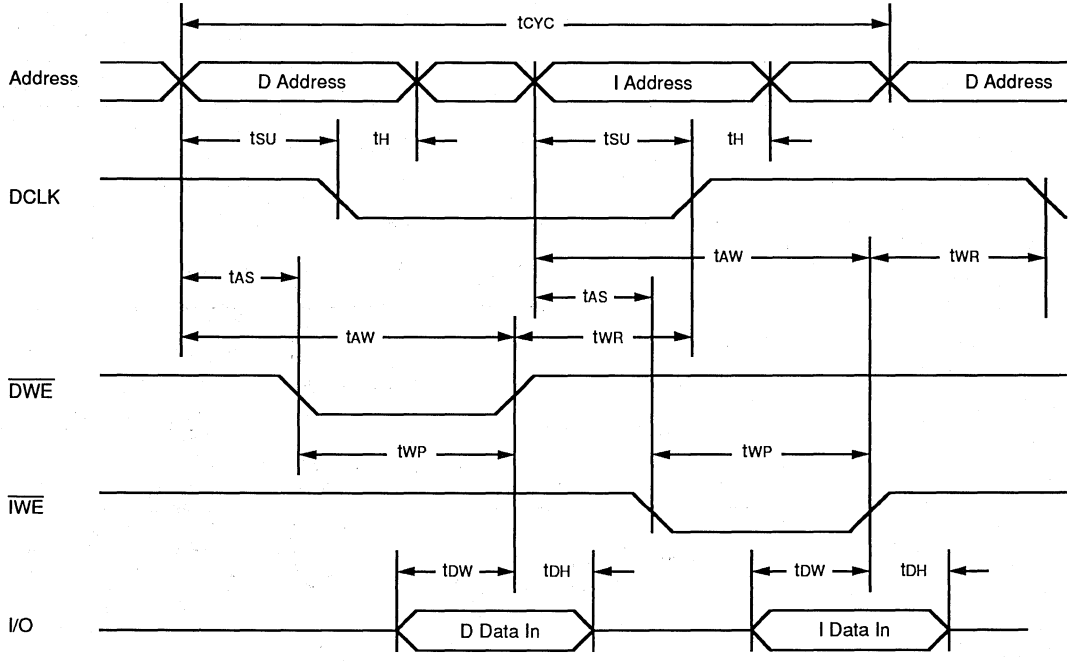
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 5%, All Temperature Ranges)

Symbol	Parameter	71B229S12		71B229S16		71B229S22		71B229S28		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle										
tCYC	Write Cycle Time(1)	25	—	30	—	40	—	50	—	ns
tSU	Address Setup Time	6	—	8	—	11	—	14	—	ns
tH	Address Hold Time	3	—	3	—	4	—	6	—	ns
tAW	Address to End of Write	18	—	20	—	22	—	28	—	ns
tAS	Address to Start of Write	5	—	5	—	5	—	5	—	ns
tWR	Write Recovery Time	-1	—	-1	—	-1	—	-1	—	ns
tWP	Write Pulse Width	10	—	13	—	16	—	20	—	ns
tDW	Data to Write Time Overlap	5.5	—	7	—	9	—	11	—	ns
tDH	Data Hold from Write Time	2	—	2	—	2	—	2	—	ns

NOTES:
1. One cycle includes both a D bank read or write and an I bank read or write.

2996 tbl 13

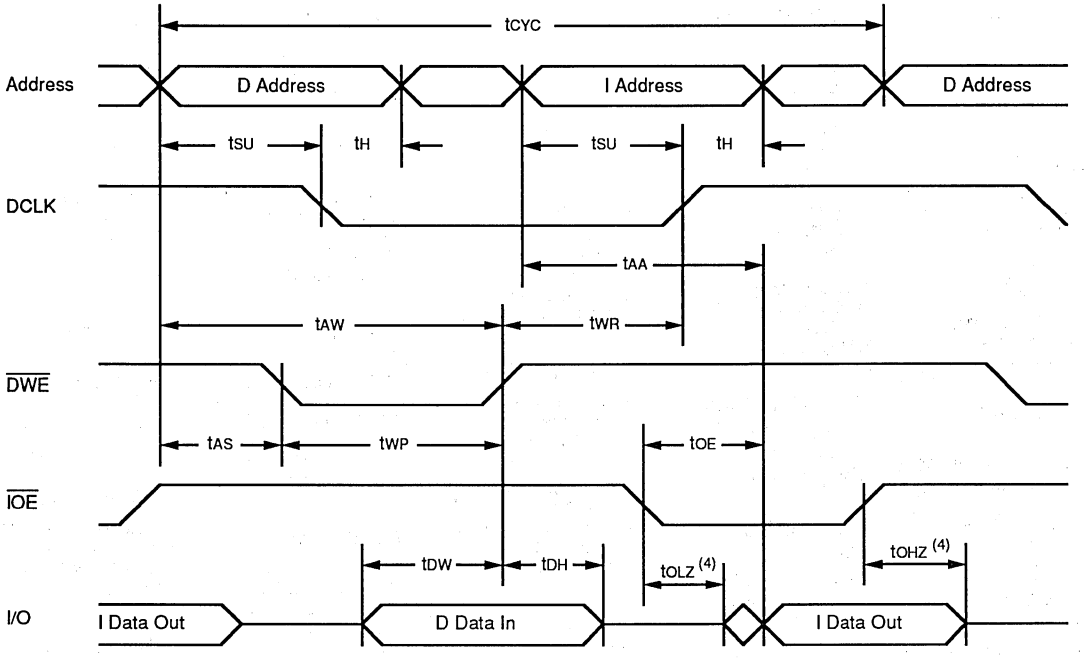
TIMING WAVEFORM OF WRITE CYCLES(1, 2)



NOTES:
1. $\overline{DOE}$ and $\overline{IOE}$ are high during write cycles.
2. $\overline{DWE}$ must be high or DCLK must be low during all address transitions. Likewise, $\overline{IWE}$ or DCLK must be high during all address transitions.

2996 drw 08

TIMING WAVEFORM OF MIXED READ AND WRITE CYCLES(1, 2, 3)



NOTE:
1. $\overline{DOE}$ and $\overline{IOE}$ are high during write cycles.
2. $\overline{DWE}$ must be high or DCLK must be low during all address transitions. Likewise, $\overline{IWE}$ or DCLK must be high during all address transitions.
3. $\overline{DWE}$ and $\overline{IWE}$ must be high during read cycles.
4. The transition is measured ±200mV from steady state with load in figure 1B.

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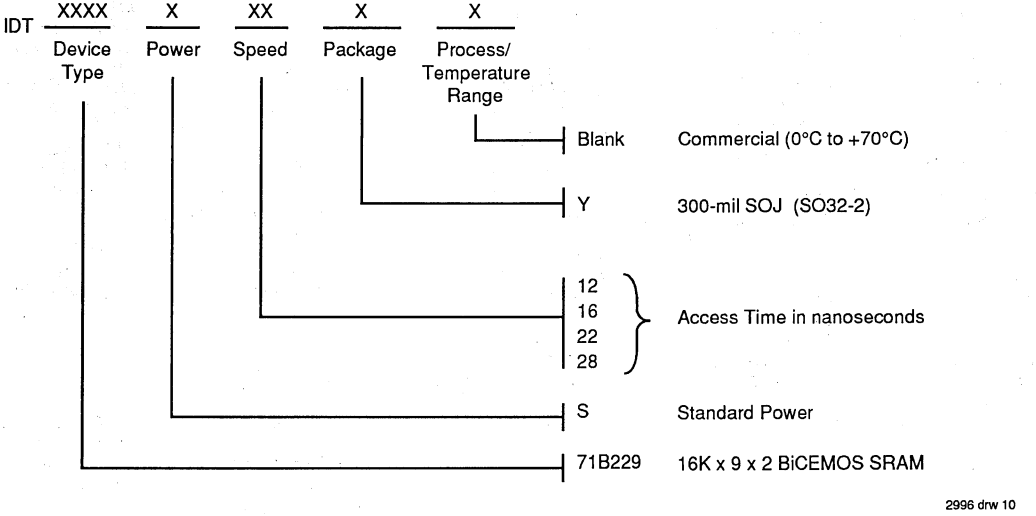

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