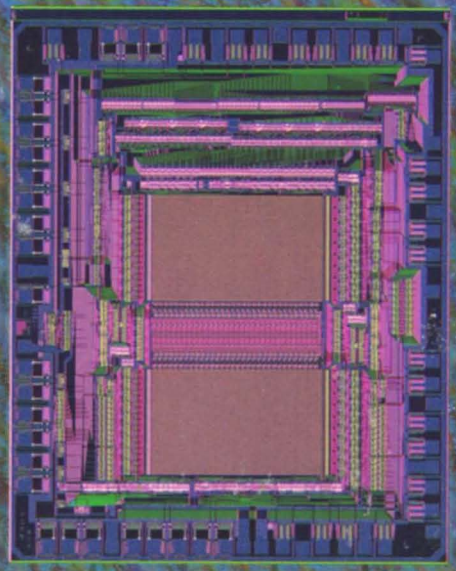
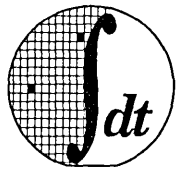
1990/91 DATABOOK

Specialized Memories



Integrated Device Technology, Inc.



Integrated Device Technology, Inc.

1990-91
SPECIALIZED MEMORIES
DATA BOOK

3236 Scott Boulevard, Santa Clara, California 95054
Telephone: (408) 727-6116 • TWX: 910-338-2070 • FAX: (408) 492-8674
Printed in U.S.A.

GENERAL INFORMATION

CONTENTS OVERVIEW

Historically, Integrated Device Technology has presented our product offerings entirely under one cover. For ease of use for our customers, we have divided the products into four separate data books — Logic, Specialized Memory, RISC and Static RAM.

IDT's 1990 Specialized Memories Data Book is comprised of new and revised data sheets and application notes for the ECL, FIFO, Speciality Memory and Subsystem product lines. Also included is a current, complete packaging section for all IDT product groups. This section will be updated in each subsequent data book with the latest available packages.

The Specialized Memories Data Book's Table of Contents contains a listing of the products contained in the 1990 Specialized Memories Data Book, as well as those products which we believe will be contained in the remaining three data books — the Logic Data Book is already in print, while RISC and SRAM will be published later in the year. The numbering scheme is slightly different from the past. The number in the bottom center of the page denotes the section number and the sequence of the data sheet within that section, (i.e. 5.5 would be the fifth data sheet in the fifth section). The number in the lower right hand corner is the page number of that particular data sheet.

Integrated Device Technology, a recognized leader in high-speed CMOS technology, produces a broad line of products, enabling us to provide a complete CMOS solution to designers of high-performance digital systems. Our products include industry standard devices, as well as products with speed, lower power, package and/or architectural benefits that allow the designer to achieve significantly improved system performance.

Use this book to find ordering information: Start with the Ordering Information chart at the back of each data sheet or the Cross Reference Guides (in Section 1), along with the Package Outline Index (page 4.2), to compose the complete IDT part number. Reference data on our Technology Capabilities and Quality Commitments are included in separate sections (2 and 3, respectively).

Use this book to find product data: Start with the Table of Contents, organized by product line (page 1.3), or with the Numeric Table of Contents across all product lines (page 1.4). These indexes will direct you to the page on which the complete technical data sheet can be found. Data sheets may be of the following type:

ADVANCE INFORMATION — contain initial descriptions, subject to change, for products that are in development, including features and block diagrams.

PRELIMINARY — contain descriptions for products soon to be, or recently, released to production, including features, pinouts and block diagrams. Timing data are based on simulation or initial characterization and are subject to change upon full characterization.

FINAL — contain minimum and maximum limits specified over the complete supply and temperature range for full production devices.

New products, product performance enhancements, additional package types and new product families are being introduced frequently. Please contact your local IDT sales representative to determine the latest device specifications, package types and product availability.

LIFE SUPPORT POLICY

Integrated Device Technology's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the manufacturer and an officer of IDT.

1. Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

1990-91 SPECIALIZED MEMORIES DATA BOOK
SUMMARY TABLE OF CONTENTS

SUMMARY TABLE OF CONTENTS (CONTINUED)

1990-91 SPECIALIZED MEMORIES DATA BOOK
TABLE OF CONTENTS

1990-91 SPECIALIZED MEMORIES DATA BOOK (CONTINUED)

APPLICATION AND TECHNICAL NOTES

FIFO Products Application Notes

1990-91 SPECIALIZED MEMORIES DATA BOOK (CONTINUED)

IDT SALES OFFICE, REPRESENTATIVE AND DISTRIBUTOR LOCATIONS

1990-91 LOGIC DATA BOOK

The following is a listing of the data sheets located in the 1990-91 Logic Data Book available under separate cover:

COMPLEX LOGIC PRODUCTS

STANDARD LOGIC PRODUCTS

PAGE

STANDARD LOGIC PRODUCTS (CONTINUED)

1990-91 LOGIC DATA BOOK (CONTINUED)

APPLICATION AND TECHNICAL NOTES

Complex Logic Products Technical Notes

1990-91 LOGIC DATA BOOK (CONTINUED)

RISC DATA BOOK

The following is a list of data sheets expected to be included in the RISC Data Book due for publication 4Q90. Until its release, please refer to your 1989 Data Book Supplement.

RISC MICROPROCESSOR PRODUCTS

RISC COMPONENTS

IDT79R3000A	Second Generation MIPS RISC CPU
IDT79R3001	IDT RISController™ CPU for Embedded and Real Time Applications
IDT79R3010A	Floating-Point Accelerator for the R3000A and R3001
IDT79R3020	RISC CPU Write Buffer for R3000A and R3001
IDT79R305x	Integrated RISC Microporccessor Family for Embedded Applications
IDT79R3720	Bus Exchanger for R305x Memory Systems
IDT79R3721	DRAM Controller for R305x Based Systems
IDT79R4000	Third Generation RISC Microprocessor
IDT79R4000SP	Third Generation RISC Microporcessor for Desktop Applications

RISC DEVELOPMENT SYSTEMS

RS1210	RISComputer™ Development System
RC2030	RISComputer™ Development System
RC3240	RISComputer™ Development System
RC3260	RISComputer™ Development System
M/2000	RISComputer™ Development System

RISC DEVELOPMENT SOFTWARE

3106 Ada	Ada Compiler
3120C-SRC (SPP)	System Programmer's Package
3123C-SRC (SPP/e)	System Programmer's Package/e
3178C-SRC (ASAPP)	Ada Stand-alone Programmer's Package

RISC SUBSYSTEM PRODUCTS

RISC CPU MODULES

IDT7RS101	R3000 Module w/64K I-Cache, 64K D-Cache, 4 Word Read Buffer and 1 Word Write Buffer
IDT7RS101F	R3000, R3010 Module w/64K I-Cache, 64K D-Cache, 4 Word Read Buffer and 1 Word Write Buffer
IDT7RS102	R3000 Module w/16K I-Cache, 16K D-Cache, 1 Word Read Buffer and 1 Word Write Buffer
IDT7RS102F	R3000, R3010 Module w/16K I-Cache, 16K D-Cache, 1 Word Read Buffer and 1 Word Write Buffer
IDT7RS103	R3000 Module w/16K I-Cache and 16K D-Cache
IDT7RS103F	R3000, R3010 Module w/16K I-Cache and16K D-Cache
IDT7RS104	R3001 Module w/ 128K I-Cache, 128K D-Cache, 1 Word Read Buffer and 1 Word Write Buffer
IDT7RS104F	R3001, R3010 Module w/128K I-Cache, 128K D-Cache, 1 Word Read Buffer and 1 Word Write Buffer
IDT7RS105	R3000 Module w/32K I-Cache, 16K D-Cache, 1 Word Read Buffer, 1 Word Write Buffer and IDT Bus
IDT7RS105F	R3000, R3010 Module w/32K I-Cache, 16K D-Cache, 1 Word Read Buffer, 1 Word Write Buffer and IDT Bus
IDT7RS107F	R3000, R3010 Module w/64K I-Cache, 64K D-Cache, 0R3020 and 1 Word Read Buffer

RISC TargetSystems

IDT7RS301	TargetSystem™ for IDT7RS101
IDT7RS302	TargetSystem™ for IDT7RS102
IDT7RS303	TargetSystem™ for IDT7RS103

RISC SUBSYSTEM PRODUCTS (CONTINUED)
RISC TargetSystems (CONTINUED)

IDT7RS304	TargetSystem™ for IDT7RS104
IDT7RS305	TargetSystem™ for IDT7RS105
IDT7RS307	TargetSystem™ for IDT7RS107

SUPPORT PRODUCTS

IDT7RS201	Nubus Board
IDT7RS202	Nubus Board, Supports Nubus Memory
IDT7RS203	Nubus Board, Supports Onboard Memory
IDT7RS340	System Board
IDT7RS341	Personality Board for IDT7RS101
IDT7RS342	Personality Board for IDT7RS102
IDT7RS343	Personality Board for IDT7RS103
IDT7RS347	Personality Board for IDT7RS107
IDT7RS353-B	JMI C-Executive™ Binary Code
IDT7RS353-MB	JMI C-Executive™ Maintenance for Binary Code
IDT7RS353-S	JMI C-Executive™ SourceCode
IDT7RS353-MS	JMI C-Executive™ Maintenance for Source Code
IDT7RS355-B	Floating Point Library Binary Code
IDT7RS355-MB	Floating Point Library Maintenance for Binary Code
IDT7RS355-S	Floating Point Library Source Code
IDT7RS355-MS	Floating Point Library Maintenance for Source Code
IDT7RS356-2B	R3000 C-Compiler Binary Code for 80286, 80386 IDT7RS356-2MB R3000 C-Compiler Maintenance for Binary Code for 80286, 80386 PC-DOS
IDT7RS356-3B	R3000 C-Compiler Binary Code for PC SCO XENIX
IDT7RS356-3MB	R3000 C-Compiler Maintenance for Binary Code SCO XENIX
IDT7RS357-1B	R3000 Macro Assembler Binary Code for 8086, 8088 PC-DOS
IDT7RS357-1MB	R3000 Macro Assembler Maintenance for Binary Code 8086, 8088
IDT7RS357-2B	R3000 Macro Assembler Binary Code for 80286, 80386 PC-DOS
IDT7RS357-2MB	R3000 Macro Assembler Maintenance for Binary Code 80286, 80386
IDT7RS357-3B	R3000 Macro Assembler Binary Code for PC SCO XENIX
IDT7RS357-3MB	R3000 Macro Assembler Maintenance for Binary Code SCO XENIX
IDT7RS361-B	IDT PROM Monitor Binary Code
IDT7RS361-MB	IDT PROM Monitor Maintenance for Binary Code
IDT7RS361-E	IDT PROM Monitor Binary Code — in 4 EPROMs
IDT7RS361-S	IDT PROM Monitor Source Code
IDT7RS361-MS	IDT PROM Monitor Maintenance for Source Code
IDT7RS363-1	R3000 PGA Breakout Board and HP 16500A Logic Analyzer Set-up Software
IDT7RS363-2	R3000 PGA Breakout Board and HP 16500A Logic Analyzer Set-up Software and 5 HP Adapters
IDT7RS364	HP 16500A Logic Analyzer Disassembler Software for 7RS300 Series TargetSystems™
IDT7RS365	R3000 Flatpack Version
IDT7RS366	R3001 PGA Version
IDT7RS382	R3000 Evaluation Board
IDT7RS383	R3001 Evaluation Board

MacStation™ DEVELOPMENT SYSTEM

IDT7RS501-1	MacStation™ Development System w/IDT7RS201 Nubus Board, IDT/ux and C-Compiler
IDT7RS501-1D	MacStation™ Development System Documentation
IDT7RS501-1M	MacStation™ Development System Maintenance
IDT7RS501-2	MacStation™ Development System w/150MB External Hard Disk, 40MB External Tape Drive, IDT7RS201 Nubus Board, IDT/ux and C-Compiler

RISC SUBSYSTEM PRODUCTS (CONTINUED)

MacStation™ DEVELOPMENT SYSTEM (CONTINUED)

IDT7RS501-3	Complete IDT7RS501 MacStation™ Development System w/MAC II Computer, 8MB RAM, 150MB Hard Disk, 40MB External Tape Drive, IDT7RS201 Nubus Board, IDT/ux and C-Compiler
IDT7RS501-4	4MB SIMM Module for MAC II
IDT7RS501-5	IDT7RS501 MacStation™ Development System w/150MB External Hard Disk, IDT7RS201 Nubus Board, IDT/ux and C-Compiler
IDT7RS501-6	IDT7RS501 MacStation™ Development System w/40MB External Tape Drive, IDT7RS201 Nubus Board, IDT/ux and C-Compiler
IDT7RS502-1	MacStation™ Development System w/IDT7RS202 Nubus Board, 8MB Nubus RAM Board, IDT/ux and C-Compiler
IDT7RS502-1D	MacStation™ Development System Documentation
IDT7RS502-1M	MacStation™ Development System Maintenance
IDT7RS502-2	IDT7RS502 MacStation™ Development System w/150MB External Hard Disk, 40MB External Tape Drive, IDT7RS202 Nubus Board, IDT/ux and C-Compiler
IDT7RS502-3	Complete IDT7RS502 MacStation™ Development System w/MAC II Computer, 8MB RAM, 150MB Hard Disk, 40MB External Tape Drive, IDT7RS202 Nubus Board, IDT/ux and C-Compiler
IDT7RS502-4	4MB SIMM Module for MAC II
IDT7RS502-5	IDT7RS502 MacStation™ Development System w/150MB External Hard Disk, IDT7RS202 Nubus Board, IDT/ux and C-Compiler
IDT7RS502-6	IDT7RS502 MacStation™ Development System w/40MB External Tape Drive, IDT7RS202 Nubus Board, IDT/ux and C-Compiler
IDT7RS503-1	MacStation™ Development System w/16MB RAM, IDT/ux and C-Compiler
IDT7RS503-1D	MacStation™ Development System Documentation
IDT7RS503-1M	MacStation™ Development System Maintenance
IDT7RS551-1B	IDT/ux — UNIX Operating System for MacStations™
IDT7RS571-1S	MIPS SPP for the MAC
IDT7RS572-1S	MIPS SPP/e for the MAC
IDT7RS573-1B	MIPS Fortran for the MAC
IDT7RS573-1MB	Maintenance for MIPS Fortran for the MAC

STATIC RAM DATA BOOK

The following is a list of data sheets expected to be included in the Static RAM Data Book due for publication 1Q91. Until its release, please refer to your 1989 Data Book Supplement.

STATIC RAM PRODUCTS

IDT6167	16K x 1 w/Power-Down
IDT6168	4K x 4 w/Power-Down
IDT6177	4K x 4 Cache-Tag w/Open Drain and Power-Down
IDT6178	4K x 4 Cache-Tag w/Power-Down
IDT61970	4K x 4 w/Output Enable and Power-Down
IDT71681	4K x 4 w/Separate I/O and Power-Down
IDT71682	4K x 4 w/Separate I/O and Power-Down
IDT6116	2K x 8 w/Power-Down
IDT7187	64K x 1 w/Power-Down
IDT6198	16K x 4 w/Output Enable and Power-Down
IDT7188	16K x 4 w/Power-Down
IDT7198	16K x 4 w/Output Enable, 2 Chip Selects and Power-Down
IDT61B98	16K x 4 BiCEMOS™ w/Output Enable
IDT71981	16K x 4 w/Separate I/O and Power Down
IDT71982	16K x 4 w/Separate I/O and Power Down
IDT71B88	16K x 4 BiCEMOS™
IDT71B98	16K x 4 BiCEMOS w/Output Enable and 2 Chip Selects
IDT7164	8K x 8 w/Power-Down
IDT7165	8K x 8 Resettable Power-Down
IDT7174	8K x 8 Cache-Tag w/Power-Down
IDT71B64	8K x 8 BiCEMOS™
IDT71B65	8K x 8 BiCEMOS™ Resettable
IDT71B74	8K x 8 BiCEMOS™ Cache-Tag
IDT7186	4K x 16 w/Power-Down
IDT71586	4K x 16 w/Address Latch and Power-Down
IDT7169	8K x 9 w/Power-Down
IDT71569	8K x 9 w/Address Latch and Power-Down
IDT71B569	8K x 9 BiCEMOS™ w/Address Latch
IDT71B69	8K x 9 BiCEMOS™
IDT71B79	8K x 9 BiCEMOS™ Cache-Tag
IDT71220	4K x 18 x 2 w/Single Address Latch and Power-Down
IDT71222	4K x 18 x 2 w/Dual Address Latches and Power-Down
IDT71270	4K x 18 x 2 Cache-Tag and Power-Down
IDT71257	256K x 1 w/Power-Down
IDT61298	64K x 4 w/Output Enable and Power-Down
IDT71258	64K x 4 w/Power-Down
IDT61B298	64K x 4 BiCEMOS™ w/Output Enable
IDT71281	64K x 4 w/Separate I/O and Power-Down
IDT71282	64K x 4 w/Separate I/O and Power-Down
IDT71B258	64K x 4 BiCEMOS™
IDT71256	32K x 8 w/Power-Down
IDT71B256	32K x 8 BiCEMOS™
IDT71B556	32K x 8 BiCEMOS™ w/Address Latch
IDT71259	32K x 9 w/Power-Down
IDT71509	32K x 9 w/Address Latch, Parity and Power-Down
IDT71559	32K x 9 w/Address Latch and Power-Down
IDT71589	32K x 9 Burst Mode w/Power-Down
IDT71027	1 Meg x 1 w/Power-Down
IDT71028	256K x 4 w/Power-Down
IDT71024	128K x 8 w/Power-Down

NUMERICAL TABLE OF CONTENTS

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NUMERICAL TABLE OF CONTENTS (CONTINUED)

NUMERICAL TABLE OF CONTENTS (CONTINUED)

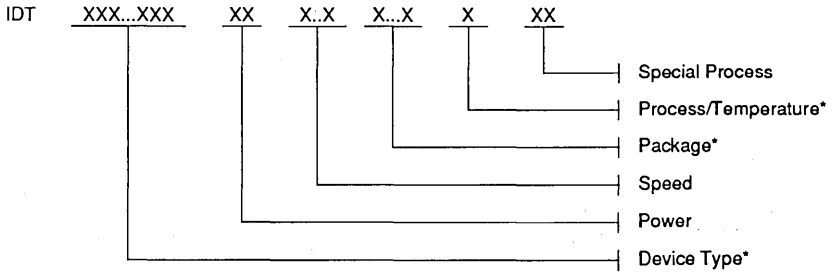
IDT PACKAGE MARKING DESCRIPTION

PART NUMBER DESCRIPTION

IDT's part number identifies the basic product, speed, power, package(s) available, operating temperature and processing grade. Each data sheet has a detailed description, using the part number, for ordering the proper product for the user's application. The part number is comprised of a series of alpha-numeric characters:

1. An "IDT" corporate identifier for Integrated Device Technology, Inc.
2. A basic device part number composed of alpha-numeric characters.
3. A device power identifier, composed of one or two alpha characters, is used to identify the power options. In most cases, the following alpha characters are used:
   "S" or "SA" is used for the standard product's power.
   "L" or "LA" is used for lower power than the standard product.
4. A device speed identifier, when applicable, is either alpha characters, such as "A" or "B", or numbers, such as 20 or 45. The speed units, depending on the product, are in nanoseconds or megahertz.
5. A package identifier, composed of one or two characters. The data sheet should be consulted to determine the packages available and the package identifiers for that particular product.
6. A temperature/process identifier. The product is available in either the commercial or military temperature range, processed to a commercial specification, or the product is available in the military temperature range with full compliance to MIL-STD-883. Many of IDT's products have burn-in included as part of the standard commercial process flow.
7. A special process identifier, composed of alpha characters, is used for products which require radiation enhancement (RE) or radiation tolerance (RT).

Example for Monolithic Devices:



* Field Identifier Applicable To All Products

2507 drw 01

ASSEMBLY LOCATION DESIGNATOR

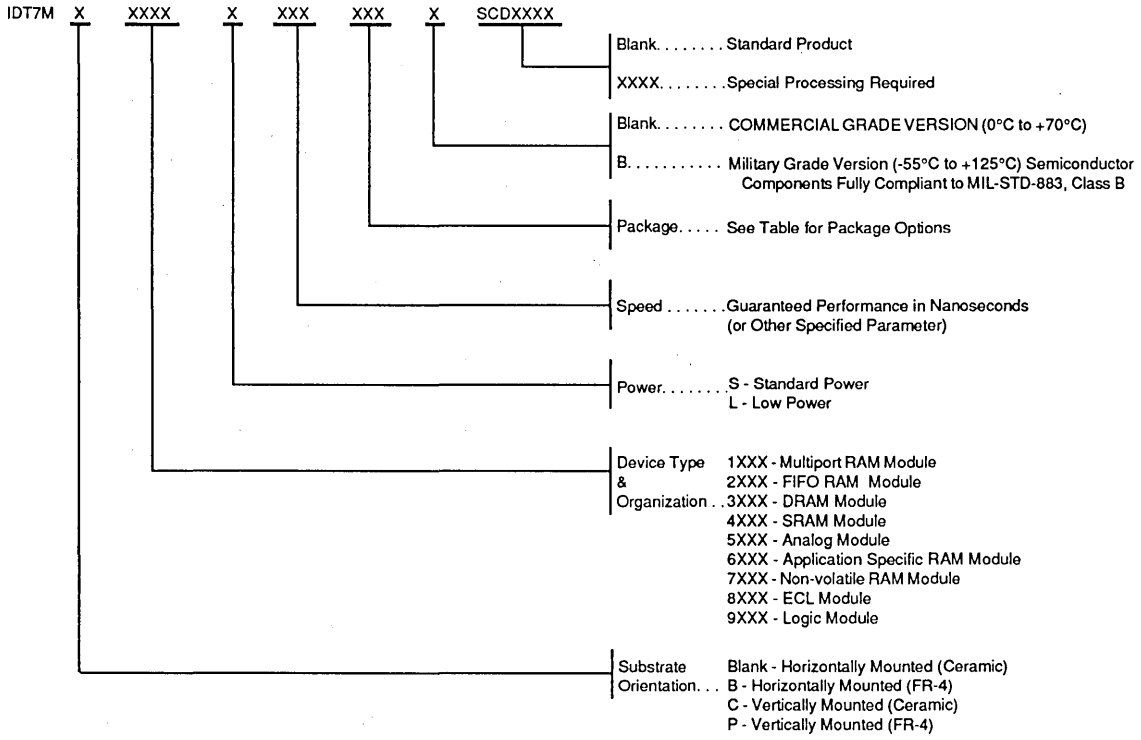
IDT uses various locations for assembly. These are identified by an alpha character in the last letter of the date code marked on the package. Presently, the assembly location alpha character is as follows:

A = Anam, Korea
I = USA
P = Penang, Malaysia

MIL-STD-883C COMPLIANT DESIGNATOR

IDT ships military products which are compliant to the latest revision of MIL-STD-883C. Such products are identified by a "C" designation on the package. The location of this designator is specified by internal documentation at IDT.

Example for Subsystem Modules:



Code	Substrate and Pin Type	Component Type
P	FR-4 DIP (Dual In-Line Package)	Plastic
C	CERAMIC DIP (Dual In-Line Package)	Ceramic
N	CERAMIC DIP (Dual In-Line Package)	Plastic
K	FR-4 QIP (Quad In-Line Package)	Plastic
CK	CERAMIC QIP (Quad In-Line Package)	Ceramic
H	FR-4 HIP (Hex In-Line Package)	Plastic
CH	CERAMIC QIP (Quad In-Line Package)	Ceramic
G	CERAMIC PGA (Pin Grid Array)	Ceramic
S	FR-4 SIP (Single In-Line Package)	Plastic
CS	CERAMIC SIP (Single In-Line Package)	Ceramic
V	FR-4 DSIP (Dual Single In-Line Package)	Plastic
CV	CERAMIC DSIP (Dual Single In-Line Package)	Ceramic
Z	FR-4 ZIP (Zip-zap In-Line Package)	Plastic
M	FR-4 SIMM (Single In-Line Memory Module)	Plastic

tbl 01

NOTES:
1. FR-4 is a multi-layered, glass filled epoxy laminate substrate.
2. Ceramic is a multi-layered, co-fired ceramic substrate.
3. Plastic refers to all surface mount devices available in various non-hermetically sealed packages (i.e. SOIC, SOJ, Flat Packs, etc.).
4. Ceramic refers to all surface mount devices available in various hermetically sealed packages (i.e. LCC, ceramic Flat Packs, etc.).

	CYPRESS-ASPEN	FUJITSU	HITACHI	NATIONAL	SYNERGY	IDT	Speed	Competitors' Package	Pinout
XXX492	**2KX9 BICMOS or BIPOLAR ECL-I/O SELF-TIMED SRAM (STRAM)**								
10K				NM4492W5			5	64 CERQUAD-.965	center power
				NM4492W7			7	64 CERQUAD-.965	center power
				NM4492W10		IDT10496RL10C†	10	64 CERQUAD-.965	center power
100K				NM100492W5			5	64 CERQUAD-.965	center power
				NM100492W7			7	64 CERQUAD-.965	center power
				NM100492W10		IDT100496RL10C†	10	64 CERQUAD-.965	center power
XXX484	**4KX4 BICMOS or BIPOLAR ECL-I/O SRAM**								
10K		MBM10A484-5F			SY10484-5FCF	**IDT10A484S5E**	5	28 CERPACK-.400	center power
		MBM10A484-5C			SY10484-5DCF	**IDT10A484S5C**	5	28 SB/CERDIP-.400	center power
	CY10E484-7JC					IDT10A484S7Y*	7	28 PLCC	center power
	CY10E484-7KC					**IDT10A484S7E**	7	28 CERPACK-.400	center power
	CY10E484-7DC					**IDT10A484S7C**	7	28 SB/CERDIP-.400	center power
		MBM10484A-8F			SY10484-8FC	**IDT10A484S8E**	8	28 CERPACK-.400	corner power
		MBM10484A-8C			SY10484-8DC	**IDT10484S8C**	8	28 SB/CERDIP-.400	corner power
		MBM10484A-10F			SY10484-10FC	**IDT10A484S10E**	10	28 CERPACK-.400	corner power
		MBM10484A-10C			SY10484-10DC	**IDT10484S10C**	10	28 SB/CERDIP-.400	corner power
		MBM10484-15F				**IDT10A484S10E**	15	28 CERPACK-.400	corner power
		MBM10484-15C				**IDT10484S10C**	15	28 SB/CERDIP-.400	corner power
100K					SY100484-5FCF	**IDT100A484S5E**	5	28 CERPACK-.400	center power
					SY100484-5DCF	**IDT100A484S5C**	5	28 SB/CERDIP-.400	center power
	CY100E484-7JC					IDT100A484S7Y*	7	28 PLCC	center power
	CY100E484-7KC					**IDT100A484S7E**	7	28 CERPACK-.400	center power
	CY100E484-7DC					**IDT100A484S7C**	7	28 SB/CERDIP-.400	center power
		MBM100484A-8F			SY100484-8FC	**IDT100484S8E**	8	28 CERPACK-.400	corner power
		MBM100484A-8C			SY100484-8DC	**IDT100484S8C**	8	28 SB/CERDIP-.400	corner power
	CY100E484-10JC					IDT100A484S10Y*	10	28 PLCC	center power
	CY100E484-10KC					**IDT100A484S10E**	10	28 CERPACK-.400	center power
	CY100E484-10DC					**IDT100A484S10C**	10	28 SB/CERDIP-.400	center power
		MBM100484A-10F			SY100484-10FC	**IDT100484S10E**	10	28 CERPACK-.400	corner power
		MBM100484A-10C			SY100484-10DC	**IDT100484S10C**	10	28 SB/CERDIP-.400	corner power
		MBM100484-15F				**IDT100484S15E**	15	28 CERPACK-.400	corner power
		MBM100484-15C				**IDT100484S15C**	15	28 SB/CERDIP-.400	corner power
101K		MBM101A484-5F			SY101484-5FCF	**IDT101A484S5E**	5	28 CERPACK-.400	center power
		MBM101A484-5C			SY101484-5DCF	**IDT101A484S5C**	5	28 SB/CERDIP-.400	center power
	CY1E484-7JC					IDT101A484S7Y*	7	28 PLCC	center power
	CY1E484-7KC					**IDT101A484S7E**	7	28 CERPACK-.400	center power
	CY1E484-7DC					**IDT101A484S7C**	7	28 SB/CERDIP-.400	center power

	CYPRESS-ASPEN	FUJITSU	HITACHI	NATIONAL	SYNERGY	IDT	Speed	Competitors' Package	Pinout
					SY101484-8FC	**IDT101484S8E**	8	28 CERPACK-.400	corner power
					SY101484-8DC	**IDT101484S8C**	8	28 SB/CERDIP-.400	corner power
					SY101484-10FC	**IDT101484S10E**	10	28 CERPACK-.400	corner power
					SY101484-10DC	**IDT101484S10C**	10	28 SB/CERDIP-.400	corner power
XXX486	**4KX4 BICMOS or BIPOLAR ECL-I/O SELF-TIMED SRAM (STRAM)**								
10K		MBM10486LL-13C				IDT10496LL13C†	13	28 SB/CERDIP-.400	center power
		MBM10486RR-13C				IDT10496RL12C†	13	28 SB/CERDIP-.400	center power
		MBM10486RL-13C				IDT10496RL12C†	13	28 SB/CERDIP-.400	center power
100K		MBM100486LL-13C				IDT100496LL13C†	13	28 SB/CERDIP-.400	center power
		MBM100486RR-13C				IDT100496RL12C†	13	28 SB/CERDIP-.400	center power
		MBM100486RL-13C				IDT100496RL12C†	13	28 SB/CERDIP-.400	center power
XXX494	**16Kx4 BICMOS or BIPOLAR ECL-I/O SRAM**								
10K	CY10E494-7JC					IDT10494S7Y*	7	28 PLCC	center power
	CY10E494-7KC	MBM10494-7F				IDT10494S7Y*	7	28 CERPACK-.400	center power
	CY10E494-7DC	MBM10494-7C				**IDT10494S7C**	7	28 SB/CERDIP-.400	center power
		MBM10494-8F				IDT10494S8Y*	8	28 CERPACK-.400	center power
		MBM10494-8C				**IDT10494S8C**	8	28 SB/CERDIP-.400	center power
	CY10E494-10JC		HM10494F-10			IDT10494S10Y*	10	28 PLCC	center power
	CY10E494-10KC		HM10494-10	NM10494F10		IDT10494S10Y*	10	28 CERPACK-.400	center power
	CY10E494-10DC			NM10494D10		**IDT10494S10C**	10	28 SB/CERDIP-.400	center power
	CY10E494-12JC					IDT10494S10Y*	12	28 PLCC	center power
	CY10E494-12KC			NM10494F12		IDT10494S10Y*	12	28 CERPACK-.400	center power
	CY10E494-12DC			NM10494D12		**IDT10494S10C**	12	28 SB/CERDIP-.400	center power
		MBM10C494-15F		NM10494F15		IDT10494S15Y*	15	28 CERPACK-.400	center power
		MBM10C494-15C		NM10494D15		**IDT10494S15C**	15	28 SB/CERDIP-.400	center power
100K			HM100494F-10			IDT100494S10Y*	10	28 CERPACK-.400	center power
			HM100494-10			**IDT100494S10C**	10	28 SB/CERDIP-.400	center power
	CY100E494-12JC					IDT100494S10Y*	12	28 PLCC	center power
	CY100E494-12KC		HM100494F-12			IDT100494S10Y*	12	28 CERPACK-.400	center power
	CY100E494-12VC					**IDT100494S10Y**	12	28 SOJ-.300	center power
	CY100E494-12DC		HM100494-12			**IDT100494S10C**	12	28 SB/CERDIP-.400	center power
		MBM100C494-15F		NM100494F15		IDT100494S15Y*	15	28 CERPACK-.400	center power
		MBM100C494-15C		NM100494D15		**IDT100494S15C**	15	28 SB/CERDIP-.400	center power
				NM100494F18		IDT100494S15Y*	18	28 CERPACK-.400	center power
				NM100494D18		**IDT100494S15C**	18	28 SB/CERDIP-.400	center power
101K	CY1E494-7JC					IDT101494S7Y*	7	28 PLCC	center power
	CY1E494-7KC	MBM101494-7F				IDT101494S7Y*	7	28 CERPACK-.400	center power
	CY1E494-7DC	MBM101494-7C				**IDT101494S7C**	7	28 SB/CERDIP-.400	center power

	CYPRESS-ASPEN	FUJITSU	HITACHI	NATIONAL	SYNERGY	IDT	Speed	Competitors' Package	Pinout
		MBM101494-8F				IDT101494S8Y*	8	28 CERPACK-.400	center power
		MBM101494-8C				**IDT101494S8C**	8	28 SB/CERDIP-.400	center power
	CY1E494-10JC					IDT101494S10Y*	10	28 PLCC	center power
	CY1E494-10KC		HM101494F-10			IDT101494S10Y*	10	28 CERPACK-.400	center power
	CY1E494-10DC		HM101494-10			**IDT101494S10C**	10	28 SB/CERDIP-.400	center power
			HM101494F-12			IDT101494S10Y*	12	28 CERPACK-.400	center power
			HM101494-12			**IDT101494S10C**	12	28 SB/CERDIP-.400	center power
XXX490	**64Kx1 BiCMOS or BIPOLAR ECL-I/O SRAM**								
10K						**IDT10490S8D**	8	22 CERDIP-.300	corner power
			HM10490-10			**IDT10490S10D**	10	22 CERDIP-.300	corner power
			HM10490-12			**IDT10490S12D**	12	22 CERDIP-.300	corner power
		MBM10490-15F				IDT10490S15Y*	15	22 FLATPACK-.300	corner power
		MBM10C490-15F				IDT10490S15Y*	15	22 FLATPACK-.300	corner power
		MBM10490-15C				**IDT10490S15D**	15	22 SB/CERDIP-.300	corner power
		MBM10C490-15C				**IDT10490S15D**	15	22 SB/CERDIP-.300	corner power
		MBM10490-25F				IDT10490S20Y*	25	22 FLATPACK-.300	corner power
		MBM10490-25C				**IDT10490S20D**	25	22 SB/CERDIP-.300	corner power
100K						**IDT100490S8D**	8	22 CERDIP-.300	corner power
			HM100490-10			**IDT100490S10D**	10	22 CERDIP-.300	corner power
			HM100490-12			**IDT100490S12D**	12	22 CERDIP-.300	corner power
		MBM100490-15F				IDT100490S15Y*	15	22 FLATPACK-.300	corner power
		MBM100C490-15F				IDT100490S15Y*	15	22 FLATPACK-.300	corner power
		MBM100490-15C				**IDT100490S15D**	15	22 SB/CERDIP-.300	corner power
		MBM100C490-15C				**IDT100490S15D**	15	22 SB/CERDIP-.300	corner power
		MBM100490-25F				IDT100490S20Y*	25	22 FLATPACK-.300	corner power
		MBM100490-25C				**IDT100490S20D**	25	22 SB/CERDIP-.300	corner power
101K						**IDT101490S8D**	8	22 CERDIP-.300	corner power
			HM101490-10			**IDT101490S10D**	10	22 CERDIP-.300	corner power
			HM101490-12			**IDT101490D12D**	12	22 CERDIP-.300	corner power
XXX504	**64Kx4 BiCMOS or BIPOLAR ECL-I/O SRAM**								
10K			HM10504F-10			IDT10504S10Y*	10	28 CERPACK-.400	center power
			HM10504F-12			IDT10504S12Y*	12	28 CERPACK-.400	center power
100K			HM100504F-10			IDT100504S10Y*	10	28 CERPACK-.400	center power
			HM100504F-12			IDT100504S12Y*	12	28 CERPACK-.400	center power
		MBM100C504-15F		NM100504F15			15	28 CERPACK-.400	center power
		MBM100C504-15C				**IDT100504S15C**	15	32 SB-.400	center power
				NM100504D15			15	28 SB-.400	corner power
				NM100504F18			18	28 CERPACK-.400	center power

	CYPRESS-ASPEN	FUJITSU	HITACHI	NATIONAL	SYNERGY	IDT	Speed	Competitors' Package	Pinout
				NM100504D18			18	28 SB-.400	corner power
101K			HM101504F-10			IDT101504S10Y*	10	32 CERPACK-.400	center power
			HM101504F-12			IDT101504S12Y*	12	32 CERPACK-.400	center power
				NM5104F12			12	28 CERPACK-.400	center power
				NM5104D12			12	28 SB-.400	corner power
				NM5104F15			15	28 CERPACK-.400	center power
				NM5104D15			15	28 SB-.400	corner power

NOTES:
1. **BOLD FACE TYPE** indicates exact replacement.
2. * Same function but in SOJ package; Flatpacks frequently have unique pinouts and do not cross between vendors.
3. † Not a direct replacement, but can be considered as alternative for new designs.

Integrated Device Technology, Inc.

FIFO
CROSS REFERENCE GUIDE

AMD	IDT
Am7200	IDT7200S/L
Am7200-25PC	25TP
Am7200-35PC	35TP
Am7200-50PC	50TP
Am7200-65PC	65TP
Am7200-80PC	80TP
Am7200-25DC	25D
Am7200-35DC	35D
Am7200-50DC	50D
Am7200-65DC	65D
Am7200-80DC	80D
Am7200-25RC	25TP
Am7200-35RC	35TP
Am7200-50RC	50TP
Am7200-65RC	65TP
Am7200-80RC	80TP
Am7200-25JC	25J
Am7200-35JC	35J
Am7200-50JC	50J
Am7200-65JC	65J
Am7200-80JC	80J
Am7200-40/BXA	40DB
Am7200-50/BXA	50DB
Am7200-65/BXA	65DB
Am7200-80/BXA	80DB
Am7201	IDT7201SA/LA
Am7201-25PC	25P
Am7201-35PC	35P
Am7201-50PC	50P
Am7201-65PC	65P
Am7201-80PC	80P
Am7201-25RC	25TP
Am7201-35RC	35TP
Am7201-50RC	50TP
Am7201-65RC	65TP
Am7201-80RC	80TP
Am7201-25JC	25J
Am7201-35JC	35J
Am7201-50JC	50J
Am7201-65JC	65J
Am7201-80JC	80J
Am7201-25DC	25D
Am7201-35DC	35D
Am7201-50DC	50D
Am7201-65DC	65D
Am7201-80DC	80D
Am7201-40/BXA	40DB
Am7201-50/BXA	50DB
Am7201-65/BXA	65DB
Am7201-80/BXA	80DB
Am7202	IDT7202SA/LA
Am7202-25PC	25P
Am7202-35PC	35P
Am7202-50PC	50P
Am7202-65PC	65P

AMD (CON'T.)	IDT
Am7202-80PC	80P
Am7202-25RC	25TP
Am7202-35RC	35TP
Am7202-50RC	50TP
Am7202-65RC	65TP
Am7202-80RC	80TP
Am7202-25JC	25J
Am7202-35JC	35J
Am7202-50JC	50J
Am7202-65JC	65J
Am7202-80JC	80J
Am7202-25DC	25D
Am7202-35DC	35D
Am7202-50DC	50D
Am7202-65DC	65D
Am7202-80DC	80D
Am7202-40/BXA	40DB
Am7202-50/BXA	50DB
Am7202-65/BXA	65DB
Am7202-80/BXA	80DB
Am7203	IDT7203S/L
Am7203-25PC	25P
Am7203-35PC	35P
Am7203-50PC	50P
Am7203-65PC	65P
Am7203-80PC	80P
Am7203-25RC	25TP
Am7203-35RC	35TP
Am7203-50RC	50TP
Am7203-65RC	65TP
Am7203-80RC	80TP
Am7203-25JC	25J
Am7203-35JC	35J
Am7203-50JC	50J
Am7203-65JC	65J
Am7203-80JC	80J
Am7203-35DC	35D
Am7203-50DC	50D
Am7203-65DC	65D
Am7203-80DC	80D
Am7203-40/BXA	40DB
Am7203-50/BXA	50DB
Am7203-65/BXA	65DB
Am7203-80/BXA	80DB
Am7204	IDT7204S/L
Am7204-25PC	25P
Am7204-35PC	35P
Am7204-50PC	50P
Am7204-65PC	65P
Am7204-80PC	80P
Am7204-25JC	25J
Am7204-35JC	35J
Am7204-50JC	50J
Am7204-65JC	65J

AMD (CON'T.)	IDT
Am7204-80JC	80J
Am7204-35DC	35D
Am7204-50DC	50D
Am7204-65DC	65D
Am7204-80DC	80D
Am7204-40/BXA	40DB
Am7204-50/BXA	50DB
Am7204-65/BXA	65DB
Am7204-80/BXA	80DB
67C401	IDT72401L
67C401-35N	35P
67C401-25N	25P
67C401-15N	15P
67C401-10N	10P
67C401-35J	35D
67C401-25J	25D
67C401-15J	15D
67C401-10J	10D
67401	
67401A-N	15P
67401-N	10P
67401A-J	15D
67401-J	10D
C67401	
C67401A-N	15P
C67401-N	10P
C67401A-J	15D
C67401-J	10D
57C401	
57C401-12J	15DB
57401	
57401A-J	10DB
57401-J	10DB
C57401	
C57401A-J	10DB
C57401-J	10DB
67C402	IDT72402L
67C402-35N	35P
67C402-25N	25P
67C402-15N	15P
67C402-10N	10P
67C402-35J	35D
67C402-25J	25D
67C402-15J	15D
67C402-10J	10D
67402	
67402A-N	15P
67402-N	10P
67402A-J	15D
67402-J	10D

AMD (Con't.)	IDT
C67402	
C67402A-N	15P
C67402-N	10P
C67402A-J	15D
C67402-J	10D
57C402	
57C402-12J	15DB
57402	
57402A-J	10DB
57402-J	10DB
C57402	
C57402A-J	10DB
C57402-J	10DB
67C4013	IDT72403L
67C4013-35N	35P
67C4013-25N	25P
67C4013-15N	15P
67C4013-10N	10P
67C4013-35J	35D
67C4013-25J	25D
67C4013-15J	15D
67C4013-10J	10D
57C4013	
57C4013-12J	15DB
67C4023	IDT72404L
67C4023-35N	35P
67C4023-25N	25P
67C4023-15N	15P
67C4023-10N	10P
67C4023-35J	35D
67C4023-25J	25D
67C4023-15J	15D
67C4023-10J	10D
57C4023	
57C4023-12J	15DB
67C4033	IDT72413L
67C4033-15N	25P
67C4033-10N	25P
67C4033-15J	25D
67C4033-10J	25D
67C413	
67C413-40N	45P
67C413-40J	45D
67413	
67413-25N	25P
67413A-35N	35P
67413-25J	25D
67413A-35J	35D
57C4033	
57C4033-12J	25DB

MOSEL	IDT
MS7200	IDT7200S/L
MS7200-25NC	25TP
MS7200-35NC	35TP
MS7200-50NC	50TP
MS7200-80NC	80TP
MS7200-25JC	25J
MS7200-35JC	35J
MS7200-50JC	50J
MS7200-80JC	80J
MS7200L-25NC	25TP
MS7200L-35NC	25TP
MS7200L-50NC	25TP
MS7200L-80NC	25TP
MS7200L-25JC	25J
MS7200L-35JC	35J
MS7200L-50JC	50J
MS7200L-80JC	80J
MS7201	IDT7201SA/LA
MS7201-50PC	50P
MS7201-65PC	65P
MS7201-80PC	80P
MS7201-120PC	120P
MS7201A	
MS7201A-25JC	25J
MS7201A-35JC	35J
MS7201A-50JC	50J
MS7201A-80JC	80J
MS7201A-25NC	25TP
MS7201A-35NC	35TP
MS7201A-50NC	50TP
MS7201A-80NC	80TP
MS7201A-25PC	25P
MS7201A-35PC	35P
MS7201A-50PC	50P
MS7201A-80PC	80P
MS7201AL-25JC	25J
MS7201AL-35JC	35J
MS7201AL-50JC	50J
MS7201AL-80JC	80J
MS7201AL-25NC	25TP
MS7201AL-35NC	35TP
MS7201AL-50NC	50TP
MS7201AL-80NC	80TP
MS7201AL-25PC	25P
MS7201AL-35PC	35P
MS7201AL-50NC	50P
MS7201AL-80PC	80P
MS7202A	IDT7202SA/LA
MS7202A-25JC	25J
MS7202A-35JC	35J
MS7202A-50JC	50J
MS7202A-80JC	80J
MS7202A-25NC	25TP
MS7202A-35NC	35TP
MS7202A-50NC	50TP
MS7202A-80NC	80TP
MS7202A-25PC	25P
MS7202A-35PC	35P
MS7202A-50PC	50P
MS7202A-80PC	80P
MS7202AL-25JC	25J
MS7202AL-35JC	35J
MS7202AL-50JC	50J

MOSEL (Con't.)	IDT
MS7202AL-80JC	80J
MS7202AL-25NC	25TP
MS7202AL-35NC	35TP
MS7202AL-50NC	50TP
MS7202AL-80NC	80TP
MS7202AL-25PC	25P
MS7202AL-35PC	35P
MS7202AL-50PC	50P
MS7202AL-80PC	80P
MS7203	IDT7203S/L
MS7203-35JC	35J
MS7203-50JC	50J
MS7203-80JC	80J
MS7203-35NC	35TP
MS7203-50NC	50TP
MS7203-80NC	80TP
MS7203-35PC	35P
MS7203-50PC	50P
MS7203-80PC	80P
MS7203L-35JC	35J
MS7203L-50JC	50J
MS7203L-80JC	80J
MS7203L-35NC	35TP
MS7203L-50NC	50TP
MS7203L-80NC	80TP
MS7203L-35PC	35P
MS7203L-50PC	50P
MS7203L-80PC	80P

SGS	IDT
MK4501	IDT7201SA/LA
MK4501N-65	65P
MK4501N-80	80P
MK4501N-10	80P
MK4501N-12	120P
MK4501N-15	120P
MK4501N-20	120P
MK4501K-65	65J
MK4501K-80	80J
MK4501K-10	80J
MK4501K-12	120J
MK4501K-15	120J
MK4501K-20	120J
MK4503	IDT7203S/L
MK4503N-50	50P
MK4503N-65	65P
MK4503N-80	80P
MK4503N-10	80P
MK4503N-12	120P
MK4503N-15	120P
MK4503N-20	120P
MK4503K-50	50J
MK4503K-65	65J
MK4503K-80	80J
MK4503K-10	80J
MK4503K-12	120J
MK4503K-15	120J
MK4503K-20	120J

DALLAS	IDT
DS2009	IDT7201SA/LA
DS2009-35	35P
DS2009-50	50P
DS2009-65	65P
DS2009-80	80P
DS2009R-35	35J
DS2009R-50	50J
DS2009R-65	65J
DS2009R-80	80J
DS2010	IDT7202SA/LA
DS2010-35	35P
DS2010-50	50P
DS2010-65	65P
DS2010-80	80P
DS2010R-35	35J
DS2010R-50	50J
DS2010R-65	65J
DS2010R-80	80J
DS2011	IDT7203S/L
DS2011-35	35P
DS2011-50	50P
DS2011-65	65P
DS2011-80	80P
DS2011R-35	35J
DS2011R-50	50J
DS2011R-65	65J
DS2011R-80	80J

SAMSUNG	IDT
KM75C01A	IDT7201SA/LA
KM75C01AP-25	25P
KM75C01AP-35	35P
KM75C01AP-50	50P
KM75C01AP-80	80P
KM75C01AJ-25	25J
KM75C01AJ-35	35J
KM75C01AJ-50	50J
KM75C01AJ-80	80J
KM75C01AN-25	25TP
KM75C01AN-35	35TP
KM75C01AN-50	50TP
KM75C01AN-80	80TP
KM75C02A	IDT7202SA/LA
KM75C02AP-25	25P
KM75C02AP-35	35P
KM75C02AP-50	50P
KM75C02AP-80	80P
KM75C02AJ-25	25J
KM75C02AJ-35	35J
KM75C02AJ-50	50J
KM75C02AJ-80	80J
KM75C02AN-25	25TP
KM75C02AN-35	35TP
KM75C02AN-50	50TP
KM75C02AN-80	80TP
KM75C03A	IDT7203SA/LA
KM75C03AP-25	25P
KM75C03AP-35	35P
KM75C03AP-50	50P
KM75C03AP-80	80P

SAMSUNG (Con't.)	IDT
KM75C03AJ-25	25J
KM75C03AJ-35	35J
KM75C03AJ-50	50J
KM75C03AJ-80	80J
KM75C03AN-25	25TP
KM75C03AN-35	35TP
KM75C03AN-50	50TP
KM75C03AN-80	80TP
SHARP	**IDT**
LH5495	IDT7200L
LH5495D-25	25TP
LH5495D-35	35TP
LH5495U-25	25J
LH5495U-35	35J
LH5496	IDT7201LA
LH5496-25	25P
LH5496-35	35P
LH5496-50	50P
LH5496D-20	20TP
LH5496D-25	25TP
LH5496D-35	35TP
LH5496D-50	50TP
LH5496U-20	20J
LH5496U-25	25J
LH5496U-35	35J
LH5497	IDT7202LA
LH5497-25	25P
LH5497-35	35P
LH5497-50	50P
LH5497D-25	25TP
LH5497D-35	35TP
LH5497D-50	50TP
LH5497U-25	25J
LH5497U-35	35J
LH5498	IDT7203L
LH5498-20	20P
LH5498-25	25P
LH5498-35	35P
LH5498-50	50P
LH5498D-20	20TP
LH5498D-25	25TP
LH5498D-35	35TP
LH5498D-50	50TP
LH5498U-20	20J
LH5498U-25	25J
LH5498U-35	35J
LH5499	IDT7204L
LH5499-20	20P
LH5499-25	25P
LH5499-35	35P
LH5499-50	50P
LH5499U-20	20J
LH5499U-25	25J
LH5499-U35	35J
TI	**IDT**
54/74ALS236	IDT72401L
SN74ALS236-30N	35P
SN54ALS236-25J	25DB

TI (Con't.)	IDT
54/74ALS234	IDT72403L
SN74ALS234-30N	35P
SN54ALS234-25J	25DB
54/74ALS235	IDT72413L
SN74ALS235-25N	25P
SN74ALS235-25DW	25SO
SN54ALS235-20J	25DB

CYPRESS	IDT
CY7C420	IDT7201SA/LA
CY7C420-30PC	25P
CY7C420-40PC	35P
CY7C420-65PC	65P
CY7C420-30DC	25D
CY7C420-40DC	35D
CY7C420-65DC	65D
CY7C420-30DMB	30DB
CY7C420-40DMB	40DB
CY7C420-65DMB	65DB
CY7C421	
CY7C421-30PC	25TP
CY7C421-40PC	35TP
CY7C421-65PC	65TP
CY7C421-30JC	25J
CY7C421-40JC	35J
CY7C421-65JC	65J
CY7C421-30VC	25Y
CY7C421-40VC	35Y
CY7C421-65VC	65Y
CY7C421-30DC	25TC
CY7C421-40DC	35TC
CY7C421-65DC	65TC
CY7C421-30DMB	30TCB
CY7C421-40DMB	40TCB
CY7C421-65DMB	65TCB
CY7C421-30LMB	30LB
CY7C421-40LMB	40LB
CY7C421-65LMB	65LB
CY7C424	IDT7202SA/LA
CY7C424-30PC	25P
CY7C424-40PC	35P
CY7C424-65PC	65P
CY7C424-30DC	25D
CY7C424-40DC	35D
CY7C424-65DC	65D
CY7C424-30DMB	30DB
CY7C424-40DMB	40DB
CY7C424-65DMB	65DB
CY7C425	
CY7C425-30PC	25TP
CY7C425-40PC	35TP
CY7C425-65PC	65TP
CY7C425-30JC	25J
CY7C425-40JC	35J
CY7C425-65JC	65J
CY7C425-30VC	25Y
CY7C425-40VC	35Y
CY7C425-65VC	65Y
CY7C425-30DC	25TC
CY7C425-40DC	35TC

CYPRESS (Con't.)	IDT
CY7C425-65DC	65TC
CY7C425-30DMB	30TCB
CY7C425-40DMB	40TCB
CY7C425-65DMB	65TCB
CY7C425-30LMB	30LB
CY7C425-40LMB	40LB
CY7C425-65LMB	65LB
CY7C428	IDT7203S/L
CY7C428-20PC	20P
CY7C428-25PC	25P
CY7C428-30PC	25P
CY7C428-40PC	35P
CY7C428-65PC	65P
CY7C428-20DC	20D
CY7C428-25DC	25D
CY7C428-30DC	25D
CY7C428-40DC	35D
CY7C428-65DC	65D
CY7C428-25DMB	20DB
CY7C428-30DMB	30DB
CY7C428-40DMB	40DB
CY7C428-65DMB	65DB
CY7C429	
CY7C429-20PC	20TP
CY7C429-25PC	25TP
CY7C429-30PC	25TP
CY7C429-40PC	35TP
CY7C429-65PC	65TP
CY7C429-20JC	20J
CY7C429-25JC	25J
CY7C429-30JC	25J
CY7C429-40JC	35J
CY7C429-65JC	65J
CY7C429-20DC	20TC
CY7C429-25DC	25TC
CY7C429-30DC	25TC
CY7C429-40DC	35TC
CY7C429-65DC	65TC
CY7C429-20VC	20Y
CY7C429-25VC	25Y
CY7C429-30VC	30Y
CY7C429-40VC	40Y
CY7C429-65VC	65Y
CY7C429-25DMB	20TCB
CY7C429-30DMB	30TCB
CY7C429-40DMB	40TCB
CY7C429-65DMB	65TCB
CY7C432/433	IDT7204S
CY7C432-25PC	25P
CY7C432-30PC	25P
CY7C432-40PC	35P
CY7C432-65PC	65P
CY7C432-25DC	25D
CY7C432-30DC	25D
CY7C432-40DC	35D
CY7C432-65DC	65D
CY7C432-25DMB	25DB
CY7C432-30DMB	30DB
CY7C432-40DMB	40DB
CY7C432-65DMB	65DB

CYPRESS (Con't.)	IDT
CY7C433	
CY7C433-25PC	25TP
CY7C433-30PC	25TP
CY7C433-40PC	35TP
CY7C433-65PC	65TP
CY7C433-25VC	25Y
CY7C433-30VC	35Y
CY7C433-40VC	40Y
CY7C432/433	IDT7204S
CY7C433-65VC	65Y
CY7C433-25JC	25J
CY7C433-30JC	25J
CY7C433-40JC	35J
CY7C433-65JC	65J
CY7C433-30DMB	30TCB
CY7C433-40DMB	40TCB
CY7C433-65DMB	65TCB
CY7C433-30LMB	30LB
CY7C433-40LMB	40LB
CY7C433-65LMB	65LB
CY3341	IDT72401L
CY3341-2PC	10P
CY3341PC	10P
CY3341-2DC	10D
CY3341DC	10D
CY3341-2DMB	10DB
CY3341DMB	10DB
CY7C401	
CY7C401-25PC	25P
CY7C401-15PC	15P
CY7C401-10PC	10P
CY7C401-5PC	10P
CY7C401-25DC	25D
CY7C401-15DC	15D
CY7C401-10DC	10D
CY7C401-5DC	10D
CY7C401-25DMB	25DB
CY7C401-15DMB	15DB
CY7C401-10DMB	10DB
CY7C402	IDT72402L
CY7C402-25PC	25P
CY7C402-15PC	15P
CY7C402-10PC	10P
CY7C402-5PC	10P
CY7C402-25DC	25D
CY7C402-15DC	15D
CY7C402-10DC	10D
CY7C402-5DC	10D
CY7C402-25DMB	25DB
CY7C402-15DMB	15DB
CY7C402-10DMB	10DB
CY7C403	IDT72403L
CY7C403-25PC	25P
CY7C403-15PC	15P
CY7C403-10PC	10P
CY7C403-25DC	25D
CY7C403-15DC	15D
CY7C403-10DC	10D

CYPRESS (Con't.)	IDT
CY7C403-25DMB	25DB
CY7C403-15DMB	15DB
CY7C403-10DMB	10DB
CY7C404	IDT72404L
CY7C404-25PC	25P
CY7C404-15PC	15P
CY7C404-10PC	10P
CY7C404-25DC	25D
CY7C404-15DC	15D

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IDT	CYPRESS	AMD	VLSI
IDT7130SA35P	CY7C130-35PC		
IDT7130SA35C	CY7C130-35DC		
IDT7130SA35L48	CY7C130-35LC		
IDT7130SA35L52	CY7C131-35LC		
IDT7130SA35J	CY7C131-35JC		
IDT7130SA35F			
IDT7130SA45P	CY7C130-45PC		
IDT7130SA45C	CY7C130-45DC		
IDT7130SA45L48	CY7C130-45LC		
IDT7130SA45L52	CY7C131-45LC		
IDT7130SA45J	CY7C131-45JC		
IDT7130SA45F			
IDT7130SA45CB	CY7C130-45DMB		
IDT7130SA45L48B	CY7C130-45LMB		
IDT7130SA45L52B	CY7C131-45LMB		
IDT7130SA45FB			
IDT7130SA55P	CY7C130-55PC	AM2130-55PC	
IDT7130SA55C	CY7C130-55DC	AM2130-55DC	
IDT7130SA55L48	CY7C130-55LC		
IDT7130SA55L52	CY7C131-55LC	AM2130-55LC	
IDT7130SA55J	CY7C131-55JC	AM2130-55JC	
IDT7130SA55F			
IDT7130SA55CB	CY7C130-55DMB		
IDT7130SA55L48B	CY7C130-55LMB		
IDT7130SA55L52B	CY7C131-55LMB		
IDT7130SA55FB			
IDT7130SA70P		AM2130-70PC	
IDT7130SA70C		AM2130-70DC	
IDT7130SA70L48			
IDT7130SA70L52		AM2130-70LC	
IDT7130SA70J		AM2130-70JC	
IDT7130SA70F			
IDT7130SA70CB		AM2130-70/BXC	
IDT7130SA70L48B			
IDT7130SA70L52B			
IDT7130SA70FB			
IDT7130SA90P			
IDT7130SA90C			
IDT7130SA90L48			
IDT7130SA90L52			
IDT7130SA90J			
IDT7130SA90F			

IDT	CYPRESS	AMD	VLSI
IDT7130SA90CB			
IDT7130SA90L48B			
IDT7130SA90L52B			
IDT7130SA90FB			
IDT7130SA100P		AM2130-10PC	
IDT7130SA100C		AM2130-10DC	
IDT7130SA100L48			
IDT7130SA100L52		AM2130-10LC	
IDT7130SA100J		AM2130-10JC	
IDT7130SA100F			
IDT7130SA100CB		AM2130-10/BXC	
IDT7130SA100L48B			
IDT7130SA100L52B			
IDT7130SA100FB			
IDT7130SA120CB		AM2130-12/BXC	
IDT7130SA120L48B			
IDT7130SA120L52B			
IDT7130SA120FB			
IDT7130LA35P			
IDT7130LA35C			
IDT7130LA35L48			
IDT7130LA35L52			
IDT7130LA35J			
IDT7130LA35F			
IDT7130LA45P			
IDT7130LA45C			
IDT7130LA45L48			
IDT7130LA45L52			
IDT7130LA45J			
IDT7130LA45F			
IDT7130LA45CB			
IDT7130LA45L48B			
IDT7130LA45L52B			
IDT7130LA45FB			
IDT7130LA55P			
IDT7130LA55C			
IDT7130LA55L48			
IDT7130LA55L52			
IDT7130LA55J			
IDT7130LA55F			
IDT7130LA55CB			
IDT7130LA55L48B			
IDT7130LA55L52B			
IDT7130LA55FB			
IDT7130LA70P			

IDT	CYPRESS	AMD	VLSI
IDT7130LA70C			
IDT7130LA70L48			
IDT7130LA70L52			
IDT7130LA70J			
IDT7130LA70F			
IDT7130LA70CB			
IDT7130LA70L48B			
IDT7130LA70L52B			
IDT7130LA70FB			
IDT7130LA90P			
IDT7130LA90C			
IDT7130LA90L48			
IDT7130LA90L52			
IDT7130LA90J			
IDT7130LA90F			
IDT7130LA90CB			
IDT7130LA90L48B			
IDT7130LA90L52B			
IDT7130LA90FB			
IDT7130LA100P			
IDT7130LA100C			
IDT7130LA100L48			
IDT7130LA100L52			
IDT7130LA100J			
IDT7130LA100F			
IDT7130LA100CB			
IDT7130LA100L48B			
IDT7130LA100L52B			
IDT7130LA100FB			
IDT7130LA120CB			
IDT7130LA120L48B			
IDT7130LA120L52B			
IDT7130LA120FB			
IDT7132SA35P	CY7C132-35PC		VT7132-35PC
IDT7132SA35C	CY7C132-35DC		
IDT7132SA35L48	CY7C132-35LC		
IDT7132SA35L52			
IDT7132SA35J			VT7132-35QC
IDT7132SA35F			
IDT7132SA45P	CY7C132-45PC		VT7132-45PC
IDT7132SA45C	CY7C132-45DC		
IDT7132SA45L48	CY7C132-45LC		
IDT7132SA45L52			
IDT7132SA45J			VT7132-45QC
IDT7132SA45F			

IDT	CYPRESS	AMD	VLSI
IDT7132SA45CB	CY7C132-45DMB		
IDT7132SA45L48B	CY7C132-45LMB		
IDT7132SA45L52B			
IDT7132SA45FB			
IDT7132SA55P	CY7C132-55PC		VT7132-55PC
IDT7132SA55C	CY7C132-55DC		
IDT7132SA55L48	CY7C132-55LC		
IDT7132SA55L52			
IDT7132SA55J			VT7132-55QC
IDT7132SA55F			
IDT7132SA55CB	CY7C132-55DMB		
IDT7132SA55L48B	CY7C132-55LMB		
IDT7132SA55L52B			
IDT7132SA55FB			
IDT7132SA70P			VT7132-70PC
IDT7132SA70C			
IDT7132SA70L48			
IDT7132SA70L52			
IDT7132SA70J			VT7132-70QC
IDT7132SA70F			
IDT7132SA70CB			
IDT7132SA70L48B			
IDT7132SA70L52B			
IDT7132SA70FB			
IDT7132SA90P			VT7132-90PC
IDT7132SA90C			
IDT7132SA90L48			
IDT7132SA90L52			
IDT7132SA90J			VT7132-90QC
IDT7132SA90F			
IDT7132SA90CB			
IDT7132SA90L48B			
IDT7132SA90L52B			
IDT7132SA90FB			
IDT7132SA100P			
IDT7132SA100C			
IDT7132SA100L48			
IDT7132SA100L52			
IDT7132SA100J			
IDT7132SA100F			
IDT7132SA100CB			
IDT7132SA100L48B			
IDT7132SA100L52B			
IDT7132SA100FB			
IDT7132SA120CB			
IDT7132SA120L48B			

IDT	CYPRESS	AMD	VLSI
IDT7132SA120L52B			
IDT7132SA120FB			
IDT7132LA35P			
IDT7132LA35C			
IDT7132LA35L48			
IDT7132LA35L52			
IDT7132LA35J			
IDT7132LA35F			
IDT7132LA45P			
IDT7132LA45C			
IDT7132LA45L48			
IDT7132LA45L52			
IDT7132LA45J			
IDT7132LA45F			
IDT7132LA45CB			
IDT7132LA45L48B			
IDT7132LA45L52B			
IDT7132LA45FB			
IDT7132LA55P			
IDT7132LA55C			
IDT7132LA55L48			
IDT7132LA55L52			
IDT7132LA55J			
IDT7132LA55F			
IDT7132LA55CB			
IDT7132LA55L48B			
IDT7132LA55L52B			
IDT7132LA55FB			
IDT7132LA70P			
IDT7132LA70C			
IDT7132LA70L48			
IDT7132LA70L52			
IDT7132LA70J			
IDT7132LA70F			
IDT7132LA70CB			
IDT7132LA70L48B			
IDT7132LA70L52B			
IDT7132LA70FB			
IDT7132LA90P			
IDT7132LA90C			
IDT7132LA90L48			
IDT7132LA90L52			
IDT7132LA90J			
IDT7132LA90F			
IDT7132LA90CB			

IDT	CYPRESS	AMD	VLSI
IDT7132LA90L48B			
IDT7132LA90L52B			
IDT7132LA90FB			
IDT7132LA100P			
IDT7132LA100C			
IDT7132LA100L48			
IDT7132LA100L52			
IDT7132LA100J			
IDT7132LA100F			
IDT7132LA100CB			
IDT7132LA100L48B			
IDT7132LA100L52B			
IDT7132LA100FB			
IDT7132LA120CB			
IDT7132LA120L48B			
IDT7132LA120L52B			
IDT7132LA120FB			
IDT71321SA35J	CY7C136-35JC		VT71321-35QC
IDT71321SA35L52	CY7C136-35LC		
IDT71321SA45J	CY7C136-45JC		VT71321-45QC
IDT71321SA45L52	CY7C136-45LC		
IDT71321SA45L52B	CY7C136-45LMB		
IDT71321SA55J	CY7C136-55JC		
IDT71321SA55L52	CY7C136-55LC		
IDT71321SA55L52B	CY7C136-55LMB		
IDT71321SA70L52B			
IDT71321LA35J			
IDT71321LA35L52			
IDT71321LA45J			
IDT71321LA45L52			
IDT71321LA45L52B			
IDT71321LA55J			
IDT71321LA55L52			
IDT71321LA55L52B			
IDT71321LA70L52B			
IDT71322S35P			
IDT71322S35C			
IDT71322S35J			
IDT71322S35L48			
IDT71322S45P			
IDT71322S45C			
IDT71322S45J			
IDT71322S45L48			

IDT	CYPRESS	AMD	VLSI
IDT71322S45CB			
IDT71322S45L48B			
IDT71322S55P			
IDT71322S55C			
IDT71322S55J			
IDT71322S55L48			
IDT71322S55CB			
IDT71322S55L48B			
IDT71322S70P			
IDT71322S70C			
IDT71322S70J			
IDT71322S70L48			
IDT71322S70CB			
IDT71322S70L48B			
IDT71322L35P			
IDT71322L35C			
IDT71322L35J			
IDT71322L35L48			
IDT71322L45P			
IDT71322L45C			
IDT71322L45J			
IDT71322L45L48			
IDT71322L45CB			
IDT71322L45L48B			
IDT71322L55P			
IDT71322L55C			
IDT71322L55J			
IDT71322L55L48			
IDT71322L55CB			
IDT71322L55L48B			
IDT71322L70P			
IDT71322L70C			
IDT71322L70J			
IDT71322L70L48			
IDT71322L70CB			
IDT71322L70L48B			
IDT7133S45XC			
IDT7133S45J			
IDT7133S45L68			
IDT7133S45G			
IDT7133S55XC			
IDT7133S55J			
IDT7133S55L68			
IDT7133S55G			

IDT	CYPRESS	AMD	VLSI
IDT7133S55L68B			
IDT7133S55GB			
IDT7133S70XC			
IDT7133S70J			
IDT7133S70L68			
IDT7133S70G			
IDT7133S70XCB			
IDT7133S70L68B			
IDT7133S70GB			
IDT7133S90XC			
IDT7133S90J			
IDT7133S90L68			
IDT7133S90G			
IDT7133S90XCB			
IDT7133S90L68B			
IDT7133S90GB			
IDT7133L45XC			
IDT7133L45J			
IDT7133L45L68			
IDT7133L45G			
IDT7133L55XC			
IDT7133L55J			
IDT7133L55L68			
IDT7133L55G			
IDT7133L55L68B			
IDT7133L55GB			
IDT7133L70XC			
IDT7133L70J			
IDT7133L70L68			
IDT7133L70G			
IDT7133L70XCB			
IDT7133L70L68B			
IDT7133L70GB			
IDT7133L90XC			
IDT7133L90J			
IDT7133L90L68			
IDT7133L90G			
IDT7133L90XCB			
IDT7133L90L68B			
IDT7133L90GB			
IDT71342S35L52			
IDT71342S35J			
IDT71342S45L52			
IDT71342S45J			

IDT	CYPRESS	AMD	VLSI
IDT71342S45L52B			
IDT71342S55L52			
IDT71342S55J			
IDT71342S55L52B			
IDT71342S70L52			
IDT71342S70J			
IDT71342S70L52B			
IDT7140SA35P	CY7C140-35PC		
IDT7140SA35C	CY7C140-35DC		
IDT7140SA35L48	CY7C140-35LC		
IDT7140SA35L52	CY7C141-35LC		
IDT7140SA35J	CY7C141-35JC		
IDT7140SA35F			
IDT7140SA45P	CY7C140-45PC		
IDT7140SA45C	CY7C140-45DC		
IDT7140SA45L48	CY7C140-45LC		
IDT7140SA45L52	CY7C141-45LC		
IDT7140SA45J	CY7C141-45JC		
IDT7140SA45F			
IDT7140SA45CB	CY7C140-45DMB		
IDT7140SA45L48B	CY7C140-45LMB		
IDT7140SA45L52B	CY7C141-45LMB		
IDT7140SA45FB			
IDT7140SA55P	CY7C140-55PC	AM2140-55PC	
IDT7140SA55C	CY7C140-55DC	AM2140-55DC	
IDT7140SA55L48	CY7C140-55LC		
IDT7140SA55L52	CY7C141-55LC	AM2140-55LC	
IDT7140SA55J	CY7C141-55JC	AM2140-55JC	
IDT7140SA55F			
IDT7140SA55CB	CY7C140-55DMB		
IDT7140SA55L48B	CY7C140-55LMB		
IDT7140SA55L52B	CY7C141-55LMB		
IDT7140SA55FB			
IDT7140SA70P		AM2140-70PC	
IDT7140SA70C		AM2140-70DC	
IDT7140SA70L48			
IDT7140SA70L52		AM2140-70LC	
IDT7140SA70J		AM2140-70JC	
IDT7140SA70F			
IDT7140SA70CB		AM2140-70/BXC	
IDT7140SA70L48B			
IDT7140SA70L52B			
IDT7140SA70FB			
IDT7140SA90P			
IDT7140SA90C			

IDT	CYPRESS	AMD	VLSI
IDT7140SA90L48			
IDT7140SA90L52			
IDT7140SA90J			
IDT7140SA90F			
IDT7140SA90CB			
IDT7140SA90L48B			
IDT7140SA90L52B			
IDT7140SA90FB			
IDT7140SA100P		AM2140-10PC	
IDT7140SA100C		AM2140-10DC	
IDT7140SA100L48			
IDT7140SA100L52		AM2140-10LC	
IDT7140SA100J		AM2140-10JC	
IDT7140SA100F			
IDT7140SA100CB		AM2140-10/BXC	
IDT7140SA100L48B			
IDT7140SA100L52B			
IDT7140SA100FB			
IDT7140SA120CB		AM2140-12/BXC	
IDT7140SA120L48B			
IDT7140SA120L52B			
IDT7140SA120FB			
IDT7140LA35P			
IDT7140LA35C			
IDT7140LA35L48			
IDT7140LA35L52			
IDT7140LA35J			
IDT7140LA35F			
IDT7140LA45P			
IDT7140LA45C			
IDT7140LA45L48			
IDT7140LA45L52			
IDT7140LA45J			
IDT7140LA45F			
IDT7140LA45CB			
IDT7140LA45L48B			
IDT7140LA45L52B			
IDT7140LA45FB			
IDT7140LA55P			
IDT7140LA55C			
IDT7140LA55L48			
IDT7140LA55L52			
IDT7140LA55J			
IDT7140LA55F			
IDT7140LA55CB			

IDT	CYPRESS	AMD	VLSI
IDT7140LA55L48B			
IDT7140LA55L52B			
IDT7140LA55FB			
IDT7140LA70P			
IDT7140LA70C			
IDT7140LA70L48			
IDT7140LA70L52			
IDT7140LA70J			
IDT7140LA70F			
IDT7140LA70CB			
IDT7140LA70L48B			
IDT7140LA70L52B			
IDT7140LA70FB			
IDT7140LA90P			
IDT7140LA90C			
IDT7140LA90L48			
IDT7140LA90L52			
IDT7140LA90J			
IDT7140LA90F			
IDT7140LA90CB			
IDT7140LA90L48B			
IDT7140LA90L52B			
IDT7140LA90FB			
IDT7140LA100P			
IDT7140LA100C			
IDT7140LA100L48			
IDT7140LA100L52			
IDT7140LA100J			
IDT7140LA100F			
IDT7140LA100CB			
IDT7140LA100L48B			
IDT7140LA100L52B			
IDT7140LA100FB			
IDT7140LA120CB			
IDT7140LA120L48B			
IDT7140LA120L52B			
IDT7140LA120FB			
IDT7142SA35P	CY7C142-35PC		VT7142-35PC
IDT7142SA35C	CY7C142-35DC		
IDT7142SA35L48	CY7C142-35LC		
IDT7142SA35L52			
IDT7142SA35J			VT7142-35QC
IDT7142SA35F			
IDT7142SA45P	CY7C142-45PC		VT7142-45PC
IDT7142SA45C	CY7C142-45DC		

IDT	CYPRESS	AMD	VLSI
IDT7142SA45L48	CY7C142-45LC		
IDT7142SA45L52			
IDT7142SA45J			VT7142-45QC
IDT7142SA45F			
IDT7142SA45CB	CY7C142-45DMB		
IDT7142SA45L48B	CY7C142-45LMB		
IDT7142SA45L52B			
IDT7142SA45FB			
IDT7142SA55P	CY7C142-55PC		VT7142-55PC
IDT7142SA55C	CY7C142-55DC		
IDT7142SA55L48	CY7C142-55LC		
IDT7142SA55L52			
IDT7142SA55J			VT7142-55QC
IDT7142SA55F			
IDT7142SA55CB	CY7C142-55DMB		
IDT7142SA55L48B	CY7C142-55LMB		
IDT7142SA55L52B			
IDT7142SA55FB			
IDT7142SA70P			VT7142-70PC
IDT7142SA70C			
IDT7142SA70L48			
IDT7142SA70L52			
IDT7142SA70J			VT7142-70QC
IDT7142SA70F			
IDT7142SA70CB			
IDT7142SA70L48B			
IDT7142SA70L52B			
IDT7142SA70FB			
IDT7142SA90P			VT7142-90PC
IDT7142SA90C			
IDT7142SA90L48			
IDT7142SA90L52			
IDT7142SA90J			VT7142-90QC
IDT7142SA90F			
IDT7142SA90CB			
IDT7142SA90L48B			
IDT7142SA90L52B			
IDT7142SA90FB			
IDT7142SA100P			
IDT7142SA100C			
IDT7142SA100L48			
IDT7142SA100L52			
IDT7142SA100J			
IDT7142SA100F			
IDT7142SA100CB			
IDT7142SA100L48B			

IDT	CYPRESS	AMD	VLSI
IDT7142SA100L52B			
IDT7142SA100FB			
IDT7142SA120CB			
IDT7142SA120L48B			
IDT7142SA120L52B			
IDT7142SA120FB			
IDT7142LA35P			
IDT7142LA35C			
IDT7142LA35L48			
IDT7142LA35L52			
IDT7142LA35J			
IDT7142LA35F			
IDT7142LA45P			
IDT7142LA45C			
IDT7142LA45L48			
IDT7142LA45L52			
IDT7142LA45J			
IDT7142LA45F			
IDT7142LA45CB			
IDT7142LA45L48B			
IDT7142LA45L52B			
IDT7142LA45FB			
IDT7142LA55P			
IDT7142LA55C			
IDT7142LA55L48			
IDT7142LA55L52			
IDT7142LA55J			
IDT7142LA55F			
IDT7142LA55CB			
IDT7142LA55L48B			
IDT7142LA55L52B			
IDT7142LA55FB			
IDT7142LA70P			
IDT7142LA70C			
IDT7142LA70L48			
IDT7142LA70L52			
IDT7142LA70J			
IDT7142LA70F			
IDT7142LA70CB			
IDT7142LA70L48B			
IDT7142LA70L52B			
IDT7142LA70FB			
IDT7142LA90P			
IDT7142LA90C			
IDT7142LA90L48			

IDT	CYPRESS	AMD	VLSI
IDT7142LA90L52			
IDT7142LA90J			
IDT7142LA90F			
IDT7142LA90CB			
IDT7142LA90L48B			
IDT7142LA90L52B			
IDT7142LA90FB			
IDT7142LA100P			
IDT7142LA100C			
IDT7142LA100L48			
IDT7142LA100L52			
IDT7142LA100J			
IDT7142LA100F			
IDT7142LA100CB			
IDT7142LA100L48B			
IDT7142LA100L52B			
IDT7142LA100FB			
IDT7142LA120CB			
IDT7142LA120L48B			
IDT7142LA120L52B			
IDT7142LA120FB			
IDT71421SA35J	CY7C146-35JC		VT71421-35QC
IDT71421SA35L52	CY7C146-35LC		
IDT71421SA45J	CY7C146-45JC		VT71421-45QC
IDT71421SA45L52	CY7C146-45LC		
IDT71421SA45L52B	CY7C146-45LMB		
IDT71421SA55J	CY7C146-55JC		
IDT71421SA55L52	CY7C146-55LC		
IDT71421SA55L52B	CY7C146-55LMB		
IDT71421SA70L52B			
IDT71421LA35J			
IDT71421LA35L52			
IDT71421LA45J			
IDT71421LA45L52			
IDT71421LA45L52B			
IDT71421LA55J			
IDT71421LA55L52			
IDT71421LA55L52B			
IDT71421LA70L52B			
IDT7134S35P			
IDT7134S35C			
IDT7134S35J			
IDT7134S35L52			

IDT	CYPRESS	AMD	VLSI
IDT7134S45P			
IDT7134S45C			
IDT7134S45J			
IDT7134S45L52			
IDT7134S45CB			
IDT7134S45L52B			
IDT7134S55P			
IDT7134S55C			
IDT7134S55J			
IDT7134S55L52			
IDT7134S55CB			
IDT7134S55L52B			
IDT7134S70P			
IDT7134S70C			
IDT7134S70J			
IDT7134S70L52			
IDT7134S70CB			
IDT7134S70L52B			
IDT7134L35P			
IDT7134L35C			
IDT7134L35J			
IDT7134L35L52			
IDT7134L45P			
IDT7134L45C			
IDT7134L45J			
IDT7134L45L52			
IDT7134L45CB			
IDT7134L45L52B			
IDT7134L55P			
IDT7134L55C			
IDT7134L55J			
IDT7134L55L52			
IDT7134L55CB			
IDT7134L55L52B			
IDT7134L70P			
IDT7134L70C			
IDT7134L70J			
IDT7134L70L52			
IDT7134L70CB			
IDT7134L70L52B			
IDT7143S45XC			
IDT7143S45J			
IDT7143S45L68			
IDT7143S45G			

IDT	CYPRESS	AMD	VLSI
IDT7143S55XC			
IDT7143S55J			
IDT7143S55L68			
IDT7143S55G			
IDT7143S55L68B			
IDT7143S55GB			
IDT7143S70XC			
IDT7143S70J			
IDT7143S70L68			
IDT7143S70G			
IDT7143S70XCB			
IDT7143S70L68B			
IDT7143S70GB			
IDT7143S90XC			
IDT7143S90J			
IDT7143S90L68			
IDT7143S90G			
IDT7143S90XCB			
IDT7143S90L68B			
IDT7143S90GB			
IDT7143L45XC			
IDT7143L45J			
IDT7143L45L68			
IDT7143L45G			
IDT7143L55XC			
IDT7143L55J			
IDT7143L55L68			
IDT7143L55G			
IDT7143L55L68B			
IDT7143L55GB			
IDT7143L70XC			
IDT7143L70J			
IDT7143L70L68			
IDT7143L70G			
IDT7143L70XCB			
IDT7143L70L68B			
IDT7143L70GB			
IDT7143L90XC			
IDT7143L90J			
IDT7143L90L68			
IDT7143L90G			
IDT7143L90XCB			
IDT7143L90L68B			
IDT7143L90GB			

IDT	CYPRESS	AMD	VLSI
IDT71342L35L52			
IDT71342L35J			
IDT71342L45L52			
IDT71342L45J			
IDT71342L45L52B			
IDT71342L55L52			
IDT71342L55J			
IDT71342L55L52B			
IDT71342L70L52			
IDT71342L70J			
IDT71342L70L52B			

Integrated Device Technology, Inc.

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CYPRESS/MULTICHIP P/N	IDT P/N DIRECT EQUIVALENT	IDT P/N SIMILAR PART	CYPRESS/MULTICHIP ORG/PACKAGE
CYM1240HD-35MB CYM1240HD-45MB	7M4042S35CB 7M4042S45CB		1 MEG (256K X 4) JEDEC 28 PIN DIP
CYM1420HD-30C CYM1420HD-35C CYM1420HD-45C CYM1420HD-55C CYM1420HD-70C	8M824S30C 8M824S35C 8M824S35N 8M824S45C 8M824S45N 8M824S50C 8M824S50N 8M824S70C 8M824S70N		1 MEG (128K X 8) JEDEC 32 PIN DIP
CYM1421HD-70MB CYM1421HD-85MB CYM1421HD-100MB	8M824S70CB 8M824S85CB 8M824S100CB		1 MEG (128K X 8) JEDEC 32 PIN DIP [Low power version]
CYM1422PS-35C CYM1422PS-45C CYM1422PS-55C	8MP824S35S 8MP824S45S 8MP824S55S		1 MEG (128K X 8) 30 PIN SIP
CYM1441PZ-25C CYM1441PZ-35C CYM1441PZ-45C		7MP4034S25Z 7MP4034S35Z 7MP4034S45Z	2 MEG (256K X 8) JEDEC 60 PIN ZIP
CYM1460PS-45C CYM1460PS-55C CYM1460PS-70C	7MP4008S45S 7MP4008S55S 7MP4008S70S		4 MEG (512K X 8) 36 PIN SIP
CYM1461PS-70C CYM1461PS-85C CYM1461PS-100C	7MP4008L70S 7MP4008L85S 7MP4008L100S	7MP4058L70S 7MP4058L85S 7MP4058L100S	4 MEG (512K X 8) 36 PIN SIP
CYM1464PD-45C CYM1464PD-55C CYM1464PD-70C	7MB4048S45P 7MB4048S50P 7M4048L70N		4 MEG (512K X 8) JEDEC 32 PIN DIP
CYM1540PS-30C CYM1540PS-35C CYM1540PS-45C		7MB4040S25P 7MB4040S35P 7MB4040S45P	2 MEG (256K X 9) 44 PIN SIP
CYM1541PD-25C CYM1541PD-35C CYM1541PD-45C	7MB4040S25P 7MB4040S35P 7MB4040S45P		2 MEG (256K X 9) 44 PIN DIP
CYM1610HD-25C CYM1610HD-35C CYM1610HD-45C CYM1610HD-50C	 8M656S40C 8M656S50C	8M656S40C 8M656S40C	256K (16K X 16) 40 PIN DIP
CYM1611HV-20C CYM1611HV-25C CYM1611HV-30C CYM1611HV-35C CYM1611HV-45C	7MC4005S20CV 7MC4005S25CV 7MC4005S30CV 7MC4005S35CV 7MC4005S45CV		256K (16K X 16) 36 PIN DSIP
CYM1620HD-30C CYM1620HD-35C CYM1620HD-45C CYM1620HD-55C	8M624S30C 8M624S35C 8M624S45C 8M624S50C		1 MEG (64K X 16) JEDEC 40 PIN DIP

CYPRESS/MULTICHIP P/N	IDT P/N DIRECT EQUIVALENT	IDT P/N SIMILAR PART	CYPRESS/MULTICHIP ORG/PACKAGE
CYM1621HD-25C CYM1621HD-30C CYM1621HD-35C CYM1621HD-45C	7M624S25C 7M624S30C 7M624S35C 7M624S45C		1 MEG (64K X 16), (128K X 8), (256K X 4) 40 PIN DIP
CYM1622HV-25C CYM1622HV-35C CYM1622HV-45C		7MP4028 7MP4028 7MP4028	1 MEG (64K X 16) 40 PIN DSIP
CYM1623HD-70MB CYM1623HD-85MB CYM1623HD-100MB	8M624S70CB 8M624S85CB 8M624S100CB		1 MEG (64K X 16) JEDEC 40 PIN DIP [low power version]
CYM1624PV-25C CYM1624PV-35C CYM1624PV-45C	7MP4028S25V 7MP4028S35V 7MP4028S45V		1 MEG (64K X 16) 40 PIN DSIP
CYM1626PS-30C CYM1626PS-35C CYM1626PS-45C	8MP624S30S 8MP624S35S 8MP624S45S		1 MEG (64K X 16) 40 PIN SIP
CYM1641HD-25C CYM1641HD-35C CYM1641HD-45C CYM1641HD-55C	7M4016S25C 7M4016S35C 7M4016S45C 7M4016S55C		4 MEG (256K X 16) 48 PIN DIP
CYM1821PZ-15C CYM1821PZ-20C CYM1821PZ-25C CYM1821PZ-35C CYM1821PZ-45C	7MP4031S15Z 7MP4031S20Z 7MP4031S25Z 7MP4031S35Z 7MP4031S35Z		512K (16K X 32) JEDEC 64 FR-4 ZIP
CYM1822HV-20C CYM1822HV-25C CYM1822HV-30C CYM1822HV-35C CYM1822HV-45C	7MC4032S20CV 7MC4032S25CV 7MC4032S30CV 7MC4032S35CV 7MC4032S45CV		512K (16K X 32) 88 PIN DSIP
CYM1830HD-25C CYM1830HD-30C CYM1830HD-35C CYM1830HD-45C CYM1830HD-55C	7M4017S25C 7M4017S30C 7M4017S35C 7M4017S45C 7M4017S50C		2 MEG (64K X 32) 60 PIN DIP
CYM1831PZ-25C CYM1831PZ-30C CYM1831PZ-35C CYM1831PZ-45C	7MP4036S25Z 7MP4036S30Z 7MP4036S35Z 7MP4036S35Z		2 MEG (64K X 32) JEDEC 64 PIN ZIP
CYM1831PM-25C CYM1831PM-30C CYM1831PM-35C CYM1831PM-45C	7MP4036S25M 7MP4036S30M 7MP4036S35M 7MP4036S35M		2 MEG (64K X 32) JEDEC 64 PIN SIMM
CYM1832PZ-25C CYM1832PZ-35C CYM1832PZ-45C CYM1832PZ-55C		7MP4036S25Z 7MP4036S35Z 7MP4036S35Z 7MP4036S35Z	2 MEG (64K X 32) 60 PIN ZIP
CYM1840HD-30C CYM1840HD-35C CYM1840HD-45C CYM1840HD-55C	7M4067S30C 7M4067S35C 7M4067S45C 7M4067S55C		8 MEG (256K X 32) 60 PIN DIP
CYM1841PZ-30C CYM1841PZ-35C CYM1841PZ-45C CYM1841PZ-55C	7MP4045S30Z 7MP4045S35Z 7MP4045S45Z 7MP4045S55Z		8 MEG (256K X 32) JEDEC 64 PIN ZIP

CYPRESS/MULTICHIP P/N	IDT P/N DIRECT EQUIVALENT	IDT P/N SIMILAR PART	CYPRESS/MULTICHIP ORG/PACKAGE
CYM1841PM-30C CYM1841PM-35C CYM1841PM-45C CYM1841PM-55C	7MP4045S30M 7MP4045S35M 7MP4045S45M 7MP4045S55M		8 MEG (256K X 32) JEDEC 64 PIN SIMM
DENSE-PAC P/N	**IDT P/N DIRECT EQUIVALENT**	**IDT P/N SIMILAR PART**	**DENSE-PAC ORG/PACKAGE**
DPS16X5-XXX	7MP564 7MP564		80K (16K X 5) 28 PIN SIP
DPS16X17-25 DPS16X17-35 DPS16X17-45 DPS16X17-55	7MC4005S25CV 7MC4005S35CV 7MC4005S45CV 7MC4005S55CV		256K (16K X 16) 36 PIN DSIP
DPS257-XXX	7M656 7M656 7M656 7M656		256K (16K X 16) (32K X 8) (64K X 4) 40 PIN DIP
DPS1024-25C DPS1024-35C DPS1024-45C DPS1024-55C		7M624 7M624 7M624 7M624	1 MEG (256K X 4), (128K X 8), (64K X 16) 42 PIN DIP
DPS1026-25C DPS1026-35C DPS1026-45C DPS1026-55C		7M624 7M624 7M624 7M624	1 MEG (256K X 4), (128K X 8), (64K X 16) 40 PIN DIP
DPS1027-25C DPS1027-35C DPS1027-45C DPS1027-55C	7M624S25C 7M624S35C 7M624S45C 7M624S55C		1 MEG (256K X 4), (128K X 8), (64K X 16) 40 PIN DIP
DPS2516-25C DPS2516-35C DPS2516-45C DPS2516-55C		7M4016 7M4016 7M4016 7M4016	4 MEG (256K X 16) 44 PIN DIP
DPS4648-85C DPS4648-100C DPS4648-120C DPS4648-150C		7M812 7M812 7M812 7M812	512K (64K X 8) 32 PIN DIP
DPS5124-45C DPS5124-55C		7MP4034 7MP4034	2 MEG (512K X 4), (256K X 8) 54 PIN DIP
DPS6432-35C DPS6432-45C DPS6432-55C DPS6432-70C	7M4017S35C 7M4017S45C 7M4017S55C 7M4017S70C		2 MEG (64K X 32) 60 PIN DIP
DPS6433-85C DPS6433-100C DPS6433-120C DPS6433-150C		7MP4034, 7M4017 7MP4034, 7M4017 7MP4034, 7M4017 7MP4034, 7M4017	2 MEG (64K X 32) (128K X 16), (256K X 8) 60 PIN DIP [low power version]
DPS6433-55C DPS6433-70C DPS6433-100C		7M4017S55C 7M4017S70C 7M4017S70C	2 MEG (64K X 32) 60 PIN DIP [low power version]
DPS8645-XXX	7MP456 7MP456		256K (64K X 4) 28 PIN SIP
DPS8808-XXX	7M864 7M864		64K (8K X 8) 28 PIN DIP

DENSE-PAC P/N	IDT P/N DIRECT EQUIVALENT	IDT P/N SIMILAR PART	DENSE-PAC ORG/PACKAGE
DPS8M612-85C DPS8M612-100C DPS8M612-120C DPS8M612-150C	8M612S85C 8M612S100C 8M612S100C 8M612S100C		512K (32K X 16) 40 PIN DIP
DPS8M624-85C DPS8M624-100C DPS8M624-120C DPS8M624-150C	8M624S85C 8M624S100C 8M624S100C 8M624S100C		1 MEG (64K X 16) 40 PIN DIP
DPS8M656-35C DPS8M656-40C DPS8M656-70C	 8M656S40C 8M656S70C	8M656S40C	256K (16K X 16) 40 PIN DIP
DPS10241-25C DPS10241-35C DPS10241-45C DPS10241-55C	 7MC4001S35CS 7MC4001S45CS 7MC4001S55CS	7MC4001S35C	1 MEG (1024K X 1) 30 PIN SIP
DPS40256-XXX	8M856 8M856		256K (32K X 8) 28 PIN DIP
DPS41257-XXX	8M856 8M856		256K (32K X 8) 28 PIN DIP
DPS41288-70C DPS41288-85C DPS41288-100C	8M824S70C	8M824L70N 8M824L85N 8M824L100N	1 MEG (128K X 8) 32 PIN DIP
DPS45128-85C DPS45128-100C DPS45128-120C DPS45128-150C		7MP4008 7MP4008 7MP4008 7MP4008	4 MEG (512K X 8) 48 PIN DIP
DPS45129-85C DPS45129-100C DPS45129-120C DPS45129-150C	7M4016S55C 7M4016S55C 7M4016S55C 7M4016S55C		4 MEG (256K X 16) 48 PIN DIP
DPS512S8-85C DPS512S8-100C DPS512S8-120C DPS512S8-150C	7M4048L85N 7M4048L100N 7M4048L120N 7M4048L120N		4 MEG (512K X 8) 32 PIN DIP
DPS3232V	7M4003SXXCH		1 MEG (32K X 32) 66 PIN HIP
DPE3232V	7M7004SXXCH		1 MEG (32K X 32) EEPROM 66 PIN HIP
EDI P/N	**IDT P/N DIRECT EQUIVALENT**	**IDT P/N SIMILAR PART**	**EDI ORG/PACKAGE**
EDI8M4257C35C4B EDI8M4257C45C4B EDI8M4257C55C4B	7M4042S35CB 7M4042S45CB 7M4042S55CB		1 MEG (256K X 4) JEDEC 28 PIN DIP
EDI8M8128C35C6C EDI8M8128C45C6C EDI8M8128C55C6C EDI8M8128C45C6B EDI8M8128C55C6B EDI8M8128C70C6B	8M824S35C 8M824S45C 8M824S50C 8M824S45CB 8M824S50CB 8M824S70CB	8M824S35N, 8MP824S35S 8M824S45N, 8MP824S45S 8M824S50N, 8MP824S50S	1 MEG (128K X 8) JEDEC 32 PIN DIP
EDI8M8128C60P6C EDI8M8128C70P6C EDI8M8128C100P6C EDI8M8128C120P6C EDI8M8128C150P6C	8M824S60N 8M824L70N 8M824L100N 8M824L100N 8M824L100N	8M824S60C, 8MP824S60S 8M824S70C, 8MP824L70S 8MP824L100S 8MP824L100S 8MP824L100S	1 MEG (128K X 8) JEDEC 32 PIN DIP

EDI P/N	IDT P/N DIRECT EQUIVALENT	IDT P/N SIMILAR PART	EDI ORG/PACKAGE
EDI8M8128C85C6B EDI8M8128C1006CB EDI8M8128C1206CB EDI8M8128C1506CB	8M824S85CB 8M824S100CB 8M824S100CB 8M824S100CB		1 MEG (128K X 8) JEDEC 32 PIN DIP [low power version]
EDI8M8256C70P6C EDI8M8256C85P6C EDI8M8256C100P6C EDI8M8256C120P6C EDI8M8256C150P6C	7M4068L70N 7M4068L85N 7M4068L100N 7M4068L120N 7M4068L120N		2 MEG (256K X 8) JEDEC 32 PIN DIP
EDI8F8257C85B6C EDI8F8257C100B6C EDI8F8257C120B6C EDI8F8257C150B6C	7M4068L85N 7M4068L100N 7M4068L120N 7M4068L120N		2 MEG (256K X 8) JEDEC 32 PIN DIP
EDI8M8257C85P6C EDI8M8257C100P6C EDI8M8257C120P6C EDI8M8257C150P6C	7M4068L85N 7M4068L100N 7M4068L120N 7M4068L120N		2 MEG (256K X 8) JEDEC 32 PIN DIP
EDI8F8257C45MSC EDI8F8257C55MSC EDI8F8257C70MSC		7MP4034S45Z 7MP4034S45Z 7MP4034S45Z	2 MEG (256K X 8) 36 PIN SIP
EDI8F8258C45MSC EDI8F8258C55MSC EDI8F8258C70MSC		7MP4034S45Z 7MP4034S45Z 7MP4034S45Z	2 MEG (256K X 8) 36 PIN SIP
EDI8M8512C85P6C EDI8M8512C100P6C EDI8M8512C120P6C EDI8M8512C150P6C EDI8M8512C85C6B EDI8M8512C100C6B EDI8M8512C120C6B EDI8M8512C150C6B	7M4048L85N 7M4048L100N 7M4048L120N 7M4048L120N 7M4048S85CB 7M4048S100CB 7M4048S120CB 7M4048S120CB		4 MEG (512K X 8) JEDEC 32 PIN DIP
EDI8F8512C45M6C EDI8F8512C55M6C EDI8F8512C70M6C EDI8M8512C45M6B EDI8M8512C55M6B EDI8M8512C70M6B	7MB4048S45P 7MB4048S55P 7M4048L70N 7M4048S45CB 7M4048S55CB 7M4048S70CB		4 MEG (512K X 8) JEDEC 32 PIN DIP
EDH816H16C-25CC-Z EDH816H16C-35CC-Z EDH816H16C-45CC-Z EDH816H16C-25CMHR-Z EDH816H16C-35CMHR-Z EDH816H16C-45CMHR-Z	7MC4005S25CV 7MC4005S35CV 7MC4005S45CV 7MC4005S25CVB 7MC4005S35CVB 7MC4005S45CVB		256K (16K X 16) 36 PIN DSIP
EDI8F1664C100PC EDI8F1664C120PC EDI8F1664C150PC	8M624S70C 8M624S70C 8M624S70C	8MP624L100S 8MP624L100S 8MP624L100S	1 MEG (64K X 16) 40 PIN DIP
EDI8M1664C45C6C EDI8M1664C55C6C EDI8M1664C60C6C EDI8M1664C70C6C EDI8M1664C85C6C EDI8M1664C100C6C EDI8M1664C55C6B EDI8M1664C60C6B EDI8M1664C70C6B EDI8M1664C85C6B EDI8M1664C100C6B	8M624S50C 8M624S50C 8M624S60C 8M624S70C 8M624S850C 8M624S100C 8M624S50CB 8M624S60CB 8M624S70CB 8M624S85CB 8M624S100CB		1 MEG (64K X 16) JEDEC 40 PIN DIP

EDI P/N	IDT P/N DIRECT EQUIVALENT	IDT P/N SIMILAR PART	EDI ORG/PACKAGE
EDI8M1664C25C9C	7M624S25C		1 MEG (64K X 16)
EDI8M1664C35C9C	7M624S35C		40 PIN DIP
EDI8M1664C45C9C	7M624S45C		
EDI8M1664C55C9C	7M624S55C		
EDI8M1664C70C9C	7M624S70C		
EDI8M1664C25C9B	7M624S25CB		
EDI8M1664C35C9B	7M624S35CB		
EDI8M1664C45C9B	7M624S45CB		
EDI8M1664C55C9B	7M624S55CB		
EDI8M1664C70C9B	7M624S70CB		
EDI8M16256C25C9C	7M4016S25C		4 MEG (256K X 16)
EDI8M16256C35C9C	7M4016S35C		48 PIN DIP
EDI8M16256C45C9C	7M4016S45C		
EDI8M16256C55C9C	7M4016S55C		
EDI8M16256C70C9C	7M4016S55C		
EDI8M16256C35C9B	7M4016S35CB		
EDI8M16256C45C9B	7M4016S45CB		
EDI8M16256C55C9B	7M4016S55CB		
EDI8M16256C70C9B	7M4016S55CB		
EDI8M16257C35M6C		7MB4066S35P	4 MEG (256K X 16)
EDI8M16257C45M6C		7MB4066S45P	40 PIN DIP
EDI8M16257C55M6C		7MB4066S55P	
EDI8M16257C70M6C		7MB4066S55P	
EDI8F3264C25M6C	7M4017S25C		2 MEG (64K X 32)
EDI8F3264C35M6C	7M4017S35C		60 PIN DIP
EDI8F3264C45M6C	7M4017S45C		
EDI8F3264C55M6C	7M4017S50C		
EDI8M3264C25C6B		7M4017S30CB	
EDI8M3264C35C6B	7M4017S35CB		
EDI8M3264C45C6B	7M4017S45CB		
EDI8M3264C55C6B	7M4017S50CB		
EDI8F3264C25MZC	7MP4036S25Z		2 MEG (64K X 32) JEDEC
EDI8F3264C35MZC	7MP4036S30Z		64 PIN ZIP
EDI8F3264C45MZC	7MP4036S35Z		
EDI8F3264C55MZC	7MP4036S35Z		
EDI8M32256C35B6C	7M4067S35C		8 MEG (256K X 32)
EDI8M32256C45B6C	7M4067S45C		60 PIN DIP
EDI8M32256C55B6C	7M4067S55C		
EDI8M32256C70B6C	7M4067S55C		
EDI8M32256C35BZC	7MP4045S35Z		8 MEG (256K X 32) JEDEC
EDI8M32256C45BZC	7MP4045S45Z		64 PIN ZIP
EDI8M32256C55BZC	7MP4045S55Z		
EDI8M32256C70BZC	7MP4045S70Z		
EDI8M8130C50CC		8M824	1 MEG (128K X 8)
EDI8M8130C60CC		8M824	32 PIN DIP
EDI8M8130C70CC		8M824	[dual chip enable]
EDI8M8130C80CC		8M824	
EDI8M8130C90CC		8M824	
EDI8M8130C100CC		8M824	
EDI8M8130C120CC		8M824	
EDI8M8130C150CC		8M824	
EDI8M8130C50CB		8M824	
EDI8M8130C60CB		8M824	
EDI8M8130C70CB		8M824	
EDI8M8130C80CB		8M824	
EDI8M8130C90CB		8M824	
EDI8M8130C100CB		8M824	
EDI8M8130C120CB		8M824	
EDI8M8130C150CB		8M824	

EDI P/N	IDT P/N DIRECT EQUIVALENT	IDT P/N SIMILAR PART	EDI ORG/PACKAGE
EDI8M8130P90CB EDI8M8130P100CB EDI8M8130P120CB EDI8M8130P150CB		8M824 8M824 8M824 8M824	1 MEG (128K X 8) 32 PIN DIP [dual chip enable] [low power version]
EDI8M864C50CC EDI8M864C60CC EDI8M864C70CC EDI8M864C80CC EDI8M864C90CC EDI8M864C100CC EDI8M864C120CC EDI8M864C150CC EDI8M864C50CB EDI8M864C60CB EDI8M864C70CB EDI8M864C80CB EDI8M864C90CB EDI8M864C100CB EDI8M864C120CB EDI8M864C150CB		7M812 7M812 7M812 7M812 7M812 7M812 7M812 7M812 7M812 7M812 7M812 7M812 7M812 7M812 7M812 7M812	512K (64K X 8) 32 PIN DIP
EDH81H256C-55 EDH81H256C-70	7MC156S55CS 7MC156S70CS	7MP156	256K (256K X 1) 28 PIN SIP
EDH84H64C-35CC-D3 EDH84H64C-45CC-D3 EDH84H64C-55CC-D3 EDH84H64C-35CMHR-D3 EDH84H64C-35CMHR-D3 EDH84H64C-35CMHR-D3 EDH84H64C-35CMHR-D3		7MP456	256K (64K X 4) 24 PIN DIP
EDH84H64C-35CC-S EDH84H64C-45CC-S EDH84H64C-55CC-S	7MP456S35S 7MP456S45S 7MP456S55S		256K (64K X 4) 28 PIN SIP
EDH8808HC-55CMHR EDH8808HC-70CMHR EDH8808C-10CMHR EDH8808C-12CMHR EDH8808C-15CMHR EDH8808CL-20CMHR EDH8808CL-25CMHR EDH8808A-10CMHR EDH8808A-12CMHR EDH8088A-15CMHR EDH8808AL-20CMHR EDH8808AL-25CMHR	 8M864L85CB 8M864L120CB 8M864L150CB 8M864L150CB 8M864L150CB 7M864L85CB 7M864L120CB 7M864L150CB 7M864L150CB 7M864L150CB	8M864L55CB 8M864L75CB	64K (8K X 8) 28 PIN DIP
EDH8832C-12C EDH8832C-15C EDH8832C-20C EDH8832C-12CMHR EDH8832C-15CMHR EDH8832C-20CMHR	8M856L85C 8M856L85C 8M856L85C 8M856L100CB 8M856L100CB 8M856L100CB	7M856S 7M856S 7M856S 7M856S 7M856S 7M856S	256K (32K X 8) 28 PIN DIP
EDH8832HC-45CMHR EDH8832HC-55CMHR EDH8832HC-70CMHR EDH8832HC-85CMHR	7M856S45CB 7M856S55CB 7M856S65CB 7M856S75CB	8M856L 8M856L 8M856L 8M856L	256K (32K X 8) 28 PIN DIP

MICRON TECHNOLOGY P/N	IDT P/N DIRECT EQUIVALENT	IDT P/N SIMILAR PART	MICRON ORG/PACKAGE
MT85C8128-30 MT85C8128-35 MT85C8128-45	8M824S30C 8M824S35C 8M824S45C		1 MEG (128K X 8) JEDEC 32 PIN DIP
MT85C1632-30 MT85C1632-35 MT85C1632-45	8M612S30C 8M612S35C 8M612S45C		512K (32K X 16) JEDEC 40 PIN DIP
MT85C1664-30 MT85C1664-35 MT85C1664-45	8M624S30C 8M624S35C 8M624S45C		1 MEG (64K X 16) JEDEC 40 PIN DIP
MT8C16256-30 MT8C16256-35 MT8C16256-45	7MB4066S30P 7MB4066S35P 7MB4066S45P		4 MEG (256K X 16) JEDEC 48 PIN DIP
MT8C3216-15 MT8C3216-20 MT8C3216-25 MT8C3216-30 MT8C3216-35 MT8C3216-45	7MP4031S15Z 7MP4031S20Z 7MP4031S25Z 7MP4031S30Z 7MP4031S35Z 7MP4031S35Z		512K (16K X 32) JEDEC 64 PIN ZIP
MT8C3264-25 MT8C3264-30 MT8C3264-35 MT8C3264-45	7MP4036S25Z 7MP4036S30Z 7MP4036S35Z 7MP4036S35Z		2 MEG (64K X 32) JEDEC 64 PIN ZIP
MT8C32256-30 MT8C32256-35 MT8C32256-45	7MP4045S30Z 7MP4045S35Z 7MP4045S45Z		8 MEG (256K X 32) JEDEC 64 PIN ZIP
MOSAIC P/N	**IDT P/N DIRECT EQUIVALENT**	**IDT P/N SIMILAR PART**	**MOSAIC ORG/PACKAGE**
MS1256CS-25 MS1256CS-35		7MP156, 7MC156 7MP156, 7MC156	256K (256K X 1) 25 PIN SIP
MS8128SLU-55 MS8128SU-70 MS8128SL-10	8M824S50C 8M824S70C 8M824S70C	8M824SXXN, 8MP824	1 MEG (128K X 8) 32 PIN DIP
MS8256RKL-10 MS8256RKL-12		7MP4034 7MP4034	2 MEG (256K X 8) 32 PIN SIP
MS8512FKX-85 MS8512FKX-10 MS8512FKX-12	7M4048L85N 7M4048L100N 7M4048L120N		4 MEG (512K X 8) JEDEC 32 PIN DIP
MS8512SCMB-85 MS8512SCMB-10 MS8512SCMB-12	7M4048S85CB 7M4048S100CB 7M4048S120CB		4 MEG (512K X 8) JEDEC 32 PIN DIP
MS8512SC-45 MS8512SC-55 MS8512SC-70	7MB4048S45P 7MB4048S50P 7M4048L70N		4 MEG (512K X 8) JEDEC 32 PIN DIP
MS8512SCMB-45 MS8512SCMB-55 MS8512SCMB-70	7M4048S45CB 7M4048S50CB 7M4048S70CB		4 MEG (512K X 8) JEDEC 32 PIN DIP
MS8512RKX-10 MS8512RKX-12 MS8512RKX-15	7MP4008L100S 7MP4008L100S 7MP4008L100S	7MP4058L100S 7MP4058L120S 7MP4058L120S	4 MEG (512K X 8) 36 PIN SIP
MS1664FKX-30 MS1664FKX-35 MS1664FKX-45	8M624S30C 8M624S35C 8M624S45C		1 MEG (64K X 16) JEDEC 40 PIN DIP

MOSAIC P/N	IDT P/N DIRECT EQUIVALENT	IDT P/N SIMILAR PART	MOSAIC ORG/PACKAGE
MS1664BCX-25 MS1664BCX-35 MS1664BCXMB-25 MS1664BCXMB-35	7M624S25C 7M624S35C 7M624S25CB 7M624S35CB		1 MEG (64K X 16) 40 PIN DIP
MS3216RKX-15 MS3216RKX-20 MS3216RKX-25 MS3216RKX-35 MS3216RKX-45	7MP4031S15Z 7MP4031S20Z 7MP4031S25Z 7MP4031S35Z 7MP4031S35Z		512K (16K X 32) JEDEC 64 PIN ZIP
PUMA 2S1000	7M4003SXXCH		1 MEG (32K X 32) 66 PIN HIP
PUMA 2E1000	7M7004SXXCH		1 MEG (32K X 32) EEPROM 66 PIN HIP
MS3264FKX-25 MS3264FKX-35 MS3264FKX-45 MS3264FKX-55	 7M4017S35C 7M4017S40C 7M4017S50C	7MP4036S25Z	2 MEG (64K X 32) 60 PIN DIP
MS3264RKX-25 MS3264RKX-35 MS3264RKX-45	7MP4036S25Z 7MP4036S35Z 7MP4036S45Z		2 MEG (64K X 32) JEDEC 64 PIN ZIP
MS32256FKX-35 MS32256FKX-45 MS32256FKX-55	7M4067S35C 7M4067S45C 7M4067S55C		8 MEG (256K X 32) 60 PIN DIP
MS32256RKX-35 MS32256RKX-45 MS32256RKX-55	7MP4045S35Z 7MP4045S45Z 7MP4045S55Z		8 MEG (256K X 32) JEDEC 64 PIN ZIP
MISC. VENDORS P/N	**IDT P/N DIRECT EQUIVALENT**	**IDT P/N SIMILAR PART**	**MISC. VENDORS ORG/PACKAGE**
AEP			
AEPSS4K32		7MC4032	128K (4K X 32)
AEPSS8K32		7MC4032	256K (8K X 32)
AEPSS64K8		7M812	512K (64K X 8)
AEPSS256K8		7MP4034	2 MEG (256K X 8)
AEPSS256K9-25 AEPSS256K9-35 AEPSS256K9-45 AEPSS256K9-55		7MB4040 7MB4040 7MB4040 7MB4040	2 MEG (256K X 9) 44 PIN SIP
AEPSS128K8		8M824, 8MP824	1 MEG (128K X 8)
AEPSS32K16		8M612, 8MP612	512K (32K X 16)
AEPSS128K16		7M4016	2 MEG (128K X16)
AEPSS2M8		NA NA	16 MEG (2M X 8) 40 PIN SIP
AEPSS512K8-35 AEPSS512K8-55 AEPSS512K8-70 AEPSS512K8-85 AEPSS512K8-10 AEPSS512K8-12	7MP4008S35S 7MP4008S55S 7MP4008S70S 7MP4008S70S 7MP4008S70S 7MP4008S70S		4 MEG (512K X 8) 36 PIN SIP
AEPSS512K8-10SL AEPSS512K8-12SL	7MP4008L100S 7MP4008L100S		4 MEG (512K X 8) 36 PIN SIP [low power version]

MISC. VENDORS P/N	IDT P/N DIRECT EQUIVALENT	IDT P/N SIMILAR PART	MISC. VENDORS ORG/PACKAGE
ARRAY TECHNOLOGY			
AT212SZ-15 AT212SZ-20			512K (16K X 32) 94 PIN ZIP REGISTERED, SEP. I/O
AT212			512K (16K X 32) 64 PIN DIP REGISTERED
AT612CP-35 AT612CP-40	8M612S35C 8M612S40C		512K (32K X 16) JEDEC 40 PIN DIP
AT656CP		8M656 8M656	256K (16K X 16) 40 PIN DIP
HARRIS			
HM-8808S, AS-100 HM-8808B, AB-120 HM-8808, A-150			64K (8K X 8) JEDEC 28 PIN DIP
HM-8816HB-70 HM-8816H-85 HM-92560		7M856, 8M656	128K (16K X 8) JEDEC 28 PIN DIP 256K (32K X 8), (16K X 16) SYNCHRONOUS 48 PIN DIP
FUJITSU			
MB85402-30 MB85402-40	7MC4005S30CV 7MC4005S35CV		256K (16K X 16) 36 PIN DSIP
MB85403A-40 MB85403A-50		7MP4034S35Z 7MP4034S45Z	2 MEG (256K X 8) 44 PIN DSIP
MB85410-30 MB85410-40		7M812 7M812	512K (64K X 8) JEDEC 60 PIN ZIP
MB85411-35 MB85411-40		7M912 7M912	512K (64K X 9) 70 PIN ZIP
MB85414-30 MB85414-40	7MP4031S25Z 7MP4031S35Z		512K (16K X 32) JEDEC 64 PIN ZIP
MB85415-35 MB85415-40		7MP4031S25Z 7MP4031S35Z	512K (16K X 36) 70 PIN ZIP
MB85420-40 MB85420-50		7MP4034S35Z 7MP4034S45Z	2 MEG (256K X 8) JEDEC 60 PIN ZIP
HITACHI			
HM66203-10 HM66203-12 HM66203-15		8M824, 8MP824 8M824, 8MP824 8M824, 8MP824	1 MEG (128K X 8) 32 PIN DIP
HM66203L-10 HM66203L-12 HM66203L-15		8M824L, 8MP824L 8M824L, 8MP824L 8M824L, 8MP824L	1 MEG (128K X 8) JEDEC 32 PIN DIP [low power version]
HM66204-12 HM66204-15	8M824L100N 8M824L100N		1 MEG (128K X 8) JEDEC 32 PIN DIP
HM62256P-8 HM62256P-10 HM62256P-12	7M856S85C 7M856S85C 7M856S85C		256K (32K X 8) 28 PIN DIP
HM62256LP-8 HM62256LP-10 HM62256LP-12	8M856L85C 8M856L85C 8M856L85C		256K (32K X 8) 28 PIN DIP LOW POWER

MISC. VENDORS P/N	IDT P/N DIRECT EQUIVALENT	IDT P/N SIMILAR PART	MISC. VENDORS ORG/PACKAGE
INOVA			
S128K8-55C S128K8-70C S128K8-85C S128K8-70M S128K8-85M S128K8-100M S128K8-120M	8M824S50C 8M824S60C 8M824S70C 8M824S70CB 8M824S85CB 8M824S100CB 8M824S100CB	8M824SXXN, 8MP824 8M824SXXN, 8MP824	1 MEG (128K X 8) JEDEC 32 PIN DIP
S128K8L-70MC		8M824S70CB	1 MEG (128K X 8) JEDEC 32 PIN DIP [low power version]
S32K8-55C S32K8-70C S32K8-85C S32K8-70M S32K8-85M S32K8-100M	7M856S50C 7M856S70C 7M856S85C 7M856S65CB 7M856S75CB 7M856S90CB	8M856L 8M856LXXCB	256K (32K X 8) JEDEC 28 PIN DIP
LOGIC DEVICES			
LMM4016-25 LMM4016-35 LMM4016-45 LMM4016-55	7M4016S25C 7M4016S35C 7M4016S45C 7M4016S55C		4 MEG (256K X 16) 48 PIN DIP
LMM624-25 LMM624-35 LMM624-45 LMM624-55	7M624S25C 7M624S35C 7M624S45C 7M624S55C		1 MEG (64K X 16) 40 PIN DIP
LMM824-40 LMM824-45 LMM824-50 LMM824-60 LMM824-70 LMM824-85 LMM824-100	8M824S40C 8M824S40N 8M824S45C 8M824S45N 8M824S50C 8M824S50N 8M824S60C 8M824S60N 8M824L70N 8M824S70C 8M824S70N 8M824L85N 8M824L100N		1 MEG (128K X 8) JEDEC 32 PIN DIP
LMM456-25 LMM456-30 LMM456-35 LMM456-45	7MP456S25S 7MP456S30S 7MP456S35S 7MP456S45S		256K (64K X 4) 28 PIN SIP
MARCONI			
SF63000	7M4016		1 MEG (256K X 16), (512K X 8) 48 PIN DIP
MEMORY X			
MXS32032LZ		7M4003 7M4003	1 MEG (32K X 32) 80 PIN ZIP
MICROELECTRONICS			
MS12808 (100ns) MS12808 (120ns) MS12808 (150ns)	8M824L100N 8M824L100N 8M824L100N		1 MEG (128K X 8) JEDEC 32 PIN DIP

MISC. VENDORS P/N	IDT P/N DIRECT EQUIVALENT	IDT P/N SIMILAR PART	MISC. VENDORS ORG/PACKAGE
MITSUBISHI			
MH12808TNA-85 MH12808TNA-10 MH12808TNA-12 MH12808TNA-15	8M824L85N 8M824L100N 8M824L100N 8M824L100N	8M824S, 8MP824 8M824S, 8MP824 8M824S, 8MP824 8M824S, 8MP824	1 MEG (128K X 8) JEDEC 32 PIN DIP
MH12908TNA-85 MH12908TNA-10 MH12908TNA-12 MH12908TNA-15		8M824L,8M824S,8MP824 8M824L,8M824S,8MP824 8M824L,8M824S,8MP824 8M824L,8M824S,8MP824	1 MEG (128K X 8) JEDEC 32 PIN DIP
MH25608TNA-85L MH25608TNA-10L MH25608TNA-12L MH25608TNA-15L		7MP4034 7MP4034 7MP4034 7MP4034	2 MEG (256K X 8) JEDEC 32 PIN DIP
MH25608TNA-85H MH25608TNA-10H MH25608TNA-12H MH25608TNA-15H		7MP4034 7MP4034 7MP4034 7MP4034	2 MEG (256K X 8) JEDEC 32 PIN DIP [low power version]
MH51208SN-70L MH51208SN-85L MH51208SN-10L MH51208SN-12L MH51208SN-15L		7MP4008 7MP4008 7MP4008 7MP4008 7MP4008	4 MEG (512K X 8) 64 PIN SIMM
MH51208SN-70H MH51208SN-85H MH51208SN-10H MH51208SN-12H MH51208SN-15H		7MP4008 7MP4008 7MP4008 7MP4008 7MP4008	4 MEG (512K X 8) 64 PIN SIMM [low power version]
MH25608S1N-70 MH25608S1N-85 MH25608S1N-10 MH25608S1N-12 MH25608S1N-15		7MP4034 7MP4034 7MP4034 7MP4034 7MP4034	2 MEG (256K X 8) 35 PIN SIMM
MOTOROLA			
MCM3264-20 MCM3264-25 MCM3264-30	7MP4036S20Z 7MP4036S25Z 7MP4036S30Z		2 MEG (64K X 32) JEDEC 64 PIN ZIP
MCM8256-20 MCM8256-25 MCM8256-30		7MP4034S20Z 7MP4034S25Z 7MP4034S25Z	2 MEG (256K X 8) JEDEC 60 PIN ZIP
MOSEL			
MS88128 (100ns) MS88128 (120ns) MS88128 (150ns)	8M824S50C 8M824S50C 8M824S50C	8M824SXXN, 8MP824	1 MEG (128K X 8) JEDEC 32 PIN DIP
NEC			
MC-120	8M824S50C	8M824SXXN, 8MP824	1 MEG (128K X 8) JEDEC 32 PIN DIP
VALTRONIC			
M107-100 M107-120 M107-150	7M624S100C 7M624S100C 7M624S100C	8M624, 8MP624	1 MEG (64K X 16) 40 PIN DIP
XXX (120ns)	7M856S85C		256K (32K X 8) JEDEC 28 PIN DIP

MISC. VENDORS P/N	IDT P/N DIRECT EQUIVALENT	IDT P/N SIMILAR PART	MISC. VENDORS ORG/PACKAGE
VITAREL			
VMS10A24-100 VMS10A24-150 VMS10A24-200		8M824SXXN, 8MP824 7M624, 8M624, 8MP624	1 MEG (64K X 16), (128K X 8), (64K X 8) 40 PIN DIP
VMS32K8-45 VMS32K8-55 VMS32K8-70	7M856S45C 7M856S50C 7M856S70C	8M856L	256K (32K X 8) JEDEC 28 PIN DIP
VMS128K8M-55 VMS128K8M-60	8M824S50C 8M824S60C	8M824SXXN, 8MP824, 8M824L	1 MEG (128K X 8) JEDEC 32 PIN DIP
WHITE TECHNOLOGY			
WS-128K8-70CM	8M824S70CB		1 MEG (128K X 8) JEDEC 32 PIN DIP
ZYREL			
Z108-10 Z108-15	8M824S70C 8M824S70C	8M824SXXN, 8MP824	1 MEG (128K X 8) JEDEC 32 PIN DIP

IDT...LEADING THE CMOS FUTURE

A major revolution is taking place in the semiconductor industry today. A new technology is rapidly displacing older NMOS and bipolar technologies as the workhorse of the 80's and beyond. That technology is high-speed CMOS. Integrated Device Technology, a company totally predicated on and dedicated to implementing high-performance CMOS products, is on the leading edge of this dramatic change.

Beginning with the introduction of the industry's fastest CMOS 2K x 8 static RAM, IDT has grown into a company with multiple divisions producing a wide range of high-speed CMOS circuits that are, in almost every case, the fastest available. These advanced products are produced with IDT's proprietary CEMOS™ technology, a twin-well, dry-etched, stepper-aligned process utilizing progressively smaller dimensions.

From inception, IDT's product strategy has been to apply the advantages of it's extremely fast CEMOS technology to produce the integrated circuit elements required to implement high-performance digital systems. IDT's goal is to provide the circuits necessary to create systems which are far superior to previous generations in performance, reliability, cost weight and size. Many of the company's innovative product designs offer higher levels of integration, advanced architectures, higher density packaging and system enhancement features that are establishing tomorrow's industry standards. The company is committed to providing its customers with an ever-expanding series of these high-speed, lower-power IC solutions to system design needs.

IDT's commitment, however, extends beyond state-of-the-art technology and advanced products to providing the highest level of customer service and satisfaction in the industry. Producing products to exacting quality standards that provide excellent, long-term reliability is given the same level of importance and priority as device performance. IDT is also dedicated to delivering these high-quality advanced products on time. The company would like to be known not only for its technological capabilities, but also for providing its customers with quick, responsive and courteous service.

IDT's product families are available in both commercial and military grades. As a bonus, commercial customers obtain the benefits of military processing disciplines, established to meet or exceed the stringent criteria of the applicable military specifications.

IDT is the leading U.S. supplier of high-speed CMOS circuits. The company's high-performance fast SRAM , FCT logic family, high-density modules, FIFOs, complex logic products, specialty memories, ECL I/O BiCEMOS™ memories, RISC subsystems, and the 32-bit RISC microprocessor family complement each other to provide high-speed CMOS solutions to a wide range of applications and systems.

Dedicated to maintaining its leadership position as a state-of-the-art IC manufacturer, IDT will continue to focus on maintaining its technology edge as well as developing a broader range of innovative products. New products and speed enhancements are continuously being added to each of the existing product families and additional product lines will be introduced. Contact your IDT field representative or factory marketing engineer to determine the latest product offerings. If you're building state-of-the-art equipment, IDT wants to help you solve some of your design problems.

IDT MILITARY AND DESC-SMD PROGRAM

IDT is a leading supplier of military, high-speed CMOS circuits. The company's high-performance Static RAMs, FCT Logic Family, Complex Logic (CLP), FIFOs, Specialty Memories (SMP), ECL I/O BiCMOS Memories, 32-bit RISC Microprocessor, RISC Subsystems and high-density Subsystems Modules product lines complement each other to provide high-speed CMOS solutions to a wide range of military applications and systems. Most of these product lines offer Class B products which are fully compliant to the latest revision of MIL-STD-883, Paragraph 1.2.1. In addition, IDT offers Radiation Tolerant (RT), as well as Radiation Enhanced (RE), products.

IDT has an active program with the Defense Electronic Supply Center (DESC) to list all of IDT's military compliant devices on Standard Military Drawings (SMD). The SMD program allows standardization of militarized products and reduction of the proliferation of non-standard source control drawings. This program will go far toward reducing the need for each defense contractor to make separate specification control drawings for purchased parts. IDT plans to have SMDs for many of its product offerings. Presently, IDT has 88 devices which are listed or pending listing. The devices are from IDT's SRAM, FCT Logic family, Complex Logic (CLP), FIFOs and Specialty Memories (SMP) product families. IDT expects to add another 20 devices to the SMD program in the near future. Users should contact either IDT or DESC for current status of products in the SMD program.

SMD	
SRAM	**IDT**
84036/D	6116
5962-88740	6116LA
84132/B	6167
5962-86015/A	7187
5962-86859	6198/7198/7188
5962-86705/A	6168
5962-85525/A	7164
5962-88552	71256L
5962-88662	71256S
5962-88611	71682L
5962-88681/A	71258S
5962-88545	71258L
5962-88544	71257L
5962-88725/A	71257S
5962-89690	6116
5962-89691	7164
5962-89692	7188
5962-89712	71982
SMP	**IDT**
5962-86875/A	7130/7140
5962-87002/A	7132/7142
5962-88610/A	7133S/7143S
5962-88665/A	7133L/7143L
FIFO	**IDT**
5962-87531	7201LA
5962-86846/A	72404
5962-88669	7203S
5962-89568	7204L
5962-89536	7202L
5962-89863	7201S
5962-89523	72403L
5962-89666	7200L
5962-89942	72103L
5962-89943	72104L
5962-89567	7203L

SMD	
LOGIC	**IDT**
5962-87630/B	54FCT244/A
5962-87629/C	54FCT245/A
5962-86862/A	54FCT299/A
5962-87644/A	54FCT373/A
5962-87628/C	54FCT374/A
5962-87627	54FCT377/A
5962-87654/A	54FCT138/A
5962-87655	54FCT240/A
5962-87656/A	54FCT273/A
5962-89533	54FCT861A/B
5962-89506	54FCT827A/B
5962-88575	54FCT841A/B
5962-88608	54FCT821A/B
5962-88543/A	54FCT521/A
5962-88640	54FCT161/A
5962-88639	54FCT573/A
5962-88656	54FCT823A/B
5962-88657	54FCT163/A
5962-88674	54FCT825A/B
5962-88661	54FCT863A/B
5962-88736	54FCT520A/B
5962-88775	54FCT646A/B
5962-89508	54FCT139/A
5962-89665	54FCT824A/B
5962-88651	54FCT533/A
5962-88652	54FCT182/A
5962-88653	54FCT645A/B
5962-88654	54FCT640A/B
5962-88655	54FCT534/A
5962-89767	54FCT540/A
5962-89766	54FCT541/A
5962-89733	54FCT191/A
5962-89732	54FCT241/A
5962-89652	54FCT399/A
5962-89513	54FCT574/A
5962-89731	54FCT833A/B
5962-88675	54FCT845A/B
5962-89730	54FCT543/A

SMD	
CLP	**IDT**
5962-87708/A	39C10B & C
5962-88535	39C01
5962-88533/A	49C460A
5962-88613	39C60A
5962-88643	49C410
5962-88743	75C48S
5962-XXXXX	75C58
5962-XXXXX	75C458S
5962-89517	49C402/A
5962-86893	7216L
5962-87686	7217L
5962-88733	7210
5962-XXXXX	49C402L
5962-XXXXX	7320L
5962-XXXXX	7321L
5962-XXXXX	7383L
5962-XXXXX	7209L

2509 tbl 01

RADIATION HARDENED TECHNOLOGY

IDT manufactures and supplies radiation hardened products for military/aerospace applications. Utilizing special processing and starting materials, IDT's radiation hardened devices are able to survive in hostile radiation environments. In total dose, dose rate and environments where single event upset is of concern, IDT products are designed to continue functioning without loss of performance. IDT can supply all its products on these processes. Total Dose radiation testing is performed in-house on an ARACOR X-Ray system. External facilities are utilized for device research on gamma cell, LINAC and other radiation equipment. IDT has an on-going research and development program for improving radiation handling capabilities (See "IDT Radiation Tolerant/Enhanced Products for Radiation Environments" in Section 3) of IDT products/ processes.

IDT LEADING EDGE CEMOS TECHNOLOGY

HIGH-PERFORMANCE CEMOS

From IDT's beginnings in 1980, it has had a belief in and a commitment to CMOS. The company developed a high-performance version of CMOS, called enhanced CMOS (CEMOS), that allows the design and manufacture of leading-edge components. It incorporates the best characteristics of traditional CMOS, including low power, high noise immunity and wide operating temperature range; it also achieves speed and output drive equal or superior to bipolar Schottky TTL. The last decade has seen development and production of four "generations" of IDT's CEMOS technology with process improvements which have reduced IDT's electrical effective (Leff) gate lengths by more than 50 percent from 1.3 microns (millionths of a meter) in 1981 to 0.6 microns in 1989.

	CEMOS I	CEMOS II		CEMOS III	CEMOS V	CEMOS VI
		A	C			
Calendar Year	**1981**	**1983**	**1985**	**1987**	**1989**	**1990**
Drawn Feature Size	2.5μ	1.7μ	1.3μ	1.2μ	1.0μ	0.8μ
Leff	1.3μ	1.1μ	0.9μ	0.8μ	0.6μ	0.45μ
Basic Proces Enhancements	Dual-well, Wet Etch, Projection Aligned	Dry Etch, Stepper	Shrink, Spacer	Silicide, BPSG, BiCEMOS I	BiCEMOS II	BiCEMOS III

2514 drw 01

CEMOS IV = CEMOS III – scaled process optimized for high-speed logic.

Figure 1.

Continual advancement of CEMOS technology allows IDT to implement progressively higher levels of integration and achieve increasingly faster speeds maintaining the company's established position as the leader in high-speed CMOS integrated circuits. In addition, the fundamental process technology has been extended to add bipolar elements to the CEMOS platform. IDT's BiCEMOS process combines the ultra-high speeds of bipolar devices with the lower power and cost of CMOS, allowing us to build even faster components than straight CMOS at a slightly higher cost.

SEM photos (miniaturization) 2514 drw 02

Figure 2. Fifteen-Hundred-Power Magnification Scanning Electron Microscope (SEM) Photos of the Four Generations of IDT's CEMOS Technology

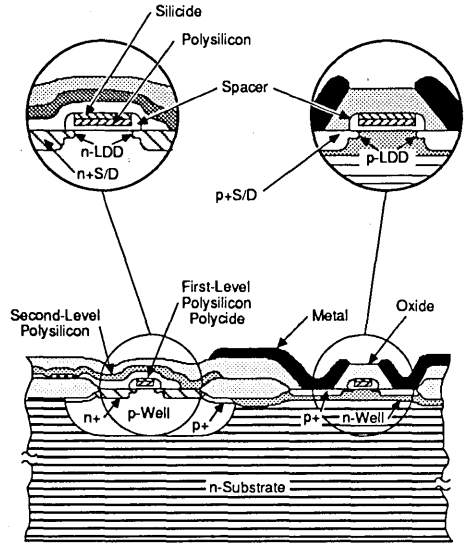


Figure 3. IDT CEMOS Device Cross Section

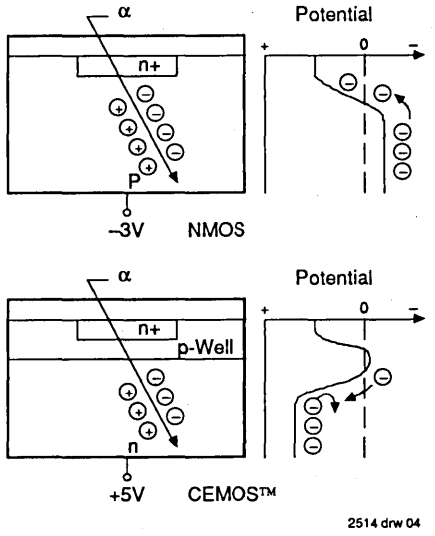


Figure 4. IDT CEMOS Built-In High Alpha Particle Immunity

ALPHA PARTICLES

Random alpha particles can cause memory cells to temporarily lose their contents or suffer a "soft error." Traveling with high energy levels, alpha particles penetrate deep into an integrated chip. As they burrow into the silicon, they leave a trail of free electron-hole pairs in their wake.

The cause of alpha particles is well documented and understood in the industry. IDT has considered various techniques to protect the cells from this hazardous occurrence. These techniques include dual-well structures (Figures 3 and 4) and a polymeric compound for die coating. Presently, a polymeric compound is used in many of IDT's SRAMs; however, the specific techniques used may vary and change from one device generation to the next as the industry and IDT improve the alpha particle protection technology.

LATCHUP IMMUNITY

A combination of careful design layout, selective use of guard rings and proprietary techniques have resulted in virtual elimination of latchup problems often associated with older CMOS processes (Figure 5). The use of NPN and N-channel I/O devices eliminates hole injection latchup. Double guard ring structures are utilized on all input and output circuits to absorb injected electrons. These effectively cut off the current paths into the internal circuits to essentially isolate I/O circuits. Compared to older CMOS processes which exhibit latchup characteristics with trigger currents from 10-20mA, IDT products inhibit latchup at trigger currents substantially greater than this.

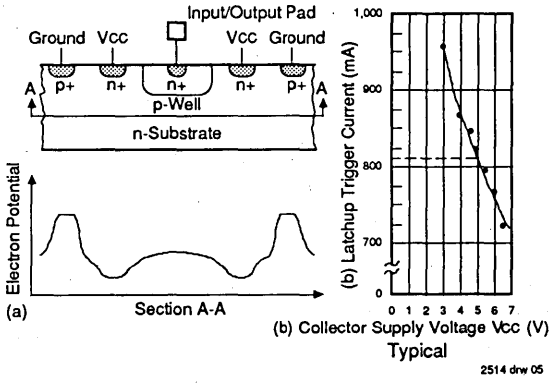


Figure 5. IDT CEMOS Latchup Suppression

SURFACE MOUNT TECHNOLOGY AND IDT'S MODULE PRODUCTS

Requirements for circuit area reduction, utilizing the most efficient and compact component placement possible and the needs of production manufacturing for electronics assemblies are the driving forces behind the advancement of circuit-board assembly technologies. These needs are closely associated with the advances being made in surface mount devices (SMD) and surface mount technology (SMT) itself. Yet, there are two major issues with SMT in production manufacturing of electronic assemblies: high capital expenditures and complexity of testing.

The capital expenditure required to convert to efficient production using SMT is still too high for the majority of electronics companies, regardless of the 20-60% increase in the board densities which SMT can bring. Because of this high barrier to entry, we will continue to see a large market segment [large even compared to the exploding SMT market] using traditional through-hole packages (i.e. DIPs, PGAs, etc) and assembly techniques. How can these types of companies take advantage of SMD and SMT? Let someone else, such as IDT, do it for them by investing time and money in SMT and then in return offer through-hole products utilizing SMT processes. Products which fit this description are multi-chip modules, consisting of SMT assembled SMDs on a through-hole type substrate. Modules enable companies to enjoy SMT density advantages and traditional package options without the expensive startup costs required to do SMT in-house.

Although subcontracting this type of work to an assembly house is an alternative, there still is the other issue of testing, an area where many contract assembly operations fall short of IDT's capability and experience. Prerequisites for adequate module testing sophisticated high performance parametric testers, customized test fixtures, and most importantly the experience to tests today's complex electronic devices. Companies can therefore take advantage of IDT's experience in testing and manufacturing high performance CMOS multi-chip modules.

At IDT, SMD components are electrically tested, environmentally screened, and performance selected for each IDT module. All modules are 100% tested as if they are a separate functional component and are guaranteed to meet all specified parameters at the module output without the customer having to understand the modules' internal workings.

Other added benefits companies get by using IDT's CMOS module products are:

1) a wide variety of high performance, through-hole products utilizing SMD packaged components,
2) fast speeds compared with NMOS based products,
3) low power consumption compared with bipolar technologies, and
4) low cost manufacturability compared with GaAs based products.

IDT has recognized the problems of SMT and began offering CMOS modules as part of its standard product portfolio. IDT modules combine the advantages of:

1) the low power characteristics of IDT's CEMOS™ and BiCEMOS™ products,
2) the density advantages of first class SMD components including those from IDT's components divisions, and
3) experience in system level design, manufacturing, and testing with its own in-house SMT operation.

IDT currently has two divisions (Subsystems and RISC Subsystems) dedicated to the development of module products ranging from simple memory modules to complex VME sized application specific modules to full system level CPU boards. These modules have surface mount devices assembled on both sides of either a multi-layer glass filled epoxy (FR-4) or a multi-layer co-fired ceramic substrate. Assembled modules come available in industry standard through-hole packages and other space-saving module packages. Industry proven vapor-phase or IR reflow techniques are used to solder the SMDs to the substrate during the assembly process. Because of our affiliation with IDT's experienced semiconductor manufacturing divisions, we thoroughly understand and therefore test all modules to the applicable datasheet specifications and customer requirements.

Thus, IDT is able to offer today's electronic design engineers a unique solution for their "need-more-for-less" problem modules. These high speed, high performance products offer the density advantages of SMD and SMT, the added benefit of low power CMOS technology, and through-hole packaged electronics without the high cost of doing it in-house.

STATE-OF-THE-ART FACILITIES AND CAPABILITIES

Integrated Device Technology is headquartered in Santa Clara, California — the heart of the "Silicon Valley." The company's operations are housed in seven facilities totaling over 500,000 square feet. These facilities house all aspects of business from research and development to design, wafer fabrication, assembly, environmental screening, test and administration. In-house capabilities include scanning electron microscope (SEM) evaluation, particle impact noise detection (PIND), plastic and hermetic packaging, military and commercial testing, burn-in, life test and a full complement of environmental screening equipment.

The over-200,000-square-foot corporate headquarters campus is composed of four buildings. The largest facility on this site is a 100,000 square foot, two-building complex. The first building, a 60,000 square foot facility, is dedicated to the Complex Logic, Standard Logic and RISC Microprocessor product lines, as well as hermetic and plastic package assembly, logic products' test, burn-in, mark and QA, and a reliability/failure analysis lab.

IDT's Packaging and Assembly Process Development teams are located here. To keep pace with the development of new products and to enhance the IDT philosophy of "Innovation," these teams have ultra modern, integrated and correspondingly sophisticated equipment and environments at their disposal. All manufacturing is completed in dedicated clean room areas (Class 10K minimum), with all preseal operations accomplished under Class 100 laminar flow hoods.

Development of assembly materials, processes and equipment is accomplished under a fully operational production environment to ensure reliability and repeatable product. The Hermetic Manufacturing and Process Development team is currently producing custom products to the strict requirements of MIL-STD-883. The fully automated plastic facility is currently producing high volumes of USA-manufactured product, while developing state-of-the-art surface mount technology patterned after MIL-STD-883.

The second building of the complex houses sales, marketing, finance and MIS.

The RISC Subsystems and Subsystems Modules Divisions are located behind the two-building complex in a 54,000 square foot facility. Also located at this facility are Quality Assurance and wafer fabrication services.

Directly across the street from the two-building complex is a newly acquired 50,000 square foot facility that houses administrative services, Northwest Area Sales, Human Resources, International Planning and Shipping and Receiving functions.

IDT's largest and newest facility, opened in 1990 in San Jose, California, is a multi-purpose 150,000 square foot, ultra modern technology development center. This facility houses a 25,000 square foot, combined Class 1 (a maximum of one particle per cubic foot of 0.2 micron or larger), sub-half-micron R&D fabrication facility and a wafer fabrication area. This fab supports both production volumes of IDT products, including some next generation SRAMs, and the R&D efforts of the technology development staff. Technology development efforts targeted for the center include advanced silicon processing and wafer fabrication techniques. A test area to support both production and research is located on-site. The building is also the new home of the FIFO and ECL product lines.

IDT's second largest facility is located in Salinas, California, about an hour away from Santa Clara. This 95,000 square foot facility, located on 14 acres, is the Static RAM Division and Specialty Memory product line. Constructed in 1985, this facility houses an ultra-modern 25,000 square foot high-volume wafer fabrication area measured at Class 2-to-3 (a maximum of 2 to 3 particles per cubic foot of 0.2 micron or larger) clean room conditions. Careful design and construction of this fabrication area created a clean room environment far beyond the 1985 average for U.S. fab areas. This made possible the production of large volumes of high-density submicron geometry, fast static RAMs. This facility also houses shipping areas for IDT's leadership family of CMOS static RAMs. This site will expand to accommodate a 250,000 square foot complex.

To extend these philosophies while maintaining strict control of our processes, IDT has an operational Assembly and Test facility located in Penang, Malaysia. This facility assembles product to USA standards, with all assemblies done under laminar flow conditions (Class 100) until the silicon is encased in its final packaging. All products in this facility are manufactured to the quality control requirements of MIL-STD-883.

All of IDT's facilities are aimed at increasing our manufacturing productivity to supply ever larger volumes of high-performance, cost-effective leadership CMOS products.

SUPERIOR QUALITY AND RELIABILITY

Maintaining the highest standards of quality in the industry on all products is the basis of Integrated Device Technology's manufacturing systems and procedures. From inception, quality and reliability are built into all of IDT's products. Quality is "designed in" at every stage of manufacturing – as opposed to being "tested-in" later – in order to ensure impeccable performance.

Dedicated commitment to fine workmanship, along with development of rigid controls throughout wafer fab, device assembly and electrical test, create inherently reliable products. Incoming materials are subjected to careful inspections. Quality monitors, or inspections, are performed throughout the manufacturing flow.

IDT military grade monolithic hermetic products are designed to meet or exceed the demanding Class B reliability levels of MIL-STD-883 and MIL-M-38510, as defined by Paragraph 1.2.1 of MIL-STD-883.

Product flow and test procedures for all monolithic hermetic military grade products are in accordance with the latest revision and notice of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with tight controls and inspections to ensure that products meet the requirements for 100% screening. Routine quality conformance lot testing is performed as defined in MIL-STD-883, Methods 5004 and 5005.

For IDT module products, screening of the fully assembled substrates is performed, in addition to the monolithic level screening, to assure package integrity and mechanical reliability. All modules receive 100% electrical tests (DC, functional and dynamic switching) to ensure compliance with the "subsystem" specifications.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that commercial, industrial and military grade products consistently meet customer requirements for quality, reliability and performance.

SPECIAL PROGRAMS

Class S. IDT also has all manufacturing, screening and test capabilities in-house (except X-ray and some Group D tests) to perform complete Class S processing per MIL-STD-883 on all IDT products and has supplied Class S products on several programs.

Radiation Hardened. IDT has developed and supplied several levels of radiation hardened products for military/aerospace applications to perform at various levels of dose rate, total dose, single event upset (SEU), upset and latchup. IDT products maintain nearly their same high-performance levels built to these special process requirements. The company has in-house radiation testing capability used both in process development and testing of deliverable product. IDT also has a separate group within the company dedicated to supplying products for radiation hardened applications and to continue research and development of process and products to further improve radiation hardening capabilities.

QSP–QUALITY, SERVICE AND PERFORMANCE

Quality from the beginning, is the foundation for IDT's commitment to supply consistently high-quality products to our customers. IDT's quality commitment is embodied in its all pervasive Constant Quality Improvement (CQI) program. Everyone who influences the quality of the product–from the designer to the shipping clerk–is committed to constantly improving the product quality.

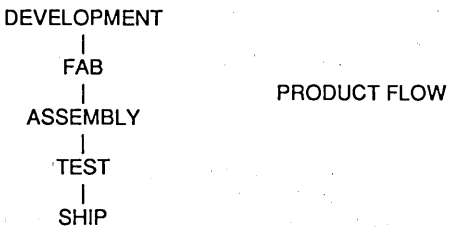
LOGIC PRODUCTS DIVISION'S FOCUS

"To make quantitative constant improvement in the quality of our actions that result in the supply of leadership products in conformance to the requirements of our customers."

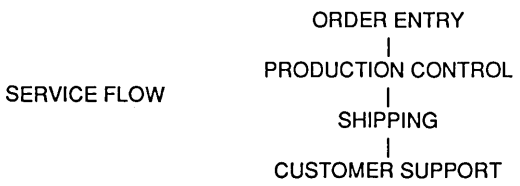
IDT's Logic Products Division has dedicated its efforts to constant quantitative improvements in quality. The result, a supply of leadership products that conform to the requirements of our customers.

LOGIC PRODUCTS DIVISION'S PRODUCT ASSURANCE STRATEGY FOR CQI

Measurable standards are essential to the success of CQI. All the processes contributing to the final quality of the product need to be monitored, measured and improved upon through the use of statistical tools.



Our customers receive the benefit of our optimized systems. Installed to enhance quality and reliability, these systems provide accurate and timely reporting on the effectiveness of manufacturing controls and the reliability and quality performance of IDT logic products and services.



These systems and controls concentrate on CQI by focusing on the following key elements:

Statistical Techniques
Using statistical techniques, including Statistical Process Control (SPC) to determine whether the product/ processes are under control.

Standardization
Implementing policies, procedures and measurement techniques that are common across different operational areas.

Documentation
Documenting and training in policies, procedures, measurement techniques and updating through characterization/ capability studies.

Productivity Improvement
Using constant improvement teams made up from employees at all levels of the organization.

Leadership
Focusing on quality as a key business parameter and strategic strength.

Total Employee Participation
Incorporating the CQI program into the IDT Corporate Culture.

Customer Service
Supporting the customer, as a partner, through performance review and pro-active problem solving.

People Excellence
Committing to growing, motivating and retaining people through training, goal setting, performance measurement and review.

PRODUCT FLOW

Product quality starts here. IDT has mechanisms and procedures in place that monitor and control the quality of our development activities. From the calibration of design capture libraries through process technology and product characterization that establish whether the performance, ratings and reliability criteria have been met. This includes failure analysis of parts that will improve the prototype product.

At the pre-production stage once again in-house qualification tests assure the quality and reliability of the product. All specifications and manufacturing flows are established and personnel trained before the product is placed into production.

Manufacturing

To make CQI during the manufacturing stage, control items are determined for major manufacturing conditions. Data is gathered and statistical techniques are used to control specific manufacturing processes that affect the quality of the product.

In-process and final inspections are fed back to earlier processes to improve product quality. All product is burned-in (where applicable) before 100% inspection of electrical characteristics takes place.

Products which pass final inspection are then subject to Quality Assurance and Reliability Tests. This data is used to improve manufacturing processes and provide reliability predictions of field applications.

Inventory and Shipping

Controls in shipping focus on ensuring parts are identified and packaged correctly. Care is also taken to see that the correct paperwork is present and the product being shipped was processed correctly.

SERVICE FLOW

Quality not only applies to the product but to the quality -of -service we give our customers. Services is also constantly improved.

Order Procedures

Checks are made at the order entry stage to ensure the correct processing of the Customer's product. After verification and data entry the Acknowledgements (sent to Customers) are again checked to ensure details are correct. As part of the CQI program, the results of these verifications are analyzed using statistical techniques and corrective actions are taken.

Production Control

Production Control (P.C.) is responsible for the flow and logistics of material as it moves through the manufacturing processes. The quality of the actions taken by P.C. greatly impinges on the quality of service the customer receives. Because many of our customers have implemented Just-in-Time (JIT) manufacturing practices, IDT as a supplier also has to adopt these same disciplines. As a result, employees receive extensive training and the performance level of key actions are kept under constant review. These key actions include:

Quotation response and accuracy.
Scheduling response and accuracy.
Response and accuracy of Expedites.
Inventory, management, and effectiveness.
On time delivery.

Customer Support

IDT has a worldwide network of sales offices and Technical Development Centers. These provide local customer support on business transactions, and in addition, support customers on applications information, technical services, benchmarking of hardware solutions, and demonstration of various Development Workstations.

The key to CQI is the timely resolution of defects and implementation of the corrective actions. This is no more important than when product failures are found by a customer. When failures are found at the customer's incoming inspection, in the production line, or the field application, the Logic Products Division Quality Assurance group is the focal point for the investigation of the cause of failure and implementation of the corrective action. IDT constantly improves the level of support we give our customers by monitoring the response time to customers that have detected a product failure. Providing the customer with an analysis of the failure, including corrective actions and the statistical analysis of defects, brings CQI full circle–full support of our customers and their designs with high-quality products.

SUMMARY

In 1990, IDT made the commitment to *"Leadership through Quality, Service, and Performance Products"*.

We believe by following that credo IDT and our cusotmers will be successful in the coming decade. With the implementation of the CQI strategy within the Logic Products Division, we will satisfy our goal...

"Leadership through Quality, Service and Performance Products".

IDT QUALITY CONFORMANCE PROGRAM

A COMMITMENT TO QUALITY

Integrated Device Technology's monolithic and modular assembly products are designed, manufactured and tested in accordance with the strict controls and procedures required by Military Standards. The documentation, design and manufacturing criteria of the Quality and Reliability Assurance Program were developed and are being maintained to the most current revisions of MIL-38510 as defined by paragraph 1.2.1 of MIL-STD-883 and MIL-STD-883 requirements.

Product flow and test procedures for all Class B *monolithic* hermetic Military Grade microcircuits are in full compliance with paragraph 1.2.1 of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with stringent controls and inspections to ensure that products meet the requirements for 100% screening and quality conformance tests as defined in MIL-STD-883, Methods 5004 and 5005.

Product flow and test procedures for all *plastic* and *commercial hermetic* products are in accordance with industry practices for producing highly reliable microcircuits to ensure that products meet the IDT requirements for 100% screening and quality conformance tests.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that our products consistently meet customer requirements for quality, reliability and performance.

SUMMARY

Monolithic Hermetic Package Processing Flow[1]

Refer to the Monolithic Hermetic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

   Wafers from each wafer fabrication area are subjected to Scanning Electron Microscope analysis on a periodic basis.

2. **Die-Sort Visual Inspection:** Wafers are cut and separated and the individual die are 100% visually inspected to strict IDT-defined internal criteria.

3. **Die Shear Monitor:** To ensure die attach integrity, product samples are routinely subjected to a shear strength test per Method 2019.

4. **Wire Bond Monitor:** Product samples are routinely subjected to a strength test per Method 2011, Condition D, to ensure the integrity of the lead bond process.

5. **Pre-Cap Visual:** Before the completed package is sealed, 100% of the product is visually inspected to Method 2010, Condition B criteria.

6. **Environmental Conditioning:** 100% of the sealed product is subjected to environmental stress tests. These thermal and mechanical tests are designed to eliminate units with marginal seal, die attach or lead bond integrity.

7. **Hermetic Testing:** 100% of the hermetic packages are subjected to fine and gross leak seal tests to eliminate marginally sealed units or units whose seals may have become defective as a result of environmental conditioning tests.

8. **Pre-Burn-In Electrical Test:** Each product is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.

9. **Burn-In:** 100% of the Military Grade product is burned-in under dynamic electrical conditions to the time and temperature requirements of Method 1015, Condition D. Except for the time, Commercial Grade product is burned-in as applicable to the same conditions as Military Grade devices.

10. **Post-Burn-In Electrical:** After burn-in, 100% of the Class B Military Grade product is electrically tested to IDT data sheet or customer specifications over the –55°C to +125°C temperature range. Commercial Grade products are sample tested to the applicable temperature extremes.

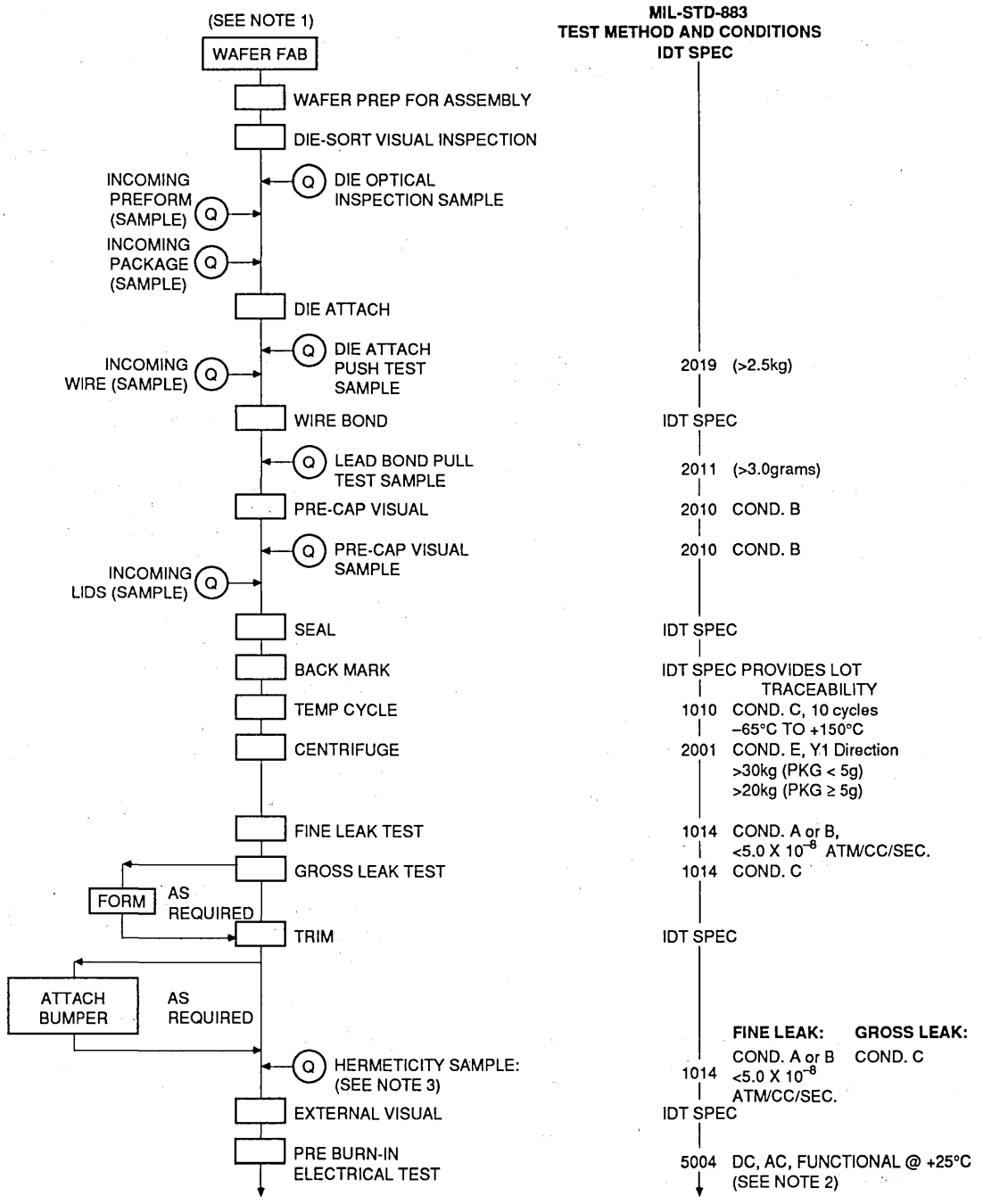
11. **Mark:** All product is marked with product type and lot code identifiers. MIL-STD-883 compliant Military Grade products are identified with the required compliant code letter.

12. **Quality Conformance Tests:** Samples of the Military Grade product which have been processed to the 100% screening tests of Method 5004 are routinely subjected to the quality conformance requirements of Method 5005.

NOTE:

1. For quality requirements beyond Class B levels such as SEM analysis, X-Ray inspection, Particle Impact Noise Reduction (PIND) test, Class S screening or other customer specified screening flows, please contact your Integrated Device Technology sales representative.

Monolithic Hermetic Package Processing Flow



2502 drw 01

SUMMARY

Monolithic Plastic Package Processing Flow

Refer to the Monolithic Plastic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

   Topside silicon nitride passivation is all applied to all wafers for better moisture barrier characteristics.

   Wafers from each wafer fabrication area are subjected to Scanning Electron Microscope analysis on a periodic basis.

2. **Die-Sort Visual Inspection:** Wafers are 100% visually inspected to strict IDT defined internal criteria.

3. **Die Push Test:** To ensure die attach integrity, product samples are routinely subjected to die push tests.

4. **Wire Bond Monitor:** Product samples are routinely subjected to wire bond pull tests to ensure the integrity of the lead bond process.

5. **Pre-Cap Visual:** Before the package is molded, 100% of the product is visually inspected to criteria patterned after MIL-STD-883, Method 2010, Condition B.

6. **Post Mold Cure:** Plastic encapsulated devices are baked to ensure an optimum plastic seal so as to enhance moisture barrier characteristics.

7. **Pre-Burn-In Electrical:** Each product is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.

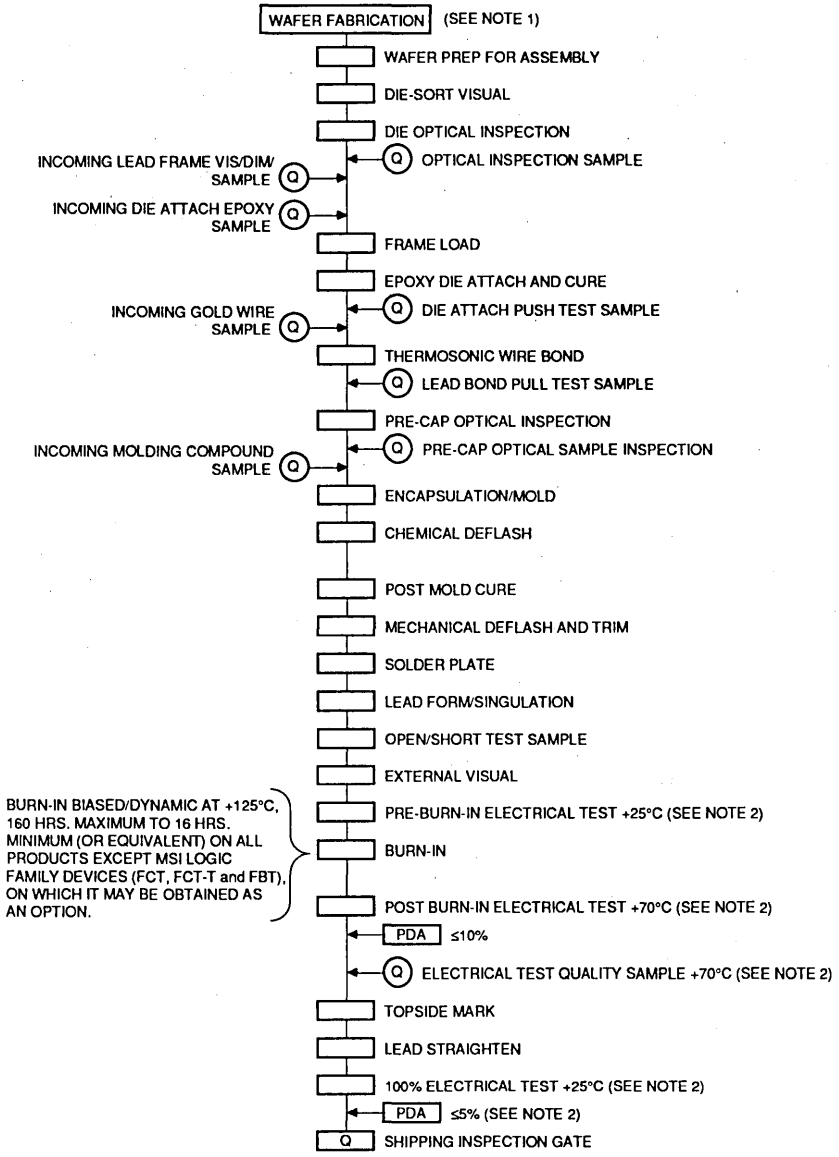
8. **Burn-In:** Except for MSI Logic family devices where it may be obtained as an option, all Commercial Grade plastic package products are burned-in 16 hours at +125°C (or equivalent), utilizing the same burn-in conditions as the Military Grade product.

9. **Post-Burn-In Electrical:** After burn-in, 100% of the plastic product is electrically tested to IDT data sheet or customer specifications at the maximum temperature extreme. The minimum temperature extreme is tested periodically on an audit basis.

10. **Mark:** All product is marked with product type and lot code identifiers.

11. **Quality Conformance Inspection:** Samples of the plastic product which have been processed to the 100% screening requirements are subjected to the Periodic Quality Conformance Inspection Program. Where indicated, the test methods are patterned after MIL-STD-883 criteria.

Monolithic Plastic Package Processing Flow



NOTE:
1. All screens are 100% unless otherwise noted.
2. All electrical test programs are per the applicable IDT test specification.
3. IDT performs a 100% electrical test at +25°C with a 5% PDA limit at this point.
4. (Q) = Quality sample inspection.

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Monolithic Hermetic Package Final Processing Flow

Operation	MIL-STD-883 Test Method	Military Compliant Class B	Commercial	
			Military Temp. Range	Commercial Temp. Range
Burn-In	1015/D at +125°C Min. or Equivalent	100% 160 Hours	100% 16 to 160 Hours	100% 16to160 Hours
Post Burn-In Electrical: Static (DC), Functional and Switching (AC)[2]	IDT Spec.	100% +25, -55 and +125°C	100% +125°C	100% +70°C
Percent Defective Allowed (PDA)[4]	5004 or IDT Spec.	5%	10%	10%
Group A Electrical: Static (DC), Functional and Switching (AC)[2]	5005 and IDT Spec.	Sample -55 and +125°C	Sample +125°C	Sample +70°C
Mark/Lead Straighten	IDT Spec.	100%	100%	100%
+25°C Electrical[2]	IDT Spec.	100%[5]	100%	100%
Final Visual/Pack	IDT Spec.	100%	100%	100%
Quality Conformance Inspection	5005 (Group B, C, D)	Yes	—	—
Quality Shipping Inspection (Visual/Plant Clearance)	IDT Spec.	Sample	Sample	Sample

2505 tbl 01

NOTES:
1. All screens are 100% unless otherwise noted.
2. All electrical test programs are per the applicable IDT test specification.
3. This hermeticity sample is performed after all lead finish operations.
4. If a lot fails the 5% PDA but is ≤10%, the lot may be resubmitted to burn-in one time only to the same time and temperature conditions as first submission. The subsequent post burn-in electrical test at +25°C will be performed to a PDA of 3%.
5. IDT performs a 100% electrical test at +25°C with a 2% PDA limit at this point to satisfy group A requirements, and considers this to be equivalent to the group A requirement of an LTPD of 2, with an accept number of 0. If a lot fails the 2% PDA limit, it may be rescreened one time only to a tightened PDA limit of 1.5%.
6. (Q) = Quality sample inspection.

MODULE SURFACE MOUNT ASSEMBLY PROCESSING FLOW[1]

Refer to the Module Assembly Package Processing Flow diagrams Figures 1 and 2 for additional information. All test methods refer to MIL-STD-883 unless otherwise stated. Refer to Table 1 for additional information on module testing.

HERMETIC FLOW

Components

1. Hermetic Military Grade Class B monolithic microcircuit components used in Subsystems modules are manufactured to the applicable datasheet specifications and screened in compliance with the applicable Mil-Std-883 quality criteria.
2. Hermetic Military Grade Class S and Rad Hard monolithic microcircuit components available upon request. Please consult your IDT sales representative for additional information regarding these non-standard process and quality flows
3. Hermetic Commercial Grade monolithic microcircuit products used in Subsystems modules differ from Military Grade components only in the time of burn-in and electrical test temperature ranges.
4. Passive components such as chip capacitors, resistors are obtained from qualified vendors to the applicable military and IDT specifications.

Modules

1. Module Assembly: The active and passive components and substrates used in the assembly of modules are subjected to incoming electrical and mechanical inspection per IDT's requirements. The components are then mounted onto a co-fired multi-layer ceramic substrate using either vapor phase or IR reflow techniques.
2. Pre-Burn-In Electrical Test: Every module is electrically tested (Static "DC", Functional "AC", and Dynamic Switching "AC"; hereafter simply referred to as Electrical Testing) at an ambient temperature of +25°C to IDT datasheet parameter specification or to customer specification.
3. Burn-In: All Military Grade modules are burned-in under conditions per Mil-Std-883, Method 1015, Condition D, for 44 +/- 4 hours at an ambient temperature of +125°C. Commercial grade modules are not burned-in.
4. Post-Burn-In Electrical & PDA Calculation: Results of a +25°C post burn-in Electrical test are used to calculate a PDA (Percent Defective Allowed) on the entire module lot. A maximum of 10% is imposed on all Military modules. Commercial grade modules are not burned-in and therefore PDA requirements are not applicable.
5. Post-Burn-In Electrical: All Class B Military Grade modules are Electrically Tested to IDT datasheet specification or customer specification at the military temperature limits of -55 °C and +125°C. Commercial grade products are tested to the commercial temperatures of +25°C and +70°C.
6. QA Electrical Test Audit: A sample of Military grade modules are taken after each Electrical Test (at either temperature extreme) and subjected to a Quality Conformance Electrical Audit at -55 °C and +125°C with a LTPD 7/1, in accordance to Mil-Std-883 requirements. Commercial grade modules are sampled tested at +70 °C to the same LTPD of 7/1.
7. Mark: All electrically acceptable modules are marked with product type and lot code identifiers. Military Grade products are identified with the required compliancy code letter as specified in Mil-Std-883, unless otherwise specified by customer.
8. 100% Group A & Final Electrical: A Final Electrical Test at +25°C is imposed on all modules with a 5% PDA limit to satisfy Mil-Std-883 Group A requirements.
9. External Visual: Prior to shipment, all modules undergo a final visual inspection for applicable workmanship criteria per IDT's specification.
10. Quality Conformance Tests: Samples of the Military Grade modules are routinely subjected to Quality Conformance Inspections requiring ongoing quality data for Mil-Std-883 Test Methods Group B, C, and D (only when such tests are applicable to module level parameters). This data is available upon request.

NOTE:

1. For special processing or additional quality requirements beyond those mentioned above, such as SEM analysis, X-ray inspection, Particle Impact Noise Detection (PIND) test, or other customer specified screening flows, please contact your IDT sales representative.

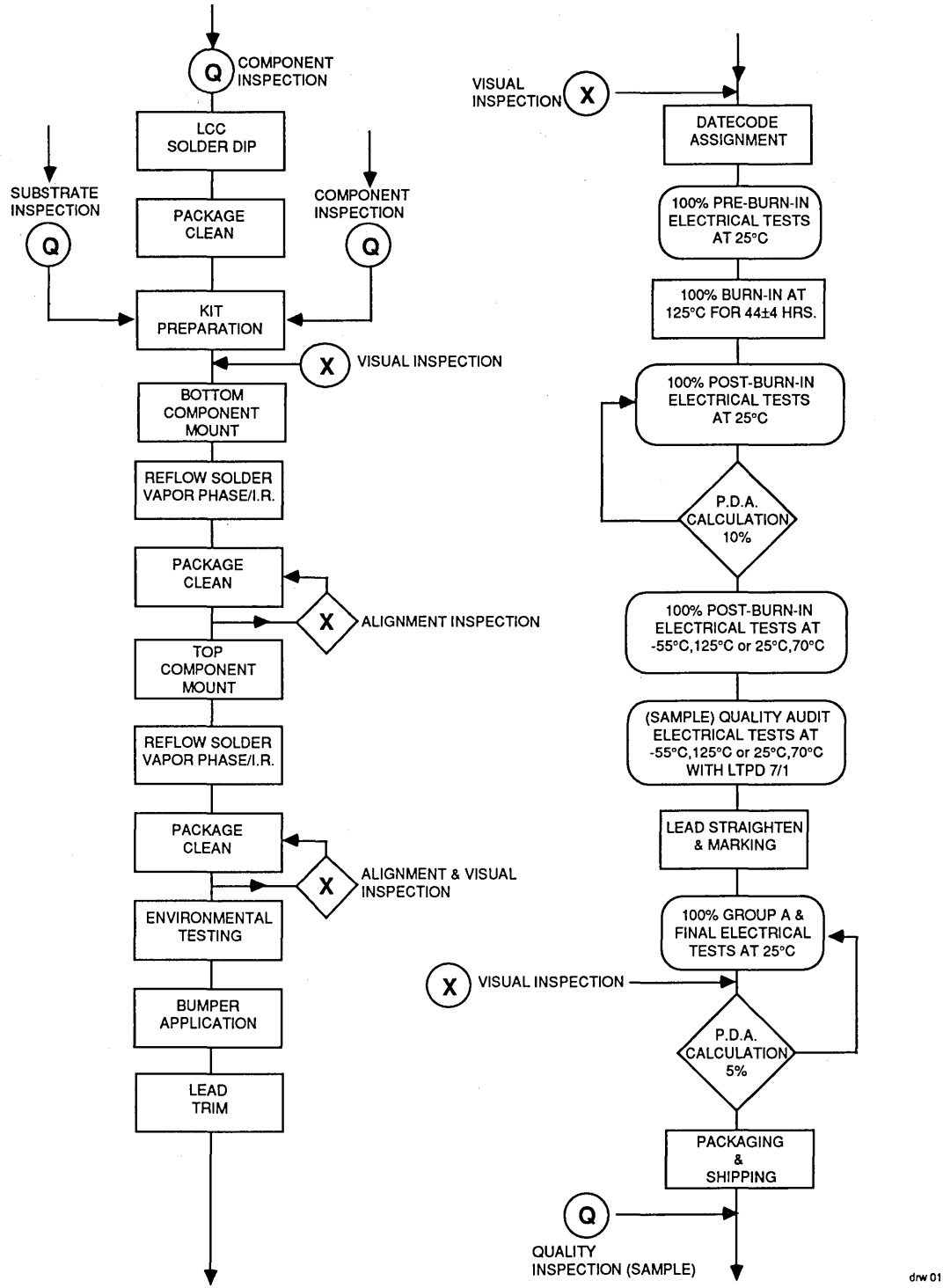
NON-HERMETIC FLOW

Components

1. Non-Hermetic or Plastic Commercial Grade monolithic microcircuit products used in Subsystems modules are manufactured to the applicable datasheet specifications and screened to the applicable IDT Quality Conformance requirements.
2. Passive components such as chip capacitors, resistors are obtained from qualified vendors to the applicable commercial and IDT specifications.

Modules

1. Module Assembly: The active and passive components and substrates used in the assembly of modules are subjected to incoming electrical and mechanical inspection per IDT's requirements. The components are then mounted onto a glass filled epoxy (FR-4) multi-layer substrate using either vapor phase or IR reflow techniques.
2. Electrical Test: Every module is electrically tested (Static "DC", Functional "AC", and Dynamic Switching "AC"; hereafter simply refered to as Electrical Testing) at an ambient temperature of +25°C to IDT datasheet parameter specification or to customer specification.
3. Electrical Test: All Commercial Grade modules are Electrically Tested to IDT datasheet specifications or customer specifications at commercial temperatures of +25°C and +70°C.
6. QA Electrical Test Audit: A sample of modules are taken and subjected to a Quality Conformance Electrical Audit at +25 °C and +70°C with a LTPD 7/1. This is patterned after Mil-Std-883 requirements.
7. Mark: All electrically acceptable modules are marked with product type and lot code identifiers, unless otherwise specified by customer.
8. 100% Group A & Final Electrical: A Final Electrical Test at +25°C is imposed on all modules at this stage of processing with a 5% PDA limit.
9. External Visual: Prior to shipment, all modules undergo a final visual inspection for applicable workmanship criteria per IDT's specification.


Q
COMPONENT INSPECTION
LCC SOLDER DIP
SUBSTRATE INSPECTION
Q
PACKAGE CLEAN
COMPONENT INSPECTION
Q
KIT PREPARATION
X
VISUAL INSPECTION
BOTTOM COMPONENT MOUNT
REFLOW SOLDER VAPOR PHASE/I.R.
PACKAGE CLEAN
X
ALIGNMENT INSPECTION
TOP COMPONENT MOUNT
REFLOW SOLDER VAPOR PHASE/I.R.
PACKAGE CLEAN
X
ALIGNMENT & VISUAL INSPECTION
ENVIRONMENTAL TESTING
BUMPER APPLICATION
LEAD TRIM
VISUAL INSPECTION
X
DATECODE ASSIGNMENT
100% PRE-BURN-IN ELECTRICAL TESTS AT 25°C
100% BURN-IN AT 125°C FOR 44±4 HRS.
100% POST-BURN-IN ELECTRICAL TESTS AT 25°C
P.D.A. CALCULATION 10%
100% POST-BURN-IN ELECTRICAL TESTS AT -55°C,125°C or 25°C,70°C
(SAMPLE) QUALITY AUDIT ELECTRICAL TESTS AT -55°C,125°C or 25°C,70°C WITH LTPD 7/1
LEAD STRAIGHTEN & MARKING
100% GROUP A & FINAL ELECTRICAL TESTS AT 25°C
X
VISUAL INSPECTION
P.D.A. CALCULATION 5%
PACKAGING & SHIPPING
Q
QUALITY INSPECTION (SAMPLE)
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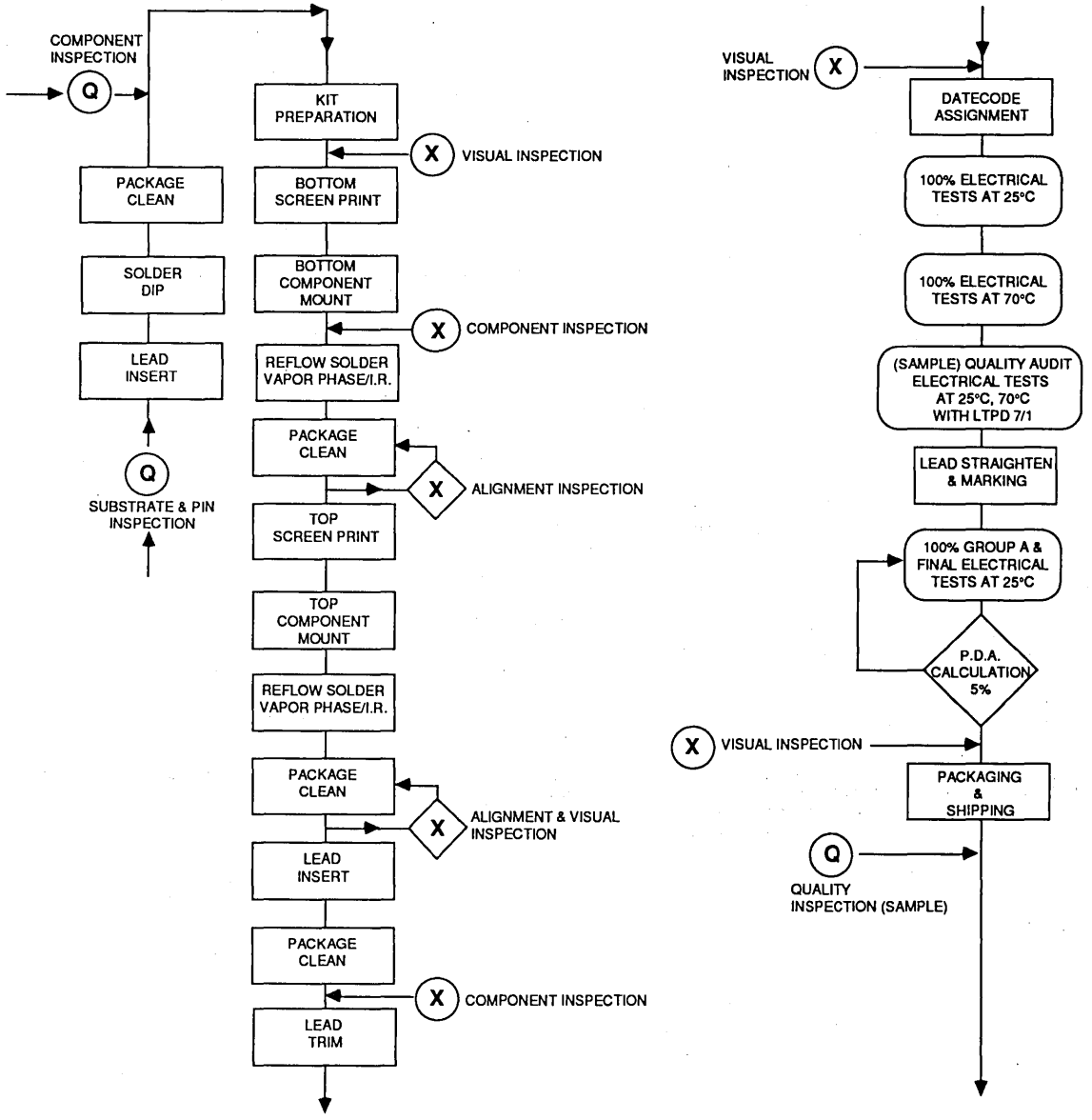

COMPONENT INSPECTION
Q
PACKAGE CLEAN
SOLDER DIP
LEAD INSERT
Q
SUBSTRATE & PIN INSPECTION
KIT PREPARATION
X
VISUAL INSPECTION
BOTTOM SCREEN PRINT
BOTTOM COMPONENT MOUNT
X
COMPONENT INSPECTION
REFLOW SOLDER VAPOR PHASE/I.R.
PACKAGE CLEAN
X
ALIGNMENT INSPECTION
TOP SCREEN PRINT
TOP COMPONENT MOUNT
REFLOW SOLDER VAPOR PHASE/I.R.
PACKAGE CLEAN
X
ALIGNMENT & VISUAL INSPECTION
LEAD INSERT
PACKAGE CLEAN
X
COMPONENT INSPECTION
LEAD TRIM
VISUAL INSPECTION
X
DATECODE ASSIGNMENT
100% ELECTRICAL TESTS AT 25°C
100% ELECTRICAL TESTS AT 70°C
(SAMPLE) QUALITY AUDIT ELECTRICAL TESTS AT 25°C, 70°C WITH LTPD 7/1
LEAD STRAIGHTEN & MARKING
100% GROUP A & FINAL ELECTRICAL TESTS AT 25°C
P.D.A. CALCULATION 5%
X
VISUAL INSPECTION
PACKAGING & SHIPPING
Q
QUALITY INSPECTION (SAMPLE)

drw 02

3

Operation	Test Method	Hermetic Military	Hermetic Commercial	FR-4 Commercial
Pre-Burn-in Electrical Test (Static DC, Function AC and Switching AC]	IDT Data Sheet Specification	100% at +25°C	100% at +25°C	100% at +25°C
Burn-in	MIL-STD-883 Method 1015/D	100% at +25°C for 44 ± 4 Hours	N.A.	N.A.
Post-Burn-in Electrical Test (Static DC, Function AC and Switching AC]	IDT Data Sheet Specification	100% at +25°C	100% at +25°C	100% at +25°C
Percent Defective Allowed (P.D.A.) (See Note 2)	MIL-STD-883 Method 5004	10%	N.A.	N.A.
Post-Burn-in Electrical Test (Static DC, Function AC and Switching AC]	IDT Data Sheet Specification	100% at –55°C and +125°C	100% at +25°C and +70°C	100% at +25°C and +70°C
(Sample) Quality Audit Electrical Test (Static DC, Function AC and Switching AC] (See Note 3)	IDT Specification	Sample at –55°C and +125°C LTPD 7/1	SAMPLE at +25°C and +70°C LTPD 7/1	SAMPLE at +25°C and +70°C LTPD 7/1
Group A and Final Electrical Test (Static DC, Function AC and Switching AC]	IDT Data Sheet Specification	100% at +25°C	100% at +25°C	100% at +25°C
Percent Defective Allowed (P.D.A.) (See Note 4)	IDT Specification	5%	5%	5%
Quality Conformance Inspection) (See Note 5	Reference MIL-STD-883 Method 5005	5%	N.A.	N.A.

tbl 01

NOTES:

1. All Electrical Tests are guard-banded by temperature and voltage and take into account test equipment variations.
2. If a lot fails P.D.A., the lot may be resubmitted (one time only) to burn-in, for the same burn-in specifications. A subsequent post-burn-in retest at 25°C must then pass 5% P.D.A.
3. If a lot fails LTPD 7/1, the lot may be resubmitted (one time only) to test for the same temperatures. This subsequent retest must then pass a 100% critical
4. These test results satisfy Group A requirements and is considered to be equivalent to an LTPD of 5 with an accept number of 1. If this lot fails P.D.A. of 5%, it may be rescreened to (for one time only) to a P.D.A. of 3%.
5. IDT Quality Conformance Inspection is patterned after MIL-STD-883, Method 5005 for monolithic microcircuits requiring periodic data sampling for Group B, C, and D parameters. The new method for multi-chip modules is currently under development by the military.

RADIATION TOLERANT/ENHANCED/HARDENED PRODUCTS FOR RADIATION ENVIRONMENTS

INTRODUCTION

The need for high-performance CMOS integrated circuits in military and space systems is more critical today than ever before. The low power dissipation that is achieved using CMOS technology, along with the high complexity and density levels, makes CMOS the nearly ideal component for all types of applications.

Systems designed for military or space applications are intended for environments where high levels of radiation may be encountered. The implication of a device failure within a military or space system clearly is critical. IDT has made a significant contribution toward providing reliable radiation-tolerant systems by offering integrated circuits with enhanced radiation tolerance. Radiation environments, IDT process enhancements and device tolerance levels achieved are described below.

THE RADIATION ENVIRONMENT

There are four different types of radiation environments that are of concern to builders of military and space systems. These environments and their effects on the device operation, summarized in Figure 1, are as follows:

Total Dose Accumulation refers to the total amount of accumulated gamma rays experienced by the devices in the system, and is measured in RADS (SI) for radiation units experienced at the silicon level. The physical effect of gamma rays on semiconductor devices is to cause threshold shifts (Vt shifts) of both the active transistors as well as the parasitic field transistors. Threshold voltages decrease as total dose is accumulated; at some point, the device will begin to exhibit parametric failures as the input/output and supply currents increase. At higher radiation accumulation levels, functional failures occur. In memory circuits, however, functional failures due to memory cell failure often occur first.

Burst Radiation or Dose Rate refers to the amount of radiation, usually photons or electrons, experienced by the devices in the system due to a pulse event, and is measured in RADS (SI) per second. The effect of a high dose rate or burst of radiation on CMOS integrated circuits is to cause temporary upset of logic states and/or CMOS latch-up. Latch-up can cause permanent damage to the device.

Single Event Upset (SEU) is a transient logic state change caused by high-energy ions, such as energetic cosmic rays, striking the integrated circuits. As the ion passes through the silicon, charge is either created through ionization or direct nuclear collision. If collected by a circuit node, this excess charge can cause a change in logic state of the circuit. Dynamic nodes that are not actively held at a particular logic state (dynamic RAM cells for example) are the most susceptible. These upsets are transient, but can cause system failures known as "soft errors."

Neutron Irradiation will cause structural damage to the silicon lattice which may lead to device leakage and, ultimately, functional failure.

Radiation Category	Primary Particle	Source	Effect
Total Dose	Gamma	Space or Nuclear Event	Permanent
Dose Rate	Photons	Nuclear Event	Temporary Upset of Logic State or Latch-up
SEU	Cosmic Rays	Space	Temporary Upset of Logic State
Neutron	Neutrons	Nuclear Event	Device Leakage Due to Silicon Lattice Damage

2510 drw 01

Figure 1.

DEVICE ENHANCEMENTS

Of the four radiation environments above, IDT has taken considerable data on the first two, Total Dose Accumulation and Dose Rate. IDT has developed a process that significantly improves the radiation tolerance of its devices within these environments. Prevention of SEU failures is usually accomplished by system-level considerations, such as Error Detection and Correction (EDC) circuitry, since the occurrence of SEUs is not particularly dependent on process technology. Through IDT's customer contracts, SEU has been gathered on some devices. Little is yet known about the effects of neutron-induced damage. For more information on SEU testing, contact IDT's Radiation Hardened Product Group.

Enhancements to IDT's standard process are used to create radiation enhanced and tolerant processes. Field and gate oxides are "hardened" to make the device less susceptible to radiation damage by modifying the process architecture to allow lower temperature processing. Device implants and Vts adjustments allow more Vt margin. In addition to process changes, IDT's radiation enhanced process utilizes epitaxial substrate material. The use of epi substrate material provides a lower substrate resistance environment to create latch-up free CMOS structures.

RADIATION HARDNESS CATEGORIES

Radiation Enhanced ('RE) or Radiation Tolerant ('RT) versions of IDT products follow IDT's military product data sheets whenever possible (consult factory). IDT's Total Dose Test plan exposes a sample of die on a wafer to a particular Total Dose level via ARACOR X-Ray radiation. This Total Dose Test plan qualifies each 'RE or 'RT wafer to a Total Dose level. Only wafers with sampled die that pass Total Dose level tests are assembled and used for orders (consult factory for more details on Total Dose sample testing). With regard to Total Dose testing, clarifications/exceptions to MIL-STD-883, Methods 5005 and 1019 are required. Consult factory for more details.

The 'RE and 'RT process enhancements enable IDT to offer integrated circuits with varying grades of radiation tolerance or radiation "hardness".

- Radiation Enhanced process uses Epi wafers and is able to provide Logic devices that can be Total Dose qualified to 10K RADs (Si) or greater by IDT's ARACOR X-Ray Total Dose sample die test plan (Total Dose levels require negotiation, consult factory for more details).
- Radiation Tolerant Logic product uses standard wafer/ process material that is qualified to 10K RADs (Si) Total Dose by IDT's ARACOR X-Ray Total Dose sample die test plan.

Integrated Device Technology can provide Radiation Tolerant/Enhanced versions of all Logic product types (some speed grades may not be available as 'RE).

Please contact your IDT sales representative or factory marketing to determine availability and price of any IDT product processed in accordance with one of these levels of radiation hardness.

CONCLUSION

There has been widespread interest within the military and space community in IDT's CMOS product line for its radiation hardness levels, as well as its high-performance and low power dissipation. To serve this growing need for CMOS circuits that must operate in a radiation environment, IDT has created a separate group within the company to concentrate on supplying products for these applications.Continuing research and development of process and products, including the use of in-house radiation testing capability, will allow Integrated Device Technology to offer continuously increasing levels of radiation-tolerant solutions.

THERMAL PERFORMANCE CALCULATIONS FOR IDT'S PACKAGES

Since most of the electrical energy consumed by microelectronic devices eventually appears as heat, poor thermal performance of the device or lack of management of this thermal energy can cause a variety of deleterious effects. This device temperature increase can exhibit itself as one of the key variables in establishing device performance and long term reliability; on the other hand, effective dissipation of internally generated thermal energy can, if properly managed, reduce the deleterious effects and improve component reliability.

A few key benefits of IDT's enhanced CEMOS™ process are: low power dissipation, high speed, increased levels of integration, wider operating temperature ranges and lower quiescent power dissipation. Because the reliability of an integrated circuit is largely dependent on the maximum temperature the device attains during operation, and as the junction stability declines with increases in junction temperature (T_J), it becomes increasingly important to maintain a low (T_J).

CMOS devices stabilize more quickly and at greatly lower temperature than bipolar devices under normal operation. The accelerated aging of an integrated circuit can be expressed as an exponential function of the junction temperature as:

$$t_A = t_o \exp\left[\frac{E_a}{k}\left(\frac{1}{T_O} - \frac{1}{T_J}\right)\right]$$

where

t_A = lifetime at elevated junction (T_J) temperature
t_O = normal lifetime at normal junction (T_O) temperature
E_a = activation energy (ev)
k = Boltzmann's constant (8.617×10^{-5} ev/k)

i.e. the lifetime of a device could be decreased by a factor of 2 for every 10°C increase temperature.

To minimize the deleterious effects associated with this potential increase, IDT has:

1. Optimized our proprietary low-power CEMOS fabrication process to ensure the active junction temperature rise is minimal.
2. Selected only packaging materials that optimize heat dissipation, which encourages a cooler running device.
3. Physically designed all package components to enhance the inherent material properties and to take full advantage of heat transfer and radiation due to case geometries.
4. Tightly controlled the assembly procedures to meet or exceed the stringent criteria of MIL-STD-883_to ensure maximum heat transfer between die and packaging materials.

The following figures graphically illustrate the thermal values of IDT's current package families. Each envelop (shaded area) depicts a typical spread of values due to the influence of a number of factors which include: circuit size, package cavity size and die attach integrity. The following range of values are to be used as a comprehensive characterization of the major variables rather than single point of reference.

When calculating junction temperature (T_J), it is necessary to know the thermal resistance of the package (θ_{JA}) as measured in "degree celsius per watt". With the accompanying data, the following equation can be used to establish thermal performance, enhance device reliability and ultimately provide you, the user, with a continuing series of high-speed, low-power CMOS solutions to your system design needs.

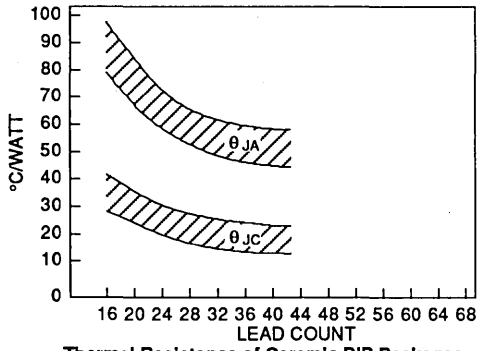
$$\theta_{JA} = [T_J - T_A]/P$$
$$T_J = T_A + P[\theta_{JA}] = T_A + P[\theta_{JC} + \theta_{CA}]$$

where

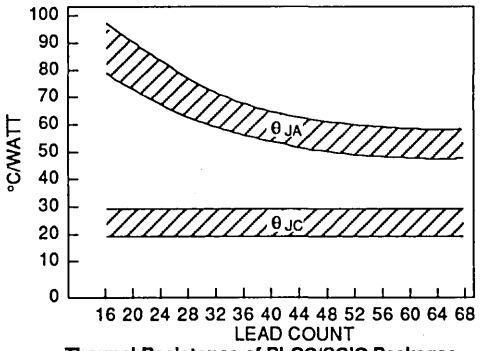
$$\frac{\theta_{JC} = T_J - T_C}{P} \qquad \frac{\theta_{CA} = T_C - T_A}{P}$$

θ = Thermal resistance
J = Junction
P = Operational power of device (dissipated)
T_A = Ambient temperature in degree celsius
T_J = Temperature of the junction
T_C = Temperature of case/package
θ_{CA} = Case to Ambient, thermal resistance—usually a measure of the heat dissipation due to natural or forced convection, radiation and mounting techniques.
θ_{JC} = Junction to Case, thermal resistance—usually measured with reference to the temperature at a specific point on the package (case) surface. (Dependent on the package material properties and package geometry.)
θ_{JA} = Junction to Ambient, thermal resistance—usually measured with respect to the temperature of a specified volume of still air. (Dependent on θ_{JC} + θ_{JA} which includes the influence of area and environmental condition.)

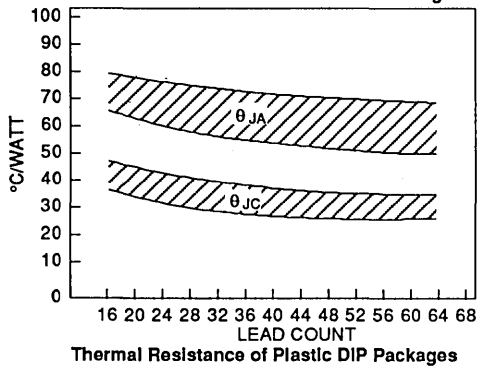
Ref. MIL-STD-883C, Method 1012.1
JEDEC ENG. Bulletin No. 20, January 1975
1986 Semi. Std., Vol. 4, Test Methods G30–86, G32–86.



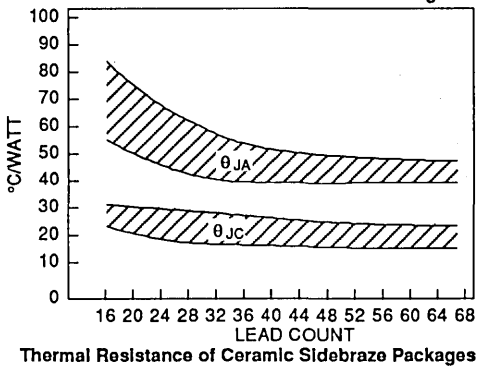
Thermal Resistance of Ceramic DIP Packages



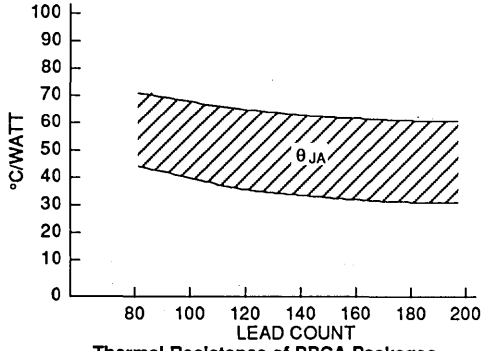
Thermal Resistance of PLCC/SOIC Packages



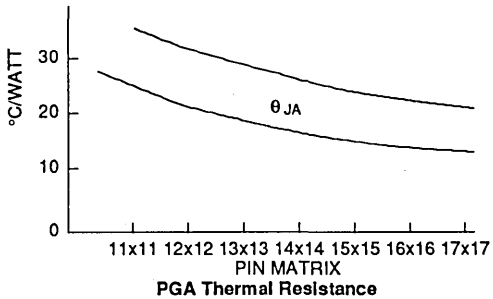
Thermal Resistance of Plastic DIP Packages



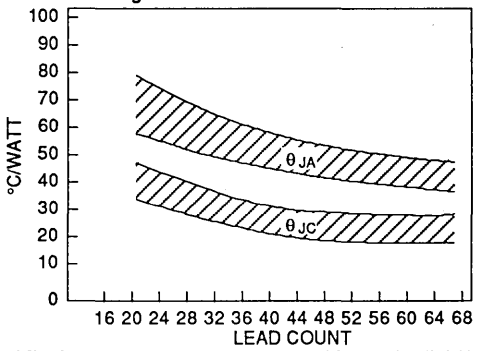
Thermal Resistance of Ceramic Sidebraze Packages



Thermal Resistance of PPGA Packages



PGA Thermal Resistance



Thermal Resistance of Ceramic Leadless Chip Carrier (LCC) Packages

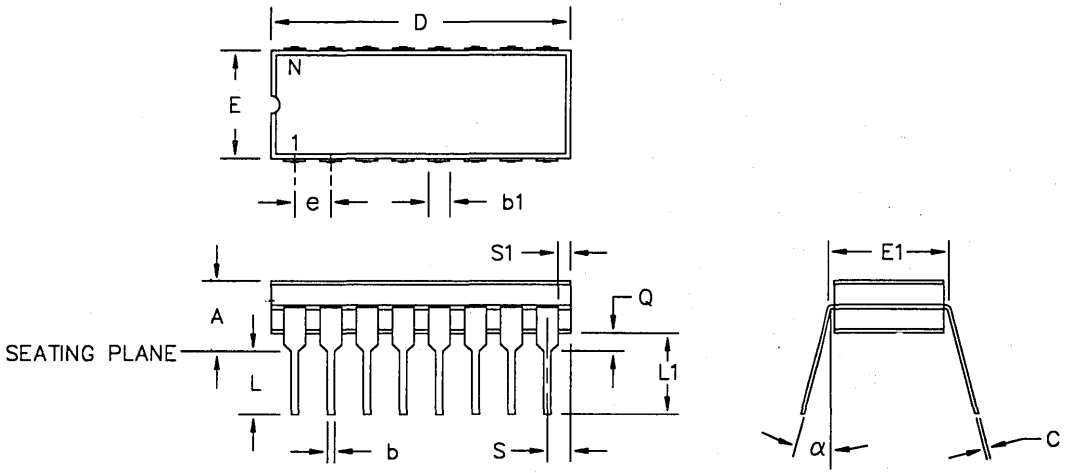
2512 drw 01

PACKAGE DIAGRAM OUTLINE INDEX

Integrated Device Technology, Inc.

PACKAGE DIAGRAM OUTLINES

DUAL IN-LINE PACKAGES



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. THE MINIMUM LIMIT FOR DIMENSION b1 MAY BE .023 FOR CORNER LEADS.

16–28 LEAD CERDIP (300 MIL)

DWG #	D16–1		D18–1		D20–1		D22–1		D24–1		D28–3	
# OF LDS (N)	16		18		20		22		24		28	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.200	.140	.200	.140	.200	.105	.175	.105	.175	.105	.175
b	.015	.021	.015	.021	.015	.021	.015	.021	.015	.021	.015	.021
b1	.038	.060	.038	.060	.038	.060	.038	.060	.045	.065	.045	.065
C	.009	.012	.009	.012	.009	.012	.009	.012	.009	.014	.009	.014
D	.750	.830	.880	.930	.935	1.060	1.050	1.080	1.240	1.280	1.440	1.490
E	.285	.310	.285	.310	.285	.310	.285	.310	.285	.310	.285	.310
E1	.290	.320	.290	.320	.290	.320	.290	.320	.300	.320	.300	.320
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC	
L	.125	.175	.125	.175	.125	.175	.125	.175	.125	.175	.125	.175
L1	.150	–	.150	–	.150	–	.150	–	.150	–	.150	–
Q	.015	.055	.015	.055	.015	.060	.015	.060	.015	.060	.015	.060
S	.020	.080	.020	.080	.020	.080	.020	.080	.030	.080	.030	.080
S1	.005	–	.005	–	.005	–	.005	–	.005	–	.005	–
α	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°

DUAL IN–LINE PACKAGES (Continued)

24–40 LEAD CERDIP (600 MIL)

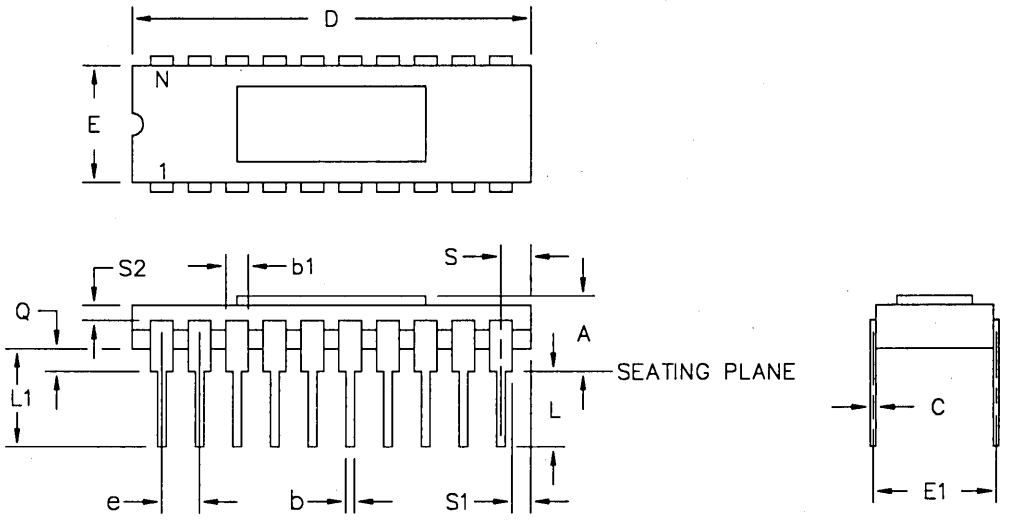
DWG #	D24–2		D28–1		D40–1	
# OF LDS (N)	24		28		40	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.190	.090	.200	.160	.220
b	.014	.023	.014	.023	.014	.023
b1	.038	.060	.038	.065	.038	.065
C	.008	.012	.008	.014	.008	.014
D	1.230	1.290	1.440	1.490	2.020	2.070
E	.500	.610	.510	.545	.510	.545
E1	.590	.620	.590	.620	.590	.620
e	.100 BSC		.100 BSC		.100 BSC	
L	.125	.200	.125	.200	.125	.200
L1	.150	–	.150	–	.150	–
Q	.015	.060	.020	.060	.020	.060
S	.030	.080	.030	.080	.030	.080
S1	.005	–	.005	–	.005	–
α	0°	15°	0°	15°	0°	15°

28–40 LEAD CERDIP (WIDE BODY)

DWG #	D28–2		D32–1		D40–2	
# OF LDS (N)	28		32		40	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.120	.210	.160	.220
b	.014	.023	.014	.023	.014	.023
b1	.038	.065	.038	.065	.038	.065
C	.008	.014	.008	.014	.008	.014
D	1.440	1.490	1.625	1.675	2.020	2.070
E	.570	.600	.570	.600	.570	.600
E1	.590	.620	.590	.620	.590	.620
e	.100 BSC		.100 BSC		.100 BSC	
L	.125	.200	.125	.200	.125	.200
L1	.150	–	.150	–	.150	–
Q	.020	.060	.020	.060	.020	.060
S	.030	.080	.030	.080	.030	.080
S1	.005	–	.005	–	.005	–
α	0°	15°	0°	15°	0°	15°

DUAL IN-LINE PACKAGES (Continued)

20-32 LEAD SIDE BRAZE (300 MIL)

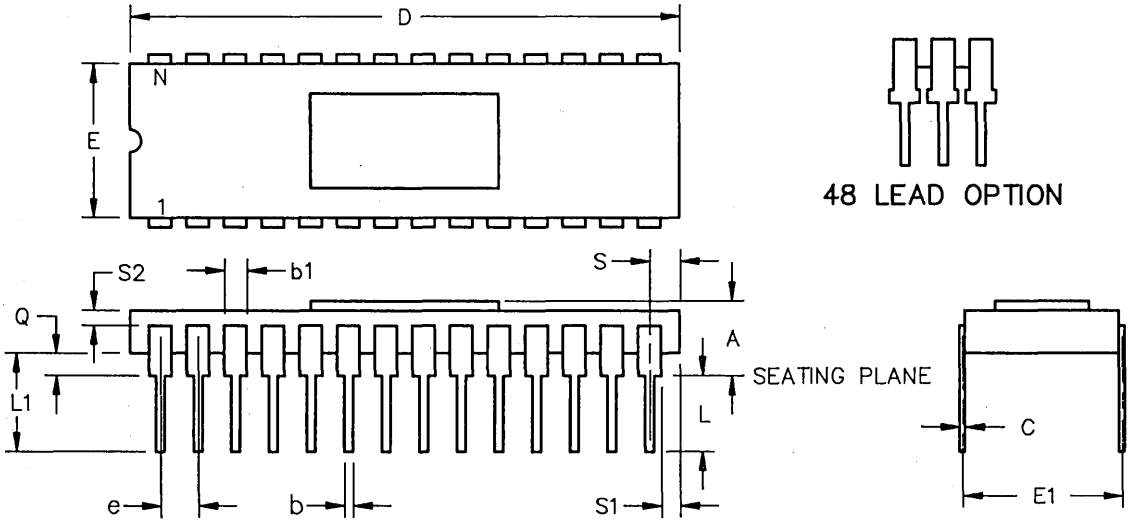


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C20-1		C22-1		C24-1		C28-1		C32-3	
# OF LDS (N)	20		22		24		28		32	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.100	.200	.090	.200	.090	.200	.090	.200
b	.014	.023	.014	.023	.015	.023	.014	.023	.014	.023
b1	.040	.060	.038	.060	.040	.060	.040	.060	.040	.060
C	.008	.015	.008	.015	.008	.015	.008	.015	.008	.014
D	.970	1.060	1.040	1.120	1.180	1.230	1.380	1.420	1.580	1.640
E	.220	.310	.260	.310	.220	.310	.220	.310	.280	.310
E1	.290	.320	.290	.320	.290	.320	.290	.320	.290	.320
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC	
L	.125	.200	.125	.200	.125	.200	.125	.200	.100	.175
L1	.150	–	.150	–	.150	–	.150	–	.150	–
Q	.015	.060	.015	.060	.015	.060	.015	.060	.030	.060
S	.030	.065	.030	.065	.030	.065	.030	.065	.030	.065
S1	.005	–	.005	–	.005	–	.005	–	.005	–
S2	.005	–	.005	–	.005	–	.005	–	.005	–

DUAL IN-LINE PACKAGES (Continued)

28-48 LEAD SIDE BRAZE (400 MIL)

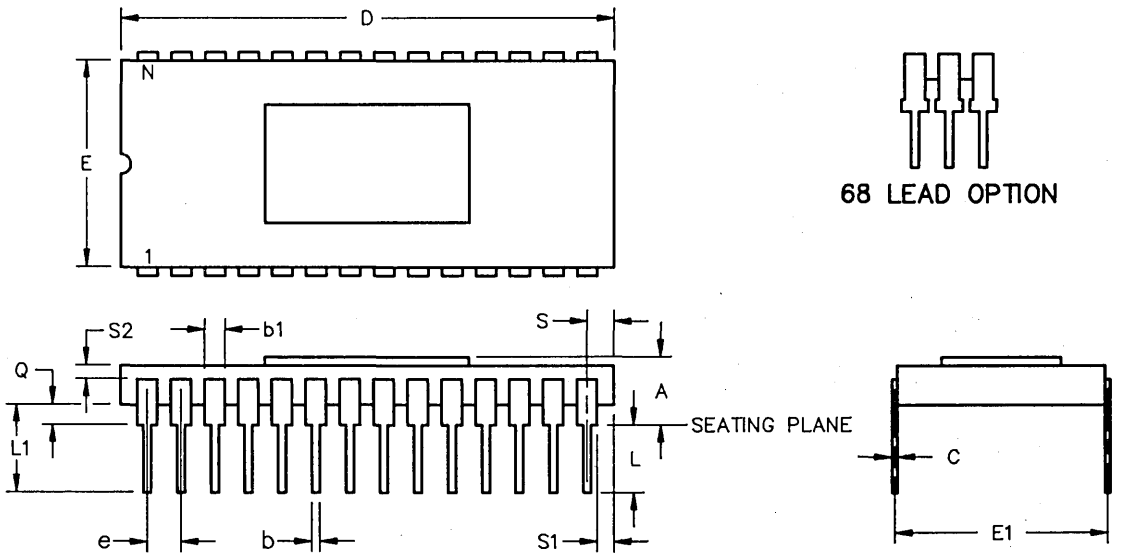


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C28-2		C32-2		C48-1	
# OF LDS (N)	28		32		48	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.090	.200	.085	.190
b	.014	.023	.014	.023	.014	.023
b1	.040	.060	.040	.060	.040	.060
C	.008	.014	.008	.014	.008	.014
D	1.380	1.420	1.580	1.640	1.690	1.730
E	.380	.420	.380	.410	.380	.410
E1	.390	.420	.390	.420	.390	.420
e	.100 BSC		.100 BSC		.070 BSC	
L	.100	.175	.100	.175	.125	.175
L1	.150	–	.150	–	.150	–
Q	.030	.060	.030	.060	.020	.070
S	.030	.065	.030	.065	.030	.065
S1	.005	–	.005	–	.005	–
S2	.005	–	.005	–	.005	–

DUAL IN-LINE PACKAGES (Continued)

24-68 LEAD SIDE BRAZE (600 MIL)

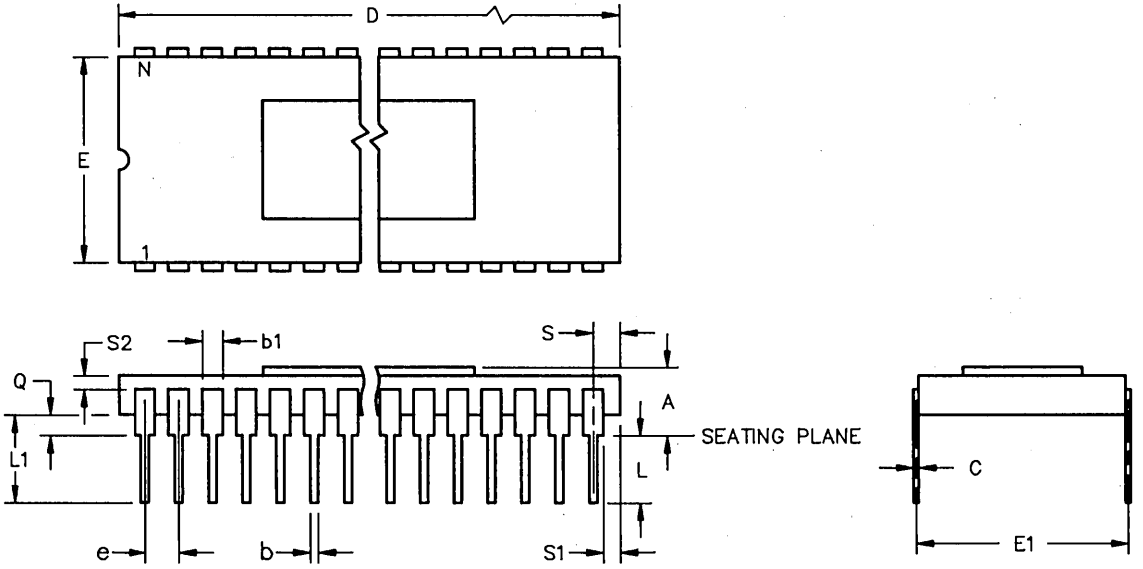


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C24-2		C28-3		C32-1		C40-1		C48-2		C68-1	
# OF LDS (N)	24		28		32		40		48		68	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.190	.085	.190	.100	.190	.085	.190	.100	.190	.085	.190
b	.015	.023	.015	.022	.015	.023	.015	.023	.015	.023	.015	.023
b1	.040	.060	.038	.060	.040	.060	.038	.060	.040	.060	.040	.060
C	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012
D	1.180	1.220	1.380	1.430	1.580	1.640	1.980	2.030	2.370	2.430	2.380	2.440
E	.575	.610	.580	.610	.580	.610	.580	.610	.550	.610	.580	.610
E1	.595	.620	.595	.620	.590	.620	.595	.620	.590	.620	.590	.620
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC		.070 BSC	
L	.125	.175	.125	.175	.125	.175	.125	.175	.125	.175	.125	.175
L1	.150	–	.150	–	.150	–	.150	–	.150	–	.150	–
Q	.020	.060	.020	.065	.020	.060	.020	.060	.020	.060	.020	.070
S	.030	.065	.030	.065	.030	.065	.030	.065	.030	.065	.030	.065
S1	.005	–	.005	–	.005	–	.005	–	.005	–	.005	–
S2	.010	–	.010	–	.005	–	.010	–	.005	–	.005	–

DUAL IN-LINE PACKAGES (Continued)

64 LEAD SIDE BRAZE (900 MIL)

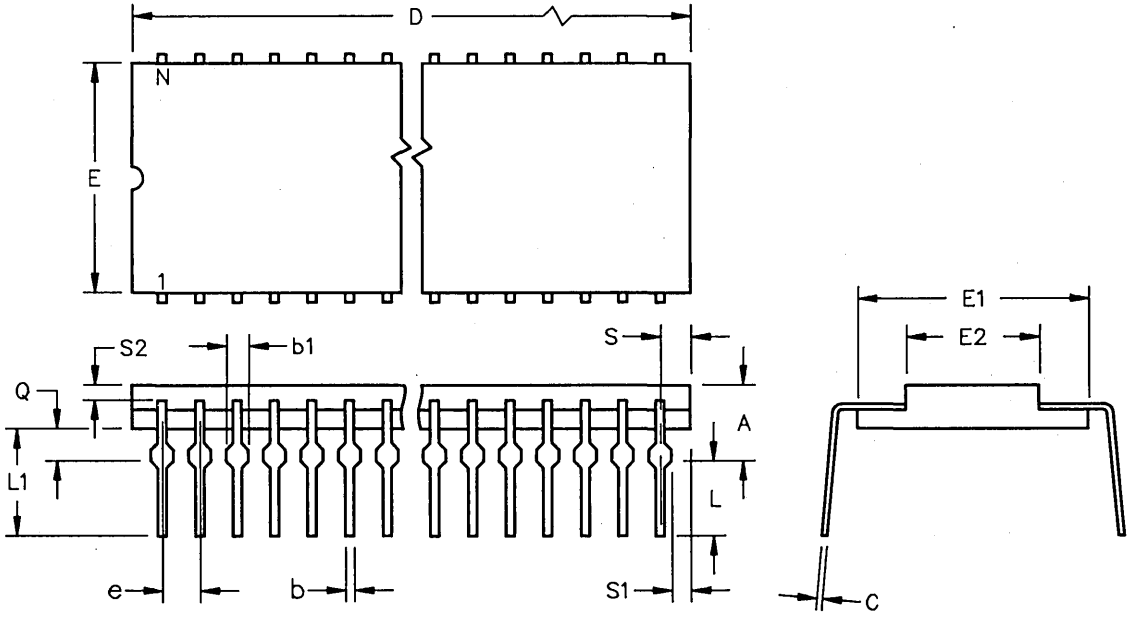


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C64-1	
# OF LDS (N)	64	
SYMBOL	MIN	MAX
A	.110	.190
b	.014	.023
b1	.040	.060
C	.008	.015
D	3.160	3.240
E	.884	.915
E1	.890	.920
e	.100 BSC	
L	.125	.200
L1	.150	–
Q	.015	.070
S	.030	.065
S1	.005	–
S2	.005	–

DUAL IN-LINE PACKAGES (Continued)

64 LEAD TOP BRAZE (900 MIL)

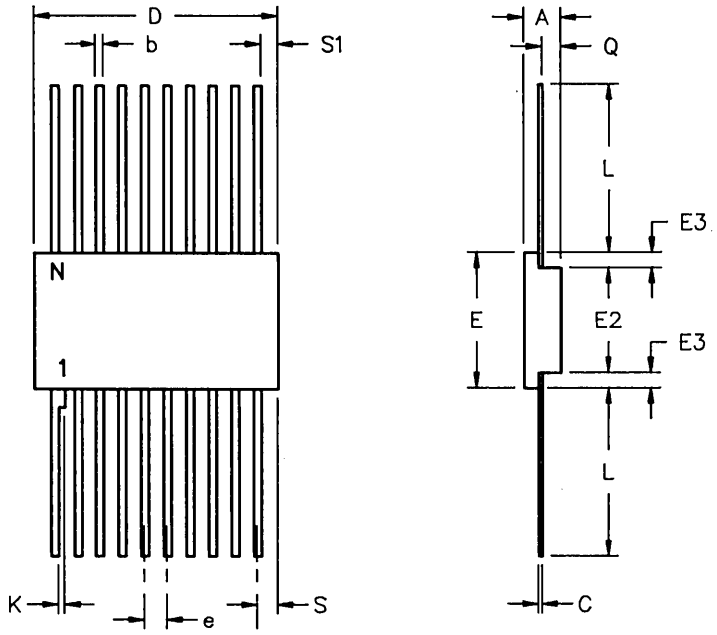


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C64-2	
# OF LDS (N)	64	
SYMBOL	MIN	MAX
A	.120	.180
b	.015	.021
b1	.040	.060
C	.009	.012
D	3.170	3.240
E	.790	.810
E1	.880	.815
E2	.640	.660
e	.100 BSC	
L	.125	.160
L1	.150	–
Q	.020	.100
S	.030	.065
S1	.005	–
S2	.005	–

FLATPACKS

20–28 LEAD FLATPACK

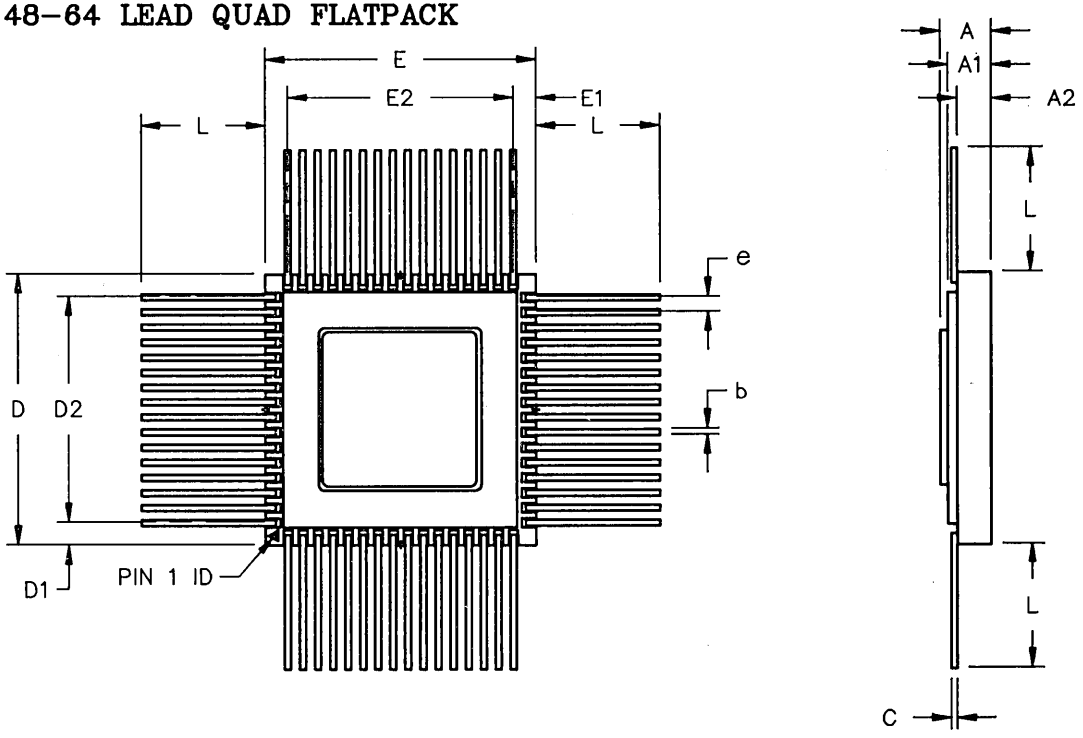


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	F20–1		F20–2		F24–1		F28–1		F28–2	
# OF LDS (N)	20		20 (.295 BODY)		24		28		28	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.045	.092	.045	.092	.045	.090	.045	.090	.045	.115
b	.015	.019	.015	.019	.015	.019	.015	.019	.015	.019
C	.003	.006	.003	.006	.003	.006	.004	.007	.003	.007
D	–	.540	–	.540	–	.640	.710	.740	.710	.740
E	.340	.360	.245	.303	.360	.420	.480	.520	.460	.520
E2	.130	–	.130	–	.180	–	.180	–	.180	–
E3	.030	–	.030	–	.030	–	.040	–	.040	–
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
K	.008	.015	.008	.015	.008	.015	.008	.015	.008	.015
L	.250	.370	.250	.370	.250	.370	.250	.370	.250	.370
Q	.010	.040	.010	.040	.010	.040	.010	.045	.010	.045
S	–	.045	–	.045	–	.045	–	.045	–	.045
S1	.005	–	.005	–	.005	–	.005	–	.005	–

FLATPACKS (Continued)

48–64 LEAD QUAD FLATPACK

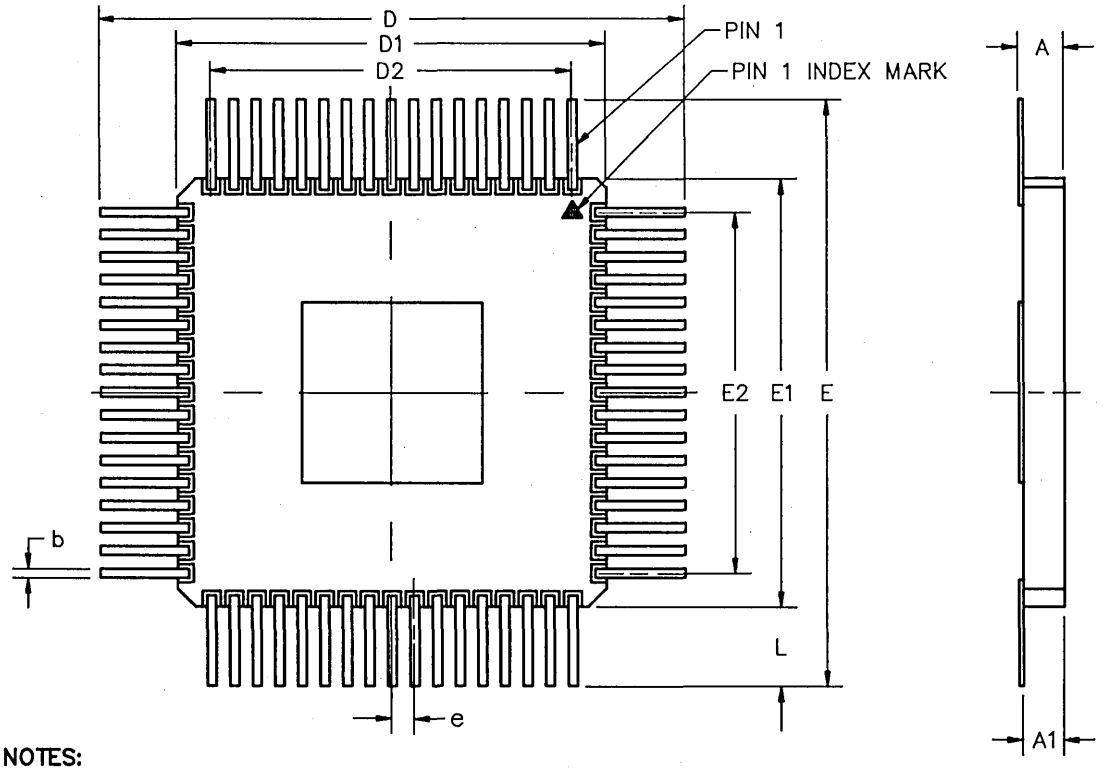


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	F48–1		F64–1	
# OF LDS (N)	48		64	
SYMBOL	MIN	MAX	MIN	MAX
A	.089	.108	.070	.090
A1	.079	.096	.060	.078
A2	.058	.073	.030	.045
b	.018	.022	.016	.020
C	.008	.010	.009	.012
D/E	–	.750	.885	.915
D1/E1	.100 REF		.075 REF	
D2/E2	.550 BSC		.750 BSC	
e	.050 BSC		.050 BSC	
L	.350	.450	.350	.450
ND/NE	12		16	

FLATPACKS (Continued)

68 LEAD QUAD FLATPACK

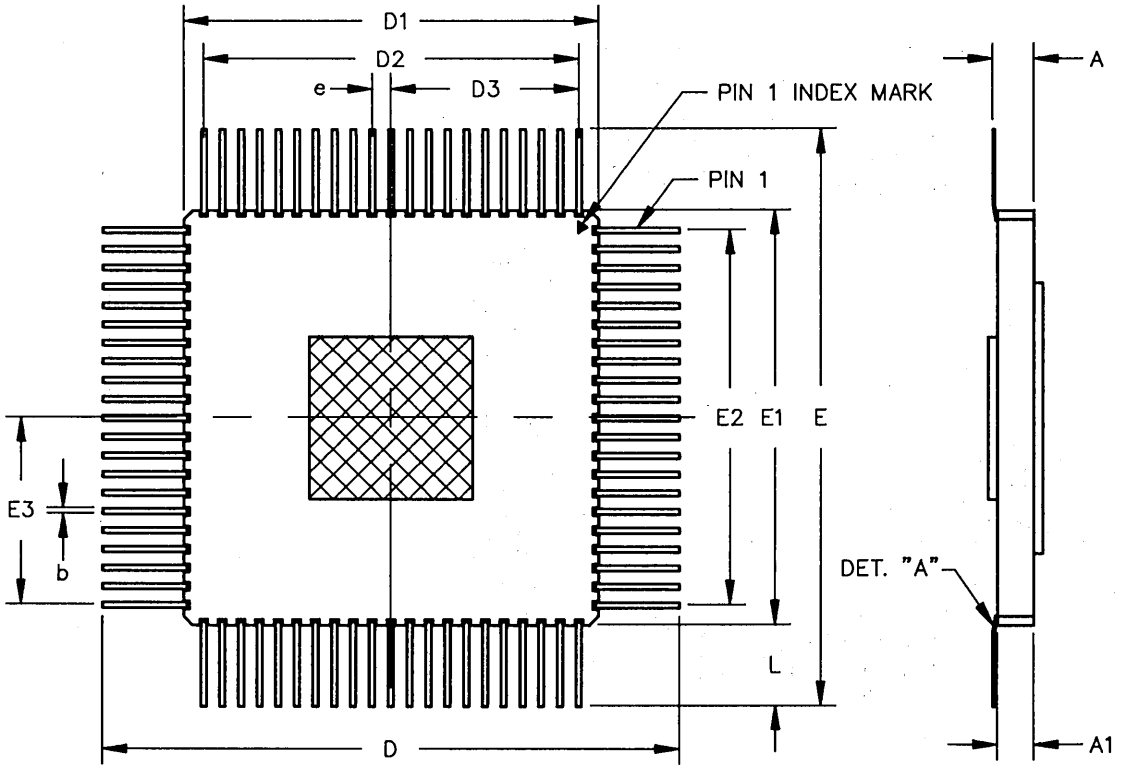


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	F68–1	
# OF LDS (N)	68	
SYMBOL	MIN	MAX
A	.080	.145
A1	.070	.090
b	.014	.021
C	.008	.012
D/E	1.640	1.870
D1/E1	.926	.970
D2/E2	.800 BSC	
e	.050 BSC	
L	.350	.450
ND/NE	17	

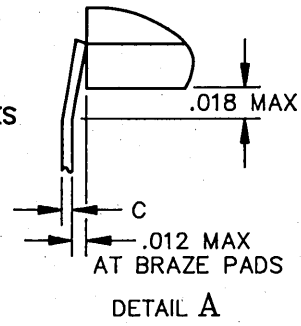
FLATPACKS (Continued)

84 LEAD QUAD FLATPACK (CAVITY DOWN)



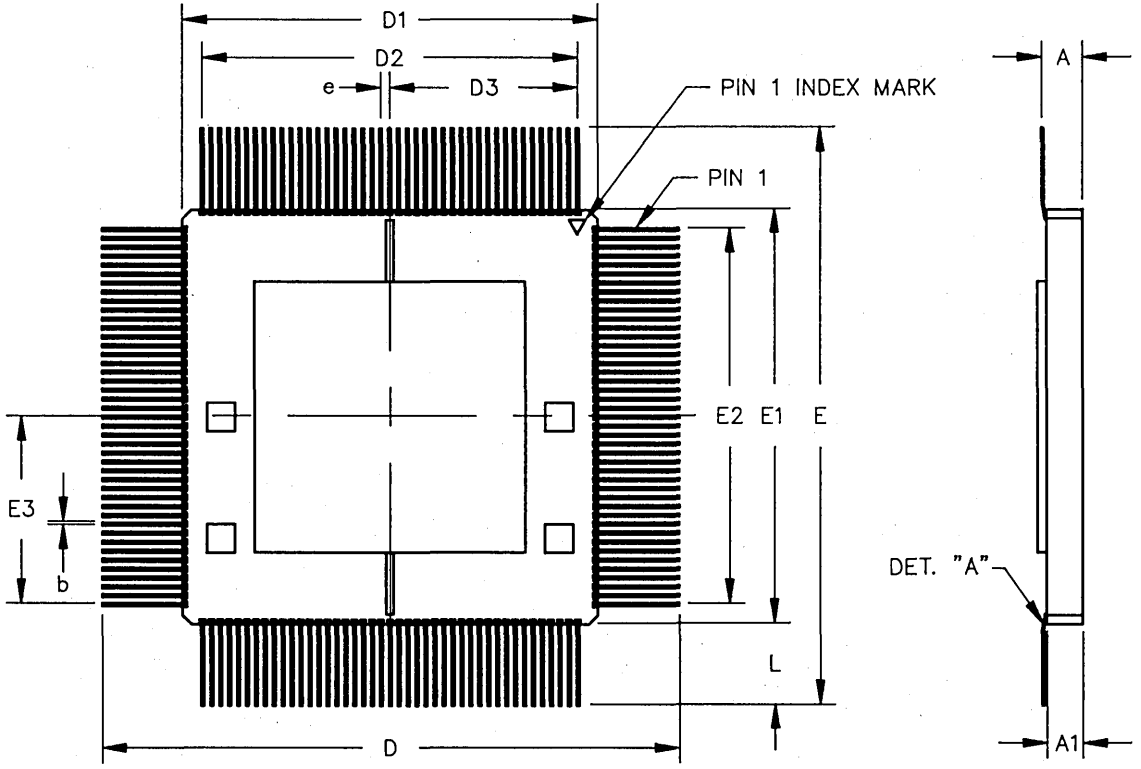
DWG #	F84-1	
# OF LDS (N)	84	
SYMBOL	MIN	MAX
A	–	.140
A1	–	.105
b	.014	.020
C	.007	.013
D/E	1.485	1.615
D1/E1	1.130	1.170
D2/E2	1.000 BSC	
D3/E3	.500 BSC	
e	.050 BSC	
L	.350	.450
ND/NE	21	

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. CROSS HATCHED AREA INDICATES INTEGRAL METALLIC HEAT SINK.



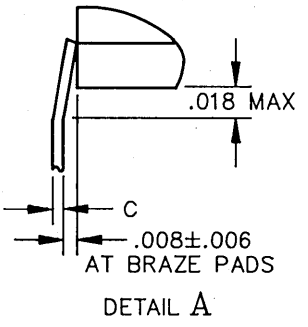
FLATPACKS (Continued)

172 LEAD QUAD FLATPACK (MIPS)



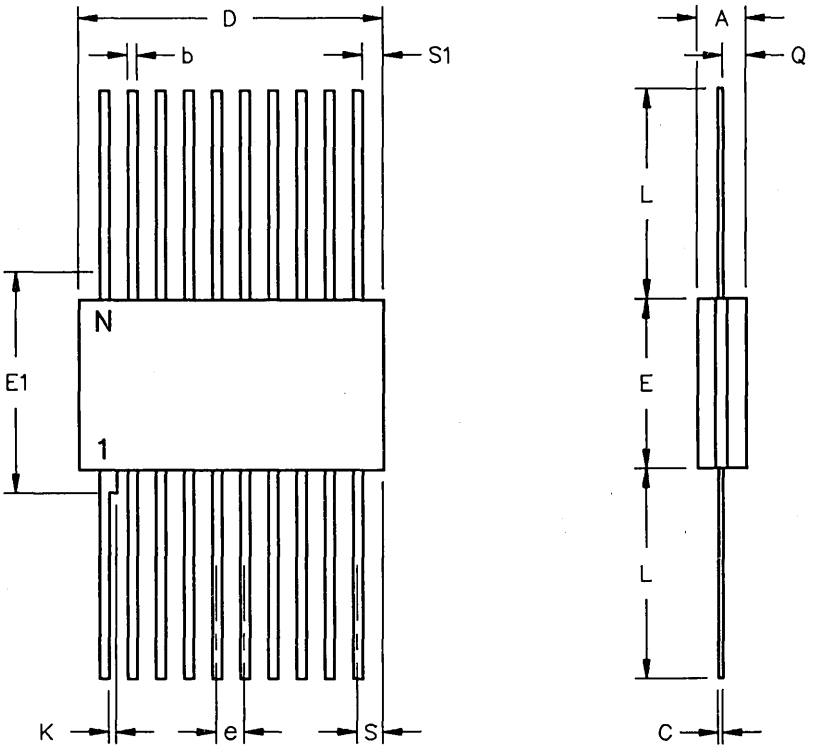
DWG #	F172-1	
# OF LDS (N)	172	
SYMBOL	MIN	MAX
A	–	.130
A1	–	.105
b	.006	.010
C	.004	.008
D/E	1.580	1.620
D1/E1	1.135	1.165
D2/E2	1.050 BSC	
D3/E3	.525 BSC	
e	.025 BSC	
L	.220	.230
ND/NE	43	

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.



CERPACKS

16–28 LEAD CERPACK

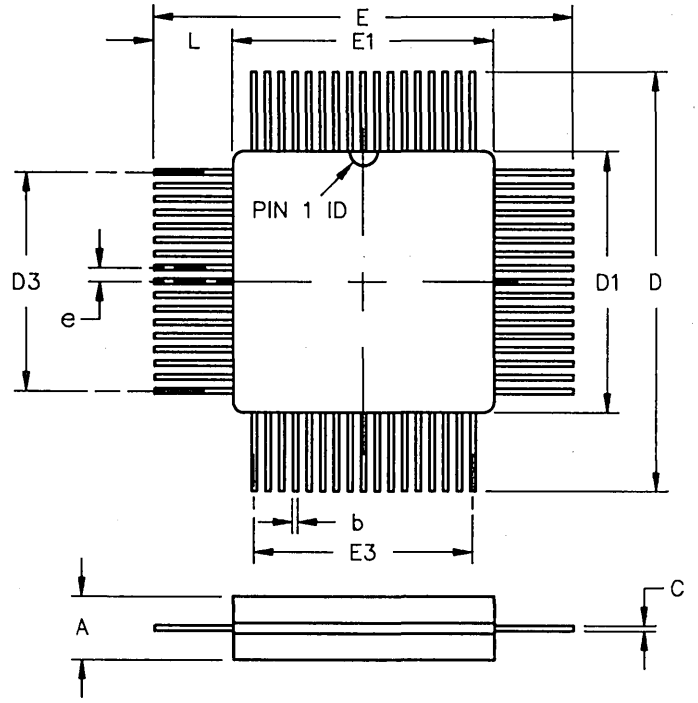


NOTES:
1. ALL DIMENSION ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	E16–1		E20–1		E24–1		E28–1		E28–2	
# OF LDS (N)	16		20		24		28		28	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.055	.085	.045	.092	.045	.090	.045	.115	.045	.090
b	.015	.019	.015	.019	.015	.019	.015	.019	.015	.019
C	.0045	.006	.0045	.006	.0045	.006	.0045	.009	.0045	.006
D	.370	.430	–	.540	–	.640	–	.740	–	.740
E	.245	.285	.245	.300	.300	.420	.460	.520	.340	.380
E1	–	.305	–	.305	–	.440	–	.550	–	.400
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
K	.008	.015	.008	.015	.008	.015	.008	.015	.008	.015
L	.250	.370	.250	.370	.250	.370	.250	.370	.250	.370
Q	.026	.040	.026	.040	.026	.040	.026	.045	.026	.045
S	–	.045	–	.045	–	.045	–	.045	–	.045
S1	.005	–	.005	–	.005	–	.005	–	.005	–

CERQUADS

68 LEAD CERQUAD (STRAIGHT LEADS)

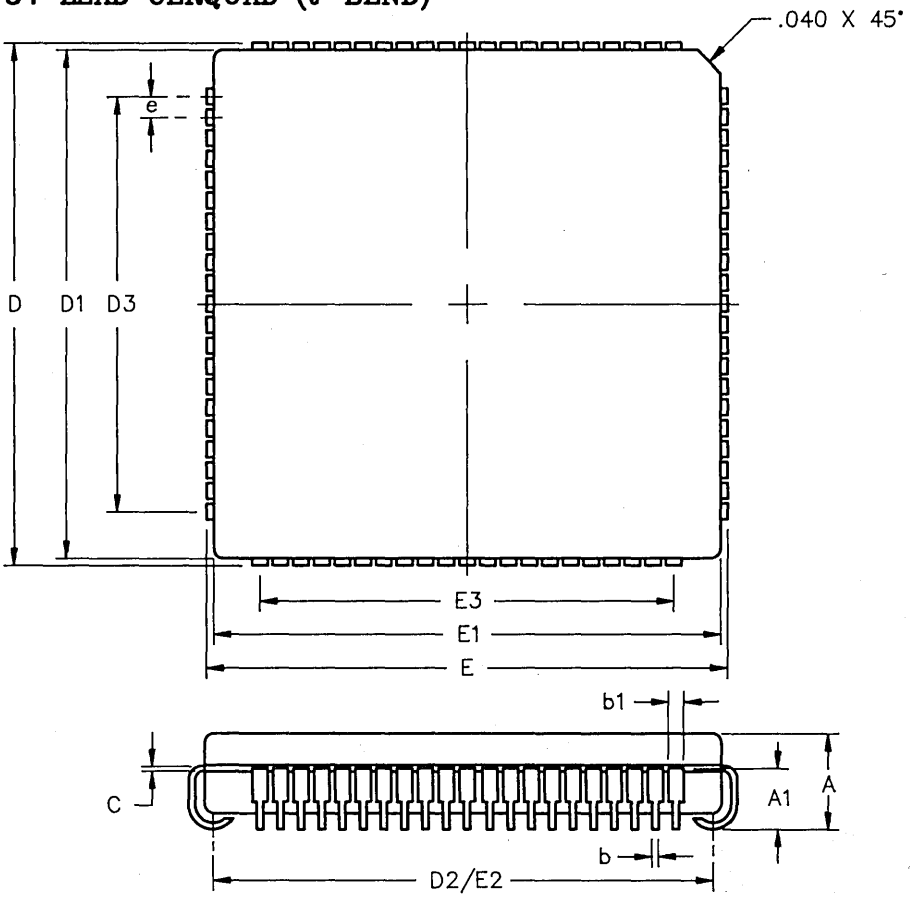


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	CQ68-1	
# OF LDS (N)	68	
SYMBOL	MIN	MAX
A	.115	.165
b	.008	.013
C	.0045	.008
D/E	.860	1.100
D1/E1	.460	.500
D3/E3	.400 REF	
e	.025 BSC	
L	.200	.300
ND/NE	17	

CERQUADS (Continued)

84 LEAD CERQUAD (J–BEND)

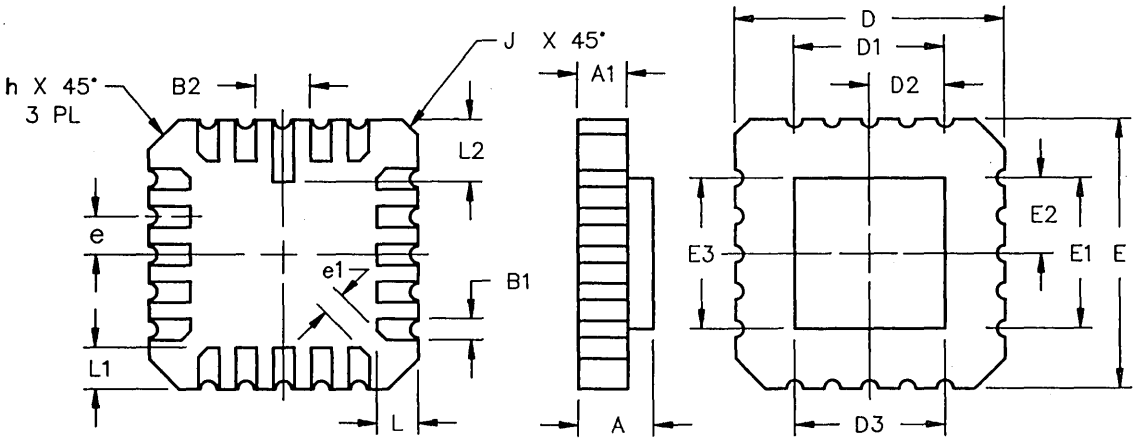


DWG #	CQ84–1	
# OF LDS (N)	84	
SYMBOL	MIN	MAX
A	.155	.200
A1	.090	.120
b1	.022	.032
b	.013	.023
C	.006	.013
D/E	1.170	1.190
D1/E1	1.138	1.162
D2/E2	1.100	.1.150
D3/.E3	1.000 BSC	
e	.050 BSC	
ND/NE	21	

NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

LEADLESS CHIP CARRIERS



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

20–48 LEAD LCC (SQUARE)

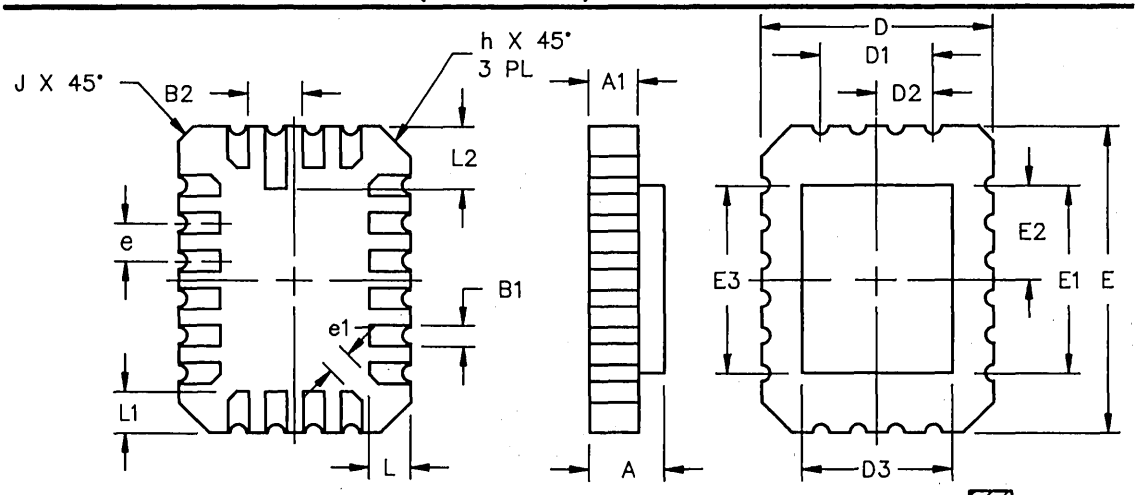
DWG #	L20–2		L28–1		L44–1		L48–1	
# OF LDS (N)	20		28		44		48	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.064	.100	.064	.100	.064	.120	.055	.120
A1	.054	.066	.050	.088	.054	.088	.045	.090
B1	.022	.028	.022	.028	.022	.028	.017	.023
B2	.072 REF		.072 REF		.072 REF		.072 REF	
B3	.006	.022	.006	.022	.006	.022	.006	.022
D/E	.342	.358	.442	.460	.640	.660	.554	.572
D1/E1	.200 BSC		.300 BSC		.500 BSC		.440 BSC	
D2/E2	.100 BSC		.150 BSC		.250 BSC		.220 BSC	
D3/E3	–	.358	–	.460	–	.560	.500	.535
e	.050 BSC		.050 BSC		.050 BSC		.040 BSC	
e1	.015	–	.015	–	.015	–	.015	–
h	.040 REF		.040 REF		.040 REF		.012 RADIUS	
J	.020 REF		.020 REF		.020 REF		.020 REF	
L	.045	.055	.045	.055	.045	.055	.033	.047
L1	.045	.055	.045	.055	.045	.055	.033	.047
L2	.077	.093	.077	.093	.077	.093	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015
ND/NE	5		7		11		12	

LEADLESS CHIP CARRIERS (Continued)

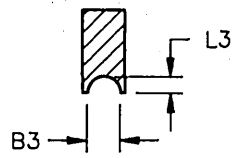
52–68 LEAD LCC (SQUARE)

DWG #	L52–1		L52–2		L68–2		L68–1	
# OF LDS (N)	52		52		68		68	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.061	.087	.082	.120	.082	.120	.065	.120
A1	.051	.077	.072	.088	.072	.088	.055	.075
B1	.022	.028	.022	.028	.022	.028	.008	.014
B2	.072 REF		.072 REF		.072 REF		.072 REF	
B3	.006	.022	.006	.022	.006	.022	.006	.022
D/E	.739	.761	.739	.761	.938	.962	.554	.566
D1/E1	.600 BSC		.600 BSC		.800 BSC		.400 BSC	
D2/E2	.300 BSC		.300 BSC		.400 BSC		.200 BSC	
D3/E3	–	.661	–	.661	–	.862	–	.535
e	.050 BSC		.050 BSC		.050 BSC		.025 BSC	
e1	.015	–	.015	–	.015	–	.015	–
h	.040 REF		.040 REF		.040 REF		.040 REF	
J	.020 REF		.020 REF		.020 REF		.020 REF	
L	.045	.055	.045	.055	.045	.055	.045	.055
L1	.045	.055	.045	.055	.045	.055	.045	.055
L2	.077	.093	.075	.093	.077	.093	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015
ND/NE	13		13		17		17	

LEADLESS CHIP CARRIERS (Continued)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

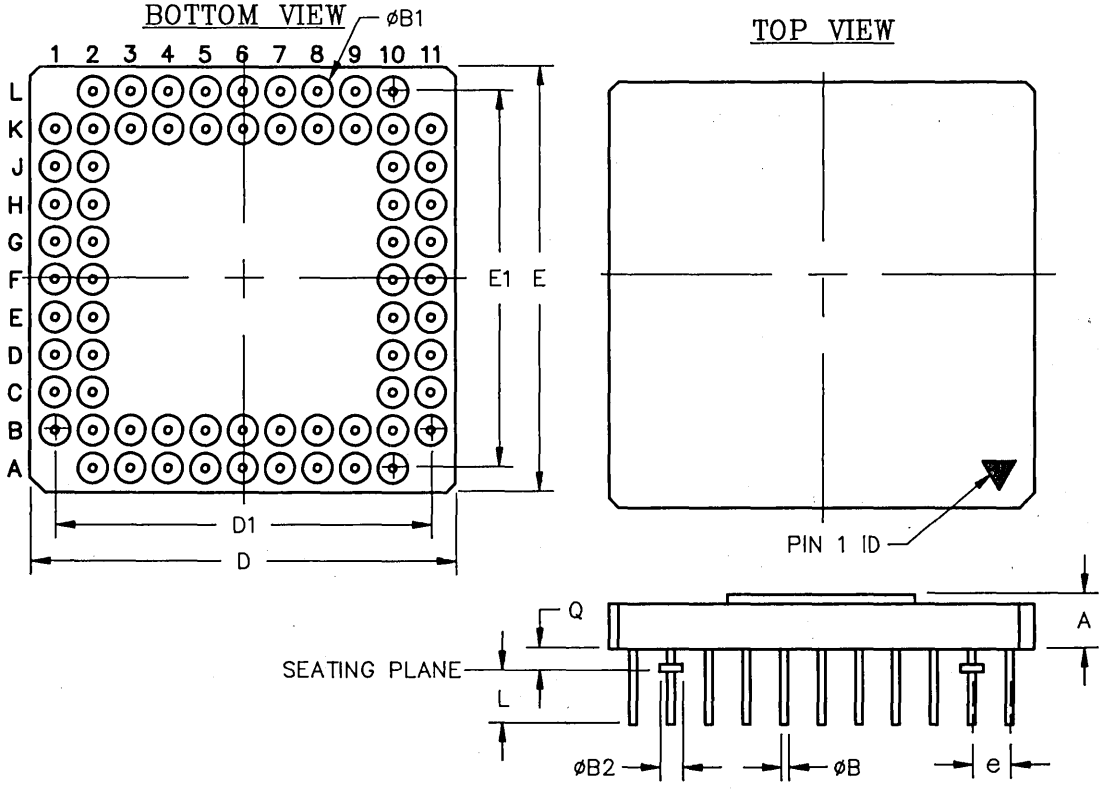


20–32 LEAD LCC (RECTANGULAR)

DWG #	L20–1		L22–1		L24–1		L28–2		L32–1	
# OF LDS (N)	20		22		24		28		32	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.060	.075	.064	.100	.064	.120	.060	.120	.060	.120
A1	.050	.065	.054	.063	.054	.066	.050	.088	.050	.088
B1	.022	.028	.022	.028	.022	.028	.022	.028	.022	.028
B2	.072 REF		.072 REF		.072 REF		.072 REF		.072 REF	
B3	.006	.022	.006	.022	.006	.022	.006	.022	.006	.022
D	.284	.296	.284	.296	.292	.308	.342	.358	.442	.458
D1	.150 BSC		.150 BSC		.200 BSC		.200 BSC		.300 BSC	
D2	.075 BSC		.075 BSC		.100 BSC		.100 BSC		.150 BSC	
D3	–	.280	–	.280	–	.308	–	.358	–	.458
E	.420	.435	.480	.496	.392	.408	.540	.560	.540	.560
E1	.250 BSC		.300 BSC		.300 BSC		.400 BSC		.400 BSC	
E2	.125 BSC		.150 BSC		.150 BSC		.200 BSC		.200 BSC	
E3	–	.410	–	.480	–	.408	–	.558	–	.558
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
e1	.015	–	.015	–	.015	–	.015	–	.015	–
h	.040 REF		.012 RADIUS		.025 REF		.040 REF		.040 REF	
J	.020 REF		.012 RADIUS		.015 REF		.020 REF		.020 REF	
L	.045	.055	.039	.051	.040	.050	.045	.055	.045	.055
L1	.045	.055	.039	.051	.040	.050	.045	.055	.045	.055
L2	.080	.095	.083	.097	.077	.093	.077	.093	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015	.003	.015
ND	4		4		5		5		7	
NE	6		7		7		9		9	

PIN GRID ARRAYS

68 PIN PGA (CAVITY UP)

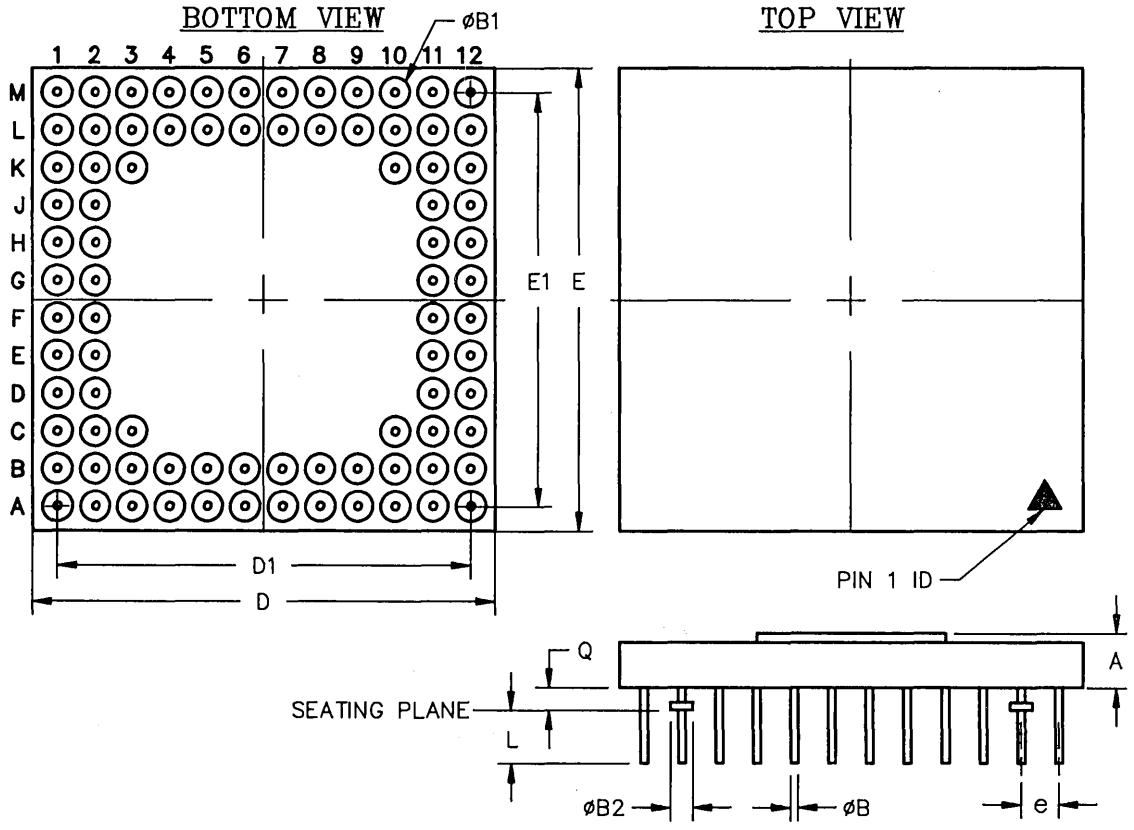


DWG #	G68-1	
# OF PINS (N)	68	
SYMBOL	MIN	MAX
A	.070	.145
øB	.016	.020
øB1	–	.080
øB2	.040	.060
D/E	1.140	1.180
D1/E1	1.000 BSC	
e	.100 BSC	
L	.120	.140
M	11	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

84 PIN PGA (CAVITY UP – 12 X 12 GRID)

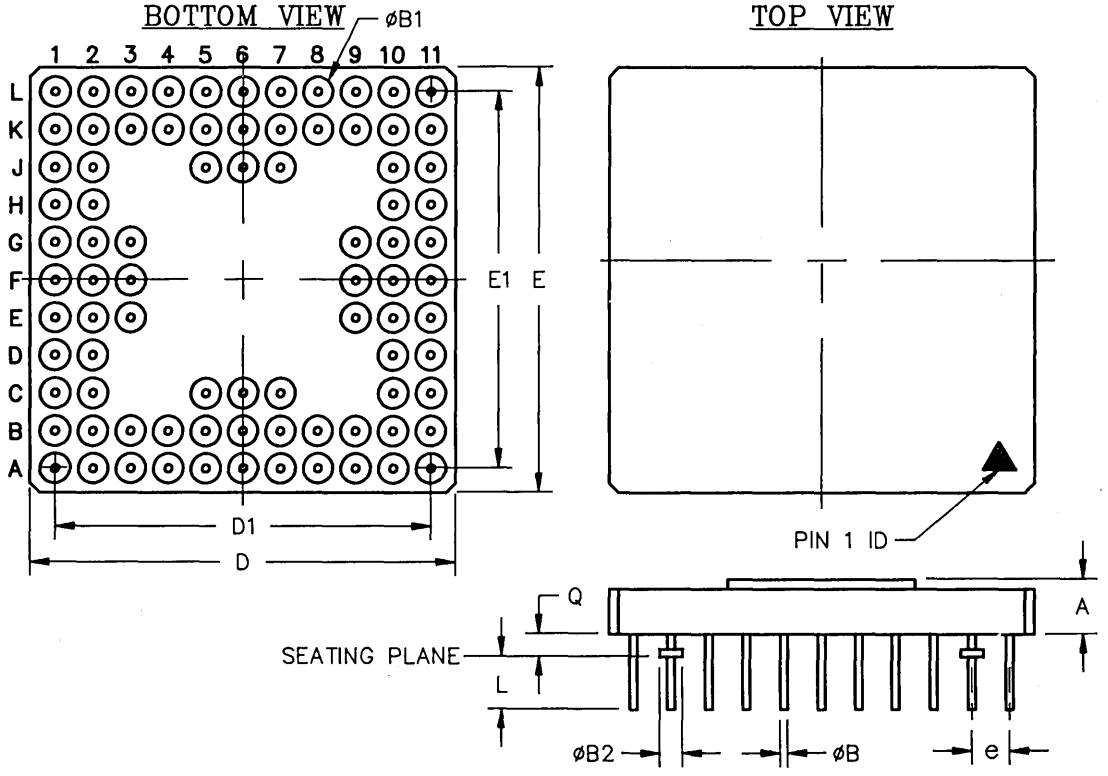


DWG #	G84–1	
# OF PINS (N)	84	
SYMBOL	MIN	MAX
A	.077	.145
ØB	.016	.020
ØB1	.040	.080
ØB2	.040	.060
D/E	1.180	1.235
D1/E1	1.100 BSC	
e	.100 BSC	
L	.120	.140
M	12	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

84 PIN PGA (CAVITY UP – 11 X 11 GRID)

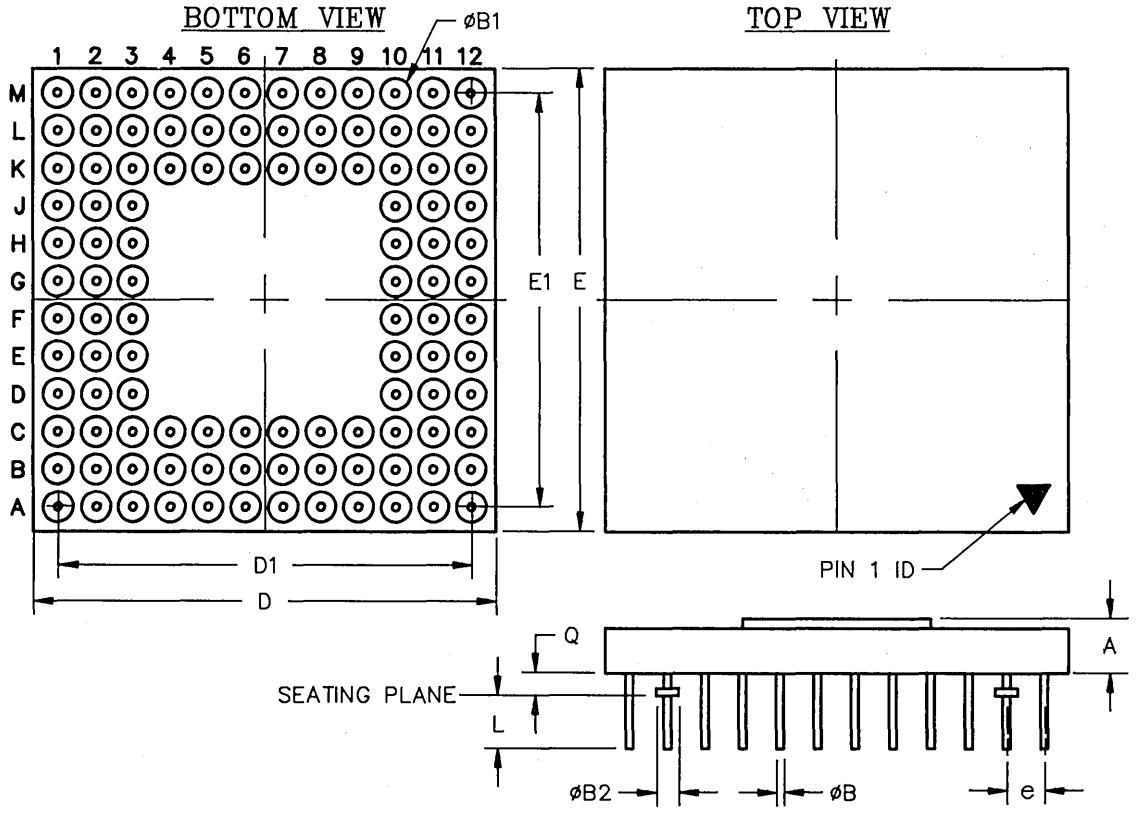


DWG #	G84-3	
# OF PINS (N)	84	
SYMBOL	MIN	MAX
A	.070	.145
ØB	.016	.020
ØB1	–	.080
ØB2	.040	.060
D/E	1.080	1.120
D1/E1	1.000 BSC	
e	.100 BSC	
L	.120	.140
M	11	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

108 PIN PGA (CAVITY UP)

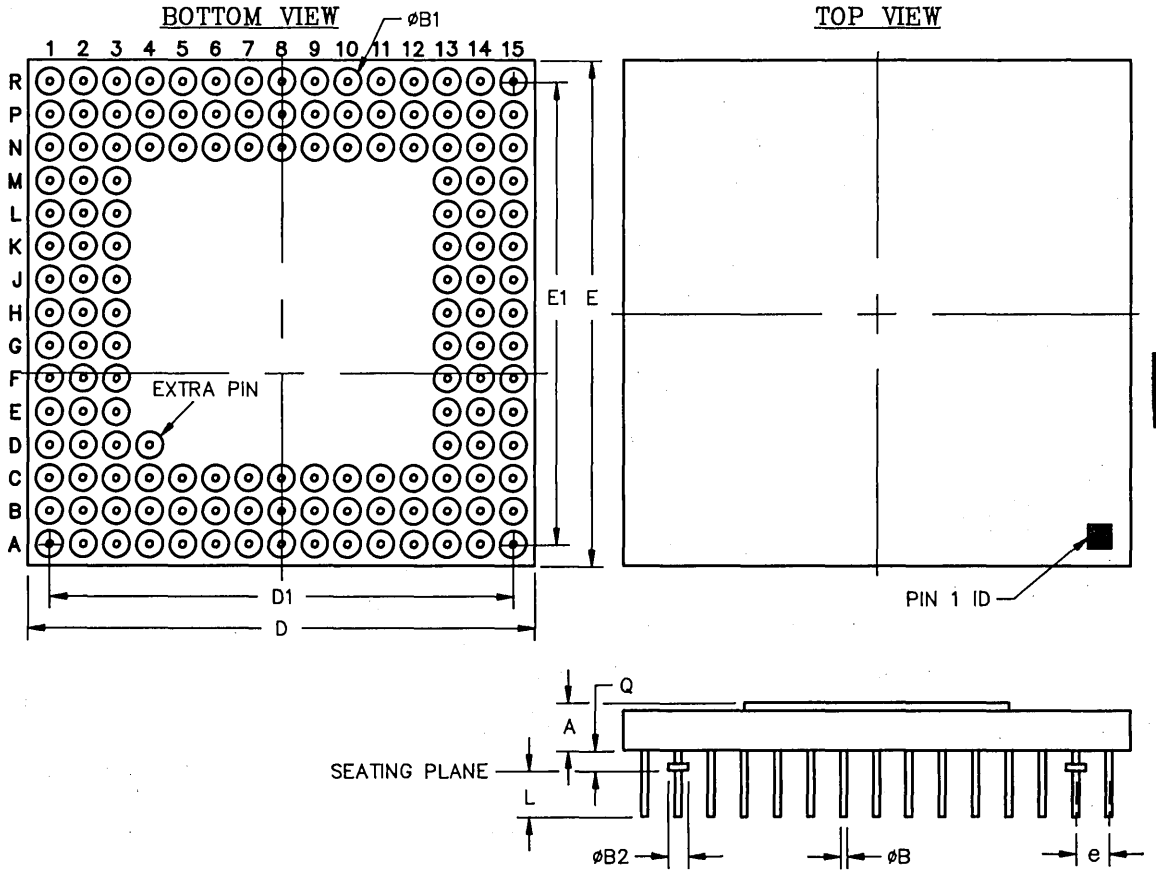


DWG #	G108-1	
# OF PINS (N)	108	
SYMBOL	MIN	MAX
A	.070	.145
ØB	.016	.020
ØB1	–	.080
ØB2	.040	.060
D/E	1.188	1.212
D1/E1	1.100 BSC	
e	.100 BSC	
L	.120	.140
M	12	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

144 PIN PGA (CAVITY UP)

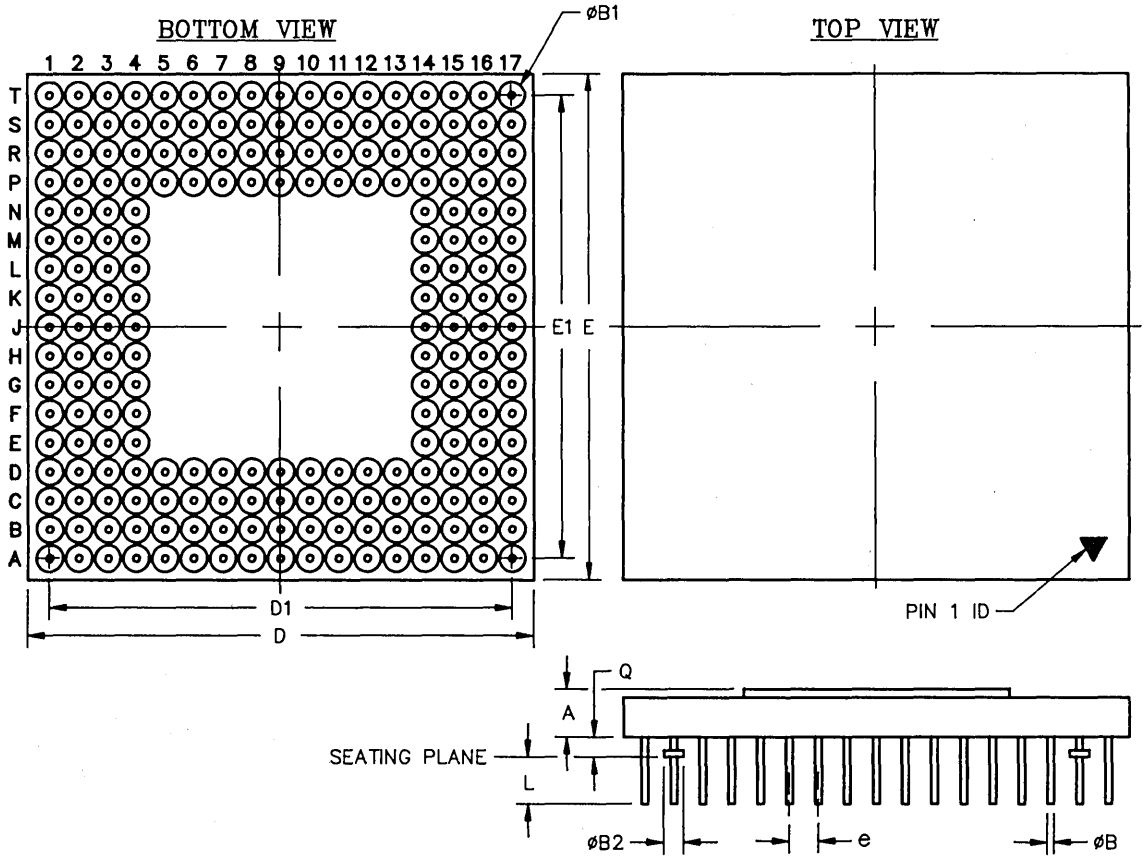


DWG #	G144-2	
# OF PINS (N)	145	
SYMBOL	MIN	MAX
A	.082	.125
ØB	.016	.020
ØB1	.060	.080
ØB2	.040	.060
D/E	1.559	1.590
D1/E1	1.400 BSC	
e	.100 BSC	
L	.120	.140
M	15	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.
6. EXTRA PIN (D-4) ELECTRICALLY CONNECTED TO D-3.

PIN GRID ARRAYS (Continued)

208 PIN PGA (CAVITY UP)

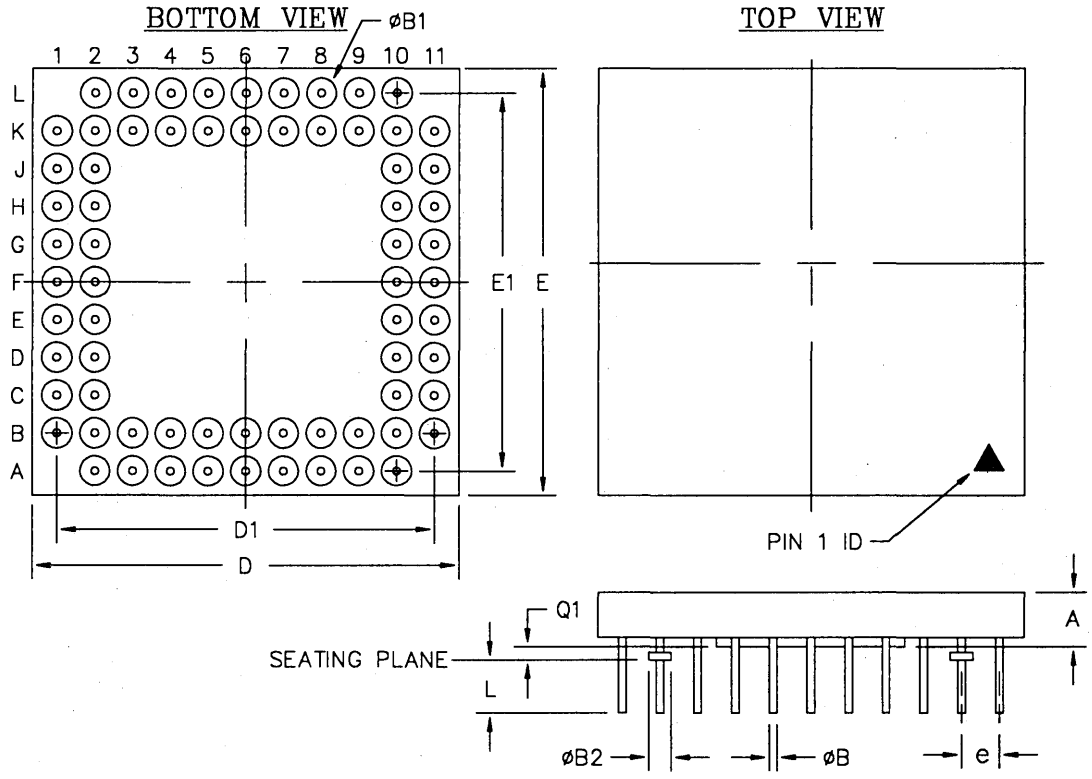


DWG #	G208-1	
# OF PINS (N)	208	
SYMBOL	MIN	MAX
A	.070	.145
øB	.016	.020
øB1	–	.080
øB2	.040	.060
D/E	1.732	1.780
D1/E1	1.600 BSC	
e	.100 BSC	
L	.125	.140
M	17	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

68 PIN PGA (CAVITY DOWN)

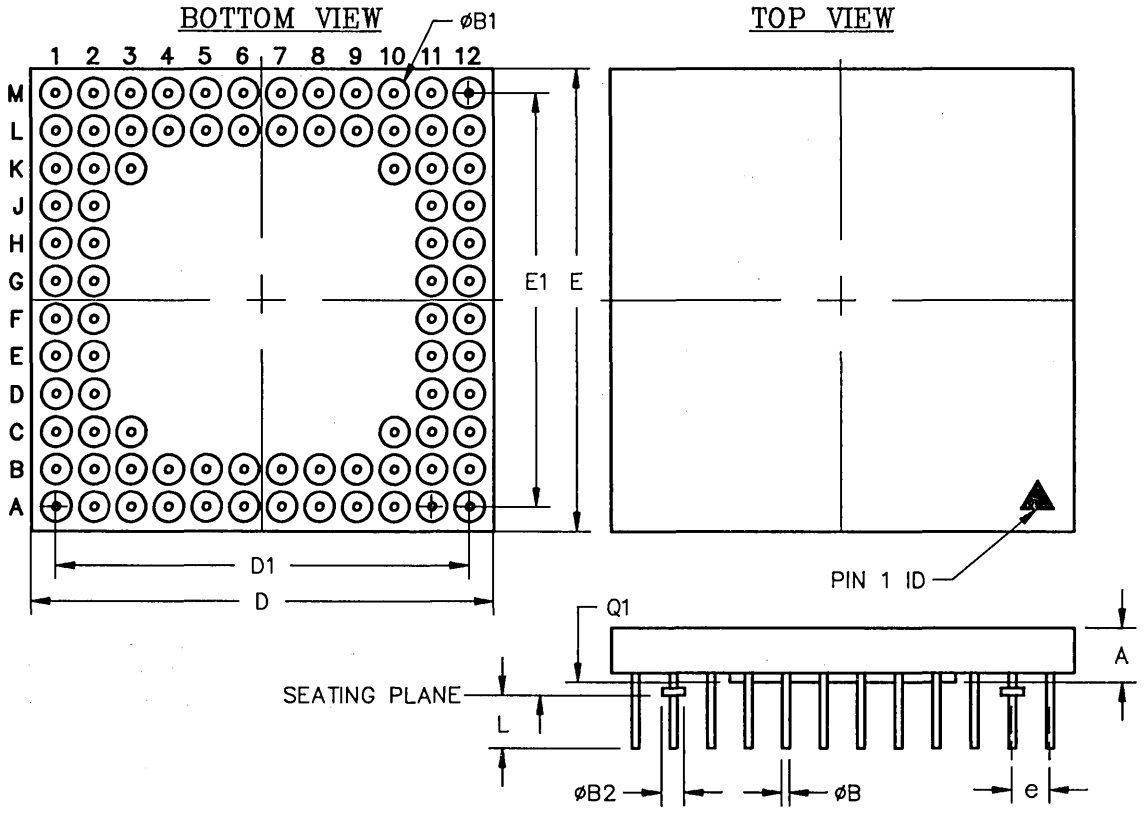


DWG #	G68-2	
# OF PINS (N)	68	
SYMBOL	MIN	MAX
A	.077	.095
øB	.016	.020
øB1	.060	.080
øB2	.040	.060
D/E	1.098	1.122
D1/E1	1.000 BSC	
e	.100 BSC	
L	.120	.140
M	11	
Q1	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

84 PIN PGA (CAVITY DOWN)

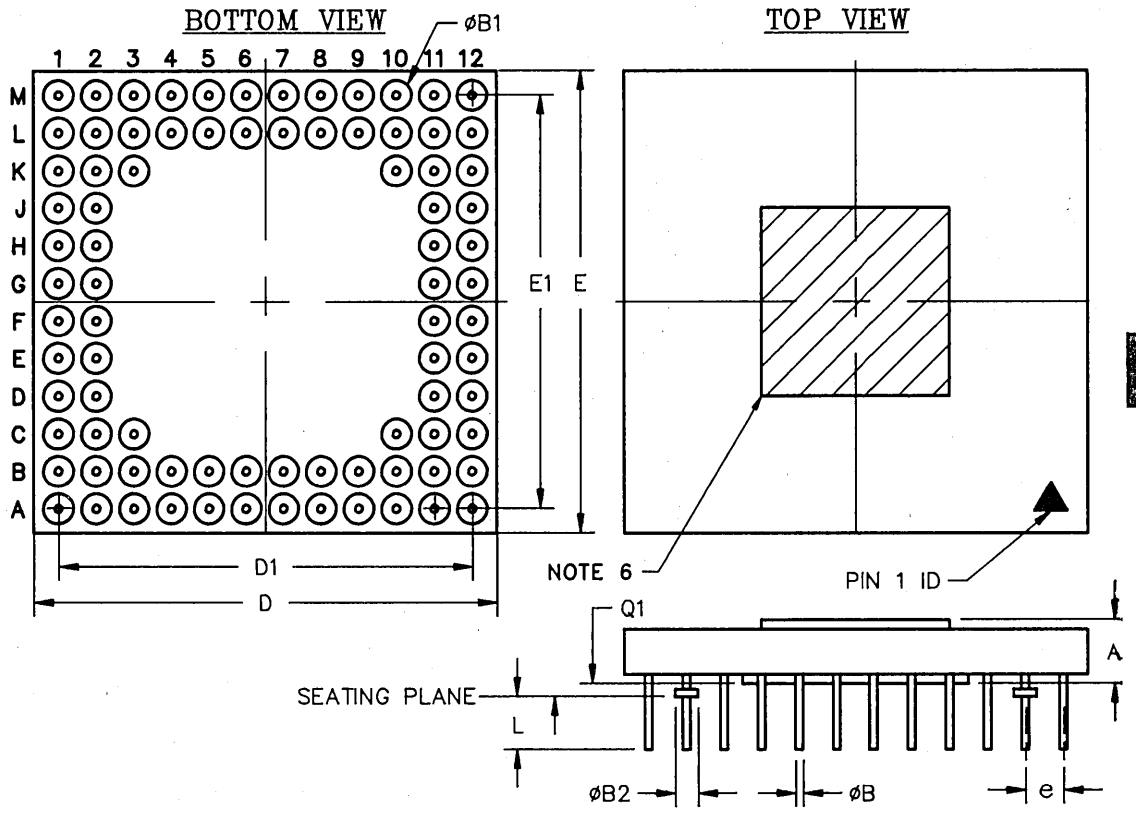


DWG #	G84-2	
# OF PINS (N)	84	
SYMBOL	MIN	MAX
A	.077	.145
ØB	.016	.020
ØB1	.060	.080
ØB2	.040	.060
D/E	1.180	1.235
D1/E1	1.100 BSC	
e	.100 BSC	
L	.100	.120
M	12	
Q1	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

84 PIN PGA (CAVITY DOWN – MIPS)

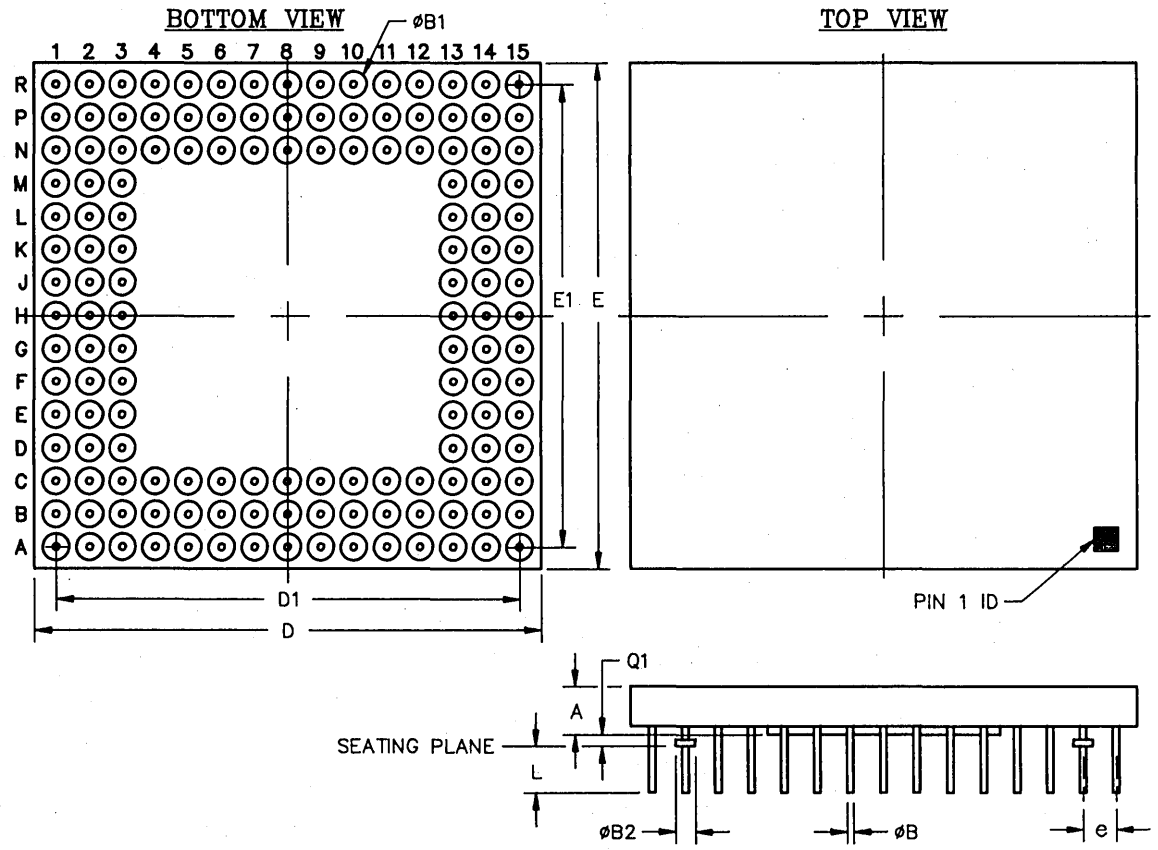


DWG #	G84-4	
# OF PINS (N)	84	
SYMBOL	MIN	MAX
A	.077	.145
øB	.016	.020
øB1	.060	.080
øB2	.040	.060
D/E	1.180	1.235
D1/E1	1.100 BSC	
e	.100 BSC	
L	.120	.140
M	12	
Q1	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.
6. CROSS HATCHED AREA INDICATES INTEGRALL METALLIC HEAT SINK.

PIN GRID ARRAYS (Continued)

144 PIN PGA (CAVITY DOWN)

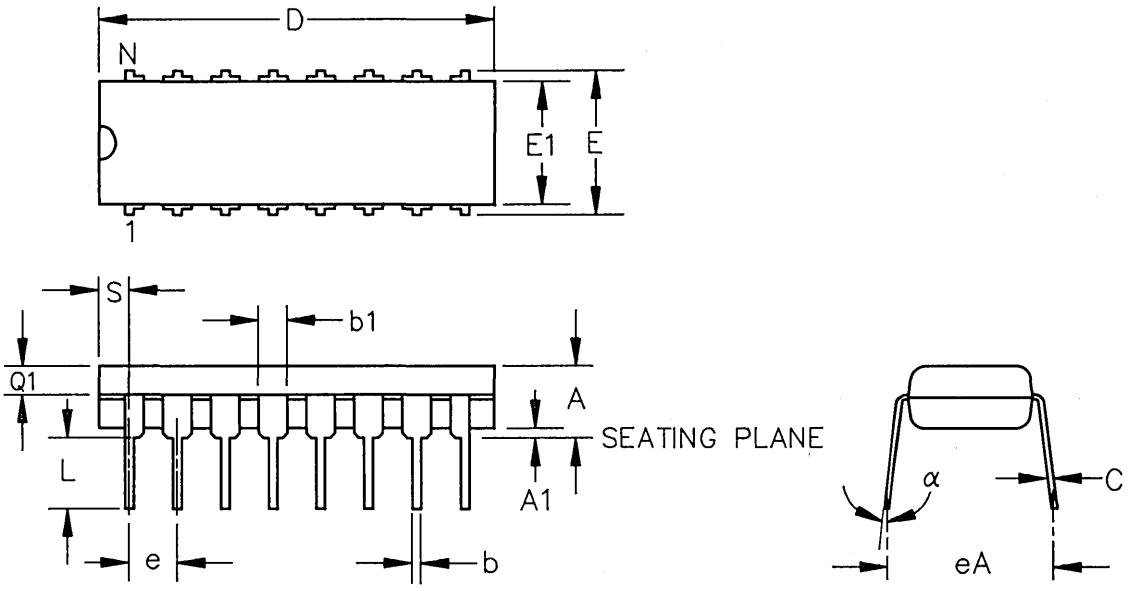


DWG #	G144-1	
# OF PINS (N)	144	
SYMBOL	MIN	MAX
A	.082	.100
ØB	.016	.020
ØB1	.060	.080
ØB2	.040	.060
D/E	1.559	1.590
D1/E1	1.400 BSC	
e	.100 BSC	
L	.120	.140
M	15	
Q1	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PLASTIC DUAL IN-LINE PACKAGES

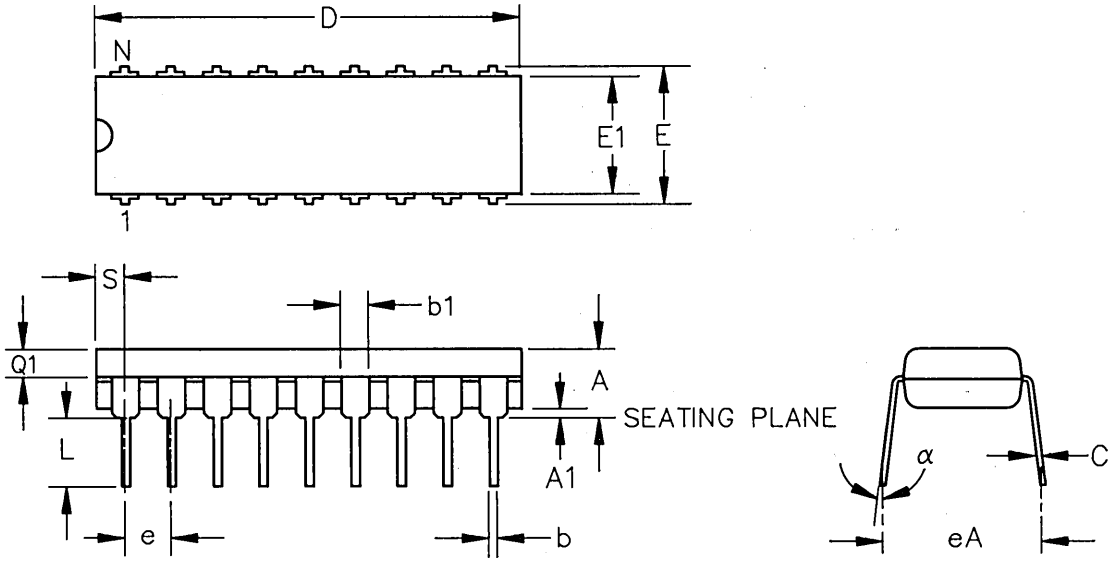
16-32 LEAD PLASTIC DIP (300 MIL)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DWG #	P16-1		P22-1		P28-2		P32-2	
# OF LDS (N)	16		22		28		32	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.165	.145	.165	.145	.180	.145	.180
A1	.015	.035	.015	.035	.015	.030	.015	.030
b	.015	.022	.015	.022	.015	.022	.016	.022
b1	.050	.070	.050	.065	.045	.065	.045	.060
C	.008	.012	.008	.012	.008	.015	.008	.015
D	.745	.760	1.050	1.060	1.345	1.375	1.545	1.585
E	.300	.325	.300	.320	.300	.325	.300	.325
E1	.247	.260	.240	.270	.270	.295	.275	.295
e	.090	.110	.090	.110	.090	.110	.090	.110
eA	.310	.370	.310	.370	.310	.400	.310	.400
L	.120	.150	.120	.150	.120	.150	.120	.150
α	0°	15°	0°	15°	0°	15°	0°	15°
S	.015	.035	.020	.040	.020	.042	.020	.060
Q1	.050	.070	.055	.075	.055	.065	.055	.065

PLASTIC DUAL IN-LINE PACKAGES (Continued)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

18-24 LEAD PLASTIC DIP (300 MIL - FULL LEAD)

DWG #	P18-1		P20-1		P24-1	
# OF LDS (N)	18		20		24	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.165	.145	.165	.145	.165
A1	.015	.035	.015	.035	.015	.035
b	.015	.020	.015	.020	.015	.020
b1	.050	.070	.050	.070	.050	.065
C	.008	.012	.008	.012	.008	.012
D	.885	.910	1.022	1.040	1.240	1.255
E	.300	.325	.300	.325	.300	.320
E1	.247	.260	.240	.280	.250	.275
e	.090	.110	.090	.110	.090	.110
eA	.310	.370	.310	.370	.310	.370
L	.120	.150	.120	.150	.120	.150
α	0°	15°	0°	15°	0°	15°
S	.040	.060	.025	.070	.055	.075
Q1	.050	.070	.055	.075	.055	.070

PLASTIC DUAL IN-LINE PACKAGES (Continued)

24-48 LEAD PLASTIC DIP (600 MIL)

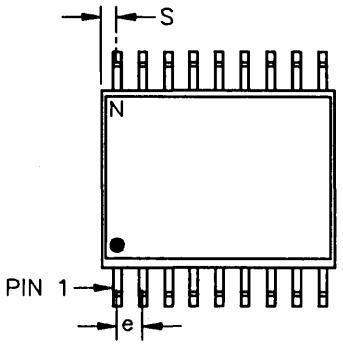
DWG #	P24-2		P28-1		P32-1		P40-1		P48-1	
# OF LEADS (N)	24		28		32		40		48	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.160	.185	.160	.185	.170	.190	.160	.185	.170	.200
A1	.015	.035	.015	.035	.015	.050	.015	.035	.015	.035
b	.015	.020	.015	.020	.016	.020	.015	.020	.015	.020
b1	.050	.065	.050	.065	.045	.055	.050	.065	.050	.065
C	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012
D	1.240	1.260	1.420	1.460	1.645	1.655	2.050	2.070	2.420	2.450
E	.600	.620	.600	.620	.600	.625	.600	.620	.600	.620
E1	.530	.550	.530	.550	.530	.550	.530	.550	.530	.560
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
eA	.610	.670	.610	.670	.610	.670	.610	.670	.610	.670
L	.120	.150	.120	.150	.125	.135	.120	.150	.120	.150
α	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°
S	.060	.080	.055	.080	.070	.080	.070	.085	.060	.075
Q1	.060	.080	.060	.080	.065	.075	.060	.080	.060	.080

4

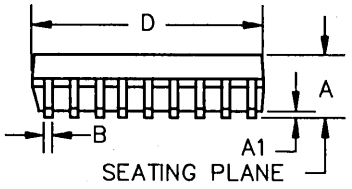
64 LEAD PLASTIC DIP (900 MIL)

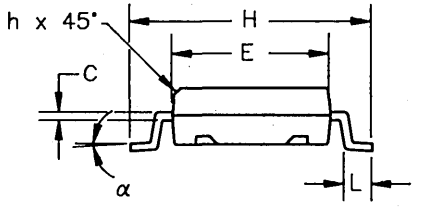
DWG #	P64-1	
# OF LEADS (N)	64	
SYMBOLS	MIN	MAX
A	.180	.230
A1	.015	.040
b	.015	.020
b1	.050	.065
C	.008	.012
D	3.200	3.220
E	.900	.925
E1	.790	.810
e	.090	.110
eA	.910	1.000
L	.120	.150
α	0°	15°
S	.045	.065
Q1	.080	.090

SMALL OUTLINE IC



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, ULESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND TO BE MEASURED FROM THE BOTTOM OF PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.

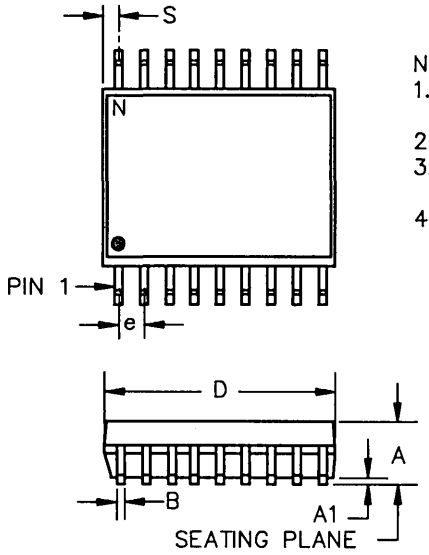




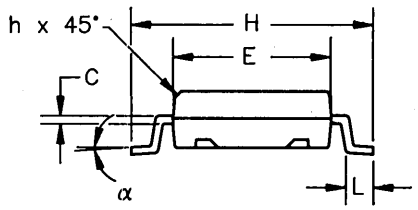
16–24 LEAD SMALL OUTLINE (GULL WING)

DWG #	SO16–1		SO18–1		SO20–2		SO24–2		SO24–3	
# OF LDS (N)	16 (.300)		18 (.300)		20 (.300")		24 (.300")		24 (.300")	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.095	.1043	.095	.1043	.095	.1043	.095	.1043	.110	.120
A1	.005	.0118	.005	.0118	.005	.0118	.005	.0118	.005	.0118
B	.014	.020	.014	.020	.014	.020	.014	.020	.014	.020
C	.0091	.0125	.0091	.0125	.0091	0125	.0091	.0125	.007	.011
D	.403	.413	.447	.462	.497	.511	.600	.614	.620	.630
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
E	.292	.2992	.292	.2992	.292	.2992	.292	.2992	.295	.305
h	.010	.020	.010	.020	.010	.020	.010	.020	.012	.020
H	.400	.419	.400	.419	.400	.419	.400	.419	.406	.419
L	.018	.045	.018	.045	.018	.045	.018	.045	.028	.045
α	0°	8°	0°	8°	0°	8°	0°	8°	0°	8°
S	.023	.035	.023	.035	.023	.035	.023	.035	.032	.043

SMALL OUTLINE IC (Continued)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.



4

28 LEAD SMALL OUTLINE (GULL WING)

DWG #	SO28–2		SO28–3	
# OF LDS (N)	28 (.300")		28 (.330")	
SYMBOL	MIN	MAX	MIN	MAX
A	.095	.1043	.110	.120
A1	.005	.0118	.005	.014
B	.014	.020	.014	.019
C	.0091	.0125	.006	.010
D	.700	.712	.718	.728
e	.050 BSC		.050 BSC	
E	.292	.2992	.340	.350
h	.010	.020	.012	.020
H	.400	.419	.462	.478
L	.018	.045	.028	.045
α	0°	8°	0°	8°
S	.023	.035	.023	.035

SMALL OUTLINE IC (Continued)

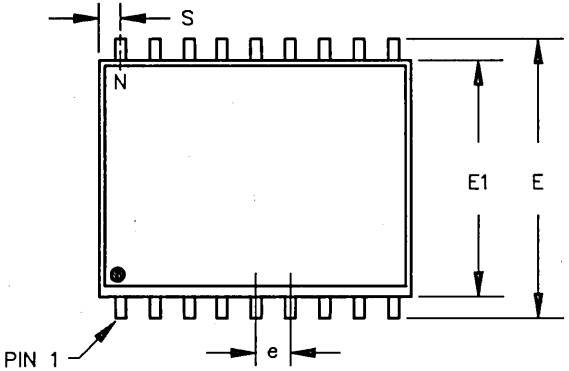
16–24 LEAD SMALL OUTLINE (EIAJ – .0315 PITCH)

DWG #	SO16–5		SO20–5		SO24–5	
# OF LDS (N)	16		20		24	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX
A	.057	.071	.069	.083	.069	.083
A1	.002 TYP		.002 TYP		.002 TYP	
B	.012	.020	.012	.020	.012	.020
C	.006	.010	.006	.010	.006	.010
D	.248	.271	.331	.354	.382	.405
E	.165	.180	.205	.220	.205	.220
e	.0315 BSC		.0315 BSC		.0315 BSC	
H	.232	.256	.295	.319	.295	.319
L	.010	–	.010	–	.010	–
α	0°	8°	0°	8°	0°	8°

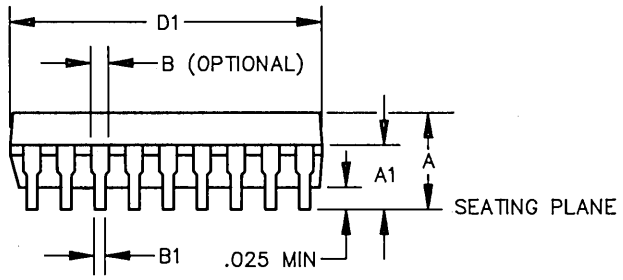
16–28 LEAD SMALL OUTLINE (EIAJ – .050 PITCH)

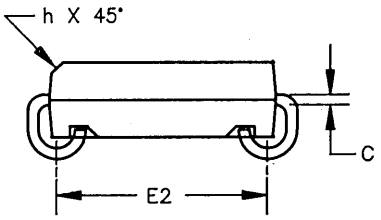
DWG #	SO16–6		SO18–6		SO20–6		SO24–6		SO28–6	
# OF LDS (N)	16		18		20		24		28	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.057	.071	.069	.083	.069	.083	.069	.083	.083	.098
A1	.002 TYP		.002 TYP		.002 TYP		.002 TYP		.002 TYP	
B	.012	.020	.012	.020	.012	.020	.012	.020	.012	.020
C	.006	.010	.006	.010	.006	.010	.006	.010	.006	.010
D	.382	.406	.437	.453	.480	.504	.580	.603	.720	.740
E	.165	.180	.205	.220	.205	.220	.205	.220	.290	.300
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
H	.232	.256	.295	.319	.295	.319	.295	.319	.378	.402
L	.010	–	.010	–	.010	–	.010	–	.010	–
α	0°	8°	0°	8°	0°	8°	0°	8°	0°	8°

SMALL OUTLINE IC (Continued)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSION AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE

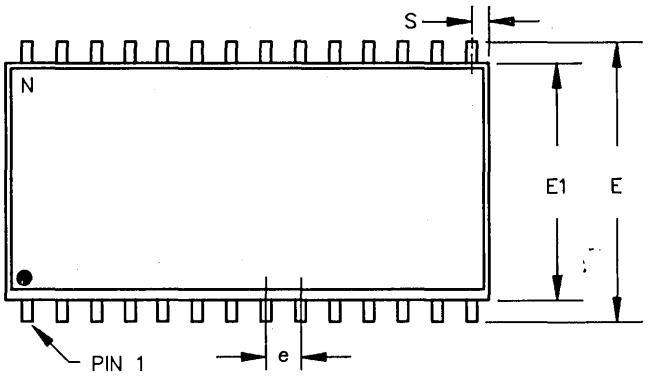




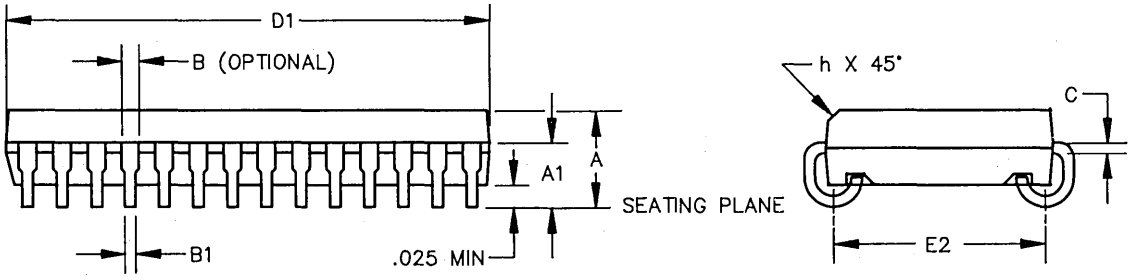
16–24 LEAD SMALL OUTLINE (J–BEND)

DWG #	SO16–2		SO20–1		SO24–4	
# OF LDS (N)	16 LD (.300")		20 LD (.300")		24 LD (.300")	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX
A	.120	.140	.120	.140	.130	.148
A1	.078	.095	.078	.095	.082	.095
B	.020	.024	.020	.024	.026	.032
B1	.014	.020	.014	.020	.015	.020
C	.008	.013	.008	.013	.007	.011
D1	.400	.412	.500	.512	.620	.630
E	.335	.347	.335	.347	.335	.345
E1	.292	.300	.292	.300	.295	.305
E2	.262	.272	.262	.272	.260	.280
e	.050 BSC		.050 BSC		.050 BSC	
h	.010	.020	.010	.020	.010	.020
S	.023	.035	.023	.035	.032	.043

SMALL OUTLINE IC (Continued)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSION AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.

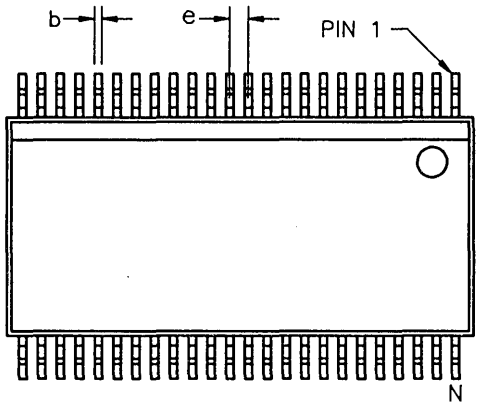


28–32 LEAD SMALL OUTLINE (J–BEND)

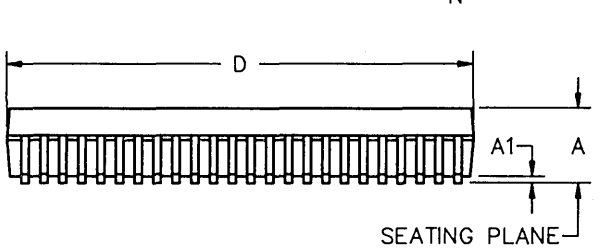
DWG #	SO28–5		SO28–4		SO32–2	
# OF LDS (N)	28 LD (.300")		28 LD (.350")		32 LD (.300")	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX
A	.120	.140	.130	.148	.130	.148
A1	.078	.095	.082	.095	.082	.095
B	.020	.024	.026	.032	.026	.032
B1	.014	.020	.016	.020	.016	.020
C	.008	.013	.007	.011	.008	.013
D1	.700	.712	.720	.730	.820	.830
E	.335	.347	.380	.390	.330	.340
E1	.292	.300	.345	.355	.295	.305
E2	.262	.272	.310	.330	.260	.275
e	.050 BSC		.050 BSC		.050 BSC	
h	.012	.020	.012	.020	.012	.020
S	.023	.035	.023	.035	.032	.043

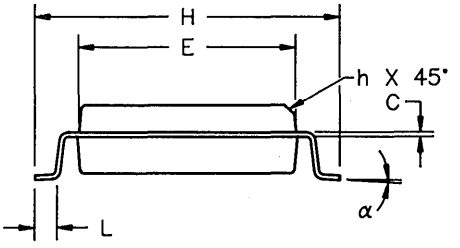
SMALL OUTLINE IC (Continued)

48 & 56 LEAD SMALL OUTLINE (SSOP – GULL WING)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.

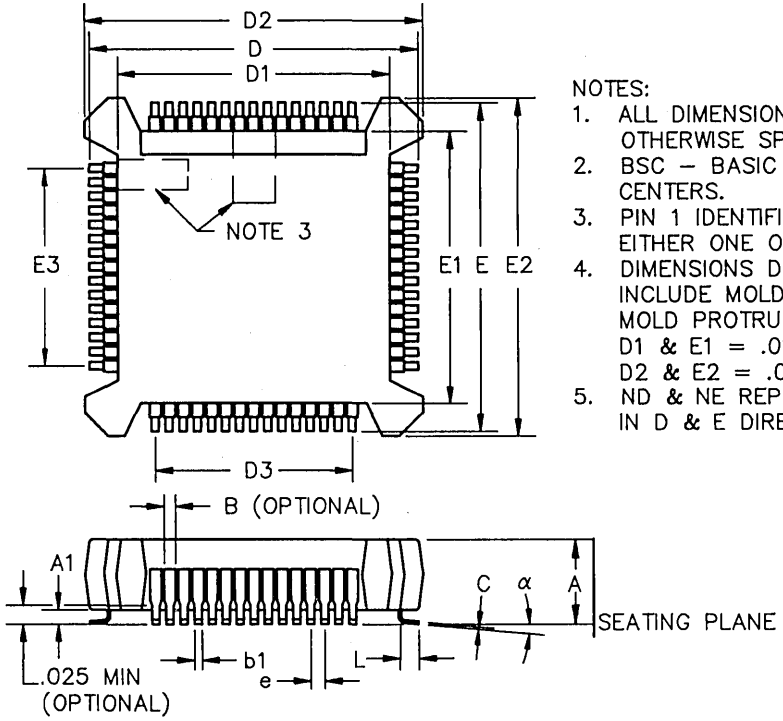




DWG #	SO48–1		SO56–1	
# OF LDS (N)	48 (.300")		56 (.300")	
SYMBOL	MIN	MAX	MIN	MAX
A	.095	.110	.095	.110
A1	.008	.016	.008	.016
b	.008	.012	.008	.012
C	.005	.009	.005	.009
D	.620	.630	.720	.730
E	.291	.299	.291	.299
e	.025 BSC		.025 BSC	
H	.395	.420	.395	.420
h	.015	.025	.015	.025
L	.020	.040	.020	.040
α	0°	8°	0°	8°

PLASTIC QUAD FLATPACKS

100–132 LEAD PLASTIC QUAD FLATPACK (JEDEC)

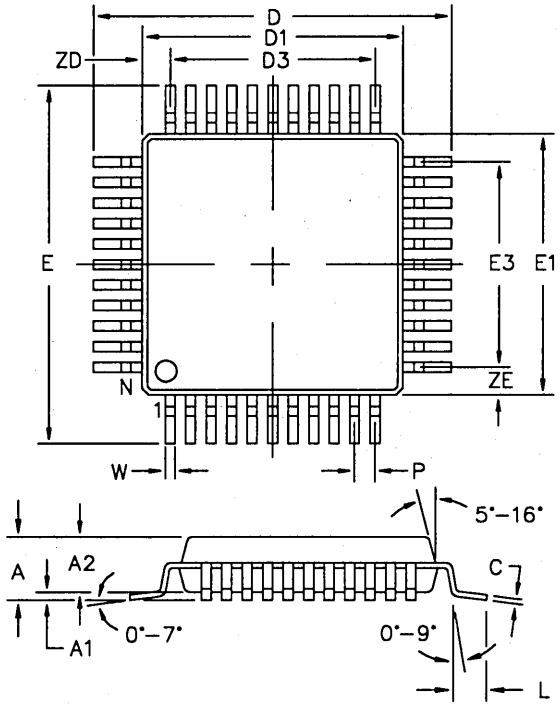


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. PIN 1 IDENTIFIER CAN BE POSITIONED AT EITHER ONE OF THESE TWO LOCATIONS.
4. DIMENSIONS D1, D2, E1, AND E2 DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE MOLD PROTRUSIONS ARE AS FOLLOWS:
   D1 & E1 = .010 MAX.
   D2 & E2 = .007 MAX.
5. ND & NE REPRESENT NUMBERS OF LEADS IN D & E DIRECTIONS RESPECTIVELY.

DWG #	PQ100–1		PQ132–1	
# OF LDS (N)	100		132	
SYMBOLS	MIN	MAX	MIN	MAX
A	.160	.180	.160	.180
A1	.020	.040	.020	.040
B	.008	.016	.008	.016
b1	.008	.012	.008	.012
C	.0055	.008	.0055	.008
D	.875	.885	1.075	1.085
D1	.747	.753	.947	.953
D2	.897	.903	1.097	1.103
D3	.600 REF		.800 REF	
e	.025 BSC		.025 BSC	
E	.875	.885	1.075	1.085
E1	.747	.753	.947	.953
E2	.897	.903	1.097	1.103
E3	.600 REF		.800 REF	
L	.020	.030	.020	.030
α	0°	8°	0°	8°
ND/NE	25/25		33/33	

PLASTIC QUAD FLATPACKS (Continued)

80–128 LEAD PLASTIC QUAD FLATPACK (EIAJ)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .010 PER SIDE.
4. ND & NE REPRESENT NUMBERS OF LEADS IN D & E DIRECTIONS RESPECTIVELY.
5. THE 3.9mm FOOTPRINT IS STANDARD, HOWEVER THE 3.2mm IS OPTIONAL & CAN BE REQUESTED.

DWG #	PQ80–2		PQ100–2		PQ120–2		PQ128–2	
# OF LDS (N)	80		100		120		128	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.110	.124	.110	.124	.136	.156	.136	.156
A1	.010	–	.010	–	.010	–	.010	–
A2	.100	.120	.100	.120	.125	.144	.125	.144
C	.005	.008	.005	.008	.005	.008	.005	.008
D	.937	.945	.937	.945	1.252	1.260	1.252	1.260
D1	.783	.791	.783	.791	1.098	1.106	1.098	1.106
D3	.724 REF		.742 REF		.913 REF		.976 REF	
E	.701	.709	.701	.709	1.252	1.260	1.252	1.260
E1	.547	.555	.547	.555	1.098	1.106	1.098	1.106
E3	.472 REF		.486 REF		.913 REF		.976 REF	
L	.026	.037	.026	.037	.026	.037	.026	.037
ND/NE	16/24		20/30		30/30		32/32	
P	.0315 BSC		.026 BSC		.026 BSC		.0315 BSC	
W	.010	.018	.012	.018	.012	.018	.012	.018
ZD	.032		.023		.094		.063	
ZE	.039		.032		.094		.063	

ALT. D [5]	.909	.917	.909	.917	1.224	1.232	1.224	1.232
ALT. E [5]	.673	.681	.673	.681	1.224	1.232	1.224	1.232

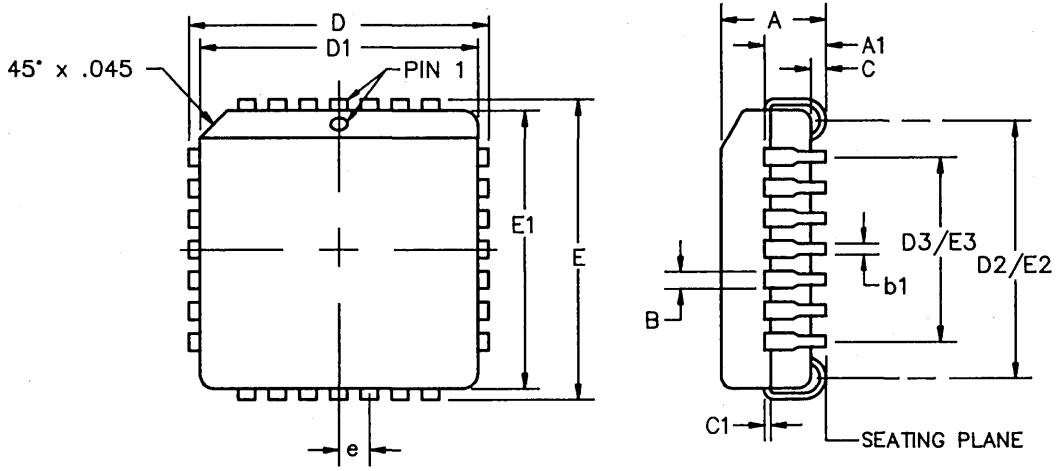
PLASTIC QUAD FLATPACKS (Continued)

144–208 LEAD PLASTIC QUAD FLATPACK (EIAJ)

DWG #	PQ144–2		PQ160–2		PQ184–2		PQ208–2	
# OF LDS (N)	144		160		184		208	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.136	.156	.136	.156	.136	.156	.136	.156
A1	.010	–	.010	–	.010	–	.010	–
A2	.125	.144	.125	.144	.125	.144	.125	.144
C	.005	.008	.005	.008	.005	.008	.005	.008
D	1.224	1.232	1.224	1.232	1.224	1.232	1.224	1.232
D1	1.098	1.106	1.098	1.106	1.098	1.106	1.098	1.106
D3	.896 REF		.998 REF		.886 REF		1.004 REF	
E	1.224	1.232	1.224	1.232	1.224	1.232	1.224	1.232
E1	1.098	1.106	1.098	1.106	1.098	1.106	1.098	1.106
E3	.896 REF		.998 REF		.886 REF		1.004 REF	
L	.026	.037	.026	.037	.026	.037	.026	.037
ND/NE	36/36		40/40		46/46		52/52	
P	.026 BSC		.026 BSC		.020 BSC		.020 BSC	
W	.009	.014	.009	.014	.009	.014	.009	.014
ZD	.103		.052		.108		.049	
ZE	.103		.052		.108		.049	

PLASTIC LEADED CHIP CARRIERS

20–84 LEAD PLCC (SQUARE)



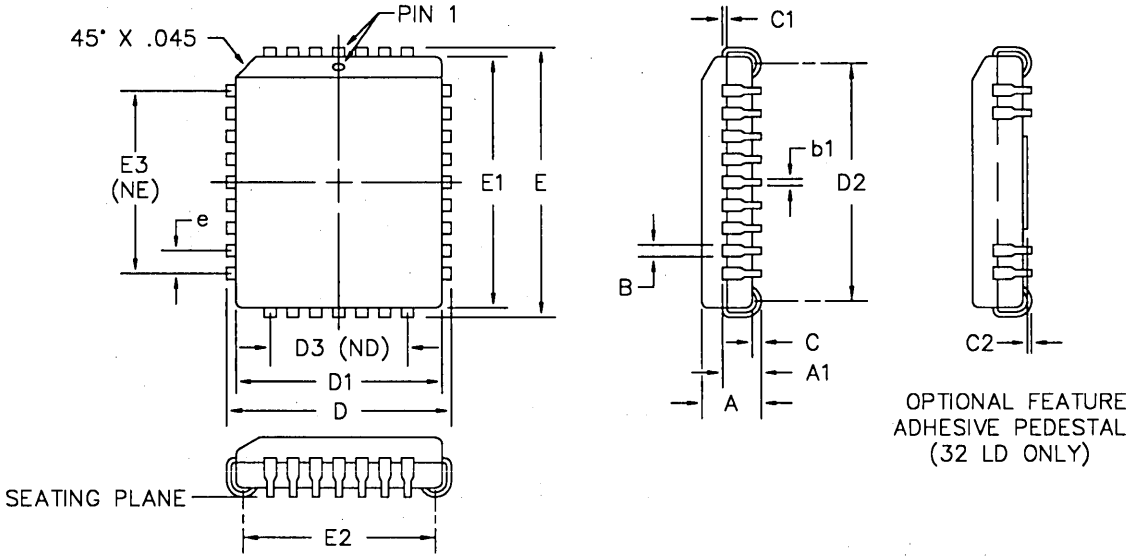
NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.
5. ND & NE REPRESENT NUMBER OF LEADS IN D & E DIRECTIONS RESPECTIVELY.
6. D1 & E1 SHOULD BE MEASURED FROM THE BOTTOM OF THE PKG.

DWG #	J20–1		J28–1		J44–1		J52–1		J68–1		J84–1	
# OF LDS	20		28		44		52		68		84	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.165	.180	.165	.180	.165	.180	.165	.180	.165	.180	.165	.180
A1	.095	.115	.095	.115	.095	.115	.095	.115	.095	.115	.095	.115
B	.026	.032	.026	.032	.026	.032	.026	.032	.026	.032	.026	.032
b1	.013	.021	.013	.021	.013	.021	.013	.021	.013	.021	.013	.021
C	.020	.040	.020	.040	.020	.040	.020	.040	.020	.040	.020	.040
C1	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012
D	.385	.395	.485	.495	.685	.695	.785	.795	.985	.995	1.185	1.195
D1	.350	.356	.450	.456	.650	.656	.750	.756	.950	.956	1.150	1.156
D2/E2	.290	.330	.390	.430	.590	.630	.690	.730	.890	.930	1.090	1.130
D3/E3	.200	REF	.300	REF	.500	REF	.600	REF	.800	REF	1.000	REF
E	.385	.395	.485	.495	.685	.695	.785	.795	.985	.995	1.185	1.195
E1	.350	.356	.450	.456	.650	.656	.750	.756	.950	.956	1.150	1.156
e	.050	BSC	.050	BSC	.050	BSC	.050	BSC	.050	BSC	.050	BSC
ND/NE	5		7		11		13		17		21	

PLASTIC LEADED CHIP CARRIERS (Continued)

18–32 LEAD PLCC (RECTANGULAR)

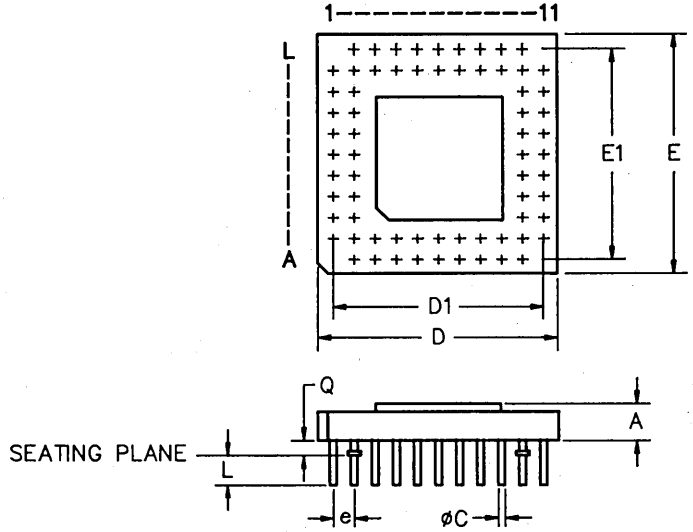


DWG #	J18–1		J32–1	
# OF LDS	18		32	
SYMBOL	MIN	MAX	MIN	MAX
A	.120	.140	.120	.140
A1	.075	.095	.075	.095
B	.026	.032	.026	.032
b1	.013	.021	.013	.021
C	.015	.040	.015	.040
C1	.008	.012	.008	.012
C2	–	–	.005	.015
D	.320	.335	.485	.495
D1	.289	.293	.449	.453
D2	.225	.265	.390	.430
D3	.150 REF		.300 REF	
E	.520	.535	.585	.595
E1	.489	.493	.549	.553
E2	.422	.465	.490	.530
E3	.200 REF		.400 REF	
e	.050 BSC		.050 BSC	
ND/NE	4 / 5		7 / 9	

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.
5. ND & NE REPRESENT NUMBERS OF LEADS IN D & E DIRECTIONS RESPECTIVELY.
6. D1 & E1 SHOULD BE MEASURED MEASURED FROM THE BOTTOM OF THE PACKAGE.

PLASTIC PIN GRID ARRAYS

68–208 PIN PGA (CAVITY UP)



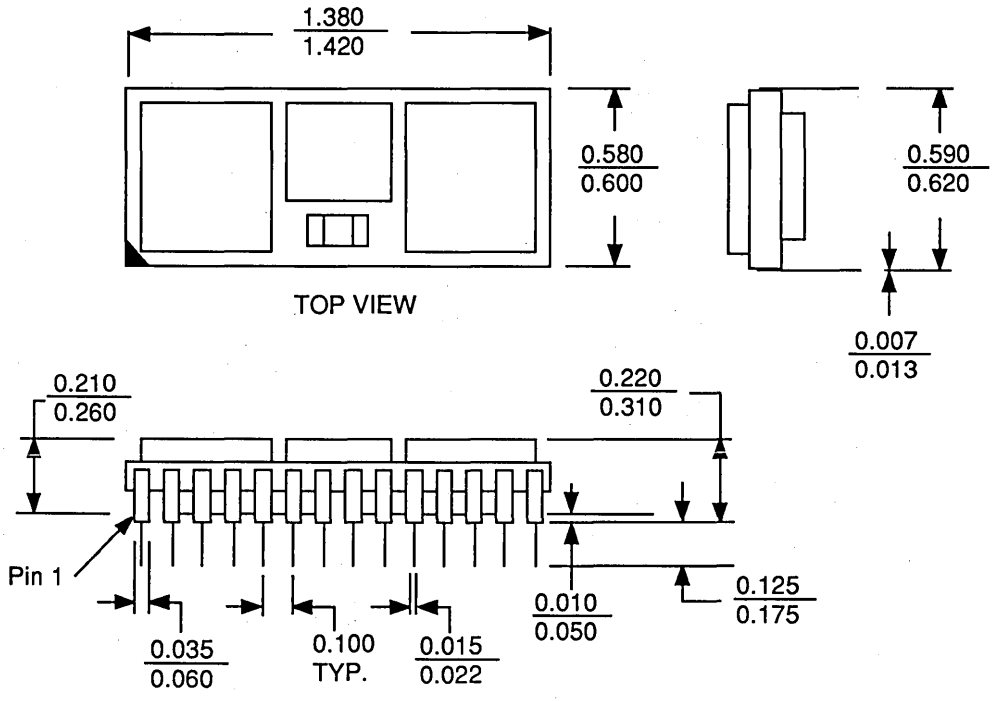
NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC PIN SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS.
5. DIM. "A" INCLUDES BOTH THE PKG BODY & THE LID. IT DOES NOT INCLUDE HEATSINK OR OTHER ATTACHED FEATURES.
6. PIN DIAMETER "C" EXCLUDES SOLDER DIP OR OTHER LEAD FINISH.
7. PIN TIPS MAY HAVE RADIUS OR CHAMFER.

DWG No.	PG 68–2		PG 84–2		PG 208–2	
# OF PINS (N)	68 PIN		84 PIN		208 PIN	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX
A	.115	.160	.115	.160	.115	.160
C	.016	.020	.016	.020	.016	.020
D	1.140	1.180	1.140	1.180	1.740	1.780
D1	1.000 BSC		1.000 BSC		1.600 BSC	
E	1.140	1.180	1.140	1.180	1.740	1.780
E1	1.000 BSC		1.000 BSC		1.600 BSC	
e	.100 BSC		.100 BSC		.100 BSC	
L	.100	.160	.100	.160	.100	.160
M	11		11		17	
Q	.040	.070	.040	.070	.040	.070

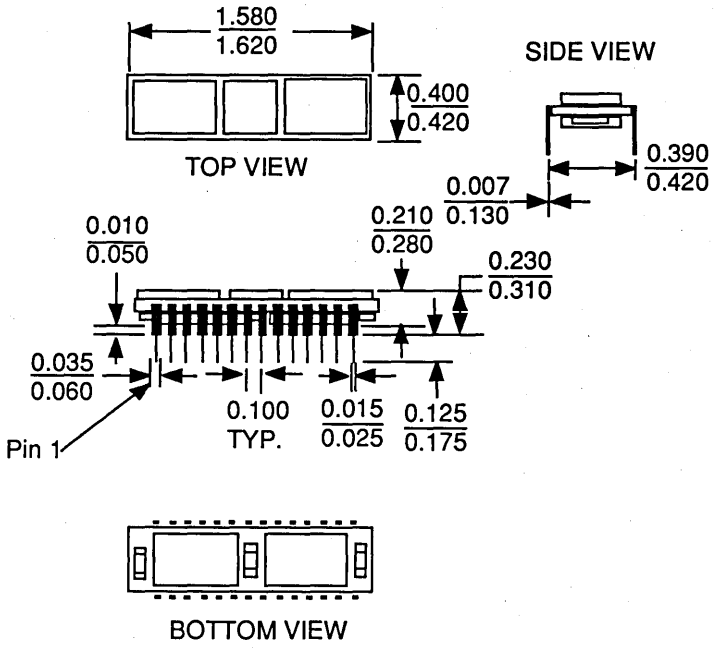
DUAL IN-LINE PACKAGES

28-Pin Ceramic Sidebraze DIP – M1



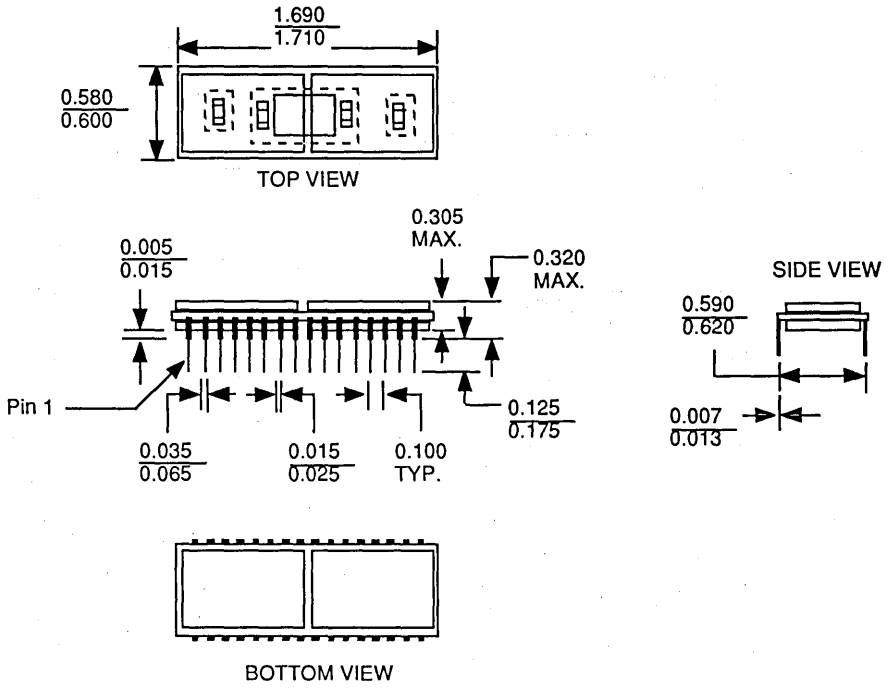
DUAL IN-LINE PACKAGES (Continued)

28-Pin Ceramic Sidebraze DIP – M2



DUAL IN-LINE PACKAGES (Continued)

32-Pin Ceramic Sidebraze DIP – M3

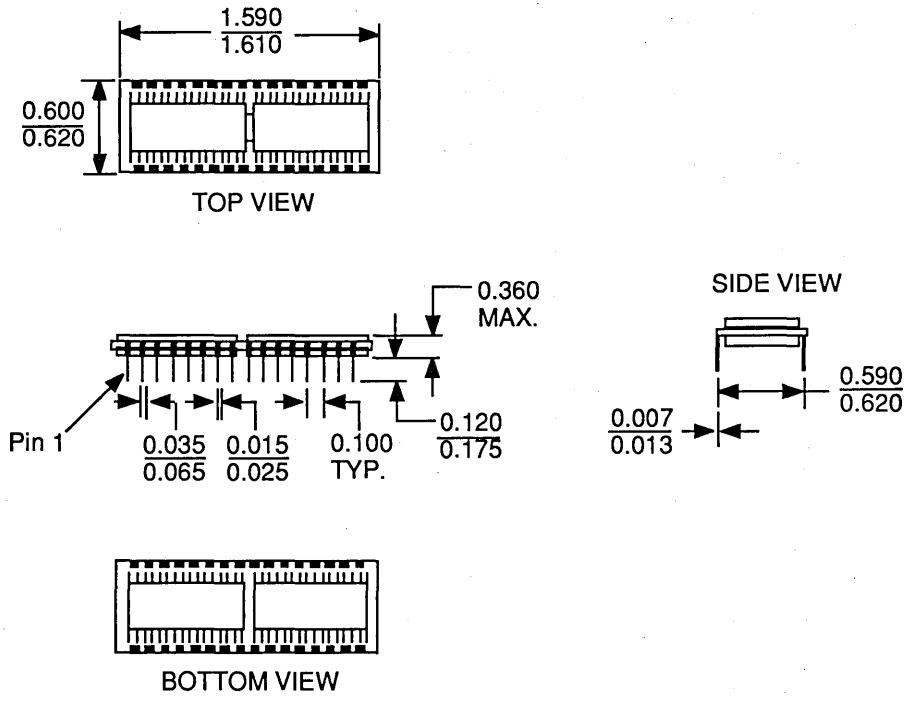


DUAL IN-LINE PACKAGES (Continued)

32-Pin Ceramic Sidebraze DIP – M4

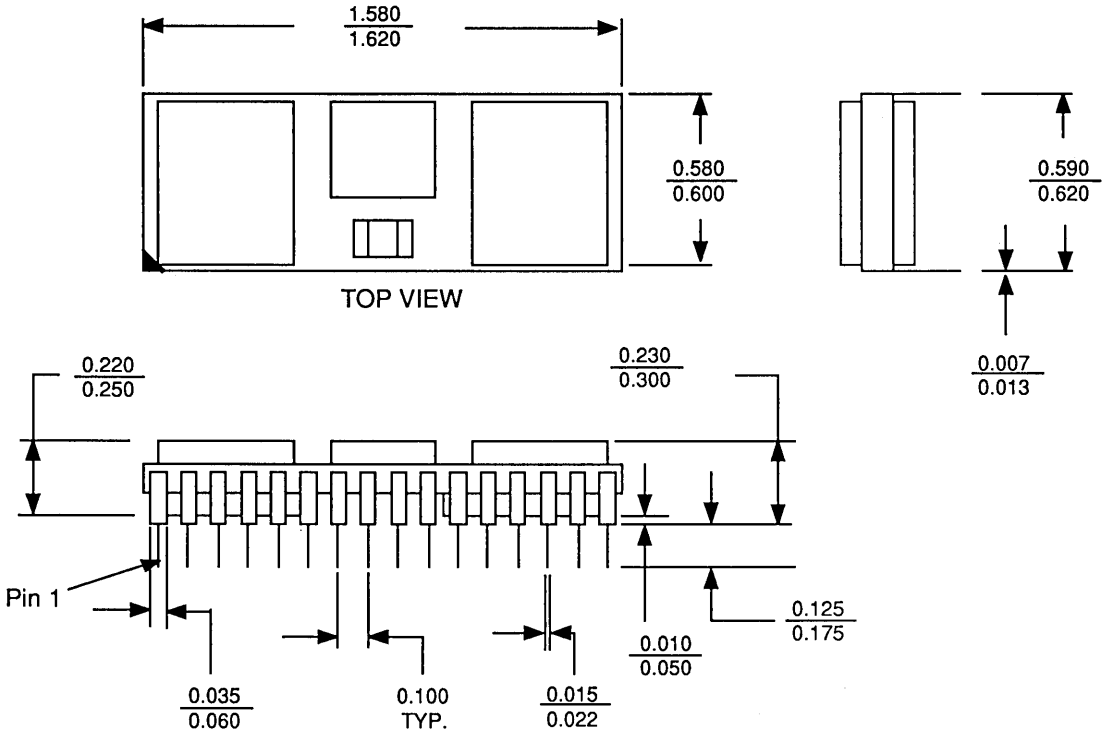
MODULE DIMENSIONS FOR PACKAGE M4 ARE NOT YET AVAILABLE.
PLEASE CONSULT THE FACTORY FOR FURTHER DETAILS.

32-Pin FR-4 DIP – M5



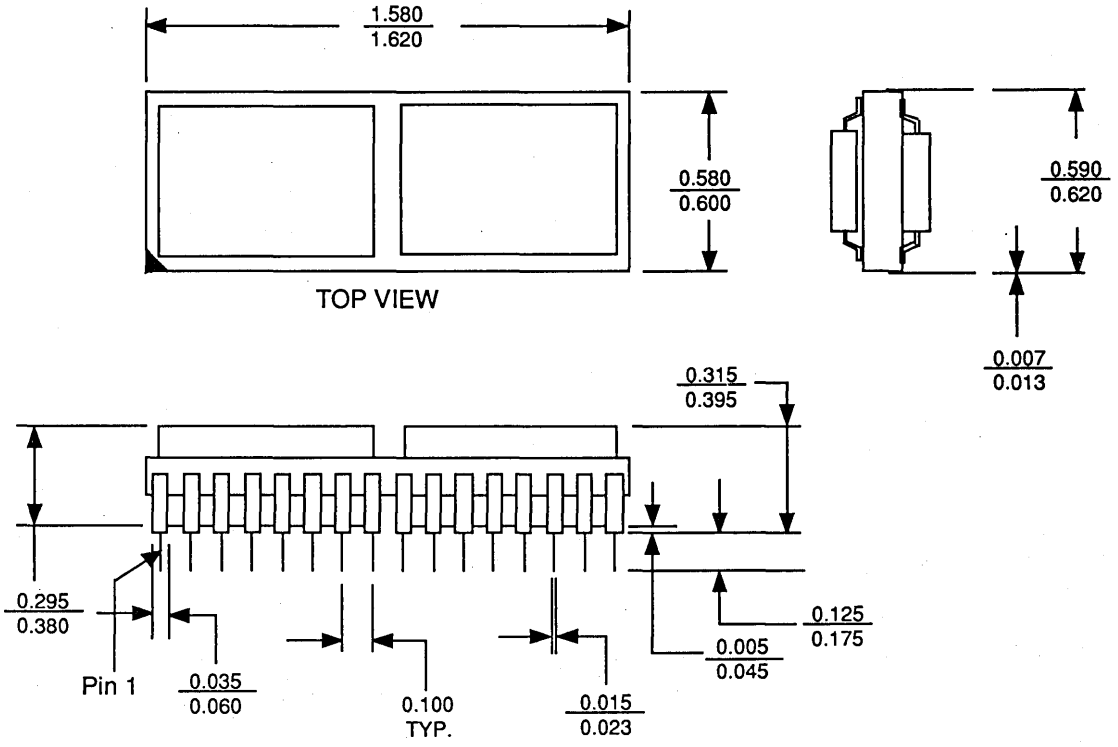
DUAL IN-LINE PACKAGES (Continued)

32-Pin Ceramic Sidebraze DIP – M6



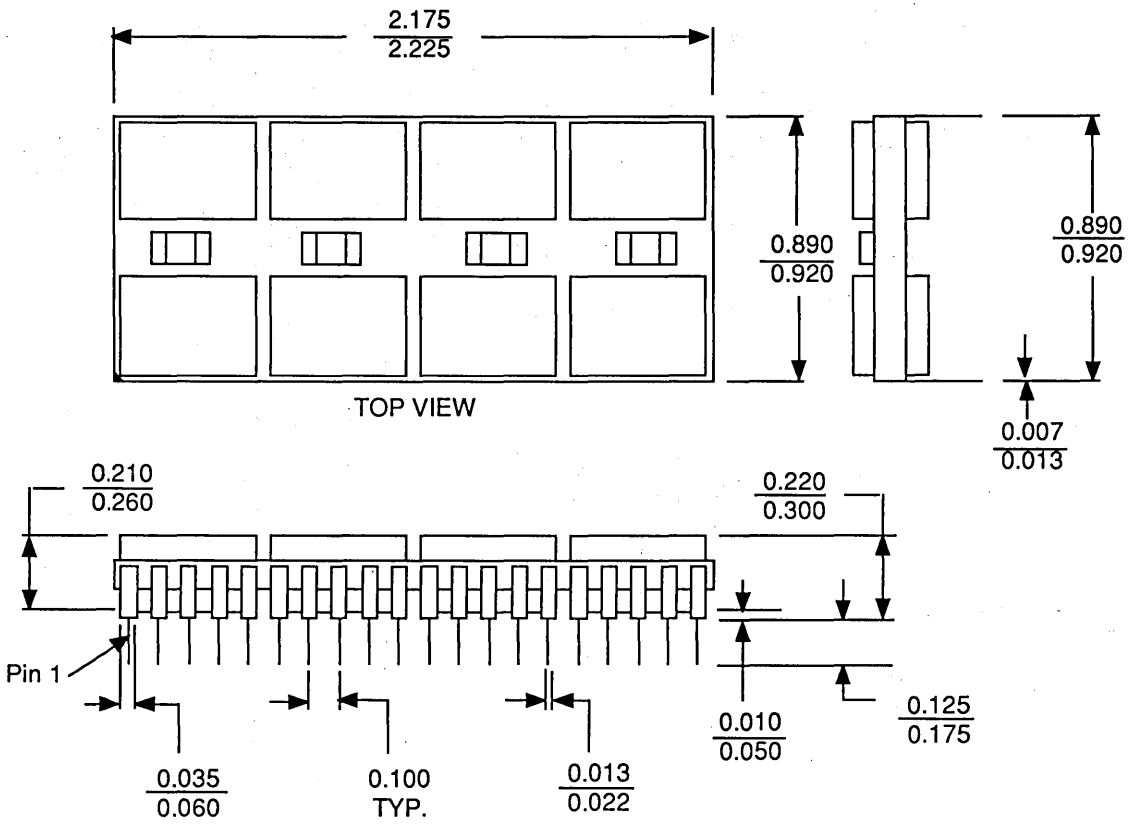
DUAL IN-LINE PACKAGES (Continued)

32-Pin Ceramic Sidebraze DIP – M7



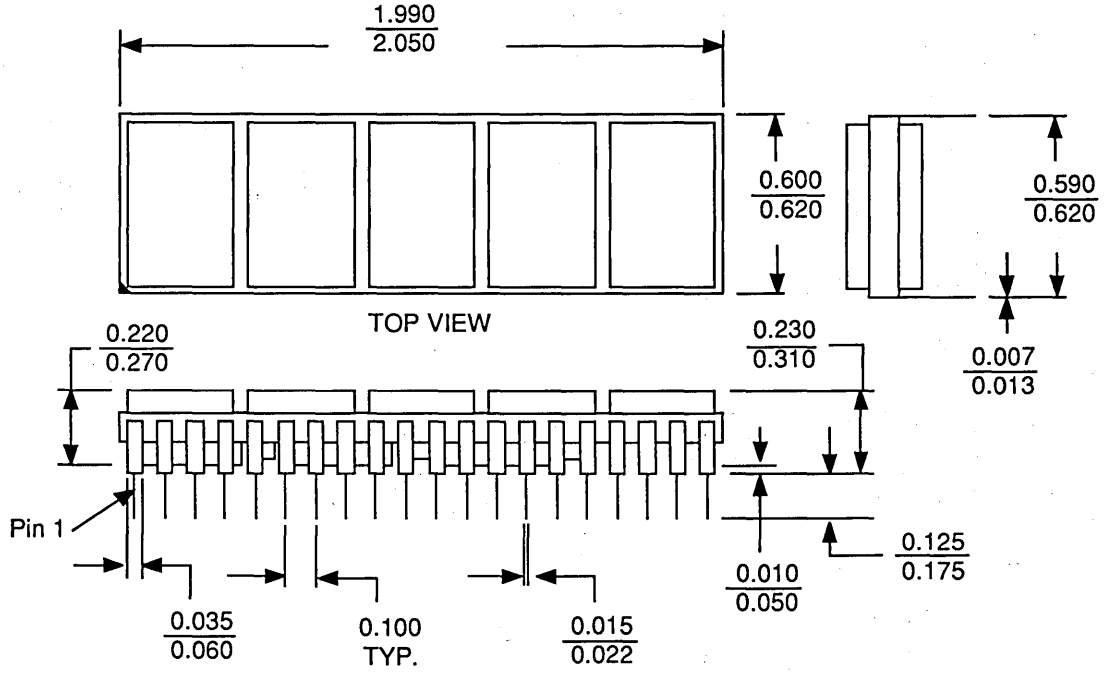
DUAL IN-LINE PACKAGES (Continued)

40-Pin Ceramic Sidebraze DIP – M8



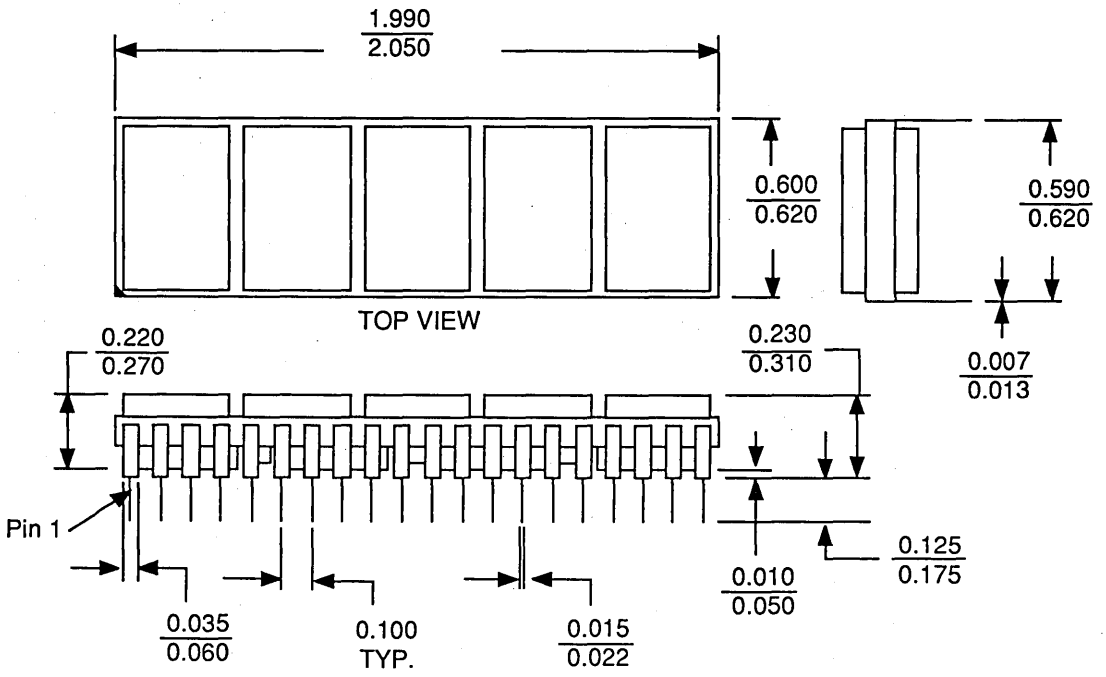
DUAL IN-LINE PACKAGES (Continued)

40-Pin Ceramic Sidebraze DIP – M9



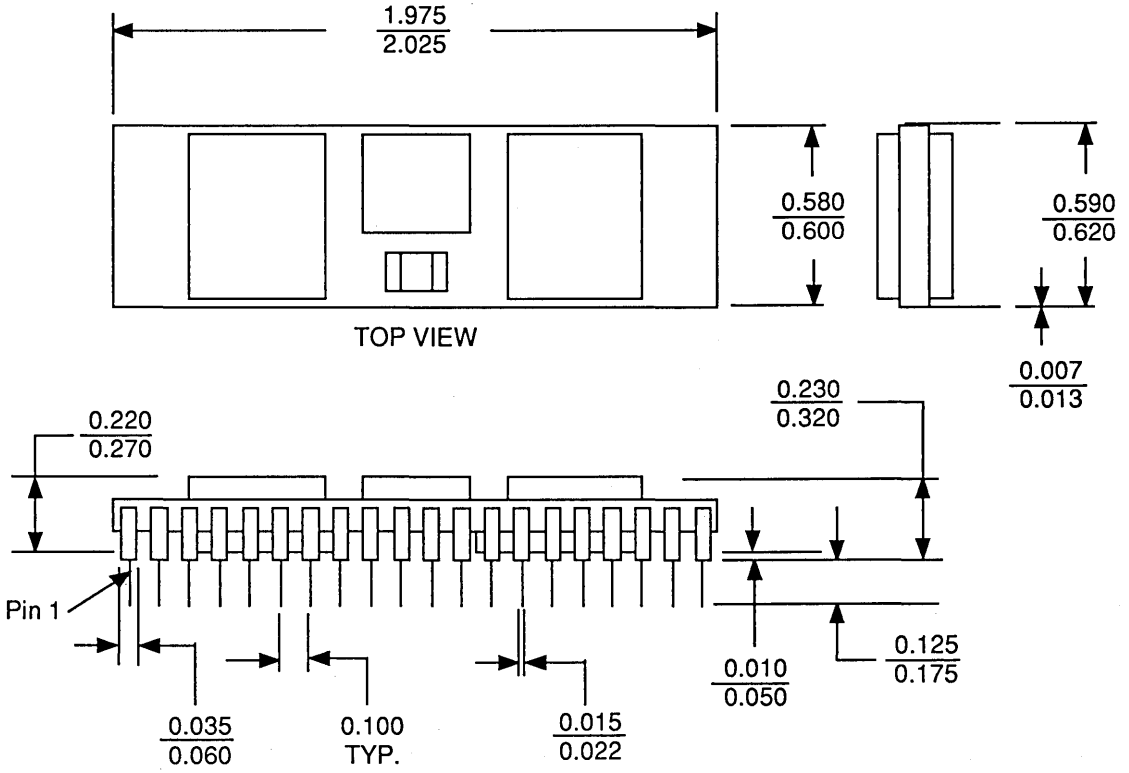
DUAL IN-LINE PACKAGES (Continued)

40-Pin Ceramic Sidebraze DIP – M10



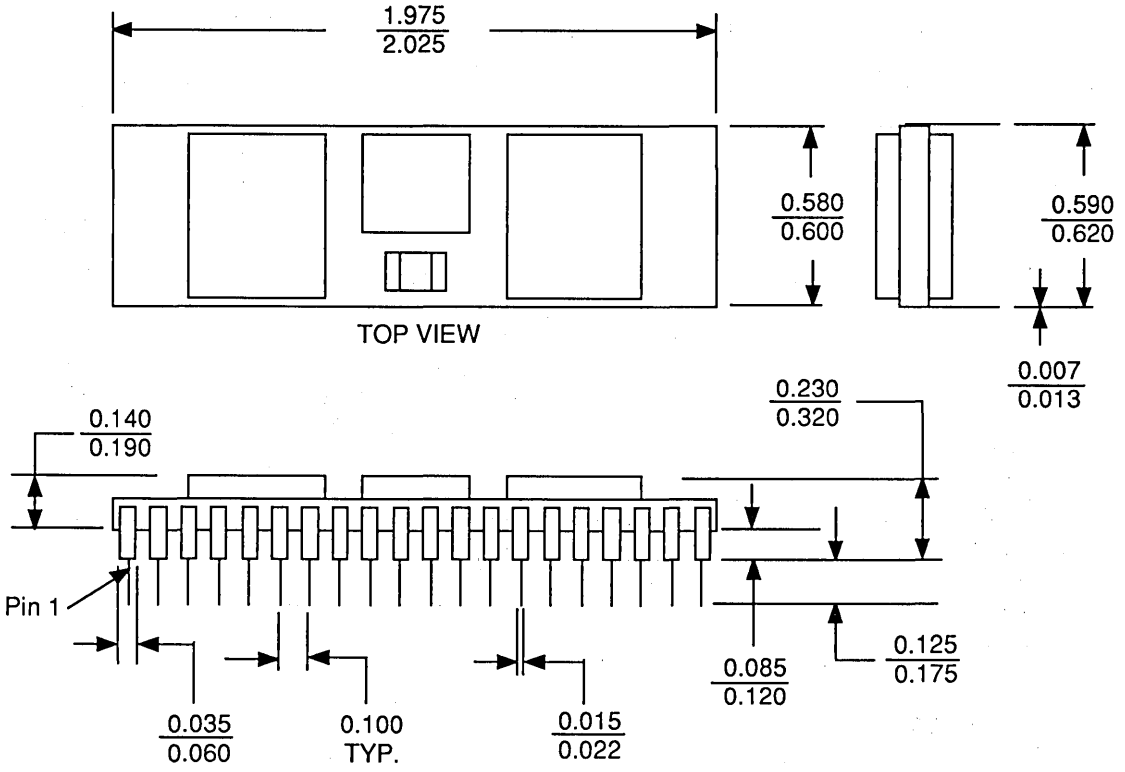
DUAL IN-LINE PACKAGES (Continued)

40-Pin Ceramic Sidebraze DIP – M11



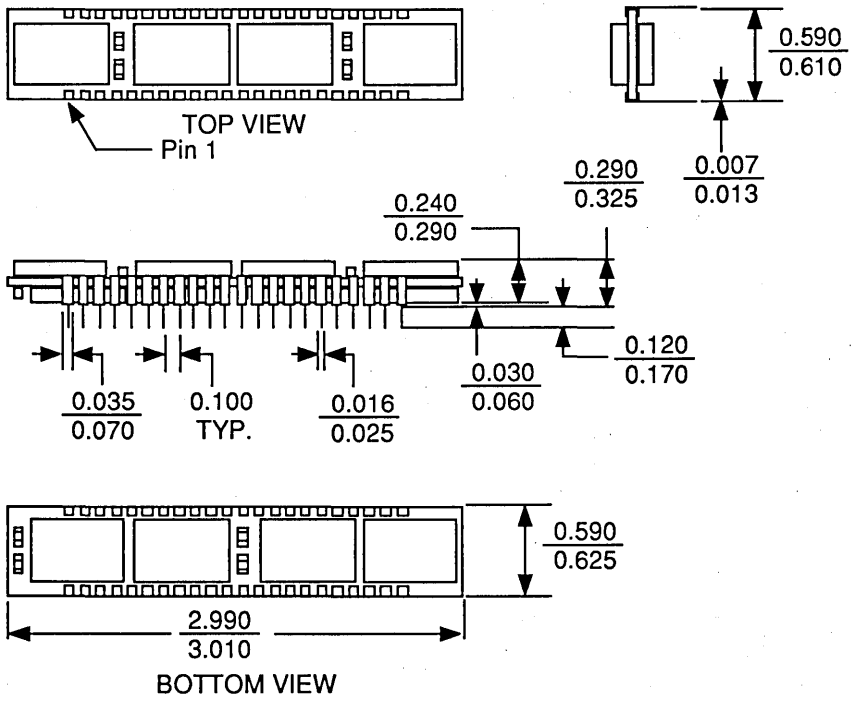
DUAL IN-LINE PACKAGES (Continued)

40-Pin Ceramic Sidebraze DIP – M12



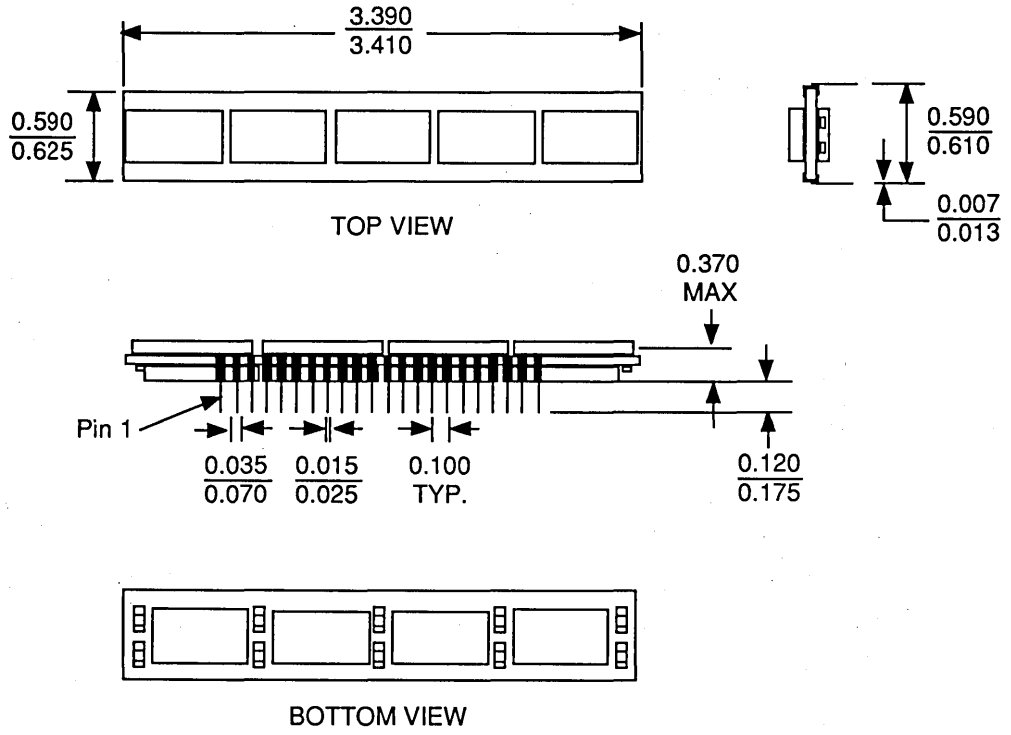
DUAL IN-LINE PACKAGES (Continued)

44-Pin FR-4 DIP – M13



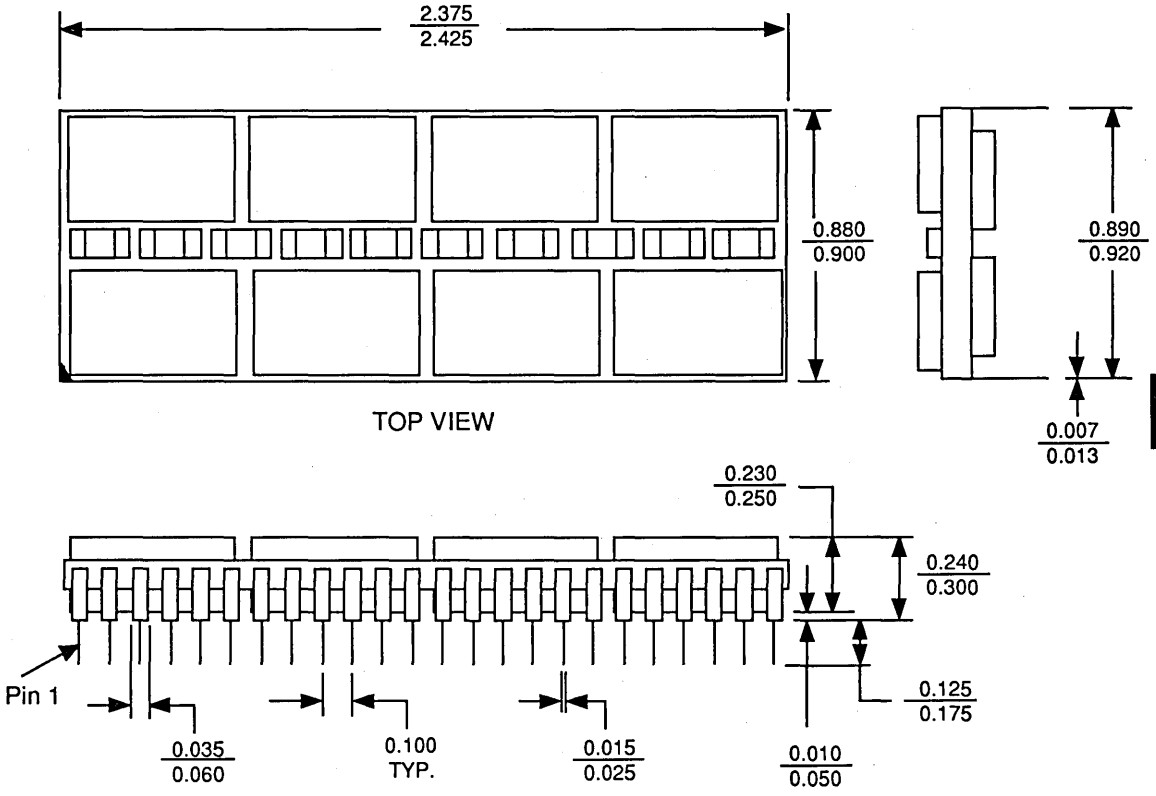
DUAL IN-LINE PACKAGES (Continued)

44-Pin FR-4 DIP – M14



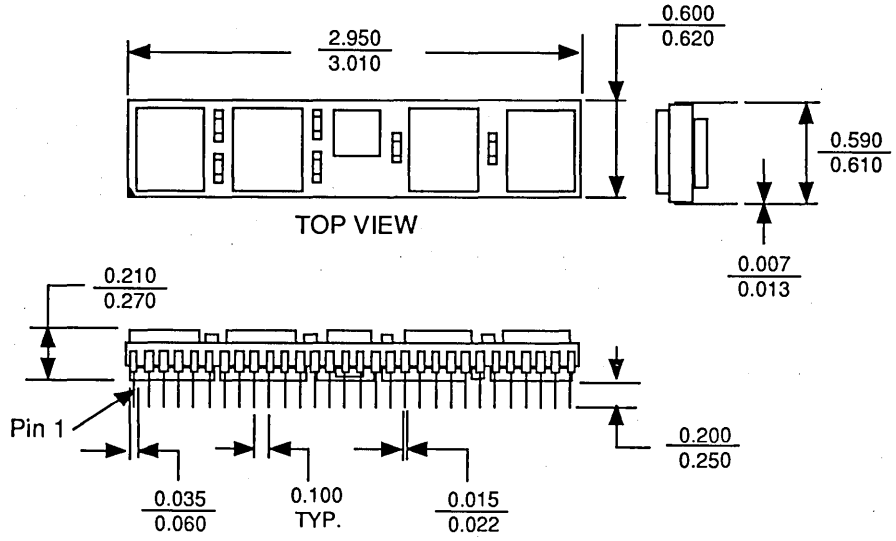
DUAL IN-LINE PACKAGES (Continued)

48-Pin Ceramic Sidebraze DIP – M15

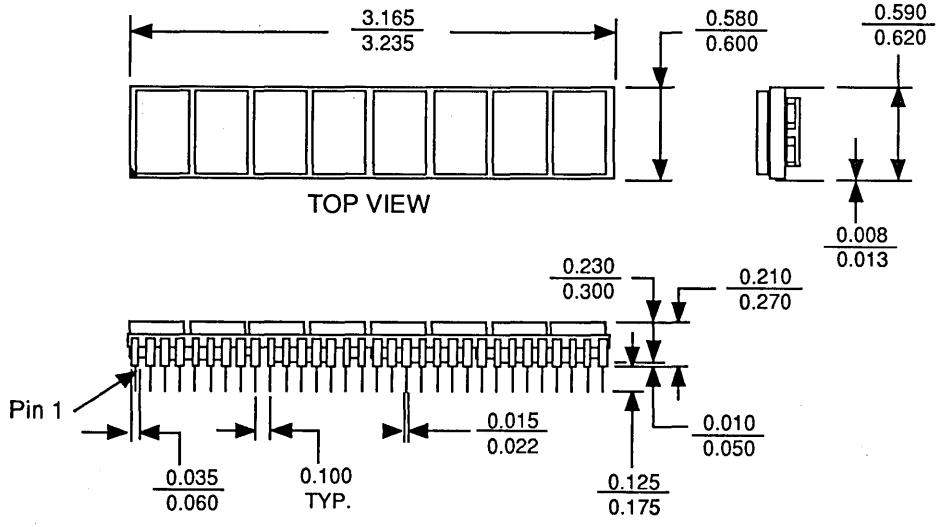


DUAL IN-LINE PACKAGES (Continued)

60-Pin Ceramic Sidebraze DIP – M16

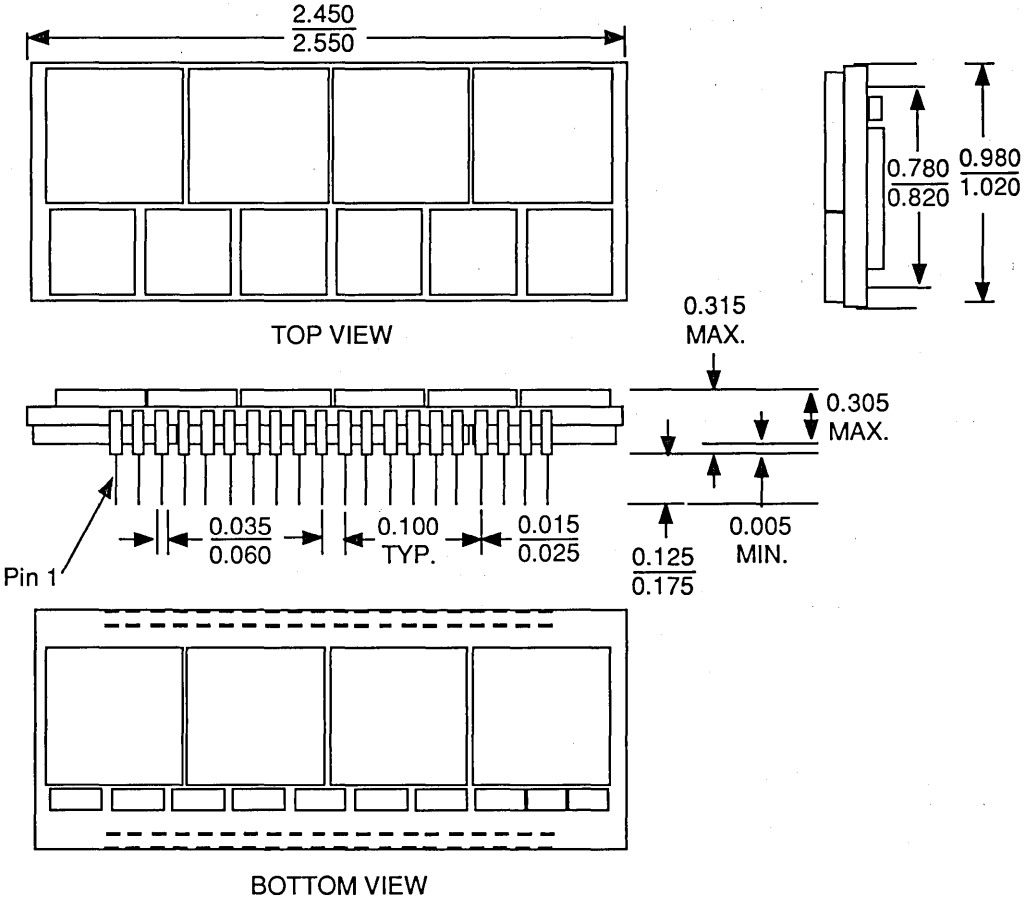


64-Pin Ceramic Sidebraze DIP – M17



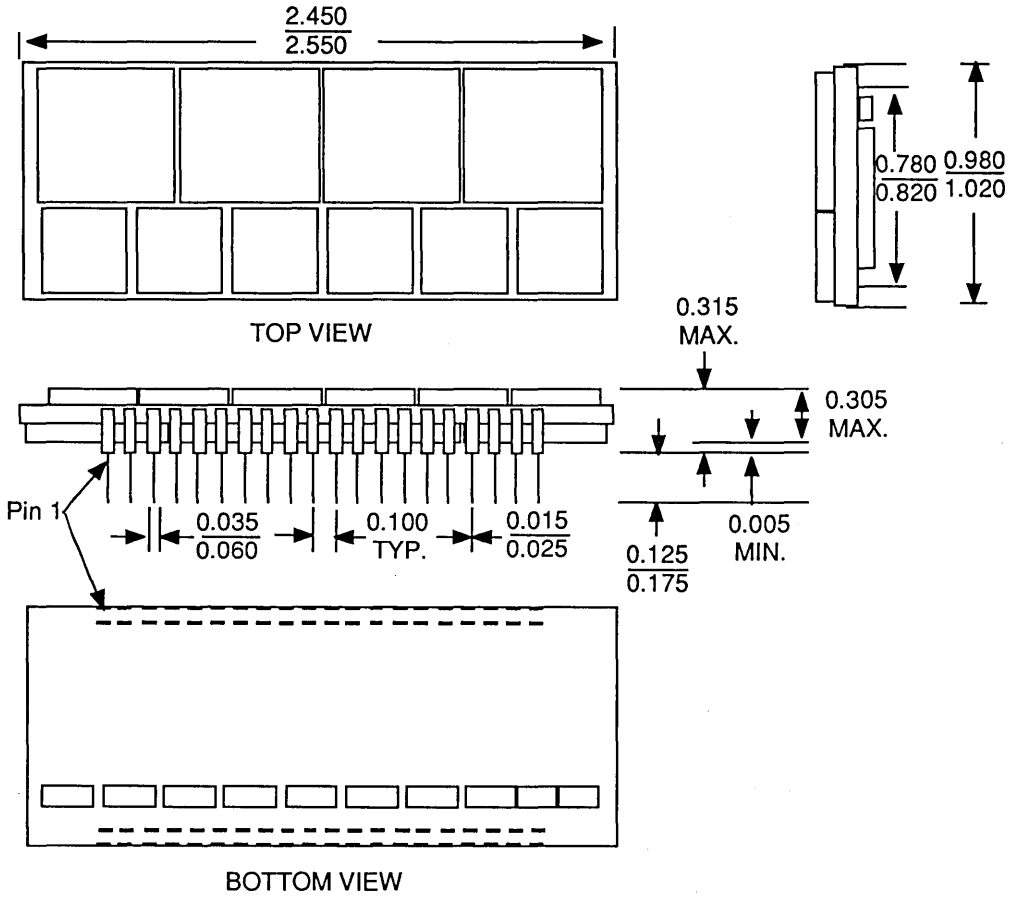
QUAD IN-LINE PACKAGES

80-Pin Ceramic Sidebraze QIP – M18



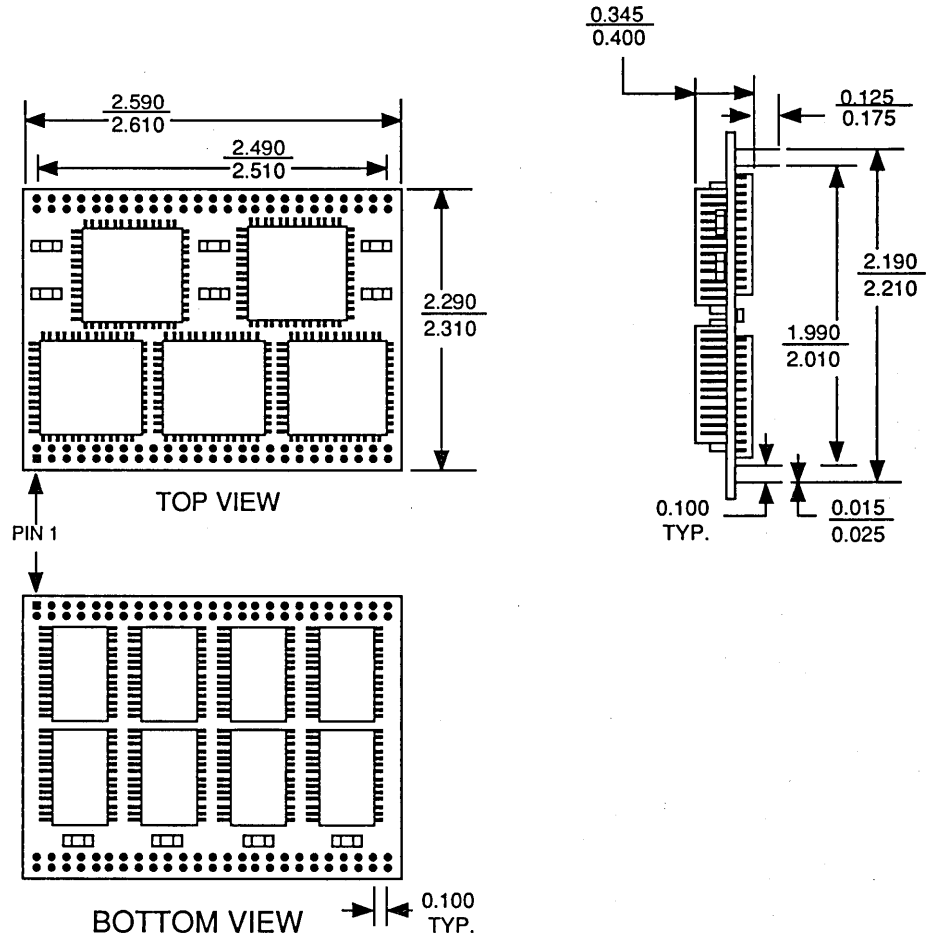
QUAD IN-LINE PACKAGES (Continued)

80-Pin Ceramic Sidebraze QIP – M19



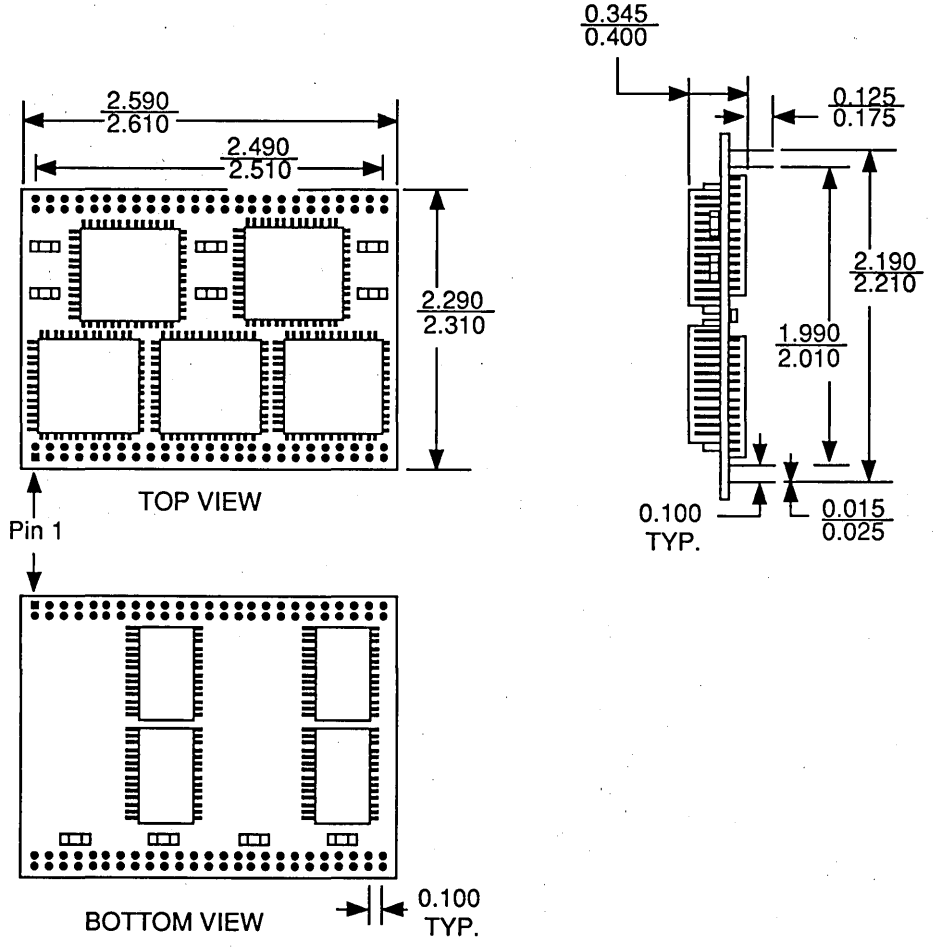
QUAD IN-LINE PACKAGES (Continued)

92-Pin FR-4 QIP – M20



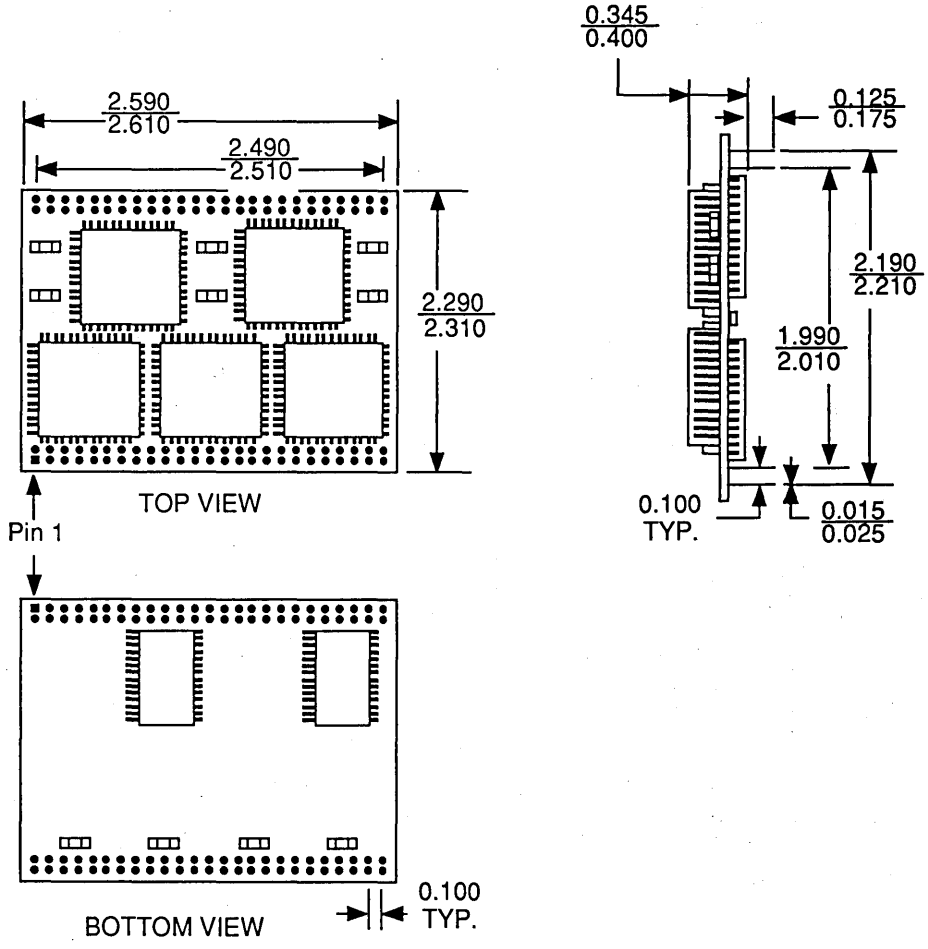
QUAD IN-LINE PACKAGES (Continued)

92-Pin FR-4 QIP – M21



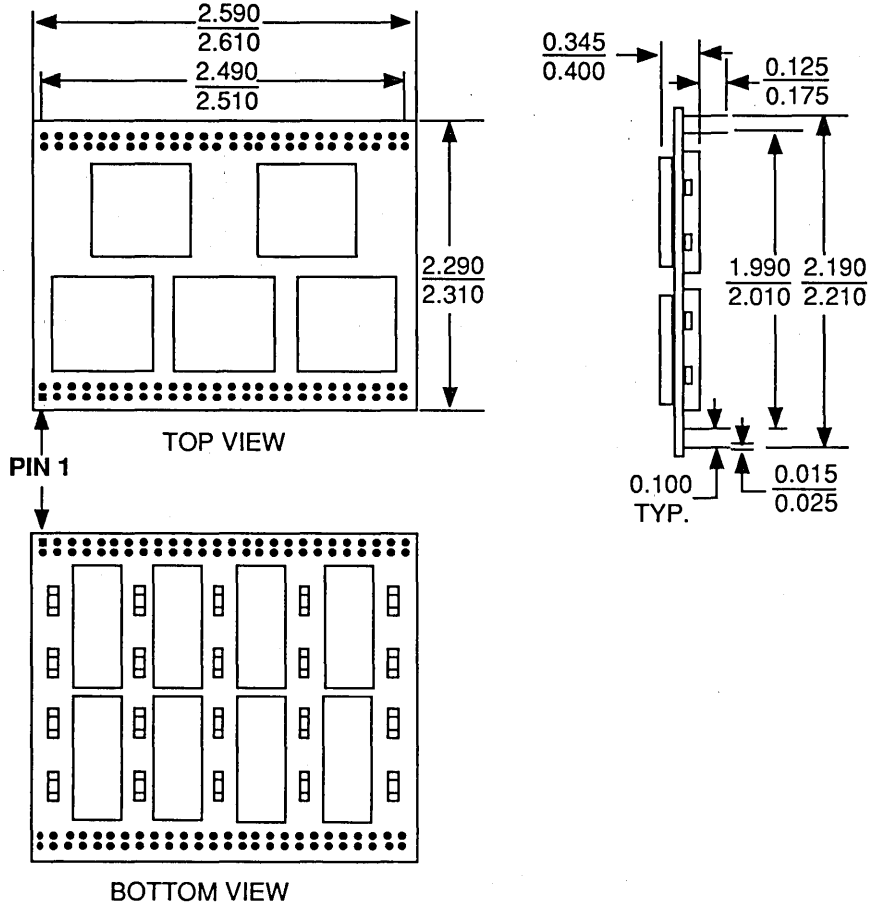
QUAD IN-LINE PACKAGES (Continued)

92-Pin FR-4 QIP – M22



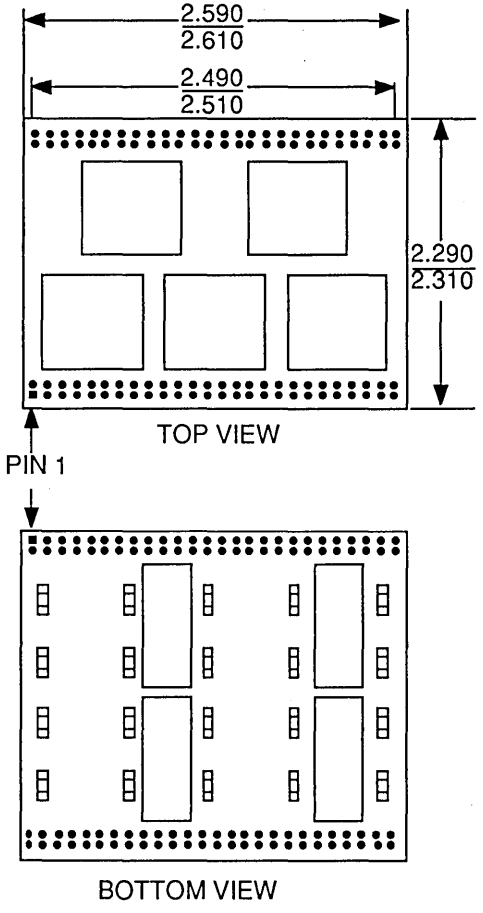
QUAD IN-LINE PACKAGES (Continued)

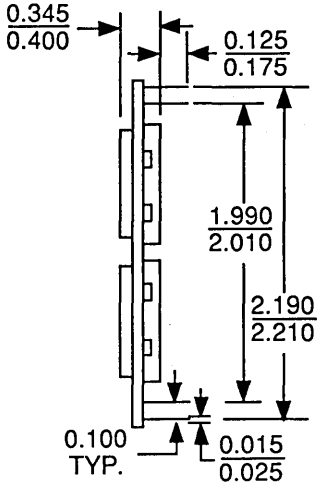
104-Pin FR-4 QIP – M23



QUAD IN-LINE PACKAGES (Continued)

104-Pin FR-4 QIP – M24

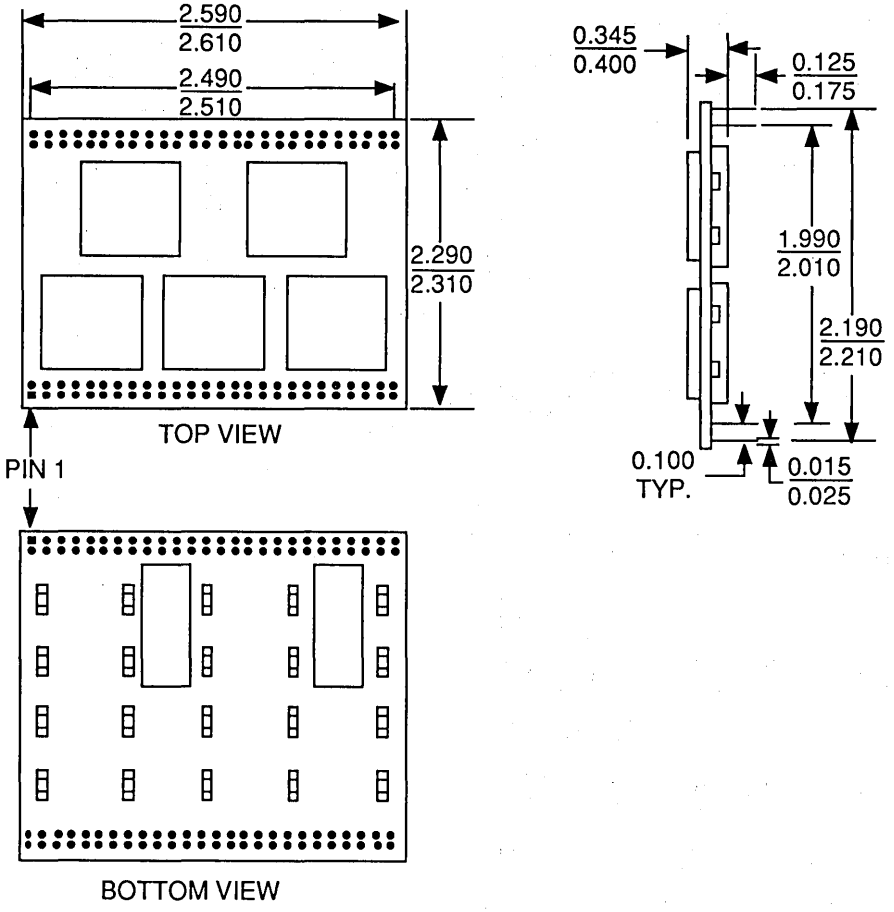




4

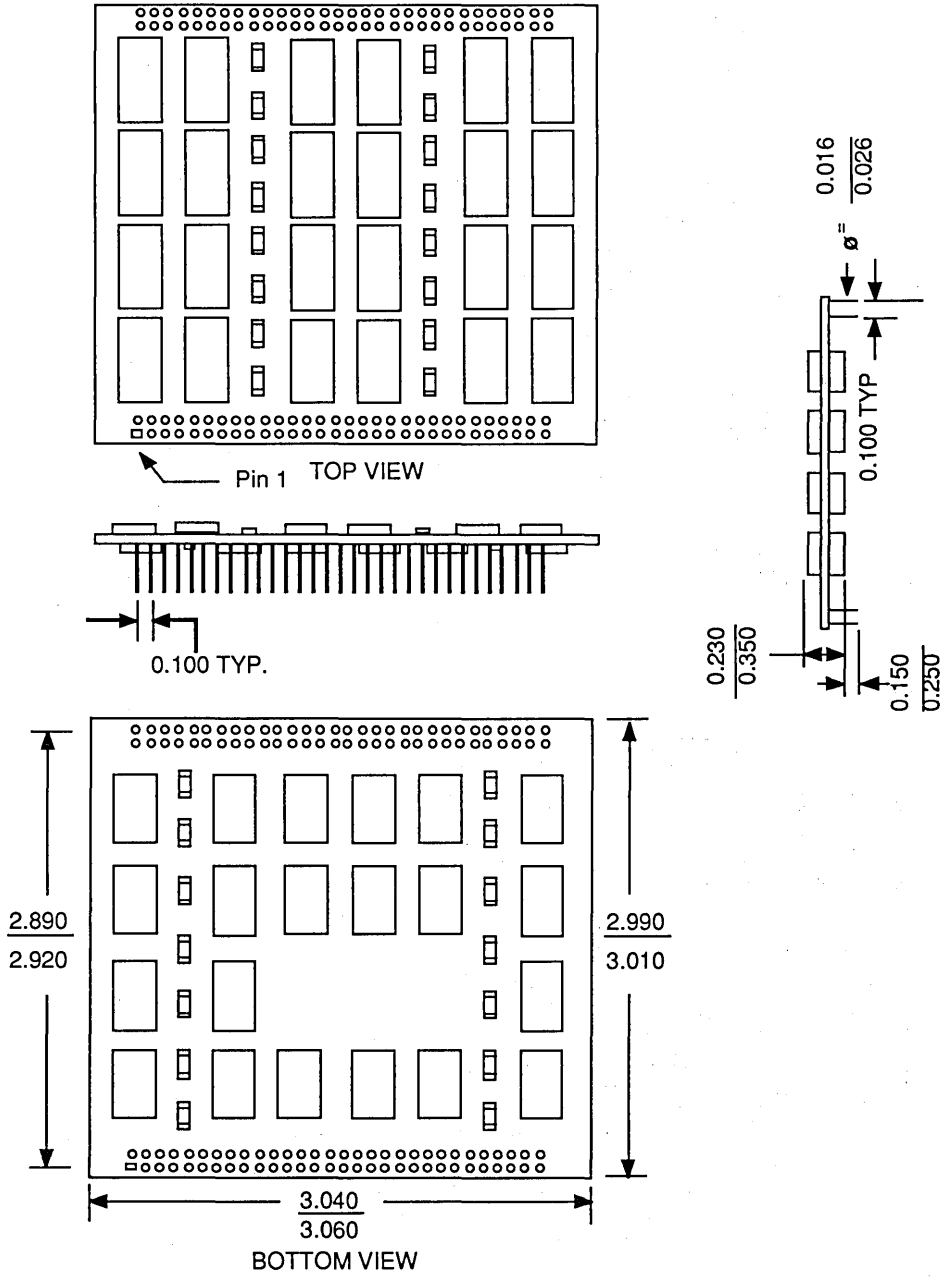
QUAD IN-LINE PACKAGES (Continued)

104-Pin FR-4 QIP – M25



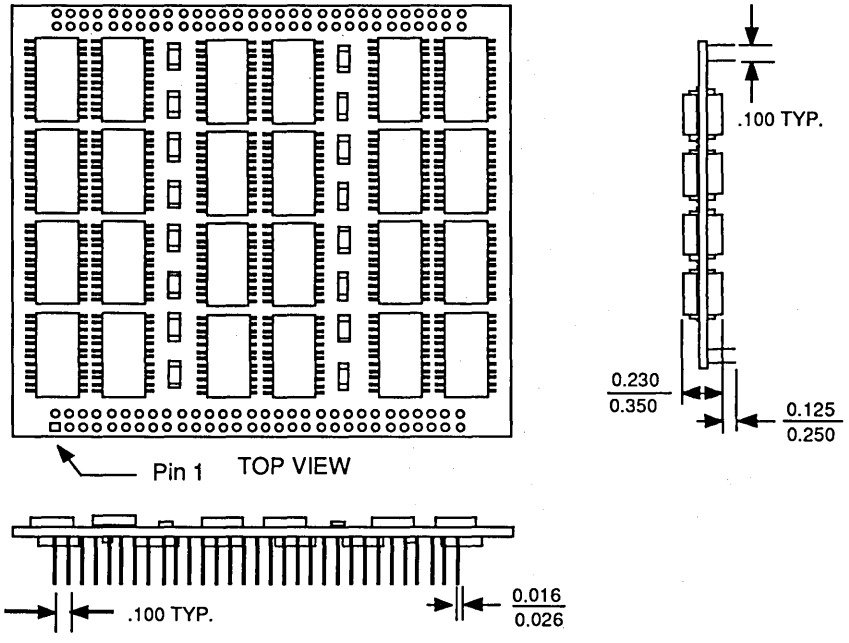
QUAD IN-LINE PACKAGES (Continued)

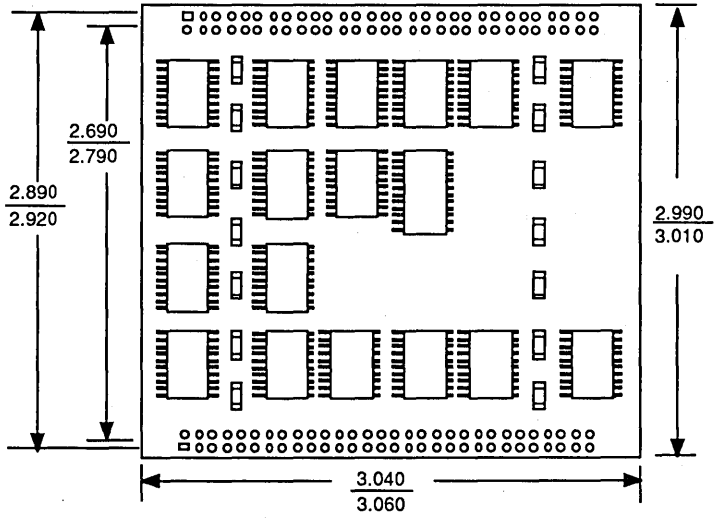
120-Pin FR-4 QIP – M26



QUAD IN-LINE PACKAGES (Continued)

120-Pin FR-4 QIP – M27

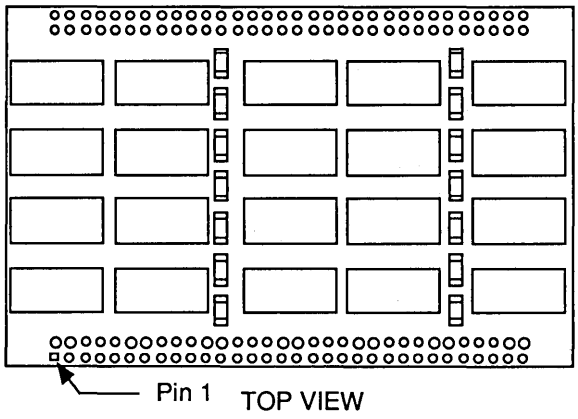


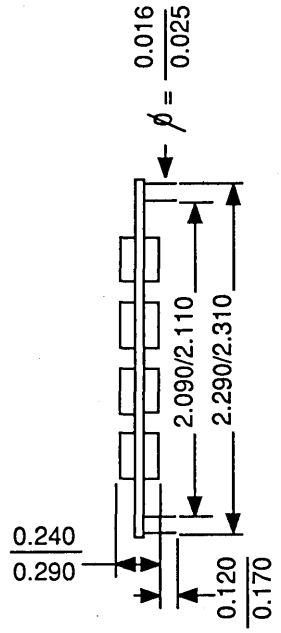


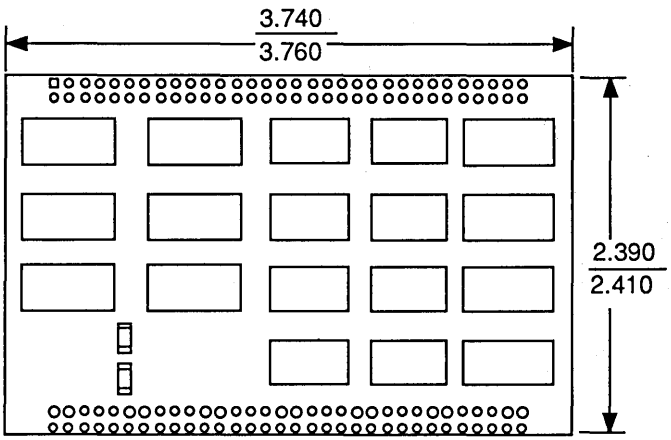
BOTTOM VIEW

QUAD IN-LINE PACKAGES (Continued)

128-Pin FR-4 QIP – M28



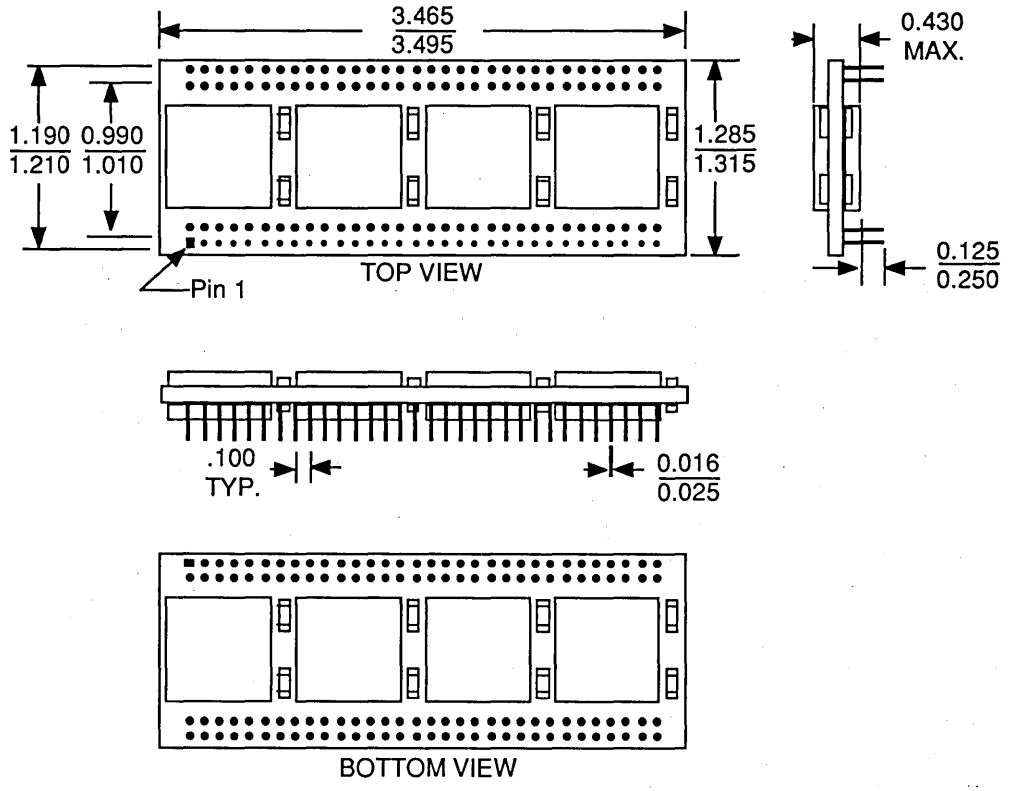




BOTTOM VIEW

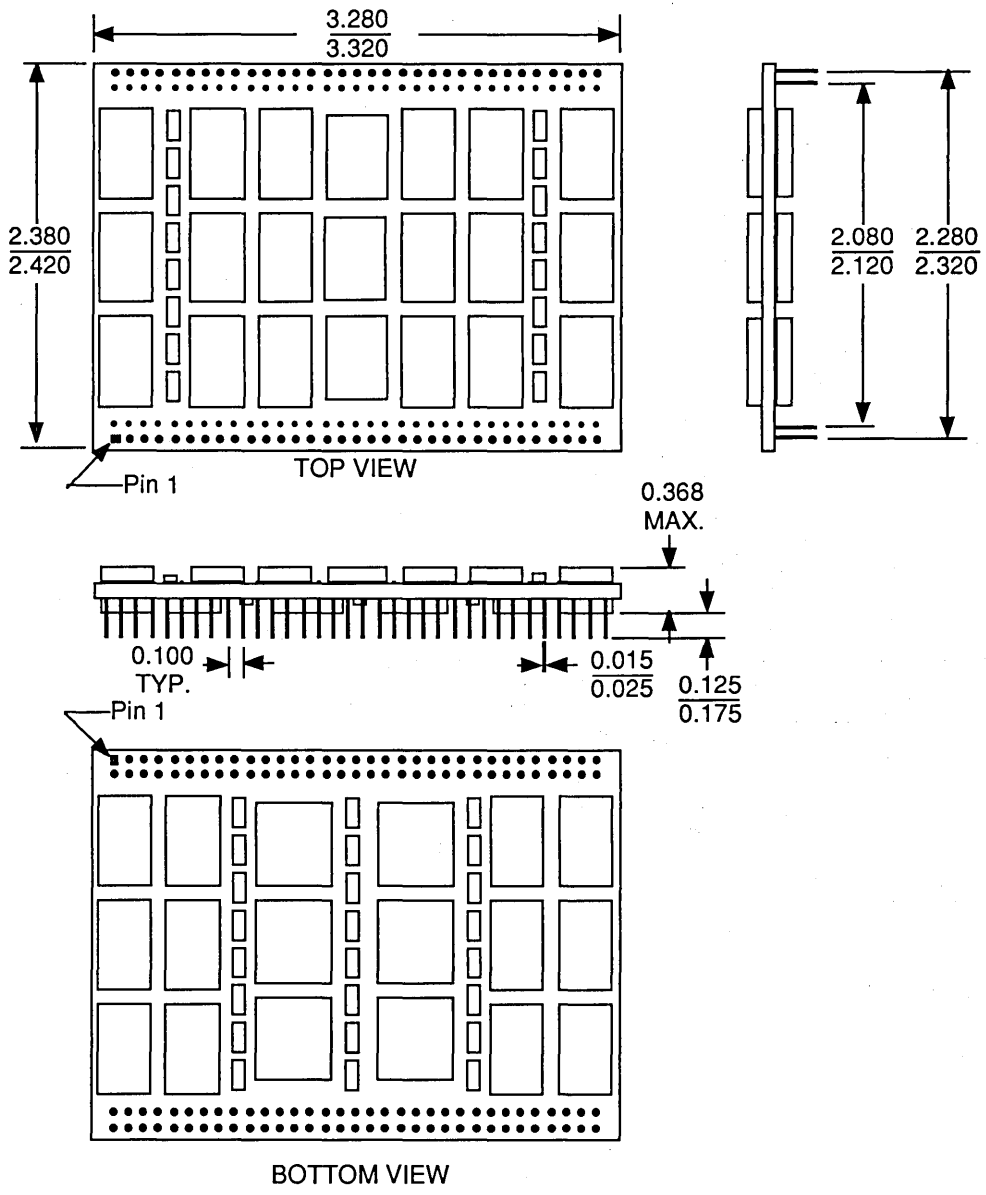
QUAD IN-LINE PACKAGES (Continued)

128-Pin FR-4 QIP – M29



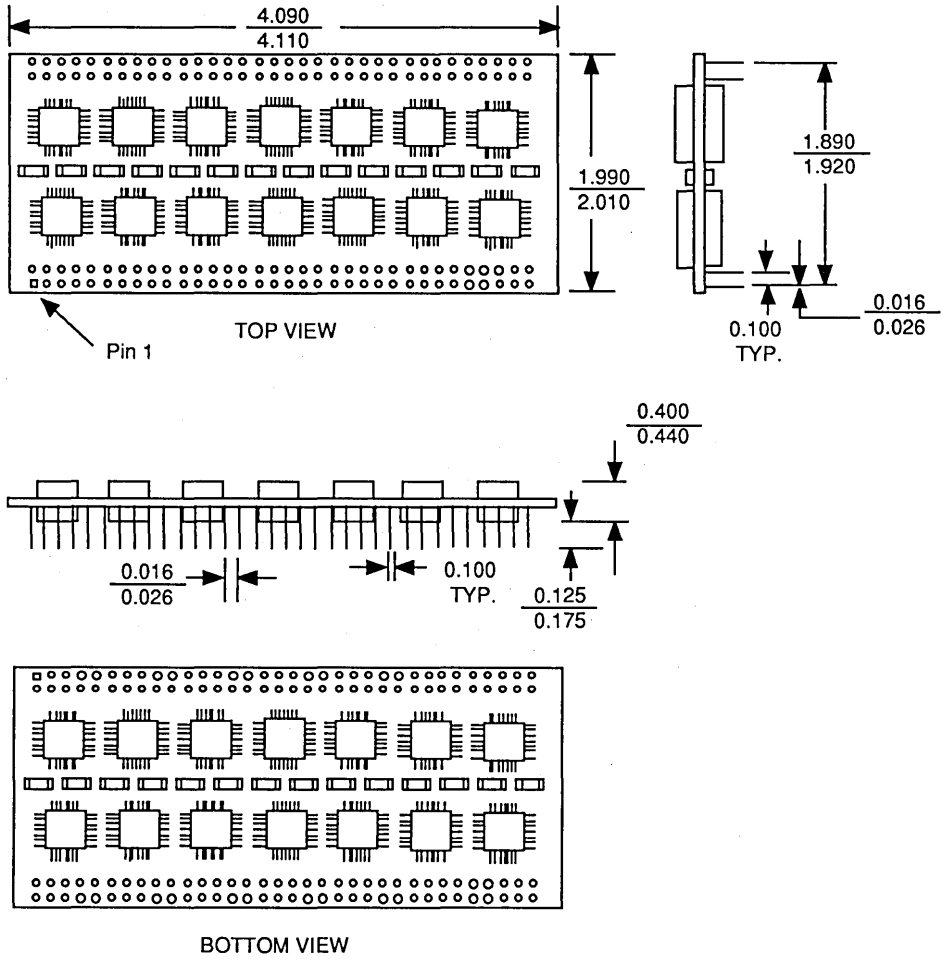
QUAD IN-LINE PACKAGES (Continued)

132-Pin FR-4 QIP – M30



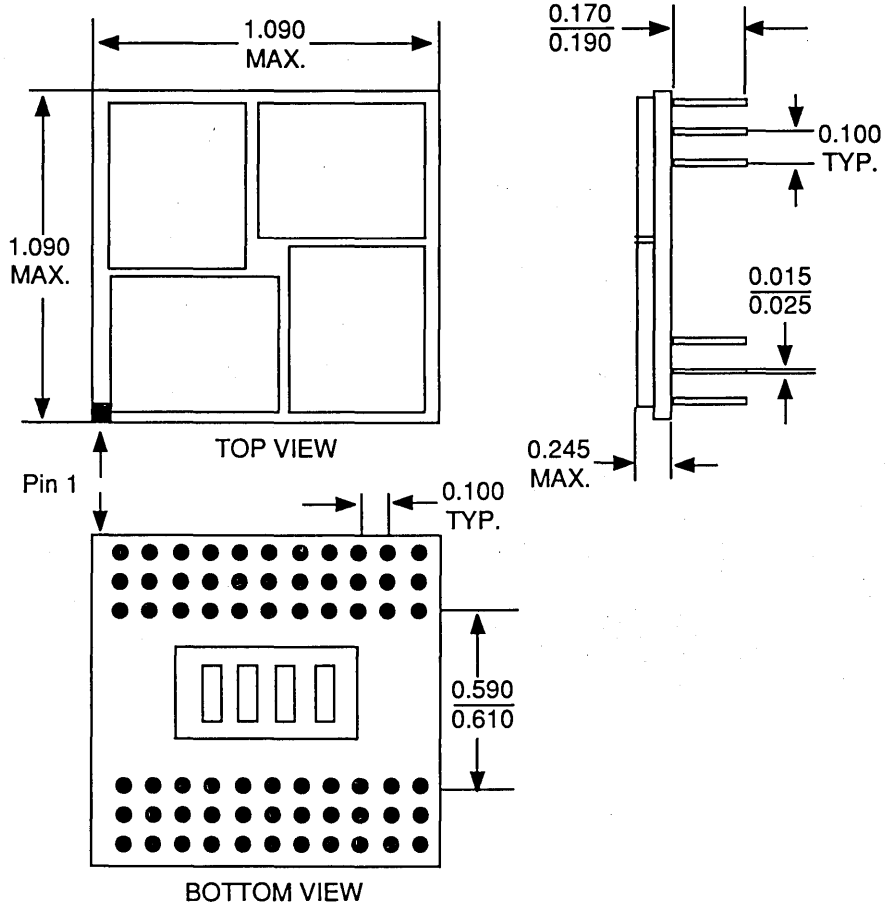
QUAD IN-LINE PACKAGES (Continued)

164-Pin FR-4 QIP – M31



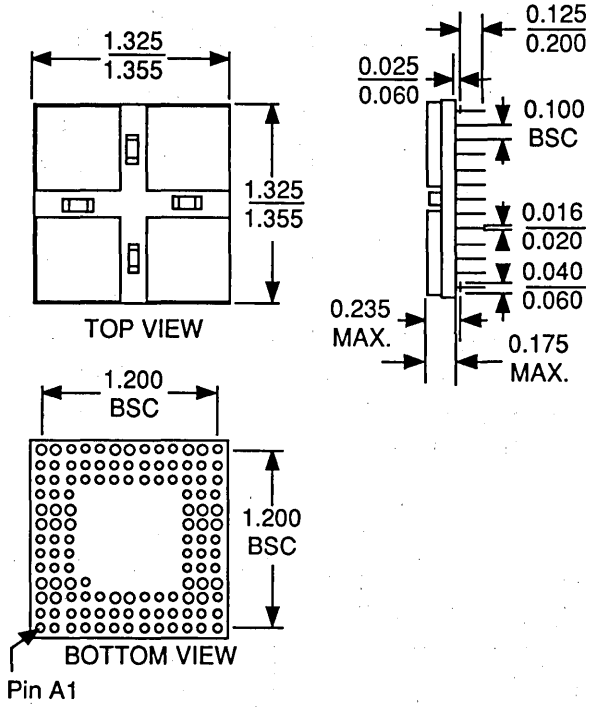
HEX IN-LINE PACKAGES

66-Pin Ceramic Sidebraze HIP – M32



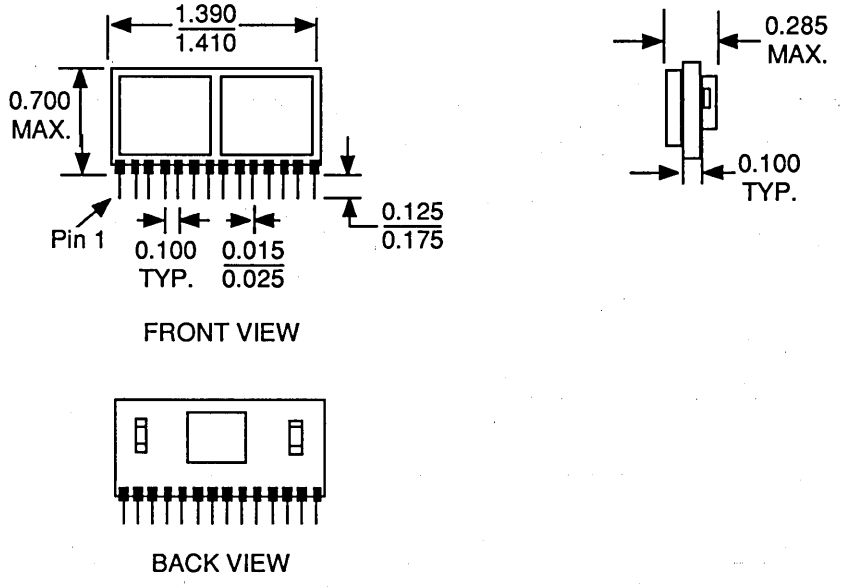
PIN GRID ARRAY PACKAGES

121-Pin Ceramic Sidebraze PGA – M33



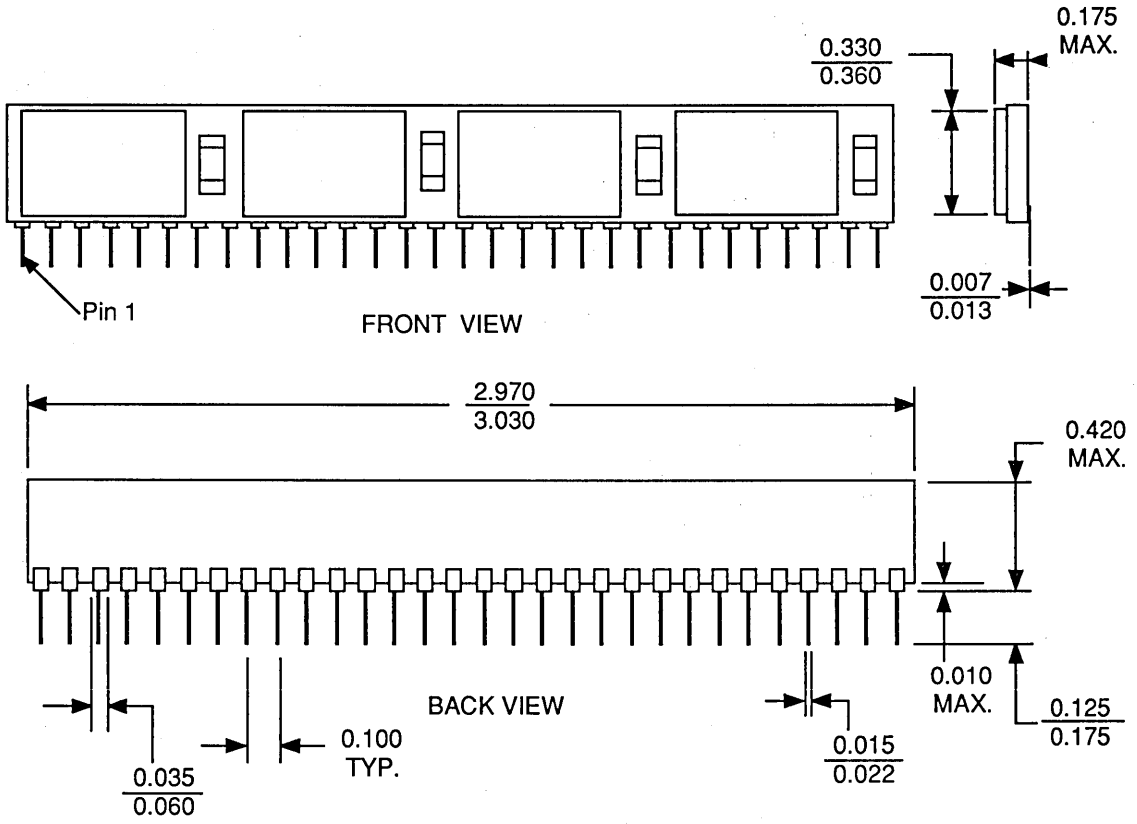
SINGLE IN-LINE PACKAGES

28-Pin FR-4 SIP – M34



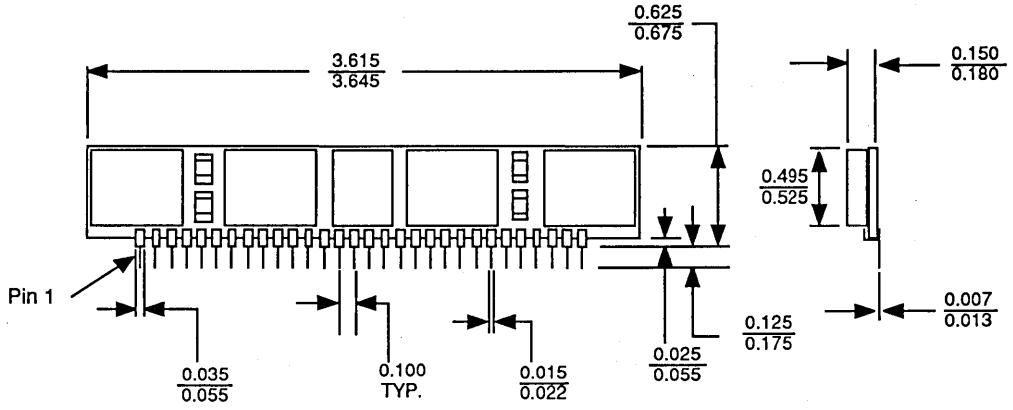
SINGLE IN-LINE PACKAGES (Continued)

30-Pin Ceramic Sidebraze SIP – M35

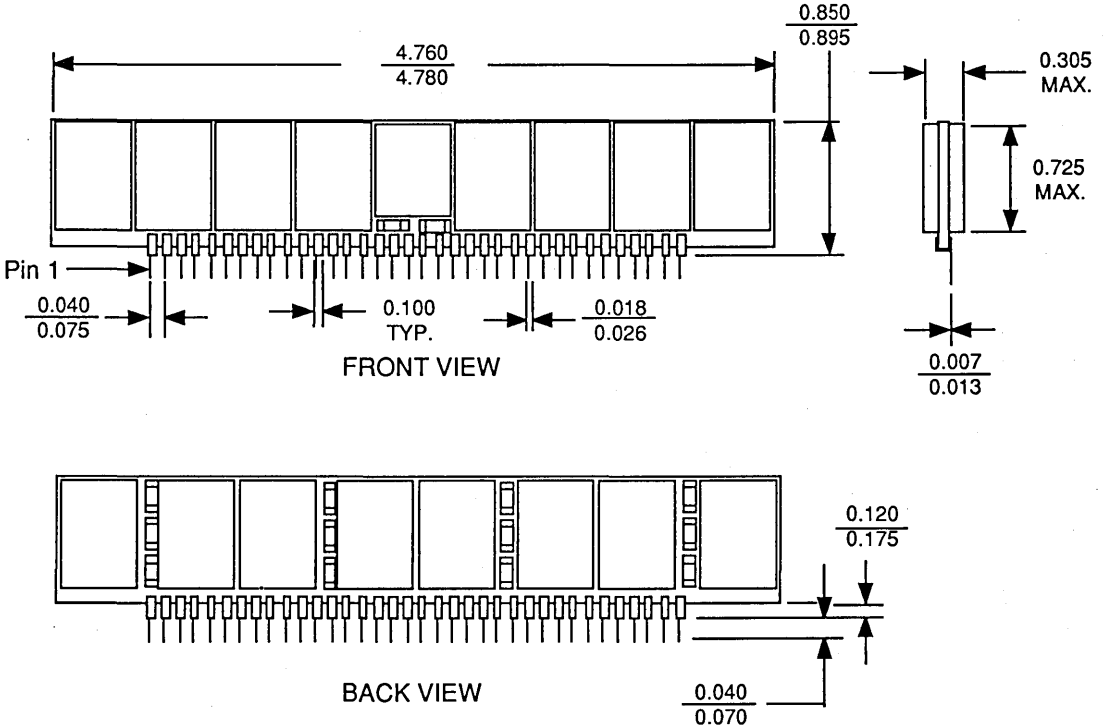


SINGLE IN-LINE PACKAGES (Continued)

30-Pin FR-4 SIP – M36



36-Pin FR-4 SIP – M37

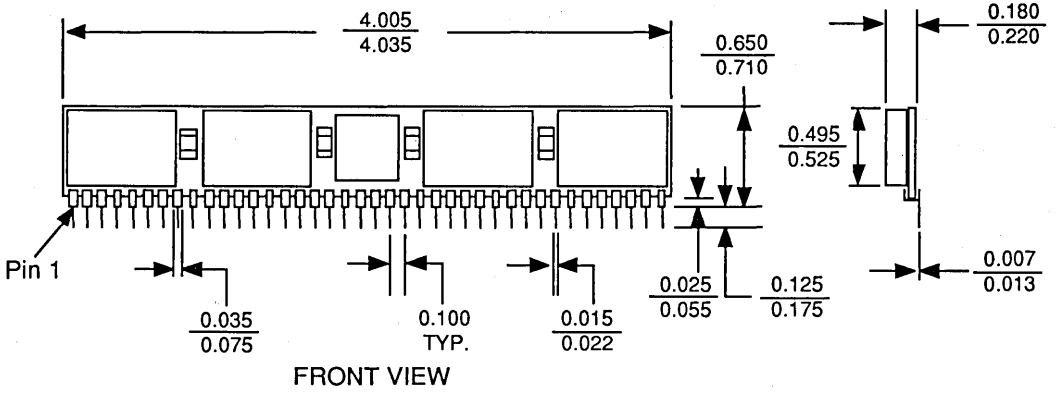


SINGLE IN-LINE PACKAGES (Continued)

36-Pin FR-4 SIP – M38

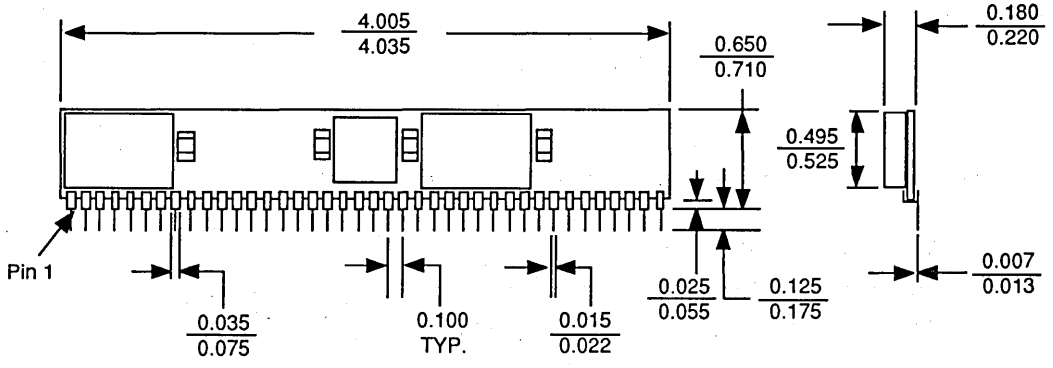
MODULE DIMENSIONS FOR PACKAGE M38 ARE NOT YET AVAILABLE. PLEASE CONSULT THE FACTORY FOR FURTHER DETAILS.

40-Pin FR-4 SIP – M39



FRONT VIEW

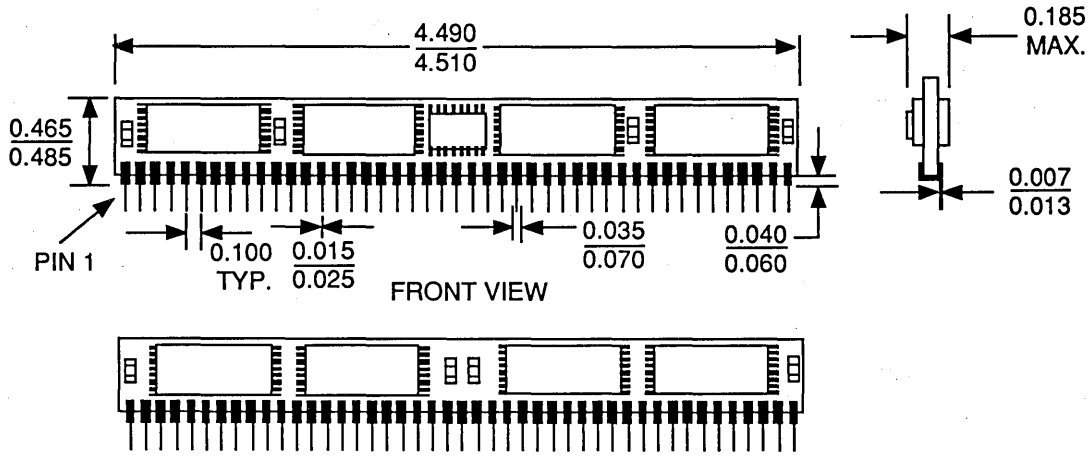
40-Pin FR-4 SIP – M40



TOP VIEW

SINGLE IN-LINE PACKAGES (Continued)

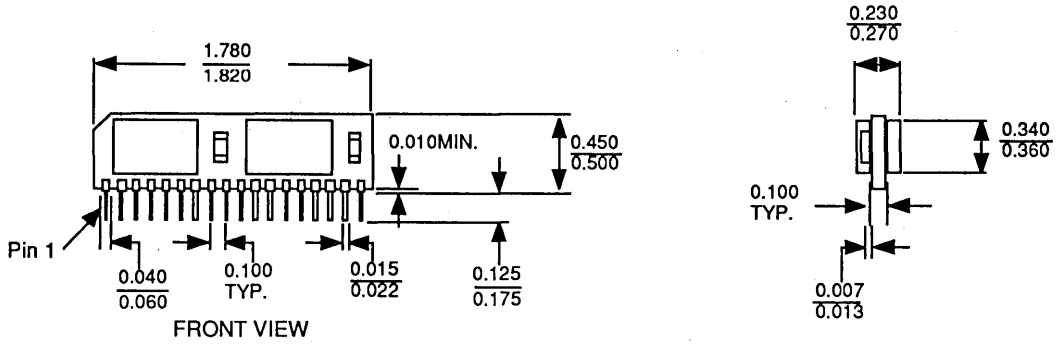
45-Pin FR-4 SIP – M41



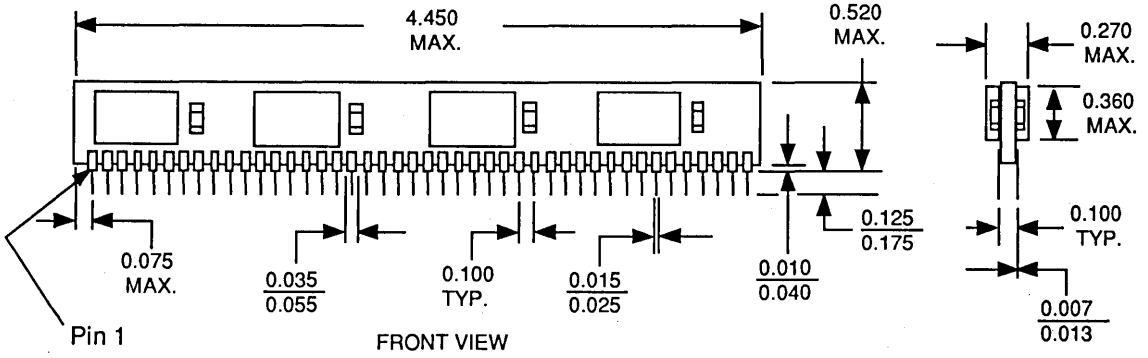
BACK VIEW

DUAL SINGLE IN-LINE PACKAGES

36-Pin Ceramic Sidebraze DSIP – M42

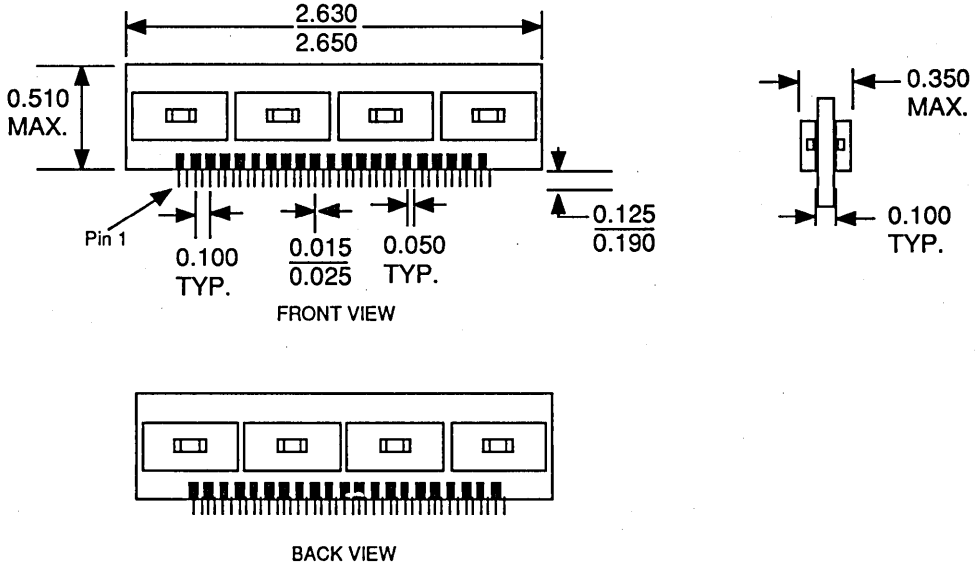


88-Pin Ceramic Sidebraze DSIP – M43

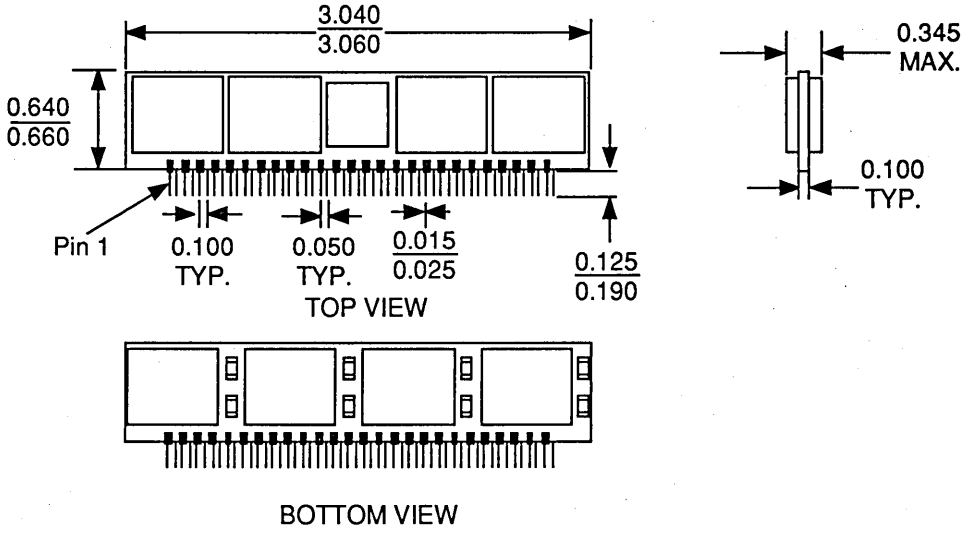


ZIG-ZAG IN-LINE PACKAGES

42-Pin FR-4 ZIP – M44

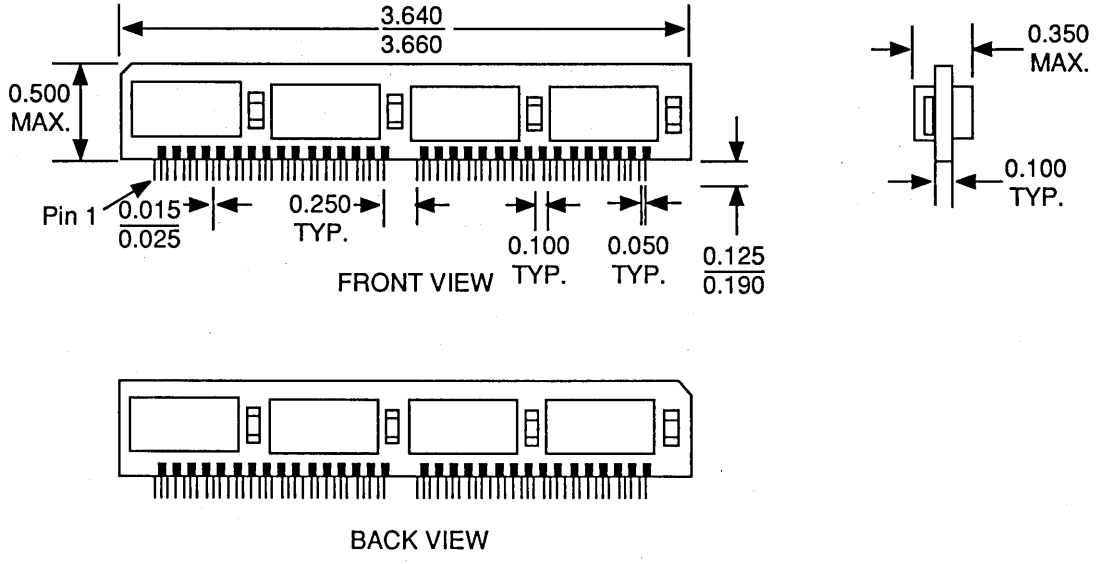


52-Pin FR-4 ZIP – M45

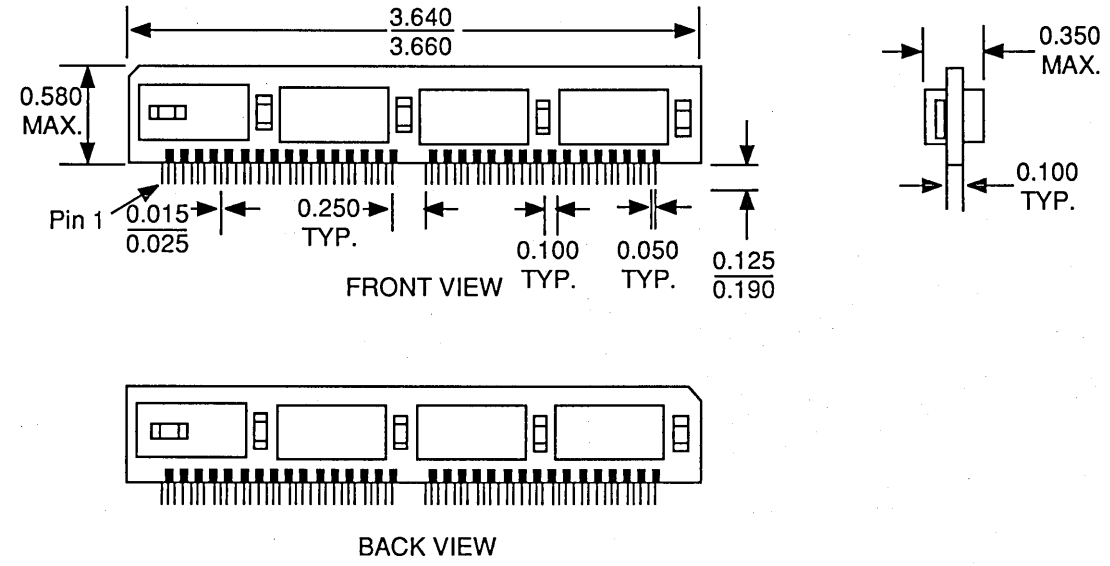


ZIG-ZAG IN-LINE PACKAGES (Continued)

64-Pin FR-4 ZIP – M46



64-Pin FR-4 ZIP – M47

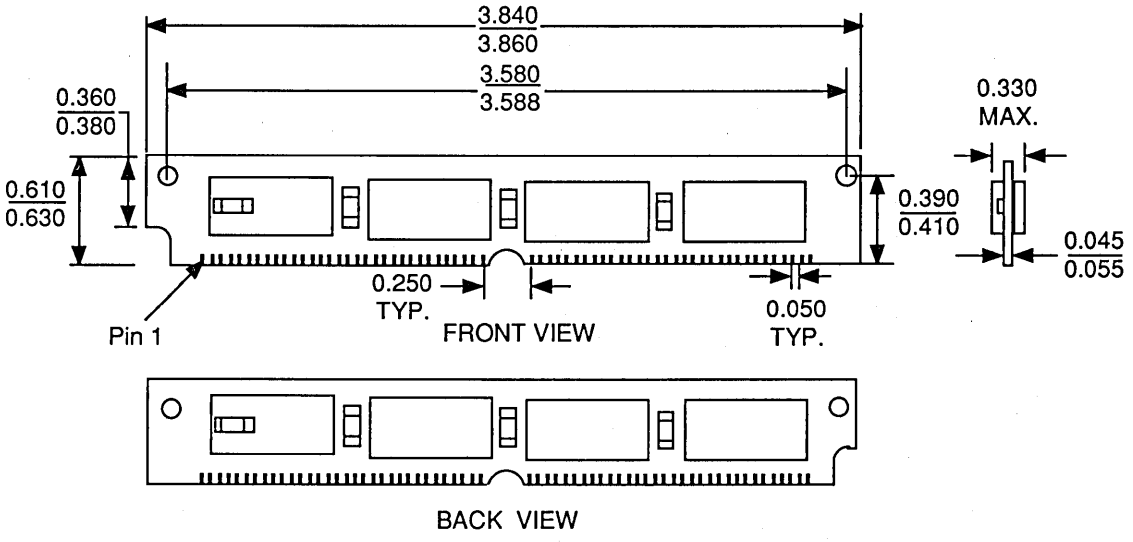


SINGLE IN-LINE PACKAGES (Continued)

40-Pin FR-4 SIMM – M48

**MODULE DIMENSIONS FOR PACKAGE M48 ARE NOT YET AVAILABLE.
PLEASE CONSULT THE FACTORY FOR FURTHER DETAILS.**

40-Pin FR-4 SIMM – M49



ECL PRODUCTS

The ECL Product Group is one of the newest product groups to be created at Integrated Device Technology, Inc. The charter of the group is to develop a leadership BiCMOS technology, create ECL-compatible products which drive and showcase that technology, and understand the needs of ECL users with the aim of creating products which more completely provide systems solutions.

The products offered by the ECL Products Group provide the designer of high-speed emitter-coupled logic (ECL) systems with a lower-power alternative to older bipolar ECL technologies. IDT BiCMOS ECL memory products allow the designer to achieve performance levels close to bipolar equivalents, yet with less engineering time and resources devoted to heat dissipation and thermal design. These products are ideal for cache, control-store, or main memory applications in mini-supercomputer and high-end workstation, or pattern generation and data capture in test equipment.

This revolution in performance-density is achieved by IDT through the development of a technology which combines high-speed CMOS with limited use of bipolar structures. Called BiCEMOS™, the technology provides greater performance in memory components by speeding up word-line drivers, sense amplifiers, and input-output buffers. Bipolar structures on-chip also allow the option of ECL-compatible interfaces.

To build components with ECL interfaces in the past required 100% bipolar circuit designs. Full bipolar designs were limited in density, however, by the high power dissipation of the chip: the level of integration available to the designer of ECL systems has thus been necessarily low when compared to CMOS. But in the past, designers looking for performance sacrificed density and solved power dissipation engineering problems in order to use bipolar ECL components. Today, BiCMOS provides the high-density and low cost of CMOS to ECL designers.

Integrated Device Technology has begun its family of BiCMOS ECL components with the most density-intensive elements: memory. Because memories benefit in speed from bipolar word-line drivers as mentioned above, larger (longer word-line) memories benefit most from BiCMOS. Thus, IDT has begun building BiCMOS ECL SRAMs at the 64K-bit density, and will offer products with ever greater levels of integration. These density enhancements will include 256K-bit memories and beyond, as well as memories including on-chip logic to improve their use in computer architectures.

The speed of memories, measured as access time, is also improved with the development of BiCMOS. Bipolar structures speed up internal elements of already fast CMOS memories. Because it is based on, and integrated into, standard IDT CMOS, BiCMOS will directly receive the benefits of enhancements made in future CMOS technology generations. Speed improvements will be achieved for both BiCMOS TTL and BiCMOS ECL memories, but the ECL output buffer is a clear speed leader over TTL, implying that ECL memories will in general out-perform TTL. In a system, ECL logic elements out-perform TTL by as much as a factor of three; IDT feels that ECL will win renewed interest as an interconnect standard for high-performance systems now that BiCMOS allows CMOS densities at ECL speeds.

Military applications will also benefit from BiCMOS ECL components. The low-power dissipation of BiCMOS allows ECL SRAMs to be offered as fully MIL-STD-883 compliant over the full -55°C to +125°C temperature range. The high density and low power will be ideal for high data rate applications such as RADAR, satellite communication, and graphics.

The lower power dissipation of BiCMOS ECL components makes the job of designing with ECL much easier than with bipolar ECL. System reliability goals are much easier to achieve because these components create less heat in a system. Heat dissipation techniques needed for system cooling benefit from a better starting point, reducing the amount of time and resources needed to prove a design. Power supply requirements are of course reduced. New packaging options are realized, such as plastic DIP and surface-mount packages.

Integrated Device Technology believes that BiCMOS will be a major technology for the coming years, and is dedicated to be the leader. To do this we have created memory products to drive the technology down the learning curve to provide our customers cost-effective high-performance. We offer standard and leadership ECL products implemented in high-performance BiCMOS. We intend to work closely with our customers to create new standard products which bring more of the advantages of BiCMOS speed, integration, and lower power to ECL systems.

TABLE OF CONTENTS

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 16K (4K x 4-BIT) SRAM

PRELIMINARY
IDT10484
IDT100484
IDT101484

FEATURES:

- 4096-words x 4-bit organization
- Address access time: 7/8/10/15 ns
- Low power dissipation: 700mW (typ.)
- Guaranteed Output Hold time
- Fully compatible with ECL logic levels
- Separate data input and output
- Traditional corner-power pin pinout
- Standard through-hole and surface mount packages

DESCRIPTION:

The IDT10484, IDT100484 and IDT101484 are 16,384-bit high-speed BiCEMOS™ ECL static random access memories organized as 4K x 4, with separate data inputs and outputs. All I/Os are fully compatible with ECL levels.

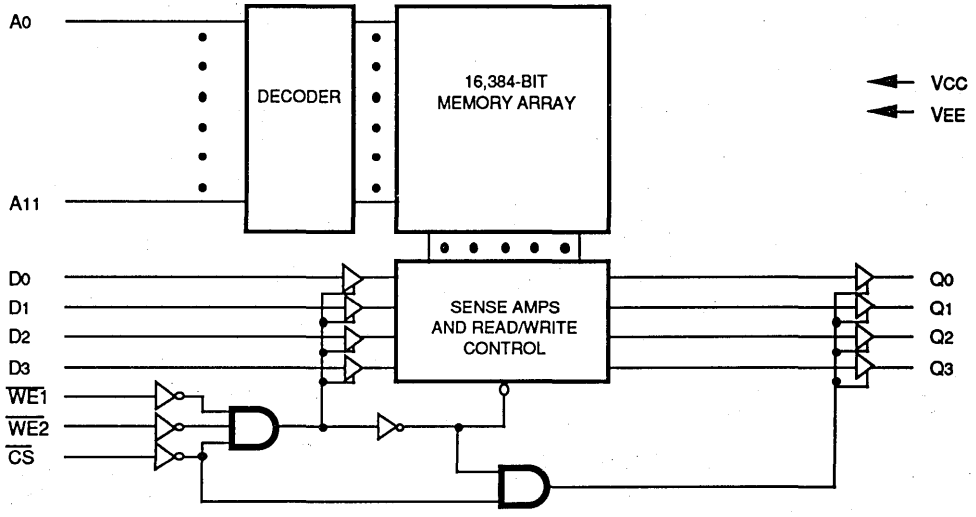
These devices are part of a family of asynchronous four-bit-wide ECL SRAMs. This device have been configured to follow the traditional corner-voltage pinout. Because they are manufactured in BiCEMOS™ technology, however, power dissipation is greatly reduced over equivalent bipolar devices.

The asynchronous SRAMs are the most straightforward to use because no additional clocks or controls are required: $Data_{OUT}$ is available an access time after the last change of address. To write data into the device requires the creation of a Write Pulse, and the write cycle disables the output pins in conventional fashion. Two Write Enable inputs are supplied, so the write pulse is created as a logical-AND of these signals to allow write gating at the device for minimal skew.

The fast access time and guaranteed Output Hold time allow greater margin for system timing variation. $Data_{IN}$ setup time specified with respect to the trailing edge of Write Pulse eases write timing allowing balanced Read and Write cycle times.

5

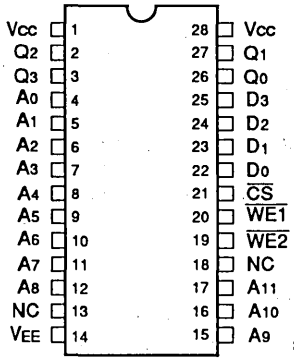
FUNCTIONAL BLOCK DIAGRAM



2756 drw 01

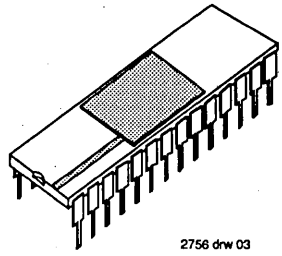
BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



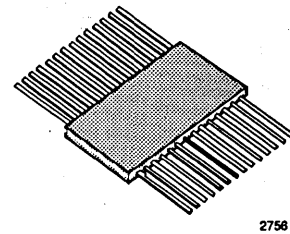
2756 drw 02

TOP VIEW



2756 drw 03

400-Mil-Wide
CERAMIC PACKAGE
C28



2756 drw 04

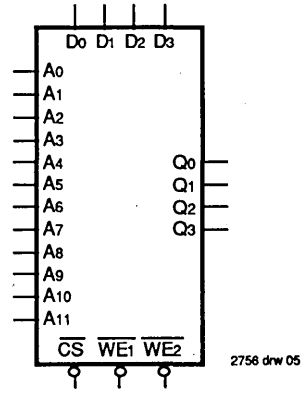
400-Mil-Wide
CERPACK
E28

PIN DESIGNATION

Symbol	Pin Name
A0 through A11	Address Inputs
D0 through D3	Data Inputs
Q0 through Q3	Data Outputs
$\overline{WE1}$, $\overline{WE2}$	Write Enable Input
$\overline{CS}$	Chip Select Input (Internal pull down)
VEE	More Negative Supply Voltage
Vcc	Less Negative Supply Voltage

2756 tbl 01

LOGIC SYMBOL



2756 drw 05

4K x 4
SRAM

AC OPERATING RANGES(1)

I/O	VEE	Temperature
10K	-5.2V ±5%	0 TO 75°C, air flow exceeding 2 m/sec
100K	-4.5V ±5%	0 TO 85°C, air flow exceeding 2 m/sec
101K	-4.75V to -5.46V	0 TO 75°C, air flow exceeding 2 m/sec

2756 tbl 02

NOTE:
1. Referenced to Vcc

CAPACITANCE (TA=+25°C, f=1.0MHz)

Symbol	Parameter	DIP Typ.	DIP Max.	Flatpack Typ.	Flatpack Max.	Unit
CIN	Input Capacitance	4	–	TBD	–	pF
COUT	Output Capacitance	6	–	TBD	–	pF

2756 tbl 03

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE1}$	$\overline{WE2}$	DataOUT	Function
H	X	X	L	Deselected
L	H	X	RAM Data	Read
L	X	H	RAM Data	Read
L	L	L	WRITE Data	Write

2756 tbl 04

NOTE:
1. H=High, L=Low, X=Don't Care

ECL-10K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2756 tbl 05

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-10K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, RL=50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit	T_A
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA	–
			Others	–	–	110	µA	–
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA	–
			Others	-50	–	90	µA	–
I_{EE}	Supply Current	All Inputs and Outputs Open		-190	-130	–	mA	–

2756 tbl 06

NOTE:

1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

ECL-100K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +85	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Output Current (Output High)		-50	mA

NOTE: 2756 tbl 07

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-100K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L=50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Condition		Min. (B)	Typ.(1)	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-170	-110	–	mA

NOTES: 2756 tbl 08

1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

ECL-101K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Output Current (Output High)		-50	mA

NOTE: 2756 tbl 09

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-101K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.5V, RL=50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

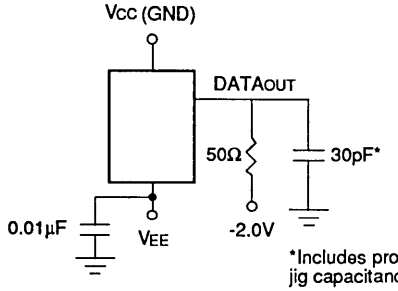
Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-190	-130	–	mA

NOTE: 2756 tbl 10

1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.

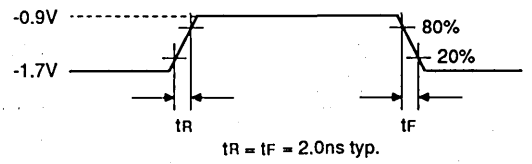
5

AC TEST LOAD CONDITION



2756 drw 06

AC TEST INPUT PULSE



Note: All timing measurements are referenced to 50% input levels.

2756 drw 07

RISE/FALL TIME

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
tR	Output Rise Time	–	–	2	–	ns
tF	Output Fall Time	–	–	2	–	ns

2756 tbl 11

FUNCTIONAL DESCRIPTION

The IDT10484, IDT100484 and IDT101484 BiCMOS ECL static RAMs (SRAM) provide high speed with low power dissipation typical of BiCMOS ECL. These devices follow the traditional corner-power pinout and functionality for 4Kx4 ECL SRAMs. (For center-power pinouts, please see the IDT10A484, IDT100A494, and IDT101A484, respectively.)The ECL-101K meets electrical specifications that combine the ECL-100K temperature and voltage compensated output levels with the high-speed of ECL-10K VEE compatibility (-5.2V).

READ TIMING

The read timing on these asynchronous devices is straightforward. DataOUT is held low until the device is selected by Chip Select ($\overline{CS}$). Then Address (ADDR) settles and data appears on the output after time tAA. Note that DataOUT is held for a short time (tOH) after the address begins to change for the next access, then ambiguous data is on the bus until a new time tAA.

WRITE TIMING

To write data to the device, a Write Pulse need be formed to control the write to the SRAM array. This Write Pulse, called $\overline{WE}$, is formed inside the device as the logical-AND of the $\overline{WE1}$ and $\overline{WE2}$ inputs; that is, when $\overline{WE1}$ and $\overline{WE2}$ both are driven low, $\overline{WE}$ goes low and the write cycle begins.

While $\overline{CS}$ and ADDR must be set-up when $\overline{WE}$ goes low, DataIN can settle after the falling edge of $\overline{WE}$, giving the data path extra margin. Data is written to the memory cell at the end of the Write Pulse, and addresses and Chip Select must be held after the rising edge of the Write Pulse to ensure satisfactory completion of the cycle.

DataOUT is disabled (held low) during the Write Cycle. If $\overline{CS}$ is held low (active) and addresses remain unchanged, the DataOUT pins will output the written data after "Write Recovery Time" (tWR).

Because of the very short Write Pulse requirement, these devices can be cycled as quickly for Writes as for Reads. Balanced cycles mean simpler timing in cache applications.

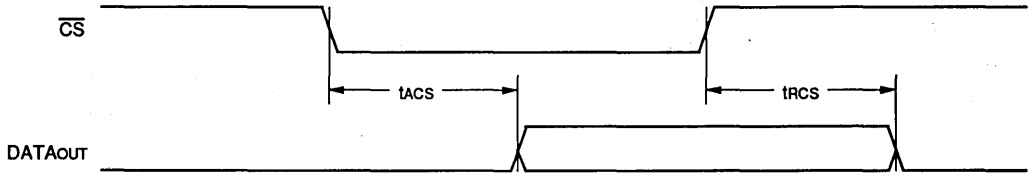
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10484S7 100484S7 101484S7		10484S8 100484S8 101484S8		10484S10 100484S10 101484S10		10484S15 100484S15 101484S15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle											
tACS	Chip Select Access Time	–	–	3	–	5	–	5	–	5	ns
tRCS	Chip Select Recovery Time	–	–	3	–	5	–	5	–	5	ns
tAA	Address Access Time	–	–	7	–	8	–	10	–	15	ns
tOH	Data Hold from Address Change	–	3	–	3	–	3	–	3	–	ns

NOTES:
1. Input and Output reference level is 50% point of waveform.

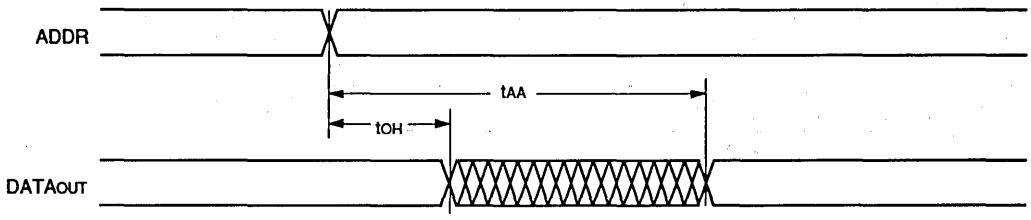
2756 tbl 12

READ CYCLE GATED BY CHIP SELECT



2756 drw 08

READ CYCLE GATED BY ADDRESS



2756 drw 09

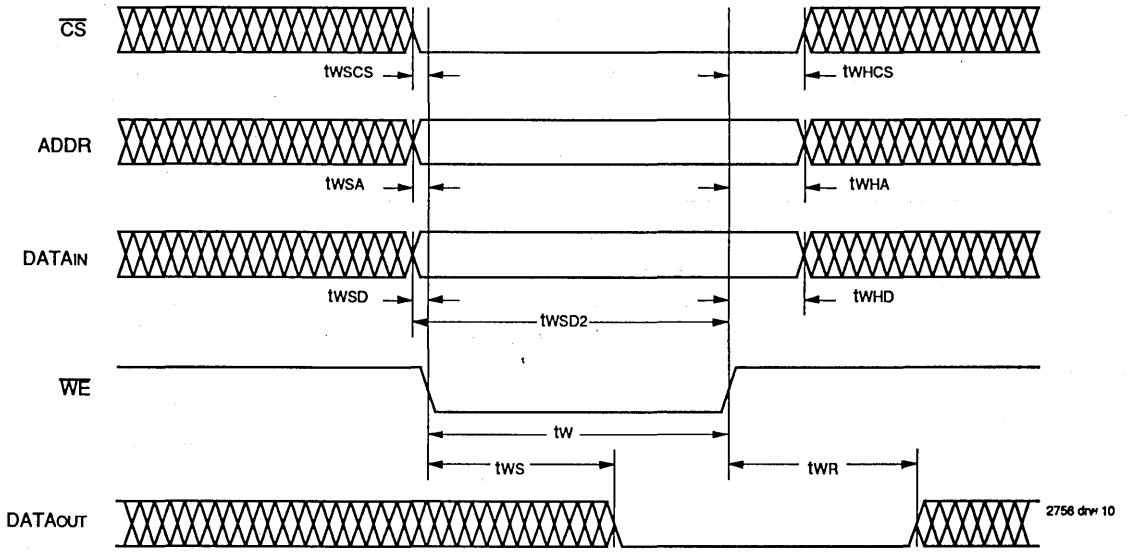
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10484S7 100484S7 101484S7		10484S8 100484S8 101484S8		10484S10 100484S10 101484S10		10484S15 100484S15 101484S15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle											
tW	Write Pulse Width	tWSA = minimum	5	–	6	–	8	–	10	–	ns
tWSD	Data Set-up Time	–	0	–	0	–	0	–	2	–	ns
tWSD2[2]	Data Set-up Time to $\overline{WE}$ High	–	5	–	5	–	5	–	5	–	ns
tWSA	Address Set-up Time	tWSA = minimum	0	–	0	–	0	–	2	–	ns
tWSCS	Chip Select Set-up Time	–	0	–	0	–	0	–	2	–	ns
tWHD	Data Hold Time	–	1	–	1	–	1	–	2	–	ns
tWHA	Address Hold Time	–	1	–	1	–	1	–	2	–	ns
tWHCS	Chip Select Hold Time	–	1	–	1	–	1	–	2	–	ns
tWS	Write Disable Time	–	–	5	–	5	–	5	–	5	ns
tWR[3]	Write Recovery Time	–	–	5	–	5	–	5	–	5	ns

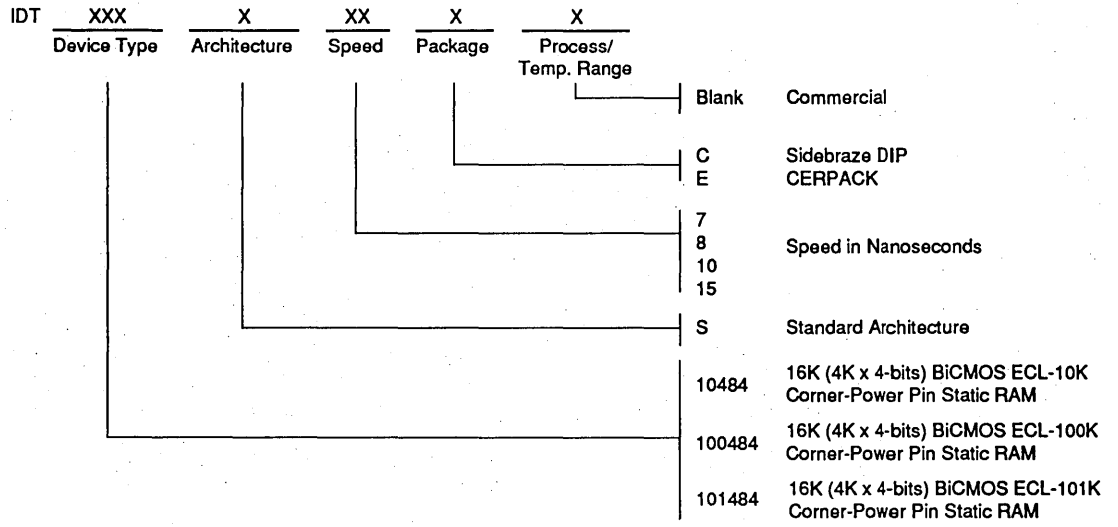
2756 tbl 13

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. tWSD is specified with respect to the falling edge of $\overline{WE}$ for compatibility with bipolar part specifications, but this device actually only requires tWSD2 with respect to rising edge of $\overline{WE}$.
3. tWR is defined as the time to reflect the newly written data on the Data Outputs (Q_0 to Q_3) when no new Address Transition occurs.

WRITE CYCLE TIMING DIAGRAM



ORDERING INFORMATION



2756 drw 11

5

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 16K (4K x 4-BIT) SRAM

PRELIMINARY
IDT10A484
IDT100A484
IDT101A484

FEATURES:

- 4096-words x 4-bit organization
- Address access time: 5/7/8/10 ns
- Low power dissipation: 700mW (typ.)
- Guaranteed Output Hold time
- Fully compatible with ECL logic levels
- Separate data input and output
- Center-power pinout for reduced noise
- Standard through-hole and surface mount packages

DESCRIPTION:

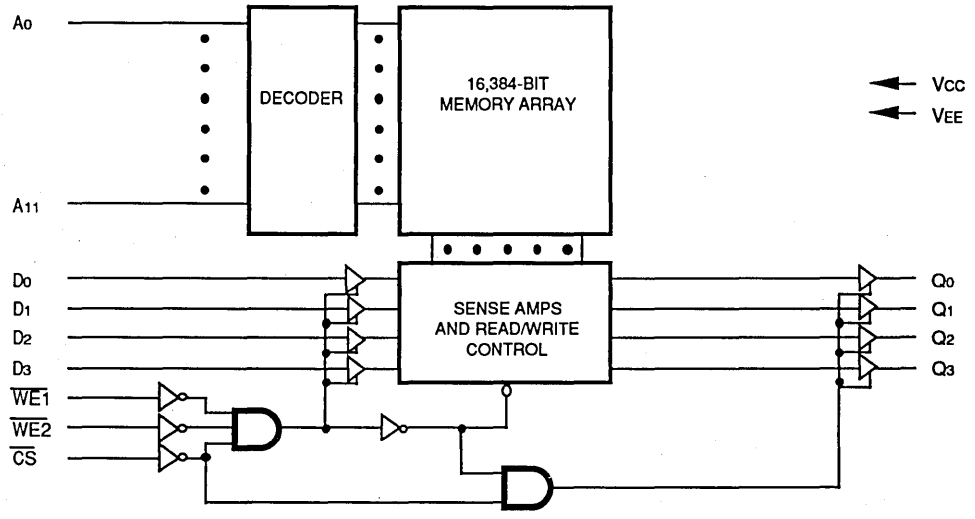
The IDT10A484, IDT100A484 and IDT101A484 are 16,384-bit high-speed BiCEMOS™ ECL static random access memories organized as 4Kx4, with separate data inputs and outputs. All I/Os are fully compatible with ECL levels.

These devices are part of a family of asynchronous four-bit-wide ECL SRAMs. This device have been configured to follow the center-power pinout for reduced noise allowing higher speed operation. Because they are manufactured in BiCEMOS™ technology, power dissipation is greatly reduced over equivalent bipolar devices.

The asynchronous SRAMs are the most straightforward to use because no additional clocks or controls are required: $Data_{OUT}$ is available an access time after the last change of address. To write data into the device requires the creation of a Write Pulse, and the write cycle disables the output pins in conventional fashion. Two Write Enable inputs are supplied, so the write pulse is created as a logical-AND of these signals to allow write gating at the device for minimal skew.

The fast access time and guaranteed Output Hold time allow greater margin for system timing variation. $Data_{IN}$ setup time specified with respect to the trailing edge of Write Pulse eases write timing allowing balanced Read and Write cycle times.

FUNCTIONAL BLOCK DIAGRAM



2811 drw 01

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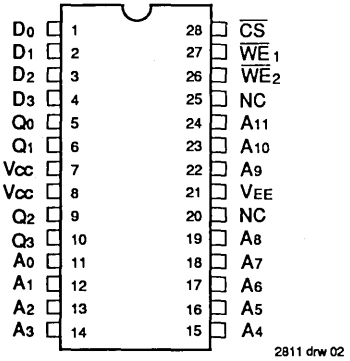
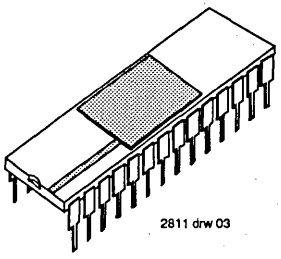
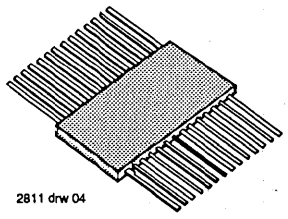
PIN CONFIGURATION



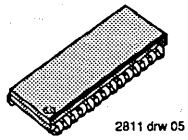
TOP VIEW



400-Mil-Wide
CERAMIC PACKAGE
C28



400-Mil-Wide
CERPACK
E28



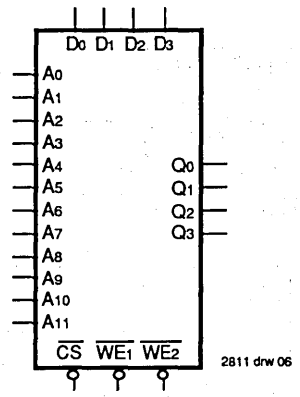
300-Mil-Wide
PLASTIC SOJ PACKAGE
Y28

PIN DESCRIPTIONS

Symbol	Pin Name
A0 through A11	Address Inputs
D0 through D3	Data Inputs
Q0 through Q3	Data Outputs
$\overline{WE1}$, $\overline{WE2}$	Write Enable Input
$\overline{CS}$	Chip Select Input (Internal pull down)
VEE	More Negative Supply Voltage
VCC	Less Negative Supply Voltage

2811 tbl 01

LOGIC SYMBOL



4Kx4
SRAM

AC OPERATING RANGES(1)

I/O	VEE	Temperature
10K	-5.2V ±5%	0 TO 75°C, air flow exceeding 2 m/sed
100K	-4.5V ±5%	0 TO 85°C, air flow exceeding 2 m/sed
101K	-4.75V to -5.46V	0 TO 75°C, air flow exceeding 2 m/sed

2811 tbl 02

NOTE:
1. Referenced to Vcc

CAPACITANCE (TA=+25°C, f=1.0MHz)

Symbol	Parameter	DIP Typ	DIP Max	FP Typ	FP Max	SOJ Typ	SOJ Max	Unit
CIN	Input Capacitance	4	–	TBD	–	3	–	pF
COUT	Output Capacitance	6	–	TBD	–	3	–	pF

2811 tbl 03

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE1}$	$\overline{WE2}$	DataOUT	Function
H	X	X	L	Deselected
L	H	X	RAM Data	Read
L	X	H	RAM Data	Read
L	L	L	WRITE Data	Write

2811 tbl 04

NOTE:
1. H=High, L=Low, X=Don't Care

ECL-10K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2811 tbl 02

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-10K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, RL=50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit	T_A
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	V_{IN} = V_{IHB} or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	V_{IN} = V_{IHB} or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	V_{IN} = V_{IHA}	$\overline{CS}$	–	–	220	µA	–
			Others	–	–	110	µA	–
I_{IL}	Input LOW Current	V_{IN} = V_{ILB}	$\overline{CS}$	0.5	–	170	µA	–
			Others	-50	–	90	µA	–
I_{EE}	Supply Current	All Inputs and Outputs Open		-190	-130	–	mA	–

2811 tbl 05

NOTE:

1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

ECL-100K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +85	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2811 tbl 07

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-100K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.5V, R_L = 50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-170	-110	–	mA

2811 tbl 08

NOTE:
1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.

5

ECL-101K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2811 tbl 09

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

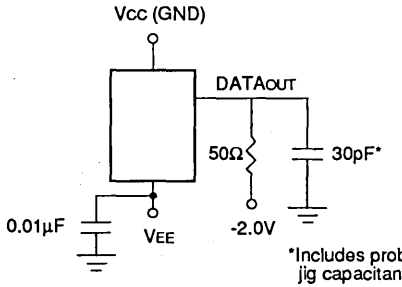
ECL-101K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L = 50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Condition		Min. (B)	Typ.(1)	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-190	-130	–	mA

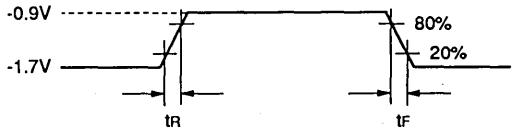
2811 tbl 10

AC TEST LOAD CONDITION



2811 drw 07

AC TEST INPUT PULSE



tR = tF = 2.0ns typ.

Note: All timing measurements are referenced to 50% input levels.

2811 drw 08

RISE/FALL TIME

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
tR	Output Rise Time	–	–	2	–	ns
tF	Output Fall Time	–	–	2	–	ns

2811 tbl 11

FUNCTIONAL DESCRIPTION

The IDT10484, IDT100484, and IDT101484 BiCMOS ECL static RAMs (SRAM) provide high speed with low power dissipation typical of BiCMOS ECL. These devices follow the center-power pinout for 4Kx4 ECL SRAMs, reducing noise over corner-power versions allowing for improved system performance. (For corner-power pinouts, please see the IDT10484, IDT100494, and IDT101484, respectively.) The ECL-101K meets electrical specifications that combine the ECL-100K temperature and voltage compensated output levels with the high-speed of ECL-10K VEE compatibility (-5.2V).

READ TIMING

The read timing on these asynchronous devices is straightforward. DataOUT is held low until the device is selected by Chip Select (CS). Then Address (ADDR) settles and data appears on the output after time tAA. Note that DataOUT is held for a short time (tOH) after the address begins to change for the next access, then ambiguous data is on the bus until a new time tAA.

WRITE TIMING

To write data to the device, a Write Pulse need be formed to control the write to the SRAM array. This Write Pulse, called $\overline{WE}$, is formed inside the device as the logical-AND of the $\overline{WE1}$ and $\overline{WE2}$ inputs; that is, when $\overline{WE1}$ and $\overline{WE2}$ both are driven low, $\overline{WE}$ goes low and the write cycle begins.

While $\overline{CS}$ and ADDR must be set-up when $\overline{WE}$ goes low, DataIN can settle after the falling edge of $\overline{WE}$, giving the data path extra margin. Data is written to the memory cell at the end of the Write Pulse, and addresses and Chip Select must be held after the rising edge of the Write Pulse to ensure satisfactory completion of the cycle.

DataOUT is disabled (held low) during the Write Cycle. If $\overline{CS}$ is held low (active) and addresses remain unchanged, the DataOUT pins will output the written data after "Write Recovery Time" (tWR).

Because of the very short Write Pulse requirement, these devices can be cycled as quickly for Writes as for Reads. Balanced cycles mean simpler timing in cache applications.

5

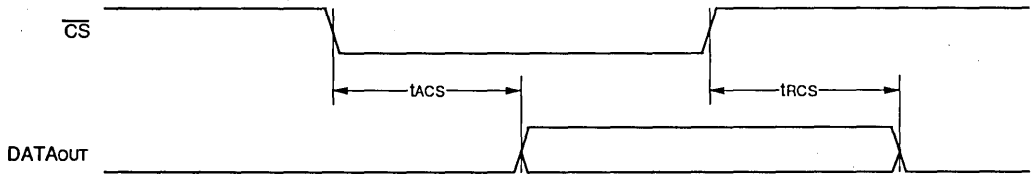
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10A484S5 100A484S5 101A484S5		10A484S7 100A484S7 101A484S7		10A484S8 100A484S8 101A484S8		10A484S10 100A484S10 101A484S10		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle											
tACS	Chip Select Access Time	–	–	2	–	3	–	5	–	5	ns
tRCS	Chip Select Recovery Time	–	–	2	–	3	–	5	–	5	ns
tAA	Address Access Time	–	–	5	–	7	–	8	–	10	ns
tOH	Data Hold from Address Change	–	2	–	3	–	3	–	3	–	ns

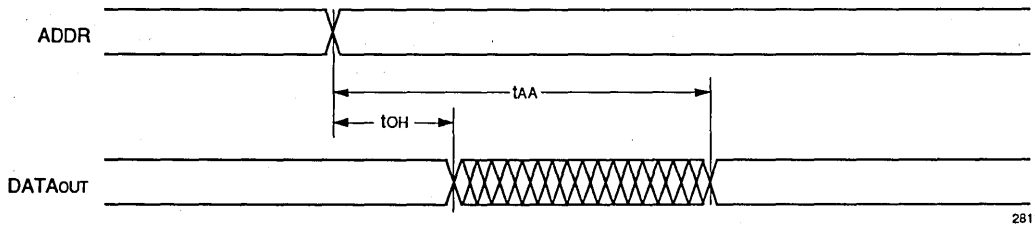
NOTE:
1. Input and Output reference level is 50% point of waveform.

2811 tbl 12

READ CYCLE GATED BY CHIP SELECT



READ CYCLE GATED BY ADDRESS



2811 drw 09

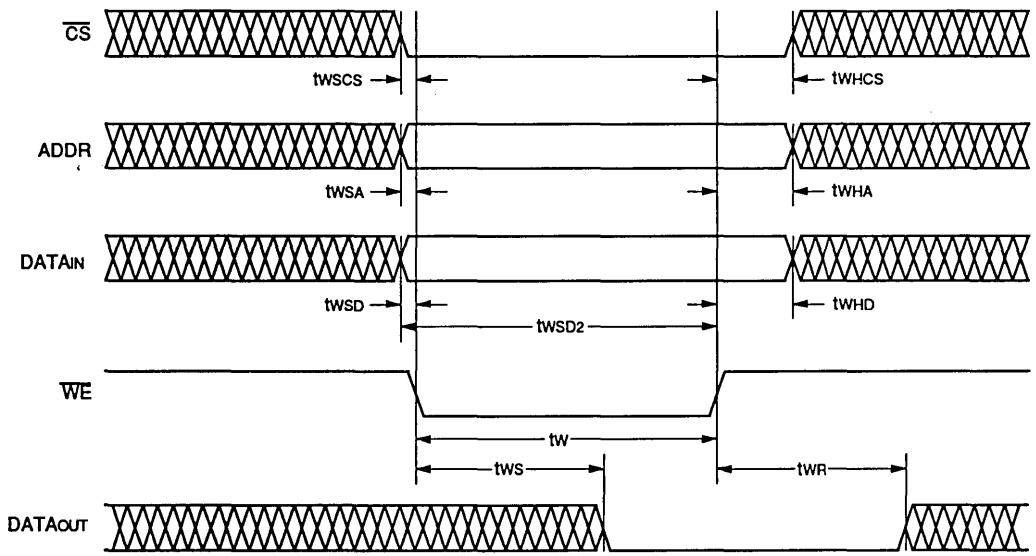
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10A484S5 100A484S5 101A484S5		10A484S7 100A484S7 101A484S7		10A484S8 100A484S8 101A484S8		10A484S10 100A484S10 101A484S10		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle											
tW	Write Pulse Width	tWSA= minimum	3	–	5	–	6	–	8	–	ns
tWSD	Data Set-up Time	–	0	–	0	–	0	–	0	–	ns
tWSD2[2]	Data Set-up Time to $\overline{WE}$ High	–	3	–	5	–	5	–	5	–	ns
tWSA	Address Set-up Time	tWSA= minimum	0	–	0	–	0	–	0	–	ns
tWSCS	Chip Select Set-up Time	–	0	–	0	–	0	–	0	–	ns
tWHD	Data Hold Time	–	1	–	1	–	1	–	1	–	ns
tWHA	Address Hold Time	–	1	–	1	–	1	–	1	–	ns
tWHCS	Chip Select Hold Time	–	1	–	1	–	1	–	1	–	ns
tWS	Write Disable Time	–	–	3	–	5	–	5	–	5	ns
tWR[3]	Write Recovery Time	–	–	3	–	5	–	5	–	5	ns

NOTES: 2811 tbl 13

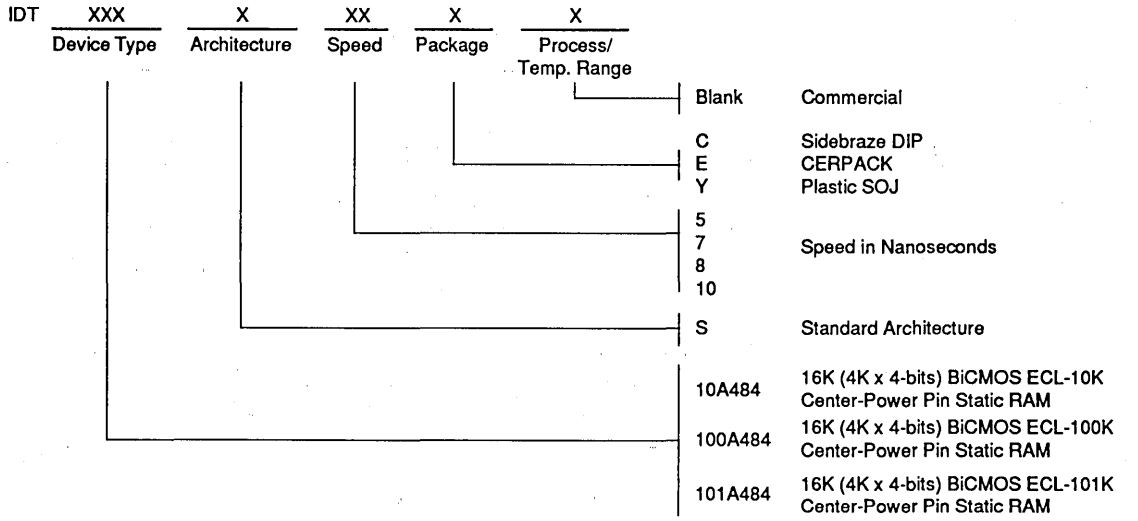
1. Input and Output reference level is 50% point of waveform.
2. tWSD is specified with respect to the falling edge of $\overline{WE}$ for compatibility with bipolar part specifications, but this device actually only requires tWSD2 with respect to rising edge of $\overline{WE}$.
3. tWR is defined as the time to reflect the newly written data on the Data Outputs (Qo to Q3) when no new Address Transition occurs.

WRITE CYCLE TIMING DIAGRAM



2811 drw 10

ORDERING INFORMATION



2811 drw 11

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 64K (64K x 1-BIT) SRAM

IDT10490
IDT100490
IDT101490

FEATURES:

- 65,536-words x 1-bit organization
- Address access time: 8/10/12/15
- Low power dissipation: 420mW (typ.)
- Guaranteed Output Hold time
- Fully compatible with ECL logic levels
- Separate data input and output
- JEDEC standard through-hole and surface mount packages

DESCRIPTION:

The IDT10490, IDT100490 and IDT101490 are 65,536-bit high-speed BiCEMOS™ ECL static random access memories organized as 64K x 1, with separate data inputs and outputs. All I/Os are fully compatible with ECL levels.

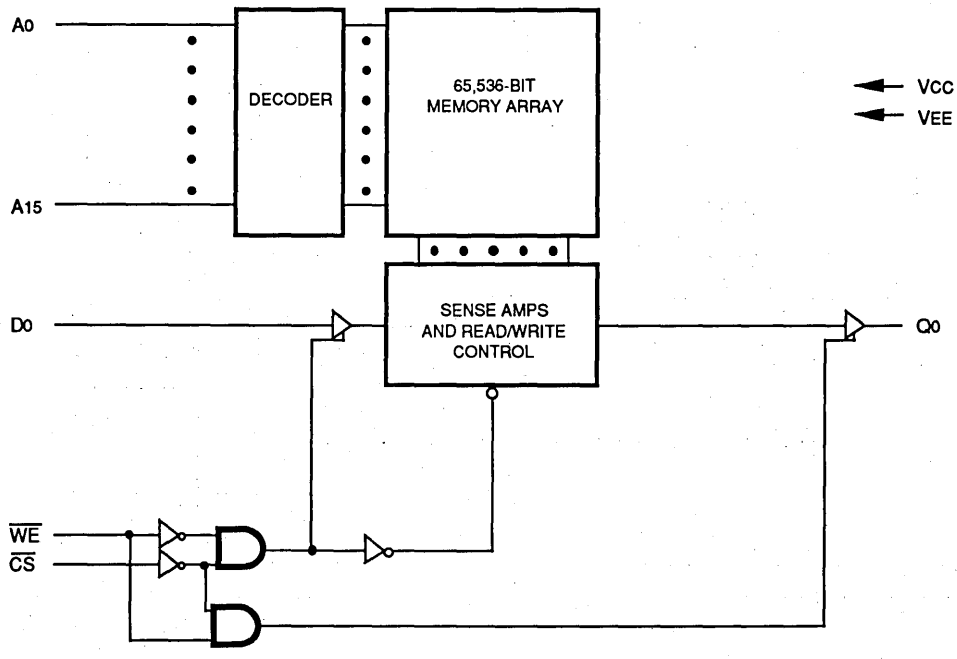
These devices are part of a family of asynchronous one-bit-wide ECL SRAMs. The devices have been configured to follow the standard ECL SRAM JEDEC pinout. Because they are manufactured in BiCEMOS™ technology, however, power dissipation is greatly reduced over equivalent bipolar devices.

The asynchronous SRAMs are the most straightforward to use because no additional clocks or controls are required: $Data_{OUT}$ is available an access time after the last change of address. To write data into the device requires the creation of a Write Pulse, and the write cycle disables the output pins in conventional fashion.

The fast access time and guaranteed Output Hold time allow greater margin for system timing variation. $Data_{IN}$ setup time specified with respect to the trailing edge of Write Pulse eases write timing allowing balanced Read and Write cycle times.

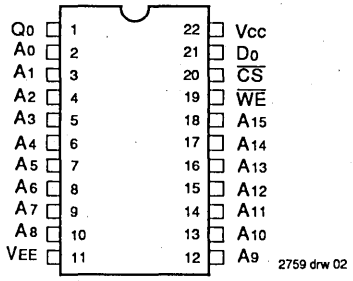
FUNCTIONAL BLOCK DIAGRAM

5

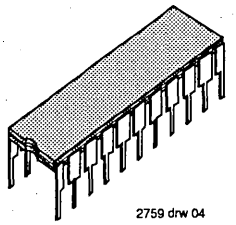


BiCEMOS is a trademark of Integrated Device Technology, Inc.

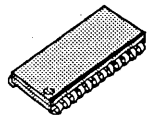
PIN CONFIGURATION



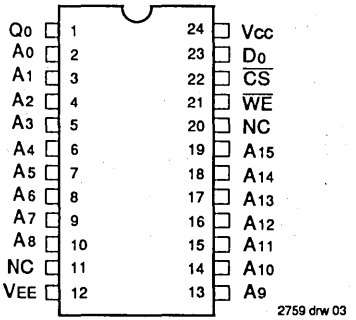
CERDIP
TOP VIEW



300-Mil-Wide
CERDIP PACKAGE
D22

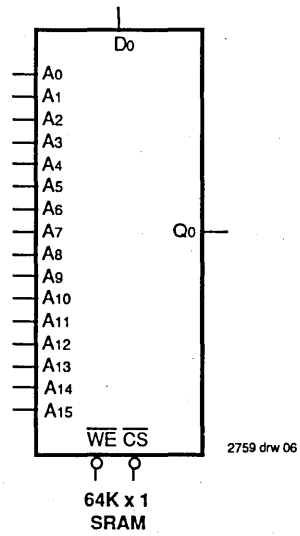


300-Mil-Wide
PLASTIC SOJ PACKAGE
Y24



SOJ
TOP VIEW

LOGIC SYMBOL



64K x 1
SRAM

PIN DESCRIPTIONS

Symbol	Pin Name
A0 through A15	Address Inputs
D0	Data Input
Q0	Data Output
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input (Internal pull down)
VEE	More Negative Supply Voltage
VCC	Less Negative Supply Voltage

2759 tbl 01

CAPACITANCE (TA =+25°C, f=1.0MHz)

Symbol	Parameter	DIP Typ.	DIP Max.	SOJ Typ.	SOJ Max.	Unit
CIN	Input Capacitance	4	–	3	–	pF
COUT	Output Capacitance	6	–	3	–	pF

2759 tbl 03

AC OPERATING RANGES(1)

I/O	VEE	Temperature
10K	-5.2V ±5%	0 TO 75°C, air flow exceeding 2 m/sed
100K	-4.5V ±5%	0 TO 85°C, air flow exceeding 2 m/sed
101K	-4.75V to -5.46V	0 TO 75°C, air flow exceeding 2 m/sed

2759 tbl 02

NOTE:
1. Referenced to VCC

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	Data OUT	Function
H	X	L	Deselected
L	H	RAM Data	Read
L	L	L	Write

2759 tbl 04

NOTE:
1. H=High, L=Low, X=Don't Care

ECL-10K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2759 tbl 05

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-10K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L =50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit	T_A
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA	–
			Others	–	–	110	µA	–
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA	–
			Others	-50	–	90	µA	–
I_{EE}	Supply Current	All Inputs and Outputs Open		-170	-80	–	mA	–

2759 tbl 06

NOTES:

1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

5

ECL-100K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +85	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Out mput Current (Output High)		-50	mA

2759 tbl 07

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-100K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.5V, R_L =50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-150	-70	–	mA

2759 tbl 08

NOTE:
1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.

ECL-101K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.0	W
I_{OUT}	DC Out mput Current (Output High)		-50	mA

2759 tbl 09

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-101K DC ELECTRICAL CHARACTERISTICS

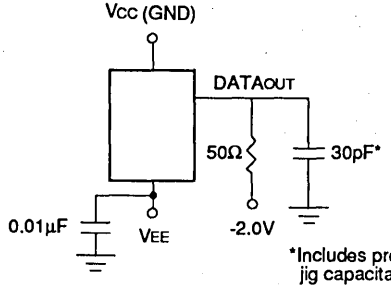
(V_{EE} = -5.2V, R_L=50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-170	-80	–	mA

2759 tbl 10

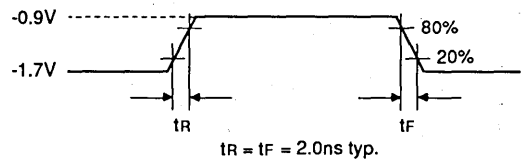
NOTE:
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

AC TEST LOAD CONDITION



2759 drw 07

AC TEST INPUT PULSE



tR = tF = 2.0ns typ.

Note: All timing measurements are referenced to 50% input levels.

2759 drw 08

RISE/FALL TIME

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
tR	Output Rise Time	–	–	2	–	ns
tF	Output Fall Time	–	–	2	–	ns

2759 tbl 11

FUNCTIONAL DESCRIPTION

The IDT10490, IDT100490 and IDT101490 BiCMOS ECL static RAMs (SRAM) provide high speed with low power dissipation typical of BiCMOS ECL. These devices follow the conventional pinout and functionality for 64Kx1 SRAMs. The ECL -101K meets electrical specifications that combine the ECL-100K temperature and voltage compensated output levels with the high-speed of ECL-10K VEE compatibility (-5.2V).

READ TIMING

The read timing on these asynchronous devices is straightforward. DataOUT is held low until the device is selected by Chip Select ($\overline{CS}$). Then Address (ADDR) settles and data appears on the output after time tAA. Note that DataOUT is held for a short time (tOH) after the address begins to change for the next access, then ambiguous data is on the bus until a new time tAA.

WRITE TIMING

To write data to the device, a Write Pulse need be formed on the Write Enable input ($\overline{WE}$) to control the write to the SRAM array. While $\overline{CS}$ and ADDR must be set-up when $\overline{WE}$ goes low, DataIN can settle after the falling edge of $\overline{WE}$, giving the data path extra margin. Data is written to the memory cell at the end of the Write Pulse, and addresses and Chip Select must be held after the rising edge of the Write Pulse to ensure satisfactory completion of the cycle.

DataOUT is disabled (held low) during the Write Cycle. If $\overline{CS}$ is held low (active) and addresses remain unchanged, the DataOUT pins will output the written data after "Write Recovery Time" (tWR).

Because of the very short Write Pulse requirement, these devices can be cycled as quickly for Writes as for Reads. Balanced cycles mean simpler timing in cache applications.

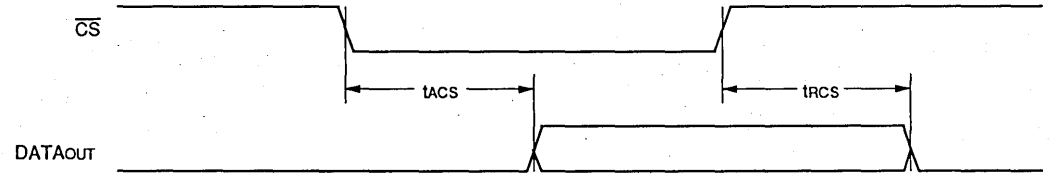
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10490S8 100490S8 101490S8		10490S10 100490S10 101490S10		10490S12 100490S12 101490S12		10490S15 100490S15 101490S15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle											
tACS	Chip Select Access Time	–	–	3	–	5	–	5	–	5	ns
tRCS	Chip Select Recovery Time	–	–	3	–	5	–	5	–	5	ns
tAA	Address Access Time	–	–	8	–	10	–	12	–	15	ns
tOH	Data Hold from Address Change	–	3	–	3.5	–	3.5	–	3.5	–	ns

NOTES:
1. Input and Output reference level is 50% point of waveform.

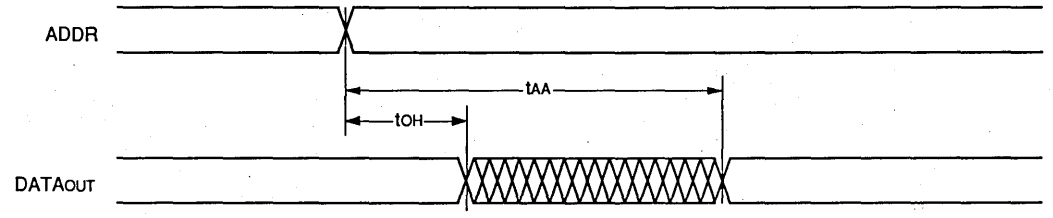
2759 tbl 12

READ CYCLE GATED BY CHIP SELECT



2759 drw 09

READ CYCLE GATED BY ADDRESS



2759 drw 10

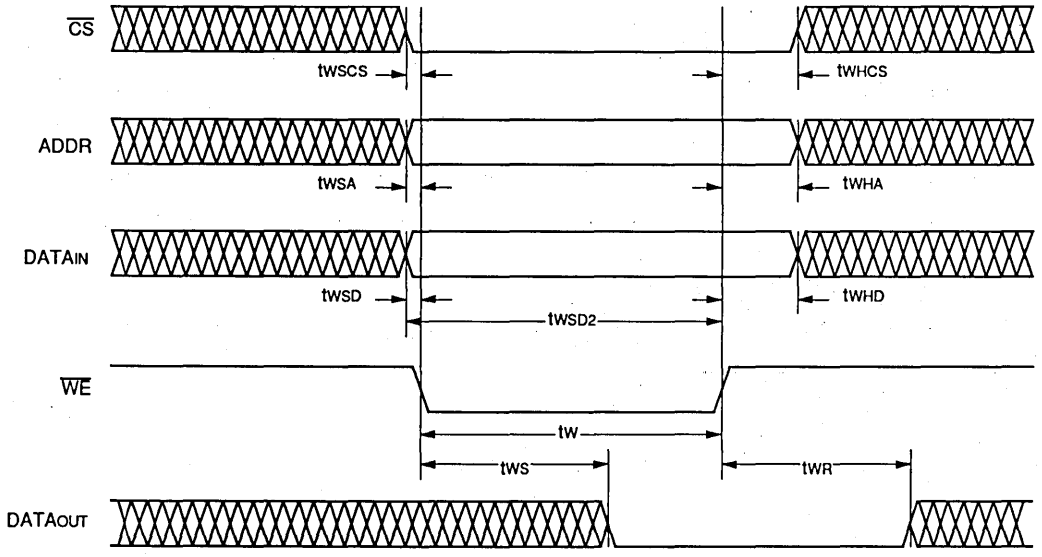
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10490S8 100490S8 101490S8		10490S10 100490S10 101490S10		10490S12 100490S12 101490S12		10490S15 100490S15 101490S15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle											
tW	Write Pulse Width	tWSA = minimum	6	–	8	–	10	–	10	–	ns
tWSD	Data Set-up Time	–	0	–	0	–	0	–	2	–	ns
tWSD2[2]	Data Set-up Time to $\overline{WE}$ High	–	5	–	5	–	5	–	5	–	ns
tWSA	Address Set-up Time	tWSA = minimum	0	–	0	–	0	–	2	–	ns
tWSCS	Chip Select Set-up Time	–	0	–	0	–	0	–	2	–	ns
tWHD	Data Hold Time	–	2	–	2	–	2	–	3	–	ns
tWHA	Address Hold Time	–	2	–	2	–	2	–	3	–	ns
tWHCS	Chip Select Hold Time	–	2	–	2	–	2	–	3	–	ns
tWS	Write Disable Time	–	–	5	–	5	–	5	–	10	ns
tWR[3]	Write Recovery Time	–	–	10	–	12	–	14	–	18	ns

2759 tbl 13

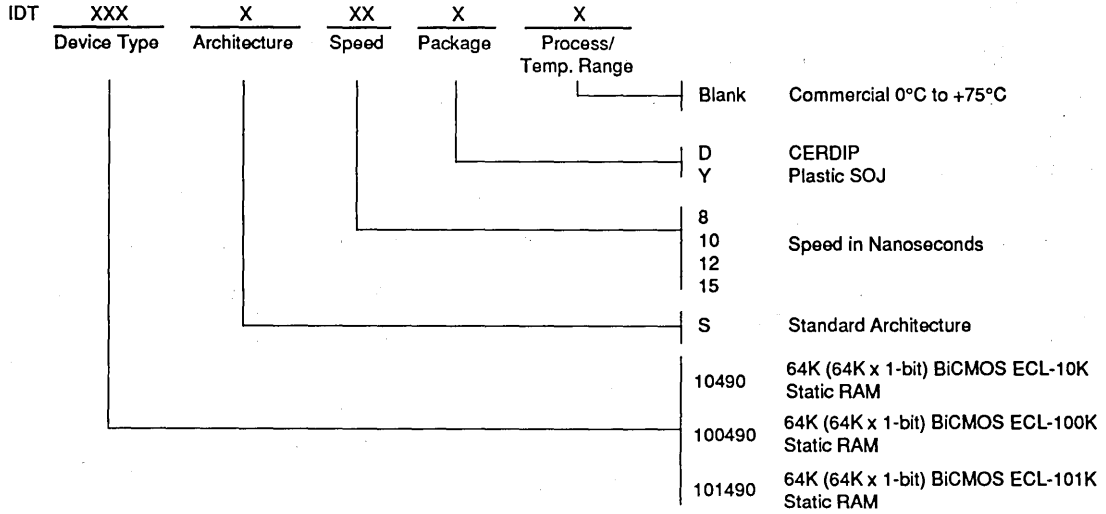
NOTES:
1. Input and Output reference level is 50% point of waveform.
2. tWSD is specified with respect to the falling edge of $\overline{WE}$ for compatibility with bipolar part specifications, but this device actually only requires tWSD2 with respect to rising edge of $\overline{WE}$.
3. tWR=tWHA + tAA and thus can include a full access time if addresses change while Chip Select is still low.

WRITE CYCLE TIMING DIAGRAM



2759 drw 11

ORDERING INFORMATION



2759 drw 12

5

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 64K (16K x 4-BIT) SRAM

IDT10494
IDT100494
IDT101494

FEATURES:

- 16,384-words x 4-bit organization
- Address access time: 7/8/10/15
- Low power dissipation: 700mW (typ.)
- Guaranteed Output Hold time
- Fully compatible with ECL logic levels
- Separate data input and output
- JEDEC standard through-hole and surface mount packages

DESCRIPTION:

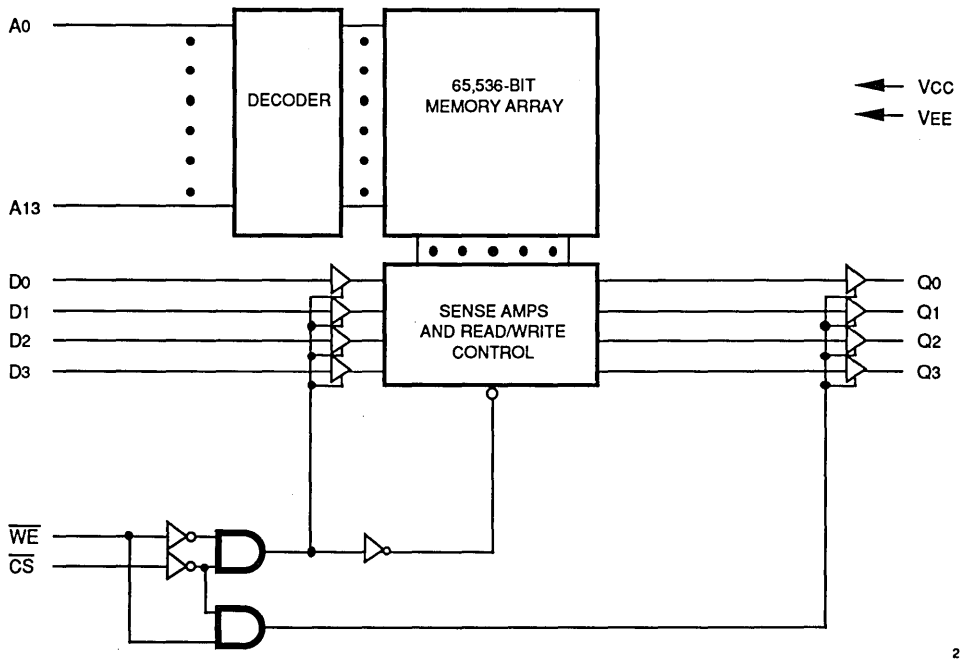
The IDT10494, IDT100494 and 101494 are 65,536-bit high-speed BiCEMOS™ ECL static random access memories organized as 16K x 4, with separate data inputs and outputs. All I/Os are fully compatible with ECL levels.

These devices are part of a family of asynchronous four-bit-wide ECL SRAMs. The devices have been configured to follow the standard ECL SRAM JEDEC pinout. Because they are manufactured in BiCEMOS™ technology, however, power dissipation is greatly reduced over equivalent bipolar devices.

The asynchronous SRAMs are the most straightforward to use because no additional clocks or controls are required: $Data_{OUT}$ is available an access time after the last change of address. To write data into the device requires the creation of a Write Pulse, and the write cycle disables the output pins in conventional fashion.

The fast access time and guaranteed Output Hold time allow greater margin for system timing variation. $Data_{IN}$ setup time specified with respect to the trailing edge of Write Pulse eases write timing allowing balanced Read and Write cycle times.

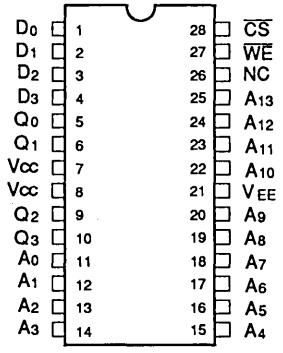
FUNCTIONAL BLOCK DIAGRAM



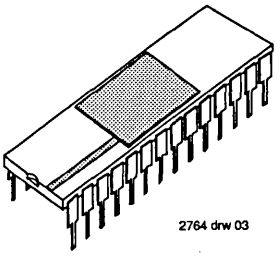
2764 drw 01

BiCEMOS is a trademark of Integrated Device Technology, Inc.

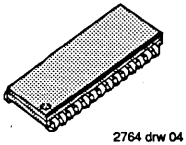
PIN CONFIGURATION



DIP/SOJ
TOP VIEW



400-Mil-Wide
CERAMIC PACKAGE
C28



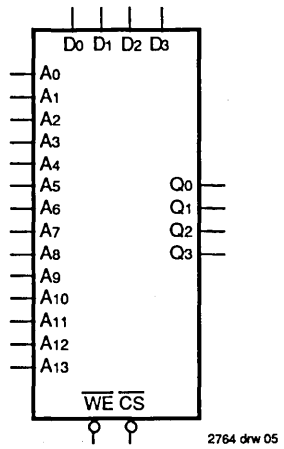
300-Mil-Wide
PLASTIC SOJ PACKAGE
Y28

PIN DESCRIPTIONS

Symbol	Pin Name
A0 through A13	Address Inputs
D0 through D3	Data Inputs
Q0 through Q3	Data Outputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input (Internal pull down)
VEE	More Negative Supply Voltage
VCC	Less Negative Supply Voltage

2764 tbl 01

LOGIC SYMBOL



16K x 4
SRAM

AC OPERATING RANGES(1)

I/O	VEE	Temperature
10K	-5.2V ±5%	0 TO 75°C, air flow exceeding 2 m/sec
100K	-4.5V ±5%	0 TO 85°C, air flow exceeding 2 m/sec
101K	-4.75V to -5.46V	0 TO 75°C, air flow exceeding 2 m/sec

2764 tbl 02

NOTE:
1. Referenced to Vcc

CAPACITANCE (TA=+25°C, f=1.0MHz)

Symbol	Parameter	DIP		SOJ		Unit
		Typ.	Max.	Typ.	Max.	
CIN	Input Capacitance	4	–	3	–	pF
COUT	Output Capacitance	6	–	3	–	pF

2764 tbl 03

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	DataOUT	Function
H	X	L	Deselected
L	H	RAM Data	Read
L	L	L	Write

NOTE:
1. H=High, L=Low, X=Don't Care

2764 tbl 04

ECL-10K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Output Current (Output High)		-50	mA

NOTE: 2764 tbl 05

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-10K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L =50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit	T_A
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA	–
			Others	–	–	110	µA	–
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA	–
			Others	-50	–	90	µA	–
I_{EE}	Supply Current	All Inputs and Outputs Open		-190	-130	–	mA	–

NOTE: 2764 tbl 06

1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

ECL-100K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
VTERM	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
TA	Operating Temperature		0 to +85	°C
TBIAS	Temperature Under Bias		-55 to +125	°C
TSTG	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
PT	Power Dissipation		1.5	W
IOUT	DC Out mput Current (Output High)		-50	mA

2762 tbl 07

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-100K DC ELECTRICAL CHARACTERISTICS

(VEE = -4.5V, RL =50Ω to -2.0V, TA = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit
VOH	Output HIGH Voltage	VIN = VIHA or VILB		-1025	-955	-880	mV
VOL	Output LOW Voltage	VIN = VIHA or VILB		-1810	-1715	-1620	mV
VOHC	Output Threshold HIGH Voltage	VIN = VIHB or VILA		-1035	–	–	mV
VOLC	Output Threshold LOW Voltage	VIN = VIHB or VILA		–	–	-1610	mV
VIH	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
VIL	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I IH	Input HIGH Current	VIN = VIHA	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I IL	Input LOW Current	VIN = VILB	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
IEE	Supply Current	All Inputs and Outputs Open		-170	-110	–	mA

2762 tbl 08

NOTE:
1. Typical parameters are specified at VEE = -4.5V, TA = +25°C and maximum loading.

5

ECL-101K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Out mput Current (Output High)		-50	mA

2763 tbl 09

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-101K DC ELECTRICAL CHARACTERISTICS

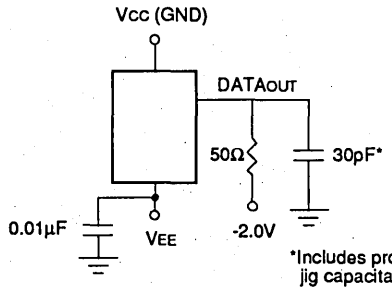
(V_{EE} = -5.2V, R_L=50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-190	-130	–	mA

2763 tbl 10

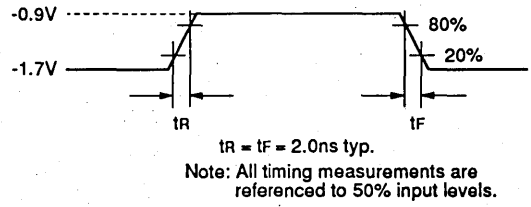
NOTE:
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

AC TEST LOAD CONDITION



2764 drw 06

AC TEST INPUT PULSE



2764 drw 07

RISE/FALL TIME

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
tR	Output Rise Time	–	–	2	–	ns
tF	Output Fall Time	–	–	2	–	ns

2764 tbl 11

FUNCTIONAL DESCRIPTION

The IDT10494, IDT100494 and IDT101494 BiCMOS ECL static RAMs (SRAM) provide high speed with low power dissipation typical of BiCMOS ECL. These devices follow the conventional pinout and functionality for 16K x 4 ECL SRAMs. The ECL-101K meets electrical specifications that combine the ECL-100K temperature and voltage compensated output levels with the high-speed of ECL-10K VEE compatibility (-5.2V).

READ TIMING

The read timing on these asynchronous devices is straightforward. DataOUT is held low until the device is selected by Chip Select ($\overline{CS}$). Then Address (ADDR) settles and data appears on the output after time tAA. Note that DataOUT is held for a short time (tOH) after the address begins to change for the next access, then ambiguous data is on the bus until a new time tAA.

WRITE TIMING

To write data to the device, a Write Pulse need be formed on the Write Enable input ($\overline{WE}$) to control the write to the SRAM array. While $\overline{CS}$ and ADDR must be set-up when $\overline{WE}$ goes low, DataIN can settle *after* the falling edge of $\overline{WE}$, giving the datapath extra margin. Data is written to the memory cell at the end of the Write Pulse, and addresses and Chip Select must be held after the rising edge of the Write Pulse to ensure satisfactory completion of the cycle.

DataOUT is disabled (held low) during the Write Cycle. If $\overline{CS}$ is held low (active) and addresses remain unchanged, the DataOUT pins will output the written data after "Write Recovery Time" (tWR).

Because of the very short Write Pulse requirement, these devices can be cycled as quickly for Writes as for Reads. Balanced cycles mean simpler timing in cache applications.

5

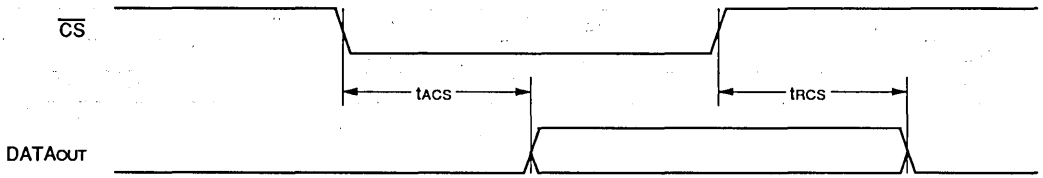
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10494S7 100494S7 101494S7		10494S8 100494S8 101494S8		10494S10 100494S10 101494S10		10494S15 100494S15 101494S15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle											
tACS	Chip Select Access Time	–	–	3	–	5	–	5	–	5	ns
tRCS	Chip Select Recovery Time	–	–	3	–	5	–	5	–	5	ns
tAA	Address Access Time	–	–	7	–	8	–	10	–	15	ns
tOH	Data Hold from Address Change	–	3	–	3	–	3	–	3	–	ns

NOTE:
1. Input and Output reference level is 50% point of waveform.

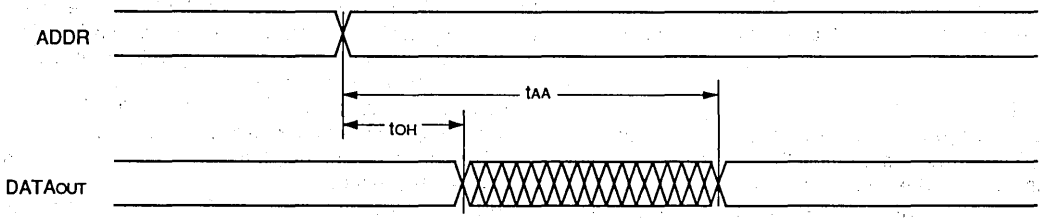
2764 tbl 12

READ CYCLE GATED BY CHIP SELECT



2764 drw 08

READ CYCLE GATED BY ADDRESS



2764 drw 09

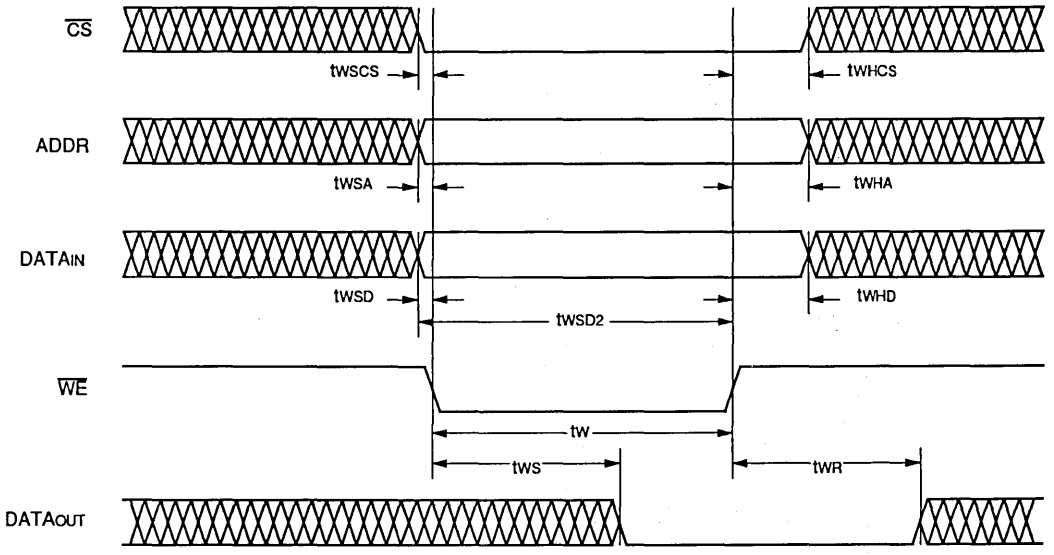
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10494S7 100494S7 101494S7		10494S8 100494S8 101494S8		10494S10 100494S10 101494S10		10494S15 100494S15 101494S15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle											
tW	Write Pulse Width	tWSA = minimum	5	–	6	–	8	–	10	–	ns
tWSD	Data Set-up Time	–	0	–	0	–	0	–	2	–	ns
tWSD2[2]	Data Set-up Time to $\overline{WE}$ High	–	5	–	5	–	5	–	5	–	ns
tWSA	Address Set-up Time	tWSA = minimum	0	–	0	–	0	–	2	–	ns
tWSCS	Chip Select Set-up Time	–	0	–	0	–	0	–	2	–	ns
tWHD	Data Hold Time	–	1	–	2	–	2	–	3	–	ns
tWHA	Address Hold Time	–	1	–	2	–	2	–	3	–	ns
tWHCS	Chip Select Hold Time	–	1	–	2	–	2	–	3	–	ns
tWS	Write Disable Time	–	–	5	–	5	–	5	–	5	ns
tWR[3]	Write Recovery Time	–	–	5	–	5	–	5	–	5	ns

2764 tbl 13

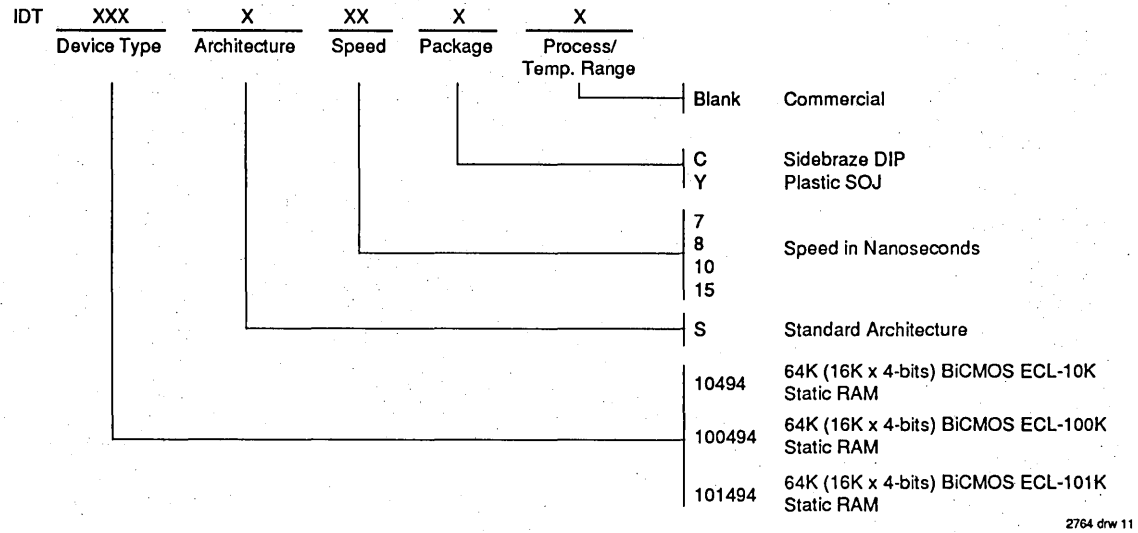
NOTES:
1. Input and Output reference level is 50% point of waveform.
2. tWSD is specified with respect to the falling edge of $\overline{WE}$ for compatibility with bipolar part specifications, but this device actually only requires tWSD2 with respect to rising edge of $\overline{WE}$.
3. tWR is defined as the time to reflect the newly written data on the Data Outputs (Q_0 to Q_3) when no new Address Transition occurs.

WRITE CYCLE TIMING DIAGRAM



2764 drw 10

ORDERING INFORMATION



2764 drw 11

Integrated Device Technology, Inc.

SELF-TIMED BiCMOS ECL STATIC RAM 64K (16K x 4-BIT) STRAM

PRELIMINARY
IDT10496LL
IDT100496LL
IDT101496LL

FEATURES:

- 16,384-words x 4-bit organization
- Self-Timed Write, with latches on inputs and latches on outputs
- Balanced Read/Write cycle time: 13/15ns
- Access time: 10/12 ns (max.)
- Fully compatible with ECL logic levels
- Through-hole DIP and surface-mount packages

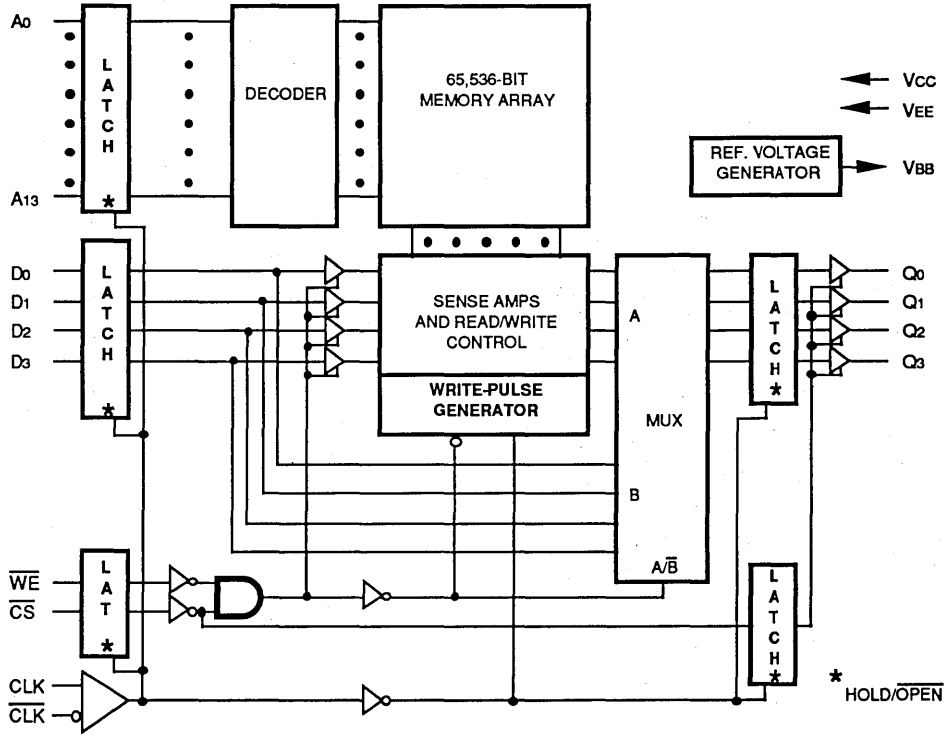
DESCRIPTION:

The IDT10496LL, IDT100496LL and IDT101496LL are 65,536-bit high-speed BiCEMOS™ ECL static random access memories organized as 16K x 4, with inputs and outputs fully compatible with ECL levels. Clocked level-sensitive latches on inputs and outputs, and the self-timed write operation, provide enhanced system performance over conventional RAMs, providing easier design and improved system level cycle times.

Inputs can flow into the device and then are latched by the leading edge of an externally supplied differential clock. The small input valid window required means more margin for system skews. Logic-to-memory propagation delay is included in device cycle time calculation, allowing this device to deliver better system performance than asynchronous SRAMs and glue logic.

Write timing is controlled internally based on the clock. Write Enable has no special requirements. The device allows balanced read and write cycle times, and reads and writes can be inserted in any order.

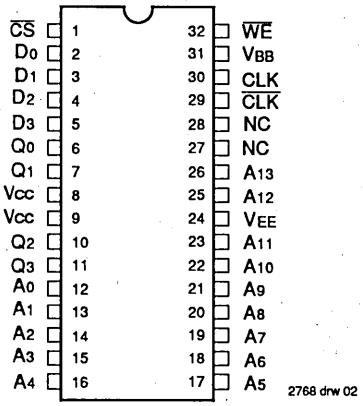
FUNCTIONAL BLOCK DIAGRAM



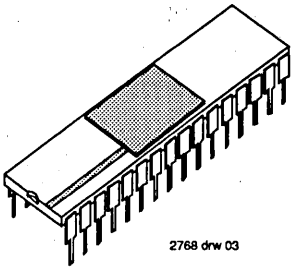
2768 drw 01

BiCEMOS is a trademark of Integrated Device Technology, Inc.

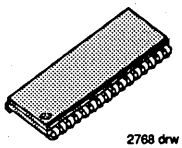
PIN CONFIGURATION



TOP VIEW



400-Mil-Wide
CERAMIC PACKAGE
C32



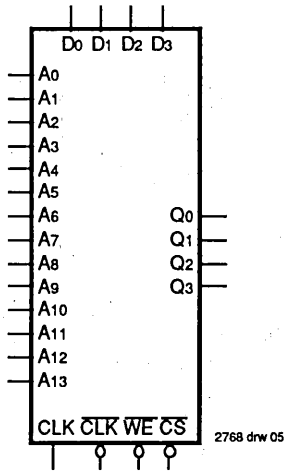
300-Mil-Wide
PLASTIC SOJ PACKAGE
Y32

PIN DESCRIPTION

Symbol	Pin Name
A0 through A13	Address Inputs
D0 through D3	Data Inputs
Q0 through Q3	Data Outputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input (Internal pull down)
CLK, $\overline{CLK}$	Differential Clock Inputs
VBB	Reference Voltage Output (≈1.32V)
VEE	More Negative Supply Voltage
VCC	Less Negative Supply Voltage
NC	No Connect - not internally bonded

2768 tbl 01

LOGIC SYMBOL



16Kx4
STRAM

AC OPERATING RANGES(1)

I/O	VEE	Temperature
10K	-5.2V ±5%	0 TO 75°C, air flow exceeding 2 m/sec
100K	-4.5V ±5%	0 TO 85°C, air flow exceeding 2 m/sec
101K	-4.75V to -5.46V	0 TO 75°C, air flow exceeding 2 m/sec

2768 tbl 02

NOTE:
1. Referenced to VCC

CAPACITANCE (TA=+25°C, f=1.0MHz)

Symbol	Parameter	DIP Typ.	DIP Max.	SOJ Typ.	SOJ Max.	Unit
CINCLK	Input Capacitance CLK/$\overline{CLK}$	6	–	3	–	pF
CIN	Input Capacitance except CLK/$\overline{CLK}$	4	–	3	–	pF
COUT	Output Capacitance	6	–	3	–	pF

2768 tbl 03

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	CLK	DataOUT(2)	Function
H	X	↑	L	Deselected
L	H	↑	RAM Data	Read
L	L	↑	WRITE Data	Write

2768 tbl 04

NOTES:
1. H=High, L=Low, X=Don't Care
2. DATAOUT changes when CLK returns high.

ECL-10K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2768 tbl 05

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-10K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L =50Ω to -2.0V, T_A = 0 to +75°C for DIP, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit	T_A
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs(2)		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs(2)		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA	–
			Others	–	–	110	µA	–
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA	–
			Others	-50	–	90	µA	–
I_{EE}	Supply Current	All Inputs and Outputs Open(2)		-260	-200	–	mA	–

2768 tbl 06

NOTES:
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.
2. Except CLK and $\overline{CLK}$, one of which is tied low and one is tied high.

5

ECL-100K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +85	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2768 tbl 07

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-100K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.5V, RL=50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs[2]		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs[2]		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open[2]		-240	-180	–	mA

2768 tbl 08

NOTES:

1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.
2. Except CLK and $\overline{CLK}$, one of which is tied low and one is tied high.

ECL-101K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2768 tbl 09

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-101K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L=50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

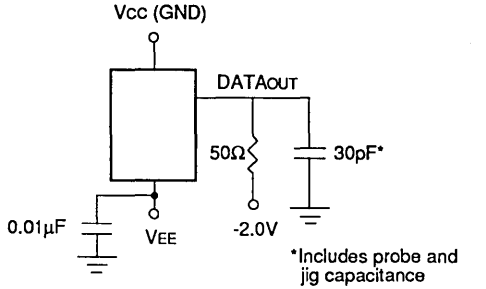
Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs(2)		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs(2)		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open(2)		-260	-200	–	mA

2768 tbl 10

NOTES:

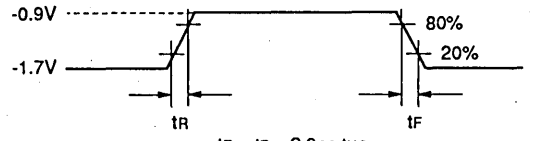
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.
2. Except CLK and $\overline{CLK}$, one of which is tied low and one is tied high.

LOAD CONDITION



2768 drw 06

INPUT PULSE



Note: All timing measurements are referenced to 50% input levels.

2768 drw 07

RISE/FALL TIME

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
tR	Output Rise Time	–	–	2	–	ns
tF	Output Fall Time	–	–	2	–	ns

2770 tbl 11

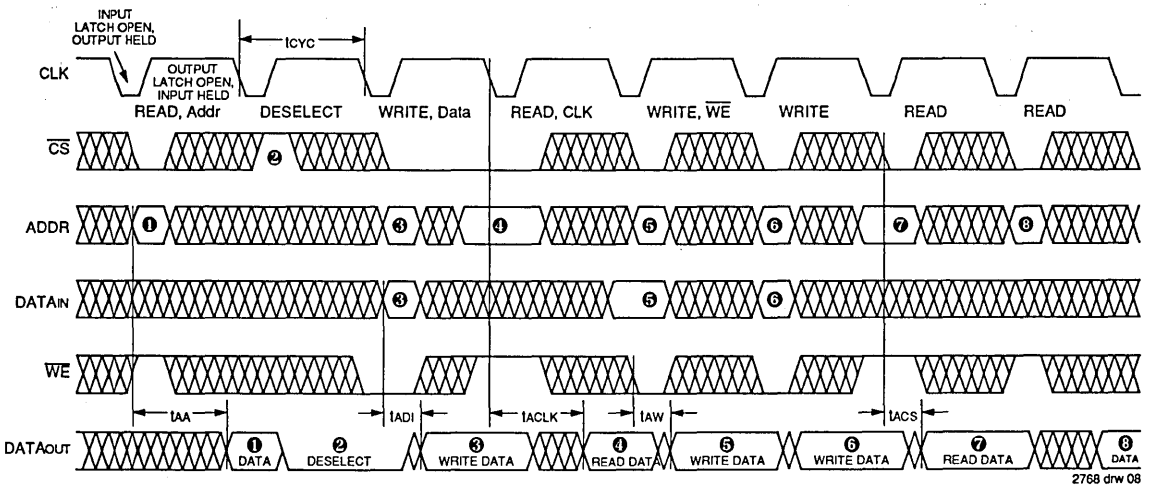
FUNCTIONAL DESCRIPTION

The IDT10496LL, IDT100496LL, and IDT101496LL Self-Timed BiCMOS ECL static RAMs (STRAM) provide high speed with low power dissipation typical of BiCMOS ECL. On-chip logic additionally helps improve system performance. The ECL-101K meets electrical specifications that combine the ECL-100K temperature and voltage compensated output levels with the high-speed of ECL-10K VEE compatibility (-5.2V).

As can be seen in the Functional Block Diagram on the title page, this device contains level-sensitive latches to sample and hold addresses, input data, and control status, and hold output data. Inputs are transparent while the clock (CLK) input is low (and $\overline{CLK}$ is high), and then hold their contents when the clock returns high. In the case of a write cycle, the memory cell is written during the clock-high time, and write data conducted to the outputs. Because the output latches are controlled by an inversion of the clock, output data flows out the output latch while clock is high and then is held into the next cycle during clock low.

The Latch-Latch architecture is most useful when read access data is needed within the same cycle that addresses settle. The input latch, when transparent, allows the access to begin as soon as addresses settle, allowing data to be ready somewhat sooner in the cycle than would be possible with a clocked-register implementation.

FUNCTIONAL DESCRIPTION TIMING EXAMPLE



2768 drw 08

READ TIMING

In a typical read cycle, the read address flows into the device while clock is low, as at ❶ below. Read access begins when the last address has settled. When clock returns high, the inputs are held so that addresses can begin to change for the next cycle.

Clock high also opens the output latches, so the read data for the read address clocked in at ❶ is gated through the output latch to the output pins. There is a short delay from rising clock to output ready, called t_{DR} (see Read Cycle Timing). If the clock-low time (t_{WL}) is shorter than the inherent access-time of the cell, output is guaranteed valid after the specified t_{AA}. But if t_{WL} is longer than the cell access-time, output data will be valid t_{DR} after clock goes high. Thus, the time it takes from address valid to data ready for any given address is

$t_{AA} = t_{AA}$ or $(t_{SA} + t_{DR})$,

whichever is larger. A permutation of this equation holds for each read and write access modes.

Because addresses and control lines (Write Enable and Chip Select) all must be stable for access to commence, there are two other read access modes, described as follows.

If addresses and controls are all stable before input latches are opened by clock going low, as at ❹ below, access begins on the low-going edge of clock. Data is available t_{ACLK} later, provided the output latch is opened by clock returning high.

If address and Write Enable are valid after clock-low, but Chip Select is last to go low, as at ❼ below, data is available t_{ACS} after the low-going edge of Chip Select.

The output latch takes some time to change state for the next cycle, but this time is very short. Therefore, data hold time from clock high (t_{DH}) is specified as zero minimum hold time.

DESELECT TIMING

Because the outputs are latched, they will continue to drive the output pins until a disable state is clocked through the device. The deselected state is achieved by de-asserting chip select ($\overline{CS}$ high) before clock returns high. This case occurs at ❷ below. Outputs then attain the disable state (low) t_{DR} later. Status of other inputs do not effect the disabling of the device when chip select is de-asserted with the proper relation to clock.

WRITE TIMING

Write cycles are identical to read cycles, except that write enable and write data need also be supplied, with the appropriate setup and hold timing. The device has on-chip timing that handles all aspects of writing data into the addressed RAM cell without the need for external write-pulse generation. The timing logic uses the clock-high time as the write pulse, and thus determines the minimum clock-high time, t_{WH}.

In addition to writing to the RAM cell, the write data is fed to the output register by a multiplexer, so that write data is available on the output pins after an access time. Thus the input data supplied at ❸ is available on the output t_{ADI} after the input data has settled, while the input data supplied at ❺ is available t_{AW} after Write Enable is asserted low. This function is sometimes called "Transparent Write," and is useful for write-through cache applications.

There are no restrictions on the order of read cycles and write cycles.

5

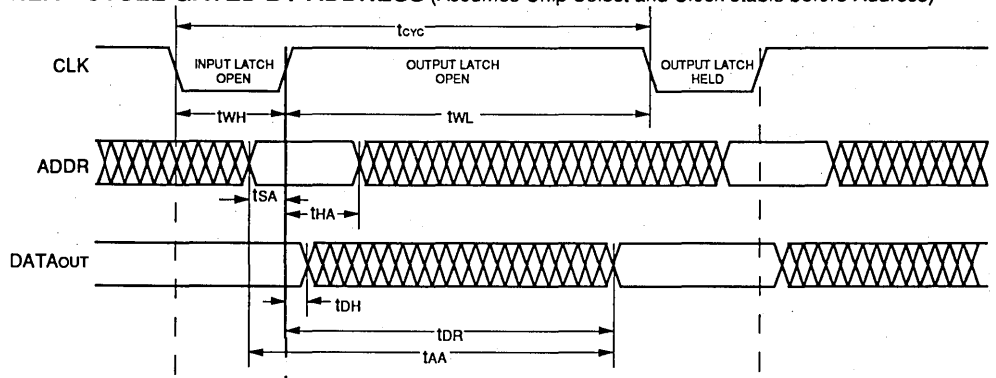
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10496LL13 100496LL13 101496LL13		10496LL15 100496LL15 101496LL15		Unit
			Min.	Max.	Min.	Max.	
Read Cycle							
tCYC	Cycle Time	–	13	–	15	–	ns
tAA[2]	Address Access Time	–	–	10	–	12	ns
tACS[3]	Chip Select Access Time	–	–	5	–	5	ns
tACLK[4]	Access Time from Clock Low	–	–	10	–	12	ns
tWL	Clock Low Pulse Width	–	3	–	3	–	ns
tWH	Clock High Pulse Width	–	10	–	12	–	ns
tSCS	Setup Time for Chip Select	–	1	–	1	–	ns
tSA	Setup Time for Address	–	1	–	1	–	ns
tHCS	Hold Time for Chip Select	–	2	–	2	–	ns
tHA	Hold Time for Address	–	2	–	2	–	ns
tDH	Data Hold from Clock Low	–	0	–	0	–	ns
tDR[5]	Data Ready from Clock Low	–	0	4	0	4	ns

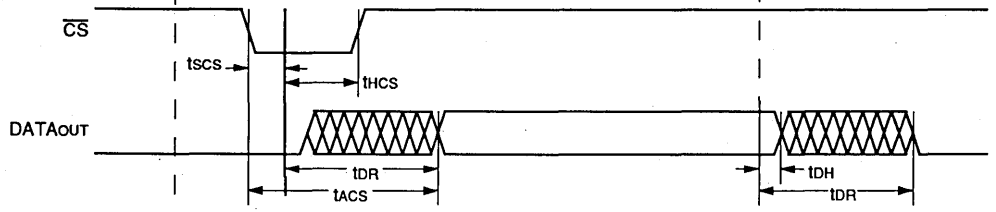
2768 tbl 12

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. Read Cycle is gated by Address when tSA < tWL so that the access begins at the settling of Address. Access time is the larger of tAA or tSA + tDR.
3. Read Cycle is gated by Chip Select when tSCS < tWL so that access begins at the falling edge of Chip Select. Access time is the larger of tACS or tSCS + tDR.
4. Read Cycle is gated by Clock when tSA > tWL so that access begins at the falling edge of Clock. Access time is the larger of tACLK or tWL + tDR.
5. tDR(max) is specified when all other gating conditions have been satisfied, specifically, for READ cycle: when tSA > tAA(max) - tDR(max) and tSCS > tACS(max) - tDR(max) and tWL > tACLK(max) - tDR(max); for WRITE cycle: when tSD > tADI(max) - tDR(max) and tSWE > tAW(max) - tDR(max).

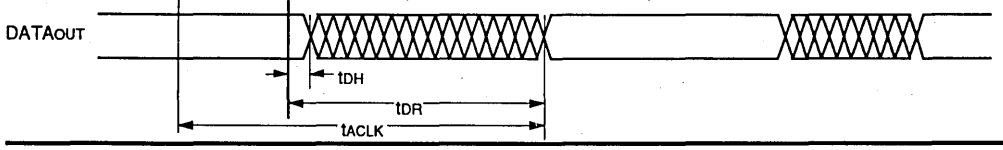
READ CYCLE GATED BY ADDRESS (Assumes Chip Select and Clock stable before Address)



READ CYCLE GATED BY CHIP SELECT (Assumes Address and Clock stable before Chip Select)



READ CYCLE GATED BY CLOCK (Assumes Address and Chip Select stable before Clock Low)



2768 drw 09

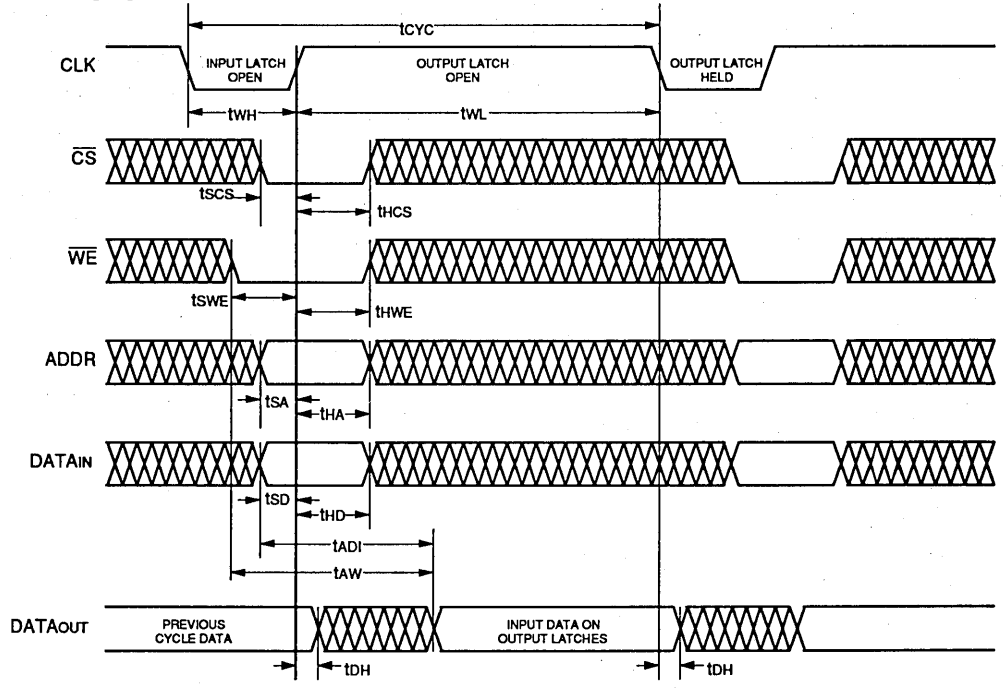
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10496LL13 100496LL13 101496LL13		10496LL15 100496LL15 101496LL15		Unit
			Min.	Max.	Min.	Max.	
Write Cycle[2]							
t_{AW}[3]	Write Enable Low to Data Valid	–	–	5	–	5	ns
t_{ADI}[4]	Data In Valid to Data Out Valid	–	–	5	–	5	ns
t_{SWE}	Setup Time for Write Enable	–	1	–	1	–	ns
t_{SD}	Setup Time for Data In	–	1	–	1	–	ns
t_{HWE}	Hold Time for Write Enable	–	2	–	2	–	ns
t_{HD}	Hold Time for Data In	–	2	–	2	–	ns

2768 tbl 13

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. All Setup, Hold, and Access timing are the same as the Read Cycle with the addition of above requirements. Write Data appears on output pins after rising edge of clock.
3. Access time is the larger of t_{AW} or t_{SWE} + t_{DR}.
4. Access time is the larger of t_{ADI} or t_{SD} + t_{DR}.

WRITE CYCLE

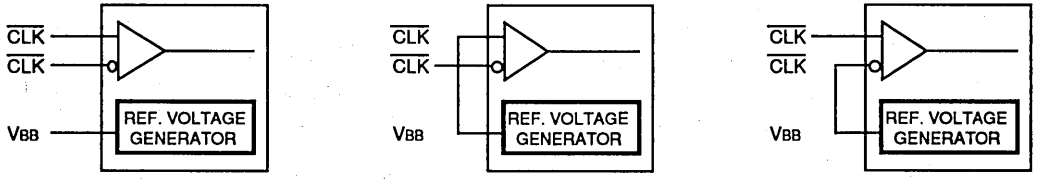


2768 drw 10

5

CLOCK INPUT

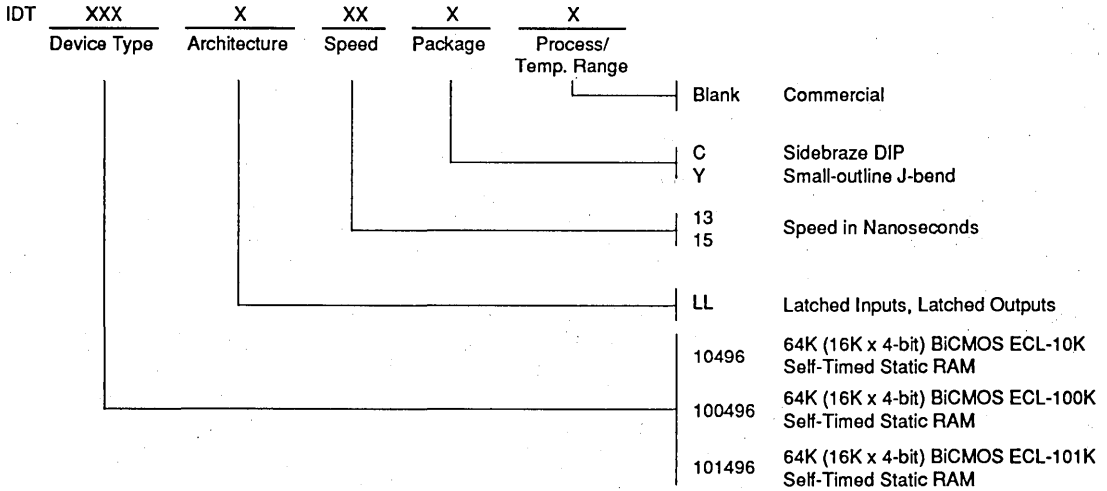
The clock input circuit has been designed to accomodate both single-ended and differential mode operation. Differential mode exhibits better common-mode noise rejection and is obtained by driving both true and complement clock lines with a differential driver, as shown in Figure (a). Single-ended operation is achieved as either falling-edge-active or rising-edge-active, as shown in Figures (b) and (c), respectively. VBB is designed to drive clock input only and is not intended to be used for any other purpose.



(a) Differential Mode **(b) Falling-Edge-Active Single-Ended Mode** **(c) Rising-Edge-Active Single-Ended Mode**

2768 drw 11

ORDERING INFORMATION



2768 drw 12

Integrated Device Technology, Inc.

SELF-TIMED BiCMOS ECL STATIC RAM 64K (16K x 4-BIT) STRAM

PRELIMINARY
IDT10496RL
IDT100496RL
IDT101496RL

FEATURES:

- 16,384-words x 4-bit organization
- Self-Timed, with registers on inputs and latches on outputs
- Balanced Read/Write cycle time: 10/12/15 ns
- Access time: 10/12/15 ns (max.)
- Fully compatible with ECL logic levels
- Through-hole DIP and surface-mount packages

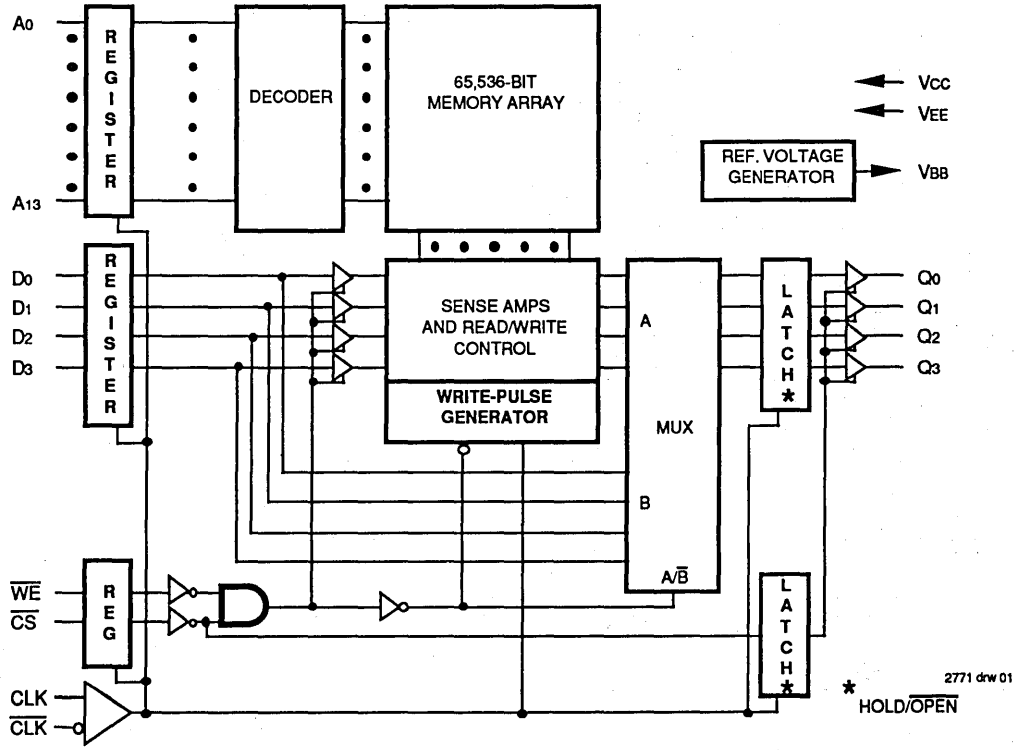
DESCRIPTION:

The IDT10496RL, IDT100496RL and IDT101496RL are 65,536-bit high-speed BiCEMOS™ ECL static random access memories organized as 16K x 4, with inputs and outputs fully compatible with ECL levels. Clocked registers on inputs and latches on outputs, and the self-timed write operation, provide enhanced system performance over conventional RAMs, providing easier design and improved system level cycle times.

Inputs are captured by the leading edge of an externally supplied differential clock. The small input valid window required means more margin for system skews. Logic-to-memory propagation delay is included in device cycle time calculation, allowing this device to deliver better system performance than asynchronous SRAMs and glue logic.

Write timing is controlled internally based on the clock. Write Enable has no special requirements. The device allows balanced read and write cycle times, and reads and writes can be inserted in any order.

FUNCTIONAL BLOCK DIAGRAM



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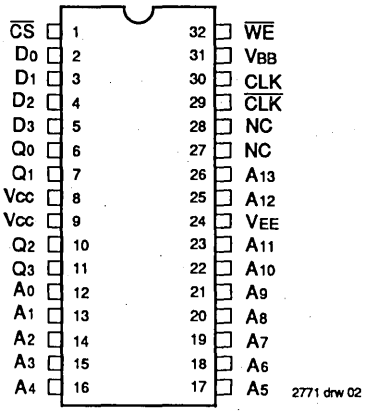
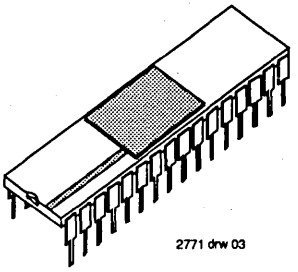
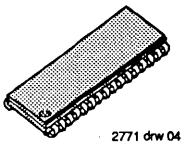
PIN CONFIGURATION



TOP VIEW



400-Mil-Wide
CERAMIC PACKAGE
C32



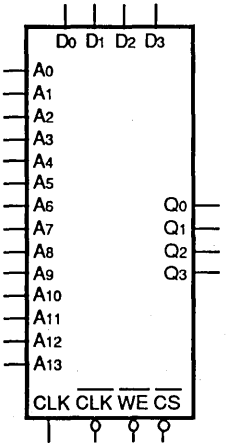
300-Mil-Wide
PLASTIC SOJ PACKAGE
Y32

PIN DESCRIPTION

Symbol	Pin Name
A0 through A13	Address Inputs
D0 through D3	Data Inputs
Q0 through Q3	Data Outputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input (Internal pull down)
CLK, $\overline{CLK}$	Differential Clock Inputs
VBB	Reference Voltage Output (≈1.32V)
VEE	More Negative Supply Voltage
VCC	Less Negative Supply Voltage
NC	No Connect - not internally bonded

2771 tbl 01

LOGIC SYMBOL



16Kx4
STRAM

2771 drw 05

AC OPERATING RANGES(1)

I/O	VEE	Temperature
10K	-5.2V ±5%	0 TO 75°C, air flow exceeding 2 m/sec
100K	-4.5V ±5%	0 TO 85°C, air flow exceeding 2 m/sec
101K	-4.75V to -5.46V	0 TO 75°C, air flow exceeding 2 m/sec

2764 tbl 02

NOTE:
1. Referenced to VCC

CAPACITANCE (TA=+25°C, f=1.0MHz)

Symbol	Parameter	DIP Typ.	DIP Max.	SOJ Typ.	SOJ Max.	Unit
CINCLK	Input Capacitance CLK/$\overline{CLK}$	6	–	3	–	pF
CIN	Input Capacitance except CLK/$\overline{CLK}$	4	–	3	–	pF
COUT	Output Capacitance	6	–	3	–	pF

2773 tbl 03

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	CLK	DataOUT(2)	Function
H	X	↑	L	Deselected
L	H	↑	RAM Data	Read
L	L	↑	WRITE Data	Write

2773 tbl 04

NOTES:
1. H=High, L=Low, X=Don't Care
2. DATAOUT initiated by falling edge of CLK.

ECL-10K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2771 tbl 05

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-10K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L =50Ω to -2.0V, T_A = 0 to +75°C for DIP, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit	T_A
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs[2]		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs[2]		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA	–
			Others	–	–	110	µA	–
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA	–
			Others	-50	–	90	µA	–
I_{EE}	Supply Current	All Inputs and Outputs Open[2]		-260	-200	–	mA	–

2771 tbl 06

NOTES:
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.
2. Except CLK and $\overline{CLK}$, one of which is tied low and one is tied high.

5

ECL-100K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +85	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2771 tbl 07

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-100K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.5V, R_L =50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs[2]		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs[2]		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open[2]		-240	-180	–	mA

2771 tbl 08

NOTES:

1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.
2. Except CLK and $\overline{CLK}$, one of which is tied low and one is tied high.

ECL-101K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2771 tbl 09

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-101K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L =50Ω to -2.0V, T_A = 0 to +75°C for DIP, air flow exceeding 2 m/sec)

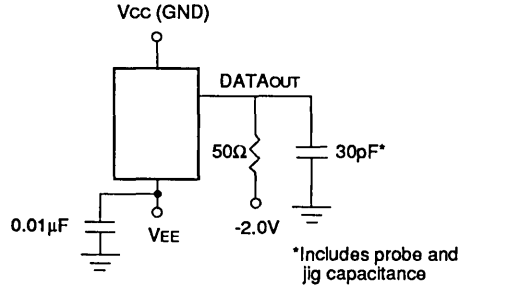
Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs[2]		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs[2]		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open[2]		-260	-200	–	mA

2771 tbl 10

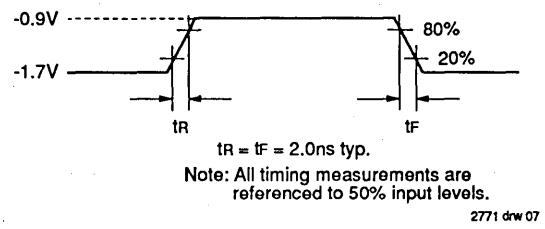
NOTES:

1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.
2. Except CLK and $\overline{CLK}$, one of which is tied low and one is tied high.

AC TEST LOAD CONDITION



AC TEST INPUT PULSE



RISE/FALL TIME

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
tR	Output Rise Time	–	–	2	–	ns
tF	Output Fall Time	–	–	2	–	ns

2771 tbl 11

FUNCTIONAL DESCRIPTION

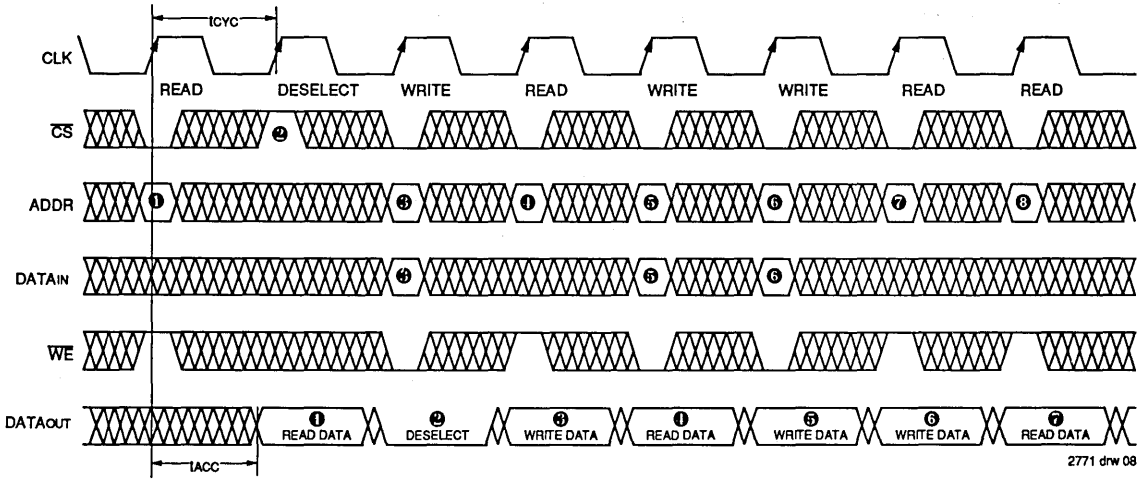
The IDT10496RL, IDT100496RL and IDT101496RL Self-Timed BiCMOS ECL static RAMs (STRAM) provide high speed with low power dissipation typical of BiCMOS ECL. On-chip logic additionally helps improve system performance. The ECL-101K meets electrical specifications that combine the ECL-100K temperature and voltage compensated output levels with the high-speed of ECL-10K VEE compatibility (-5.2V).

As can be seen in the Functional Block Diagram on the title page, this device contains clocked input registers to sample and hold addresses, input data, and control status. Inputs are sampled on the rising edge of the clock (CLK) input (falling edge of $\overline{CLK}$). In the case of a write cycle, the memory cell is written during the clock-high time, and write data conducted to the outputs. Output data flows out the output latch and is held into the next cycle.

READ TIMING

In a typical read cycle, the read address is captured by the rising edge of clock, as at ❶ below. Then, when clock goes low, the read data for the read address clocked in at ❶ is gated through the output latch to the output pins. There is a short delay from falling clock to output ready, called tDR (see Read Cycle Timing). If the clock-high time (tWH) is shorter than the inherent access-time of the cell, output is guaranteed valid after the specified tACC. But if tWH is longer than the cell access-time, output data will be valid tDR after clock goes low. Thus, the time it takes from clock-to-output for any given

FUNCTIONAL DESCRIPTION TIMING EXAMPLE



address (the latency, or t_{ACC}) is

$$t_{ACC} = t_{ACC} \text{ or } (t_{WH} + t_{DR}),$$

whichever is larger.

The output latch takes some time to change state for the next cycle, but this time is very short. Therefore, data hold time from clock low (t_{DH}) is specified as zero minimum hold time.

DESELECT TIMING

Because the outputs are latched, they will continue to drive the output pins until a disable state is clocked through the device. The deselected state is achieved by de-asserting chip select ($\overline{CS}$ high) at rising edge of clock. This case occurs at ❷ below. Outputs then attain the disable state (low) t_{ACC} later. Status of other inputs do not effect the disabling of the device when chip select is de-asserted with the proper relation to clock.

WRITE TIMING

Write cycles are identical to read cycles, except that write enable and write data need also be supplied, with the appropriate setup and hold timing. The device has on-chip timing that handles all aspects of writing data into the addressed RAM cell without the need for external write-pulse generation. The timing logic uses the clock-high time as the write pulse, and thus determines the minimum clock-high time, t_{WH}.

In addition to writing to the RAM cell, the write data is fed to the output register by a multiplexer, so that write data is available on the output pins in the appropriate time slot (i.e. after $t_{WH} + t_{DR}$). This function is sometimes called "Transparent Write," and is useful for write-through cache applications. Thus the input data sampled at ❽ is available on the output at the end of the cycle.

There are no restrictions on the order of read cycles and write cycles.

5

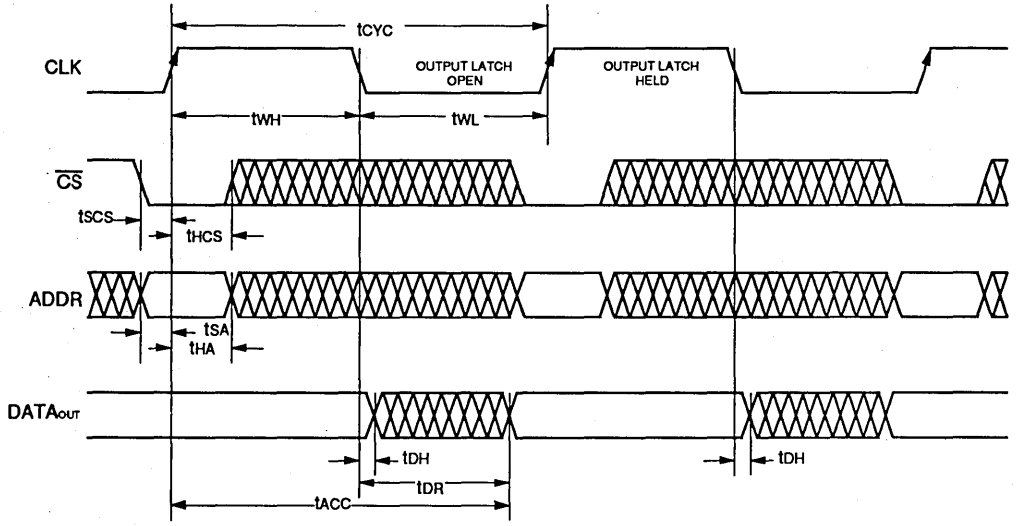
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10496RL10 100496RL10 101496RL10		10496RL12 100496RL12 101496RL12		10496RL15 100496RL15 101496RL15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle									
tCYC	Cycle Time	–	10	–	12	–	15	–	ns
tACC[2]	Access Time from Clock High	–	–	10	–	12	–	15	ns
tWL	Clock Low Pulse Width	–	5	–	5	–	6	–	ns
tWH	Clock High Pulse Width	–	5	–	5	–	6	–	ns
tSCS	Setup Time for Chip Select	–	1	–	1	–	1	–	ns
tSA	Setup Time for Address	–	1	–	1	–	1	–	ns
tHCS	Hold Time for Chip Select	–	2	–	2.5	–	2.5	–	ns
tHA	Hold Time for Address	–	2	–	2.5	–	2.5	–	ns
tDH	Data Hold from Clock Low	–	2	–	2	–	2	–	ns
tDR	Data Ready from Clock Low	–	0	5	0	5	0	5	ns

2771 tbl 11

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. Access time is the larger of tACC or tWH + tDR.

READ CYCLE TIMING DIAGRAM



2771 drw 09

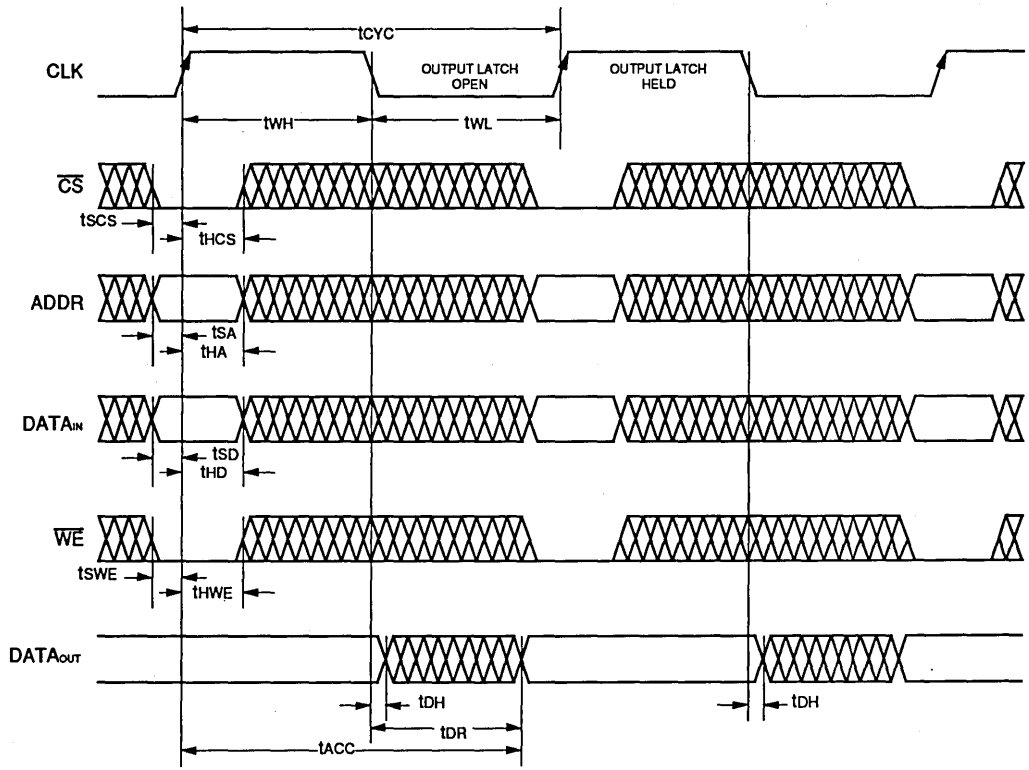
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10496RL10 100496RL10 101496RL10		10496RL12 100496RL12 101496RL12		10496RL15 100496RL15 101496RL15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle[2]									
tSWE	Setup Time for Write Enable	–	1	–	1	–	1	–	ns
tSD	Setup Time for Data In	–	1	–	1	–	1	–	ns
tHWE	Hold Time for Write Enable	–	2	–	2.5	–	2.5	–	ns
tHD	Hold Time for Data In	–	2	–	2.5	–	2.5	–	ns

2771 tbl 12

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. All Setup, Hold, and Access timing are the same as the Read Cycle with the addition of above requirements. Write Data appears on output pins after falling edge of clock.

WRITE CYCLE TIMING DIAGRAM

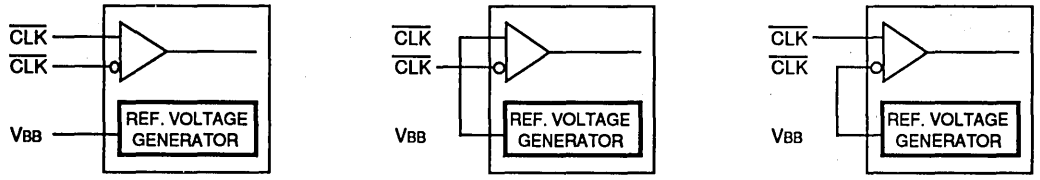


2771 drw 10

5

CLOCK INPUT

The clock input circuit has been designed to accomodate both single-ended and differential mode operation. Differential mode exhibits better common-mode noise rejection and is obtained by driving both true and complement clock lines with a differential driver, as shown in Figure (a). Single-ended operation is achieved as either falling-edge-active or rising-edge-active, as shown in Figures (b) and (c), respectively. VBB is designed to drive clock input only and is not intended to be used for any other purpose.



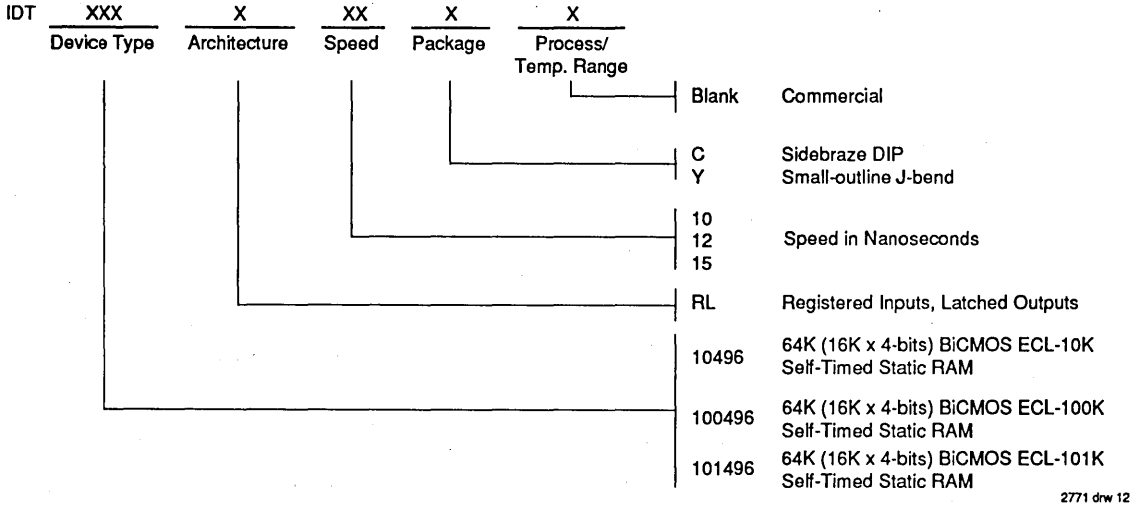
(a) Differential Mode

(b) Falling-Edge-Active Single-Ended Mode

(c) Rising-Edge-Active Single-Ended Mode

2771 drw 11

ORDERING INFORMATION



2771 drw 12

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 64K (16K x 4-BIT) with SYNCHRONOUS WRITE

ADVANCE INFORMATION
IDT10497
IDT100497
IDT101497

FEATURES:

- 16,384-words x 4-bit organization
- Address access time: 12/15 ns
- Read Data output latch for extended hold time
- Short Write Cycle input data and address valid time
- Pin compatible with standard 16K x 4
- Through-hole DIP and surface-mount packages

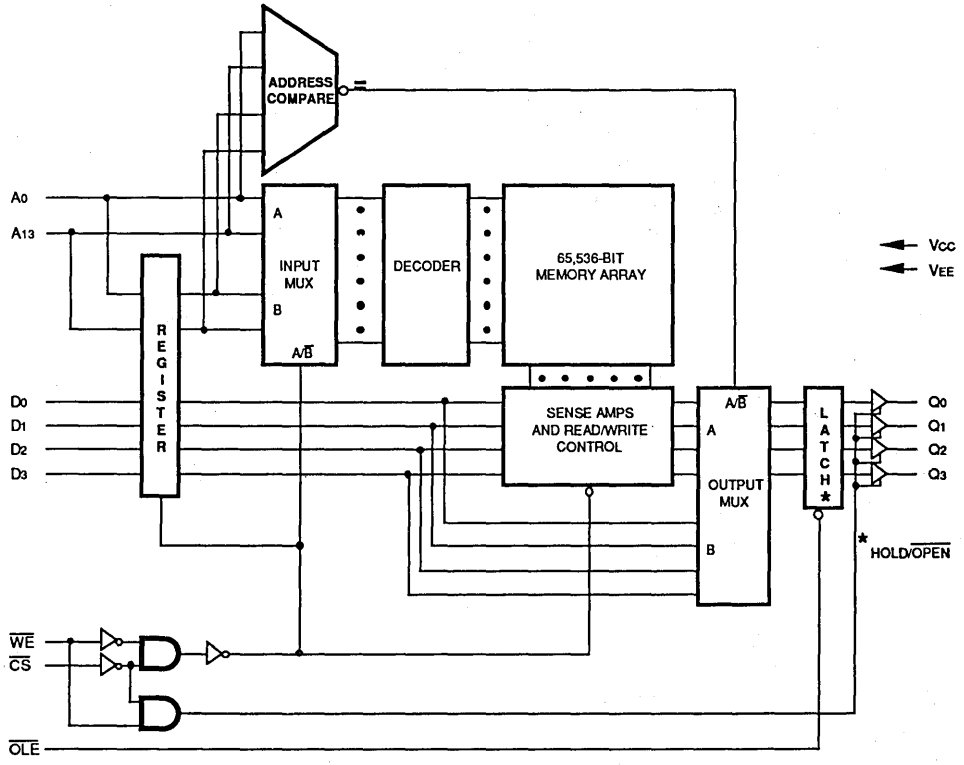
DESCRIPTION:

The IDT10497, IDT100497 and IDT101497 are 65,536-bit high-speed BiCEMOS™ ECL static random access memories organized as 16K x 4, with inputs and outputs fully compatible with ECL levels. Internal registers on inputs provide enhanced Write Cycle performance over conventional RAMs, while output read data latch allows longer output data hold time providing easier design and improved system level cycle times.

In the read mode, this device is pinout and timing compatible with the standard asynchronous SRAMs (IDT10494), yet the addition of an output latch with separate enable control allow output data to be captured and held long into the next cycle. This minimizes noise on the data bus and provides better set-up time margin for the next logic stage in pipelined applications.

In the write mode, the device adds an invisible pipeline stage in the write address and data paths, allowing very short set-up and hold times for these inputs and less stringent requirements for the write pulse input.

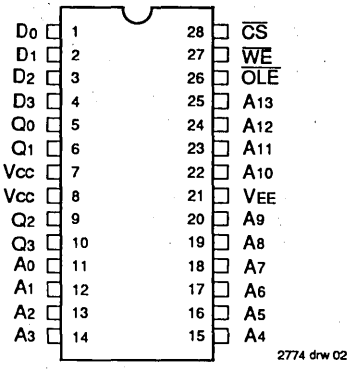
FUNCTIONAL BLOCK DIAGRAM



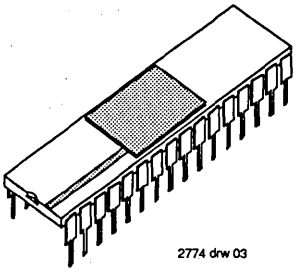
2774 drw 01

BiCEMOS is a trademark of Integrated Device Technology, Inc.

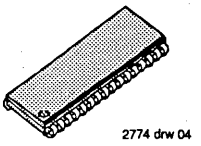
PIN CONFIGURATION



TOP VIEW



400-Mil-Wide
CERAMIC PACKAGE
C32



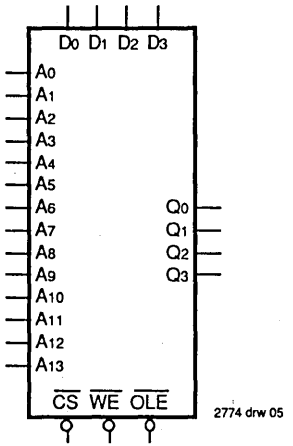
300-Mil-Wide
PLASTIC SOJ PACKAGE
732

PIN DESCRIPTIONS

Symbol	Pin Name
A0 through A13	Address Inputs
D0 through D3	Data Inputs
Q0 through Q3	Data Outputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input (Internal pull down)
$\overline{OLE}$	Output Latch Enable
VEE	More Negative Supply Voltage
VCC	Less Negative Supply Voltage

2774 tbl 01

LOGIC SYMBOL



16Kx4
SRAM

AC OPERATING RANGES(1)

I/O	VEE	Temperature
10K	-5.2V ±5%	0 TO 75°C, air flow exceeding 2 m/sec
100K	-4.5V ±5%	0 TO 85°C, air flow exceeding 2 m/sec
101K	-4.75V to -5.46V	0 TO 75°C, air flow exceeding 2 m/sec

2774 tbl 02

NOTE:
1. Referenced to Vcc

CAPACITANCE (TA=+25°C, f=1.0MHz)

Symbol	Parameter	DIP Typ.	DIP Max.	SOJ Typ.	SOJ Max.	Unit
CIN	Input Capacitance	4	–	3	–	pF
COUT	Output Capacitance	6	–	3	–	pF

2774 tbl 03

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	$\overline{OLE}$	DataOUT(2)	Function
H	X	X	L	Deselected
L	H	L	RAM Data	Read
L	H	H	RAM Data	Output Held
L	L	X	L	Write

2774 tbl 04

NOTES:
1. H=High, L=Low, X=Don't Care
2. DATAOUT initiated by falling edge of $\overline{OLE}$.

ECL-10K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2774 tbl 05

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-10K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L=50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit	T_A
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	V_{IN} = V_{IHB} or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	V_{IN} = V_{IHB} or V_{ILA}		– – –	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	V_{IN} = V_{IHA}	$\overline{CS}$	–	–	220	µA	–
			Others	–	–	110	µA	–
I_{IL}	Input LOW Current	V_{IN} = V_{ILB}	$\overline{CS}$	0.5	–	170	µA	–
			Others	-50	–	90	µA	–
I_{EE}	Supply Current	All Inputs and Outputs Open		-260	-200	–	mA	–

2774 tbl 06

NOTES:

1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

ECL-100K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to + 85	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
P_T	Power Dissipation		1.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

NOTE: 2774 tbl 07

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-100K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.5V, R_L =50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-240	-180	–	mA

NOTE: 2774 tbl 08

1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.

ECL-101K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2774 tbl 09

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-101K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L =50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

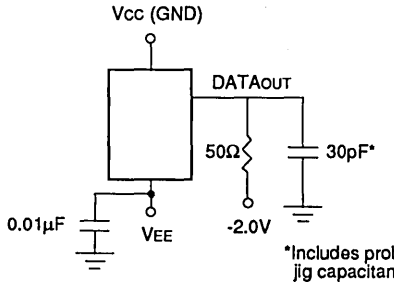
Symbol	Parameter	Test Condition		Min. (B)	Typ.(1)	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-260	-200	–	mA

2774 tbl 10

NOTE:

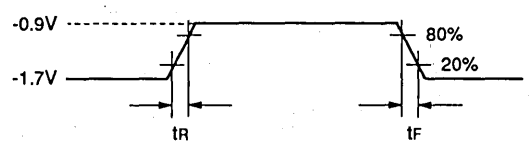
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

AC TEST LOAD CONDITION



2774 drw 06

AC TEST INPUT PULSE



tR = tF = 2.0ns typ.

Note: All timing measurements are referenced to 50% input levels.

2774 drw 07

RISE/FALL TIME

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_R	Output Rise Time	–	–	2	–	ns
t_F	Output Fall Time	–	–	2	–	ns

2774 tbl 11

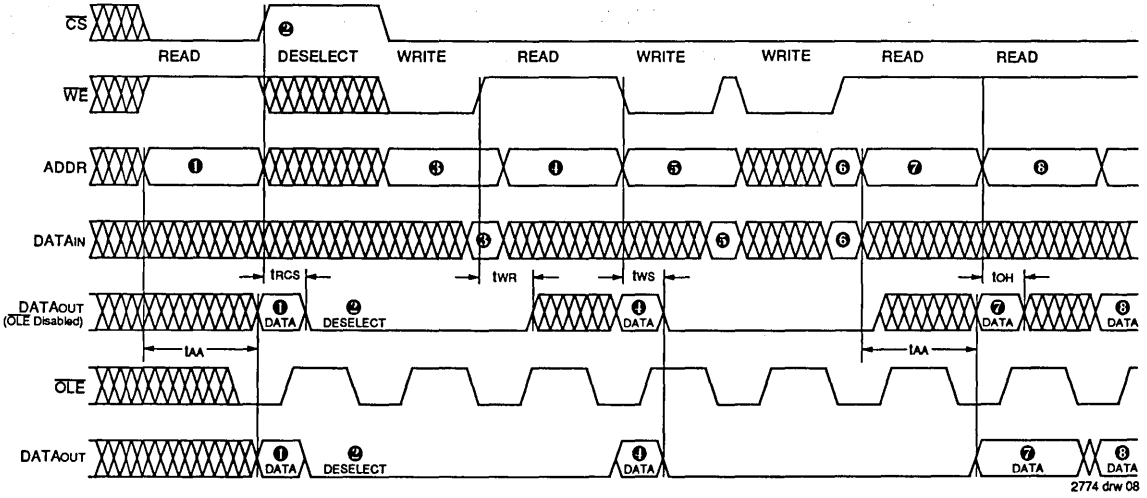
FUNCTIONAL DESCRIPTION

The IDT10497. IDT100497, and IDT101497 BiCMOS ECL static RAMs (SRAM) with SYNCHRONOUS WRITE provide high speed with low power dissipation typical of BiCMOS ECL. On-chip logic additionally helps improve system performance, yet the device is pinout-compatible with asynchronous equivalents (i.e... IDT10494, IDT100494, and IDT101494 respectively). The ECL-101K meets electrical specifications that combine the ECL-100K temperature and voltage compensated output levels with the high-speed of ECL-10K VEE compatibility (-5.2V).

As can be seen in the Functional Block Diagram on the title page, this device contains clocked input registers to sample and hold addresses and input data, during a write cycle only. Inputs are sampled on the rising edge of the Write Enable ($\overline{WE}$). The write cycle is pipelined: the memory cell is written during the $\overline{WE}$-low time in the next cycle.

Read cycles are not pipelined and operate identically to an asynchronous device, except that an output latch is provided to capture and hold Read data.

FUNCTIONAL DESCRIPTION TIMING EXAMPLE



2774 drw 08

READ TIMING

The read timing on the device is asynchronous. DataOUT is held low until the device is selected by Chip Select ($\overline{CS}$). Then Address (ADDR) settles and data appears on the output after time t_{AA}, as at ❶ below.

DataOUT is held for a short time (t_{OH}) after the address begins to change for the next access, as can be seen at ❼ — allowing addresses to begin to change early for the next cycle — then ambiguous data is on the bus until a new time t_{AA}.

To avoid this noise on the bus and provide for longer output hold time, this device includes an output Read data latch which allows Read data to flow out while Output Latch Enable ($\overline{OLE}$) is low, and then hold when $\overline{OLE}$ is high. Thus in the example below Read data at ❼ is held until Read data at ❽ is ready for output.

Note that DataOUT is disabled (held low) by $\overline{CS}$ high or $\overline{WE}$ low, regardless of the state of the Output Latch.

DESELECT TIMING

Deselect timing is identical to a standard asynchronous device. This case occurs at ❷ below. Outputs attain the disable state (low) t_{RCS} later Chip Select ($\overline{CS}$) is taken to a high logic state. Status of other inputs do not effect the disabling of the device when chip select is de-asserted.

WRITE TIMING

Write cycles pipelined to allow easier design and higher system performance. The write pulse created on the $\overline{WE}$ input is used as a strobe to clock in the Write Address and Data into a register. This address and data are held in the register until the next write cycle, when they are used to write into the memory array through the Input Multiplexor.

Note the very short valid window required for Write Address and Data inputs. This is because these signals are captured by the input register. This means that input data may arrive late in the cycle, as at ❸ below, or data and address may arrive late, as at ❻ below.

DataOUT is disabled during the Write Cycle. If $\overline{CS}$ is held low (active) and addresses remain unchanged, the DataOUT pins will output the written data after "Write Recovery Time" (t_{WR}), as for a standard asynchronous device.

There is a special case when a Read cycle follows directly a Write Cycle to the same address. The memory array has not yet been updated with the Write data — it is still in the input register. This case is handled by including an address comparator and Output Multiplexor on the device: if the address being presented on the input pins is the same as the address stored in the input register, the data presented to the output pins is also from the input register.

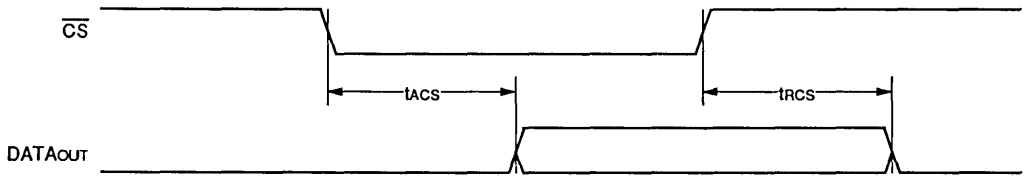
5

AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

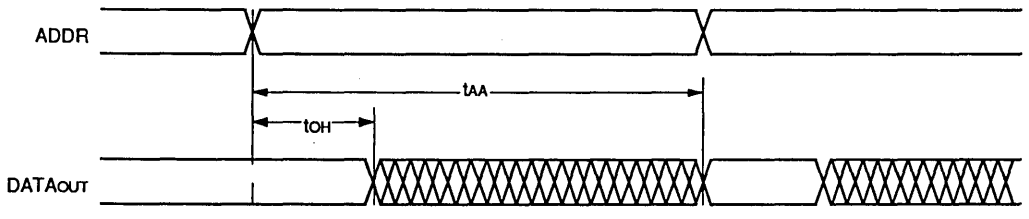
Symbol	Parameter[1]	Test Condition	10497S12 100497S12 101497S12		10497S15 100497S15 101497S15		Unit
			Min.	Max.	Min.	Max.	
Read Cycle							
t_{AA}[2]	Address Access Time	–	–	12	–	15	ns
t_{ACS}	Chip Select Access Time	–	–	5	–	5	ns
t_{RCS}	Chip Select Recovery Time	–	–	5	–	5	ns
t_{OH}	Data Hold from Address Change	–	3	–	3	–	ns
t_{OLEL}	Latch Enable Low Pulse Width	–	5	–	5	–	ns
t_{AHO}	Address Valid to $\overline{OLE}$ High	–	14	–	17	–	ns
t_{DH}	Data Hold from Clock Low	–	0	–	0	–	ns
t_{DR}	Data Ready from Clock Low	–	0	4	0	4	ns

NOTES: 2774 tbl 12
1. Input and Output reference level is 50% point of waveform.
2. Read Data is valid at t_{AA} or t_{AHO} - t_{OLEL} + t_{DR}, whichever is larger; that is, Read Data is valid at the access time unless Output Latch Enable is high, and then access is t_{DR} after $\overline{OLE}$ goes low.

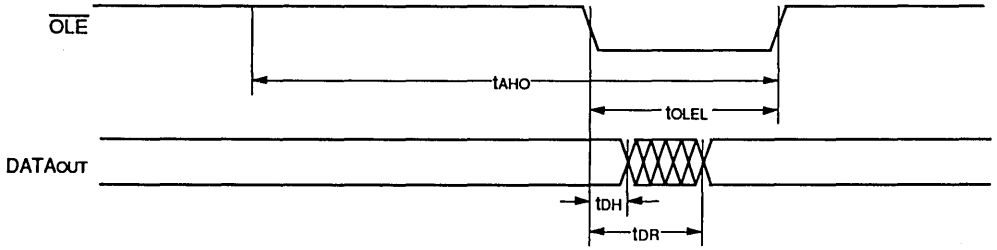
READ CYCLE GATED BY CHIP SELECT



READ CYCLE GATED BY ADDRESS



OUTPUT LATCH TIMING



2774 drw 09

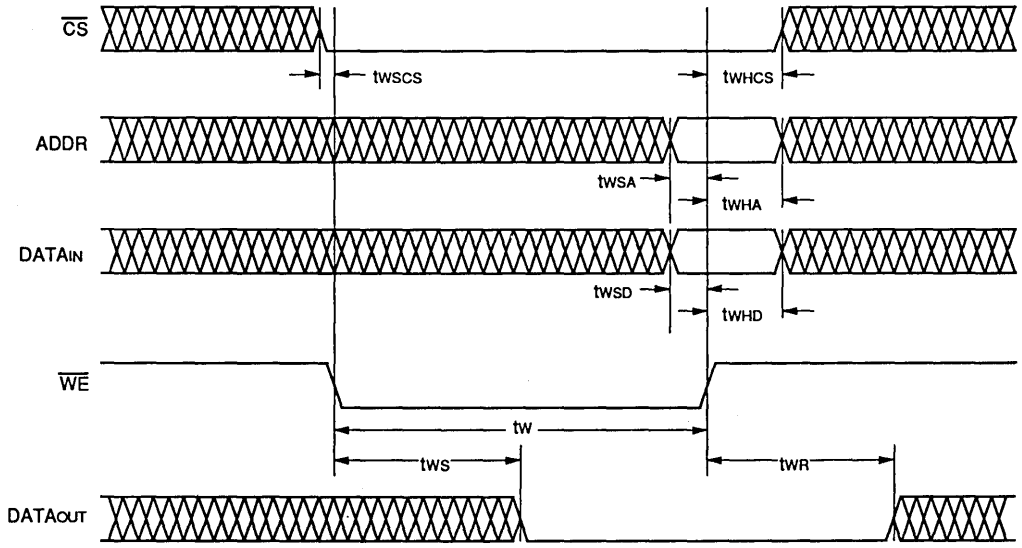
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10497S12 100497S12 101497S12		10497S15 100497S15 101497S15		Unit
			Min.	Max.	Min.	Max.	
Write Cycle							
tW	Write Pulse Width	–	10	–	12	–	ns
tWSCS	Setup Time for Chip Select	–	0	–	1	–	ns
tWSA	Setup Time for Address	–	1	–	1	–	ns
tWSD	Setup Time for Data In	–	1	–	1	–	ns
tWHCS	Hold Time for Chip Select	–	2	–	2	–	ns
tWHA	Hold Time for Address	–	2	–	2	–	ns
tWHD	Hold Time for Data In	–	2	–	2	–	ns
tWS	Write Disable Time	–	–	5	–	5	ns
tWR	Write Recovery Time	–	–	5	–	5	ns

NOTE:
1. Input and Output reference level is 50% point of waveform.

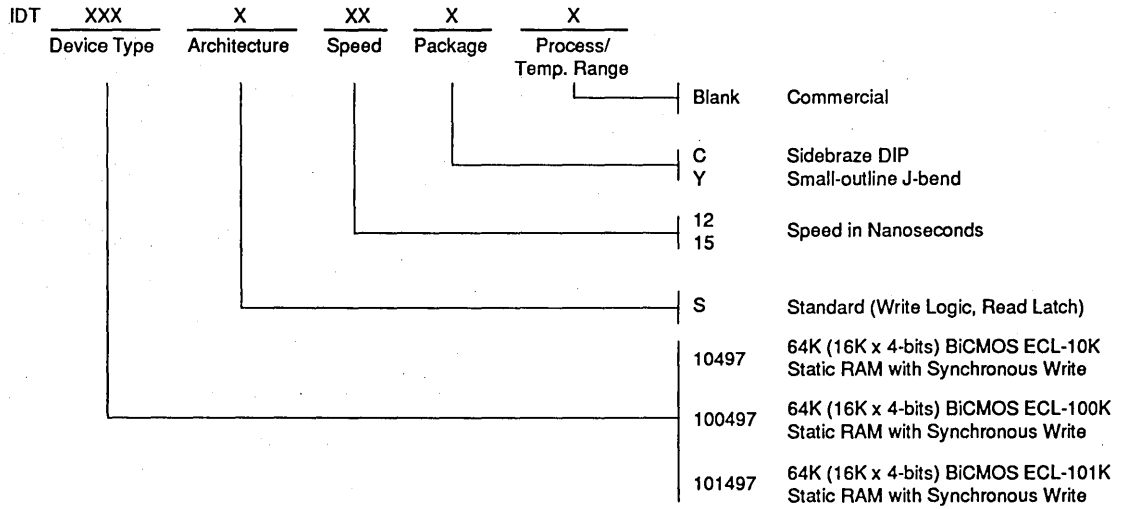
2774 tbl 13

WRITE CYCLE TIMING DIAGRAM



2774 drw 10

ORDERING INFORMATION



2774 drw 11

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 64K (16K x 4-BIT) with CONDITIONAL WRITE

ADVANCE INFORMATION
IDT10498
IDT100498
IDT101498

FEATURES:

- 16,384-words x 4-bit organization
- Address access time: 12/15ns
- Read Data output latch for extended hold time
- Short Write Cycle input data and address valid time
- Write Cycle may be terminated very late in the cycle
- Pin compatible with standard 16K x 4
- Through-hole DIP and surface-mount packages

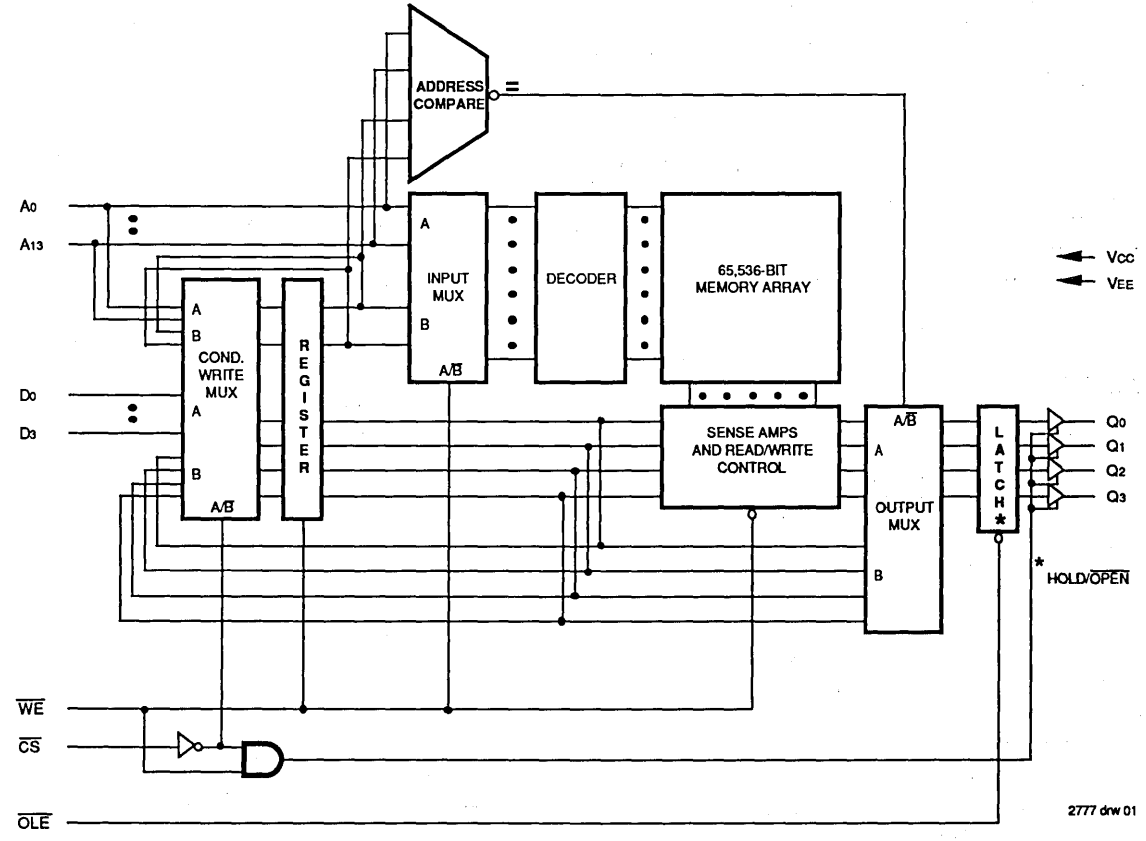
DESCRIPTION:

The IDT10498, IDT100498 and IDT101498 are 65,536-bit high-speed BiCEMOS™ ECL static random access memories organized as 16K x 4, with inputs and outputs fully compatible with ECL levels. Internal registers on inputs provide enhanced Write Cycle performance over conventional RAMs, while output read data latch allows longer output data hold time providing easier design and improved system level cycle times.

In the read mode, this device is pinout and timing compatible with the standard asynchronous SRAMs (IDT10494), yet the addition of an output latch with separate enable control allow output data to be captured and held long into the next cycle. This minimizes noise on the data bus and provides better set-up time margin for the next logic stage in pipelined applications.

In the write mode, the device adds an invisible pipeline stage in the write address and data paths, allowing very short set-up and hold times for these inputs and less stringent requirements for the write pulse input. Additionally, the address and data paths to the input register are gated by the Conditional Write Multiplexor, which allows termination of a Write cycle late in the cycle.

FUNCTIONAL BLOCK DIAGRAM



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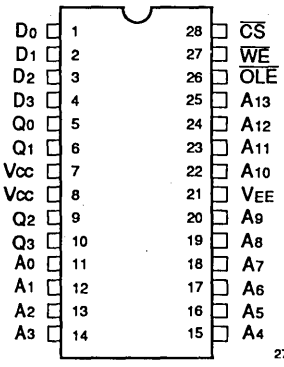
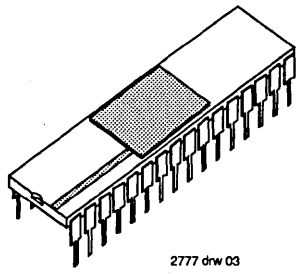
PIN CONFIGURATION



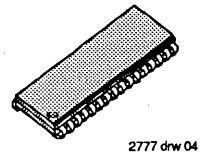
TOP VIEW

2777 drw 02



2777 drw 03

400-Mil-Wide
CERAMIC PACKAGE
C32



2777 drw 04

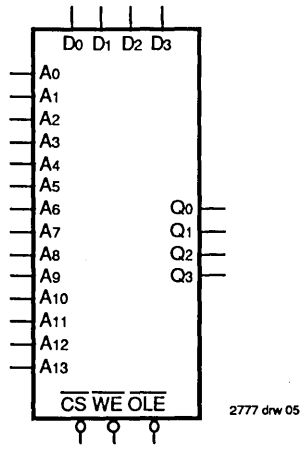
300-Mil-Wide
PLASTIC SOJ PACKAGE
Y32

PIN DESCRIPTIONS

Symbol	Pin Name
A_0 through A_{13}	Address Inputs
D_0 through D_3	Data Inputs
Q_0 through Q_3	Data Outputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input (Internal pull down)
$\overline{OLE}$	Output Latch Enable
V_{EE}	More Negative Supply Voltage
V_{CC}	Less Negative Supply Voltage

2777 tbl 01

LOGIC SYMBOL



2777 drw 05

16Kx4
SRAM

AC OPERATING RANGES[1]

I/O	V_{EE}	Temperature
10K	-5.2V ±5%	0 TO 75°C, air flow exceeding 2 m/sed
100K	-4.5V ±5%	0 TO 85°C, air flow exceeding 2 m/sed
101K	-4.75V to -5.46V	0 TO 75°C, air flow exceeding 2 m/sed

2777 tbl 02

NOTE:
1. Referenced to Vcc

CAPACITANCE (T_A=+25°C, f=1.0MHz)

Symbol	Parameter	DIP Typ.	DIP Max.	SOJ Typ.	SOJ Max.	Unit
C_{IN}	Input Capacitance	4	–	3	–	pF
C_{OUT}	Output Capacitance	6	–	3	–	pF

2777 tbl 03

TRUTH TABLE[1]

$\overline{CS}$	$\overline{WE}$	$\overline{OLE}$	Data $_{OUT}$ [2]	Function
H	X	X	L	Deselected
L	H	L	RAM Data	Read
L	H	H	RAM Data	Output Held
L	L	X	L	Write

2777 tbl 04

NOTES:
1. H=High, L=Low, X=Don't Care
2. $DATA_{OUT}$ initiated by falling edge of $\overline{OLE}$.

ECL-10K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2777 tbl 05

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions

ECL-10K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L =50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit	T_A
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA	–
			Others	–	–	110	µA	–
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA	–
			Others	-50	–	90	µA	–
I_{EE}	Supply Current	All Inputs and Outputs Open		-260	-200	–	mA	–

2777 tbl 06

NOTE:
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

ECL-100K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to + 85	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2777 tbl 07

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-100K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.5V, R_L =50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-240	-180	–	mA

2777 tbl 08

NOTE:

1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.

ECL-101K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2778 tbl 09

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-101K DC ELECTRICAL CHARACTERISTICS

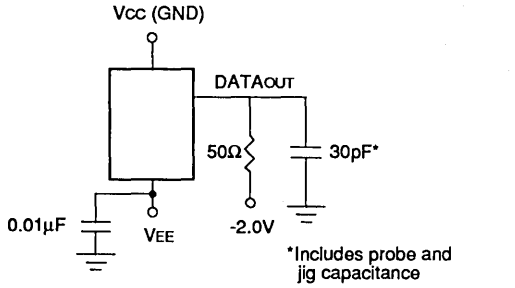
(V_{EE} = -5.2V, R_L =50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Condition		Min. (B)	Typ.[1]	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-260	-200	–	mA

2778 tbl 10

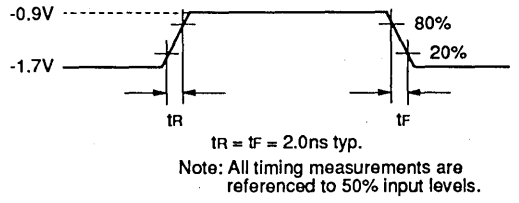
NOTE:
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

AC TEST LOAD CONDITION



2779 drw 06

AC TEST INPUT PULSE



2779 drw 07

RISE/FALL TIME

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_R	Output Rise Time	–	–	2	–	ns
t_F	Output Fall Time	–	–	2	–	ns

2779 tbl 11

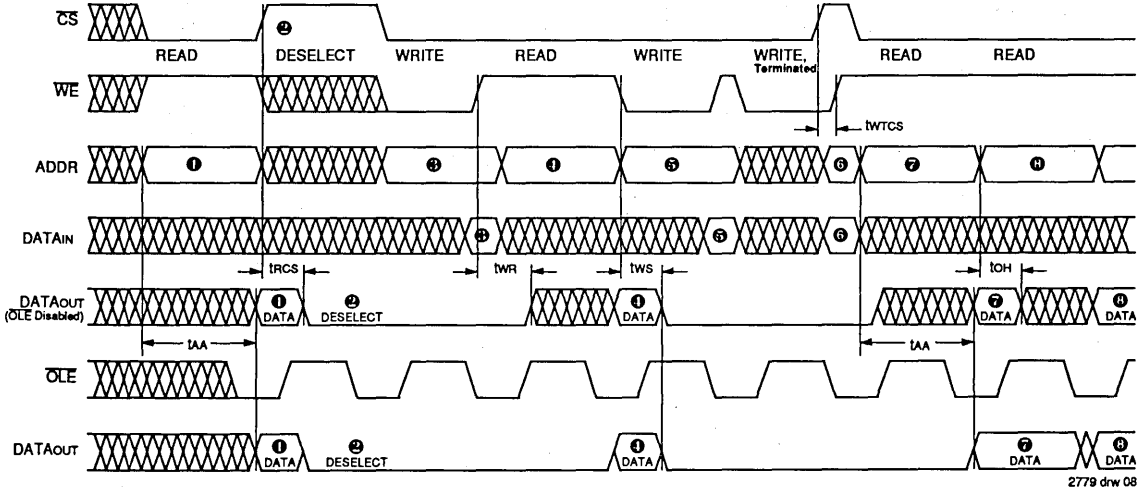
FUNCTIONAL DESCRIPTION

The IDT10498, IDT100498, and IDT101498 BiCMOS ECL static RAMs (SRAM) with CONDITIONAL WRITE provide high speed with low power dissipation typical of BiCMOS ECL. On-chip logic additionally helps improve system performance, yet the device is pinout-compatible with asynchronous equivalents (i.e... IDT10494, IDT100494, and IDT101494 respectively). The ECL-101K meets electrical specifications that combine the ECL-100K temperature and voltage compensated output levels with the high-speed of ECL-10K VEE compatibility (-5.2V).

As can be seen in the Functional Block Diagram on the title page, this device contains clocked input registers to sample and hold addresses and input data, during a write cycle only. Inputs are sampled on the rising edge of the Write Enable ($\overline{WE}$). The write cycle is pipelined: the memory cell is written during the $\overline{WE}$-low time in the next cycle. Additionally, the address and data paths to the input register are gated by the Conditional Write Multiplexor, which allows termination of a Write cycle late in the cycle.

Read cycles are not pipelined and operate identically to an asynchronous device, except that an output latch is provided to capture and hold Read data.

FUNCTIONAL DESCRIPTION TIMING EXAMPLE



2779 drw 08

READ TIMING

The read timing on the device is asynchronous. DataOUT is held low until the device is selected by Chip Select ($\overline{CS}$). Then Address (ADDR) settles and data appears on the output after time t_{AA}, as at ❶ below.

DataOUT is held for a short time (t_{OH}) after the address begins to change for the next access, as can be seen at ❼ — allowing addresses to begin to change early for the next cycle — then ambiguous data is on the bus until a new time t_{AA}.

To avoid this noise on the bus and provide for longer output hold time, this device includes an output Read data latch which allows Read data to flow out while Output Latch Enable ($\overline{OLE}$) is low, and then hold when $\overline{OLE}$ is high. Thus in the example below Read data at ❼ is held until Read data at ❽ is ready for output.

Note that DataOUT is disabled (held low) by $\overline{CS}$ high or $\overline{WE}$ low, regardless of the state of the Output Latch.

DESELECT TIMING

Deselect timing is identical to a standard asynchronous device. This case occurs at ❷ below. Outputs attain the disable state (low) t_{RCS} later Chip Select ($\overline{CS}$) is taken to a high logic state. Status of other inputs do not effect the disabling of the device when chip select is de-asserted.

WRITE TIMING

Write cycles pipelined to allow easier design and higher system performance. The write pulse created on the $\overline{WE}$ input is used as a strobe to clock in the Write Address and Data into a register. This address and data are held in the register until the next write cycle, when they are used to write into the memory array through the Input Multiplexor.

Note the very short valid window required for Write Address and Data inputs. This is because these signals are captured by the input register. This means that input data may arrive late in the cycle, as at ❸ below, or data and address may arrive late, as at ❻ below.

DataOUT is disabled during the Write Cycle. If $\overline{CS}$ is held low (active) and addresses remain unchanged, the DataOUT pins will output the written data after "Write Recovery Time" (t_{WR}), as for a standard asynchronous device.

There is a special case when a Read cycle follows directly a Write Cycle to the same address. The memory array has not yet been updated with the Write data — it is still in the input register. This case is handled by including an address comparator and Output Multiplexor on the device: if the address being presented on the input pins is the same as the address stored in the input register, the data presented to the output pins is also from the input register.

CONDITIONAL WRITE

In certain system architectures, the decision whether to write data within a cycle occurs late in the cycle. An example might be cache hit logic taking time to decide if a cache line needs to be updated. This device allows a write to be initiated, yet terminated very late in the cycle by using Chip Select should a write not be required by the system.

The Conditional Write Multiplexor controlled by Chip Select makes this possible. In a normal Write cycle, $\overline{CS}$ is low and the Multiplexor delivers the state of the addresses and data on the input pins to the Input Multiplexor and Input Register, respectively. Because $\overline{CS}$ does not gate the Write Pulse logic, it has a short valid window requirement.

To terminate the Write cycle, as shown at ❻ below, all that is required is to bring $\overline{CS}$ to a high logic state. This switches the Conditional Write Multiplexor to circulate the previously written address and data (held in the Input Register) around to be clocked again into the Input Register. No Write cycle is apparent to the system.

5

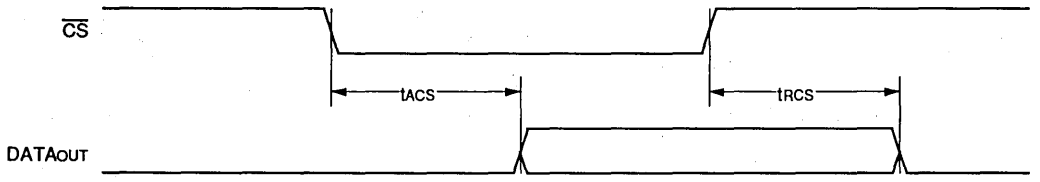
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10498S12 100498S12 101498S12		10498S15 100498S15 101498S15		Unit
			Min.	Max.	Min.	Max.	
Read Cycle							
t_{AA}[2]	Address Access Time	–	–	12	–	15	ns
t_{ACS}	Chip Select Access Time	–	–	5	–	5	ns
t_{RCS}	Chip Select Recovery Time	–	–	5	–	5	ns
t_{OH}	Data Hold from Address Change	–	3	–	3	–	ns
t_{OLEL}	Latch Enable Low Pulse Width	–	5	–	5	–	ns
t_{AHO}	Address Valid to $\overline{OLE}$ High	–	14	–	17	–	ns
t_{DH}	Data Hold from Clock Low	–	0	–	0	–	ns
t_{DR}	Data Ready from Clock Low	–	0	4	0	4	ns

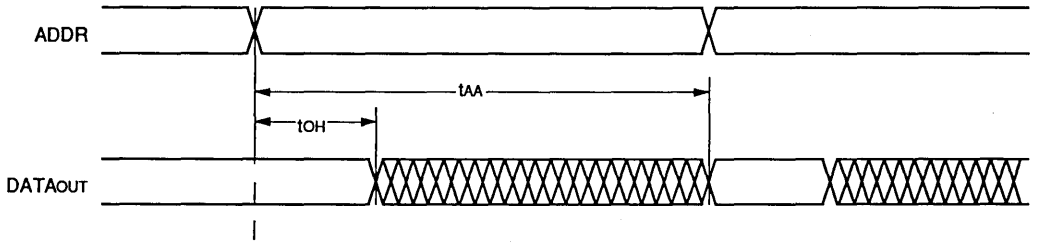
2779 tbl 12

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. Read Data is valid at t_{AA} or t_{AHO} - t_{OLEL} + t_{DR}, whichever is larger; that is, Read Data is valid at the access time unless Output Latch Enable is high, and then access is t_{DR} after $\overline{OLE}$ goes low.

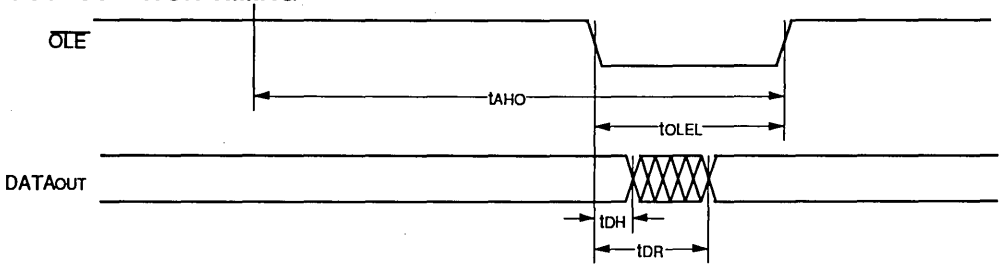
READ CYCLE GATED BY CHIP SELECT



READ CYCLE GATED BY ADDRESS



OUTPUT LATCH TIMING



2779 drw 09

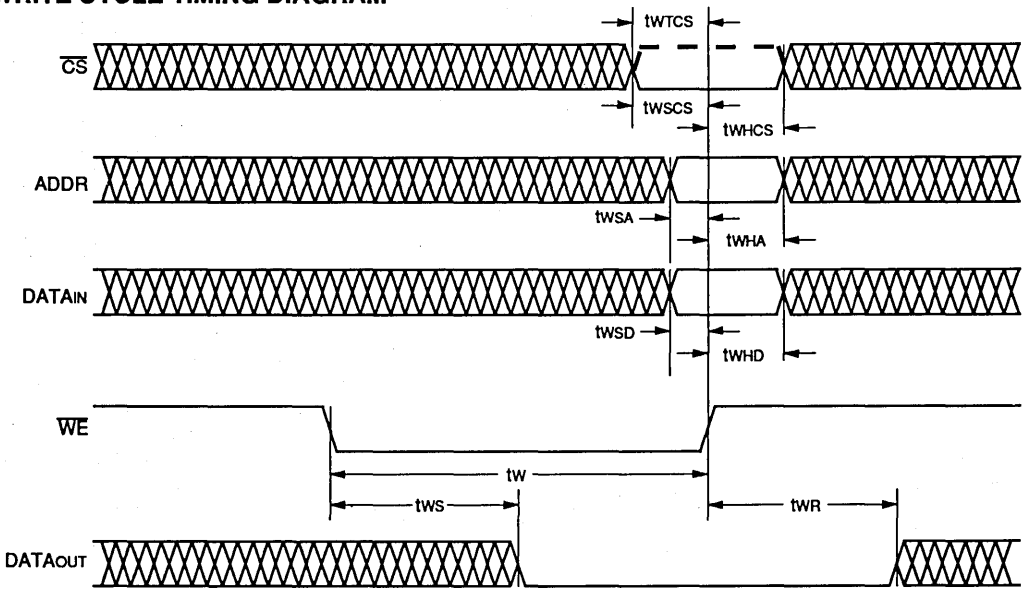
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10498S12 100498S12 101498S12		10498S15 100498S15 101498S15		Unit
			Min.	Max.	Min.	Max.	
Write Cycle							
tW	Write Pulse Width	–	10	–	12	–	ns
tWSCS	Setup Time for Chip Select	–	1	–	1	–	ns
tWTCS	$\overline{CS}$ Set-Up, Terminated Write	–	2	–	2	–	ns
tWSA	Setup Time for Address	–	1	–	1	–	ns
tWSD	Setup Time for Data In	–	1	–	1	–	ns
tWHCS	Hold Time for Chip Select	–	2	–	2	–	ns
tWHA	Hold Time for Address	–	2	–	2	–	ns
tWHD	Hold Time for Data In	–	2	–	2	–	ns
tWS	Write Disable Time	–	–	5	–	5	ns
tWR	Write Recovery Time	–	–	5	–	5	ns

NOTES:
1. Input and Output reference level is 50% point of waveform.

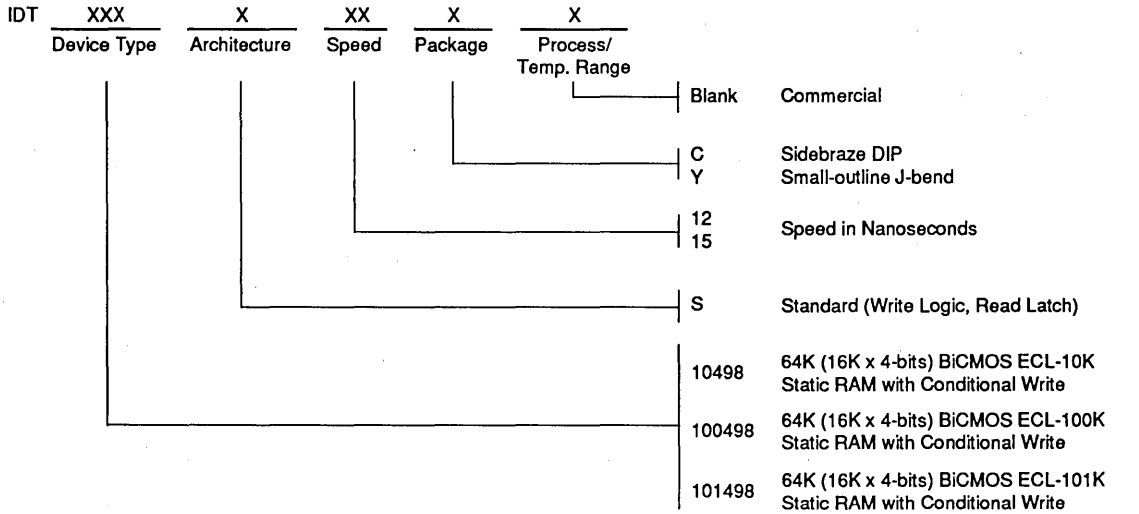
2779 tbl 13

WRITE CYCLE TIMING DIAGRAM



2779 drw 10

ORDERING INFORMATION



2779 drw 11

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 256K (64K x 4-BIT) SRAM

IDT10504
IDT100504
IDT101504

FEATURES:

- 65,536-words x 4-bit organization
- Address access time: 8/10/12/15
- Low power dissipation: 800mW (typ.)
- Guaranteed Output Hold time
- Fully compatible with ECL logic levels
- Separate data input and output
- JEDEC standard through-hole and surface mount packages

DESCRIPTION:

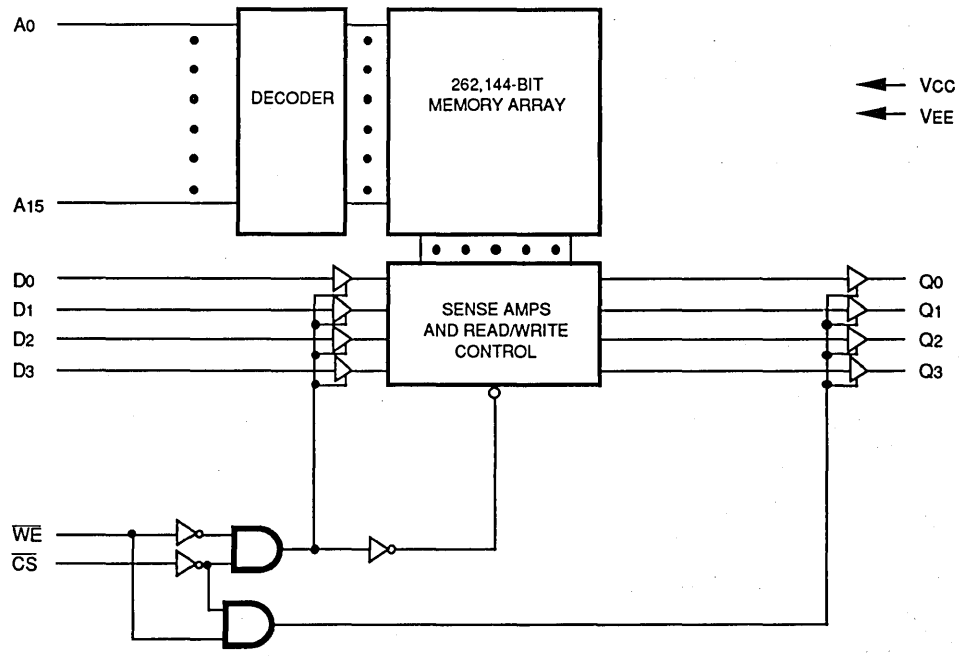
The IDT10504, IDT100504 and IDT101504 are 262,144-bit high-speed BiCEMOS™ ECL static random access memories organized as 64Kx4, with separate data inputs and outputs. All I/Os are fully compatible with ECL levels.

These devices are part of a family of asynchronous four-bit-wide ECL SRAMs. The devices have been configured to follow the standard ECL SRAM family pinout. Because they are manufactured in BiCEMOS™ technology, however, power dissipation is greatly reduced over equivalent bipolar devices.

The asynchronous SRAMs are the most straightforward to use because no additional clocks or controls are required: $Data_{OUT}$ is available an access time after the last change of address. To write data into the device requires the creation of a Write Pulse, and the write cycle disables the output pins in conventional fashion.

The fast access time and guaranteed Output Hold time allow greater margin for system timing variation. $Data_{IN}$ setup time specified with respect to the trailing edge of Write Pulse eases write timing allowing balanced Read and Write cycle times.

FUNCTIONAL BLOCK DIAGRAM



2780 drw 01

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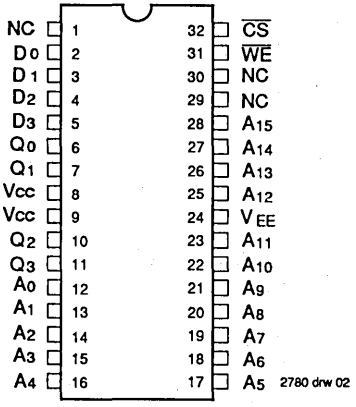
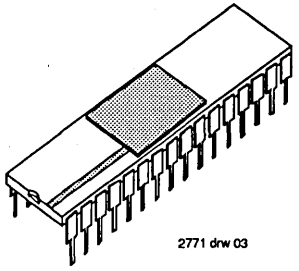
COMMERCIAL TEMPERATURE RANGE **AUGUST 1990**

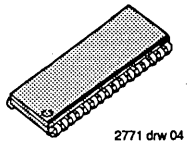
PIN CONFIGURATION



TOP VIEW



400-Mil-Wide
CERAMIC PACKAGE
C32



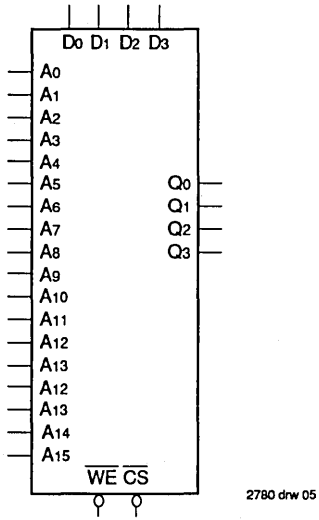
300-Mil-Wide
PLASTIC SOJ PACKAGE
Y32

PIN DESCRIPTION

Symbol	Pin Name
A0 through A15	Address Inputs
D0 through D3	Data Inputs
Q0 through Q3	Data Outputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input (Internal pull down)
VEE	More Negative Supply Voltage
VCC	Less Negative Supply Voltage
NC	No Connect (Not Internally Connected

2780 tbl 01

LOGIC SYMBOL



64Kx4
SRAM

AC OPERATING RANGES(1)

I/O	VEE	Temperature
10K	-5.2V ±5%	0 TO 75°C, air flow exceeding 2 m/sec
100K	-4.5V ±5%	0 TO 85°C, air flow exceeding 2 m/sec
101K	-4.75V to -5.46V	0 TO 75°C, air flow exceeding 2 m/sec

2780 tbl 02

NOTE:
1. Referenced to VCC

CAPACITANCE (TA=+25°C, f=1.0MHz)

Symbol	Parameter	DIP		SOJ		Unit
		Typ.	Max.	Typ.	Max.	
CIN	Input Capacitance	4	–	3	–	pF
COUT	Output Capacitance	6	–	3	–	pF

2780 tbl 03

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	DATAOUT	Function
H	X	L	Deselected
L	H	RAM Data	Read
L	L	L	Write

NOTE:
1. H=High, L=Low, X=Don't Care

2780 tbl 04

ECL-10K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Output Current (Output High)		-50	mA

NOTE: 2782 tbl 05

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-10K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, RL=50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit	T_A
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA	–
			Others	–	–	110	µA	–
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA	–
			Others	-50	–	90	µA	–
I_{EE}	Supply Current	All Inputs and Outputs Open		-220	-150	–	mA	–

NOTE: 2782 tbl 06

1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

ECL-100K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +85	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Output Current (Output High)		-50	mA

NOTE: 2780 tbl 07

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-100K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.5V, RL=50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-200	-130	–	mA

NOTES: 2780 tbl 08

1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.

ECL-101K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
VTERM	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
TA	Operating Temperature		0 to +75	°C
TBIAS	Temperature Under Bias		-55 to +125	°C
TSTG	Storage Temperature	Ceramic Plastic	-65 to +150 -55 to +125	°C
PT	Power Dissipation		1.5	W
IOUT	DC Out mput Current (Output High)		-50	mA

2781 tbl 09

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-101K DC ELECTRICAL CHARACTERISTICS

(VEE = -5.2V, RL=50Ω to -2.0V, TA = 0 to +75°C, air flow exceeding 2 m/sec)

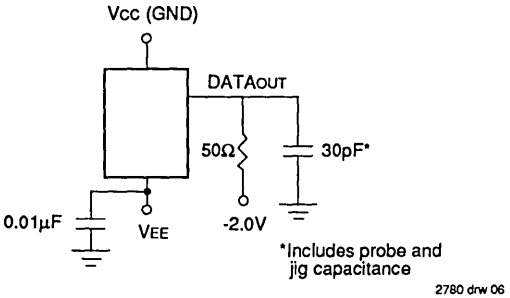
Symbol	Parameter	Test Condition		Min. (B)	Typ.[1]	Max. (A)	Unit
VOH	Output HIGH Voltage	V IN = V IHA or V ILB		-1025	-955	-880	mV
VOL	Output LOW Voltage	V IN = V IHA or V ILB		-1810	-1715	-1620	mV
VOHC	Output Threshold HIGH Voltage	V IN = V IHB or V ILA		-1035	–	–	mV
VOLC	Output Threshold LOW Voltage	V IN = V IHB or V ILA		–	–	-1610	mV
VIH	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
VIL	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I IH	Input HIGH Current	V IN = V IHA	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I IL	Input LOW Current	V IN = V ILB	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
IEE	Supply Current	All Inputs and Outputs Open		-220	-150	–	mA

2781 tbl 10

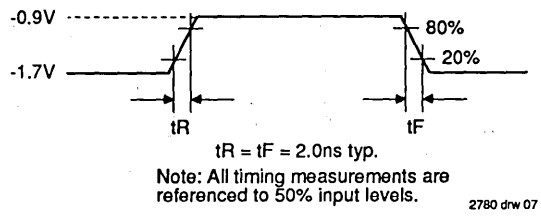
NOTES:

1. Typical parameters are specified at VEE = -5.2V, TA = +25°C and maximum loading.

AC TEST LOAD CONDITION



AC TEST INPUT PULSE



RISE/FALL TIME

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
tR	Output Rise Time	–	–	2	–	ns
tF	Output Fall Time	–	–	2	–	ns

2780 tbl 11

FUNCTIONAL DESCRIPTION

The IDT10504, IDT100504 and IDT101504 BiCMOS ECL static RAMs (SRAM) provide high speed with low power dissipation typical of BiCMOS ECL. These devices follow the conventional pinout and provide an upgrade path from 16Kx4 SRAMs.The ECL-101K meets electrical specifications that combine the ECL-100K temperature and voltage compensated output levels with the high-speed of ECL-10K VEE compatibility (-5.2V).

READ TIMING

The read timing on these asynchronous devices is straightforward. DataOUT is held low until the device is selected by Chip Select ($\overline{CS}$). Then Address (ADDR) settles and data appears on the output after time tAA. Note that DataOUT is held for a short time (tOH) after the address begins to change for the next access, then ambiguous data is on the bus until a new time tAA.

WRITE TIMING

To write data to the device, a Write Pulse need be formed on the Write Enable input ($\overline{WE}$) to control the write to the SRAM array. While $\overline{CS}$ and ADDR must be set-up when $\overline{WE}$ goes low, DataIN can settle after the falling edge of $\overline{WE}$, giving the data path extra margin. Data is written to the memory cell at the end of the Write Pulse, and addresses and Chip Select must be held after the rising edge of the Write Pulse to ensure satisfactory completion of the cycle.

DataOUT is disabled (held low) during the Write Cycle. If $\overline{CS}$ is held low (active) and addresses remain unchanged, the DataOUT pins will output the written data after "Write Recovery Time" (tWR).

Because of the very short Write Pulse requirement, these devices can be cycled as quickly for Writes as for Reads. Balanced cycles mean simpler timing in cache applications.

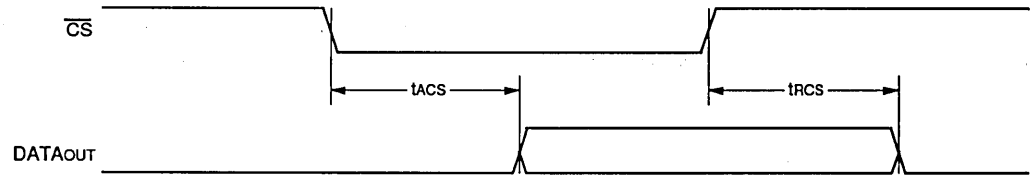
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10504S8 100504S8 101504S8		10504S10 100504S10 101504S10		10504S12 100504S12 101504S12		10504S15 100504S15 101504S15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle											
tACS	Chip Select Access Time	–	–	5	–	5	–	5	–	5	ns
tRCS	Chip Select Recovery Time	–	–	5	–	5	–	5	–	5	ns
tAA	Address Access Time	–	–	8	–	10	–	12	–	15	ns
tOH	Data Hold from Address Change	–	3	–	3	–	3	–	3	–	ns

NOTE:
1. Input and Output reference level is 50% point of waveform.

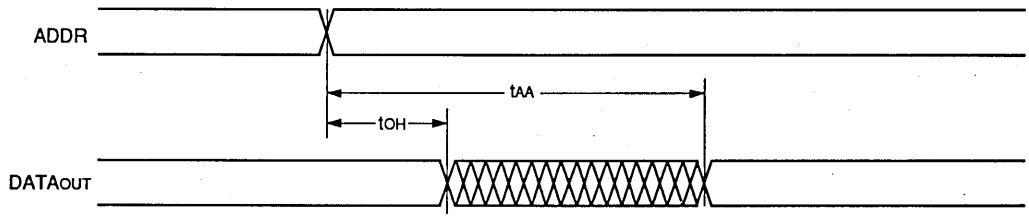
2780 tbl 12

READ CYCLE GATED BY CHIP SELECT



2780 drw 08

READ CYCLE GATED BY ADDRESS



2780 drw 09

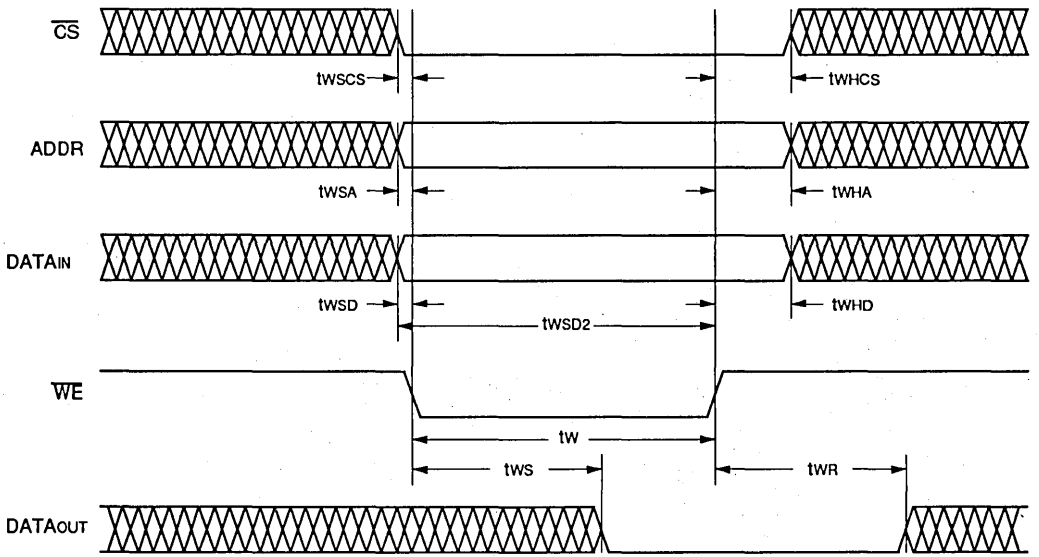
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10504S8 100504S8 101504S8		10504S10 100504S10 101504S10		10504S12 100504S12 101504S12		10504S15 100504S15 101504S15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle											
tW	Write Pulse Width	tWSA= minimum	6	–	8	–	10	–	10	–	ns
tWSD	Data Set-up Time	–	0	–	0	–	0	–	2	–	ns
tWSD2[2]	Data Set-up Time to $\overline{WE}$ High	–	5	–	5	–	5	–	5	–	ns
tWSA	Address Set-up Time	tWSA= minimum	0	–	0	–	0	–	2	–	ns
tWSCS	Chip Select Set-up Time	–	0	–	0	–	0	–	2	–	ns
tWHD	Data Hold Time	–	2	–	2	–	2	–	3	–	ns
tWHA	Address Hold Time	–	2	–	2	–	2	–	3	–	ns
tWHCS	Chip Select Hold Time	–	2	–	2	–	2	–	3	–	ns
tWS	Write Disable Time	–	–	5	–	5	–	5	–	5	ns
tWR[3]	Write Recovery Time	–	–	5	–	5	–	5	–	5	ns

2782 tbl 13

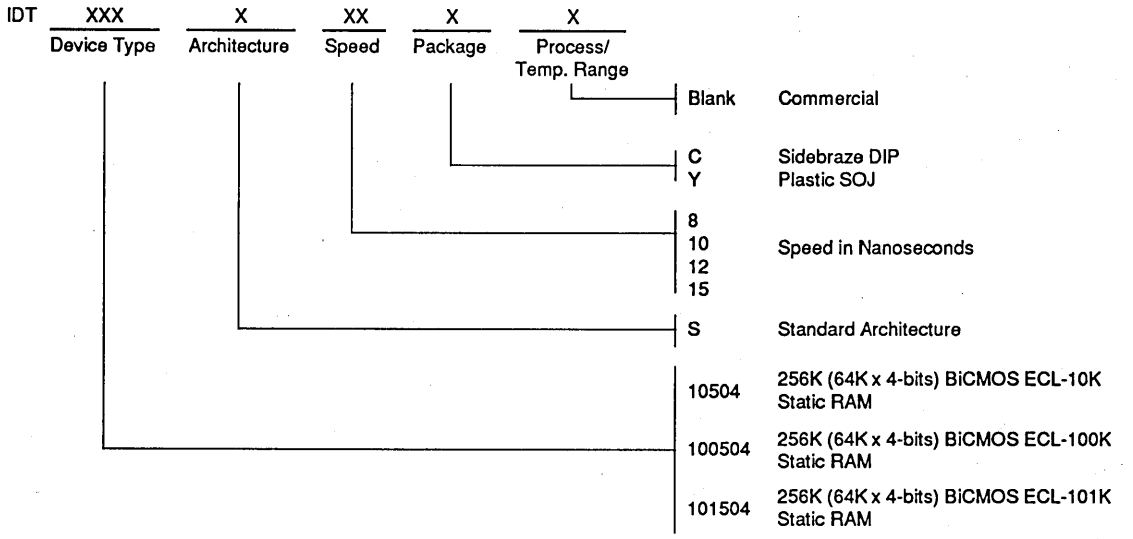
NOTES:
1. Input and Output reference level is 50% point of waveform.
2. tWSD is specified with respect to the falling edge of $\overline{WE}$ for compatibility with bipolar part specifications, but this device actually only requires tWSD2 with respect to rising edge of $\overline{WE}$.
3. tWR is defined as the time to reflect the newly written data on the Data Outputs (Q_0 to Q_3) when no new Address Transition occurs.

WRITE CYCLE TIMING DIAGRAM



2782 drw 10

ORDERING INFORMATION



2782 drw 11

5

Integrated Device Technology, Inc.

SELF-TIMED BiCMOS ECL STATIC RAM 256K (64K x 4-BIT) STRAM

PRELIMINARY
IDT10506LL
IDT100506LL
IDT101506LL

FEATURES:

- 65,536-words x 4-bit organization
- Self-Timed Write, with latches on inputs and latches on outputs
- Balanced Read/Write cycle time: 15/18ns
- Access time: 12/15 ns (max.)
- Fully compatible with ECL logic levels
- Through-hole DIP and surface-mount packages

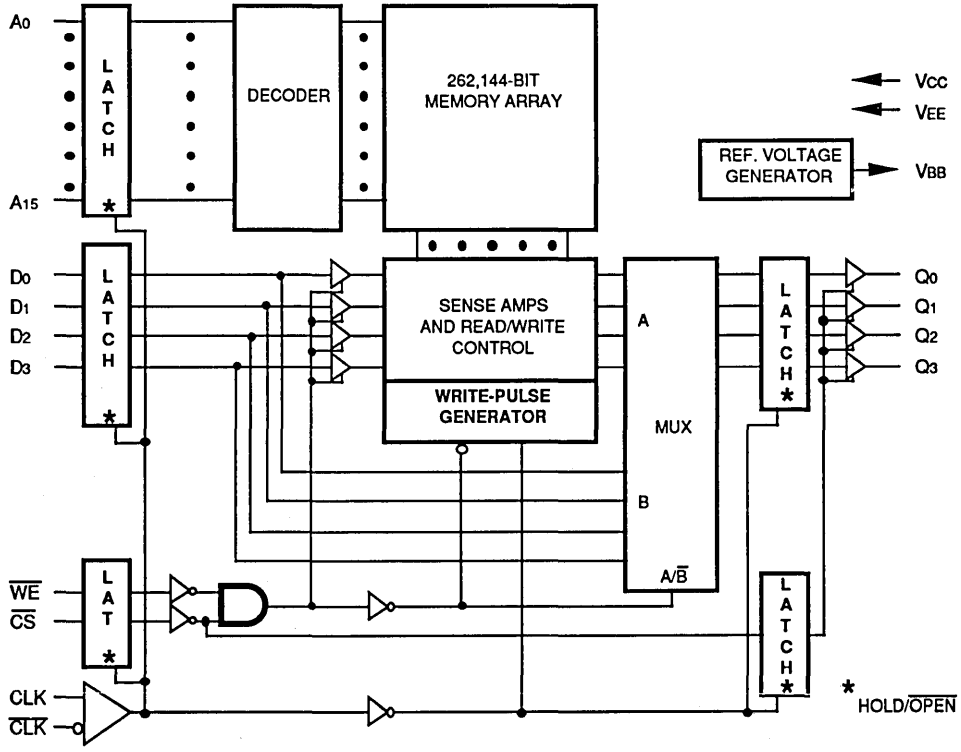
DESCRIPTION:

The IDT10506LL, IDT100506LL and IDT101506LL are 65,536-bit high-speed BiCEMOS™ ECL static random access memories organized as 64K x 4, with inputs and outputs fully compatible with ECL levels. Clocked level-sensitive latches on inputs and outputs, and the self-timed write operation, provide enhanced system performance over conventional RAMs, providing easier design and improved system level cycle times.

Inputs can flow into the device and then are latched by the leading edge of an externally supplied differential clock. The small input valid window required means more margin for system skews. Logic-to-memory propagation delay is included in device cycle time calculation, allowing this device to deliver better system performance than asynchronous SRAMs and glue logic.

Write timing is controlled internally based on the clock. Write Enable has no special requirements. The device allows balanced read and write cycle times, and reads and writes can be inserted in any order.

FUNCTIONAL BLOCK DIAGRAM



2783 drw 01

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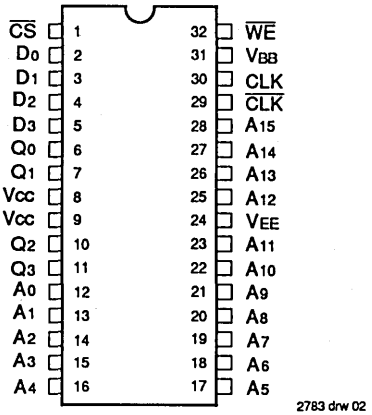
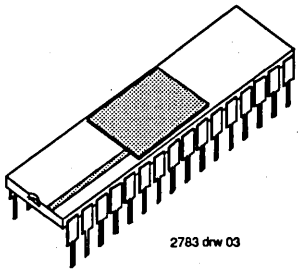
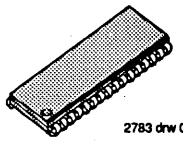
PIN CONFIGURATION



DIP/SOJ
TOP VIEW



400-Mil-Wide
CERAMIC PACKAGE
C32



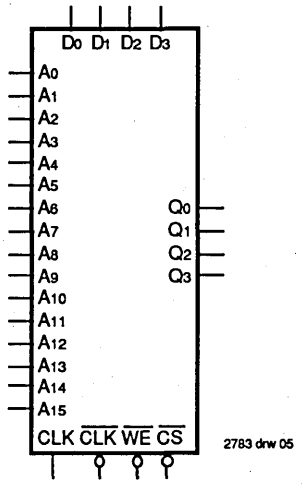
300-Mil-Wide
PLASTIC SOJ PACKAGE
Y32

PIN DESCRIPTIONS

Symbol	Pin Name
A0 through A15	Address Inputs
D0 through D3	Data Inputs
Q0 through Q3	Data Outputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input (Internal pull down)
CLK, $\overline{CLK}$	Differential Clock Inputs
VBB	Reference Voltage Output (≈1.32V)
VEE	More Negative Supply Voltage
VCC	Less Negative Supply Voltage

2783 tbl 01

LOGIC SYMBOL



64Kx4
STRAM

AC OPERATING RANGES(1)

I/O	VEE	Temperature
10K	-5.2V ±5%	0 TO 75°C, air flow exceeding 2 m/sec
100K	-4.5V ±5%	0 TO 85°C, air flow exceeding 2 m/sec
101K	-4.75V to -5.46V	0 TO 75°C, air flow exceeding 2 m/sec

2783 tbl 02

NOTE:
1. Referenced to Vcc

CAPACITANCE (TA=+25°C, f=1.0MHz)

Symbol	Parameter	DIP Typ.	DIP Max.	SOJ Typ.	SOJ Max.	Unit
CINCLK	Input Capacitance CLK/$\overline{CLK}$	6	–	3	–	pF
CIN	Input Capacitance except CLK/$\overline{CLK}$	4	–	3	–	pF
COUT	Output Capacitance	6	–	3	–	pF

2783 tbl 03

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	CLK	DataOUT(2)	Function
H	X	↑	L	Deselected
L	H	↑	RAM Data	Read
L	L	↑	WRITE Data	Write

2783 tbl 04

NOTES:
1. H=High, L=Low, X=Don't Care
2. DATAOUT changes when CLK returns high.

ECL-10K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to + 75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2783 tbl 05

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-10K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L = 50Ω to -2.0V, T_A = 0 to +75°C for DIP, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit	T_A
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs[2]		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs[2]		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA	–
			Others	–	–	110	µA	–
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA	–
			Others	-50	–	90	µA	–
I_{EE}	Supply Current	All Inputs and Outputs Open[2]		-280	-220	–	mA	–

2783 tbl 06

NOTES:

1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.
2. Except CLK and $\overline{CLK}$, one of which is tied low and one is tied high.

ECL-100K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to + 85	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2783 tbl 07

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-100K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.5V, R_L =50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs[2]		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs[2]		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open[2]		-260	-200	–	mA

2783 tbl 08

NOTES:
1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.
2. Except CLK and $\overline{CLK}$, one of which is tied low and one is tied high.

5

ECL-101K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to + 75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2783 tbl 09

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-101K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L =50Ω to -2.0V, T_A = 0 to +75°C for DIP, air flow exceeding 2 m/sec)

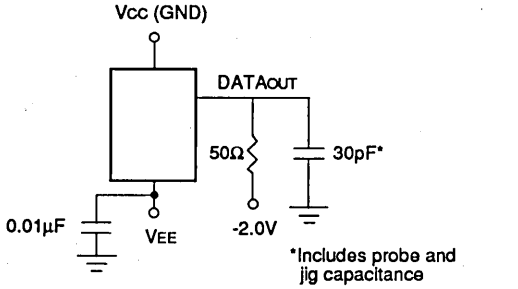
Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs(2)		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs(2)		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open(2)		-280	-220	–	mA

2783 tbl 10

NOTES:

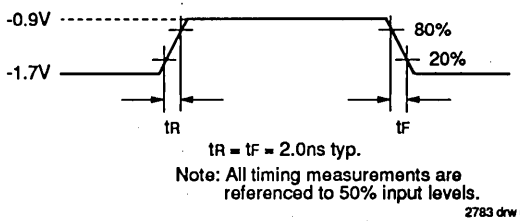
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.
2. Except CLK and $\overline{CLK}$, one of which is tied low and one is tied high.

AC TEST LOAD CONDITION



2783 drw 06

AC TEST INPUT PULSE



2783 drw 07

RISE/FALL TIME

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
tR	Output Rise Time	–	–	2	–	ns
tF	Output Fall Time	–	–	2	–	ns

2783 tbl 11

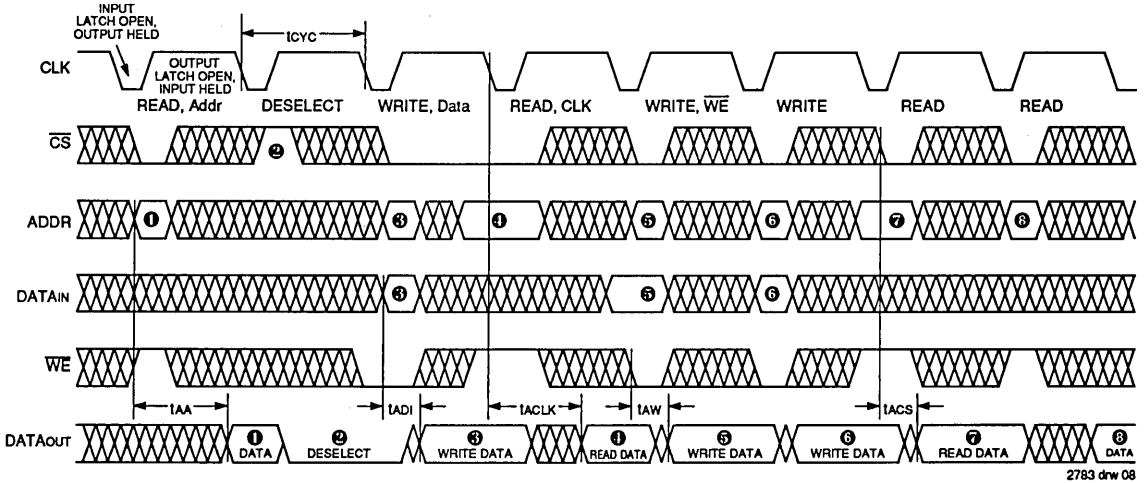
FUNCTIONAL DESCRIPTION

The IDT10506LL, IDT100506LL, and IDT101506LL Self-Timed BiCMOS ECL static RAMs (STRAM) provide high speed with low power dissipation typical of BiCMOS ECL. On-chip logic additionally helps improve system performance. The ECL-101K meets electrical specifications that combine the ECL-100K temperature and voltage compensated output levels with the high-speed of ECL-10K VEE compatibility (-5.2V).

As can be seen in the Functional Block Diagram on the title page, this device contains level-sensitive latches to sample and hold addresses, input data, and control status, and hold output data. Inputs are transparent while the clock (CLK) input is low (and $\overline{CLK}$ is high), and then hold their contents when the clock returns high. In the case of a write cycle, the memory cell is written during the clock-high time, and write data conducted to the outputs. Because the output latches are controlled by an inversion of the clock, output data flows out the output latch while clock is high and then is held into the next cycle during clock low.

The Latch-Latch architecture is most useful when read access data is needed within the same cycle that addresses settle. The input latch, when transparent, allows the access to begin as soon as addresses settle, allowing data to be ready somewhat sooner in the cycle than would be possible with a clocked-register implementation.

FUNCTIONAL DESCRIPTION TIMING EXAMPLE



2783 drw 08

READ TIMING

In a typical read cycle, the read address flows into the device while clock is low, as at ❶ below. Read access begins when the last address has settled. When clock returns high, the inputs are held so that addresses can begin to change for the next cycle.

Clock high also opens the output latches, so the read data for the read address clocked in at ❶ is gated through the output latch to the output pins. There is a short delay from rising clock to output ready, called t_{DR} (see Read Cycle Timing). If the clock-low time (t_{WL}) is shorter than the inherent access-time of the cell, output is guaranteed valid after the specified t_{AA}. But if t_{WL} is longer than the cell access-time, output data will be valid t_{DR} after clock goes high. Thus, the time it takes from address valid to data ready for any given address is

$$t_{AA} = t_{AA} \text{ or } (t_{SA} + t_{DR}),$$

whichever is larger. A permutation of this equation holds for each read and write access modes.

Because addresses and control lines (Write Enable and Chip Select) all must be stable for access to commence, there are two other read access modes, described as follows.

If addresses and controls are all stable before input latches are opened by clock going low, as at ❹ below, access begins on the low-going edge of clock. Data is available t_{ACLK} later, provided the output latch is opened by clock returning high.

If address and Write Enable are valid after clock-low, but Chip Select is last to go low, as at ❼ below, data is available t_{ACS} after the low-going edge of Chip Select.

The output latch takes some time to change state for the next cycle, but this time is very short. Therefore, data hold time from clock high (t_{DH}) is specified as zero minimum hold time.

DESELECT TIMING

Because the outputs are latched, they will continue to drive the output pins until a disable state is clocked through the device. The deselected state is achieved by de-asserting chip select ($\overline{CS}$ high) before clock returns high. This case occurs at ❷ below. Outputs then attain the disable state (low) t_{DR} later. Status of other inputs do not effect the disabling of the device when chip select is de-asserted with the proper relation to clock.

WRITE TIMING

Write cycles are identical to read cycles, except that write enable and write data need also be supplied, with the appropriate setup and hold timing. The device has on-chip timing that handles all aspects of writing data into the addressed RAM cell without the need for external write-pulse generation. The timing logic uses the clock-high time as the write pulse, and thus determines the minimum clock-high time, t_{WH}.

In addition to writing to the RAM cell, the write data is fed to the output register by a multiplexer, so that write data is available on the output pins after an access time. Thus the input data supplied at ❸ is available on the output t_{ADI} after the input data has settled, while the input data supplied at ❺ is available t_{AW} after Write Enable is asserted low. This function is sometimes called "Transparent Write," and is useful for write-through cache applications.

There are no restrictions on the order of read cycles and write cycles.

AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

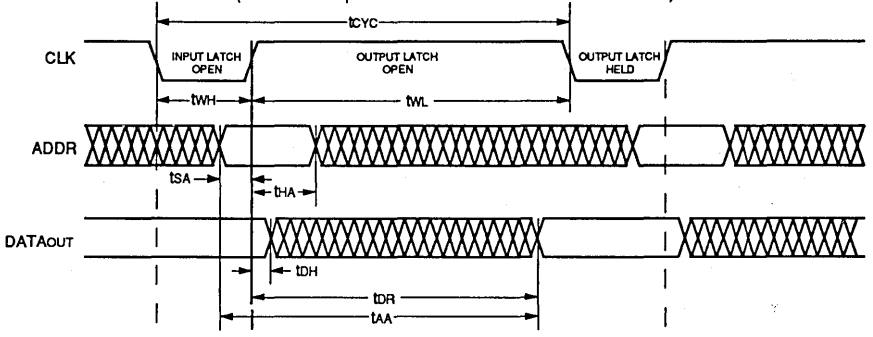
Symbol	Parameter[1]	Test Condition	10506LL15 100506LL15 101506LL15 Min.	10506LL15 100506LL15 101506LL15 Max.	10506LL18 100506LL18 101506LL18 Min.	10506LL18 100506LL18 101506LL18 Max.	Unit
Read Cycle							
tCYC	Cycle Time	–	15	–	18	–	ns
tAA[2]	Address Access Time	–	–	12	–	15	ns
tACS[3]	Chip Select Access Time	–	–	5	–	5	ns
tACLK[4]	Access Time from Clock Low	–	–	12	–	15	ns
tWL	Clock Low Pulse Width	–	3	–	3	–	ns
tWH	Clock High Pulse Width	–	12	–	15	–	ns
tSCS	Setup Time for Chip Select	–	1	–	1	–	ns
tSA	Setup Time for Address	–	1	–	1	–	ns
tHCS	Hold Time for Chip Select	–	2	–	2	–	ns
tHA	Hold Time for Address	–	2	–	2	–	ns
tDH	Data Hold from Clock Low	–	0	–	0	–	ns
tDR[5]	Data Ready from Clock Low	–	0	4	0	4	ns

2783 tbl 12

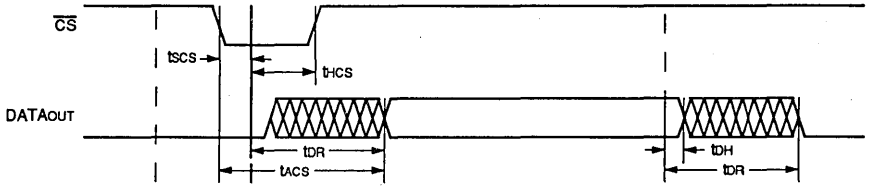
NOTES:
1. Input and Output reference level is 50% point of waveform.
2. Read Cycle is gated by Address when tSA < tWL so that the access begins at the settling of Address. Access time is the larger of tAA or tSA + tDR.
3. Read Cycle is gated by Chip Select when tSCS < tWL so that access begins at the falling edge of Chip Select. Access time is the larger of tACS or tSCS + tDR.
4. Read Cycle is gated by Clock when tSA > tWL so that access begins at the falling edge of Clock. Access time is the larger of tACLK or tWL + tDR.
5. tDR(max) is specified when all other gating conditions have been satisfied, specifically, for READ cycle: when tSA > tAA(max) - tDR(max) and tSCS > tACS(max) - tDR(max) and tWL > tACLK(max) - tDR(max); for WRITE cycle: when tSD > tADI(max) - tDR(max) and tSWE > tAW(max) - tDR(max).

5

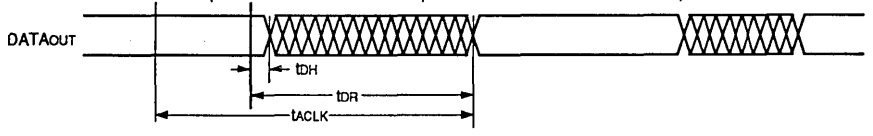
READ CYCLE GATED BY ADDRESS (Assumes Chip Select and Clock stable before Address)



READ CYCLE GATED BY CHIP SELECT (Assumes Address and Clock stable before Chip Select)



READ CYCLE GATED BY CLOCK (Assumes Address and Chip Select stable before Clock Low)



2783 drw 09

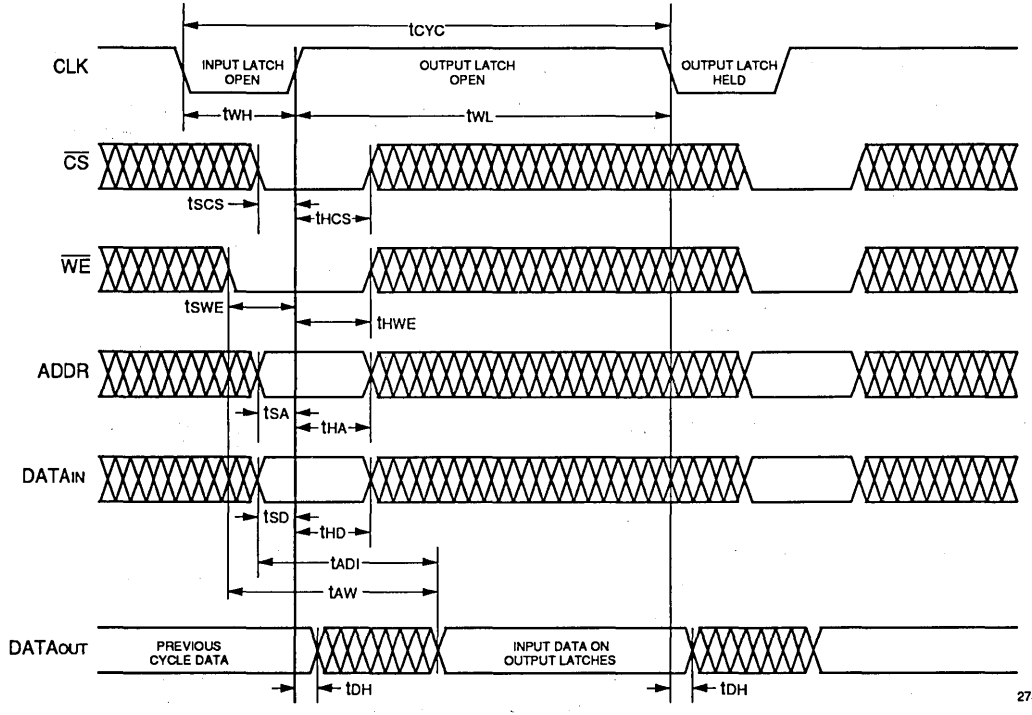
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10506LL15 100506LL15 101506LL15		10506LL18 100506LL18 101506LL18		Unit
			Min.	Max.	Min.	Max.	
Write Cycle[2]							
tAW[3]	Write Enable Low to Data Valid	–	–	5	–	5	ns
tADI[4]	Data In Valid to Data Out Valid	–	–	5	–	5	ns
tSWE	Setup Time for Write Enable	–	1	–	1	–	ns
tSD	Setup Time for Data In	–	1	–	1	–	ns
tHWE	Hold Time for Write Enable	–	2	–	2	–	ns
tHD	Hold Time for Data In	–	2	–	2	–	ns

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. All Setup, Hold, and Access timing are the same as the Read Cycle with the addition of above requirements. Write Data appears on output pins after rising edge of clock.
3. Access time is the larger of tAW or tSWE + tDR.
4. Access time is the larger of tADI or tSD + tDR.

2783 tbl 13

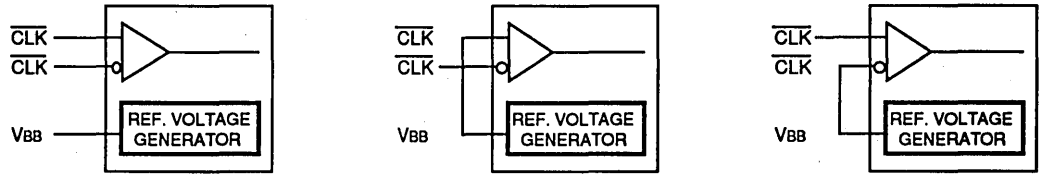
WRITE CYCLE



2783 drw 10

CLOCK INPUT

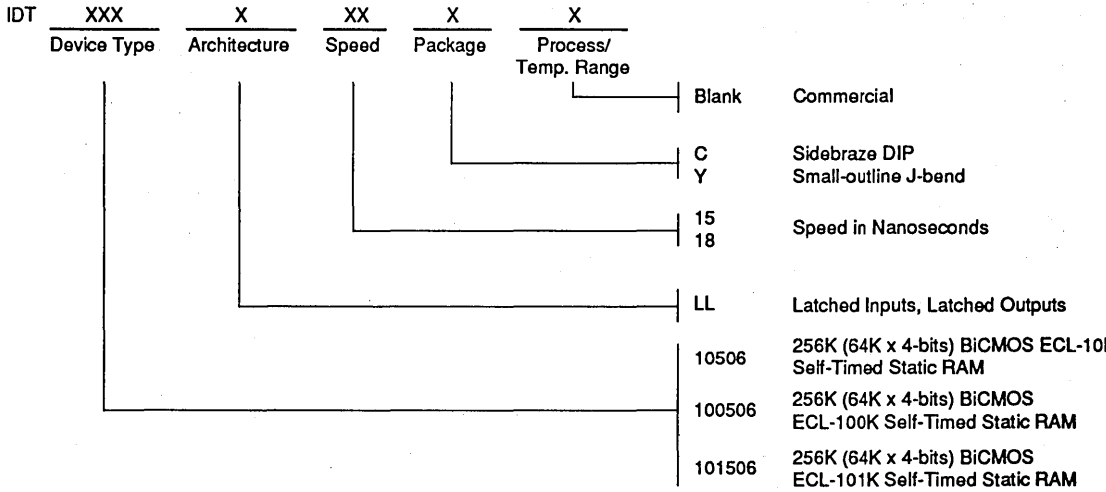
The clock input circuit has been designed to accomodate both single-ended and differential mode operation. Differential mode exhibits better common-mode noise rejection and is obtained by driving both true and complement clock lines with a differential driver, as shown in Figure (a). Single-ended operation is achieved as either falling-edge-active or rising-edge-active, as shown in Figures (b) and (c), respectively. VBB is designed to drive clock input only and is not intended to be used for any other purpose.



(a) Differential Mode (b) Falling-Edge-Active Single-Ended Mode (c) Rising-Edge-Active Single-Ended Mode

2785 drw 11

ORDERING INFORMATION



2785 drw 12

5

Integrated Device Technology, Inc.

SELF-TIMED BiCMOS ECL STATIC RAM 256K (64K x 4-BIT) STRAM

IDT10506RL
IDT100506RL
IDT101506RL

FEATURES:

- 65,536-words x 4-bit organization
- Self-Timed Write, with registers on inputs and latches on outputs
- Balanced Read/Write cycle time: 12/15ns
- Access time: 12/15 ns (max.)
- Low power dissipation: 800mW (typ.)
- Fully compatible with ECL logic levels
- Through-hole DIP and surface-mount packages

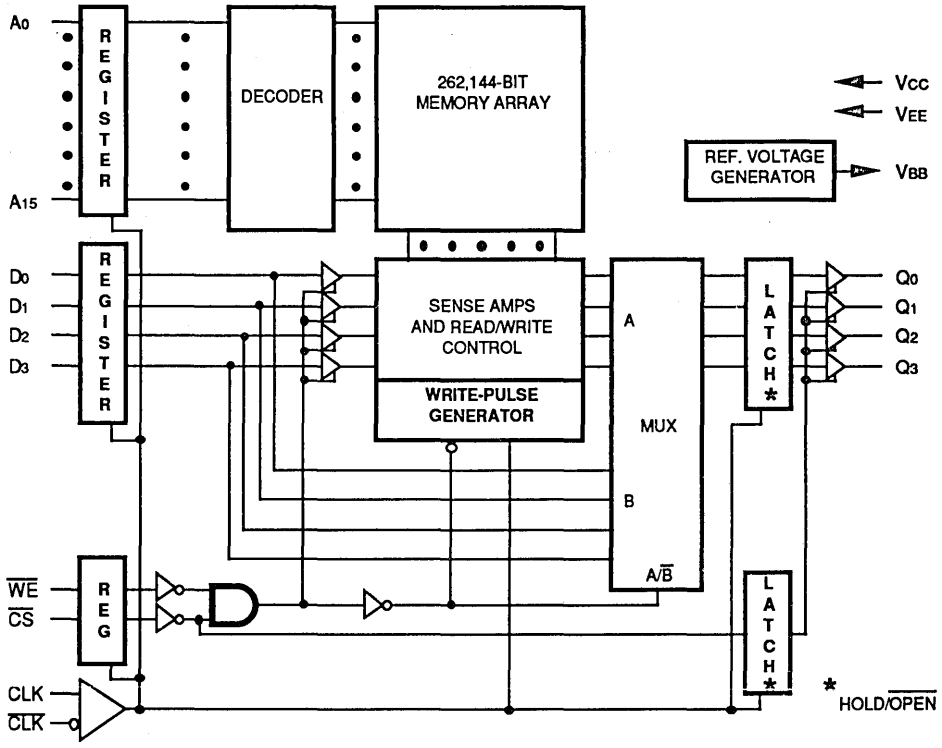
DESCRIPTION:

The IDT10506RL, IDT100506RL and IDT101506RL are 262,144-bit high-speed BiCEMOS™ ECL static random access memories organized as 16K x 4, with inputs and outputs fully compatible with ECL levels. Clocked registers on inputs and latches on outputs, and the self-timed write operation, provide enhanced system performance over conventional RAMs, providing easier design and improved system level cycle times.

Inputs are captured by the leading edge of an externally supplied differential clock. The small input valid window required means more margin for system skews. Logic-to-memory propagation delay is included in device cycle time calculation, allowing this device to deliver better system performance than asynchronous SRAMs and glue logic.

Write timing is controlled internally based on the clock. Write Enable has no special requirements. The device allows balanced read and write cycle times, and reads and writes can be inserted in any order.

FUNCTIONAL BLOCK DIAGRAM



2788 drw 01

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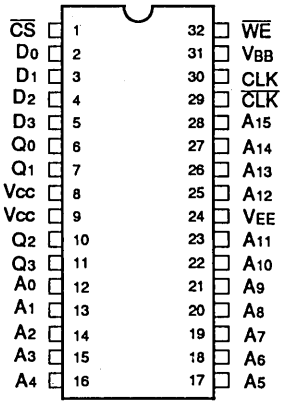
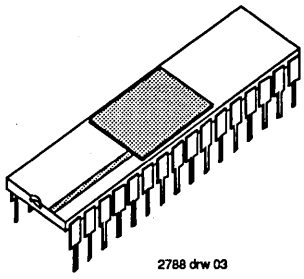
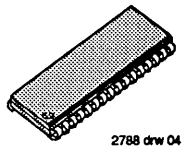
PIN CONFIGURATION



DIP/SOJ
TOP VIEW



400-Mil-Wide
CERAMIC PACKAGE
C32



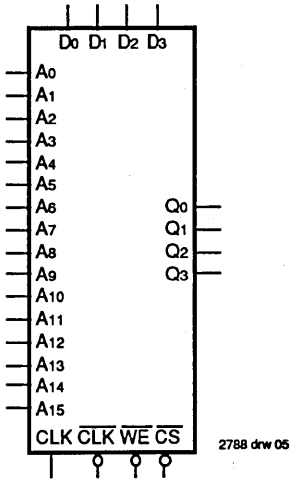
300-Mil-Wide
PLASTIC SOJ PACKAGE
Y32

PIN DESCRIPTION

Symbol	Pin Name
A0 through A15	Address Inputs
D0 through D3	Data Inputs
Q0 through Q3	Data Outputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input (Internal pull down)
CLK, $\overline{CLK}$	Differential Clock Inputs
VBB	Reference Voltage Output (≈1.32V)
VEE	More Negative Supply Voltage
VCC	Less Negative Supply Voltage
NC	No Connect - not internally connected

2788 tbl 01

LOGIC SYMBOL



64Kx4
STRAM

AC OPERATING RANGES(1)

I/O	VEE	Temperature
10K	-5.2V ±5%	0 TO 75°C, air flow exceeding 2 m/sec
100K	-4.5V ±5%	0 TO 85°C, air flow exceeding 2 m/sec
101K	-4.75V to -5.46V	0 TO 75°C, air flow exceeding 2 m/sec

NOTE: 2788 tbl 02
1. Referenced to Vcc

CAPACITANCE (TA=+25°C, f=1.0MHz)

Symbol	Parameter	DIP Typ.	DIP Max.	SOJ Typ.	SOJ Max.	Unit
CINCLK	Input Capacitance CLK/$\overline{CLK}$	6	–	3	–	pF
CIN	Input Capacitance except CLK/$\overline{CLK}$	4	–	3	–	pF
COUT	Output Capacitance	6	–	3	–	pF

2788 tbl 03

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	CLK	DataOUT(2)	Function
H	X	↕	L	Deselected
L	H	↕	RAM Data	Read
L	L	↕	WRITE Data	Write

2788 tbl 04
NOTES:
1. H=High, L=Low, X=Don't Care
2. DATAOUT initiated by an internal timer and gated by falling edge of CLK.

ECL-10K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2788 tbl 05

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-10K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L = 50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit	T_A
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	V_{IN} = V_{IHB} or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	V_{IN} = V_{IHB} or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs(2)		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs(2)		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	V_{IN} = V_{IHA}	$\overline{CS}$	–	–	220	µA	–
			Others	–	–	110	µA	–
I_{IL}	Input LOW Current	V_{IN} = V_{ILB}	$\overline{CS}$	0.5	–	170	µA	–
			Others	-50	–	90	µA	–
I_{EE}	Supply Current	All Inputs and Outputs Open(2)		-280	-220	–	mA	–

2788 tbl 06

NOTES:

1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.
2. Except CLK and $\overline{CLK}$, one of which is tied low and one is tied high.

ECL-100K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +85	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2788 tbl 07

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-100K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.5V, R_L = 50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs[2]		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs[2]		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open[2]		-260	-200	–	mA

2788 tbl 08

NOTES:

1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.
2. Except CLK and $\overline{CLK}$, one of which is tied low and one is tied high.

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ECL-101K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2788 tbl 09

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-101K DC ELECTRICAL CHARACTERISTICS

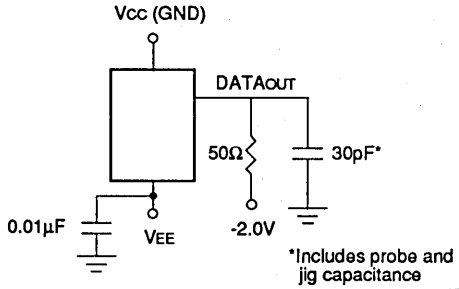
(V_{EE} = -5.2V, R_L = 50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs(2)		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs(2)		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open(2)		-280	-220	–	mA

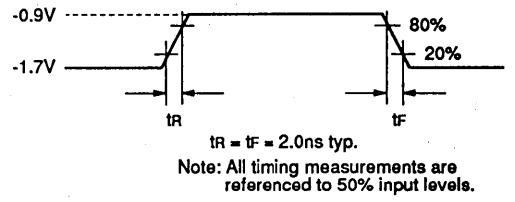
2789 tbl 10

NOTES:
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.
2. Except CLK and $\overline{CLK}$, one of which is tied low and one is tied high.

AC TEST LOAD CONDITION



AC TEST INPUT PULSE



RISE/FALL TIME

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
tR	Output Rise Time	–	–	2	–	ns
tF	Output Fall Time	–	–	2	–	ns

2788 tbl 11

FUNCTIONAL DESCRIPTION

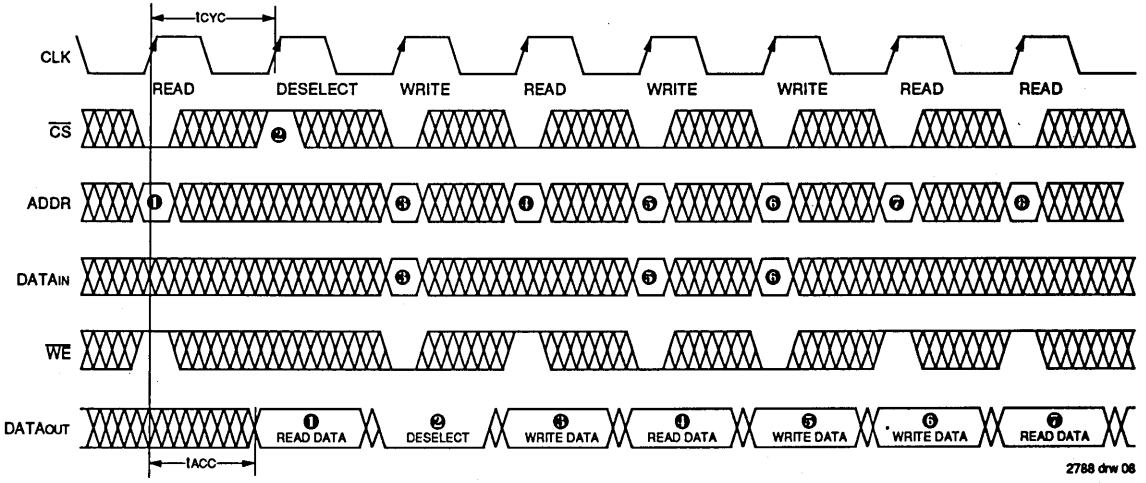
The IDT10496RL, IDT100496RL and IDT101496RL Self-Timed BiCMOS ECL static RAMs (STRAM) provide high speed with low power dissipation typical of BiCMOS ECL. On-chip logic additionally helps improve system performance. The ECL-101K meets electrical specifications that combine the ECL-100K temperature and voltage compensated output levels with the high-speed of ECL-10K VEE compatibility (-5.2V).

As can be seen in the Functional Block Diagram on the title page, this device contains clocked input registers to sample and hold addresses, input data, and control status. Inputs are sampled on the rising edge of the clock (CLK) input (falling edge of $\overline{CLK}$). In the case of a write cycle, the memory cell is written during the clock-high time, and write data conducted to the outputs. Output data flows out the output latch and is held into the next cycle.

READ TIMING

In a typical read cycle, the read address is captured by the rising edge of clock, as at ❶ below. Then, when clock goes low, the read data for the read address clocked in at ❶ is gated through the ouptut latch to the output pins. There is a delay from falling clock to output ready, called tDR (see Read Cycle Timing). If the clock-high time (tWH) is shorter than the inherent access-time of the cell, output is guaranteed valid after the specified tACC. But if tWH is longer than the cell access-time, output data will be valid tDR after clock goes low. Thus, the time it takes from clock-to-output for any given address (the

FUNCTIONAL DESCRIPTION TIMING EXAMPLE



latency, or tACC) is

tACC = tACC or (tWH + tDR), whichever is larger.

The output latch takes some time to change state for the next cycle, and this time is controlled by an internal timer. Therefore, data hold time from clock high at the beginning of the cycle (tDH) is specified. If the clock-high time (tWH) is longer than the tDH , then data will begin to switch immediately upon the clock-low transition and be steady at tACC.

DESELECT TIMING

Because the outputs are latched, they will continue to drive the output pins until a disable state is clocked through the device. The deselected state is achieved by de-asserting chip select ($\overline{CS}$ high) at rising edge of clock. This case occurs at ❷ below. Outputs then attain the disable state (low) tACC later. Status of other inputs do not effect the disabling of the device when chip select is de-asserted with the proper relation to clock.

WRITE TIMING

Write cycles are identical to read cycles, except that write enable and write data need also be supplied, with the appropriate setup and hold timing. The device has on-chip timing that handles all aspects of writing data into the addressed RAM cell without the need for external write-pulse generation. The timing logic uses an internal timer to generate the write pulse, so the falling edge of clock is not critical.

In addition to writing to the RAM cell, the write data is fed to the output register by a multiplexer, so that write data is available on the output pins in the appropriate time slot (i.e. after tACC or tWH + tDR). This function is sometimes called "Transparent Write," and is useful for write-through cache applications. Thus the input data sampled at ❸ is available on the output at the end of the cycle.

There are no restrictions on the order of read cycles and write cycles.

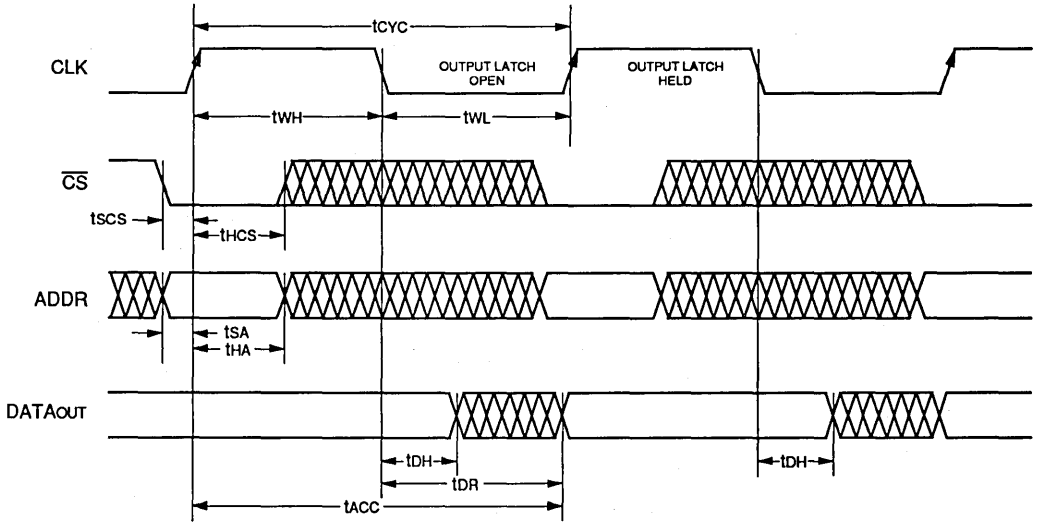
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Ranges)

Symbol	Parameter[1]	Test Condition	10506RL12 100506RL12 101506RL12		10506RL15 100506RL15 101506RL15		Unit
			Min.	Max.	Min.	Max.	
Read Cycle							
tCYC	Cycle Time	–	12	–	15	–	ns
tACC[2]	Access Time from Clock High	–	–	12	–	15	ns
tWL	Clock Low Pulse Width	–	5	–	6	–	ns
tWH	Clock High Pulse Width	–	5	–	6	–	ns
tSCS	Setup Time for Chip Select	–	1	–	1	–	ns
tSA	Setup Time for Address	–	1	–	1	–	ns
tHCS	Hold Time for Chip Select	–	2.5	–	2.5	–	ns
tHA	Hold Time for Address	–	2.5	–	2.5	–	ns
tDH	Data Hold from Clock Low	–	2	–	2	–	ns
tDR	Data Ready from Clock Low	–	0	5	0	5	ns

2788 tbl 12

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. Access time is the larger of tACC or tWH + tDR.

READ CYCLE TIMING DIAGRAM



2788 drw 09

5

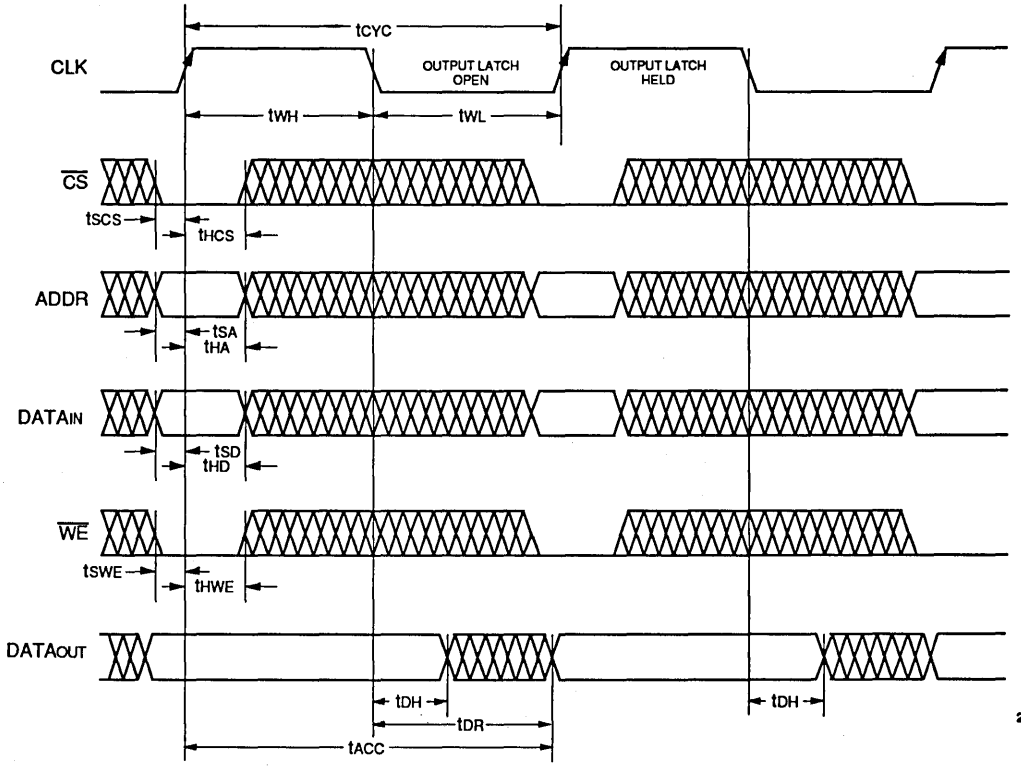
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10506RL12 100506RL12 101506RL12		10506RL15 100506RL15 101506RL15		Unit
			Min.	Max.	Min.	Max.	
Write Cycle[2]							
tSWE	Setup Time for Write Enable	–	1	–	1	–	ns
tSD	Setup Time for Data In	–	1	–	1	–	ns
tHWE	Hold Time for Write Enable	–	2.5	–	2.5	–	ns
tHD	Hold Time for Data In	–	2.5	–	2.5	–	ns

2788 tbl 13

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. All Setup, Hold, and Access timing are the same as the Read Cycle with the addition of above requirements.

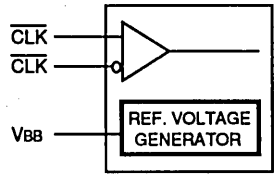
WRITE CYCLE TIMING DIAGRAM



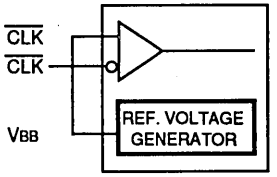
2788 drw 10

CLOCK INPUT

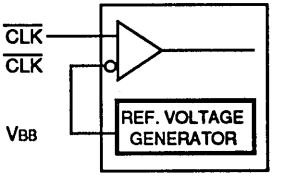
The clock input circuit has been designed to accomodate both single-ended and differential mode operation. Differential mode exhibits better common-mode noise rejection and is obtained by driving both true and complement clock lines with a differential driver, as shown in Figure (a). Single-ended operation is achieved as either falling-edge-active or rising-edge-active, as shown in Figures (b) and (c), respectively. VBB is designed to drive clock input only and is not intended to be used for any other purpose.



(a) Differential Mode



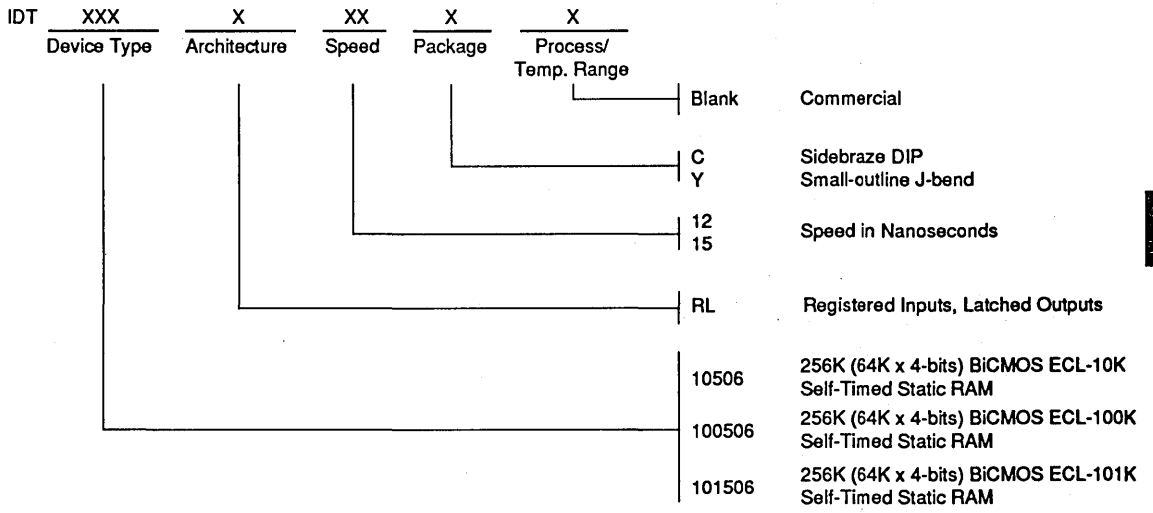
(b) Falling-Edge-Active Single-Ended Mode



(c) Rising-Edge-Active Single-Ended Mode

2788 drw 11

ORDERING INFORMATION



2788 drw 12

5

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 256K (64K x 4-BIT) with SYNCHRONOUS WRITE

ADVANCE INFORMATION
IDT10507
IDT100507
IDT101507

FEATURES:

- 65,535-words x 4-bit organization
- Address access time: 12/15 ns
- Read Data output latch for extended hold time
- Short Write Cycle input data and address valid time
- Pin compatible with standard 64K x 4
- Through-hole DIP and surface-mount packages

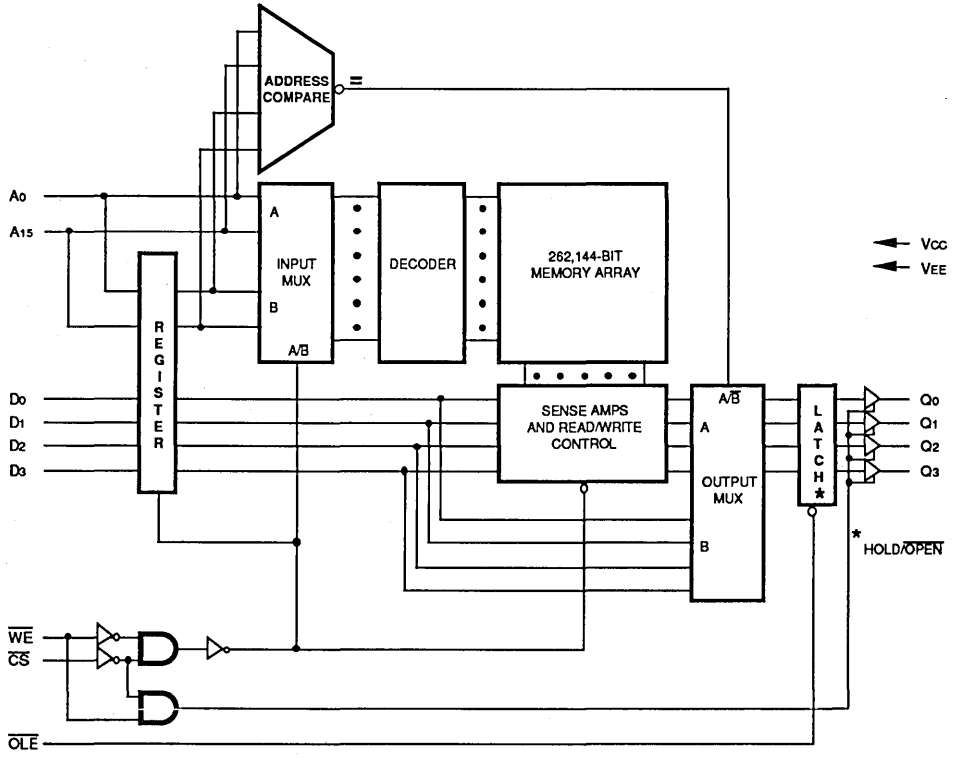
DESCRIPTION:

The IDT10507, IDT100507 and IDT101507 are 262,144-bit high-speed BiCEMOS™ ECL static random access memories organized as 64K x 4, with inputs and outputs fully compatible with ECL levels. Internal registers on inputs provide enhanced Write Cycle performance over conventional RAMs, while output read data latch allows longer output data hold time providing easier design and improved system level cycle times.

In the read mode, this device is pinout and timing compatible with the standard asynchronous SRAMs (IDT10504), yet the addition of an output latch with separate enable control allow output data to be captured and held long into the next cycle. This minimizes noise on the data bus and provides better set-up time margin for the next logic stage in pipelined applications.

In the write mode, the device adds an invisible pipeline stage in the write address and data paths, allowing very short set-up and hold times for these inputs and less stringent requirements for the write pulse input.

FUNCTIONAL BLOCK DIAGRAM



2789 drw 01

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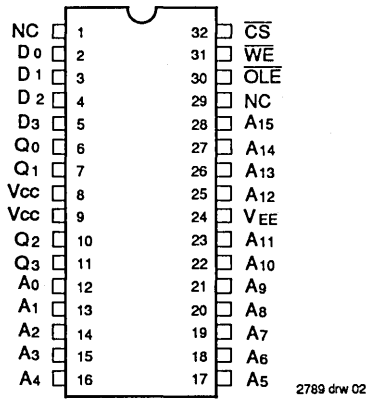
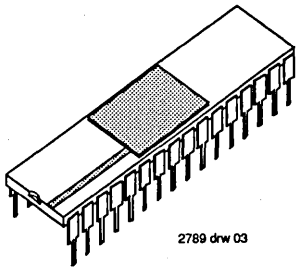
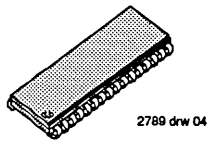
PIN CONFIGURATION



TOP VIEW



400-Mil-Wide
CERAMIC PACKAGE
C32



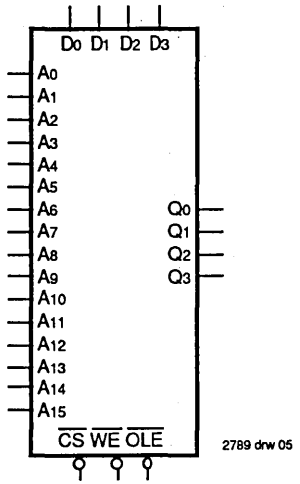
300-Mil-Wide
PLASTIC SOJ PACKAGE
Y32

PIN DESCRIPTIONS

Symbol	Pin Name
A0 through A15	Address inputs
D0 through D3	Data Inputs
Q0 through Q3	Data Outputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input (Internal pull down)
$\overline{OLE}$	Output Latch Enable
VEE	More Negative Supply Voltage
Vcc	Less Negative Supply Voltage

2789 tbl 01

LOGIC SYMBOL



64Kx4
SRAM

AC OPERATING RANGES(1)

I/O	VEE	Temperature
10K	-5.2V ±5%	0 TO 75°C, air flow exceeding 2 m/sec
100K	-4.5V ±5%	0 TO 85°C, air flow exceeding 2 m/sec
101K	-4.75V to -5.46V	0 TO 75°C, air flow exceeding 2 m/sec

2789 tbl 02

NOTE:
1. Referenced to Vcc

CAPACITANCE (TA=+25°C, f=1.0MHz)

Symbol	Parameter	DIP Typ.	DIP Max.	SOJ Typ.	SOJ Max.	Unit
CIN	Input Capacitance	4	–	3	–	pF
COUT	Output Capacitance	6	–	3	–	pF

2789 tbl 03

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	$\overline{OLE}$	DataOUT(2)	Function
H	X	X	L	Deselected
L	H	L	RAM Data	Read
L	H	H	RAM Data	Output Held
L	L	X	L	Write

2789 tbl 04

NOTES:
1. H=High, L=Low, X=Don't Care
2. DATAOUT initiated by falling edge of $\overline{OLE}$.

ECL-10K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2789 tbl 05

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-10K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L = 50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit	T_A
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA	–
			Others	–	–	110	µA	–
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA	–
			Others	-50	–	90	µA	–
I_{EE}	Supply Current	All Inputs and Outputs Open		-280	-220	–	mA	–

2789 tbl 06

NOTE:
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

ECL-100K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +85	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2789 tbl 07

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-100K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.5V, R_L = 50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-260	-200	–	mA

2789 tbl 08

NOTE:
1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.

5

ECL-101K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2789 tbl 09

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions

ECL-101K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L = 50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

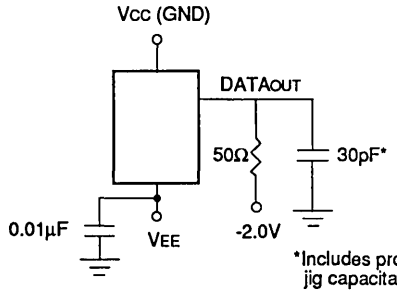
Symbol	Parameter	Test Condition		Min. (B)	Typ.[1]	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-280	-220	–	mA

2789 tbl 10

NOTE:

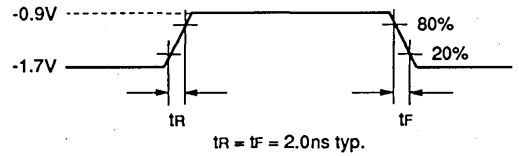
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

AC TEST LOAD CONDITION



2789 drw 06

AC TEST INPUT PULSE



tR = tF = 2.0ns typ.

Note: All timing measurements are referenced to 50% input levels.

2789 drw 07

RISE/FALL TIME

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
tR	Output Rise Time	–	–	2	–	ns
tF	Output Fall Time	–	–	2	–	ns

2789 tbl 11

FUNCTIONAL DESCRIPTION

The IDT10507, IDT100507 and IDT101507 BiCMOS ECL static RAMs (SRAM) with SYNCHRONOUS WRITE provide high speed with low power dissipation typical of BiCMOS ECL. On-chip logic additionally helps improve system performance, yet the device is pinout-compatible with asynchronous equivalents (i.e... IDT10504, IDT100504, and IDT101504 respectively). The ECL-101K meets electrical specifications that combine the ECL-100K temperature and voltage compensated output levels with the high-speed of ECL-10K VEE compatibility (-5.2V).

As can be seen in the Functional Block Diagram on the title page, this device contains clocked input registers to sample and hold addresses and input data, during a write cycle only. Inputs are sampled on the rising edge of the Write Enable ($\overline{WE}$). The write cycle is pipelined: the memory cell is written during the $\overline{WE}$-low time in the next cycle.

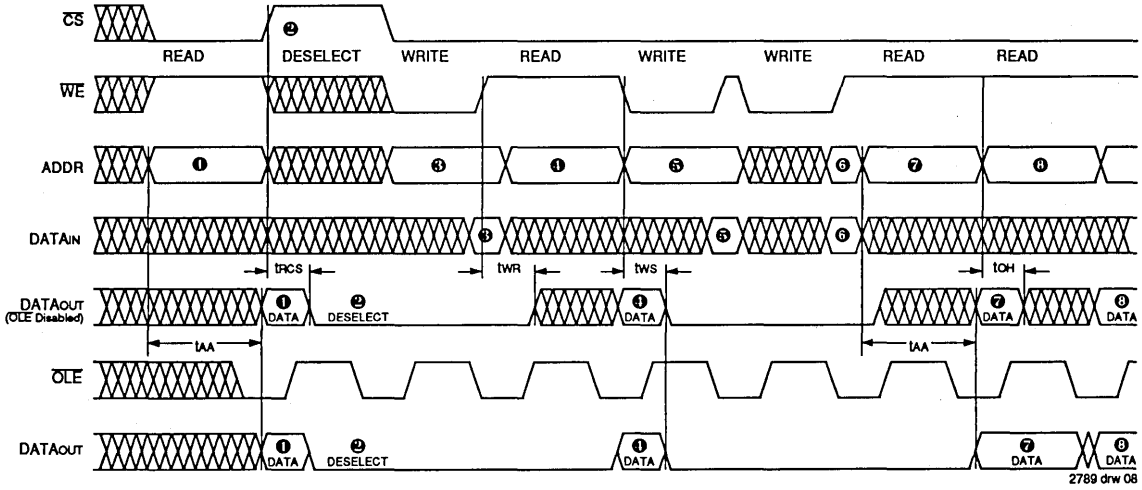
Read cycles are not pipelined and operate identically to an asynchronous device, except that an output latch is provided to capture and hold Read data.

READ TIMING

The read timing on the device is asynchronous. DataOUT is held low until the device is selected by Chip Select ($\overline{CS}$). Then Address (ADDR) settles and data appears on the output after time tAA, as at ❶ below.

DataOUT is held for a short time (tOH) after the address

FUNCTIONAL DESCRIPTION TIMING EXAMPLE



2789 drw 08

begins to change for the next access, as can be seen at ❼ — allowing addresses to begin to change early for the next cycle — then ambiguous data is on the bus until a new time t_{AA}.

To avoid this noise on the bus and provide for longer output hold time, this device includes an output Read data latch which allows Read data to flow out while Output Latch Enable ($\overline{OLE}$) is low, and then hold when $\overline{OLE}$ is high. Thus in the example below Read data at ❼ is held until Read data at ❽ is ready for output.

Note that $Data_{OUT}$ is disabled (held low) by $\overline{CS}$ high or $\overline{WE}$ low, regardless of the state of the Output Latch.

DESELECT TIMING

Deselect timing is identical to a standard asynchronous device. This case occurs at ❷ below. Outputs attain the disable state (low) t_{RCS} later Chip Select ($\overline{CS}$) is taken to a high logic state. Status of other inputs do not effect the disabling of the device when chip select is de-asserted.

WRITE TIMING

Write cycles pipelined to allow easier design and higher system performance. The write pulse created on the $\overline{WE}$ input is used as a strobe to clock in the Write Address and Data into a register. This address and data are held in the register until the next write cycle, when they are used to write into the memory array through the Input Multiplexor.

Note the very short valid window required for Write Address and Data inputs. This is because these signals are captured by the input register. This means that input data may arrive late in the cycle, as at ❸ below, or data and address may arrive late, as at ❻ below.

$Data_{OUT}$ is disabled during the Write Cycle. If $\overline{CS}$ is held low (active) and addresses remain unchanged, the $Data_{OUT}$ pins will output the written data after "Write Recovery Time" (t_{WR}), as for a standard asynchronous device.

There is a special case when a Read cycle follows directly a Write Cycle to the same address. The memory array has not yet been updated with the Write data — it is still in the input register. This case is handled by including an address comparator and Output Multiplexor on the device: if the address being presented on the input pins is the same as the address stored in the input register, the data presented to the output pins is also from the input register.

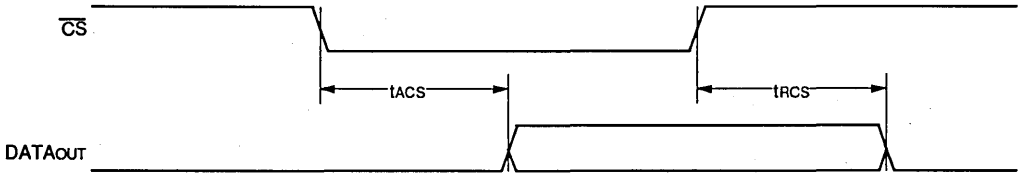
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10507S12 100507S12 101507S12		10507S15 100507S15 101507S15		Unit
			Min.	Max.	Min.	Max.	
Read Cycle							
t_{AA}[2]	Address Access Time	–	–	12	–	15	ns
t_{ACS}	Chip Select Access Time	–	–	5	–	5	ns
t_{RCS}	Chip Select Recovery Time	–	–	5	–	5	ns
t_{OH}	Data Hold from Address Change	–	3	–	3	–	ns
t_{OLEL}	Latch Enable Low Pulse Width	–	5	–	5	–	ns
t_{AHO}	Address Valid to $\overline{OLE}$ High	–	14	–	17	–	ns
t_{DH}	Data Hold from Clock Low	–	0	–	0	–	ns
t_{DR}	Data Ready from Clock Low	–	0	4	0	4	ns

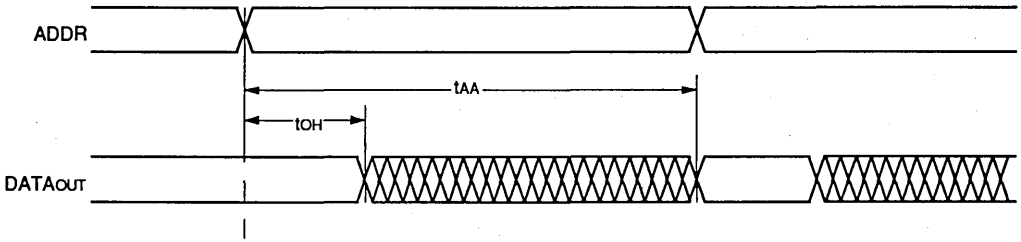
2789 tbl 12

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. Read Data is valid at t_{AA} or t_{AHO} - t_{OLEL} + t_{DR}, whichever is larger; that is, Read Data is valid at the access time unless Output Latch Enable is high, and then access is t_{DR} after $\overline{OLE}$ goes low.

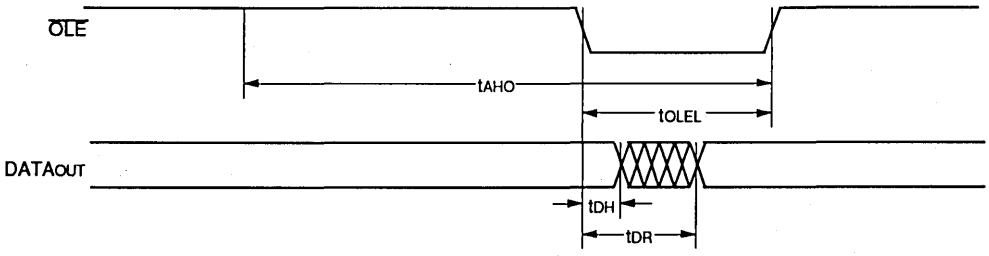
READ CYCLE GATED BY CHIP SELECT



READ CYCLE GATED BY ADDRESS



OUTPUT LATCH TIMING



2789 drw 09

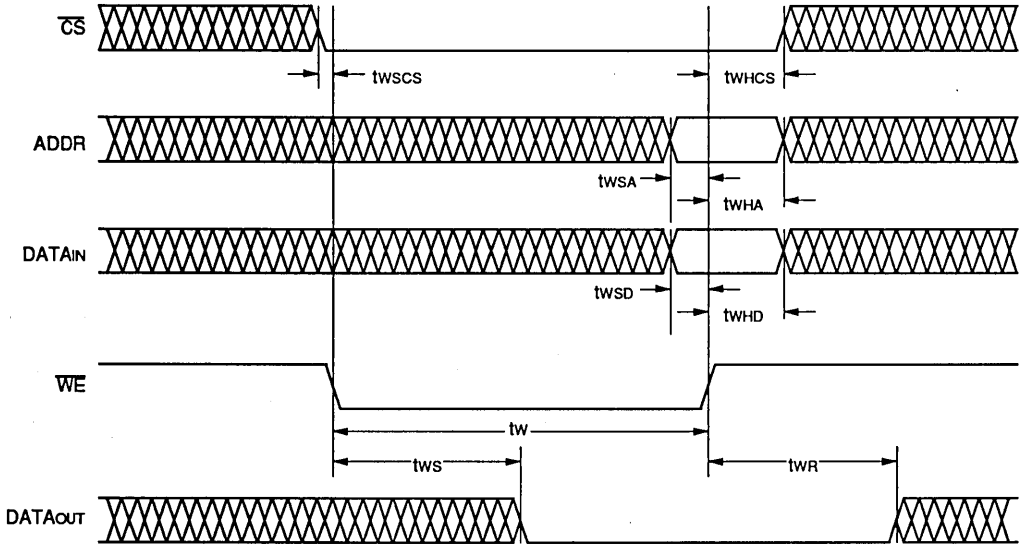
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10507S12 100507S12 101507S12		10507S15 100507S15 101507S15		Unit
			Min.	Max.	Min.	Max.	
Write Cycle							
tW	Write Pulse Width	–	10	–	12	–	ns
tWSCS	Setup Time for Chip Select	–	0	–	1	–	ns
tWSA	Setup Time for Address	–	1	–	1	–	ns
tWSD	Setup Time for Data In	–	1	–	1	–	ns
tWHCS	Hold Time for Chip Select	–	2	–	2	–	ns
tWHA	Hold Time for Address	–	2	–	2	–	ns
tWHD	Hold Time for Data In	–	2	–	2	–	ns
tWS	Write Disable Time	–	–	5	–	5	ns
tWR	Write Recovery Time	–	–	5	–	5	ns

NOTE:
1. Input and Output reference level is 50% point of waveform.

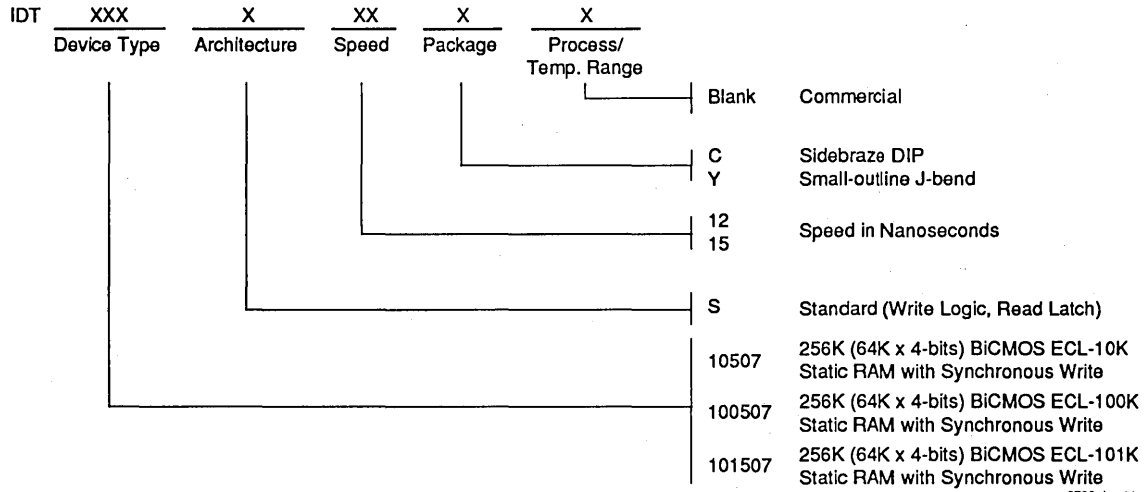
2789 tbl 13

WRITE CYCLE TIMING DIAGRAM



2789 drw 10

ORDERING INFORMATION



2789 drw 11

5

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 256K (64K x 4-BIT) with CONDITIONAL WRITE

ADVANCE INFORMATION
IDT10508
IDT100508
IDT101508

FEATURES:

- 65,535-words x 4-bit organization
- Address access time: 12/15 ns
- Read Data output latch for extended hold time
- Short Write Cycle input data and address valid time
- Write Cycle may be terminated very late in the cycle
- Pin compatible with standard 64Kx4
- Through-hole DIP and surface-mount packages

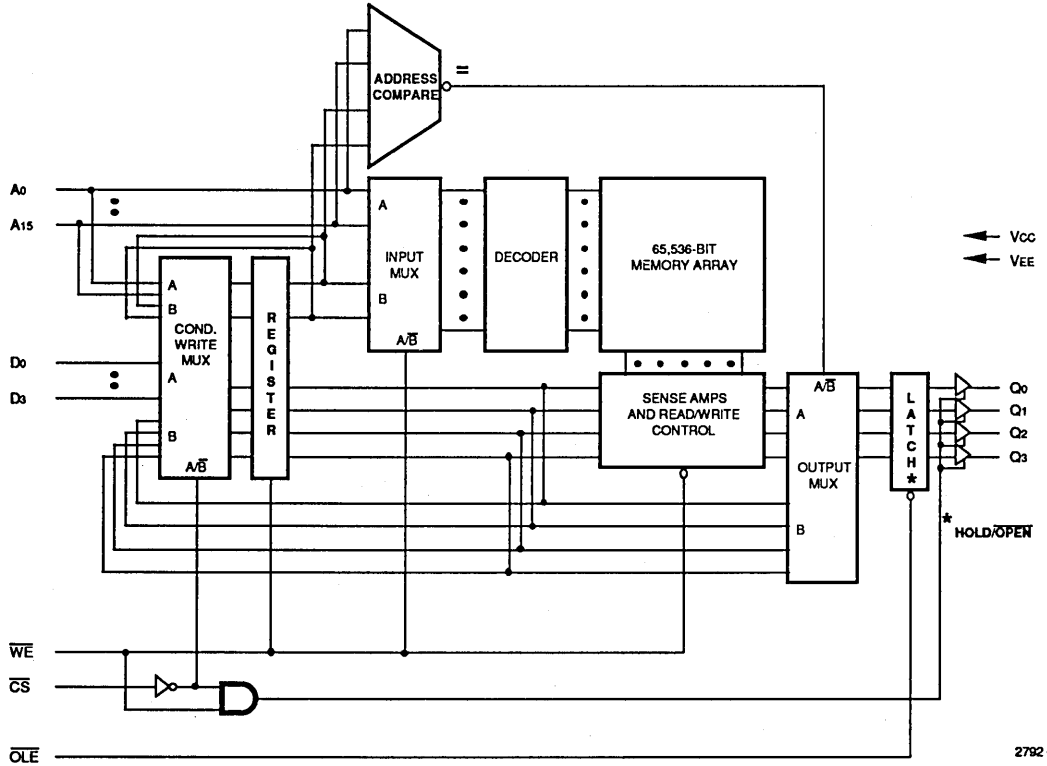
DESCRIPTION:

The IDT10508, IDT100508 and IDT101508 are 262,144-bit high-speed BiCEMOS™ ECL static random access memories organized as 64K x 4, with inputs and outputs fully compatible with ECL levels. Internal registers on inputs provide enhanced Write Cycle performance over conventional RAMs, while output read data latch allows longer output data hold time providing easier design and improved system level cycle times.

In the read mode, this device is pinout and timing compatible with the standard asynchronous SRAMs (IDT10504), yet the addition of an output latch with separate enable control allow output data to be captured and held long into the next cycle. This minimizes noise on the data bus and provides better set-up time margin for the next logic stage in pipelined applications.

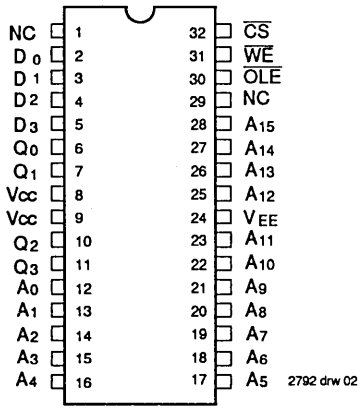
In the write mode, the device adds an invisible pipeline stage in the write address and data paths, allowing very short set-up and hold times for these inputs and less stringent requirements for the write pulse input. Additionally, the address and data paths to the input register are gated by the Conditional Write Multiplexor, which allows termination of a Write cycle late in the cycle.

FUNCTIONAL BLOCK DIAGRAM

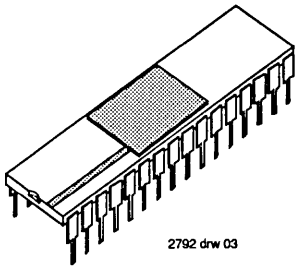


BiCEMOS is a trademark of Integrated Device Technology, Inc.

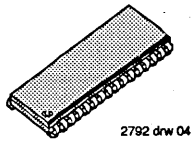
PIN CONFIGURATION



TOP VIEW



400-Mil-Wide
CERAMIC PACKAGE
C32



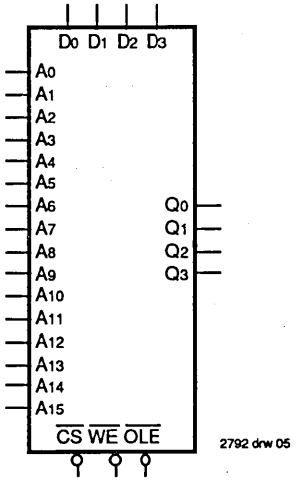
300-Mil-Wide
PLASTIC SOJ PACKAGE
Y32

PIN DESCRIPTIONS

Symbol	Pin Name
A0 through A15	Address Inputs
D0 through D3	Data Inputs
Q0 through Q3	Data Outputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input (Internal pull down)
$\overline{OLE}$	Output Latch Enable
VEE	More Negative Supply Voltage
Vcc	Less Negative Supply Voltage

2792 tbl 01

LOGIC SYMBOL



64Kx4
SRAM

AC OPERATING RANGES(1)

I/O	VEE	Temperature
10K	-5.2V ±5%	0 TO 75°C, air flow exceeding 2 m/sec
100K	-4.5V ±5%	0 TO 85°C, air flow exceeding 2 m/sec
101K	-4.75V to -5.46V	0 TO 75°C, air flow exceeding 2 m/sec

2792 tbl 02

NOTE:
1. Referenced to Vcc

CAPACITANCE (TA=+25°C, f=1.0MHz)

Symbol	Parameter	DIP Typ.	DIP Max.	SOJ Typ.	SOJ Max.	Unit
CIN	Input Capacitance	4	–	3	–	pF
COUT	Output Capacitance	6	–	3	–	pF

2792 tbl 03

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	$\overline{OLE}$	Data OUT (2)	Function
H	X	X	L	Deselected
L	H	L	RAM Data	Read
L	H	H	RAM Data	Output Held
L	L	X	L	Write

2792 tbl 04

NOTES:
1. H=High, L=Low, X=Don't Care
2. DATAOUT initiated by falling edge of $\overline{OLE}$.

ECL-10K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2792 tbl 05

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-10K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L = 50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit	T_A
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA	–
			Others	–	–	110	µA	–
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA	–
			Others	-50	–	90	µA	–
I_{EE}	Supply Current	All Inputs and Outputs Open		-280	-220	–	mA	–

2792 tbl 06

NOTE:

1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

ECL-100K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +85	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2792 tbl 07

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-100K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.5V, R_L = 50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-260	-200	–	mA

2792 tbl 08

NOTE:
1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.

ECL-101K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2792 tbl 09

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-101K DC ELECTRICAL CHARACTERISTICS

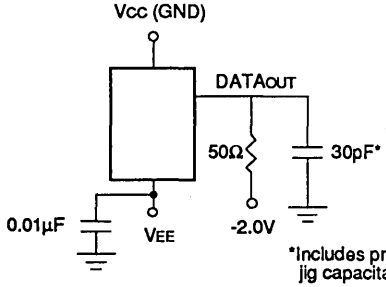
(V_{EE} = -5.2V, R_L = 50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Condition		Min. (B)	Typ.[1]	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-280	-220	–	mA

2792 tbl 10

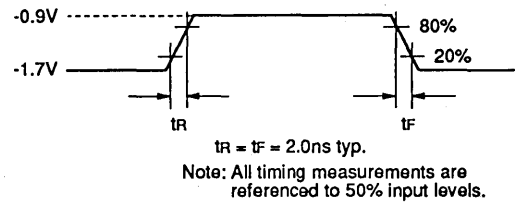
NOTE:
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

AC TEST LOAD CONDITION



2792 drw 06

AC TEST INPUT PULSE



2792 drw 07

RISE/FALL TIME

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_R	Output Rise Time	–	–	2	–	ns
t_F	Output Fall Time	–	–	2	–	ns

2792 tbl 11

FUNCTIONAL DESCRIPTION

The IDT10508, IDT100508, and IDT101508 BiCMOS ECL static RAMs (SRAM) with CONDITIONAL WRITE provide high speed with low power dissipation typical of BiCMOS ECL. On-chip logic additionally helps improve system performance, yet the device is pinout-compatible with asynchronous equivalents (i.e... IDT10504, IDT100504, and IDT101504 respectively). The ECL-101K meets electrical specifications that combine the ECL-100K temperature and voltage compensated output levels with the high-speed of ECL-10K VEE compatibility (-5.2V).

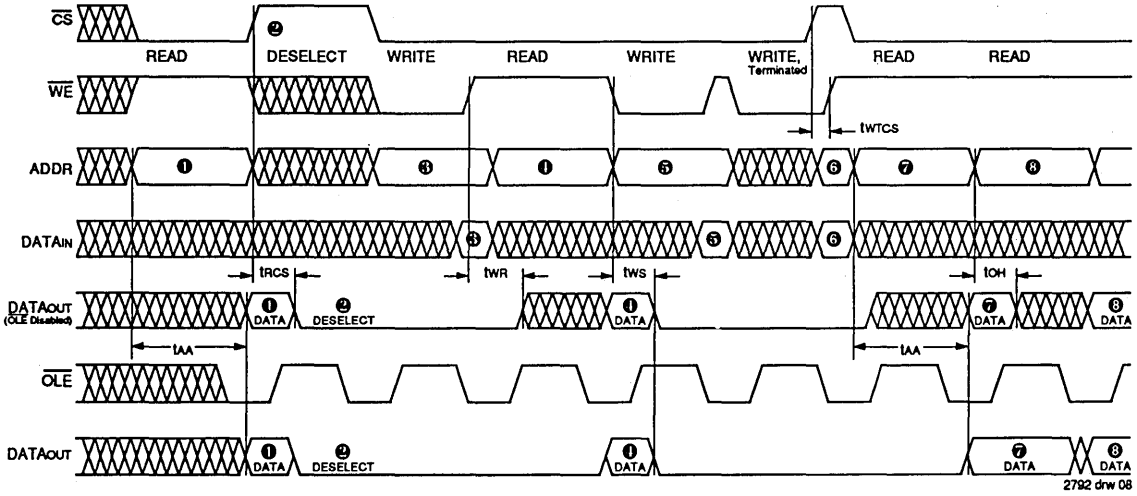
As can be seen in the Functional Block Diagram on the title page, this device contains clocked input registers to sample and hold addresses and input data, during a write cycle only. Inputs are sampled on the rising edge of the Write Enable ($\overline{WE}$). The write cycle is pipelined: the memory cell is written during the $\overline{WE}$-low time in the next cycle. Additionally, the address and data paths to the input register are gated by the Conditional Write Multiplexor, which allows termination of a Write cycle late in the cycle.

Read cycles are not pipelined and operate identically to an asynchronous device, except that an output latch is provided to capture and hold Read data.

READ TIMING

The read timing on the device is asynchronous. DataOUT is held low until the device is selected by Chip Select ($\overline{CS}$).

FUNCTIONAL DESCRIPTION TIMING EXAMPLE



2792 drw 08

Then Address (ADDR) settles and data appears on the output after time t_{AA}, as at ❶ below.

$Data_{OUT}$ is held for a short time (t_{OH}) after the address begins to change for the next access, as can be seen at ❼ — allowing addresses to begin to change early for the next cycle — then ambiguous data is on the bus until a new time t_{AA}.

To avoid this noise on the bus and provide for longer output hold time, this device includes an output Read data latch which allows Read data to flow out while Output Latch Enable ($\overline{OLE}$) is low, and then hold when $\overline{OLE}$ is high. Thus in the example below Read data at ❼ is held until Read data at ❽ is ready for output.

Note that $Data_{OUT}$ is disabled (held low) by $\overline{CS}$ high or $\overline{WE}$ low, regardless of the state of the Output Latch.

DESELECT TIMING

Deselect timing is identical to a standard asynchronous device. This case occurs at ❷ below. Outputs attain the disable state (low) t_{RCS} later Chip Select ($\overline{CS}$) is taken to a high logic state. Status of other inputs do not effect the disabling of the device when chip select is de-asserted.

WRITE TIMING

Write cycles pipelined to allow easier design and higher system performance. The write pulse created on the $\overline{WE}$ input is used as a strobe to clock in the Write Address and Data into a register. This address and data are held in the register until the next write cycle, when they are used to write into the memory array through the Input Multiplexor.

Note the very short valid window required for Write Address and Data inputs. This is because these signals are captured by the input register. This means that input data may arrive late in the cycle, as at ❸ below, or data and address may arrive late, as at ❻ below.

$Data_{OUT}$ is disabled during the Write Cycle. If $\overline{CS}$ is held low (active) and addresses remain unchanged, the $Data_{OUT}$ pins will output the written data after "Write Recovery Time" (t_{WR}), as for a standard asynchronous device.

There is a special case when a Read cycle follows directly a Write Cycle to the same address. The memory array has not yet been updated with the Write data — it is still in the input register. This case is handled by including an address comparator and Output Multiplexor on the device: if the address being presented on the input pins is the same as the address stored in the input register, the data presented to the output pins is also from the input register.

CONDITIONAL WRITE

In certain system architectures, the decision whether to write data within a cycle occurs late in the cycle. An example might be cache hit logic taking time to decide if a cache line needs to be updated. This device allows a write to be initiated, yet terminated very late in the cycle by using Chip Select should a write not be required by the system.

The Conditional Write Multiplexor controlled by Chip Select makes this possible. In a normal Write cycle, $\overline{CS}$ is low and the Multiplexor delivers the state of the addresses and data on the input pins to the Input Multiplexor and Input Register, respectively. Because $\overline{CS}$ does not gate the Write Pulse logic, it has a short valid window requirement.

To terminate the Write cycle, as shown at ❻ below, all that is required is to bring $\overline{CS}$ to a high logic state. This switches the Conditional Write Multiplexor to circulate the previously written address and data (held in the Input Register) around to be clocked again into the Input Register. No Write cycle is apparent to the system.

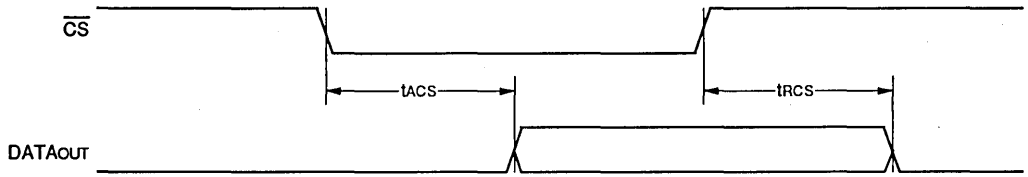
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10508S12 100508S12 101508S12		10508S15 100508S15 101508S15		Unit
			Min.	Max.	Min.	Max.	
Read Cycle							
t_{AA}[2]	Address Access Time	–	–	12	–	15	ns
t_{ACS}	Chip Select Access Time	–	–	5	–	5	ns
t_{RCS}	Chip Select Recovery Time	–	–	5	–	5	ns
t_{OH}	Data Hold from Address Change	–	3	–	3	–	ns
t_{OLEL}	Latch Enable Low Pulse Width	–	5	–	5	–	ns
t_{AHO}	Address Valid to $\overline{OLE}$ High	–	14	–	17	–	ns
t_{DH}	Data Hold from Clock Low	–	0	–	0	–	ns
t_{DR}	Data Ready from Clock Low	–	0	4	0	4	ns

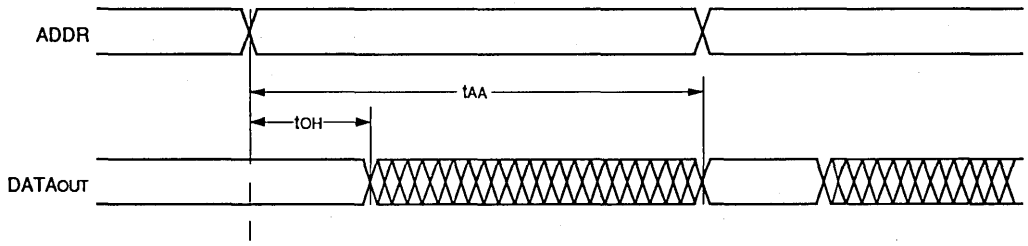
2792 tbl 12

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. Read Data is valid at t_{AA} or t_{AHO} - t_{OLEL} + t_{DR}, whichever is larger; that is, Read Data is valid at the access time unless Output Latch Enable is high, and then access is t_{DR} after $\overline{OLE}$ goes low.

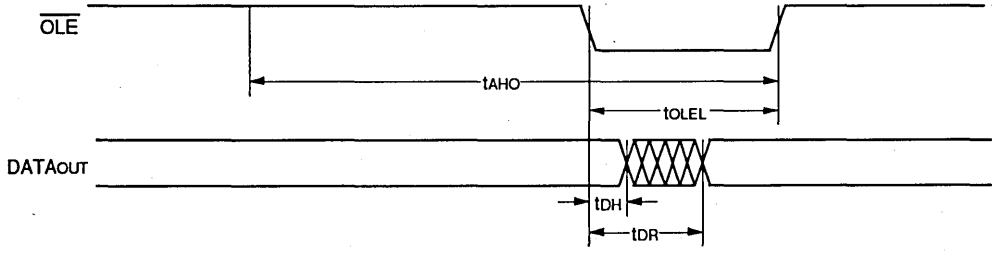
READ CYCLE GATED BY CHIP SELECT



READ CYCLE GATED BY ADDRESS



OUTPUT LATCH TIMING



2792 drw 09

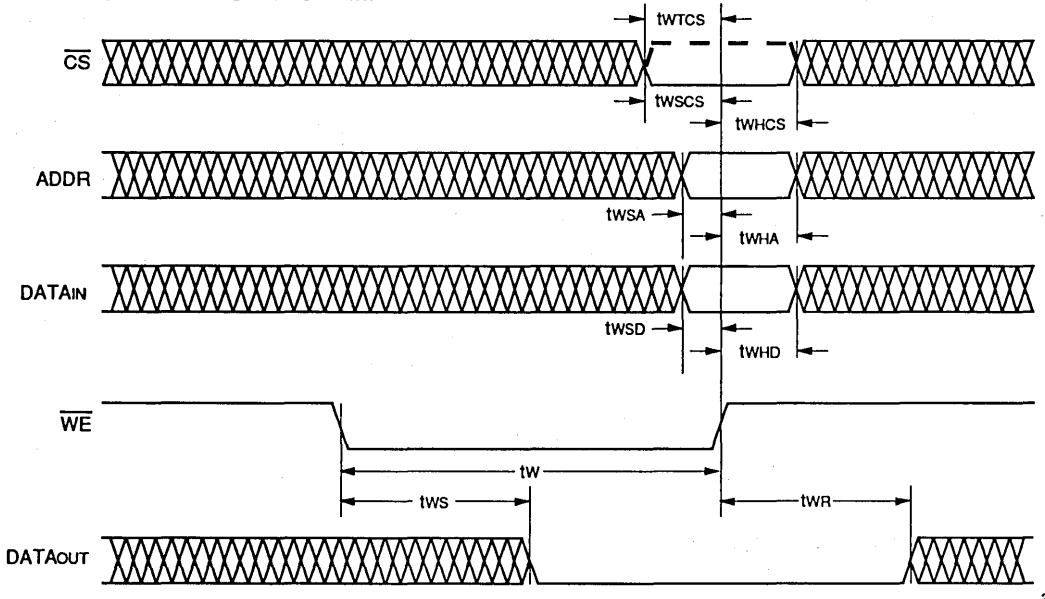
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10508S12 100508S12 101508S12		10508S15 100508S15 101508S15		Unit
			Min.	Max.	Min.	Max.	
Write Cycle							
tW	Write Pulse Width	–	10	–	12	–	ns
tWSCS	Setup Time for Chip Select	–	1	–	1	–	ns
tWTCS	$\overline{CS}$ Set-Up, Terminated Write	–	2	–	2	–	ns
tWSA	Setup Time for Address	–	1	–	1	–	ns
tWSD	Setup Time for Data In	–	1	–	1	–	ns
tWHCS	Hold Time for Chip Select	–	2	–	2	–	ns
tWHA	Hold Time for Address	–	2	–	2	–	ns
tWHD	Hold Time for Data In	–	2	–	2	–	ns
tWS	Write Disable Time	–	–	5	–	5	ns
tWR	Write Recovery Time	–	–	5	–	5	ns

NOTE:
1. Input and Output reference level is 50% point of waveform.

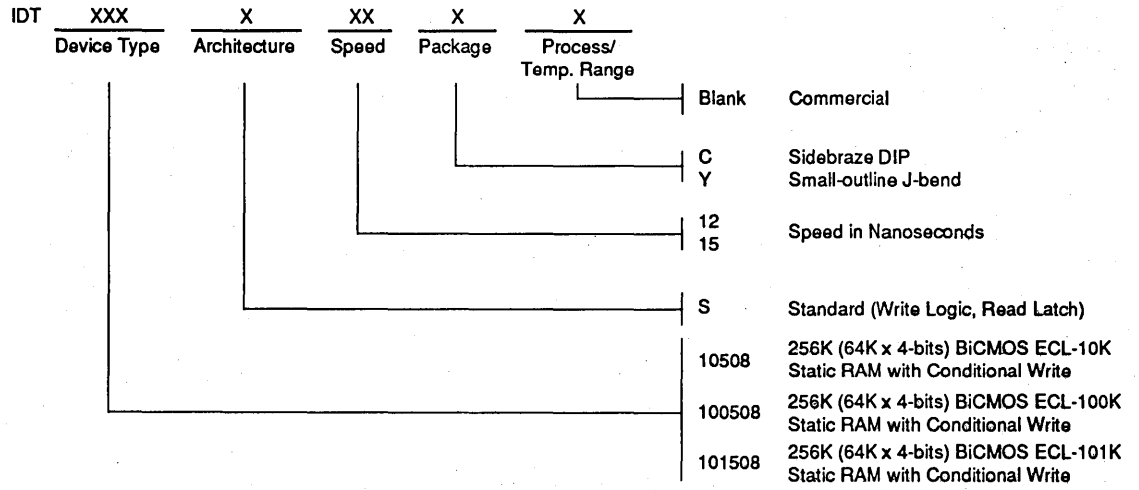
2792 tbl 13

WRITE CYCLE TIMING DIAGRAM



2792 drw 10

ORDERING INFORMATION



2792 drw 11

5

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 256K (32K x 9-BIT) SRAM

PRELIMINARY
IDT10509D
IDT100509D
IDT101509D

FEATURES:

- 32,768-words x 9-bit organization
- Address access time: 8/10/12/15
- Wide word for reduced address loading
- Guaranteed Output Hold time
- Differential Write Clock and Single-Ended Write Enable
- Fully compatible with ECL logic levels
- Separate data input and output
- Standard pinouts

DESCRIPTION:

The IDT10509D, IDT100509D and IDT101509D are 294,912-bit high-speed BiCEMOS™ ECL static random access memories organized as 32Kx9, with separate data inputs and outputs. All I/Os are fully compatible with ECL levels.

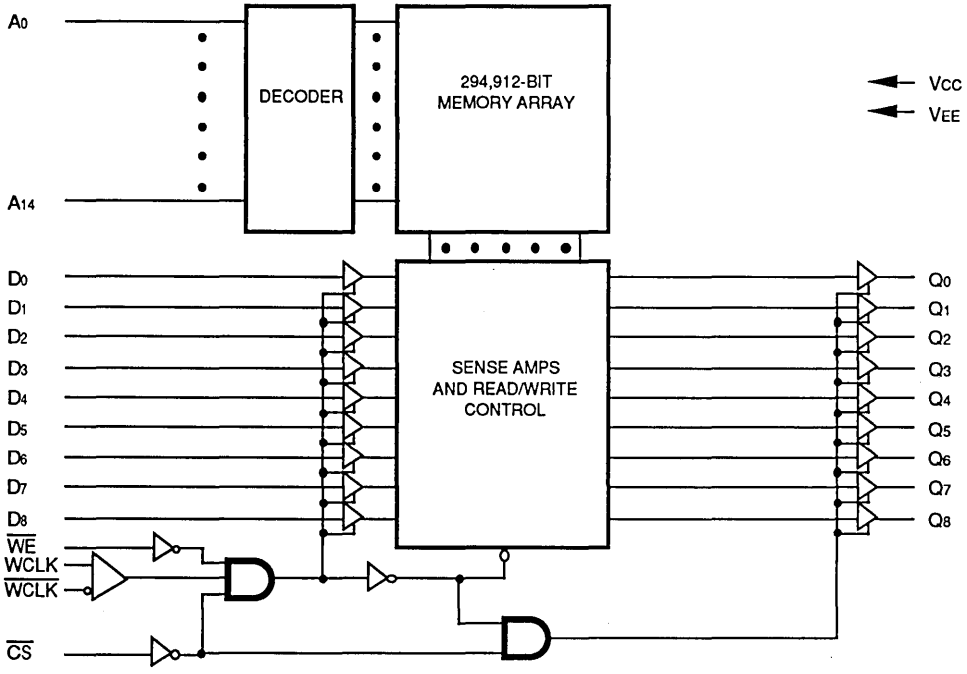
These devices are part of a family of nine-bit-wide ECL SRAMs. The devices have been configured to follow the proposed ECL SRAM JEDEC pinout. Because they are manufactured in BiCEMOS™ technology, however, power dissipation is similar to CMOS devices of equivalent density.

The asynchronous SRAMs are the most straightforward to use because no additional clocks or controls are required: DataOUT is available an access time after the last change of address.

The fast access time and guaranteed Output Hold time allow greater margin for system timing variation.

To write data into this device requires the creation of a Write Pulse, which is the combination of the Write Enable and the Write Clock. The differential Write Clock ensures easy creation of a clean write pulse throughout the memory array, reducing requirements on the skew of Write Enable with respect to addresses. Write cycles can be operated in traditional manner by disabling the Write-Clock and using the Write Enable only. Write cycle disables the output pins in conventional fashion.

FUNCTIONAL BLOCK DIAGRAM



2810 drw 01

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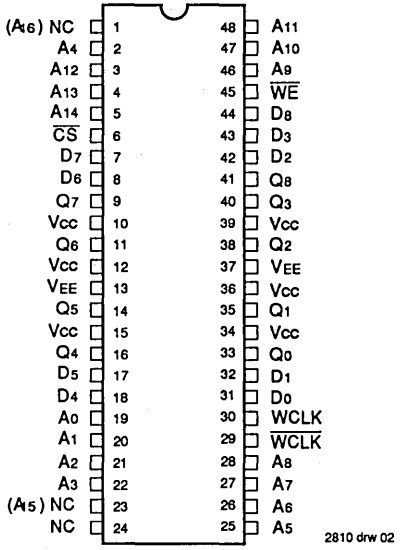
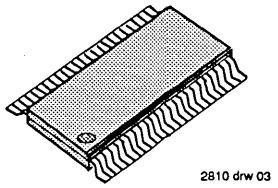
PIN CONFIGURATION



2810 drw 02

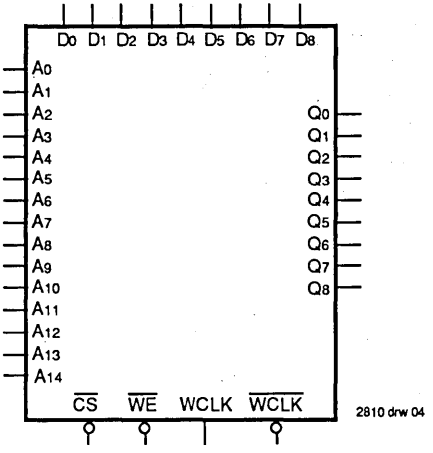
TOP VIEW



2810 drw 03

300-Mil-Wide
Plastic SSOP Package
48

LOGIC SYMBOL



2810 drw 04

32Kx9
SRAM

PIN DESCRIPTIONS

Symbol	Pin Name
A0 through A14	Address Inputs
D0 through D8	Data Inputs
Q0 through Q8	Data Outputs
$\overline{CS}$	Chip Select Input (Internal pull down)
$\overline{WE}$	Write Enable Input
$\overline{WCLK}$, WCLK	Differential Write Clock Inputs
VEE	More Negative Supply Voltage
Vcc	Less Negative Supply Voltage
NC	No Connect (Not internally bonded)

2810 tbl 01

AC OPERATING RANGES(1)

I/O	VEE	Temperature
10K	-5.2V ±5%	0 TO 75°C, air flow exceeding 2 m/sec
100K	-4.5V ±5%	0 TO 85°C, air flow exceeding 2 m/sec
101K	-4.75V to -5.46V	0 TO 75°C, air flow exceeding 2 m/sec

2810 tbl 02

NOTE:
1. Referenced to Vcc

CAPACITANCE (TA=+25°C, f=1.0MHz)

Symbol	Parameter	SSOP Typ.	SSOP Max.	Unit
CIN	Input Capacitance	TBD	–	pF
COUT	Output Capacitance	TBD	–	pF

2810 tbl 03

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	WCLK	$\overline{WCLK}$	Data OUT	Function
H	X	X	X	L	Deselected
L	H	X	X	RAM Data	Read
L	X	L	H	RAM Data	Read
L	L	H	L	L	Write, Diff. Clock
L	L	VEE	L	L	Write, Low Clock
L	L	H	VEE	L	Write, High Clock
L	L	VEE	VEE	L	Write, Single Enable

2810 tbl 04

NOTE:
1. H=High, L=Low, X=Don't Care

ECL-10K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2810 tbl 05

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this

ECL-10K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L = 50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit	T_A
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA	–
			Others	–	–	110	µA	–
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA	–
			Others	-50	–	90	µA	–
I_{EE}	Supply Current	All Inputs and Outputs Open		-280	-220	–	mA	–

2810 tbl 06

NOTE:
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

ECL-100K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +85	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2810 tbl 07

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-100K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.5V, R_L = 50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-260	-200	–	mA

2810 tbl 08

NOTE:
1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.

5

ECL-101K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2810 tbl 09

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-101K DC ELECTRICAL CHARACTERISTICS

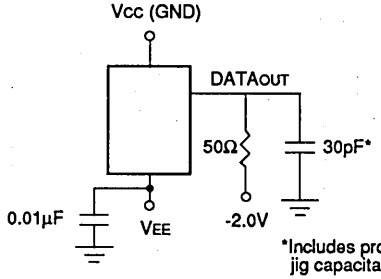
(V_{EE} = -5.2V, R_L = 50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Condition		Min. (B)	Typ.(1)	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-280	-220	–	mA

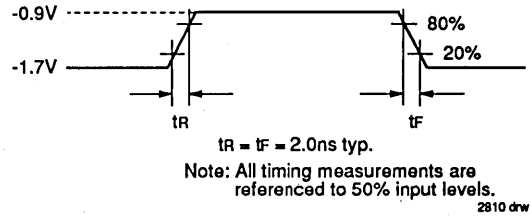
2810 tbl 10

NOTE:
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

AC TEST LOAD CONDITION



AC TEST INPUT PULSE



RISE/FALL TIME

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
tR	Output Rise Time	–	–	2	–	ns
tF	Output Fall Time	–	–	2	–	ns

2810 tbl 11

FUNCTIONAL DESCRIPTION

The IDT10509D, IDT100509D, and IDT101509D BiCMOS ECL static RAMs (SRAM) provide high speed with low power dissipation typical of BiCMOS ECL. These devices follow the proposed pinout and functionality for 32Kx9 ECL SRAMs. The ECL-101K meets electrical specifications that combine the ECL-100K temperature and voltage compensated output levels with the high-speed of ECL-10K VEE compatibility (-5.2V).

READ TIMING

The read timing on these asynchronous devices is straightforward. DataOUT is held low until the device is selected by Chip Select ($\overline{CS}$). Then Address (ADDR) settles and data appears on the output after time tAA. Note that DataOUT is held for a short time (tOH) after the address begins to change for the next access, then ambiguous data is on the bus until a new time tAA.

WRITE TIMING

To write data to the device, a Write Pulse need be formed to control the write to the SRAM array. This device includes on-board logic that provides an internal Write Pulse defined as the logical NOT-AND combination (i.e. NOR, see block diagram) of Write Clock ($\overline{WCLK}$) asserted low and the Write Enable ($\overline{WE}$) asserted low. Note that the Write Clock is a differential input allowing for greater noise rejection and cleaner signal forming over the memory array. This combination of signals is useful for the development of the very short Write Pulse that asynchronous SRAMs need: Write Clock is a carefully formed free-running signal that is de-skewed over the memory array layout; Write Enable is a control signal that can be generated and delivered with the same skew tolerance as address signals.

While $\overline{CS}$, ADDR, and DataIN must be valid when Write Pulse (see definition above) goes low. Data is written to the memory cell at the end of the Write Pulse, and inputs must be held after the rising edge of the Write Pulse to ensure satisfactory completion of the cycle.

DataOUT is disabled (held low) during the Write Cycle. If $\overline{CS}$ is held low (active) and addresses remain unchanged, the DataOUT pins will output the written data after "Write Recovery Time" (tWR).

Because of the very short Write Pulse requirement, these devices can be cycled as quickly for Writes as for Reads. Balanced cycles mean simpler timing in cache applications.

ALTERNATIVE WRITE OPERATION

The device may also be used other Write Pulse modes, if preferred. The Write Clock input may be converted from differential to single-ended operation as described in the Truth Table. The Write Clock may be disabled altogether, and only the Write Enable used to form Write Pulse, by externally connecting both inputs of the differential Write Clock (WCLK and $\overline{WCLK}$) to the VEE supply voltage.

Tying the positive side of the differential Write Clock (WCLK) to the VEE voltage will allow for two single-ended write enables, $\overline{WE}$ and $\overline{WCLK}$. The internal Write Pulse is in Write mode when both are low.

Tying the negative side of the differential Write Clock ($\overline{WCLK}$) to the VEE voltage will allow for two single-ended write enables, $\overline{WE}$ and WCLK. The internal Write Pulse is in Write mode when $\overline{WE}$ is low and WCLK is high.

5

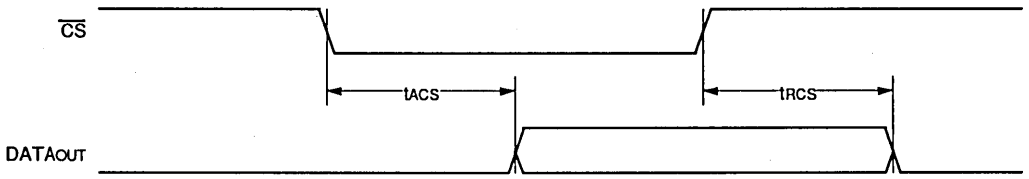
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10509D8 100509D8 101509D8		10509D10 100509D10 101509D10		10509D12 100509D12 101509D12		10509D15 100509D15 101509D15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle											
tACS	Chip Select Access Time	–	–	5	–	5	–	5	–	5	ns
tRCS	Chip Select Recovery Time	–	–	5	–	5	–	5	–	5	ns
tAA	Address Access Time	–	–	8	–	10	–	12	–	15	ns
tOH	Data Hold from Address Change	–	3	–	3	–	3	–	3	–	ns

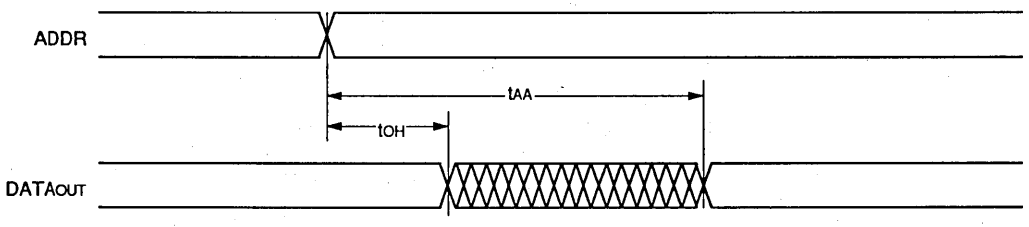
NOTE:
1. Input and Output reference level is 50% point of waveform.

2810 tbl 12

READ CYCLE GATED BY CHIP SELECT



READ CYCLE GATED BY ADDRESS



2810 drw 07

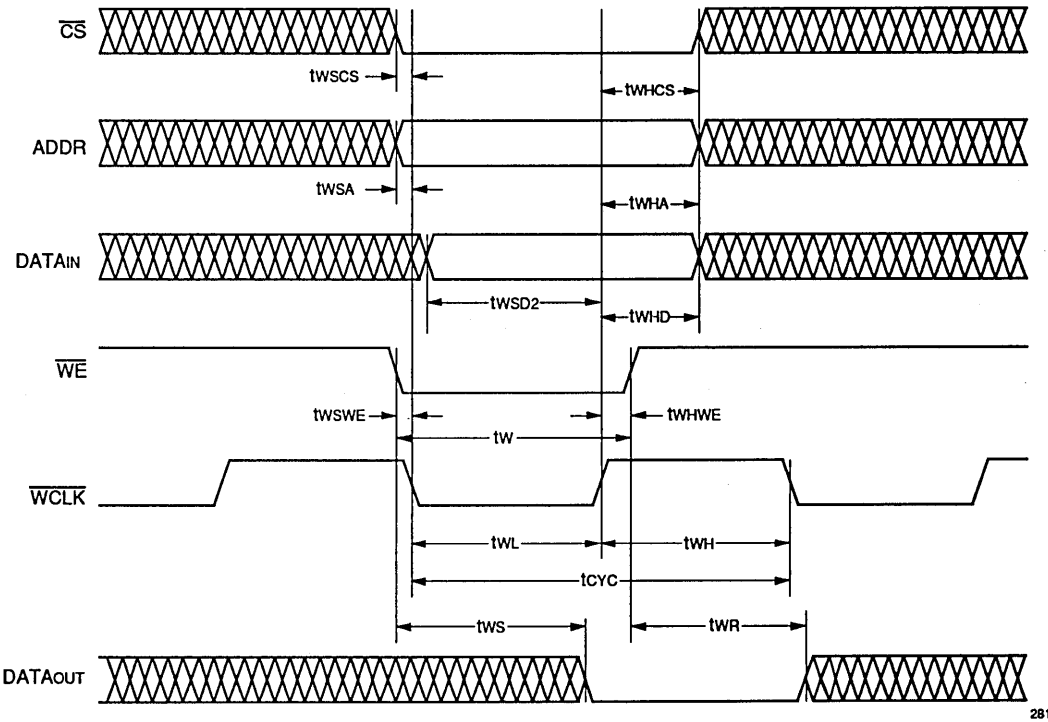
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter [1]	Test Condition	10509D8 100509D8 101509D8		10509D10 100509D10 101509D10		10509D12 100509D12 101509D12		10509D15 100509D15 101509D15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle											
tCYC	Cycle Time	–	8	–	10	–	12	–	15	–	ns
tW	Write Enable Pulse Width	–	6	–	8	–	10	–	13	–	ns
tWL	$\overline{WCLK}$ Low Pulse Width	–	6	–	8	–	10	–	13	–	ns
tWH	$\overline{WCLK}$ High Pulse Width	–	2	–	2	–	2	–	2	–	ns
tWSCS	Chip Select Set-up Time	–	0	–	0	–	0	–	0	–	ns
tWSA	Address Set-up Time	–	0	–	0	–	0	–	0	–	ns
tWSD2	Data Set-up Time	–	6	–	8	–	10	–	13	–	ns
tWSWE	Write Enable Set-up Time	–	0	–	0	–	0	–	0	–	ns
tWHCS[2]	Chip Select Hold Time	–	1	–	1	–	1	–	2	–	ns
tWHA[2]	Address Hold Time	–	1	–	1	–	1	–	2	–	ns
tWHD[2]	Data Hold Time	–	1	–	1	–	1	–	2	–	ns
tWHWE[2]	Write Enable Hold Time	–	0	–	0	–	0	–	0	–	ns
tWS	Write Disable Time	–	–	5	–	5	–	5	–	5	ns
tWR[3]	Write Recovery Time	–	–	5	–	5	–	5	–	5	ns

2810 tbl 13

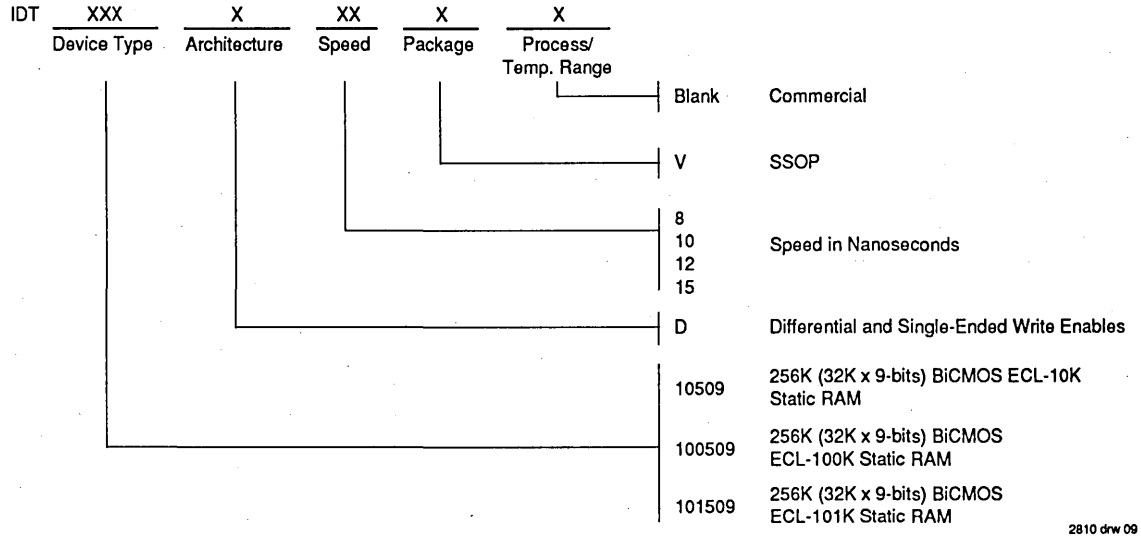
NOTES:
1. Input and Output reference level is 50% point of waveform.
2. Write Pulse Width is the logical NOT-AND of $\overline{WE1}$ and $\overline{WE2}$, that is, when both are logical low.
3. tWRis defined as the time to reflect the newly written data on the Data Outputs (Q_0 to Q_3) when no new Address Transition occurs.

WRITE CYCLE TIMING DIAGRAM



2810 drw 08

ORDERING INFORMATION



2810 drw 09

FIFO MEMORIES

Integration of IDT high-speed static RAM technology with internal support logic yields high-performance, high-density FIFO memories. A FIFO is used as a memory buffer between two asynchronous systems with simultaneous read/write access. The data rate between the two systems can be regulated by monitoring the status flags and throttling the read and write accesses. Since these FIFOs are built with an internal RAM pointer architecture, there is no fall-through time between a write to a memory location and a read from that memory location. System performance is significantly improved over the shift register-based architecture of previous FIFO designs which are handicapped with long fall-through times.

IDT offers the widest selection of monolithic FIFOs, ranging from shallows 64x4 and 64x5 to the high-density 16Kx9. Shallow FIFOs regulate data flow in tightly couped computational engines. High-density FIFOs store large blocks in networking, telecommunication and data storage systems. The IDT7200 FIFO family (256x9 through the 16Kx9 FIFOs) are all pin and function compatible, making density upgrades simple. All IDT FIFOs can be cascaded to greater word depths and expanded to greater word widths with no external support logic.

IDT's high-speed SyncFIFO™ is ideal for multiprocessor systems, workstations and high-end graphics. The innovative architecture of the SyncFIFO (internal I/O registers with separate clock and enable inputs), along with wider data bus, simplifies design and reduces interface logic.

The Parallel-Serial FIFOs incorporate a serial input or a serial output shifter for serial-to-parallel or parallel-to-serial bus interface. The Parallel-Serial FIFOs also offer six status flags for flexible data throttling.

A variety of packages are available: standard plastic DIP and CERDIP, surface mount ceramic LCC, PLCC and SOIC, and high-reliability flatpack. Increasing board density is the overwhelming goal of IDT's package development efforts, as demonstrated by the introduction of the 300 mil ThinDIP.

FIFO modules, composed of four LCC devices mounted on a multi-layer co-fired ceramic substrate, increase densities to 32Kx18 which are pin-compatible with current monolithic versions.

IDT is committed to offering FIFOs of increasing density, speed and enhanced architectural innovations, such as Flexishift™ and the BiFIFO, for easier system interface.

TABLE OF CONTENTS

Integrated Device Technology, Inc.

CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 256 x 9-BIT & 512 x 9-BIT

IDT7200S/L
IDT7201SA/LA

FEATURES:

- First-In/First-Out dual-port memory
- 256 x 9 organization (IDT7200)
- 512 x 9 organization (IDT7201A)
- Low power consumption
  - — Active: 770mW (max.)
  - — Power-down: 27.5mW (max.)
- Ultra high speed—15ns access time
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Pin and functionally compatible with 720X family
- Status Flags: Empty, Half-Full, Full
- Auto-retransmit capability
- High-performance CEMOS™ technology
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-87531, 5962-89666, and 5962-89863 are listed on this function.

DESCRIPTION:

The IDT7200/7201A are dual-port memories that load and empty data on a first-in/first-out basis. The devices use Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the devices through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins. The devices have a read/write cycle time of 25ns (40MHz).

The devices utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features a Retransmit ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed low to allow for retransmission from the beginning of data. A Half-Full Flag is available in the single device mode and width expansion modes.

The IDT7200/1A is fabricated using IDT's high-speed CEMOS technology. They are designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

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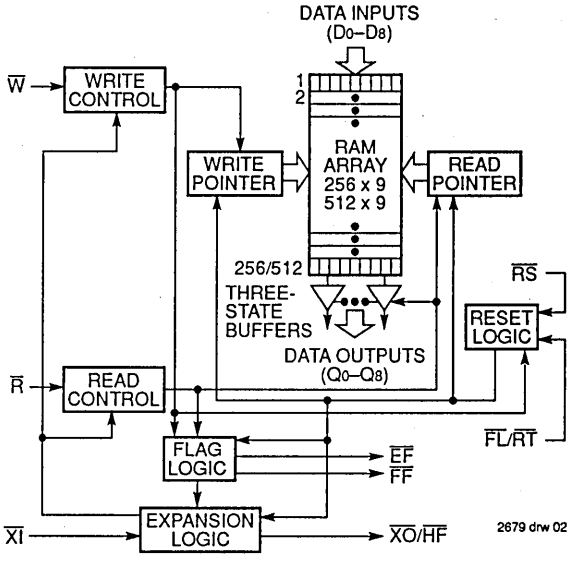
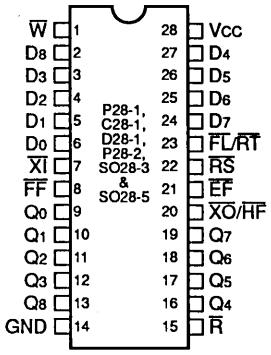
FUNCTIONAL BLOCK DIAGRAM

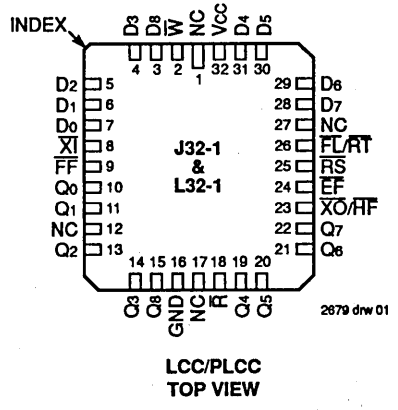


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP/SOIC/FLATPACK
TOP VIEW



LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +155	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2679 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

CAPACITANCE (TA = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Condition	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE: 2679 tbl 02

1. This parameter is sampled and not 100% tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH(1)	Input High Voltage Commercial	2.0	—	—	V
VIH(1)	Input High Voltage Mlitary	2.2	—	—	V
VIL(2)	Input Low Voltage Commercial and Military	—	—	0.8	V

NOTE: 2679 tbl 03

1. VIH = 2.6V for $\overline{XI}$ input (commercial).
   VIH = 2.8V for $\overline{XI}$ input (military).
2. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V±10%, T_A = −55°C to +125°C)

		IDT7200 IDT7201 Commercial t_A = 15,20ns			IDT7200 IDT7201 Military t_A = 20ns			IDT7200 IDT7201 Commercial t_A = 25,35ns			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
I_{LI}[1]	Input Leakage Current (Any Input)	−1	—	1	−10	—	10	−1	—	1	µA
I_{LO}[2]	Output Leakage Current	−10	—	10	−10	—	10	−10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OH} = −2mA	2.4	—	—	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OH} = 8mA	—	—	0.4	—	—	0.4	—	—	0.4	V
I_{CC1}[3]	Active Power Supply Current	—	—	140[4]	—	—	160[4]	—	—	125[4]	mA
I_{CC2}[3]	Standby Current ($\overline{R}$=$\overline{W}$=$\overline{RS}$=$\overline{FL/RT}$=V_{IH})	—	—	15	—	—	20	—	—	15	mA
$I_{CC3(L)}$[3]	Power Down Current (All Input = V_{CC} - 0.2V)	—	—	5	—	—	9	—	—	0.5	mA
$I_{CC3(S)}$[3]	Power Down Current (All Input = V_{CC} - 0.2V)							—	—	5	mA

2679 tbl 04

DC ELECTRICAL CHARACTERISTICS (Continued)

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V±10%, T_A = −55°C to +125°C)

		IDT7200 IDT7201 Military t_A = 30,40ns			IDT7200 IDT7201 Commercial t_A = 50,65,80,120ns			IDT7200 IDT7201 Military t_A = 50,65,80,120ns			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
I_{LI}[1]	Input Leakage Current (Any Input)	−10	—	10	−1	—	1	−10	—	10	µA
I_{LO}[2]	Output Leakage Current	−10	—	10	−10	—	10	−10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OH} = −2mA	2.4	—	—	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OH} = 8mA	—	—	0.4	—	—	0.4	—	—	0.4	V
I_{CC1}[3]	Active Power Supply Current	—	—	140[4]	—	50	80	—	70	100	mA
I_{CC2}[3]	Standby Current ($\overline{R}$=$\overline{W}$=$\overline{RS}$=$\overline{FL/RT}$=V_{IH})	—	—	20	—	5	8	—	8	15	mA
$I_{CC3(L)}$[3]	Power Down Current (All Input = V_{CC} - 0.2V)	—	—	0.9	—	—	0.5	—	—	0.9	mA
$I_{CC3(S)}$[3]	Power Down Current (All Input = V_{CC} - 0.2V)	—	—	9	—	—	5	—	—	9	mA

2679 tbl 05

NOTES:
1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Icc measurements are made with outputs open (only capacitive loading).
4. Tested at f = 20MHz.

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AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V±10%, T_A = –55°C to +125°C)

		Com'l.		Com'l. & Mil.		Com'l.		Mil.		Com'l.		
		7200L15 7201LA15		7200L20 7201LA20		7200S/L25 7201SA/LA25		7200S/L30 7201SA/LA30		7200S/L35 7201SA/LA35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_S	Shift Frequency	—	40	—	33.3	—	28.5	—	25	—	22.2	MHz
t_{RC}	Read Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_A	Access Time	—	15	—	20	—	25	—	30	—	35	ns
t_{RR}	Read Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{RPW}	Read Pulse Width[2]	15	—	20	—	25	—	30	—	35	—	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z[3]	5	—	5	—	5	—	5	—	5	—	ns
t_{WLZ}	Write Pulse High to Data Bus at Low Z[3,4]	5	—	5	—	5	—	5	—	10	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z[3]	—	15	—	15	—	18	—	20	—	20	ns
t_{WC}	Write Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_{WPW}	Write Pulse Width[2]	15	—	20	—	25	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{DS}	Data Set-up Time	11	—	12	—	15	—	18	—	18	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{RSC}	Reset Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_{RS}	Reset Pulse Width[2]	15	—	20	—	25	—	30	—	35	—	ns
t_{RSS}	Reset Set-up Time[3]	15	—	20	—	25	—	30	—	35	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{RTC}	Retransmit Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_{RT}	Retransmit Pulse Width[2]	15	—	20	—	25	—	30	—	35	—	ns
t_{RTS}	Retransmit Set-up Time[3]	15	—	20	—	25	—	30	—	35	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{EFL}	Reset to Empty Flag Low	—	25	—	30	—	35	—	40	—	45	ns
$t_{HFH,FFH}$	Reset to Half-Full and Full Flag High	—	25	—	30	—	35	—	40	—	45	ns
t_{REF}	Read Low to Empty Flag Low	—	15	—	20	—	25	—	30	—	30	ns
t_{RFF}	Read High to Full Flag High	—	15	—	20	—	25	—	30	—	30	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ High	15	—	20	—	25	—	30	—	35	—	ns
t_{WEF}	Write High to Empty Flag High	—	15	—	20	—	25	—	30	—	30	ns
t_{WFF}	Write Low to Full Flag Low	—	15	—	20	—	25	—	30	—	30	ns
t_{WHF}	Write Low to Half-Full Flag Low	—	25	—	30	—	35	—	40	—	45	ns
t_{RHF}	Read High to Half-Full Flag High	—	25	—	30	—	35	—	40	—	45	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	15	—	20	—	25	—	30	—	35	—	ns
t_{XOL}	Read/Write to $\overline{XO}$ Low	—	15	—	20	—	25	—	30	—	35	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	—	15	—	20	—	25	—	30	—	35	ns
t_{XI}	$\overline{XI}$ Pulse Width[2]	15	—	20	—	25	—	30	—	35	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	10	—	10	—	10	—	10	—	10	—	ns

NOTES:

2679 tbl 05

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

AC ELECTRICAL CHARACTERISTICS (Continued)

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V±10%, T_A = –55°C to +125°C)

		Military		Commmercial and Military								
		7200S/L40 7201SA/LA40		7200S/L50 7201SA/LA50		7200S/L65 7201SA/LA65		7200S/L80 7201SA/LA80		7200S/L120 7201SA/LA120		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_S	Shift Frequency	—	20	—	15	—	12.5	—	10	—	7	MHz
t_{RC}	Read Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
t_A	Access Time	—	40	—	50	—	65	—	80	—	120	ns
t_{RR}	Read Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
t_{RPW}	Read Pulse Width[2]	40	—	50	—	65	—	80	—	120	—	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z[3]	5	—	10	—	10	—	10	—	10	—	ns
t_{WLZ}	Write Pulse High to Data Bus at Low Z[3,4]	10	—	15	—	15	—	20	—	20	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z[3]	—	25	—	30	—	30	—	30	—	35	ns
t_{WC}	Write Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
t_{WPW}	Write Pulse Width[2]	40	—	50	—	65	—	80	—	120	—	ns
t_{WR}	Write Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
t_{DS}	Data Set-up Time	20	—	30	—	30	—	40	—	40	—	ns
t_{DH}	Data Hold Time	0	—	5	—	10	—	10	—	10	—	ns
t_{RSC}	Reset Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
t_{RS}	Reset Pulse Width[2]	40	—	50	—	65	—	80	—	120	—	ns
t_{RSS}	Reset Set-up Time[3]	40	—	50	—	65	—	80	—	120	—	ns
t_{RSR}	Reset Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
t_{RTC}	Retransmit Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
t_{RT}	Retransmit Pulse Width[2]	40	—	50	—	65	—	80	—	120	—	ns
t_{RTS}	Retransmit Set-up Time[3]	40	—	50	—	65	—	80	—	120	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
t_{EFL}	Reset to Empty Flag Low	—	50	—	65	—	80	—	100	—	140	ns
$t_{HFH,FFH}$	Reset to Half-Full and Full Flag High	—	50	—	65	—	80	—	100	—	140	ns
t_{REF}	Read Low to Empty Flag Low	—	30	—	45	—	60	—	60	—	60	ns
t_{RFF}	Read High to Full Flag High	—	35	—	45	—	60	—	60	—	60	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ High	40	—	50	—	65	—	80	—	120	—	ns
t_{WEF}	Write High to Empty Flag High	—	35	—	45	—	60	—	60	—	60	ns
t_{WFF}	Write Low to Full Flag Low	—	35	—	45	—	60	—	60	—	60	ns
t_{WHF}	Write Low to Half-Full Flag Low	—	50	—	65	—	80	—	100	—	140	ns
t_{RHF}	Read High to Half-Full Flag High	—	50	—	65	—	80	—	100	—	140	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	40	—	50	—	65	—	80	—	120	—	ns
t_{XOL}	Read/Write to $\overline{XO}$ Low	—	40	—	50	—	65	—	80	—	120	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	—	40	—	50	—	65	—	80	—	120	ns
t_{XI}	$\overline{XI}$ Pulse Width[2]	40	—	50	—	65	—	80	—	120	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	10	—	15	—	15	—	15	—	15	—	ns

NOTES:

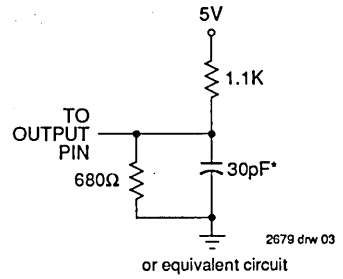
2679 tbl 06

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2679 tbl 08



or equivalent circuit

Figure 1. Output Load

* Includes scope and jig capacitances.

SIGNAL DESCRIPTIONS

INPUTS:

DATA IN ($D_0 - D_8$)

Data inputs for 9-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. **Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in the high state during the window shown in Figure 2, (i.e., t_{RSS} before the rising edge of $\overline{RS}$) and should not change until t_{RSR} after the rising edge of $\overline{RS}$. Half-Full Flag ($\overline{HF}$) will be reset to high after Reset ($\overline{RS}$).**

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of the Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any on-going read operation.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$) provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operations. After Read Enable ($\overline{R}$) goes high, the Data Outputs ($Q_0 - Q_8$) will return to a high impedance condition until the next Read operation. When all data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, allowing the "final" read cycle but inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go high after t_{WEF} and a valid Read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes in $\overline{R}$ will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$)

This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first loaded (see Operating Modes). In the Single Device Mode, this pin acts as the restransmit input. The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The IDT7200/7201A can be made to retransmit data when the Retransmit Enable control ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than 256/512 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode and will affect the Half-Full Flag ($\overline{HF}$), depending on the relative locations of the read and write pointers.

EXPANSION IN ($\overline{XI}$)

This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

OUTPUTS:

FULL FLAG ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location less than the read pointer, indicating that the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full-Flag ($\overline{FF}$) will go low after 256 writes for IDT7200 and 512 writes for the IDT7201A.

EMPTY FLAG ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$)

This is a dual-purpose output. In the single device mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by using rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.

DATA OUTPUTS ($Q_0 - Q_8$)

Data outputs for 9-bit wide data. This data is in a high impedance condition whenever Read ($\overline{R}$) is in a high state.

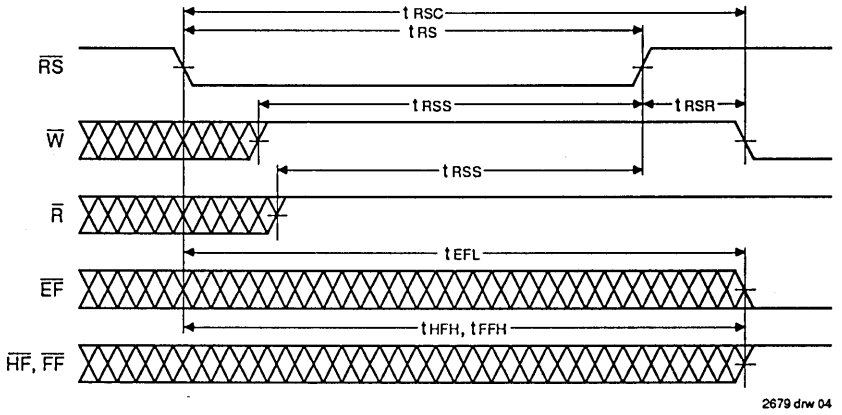


Figure 2. Reset

NOTES:
1. $\overline{EF}$, $\overline{FF}$, $\overline{HF}$ may change status during Reset, but flags will be valid at tRSC.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{RS}$.

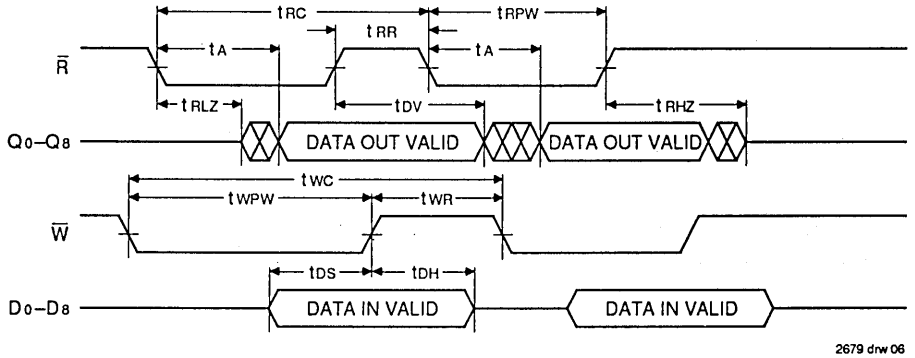


Figure 3. Asynchronous Write and Read Operation

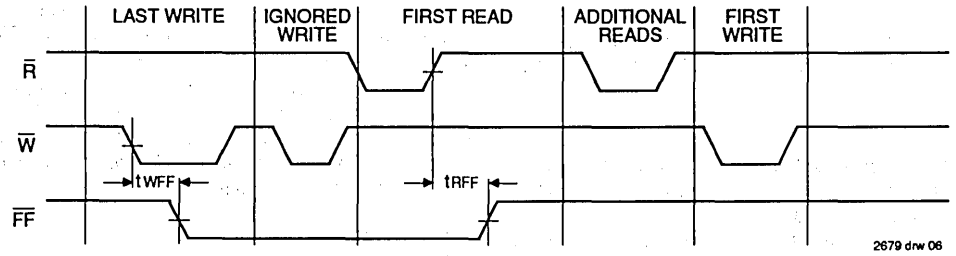


Figure 4. Full Flag From Last Write to First Read

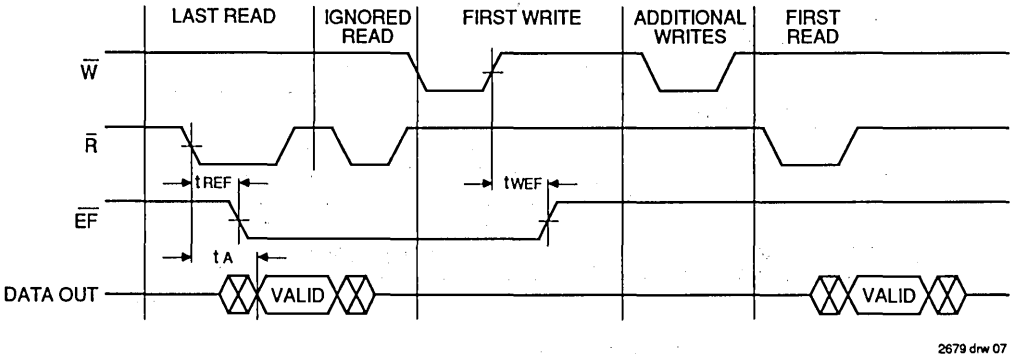


Figure 5. Empty Flag From Last Read to First Write

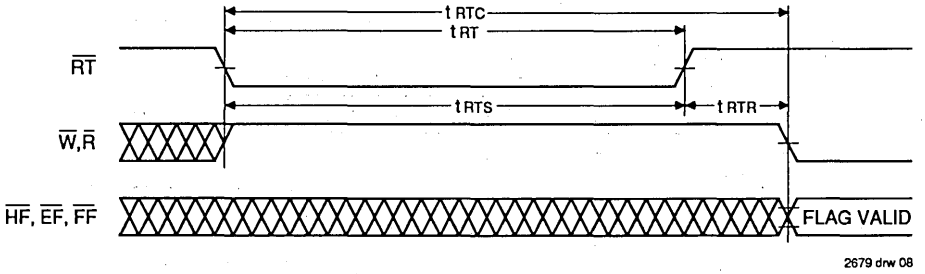


Figure 6. Retransmit

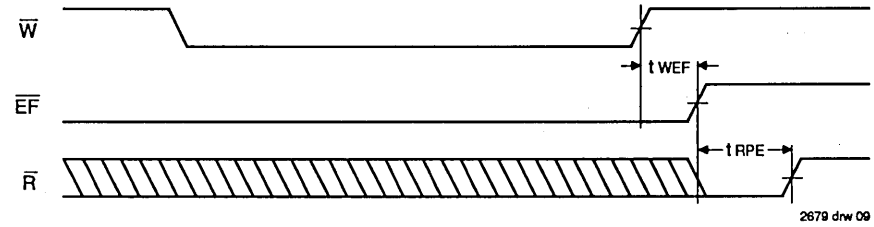


Figure 7. Empty Flag Timing

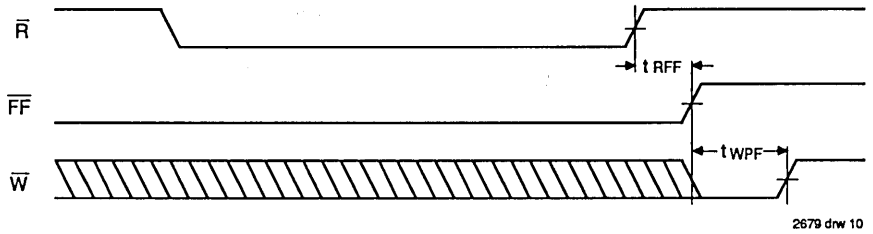


Figure 8. Full Flag Timing

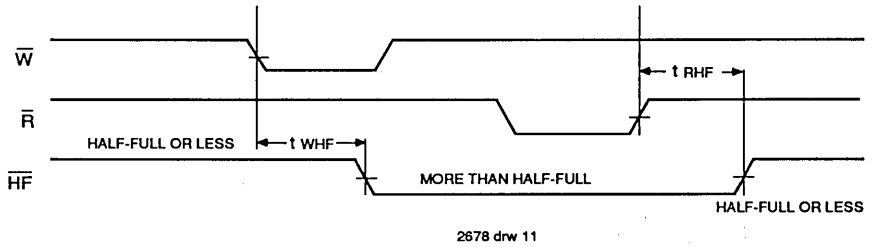


Figure 9. Half-Full Flag Timing

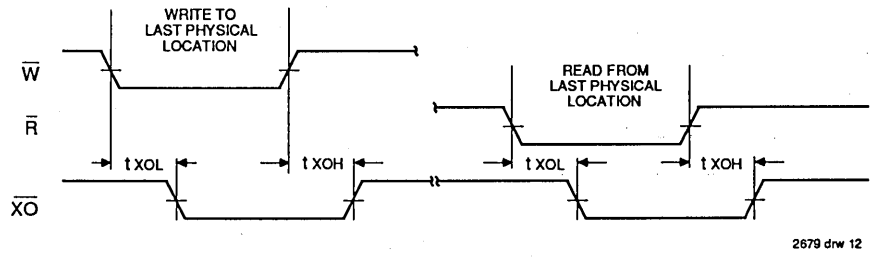


Figure 10. Expansion Out

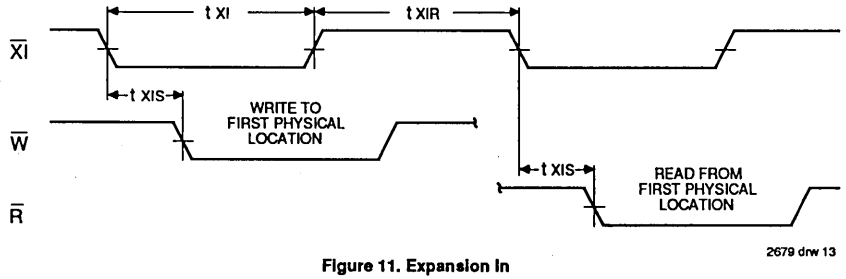


Figure 11. Expansion In

OPERATING MODES

SINGLE DEVICE MODE

A single IDT7200/7201A may be used when the application requirements for 256/512 words or less. The IDT7200/7201A is in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 12). In the mode the Half-Full Flag ($\overline{HF}$), which is an active low output, is shared with Expansion Out ($\overline{XO}$).

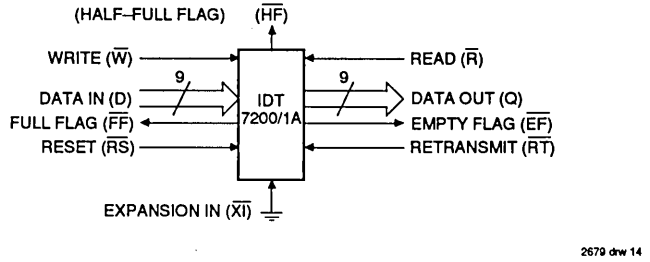


Figure 12. Block Diagram of Single 256/512 x 9 FIFO

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two IDT7201As. Any word width can be attained by adding additional IDT7201As.

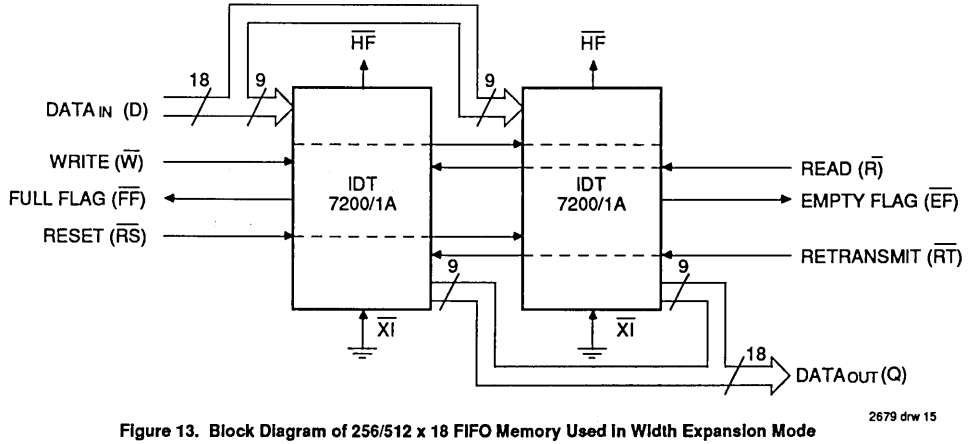


Figure 13. Block Diagram of 256/512 x 18 FIFO Memory Used in Width Expansion Mode

DEPTH EXPANSION (DASIY CHAIN) MODE

The IDT7200/7201A can easily be adapted to applications where the requirements are for greater than 256/512 words. Figure 14 demonstrates Depth Expansion using three IDT7200/7201As. Any depth can be attained by adding additional IDT7200/7201As. The IDT7200/7201A operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 14.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 14.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

For additional information refer to Tech Note 9: "Cascading FIFOs or FIFO Modules".

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see Figure 15).

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT7200/7201As as shown in Figure 16. Care must be taken to assure that the appropriate flag is monitored by each system (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted: a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17), the FIFO permits the reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary de-assertion and then would be asserted. In the interval of time that $\overline{R}$ is low, more words can be written to the FIFO (the subsequent writes after the first write edge will be de-assert the Empty Flag); however, the same word (written on the first write edge) presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ was low. On toggling $\overline{R}$, the other words that are written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be de-asserted but the $\overline{W}$ line, being low, causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

For additional information refer to Tech Note 8: "Operating FIFOs on Full and Empty Boundary Conditions" and Tech Note 6: "Designing with FIFOs".

6

TABLE I—RESET AND RETRANSMIT

Single Device Configuration/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X

NOTE: 2679 tbl 09

1. Pointer will increment if flag is High.

TABLE II—RESET AND FIRST LOAD TRUTH TABLE

Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTE: 2679 tbl 10

1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 15. $\overline{RS}$ = Reset Input $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Flag Full Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output

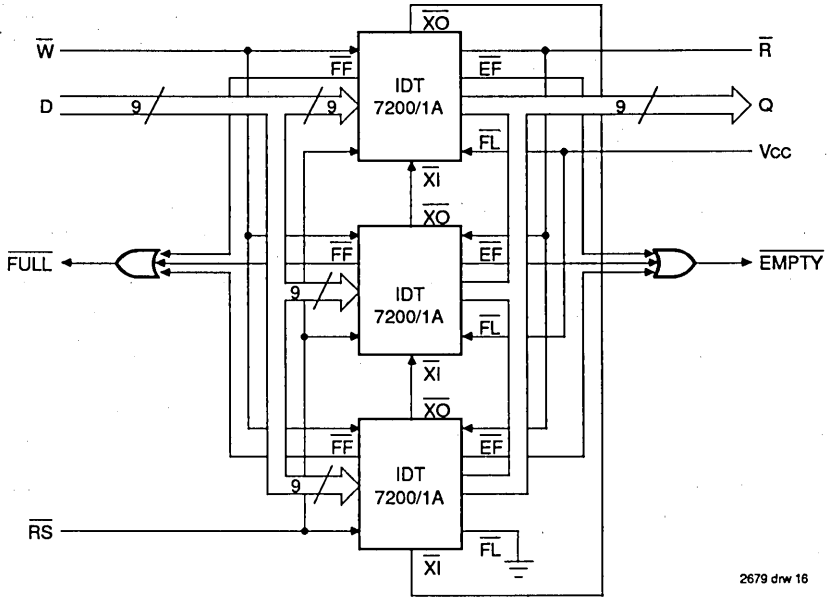


Figure 14. Block Diagram of 1538 x 9 FIFO Memory (Depth Expansion)

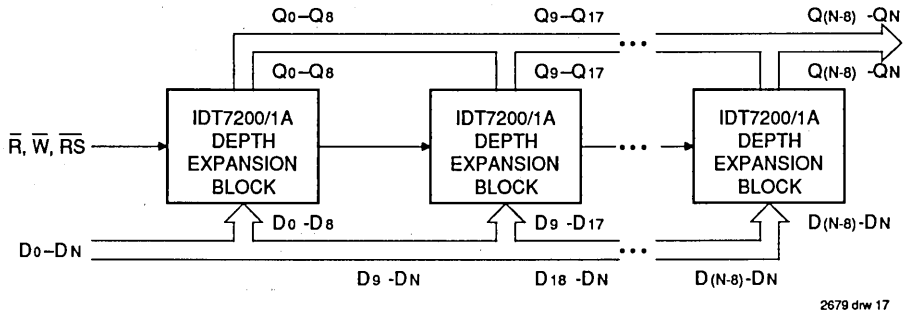


Figure 15. Compound FIFO Expansion

NOTES:
1. For depth expsansion block see section on Depth Expansion and Figure 14.
2. For Flag detection see section on Width Expansion and Figure 13.

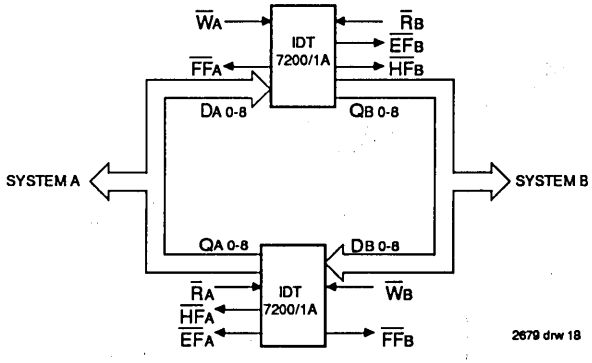


Figure 16. Bidirectional FIFO Mode

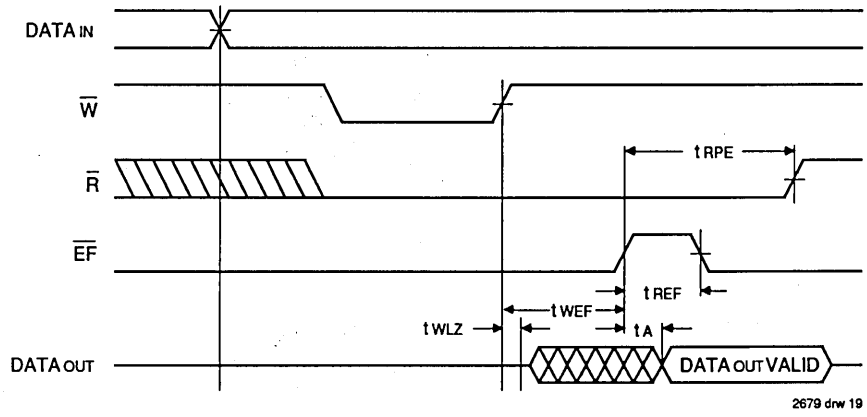


Figure 17. Read Data Flow-Through Mode

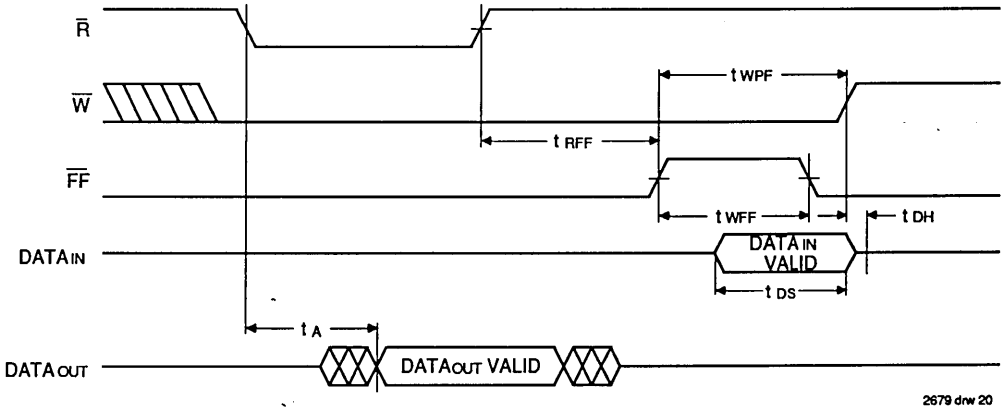
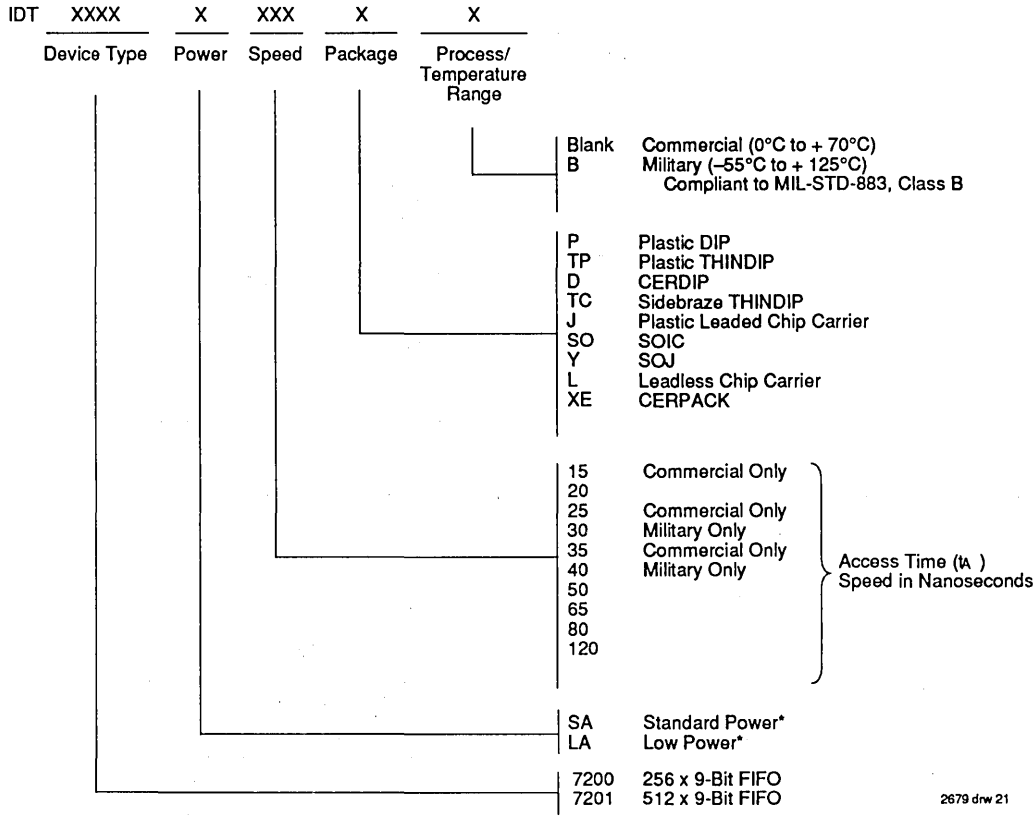


Figure 18. Write Data Flow-Through Mode

ORDERING INFORMATION



* "A" to be included for 7201 ordering part number only.

Integrated Device Technology, Inc.

CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 1024 x 9-BIT

IDT7202SA/LA

FEATURES:

- First-In/First-Out dual-port memory
- 1024 x 9 organization
- Low power consumption
  - — Active: 770mW (Max.)
  - — Power-down: 27.5mW(Max.)
- Ultra high-speed: 15ns access time
- Asynchronous and simultaneous read and write
- Fully expandable by both work depth and/or bit width
- Pin and functionality compatible with 720X family
- Status Flags: Empty, Half-Full, Full
- Auto retransmit capability
- High-performance CEMOS™ technology
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-89536 is listed on this function

DESCRIPTION:

The IDT7202A is a dual-port memory that loads and empties data on a first-in/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

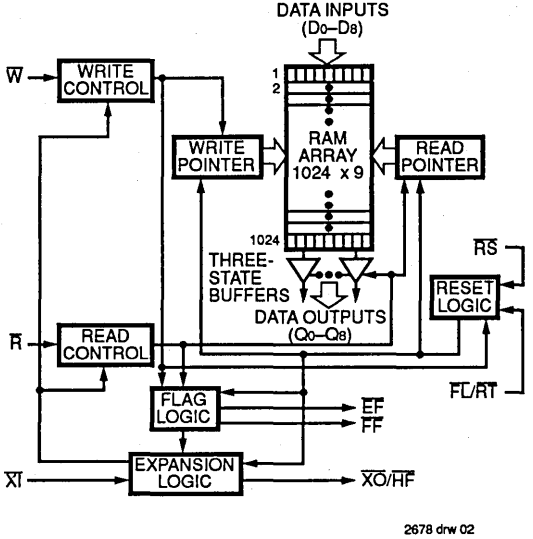
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins. The device has a read/write cycle time of 25ns (40MHz).

The device utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. It also features a Retransmit ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed low to allow for retransmission from the beginning of data. A Half-Full Flag is available in the single device mode and width expansion modes.

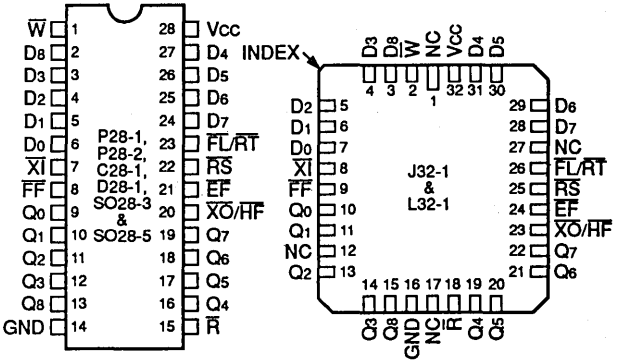
The IDT7202A is fabricated using IDT's high-speed CEMOS technology. It is designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications. The 1024 x 9 organization of the IDT7202A allows a 1024 deep word structure without the need for expansion.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP/SOIC/SOJ/FLATPACK TOP VIEW

LCC/PLCC TOP VIEW

CONSULT FACTORY FOR CERPACK PINOUT

2678 drw 01

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2678 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vccc	Military Supply Voltage	4.5	5.0	5.5	V
Vccm	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}(1)	Input High Votage Commercial	2.0	—	—	V
V_{IH}(1)	Input High Votage Military	2.2	—	—	V
V_{IL}(2)	Input Low Voltage	—	—	0.8	V

NOTE: 2678 tbl 02

1. V_{IH} = 2.6V for $\overline{XI}$ input (commercial).
   V_{IH} = 2.8V for $\overline{XI}$ input (military).
2. 1.5V undershoots are allowed for 10ns one per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 5.0V±10%, T_A = 0°C to +70°C; Military: Vcc = 5V±10%, T_A = –55°C to +125°C)

		IDT7202LA Commercial t_A =15,20ns			IDT7202LA Military t_A =20ns			IDT7202SA/LA Commercial t_A =25,35ns			IDT7202SA/LA Military t_A =30,40ns			IDT7202SA/LA Commercial t_A =50,65,80ns			IDT7202SA/LA Military t_A =50,65,80,120			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
I_{LI}(1)	Input Leakage Current (Any Input)	–1	—	1	–10	—	10	–1	—	1	–10	—	10	–1	—	1	–10	—	10	µA
I_{LO}(2)	Output Leakage Current	–10	—	10	–10	—	10	–10	—	10	–10	—	10	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OH} = –2mA	2.4	—	—	2.4	—	—	2.4	—	—	2.4	—	—	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OH} = 8mA	—	—	0.4	—	—	0.4	—	—	0.4	—	—	0.4	—	—	0.4	—	—	0.4	V
I_{CC1}(3)	Active Power Supply Current	—	—	140(4)	—	—	160(4)	—	—	125(4)	—	—	140(4)	—	50	80	—	70	100	mA
I_{CC2}(3)	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH})	—	—	19	—	—	20	—	—	15	—	—	20	—	5	8	—	8	15	mA
$I_{CC3(L)}$(3)	Power Down Current (All Input = Vcc – 0.2V)	—	—	5	—	—	9	—	—	0.5	—	—	0.9	—	—	0.5	—	—	0.9	mA
$I_{CC3(S)}$(3)	Power Down Current (All Input = Vcc – 0.2V)							—	—	5	—	—	9	—	—	5	—	—	9	mA

NOTES: 2678 tbl 03

1. Measurements with 0.4 ≤ V_{IN} ≤ Vcc.
2. $\overline{R}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ Vcc.
3. Icc measurements are made with outputs open.
4. Tested at f = 20MHz.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V±10%, T_A = –55°C to +125°C)

		Com'l.		Com'l & Mil.		Com'l		Mil.		Com'l		
		7202SA/LA15		7202SA/LA20		7202SA/LA25		7202SA/LA30		7202SA/LA35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_S	Shift Frequency	—	40	—	33.3	—	28.5	—	25	—	22.2	MHz
t_{RC}	Read Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_A	Access Time	—	15	—	20	—	25	—	30	—	35	ns
t_{RR}	Read Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{RPW}	Read Pulse Width[2]	15	—	20	—	25	—	30	—	35	—	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z[3]	5	—	5	—	5	—	5	—	5	—	ns
t_{WLZ}	Write Pulse High to Data Bus at Low Z[3,4]	5	—	5	—	5	—	5	—	10	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z[3]	—	15	—	15	—	18	—	20	—	20	ns
t_{WC}	Write Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_{WPW}	Write Pulse Width[2]	15	—	20	—	25	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{DS}	Data Set-up Time	11	—	12	—	15	—	18	—	18	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{RSC}	Reset Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_{RS}	Reset Pulse Width[2]	15	—	20	—	25	—	30	—	35	—	ns
t_{RSS}	Reset Set-up Time[3]	15	—	20	—	25	—	30	—	35	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{RTC}	Retransmit Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_{RT}	Retransmit Pulse Width[2]	15	—	20	—	25	—	30	—	35	—	ns
t_{RTS}	Retransmit Set-up Time[3]	15	—	20	—	25	—	30	—	35	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{EFL}	Reset to Empty Flag Low	—	25	—	30	—	35	—	40	—	45	ns
$t_{HFH,FFL}$	Reset to Half-Full and Full Flag High	—	25	—	30	—	35	—	40	—	45	ns
t_{REF}	Read Low to Empty Flag Low	—	15	—	20	—	25	—	30	—	30	ns
t_{RFF}	Read High to Full Flag High	—	15	—	20	—	25	—	30	—	30	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ High	15	—	20	—	25	—	30	—	35	—	ns
t_{WEF}	Write High to Empty Flag High	—	15	—	20	—	25	—	30	—	30	ns
t_{WFF}	Write Low to Empty Flag Low	—	15	—	20	—	25	—	30	—	30	ns
t_{WHF}	Write Low to Half-Full Flag Low	—	25	—	30	—	35	—	40	—	45	ns
t_{RHF}	Read High to Half-Full Flag High	—	25	—	30	—	35	—	40	—	45	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	15	—	20	—	25	—	30	—	35	—	ns
t_{XOL}	Read/Write to $\overline{XO}$ Low	—	15	—	20	—	25	—	30	—	35	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	—	15	—	20	—	25	—	30	—	35	ns
t_{XI}	$\overline{XI}$ Pulse Width[2]	15	—	20	—	25	—	30	—	35	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	10	—	10	—	10	—	10	—	10	—	ns

NOTES:

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

2678 tbl 04

AC ELECTRICAL CHARACTERISTICS (Continued)

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V±10%, T_A = –55°C to +125°C)

		Military		Military and Commercial								
		7202SA/LA40		7202SA/LA50		7202SA/LA65		7202SA/LA80		7202SA/LA120		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_S	Shift Frequency	—	20	—	15	—	—	—	10	—	7	MHz
t_{RC}	Read Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
t_A	Access Time	—	40	—	50	—	—	—	80	—	120	ns
t_{RR}	Read Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
t_{RPW}	Read Pulse Width[2]	40	—	50	—	65	—	80	—	120	—	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z[3]	5	—	10	—	10	—	10	—	10	—	ns
t_{WLZ}	Write Pulse High to Data Bus at Low Z[3, 4]	10	—	15	—	15	—	20	—	20	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z[3]	—	25	—	30	—	—	—	30	—	35	ns
t_{WC}	Write Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
t_{WPW}	Write Pulse Width[2]	40	—	50	—	65	—	80	—	120	—	ns
t_{WR}	Write Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
t_{DS}	Data Set-up Time	20	—	30	—	30	—	40	—	40	—	ns
t_{DH}	Data Hold Time	0	—	5	—	10	—	10	—	10	—	ns
t_{RSC}	Reset Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
t_{RS}	Reset Pulse Width[2]	40	—	50	—	65	—	80	—	120	—	ns
t_{RSS}	Reset Set-up Time[3]	40	—	50	—	65	—	80	—	120	—	ns
t_{RSR}	Reset Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
t_{RTC}	Retransmit Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
t_{RT}	Retransmit Pulse Width[2]	40	—	50	—	65	—	80	—	120	—	ns
t_{RTS}	Retransmit Set-up Time[3]	40	—	50	—	65	—	80	—	120	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
t_{EFL}	Reset to Empty Flag Low	—	50	—	65	—	—	—	100	—	140	ns
$t_{HFH,FFL}$	Reset to Half-Full and Full Flag High	—	50	—	65	—	—	—	100	—	140	ns
t_{REF}	Read Low to Empty Flag Low	—	30	—	45	—	—	—	60	—	60	ns
t_{RFF}	Read High to Full Flag High	—	35	—	45	—	—	—	60	—	60	ns
t_{RPE}	Read Pulse Width after EF High	40	—	50	—	65	—	80	—	120	—	ns
t_{WEF}	Write High to Empty Flag High	—	35	—	45	—	—	—	60	—	60	ns
t_{WFF}	Write Low to Empty Flag Low	—	35	—	45	—	—	—	60	—	60	ns
t_{WHF}	Write Low to Half-Full Flag Low	—	50	—	65	—	—	—	100	—	140	ns
t_{RHF}	Read High to Half-Full Flag High	—	50	—	65	—	—	—	100	—	140	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	40	—	50	—	65	—	80	—	120	—	ns
t_{XOL}	Read/Write to $\overline{XO}$ Low	—	40	—	50	—	—	—	80	—	120	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	—	40	—	50	—	—	—	80	—	120	ns
t_{XI}	$\overline{XI}$ Pulse Width[2]	40	—	50	—	65	—	80	—	120	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	10	—	10	—	10	—	10	—	10	—	ns

NOTES:

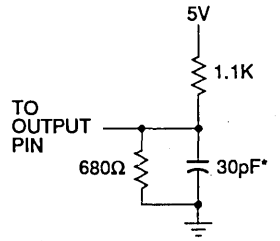
2678 tbl 05

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2678 tbl 06



or equivalent circuit

Figure 1. Output Load

2678 drw 03

*Includes jig and scope capacitances.

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter[1]	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:
1. This parameter is sampled and not 100% tested.

2678 tbl 07

SIGNAL DESCRIPTIONS

INPUTS:

DATA IN (D_0–D_8)

Data inputs for 9-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. **Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in the high state during the window shown in Figure 2, (i.e., t_{RSS} before the rising edge of $\overline{RS}$) and should not change until t_{RSR} after the rising edge of $\overline{RS}$. Half-Full Flag ($\overline{HF}$) will be reset to high after Reset ($\overline{RS}$).**

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of the Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any on-going read operation.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$) provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operations. After Read Enable ($\overline{R}$) goes high, the Data Outputs (Q0 – Q8) will return to a high impedance condition until the next Read operation. When all data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, allowing the "final" read cycle by inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go high after t_{WEF} and a valid Read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes in $\overline{R}$ will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$)

This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first loaded (see Operating Modes). In the Single Device Mode, this pin acts as the restransmit input. The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The IDT7202A can be made to retransmit data when the Retransmit Enable Control ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than 1024 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode and will affect the Half-Full Flag ($\overline{HF}$), depending on the relative locations of the read and write pointers.

EXPANSION IN ($\overline{XI}$)

This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

6

OUTPUTS:

FULL FLAG ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location less than the read pointer, indicating that the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full-Flag ($\overline{FF}$) will go low after 1024 writes.

EMPTY FLAG ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$)

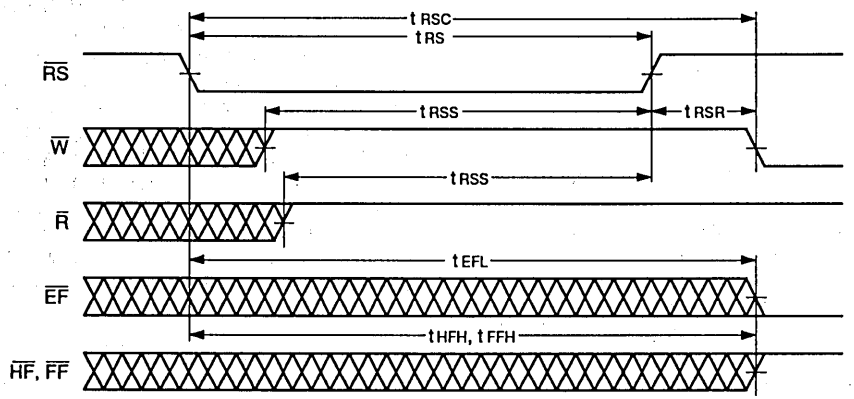
This is a dual-purpose output. In the single device mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by using rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Put ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.

Data outputs for 9-bit wide data. This data is in a high impedance condition whenever Read ($\overline{R}$) is in a high state.

DATA OUTPUTS (Q_0–Q_8)



2678 drw 04

NOTE:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Reset, but flags will be valid at t_{RSC}.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{RS}$.

Figure 2. Reset

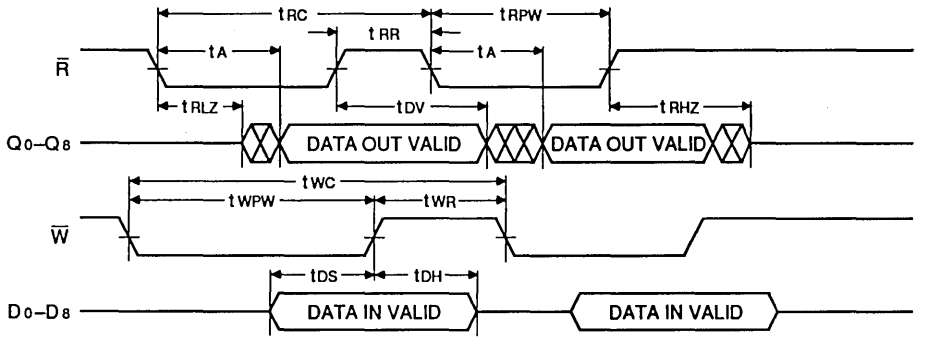


Figure 3. Asynchronous Write and Read Operation

2678 drw 05

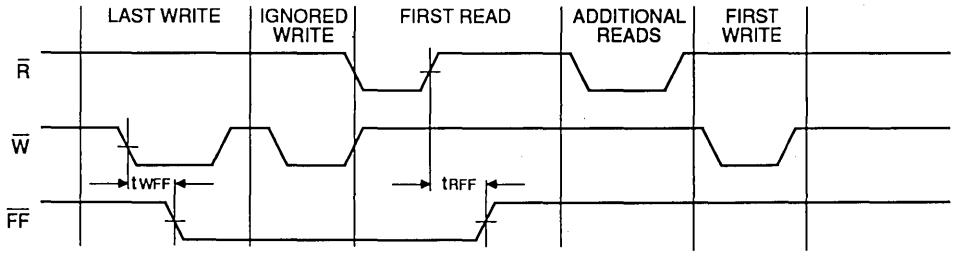


Figure 4. Full Flag From Last Write to First Read

2678 drw 06

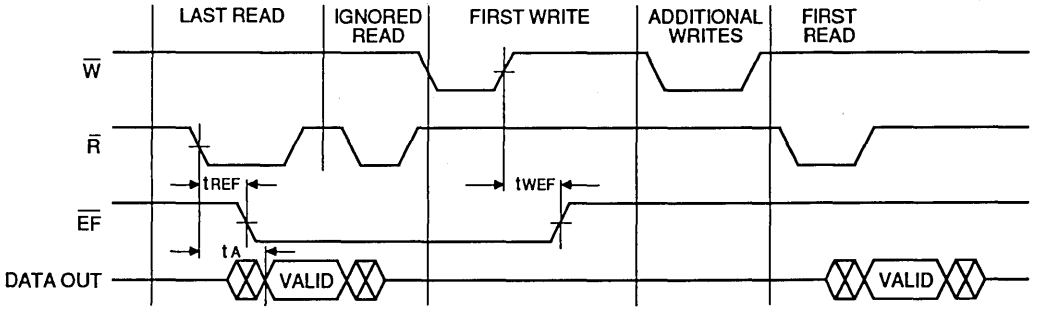
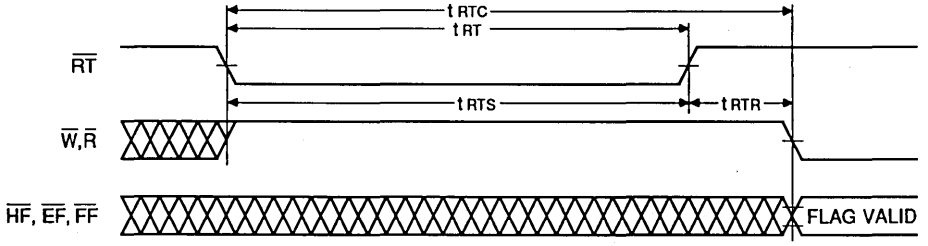


Figure 5. Empty Flag From Last Read to First Write

2678 drw 07



NOTE:
1. EF, FF and HF may change status during Retransmit, but flags will be valid at tRTC.

2678 drw 08

Figure 6. Retransmit

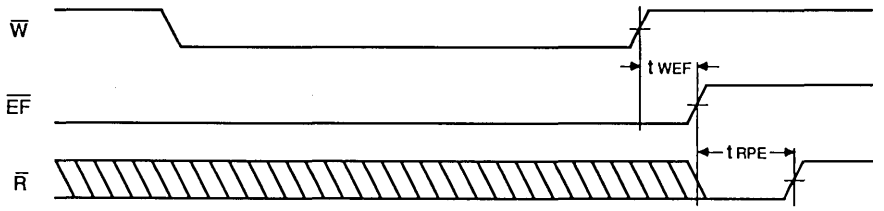


Figure 7. Empty Flag Timing

2678 drw 09

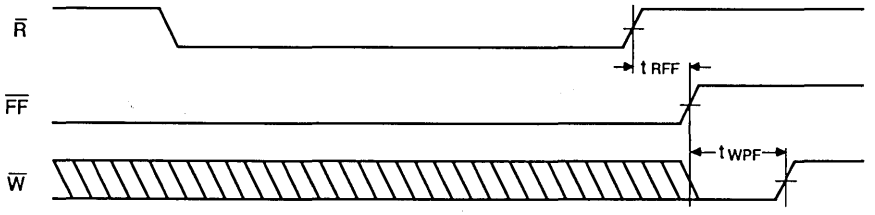


Figure 8. Full Flag Timing

2678 drw 10

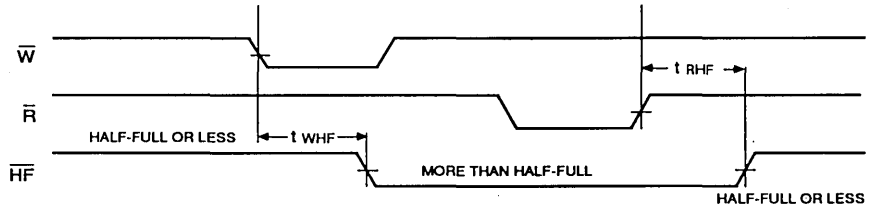


Figure 9. Half-Full Flag Timing

2678 drw 11

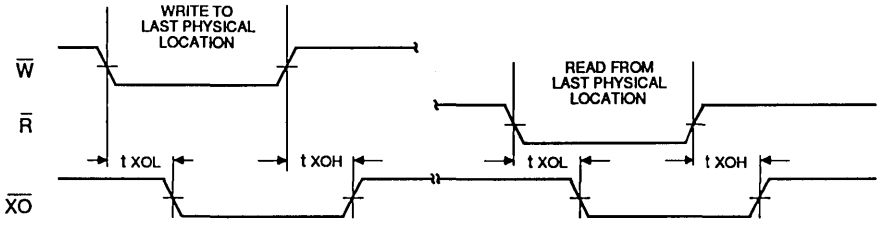


Figure 10. Expansion Out

2678 drw 12

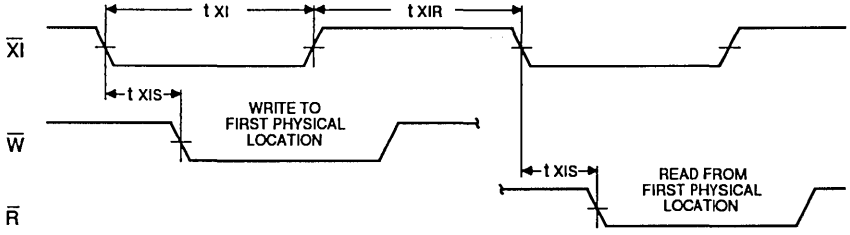


Figure 11. Expansion In

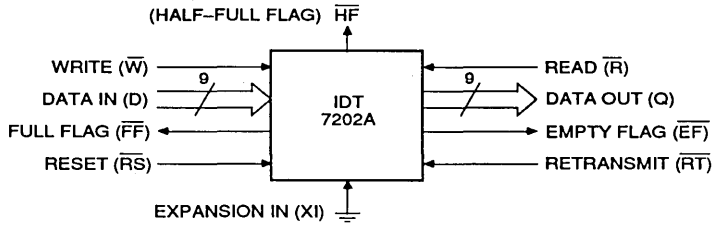
2678 drw 13

6

OPERATING MODES

SINGLE DEVICE MODE

A single IDT7202A may be used when the application requirements for 1024 words or less. The IDT7202A is in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 12). In the mode the Half-Full Flag ($\overline{HF}$), which is an active low output, is shared with Expansion Out ($\overline{XO}$).



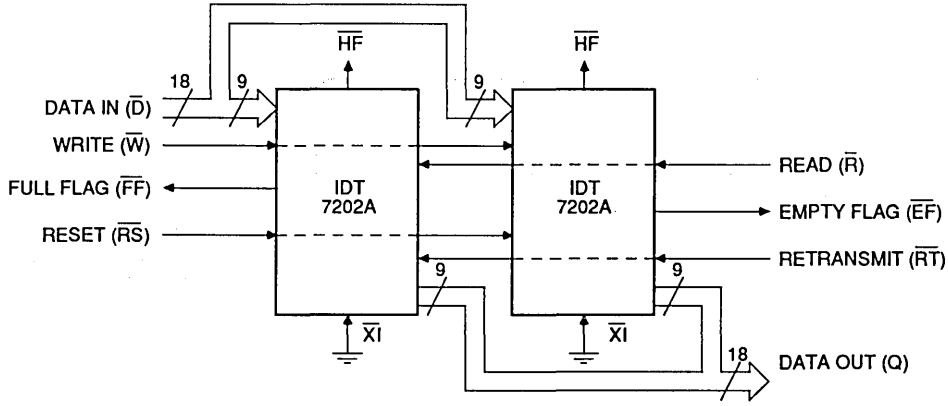
2678 Drw 14

Figure 12. Block Diagram of Single 1024 x 9 FIFO

2678 drw 14

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two IDT7202As. Any word width can be attained by adding additional IDT7202As.



NOTE:

2678 drw 15

1. Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$ and the $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 13. Block Diagram of 1024 x 18 FIFO Memory Used in Width Expansion Mode

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT7202A can easily be adapted to applications where the requirements are for greater than 1024 words. Figure 14 demonstrates Depth Expansion using three IDT7202As. Any depth can be attained by adding additional IDT7202As. The IDT7202As operate in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 14.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 14.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.
   For additional information refer to Tech Note 9: "Cascading FIFOs or FIFO Modules".

COMPOUND EXPANSION MODE

The two expansion techinques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 15).

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT7202As as shown in Figure 16. Care must be taken to assure that the appropriate flag is monitored by each system (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted: a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17), the FIFO permits the reading of a single wors after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary de-assertion and then would be asserted. In the interval of time that $\overline{R}$ is low, more words can be written to the FIFO (the subsequent writes after the first write edge will be de-assert the Empty Flag); however, the same word (written on the first write edge) presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ was low. On toggling $\overline{R}$, the other words that are written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be de-asserted but the $\overline{W}$ line, being low, causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

For additional information refer to Tech Note 8: "Operating FIFOs on Full and Empty Boundary Conditions" and Tech Note 6: "Designing with FIFOs".

6

TABLE I—RESET AND RETRANSMIT

Single Device Configuration/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment[1]	Increment[1]	X	X	X

NOTE: 2678 tbl 08

1. Pointer will increment if flag is High.

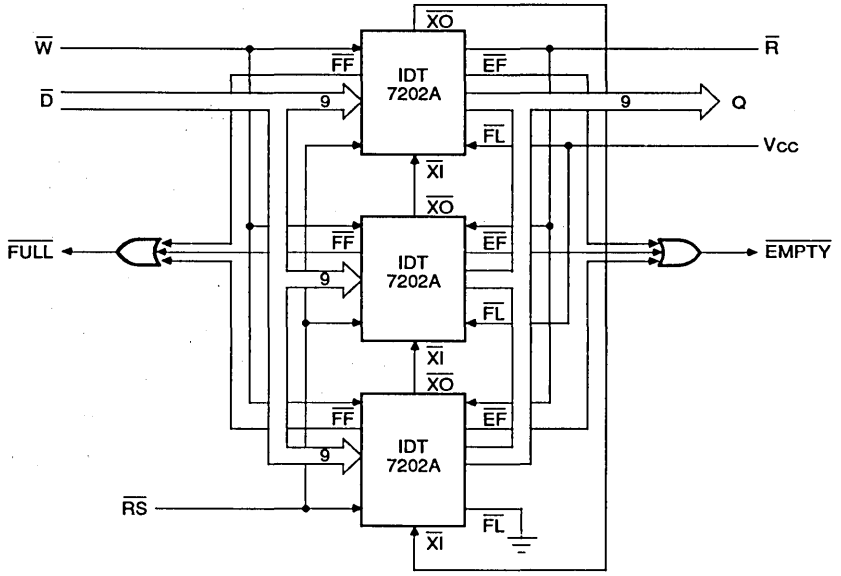
TABLE II—RESET AND FIRST LOAD TRUTH TABLE

Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTE: 2678 tbl 09

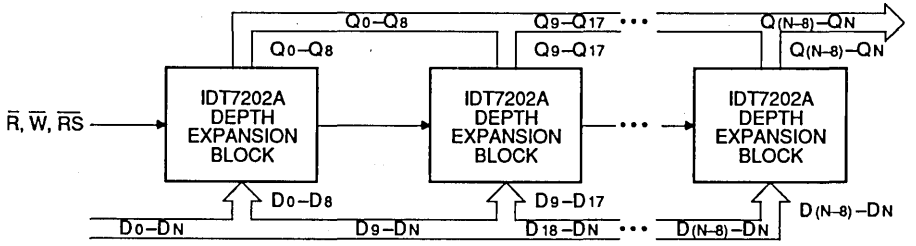
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14. $\overline{RS}$ = Reset Input $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Flag Full Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output



2678 Drw 18

Figure 14. Block Diagram of 3072 x 9 FIFO Memory (Depth Expansion)

2678 drw 16



NOTE:

1. For depth expansion block see section on Depth Expansion and Figure 14.
2. For Flag detection see section on Width Expansion and Figure 13.

2678 drw 17

Figure 15. Compound FIFO Expansion

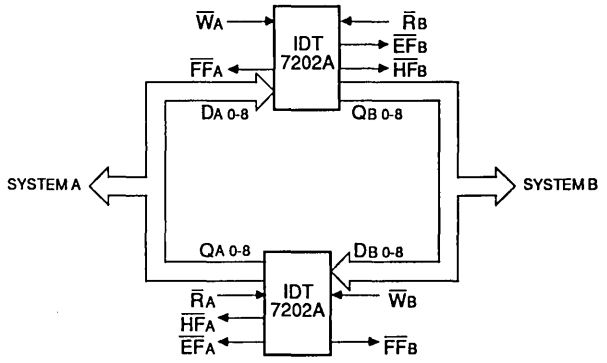


Figure 16. Bidirectional FIFO Mode

2678 drw 18

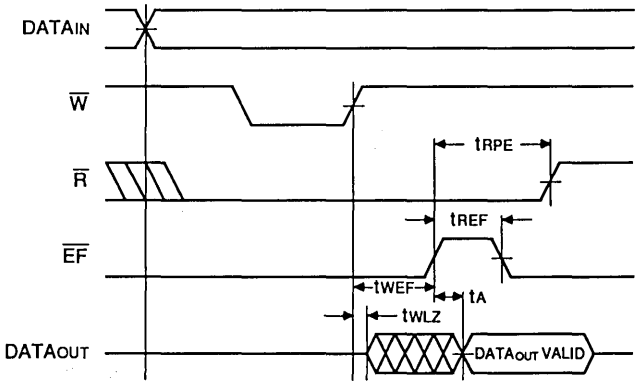


Figure 17. Read Data Flow-Through Mode

2678 drw 19

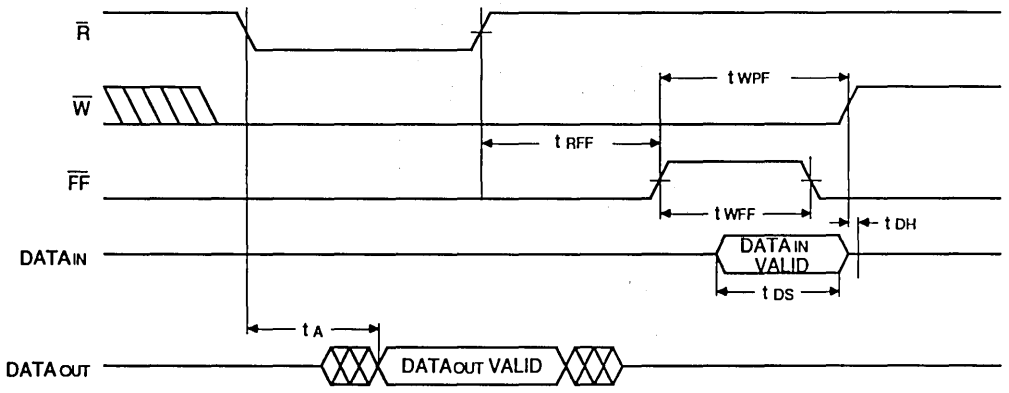


Figure 18. Write Data Flow-Through Mode

2678 drw 20

ORDERING INFORMATION

IDT XXXX XX XXX X X

- Device Type: 7202 — 1024 x 9-Bit FIFO
- Power: SA — Standard Power; LA — Low Power
- Speed (Access Time (t_A), Speed in Nanoseconds): 15 — Commercial Only; 20; 25 — Commercial Only; 30 — Military Only; 35 — Commercial Only; 40 — Military Only; 50; 65; 80; 120
- Package: P — Plastic DIP; TP — Plastic THINDIP; D — CERDIP; TC — Sidebraze THINDIP; J — Plastic Leaded Chip Carrier; L — Leadless Chip Carrier; Y — SOJ; SO — SOIC; XE — Cerpack
- Process/Temperature Range: Blank — Commercial (0°C to+70°C); B — Military (–55°C to+125°C) Compliant to MIL-STD-883, Class B

Integrated Device Technology, Inc.

CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 2048 x 9-BIT and 4096 x 9-BIT

IDT7203S/L
IDT7204S/L

FEATURES:

- First-In/First-Out dual-port memory
- 2048 x 9 organization (IDT7203)
- 4096 x 9 organization (IDT7204)
- Ultra high-speed: 15ns access time
- Low power consumption
  - — Active: 880mW (max.)
  - — Power-down: 44mW (max.)
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Pin and functionally compatible with IDT720X family
- Status Flags: Empty, Half-Full, Full
- Auto retransmit capability
- High-performance CEMOS™ technology
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-88669, 5962-89567, and 5962-89568 are listed on this function.

DESCRIPTION:

The IDT7203/7204 are dual-port memories that load and empty data on a first-in/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

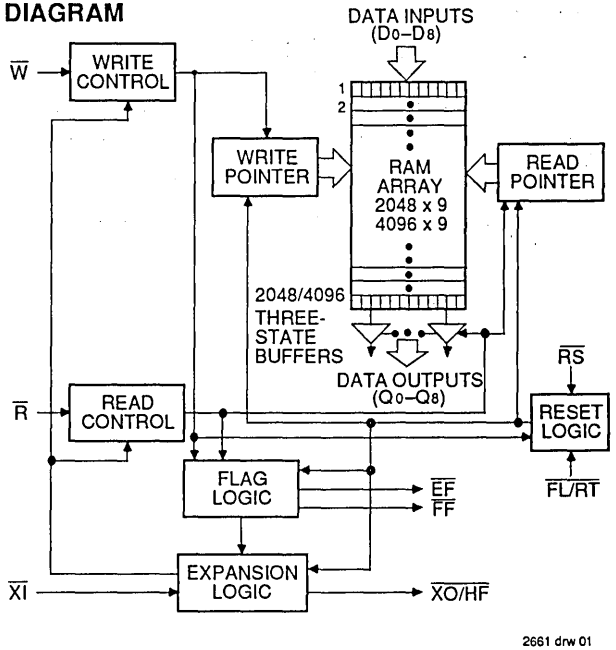
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins. The device has a read/write cycle time of 25ns (40MHz).

The device utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. It also features a Retransmit ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed low. A Half-Full Flag is available in the single device and width expansion modes.

The IDT7203/7204 is fabricated using IDT's high-speed CEMOS technology. They are designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications.

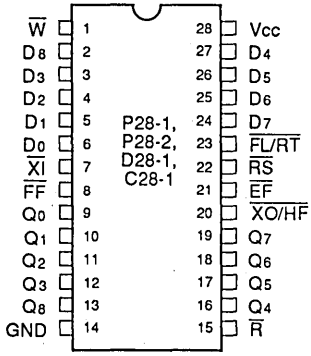
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



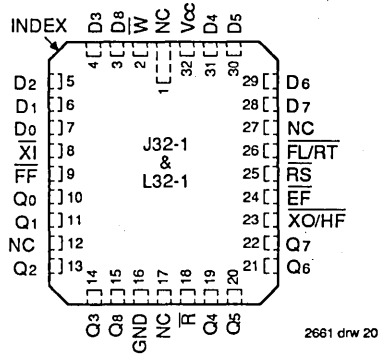
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW

Consult Factory for CERPACK Pinout.



PLCC/LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to + 7.0	-0.5 to + 7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	° C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	° C
TSTG	Storage Temperature	-55 to + 125	-65 to + 155	° C
IOUT	DC Output Current	50	50	mA

NOTE: 2661 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH(1)	Input High Voltage Commercial	2.0	—	—	V
VIH(1)	Input High Voltage Military	2.2	—	—	V
VIL (2,)	Input Low Voltage Commercial and Military	—	—	0.8	V

NOTES: 2661 tbl 02

1. VIH = 2.6V for $\overline{XI}$ input (commercial).
   VIH = 2.8V for $\overline{XI}$ input (military).
2. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	IDT7203, IDT7204 Commercial t_A = 15, 20ns			IDT7203, IDT7204 Military t_A = 20ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI} (1)	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	µA
I_{LO} (2)	Output Leakage Current	-10	—	10	-10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = -2mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8mA	—	—	0.4	—	—	0.4	V
I_{CC1} (3,4)	Active Power Supply Current	—	—	160	—	—	200	mA
I_{CC2} (3)	Average Standby Current, ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH})	—	—	14	—	—	19	mA
I_{CC3} (L) (3)	Power Down Current (All Input = V_{CC} - 0.2V)	—	—	8	—	—	12	mA

2661 tbl 03

NOTES:
1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. I_{CC} measurements are made with outputs open (only capacitive loading).
4. Tested at f = 20 MHz

DC ELECTRICAL CHARACTERISTICS (Continued)

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	IDT7203, IDT7204 Commercial t_A = 25, 35, 50, 65 80, 120ns			IDT7203, IDT7204 Military t_A = 30, 40, 50, 65 80, 120ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI} (1)	Input Leakage Current (Any Input)	-1	—	-1	-10	—	10	µA
I_{LO} (2)	Output Leakage Current	-10	—	10	-10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = 2mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8mA	—	—	0.4	—	—	0.4	V
I_{CC1} (3, 4)	Active Power Supply Current	—	75	120	—	100	150	mA
I_{CC2} (3)	Average Standby Current, ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH})	—	8	12	—	12	25	mA
I_{CC3} (L) (3)	Power Down Current (All Input = V_{CC} - 0.2V)	—	—	2	—	—	4	mA
I_{CC3} (S) (3)	Power Down Current (All Input = V_{CC} - 0.2V)	—	—	8	—	—	12	mA

2661 tbl 04

NOTES:
1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}
2. $\overline{R}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. I_{CC} measurements are made with outputs open.
4. Tested at f = 20MHz.

6

AC ELECTRICAL CHARACTERISTICS[1]

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	Commercial 7203/04L15		Com'l. & Mil. 7203/04L20		Commercial 7203/04L25		Military 7203/04L30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_S	Shift Frequency	—	40	—	33.3	—	28.5	—	25	MHz
t_{RC}	Read Cycle Time	25	—	30	—	35	—	40	—	ns
t_A	Access Time	—	15	—	20	—	25	—	30	ns
t_{RR}	Read Recovery Time	10	—	10	—	10	—	10	—	ns
t_{RPW}	Read Pulse Width[2]	15	—	20	—	25	—	30	—	ns
t_{RLZ}	Read Low to Data Bus Low Z[3]	5	—	5	—	5	—	5	—	ns
t_{WLZ}	Write High to Data Bus Low Z[3, 4]	5	—	5	—	5	—	5	—	ns
t_{DV}	Data Valid from Read High	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read High to Data Bus High Z[3]	—	15	—	15	—	18	—	20	ns
t_{WC}	Write Cycle Time	25	—	30	—	35	—	40	—	ns
t_{WPW}	Write Pulse Width[2]	15	—	20	—	25	—	30	—	ns
t_{WR}	Write Recovery Time	10	—	10	—	10	—	10	—	ns
t_{DS}	Data Set-up Time	11	—	12	—	15	—	18	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{RSC}	Reset Cycle Time	25	—	30	—	35	—	40	—	ns
t_{RS}	Reset Pulse Width[2]	15	—	20	—	25	—	30	—	ns
t_{RSS}	Reset Set-up Time	15	—	20	—	25	—	30	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	10	—	10	—	ns
t_{RTC}	Retransmit Cycle Time	25	—	30	—	35	—	40	—	ns
t_{RT}	Retransmit Pulse Width[2]	15	—	20	—	25	—	30	—	ns
t_{RTS}	Retransmit Set-up Time	15	—	20	—	25	—	30	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	10	—	10	—	10	—	ns
t_{EFL}	Reset to Empty Flag Low	—	25	—	30	—	35	—	40	ns
t_{HFH},t_{FFH}	Reset to $\overline{HF}$ and $\overline{FF}$ High	—	25	—	30	—	35	—	40	ns
t_{REF}	Read Low to Empty Flag Low	—	15	—	20	—	25	—	30	ns
t_{RFF}	Read High to Full Flag High	—	18	—	20	—	25	—	30	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ High	15	—	20	—	25	—	30	—	ns
t_{WEF}	Write High to Empty Flag High	—	18	—	20	—	25	—	30	ns
t_{WFF}	Write Low to Full Flag Low	—	15	—	20	—	25	—	30	ns
t_{WHF}	Write Low to Half-Full Flag Low	—	25	—	30	—	35	—	40	ns
t_{RHF}	Read High to Half-Full Flag High	—	25	—	30	—	35	—	40	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	15	—	20	—	25	—	30	—	ns
t_{XOL}	Read/Write Low to $\overline{XO}$ Low	—	15	—	20	—	25	—	30	ns
t_{XOH}	Read/Write High to $\overline{XO}$ High	—	15	—	20	—	25	—	30	ns
t_{XI}	$\overline{XI}$ Pulse Width[2]	15	—	20	—	25	—	30	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	10	—	10	—	10	—	10	—	ns

2661 tbl 05

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

AC ELECTRICAL CHARACTERISTICS[1] (Continued)

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

		Com'l.		Military		Commercial and Military								
		7203S/L35 7204S/L35		7203S/L40 7204S/L40		7203S/L50 7204S/L50		7203S/L65 7204S/L65		7203S/L80 7204S/L80		7203S/L120 7204S/L120		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
f_S	Shift Frequency	—	22.2	—	20	—	15	—	12.5	—	10	—	7	MHz
t_{RC}	Read Cycle Time	45	—	50	—	65	—	80	—	100	—	140	—	ns
t_A	Access Time	—	35	—	40	—	50	—	65	—	80	—	120	ns
t_{RR}	Read Recovery Time	10	—	10	—	15	—	15	—	20	—	20	—	ns
t_{RPW}	Read Pulse Width[2]	35	—	40	—	50	—	65	—	80	—	120	—	ns
t_{RLZ}	Read Low to Data Bus Low Z[3]	5	—	5	—	10	—	10	—	10	—	10	—	ns
t_{WLZ}	Write High to Data Bus Low Z[3,4]	10	—	10	—	5	—	5	—	5	—	5	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read High to Data Bus High Z[3]	—	20	—	25	—	30	—	30	—	30	—	35	ns
t_{WC}	Write Cycle Time	45	—	50	—	65	—	80	—	100	—	140	—	ns
t_{WPW}	Write Pulse Width[2]	35	—	40	—	50	—	65	—	80	—	120	—	ns
t_{WR}	Write Recovery Time	10	—	10	—	15	—	15	—	20	—	20	—	ns
t_{DS}	Data Set-up Time	18	—	20	—	30	—	30	—	40	—	40	—	ns
t_{DH}	Data Hold Time	0	—	0	—	5	—	10	—	10	—	10	—	ns
t_{RSC}	Reset Cycle Time	45	—	50	—	65	—	80	—	100	—	140	—	ns
t_{RS}	Reset Pulse Width[2]	35	—	40	—	50	—	65	—	80	—	120	—	ns
t_{RSS}	Reset Set-up Time	35	—	40	—	50	—	65	—	80	—	120	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	15	—	15	—	20	—	20	—	ns
t_{RTC}	Retransmit Cycle Time	45	—	50	—	65	—	80	—	100	—	140	—	ns
t_{RT}	Retransmit Pulse Width[2]	35	—	40	—	50	—	65	—	80	—	120	—	ns
t_{RTS}	Retransmit Set-up Time [3]	35	—	40	—	50	—	65	—	80	—	120	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	10	—	15	—	15	—	20	—	20	—	ns
t_{EFL}	Reset to Empty Flag Low	—	45	—	50	—	65	—	80	—	100	—	140	ns
t_{HFH}, t_{FFH}	Reset to $\overline{HF}$ and $\overline{FF}$ High	—	45	—	50	—	65	—	80	—	100	—	140	ns
t_{REF}	Read Low to Empty Flag Low	—	30	—	35	—	45	—	60	—	60	—	60	ns
t_{RFF}	Read High to Full Flag High	—	30	—	35	—	45	—	60	—	60	—	60	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ High	35	—	40	—	50	—	65	—	80	—	120	—	ns
t_{WEF}	Write High to Empty Flag High	—	30	—	35	—	45	—	60	—	60	—	60	ns
t_{WFF}	Write Low to Full Flag Low	—	30	—	35	—	45	—	60	—	60	—	60	ns
t_{WHF}	Write Low to Half-Full Flag Low	—	45	—	50	—	65	—	80	—	100	—	140	ns
t_{RHF}	Read High to Half-Full Flag High	—	45	—	50	—	65	—	80	—	100	—	140	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	35	—	40	—	50	—	65	—	80	—	120	—	ns
t_{XOL}	Read/Write Low to $\overline{XO}$ Low	—	35	—	40	—	50	—	65	—	80	—	120	ns
t_{XOH}	Read/Write High to $\overline{XO}$ High	—	35	—	40	—	50	—	65	—	80	—	120	ns
t_{XI}	$\overline{XI}$ Pulse Width[2]	35	—	40	—	50	—	65	—	80	—	120	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	15	—	15	—	15	—	15	—	15	—	15	—	ns

2661 tbl 05

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

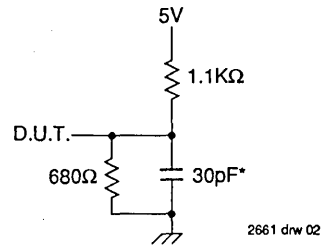
2661 tbl 08

CAPACITANCE[1] (TA = + 25° C, f = 1.0MHZ)

Symbol	Parameter	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT[2]	Output Capacitance	VOUT = 0V	12	pF

2661 tbl 09

NOTES:
1. This parameter is sampled and not 100% tested.
2. With output deselected.



or equivalent circuit

Figure 1. Output Load

* Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS:

Inputs:

DATA IN (D0–D8) — Data inputs for 9-bit wide data.

Controls:

RESET ($\overline{RS}$) — Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place. **Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in the high state during the window shown in Figure 2 (i.e. tRSS before the rising edge of $\overline{RS}$) and should not change until tRSR after the rising edge of $\overline{RS}$. Half-Full Flag ($\overline{HF}$) will be reset to high after master Reset ($\overline{RS}$).**

WRITE ENABLE ($\overline{W}$) — A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of the Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any on-going read operation.

After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go high after tRFF, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$) — A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$) provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis independent of any ongoing write operations. After Read Enable ($\overline{R}$) goes high, the Data Outputs (Q0 through Q8) will return to a high impedance condition until the next Read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, allowing the "final" read cycle but inhibiting further read operations, with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go high after tWEF and a valid Read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$) — This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first device loaded (see Operating Modes). In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The IDT7203/7204 can be made to retransmit data when the Retransmit Enable Control ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than 2048/4096 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode and will affect the status of the flags depending on the relative locations of the read and write pointers.

EXPANSION IN ($\overline{XI}$) — This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the Single Device Mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

Outputs:

FULL FLAG ($\overline{FF}$) — The Full Flag ($\overline{FF}$) will go low, inhibiting further write operations, when the write pointer is equal to the read pointer, indicating that the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go low after 2048 writes for the IDT7203 and 4096 writes for the IDT7204.

EMPTY FLAG ($\overline{EF}$) — The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

Expansion Out/Half Full Flag ($\overline{XO}/\overline{HF}$)

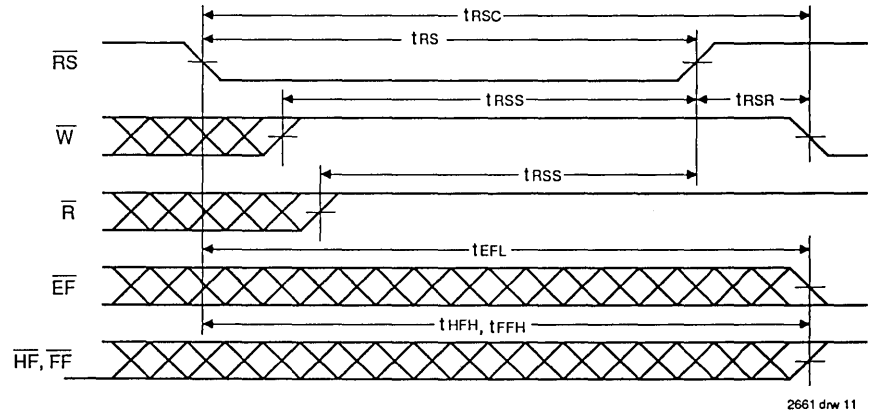
This is a dual-purpose output. In the single device mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory. There will be an $\overline{XO}$ pulse when the Write pointer reaches the last location of memory, and an additional $\overline{XO}$ pulse when the Read pointer reaches the last location of memory.

Data Outputs (Q_0-Q_8)

Q_0-Q_8 are data outputs for 9-bit wide data. These outputs are in a high impedance condition whenever Read ($\overline{R}$) is in a high state.



NOTES:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Reset, but flags will be valid at tRSO.
2. $\overline{W}$ and $\overline{R}$ = VIH around the rising edge of $\overline{RS}$.

Figure 2. Reset

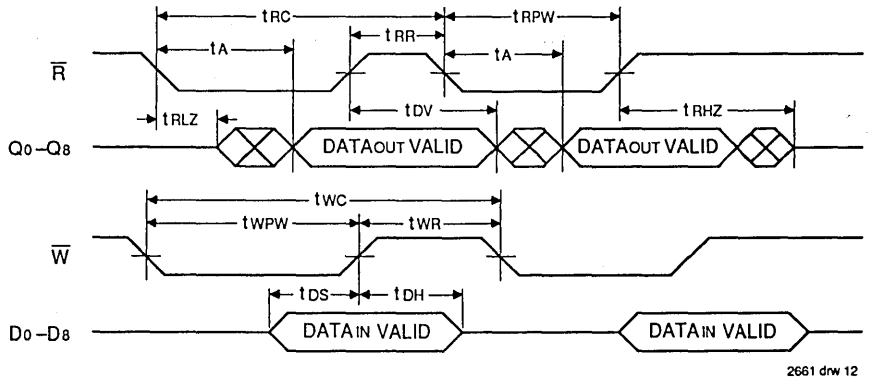


Figure 3. Asynchronous Write and Read Operation

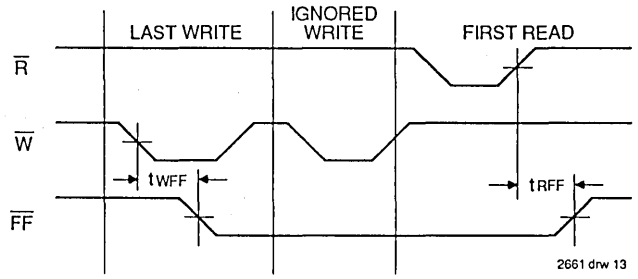


Figure 4. Full Flag From Last Write to First Read

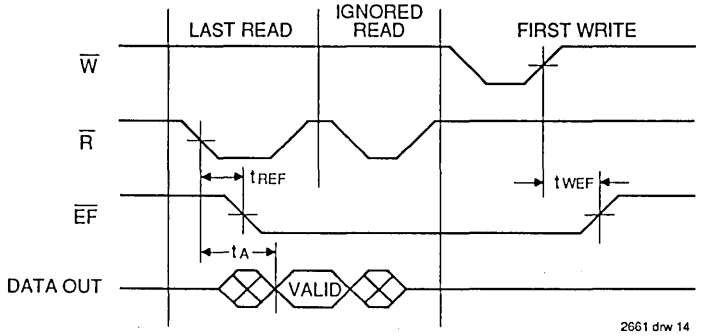
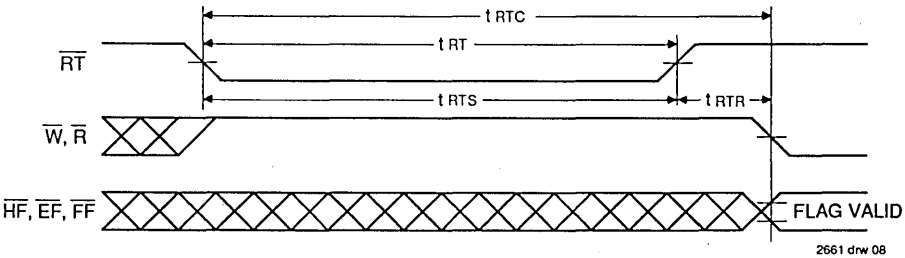


Figure 5. Empty Flag From Last Read to First Write



NOTE:
1. EF, FF and HF may change status during Retransmit, but flags will be valid at tRTC.

Figure 6. Retransmit

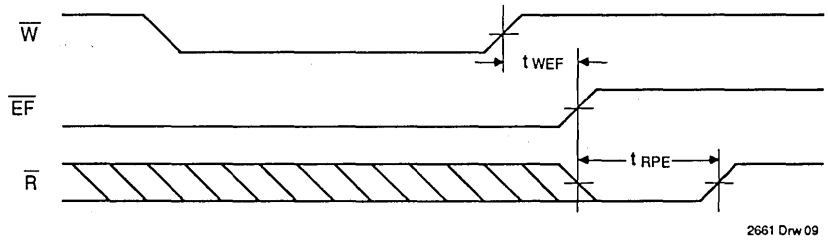


Figure 7. Empty Flag Timing

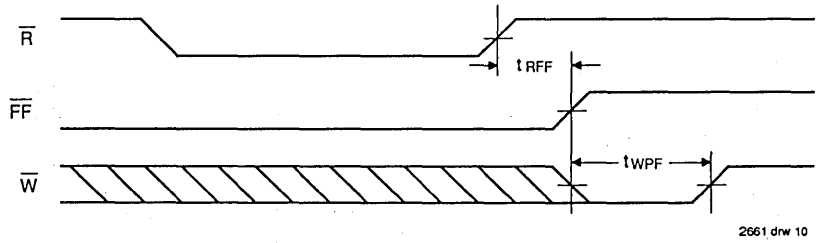


Figure 8. Full Flag Timing

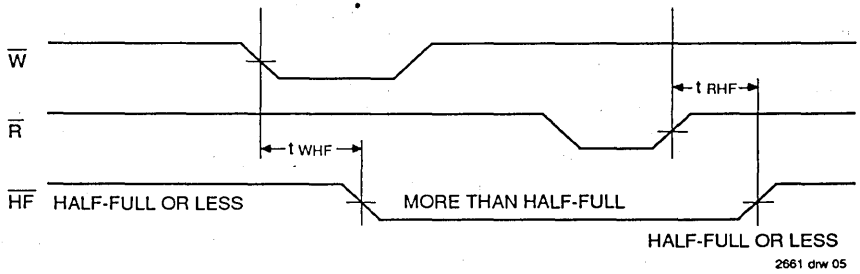


Figure 9. Half-Full Flag Timing

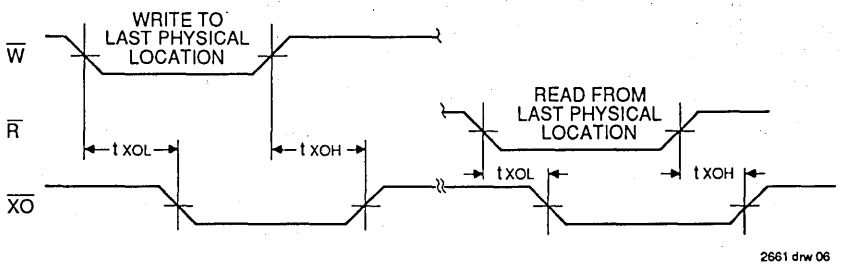


Figure 10. Expansion Out

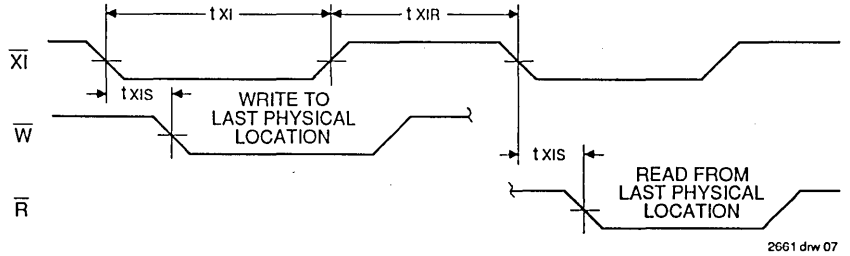


Figure 11. Expansion In

OPERATING MODES:

Single Device Mode

A single IDT7203/7204 may be used when the application requirements are for 2048/4096 words or less. The IDT7203/7204 are in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 12).

Width Expansion Mode

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two IDT7203/7204s. Any word width can be attained by adding additional IDT7203/7204s.

Depth Expansion (Daisy Chain Mode)

The IDT7203/7204 can easily be adapted to applications when the requirements are for greater than 2048/4096 words. Figure 14 demonstrates Depth Expansion using three IDT7203/7204s. Any depth can be attained by adding additional IDT7203/7204s. The IDT7203/7204 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 14.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 14.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

For additional information, refer to Tech Note 9: *Cascading FIFOs or FIFO Modules.*

Compound Expansion Mode

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 15).

Bidirectional Mode

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT7203/7204s as shown in Figure 16. Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

Data Flow-Through Modes

Two types of flow-through modes are permitted, a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary deassertion and then would be asserted. In the interval of time that $\overline{R}$ was low, more words can be written to the FIFO (the subsequent writes after the first write edge will deassert the empty flag); however, the same word (written on the first write edge), presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ is low. On toggling $\overline{R}$, the other words that were written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be deasserted but the $\overline{W}$ line being low causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

For additional information, refer to Tech Note 8: *Operating FIFOs on Full and Empty Boundary Conditions* and Tech Note 6: *Designing with FIFOs.*

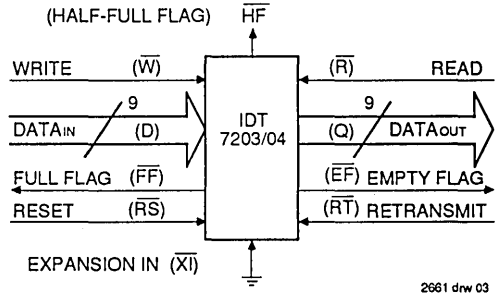
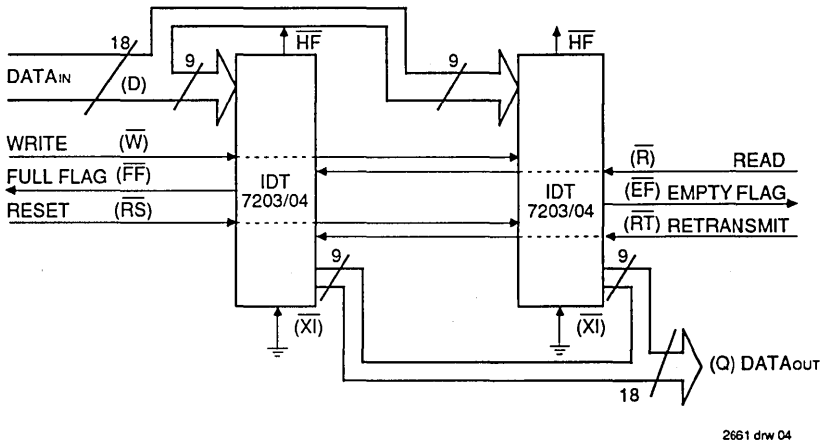


Figure 12. Block Diagram of 2048 x 9/4096 x 9 FIFO Used in Single Device Mode.



NOTE:
1. Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$ and $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 13. Block Diagram of 2048 x 18/4096 x 18 FIFO Memory Used in Width Expansion Mode

6

TRUTH TABLES

TABLE I – RESET AND RETRANSMIT

SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will Increment if flag is high.

2661 tbl 10

TABLE II – RESET AND FIRST LOAD TRUTH TABLE

DEPTH EXPANSION/COMPOUND EXPANSION MODE

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 12.
2. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output

2661 tbl 11

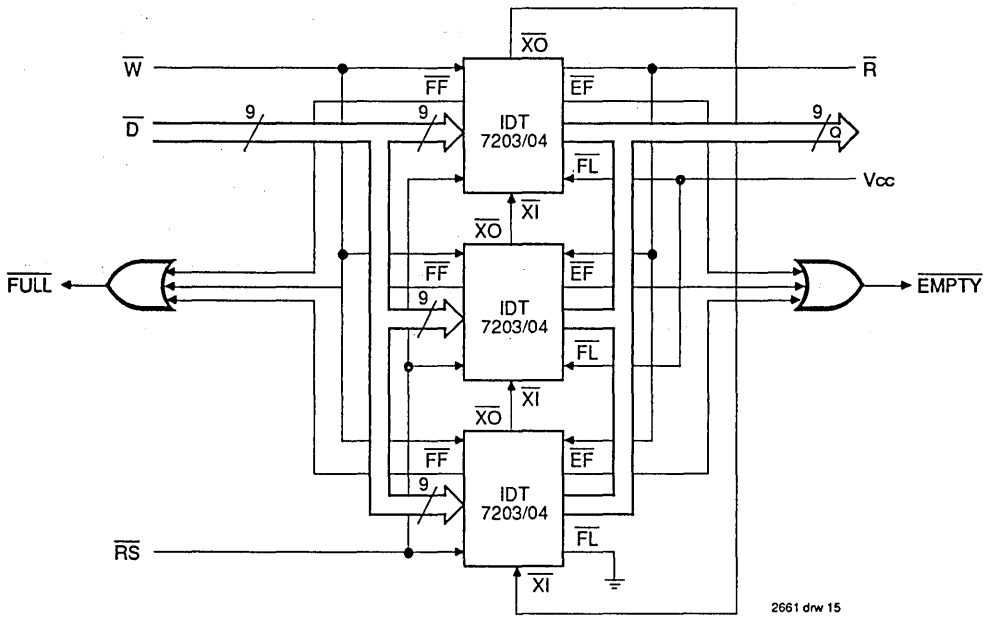
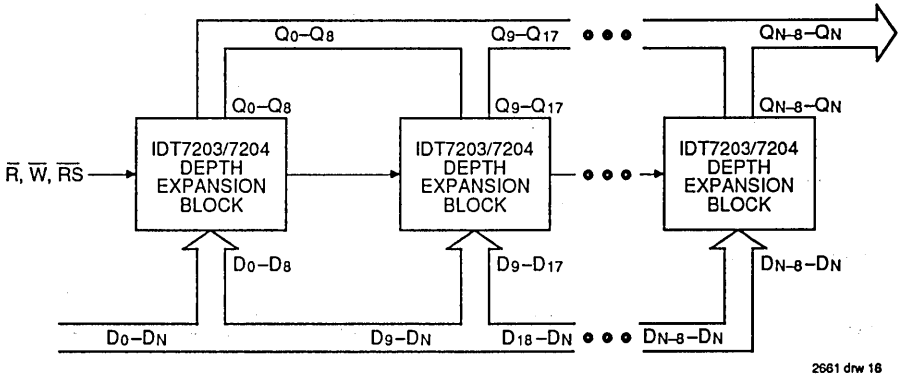


Figure 14. Block Diagram of 6,144 x 9/12,288 x 9 FIFO Memory (Depth Expansion)



NOTES:
1. For depth expansion block see section on Depth Expansion and Figure 14.
2. For Flag detection see section on Width Expansion and Figure 13.

Figure 15. Compound FIFO Expansion

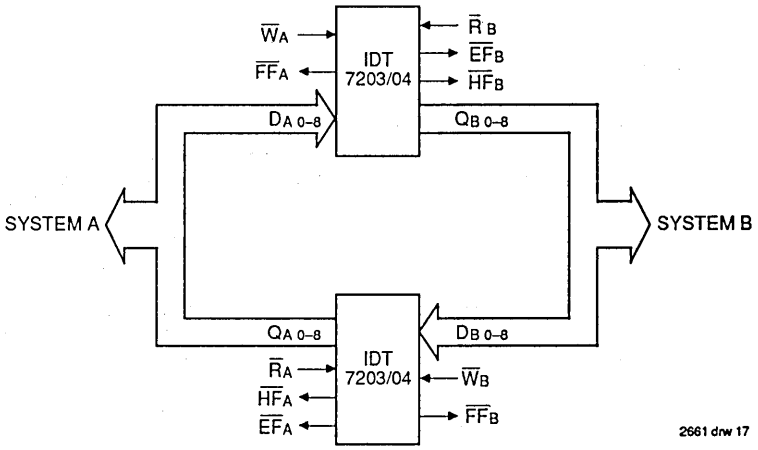


Figure 16. Bidirectional FIFO Mode

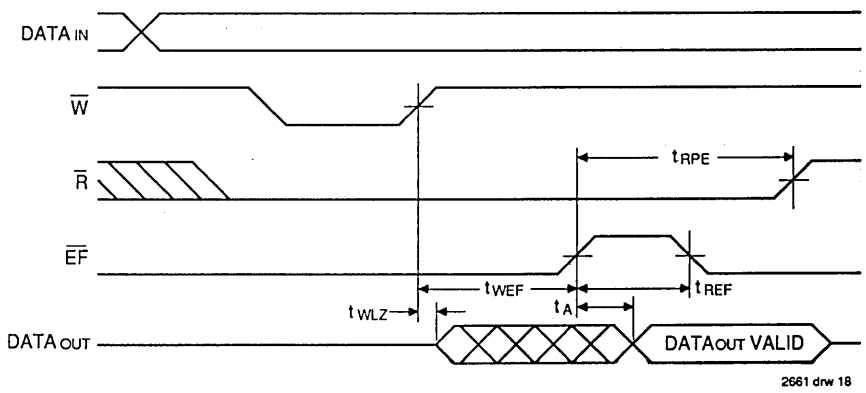


Figure 17. Read Data Flow-Through Mode

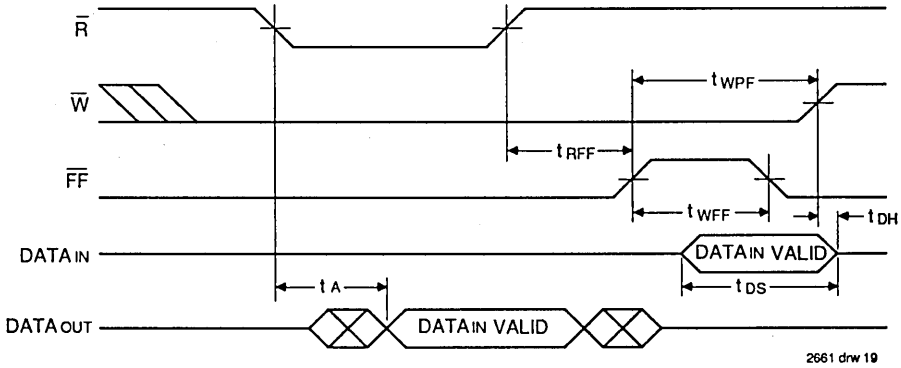
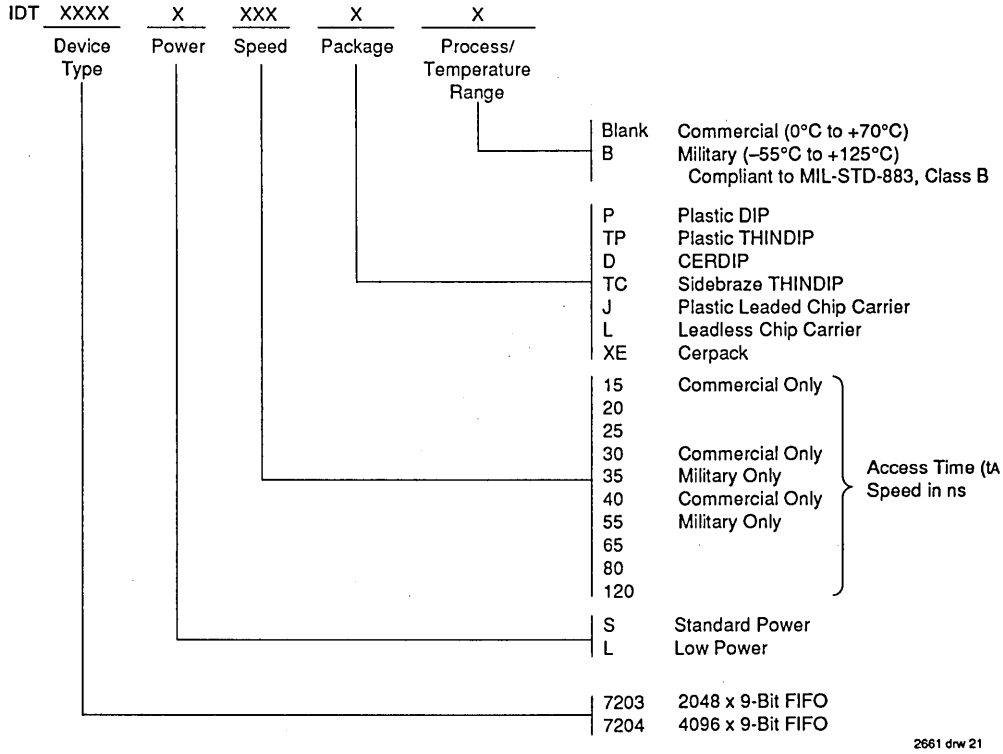


Figure 18. Write Data Flow-Through Mode

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 8192 x 9-BIT

IDT7205

FEATURES:

- First-In/First-Out dual-port memory
- 8192 x 9 organization
- Ultra high-speed: 20ns access time
- Low power consumption
  - — Active: 770mW (max.)
  - — Power-down: 27.5mW (max.)
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Pin and functionally compatible with IDT720X family
- Status Flag: Empty, Half-Full, Full
- Auto retransmit capability
- High-performance CEMOS™ technology
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7205 is a dual-port memory that loads and empties data on a first-in/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

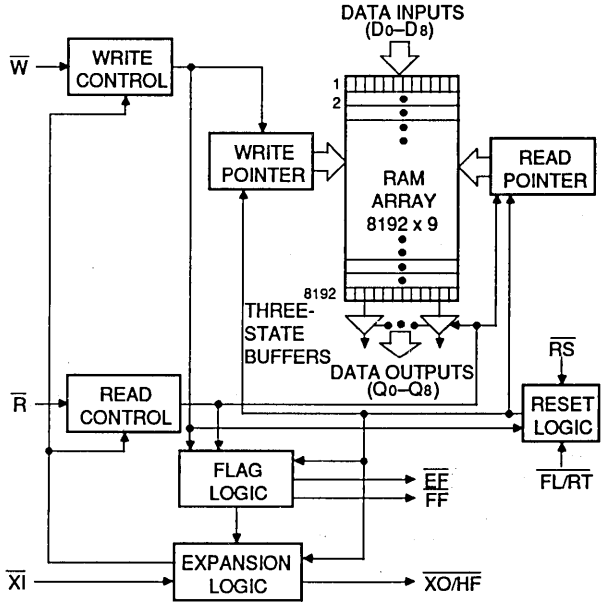
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins. The device has a read/write cycle time of 30ns (33MHz).

The device utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. It also features a Retransmit ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed low. A Half-Full Flag is available in the single device and width expansion modes.

The IDT7205 is fabricated using IDT's high-speed CEMOS technology. It is designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

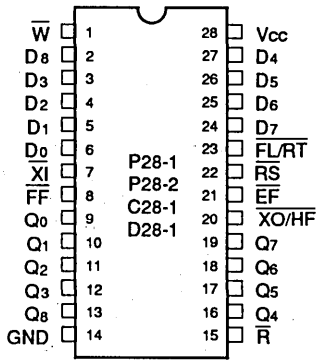
FUNCTIONAL BLOCK DIAGRAM



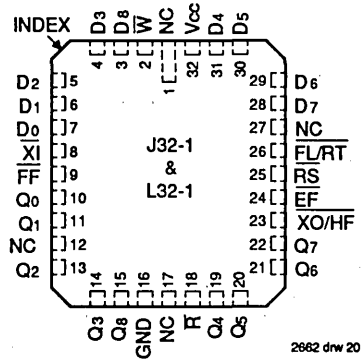
2662 drw 01

CEMOS is a trademark of Integrated Device Techology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW



PLCC/LCC
TOP VIEW

Consult Factory for CERPACK Pinout

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to + 7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	° C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	° C
TSTG	Storage Temperature	-55 to + 125	-65 to +155	° C
IOUT	DC Output Current	50	50	mA

2662 tbl 01

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH(1)	Input High Voltage Commercial	2.0	—	—	V
VIH(1)	Input High Voltage Military	2.2	—	—	V
VIL(2)	Input Low Voltage Commercial and Military	—	—	0.8	V

2662 tbl 02

NOTES:

1. VIH = 2.6V for $\overline{XI}$ input (commercial).
   VIH = 2.8V for $\overline{XI}$ input (military).
2. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: VCC = 5V ± 10%, TA = 0°C to +70°C; Military: VCC = 5V ± 10%, TA = -55°C to +125°C)

Symbol	Parameter	IDT7205L Commercial tA=20,25,35,50,80ns Min.	Typ.	Max.	IDT7205L Military tA=30,50,80ns Min.	Typ.	Max.	Unit
ILI(1)	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	µA
ILO(2)	Output Leakage Current	-10	—	10	-10	—	10	µA
VOH	Output Logic "1" Voltage, IOH = -2mA	2.4	—	—	2.4	—	—	V
VOL	Output Logic "0" Voltage, IOL = 8mA	—	—	0.4	—	—	0.4	V
ICC1(3, 4)	Active Power Supply Current	—	—	140	—	—	180	mA
ICC2(3)	Average Standby Current, ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = VIH)	—	—	15	—	—	20	mA
ICC3(3)	Power Down Current (All Input = VCC - 0.2V)	—	—	8	—	—	12	mA

2662 tbl 03

NOTES:

1. Measurements with 0.4 V≤ VIN ≤ VCC.
2. $\overline{R}$ ≥ VIH, 0.4 ≤ VOUT ≤ VCC.
3. ICC measurements are made with outputs open (only capacitive loading).
4. Tested at f = 20MHz.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameters	Commercial 7205L20 Min.	Commercial 7205L20 Max.	Commercial 7205L25 Min.	Commercial 7205L25 Max.	Military 7205L30 Min.	Military 7205L30 Max.	Unit
f_s	Shift Frequency	—	33.3	—	28.5	—	25	MHz
t_{RC}	Read Cycle Time	30	—	35	—	40	—	ns
t_A	Access Time	—	20	—	25	—	30	ns
t_{RR}	Read Recovery Time	10	—	10	—	10	—	ns
t_{RPW}	Read Pulse Width (2)	20	—	25	—	30	—	ns
t_{RLZ}	Read Low to Data Bus Low (3)	5	—	5	—	5	—	ns
t_{WLZ}	Write High to Data Bus Low Z (3,4)	5	—	5	—	5	—	ns
t_{DV}	Data Valid from Read High	5	—	5	—	5	—	ns
t_{RHZ}	Read High to Data Bus High Z (3)	—	15	—	18	—	20	ns
t_{WC}	Write Cycle Time	30	—	35	—	40	—	ns
t_{WPW}	Write Pulse Width (2)	20	—	25	—	30	—	ns
t_{WR}	Write Recovery Time	10	—	10	—	10	—	ns
t_{DS}	Data Set-up Time	12	—	15	—	18	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{RSC}	Reset Cycle Time	30	—	35	—	40	—	ns
t_{RS}	Reset Pulse Width(2)	20	—	25	—	30	—	ns
t_{RSS}	Reset Set-up Time(3)	20	—	25	—	30	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	10	—	ns
t_{RTC}	Retransmit Cycle Time	30	—	35	—	40	—	ns
t_{RT}	Retransmit Pulse Width(2)	20	—	25	—	30	—	ns
t_{RTS}	Retransmit Set-up Time (3)	20	—	25	—	30	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	10	—	10	—	ns
t_{EFL}	Reset to Empty Flag Low	—	30	—	35	—	40	ns
t_{HFH}, t_{FFH}	Reset to $\overline{HF}$ and $\overline{FF}$ High	—	30	—	35	—	40	ns
t_{REF}	Read Low to Empty Flag Low	—	20	—	25	—	30	ns
t_{RFF}	Read High to Full Flag High	—	20	—	25	—	30	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ High	20	—	25	—	30	—	ns
t_{WEF}	Write High to Empty Flag High	—	20	—	25	—	30	ns
t_{WFF}	Write Low to Full Flag Low	—	20	—	25	—	30	ns
t_{WHF}	Write Low to Half-Full Flag Low	—	30	—	35	—	40	ns
t_{RHF}	Read High to Half-Full Flag High	—	30	—	35	—	40	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	20	—	25	—	30	—	ns
t_{XOL}	Read/Write Low to $\overline{XO}$ Low	—	20	—	25	—	30	ns
t_{XOH}	Read/Write High to $\overline{XO}$ High	—	20	—	25	—	30	ns
t_{XI}	$\overline{XI}$ Pulse Width(2)	20	—	25	—	30	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	10	—	10	—	10	—	ns

NOTES:

2662 tbl 04

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

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AC ELECTRICAL CHARACTERISTICS (Continued)

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameters	Commercial		Commercial and Military				Unit
		7205L35		7205L50		7205L80		
		Min.	Max.	Min.	Max.	Min.	Max.	
f_S	Shift Frequency	—	22.2	—	15	—	10	MHz
t_{RC}	Read Cycle Time	45	—	65	—	100	—	ns
t_A	Access Time	—	35	—	50	—	80	ns
t_{RR}	Read Recovery Time	10	—	15	—	20	—	ns
t_{RPW}	Read Pulse Width (2)	35	—	50	—	80	—	ns
t_{RLZ}	Read Low to Data Bus Low (3)	5	—	10	—	10	—	ns
t_{WLZ}	Write High to Data Bus Low Z (3,4)	10	—	15	—	20	—	ns
t_{DV}	Data Valid from Read High	5	—	5	—	5	—	ns
t_{RHZ}	Read High to Data Bus High Z (3)	—	20	—	30	—	30	ns
t_{WC}	Write Cycle Time	45	—	65	—	100	—	ns
t_{WPW}	Write Pulse Width (2)	35	—	50	—	80	—	ns
t_{WR}	Write Recovery Time	10	—	15	—	20	—	ns
t_{DS}	Data Set-up Time	18	—	30	—	40	—	ns
t_{DH}	Data Hold Time	0	—	5	—	10	—	ns
t_{RSC}	Reset Cycle Time	45	—	65	—	100	—	ns
t_{RS}	Reset Pulse Width(2)	35	—	50	—	80	—	ns
t_{RSS}	Reset Set-up Time(3)	35	—	50	—	80	—	ns
t_{RSR}	Reset Recovery Time	10	—	15	—	20	—	ns
t_{RTC}	Retransmit Cycle Time	45	—	65	—	100	—	ns
t_{RT}	Retransmit Pulse Width(2)	35	—	50	—	80	—	ns
t_{RTS}	Retransmit Set-up Time (3)	35	—	50	—	80	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	15	—	20	—	ns
t_{EFL}	Reset to Empty Flag Low	—	45	—	65	—	100	ns
t_{HFH}, t_{FFH}	Reset to $\overline{HF}$ and $\overline{FF}$ High	—	45	—	65	—	100	ns
t_{REF}	Read Low to Empty Flag Low	—	30	—	45	—	60	ns
t_{RFF}	Read High to Full Flag High	—	30	—	45	—	60	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ High	35	—	50	—	80	—	ns
t_{WEF}	Write High to Empty Flag High	—	30	—	45	—	60	ns
t_{WFF}	Write Low to Full Flag Low	—	30	—	45	—	60	ns
t_{WHF}	Write Low to Half-Full Flag Low	—	45	—	65	—	100	ns
t_{RHF}	Read High to Half-Full Flag High	—	45	—	65	—	100	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	35	—	50	—	80	—	ns
t_{XOL}	Read/Write Low to $\overline{XO}$ Low	—	35	—	50	—	80	ns
t_{XOH}	Read/Write High to $\overline{XO}$ High	—	35	—	50	—	80	ns
t_{XI}	$\overline{XI}$ Pulse Width(2)	35	—	50	—	80	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	15	—	15	—	15	—	ns

NOTES:

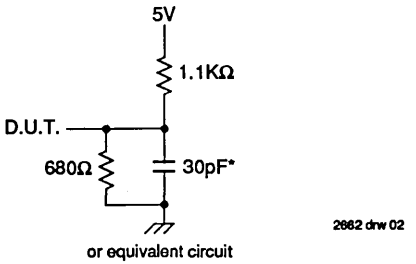
2662 tbl 04A

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2662 tbl 05



or equivalent circuit

Figure 1. Output Load

*Includes jig and scope capacitances.

CAPACITANCE[1] (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Condition	Max.	Unit
C_{IN}[3]	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}[2,3]	Output Capacitance	V_{OUT} = 0V	10	pF

2662 tbl 06

NOTES:
1. This parameter is sampled and not 100% tested.
2. With output deselected.
3. Characterized values, not currently tested.

SIGNAL DESCRIPTIONS

Inputs:

DATA IN (D_0–D_8) — Data inputs for 9-bit wide data.

Controls:

RESET ($\overline{RS}$) — Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place. **Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in the high state during the window shown in Figure 2 (i.e. t_{RSS} before the rising edge of $\overline{RS}$) and should not change until t_{RSR} after the rising edge of $\overline{RS}$. Half-Full Flag ($\overline{HF}$) will be reset to high after master Reset ($\overline{RS}$).**

WRITE ENABLE ($\overline{W}$) — A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of the Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any on-going read operation.

After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$) — A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$) provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis independent of any ongoing write operations. After Read Enable ($\overline{R}$) goes high, the Data Outputs (Q_0 through Q_8) will return to a high impedance condition until the next Read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, allowing the "final" read cycle but inhibiting further read operations, with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go high after t_{WEF} and a valid Read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$) — This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first device loaded (see Operating Modes). The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The IDT7205 can be made to retransmit data when the Retransmit Enable Control ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than 8192 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode and will affect the status of the Flags depending on the relative locations of the read and write pointers.

EXPANSION IN ($\overline{XI}$) — This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

6

Outputs:

FULL FLAG ($\overline{FF}$) — The Full Flag ($\overline{FF}$) will go low, inhibiting further write operations, when the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go low after 8192 writes.

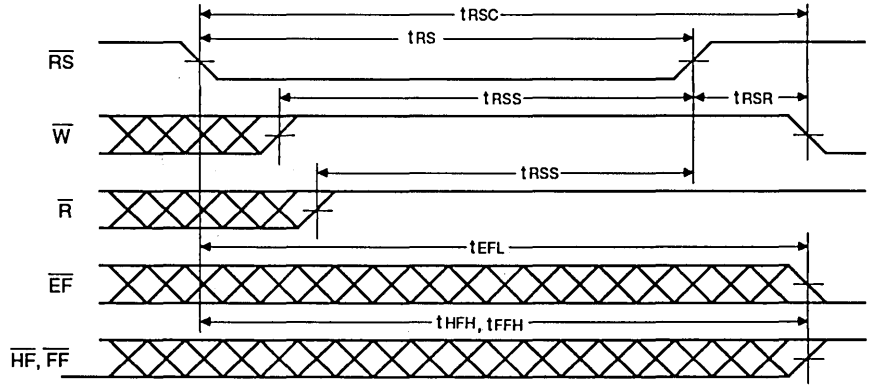
EMPTY FLAG ($\overline{EF}$) — The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$) — This is a dual-purpose output. In the single device mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory. There will be an $\overline{XO}$ pulse when the Write pointer reaches the last location of memory, and an additional $\overline{XO}$ pulse when the Read pointer reaches the last location of memory.

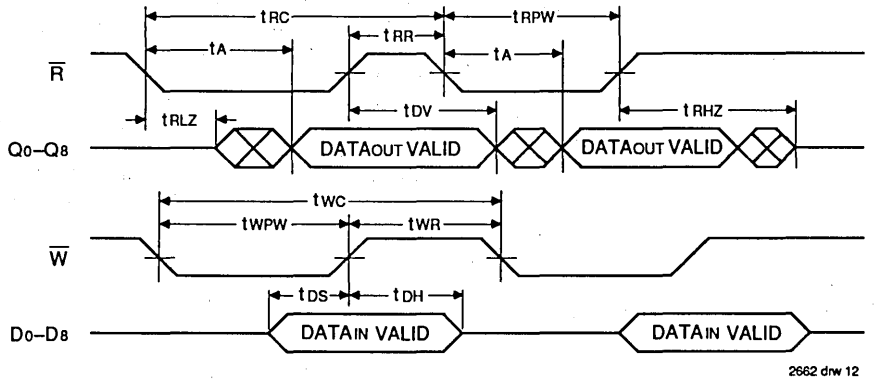
DATA OUTPUTS (Q_0-Q_8) — Q_0-Q_8 are data outputs for 9-bit wide data. These outputs are in a high impedance condition whenever Read ($\overline{R}$) is in a high state.



2662 drw 11

NOTES:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Reset, but flags will be valid at t_{RSC}.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{RS}$.

Figure 2. Reset



2662 drw 12

Figure 3. Asynchronous Write and Read Operation

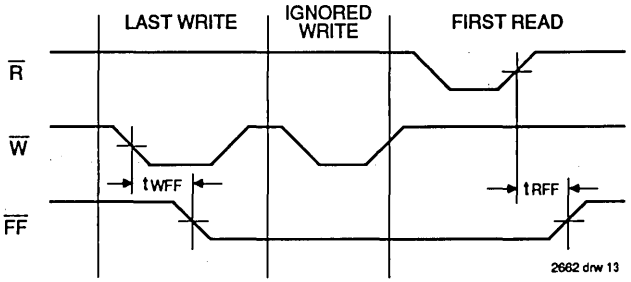


Figure 4. Full Flag From Last Write to First Read

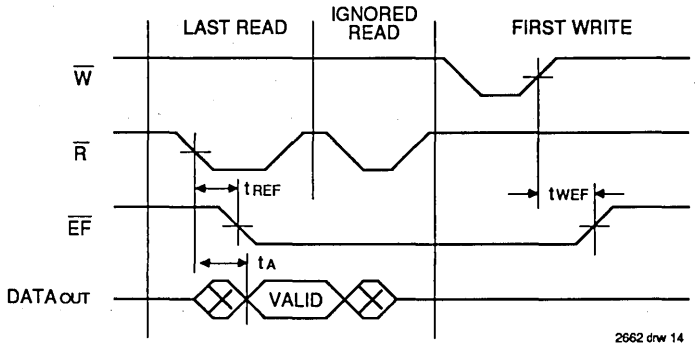
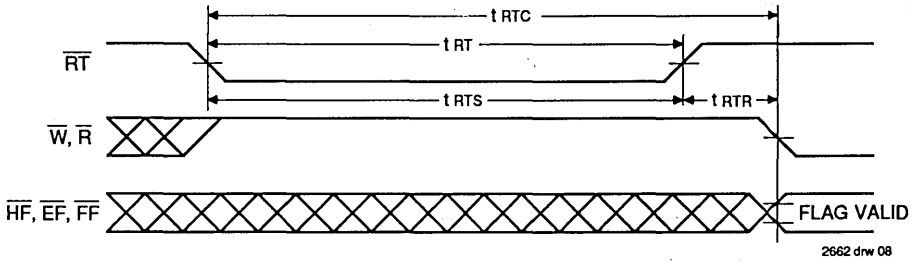


Figure 5. Empty Flag From Last Read to First Write



NOTE:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Retransmit, but flags will be valid at tRTC.

Figure 6. Retransmit

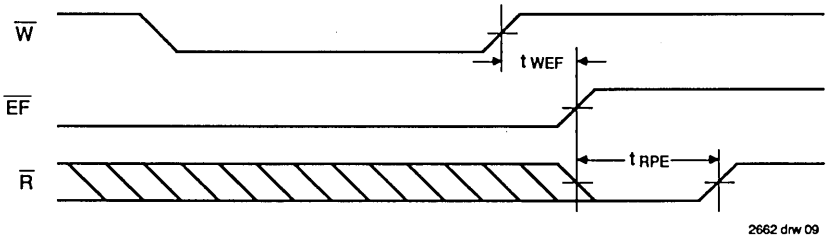


Figure 7. Empty Flag Timing

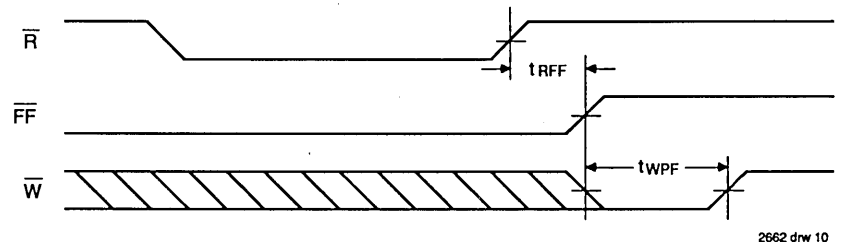


Figure 8. Full Flag Timing

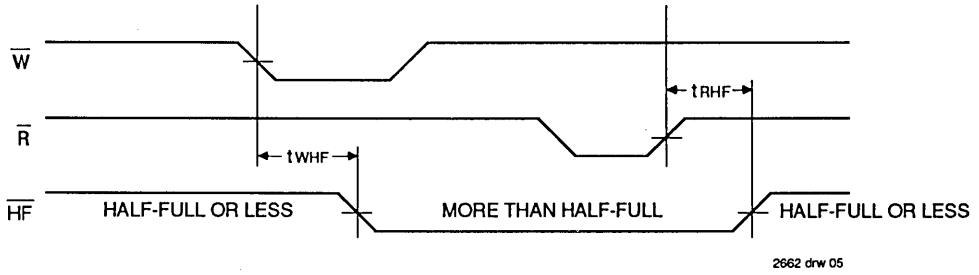


Figure 9. Half-Full Flag Timing

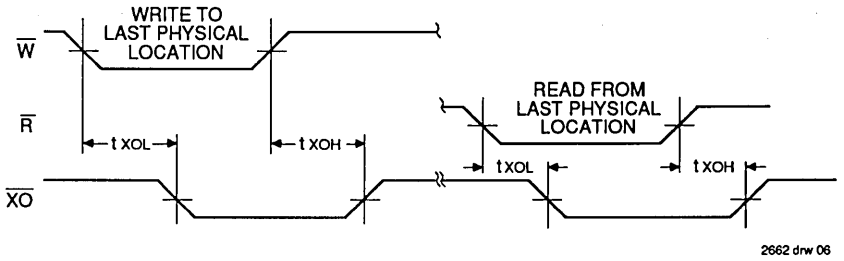


Figure 10. Expansion Out

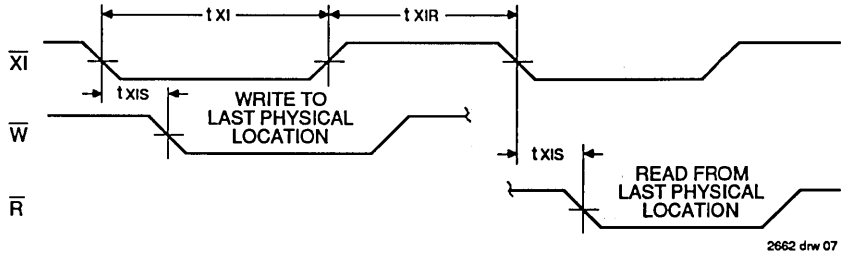


Figure 11. Expansion In

OPERATING MODES:

Single Device Mode

A single IDT7205 may be used when the application requirements are for 8192 words or less. The IDT7205 is in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 12).

Width Expansion Mode

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two IDT7205s. Any word width can be attained by adding additional IDT7205s.

Depth Expansion (Daisy Chain Mode)

The IDT7205 can easily be adapted to applications when the requirements are for greater than 8192 words. Figure 14 demonstrates Depth Expansion using three IDT7205s. Any depth can be attained by adding additional IDT7205s. The IDT7205 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 14.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 14.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

For additional information, refer to Tech Note 9: *Cascading FIFOs or FIFO Modules.*

Compound Expansion Mode

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 15).

Bidirectional Mode

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT7205s as shown in Figure 16. Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

Data Flow-Through Modes

Two types of flow-through modes are permitted, a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in (t_{WEF} + t_A) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary deassertion and then would be asserted. In the interval of time that $\overline{R}$ was low, more words can be written to the FIFO (the subsequent writes after the first write edge will deassert the empty flag); however, the same word (written on the first write edge), presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ is low. On toggling $\overline{R}$, the other words that were written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be deasserted but the $\overline{W}$ line being low causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

For additional information, refer to Tech Note 8: *Operating FIFOs on Full and Empty Boundary Conditions* and Tech Note 6: *Designing with FIFOs.*

6

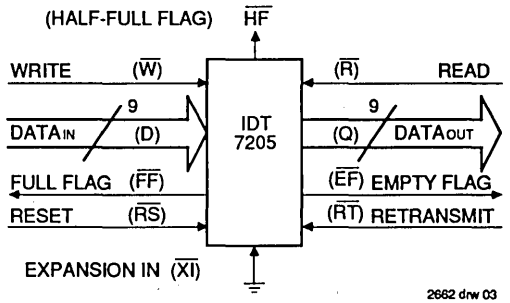
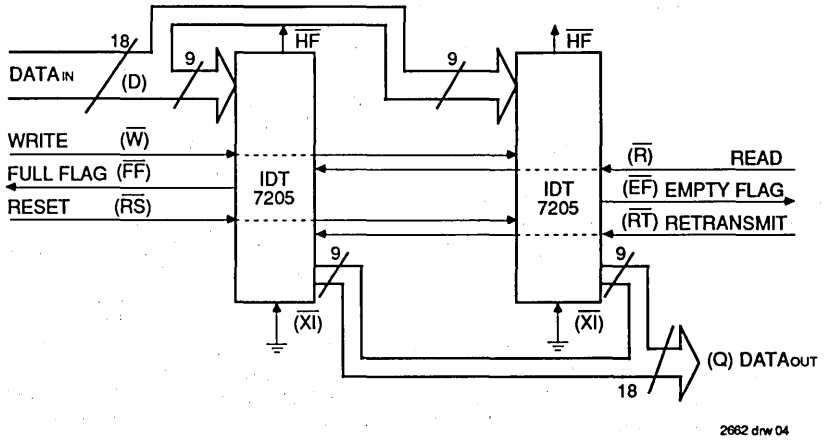


Figure 12. Block Diagram of 8192 x 9 FIFO Used in Single Device Mode



NOTE:
1. Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$ and $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output signals together.

Figure 13. Block Diagram of 8192 x 18 FIFO Memory Used in Width Expansion Mode

TRUTH TABLES

TABLE I – RESET AND RETRANSMIT

SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE:
1. Pointer will Increment if flag is high.

2662 tbl 07

TABLE II – RESET AND FIRST LOAD

DEPTH EXPANSION/COMPOUND EXPANSION MODE

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14.
2. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output

2662 tbl 08

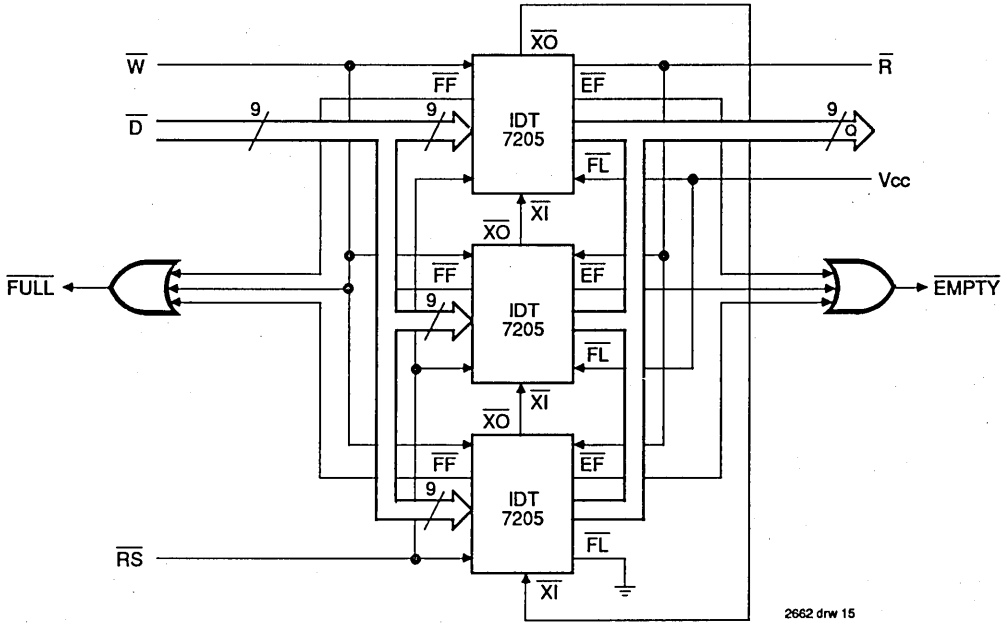
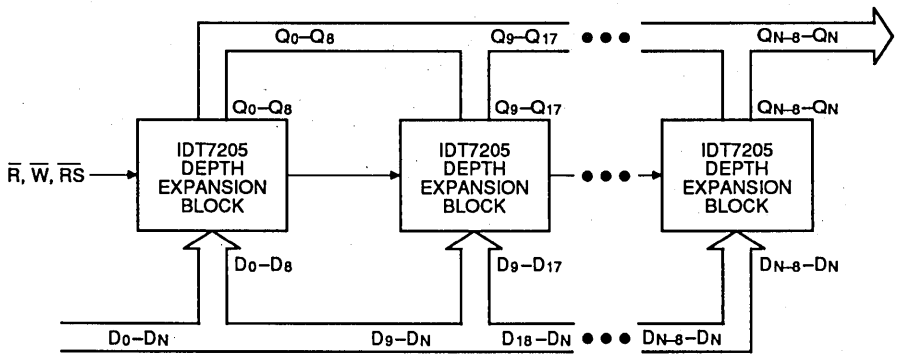


Figure 14. Block Diagram of 24,576 x 9 FIFO Memory (Depth Expansion)

6



NOTES:
1. For depth expansion block see section on Depth Expansion and Figure 14.
2. For Flag detection see section on Width Expansion and Figure 13.

Figure 15. Compound FIFO Expansion

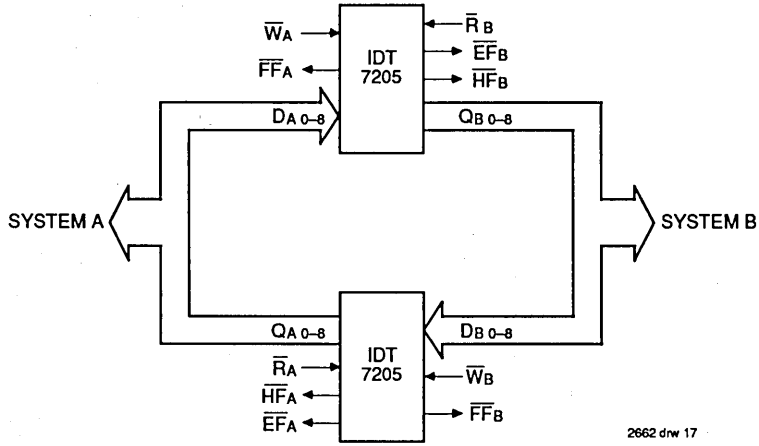


Figure 16. Bidirectional FIFO Mode

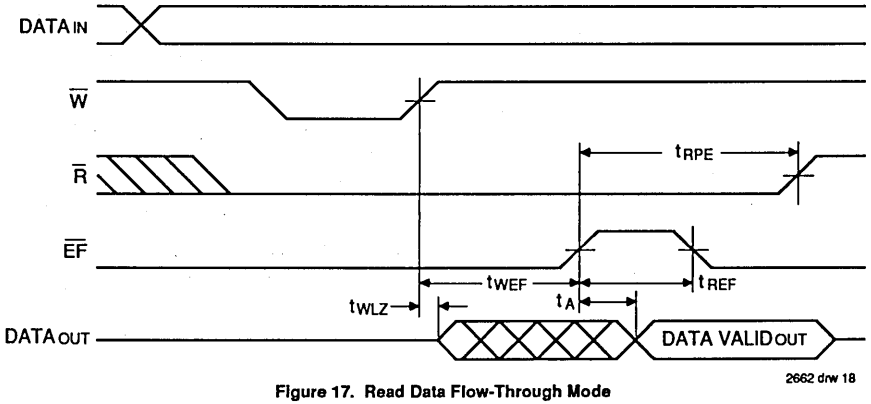


Figure 17. Read Data Flow-Through Mode

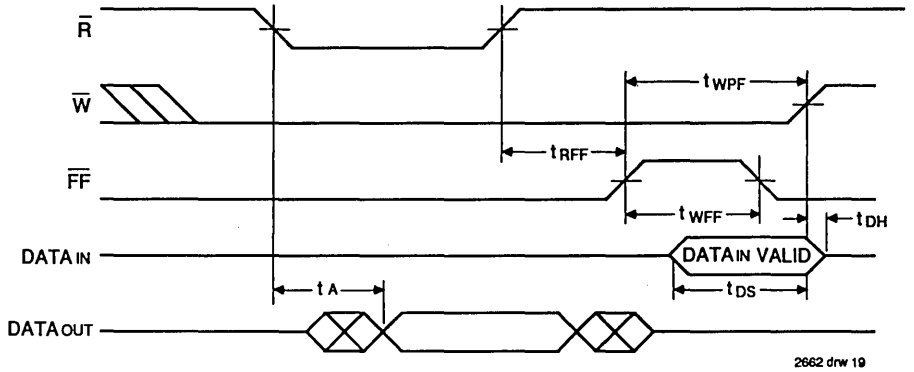
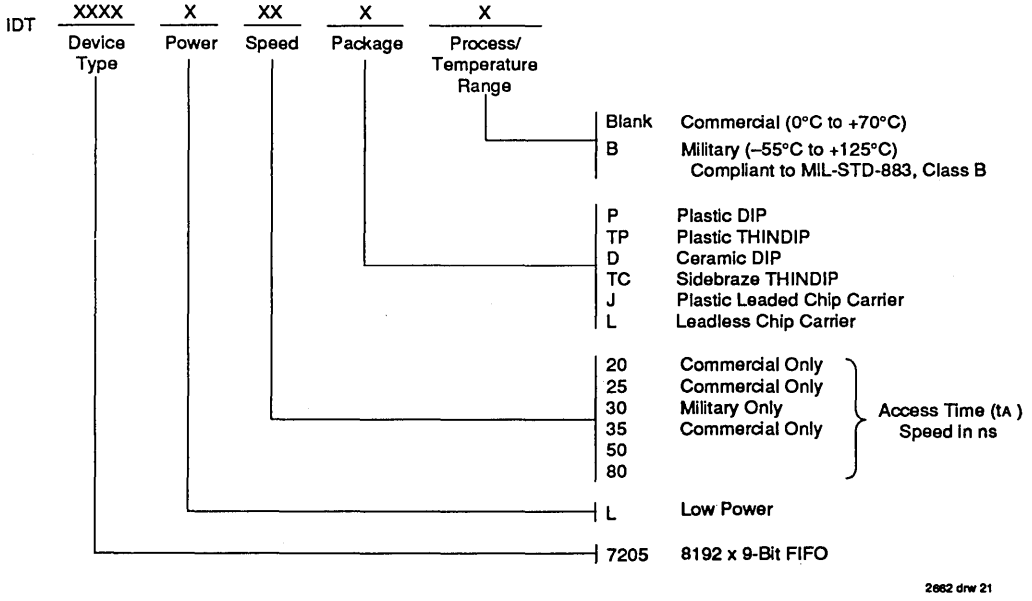


Figure 18. Write Data Flow-Through Mode

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 16K x 9-BIT

ADVANCE INFORMATION
IDT7206

FEATURES:

- First-In/First-Out dual-port memory
- 16K x 9-bit organization
- Low power consumption
- Ultra high speed: 25ns access time
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Pin-compatible with IDT720X FIFO family
- Half-Full Flag capability in single device mode
- Status flags: Empty, Half-Full, Full
- Auto retransmit capability
- High-performance submicron CEMOS™ technology
- Available in 28-pin plastic DIP, CERDIP and 32-pin surface mount LCC and PLCC
- Military product is compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7206 is a dual-port memory that loads and empties data on a first-in/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

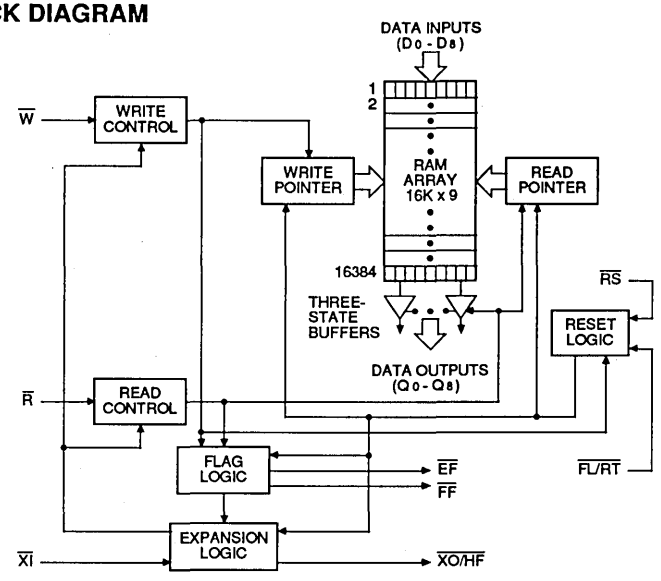
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The device has a read/write cycle time of 35ns (28MHz).

The device utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. It also features a RETRANSMIT ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position, when $\overline{RT}$ is pulsed low. A Half-Full Flag is available in the single device mode and width expansion modes.

The IDT7206 is fabricated using IDT's high-speed CEMOS submicron technology. They are designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications. The 16K x 9 allows a 16384 word structure without the need for expansion.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

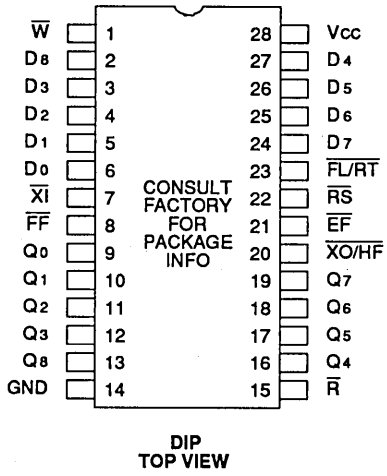
FUNCTIONAL BLOCK DIAGRAM



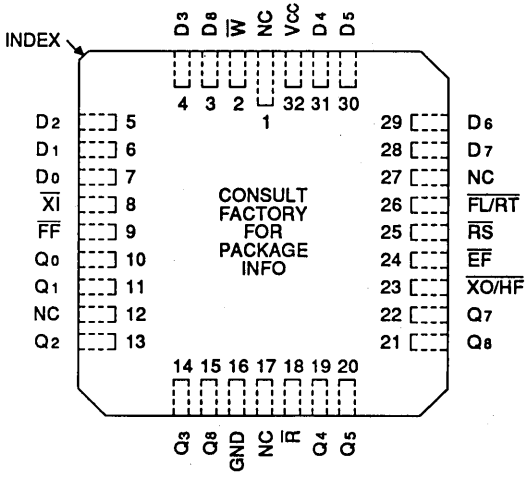
2705 drw 02

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW



LCC/PLCC
TOP VIEW

2705 drw 01

6

Integrated Device Technology, Inc.

CMOS PARALLEL FLAGGED FIFO WITH $\overline{OE}$ 1K x 9, 2K x 9, 4K x 9

IDT72021
IDT72031
IDT72041

FEATURES:

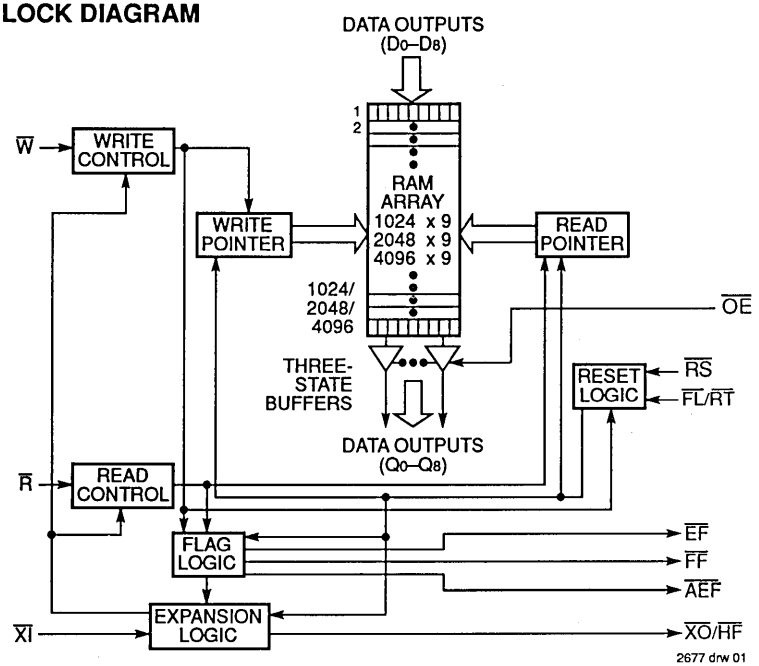
- First-In/First-Out dual-port memory
- Bit organization
  - IDT72021—1K x 9
  - IDT72031—2K x 9
  - IDT72041—4K x 9
- Ultra high speed
  - IDT72021—25ns access time, 35ns cycle time
  - IDT72031—35ns access time, 45ns cycle time
  - IDT72041—35ns access time, 45ns cycle time
- Easily expandable in word depth and/or width
- Asynchronous and simultaneous read and write
- Functionally equivalent to IDT7202/03/04 with Output Enable ($\overline{OE}$) and Almost Empty/Almost Full Flag ($\overline{AEF}$)
- Four status flags: Full, Empty, Half-Full (single device mode), and Almost Empty/Almost Full (7/8 empty or 7/8 full in single device mode)
- Output Enable controls the data output port
- Auto-retransmit capability
- Available in 32-pin DIP and surface mount 32-pin LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

IDT72021/031/041s are high-speed, low-power, dual-port memory devices commonly known as FIFOs (First-In/First-Out). Data can be written into and read from the memory at independent rates. The order of information stored and extracted does not change, but the rate of data entering the FIFO might be different than the rate leaving the FIFO. Unlike a static RAM, no address information is required because the read and write pointers advance sequentially. The IDT72021/031/041s can perform asynchronous and simultaneous read and write operations. There are four status flags, ($\overline{HF}$, $\overline{FF}$, $\overline{EF}$, $\overline{AEF}$) to monitor data overflow and underflow. Output Enable ($\overline{OE}$) is provided to control the flow of data through the output port. Additional key features are Write ($\overline{W}$), Read ($\overline{R}$), Retransmit ($\overline{RT}$), First Load ($\overline{FL}$), Expansion In ($\overline{XI}$) and Expansion Out ($\overline{XO}$). The IDT72021/031/041s are designed for those applications requiring data control flags and Output Enable ($\overline{OE}$) in multiprocessing and rate buffer applications.

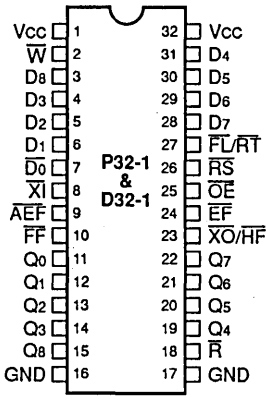
The IDT72021/031/041s are fabricated using IDT's CEMOS™ technology. Military grade product is manufactured in compliance with the latest version of MIL-STD-883, Class B, for high reliability systems.

FUNCTIONAL BLOCK DIAGRAM

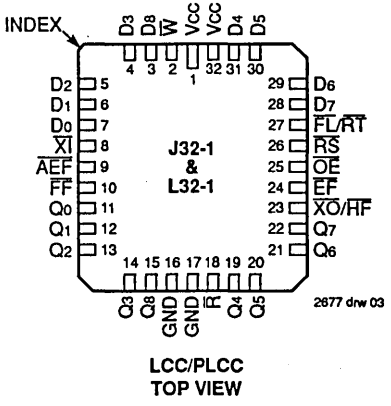


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW



LCC/PLCC
TOP VIEW

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D0–D8	Inputs	I	Data inputs for 9-bit wide data.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{HF}$ and $\overline{FF}$ go high, and $\overline{AEF}$ and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up. $\overline{R}$ and $\overline{W}$ must be high during $\overline{RS}$ cycle.
$\overline{W}$	Write	I	When WRITE is low, data can be written into the RAM array sequentially, independent of READ. In order for WRITE to be active, $\overline{FF}$ must be high. When the FIFO is full ($\overline{FF}$-low), the internal WRITE operation is blocked.
$\overline{R}$	Read	I	When READ is low, data can be read from the RAM array sequentially, independent of WRITE. In order for READ to be active, $\overline{EF}$ must be high. When the FIFO is empty ($\overline{EF}$-low), the internal READ operation is blocked. The three-state output buffer is controlled by the read signal and the external output control ($\overline{OE}$).
$\overline{FL/RT}$	First Load/ Retransmit	I	This is a dual purpose input. In the single device configuration ($\overline{XI}$ grounded), activating retransmit ($\overline{FL/RT}$-low) will set the internal READ pointer to the first location. There is no effect on the WRITE pointer. $\overline{R}$ and $\overline{W}$ must be high before setting $\overline{FL/RT}$ low. Retransmit is not compatible with depth expansion. In the depth expansion configuration, $\overline{FL/RT}$-low indicates the first activated device.
$\overline{XI}$	Expansion In	I	In the single device configuration, $\overline{XI}$ is grounded. In depth expansion or daisy chain expansion, $\overline{XI}$ is connected to $\overline{XO}$ (expansion out) of the previous device.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is set high, the data flow through the three-state output buffer is inhibited regardless of an active READ operation. A read operation does increment the read pointer in this situation. When $\overline{OE}$ is set low, Q0-Q8 are still in a high impedance condition if no READ occurs. For a complete READ operation with data ppearing on Q0-Q8, both $\overline{R}$ and $\overline{OE}$ should be asserted low.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ goes low, the device is full and further WRITE operations are inhibited. When $\overline{FF}$ is high, the device is not full.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ goes low, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is high, the device is not empty.
$\overline{AEF}$	Almost-Empty/ Almost-Full Flag	O	When $\overline{AEF}$ is low, the device is empty to 1/8 full or 7/8 to completely full. When $\overline{AEF}$ is high, the device is greater than 1/8 full, but less than 7/8 full.
$\overline{XO/HF}$	Expansion Out/ Half-Full Flag	O	This is a dual purpose output. In the single device configuration ($\overline{XI}$ grounded), the device is more than half full when $\overline{HF}$ is low. In the depth expansion configuration ($\overline{XO}$ connected to $\overline{XI}$ of the next device), a pulse is sent from $\overline{XO}$ to $\overline{XI}$ when the last location in the RAM array is filled.
Q0–Q8	Outputs	O	Data outputs for 9-bit wide data.

2677 tbl 01

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STATUS FLAG

Number of Words in FIFO						
1K	2K	4K	$\overline{FF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF}$
0	0	0	H	L	H	L
1-127	1-255	1-511	H	L	H	H
128-512	256-1024	512-2048	H	H	H	H
513-896	1025-1792	2049-3584	H	H	L	H
897-1023	1793-2047	3585-4095	H	L	L	H
1024	2048	4096	L	L	L	H

2677 tbl 102

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2677 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	pF

NOTE: 2677 tbl 04

1. These parameters are sampled and not 100% tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}(1)	Input Low Voltage Commercial and Military	—	—	0.8	V

NOTE: 2677 tbl 05

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS — IDT72021

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V±10%, T_A = –55°C to +125°C)

Symbol	Parameter	IDT72021 Commercial t_A=25,35ns			IDT72021 Military t_A=30,40ns			IDT72021 Commercial t_A=50,65,80,120ns			IDT72021 Military t_A=50,65,80,120ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI}[1]	Input Leakage Current (Any Input)	–1	—	1	–10	—	10	–1	—	1	–10	—	10	µA
I_{LO}[2]	Output Leakage Current	–10	—	10	–10	—	10	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OH} = –2mA	2.4	—	—	2.4	—	—	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8mA	—	—	0.4	—	—	0.4	—	—	0.4	—	—	0.4	V
I_{CC1}[3,4]	Active Power Supply Current	—	—	120	—	—	140	—	50	80	—	70	100	mA
I_{CC2}[3]	Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH})	—	—	12	—	—	20	—	5	8	—	8	15	mA
I_{CC3}[3]	Power Down Current (All Input = V_{CC} – 0.2V)	—	—	500	—	—	900	—	—	500	—	—	900	µA

2677 tbl 06

DC ELECTRICAL CHARACTERISTICS — IDT72031, IDT72041

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V±10%, T_A = –55°C to +125°C)

Symbol	Parameter	IDT72031 IDT72041 Commercial t_A=35,50,65,80,120ns			IDT72031 IDT72041 Military t_A=40,50,65,80,120ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI}[1]	Input Leakage Current (Any Input)	–1	—	1	–10	—	10	µA
I_{LO}[2]	Output Leakage Current	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = –2mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA	—	—	0.4	—	—	0.4	V
I_{CC1}[3,5]	Active Power Supply Current	—	75	120	—	100	150	mA
I_{CC2}[3]	Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RST}$ = $\overline{FL/RT}$ = V_{IH})	—	8	12	—	12	25	mA
I_{CC3}[3]	Power Down Current (All Input = V_{CC} – 0.2V)	—	—	2	—	—	4	mA

2677 tbl 07

NOTES:
1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. I_{CC} measurements are made with $\overline{OE}$ = HIGH.
4. Tested at f = 20MHz.
5. Tested at f = 15.3 MHz.

6

AC ELECTRICAL CHARACTERISTICS — IDT72021[1]

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V±10%, T_A = –55°C to +125°C)

		Com'l		Mil.		Com'l		Mil.		
		72021 x 25		72021 x 30		72021 x 35		72021 x 40		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
fS	Shift Frequency	—	28.5	—	25	—	22.2	—	20	MHz
tRC	$\overline{R}$ Cycle Time	35	—	40	—	45	—	50	—	ns
tA	Access Time	—	25	—	30	—	35	—	40	ns
tRR	$\overline{R}$ Recovery Time	10	—	10	—	10	—	10	—	ns
tRPW	$\overline{R}$ Pulse Width[2]	25	—	30	—	35	—	40	—	ns
tRLZ	$\overline{R}$ Pulse Low to Data Bus at Low Z[3]	5	—	5	—	5	—	5	—	ns
tWLZ	$\overline{W}$ Pulse High to Data Bus at Low Z[3,4]	5	—	5	—	5	—	5	—	ns
tDV	Data Valid from $\overline{R}$ Pulse High	5	—	5	—	5	—	5	—	ns
tRHZ	$\overline{R}$ Pulse High to Data Bus at High Z[3]	—	18	—	20	—	20	—	25	ns
tWC	$\overline{W}$ Cycle Time	35	—	40	—	45	—	50	—	ns
tWPW	$\overline{W}$ Pulse Width[2]	25	—	30	—	35	—	40	—	ns
tWR	$\overline{W}$ Recovery Time	10	—	10	—	10	—	10	—	ns
tDS	Data Set-up Time	15	—	18	—	18	—	20	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tRSC	$\overline{RS}$ Cycle Time	35	—	40	—	45	—	50	—	ns
tRS	$\overline{RS}$ Pulse Width[2]	25	—	30	—	35	—	40	—	ns
tRSS	$\overline{RS}$ Set-up Time	25	—	30	—	35	—	40	—	ns
tRSR	$\overline{RS}$ Recovery Time	10	—	10	—	10	—	10	—	ns
tRTC	$\overline{RT}$ Cycle Time	35	—	40	—	45	—	50	—	ns
tRT	$\overline{RT}$ Pulse Width[2]	25	—	30	—	35	—	40	—	ns
tRTR	$\overline{RT}$ Recovery Time	10	—	10	—	10	—	10	—	ns
tRSF1	$\overline{RS}$ to $\overline{EF}$ and $\overline{AEF}$ Low	—	35	—	40	—	45	—	50	ns
tRSF2	$\overline{RS}$ to $\overline{HF}$ and $\overline{FF}$ High	—	35	—	40	—	45	—	50	ns
tREF	$\overline{R}$ Low to $\overline{EF}$ Low	—	25	—	30	—	30	—	35	ns
tRFF	$\overline{R}$ High to $\overline{FF}$ High	—	25	—	30	—	30	—	35	ns
tRPE	$\overline{R}$ Pulse Width After $\overline{EF}$ High	25	—	30	—	35	—	40	—	ns
tWEF	$\overline{W}$ High to $\overline{EF}$ High	—	25	—	30	—	30	—	35	ns
tWFF	$\overline{W}$ Low to $\overline{EF}$ Low	—	25	—	30	—	30	—	35	ns
tWHF	$\overline{W}$ Low to $\overline{HF}$ Low	—	35	—	40	—	45	—	50	ns
tRHF	$\overline{R}$ High to $\overline{HF}$ High	—	35	—	40	—	45	—	50	ns
tWPF	$\overline{W}$ Pulse Width after $\overline{FF}$ High	25	—	30	—	35	—	40	—	ns
tRF	$\overline{R}$ High to Transitioning $\overline{AEF}$	—	35	—	40	—	45	—	50	ns
tWF	$\overline{W}$ Low to Transitioning $\overline{AEF}$	—	35	—	40	—	45	—	50	ns
tOEHZ	$\overline{OE}$ High to High-Z (Disable)[3]	0	12	0	15	0	17	0	20	ns
tOELZ	$\overline{OE}$ Low to Low-Z (Enable)[3]	0	12	0	15	0	17	0	20	ns
tAOE	$\overline{OE}$ Low Data Valid (Q_0–Q_8)	—	15	—	18	—	20	—	25	ns

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

2677 tbl 08

AC ELECTRICAL CHARACTERISTICS — IDT72021[1] (Continued)

(Commercial: Vcc = 5.0V±10%, TA = 0°C to +70°C; Military: Vcc = 5V±10%, TA = –55°C to +125°C)

		Military and Commercial								
		72021 x 50		72021 x 65		72021 x 80		72021 x 120		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
fS	Shift Frequency	—	15	—	12.5	—	10	—	7	MHz
tRC	$\overline{R}$ Cycle Time	65	—	80	—	100	—	140	—	ns
tA	Access Time	—	50	—	65	—	80	—	120	ns
tRR	$\overline{R}$ Recovery Time	15	—	15	—	20	—	20	—	ns
tRPW	$\overline{R}$ Pulse Width[2]	50	—	65	—	80	—	120	—	ns
tRLZ	$\overline{R}$ Pulse Low to Data Bus at Low Z[3]	10	—	10	—	10	—	10	—	ns
tWLZ	$\overline{W}$ Pulse High to Data Bus at Low Z[3,4]	5	—	5	—	5	—	5	—	ns
tDV	Data Valid from $\overline{R}$ Pulse High	5	—	5	—	5	—	5	—	ns
tRHZ	$\overline{R}$ Pulse High to Data Bus at High Z[3]	—	30	—	30	—	30	—	35	ns
tWC	$\overline{W}$ Cycle Time	65	—	80	—	100	—	140	—	ns
tWPW	$\overline{W}$ Pulse Width[2]	50	—	65	—	80	—	120	—	ns
tWR	$\overline{W}$ Recovery Time	15	—	15	—	20	—	20	—	ns
tDS	Data Set-up Time	30	—	30	—	40	—	40	—	ns
tDH	Data Hold Time	5	—	10	—	10	—	10	—	ns
tRSC	$\overline{RS}$ Cycle Time	65	—	80	—	100	—	140	—	ns
tRS	$\overline{RS}$ Pulse Width[2]	50	—	65	—	80	—	120	—	ns
tRSS	$\overline{RS}$ Set-up Time	50	—	65	—	80	—	120	—	ns
tRSR	$\overline{RS}$ Recovery Time	15	—	15	—	20	—	20	—	ns
tRTC	$\overline{RT}$ Cycle Time	65	—	80	—	100	—	140	—	ns
tRT	$\overline{RT}$ Pulse Width[2]	50	—	65	—	80	—	120	—	ns
tRTR	$\overline{RT}$ Recovery Time	15	—	15	—	20	—	20	—	ns
tRSF1	$\overline{RS}$ to $\overline{EF}$ and $\overline{AEF}$ Low	—	65	—	80	—	100	—	140	ns
tRSF2	$\overline{RS}$ to $\overline{HF}$ and $\overline{FF}$ High	—	65	—	80	—	100	—	140	ns
tREF	$\overline{R}$ Low to $\overline{EF}$ Low	—	45	—	60	—	60	—	60	ns
tRFF	$\overline{R}$ High to $\overline{FF}$ High	—	45	—	60	—	60	—	60	ns
tRPE	$\overline{R}$ Pulse Width After $\overline{EF}$ High	50	—	65	—	80	—	120	—	ns
tWEF	$\overline{W}$ High to $\overline{EF}$ High	—	45	—	60	—	60	—	60	ns
tWFF	$\overline{W}$ Low to $\overline{EF}$ Low	—	45	—	60	—	60	—	60	ns
tWHF	$\overline{W}$ Low to $\overline{HF}$ Low	—	65	—	80	—	100	—	140	ns
tRHF	$\overline{R}$ High to $\overline{HF}$ High	—	65	—	80	—	100	—	140	ns
tWPF	$\overline{W}$ Pulse Width after $\overline{FF}$ High	50	—	65	—	80	—	120	—	ns
tRF	$\overline{R}$ High to Transitioning $\overline{AEF}$	—	65	—	80	—	100	—	140	ns
tWF	$\overline{W}$ Low to Transitioning $\overline{AEF}$	—	65	—	80	—	100	—	140	ns
tOEHZ	$\overline{OE}$ High to High-Z (Disable)[3]	0	25	0	30	0	30	0	30	ns
tOELZ	$\overline{OE}$ Low to Low-Z (Enable)[3]	0	25	0	30	0	30	0	30	ns
tAOE	$\overline{OE}$ Low Data Valid (Q_0–Q_8)	—	30	—	40	—	40	—	40	ns

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

2677 tbl 09

6

AC ELECTRICAL CHARACTERISTICS — IDT72031, IDT72041[1]

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V±10%, T_A = −55°C to +125°C)

		72031 x 35 72041 x 35		72031 x 40 72041 x 40		72031 x 50 72041 x 50		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
f_S	Shift Frequency	—	22.2	—	20	—	15	MHz
t_{RC}	$\overline{R}$ Cycle Time	45	—	50	—	65	—	ns
t_A	Access Time	—	35	—	40	—	50	ns
t_{RR}	$\overline{R}$ Recovery Time	10	—	10	—	15	—	ns
t_{RPW}	$\overline{R}$ Pulse Width[2]	35	—	40	—	50	—	ns
t_{RLZ}	$\overline{R}$ Pulse Low to Data Bus at Low Z[3]	5	—	5	—	10	—	ns
t_{WLZ}	$\overline{W}$ Pulse High to Data Bus at Low Z[3,4]	5	—	5	—	5	—	ns
t_{DV}	Data Valid from $\overline{R}$ Pulse High	5	—	5	—	5	—	ns
t_{RHZ}	$\overline{R}$ Pulse High to Data Bus at High Z[3]	—	20	—	25	—	30	ns
t_{WC}	$\overline{W}$ Cycle Time	45	—	50	—	65	—	ns
t_{WPW}	$\overline{W}$ Pulse Width[2]	35	—	40	—	50	—	ns
t_{WR}	$\overline{W}$ Recovery Time	10	—	10	—	15	—	ns
t_{DS}	Data Set-up Time	18	—	20	—	30	—	ns
t_{DH}	Data Hold Time	0	—	0	—	5	—	ns
t_{RSC}	$\overline{RS}$ Cycle Time	45	—	50	—	65	—	ns
t_{RS}	$\overline{RS}$ Pulse Width[2]	35	—	40	—	50	—	ns
t_{RSS}	$\overline{RS}$ Set-up Time	35	—	40	—	50	—	ns
t_{RSR}	$\overline{RS}$ Recovery Time	10	—	10	—	15	—	ns
t_{RTC}	$\overline{RT}$ Cycle Time	45	—	50	—	65	—	ns
t_{RT}	$\overline{RT}$ Pulse Width[2]	35	—	40	—	50	—	ns
t_{RTR}	$\overline{RT}$ Recovery Time	10	—	10	—	15	—	ns
t_{RSF1}	$\overline{RS}$ to $\overline{EF}$ and $\overline{AEF}$ Low	—	45	—	50	—	65	ns
t_{RSF2}	$\overline{RS}$ to $\overline{HF}$ and $\overline{FF}$ High	—	45	—	50	—	65	ns
t_{REF}	$\overline{R}$ Low to $\overline{EF}$ Low	—	30	—	35	—	45	ns
t_{RFF}	$\overline{R}$ High to $\overline{FF}$ High	—	30	—	35	—	45	ns
t_{RPE}	$\overline{R}$ Pulse Width After $\overline{EF}$ High	35	—	40	—	50	—	ns
t_{WEF}	$\overline{W}$ High to $\overline{EF}$ High	—	30	—	35	—	45	ns
t_{WFF}	$\overline{W}$ Low to $\overline{EF}$ Low	—	30	—	35	—	45	ns
t_{WHF}	$\overline{W}$ Low to $\overline{HF}$ Low	—	45	—	50	—	65	ns
t_{RHF}	$\overline{R}$ High to $\overline{HF}$ High	—	45	—	50	—	65	ns
t_{WPF}	$\overline{W}$ Pulse Width after $\overline{FF}$ High	35	—	40	—	50	—	ns
t_{RF}	$\overline{R}$ High to Transitioning $\overline{AEF}$	—	45	—	50	—	65	ns
t_{WF}	$\overline{W}$ Low to Transitioning $\overline{AEF}$	—	45	—	50	—	65	ns
t_{OEHZ}	$\overline{OE}$ High to High-Z (Disable)[3]	0	17	0	20	0	25	ns
t_{OELZ}	$\overline{OE}$ Low to Low-Z (Enable)[3]	0	17	0	20	0	25	ns
t_{AOE}	$\overline{OE}$ Low Data Valid (Q_0–Q_8)	—	20	—	25	—	30	ns

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

2677 tbl 10

AC ELECTRICAL CHARACTERISTICS — IDT72031, IDT72041[1] (Continued)

(Commercial: Vcc = 5.0V±10%, TA = 0°C to +70°C; Military: Vcc = 5V±10%, TA = –55°C to +125°C)

Symbol	Parameter	72031 x 65 72041 x 65		72031 x 80 72041 x 80		72031 x 120 72041 x 120		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
fS	Shift Frequency	—	12.5	—	10	—	7	MHz
tRC	$\overline{R}$ Cycle Time	80	—	100	—	140	—	ns
tA	Access Time	—	65	—	80	—	120	ns
tRR	$\overline{R}$ Recovery Time	15	—	20	—	20	—	ns
tRPW	$\overline{R}$ Pulse Width[2]	65	—	80	—	120	—	ns
tRLZ	$\overline{R}$ Pulse Low to Data Bus at Low Z[3]	10	—	10	—	10	—	ns
tWLZ	$\overline{W}$ Pulse High to Data Bus at Low Z[3,4]	5	—	5	—	5	—	ns
tDV	Data Valid from $\overline{R}$ Pulse High	5	—	5	—	5	—	ns
tRHZ	$\overline{R}$ Pulse High to Data Bus at High Z[3]	—	30	—	30	—	35	ns
tWC	$\overline{W}$ Cycle Time	80	—	100	—	140	—	ns
tWPW	$\overline{W}$ Pulse Width[2]	65	—	80	—	120	—	ns
tWR	$\overline{W}$ Recovery Time	15	—	20	—	20	—	ns
tDS	Data Set-up Time	30	—	40	—	40	—	ns
tDH	Data Hold Time	10	—	10	—	10	—	ns
tRSC	$\overline{RS}$ Cycle Time	80	—	100	—	140	—	ns
tRS	$\overline{RS}$ Pulse Width[2]	65	—	80	—	120	—	ns
tRSS	$\overline{RS}$ Set-up Time	65	—	80	—	120	—	ns
tRSR	$\overline{RS}$ Recovery Time	15	—	20	—	20	—	ns
tRTC	$\overline{RT}$ Cycle Time	80	—	100	—	140	—	ns
tRT	$\overline{RT}$ Pulse Width[2]	65	—	80	—	120	—	ns
tRTR	$\overline{RT}$ Recovery Time	15	—	20	—	20	—	ns
tRSF1	$\overline{RS}$ to $\overline{EF}$ and $\overline{AEF}$ Low	—	80	—	100	—	140	ns
tRSF2	$\overline{RS}$ to $\overline{HF}$ and $\overline{FF}$ High	—	80	—	100	—	140	ns
tREF	$\overline{R}$ Low to $\overline{EF}$ Low	—	60	—	60	—	60	ns
tRFF	$\overline{R}$ High to $\overline{FF}$ High	—	60	—	60	—	60	ns
tRPE	$\overline{R}$ Pulse Width After $\overline{EF}$ High	65	—	80	—	120	—	ns
tWEF	$\overline{W}$ High to $\overline{EF}$ High	—	60	—	60	—	60	ns
tWFF	$\overline{W}$ Low to $\overline{EF}$ Low	—	60	—	60	—	60	ns
tWHF	$\overline{W}$ Low to $\overline{HF}$ Low	—	80	—	100	—	140	ns
tRHF	$\overline{R}$ High to $\overline{HF}$ High	—	80	—	100	—	140	ns
tWPF	$\overline{W}$ Pulse Width after $\overline{FF}$ High	65	—	80	—	120	—	ns
tRF	$\overline{R}$ High to Transitioning $\overline{AEF}$	—	80	—	100	—	140	ns
tWF	$\overline{W}$ Low to Transitioning $\overline{AEF}$	—	80	—	100	—	140	ns
tOEHZ	$\overline{OE}$ High to High-Z (Disable)[3]	0	30	0	30	0	30	ns
tOELZ	$\overline{OE}$ Low to Low-Z (Enable)[3]	0	30	0	30	0	30	ns
tAOE	$\overline{OE}$ Low Data Valid (Q0–Q8)	—	40	—	40	—	40	ns

NOTES:

2677 tbl 11

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

6

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2677 tbl 12

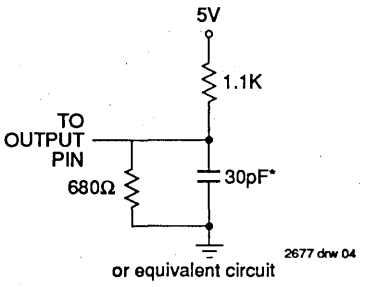


Figure 1. Output Load

* Includes scope and jig capacitances.

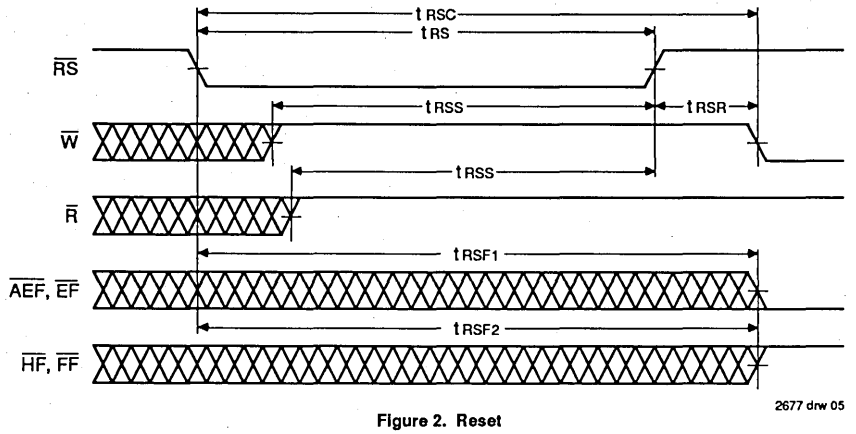


Figure 2. Reset

NOTES:
1. $\overline{EF}$, $\overline{FF}$, $\overline{HF}$, and $\overline{AEF}$ may change status during Reset, but flags will be valid at tRSC.
2. $\overline{W}$ and $\overline{R}$ = VIH around the rising edge of $\overline{RS}$.

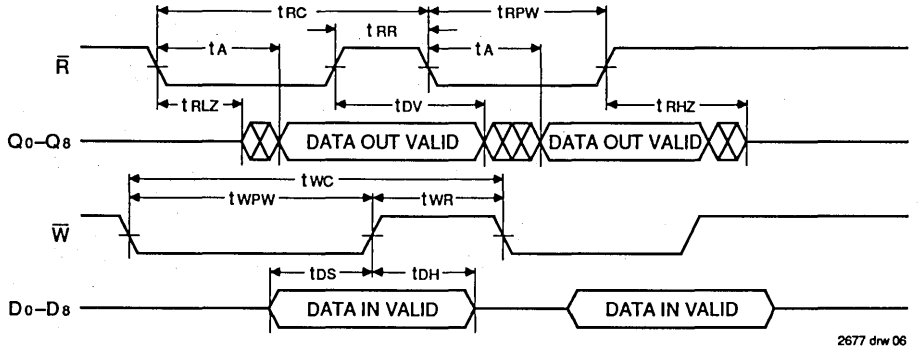


Figure 3. Asynchronous Write and Read Operation

NOTE:
1. Assume $\overline{OE}$ is asserted low.

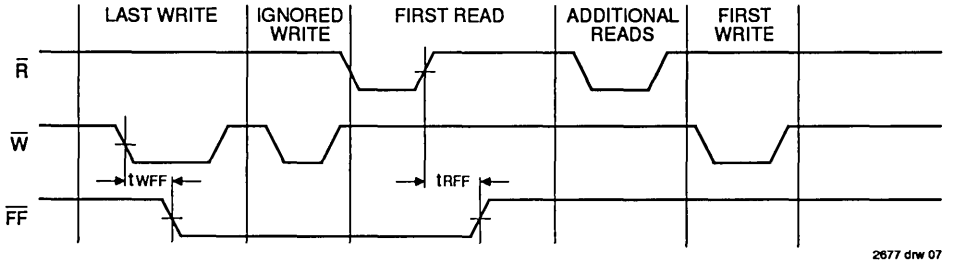


Figure 4. Full Flag From Last Write to First Read

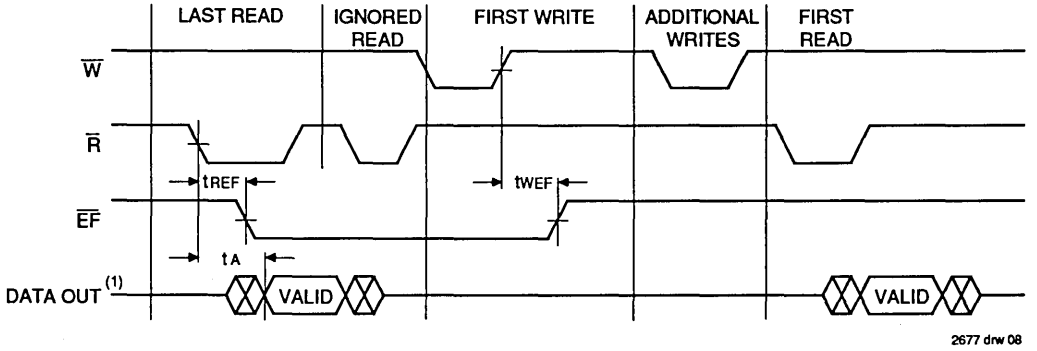


Figure 5. Empty Flag From Last Read to First Write

NOTE:
1. Assume $\overline{OE}$ is asserted low.

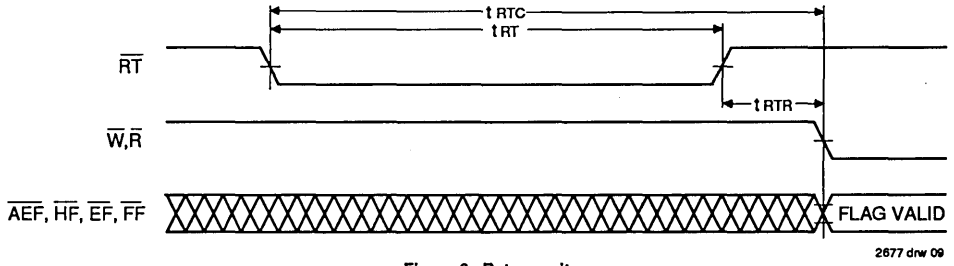


Figure 6. Retransmit

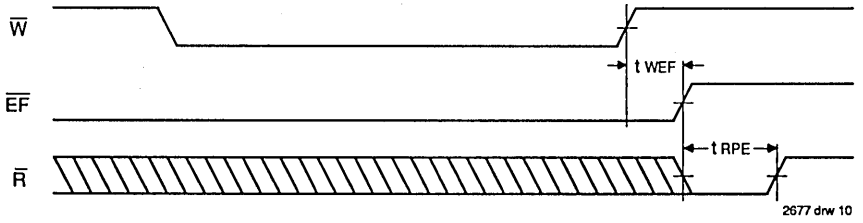


Figure 7. Empty Flag Timing

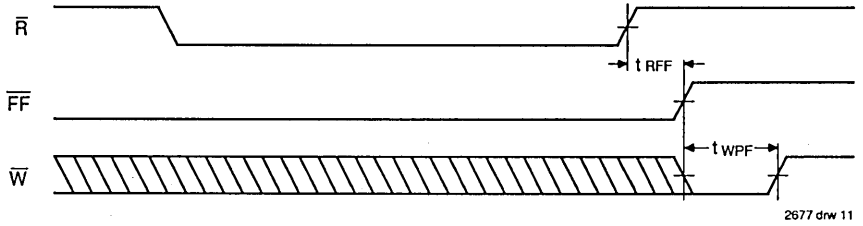


Figure 8. Full Flag Timing

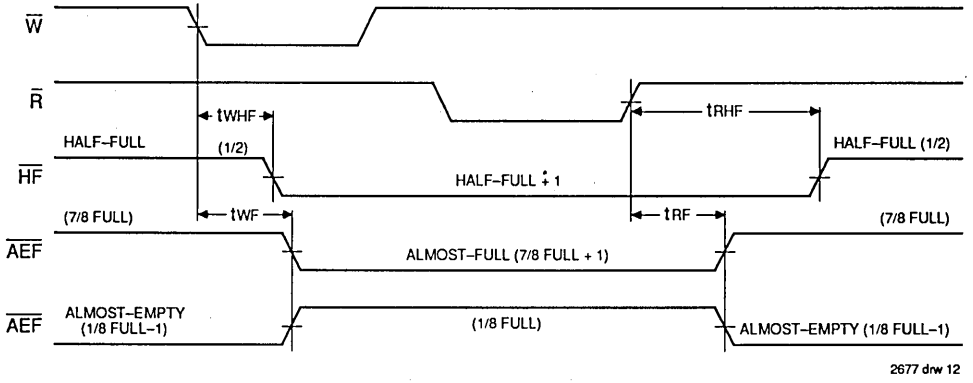


Figure 9. Almost-Empty/Almost-Full Flag and Half-Full Timings

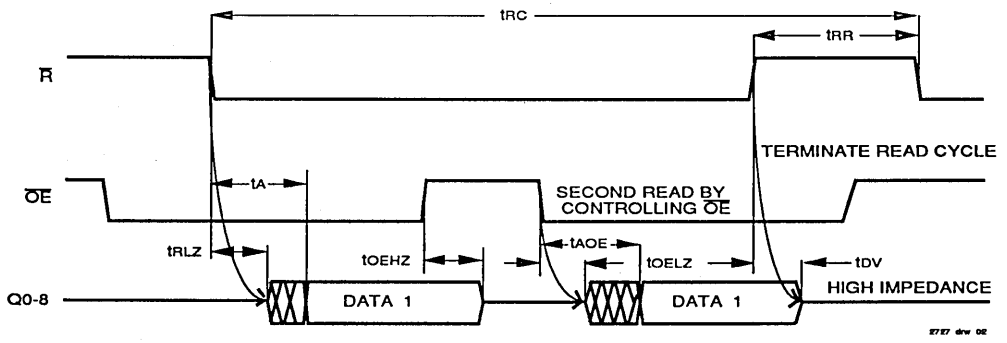


Figure 10. Output Enable and Read Operation Timings

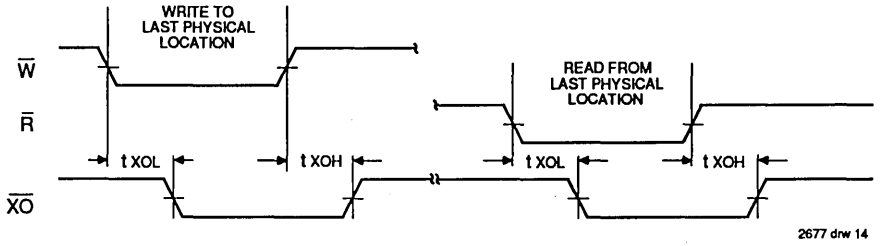


Figure 11. Expansion Out

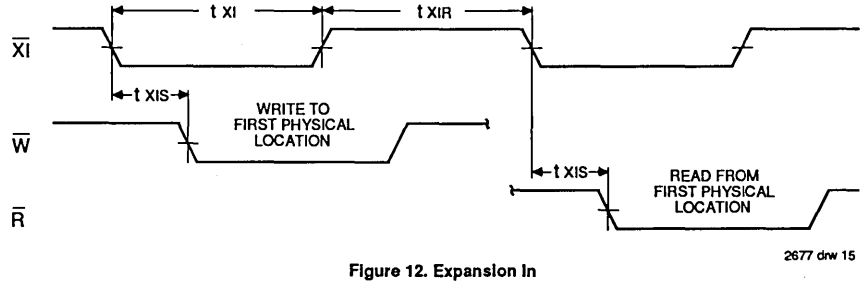


Figure 12. Expansion In

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION

The IDT72021/031/041 is in the Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 13).

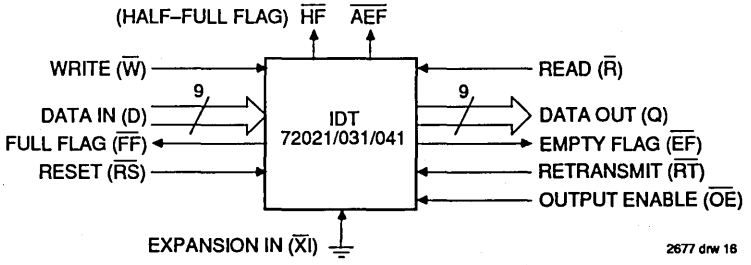


Figure 13. Block Diagram of Single 1K/2K/4K x 9 FIFO

WIDTH EXPANSION CONFIGURATION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$, $\overline{HF}$, and $\overline{AEF}$) can be detected from any one device. Figure 14 demonstrates an 18-bit word width by using two IDT72021/031/041 devices. Any word width can be attained by adding additional IDT72021/031/041s.

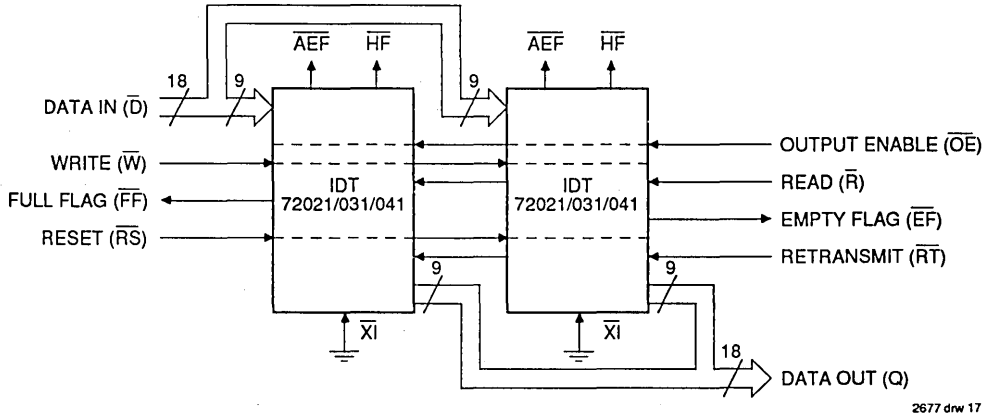


Figure 14. Block Diagram of 1K/2K/4K x 18 FIFO Memory Used in Width Expansion Configuration

NOTE:
1. Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$, $\overline{HF}$ and $\overline{AEF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output signals together.

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT72021/031/041 can easily be adapted to applications when the requirements are for greater than 1K/2K/4K words. Figure 15 demonstrates Depth Expansion using three IDT72021/031/041s. Any depth can be attained by adding additional devices. The IDT72021/031/041 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 15.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 15.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

For additional information refer to Tech Note 9: "Cascading FIFOs or FIFO Modules".

COMPOUND EXPANSION MODE

The two expansion techinques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see Figure 16).

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT72021/031/041s as shown in Figure 17. Care must be taken to assure that the appropriate flag is monitored by each system (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted: a read flow-through and write flow-through mode. For the read flow-through mode (Figure 18), the FIFO permits the reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge. It remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary deassertion and then would be asserted. In the interval of time that $\overline{R}$ was low, more words can be written to the FIFO (the subsequent writes after the first write edge will be deassert the Empty Flag); however, the same word (written on the first write edge), presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ was low. On toggling $\overline{R}$, the other words that are written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be deasserted but the $\overline{W}$ line, being low causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

For additional information refer to Tech Note 8: "Operating FIFOs on Full and Empty Boundary Conditions" and Tech Note 6: "Designing with FIFOs".

TRUTH TABLES

TABLE I—RESET AND RETRANSMIT

Single Device Configuration/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs			
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$	$\overline{AEF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1	0
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X	X

NOTE: 2677 tbl 13
1. Pointer will increment if flag is High.

TABLE II—RESET AND FIRST LOAD TRUTH TABLE

Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTE: 2677 tbl 14
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 15. $\overline{RS}$ = Reset Input $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Flag Full Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output, $\overline{AEF}$ = Almost Empty/Almost Full Flag.

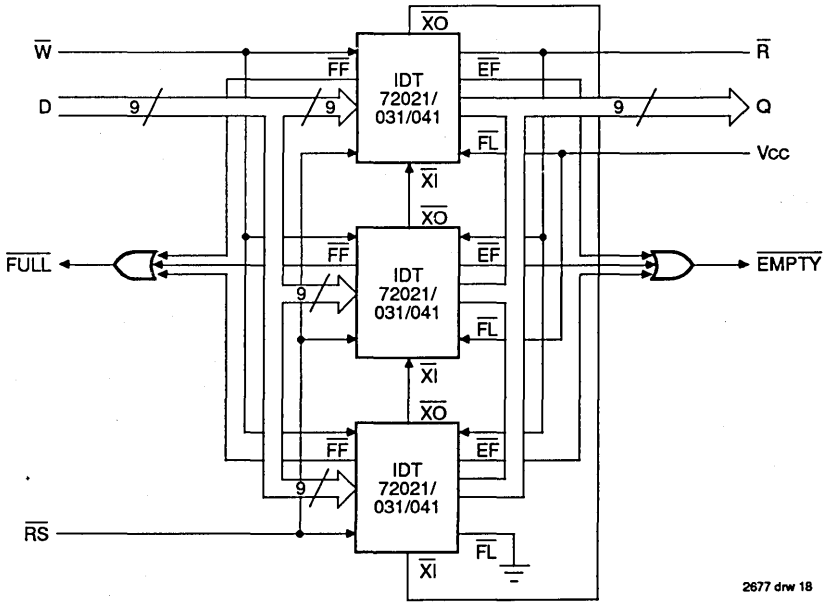


Figure 15. Block Diagram of 3K/6K/12K x 9 FIFO Memory (Depth Expansion)

NOTE:
1. IDT only guarantees depth expansion with identical IDT part numbers and speed.

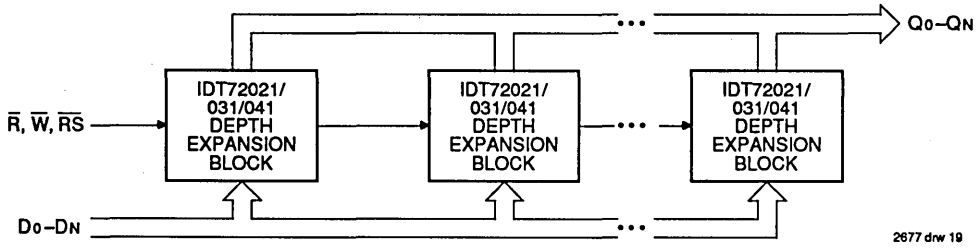


Figure 16. Compound FIFO Expansion

NOTES:
1. For depth expansion block see section od Depth Expansion and Figure 15.
2. For Flag detection see section on Width Expansion and Figure 14.

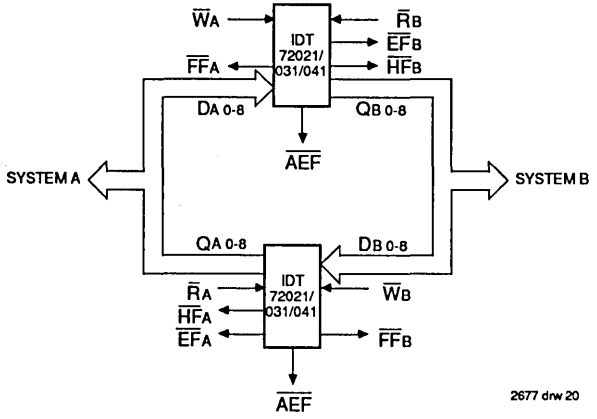


Figure 17. Bidirectional FIFO Mode

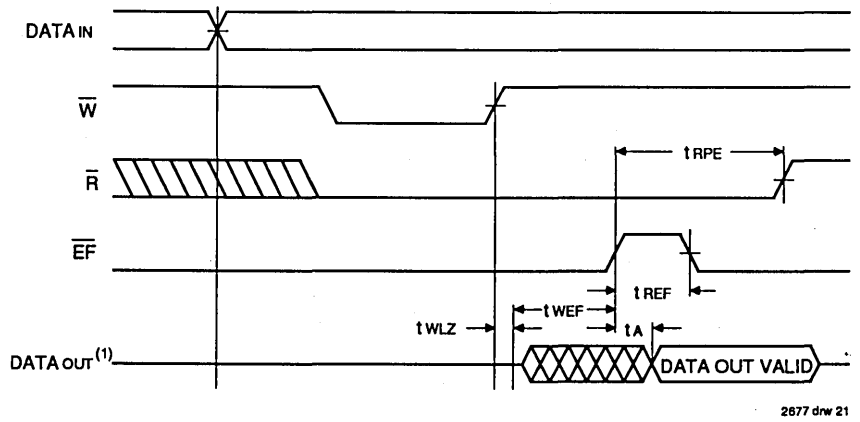


Figure 18. Read Data Flow-Through Mode

NOTE:
1. Assume $\overline{OE}$ is asserted low.

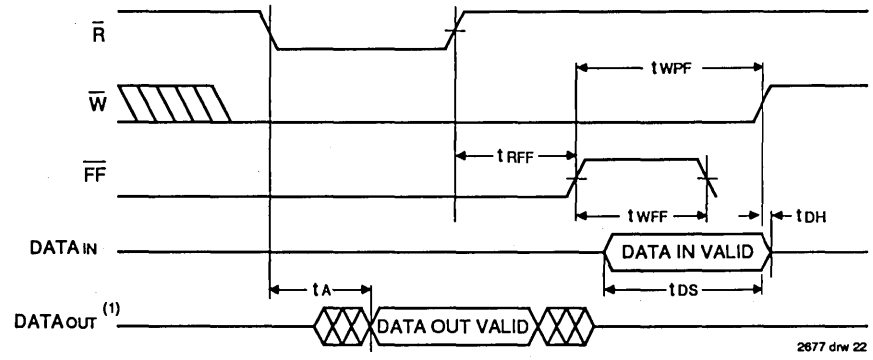
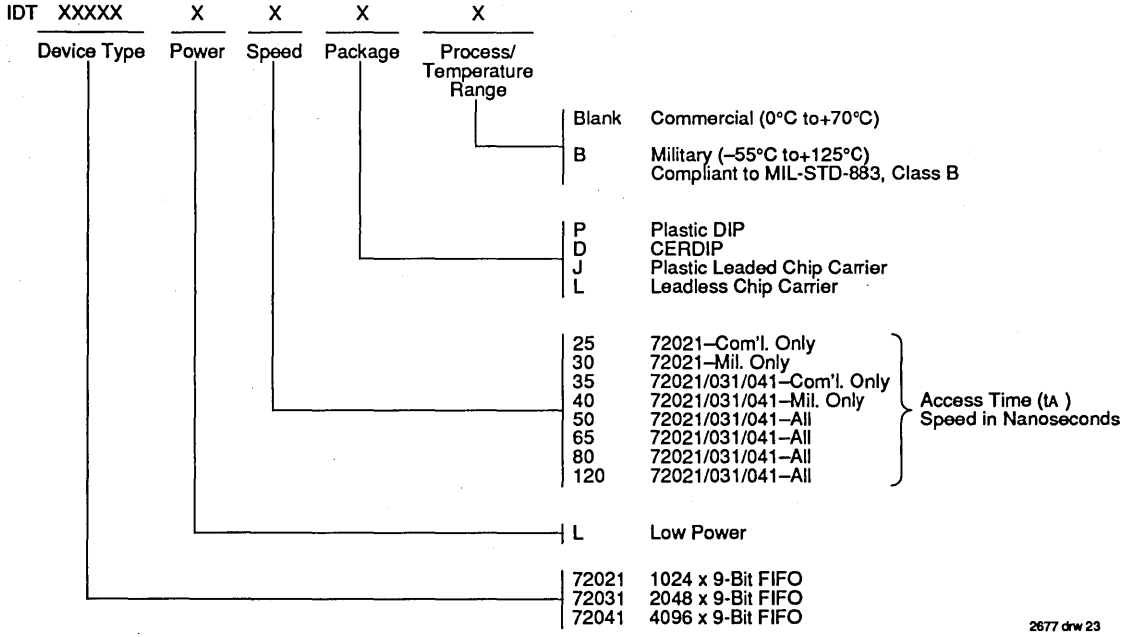


Figure 19. Write Data Flow-Through Mode

NOTE:
1. Assume $\overline{OE}$ is asserted low.

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS PARALLEL-SERIAL FIFO 2048 x 9-BIT & 4096 x 9-BIT

IDT72103
IDT72104

FEATURES:

- 35ns parallel port access time, 45ns cycle time
- 50MHz serial input/output frequency
- Serial-to-parallel, parallel-to-serial, serial-to-serial, and parallel-to-parallel operations
- Expandable in both depth and width with no external components
- Flexishift™ — Sets programmable serial word width from 4 bits to any width with no external components
- Multiple flags: Full, Almost-Full (Full-1/8),Full-Minus-One, Empty, Almost-Empty (Empty + 1/8), Empty-Plus One, and Half-Full
- Asynchronous and simultaneous read or write operations
- Dual-port, zero fall-through time architecture
- Retransmit capability in single-device mode
- Packaged in 40-pin ceramic and plastic DIP, 44-pin LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

APPLICATIONS:

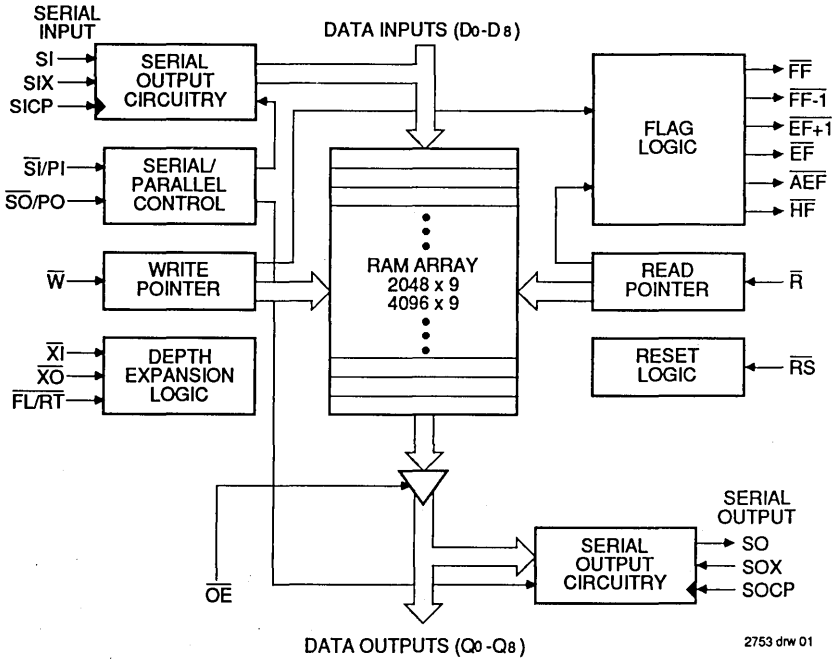
- High-speed data acquisition systems
- Local area network (LAN) buffer
- High-speed modem data buffer
- Remote telemetry data buffer
- FAX raster video data buffer
- Laser printer engine data buffer
- High-speed parallel bus-to-bus communications
- Magnetic media controllers
- Serial link buffer

DESCRIPTION:

The IDT72103/72104 are high-speed Parallel-Serial FIFOs to be used with high-performance systems for functions such as serial communications, laser printer engine control and local area networks.

A serial input, a serial output and two 9-bit parallel ports make four modes of data transfer possible: serial-to-parallel, parallel-to-serial, serial-to-serial, and parallel-to-parallel. The IDT72103/ 72104 are expandable in both depth and width for all of these operational configurations.

FUNCTIONAL BLOCK DIAGRAM



CEMOS and Flexishift are trademarks of Integrated Device Technology, Inc.

DESCRIPTION (CONTINUED)

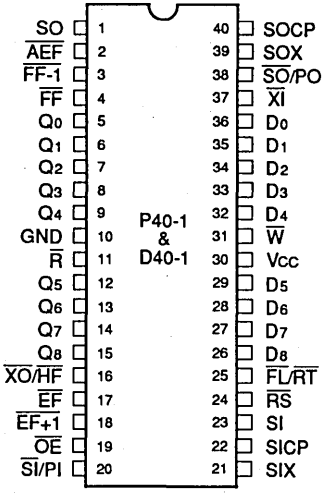
The IDT72103/72104 may be configured to handle serial word widths of four or greater using IDT's unique Flexishift feature. Flexishift allows serial width and depth expansion without external components. For example, you may configure a 4K x 24 FIFO using three IDT72104s in a serial width expansion configuration.

Seven flags are provided to signal memory status of the FIFO. The flags are $\overline{FF}$ (Full), $\overline{AF}$ (7/8 full), $\overline{FF-1}$ (Full-minus-one), $\overline{EF}$ (Empty), $\overline{AE}$ (1/8 full), $\overline{EF+1}$ (Empty-plus-one), and $\overline{HF}$ (Half-full).

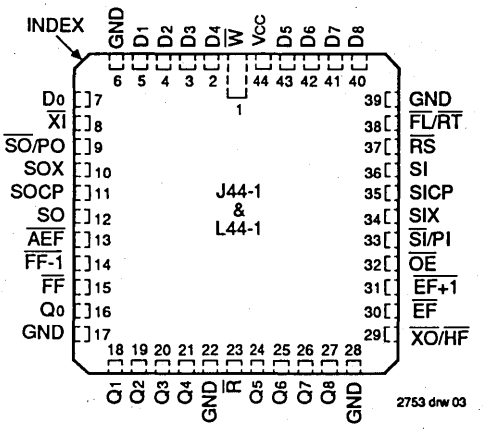
Read ($\overline{R}$) and Write ($\overline{W}$) control pins are provided for asynchronous and simultaneous operations. An output enable ($\overline{OE}$) control pin is available on the parallel output port for high impedance control. The depth expansion control pins $\overline{XO}$ and $\overline{XI}$ are provided to allow cascading for deeper FIFOs.

The IDT72103/72104 are manufactured using IDT's CEMOS™ technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

PIN CONFIGURATIONS



DIP
TOP VIEW



LCC/PLCC
TOP VIEW

6

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +155	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2753 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	10	pF
COUT	Output Capacitance	VOUT = 0V	12	pF

NOTE: 2753 tbl 04
1. This parameter is sampled and not 100% tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage Commercial	2.0	—	—	V
VIH	Input High Voltage Military	2.2	—	—	V
VIL(1)	Input Low Voltage	—	—	0.8	V

NOTE: 2753 tbl 05
1. 1.5V undershoots are allowed for 10ns once per cycle.

PIN DESCRIPTION

Symbol	Name	I/O	Description
D0-D8	Data Inputs Serial Input Word Width Select	I/O	In a parallel input configuration - data inputs for 9-bit wide data. In a serial input configuration - one of the nine output pins is used to select the serial input word width.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{EF}$, $\overline{EF+1}$, $\overline{AEF}$ are all LOW after a reset, while $\overline{FF}$, $\overline{FF-1}$, $\overline{HF}$ are HIGH after a reset.
$\overline{W}$	Write	I	A parallel word write cycle is initiated on the falling edge of $\overline{W}$ if the $\overline{FF}$ is high. When the FIFO is full, FF will go low inhibiting further write operations to prevent data overflow. In a serial input configuration, data bits are clocked into the input shift register and the write pointer does not advance until a full parallel word is assembled. One of the pins, Di, is connected to $\overline{W}$ and advances the write pointer every i-th serial input clock.
$\overline{R}$	Read	I	A read cycle is initiated on the falling edge of $\overline{R}$ if the $\overline{EF}$ is high. After all the data from the FIFO has been read $\overline{EF}$ will go low Inhibiting further read operations. In a serial output configuration, a data word is read from memory into the output shift register. One of the pins, Qj, is connected to $\overline{R}$ and advances the read pointer every j-th serial output clock.
$\overline{FL/RT}$	First Load/ Retransmit	I	This is a dual-purpose pin. In multiple-device mode, $\overline{FL/RT}$ is grounded to indicate the first device loaded. In single-device mode, $\overline{FL/RT}$ acts as the retransmit input. Single-device mode is initiated by grounding the $\overline{XI}$ pin.
$\overline{XI}$	Expansion In	I	In single-device mode, $\overline{XI}$ is grounded. In depth expansion or daisy chain mode, $\overline{XI}$ is connected to the $\overline{XO}$ pin of the previous device.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, both parallel and serial outputs are enabled. When $\overline{OE}$ is HIGH, the parallel output buffers are placed in a high-impedance state.
Q0-Q8	Data Outputs / Serial Output Word Width Select	O	In a parallel output configuration - data outputs for 9-bit wide data. In a serial output configuration - one of nine output pins used to select the serial output word width.
$\overline{FF}$	Full Flag	O	$\overline{FF}$ is asserted LOW when the FIFO is full and further write operations are inhibited. When the $\overline{FF}$ is HIGH, the FIFO is not full and data can be written into the FIFO.
$\overline{FF-1}$	Full-1 Flag	O	$\overline{FF-1}$ goes LOW when the FIFO memory array is one word away from being full. It will remain LOW when every memory location is filled.

2753 tbl 01

PIN DESCRIPTION

Symbol	Name	I/O	Description
$\overline{XO}/\overline{HF}$	Expansion Out/ Half-Full Flag	O	$\overline{HF}$ is LOW when the FIFO is more than half-full in the single device or width expansion modes. The $\overline{HF}$ will remain LOW until the difference between the write and read pointers is less than or equal to one-half of the FIFO memory. In depth expansion mode, a pulse is written from $\overline{XO}$ to $\overline{XI}$ of the next device when the last location in the FIFO is filled. Another pulse is sent from $\overline{XO}$ to $\overline{XI}$ of the next device when the last FIFO location is read.
$\overline{AEF}$	Almost-Empty/ Almost-Full Flag	O	When $\overline{AEF}$ is LOW, the FIFO is empty to 1/8 full or 7/8 full to completely full. If $\overline{AEF}$ is HIGH, then the FIFO is greater than 1/8 full, but less than 7/8 full.
$\overline{EF+1}$	Empty+1 Flag	O	$\overline{EF+1}$ is LOW when there is zero or one word word in the FIFO memory array.
$\overline{EF}$	Empty Flag	O	$\overline{EF}$ goes LOW when the FIFO is empty and further read operations are inhibited. $\overline{FF}$ is HIGH when the FIFO is not empty and data reads are permitted.
SI	Serial Input	I	Data input for serial data.
SO	Serial Output	O	Data output for serial data.
SICP	Serial Input Clock	I	This pin is the serial input clock. On the rising edge of the SICP signal, new serial data bits are read into the serial input shift register.
SOCP	Serial Output Clock	I	This pin is the serial output clock. On the rising edge of the SOCP signal, new serial data bits are read from the serial output shift register.
SIX	Serial Input Expansion	I	SIX controls the serial input expansion for word widths greater than 9 bits. In a serial input configuration, the SIX pin of the least significant device is tied HIGH. The SIX pin of all other devices is connected to the D_8 pin of the previous device. In parallel input configurations or serial input configurations of 9 bits or less, SIX is tied HIGH.
SOX	Serial Output Expansion	I	SOX controls the serial output expansion for word widths greater than 9 bits. In a serial output configuration, the SOX pin of the least significant device is tied HIGH. The SOX pin of all other devices is connected to the Q_8 pin of the previous device. In parallel output configurations or serial output configurations of 9 bits or less, SOX is tied HIGH.
$\overline{SI}$/PI	Serial/Parallel Input	I	When this pin is HIGH, the FIFO is in a parallel input configuration and accepts input data through D_0-D_8. When $\overline{SI}$/PI is LOW, the FIFO is in a serial input configuration and data is input through SI.
$\overline{SO}$/PO	Serial/Parallel Output	I	When this pin is HIGH, the FIFO is in a parallel output configuration and sends output data through Q_0-Q_8. When $\overline{SO}$/PO is LOW the FIFO is in a serial output configuration and data is input through SO.
GND	Ground		One ground pin for the DIP package and five ground pins for the LCC/PLCC packages.
Vcc	Power		One + 5V power pin.

2753 tbl 02

6

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	IDT72103/72104 Commercial t_A = 35, 50, 65, 80, 120 ns			IDT72103/72104 Military t_A = 40, 50, 65, 80, 120 ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{IL}[1]	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	µA
I_{OL}[2]	Output Leakage Current	-10	—	10	-10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OUT} = -2mA[4]	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OUT} = 8mA[5]	—	—	0.4	—	—	0.4	V
I_{CC1}[3]	Average Vcc Power Supply Current	—	90	140	—	100	160	mA
I_{CC2}[3]	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH}) (SOCP = SICP = V_{IL})	—	8	12	—	12	25	mA
$I_{CC3(L)}$[3,6]	Power Down Current	—	—	2	—	—	4	mA
$I_{CC3(S)}$[3,6]	Power Down Current	—	—	8	—	—	12	mA

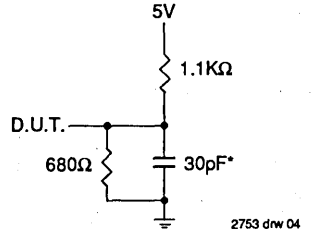
2753 tbl 06

NOTES:
1. Measurements with 0.4 ≤ V_{IN} ≤ Vcc.
2. $\overline{R}$ ≥ V_{IH}, SOCP ≤ V_{IL}, 0.4 ≤ V_{OUT} ≤ Vcc.
3. Icc measurements are made with outputs open.
4. For SO, I_{OUT} = -8mA.
5. For SO, I_{OUT} =16mA.
6. SOCP = SICP ≤ 0.2V; other Inputs = Vcc -0.2V.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2753 tbl 07



or equivalent circuit

Figure 1. Ouput Load

*Includins jig and scope capacitances

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)

		Commercial		Military		Mil. and Com'l.			
		IDT72103x35 IDT72104x35		IDT72103x40 IDT72104x40		IDT72103x50 IDT72104x50			Timing
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Figure
f_S	Parallel Shift Frequency	—	22.2	—	20	—	15	MHz	—
f_{SOCP}	Serial-Out Shift Frequency	—	50	—	50	—	40	MHz	—
f_{SICP}	Serial-In Shift Frequency	—	50	—	50	—	40	MHz	—
PARALLEL-OUTPUT MODE TIMINGS									
t_A	Access Time	—	35	—	40	—	50	ns	4
t_{RR}	Read Recovery Time	10	—	10	—	15	—	ns	4
t_{RPW}	Read Pulse Width	35	—	40	—	50	—	ns	4
t_{RC}	Read Cycle Time	45	—	50	—	65	—	ns	4
t_{WLZ}	Write Pulse Low to Data Bus at Low $Z^{(1)}$	5	—	5	—	15	—	ns	15
t_{RLZ}	Read Pulse Low to Data Bus at Low $Z^{(1)}$	5	—	5	—	10	—	ns	4
t_{RHZ}	Read Pulse High to Data Bus at High $Z^{(1)}$	—	20	—	25	—	30	ns	4
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	ns	4
PARALLEL-INPUT MODE TIMINGS									
t_{DS}	Data Set-up Time	18	—	20	—	30	—	ns	3
t_{DH}	Data Hold Time	0	—	0	—	5	—	ns	3
t_{WC}	Write Cycle Time	45	—	50	—	65	—	ns	3
t_{WPW}	Write Pulse Width	35	—	40	—	50	—	ns	3
t_{WR}	Write Recovery Time	10	—	10	—	15	—	ns	3
RESET TIMINGS									
t_{RSC}	Reset Cycle Time	45	—	50	—	65	—	ns	2,18
t_{RS}	Reset Pulse Width	35	—	40	—	50	—	ns	2,18
t_{RSS}	Reset Set-up Time	35	—	40	—	50	—	ns	2,18
t_{RSR}	Reset Recovery Time	10	—	10	—	15	—	ns	2,17,18
RESET TO FLAG TIMINGS									
t_{RSF1}	Reset to $\overline{EF}$, $\overline{AEF}$, and $\overline{EF+1}$ Low	—	45	—	50	—	65	ns	2
t_{RSF2}	Reset to $\overline{HF}$, $\overline{FF}$, and $\overline{FF-1}$ Low	—	45	—	50	—	65	ns	2
RESET TO OUTPUT TIMINGS – SERIAL MODE ONLY									
t_{RSOL}	Reset Going Low to Q_{0-8} Low	20	—	20	—	35	—	ns	18
t_{RSOH}	Reset Going High to Q_{0-8} High	20	—	20	—	35	—	ns	18
t_{RSDL}	Reset Going Low to D_{0-8} Low	20	—	20	—	35	—	ns	17
RETRANSMIT TIMINGS									
t_{RTC}	Retransmit Cycle Time	45	—	50	—	65	—	ns	5
t_{RT}	Retransmit Pulse Width	35	—	40	—	50	—	ns	5
t_{RTS}	Retransmit Set-up Time	35	—	40	—	50	—	ns	5
t_{RTR}	Retransmit Recovery Time	10	—	10	—	15	—	ns	5
PARALLEL MODE FLAG TIMINGS									
t_{REF}	Read Low to $\overline{EF}$ Low	—	30	—	35	—	45	ns	6
t_{RFF}	Read High to $\overline{FF}$ High	—	30	—	35	—	45	ns	7
t_{RF}	Read High to Transitioning $\overline{HF}$, $\overline{AEF}$ and $\overline{FF-1}$	—	45	—	50	—	65	ns	8,9,10
t_{RE}	Read Low to Transitioning $\overline{AEF}$ and $\overline{EF+1}$	—	45	—	45	—	65	ns	11
t_{RPE}	Read Pulse Width after $\overline{EF}$ High	35	—	40	—	50	—	ns	15
t_{WEF}	Write High to $\overline{EF}$ High	—	30	—	35	—	45	ns	6
t_{WFF}	Write Low to $\overline{FF}$ Low	—	30	—	35	—	45	ns	7
t_{WF}	Write Low to Transitioning $\overline{HF}$, $\overline{AEF}$ and $\overline{FF-1}$	—	45	—	50	—	65	ns	8,9,10
t_{WE}	Write High to Transitioning $\overline{AEF}$ and $\overline{EF+1}$	—	45	—	50	—	65	ns	11
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	35	—	40	—	50	—	ns	16

2753 tbl 08

NOTE:
1. Values guaranteed by design, not tested.

AC ELECTRICAL CHARACTERISTICS (Continued)

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	Commercial and Military						Unit	Timing Figure
		IDT72103x65 IDT72104x65		IDT72103x80 IDT72104x80		IDT72103x120 IDT72104x120			
		Min.	Max.	Min.	Max.	Min.	Max.		
f_S	Parallel Shift Frequency	—	12.5	—	10	—	7	MHz	—
f_{SOCP}	Serial-Out Shift Frequency	—	33	—	28	—	25	MHz	—
f_{SICP}	Serial-In Shift Frequency	—	33	—	28	—	25	MHz	—
PARALLEL-OUTPUT MODE TIMINGS									
t_A	Access Time	—	65	—	80	—	120	ns	4
t_{RR}	Read Recovery Time	15	—	20	—	20	—	ns	4
t_{RPW}	Read Pulse Width	65	—	80	—	120	—	ns	4
t_{RC}	Read Cycle Time	80	—	100	—	140	—	ns	4
t_{WLZ}	Write Pulse Low to Data Bus at Low $Z^{(1)}$	15	—	20	—	20	—	ns	15
t_{RLZ}	Read Pulse Low to Data Bus at Low $Z^{(1)}$	10	—	10	—	10	—	ns	4
t_{RHZ}	Read Pulse High to Data Bus at High $Z^{(1)}$	—	30	—	35	—	35	ns	4
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	ns	4
PARALLEL-INPUT MODE TIMINGS									
t_{DS}	Data Set-up Time	30	—	40	—	40	—	ns	3
t_{DH}	Data Hold Time	10	—	10	—	10	—	ns	3
t_{WC}	Write Cycle Time	80	—	100	—	140	—	ns	3
t_{WPW}	Write Pulse Width	65	—	80	—	120	—	ns	3
t_{WR}	Write Recovery Time	15	—	20	—	20	—	ns	3
RESET TIMINGS									
t_{RSC}	Reset Cycle Time	80	—	100	—	140	—	ns	2,18
t_{RS}	Reset Pulse Width	65	—	80	—	120	—	ns	2,18
t_{RSS}	Reset Set-up Time	65	—	80	—	120	—	ns	2,18
t_{RSR}	Reset Recovery Time	15	—	20	—	20	—	ns	2,17,18
RESET TO FLAG TIMINGS									
t_{RSF1}	Reset to $\overline{EF}$, $\overline{AEF}$, and $\overline{EF+1}$ Low	—	80	—	100	—	140	ns	2
t_{RSF2}	Reset to $\overline{HF}$, $\overline{FF}$, and $\overline{FF-1}$ Low	—	80	—	100	—	140	ns	2
RESET TO OUTPUT TIMINGS – SERIAL MODE ONLY									
t_{RSQL}	Reset Going Low to Q_{0-8} Low	50	—	65	—	105	—	ns	18
t_{RSQH}	Reset Going High to Q_{0-8} High	50	—	65	—	105	—	ns	18
t_{RSDL}	Reset Going Low to D_{0-8} Low	50	—	65	—	105	—	ns	17
RETRANSMIT TIMINGS									
t_{RTC}	Retransmit Cycle Time	80	—	100	—	140	—	ns	5
t_{RT}	Retransmit Pulse Width	65	—	80	—	120	—	ns	5
t_{RTS}	Retransmit Set-up Time	65	—	80	—	120	—	ns	5
t_{RTR}	Retransmit Recovery Time	15	—	20	—	20	—	ns	5
PARALLEL MODE FLAG TIMINGS									
t_{REF}	Read Low to $\overline{EF}$ Low	—	60	—	60	—	60	ns	6
t_{RFF}	Read High to $\overline{FF}$ High	—	60	—	60	—	60	ns	7
t_{RF}	Read High to Transitioning $\overline{HF}$, $\overline{AEF}$ and $\overline{FF-1}$	—	80	—	100	—	140	ns	8,9,10
t_{RE}	Read Low to Transitioning $\overline{AEF}$ and $\overline{EF+1}$	—	80	—	100	—	140	ns	11
t_{RPE}	Read Pulse Width after $\overline{EF}$ High	65	—	80	—	120	—	ns	15
t_{WEF}	Write High to $\overline{EF}$ High	—	60	—	60	—	60	ns	6
t_{WFF}	Write Low to $\overline{FF}$ Low	—	60	—	60	—	60	ns	7
t_{WF}	Write Low to Transitioning $\overline{HF}$, $\overline{AEF}$ and $\overline{FF-1}$	—	80	—	100	—	140	ns	8,9,10
t_{WE}	Write High to Transitioning $\overline{AEF}$ and $\overline{EF+1}$	—	80	—	100	—	140	ns	11
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	65	—	80	—	120	—	ns	16

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NOTE:
1. Values guaranteed by design, not tested.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	Commercial IDT72103x35 IDT72104x35 Min.	Commercial IDT72103x35 IDT72104x35 Max.	Military IDT72103x40 IDT72104x40 Min.	Military IDT72103x40 IDT72104x40 Max.	Mil. and Com'l. IDT72103x50 IDT72104x50 Min.	Mil. and Com'l. IDT72103x50 IDT72104x50 Max.	Unit	Timing Figure
DEPTH EXPANSION MODE TIMINGS									
t_{XOL}	Read/Write to $\overline{XO}$ Low	—	35	—	40	—	50	ns	13
t_{XOH}	Read/Write to $\overline{XO}$ High	—	35	—	40	—	50	ns	13
t_{XI}	$\overline{XI}$ Pulse Width	35	—	40	—	50	—	ns	14
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	ns	14
t_{XIS}	$\overline{XI}$ Set-up Time	15	—	15	—	15	—	ns	14
SERIAL-INPUT MODE TIMINGS									
t_{S2}	Serial Data In Set-up Time to SICP Rising Edge	12	—	12	—	15	—	ns	19
t_{H2}	Serial Data In Hold Time to SICP Rising Edge	0	—	0	—	0	—	ns	19
t_{S3}	SIX Set-up Time to SICP Rising Edge	5	—	5	—	5	—	ns	19
t_{S4}	$\overline{W}$ Set-up Time to SICP Rising Edge	5	—	5	—	5	—	ns	19
t_{H4}	$\overline{W}$ Hold Time to SICP Rising Edge	7	—	7	—	7	—	ns	19
t_{SICW}	Serial In Clock Width High/Low	8	—	8	—	10	—	ns	19
t_{S5}	SI/PI Set-up Time to SICP Rising Edge	35	—	40	—	50	—	ns	19
SERIAL-OUTPUT MODE TIMINGS									
t_{S6}	SO/PO Set-up Time to SOCP Rising Edge	35	—	40	—	50	—	ns	20
t_{S7}	SOX Set-up Time to SOCP Rising Edge	5	—	5	—	5	—	ns	20
t_{S8}	$\overline{R}$ Set-up Time to SOCP Rising Edge	5	—	5	—	5	—	ns	20
t_{H8}	$\overline{R}$ Hold Time to SOCP Rising Edge	7	—	7	—	7	—	ns	20
t_{SOCW}	Serial Out Clock Width High/Low	8	—	8	—	10	—	ns	20
SERIAL MODE RECOVERY TIMINGS									
t_{REFSO}	Recovery Time SOCP after $\overline{EF}$ Goes High	35	—	40	—	80	—	ns	22
t_{RFFSI}	Recovery Time SICP after $\overline{FF}$ Goes High	15	—	15	—	15	—	ns	23
SERIAL MODE FLAG TIMINGS									
t_{SOCEF}	SOCP Rising Edge (Bit 0- Last Word) to $\overline{EF}$ Low	—	20	—	25	—	25	ns	22
t_{SOCFF}	SOCP Rising Edge (Bit 0- First Word) to $\overline{FF}$ High	—	30	—	35	—	40	ns	24
t_{SOCF}	SOCP Rising Edge to $\overline{FF}$-1, $\overline{HF}$, $\overline{AEF}$ High	—	30	—	35	—	40	ns	24,26
t_{SOCF}	SOCP Rising Edge to $\overline{AEF}$, $\overline{EF}$, $\overline{EF}$+1 Low	—	30	—	35	—	40	ns	22,26
t_{SICEF}	SICP Rising Edge (Last Bit-First Word) to $\overline{EF}$ High	—	45	—	50	—	65	ns	21
t_{SICFF}	SICP Rising Edge (Bit 1-Last Word) to $\overline{FF}$ Low	—	30	—	35	—	40	ns	23
t_{SICF}	SICP Rising Edge to $\overline{EF}$+1, $\overline{AEF}$ High	—	45	—	50	—	65	ns	21,25
t_{SICF}	SICP Rising Edge to $\overline{FF}$-1, $\overline{HF}$, $\overline{AEF}$ High	—	45	—	50	—	65	ns	23,25
SERIAL-INPUT MODE TIMINGS									
t_{PD1}	SICP Rising Edge to D[1]	5	17	5	17	5	20	ns	17,19
SERIAL-OUTPUT MODE TIMINGS									
t_{PD2}	SOCP Rising Edge to Q[1]	5	17	5	17	5	20	ns	20
t_{SOHZ}	SOCP Rising Edge to SO at High-Z[1]	5	16	5	16	5	16	ns	20
t_{SOLZ}	SOCP Rising Edge to SO at Low-Z[1]	5	22	5	22	5	22	ns	20
t_{SOPD}	SOCP Rising Edge to Valid Data on SO	—	18	—	18	—	18	ns	20
OUTPUT ENABLE/DISABLE TIMINGS									
t_{OEHZ}	Output Enable to High-Z (Disable)[1]	—	16	—	16	—	16	ns	12
t_{OELZ}	Output Enable to Low-Z (Enable)[1]	5	—	5	—	5	—	ns	12
t_{AOE}	Output Enable to Data Valid (Q_{0-8})	—	20	—	20	—	22	ns	12

NOTE:
1. Values guaranteed by design, not tested.

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AC ELECTRICAL CHARACTERISTICS (Continued)

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	Commercial and Military						Unit	Timing Figure
		IDT72103x65 IDT72104x65		IDT72103x80 IDT72104x80		IDT72103x120 IDT72104x120			
		Min.	Max.	Min.	Max.	Min.	Max.		
DEPTH EXPANSION MODE TIMINGS									
t_{XOL}	Read/Write to $\overline{XO}$ Low	—	65	—	80	—	120	ns	13
t_{XOH}	Read/Write to $\overline{XO}$ High	—	65	—	80	—	120	ns	13
t_{XI}	$\overline{XI}$ Pulse Width	65	—	80	—	120	—	ns	14
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	ns	14
t_{XIS}	$\overline{XI}$ Set-up Time	15	—	15	—	15	—	ns	14
SERIAL-INPUT MODE TIMINGS									
t_{S2}	Serial Data In Set-up Time to SICP Rising Edge	15	—	20	—	20	—	ns	19
t_{H2}	Serial Data In Hold Time to SICP Rising Edge	0	—	5	—	5	—	ns	19
t_{S3}	SIX Set-up Time to SICP Rising Edge	5	—	5	—	5	—	ns	19
t_{S4}	$\overline{W}$ Set-up Time to SICP Rising Edge	5	—	5	—	5	—	ns	19
t_{H4}	$\overline{W}$ Hold Time to SICP Rising Edge	10	—	12	—	15	—	ns	19
t_{SICW}	Serial In Clock Width High/Low	10	—	15	—	15	—	ns	19
t_{S5}	SI/PI Set-up Time to SICP Rising Edge	65	—	80	—	120	—	ns	19
SERIAL-OUTPUT MODE TIMINGS									
t_{S6}	SO/PO Set-up Time to SOCP Rising Edge	65	—	80	—	120	—	ns	20
t_{S7}	SOX Set-up Time to SOCP Rising Edge	5	—	5	—	5	—	ns	20
t_{S8}	$\overline{R}$ Set-up Time to SOCP Rising Edge	5	—	5	—	5	—	ns	20
t_{H8}	$\overline{R}$ Hold Time to SOCP Rising Edge	10	—	12	—	15	—	ns	20
t_{SOCW}	Serial Out Clock Width High/Low	10	—	15	—	15	—	ns	20
SERIAL MODE RECOVERY TIMINGS									
t_{REFSO}	Recovery Time SOCP after $\overline{EF}$ Goes High	65	—	80	—	120	—	ns	22
t_{RFFSI}	Recovery Time SICP after $\overline{FF}$ Goes High	15	—	20	—	20	—	ns	23
SERIAL MODE FLAG TIMINGS									
t_{SOCEF}	SOCP Rising Edge (Bit 0- Last Word) to $\overline{EF}$ Low	—	30	—	30	—	30	ns	22
t_{SOCFF}	SOCP Rising Edge (Bit 0- First Word) to $\overline{FF}$ High	—	50	—	60	—	60	ns	24
t_{SOCF}	SOCP Rising Edge to $\overline{FF-1}$, $\overline{HF}$, $\overline{AEF}$ High	—	50	—	60	—	60	ns	24,26
t_{SOCF}	SOCP Rising Edge to $\overline{AEF}$, $\overline{EF}$, $\overline{EF+1}$ Low	—	50	—	60	—	60	ns	22,26
t_{SICEF}	SICP Rising Edge (Last Bit-First Word) to $\overline{EF}$ High	—	80	—	80	—	80	ns	21
t_{SICFF}	SICP Rising Edge (Bit 1-Last Word) to $\overline{FF}$ Low	—	50	—	60	—	60	ns	23
t_{SICF}	SICP Rising Edge to $\overline{EF+1}$, $\overline{AEF}$ High	—	80	—	80	—	80	ns	21,25
t_{SICF}	SICP Rising Edge to $\overline{FF-1}$, $\overline{HF}$, $\overline{AEF}$ High	—	80	—	80	—	80	ns	23,25
SERIAL-INPUT MODE TIMINGS									
t_{PD1}	SICP Rising Edge to D[1]	5	25	5	30	5	35	ns	17,19
SERIAL-OUTPUT MODE TIMINGS									
t_{PD2}	SOCP Rising Edge to Q[1]	5	25	5	30	5	35	ns	20
t_{SOHZ}	SOCP Rising Edge to SO at High-Z[1]	5	20	5	25	5	30	ns	20
t_{SOLZ}	SOCP Rising Edge to SO at Low-Z[1]	5	22	5	30	5	35	ns	20
t_{SOPD}	SOCP Rising Edge to Valid Data on SO	—	22	5	30	5	35	ns	20
OUTPUT ENABLE/DISABLE TIMINGS									
t_{OEHZ}	Output Enable to High-Z (Disable)[1]	—	20	—	25	—	30	ns	12
t_{OELZ}	Output Enable to Low-Z (Enable)[1]	5	—	5	—	5	—	ns	12
t_{AOE}	Output Enable to Data Valid (Q_{0-8})	—	25	—	30	—	35	ns	12

NOTE:
1. Values guaranteed by design, not tested.

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GENERAL SIGNAL DESCRIPTION

INPUTS:

Data Inputs (D_0-D_8)

The parallel-in mode is selected by connecting the $\overline{SI}$/PI pin to Vcc. D_0-D_8 are the data input lines.

The serial-input mode is selected by grounding the $\overline{SI}$/PI pin. The D_0-D_8 lines are control output pins used to program the serial word width.

Reset ($\overline{RS}$)

Reset is accomplished whenever the $\overline{RS}$ input is taken to a low state. Both internal read and write pointers are set to the first location during reset. A reset is required after power up before a write operation can take place. Both Read ($\overline{R}$) and Write ($\overline{W}$) inputs must be high during reset.

Write ($\overline{W}$)

A write cycle is initiated on the falling edge of $\overline{W}$ provided the Full Flag ($\overline{FF}$) is not asserted. Data set-up and hold times must be met with respect to the rising edge of $\overline{W}$. Data is stored in the RAM array sequentially and independently of any on going read operation.

When the FIFO is full, the $\overline{FF}$ will go low inhibiting further write operations to prevent data overflow. After a valid read operation is completed, the $\overline{FF}$ will go high after t_{RFF} allowing a valid write to begin.

Read ($\overline{R}$)

A read cycle is initiated on the falling edge of $\overline{R}$, provided the $\overline{EF}$ is not set. Data is accessed on a first-in/first out basis independent of any on going write operations. After $\overline{R}$ goes high, the Data Outputs (Q_0-Q_8) go to a high impedance condition until the next read operation. When all the data has been read from the FIFO, the $\overline{EF}$ will go low, and Q_0-Q_8 will go to a high impedance state inhibiting further read operations. After the completion of a valid write operation, the $\overline{EF}$ will go high after t_{WEF} allowing a valid read to begin.

First Load/Retransmit ($\overline{FL}/\overline{RT}$)

In the depth-expansion mode, the $\overline{FL}/\overline{RT}$ pin is grounded to indicate that it is the first device loaded. In the single-device mode, the $\overline{FL}/\overline{RT}$ pin acts as the retransmit input. The single-device mode is initiated by grounding the Expansion-In ($\overline{XI}$) pin.

The IDT72103/72104 can be made to retransmit data when the $\overline{RT}$ input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. During retransmit, $\overline{R}$ and $\overline{W}$ must be set high and the $\overline{FF}$ will be affected depending on the relative locations of the read and write pointers. This feature is useful when less than 2048/4096 writes are performed between resets. The retransmit feature is not available in the depth expansion mode.

Expansion In ($\overline{XI}$)

The $\overline{XI}$ pin is grounded to indicate an operation in the the single-device mode. In the depth expansion or daisy-chain mode, the $\overline{XI}$ pin is connected to the $\overline{XO}$ pin of the previous device.

Output Enable ($\overline{OE}$)

When $\overline{OE}$ is high, the parallel output buffers are tristated. When $\overline{OE}$ is low, both parallel and serial outputs are enabled.

Serial Input (SI)

Serial data is read into the serial input register via the SI pin. In both depth and serial width expansion modes, the serial-input signals of the different FIFOs in the expansion array are connected together.

Serial Input Clock (SICP)

Serial data is read into the serial input register on the rising edge of the SICP signal. In both depth and serial width expansion modes, the SICP signals of the different FIFOs in the expansion array are connected together.

Serial Output Clock (SOCP)

New serial data bits are read from the serial output register on the rising edge of the SOCP signal. In both depth and serial width expansion modes, the SOCP signals of the different FIFOs in the expansion array are connected together.

Serial Input Expansion (SIX)

The SIX pin is tied high for single-device serial or parallel input operation. In a serial input configuration, the SIX pin of the least significant device is tied HIGH. The SIX pin of all other devices is connected to the D_8 pin of the previous device.

Serial Output Expansion (SOX)

The SOX pin is tied high for single-device serial or parallel output operation. In a serial output configuration, the SOX pin of the least significant device is tied HIGH. The SOX pin of all other devices is connected to the Q_8 pin of the previous device.

Serial/Parallel Input ($\overline{SI}$/PI)

The $\overline{SI}$/PI pin programs whether the IDT72103/72104 accepts parallel or serial data as input. When this pin is low, the FIFO expects serial data and the D_0-D_8 pins become output pins used to program the write signal and the serial input word width. For instance, connecting D_8 to $\overline{W}$ will program a serial word width of 7 bits; connecting D_7 to $\overline{W}$ will program a serial word width of 8 bits and so on.

Serial/Parallel Output ($\overline{SO}$/PO)

The $\overline{SO}$/PO pin programs whether the IDT72103/72104 outputs parallel or serial data. When this pin is low, the FIFO expects serial data and the Q_0-Q_8 pins output signals used to program the read signal and the serial output word width.

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OUTPUTS:

Data Outputs (Q_0-Q_8)

Data outputs for 9-bit wide data. These output lines are in a high impedance condition whenever $\overline{R}$ is in a high state. The serial output mode is selected by grounding the $\overline{SO}$/PO pin. The Q_0-Q_8 lines are control pins used to program the serial word width.

Serial Output (SO)

Serial data is output on the SO pin. In both depth and serial width expansion modes the serial output signals of the different FIFOs in the expansion array are connected together. Following reset, SO is tristated until the first rising edge of the Serial Out Clock (SOCP) signal. Data is clocked out least significant bit first. In the serial width expansion mode, SO is tristated again after the ninth bit is output.

Full Flag ($\overline{FF}$)

$\overline{FF}$ is asserted low when the FIFO is full. When the FIFO is full, the internal write pointer will not be incremented by any additional write pulses.

Full Flag - Serial In Mode

When the FIFO is loaded serially, the Serial In Clock (SICP) asserts the $\overline{FF}$. On the second rising edge of the SICP for the last word in the FIFO, the $\overline{FF}$ will assert low, and it will remain asserted until the next read operation. Note that when the FF is asserted, the last SICP for that word will have to be stretched as shown in Figure 23.

Full Flag - Parallel-In Mode

When the FIFO is in the Parallel-In mode, the falling edge of $\overline{W}$ asserts the $\overline{FF}$ (low). The $\overline{FF}$ is then de-asserted (high) by subsequent read operations - either serial or parallel.

Full-Minus-One Flag ($\overline{FF-1}$)

The $\overline{FF-1}$ flag is asserted low when the FIFO is one word away from being full. It will remain asserted when the FIFO is full.

Expansion Out/Half-Full Flag ($\overline{XO}/\overline{HF}$)

In the single-device mode, the $\overline{XO}/\overline{HF}$ pin operates as a $\overline{HF}$ pin when the $\overline{XI}$ pin is grounded. After half of the memory is filled, the $\overline{HF}$ will be set to low at the falling edge of the next write operation. It will remain set until the difference between the write pointer and read pointer is less than or equal to one-half of the FIFO total memory. The $\overline{HF}$ is then reset by the rising edge of the read operation.

In the multiple-device mode, the $\overline{XI}$ pin is connected to the $\overline{XO}$ pin of the previous device. The $\overline{XO}$ pin signals a pulse to the next device when the previous device reaches the best location of memory in the daisy chain configuration.

Almost-Empty or Almost-Full Flag ($\overline{AEF}$)

The $\overline{AEF}$ asserts low if there are 0-255 or 1793-2048 bytes in the IDT72103, 2K x 9 FIFO. The $\overline{AEF}$ asserts low if there are 0-511 or 3585-4096 bytes in the IDT72104, 4K x 9 FIFO.

Empty-Plus-One Flag ($\overline{EF+1}$)

In the parallel-output mode, the $\overline{EF+1}$ flag is asserted low when there is one word or less in the FIFO. It will remain low when the FIFO is empty.

In the serial-output mode, the $\overline{EF+1}$ flag operates as an $\overline{EF+2}$ flag. It goes low when the second to the last word is read from the RAM array and is ready to be shifted out.

Empty Flag ($\overline{EF}$) - Parallel-Out Mode

When the FIFO is in the parallel out mode and there is only one word in the FIFO, the falling edge of the $\overline{R}$ line will cause the $\overline{EF}$ line to be asserted low. This is shown in Figure 6. The $\overline{EF}$ is then de-asserted high by either the rising edge of $\overline{W}$ or the rising edge of SICP, as shown in Figure 6.

Empty Flag - Serial-Out Mode

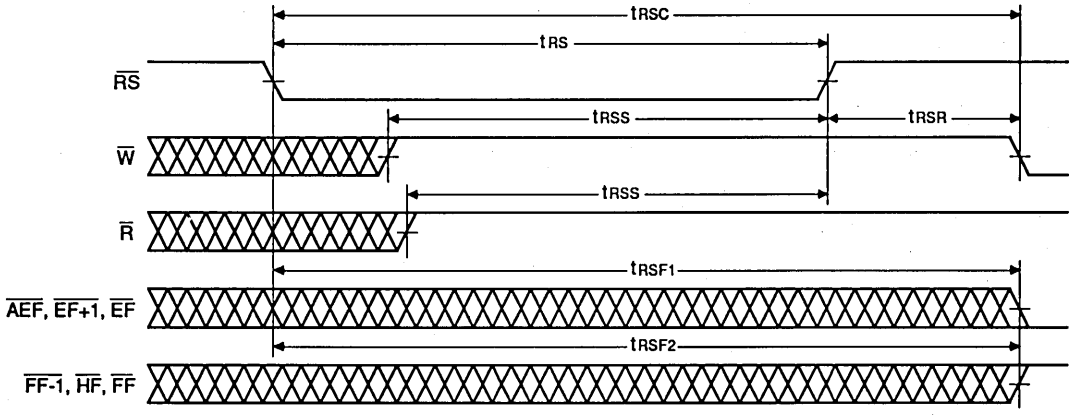
The use of the EF is important for proper serial-out operation when the FIFO is almost empty. The $\overline{EF}$ flag is asserted low after the first bit of the last word is shifted out. This is shown in Figure 22.

TABLE 1 — STATUS FLAGS

Number of Words In FIFO IDT72132	Number of Words In FIFO IDT72142	$\overline{FF}$	$\overline{FF-1}$	$\overline{AEF}$	$\overline{HF}$	(1) $\overline{EF+1}$	$\overline{EF}$
0	0	H	H	L	H	L	L
1	1	H	H	L	H	L	H
2-255	2-511	H	H	L	H	H	H
256-1024	512-2048	H	H	H	H	H	H
1025-1792	2049-3584	H	H	H	L	H	H
1793-2046	3585-4094	H	H	L	L	H	H
2047	4095	H	L	L	L	H	H
2048	4096	L	L	L	L	H	H

NOTE: 2753 tbl 12
1. $\overline{EF+1}$ acts as $\overline{EF+2}$ in the serial out mode.

PARALLEL TIMINGS:



NOTE:
1. All flags may change status during Reset, but flags will be valid at tRSC.

Figure 2. Reset

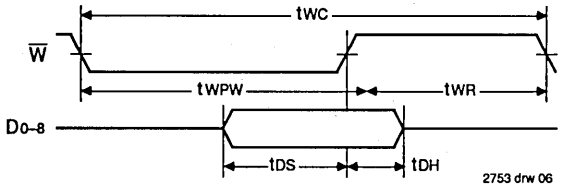


Figure 3. Write Operation in Parallel Data In Mode

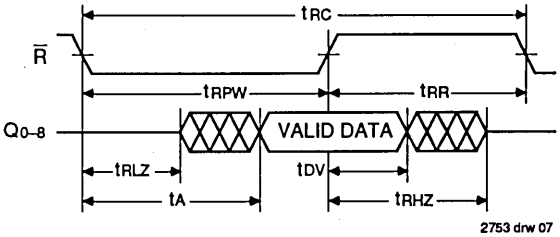
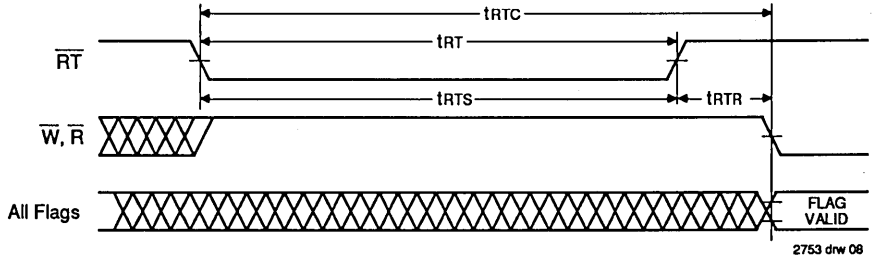
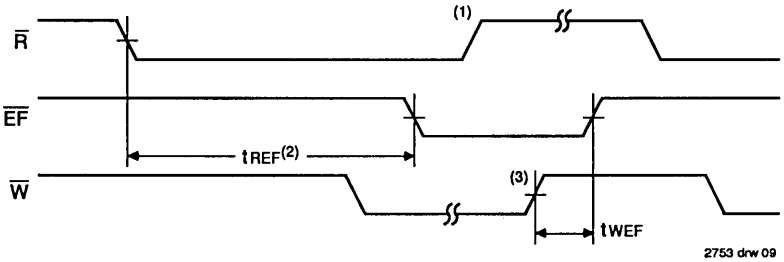


Figure 4. Read Operation in Parallel Data Out Mode



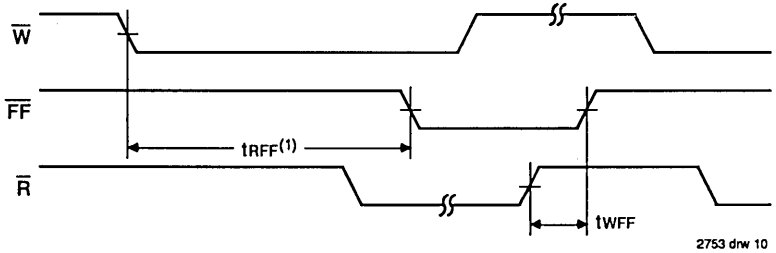
NOTE:
1. All flags may change status during Retransmit, but flags will be valid at tRTC.

Figure 5. Retransmit



NOTES:
1. Data is valid on this edge.
2. The Empty Flag is asserted by R in the Parallel-Out mode and is specified by tREF. The EF flag is deasserted by the rising edge of W.
3. First rising edge of Write after EF is set.

Figure 6. Empty Flag Timings In Parallel Out Mode



NOTE:
1. For the assertion time, tWFF is used when data is written in the Parallel mode. The FF is de-asserted by the rising edge of R.

Figure 7. Full Flag Timings In Parallel-In Mode

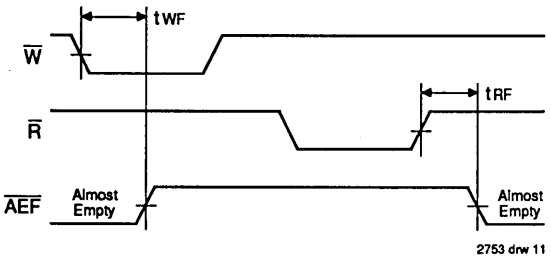


Figure 8. Almost-Empty Flag Region

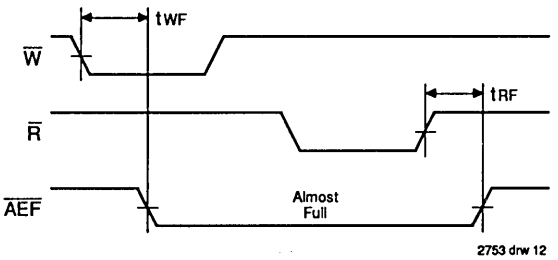


Figure 9. Almost-Full Flag Region

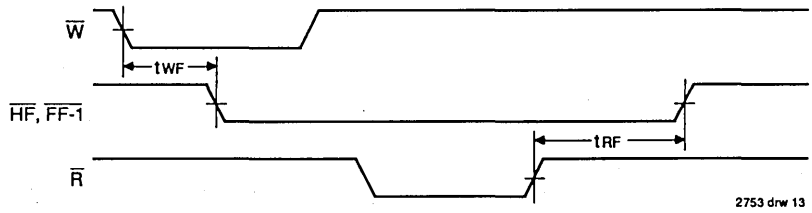


Figure 10. Half-Full and Full-minus-1 Flag Timings

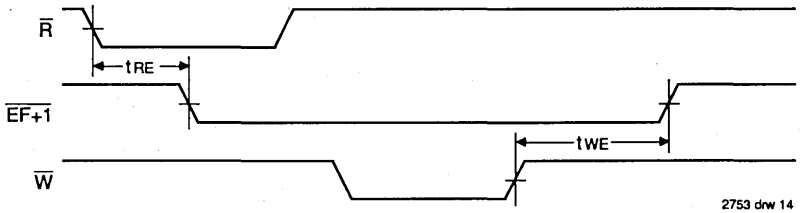


Figure 11. Empty+1 Flag Timings

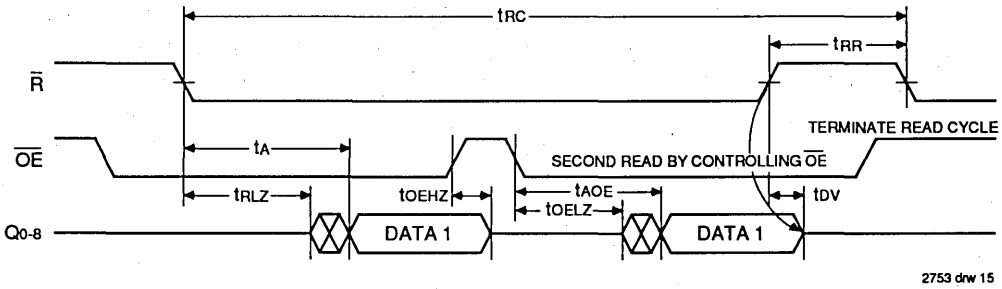


Figure 12. Output Enable Timings

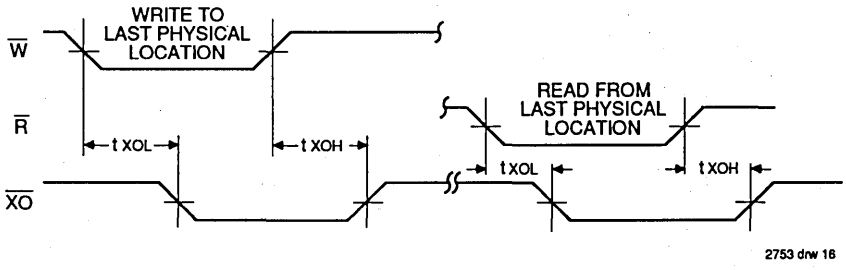


Figure 13. Expansion-Out

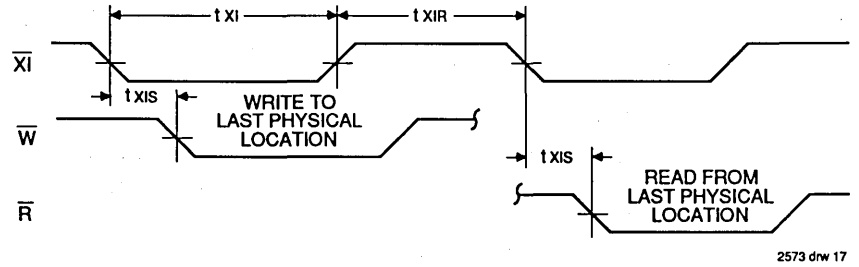


Figure 14. Expansion-In

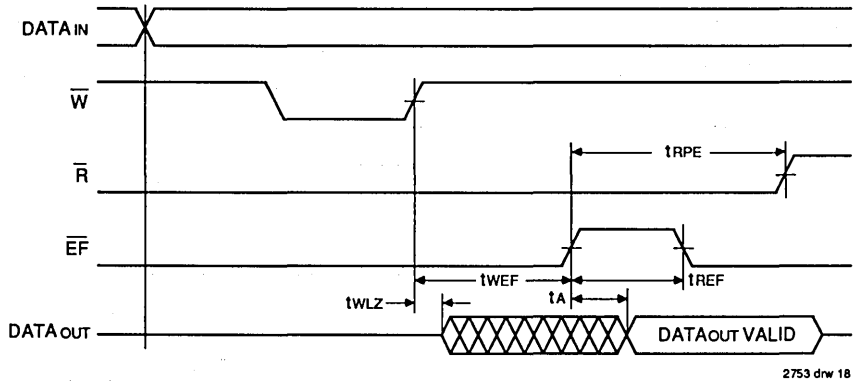


Figure 15. Read Data Flow-Through Mode

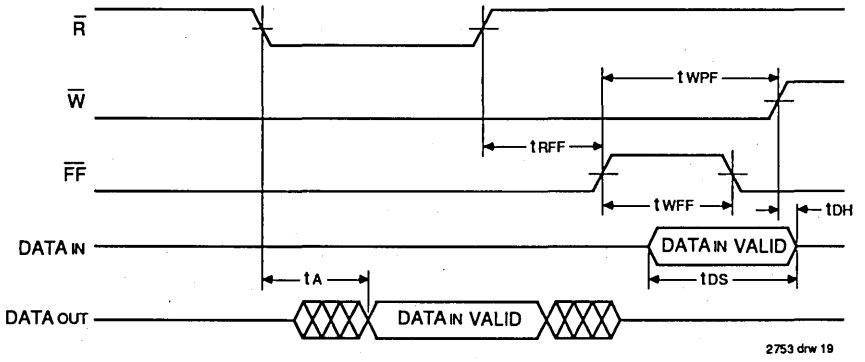
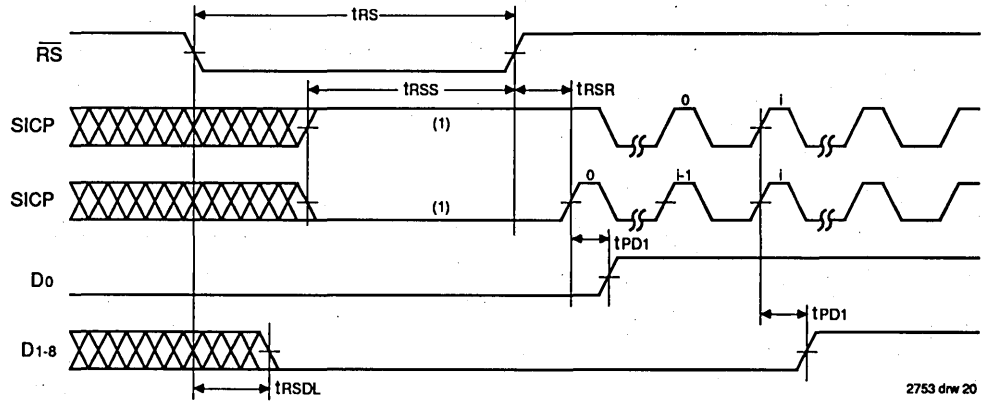


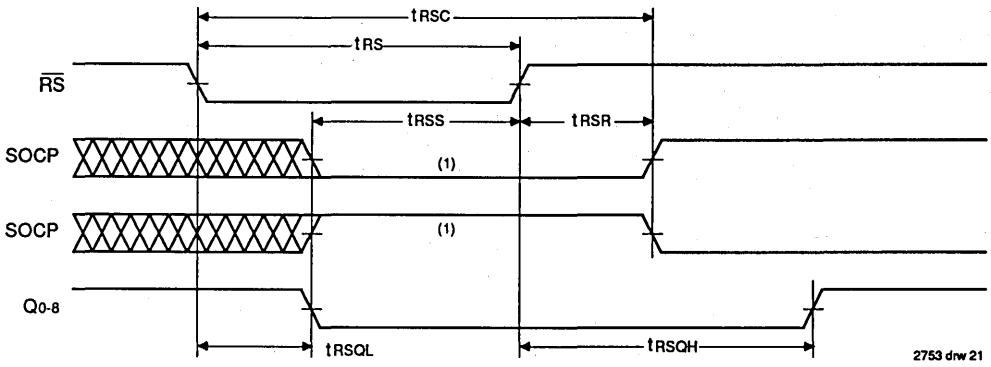
Figure 16. Write Data Flow-Through Mode

SERIAL TIMINGS:



NOTE:
1. SICP should be in the steady low or high during tRSS. The first low-high (or high-low) transition can begin after tRSR.

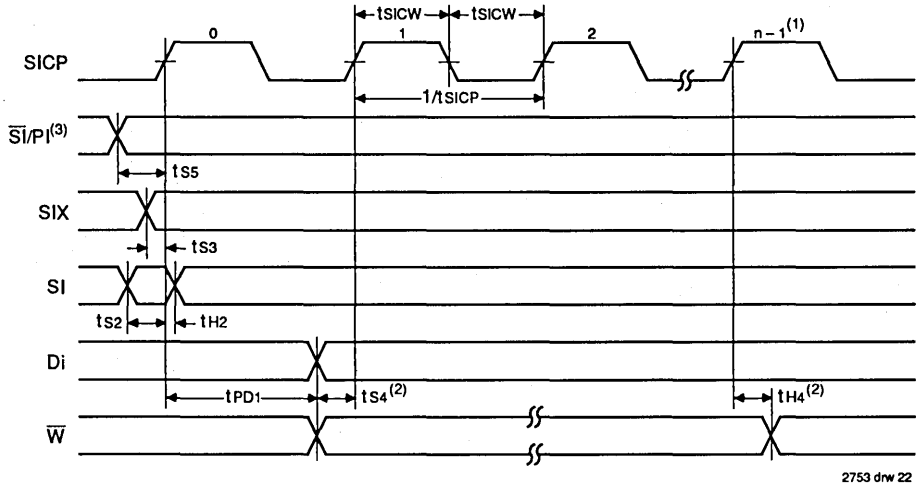
Figure 17. Reset Timings for Serial-In Mode



NOTE:
1. SOCP should be in the steady low or high during tRSS. The first low-high (or high-low) transition can begin after tRSR.

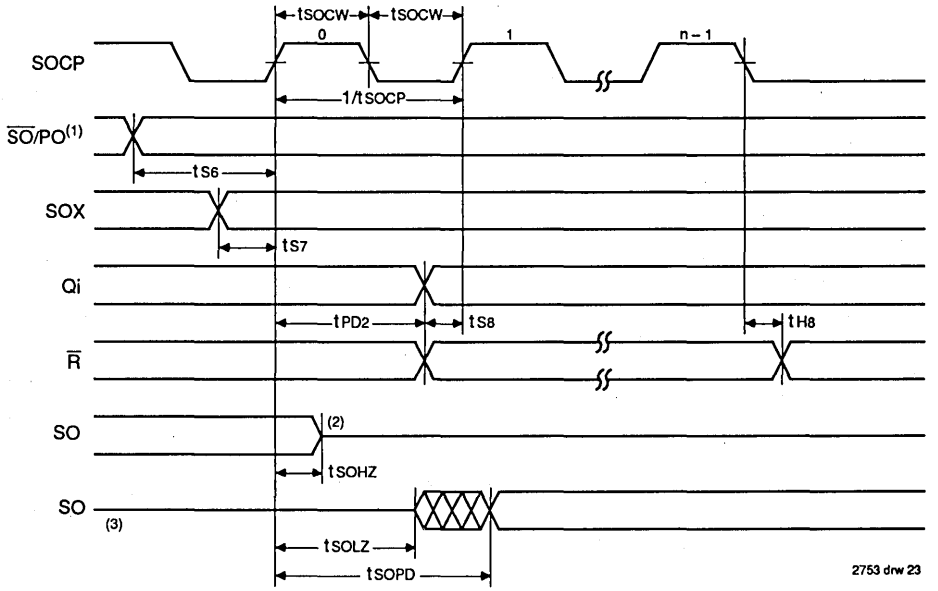
Figure 18. Reset Timings for Serial-Out Mode

6



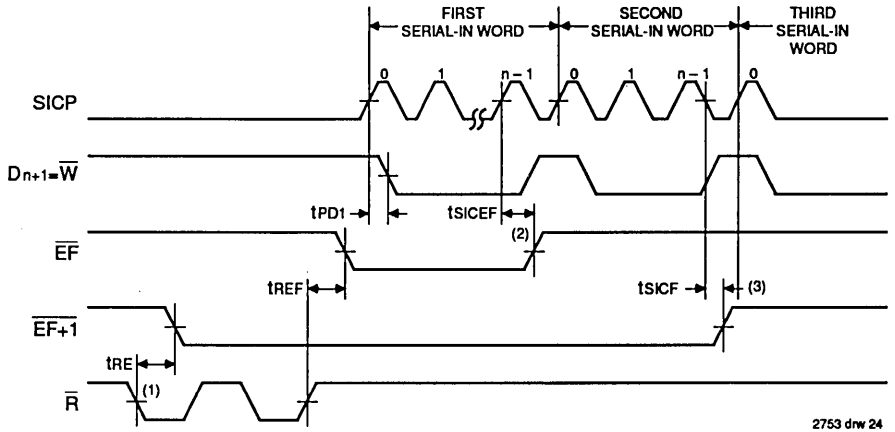
NOTES:
1. For the stand alone mode, N ≥ 4 and the input bits are numbered 0 to N-1.
2. For the recommended interconnections, Di is to be directly tied to $\overline{W}$ and the t_{S4} and t_{H4} requirements will be satisfied. For users that modify $\overline{W}$ externally, t_{S4} and t_{H4} requirements have to be met.
3. After $\overline{SI}$/PI has been set up, it cannot be dynamically changed; it can only be changed after a reset operation.

Figure 19. Write Operation In Serial-In Mode



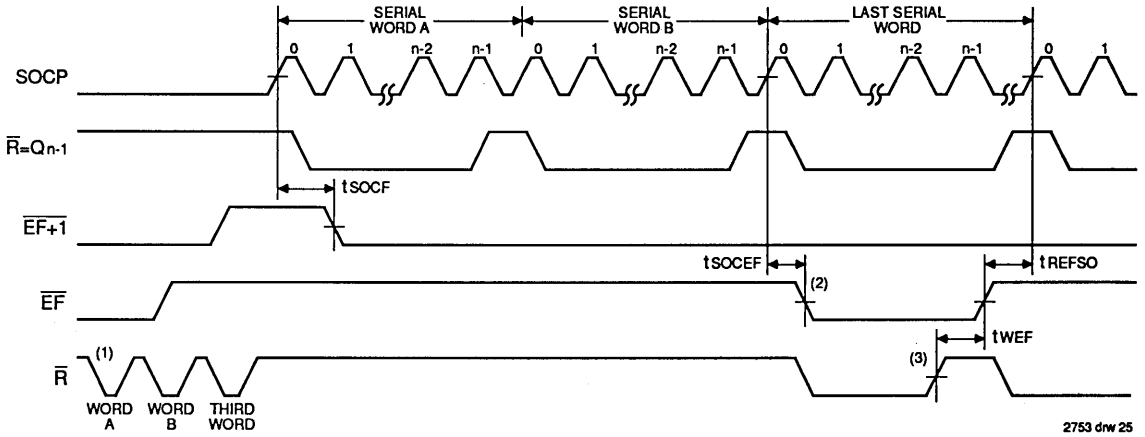
NOTES:
1. After $\overline{SO}$/PO has been set up, it cannot be dynamically changed; it can only be changed after a reset operation.
2. For single device: Read out the last bit before $\overline{EF}$ is asserted.
   For Serial Width Expansion mode: Read out the last bit of the current memory location from the active device.
3. For single device: The operation starts after Reset.
   For Serial Width Expansion mode: Read the first bit of the current memory location from the active device.

Figure 20. Read Operation In Serial-Out Mode



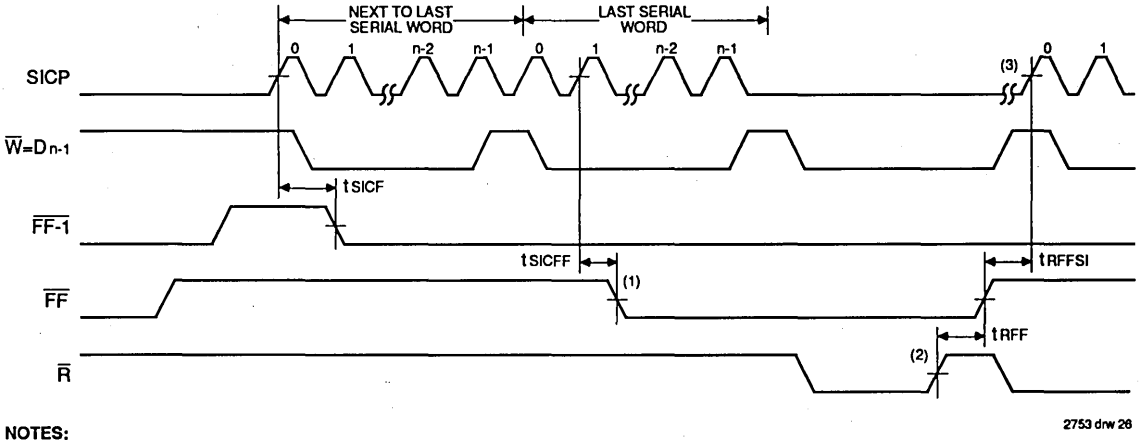
NOTES:
1. Parallel Read shown for reference only. Can also use serial output mode.
2. The Empty Flag is de-asserted after the N–1 rising edge of SICP of the first serial-in word. In the Serial-Out mode, a new read operation can begin tREFSO after EF goes HIGH. In the Parallel-Out mode, a new read operation can occur immedately after FF goes HIGH.
3. The EF+1 Flag is de-asserted after the N–1 rising edge of SICP of the second serial-in word.

Figure 21. Empty Flag and Empty+1 Flag De-assertion In the Serial-In Mode



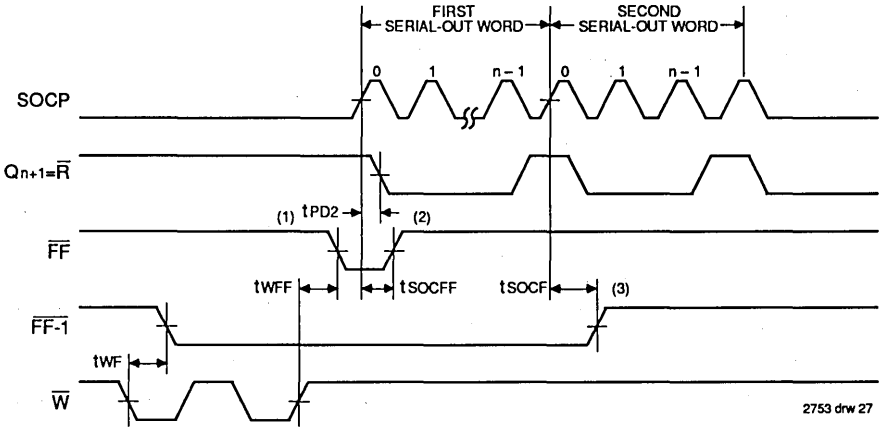
NOTES:
1. Parallel write shown for reference only. Can also use serial input mode.
2. The Empty Flag (EF) is asserted in Serial-Out mode by using the tSOCEF parameter. This parameter is measured in the worst case condition from the rising edge of the SOCP used to clock data bit 0. Whenever EF goes LOW, there is only one word to be shifted out. In the Parallel-In mode, the EF flag is de-asserted by the rising edge of W. In the Serial-In mode, the EF flag is de-asserted by the rising edge of W.
3. First Write rising edge after EF is set.
4. SOCP should not be clocked until EF goes HIGH.

Figure 22. Empty Flag and Empty+1 Flag Assertion In the Serial-Out Mode (FIFO Being Emptied)



NOTES:
1. The Full Flag is asserted in the Serial-In mode by using the tSICFF parameter. This parameter is measured in the worst case condition from the rising edge of SICP followed by a (tPD1+tWFF) delay from the first rising edge of SICP of the last word.
2. First Read rising edge after $\overline{FF}$ is set.
3. SICP should not be clocked until $\overline{FF}$ goes HIGH.

Figure 23. Full Flag and Full-1 Flag Assertion in the Serial-In Mode (FIFO Being Filled)



NOTES:
1. The FIFO is full and a new read sequence is started.
2. On the first rising edge of SOCP, the $\overline{FF}$ is de-asserted. In the Serial-In mode, a new write operation can begin following tRFFS1 after $\overline{FF}$, goes HIGH. In the Parallel-In mode, a new write operation can occur immediately after $\overline{FF}$ goes HIGH.
3. The $\overline{FF-1}$ flag is de-asserted after the first SOCP of the second serial word.

Figure 24. Full Flag and Full-1 Flag De-assertion in the Serial-Out Mode

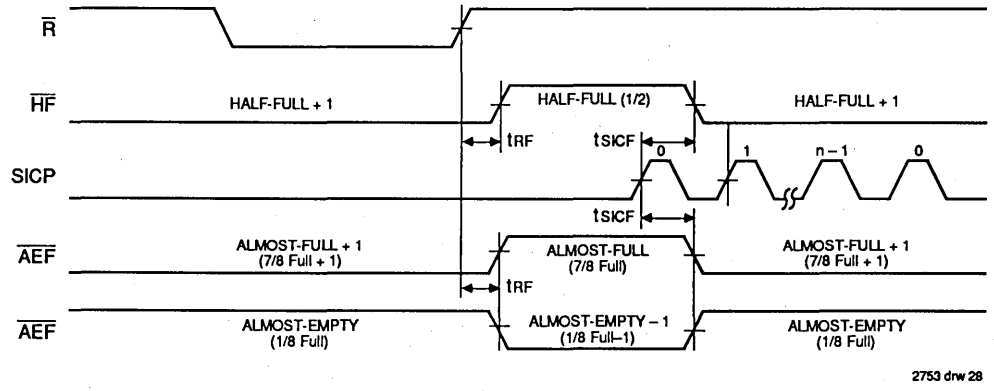


Figure 25. Half-Full, Almost-Full and Almost-Empty Timings for Serial-In Mode

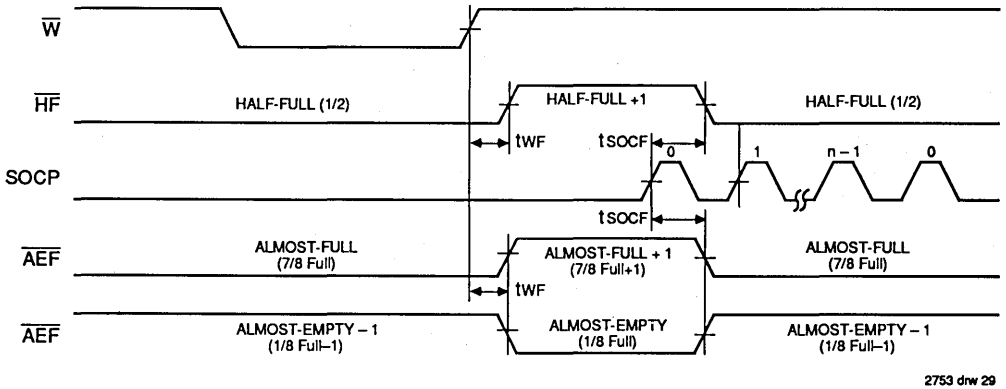


Figure 26. Half-Full, Almost-Full and Almost-Empty Timings for Serial-Out Mode

6

OPERATING DESCRIPTION

PARALLEL OPERATING MODES:

Parallel Data Input

By setting $\overline{SI}$/PI high, data is written into the FIFO in parallel through the D_0-D_8 input data lines.

Parallel Data Output

By setting $\overline{SO}$/PO high, the parallel-out mode is chosen. In the parallel-out mode, as shown in Figure 4, data is available t_A after the falling edge of $\overline{R}$ and the output bus Q goes into high impedance after $\overline{R}$ goes high.

Alternately, the user can access the FIFO by keeping $\overline{R}$ low and enabling data on the bus by asserting $\overline{OE}$. When $\overline{R}$ is low, the $\overline{OE}$ is high and the output bus is tri-stated. When $\overline{R}$ is high, the output bus is disabled irrespective of $\overline{OE}$. The enable and disable timings for $\overline{OE}$ are shown in Figure 12.

Single Device Mode

A single ID172103/72104 may be used when application requirements are for 2048/4096 words or less. The IDT72103/72104 is in the Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (See Figure 27). In this mode, the $\overline{HF}$/$\overline{XO}$ is used as an Half-Full flag.

Width Expansion Mode

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags can be detected from any one of the connected devices. Figure 28 demonstrates an 18-bit word width by using two IDT72103/72104s. Any word width can be attained by adding additional IDT72103/72104.

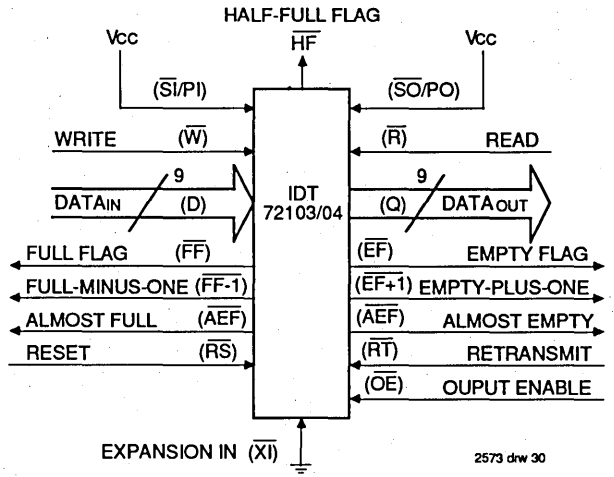


Figure 27. Block Diagram of Single 2048 x 9/4096 x 9 FIFO in Parallel Mode

INPUT CONFIGURATION TABLE

Pin	Parallel Input	Serial Input			
			Width Expansion		
		Single Device	Least Significant Device	All Other Devices	Most Significant Device
$\overline{SI}$/PI	HIGH	LOW	LOW	LOW	LOW
SI	HIGH	Input Data	Input Data	Input Data	Input Data
SICP	HIGH	Input Clock	Input Clock	Input Clock	Input Clock
SIX	HIGH	HIGH	HIGH	D_8 of next least significant device	D_8 of next least significant device
$\overline{W}$	Write Control	Di	Di of most significant device	Di of most significant device	Di of most significant device
D_0-D_8	Input Data	No connect except Di	No connect except D_8	No connect except D_8	No connect except Di
D_i[1]	—	$\overline{W}$	—	—	$\overline{W}$ of all devices
D_8	—	—	—	SIX of next most significant device	SIX of next most significant device

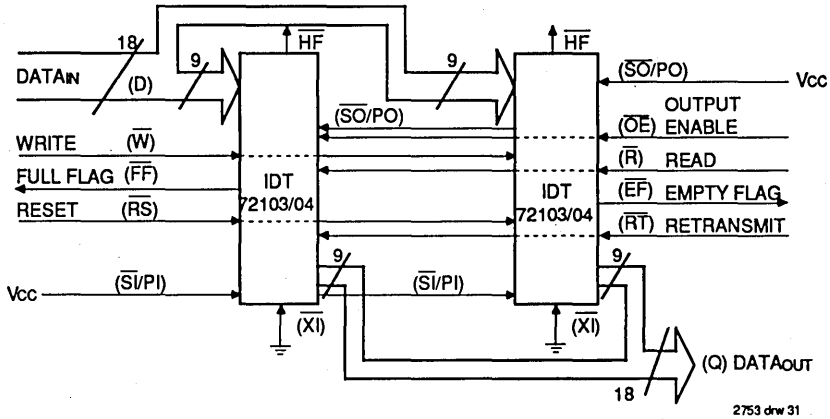
NOTE: 2753 tbl 13
1. Di refers to the most significant bit of the serial word. If multiple devices are width cascaded, Di is the most significant bit from the most significant device.

OUTPUT CONFIGURATION TABLE

Pin	Parallel Input	Serial Input			
			Width Expansion		
		Single Device	Least Significant Device	All Other Devices	Most Significant Device
$\overline{SO}$/PO	HIGH	LOW	LOW	LOW	LOW
SO	HIGH	Output Data	Output Data	Output Data	Output Data
SOCP	HIGH	Output Clock	Output Clock	Output Clock	Output Clock
SOX	HIGH	HIGH	HIGH	Q_8 of next least significant device	Q_8 of next least significant device
$\overline{R}$	Read Control	Qi	Qi of most significant device	Qi of most significant device	Di of most significant device
Q_0-Q_8	Output Data	No connect except Di	No connect except Q_8	No connect except Q_8	No connect except Qi
Q_i[1]	—	$\overline{R}$	—	—	$\overline{W}$ of all devices
Q_8	—	—	SOX of next most significant device	SOX of next most significant device	—

NOTE: 2753 tbl 14
1. Qi refers to the most significant bit of the serial word. If multiple devices are width cascaded, Qi is the most significant bit from the most significant device.

6



NOTE:
1. Flag detection is accomplished by monitoring all the flag signals of either (any) device used in the width expansion configuration. Do not connect any flag signals together.

Figure 28. Block Diagram of 2048 x 18/4096 x 18 FIFO Memory Used in Width Expansion in Parallel Mode

TRUTH TABLES
TABLE 2: RESET AND RETRANSMIT — SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION IN PARALLEL MODE

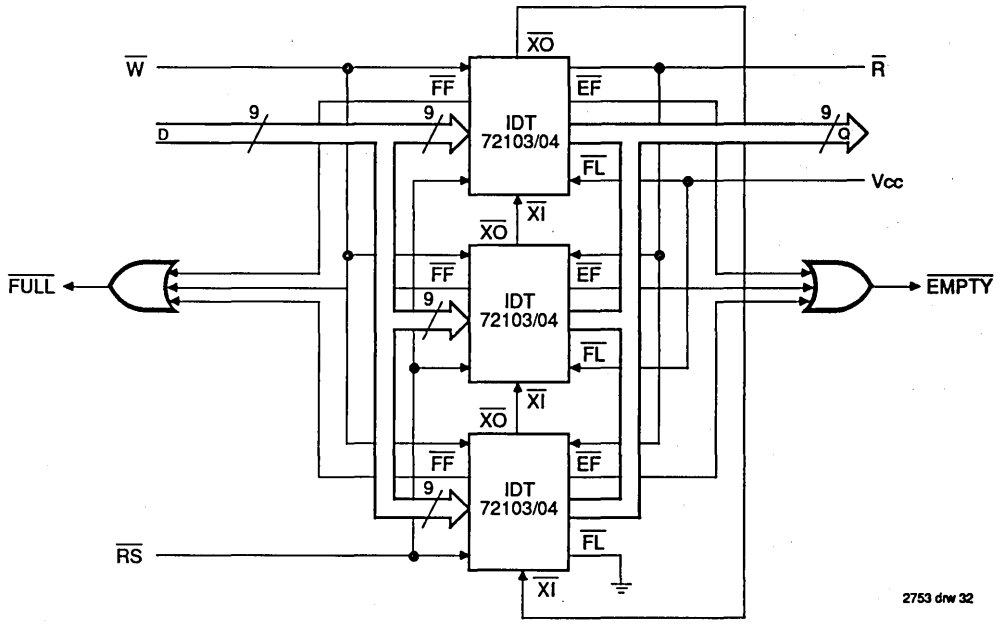
	Inputs[2]			Internal Status[1]		Outputs		
Mode	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{AEF}$, $\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment[1]	Increment[1]	X	X	X

NOTES: 2753 tbl 15
1. Pointer will increment if appropriate flag is HIGH.
2. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input.

Depth Expansion (Daisy Chain) Mode

The IDT72103/4 can be easily adapted to applications where the requirements are for greater than 2048/4096 words. Figure 29 demonstrates Depth Expansion using three IDT72103/4s. Any memory depth can be attained by adding additional IDT72103/4s. The IDT72103/4 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input pin.
2. All other devices must have the $\overline{FL}$ pin in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 29.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the OR-ing of all $\overline{EF}$s and OR-ing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite FF or E F). See Figure 29.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion mode.

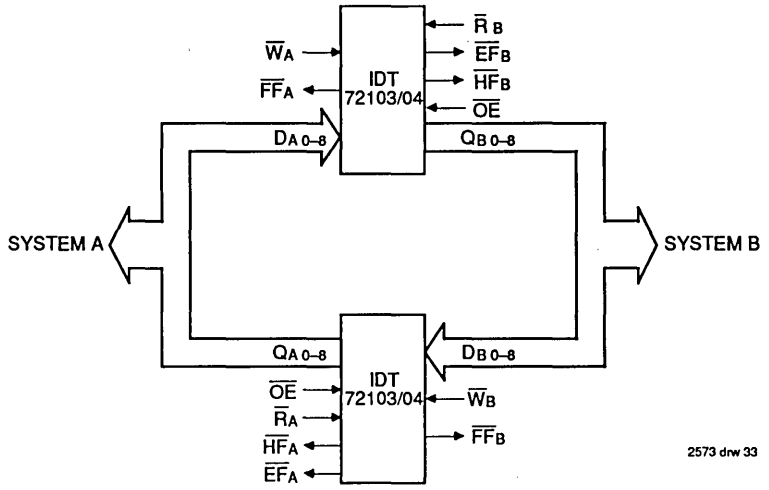


NOTE:
1. $\overline{SI}$/PI and $\overline{SO}$/PO pins are tied to Vcc.

Figure 29. Block Diagram of 6,144 x 9/12,288 x 9-FIFO Memory, Depth Expansion In Parallel Mode

Bidirectional Mode

Applications requiring data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT72103/4 as shown in Figure 30. Both Depth Expansion and Width Expansion may be used in this mode.

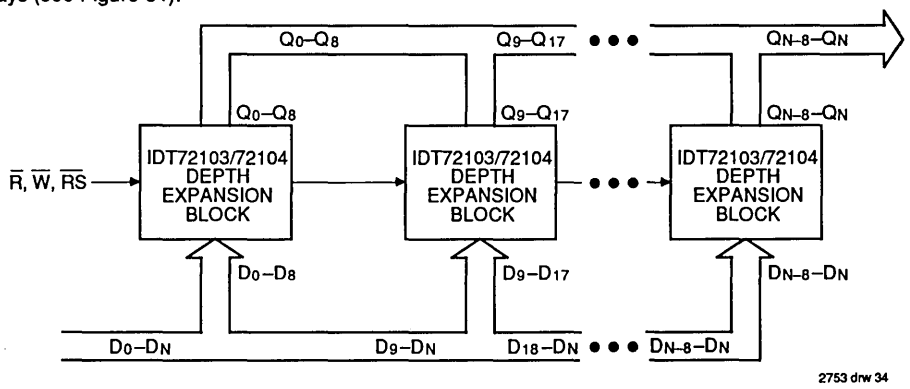


NOTE:
1. $\overline{SI}$/PI and $\overline{SO}$/PO pins are tied to Vcc.

Figure 30. Bidirectional FIFO Mode

Compound Expansion Mode

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 31).



NOTE:
1. $\overline{SI}$/PI and $\overline{SO}$/PO pins are tied to Vcc.
2. For depth expansion block see DEPTH EXPANSION Section and Figure 29.
3. For Flag Detection see WIDTH EXPANSION SECTION and Figure 28.

Figure 31. Compound FIFO Expansion

TABLE 3: RESET AND FIRST LOAD TRUTH TABLE — DEPTH EXPANSION/COMPOUND EXPANSION MODE

Mode	Inputs[2]			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Retransmit all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES: 2753 tbl 16
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device.
2. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Ouput, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input.

SERIAL OPERATING MODES:

Serial Data Input

The Serial Input mode is selected by grounding the $\overline{SI}$/PI line. The D_{0-8} lines are then outputs which are used to program the width of the serial word. They are taps off a digital delay line which, are meant for connection to the $\overline{W}$ input. For instance, connecting D_6 to $\overline{W}$ will program a serial word width of 7 bits, connecting D_7 to $\overline{W}$ will program a serial word width of 8 bits and so on.

By programming the serial word width, an economy of clock cycles is achieved. As an example, if the word width is 6 bits, then on every 6th clock cycle the serial data register is written in parallel into the FIFO RAM array. Thus, the possible clock cycles for an extra 3 bits of width in the RAM array are not required.

The SIX signal is used for Serial-In Expansion. When the serial word width is 9 or less, the SIX input must be tied HIGH. When more than 9 bits of serial word width is required, more than one device is required. The SIX input of the least significant device must be tied HIGH. The D_8 pin of the least significant device must be tied to SIX of the next significant device. In other words, the SIX input of the most significant and intermediate devices must always be connected to the D_8 of the next least significant device.

Figure 32 shows the relationship of the SIX, SICP and D_{0-8} lines. In the stand alone case (Figure 32), on the first LOW-to-HIGH of SICP, the D_{1-7} lines go LOW and the D0 line remains HIGH. On the next SICP clock edge, the D_1 goes HIGH, then D_2 and so on. This continues until the D line, which is connected to $\overline{W}$, goes HIGH. On the next clock cycle, after $\overline{W}$ is HIGH, all of the D lines go LOW again and a new serial word input starts.

In the cascaded case, the first LOW-to-HIGH SICP clock edge for a serial word will cause all timed outputs (D) to go LOW except for D_0 of the least significant device. The D outputs of the least significant device will go high on consecutive clock cycles until D_8. When D_8 goes HIGH, the SIX of the next device goes HIGH. On the next cycle after the SIX input is brought HIGH, the D_0 goes HIGH; then on the next cycle D_1 and so on. A D_1 output from the most significant device is issued to create the $\overline{W}$ for all cascaded devices.

The minimum serial word width is 4 bits and the maximum is virtually unlimited.

When in the Serial mode, the Least Significant Bit of a serial stream is shifted in first. If the FIFO output is in the Parallel mode, the first serial bit will come out on Q_0. The second bit shifted in is on Q_1 and so on.

In the Serial Cascade mode, the serial input (SI) pins must be connected together. Each of the devices then receives serial information together and uses the SIX and D_{0-8} lines to determine whether to store it or not.

The example shown in Figure 34 shows the interconnections for a serializing FIFO that transfers data to the internal RAM in 16-bit quantities (i.e. every 16 SICP cycles). This corresponds to incrementing the write pointer every 16 SICP cycles.

6

SINGLE DEVICE SERIAL INPUT CONFIGURATION

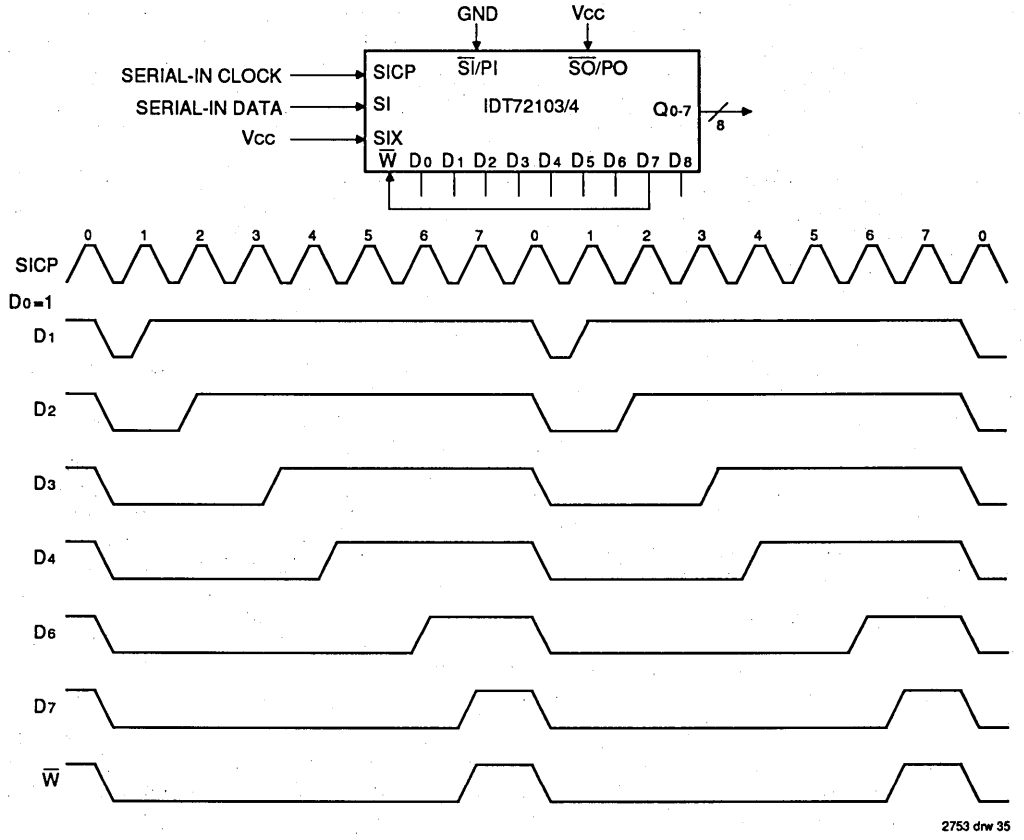


Figure 32. Serial-In Mode Where 8-Bit Parallel Output Data Is Read

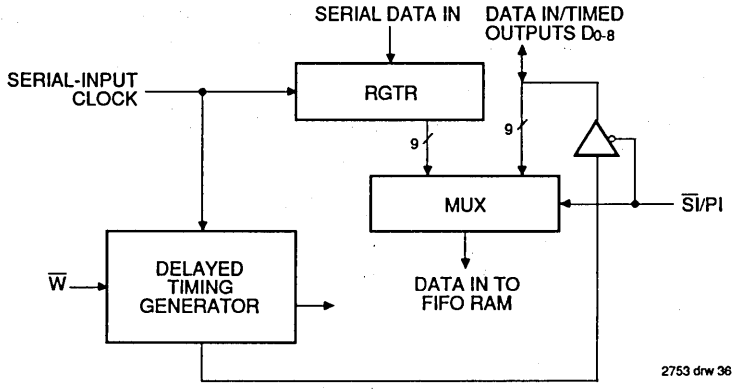


Figure 33. Serial-Input Circuitry

SERIAL INPUT WIDTH EXPANSION

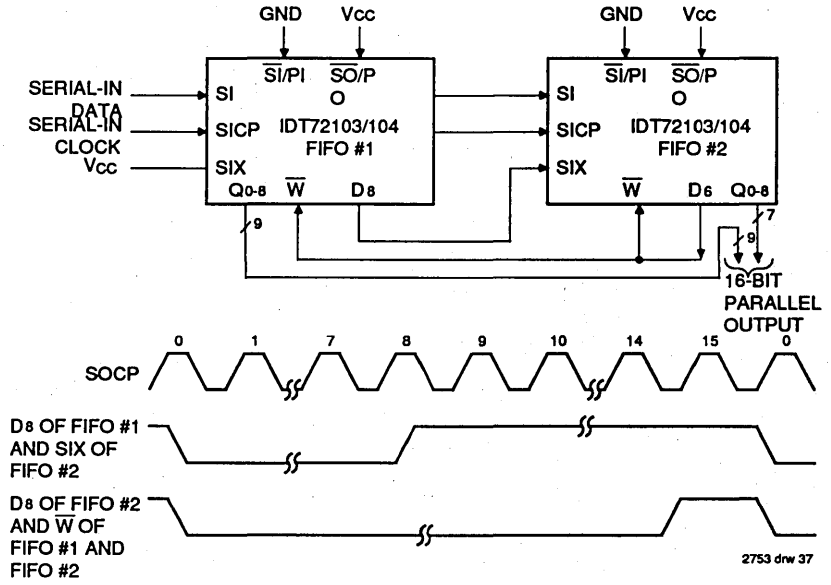
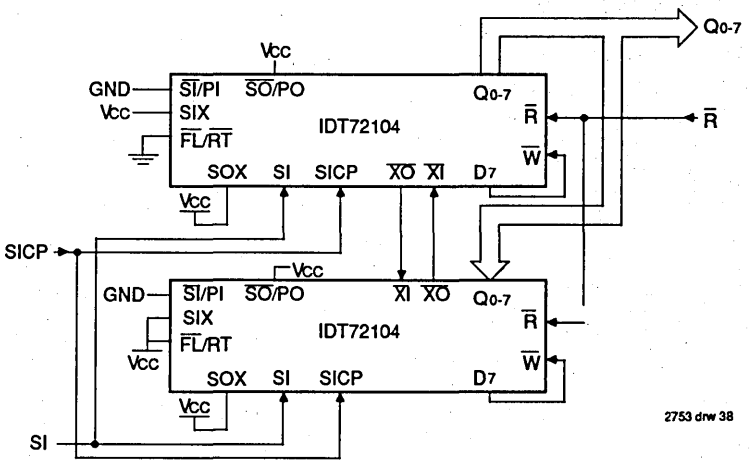


Figure 34. Serial-In Configuration for Serial-In to Parallel-Out Data of 16 bits

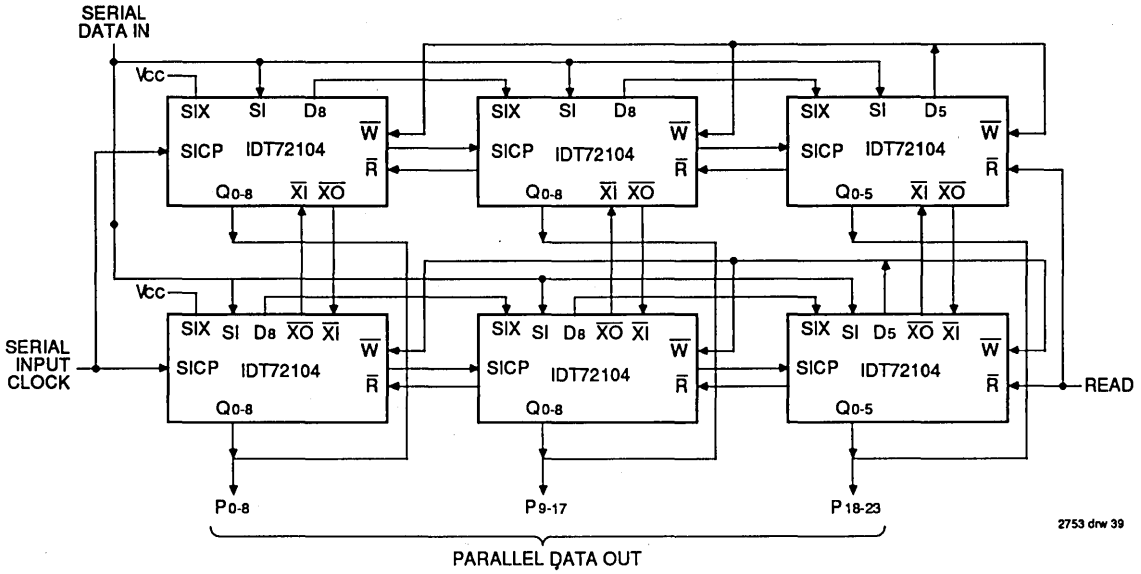
SERIAL INPUT WITH DEPTH EXPANSION



NOTE:
1. All SI/PI pins are tied to GND and SO/PO pins are tied to Vcc. OE is tied LOW. For FF and EF connections see Figure 17.

Figure 35. An 8K x 8 Serial-In, Parallel-Out FIFO

SERIAL INPUT WITH WIDTH AND DEPTH EXPANSION



NOTE:
1. All $\overline{SI}$/PI pins are tied to GND. $\overline{SO}$/PO pins are tied to Vcc. For $\overline{FF}$ and $\overline{EF}$ connections see Figure 17.

Figure 36. An 8K x 24 Serial-In, Parallel-Out FIFO Using Six IDT72104s

Serial Data Output

The Serial Output mode is selected by setting the $\overline{SO}$/PO line low. When in the Serial-Out mode, one of the Q_{0-2} lines should be used to control the $\overline{R}$ signal. In the Serial-Out mode, the Q_{0-8} are taps off a digital delay line. By selecting one of these taps and connecting n to the input, the width of the serial word to be read and shifted is programmed. For instance, if the Q_5 line is connected to the $\overline{R}$ input, on every sixth clock cycle a new word is read from the FIFO RAM array and begins to be shifted out. The serial word is shifted out Least Significant Bit First. If the input mode of the FIFO is parallel, the information that was written into the D_0 bit will come out as the first bit of the serial word. The second bit of the serial stream will be the D_1 bit and so on.

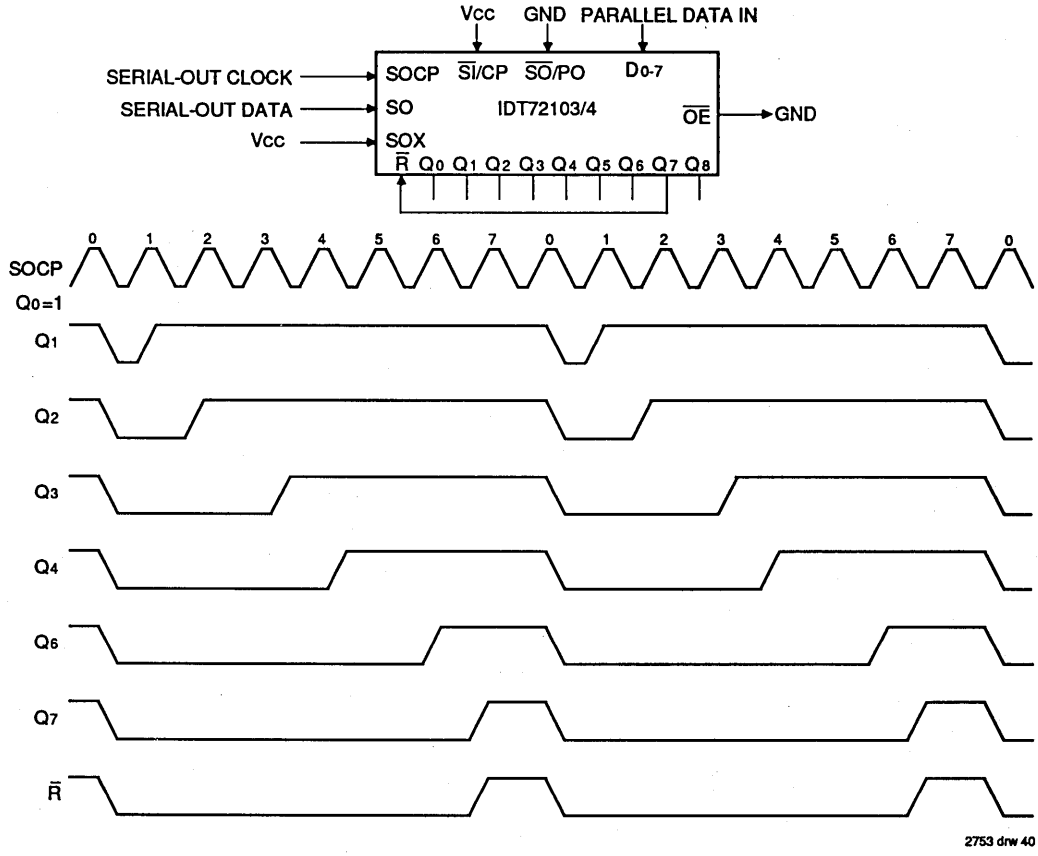
In the stand alone case, the SOX line is tied HIGH and not used. On the first LOW-to-HIGH of the SOCP clock, all of the Q outputs except for Q_0 go LOW and a new serial word is started. On the next clock cycle, Q_1 will go HIGH, Q_2 on the next clock cycle and so on, as shown in Figure 37. This continues until the Q line, shich is connected to $\overline{R}$, goes HGIH at which point all of the Q lines go LOW on the next clock and a new word is started.

In the cascaded case, word width of more than 9 bits can be achieved by using more than one device. By tieing the SOX line of the least significant device HIGH and the SOX of the subsequent deviced to Q_8 of the previous devices, a cascaded serial word is achieved. On the first LOW-to-HIGH clock edge of SOCP, all the lines except for Q_0. Just as in the stand alone case, on each consecutive clock cycle, each Q line goes HIGH in the order of least to most significant. When Q8 (which is connected to the SOX input of the next device) goes HIGH, the D_0 of that device goes HIGH, thus cascading from one device to the next. The Q line of the most significant device, which programs the serial word width, is connected to all $\overline{R}$ inputs.

The Serial Data Output (SO) of each device in the serial word must be tied together. Since the SO pin is tri-stated, only the device which is currently shifting out is enabled and driving the 1-bit bus.

Figure 39 shows an example of the interconnections for a 16-bit serialized FIFO.

SINGLE DEVICE SERIAL OUTPUT CONFIGURATION



NOTE:
1. Input data is loaded in 8-bit quantities and read out serially.

Figure 37. Serial-Out Configuration

6

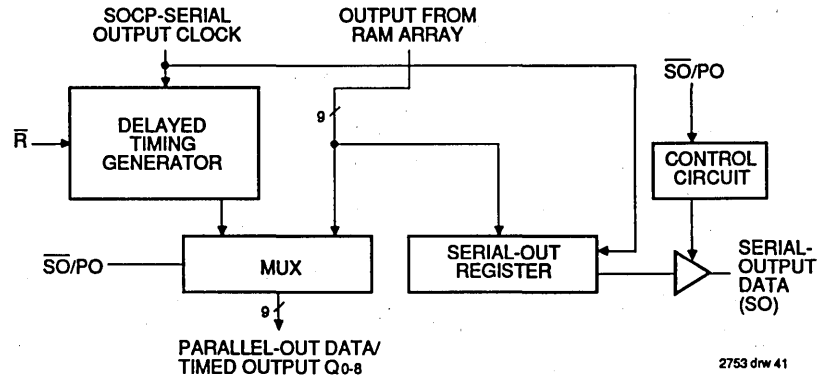
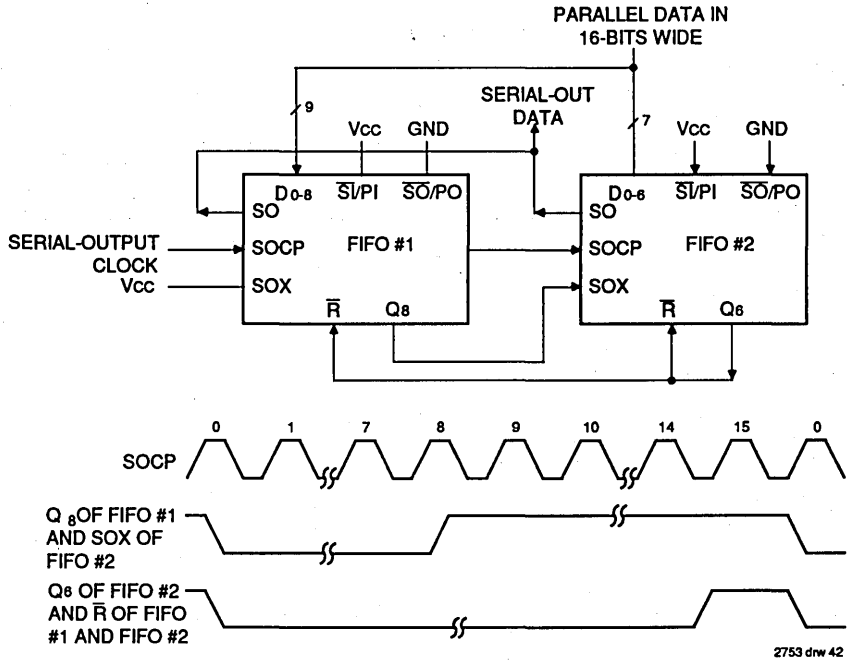


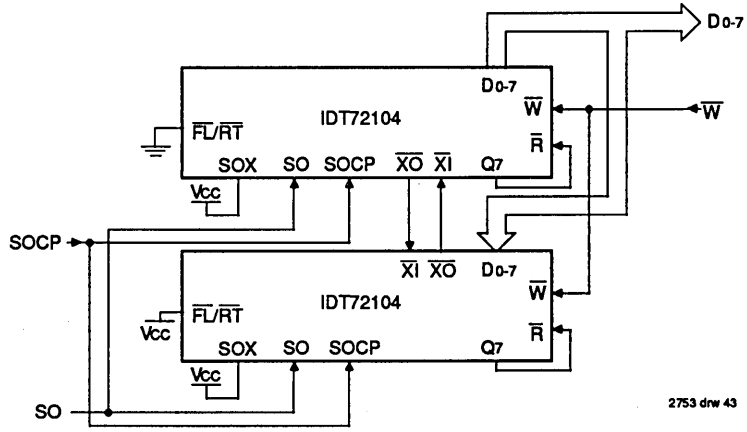
Figure 38. Serial-Output Circuitry



NOTE:
1. The parallel Data In is tied to D0-8 of FIFO #1 and D0-6 of FIFO #2.

Figure 39. Serial-Output for 16-Bit Parallel Data In

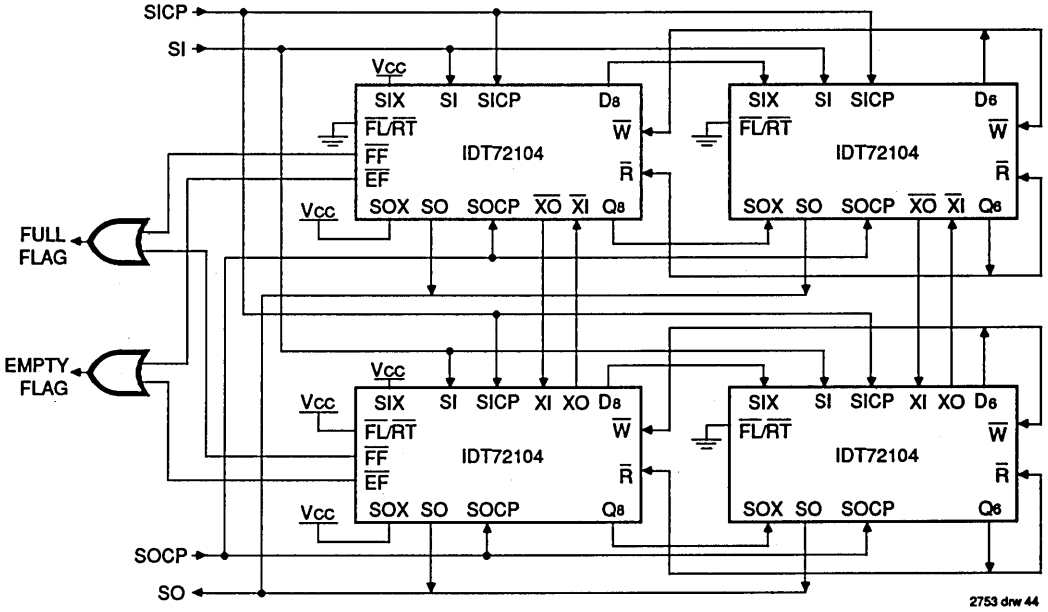
SERIAL OUTPUT WITH DEPTH EXPANSION



NOTE:
1. All SI/PI pins are tied to Vcc and SO/PO pins are tied to GND. OE is tied LOW. For FF and EF connections see Figure 17.

Figure 40. An 8K x 8 Parallel-In Serial-Out FIFO

SERIAL IN AND SERIAL OUT WITH WIDTH AND DEPTH EXPANSION

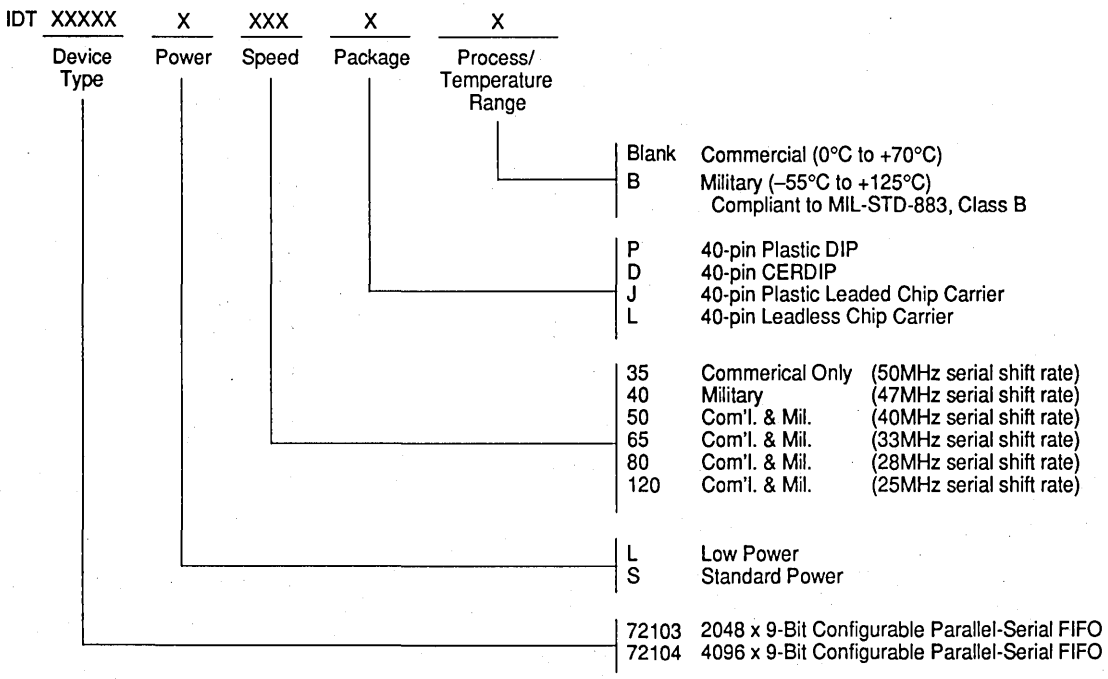


NOTE:
1. All RS pins are connected together. All OE pins are connected LOW. All SI/PI and SO/PO pins are grounded.

Figure 41. 128K x 1 Serial-In Serial-Out FIFO

6

ORDERING INFORMATION



2753 drw 45

Integrated Device Technology, Inc.

CMOS PARALLEL-TO-SERIAL FIFO 256 x 16, 512 x 16, 1024 x 16

IDT72105
IDT72115
IDT72125

FEATURES:

- 15ns parallel port access time, 25ns cycle time
- 50MHz serial output shift rate
- Wide x16 organization offering easy expansion
- Low power consumption (50mA typical)
- Least/Most Significant Bit first read selected by asserting the $\overline{FL}$/DIR pin
- Featuring five memory status flags: Empty, Full, Half-Full, Almost-Empty and Almost-Full
- Dual-port zero fall-through architecture
- Available in 28-pin 300 mil plastic and ceramic DIP, 28-pin SOIC and 32-pin PLCC
- Military product compliant to Mil-STD-883, Class B

DESCRIPTION:

The IDT72105/72115/72125s are very high speed, low power dedicated parallel-to-serial FIFOs. These FIFOs possess a 16-bit parallel input port and a serial output port offering 256, 512 and 1K word depths, respectively.

The ability to buffer wide word widths (x16) make these FIFOs ideal for laser printers, FAX machines, local area networks (LANs), video storage and disk/tape controller applications.

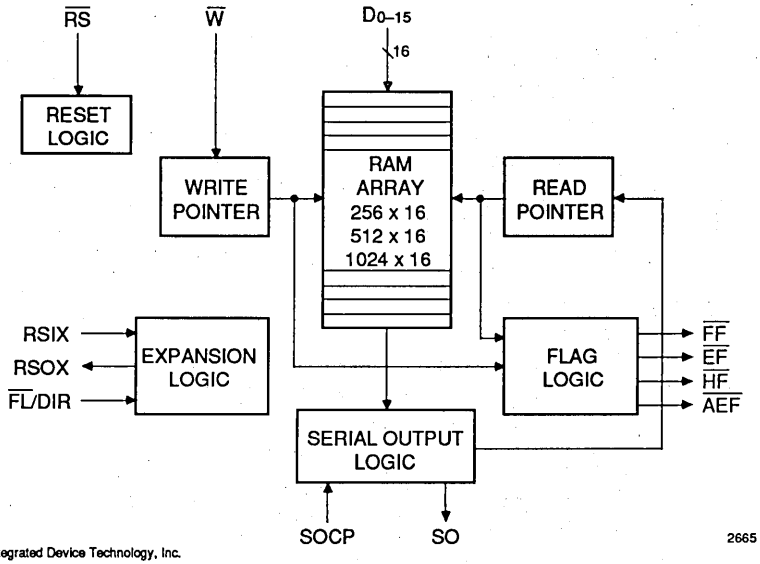
Expansion in width and depth can be achieved using multiple chips. IDT's unique serial expansion logic (RSIX, RSOX, $\overline{FL}$/DIR) makes this possible using a minimum of pins.

The unique serial output port is driven by one data pin (SO) and one clock pin (SOCP). The Least Significant or Most Significant Bit can be read first by programming the DIR pin after a reset.

Monitoring the FIFO is eased by the availability of five status flags: Empty, Full, Half-Full, Almost-Empty and Almost-Full. The Full and Empty flags prevent any FIFO data overflow or underflow conditions. The Half-Full Flag is available in both single and expansion mode configurations. The Almost-Empty and Almost-Full Flags are available only in a single device mode.

The IDT72105/15/25 are fabricated using IDT's leading edge, submicron CEMOS™ technology. Military grade product is manufactured in compliance with the latest revision of Mil-STD-883, Class B.

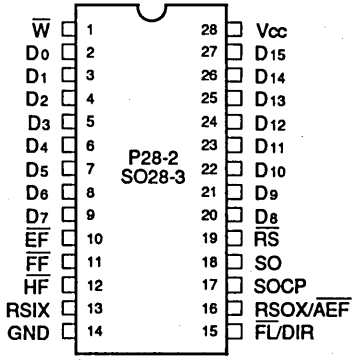
FUNCTIONAL BLOCK DIAGRAM



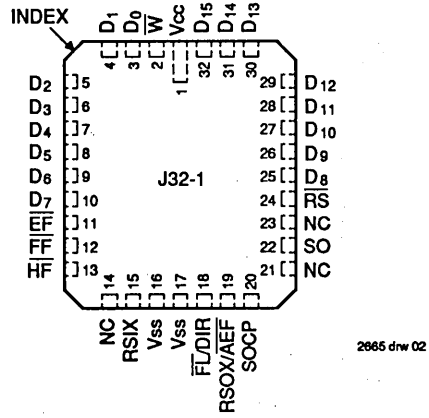
2665 drw 01

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP/SOIC
TOP VIEW



PLCC
TOP VIEW

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D0–D15	Inputs	I	Data inputs for 16-bit wide data.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{FF}$ and $\overline{HF}$ go HIGH. $\overline{EF}$ and $\overline{AEF}$ go LOW. A reset is required before an initial WRITE after power-up. $\overline{W}$ must be high during the $\overline{RS}$ cycle. Also the First Load pin ($\overline{FL}$) is programmed only during Reset.
$\overline{W}$	Write	I	A write cycle is initiated on the falling edge of WRITE if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of WRITE. Data is stored in the RAM array sequentially and independently of any ongoing read operation.
SOCP	Serial Output Clock	I	A serial bit read cycle is initiated on the rising edge of SOCP if the Empty Flag ($\overline{EF}$) is not set. In both Depth and Serial Word Width Expansion modes, all of the SOCP pins are tied together.
$\overline{FL}$/DIR	First Load/ Direction	I	This is a dual purpose input used in the width and depth expansion configurations. The First Load ($\overline{FL}$) function is programmed only during Reset ($\overline{RS}$) and a LOW on $\overline{FL}$ indicates the first device to be loaded with a byte of data. All other devices should be programmed HIGH. The Direction (DIR) function is programmed during operation after Reset and tells the device whether to read out the Least Significant or Most Significant bit first.
RSIX	Read Serial In Expansion	I	In the single device configuration, RSIX is set HIGH. In depth expansion or daisy chain expansion, RSIX is connected to RSOX (expansion out) of the previous device.
SO	Serial Output	O	Serial data is output on the Serial Output (SO) pin. Data is clocked out LSB or MSB depending on the Direction pin programming. During Expansion the SO pins are tied together.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ goes LOW, the device is full and further WRITE operations are inhibited. When $\overline{FF}$ is HIGH, the device is not full.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ goes LOW, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is HIGH, the device is not empty.
$\overline{HF}$	Half-Full Flag	O	When $\overline{HF}$ is LOW, the device is more than half-full. When $\overline{HF}$ is HIGH, the device is empty to half-full.
RSOX/$\overline{AEF}$	Read Serial Out Expansion Almost-Empty, Almost-Full Flag	O	This is a dual purpose output. In the single device configuration (RSIX HIGH), this is an $\overline{AEF}$ output pin. When $\overline{AEF}$ is LOW, the device is empty-to-(1/8 full -1) or (7/8 full +1)-to-full. When $\overline{AEF}$ is HIGH, the device is 1/8-full up to 7/8-full. In the Expansion configuration (RSOX connected to RSIX of the next device) a pulse is sent from RSOX to RSIX to coordinate the width, depth or daisy chain expansion.
Vcc	Power Supply		Single power supply of 5V.
GND	Ground		Single ground of 0V.

2665 tbl 01

STATUS FLAGS

Number of Words in FIFO						
IDT72105	IDT72115	IDT72125	$\overline{FF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF}$
0	0	0	H	L	H	L
1–31	1–63	1–127	H	L	H	H
32–128	64–256	128–512	H	H	H	H
129–224	257–448	513–896	H	H	L	H
225–255	449–511	897–1023	H	L	L	H
256	512	1024	L	L	L	H

2665 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to + 7.0	-0.5 to + 7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	° C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	° C
T_{STG}	Storage Temperature	-55 to + 125	-65 to + 155	° C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2665 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vccc	Commercial Supply Voltage	4.5	5.0	5.5	V
Vccm	Military Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}(1)	Input Low Voltage Commercial & Military	—	—	0.8	V

NOTE: 2665 tbl 04

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial Vcc = 5.0V ± 10%, TA = 0°C to +70°C; Military Vcc = 5V ± 10%, TA = -55°C to +125°C)

Symbol	Parameter	IDT72105/IDT72115/ IDT72125 Commercial Min.	Typ.	Max.	IDT72105/IDT72115/ IDT72125 Military Min.	Typ.	Max.	Unit
I_{IL}(1)	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	µA
I_{OL}(2)	Output Leakage Current	-10	—	10	-10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = -2mA(5)	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA(6)	—	—	0.4	—	—	0.4	V
I_{CC1}(3)	Power Supply Current	—	50	100	—	75	125	mA
I_{CC2}(3)	Average Standby Current ($\overline{W}$ = $\overline{RS}$ = $\overline{FL}$/DIR = V_{IH})(SOCP = V_{IL})	—	4	8	—	4	12	mA
I_{CC3}(3,4,7)	Power Down Current	—	1	6	—	1	8	mA

NOTES: 2665 tbl 05

1. Measurements with 0.4 ≤ V_{IN} ≤ V_{OUT}.
2. SOCP ≤ V_{IL}, 0.4 ≤ V_{OUT} ≤ Vcc.
3. Icc measurements are made with outputs open.
4. $\overline{RS}$ = $\overline{FL}$/DIR = $\overline{W}$ = Vcc - 0.2V; SOCP ≤ 0.2V; all other inputs ≥ Vcc - 0.2 or ≤ 0.2V.
5. For SO, I_{OUT} = -4mA.
6. For SO, I_{OUT} = 16mA.
7. Measurements are made after reset.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	Figure	COM'L		COMMERCIAL AND MILITARY						Unit
			72105L15 72115L15 72125L15		72105x25 72115x25 72125x25		72105x50 72115x50 72125x50		72105x80 72115x80 72125x80		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tS	Parallel Shift Frequency	—	—	40	—	28.5	—	15	—	10	MHz
tSOCP	Serial Shift Frequency	—	—	50	—	50	—	40	—	28	MHz
PARALLEL INPUT TIMINGS											
tWC	Write Cycle Time	2	25	—	35	—	65	—	100	—	ns
tWPW	Write Pulse Width	2	15	—	25	—	50	—	80	—	ns
tWR	Write Recovery Time	2	10	—	10	—	15	—	20	—	ns
tDS	Data Set-up Time	2	10	—	12	—	15	—	15	—	ns
tDH	Data Hold Time	2	0	—	0	—	2	—	5	—	ns
tWEF	Write High to $\overline{EF}$ High	5, 6	—	30	—	35	—	45	—	50	ns
tWFF	Write Low to $\overline{FF}$ Low	4, 7	—	30	—	35	—	45	—	50	ns
tWF	Write Low to Transitioning $\overline{HF}$, $\overline{AEF}$	8	—	30	—	35	—	45	—	50	ns
tWPF	Write Pulse Width After $\overline{FF}$ High	7	15	—	25	—	50	—	80	—	ns
SERIAL OUTPUT TIMINGS											
tSOCP	Serial Clock Cycle Time	3	20	—	20	—	25	—	35	—	ns
tSOCW	Serial Clock Width High/Low	3	8	—	8	—	10	—	15	—	ns
tSOPD	SOCP Rising Edge to SO Valid Data	3	—	14	—	14	—	15	—	17	ns
tSOHZ	SOCP Rising Edge to SO at High Z[1]	3	3	14	3	14	3	15	3	17	ns
tSOLZ	SOCP Rising Edge to SO at Low Z[1]	3	3	14	3	14	3	15	3	17	ns
tSOCEF	SOCP Rising Edge to $\overline{EF}$ Low	5, 6	—	35	—	35	—	45	—	50	ns
tSOCFF	SOCP Rising Edge to $\overline{FF}$ High	4, 7	—	35	—	35	—	45	—	50	ns
tSOCF	SOCP Rising Edge to Transitioning $\overline{HF}$, $\overline{AEF}$	8	—	35	—	35	—	45	—	50	ns
tREFSO	SOCP Delay After $\overline{EF}$ High	6	35	—	35	—	65	—	100	—	ns
RESET TIMINGS											
tRSC	Reset Cycle Time	1	25	—	35	—	65	—	100	—	ns
tRS	Reset Pulse Width	1	15	—	25	—	50	—	80	—	ns
tRSS	Reset Set-up Time	1	15	—	25	—	50	—	80	—	ns
tRSR	Reset Recovery Time	1	10	—	10	—	15	—	20	—	ns
EXPANSION MODE TIMINGS											
tFLS	$\overline{FL}$ Set-up Time to $\overline{RS}$ Rising Edge	9	7	—	7	—	8	—	10	—	ns
tFLH	$\overline{FL}$ Hold Time to $\overline{RS}$ Rising Edge	9	0	—	0	—	2	—	5	—	ns
tDIRS	DIR Set-up Time to SOCP Rising Edge	9	10	—	10	—	12	—	10	—	ns
tDIRH	DIR Hold Time from SOCP Rising Edge	9	5	—	5	—	5	—	5	—	ns
tSOXD1	SOCP Rising Edge to RSOX Rising Edge	9	—	15	—	15	—	17	—	20	ns
tSOXD2	SOCP Rising Edge to RSOX Falling Edge	9	—	15	—	15	—	17	—	20	ns
tSIXS	RSIX Set-up Time to SOCP Rising Edge	9	5	—	5	—	8	—	15	—	ns
tSIXPW	RSIX Pulse Width	9	10	—	10	—	15	—	20	—	ns

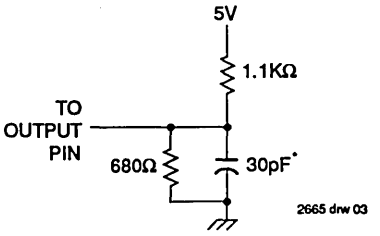
NOTE:
1. Guaranteed by design minimum times, not tested.

2665 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure A

2665 tbl 07



or equivalent circuit

Figure A. Output Load

*Includes jig and scope capacitances.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	10	pF
COUT	Output Capacitance	VOUT = 0V	12	pF

NOTE: 2665 tbl 08

1. This parameter is sampled and not 100% tested.

FUNCTIONAL DESCRIPTION

Parallel Data Input

The device must be reset before beginning operation so that all flags are set to initial state. In width or depth expansion the First Load pin ($\overline{FL}$/) must be programmed to indicate the first device.

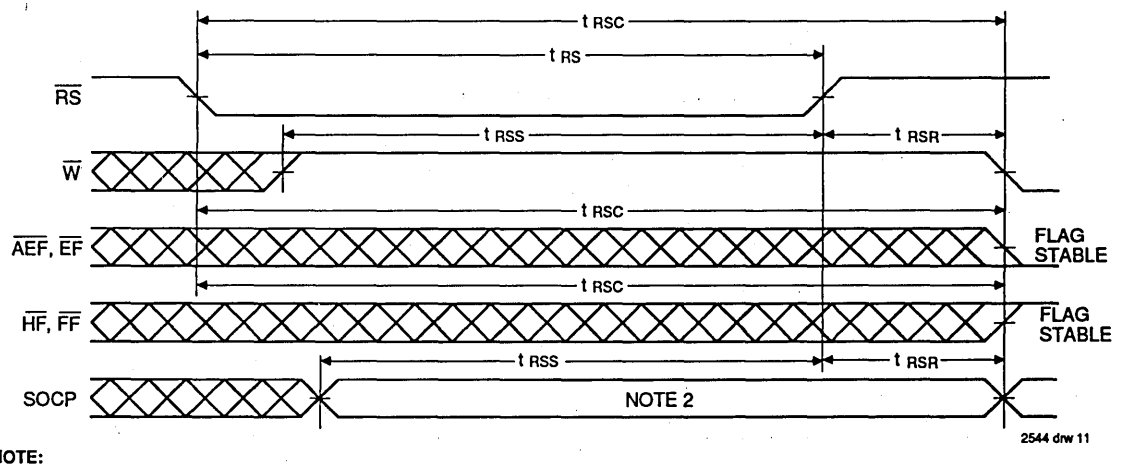
The data is written into the FIFO in parallel through the D0–15 input data lines. A write cycle is initiated on the falling edge of the Write ($\overline{W}$) signal provided the Full Flag ($\overline{FF}$) is not asserted. If the $\overline{W}$ signal changes from HIGH-to-LOW and the Full Flag ($\overline{FF}$) is already set, the write line is inhibited internally from incrementing the write pointer and no write operation occurs.

Data set-up and hold times must be met with respect to the rising edge of Write. On the rising edge of $\overline{W}$, the write pointer is incremented. Write operations can occur simultaneously or asynchronously with read operations.

Serial Data Output

The serial data is output on the SO pin. The data is clocked out on the rising edge of SOCP providing the Empty Flag ($\overline{EF}$) is not asserted. If the Empty Flag is asserted then the next data word is inhibited from moving to the output register and being clocked out by SOCP.

The serial word is shifted out Least Significant Bit or Most Significant Bit first, depending on the $\overline{FL}$/DIR level during operation. A LOW on DIR will cause the Least Significant Bit to be read out first. A HIGH on DIR will cause the Most Significant Bit to be read out first.



NOTE:
1. $\overline{EF}$, $\overline{FF}$, $\overline{HF}$ and $\overline{AEF}$ may change status during Reset, but flags will be valid at tRSC.
2. SOCP should be in the steady low or high during tRSS. The first low-high (or high-low) transition can begin after tRSR.

Figure 1. Reset

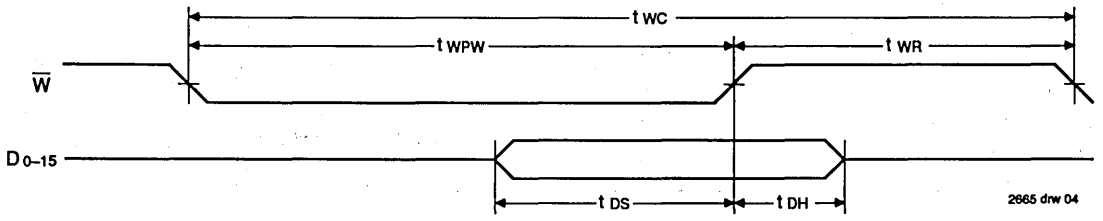
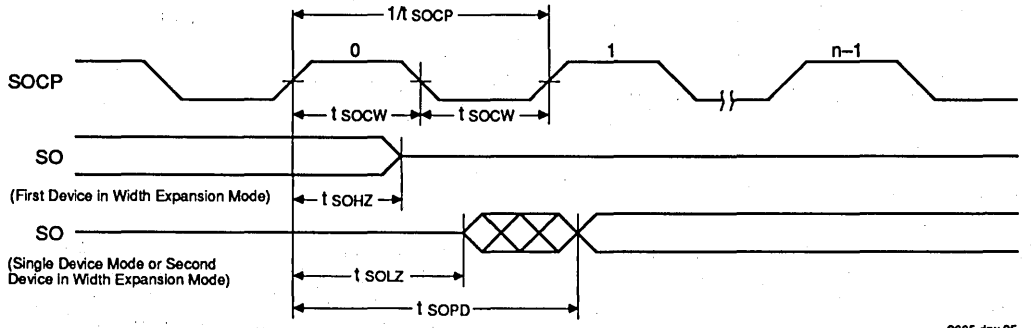


Figure 2. Write Operation



NOTE:
1. In Single Device Mode, SO will not tri-state except after reset.

Figure 3. Read Operation

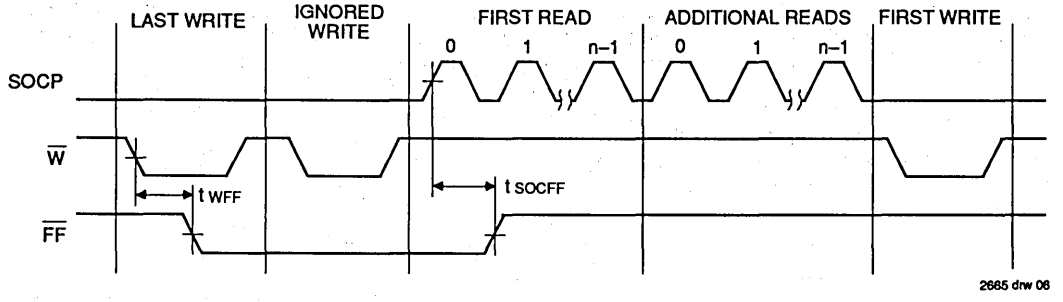
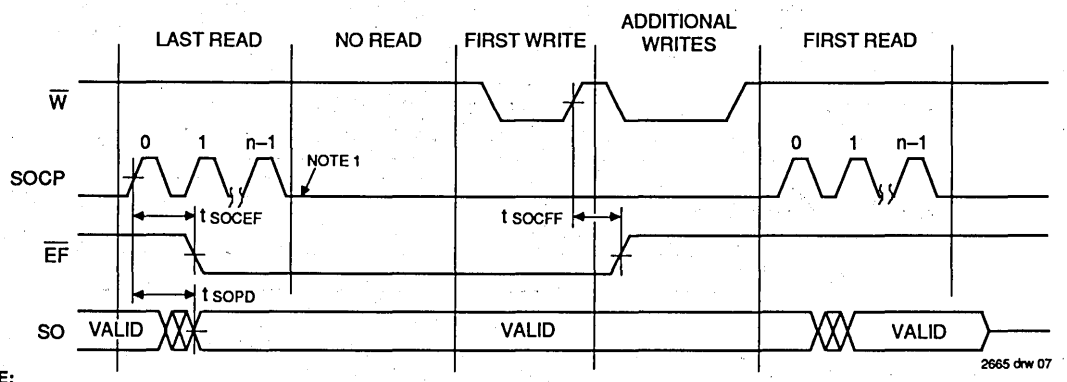
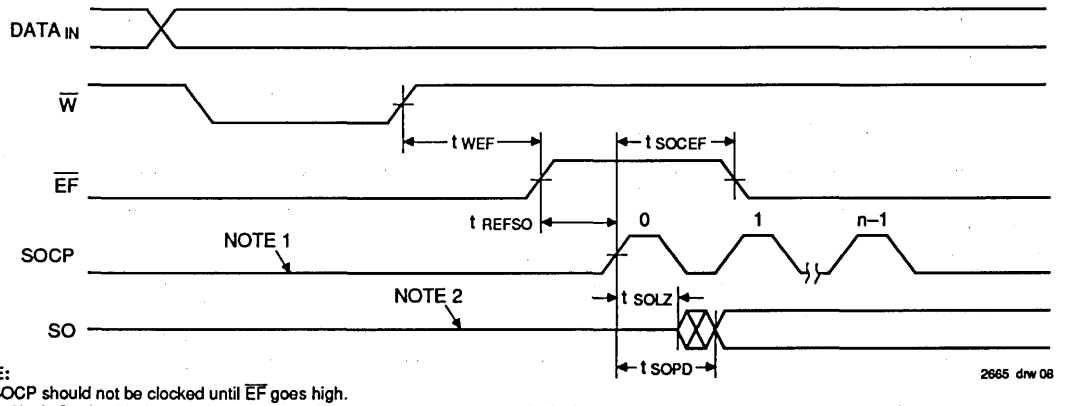


Figure 4. Full Flag from Last Write to First Read



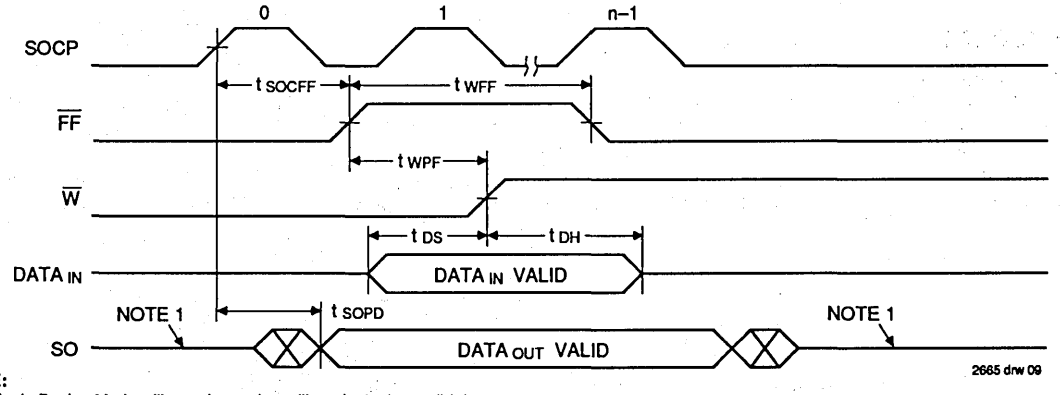
NOTE:
1. SOCP should not be clocked until $\overline{EF}$ goes high.

Figure 5. Empty Flag from Last Read to First Write



NOTE:
1. SOCP should not be clocked until $\overline{EF}$ goes high.
2. In Single Device Mode, SO will not tri-state except after Reset. It will retain the last valid data.

Figure 6. Empty Boundary Condition Timing



NOTE:
1. Single Device Mode will not tri-state but will retain the last valid data.

Figure 7. Full Boundary Condition Timing

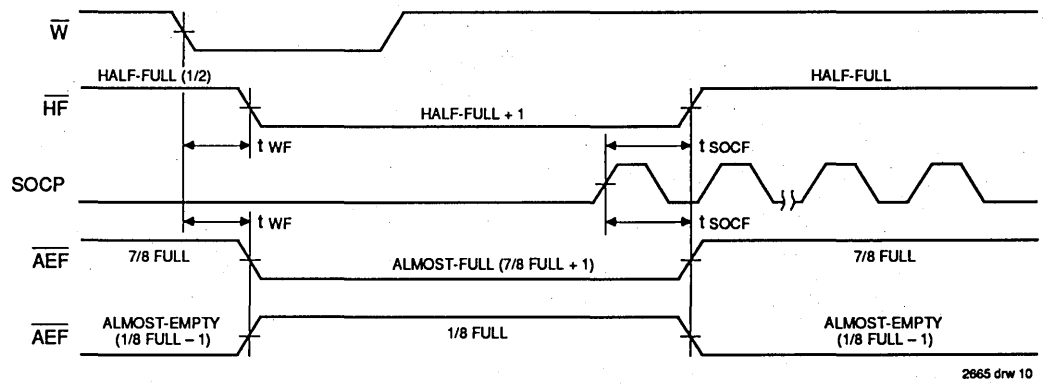


Figure 8. Half-Full, Almost-Full and Almost-Empty Timings

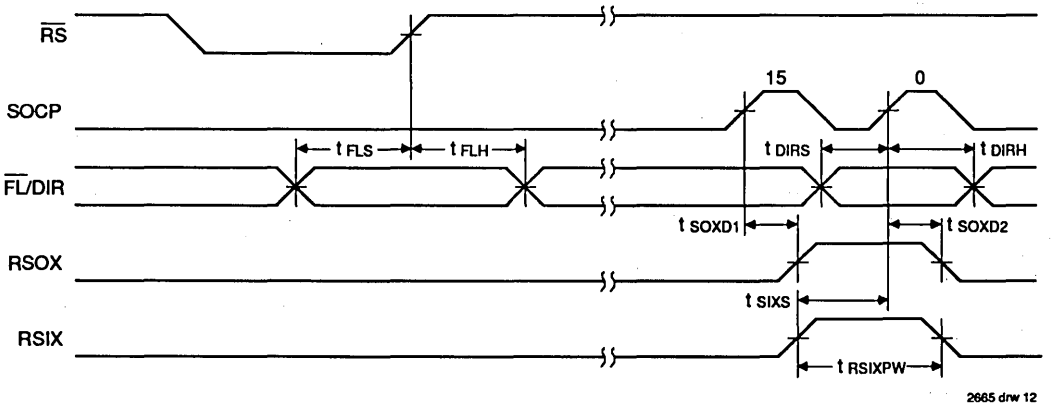


Figure 9. Serial Read Expansion

OPERATING CONFIGURATIONS

Single Device Mode

The device must be reset before beginning operation so that all flags are set to location zero. In the standalone case, the RSIX line is tied HIGH and indicates single device operation to the device. The RSOX/$\overline{AEF}$ pin defaults to $\overline{AEF}$ and outputs the Almost-Empty and Almost-Full Flag.

Width Expansion Mode

In the cascaded case, word widths of more than 16 bits can be achieved by using more than one device. By tying the RSOX and RSIX pins together, as shown in Figure 11, and programming which is the Least Significant Device, a cascaded serial word is achieved. The Least Significant Device

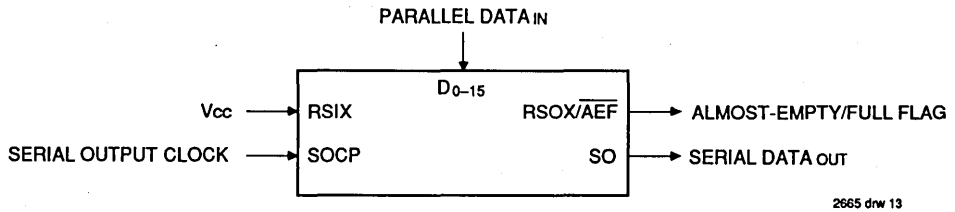


Figure 10. Single Device Configuration

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}$	DIR	Read Pointer	Write Pointer	$\overline{AEF}$, $\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	X	Location Zero	Location Zero	0	1	1
Read/Write	1	X	0,1	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will increment if appropriate flag is HIGH.

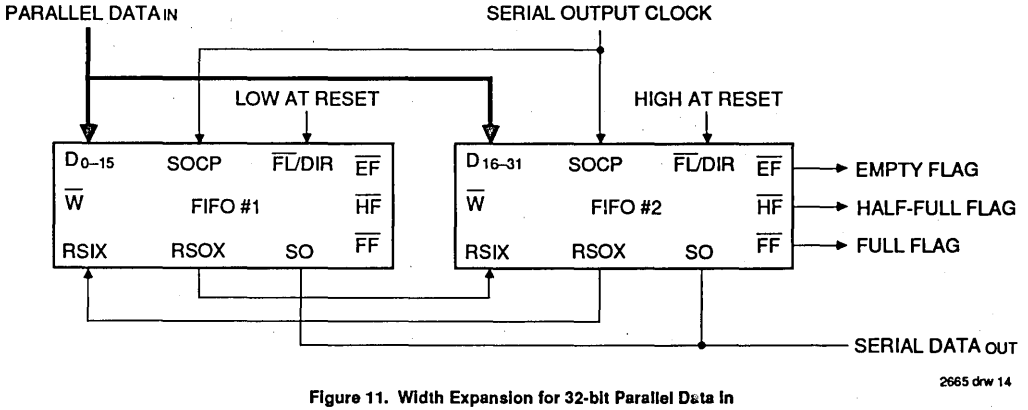
2665 tbl 09

Table 1. Reset and First Load Truth Table–Single Device Configuration

is programmed by a LOW on the $\overline{FL}$/DIR pin during reset. All other devices should be programmed HIGH on the $\overline{FL}$/DIR pin at reset.

The Serial Data Output (SO) of each device in the serial word must be tied together. Since the SO pin is three stated, only the device which is currently shifting out is enabled and driving the 1-bit bus. NOTE: After reset, the level on the $\overline{FL}$/DIR pin decides if the Least Significant or Most Significant Bit is read first out of each device.

The three flag outputs, Empty ($\overline{EF}$), Half-Full ($\overline{HF}$) and Full ($\overline{FF}$), should be taken from the Most Significant Device (in the example, FIFO #2). The Almost-Empty and Almost-Full Flags are not available due to using the RSOX pin for expansion.



2665 drw 14

Figure 11. Width Expansion for 32-bit Parallel Data In

Depth Expansion (Daisy Chain) Mode

The IDT72105/15/25 can easily be adapted to applications where the requirements are for greater than 1024 words. Figure 12 demonstrates Depth Expansion using three IDT72105/15/25s and an IDT74FCT138 Address Decoder. Any depth can be attained by adding additional devices. The Address Decoder is necessary to determine which FIFO to write data into. A byte of data should be written sequentially into each FIFO so that the RSOX/RSIX handshake can control reading out the data in the correct sequence. The IDT72105/15/25 operates in the Depth Expansion Mode when the following conditions are met:

1. The first device must be designated by programming $\overline{FL}$ LOW at Reset. All other devices to be programmed HIGH.
2. The Read Serial Out Expansion (RSOX) of each device must be tied to the Read Serial In Expansion (RSIX of the next device in the manner shown).
3. External logic is needed to generate composite Empty, Half-Full and Full Flags. This requires the OR-ing of all $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ Flags.
4. The Almost-Empty and Almost-Full Flag is not available due to using the RSOX pin for expansion.

Compound Expansion (Daisy Chain) Mode

The IDT72105/15/25 can be expanded in both depth and width as Figure 13 indicates:

1. The RSOX-to-RSIX expansion signals are wrapped around sequentially.
2. The write ($\overline{W}$) signal is expanded in width.
3. Flag signals are only taken from the Most Significant Devices.
4. The Least Significant Device in the array must be programmed with a LOW on $\overline{FL}$/DIR during reset.

6

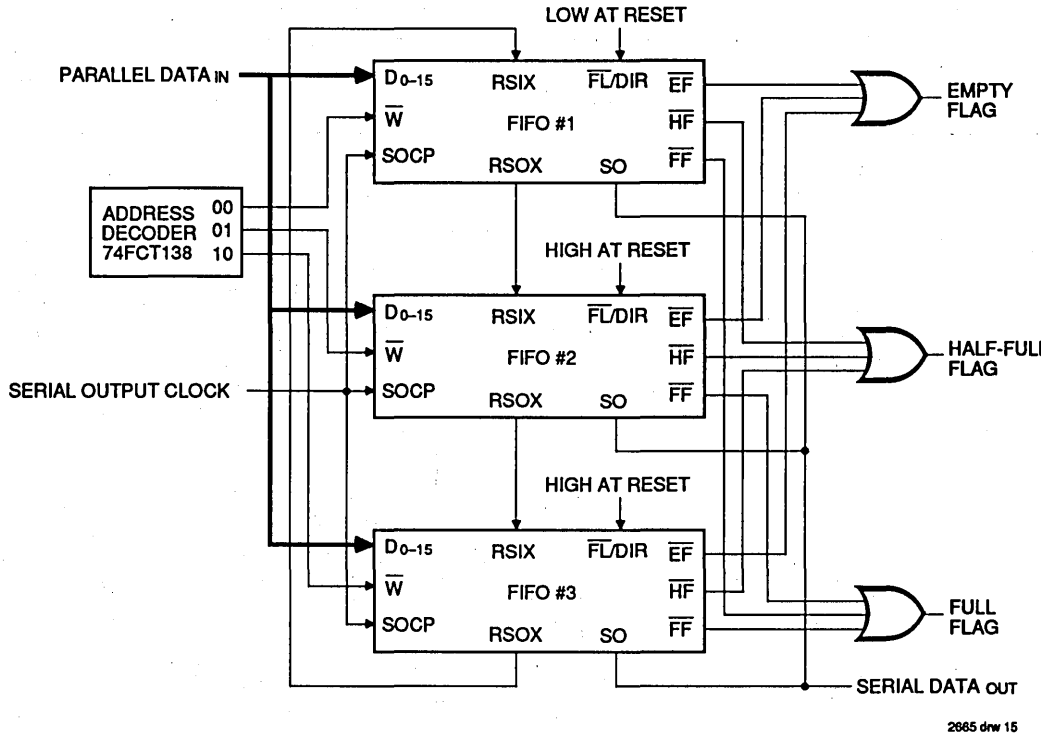


Figure 12. A 3K x 16 Parallel-to-Serial FIFO using the IDT72125

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	DIR	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{HF}$, $\overline{FF}$
Reset-First Device	0	0	X	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	X	Location Zero	Location Zero	0	1
Read/Write	1	X	0,1	X	X	X	X

NOTE: 2665 tbl 10
1. $\overline{RS}$ = Reset Input, $\overline{FL}$/FIR = First Load/Direction, $\overline{EF}$ = Empty Flag Output, $\overline{HF}$ = Half- Full Flag Output, $\overline{FF}$ = Full Flag Output.

Table 2. Reset and First Load Truth Table–Width/Depth Compound Expansion Mode

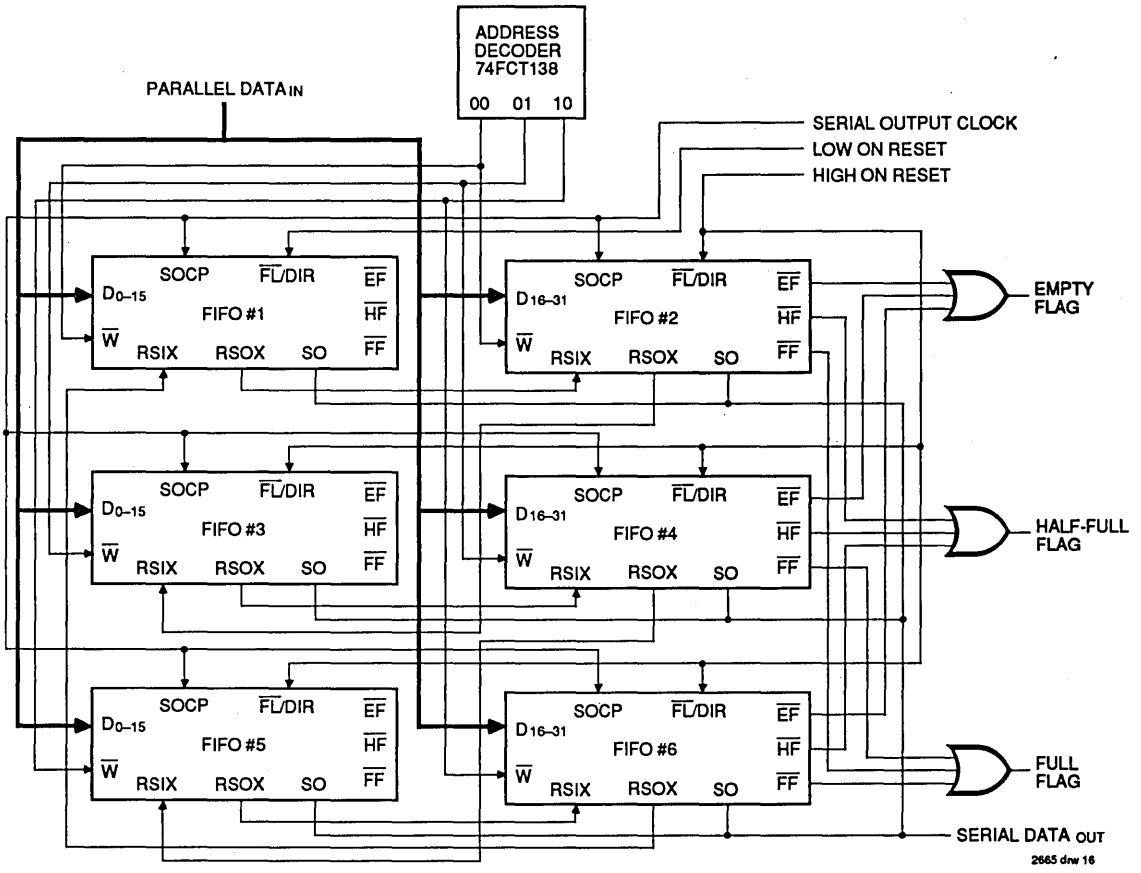
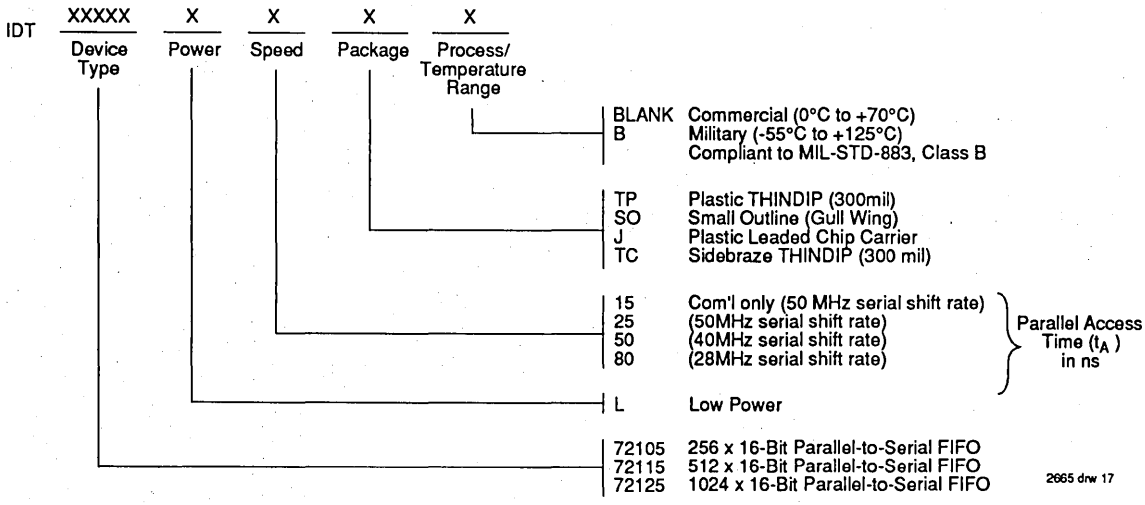


Figure 13. A 3K x 32 Parallel-to-Serial FIFO using the IDT72125

6

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS PARALLEL-TO-SERIAL FIFO 2048 x 9-BIT & 4096 x 9-BIT

IDT72131
IDT72141

FEATURES:

- 35ns parallel port access time, 45ns cycle time
- 50MHz serial port shift rate
- Expandable in depth and width with no external components
- Programmable word lengths including 7-9, 16-18, 32-36 bit using Flexishift™ serial output without using any additional components
- Multiple status flags: Full, Almost-Full (1/8 from full), Half-Full, Almost Empty (1/8 from empty), and Empty
- Asynchronous and simultaneous read and write operations
- Dual-port zero fall-through architecture
- Retransmit capability in single device mode
- Produced with high-performance, low power CEMOS™ technology
- Available in 28-pin ceramic and plastic DIP packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

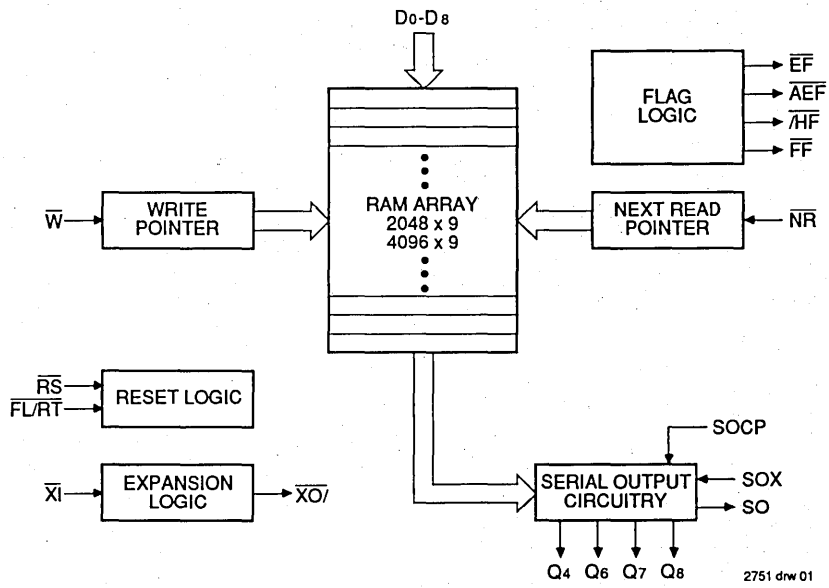
The IDT72131/72141 are high-speed, low power parallel-to-serial FIFOs. These FIFOs are ideally suited to serial communications applications, tape/disk controllers, and local area networks (LANs). The IDT72131/72141 can be configured with the IDTs serial-to-parallel FIFOs (IDT72132/72142) for bidirectional serial data buffering.

The FIFO has a 9-bit parallel input port and a serial output port. Wider and deeper parallel-to-serial data buffers can be built using multiple IDT72131/72141 chips. IDTs unique Flexishift serial expansion logic (SOX, $\overline{NR}$) makes width expansion possible with no additional components. These FIFOs will expand to a variety of word widths including 8, 9, 16, and 32 bits. The IDT72131/141 can also be directly connected for depth expansion.

Five flags are provided to monitor the FIFO. The full and empty flags prevent any FIFO data overflow or underflow conditions. The almost-full (7/8), half-full, and almost empty (1/8) flags signal memory utilization within the FIFO.

The IDT72131/72141 is fabricated using IDTs high-speed submicron CEMOS technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



CEMOS and Flexishift are trademarks of Integrated Device Technology, Inc.

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D_0–D_8	Inputs	I	Data inputs for 9-bit wide data.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{HF}$ and $\overline{FF}$ go high, and $\overline{AEF}$ and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up. $\overline{W}$ must be high and SOCP must be low during $\overline{RS}$ cycle.
$\overline{W}$	Write	I	A write cycle is initiated on the falling edge of WRITE if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of WRITE. Data is stored in the RAM array sequentially and independently of any ongoing read operation.
SOCP	Serial Output Clock	I	A serial bit read cycle is initiated on the rising edge of SOCP if the Empty Flag ($\overline{EF}$) is not set. In both Depth and Serial Word Width Expansion modes, all of the SOCP pins are tied together.
$\overline{NR}$	Next Read	I	To program the Serial Out data word width , connect $\overline{NR}$ with one of the Data Set pins (Q_4, Q_6, Q_7 and Q_8). For example, $\overline{NR}$ - Q_7 programs for a 8-bit Serial Out word width.
$\overline{FL/RT}$	First Load/ Retransmit	I	This is a dual purpose input. In the single device configuration ($\overline{XI}$ grounded), activating retransmit ($\overline{FL/RT}$-low) will set the internal READ pointer to the first location. There is no effect on the WRITE pointer. $\overline{W}$ must be high and SOCP must be low before setting $\overline{FL/RT}$ low. Retransmit is not compatible with depth expansion. In the depth expansion configuration, $\overline{FL/RT}$ grounded indicates the first activated device.
$\overline{XI}$	Expansion In	I	In the single device configuration, $\overline{XI}$ is grounded. In depth expansion or daisy chain expansion, $\overline{XI}$ is connected to $\overline{XO}$ (expansion out) of the previous device.
SOX	Serial Output Expansion	I	In the Serial Output Expansion mode, the SOX pin of the least significant device is tied high. The SOX pin of all other devices is connected to the Q_8 pin of the previous device. Data is then clocked out least significant bit first. For single device operation, SOX is tied high.
SO	Serial Output	O	Serial data is output on the Serial Output (SO) pin. Data is clocked out Least Significant Bit first. In the Serial Width Expansion mode the SO pins are tied together and each SO pin is tristated at the end of the byte.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ goes low, the device is full and further WRITE operations are inhibited. When $\overline{FF}$ is high, the device is not full.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ goes low, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is high, the device is not empty.
$\overline{AEF}$	Almost-Empty/ Almost-Full Flag	O	When $\overline{AEF}$ is low, the device is empty to 1/8 full or 7/8 to completely full. When $\overline{AEF}$ is high, the device is greater than 1/8 full, but less than 7/8 full.
$\overline{XO/HF}$	Expansion Out/ Half-Full Flag	O	This is a dual-purpose output. In the single device configuration ($\overline{XI}$ grounded), the device is more than half full when HF is low. In the depth expansion configuration ($\overline{XO}$ connected to $\overline{XI}$ of the next device), a pulse is sent from $\overline{XO}$ to $\overline{XI}$ when the last location in the RAM array is filled.
Q_4, Q_6, Q_7 and Q_8	Data Set	O	The appropriate Data Set pin (Q_4, Q_6, Q_7 and Q_8) is connected to $\overline{NR}$ to program the Serial Out data word width. For example: Q_6 - $\overline{NR}$ programs a 7-bit word width, Q_8 - $\overline{NR}$ programs a 9-bit word width, etc.
V_{CC}	Power Supply		Single Power Supply of 5V.
GND	Ground		Single ground at 0V.

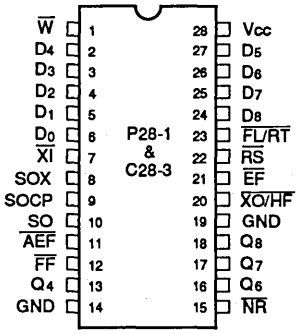
2751 tbl 01

STATUS FLAGS

Number of Words in FIFO					
IDT72131	IDT72141	$\overline{FF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF}$
0	0	H	L	H	L
1-255	1-511	H	L	H	H
256-1024	512-2048	H	H	H	H
1025-1792	2049-3584	H	H	L	H
1793-2047	3585-4095	H	L	L	H
2048	4096	L	L	L	H

2751 tbl 02

PIN CONFIGURATION



DIP
TOP VIEW

2751 drw 02

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}[1]	Input Low Voltage	—	—	0.8	V

NOTE: 2751 tbl 05
1. 1.5V undershoots are allowed for 10ns once per cycle.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2751 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2751 tbl 04
1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	IDT72131/IDT72141 Commercial			IDT72131/IDT72141 Military			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{IL}[1]	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	µA
I_{OL}[2]	Output Leakage Current	-10	—	10	-10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OUT} = -8mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 16mA	—	—	0.4	—	—	0.4	V
I_{CC1}[3]	Power Supply Current	—	90	140	—	100	160	mA
I_{CC2}[3]	Average Standby Current ($\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH}) (SOCP = V_{IL})	—	8	12	—	12	25	mA
$I_{CC3(L)}$[3,4]	Power Down Current	—	—	2	—	—	4	mA
$I_{CC3(S)}$[3,4]	Power Down Current	—	—	8	—	—	12	mA

NOTES: 2751 tbl 06
1. Measurements with 0.4 ≤ V_{IN} ≤ V_{OUT}.
2. SOCP ≤ V_{IL}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Icc measurements are made with outputs open.
4. $\overline{RS}$ = $\overline{FL/RT}$ = $\overline{W}$ = Vcc -0.2V; SOCP ≤ 0.2V; all other inputs ≥ Vcc -0.2V or ≤ 0.2V.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)

		Commercial		Military		Mil. and Com'l.		
		IDT72131x35 IDT72141x35		IDT72131x40 IDT72141x40		IDT72131x50 IDT72141x50		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_S	Parallel Shift Frequency	—	22.2	—	20	—	15	MHz
t_{SOCP}	Serial-Out Shift Frequency	—	50	—	50	—	40	MHz
PARALLEL INPUT TIMINGS								
t_{DS}	Data Set-up Time	18	—	20	—	30	—	ns
t_{DH}	Data Hold Time	0	—	0	—	5	—	ns
t_{WC}	Write Cycle Time	45	—	50	—	65	—	ns
t_{WPW}	Write Pulse Width	35	—	40	—	50	—	ns
t_{WR}	Write Recovery Time	10	—	10	—	15	—	ns
t_{WEF}	Write High to $\overline{EF}$ High	—	30	—	35	—	45	ns
t_{WFF}	Write Low to $\overline{FF}$ Low	—	30	—	35	—	45	ns
t_{WF}	Write Low to Transitioning $\overline{HF}$, $\overline{AEF}$	—	45	—	50	—	65	ns
t_{WPF}	Write Pulse Width After $\overline{FF}$ High	35	—	40	—	50	—	ns
SERIAL OUTPUT TIMINGS								
t_{SOHZ}	SOCP Rising Edge to SO at High Z[1]	5	16	5	16	5	26	ns
t_{SOLZ}	SOCP Rising Edge to SO at Low Z[1]	5	22	5	22	5	22	ns
t_{SOPD}	SOCP Rising Edge to Valid Data on SO	—	18	—	18	—	18	ns
t_{SOX}	SOX Set-up Time to SOCP Rising Edge	5	—	5	—	5	—	ns
t_{SOCW}	Serial In Clock Width High/Low	8	—	8	—	10	—	ns
t_{SOCEF}	SOCP Rising Edge (Bit 0 - Last Word) to $\overline{EF}$ Low	—	20	—	25	—	25	ns
t_{SOCFF}	SOCP Rising Edge to $\overline{FF}$ High	—	30	—	35	—	40	ns
t_{SOCF}	SOCP Rising Edge to $\overline{HF}$, $\overline{AEF}$, High	—	30	—	35	—	40	ns
t_{REFSO}	Recovery Time SOCP After $\overline{EF}$ High	35	—	40	—	50	—	ns
RESET TIMINGS								
t_{RSC}	Reset Cycle Time	45	—	50	—	65	—	ns
t_{RS}	Reset Pulse Width	35	—	40	—	50	—	ns
t_{RSS}	Reset Set-up Time	35	—	40	—	50	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	15	—	ns
t_{RSF1}	Reset to $\overline{EF}$ and $\overline{AEF}$ Low	—	45	—	50	—	65	ns
t_{RSF2}	Reset to $\overline{HF}$ and $\overline{FF}$ High	—	45	—	50	—	65	ns
t_{RSQL}	Reset to Q Low	20	—	20	—	35	—	ns
t_{RSQH}	Reset to Q High	20	—	20	—	35	—	ns
RETRANSMIT TIMINGS								
t_{RTC}	Retransmit Cycle Time	45	—	50	—	65	—	ns
t_{RT}	Retransmit Pulse Width	35	—	40	—	50	—	ns
t_{RTS}	Retransmit Set-up Time	35	—	40	—	50	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	10	—	15	—	ns
DEPTH EXPANSION MODE TIMINGS								
t_{XOL}	Read/Write to $\overline{XO}$ Low	—	35	—	40	—	50	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	—	35	—	40	—	50	ns
t_{XI}	$\overline{XI}$ Pulse Width	35	—	40	—	50	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	15	—	15	—	15	—	ns

NOTE:
1. Guaranteed by design minimum times, not tested.

2751 tbl 07

AC ELECTRICAL CHARACTERISTICS (Continued)

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	Military and Commercial						Unit
		IDT72131x65 IDT72141x65		IDT72131x80 IDT72141x80		IDT72131x120 IDT72141x120		
		Min.	Max.	Min.	Max.	Min.	Max.	
tS	Parallel Shift Frequency	—	12.5	—	10	—	7	MHz
tSOCP	Serial-Out Shift Frequency	—	33	—	28	—	25	MHz
PARALLEL INPUT TIMINGS								
tDS	Data Set-up Time	30	—	40	—	40	—	ns
tDH	Data Hold Time	10	—	10	—	10	—	ns
tWC	Write Cycle Time	80	—	100	—	140	—	ns
tWPW	Write Pulse Width	65	—	80	—	120	—	ns
tWR	Write Recovery Time	15	—	20	—	20	—	ns
tWEF	Write High to $\overline{EF}$ High	—	60	—	60	—	60	ns
tWFF	Write Low to $\overline{FF}$ Low	—	60	—	60	—	60	ns
tWF	Write Low to Transitioning $\overline{HF}$, $\overline{AEF}$	—	80	—	100	—	140	ns
tWPF	Write Pulse Width After $\overline{FF}$ High	65	—	80	—	120	—	ns
SERIAL OUTPUT TIMINGS								
tSOHZ	SOCP Rising Edge to SO at High Z[1]	5	20	5	25	5	35	ns
tSOLZ	SOCP Rising Edge to SO at Low Z[1]	5	22	5	30	5	35	ns
tSOPD	SOCP Rising Edge to Valid Data on SO	—	22	—	30	—	35	ns
tSOX	SOX Set-up Time to SOCP Rising Edge	5	—	5	—	5	—	ns
tSOCW	Serial In Clock Width High/Low	10	—	15	—	15	—	ns
tSOCEF	SOCP Rising Edge (Bit 0 - Last Word) to $\overline{EF}$ Low	—	30	—	30	—	30	ns
tSOCFF	SOCP Rising Edge to $\overline{FF}$ High	—	50	—	60	—	65	ns
tSOCF	SOCP Rising Edge to $\overline{HF}$, $\overline{AEF}$, High	—	50	—	60	—	65	ns
tREFSO	Recovery Time SOCP After $\overline{EF}$ High	65	—	80	—	120	—	ns
RESET TIMINGS								
tRSC	Reset Cycle Time	80	—	100	—	140	—	ns
tRS	Reset Pulse Width	65	—	80	—	120	—	ns
tRSS	Reset Set-up Time	65	—	80	—	120	—	ns
tRSR	Reset Recovery Time	15	—	20	—	20	—	ns
tRSF1	Reset to $\overline{EF}$ and $\overline{AEF}$ Low	—	80	—	100	—	140	ns
tRSF2	Reset to $\overline{HF}$ and $\overline{FF}$ High	—	80	—	100	—	140	ns
tRSQL	Reset to Q Low	50	—	65	—	105	—	ns
tRSQH	Reset to Q High	50	—	65	—	105	—	ns
RETRANSMIT TIMINGS								
tRTC	Retransmit Cycle Time	80	—	100	—	140	—	ns
tRT	Retransmit Pulse Width	65	—	80	—	120	—	ns
tRTS	Retransmit Set-up Time	65	—	80	—	120	—	ns
tRTR	Retransmit Recovery Time	15	—	20	—	20	—	ns
DEPTH EXPANSION MODE TIMINGS								
tXOL	Read/Write to $\overline{XO}$ Low	—	65	—	80	—	120	ns
tXOH	Read/Write to $\overline{XO}$ High	—	65	—	80	—	120	ns
tXI	$\overline{XI}$ Pulse Width	65	—	80	—	120	—	ns
tXIR	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	ns
tXIS	$\overline{XI}$ Set-up Time	15	—	15	—	15	—	ns

NOTE:
1. Guaranteed by design minimum times, not tested.

2751 tbl 08

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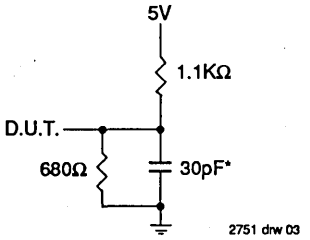
AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure A

2751 tbl 09



or equivalent circuit

Figure A. Ouput Load

*Including jig and scope capacitances

FUNCTIONAL DESCRIPTION

Parallel Data Input

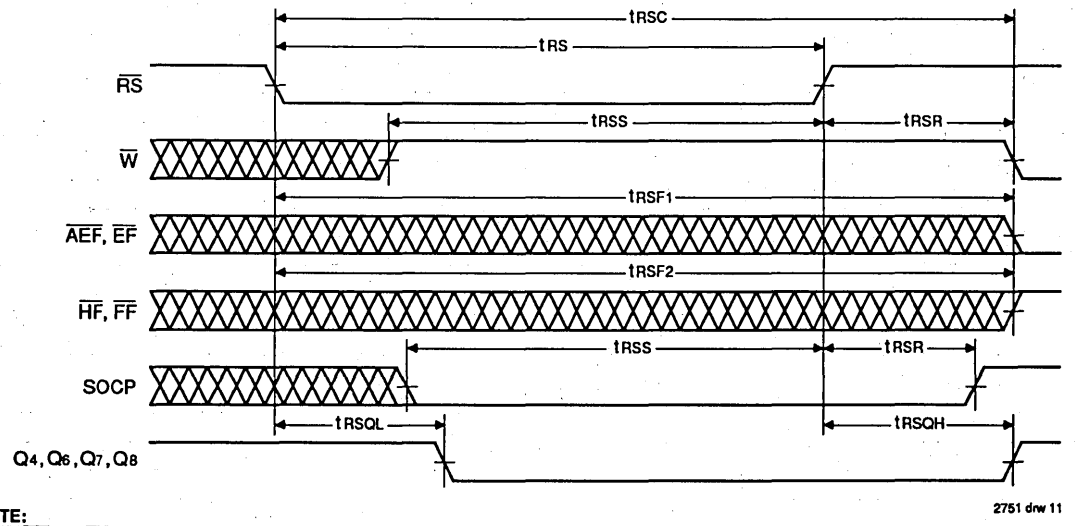
The data is written into the FIFO in parallel through the D_{0-8} input data lines. A write cycle is initiated on the falling edge of the Write ($\overline{W}$) signal provided the Full Flag ($\overline{FF}$) is not asserted. If the $\overline{W}$ signal changes from HIGH-to-LOW and the Full-Flag ($\overline{FF}$) is already set, the write line is inhibited internally from incrementing the write pointer and no write operation occurs.

Data set-up and hold times must be met with respect to the rising edge of Write. The data is written to the RAM at the write pointer. On the rising edge of $\overline{W}$, the write pointer is incremented. Write operations can occur simultaneously or asynchronously with read operations.

Serial Data Output

The serial data is output on the SO pin. The data is clocked out on the rising edge of SOCP providing the Empty Flag ($\overline{EF}$) is not asserted. If the Empty Flag is asserted then the next data word is inhibited from moving to the output register and being clocked out by SOCP. NOTE: SOCP should not be clocked while the Empty Flag is low. If it is, then two things will occur. One, invalid data will be read by SOCP and two, SOCP will be out of sync with Next Read ($\overline{NR}$).

The serial word is shifted out Least Significant Bit first, that is the first bit will be D0, then D1 and so on up to the serial word width. The serial word width must be programmed by connecting the appropriate Data Set line (Q4, Q6, Q7 or Q8) to the $\overline{NR}$ input. The Data Set lines are taps off a digital delay line. Selecting one of these taps, programs the width of the serial word to be read and shifted out.



NOTE:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Reset, but flags will be valid at t_{RSC}.

Figure 1. Reset

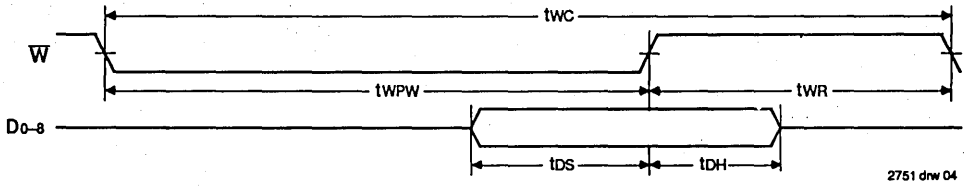


Figure 2. Write Operation

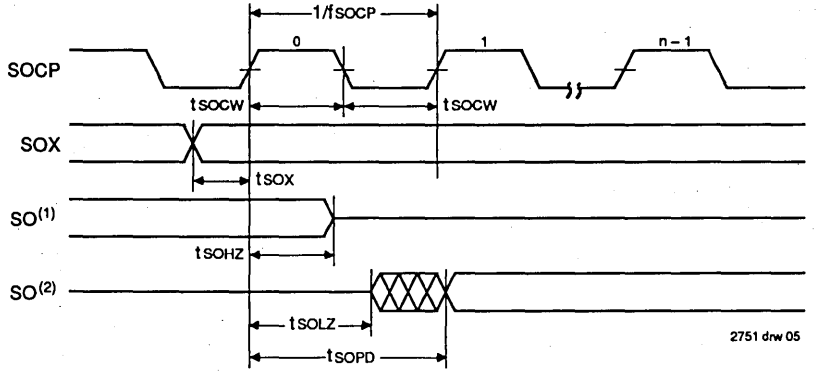


Figure 3. Read Operation

NOTES:
1. This timing applies to the Active Device in Width Expansion Mode.
2. This timing applies to Single Device Mode at Empty Boundary ($\overline{EF}$ = low) and the Next Active Device in Width Expansion Mode.

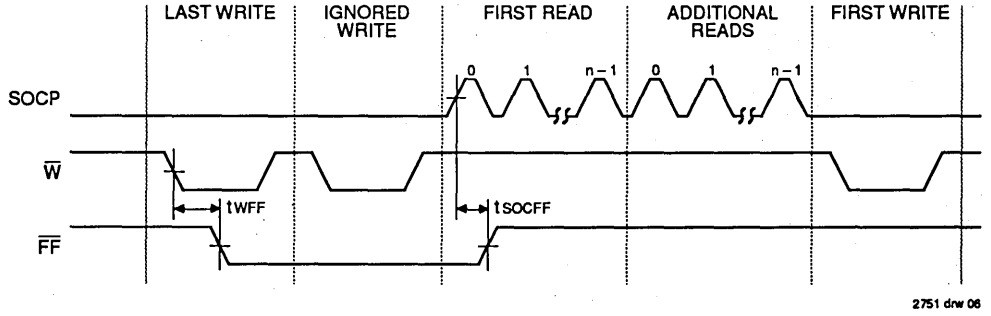
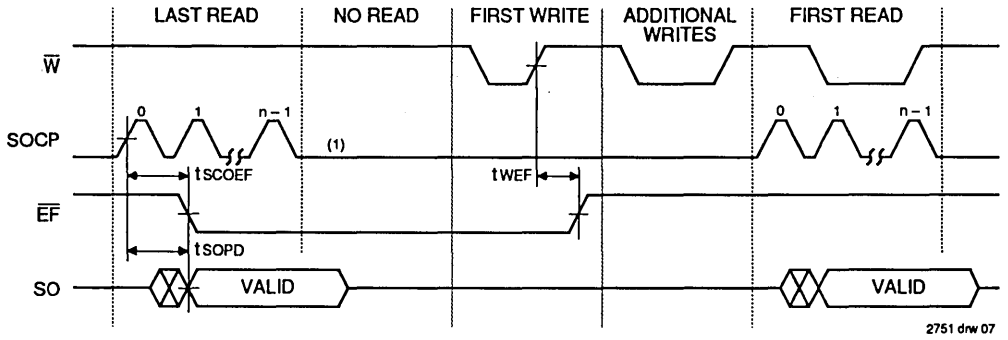
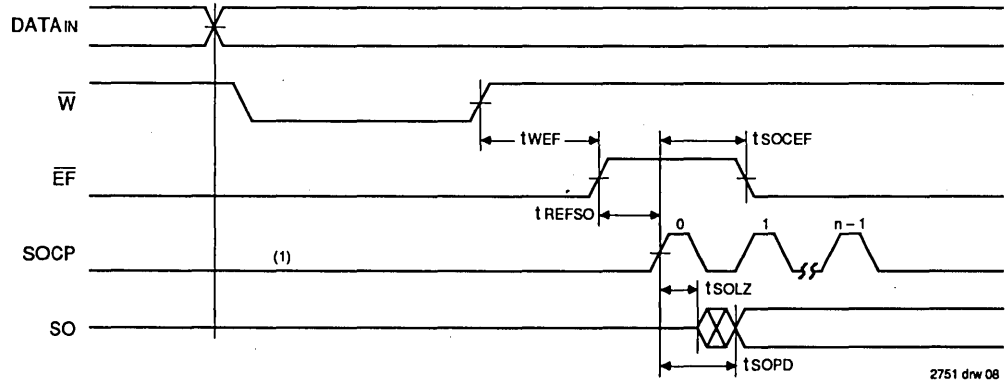


Figure 4. Full Flag from Last Write to First Read



NOTE:
1. SOCP should not be clocked until $\overline{EF}$ goes high.

Figure 5. Empty Flag from Last Read to First Write



NOTE:
1. SOCP should not be clocked until $\overline{EF}$ goes high.

Figure 6. Empty Boundary Condition Timing

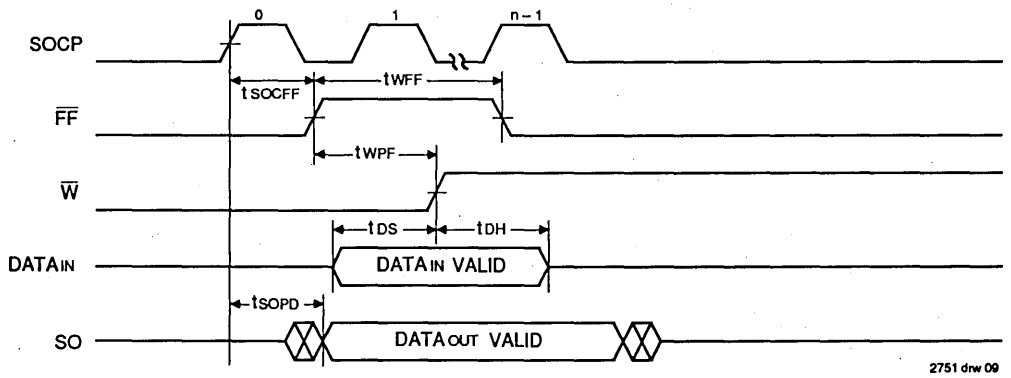


Figure 7. Full Boundry Condition Timing

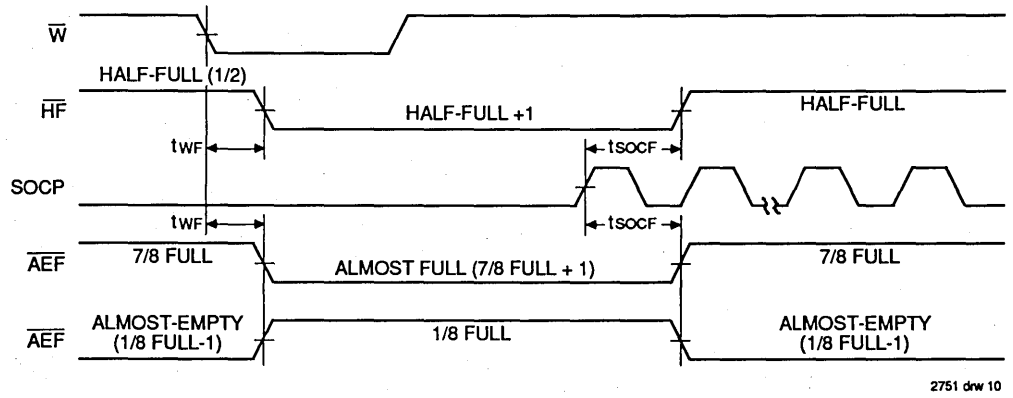
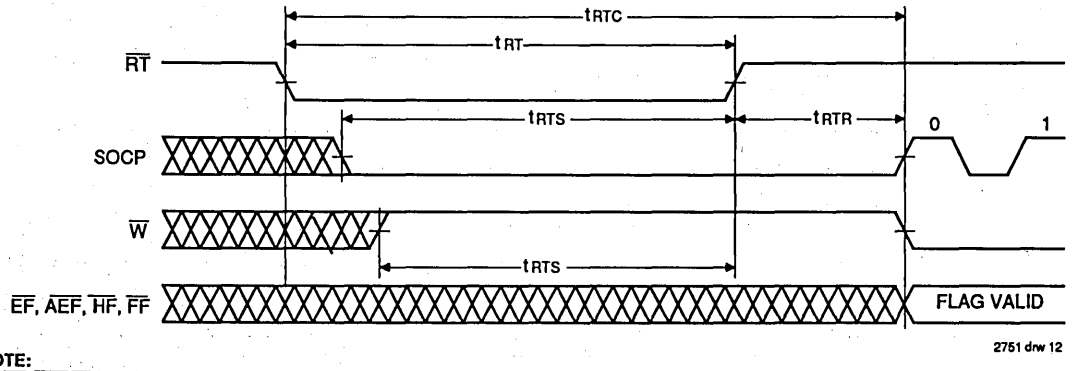


Figure 8. Half Full, Almost Full and Almost Empty Timings

6



NOTE:
1. EF, AEF, HF and FF may change status during Retransmit, but flags will be valid at tRTC.

Figure 9. Retransmit

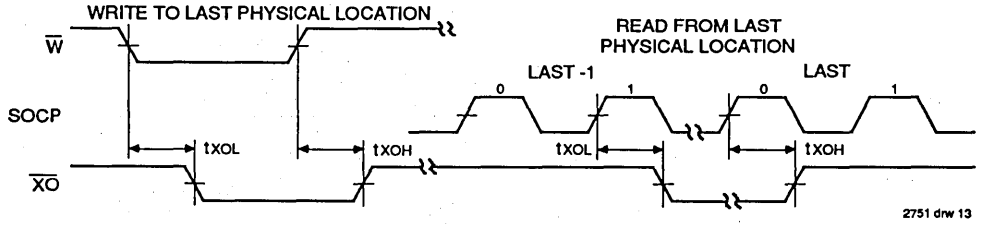


Figure 10. Expansion-Out

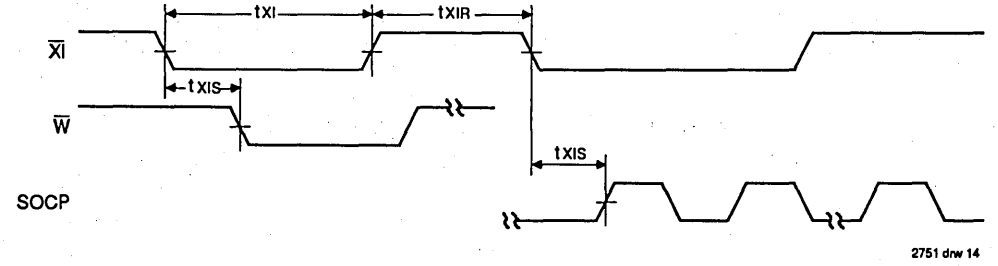


Figure 11. Expansion-In

OPERATING CONFIGURATIONS

Single Device Configuration

In the standalone case, the SOX line is tied HIGH and not used. On the first LOW-to-HIGH of the SOCP clock, all of the Data Set lines (Q4, Q8) go low and a new serial word is started. The Data Set lines then go high on the equivalent SOCP clock pulse. This continues until the Q line connected to $\overline{NR}$ goes high completing the serial word. The cycle is then repeated with the next LOW-to-HIGH transition of SOCP.

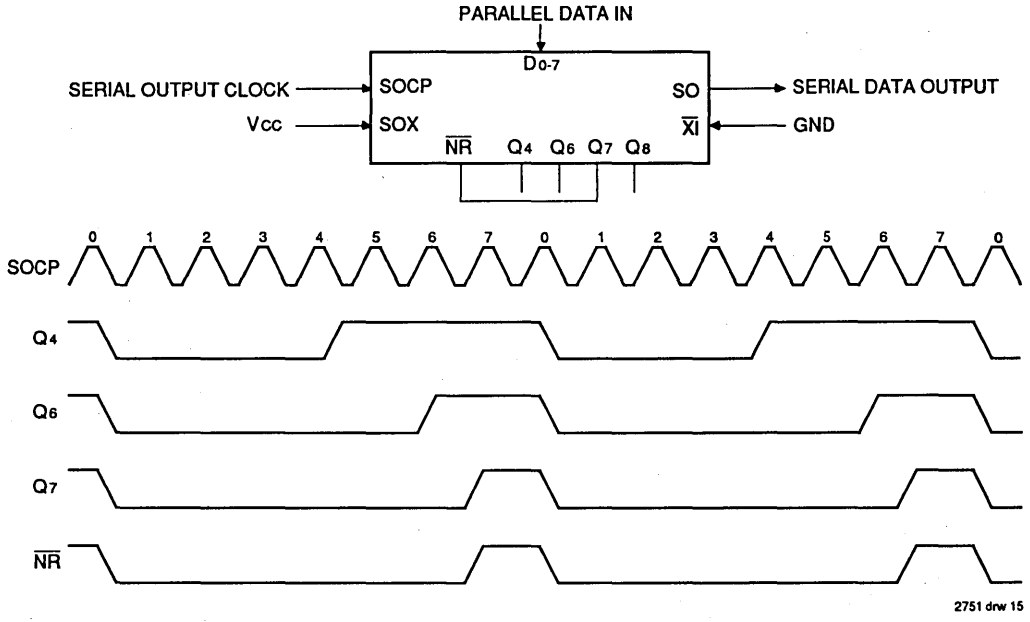


Figure 12. Eight-Bit Word Single Device Configuration

6

TRUTH TABLES

TABLE 1: RESET AND RETRANSMIT — SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{AEF}$, $\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment[1]	Increment[1]	X	X	X

NOTE:
1. Pointer will increment if appropriate flag is HIGH.

Width Expansion Configuration

In the cascaded case, word widths of more than 9 bits can be achieved by using more than one device. By tying the SOX line of the least significant device HIGH and the SOX of the subsequent devices to the appropriate Data Set lines of the previous devices, a cascaded serial word is achieved.

On the first LOW-to-HIGH clock edge of SOCP, all lines go LOW. Just as in the standalone case, on each corresponding clock cycle, the equivalent Data Set line goes HIGH in order of least to most significant. When the Data Set line which is connected to the SOX input of the next device goes HIGH, the Do of that device goes HIGH, the cascading from one device to the next. The Data Set line of the most significant bit programs the serial word width by being connected to all NR inputs.

The Serial Data Output (SO) of each device in the serial word must be tied together. Since the SO pin is three stated, only the device which is currently shifting out is enabled and driving the 1-bit-bus.

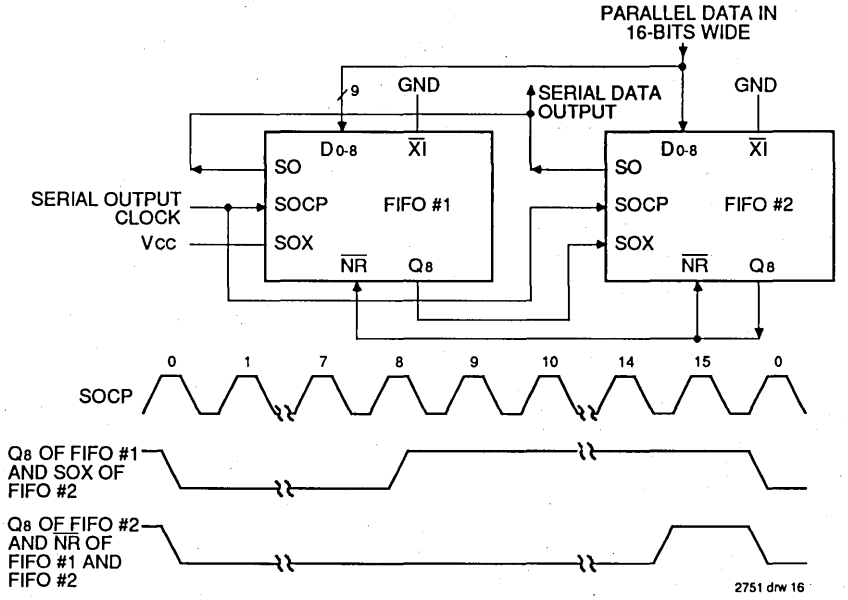


Figure 13. Width Wxpansion for 16-bit Parallel Data In. The Parallel Data In is tied to Do-8 of FIFO #1 and Do-8 of FIFO #2.

Depth Expansion (Daisy Chain) Mode

The IDT72131/41 can be easily adapted to applications where the requirements are for greater than 2048/4096 words. Figure 14 demonstrates Depth Expansion using three IDT72131/41. Any depth can be attained by adding additional IDT72131/41 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the OR-ing of all $\overline{EF}$s and OR-ing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion mode.

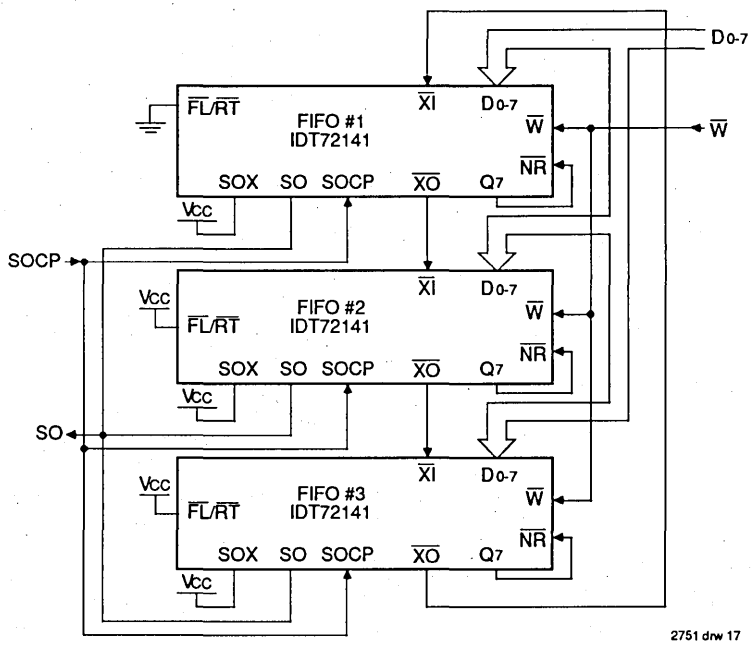


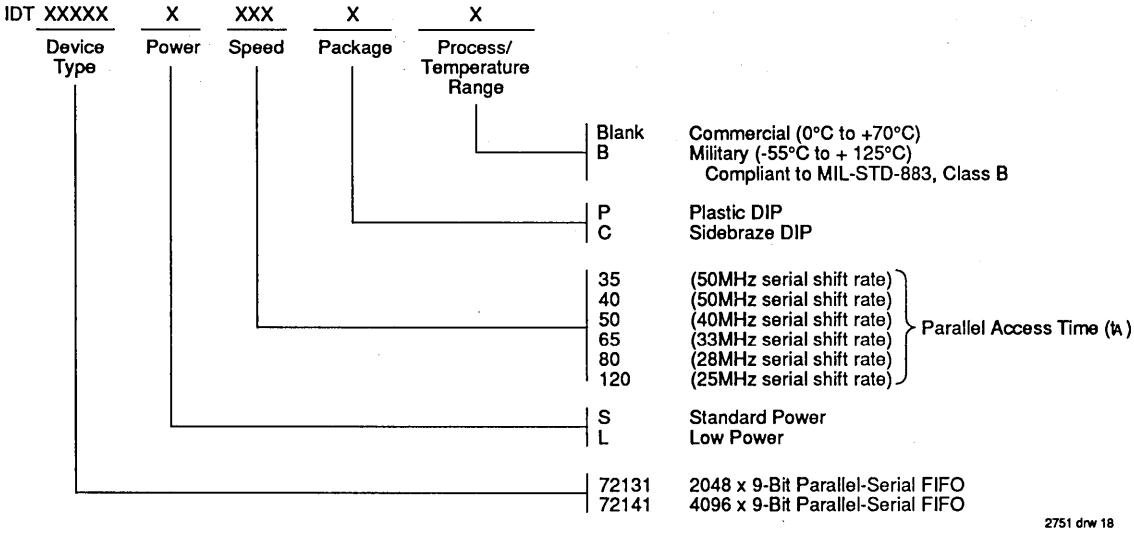
Figure 14. A 12K x 8 Parallel-In Serial-Out FIFO

TABLE 2: RESET AND FIRST LOAD TRUTH TABLE — DEPTH EXPANSION/COMPOUND EXPANSION MODE

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Retransmit all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device.
2. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Ouput, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input.

ORDERING INFORMATION



2751 drw 18

Integrated Device Technology, Inc.

CMOS SERIAL-TO-PARALLEL FIFO 2048 x 9-BIT 4096 X 9-BIT

IDT72132
IDT72142

FEATURES:

- 35ns parallel port access time, 45ns cycle time
- 50MHz serial port shift rate
- Expandable in depth and width with no external components
- Programmable word lengths including 8, 9, 16-18, and 32-36 bit using Flexshift™ serial input without using any additional components
- Multiple status flags: Full, Almost-Full (1/8 from full), Half-Full, Almost Empty (1/8 from empty), and Empty
- Asynchronous and simultaneous read and write operations
- Dual-port zero fall-through architecture
- Retransmit capability in single device mode
- Produced with high-performance, low-power CEMOS™ technology
- Available in a 28-pin ceramic and plastic DIP packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

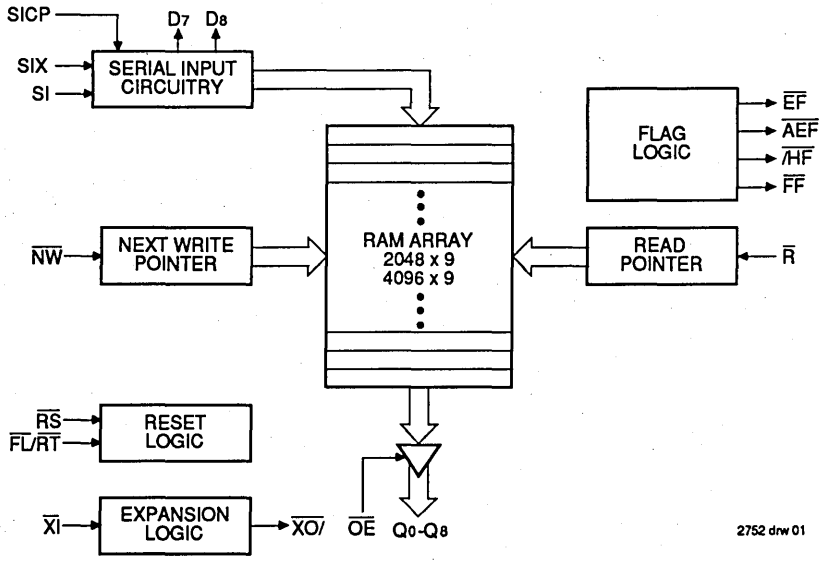
The IDT72132/72142 are high-speed, low-power serial-to-parallel FIFOs. These FIFOs are ideally suited to serial communications applications, tape/disk controllers, and local area networks (LANs). The IDT72132/72142 can be configured with the IDTs parallel-to-serial FIFOs (IDT72131/72141) for bidirectional serial data buffering.

The FIFO has a serial input port and a 9-bit parallel output port. Wider and deeper serial-to-parallel data buffers can be built using multiple IDT72132/72142 chips. IDTs unique Flexshift serial expansion logic (SIX, $\overline{NW}$) makes width expansion possible with no additional components. These FIFOs will expand to a variety of word widths including 8, 9, 16, and 32 bits. The IDT72132/142 can also be directly connected for depth expansion.

Five flags are provided to monitor the FIFO. The full and empty flags prevent any FIFO data overflow or underflow conditions. The Almost-Full (7/8), Half-Full, and Almost Empty (1/8) flags signal memory utilization within the FIFO.

The IDT72132/72142 is fabricated using IDTs high-speed submicron CEMOS technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



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CEMOS and Flexishift are trademarks of Integrated Device Technology, Inc.

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
SI	Serial Input	I	Serial data is shifted in least significant bit first. In the serial cascade mode, the Serial Input (SI) pins are tied together and SIX plus D_7, D_8 determine which device stores the data.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{HF}$ and $\overline{FF}$ go high, and $\overline{AEF}$, and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up. $\overline{R}$ must be high during an $\overline{RS}$ cycle.
$\overline{NW}$	Next Write	I	To program the Serial In word width , connect $\overline{NW}$ with one of the Data Set pins (D_7, D_8).
SICP	Serial Input Clock	I	Serial data is read into the serial input register on the rising edge of SICP. In both Depth and Serial Word Width Expansion modes, all of the SICP pins are tied together.
$\overline{R}$	Read	I	When READ is low, data can be read from the RAM array sequentially, independent of SICP. In order for READ to be active, $\overline{EF}$ must be high. When the FIFO is empty ($\overline{EF}$-low), the internal READ operation is blocked and Q_0-Q_8 are in a high impedance condition.
$\overline{FL/RT}$	First Load/ Retransmit	I	This is a dual purpose input. In the single device configuration ($\overline{XI}$ grounded), activating retransmit ($\overline{FL/RT}$-low) will set the internal READ pointer to the first location. There is no effect on the WRITE pointer. $\overline{R}$ must be high and SICP must be low before setting $\overline{FL/RT}$ low. Retransmit is not possible in depth expansion. In the depth expansion configuration, $\overline{FL/RT}$ grounded indicates the first activated device.
$\overline{XI}$	Expansion In	I	In the single device configuration, $\overline{XI}$ is grounded. In depth expansion or daisy chain expansion, $\overline{XI}$ is connected to $\overline{XO}$ (expansion out) of the previous device.
SIX	Serial Input Expansion	I	In the Expansion mode, the SIX pin of the least significant device is tied high. The SIX pin of all other devices is connected to the D_8 pin of the previous device. For single device operation, SIX is tied high.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is set low, the parallel output buffers receive data from the RAM array. When $\overline{OE}$ is set high, parallel three state buffers inhibit data flow.
Q_0–Q_8	Output Data	O	Data outputs for 9-bit wide data.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ goes low, the device is full and data must not be clocked by SICP. When $\overline{FF}$ is high, the device is not full.
$\overline{EF}$	Empty Flag Almost-Full Flag	O	When $\overline{EF}$ goes low, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is high, the device is not empty.
$\overline{AEF}$	Almost-Empty/ Half-Full Flag	O	When $\overline{AEF}$ is low, the device is empty to 1/8 full or 7/8 to completely full. When $\overline{AEF}$ is high, the device is greater than 1/8 full, but less than 7/8 full.
$\overline{XO/HF}$	Expansion Out/	O	This is a dual purpose output. In the single device configuration ($\overline{XI}$ grounded), the device is more than half full when $\overline{HF}$ is low. In the depth expansion configuration ($\overline{XO}$ connected to $\overline{XI}$ of the next device), a pulse is sent from $\overline{XO}$ to $\overline{XI}$ when the last location in the RAM array is filled.
D_7, D_8	Data Set	O	The appropriate Data Set pin (D_7, D_8) is connected to $\overline{NW}$ to program the Serial In data word width. For example: D_7 - $\overline{NW}$ programs a 8-bit word width, D_8 - $\overline{NW}$ programs a 9-bit word width, etc.
Vcc	Power Supply		Single Power Supply of 5V.
GND	Ground		Three grounds at 0V.

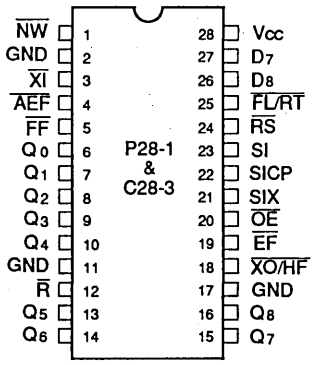
2752 tbl 01

STATUS FLAGS

Number of Words in FIFO					
IDT72132	IDT72142	$\overline{FF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF}$
0	0	H	L	H	L
1-255	1-511	H	L	H	H
256-1024	512-2048	H	H	H	H
1025-1792	2049-3584	H	H	L	H
1793-2047	3585-4095	H	L	L	H
2048	4096	L	L	L	H

2752 tbl 02

PIN CONFIGURATIONS



DIP
TOP VIEW
2752 drw 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage Commercial	2.0	—	—	V
VIH	Input High Voltage Military	2.2	—	—	V
VIL(1)	Input Low Voltage	—	—	0.8	V

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

2752 tbl 05

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2752 tbl 03

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	10	pF
COUT	Output Capacitance	VOUT = 0V	12	pF

NOTE:
1. This parameter is sampled and not 100% tested.

2752 tbl 04

DC ELECTRICAL CHARACTERISTICS

(Commercial: VCC = 5.0V ± 10%, TA = 0°C to +70°C; Military: VCC = 5.0V ± 10%, TA = -55°C to +125°C)

Symbol	Parameter	IDT72132/IDT72142 Commercial			IDT72132/IDT72142 Military			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
ILI(1)	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	µA
ILO(2)	Output Leakage Current	-10	—	10	-10	—	10	µA
VOH	Output Logic "1" Voltage, IOUT = -2mA	2.4	—	—	2.4	—	—	V
VOL	Output Logic "0" Voltage, IOUT = 8mA	—	—	0.4	—	—	0.4	V
ICC1(3)	Power Supply Current	—	90	140	—	100	160	mA
ICC2(3)	Average Standby Current ($\overline{R}$ = $\overline{RS}$ = $\overline{FL/RT}$ = VIH) (SICP = VIL)	—	8	12	—	12	25	mA
ICC3(L)(3,4)	Power Down Current	—	—	2	—	—	4	mA
ICC3(S)(3,4)	Power Down Current	—	—	8	—	—	12	mA

NOTES:
1. Measurements with 0.4 ≤ VIN ≤ VOUT.
2. $\overline{R}$ ≥ VIH, 0.4 ≤ VOUT ≤ VCC.
3. ICC measurements are made with outputs open.
4. $\overline{RS}$ = $\overline{FL/RT}$ = $\overline{R}$ = VCC -0.2V; SICP ≤ 0.2V; all other inputs ≥ VCC -0.2V or ≤ 0.2V.

2752 tbl 06

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AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)

		Commercial		Military		Mil. and Com'l.		
		IDT72132x35 IDT72142x35		IDT72132x40 IDT72142x40		IDT72132x50 IDT72142x50		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_S	Parallel Shift Frequency	—	22.2	—	20	—	15	MHz
t_{SICP}	Serial-InShift Frequency	—	50	—	50	—	40	MHz
PARALLEL OUTPUT TIMINGS								
t_A	Access Time	—	35	—	40	—	50	ns
t_{RR}	Read Recovery Time	10	—	10	—	15	—	ns
t_{RPW}	Read Pulse Width	35	—	40	—	50	—	ns
t_{RC}	Read Cycle Time	45	—	50	—	65	—	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z[1]	5	—	5	—	10	—	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z[1]	—	20	—	25	—	30	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	ns
t_{OEHZ}	Output Enable to High-Z (Disable)[1]	—	15	—	15	—	15	ns
t_{OELZ}	Output Enable to Low-Z (Enable)[1]	5	—	5	—	5	—	ns
t_{AOE}	Output Enable to Data Valid (Q_{0-8})	—	20	—	20	—	22	ns
SERIAL INPUT TIMINGS								
t_{SIS}	Serial Data in Set-Up Time to SICP Rising Edge	12	—	12	—	15	—	ns
t_{SIH}	Serial Data in Hold Time to SICP Rising Edge	0	—	0	—	0	—	ns
t_{SIX}	SIX Set-Up Time to SICP Rising Edge	5	—	5	—	5	—	ns
t_{SICW}	Serial-In Clock Width High/Low	8	—	8	—	10	—	ns
FLAG TIMINGS								
t_{SICEF}	SICP Rising Edge (Last Bit - First Word) to $\overline{EF}$ High	—	45	—	50	—	65	ns
t_{SICFF}	SICP Rising Edge (Bit 1 - Last Word) to $\overline{FF}$ Low	—	30	—	35	—	40	ns
t_{SICF}	SICP Rising Edge to $\overline{HF}$, $\overline{AEF}$	—	45	—	50	—	65	ns
t_{RFFSI}	Recovery Time SICP After $\overline{FF}$ Goes High	15	—	15	—	15	—	ns
t_{REF}	Read Low to $\overline{EF}$ Low	—	30	—	35	—	45	ns
t_{RFF}	Read High to $\overline{FF}$ High	—	30	—	35	—	45	ns
t_{RF}	Read High to Transitioning $\overline{HF}$ and $\overline{AEF}$	—	45	—	50	—	65	ns
t_{RPE}	Read Pulse Width After $\overline{EF}$ High	35	—	40	—	50	—	ns
RESET TIMINGS								
t_{RSC}	Reset Cycle Time	45	—	50	—	65	—	ns
t_{RS}	Reset Pulse Width	35	—	40	—	50	—	ns
t_{RSS}	Reset Set-up Time	35	—	40	—	50	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	15	—	ns
t_{RSF1}	Reset to $\overline{EF}$ and $\overline{AEF}$ Low	—	45	—	50	—	65	ns
t_{RSF2}	Reset to $\overline{HF}$ and $\overline{FF}$ High	—	45	—	50	—	65	ns
t_{RSDL}	Reset to D Low	20	—	20	—	35	—	ns
t_{POI}	SICP Rising Edge to D	5	17	5	17	5	20	ns
RETRANSMIT TIMINGS								
t_{RTC}	Retransmit Cycle Time	45	—	50	—	65	—	ns
t_{RT}	Retransmit Pulse Width	35	—	40	—	50	—	ns
t_{RTS}	Retransmit Set-up Time	35	—	40	—	50	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	10	—	15	—	ns
DEPTH EXPANSION MODE TIMINGS								
t_{XOL}	Read/Write to $\overline{XO}$ Low	—	40	—	45	—	50	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	—	40	—	45	—	50	ns
t_{XI}	$\overline{XI}$ Pulse Width	35	—	40	—	50	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	16	—	15	—	15	—	ns

NOTE:
1. Guaranteed by design minimum times, not tested

2752 tbl 07

AC ELECTRICAL CHARACTERISTICS (Continued)

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	Military and Commercial						Unit
		IDT72132x65 IDT72142x65		IDT72132x80 IDT72142x80		IDT72132x120 IDT72142x120		
		Min.	Max.	Min.	Max.	Min.	Max.	
tS	Parallel Shift Frequency	—	12.5	—	10	—	7	MHz
tSOCP	Serial-Out Shift Frequency	—	33	—	28	—	25	MHz
PARALLEL OUTPUT TIMINGS								
tA	Access Time	—	65	—	80	—	120	ns
tRR	Read Recovery Time	15	—	20	—	20	—	ns
tRPW	Read Pulse Width	65	—	80	—	120	—	ns
tRC	Read Cycle Time	80	—	100	—	140	—	ns
tRLZ	Read Pulse Low to Data Bus at Low Z[1]	10	—	10	—	10	—	ns
tRHZ	Read Pulse Highto Data Bus at High Z[1]	—	30	—	35	—	35	ns
tDV	Data Valid from Read Pulse High	5	—	5	—	5	—	ns
tOEHZ	Output Enable to High-Z (Disable)[1]	—	20	—	25	—	30	ns
tOELZ	Output Enable to Low-Z (Enable)[1]	5	—	5	—	5	—	ns
tAOE	Output Enable to Data Valid (Q_{0-8})	—	25	—	30	—	35	ns
SERIAL INPUT TIMINGS								
tSIS	Serial Data in Set-Up Time to SICP Rising Edge	15	—	20	—	20	—	ns
tSIH	Serial Data in Hold Time to SICP Rising Edge	0	—	5	—	5	—	ns
tSIX	SIX Set-Up Time to SICP Rising Edge	5	—	5	—	5	—	ns
tSICW	Serial-In Clock Width High/Low	10	—	15	—	15	—	ns
FLAG TIMINGS								
tSICEF	SICP Rising Edge (Last Bit - First Word) to $\overline{EF}$ High	—	80	—	80	—	80	ns
tSICFF	SICP Rising Edge (Bit 1 - Last Word) to $\overline{FF}$ Low	—	50	—	60	—	60	ns
tSICF	SICP Rising Edge to $\overline{HF}$, $\overline{AEF}$	—	80	—	80	—	80	ns
tRFFSI	Recovery Time SICP After $\overline{FF}$ Goes High	15	—	20	—	20	—	ns
tREF	Read Low to $\overline{EF}$ Low	—	60	—	60	—	60	ns
tRFF	Read High to $\overline{FF}$ High	—	60	—	60	—	60	ns
tRF	Read High to Transitioning $\overline{HF}$ and $\overline{AEF}$	—	80	—	100	—	140	ns
tRPE	Read Pulse Width After $\overline{EF}$ High	65	—	80	—	120	—	ns
RESET TIMINGS								
tRSC	Reset Cycle Time	80	—	100	—	140	—	ns
tRS	Reset Pulse Width	65	—	80	—	120	—	ns
tRSS	Reset Set-up Time	65	—	80	—	120	—	ns
tRSR	Reset Recovery Time	15	—	20	—	20	—	ns
tRSF1	Reset to $\overline{EF}$ and $\overline{AEF}$ Low	—	80	—	100	—	140	ns
tRSF2	Reset to $\overline{HF}$ and $\overline{FF}$ High	—	80	—	100	—	140	ns
tRSDL	Reset to D Low	50	—	65	—	105	—	ns
tPOI	SICP Rising Edge to D	5	25	5	30	5	35	ns
RETRANSMIT TIMINGS								
tRTC	Retransmit Cycle Time	80	—	100	—	140	—	ns
tRT	Retransmit Pulse Width	65	—	80	—	120	—	ns
tRTS	Retransmit Set-up Time	65	—	80	—	120	—	ns
tRTR	Retransmit Recovery Time	15	—	20	—	20	—	ns
DEPTH EXPANSION MODE TIMINGS								
tXOL	Read/Write to $\overline{XO}$ Low	—	65	—	80	—	120	ns
tXOH	Read/Write to $\overline{XO}$ High	—	65	—	80	—	120	ns
tXI	$\overline{XI}$ Pulse Width	65	—	80	—	120	—	ns
tXIR	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	ns
tXIS	$\overline{XI}$ Set-up Time	15	—	15	—	15	—	ns

NOTE:
1. Guaranteed by design minimum times, not tested.

2752 tbl 08

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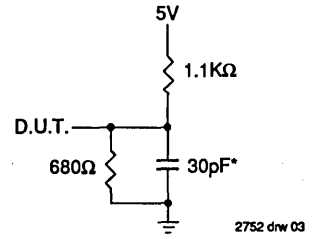
AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure A

2752 tbl 09



or equivalent circuit

Figure A. Output Load

*Includes jig and scope capacitances

FUNCTIONAL DESCRIPTION

Serial Data Input

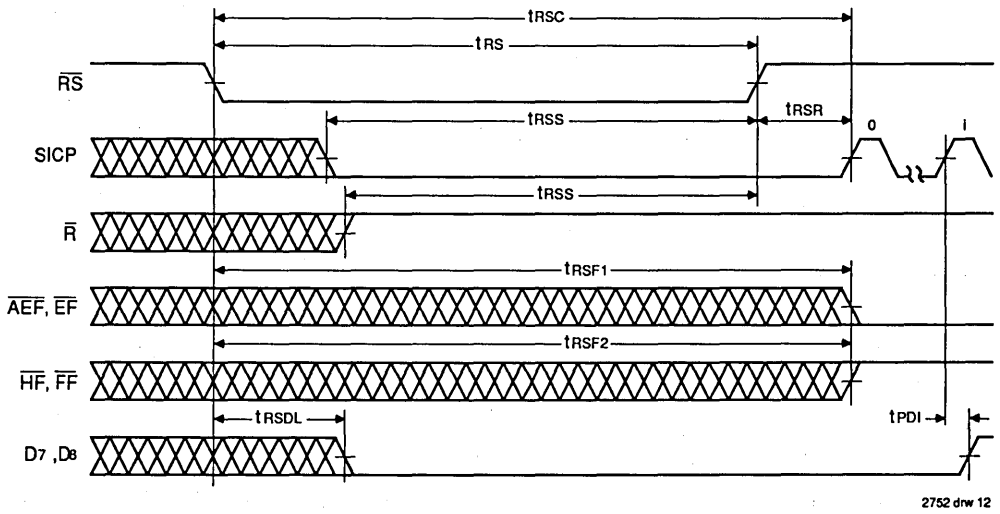
The serial data is input on the SI pin. The data is clocked in on the rising edge of SICP providing the Full Flag ($\overline{FF}$) is not asserted. If the Full Flag is asserted then the next data word is inhibited from moving into the RAM array. NOTE: SICP should not be clocked while the Full Flag is low. If it is, then then the input data will be lost.

The serial word is shifted in Least Significant Bit first. Thus, when the FIFO is read, the Least Significant Bit will come out on Q_0 and the second bit is on Q_1 and so on. The serial word width must be programmed by connecting the appropriate Data Set line (D_7, D_8) to the $\overline{NW}$ input. The data set lines are taps, programs the width of the serial word to be read in.

Parallel Data Output

A read cycle is initiated on the falling edge of Read ($\overline{R}$) provided the Empty Flag is not set. The output data is accessed on a first-in/first-out basis, independent of the ongoing write operations. The data is available t_A after the falling edge of $\overline{R}$ and the output bus Q goes into high impedance after $\overline{R}$ goes HIGH.

Alternately, the user can access the FIFO by keeping $\overline{R}$ LOW and enabling data on the bus by asserting Output Enable ($\overline{OE}$). When $\overline{R}$ is LOW, the $\overline{OE}$ signal enables data on the output bus. When $\overline{R}$ is LOW and $\overline{OE}$ is HIGH, the output bus is three-stated. When $\overline{R}$ is HIGH, the output bus is disabled irrespective of $\overline{OE}$.



NOTE:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Reset, but flags will be valid at t_{RSC}.

Figure 1. Reset

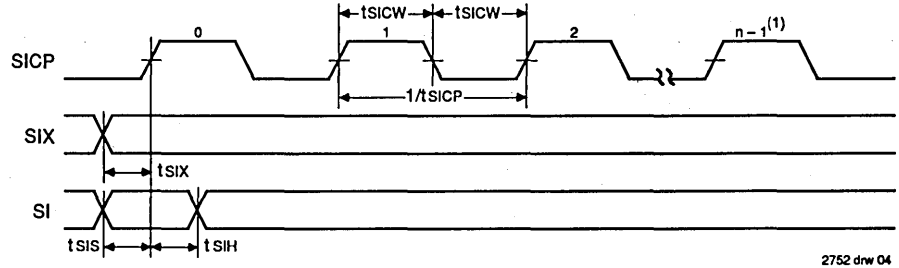


Figure 2. Write Operation

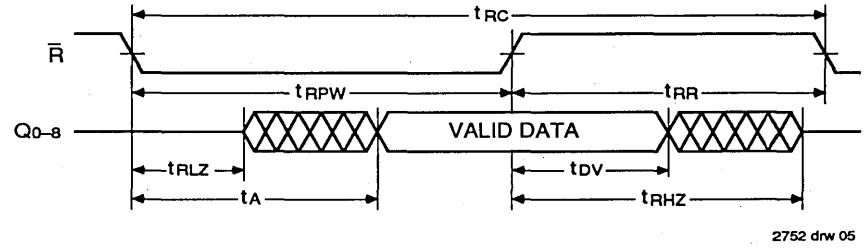


Figure 3. Read Operation

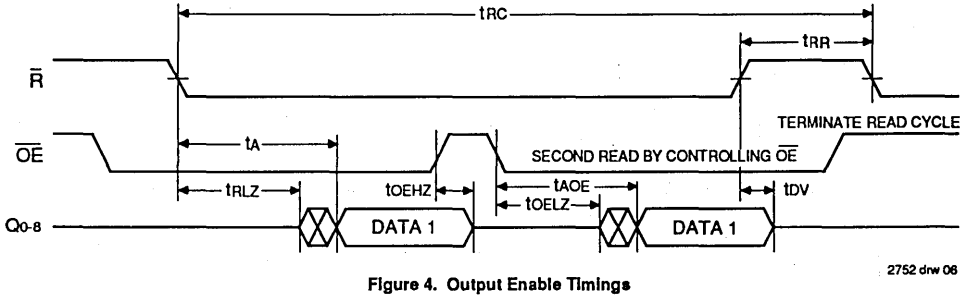
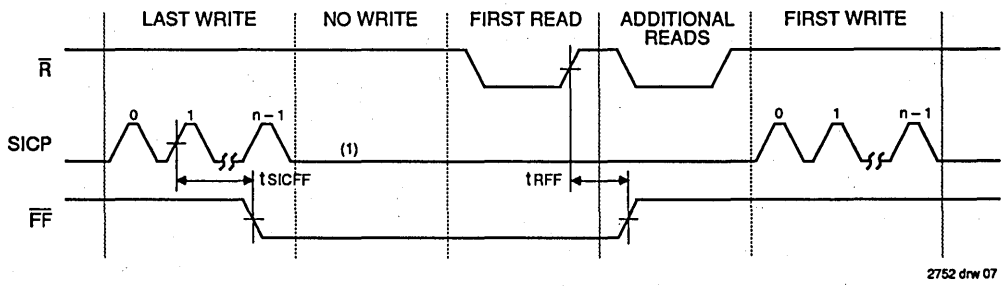


Figure 4. Output Enable Timings

6



NOTE:
1. SICP should not be clocked until $\overline{FF}$ goes high.

Figure 5. Full Flag from Last Write to First Read

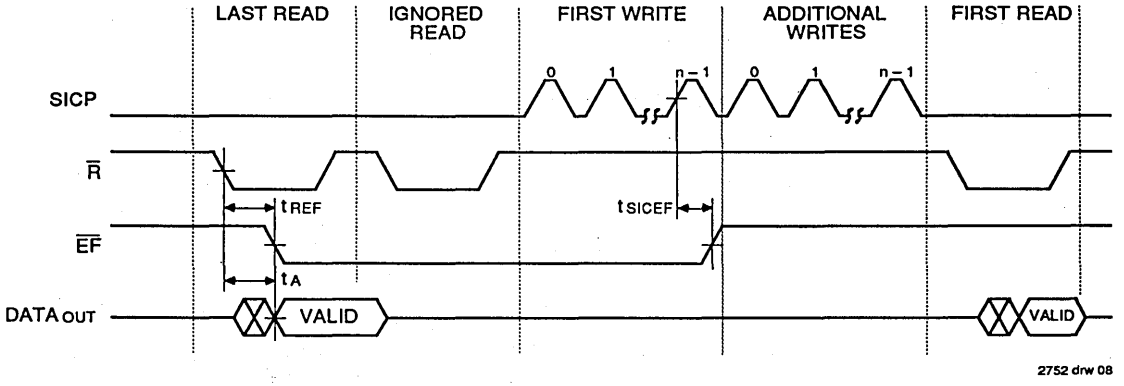


Figure 6. Empty Flag from Last Read to First Write

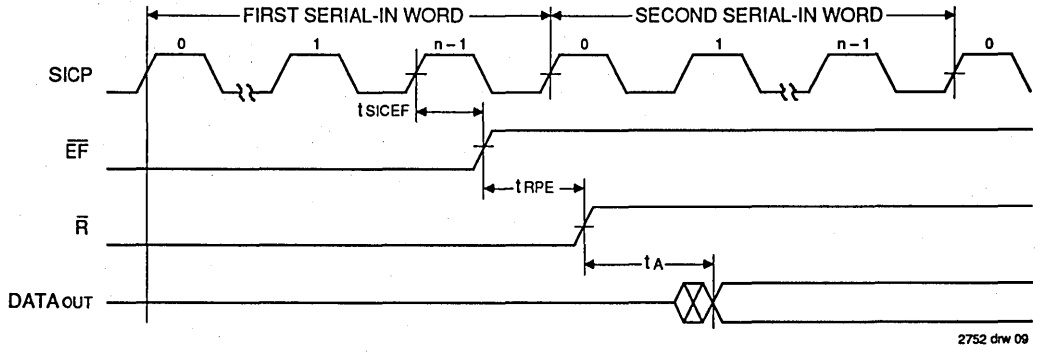
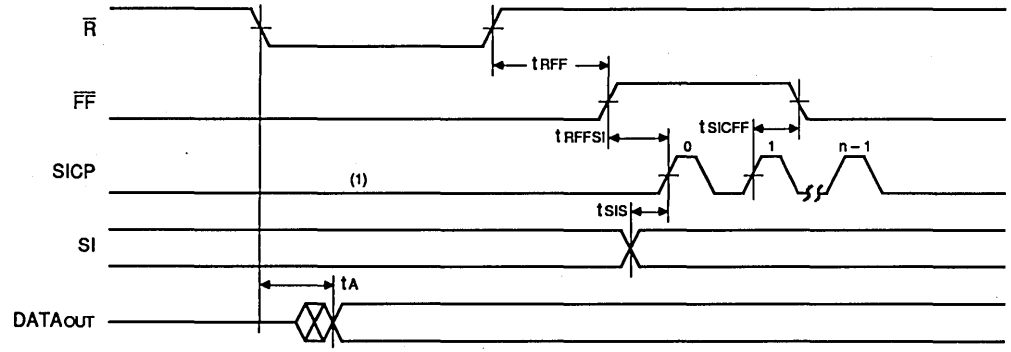


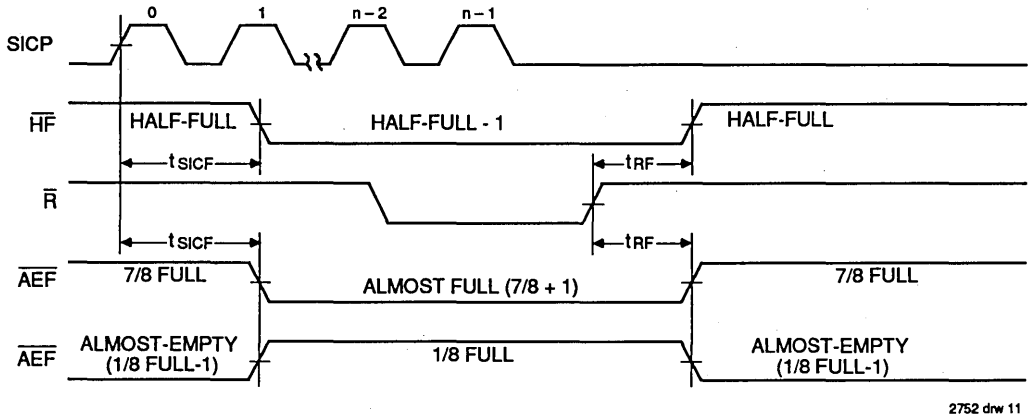
Figure 7. Empty Boundry Condition Timing



NOTE:
1. SICP should remain low unti afterI FF goes high.

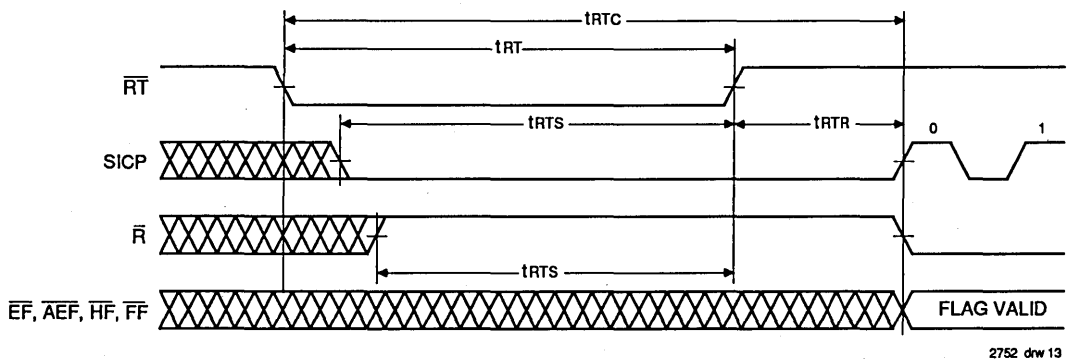
2752 drw 10

Figure 8. Full Boundry Condition Timing



2752 drw 11

Figure 9. Half Full, Almost Full and Almost Empty Timings



2752 drw 13

NOTE:
1. EF, AEF, HF and FF may change status during Retransmit, but flags will be valid at tRTC.

Figure 10. Retransmit

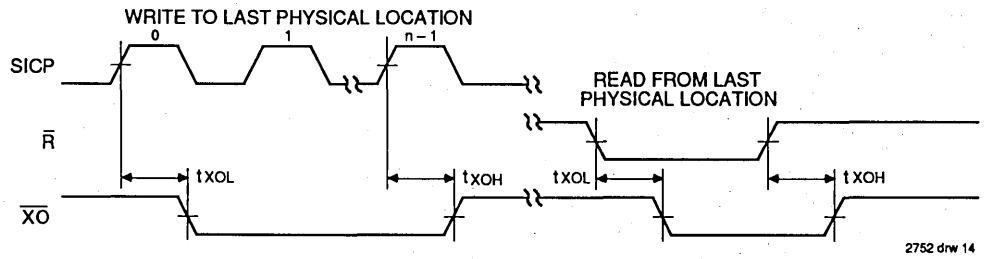


Figure 11. Expansion-Out

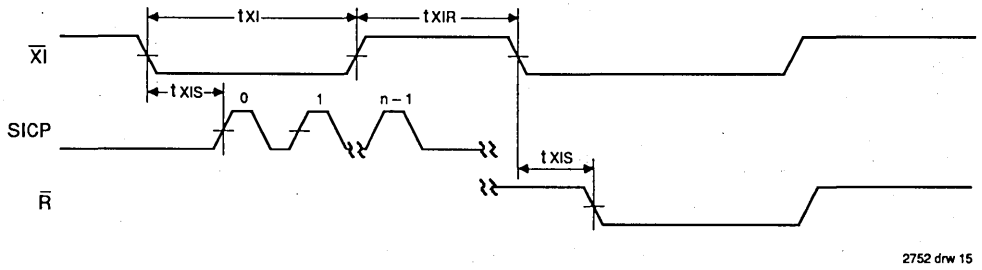


Figure 12. Expansion-In

OPERATING CONFIGURATIONS

Single Device Configuration

In the standalone case, the SIX line is tied HIGH and not used. On the first LOW-to-HIGH of the SICP clock, both of the Data Set lines (D_7, D_8) go low and a new serial word is started. The Data Set lines then go high on the equivalent SICP clock pulse. This continues until the D line connected to $\overline{NW}$ goes high completing the serial word. The cycle is then repeated with the next LOW-to-HIGH transition of SICP.

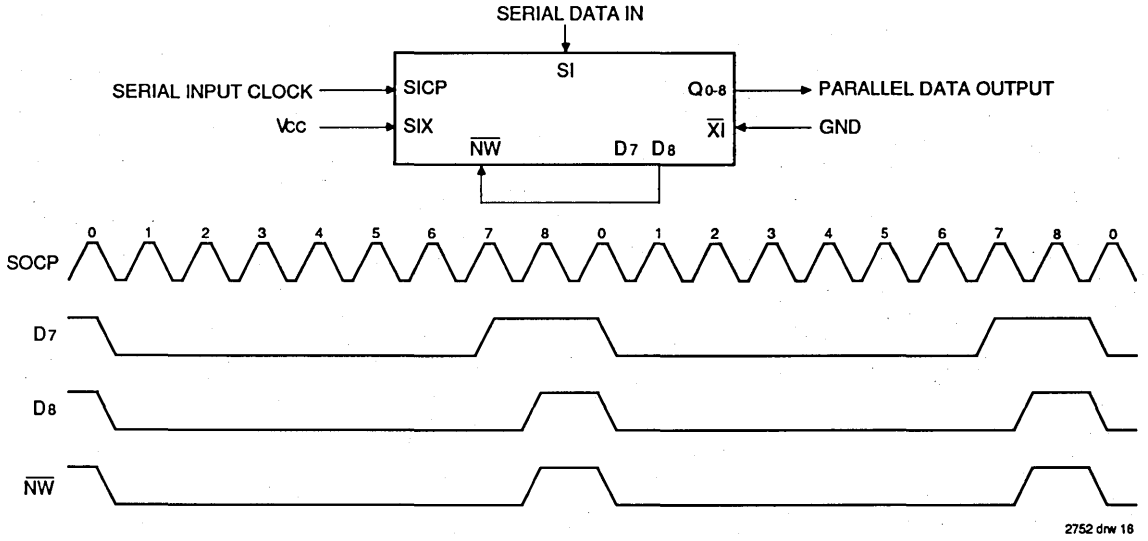


Figure 13. Nine-Bit Word Single Device Configuration

TRUTH TABLES

TABLE 1: RESET AND RETRANSMIT — SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{AEF}$, $\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will increment if appropriate flag is HIGH.

Width Expansion Configuration

In the cascaded case, word widths of more than 9 bits can be achieved by using more than one device. By tying the SIX line of the least significant device HIGH and the SIX of the subsequent devices to the appropriate Data Set lines of the previous devices, a cascaded serial word is achieved.

On the first LOW-to-HIGH clock edge of SICP, both the Data Set lines go LOW. Just as in the standalone case, on each corresponding clock cycle, the equivalent Data Set line goes HIGH in order of least to most significant.

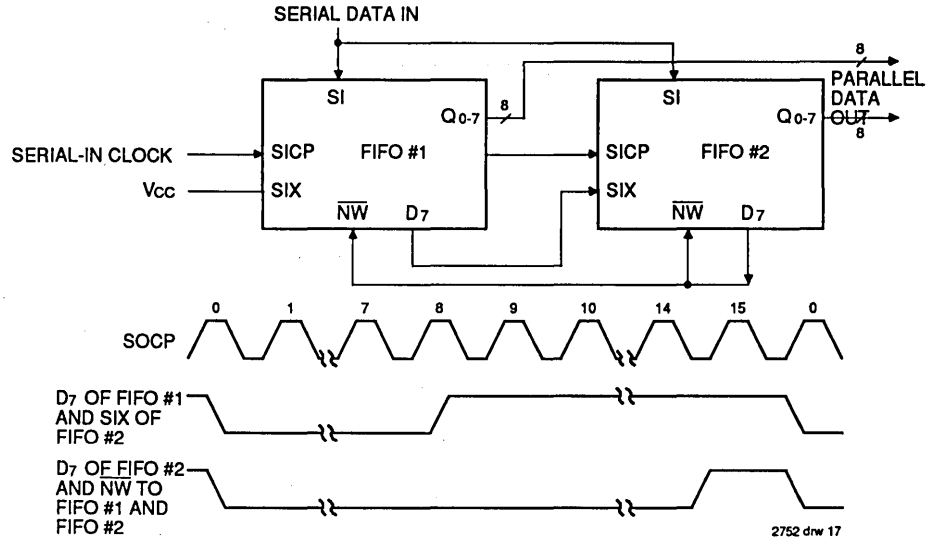


Figure 14. Serial-In to Parallel-Out Data of 16 Bits

Depth Expansion (Daisy Chain) Mode

The IDT72132/42 can be easily adapted to applications where the requirements are for greater than 2048/4096 words. Figure 15 demonstrates Depth Expansion using three IDT72132/42. Any depth can be attained by adding additional IDT72132/42 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin and Expansion In ($\overline{XI}$) pin of each device must be tied together.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the OR-ing of all $\overline{EF}$s and OR-ing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite ($\overline{FF}$) or ($\overline{EF}$).
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion mode.

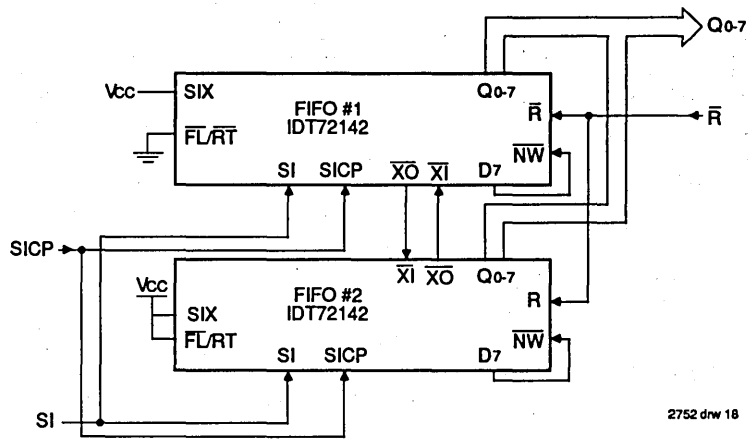


Figure 15. An 8K x 8 Serial-In Parallel-Out FIFO

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TABLE 2: RESET AND FIRST LOAD TRUTH TABLE — DEPTH EXPANSION/COMPOUND EXPANSION MODE

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Retransmit all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of the previous device.
2. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Ouput, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input.

SERIAL INPUT WITH WIDTH AND DEPTH EXPANSION

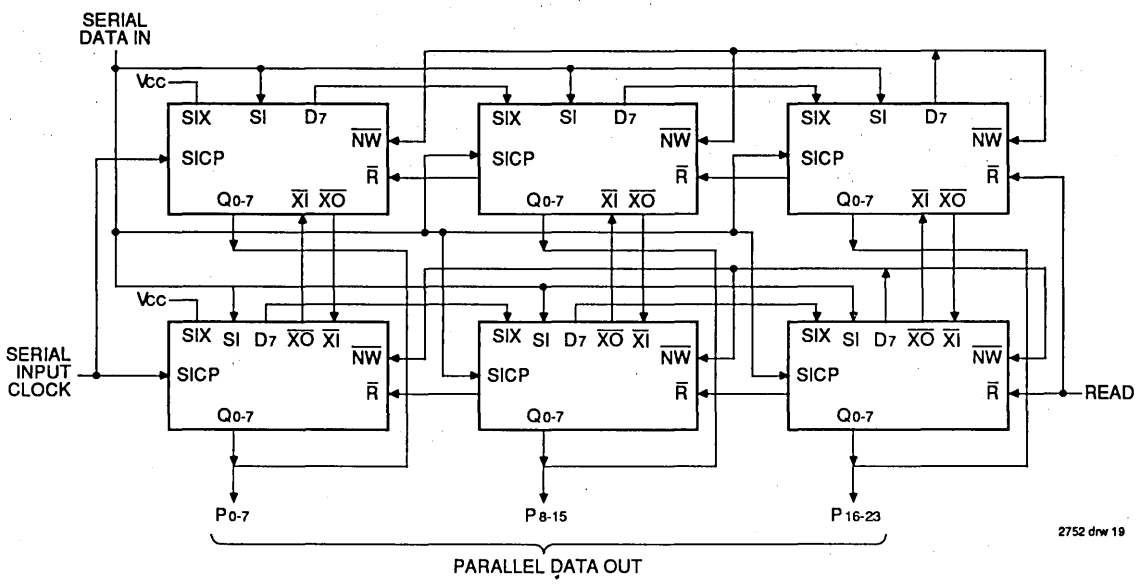
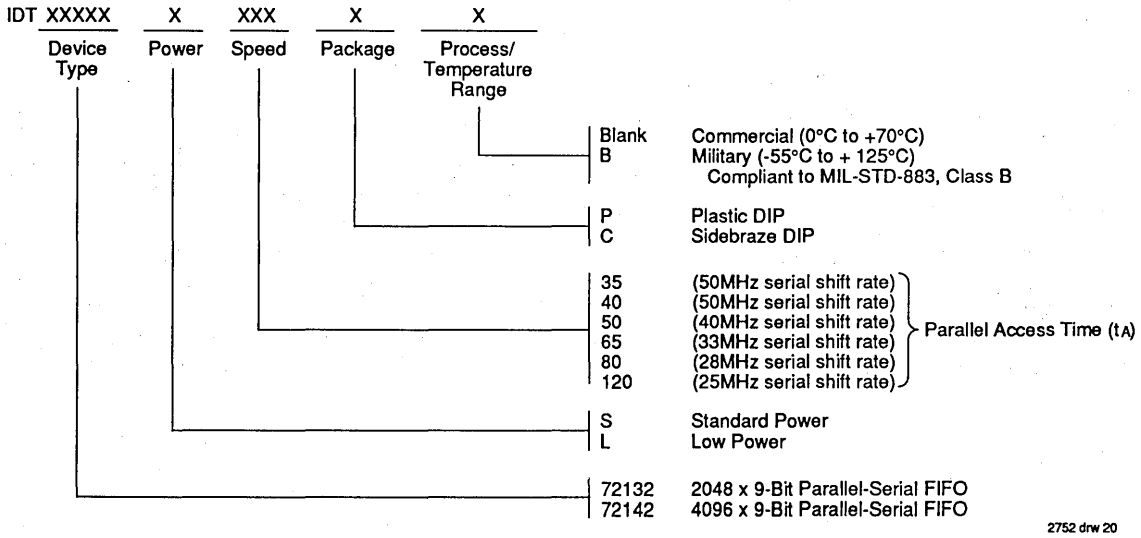


Figure 16. An 8K x 24 Serial-In, Parallel-Out FIFO Using Six IDT72142s

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS PARALLEL SyncFIFO™ (CLOCKED FIFO) 256 X 8-BIT, 512 X 8-BIT & 64 X 8-BIT

IDT72200
IDT72210
IDT72420

FEATURES:

- 64, 256, and 512 x 8-bit memory array structures
- 15ns read/write cycle time
- Read and write clocks can be asynchronous or coincident
- Dual-ported zero fall-through time architecture
- Empty and Full flags signal FIFO status
- Almost-empty and almost-full flags set to Empty+7 and Full-7, respectively
- Output enable puts output data bus in high impedance state
- Produced with advanced submicron CEMOS™ technology
- Available in 28-pin 300 mil plastic DIP and 300 mil ceramic DIP
- For surface mount product please see the IDT72201/ 72211/72421 data sheet
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

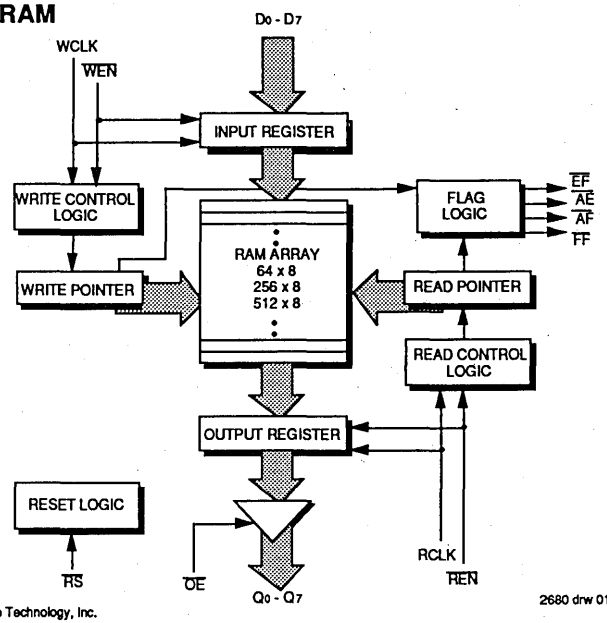
The IDT72200/72210/72420 SyncFIFO™ are very high speed, low-power first-in, first-out (FIFO) memories with clocked read and write controls. The IDT72200/72210/ 72420 have a 256, 512, and 64 x 8-bit memory array, respectively. These FIFOs are applicable for a wide variety of data buffering needs, such as graphics, local area networks (LANs), and interprocessor communication.

These FIFOs have 8-bit input and output ports. The input port is controlled by a free-running clock (WCLK), and a write enable pin ($\overline{WEN}$). Data is read into the Synchronous FIFO on every clock when $\overline{WEN}$ is asserted. The output port is controlled by another clock pin (RCLK) and a read enable pin ($\overline{REN}$). The read clock can be tied to the write clock for single clock operation or the two clocks can run asynchronous of one another for dual clock operation. An output enable pin ($\overline{OE}$) is provided on the read port for three-state control of the output.

These Synchronous FIFOs have two end-point flags, Empty ($\overline{EF}$) and Full ($\overline{FF}$). Two partial flags, Almost-Empty ($\overline{AE}$) and Almost-Full ($\overline{AF}$), are provided for improved system control. The partial ($\overline{AE}$) flags are set to Empty+7 and Full-7 for $\overline{AE}$ and $\overline{AF}$ respectively.

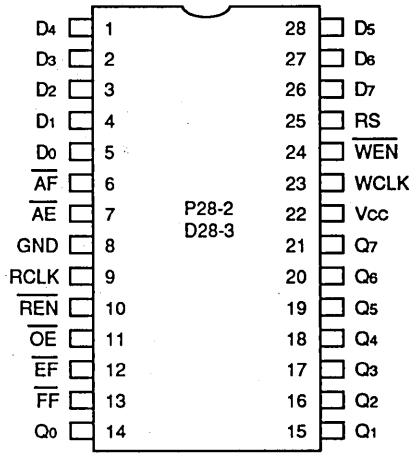
The IDT72200/72210/72420 are fabricated using IDT's high speed submicron CEMOS™ technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



SyncFIFO and CEMOS are trademarks of Integrated Device Technology, Inc.

PIN CONFIGURATION



2680 drw 02

DIP
TOP VIEW

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D0 - D7	Data Inputs	I	Data inputs for a 8-bit bus.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal read and write pointers are set to the first location of the RAM array, $\overline{FF}$ and $\overline{PAF}$ go high, and $\overline{PAE}$ and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up.
WCLK	Write Clock	I	Data is written into the FIFO on a LOW-to-HIGH transition of WCLK when $\overline{WEN}$ is asserted.
$\overline{WEN}$	Write Enable	I	When $\overline{WEN}$ is LOW, data is written into the FIFO on every LOW-to-HIGH transition of WCLK. Data will not be written into the FIFO if the $\overline{FF}$ is LOW.
Q0 - Q7	Data Outputs	O	Data outputs for a 8-bit bus.
RCLK	Read Clock	I	Data is read from the FIFO on a LOW-to-HIGH transition of RCLK when $\overline{REN}$ is asserted.
$\overline{REN}$	Read Enable	I	When $\overline{REN}$ is LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the data output bus is active. If $\overline{OE}$ is HIGH, the output data bus will be in a high impedance state.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty and further data reads from the output are inhibited. When $\overline{EF}$ is HIGH, the FIFO is not empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{AE}$	Almost-Empty Flag	O	When $\overline{AE}$ is LOW, the FIFO is almost empty based on the offset Empty+7. $\overline{AE}$ is synchronized to RCLK.
$\overline{AF}$	Almost-Full Flag	O	When $\overline{AF}$ is LOW, the FIFO is almost full based on the offset Full-7. $\overline{AF}$ is synchronized to WCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full and further data writes into the input are inhibited. When $\overline{FF}$ is HIGH, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK.
VCC	Power		One +5 volt power supply pin.
GND	Ground		One 0 volt ground pin.

2680 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to + 7.0	–0.5 to + 7.0	V
TA	Operating Temperature	0 to + 70	–55 to + 125	°C
TBIAS	Temperature Under Bias	–55 to + 125	–65 to + 135	°C
TSTG	Storage Temperature	–55 to + 125	–65 to + 135	°C
IOUT	DC Output Current	50	50	mA

2680 tbl 02

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage Commercial	2.0	—	—	V
VIH	Input High Voltage Military	2.2	—	—	V
VIL	Input Low Voltage Commercial & Military	—	—	0.8	V

2680 tbl 03

DC ELECTRICAL CHARACTERISTICS

(Commercial: VCC = 5V ± 10%, TA = 0°C to +70°C; Military: VCC = 5V ± 10%, TA = -55°C to +125°C)

Symbol	Parameter	IDT72200 IDT72210 IDT72420 Commercial tCLK = 15, 20, 25, 50 ns Min.	Typ.	Max.	IDT72200 IDT72210 IDT72420 Military tCLK = 20, 25, 50 ns Min.	Typ.	Max.	Units
ILI(1)	Input Leakage Current (any input)	-1	—	1	-10	—	10	µA
ILO(2)	Output Leakage Current	-10	—	10	-10	—	10	µA
VOH	Output Logic "1" Voltage, IOH = –2 mA	2.4	—	—	2.4	—	—	V
VOL	Output Logic "0" Voltage, IOL = 8 mA	—	—	0.4	—	—	0.4	V
ICC1(3)	Active Power Supply Current	—	—	140	—	—	160	mA

NOTES:

1. Measurements with 0.4 ≤ VIN ≤ VOUT.
2. $\overline{OE}$ ≥ VIH, 0.4 ≤ VOUT ≤ VCC.
3. Measurements are made with outputs open. Tested at fCLK = 20 MHz.
   Typical ICC1 = 65 + (fCLK * 1.1/MHz) + (fCLK * CL * 0.03/MHz-pF) mA
   fCLK = 1 / tCLK
   CL = external capacitive load (30 pF typical)

2680 tbl 04

CAPACITANCE (TA = +25°C, f = 1.0 MHz)

Symbol	Parameter	Conditions	Max.	Unit
CIN(2)	Input Capacitance	VIN = 0V	10	pF
COUT(1, 2)	Output Capacitance	VOUT = 0V	10	pF

NOTES:

1. With output deselected. ($\overline{OE}$ = high)
2. Characterized values, not currently tested.

2680 tbl 05

6

AC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 5V ± 10%, TA = 0°C to + 70°C; Military: Vcc = 5V ± 10%, TA = -55°C to +125°C)

Symbol	Parameter	Com'l. IDT72200L15 IDT72210L15 IDT72420L15 Min.	Max.	Commercial & Military IDT72200L20 IDT72210L20 IDT72420L20 Min.	Max.	IDT72200L25 IDT72210L25 IDT72420L25 Min.	Max.	IDT72200L50 IDT72210L50 IDT72420L50 Min.	Max.	Unit
fS	Clock Cycle Frequency	—	66.7	—	50	—	40	—	20	MHz
tA	Data Access Time	2	10	2	12	3	15	3	25	ns
tCLK	Clock Cycle Time	15	—	20	—	25	—	50	—	ns
tCLKH	Clock High Time	6	—	8	—	10	—	20	—	ns
tCLKL	Clock Low Time	6	—	8	—	10	—	20	—	ns
tDS	Data Set-up Time	4	—	5	—	6	—	10	—	ns
tDH	Data Hold Time	1	—	1	—	1	—	2	—	ns
tENS	Enable Set-up Time	4	—	5	—	6	—	10	—	ns
tENH	Enable Hold Time	1	—	1	—	1	—	2	—	ns
tRS	Reset Pulse Width[1]	15	—	20	—	25	—	50	—	ns
tRSS	Reset Set-up Time	15	—	20	—	25	—	50	—	ns
tRSF	Reset to Flag and Output Time	—	15	—	20	—	25	—	50	ns
tOLZ	Output Enable to Output in Low Z[2]	0	—	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	3	8	3	10	3	13	3	28	ns
tOHZ	Output Enable to Output in High Z[2]	3	8	3	10	3	13	3	28	ns
tWFF	Write Clock to Full Flag	—	10	—	12	—	15	—	30	ns
tREF	Read Clock to Empty Flag	—	10	—	12	—	15	—	30	ns
tAF	Write Clock to Almost-Full Flag	—	10	—	12	—	15	—	30	ns
tAE	Read Clock to Almost-Empty Flag	—	10	—	12	—	15	—	30	ns
tSKEW1	Skew time between Read Clock & Write Clock for Empty Flag & Full Flag	6	—	8	—	10	—	15	—	ns
tSKEW2	Skew time between Read Clock & Write Clock for Almost-Empty Flag & Almost-Full Flag	15	—	18	—	20	—	30	—	ns

NOTES:

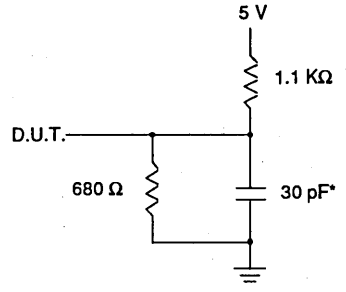
1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

2680 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2680 tbl 07



or equivalent circuit

2680 drw 03

Figure 1. Output Load

*Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS

INPUTS:

Data In (D_0 - D_7) - Data inputs for 8-bit wide data.

CONTROLS:

Reset ($\overline{RS}$) - Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. The Full Flag ($\overline{FF}$) and Almost Full Flag ($\overline{AF}$) will be reset to high after t_{RSF}. The Empty Flag ($\overline{EF}$) and Almost Empty Flag ($\overline{AE}$) will be reset to low after t_{RSF}. During reset, the output register is initialized to all zeros.

Write Clock (WCLK) - A write cycle is initiated on the low-to-high transition of the write clock (WCLK). Data set-up and hold times must be met in respect to the low-to-high transition of the write clock (WCLK). The Full Flag ($\overline{FF}$) and Almost Full Flag ($\overline{AF}$) are synchronized with respect to the low-to-high transition of the write clock (WCLK).

The write and read clocks can be asynchronous or coincident.

Write Enable ($\overline{WEN}$) - When Write Enable ($\overline{WEN}$) is low, data can be loaded into the input register and RAM array on the low-to-high transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

When Write Enable ($\overline{WEN}$) is high, the input register holds the previous data and no new data is allowed to be loaded into the register.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read cycle, the Full Flag ($\overline{FF}$) will go high after t_{WFF}, allowing a valid write to begin. Write Enable ($\overline{WEN}$) is ignored when the FIFO is full.

Read Clock (RCLK) - Data can be read on the outputs on the low-to-high transition of the read clock (RCLK). The Empty Flag ($\overline{EF}$) and Almost-Empty Flag ($\overline{AE}$) are synchronized with respect to the low-to-high transition of the read clock (RCLK).

The write and read clocks can be asynchronous or coincident.

Read Enable ($\overline{REN}$) - When Read Enable ($\overline{REN}$) is low, data is read from the RAM array to the output register on the low-to-high transition of the read clock (RCLK).

When Read Enable ($\overline{REN}$) is high, the output register holds the previous data and no new data is allowed to be loaded into the register.

When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go high after t_{REF} and a valid read can begin. Read Enable ($\overline{REN}$) is ignored when the FIFO is empty.

Output Enable ($\overline{OE}$) - When Output Enable ($\overline{OE}$) is enabled (low), the parallel output buffers receive data from the output register. When Output Enable ($\overline{OE}$) is disabled (high), the Q output data bus is in a high impedance state.

OUTPUTS:

Full Flag ($\overline{FF}$) - The Full Flag ($\overline{FF}$) will go low, inhibiting further write operation, when the device is full. If no reads are performed after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go low after 256 writes for the IDT72200, 512 writes for the IDT72210, and 64 writes for the IDT72420.

The Full Flag ($\overline{FF}$) is synchronized with respect to the low-to-high transition of the write clock (WCLK).

Empty Flag ($\overline{EF}$) - The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating the device is empty.

The Empty Flag ($\overline{EF}$) is synchronized with respect to the low-to-high transition of the read clock (RCLK).

Almost Full Flag ($\overline{AF}$) - The Almost Full Flag ($\overline{AF}$) will go low when the FIFO reaches the Almost-Full condition. If no reads are performed after Reset ($\overline{RS}$), the Almost Full Flag ($\overline{AF}$) will go low after 249 writes for the IDT72200, 505 writes for the IDT72210, and 57 writes for the IDT72420.

The Almost Full Flag ($\overline{AF}$) is synchronized with respect to the low-to-high transition of the write clock (WCLK).

Almost Empty Flag ($\overline{AE}$) - The Almost Empty Flag ($\overline{AE}$) will go low when the FIFO reaches the Almost-Empty condition. If no reads are performed after Reset ($\overline{RS}$), the Almost Empty Flag ($\overline{AE}$) will go high after 8 writes for the IDT72200, IDT72210, and IDT72420.

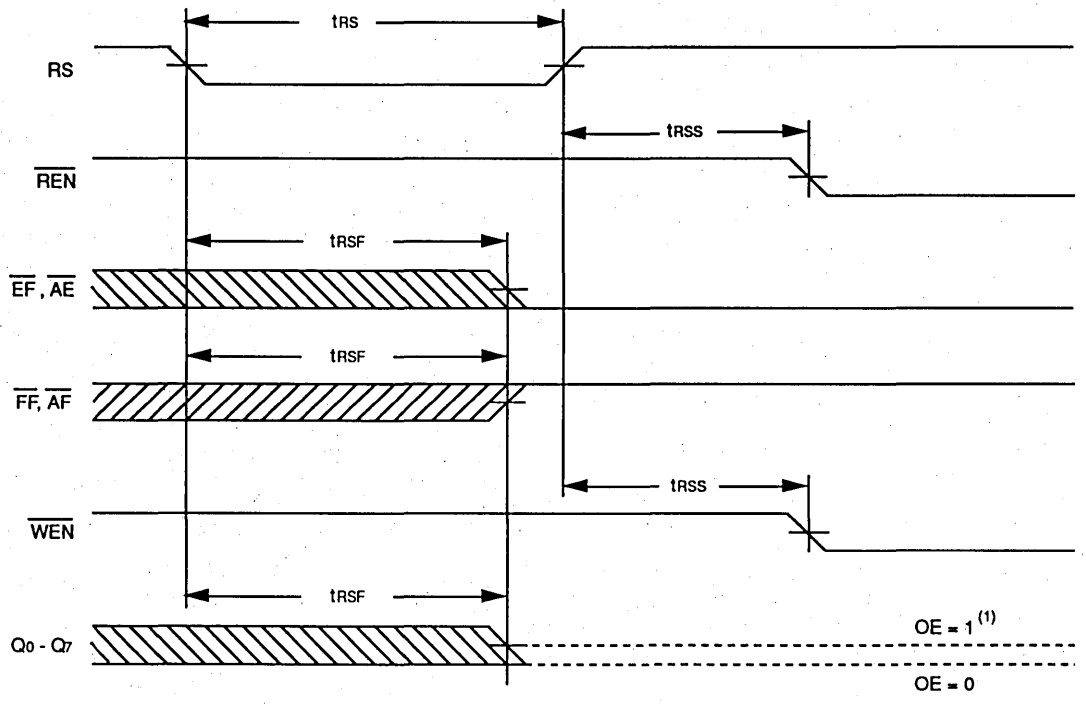
The Almost Empty Flag ($\overline{AE}$) is synchronized with respect to the low-to-high transition of the read clock (RCLK)

Data Outputs (Q_0 - Q_7) - Data outputs for a 8-bit wide data.

TABLE 1: STATUS FLAGS

Number of Words In FIFO						
IDT72200	IDT72210	IDT72420	$\overline{FF}$	$\overline{AF}$	$\overline{AE}$	$\overline{EF}$
0	0	0	H	H	L	L
1 to 7	1 to 7	1 to 7	H	H	L	H
8 to 248	8 to 504	8 to 56	H	H	H	H
249 to 255	505 to 511	57 to 63	H	L	H	H
256	512	64	L	L	H	H

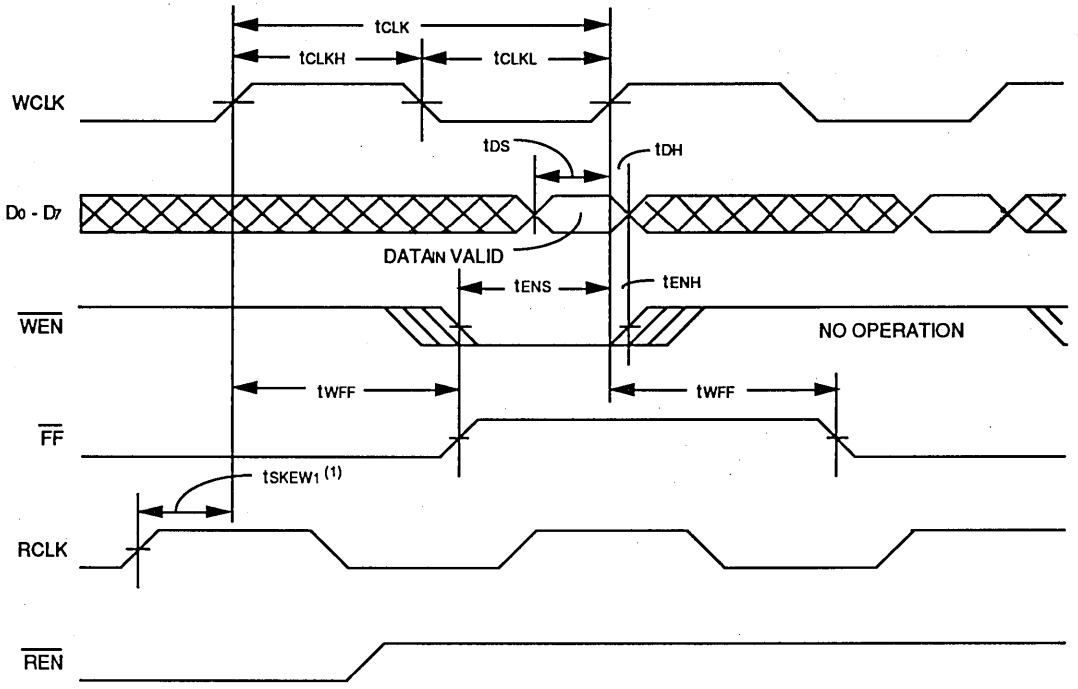
2680 tbl 08



2680 drw 04

NOTE:
1. After reset, the outputs will be low if $\overline{OE}$ = 0 and tri-state if $\overline{OE}$ = 1.
2. The clocks (RCLK, WCLK) can be free-running during reset.

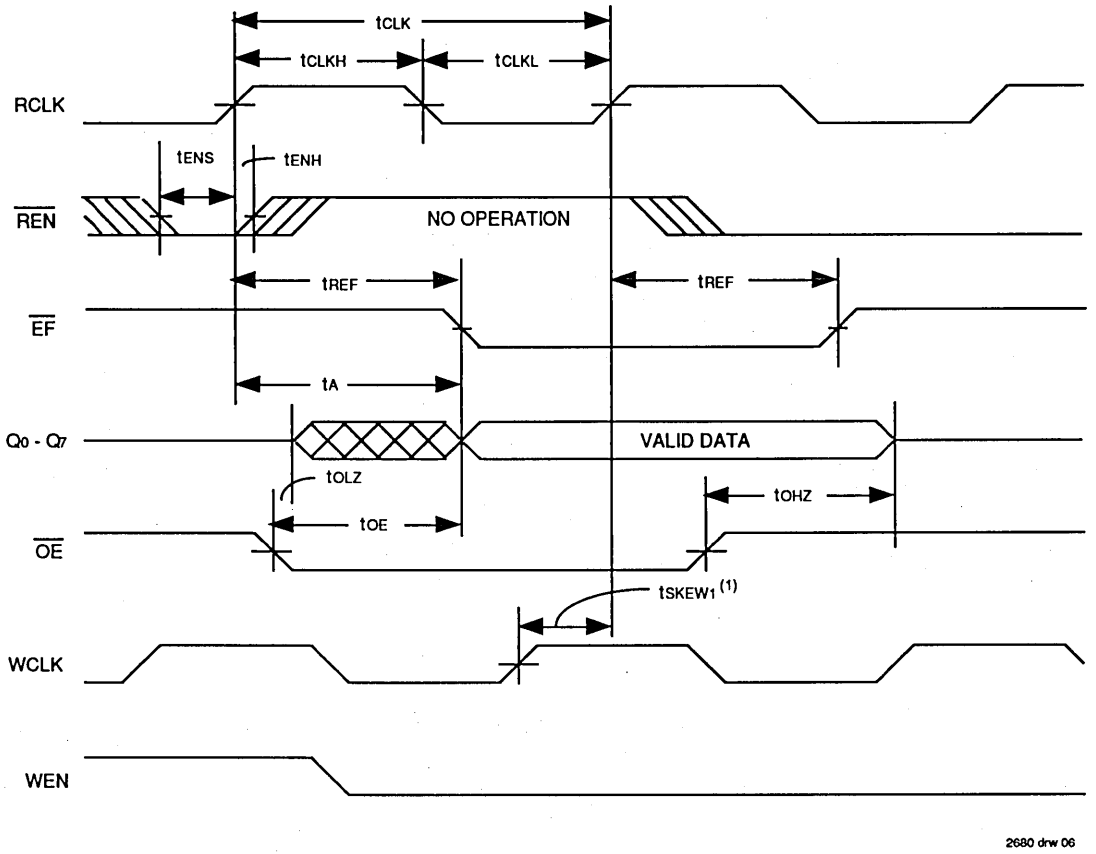
Figure 2. Reset Timing



NOTE:
1. tSKEW1 is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{FF}$ to change during the curent clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than tSKEW1, then $\overline{FF}$ may not change state until the next WCLK edge.

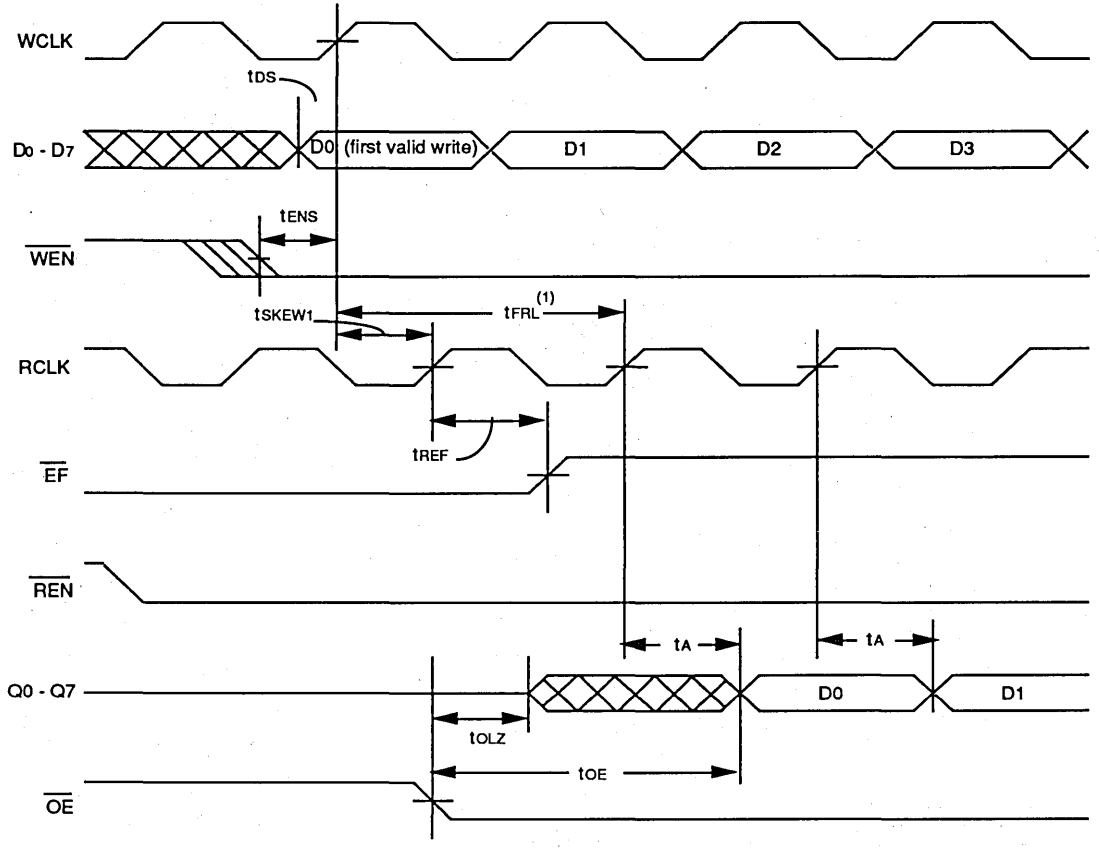
Figure 3. Write Cycle Timing

6



NOTE:
1. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{EF}$ to change during the curent clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW1}, then $\overline{EF}$ may not change state until the next RCLK edge.

Figure 4. Read Cycle Timing



2680 drw 07

NOTE:
1. When $t_{SKEW} \geq$ minimum specification, t_{FRL} maximum = $t_{CLK} + t_{SKEW1}$
   $t_{SKEW} <$ minimum specification, t_{FRL} maximum = $2t_{CLK} + t_{SKEW1}$
   The Latency Timing apply only at the Empty Boundry ($\overline{EF}$ = LOW).

Figure 5. First Data Word Latency Timing

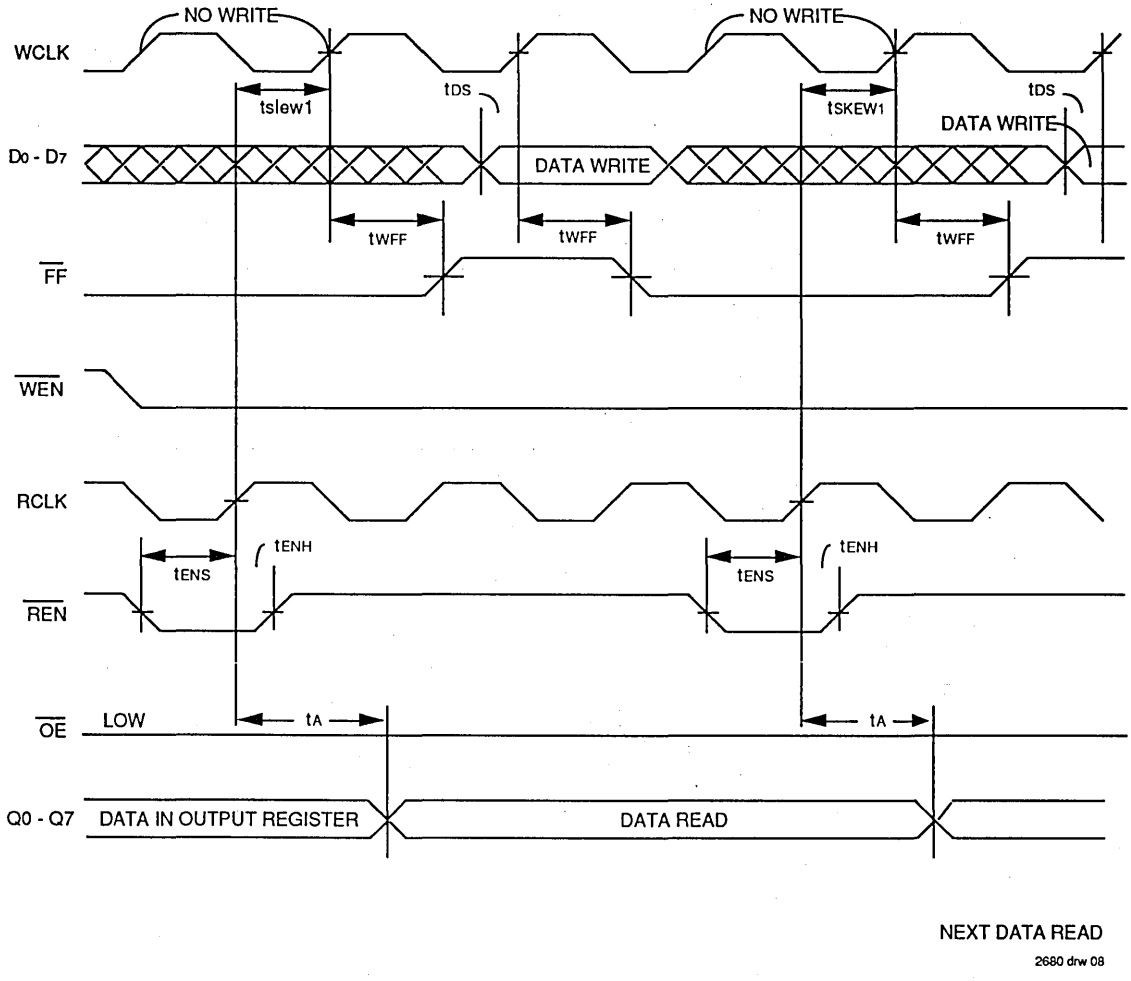
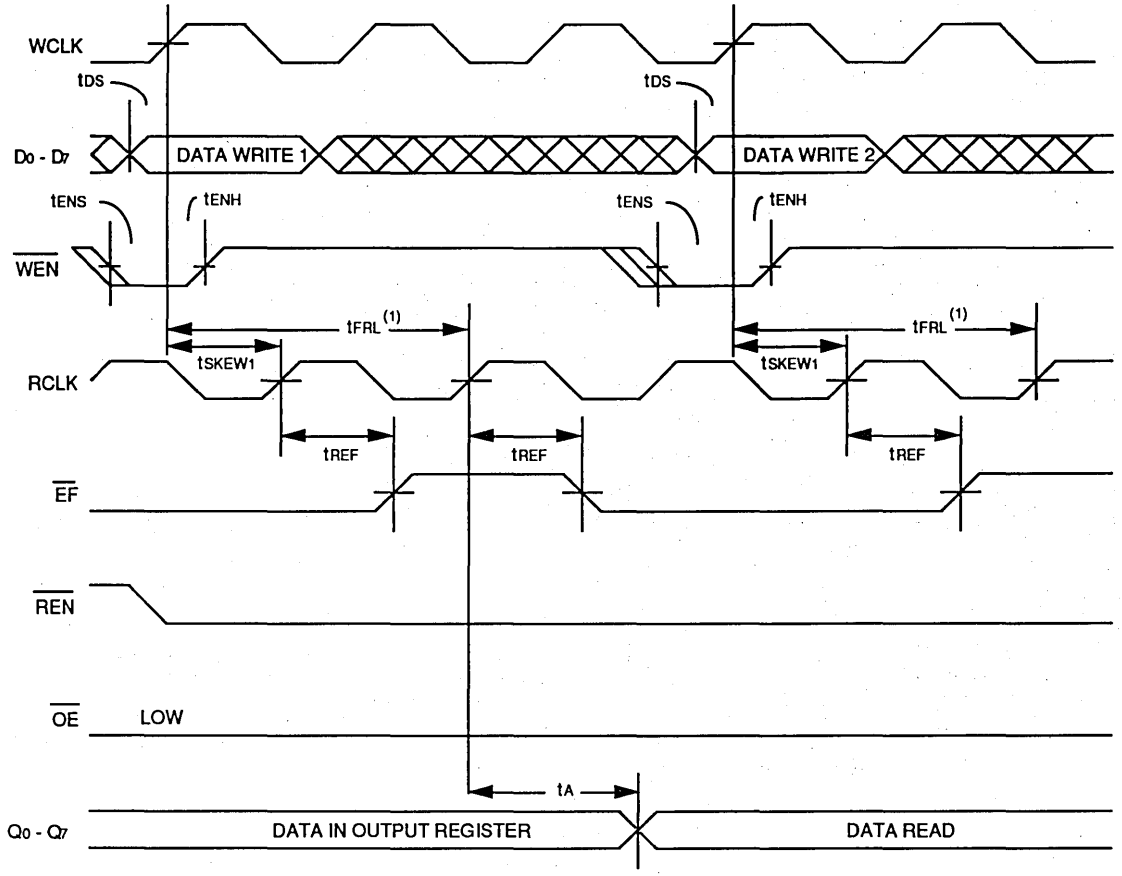


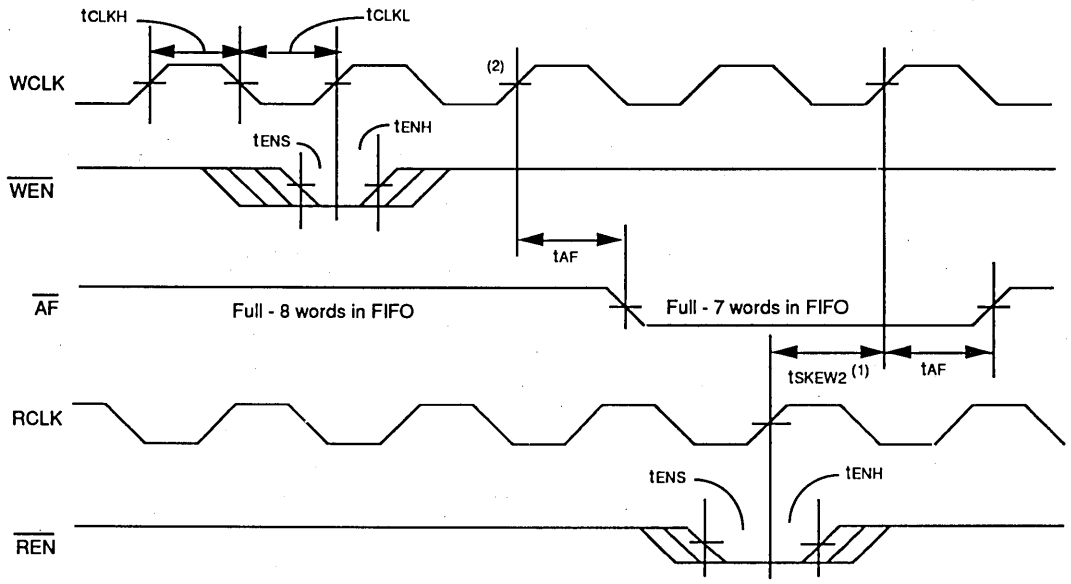
Figure 6. Full Flag Timing



2680 drw 09

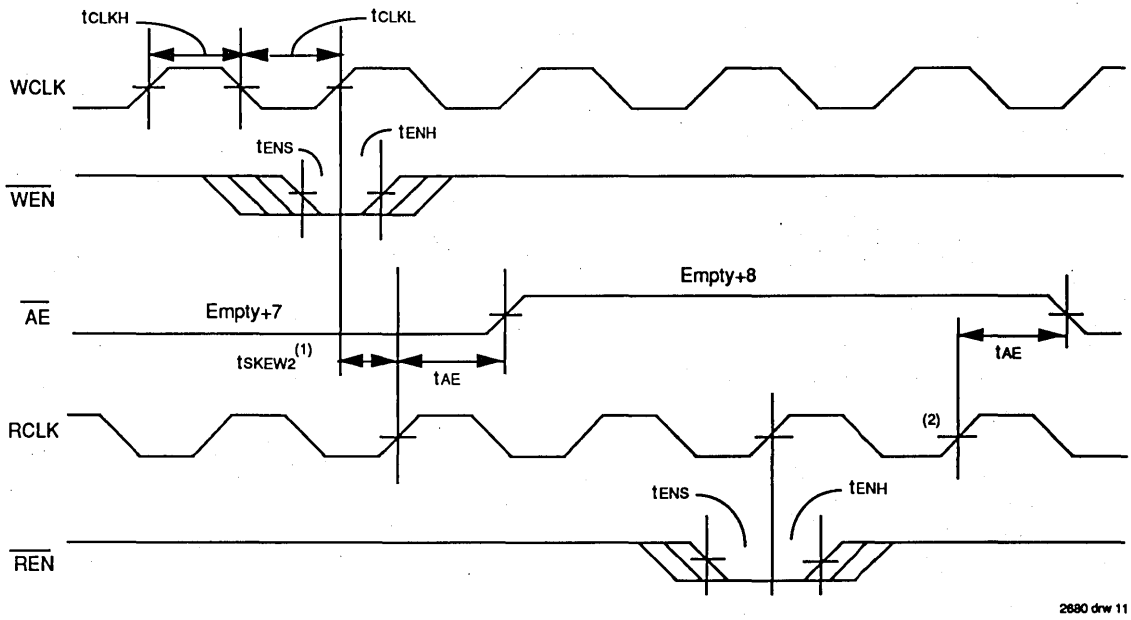
NOTE:
1. When $t_{SKEW} \geq$ minimum specification, t_{FRL} maximum = $t_{CLK} + t_{SKEW1}$
   $t_{SKEW} <$ minimum specification, t_{FRL} maximum = $2t_{CLK} + t_{SKEW1}$
   The Latency Timing apply only at the Empty Boundry ($\overline{EF}$ = LOW).

Figure 7. Empty Flag Timing



NOTES:
1. tSKEW2 is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{AF}$ to change during the curent clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than tSKEW2, then $\overline{AF}$ may not change state until the next WCLK edge.
2. If a write is performed on this rising edge of the write clock, there will be a Full - 6 words in the FIFO when $\overline{AF}$ goes low.

Figure 8. Almost Full Flag Timing



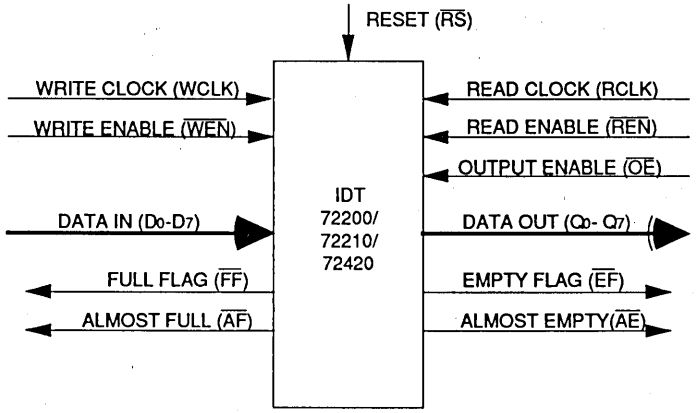
NOTES:
1. tSKEW2 is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{AE}$ to change during the curent clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than tSKEW2, then $\overline{AE}$ may not change state until the next RCLK edge.
2. If a read is performed on this rising edge of the read clock, there will be a Empty - 6 words in the FIFO when $\overline{AE}$ goes low.

Figure 9. Almost Empty Flag Timing

6

OPERATING CONFIGURATIONS

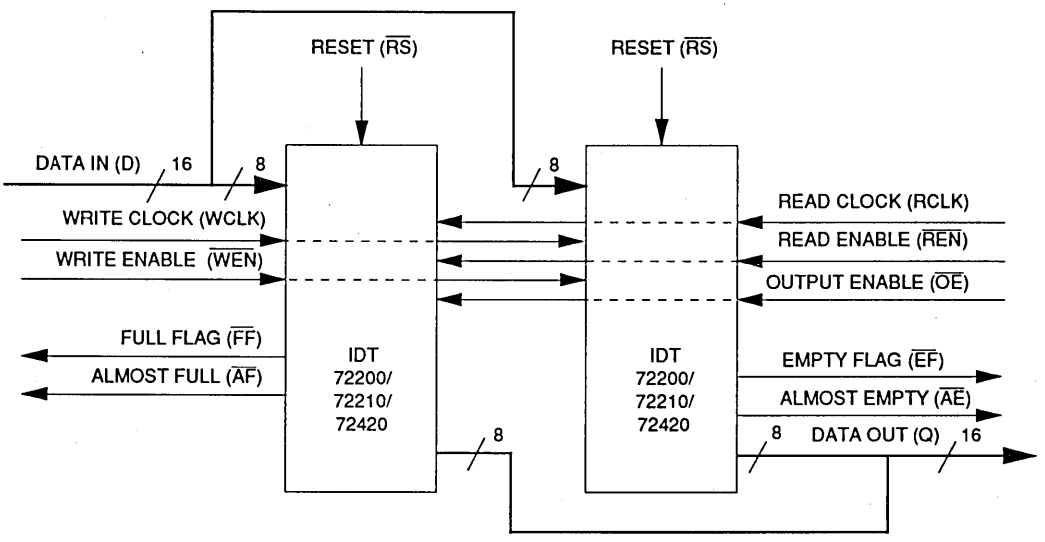
SINGLE DEVICE CONFIGURATION - A single IDT72200/72210/72420 may be used when the application requirements are for 256/512/64 words or less. See Figure 10.



2680 drw 12

Figure 10. Block Diagram of Single 256 x 8/512 x 8/64 x 8 Synchronous FIFO

WIDTH EXPANSION CONFIGURATION - Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags (EF, AE, AF and FF) can be detected from any one device. Figure 11 demonstrates a 16-bit word width by using two IDT72200/72210/72420s. Any word width can be attained by adding additional IDT72200/72210/72420s.



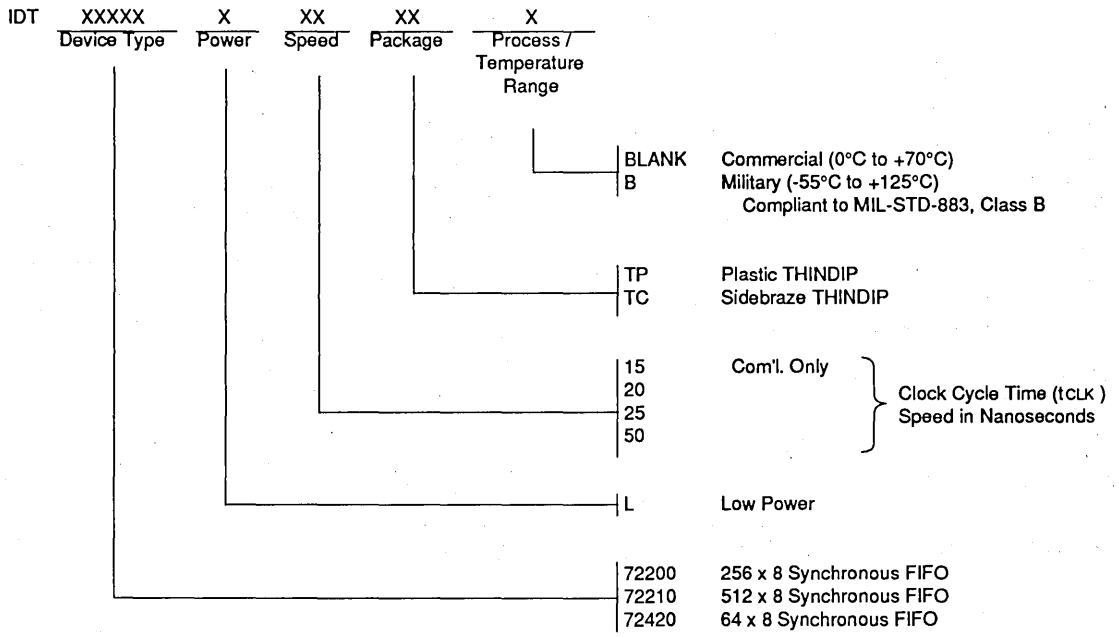
2680 drw 13

Figure 11. Block Diagram of 256 x 16/512 x 16/64 x 16 Synchronous FIFO Used in a Width Expansion Configuration

DEPTH EXPANSION - The IDT72200/72210/72420 can be adapted to applications when the requirements are for greater than 256/512/64 words. Depth expansion is possible by using expansion logic to direct the flow of data. A typical application would have the expansion logic alternate data accesses from one device to the next in a sequential manner.

Please see the Application Note "DEPTH EXPANSION USING 72211 SYNCHRONOUS FIFOs" for details of this configuration.

ORDERING INFORMATION



6

Integrated Device Technology, Inc.

CMOS PARALLEL SyncFIFO™ (CLOCKED FIFO) 256 x 9-BIT, 512 x 9-BIT AND 64 x 9-BIT

IDT72201
IDT72211
IDT72421

FEATURES:

- 64, 256, and 512 x 9-bit memory array structures
- 15ns read/write cycle time
- Read and write clocks can be asynchronous or coincident
- Dual-ported zero fall-through time architecture
- Empty and Full flags signal FIFO status
- Programmable Almost-Empty and Almost-Full flags can be set to any depth
- Programmable Almost-Empty and Almost-Full flags default to Empty+7, and Full-7, respectively
- Output enable puts output data bus in high impedance state
- Produced with advanced submicron CEMOS™ technology
- Available in 32-pin plastic leaded chip carrier (PLCC) and ceramic leadless chip carrier (LCC)
- For Through-Hole product please see the IDT72200/72210/72420 data sheet
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

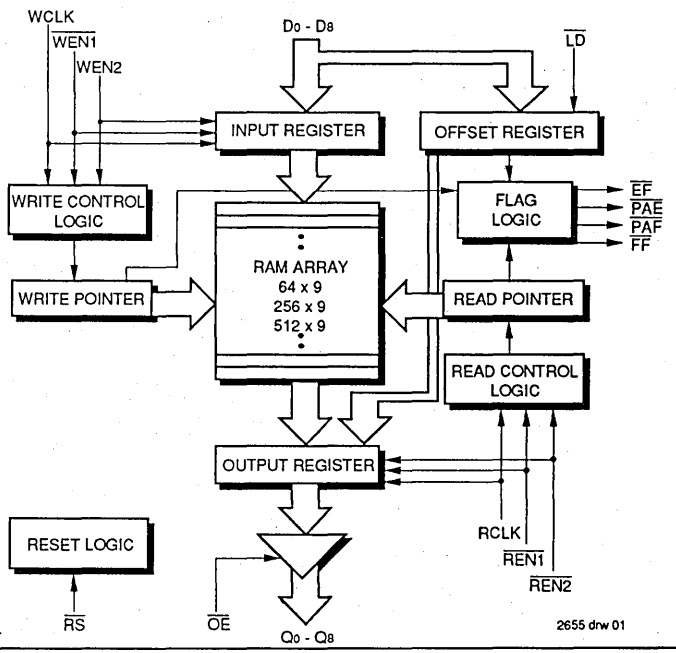
The IDT72201/72211/72420 SyncFIFO™ are very high-speed, low-power first-in, first-out (FIFO) memories with clocked read and write controls. The IDT72201/72211/72420 have a 256, 512, and 64 x 9-bit memory array, respectively. These FIFOs are applicable for a wide variety of data buffering needs such as graphics, local area networks (LANs) and interprocessor communication.

These FIFOs have 9-bit input and output ports. The input port is controlled by a free-running clock (WCLK), and two write enable pins ($\overline{WEN1}$, WEN2). Data is read into the Synchronous FIFO on every clock when the write enable pins are asserted. The output port is controlled by another clock pin (RCLK) and two read enable pins ($\overline{REN1}$, $\overline{REN2}$). The read clock can be tied to the write clock for single clock operation or the two clocks can run asynchronous of one another for dual clock operation. An output enable pin ($\overline{OE}$) is provided on the read port for three-state control of the output.

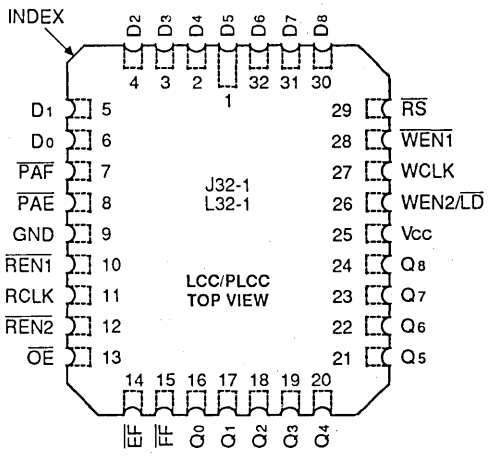
The Synchronous FIFOs have two fixed flags, Empty ($\overline{EF}$) and Full ($\overline{FF}$). Two programmable flags, Almost-Empty ($\overline{PAE}$) and Almost-Full ($\overline{PAF}$), are provided for improved system control. The programmable flags default to Empty+7 and Full-7 for $\overline{PAE}$ and $\overline{PAF}$, respectively. The programmable flag offset loading is controlled by a simple state machine and is initiated by asserting the load pin ($\overline{LD}$).

The IDT72201/72211/72420 are fabricated using IDT's high-speed submicron CEMOS™ technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



2655 drw 02

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D0-D8	Data Inputs	I	Data inputs for a 9-bit bus.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal read and write pointers are set to the first location of the RAM array, $\overline{FF}$ and $\overline{PAF}$ go high, and $\overline{PAE}$ and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up.
WCLK	Write Clock	I	Data is written into the FIFO on a LOW-to-HIGH transition of WCLK when the Write Enable(s) are asserted.
$\overline{WEN1}$	Write Enable 1	I	If the FIFO is configured to have programmable flags, $\overline{WEN1}$ is the only write enable pin. When $\overline{WEN1}$ is LOW, data is written into the FIFO on every LOW-to-HIGH transition WCLK. If the FIFO is configured to have two write enables, $\overline{WEN1}$ must be LOW and WEN2 must be HIGH to write data into the FIFO. Data will not be written into the FIFO if the $\overline{FF}$ is LOW.
WEN2/$\overline{LD}$	Write Enable 2/ Load	I	The FIFO is configured at reset to have two write enables or programmable flags. If WEN2/$\overline{LD}$ is HIGH at reset, this pin operates as a second write enable. If WEN2/$\overline{LD}$ is LOW at reset, this pin operates as a control to load and read the programmable flag offsets. If the FIFO is configured to have two write enables, $\overline{WEN1}$ must be LOW and WEN2 must be HIGH to write data into the FIFO. Data will not be written into the FIFO if the $\overline{FF}$ is LOW. If the FIFO is configured to have programmable flags, WEN2/$\overline{LD}$ is held LOW to write or read the programmable flag offsets.
Q0-Q8	Data Outputs	O	Data outputs for a 9-bit bus.
RCLK	Read Clock	I	Data is read from the FIFO on a LOW-to-HIGH transition of RCLK when $\overline{REN1}$ and $\overline{REN2}$ are asserted.
$\overline{REN1}$	Read Enable 1	I	When $\overline{REN1}$ and $\overline{REN2}$ are LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{REN2}$	Read Enable 2	I	When $\overline{REN1}$ and $\overline{REN2}$ are LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the data output bus is active. If $\overline{OE}$ is HIGH, the output data bus will be in a high impedance state.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty and further data reads from the output are inhibited. When $\overline{EF}$ is HIGH, the FIFO is not empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{PAE}$	Programmable Almost-Empty Flag	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the offset programmed into the FIFO. The default offset at reset is Empty+7. $\overline{PAE}$ is synchronized to RCLK.
$\overline{PAF}$	Programmable Almost-Full Flag	O	When $\overline{PAF}$ is LOW, the FIFO is almost full based on the offset programmed into the FIFO. The default offset at reset is Full-7. $\overline{PAF}$ is synchronized to WCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full and further data writes into the input are inhibited. When $\overline{FF}$ is HIGH, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK.
Vcc	Power		One +5 volt power supply pin.
GND	Ground		One 0 volt ground pin.

2655 tbl 01

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +135	°C
I_{OUT}	DC Output Current	50	50	mA

2655 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}	Input Low Voltage Commercial & Military	—	—	0.8	V

2655 tbl 03

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	IDT72201 IDT72211 IDT72421 Commercial t_{CLK} = 15, 20, 25, 50ns			IDT72201 IDT72211 IDT72421 Military t_{CLK} = 20, 25, 50ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI}(1)	Input Leakage Current (Any Input)	-1	—	-1	-10	—	10	µA
I_{LO}(2)	Output Leakage Current	-10	—	10	-10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = -2 mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8 mA	—	—	0.4	—	—	0.4	V
I_{CC}(3)	Active Power Supply Current	—	—	140	—	—	160	mA

2655 tbl 04

NOTES:
1. Measurements with 0.4 ≤ V_{IN} ≤ V_{OUT}.
2. $\overline{OE}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Measurements are made with outputs open. Tested at f_{CLK} = 20MHz.

   Typical I_{CC1} = 65 + (f_{CLK} * 1.1/MHz) + (f_{CLK} * C_L * 0.03/MHz-pF) mA

   f_{CLK} = 1/t_{CLK}.

   C_L = external capacitive load (30pF typical)

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}(2)	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}(1,2)	Output Capacitance	V_{OUT} = 0V	10	pF

2655 tbl 05

NOTES:
1. With output deselected ($\overline{OE}$ = HIGH).
2. Characterized values, not currently tested.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	Com'l. IDT72201L15 IDT72211L15 IDT72421L15 Min.	Com'l. IDT72201L15 IDT72211L15 IDT72421L15 Max.	Commercial and Military IDT72201L20 IDT72211L20 IDT72421L20 Min.	Commercial and Military IDT72201L20 IDT72211L20 IDT72421L20 Max.	Commercial and Military IDT72201L25 IDT72211L25 IDT72421L25 Min.	Commercial and Military IDT72201L25 IDT72211L25 IDT72421L25 Max.	Commercial and Military IDT72201L50 IDT72211L50 IDT72421L50 Min.	Commercial and Military IDT72201L50 IDT72211L50 IDT72421L50 Max.	Unit
fS	Clock Cycle Frequency	—	66.7	—	50	—	40	—	20	MHz
tA	Data Access Time	2	10	2	12	3	15	3	25	ns
tCLK	Clock Cycle Time	15	—	20	—	25	—	50	—	ns
tCLKH	Clock High Time	6	—	8	—	10	—	20	—	ns
tCLKL	Clock Low Time	6	—	8	—	10	—	20	—	ns
tDS	Data Set-up Time	4	—	5	—	6	—	10	—	ns
tDH	Data Hold Time	1	—	1	—	1	—	2	—	ns
tENS	Enable Set-up Time	4	—	5	—	6	—	10	—	ns
tENH	Enable Hold Time	1	—	1	—	1	—	2	—	ns
tRS	Reset Pulse Width(1)	15	—	20	—	25	—	50	—	ns
tRSS	Reset Set-up Time	15	—	20	—	25	—	50	—	ns
tRSF	Reset to Flag Time and Output Time	—	15	—	20	—	25	—	50	ns
tOLZ	Output Enable to Output in Low Z(2)	0	—	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	3	8	3	10	3	13	3	28	ns
tOHZ	Output Enable to Output in High Z(2)	3	8	3	10	3	13	3	28	ns
tWFF	Write Clock to Full Flag	—	10	—	12	—	15	—	30	ns
tREF	Read Clock to Empty Flag	—	10	—	12	—	15	—	30	ns
tPAF	Write Clock to Programmable Almost-Full Flag	—	10	—	12	—	15	—	30	ns
tPAE	Read Clock to Programmable Almost-Empty Flag	—	10	—	12	—	15	—	30	ns
tSKEW1	Skew Time Between Read Clock and Write Clock for Empty Flag and Full Flag	6	—	8	—	10	—	15	—	ns
tSKEW2	Skew Time Between Read Clock and Write Clock for Programmable Almost-Empty Flag and Programmable Almost-Full Flag	15	—	18	—	20	—	30	—	ns

2655 tbl 06

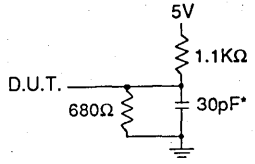
NOTES:
1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

6

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2655 tbl 07



or equivalent circuit

Figure 1. Output Load

*Includes jig and scope capacitances.

2655 drw 03

SIGNAL DESCRIPTIONS

INPUTS:

Data In (D_0 - D_8) — Data inputs for 9-bit wide data.

CONTROLS:

Reset ($\overline{RS}$) — Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place. The Full Flag ($\overline{FF}$) and Programmable Almost-Full Flag ($\overline{PAF}$) will be reset to high after t_{RSF}. The Empty Flag ($\overline{EF}$) and Programmable Almost-Empty Flag ($\overline{PAE}$) will be reset to low after t_{RSF}. During reset, the output register is initialized to all zeros and the offset registers are initialized to their default values.

Write Clock (WCLK) — A write cycle is initiated on the LOW-to-HIGH transition of the write clock (WCLK). Data set-up and hold times must be met in respect to the LOW-to-HIGH transition of the write clock (WCLK). The Full Flag ($\overline{FF}$) and Programmable Almost-Full Flag ($\overline{PAF}$) are synchronized with respect to the LOW-to-HIGH transition of the write clock (WCLK).

The write and read clocks can be asynchronous or coincident.

Write Enable 1 ($\overline{WEN1}$) — If the FIFO is configured for programmable flags, Write Enable 1 ($\overline{WEN1}$) is the only enable control pin. In this configuration, when Write Enable 1 ($\overline{WEN1}$) is low, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

In this configuration, when Write Enable 1 ($\overline{WEN1}$) is high, the input register holds the previous data and no new data is allowed to be loaded into the register.

If the FIFO is configured to have two write enables, which allows for depth expansion, there are two enable control pins. See Write Enable 2 paragraph below for operation in this configuration.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read cycle, the Full Flag ($\overline{FF}$) will go high after t_{WFF}, allowing a valid write to begin. Write Enable 1 ($\overline{WEN1}$) is ignored when the FIFO is full.

Read Clock (RCLK) — Data can be read on the outputs on the LOW-to-HIGH transition of the read clock (RCLK). The Empty Flag ($\overline{EF}$) and Programmable Almost-Empty Flag ($\overline{PAE}$) are synchronized with respect to the LOW-to-HIGH transition of the read clock (RCLK).

The write and read clocks can be asynchronous or coincident.

Read Enables ($\overline{REN1}$, $\overline{REN2}$) — When both Read Enables ($\overline{REN1}$, $\overline{REN2}$) are low, data is read from the RAM array to the output register on the LOW-to-HIGH transition of the read clock (RCLK).

When either Read Enable ($\overline{REN1}$, $\overline{REN2}$) is high, the output register holds the previous data and no new data is allowed to be loaded into the register.

When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go high after t_{REF} and a valid read can begin. The Read Enables ($\overline{REN1}$, $\overline{REN2}$) are ignored when the FIFO is empty.

Output Enable ($\overline{OE}$) — When Output Enable ($\overline{OE}$) is enabled (LOW), the parallel output buffers receive data from the output register. When Output Enable ($\overline{OE}$) is disabled (HIGH), the Q output data bus is in a high-impedance state.

Write Enable 2/Load (WEN2/$\overline{LD}$) — This is a dual-purpose pin. The FIFO is configured at Reset to have programmable flags or to have two write enables, which allows depth expansion. If Write Enable 2/Load (WEN2/$\overline{LD}$) is set high at Reset ($\overline{RS}$=low), this pin operates as a control to load and read the programmable flag offsets.

If the FIFO is configured to have two write enables, when Write Enable ($\overline{WEN1}$) is low and Write Enable 2/Load (WEN2/$\overline{LD}$) is high, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

In this configuration, when Write Enable ($\overline{WEN1}$) is high and/or Write Enable 2/Load (WEN2/$\overline{LD}$) is low, the input register holds the previous data and no new data is allowed to be loaded into the register.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read cycle, the Full Flag ($\overline{FF}$) will go high after t_{WFF}, allowing a valid write to begin. Write Enable 1 ($\overline{WEN1}$) and Write Enable 2/Load (WEN2/$\overline{LD}$) are ignored when the FIFO is full.

The FIFO is configured to have programmable flags when the Write Enable 2/Load (WEN2/$\overline{LD}$) is set low at Reset ($\overline{RS}$=low). The IDT72201/72211/72420 devices contain four 8-bit offset registers which can be loaded with data on the inputs, or read on the outputs. See Figure 3 for details of the size of the registers and the default values.

If the FIFO is configured to have programmable flags when the Write Enable 1 ($\overline{WEN1}$) and Write Enable 2/Load (WEN2/$\overline{LD}$) are set low, data on the inputs D is written into the Empty (Least Significant Bit) offset register on the first LOW-to-HIGH transition of the write clock (WCLK). Data is written into the Empty (Most Significant Bit) offset register on the second LOW-to-HIGH transition of the write clock (WCLK), into the Full (Least Significant Bit) offset register on the third transition, and into the Full (Most Significant Bit) offset register on the fourth transition. The fifth transition of the write clock (WCLK) again writes to the Empty (Least Significant Bit) offset register.

However, writing all offset registers does not have to occur at one time. One or two offset registers can be written and then by bringing the Write Enable 2/Load (WEN2/$\overline{LD}$) pin high, the FIFO is returned to normal read/write operation. When the Write Enable 2/Load (WEN2/$\overline{LD}$) pin is set low, and Write Enable 1 ($\overline{WEN1}$) is low, the next offset register in sequence is written.

The contents of the offset registers can be read on the output lines when the Write Enable 2/Load (WEN2/$\overline{LD}$) pin is set low and both Read Enables ($\overline{REN1}$, $\overline{REN2}$) are set low. Data can be read on the LOW-to-HIGH transition of the read clock (RCLK).

A read and write should not be performed simultaneously to the offset registers.

$\overline{LD}$	$\overline{WEN1}$	WCLK[1]	Selection
0	0	↑	Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)
0	1	↑	No Operation
1	0	↑	Write Into FIFO
1	1	↑	No Operation

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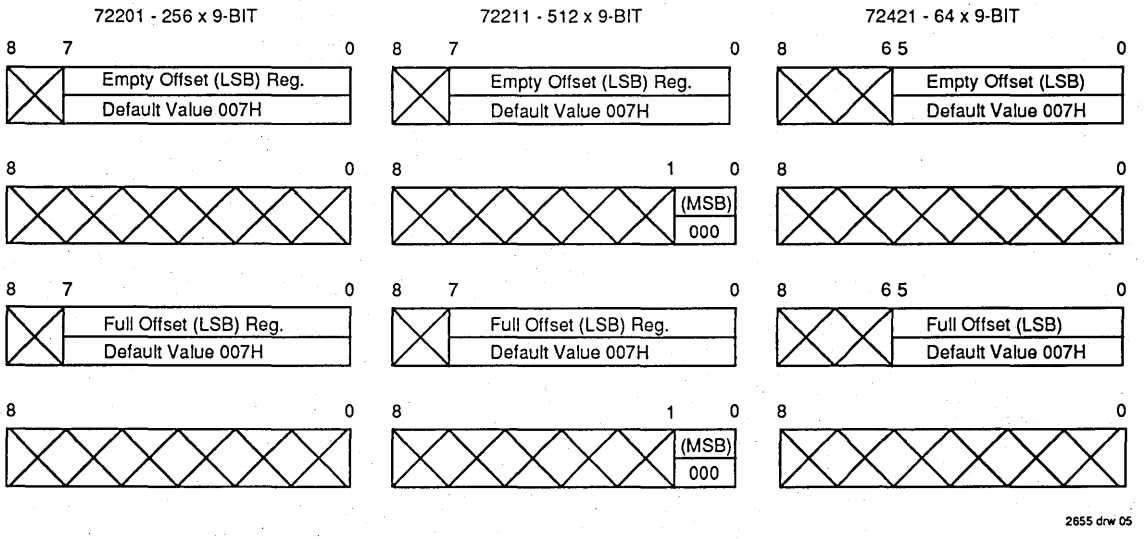
NOTE:
1. The same selection sequence applies to reading from the registers. $\overline{REN1}$ and $\overline{REN2}$ are enabled and read is performed on the LOW-to-HIGH transition of RCLK.

Figure 2. Write Offset Register



2655 drw 05

Figure 3. Offset Register Location and Default Values

OUTPUTS:

Full Flag ($\overline{FF}$) — The Full Flag ($\overline{FF}$) will go low, inhibiting further write operation, when the device is full. If no reads are performed after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go low after 256 writes for the IDT72201, 512 writes for the IDT72211, and 64 writes for the IDT72421.

The Full Flag ($\overline{FF}$) is synchronized with respect to the LOW-to-HIGH transition of the write clock (WCLK).

Empty Flag ($\overline{EF}$) — The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating the device is empty.

The Empty Flag ($\overline{EF}$) is synchronized with respect to the LOW-to-HIGH transition of the read clock (RCLK).

Programmable Almost-Full Flag ($\overline{PAF}$) — The Programmable Almost-Full Flag ($\overline{PAF}$) will go low when the FIFO reaches the Almost-Full condition. If no reads are performed after Reset ($\overline{RS}$), the Programmable Almost-Full Flag ($\overline{PAF}$) will go low after (256-m) writes for the IDT72201, (512-m) writes for the IDT72211, and (64-m) writes for the IDT72421. The offset "m" is defined in the Full offset registers.

If there is no Full offset specified, the Programmable Almost-Full Flag ($\overline{PAF}$) will go low at Full-7 words.

The Programmable Almost-Full Flag ($\overline{PAF}$) is synchronized with respect to the LOW-to-HIGH transition of the write clock (WCLK).

Programmable Almost-Empty Flag ($\overline{PAE}$) — The Programmable Almost-Empty Flag ($\overline{PAE}$) will go low when the read pointer is "n+1" locations less than the write pointer. The offset "n" is defined in the Empty offset registers. If no reads are performed after Reset the Programmable Almost-Empty Flag ($\overline{PAE}$) will go high after "n+1" for the IDT72201/72211/72421.

If there is no Empty offset specified, the Programmable Almost-Empty Flag ($\overline{PAE}$) will go low at Empty+7 words.

The Programmable Almost-Empty Flag ($\overline{PAE}$) is synchronized with respect to the LOW-to-HIGH transition of the read clock (RCLK).

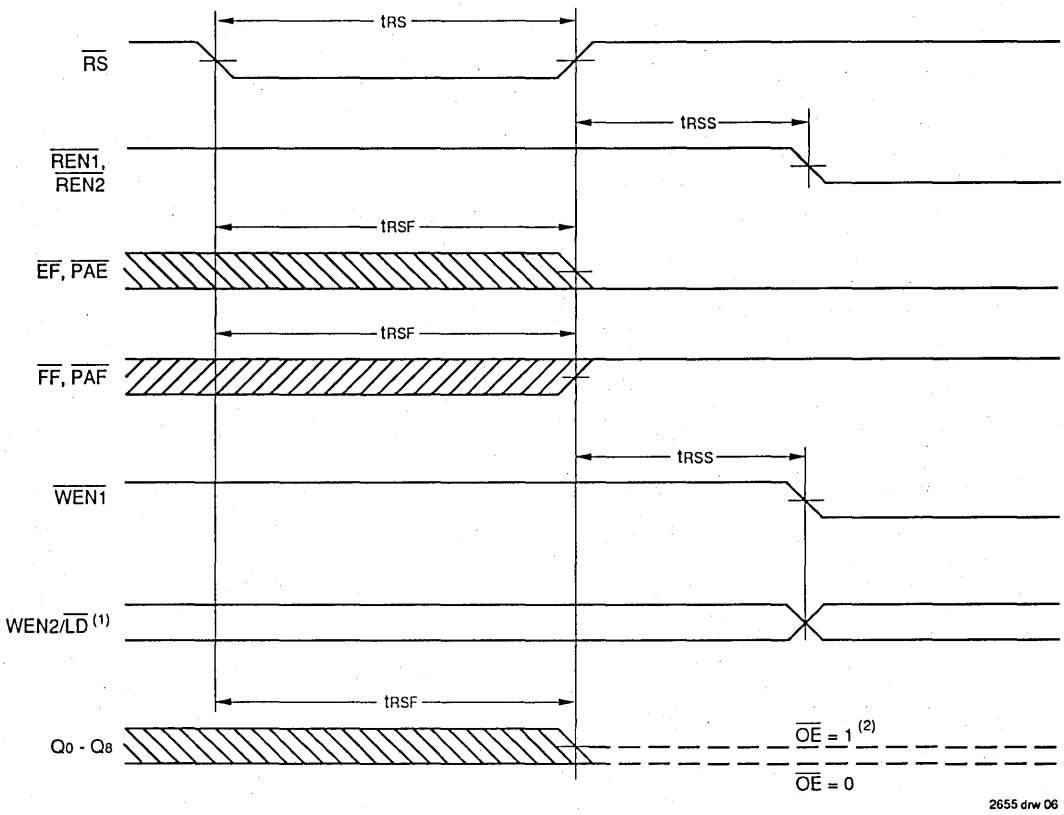
Data Outputs (Q_0 - Q_8) — Data outputs for a 9-bit wide data.

TABLE 1: STATUS FLAGS

NUMBER OF WORDS IN FIFO			$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
72201	72211	72421				
0	0	0	H	H	L	L
1 to n[1]	1 to n[1]	1 to n[1]	H	H	L	H
(n+1) to (256-(m+1))	(n+1) to (512-(m+1))	(n+1) to (64-(m+1))	H	H	H	H
(256-m)[2] to 255	(512-m)[2] to 511	(64-m)[2] to 63	H	L	H	H
256	512	64	L	L	H	H

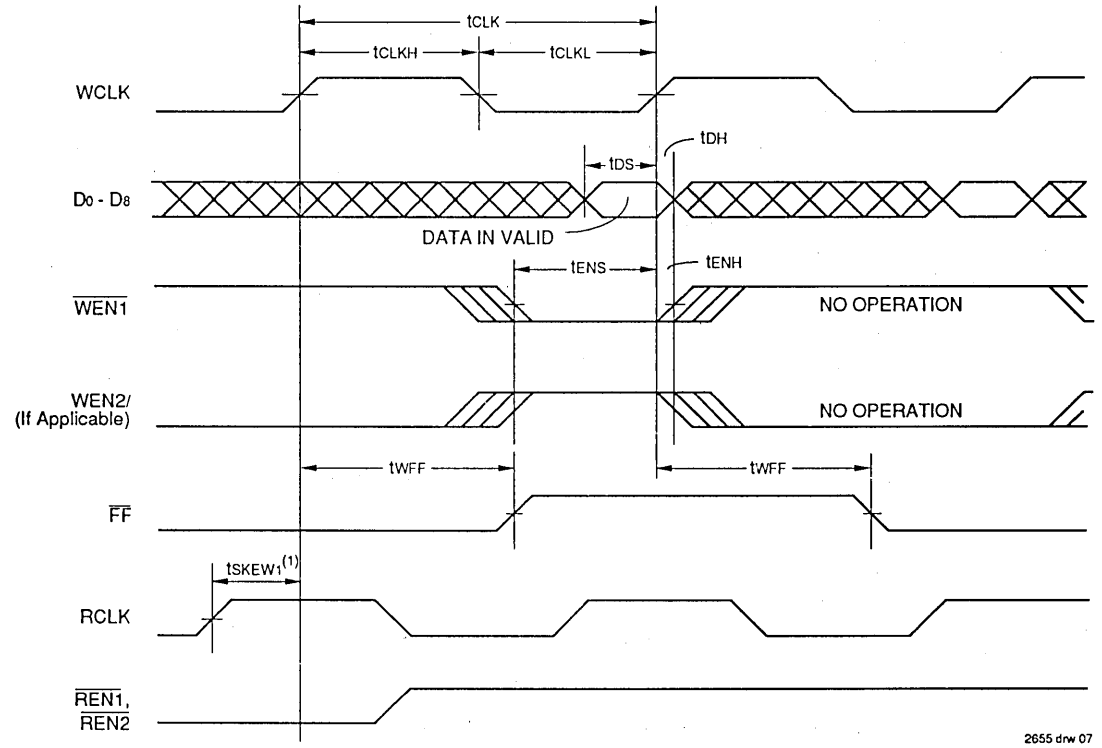
2655 tbl 08

NOTES:
1. n = Empty Offset (n = 7 default value)
2. m = Full Offset (m = 7 default value)



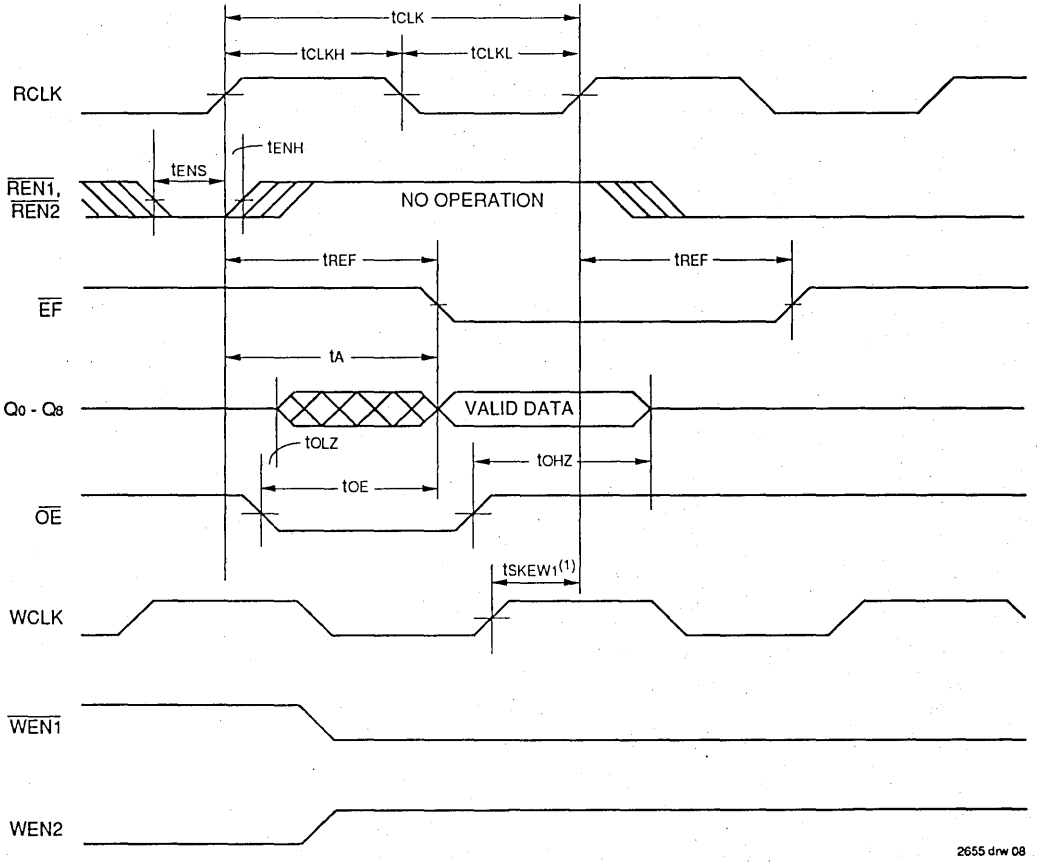
NOTES:
1. Holding WEN2/$\overline{LD}$ high during reset will make the pin act as a second write enable pin. Holding WEN2/$\overline{LD}$ low during reset will make the pin act as a load enable for the programmable flag offset registers.
2. After reset, the outputs will be low if $\overline{OE}$ = 0 and tri-state if $\overline{OE}$ = 1.
3. The clocks (RCLK, WCLK) can be free-running furing reset.

Figure 4. Reset Timing



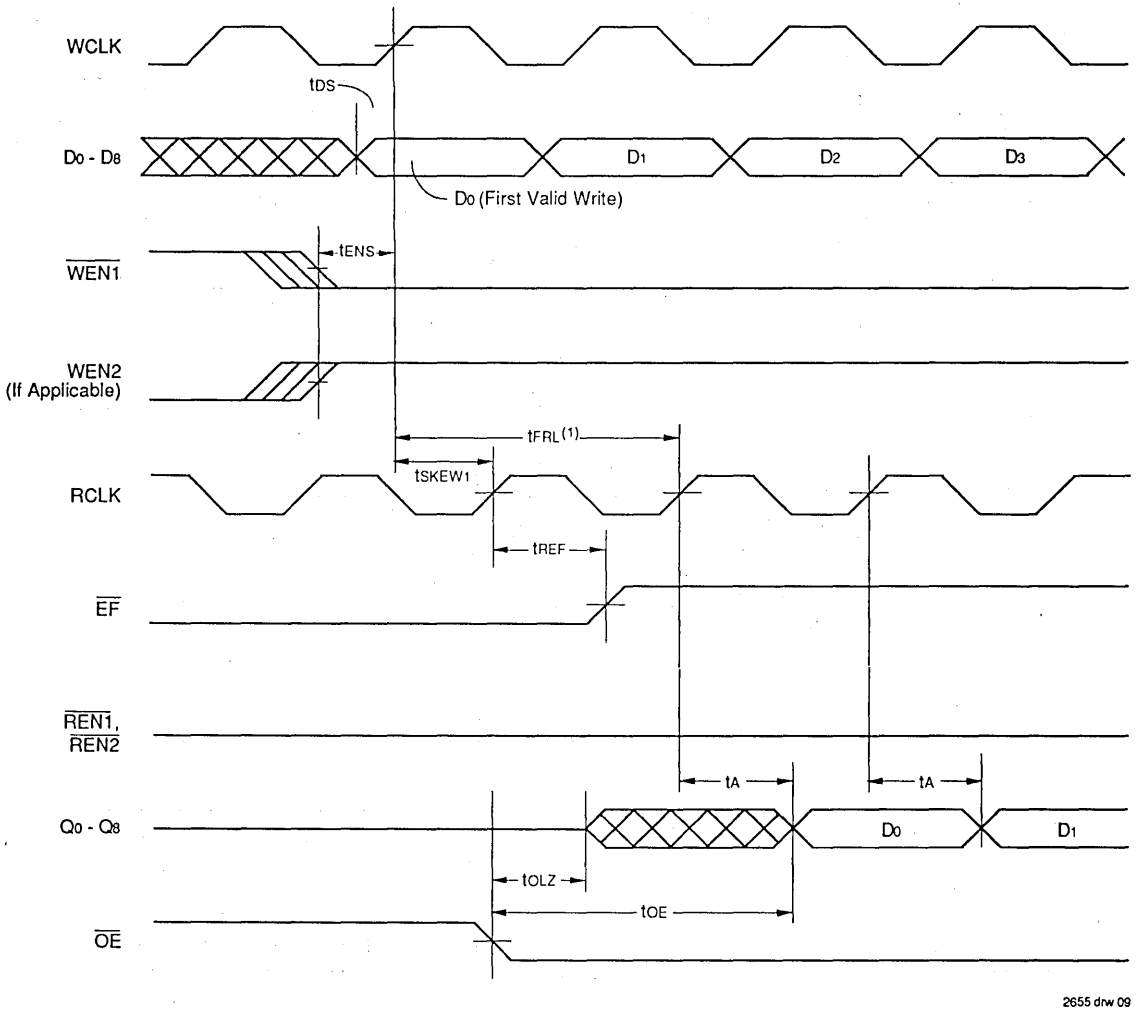
NOTE:
1. tSKEW1 is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{FF}$ to change during the current clock cycle. If the time between

Figure 5. Write Cycle Timing



NOTE:
1. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{EF}$ to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{EF}$ may not change state until the next RCLK edge. Figure 6. Read Cycle Timing

Figure 6. Read Cycle Timing



NOTE:
1. When $t_{SKEW1} \geq$ minimum specification, $t_{FRL} = t_{CLK} + t_{SKEW1}$
   $t_{SKEW1} <$ minimum specification, $t_{FRL} = 2t_{CLK} + t_{SKEW1}$
   The Latency Timings apply only at the Empty Boundary ($\overline{EF}$ = LOW).

Figure 7. First Data Word Latency Timing

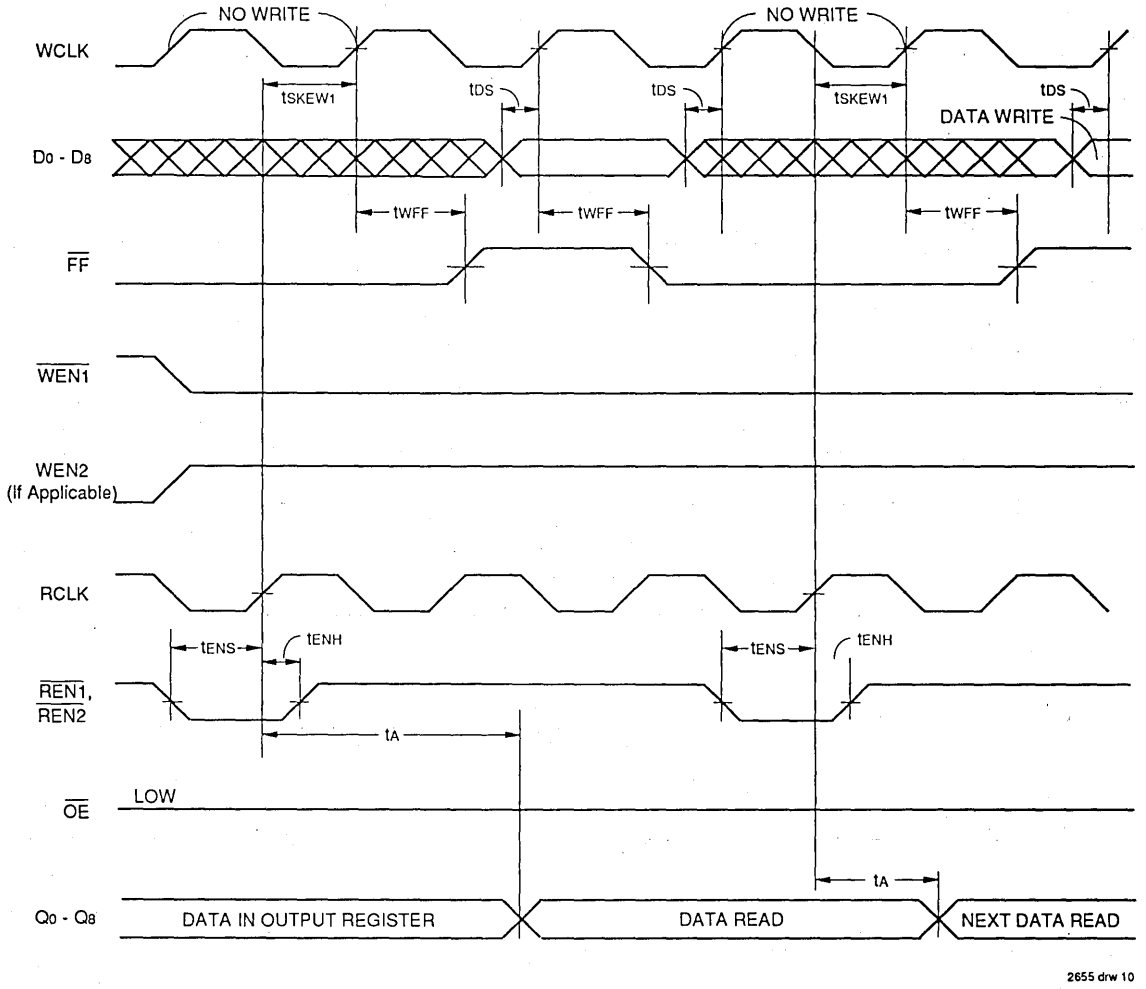
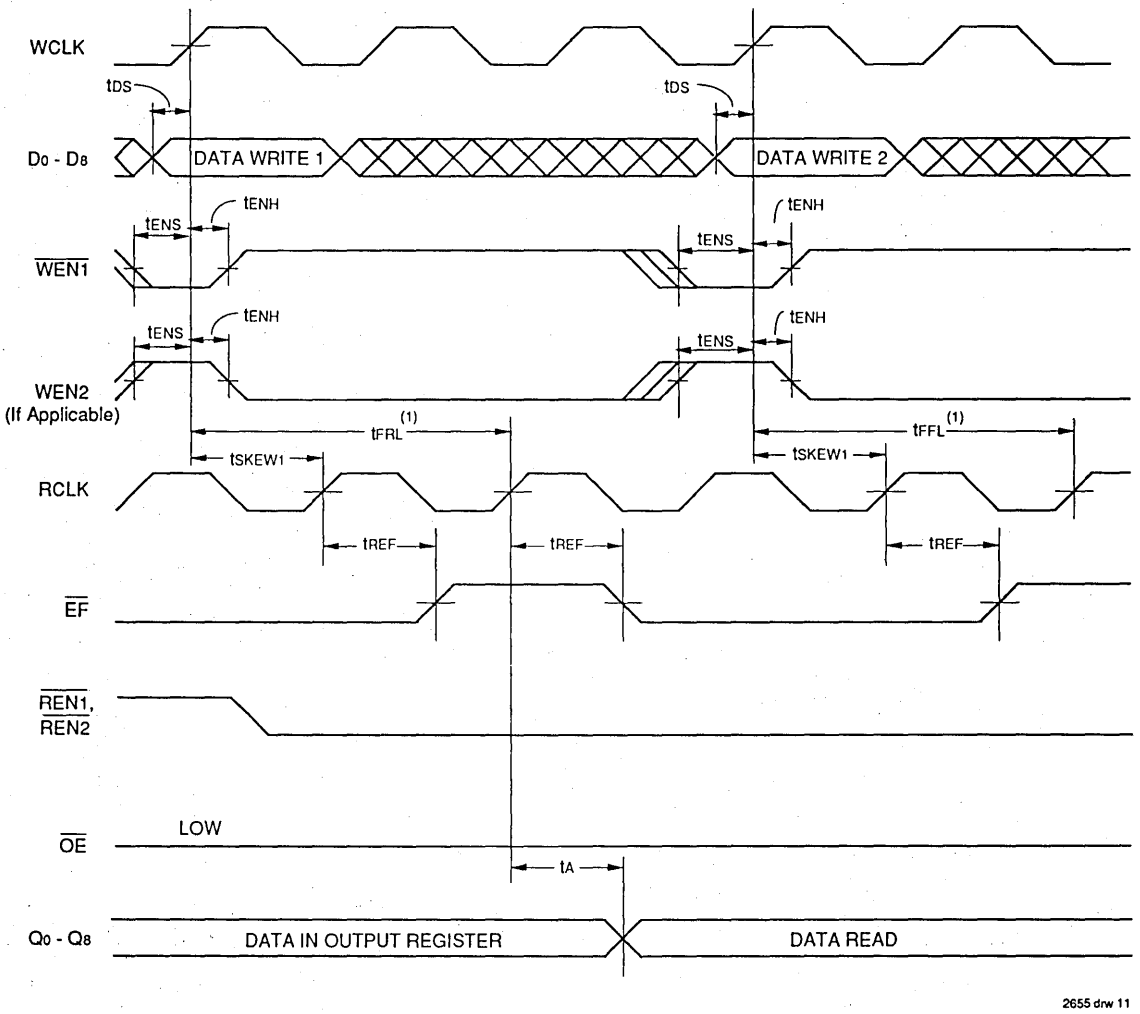
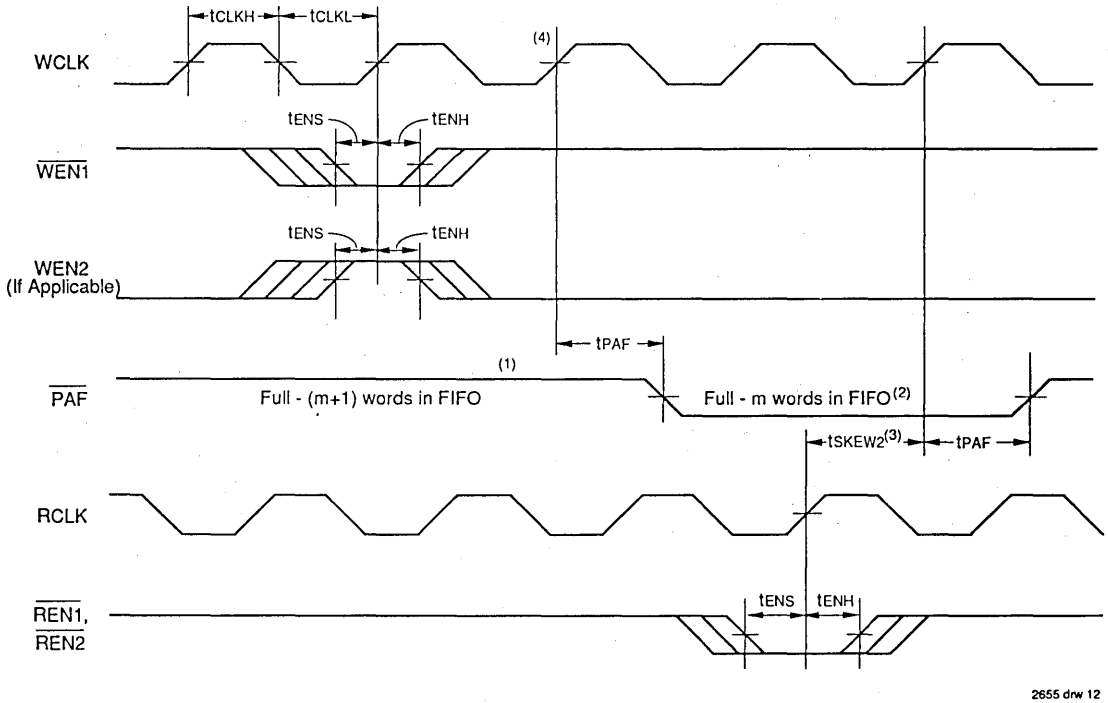


Figure 8. Full Flag Timing



NOTE:
1. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} maximum = $t_{CLK} + t_{SKEW1}$
   $t_{SKEW1} <$ minimum specification, t_{FRL} maximum = $2t_{CLK} + t_{SKEW1}$
   The Latency Timings apply only at at the Empty Boundary ($\overline{EF}$ + LOW).

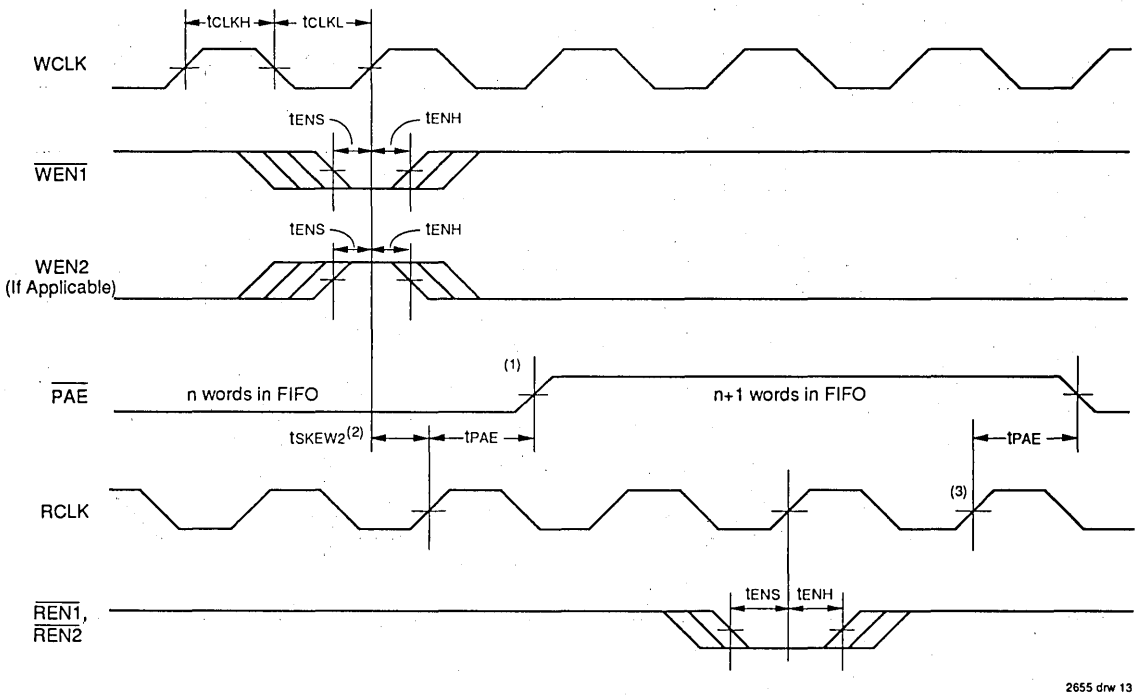
Figure 9. Empty Flag Timing



NOTES:
1. PAF offset = m.
2. 256 - m words in FIFO for IDT72201. 512 - m words for IDT72211. 64 - m words in FIFO for IDT72421.
3. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{PAF}$ to change during that clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then $\overline{PAF}$ may not change state until the next WCLK rising edge.
4. If a write is performed on this rising edge of the write clock, there will be Full - (m-1) words in the FIFO when $\overline{PAF}$ goes low.

6

Figure 10. Programmable Full Flag Timing



NOTES:
1. PAE offset = n.
2. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{PAE}$ to change during that clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{PAE}$ may not change state until the next RCLK rising edge.
3. If a read is performed on this rising edge of the read clock, there will be Empty + (n-1) words in the FIFO when $\overline{PAE}$ goes low.

Figure 11. Programmable Empty Flag Timing

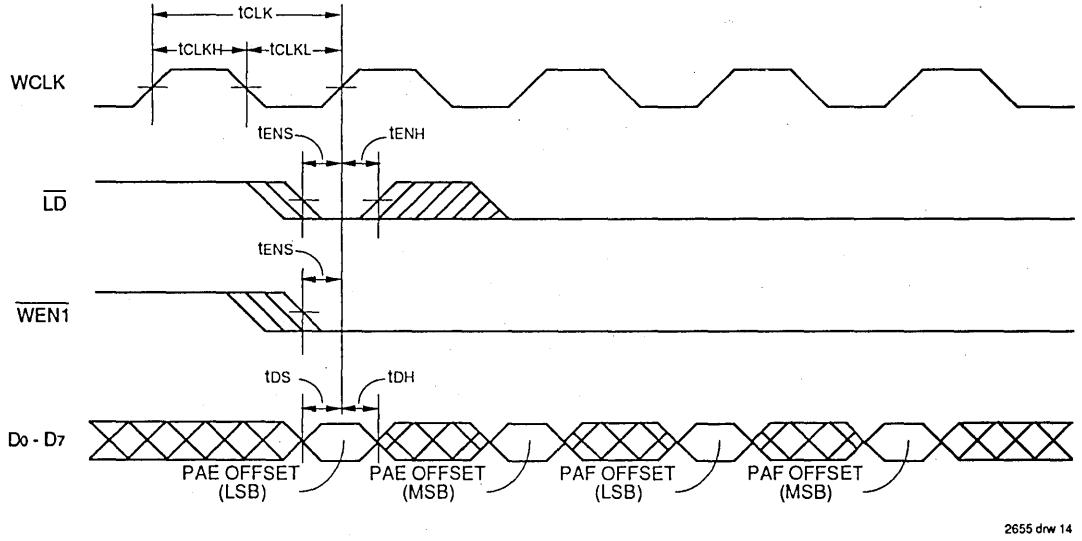


Figure 12. Write Offset Registers Timing

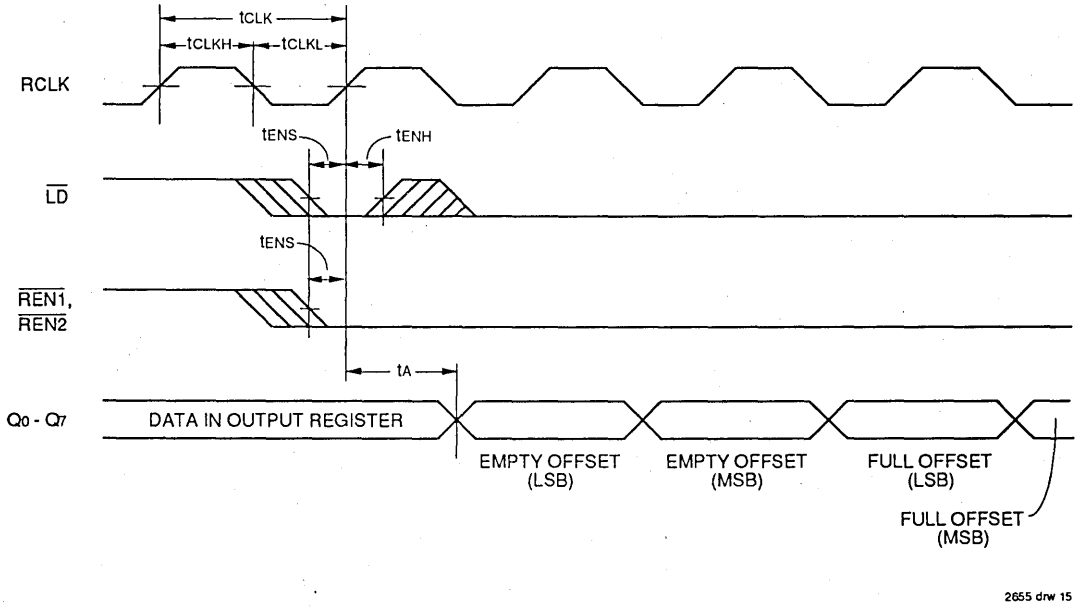
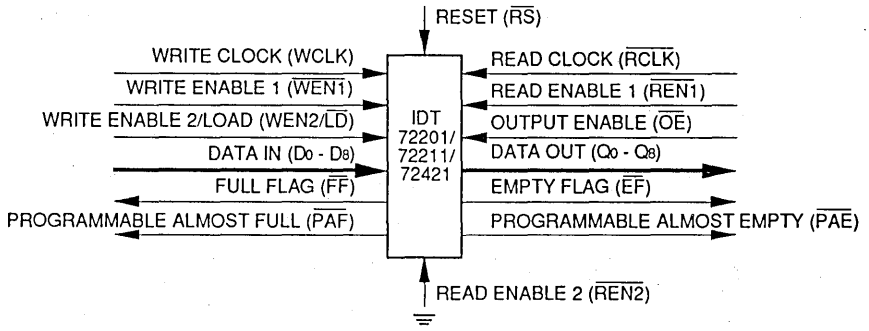


Figure 13. Read Offset Registers Timing

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION - A single IDT72201/72211/72421 may be used when the application requirements are for 256/512/64 words or less. When the IDT72201/72211/72421 are in a Single Device Configuration, the Read Enable 2 ($\overline{REN2}$) control input can be grounded (see Figure 14). In this configuration, the Write Enable 2/Load (WEN2/LD) pin is set low at Reset so that the pin operates as a control to load and read the programmable flag offsets.



2655 drw 16

Figure 14. Block Diagram of Single 256 x 9/512 x 9/64 x 9 Synchronous FIFO

WIDTH EXPANSION CONFIGURATION - Word width may be increased simply by connecting the corresponding input controls signals of multiple devices. Status flags ($\overline{EF}$, $\overline{PAE}$, $\overline{PAF}$ and $\overline{FF}$) can be detected from any one device. Figure 15 demonstrates a 18-bit word width by using two IDT72201/72211/72421s. Any word width can be attained by adding additional IDT72201/72211/72421s.

When the IDT72201/72211/72421 are in a Width Expansion Configuration, the Read Enable 2 ($\overline{REN2}$) control input can be grounded (see Figure 15). In this configuration, the Write Enable 2/Load (WEN2/LD) pin is set low at Reset so that the pin operates as a control to load and read the programmable flag offsets.

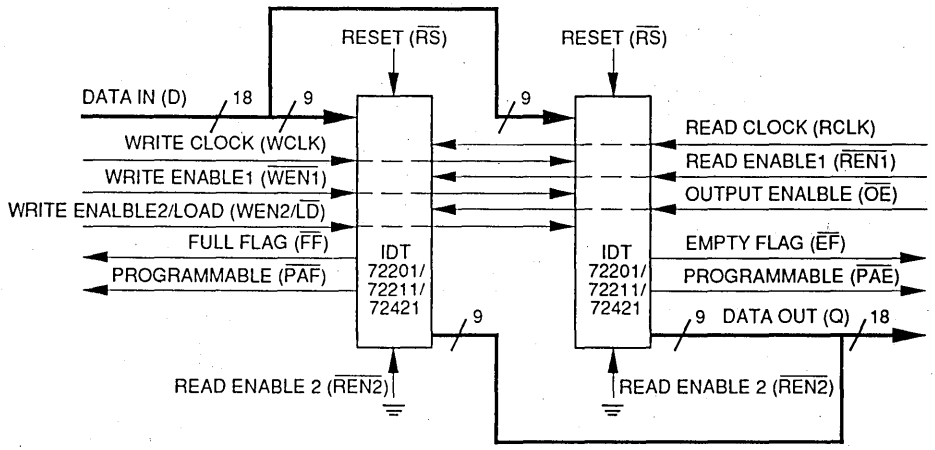


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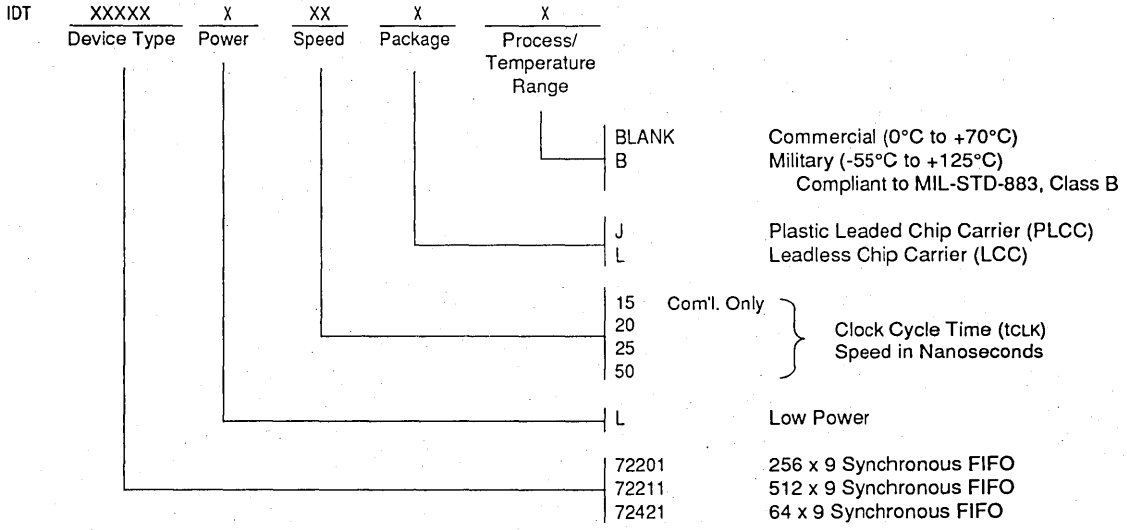
Figure 15. Block Diagram of 256 x 18/512 x 18/64 x 18 Synchronous FIFO Used in a Width Expansion Configuration

DEPTH EXPANSION - The IDT7221/72211/72421 can be adapted to applications when the requirements are for greater than 256/512/64 words. The existence of two enable pins on the read and write port allow depth expansion. The Write Enable 2/Load pin is used as a second write enable in a depth expansion configuration thus the Programmable flags are set to the default values. Depth expansion is possible by using one enable input for system control while the other enable input is controlled by expansion logic to direct the flow of data. A typical application would have the expansion logic alternate data access from one device to the next in a sequential manner. The IDT72201/72211/72421 operates in the Depth Expansion configuration when the following conditions are met:

1. The WEN2/$\overline{LD}$ pin is held high during Reset so that this pin operates a second Write Enable.
2. External logic is used to control the flow of data.

Please see the Applicatioin Note" DEPTH EXPANSION USING 72211 SYNCHRONOUS FIFOs" for details of this configuration.

ORDERING INFORMATION



2655 drw 18

6

Integrated Device Technology, Inc.

CMOS PARALLEL SyncFIFO™ (CLOCKED FIFO) 512 x 18-BIT & 1024 x 18-BIT

PRELIMINARY
IDT72215A
IDT72225A

FEATURES:

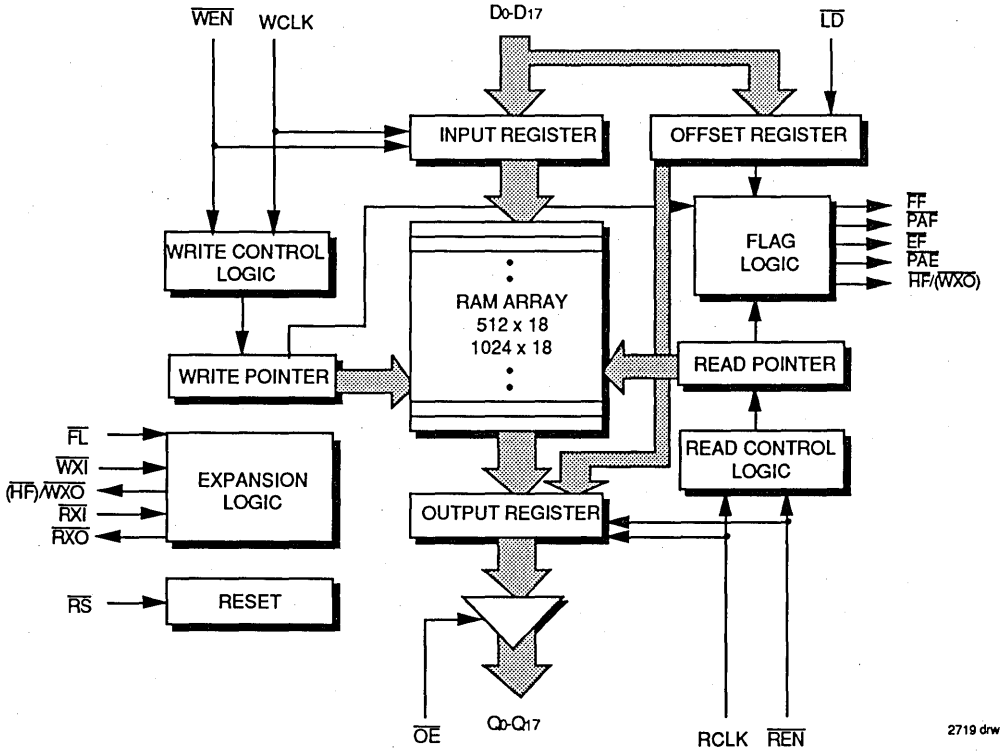
- 512 x 18-bit and 1024 x 18-bit memory array structures
- 20ns read / write cycle time
- Easily expandable in depth and width
- Read and write clocks can be asynchronous or coincident
- Dual-port zero fall-through time architecture
- Programmable almost-empty and almost-full flags
- Empty and Full flags signal FIFO status
- Half-Full flag capability in a single device configuration
- Output enable puts output data bus in high impedance
- First device controls all flag logic in depth expansion
- Produced with advanced submicron CEMOS™ technology
- Available in a 68-lead pin grid array (PGA), and plastic leaded chip carrier (PLCC)
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72215A and IDT72225A are very high speed, low-power first-in, first-out (FIFO) memories with clocked read and write controls. The IDT72215A has a 512 x 18-bit memory array, while the IDT72225A has a 1024 x 18-bit memory array. These FIFOs are applicable for a wide variety of data buffering needs, such as optical disk controllers, local area networks (LANs), and interprocessor communication.

Both FIFOs have 18-bit input and output ports. The input port is controlled by a free-running clock (WCLK), and a data input enable pin ($\overline{WEN}$). Data is read into the synchonous FIFO on every clock when $\overline{WEN}$ is asserted. The output port is controlled by another clock pin (RCLK) and another enable pin ($\overline{REN}$). The read clock can be tied to the write clock for single clock operation or the two clocks can run asynchronous of one another for dual clock operation. An output enable pin ($\overline{OE}$) is provided on the read port for three-state control of the output.

FUNCTIONAL BLOCK DIAGRAM



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DESCRIPTION (Continued):

The synchronous FIFOs have two fixed flags, Empty ($\overline{EF}$) and Full ($\overline{FF}$), and two programmable flags, Almost-Empty ($\overline{PAE}$) and Almost-Full ($\overline{PAF}$). The offset loading of the programmable flags is controlled by a simple state machine, and is initiated by asserting the load pin ($\overline{LD}$). A Half-Full flag ($\overline{HF}$) is available when the FIFO is used in a single device configuration.

The IDT72215A and IDT72225A are depth expandable using a daisy-chain technique. The $\overline{XI}$ and $\overline{XO}$ pins are used to expand the FIFOs. To permit programmable flags in depth expansion, the first device indicated by setting $\overline{FL}$ to low, controls the flags.

The IDT72215A/72225A is fabricated using IDTs high speed submicron CEMOS technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

PIN CONFIGURATIONS

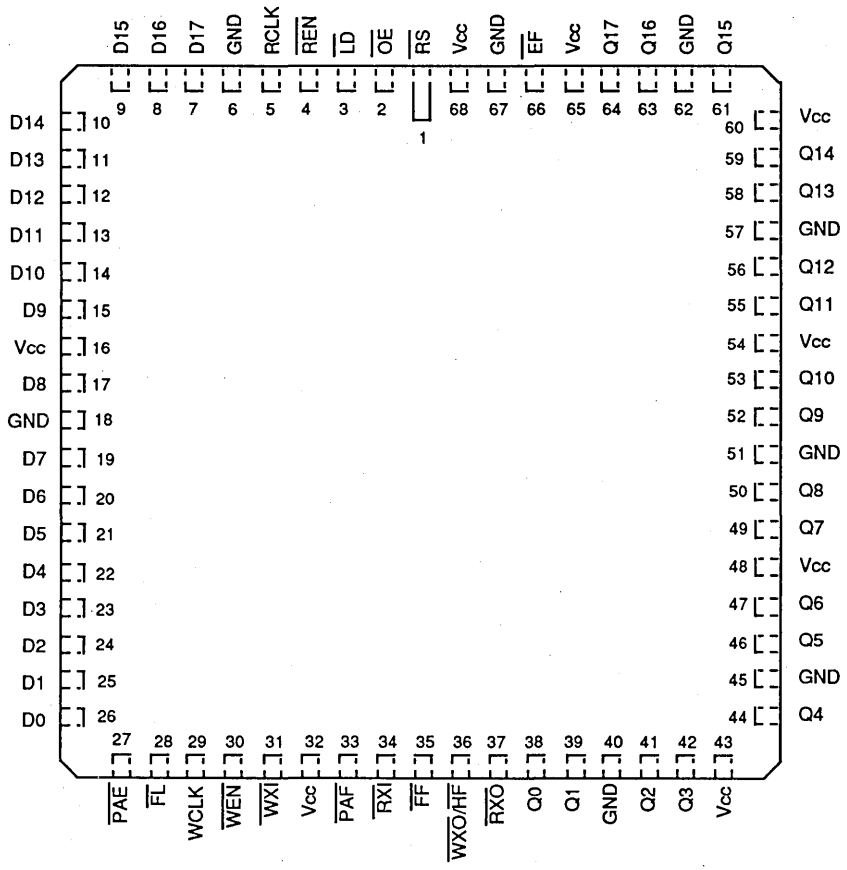
	A	B	C	D	E	F	G	H	J	K	L
11		Vcc	Q3	GND	Q0	$\overline{WXO/HF}$	$\overline{RXI}$	Vcc	$\overline{WEN}$	$\overline{FL}$	
10	GND	Q4	Q2	Q1	$\overline{RXO}$	$\overline{FF}$	$\overline{PAF}$	$\overline{WXI}$	WCLK	$\overline{PAE}$	D0
09	Q6	Q5								D2	D1
08	Q7	Vcc								D4	D3
07	GND	Q8								D6	D5
06	Q10	Q9								GND	D7
05	Q11	Vcc								Vcc	D8
04	GND	Q12								D10	D9
03	Q14	Q13								D12	D11
02	Vcc	Q15	Q16	Vcc	GND	$\overline{RS}$	$\overline{LD}$	RCLK	D17	D14	D13
01		GND	Q17	$\overline{EF}$	Vcc	$\overline{OE}$	$\overline{REN}$	GND	D16	D15	

Pin 1 Designator

2719 drw 02

PGA
TOP VIEW

PIN CONFIGURATIONS (Continued)



2719 drw 03

PLCC
TOP VIEW

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D_0 - D_{17}	Data Inputs	I	Data inputs for a 18-bit bus.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal read and write pointers are set to the first location of the RAM array, $\overline{FF}$ and $\overline{PAF}$ go high, and $\overline{PAE}$ and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up.
WCLK	Write Clock	I	Data is written into the FIFO on a LOW-to-HIGH transition of WCLK when Write Enable $\overline{WEN}$ is asserted (LOW).
$\overline{WEN}$	Write Enable	I	When $\overline{WEN}$ is LOW, data is written into the FIFO on every LOW-to-HIGH transition of WCLK. When $\overline{WEN}$ is high, the FIFO holds the previous data. Data will not be written into the FIFO if the $\overline{FF}$ is LOW.
RCLK	Read Clock	I	Data is read from the FIFO on a LOW-to-HIGH transition of RCLK when Read Enable $\overline{REN}$ is asserted (LOW).
$\overline{REN}$	Read Enable	I	When $\overline{REN}$ is LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. When $\overline{REN}$ is high, the output register holds the previous data. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the data output bus is active. If $\overline{OE}$ is HIGH, the output data bus will be in a high impedance state.
$\overline{LD}$	Load	I	When $\overline{LD}$ is LOW, data on the inputs D_0-D_{15} is written to the offset and depth registers on the LOW-to-HIGH transition of the WCLK, when $\overline{WEN}$ is LOW. When $\overline{LD}$ is LOW, data on the outputs Q_0-Q_{15} is read from the offset and depth registers on the LOW-to-HIGH transition of the RCLK, when $\overline{REN}$ is LOW.
$\overline{FL}$	First Load	I	In the single device or width expansion configuration, $\overline{FL}$ is grounded. In the depth expansion configuration, $\overline{FL}$ is grounded on the first device (first load device) and set to high for all other devices in the daisy chain.
$\overline{WXI}$	Write Expansion Input	I	In the single device or width expansion configuration, $\overline{WXI}$ is grounded. In the depth expansion configuration, $\overline{WXI}$ is connected to $\overline{WXO}$ (Write Expansion Out) of the previous device.
$\overline{RXI}$	Read Expansion Input	I	In the single device or width expansion configuration, $\overline{RXI}$ is grounded. In the depth expansion configuration, $\overline{RXI}$ is connected to $\overline{RXO}$ (Read Expansion Out) of the previous device.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty and further data reads from the output are inhibited. When $\overline{EF}$ is HIGH, the FIFO is not empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{PAE}$	Programmable Almost-Empty Flag	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the offset programmed into the FIFO. The default offset at reset is 1/8 full.
$\overline{PAF}$	Programmable Almost-Full Flag	O	When $\overline{PAF}$ is LOW, the FIFO is almost full based on the offset programmed into the FIFO. The default offset at reset is 7/8 full.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full and further data writes into the input are inhibited. When $\overline{FF}$ is HIGH, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK.
$\overline{WXO}/\overline{HF}$	Write Expansion Out/Half-Full Flag	O	In the single device or width expansion configuration, the device is more than half full when $\overline{HF}$ is LOW. In the depth expansion configuration, a pulse is sent from $\overline{WXO}$ to $\overline{WXI}$ of the next device when the last location in the FIFO is written.
$\overline{RXO}$	Read Expansion Out	O	In the depth expansion configuration, a pulse is sent from $\overline{RXO}$ to $\overline{RXI}$ of the next device when the last location in the FIFO is read.
Q_0 - Q_{17}	Data Outputs	O	Data outputs for a 18-bit bus.
V_{CC}	Power		Eight +5 volt power supply pins.
GND	Ground		Eight 0 volt ground pins.

2719 tbl 01

6

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +155	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2719 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

CAPACITANCE (TA = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Condition	Max.	Unit
CIN(2)	Input Capacitance	VIN = 0V	10	pF
COUT(1,2)	Output Capacitance	VOUT = 0V	10	pF

NOTES: 2719 tbl 03

1. With output deselected. ($\overline{OE}$ = high)
2. Characterized values, not currently tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Votage Commercial	2.0	—	—	V
VIH	Input High Votage Military	2.2	—	—	V
VIL(1)	Input Low Voltage Com'l. and Mil.	—	—	0.8	V

NOTE: 2719 tbl 04

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: VCC = 5.0V ± 10%, TA = 0°C to +70°C; Military: VCC = 5.0V ± 10%, TA = -55°C + 125°C)

Symbol	Parameter	IDT72215A IDT72225A Commercial tCLK = 20, 25, 50 ns			IDT72215A IDT72225A Military tCLK = 25, 30, 50 ns			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI} (1)	Input Leakage Current (any input)	–1	—	1	–10	—	10	µA
I_{LO} (2)	Output Leakage Current	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = –2 mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8 mA	—	—	0.4	—	—	0.4	V
I_{CC1} (3)	Active Power Supply Current	—	—	250	—	—	300	mA
I_{CC2} (3)	Average Standby Current (All Input = V_{CC} – 0.2V, except RCLK and WCLK which are free-running)	—	—	60	—	—	75	mA

NOTES: 2917 tbl 05

1. Measurements with 0.4 ≤ VIN ≤ VOUT.
2. $\overline{OE}$ ≥ VIH, 0.4 ≤ VOUT ≤ VCC.
3. Tested at f = 20 MHz.

AC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 5.0V ± 10%, TA = 0°C to +70°C; Military: Vcc = 5.0V ± 10%, TA = -55°C + 125°C)

Symbol	Parameter	Com'l. IDT72215L20 IDT72225L20		Com'l. & Mil. IDT72215L25 IDT72225L25		Mil. IDT72215L30 IDT72225L30		Com'l. & Mil. IDT72215L50 IDT72225L50		Unit
		Mlin.	Max.	Mlin.	Max.	Mlin.	Max.	Mlin.	Max.	
fS	Clock Cycle Frequency	—	50	—	40	—	33	—	20	MHz
tA	Data Access Time	2	14	3	15	3	18	3	25	ns
tCLK	Clock Cycle Time	20	—	25	—	30	—	50	—	ns
tCLKH	Clock High Time	8	—	10	—	12	—	20	—	ns
tCLKL	Clock Low Time	9	—	10	—	12	—	20	—	ns
tDS	Data Set-up Time	5	—	6	—	7	—	10	—	ns
tDH	Data Hold Time	1	—	1	—	1	—	2	—	ns
tENS	Enable Set-up Time	5	—	6	—	7	—	10	—	ns
tENH	Enable Hold Time	1	—	1	—	1	—	2	—	ns
tRS	Reset Pulse Width (1)	20	—	25	—	30	—	50	—	ns
tRSS	Reset Set-up Time (2)	12	—	15	—	18	—	30	—	ns
tRSF	Reset to Flag and Output Time	—	20	—	25	—	30	—	50	ns
tOLZ	Output Enable to Output in Low Z (2)	0	—	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	—	9	—	12	—	15	—	20	ns
tOHZ	Output Enable to Output in High Z (2)	1	9	1	12	1	15	1	20	ns
tWFF	Write Clock to Full Flag	—	14	—	16	—	18	—	30	ns
tREF	Read Clock to Empty Flag	—	12	—	15	—	18	—	30	ns
tPAF	Clock to Programmable Almost-Full Flag	—	20	—	22	—	24	—	35	ns
tPAE	Clock to Programmable Almost-Empty Flag	—	20	—	22	—	24	—	35	ns
tHF	Clock to Half-Full Flag	—	20	—	22	—	24	—	35	ns
tXO	Clock to Expansion Out	—	12	—	15	—	18	—	30	ns
tXI	Expansion In Pulse Width	8	—	10	—	12	—	20	—	ns
tXIS	Expansion In Set-Up Time	8	—	10	—	12	—	20	—	ns
tSKEW1	Skew time between Read Clock & Write Clock for Full Flag	14	—	16	—	18	—	20	—	ns
tSKEW2	Skew time between Read Clock & Write Clock for Empty Flag	14	—	16	—	18	—	20	—	ns

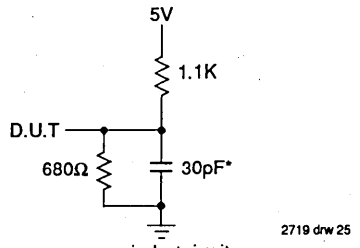
NOTES:
1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

2719 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2719 tbl 07



2719 drw 25

or equivalent circuit

Figure 1. Output Load

*Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D_0 - D_{17})
Data inputs for 18-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)
Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. The Full Flag ($\overline{FF}$), Half-Full Flag ($\overline{HF}$), and Programmable Almost-Full Flag ($\overline{PAF}$) will be reset to high after t_{RSF}. The Empty Flag ($\overline{EF}$) and Programmable Almost-Empty Flag ($\overline{PAE}$) will be reset to low after t_{RSF}.

WRITE CLOCK (WCLK)
A write cycle is initiated on the low-to-high transition of the write clock (WCLK). Data set-up and hold times must be met with respect to the low-to-high transition of the write clock (WCLK).

The write and read clocks can be asynchronous or coincident.

WRITE ENABLE ($\overline{WEN}$)
When Write Enable ($\overline{WEN}$) is low, data can be loaded into the input register and RAM array on the low-to-high transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

When Write Enable ($\overline{WEN}$) is high, the input register holds the previous data and no new data is loaded into the FIFO.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read cycle, the Full Flag ($\overline{FF}$) will go high after t_{WFF} allowing a write to begin. Write Enable ($\overline{WEN}$) is ignored when the FIFO is full.

READ CLOCK (RCLK)
Data can be read on the outputs on the low-to-high transition of the read clock (RCLK), when Output Enable ($\overline{OE}$) is set low.

The write and read clocks can be asynchronous or coincident.

READ ENABLE ($\overline{REN}$)
When Read Enable ($\overline{REN}$) is low, data is loaded into the RAM array to the output register on the low-to-high transition of the read clock (RCLK).

When Read Enable ($\overline{REN}$) is high, the output register holds the previous data and no new data is loaded into the register.

When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations. Once a write is performed, the Empty Flag ($\overline{EF}$) will go high after t_{REF} and a read can begin. Read Enable ($\overline{REN}$) is ignored when the FIFO is empty.

OUTPUT ENABLE ($\overline{OE}$)
When Output Enable ($\overline{OE}$) is enabled (low), the parallel output buffers receive data from the output register. When Output Enable ($\overline{OE}$) is disabled (high), the Q output data bus is in a high impedance state.

LOAD ($\overline{LD}$)
The IDT72215A and IDT72225A devices contain two 16-bit offset registers and a 6-bit depth register which can be loaded with data on the inputs, or read on the outputs. When the Load ($\overline{LD}$) pin is set low and $\overline{WEN}$ is set low, data on the inputs D0-D15 is written into the Empty offset register on the first low-to-high transition of the write clock (WCLK). When the Load ($\overline{LD}$) pin and Write Enable ($\overline{WEN}$) are held low then data is written into the Full offset register on the second low-to-high transition of the write clock (WCLK) and into the Depth register on the third transition. The fourth transition of the write clock (WCLK) again writes to the Empty offset register.

However, writing all offset registers does not have to occur at one time. One or two offset registers can be written and then by bringing the Load ($\overline{LD}$) pin high, the FIFO is returned to normal read/write operation. When the Load ($\overline{LD}$) pin is set low, and Write Enable ($\overline{WEN}$) is low, the next offset register in sequence is written.

When the Load pin is low and Write Enable is high, the offset register counter increments without writing into the offset registers.

The contents of the offset registers can be read on the output lines when the Load ($\overline{LD}$) pin is set low and $\overline{REN}$ is set low. Data can be read on the low-to-high transition of the read clock (RCLK) when $\overline{REN}$ is enabled (low).

A read and a write should not be performed simultaneously to the offset registers.

$\overline{LD}$	$\overline{WEN}$	WCLK[1]	SELECTION
0	0		WRITING TO OFFSET REGISTERS: EMPTY OFFSET FULL OFFSET DEPTH REGISTER
0	1		INCREMENTING OFFSET REGISTER COUNTER BUT NOT WRITING: EMPTY OFFSET FULL OFFSET DEPTH REGISTER
1	0		WRITE INTO FIFO
1	1		NO OPERATION

NOTE: 2719 drw 04
1. The same selection sequence applies to reading from the registers. $\overline{REN}$ is enabled and read is performed on the low-to-high transition of RCLK.

Figure 2. Write Offset Register

FIRST LOAD ($\overline{FL}$)

First Load ($\overline{FL}$) is grounded to indicate operation in the Single Device or Width Expansion mode. In the Depth Expansion configuration, First Load ($\overline{FL}$) is grounded to indicate it is the first device loaded and is set to high for all other devices in the daisy chain. (See Operating Configurations for further details.)

WRITE EXPANSION INPUT ($\overline{WXI}$)

This is a dual purpose pin. Write Expansion In ($\overline{WXI}$) is grounded to indicate operation in the Single Device or Width Expansion mode. Write Expansion In ($\overline{WXI}$) is connected to Write Expansion Out ($\overline{WXO}$) of the previous device in the Depth Expansion or Daisy Chain mode.

READ EXPANSION INPUT ($\overline{RXI}$)

This is a dual purpose pin. Read Expansion In ($\overline{RXI}$) is grounded to indicate operation in the Single Device or Width Expansion mode. Read Expansion In ($\overline{RXI}$) is connected to Read Expansion Out ($\overline{RXO}$) of the previous device in the Depth Expansion or Daisy Chain mode.

OUTPUTS:

FULL FLAG ($\overline{FF}$)

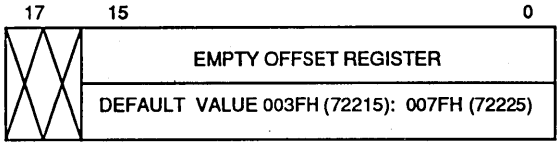
The Full Flag ($\overline{FF}$) will go low, inhibiting further write operation, indicating that the device is full. If no reads are performed after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go low after 512 writes for the IDT72215SA and 1024 writes for the IDT72225A.

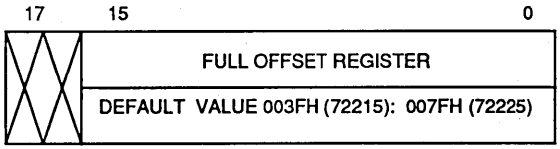
The Full Flag ($\overline{FF}$) is updated on the low-to-high transition of the write clock (WCLK).

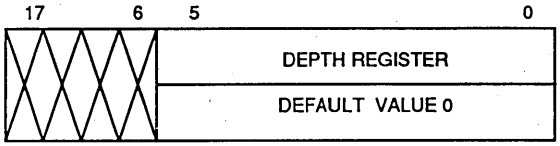
EMPTY FLAG ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating the device is empty.

The Empty Flag ($\overline{EF}$) is updated on the low-to-high transition the read clock (RCLK).







NOTE: 2719 drw 24
1. Any bits of the offset register not being programmed should be set to zero.

Figure 3. Offset Register Location and Default Values

IDT72215A		IDT72225A	
Data Loaded In Depth Register	Total Depth In Expansion Configuration	Data Loaded In Depth Register	Total Depth In Expansion Configuration
0 or 1	512	0 or 1	1024
2	1024	2	2048
3	1536	3	3072
4	2048	4	4096
5	2560	5	5120
6	3072	6	6144
•	•	•	•
•	•	•	•
•	•	•	•
32	16384	32	32768

Figure 4. Depth Register Programming

TABLE I — STATUS FLAGS

Number of Words in FIFO						
72215A	72225A	$\overline{FF}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{EF}$
0	0	H	H	H	L	L
1 to n[1]	1 to n[1]	H	H	H	L	H
(n+1) to 257	(n+1) to 513	H	H	H	H	H
258 to (512-(m+1))	514 to (1024-(m+1))	H	H	L	H	H
(512-m) [2] to 511	(1024-m) [2] to 1023	H	L	L	H	H
512	1024	L	L	L	H	H

NOTES:
1. n = Empty Offset (Default Values : 72215A n = 63 : 72225A n = 127)
2. m = Full Offset (Default Values : 72215A m = 63 : 72225A m = 127)

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PROGRAMMABLE ALMOST-FULL FLAG ($\overline{PAF}$)

The Programmable Almost-Full Flag ($\overline{PAF}$) will go low when FIFO reaches the Almost-Full condition. If no reads are performed after Reset ($\overline{RS}$), the Programmable Almost Full Flag ($\overline{PA}$) will go low after (512–m) writes for the IDT72215A and (1024–m) writes for the IDT72225A. The offset "m" is defined in the FULL offset register.

If there is no Full offset specified, the Programmable Almost-Full Flag ($\overline{PAF}$) will be low when the device is 7/8 full to completely full.

The Programmable Almost-Full Flag ($\overline{PAF}$) is asserted low on the low-to-high transition of the write clock (WCLK). $\overline{PAF}$ is reset to high on the low-to-high transition of the read clock (RCLK). Thus the $\overline{PAF}$ is asychronous.

PROGRAMMABLE ALMOST-EMPTY FLAG ($\overline{PAE}$)

The Programmable Almost-Empty Flag ($\overline{PAE}$) will go low when the read pointer is "n+1" locations less than the write pointer. The offset "n" is defined in the EMPTY offset register.

If there is no Empty offset specified, the Programmable Almost Empty Flag ($\overline{PAE}$) will be low when the device is completely empty to 1/8 full.

The Programmable Almost-Empty Flag ($\overline{PAE}$) is asserted low on the low-to-high transition of the read clock (RCLK). $\overline{PAE}$ is reset to high on the low-to-high transition of the write clock (WCLK). Thus the $\overline{PAF}$ is asychronous.

WRITE EXPANSION OUT/HALF-FULL FLAG ($\overline{WXO}/\overline{HF}$)

This is a dual-purpose output. In the Single Device and Width Expansion mode, when Write Expansion In ($\overline{WXI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled, and at the low-to-high transition of the next write cycle, the Half-Full Flag goes low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset to high by the low-to-high transition of the read clock (RCLK). The $\overline{HF}$ is asychronous.

In the Depth Expansion or Daisy Chain mode, Write Expansion In ($\overline{WXI}$) is connected to Write Expansion Out ($\overline{WXO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse when the previous device write to the last location of memory.

READ EXPANSION OUT ($\overline{RXO}$)

In the Depth Expansion or Daisy Chain configuration, Read Expansion In ($\overline{RXI}$) is connected to Read Expansion Out ($\overline{RXO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse when the previous device reads from the last location of memory.

DATA OUTPUTS (Q_0-Q_{17})

Q_0-Q_{17} are data outputs for 18-bit wide data.

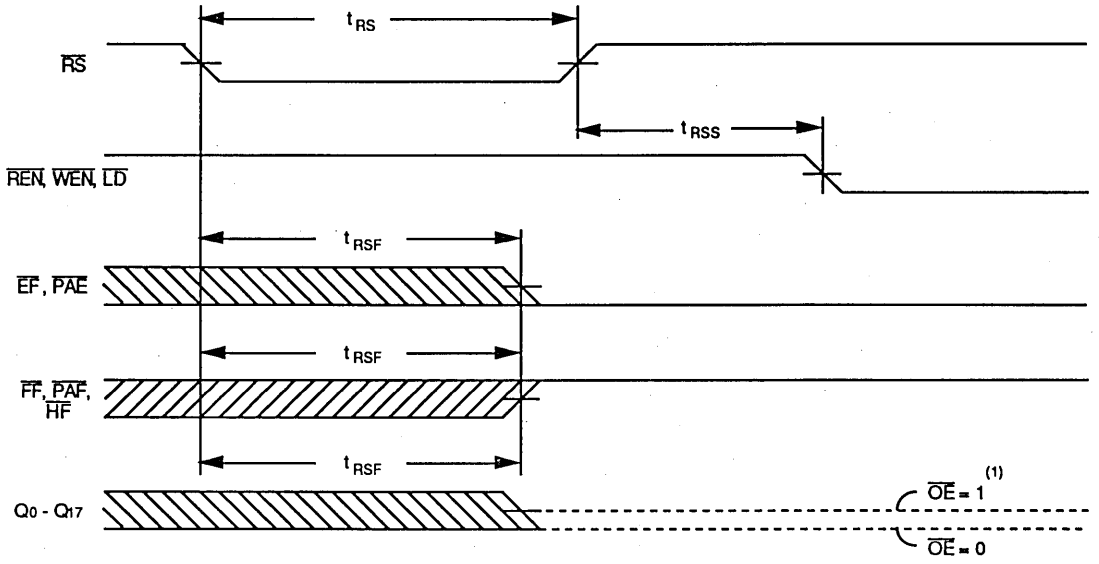


Figure 5. Reset Timing[2]

NOTE:
1. After reset, the outputs will be low if $\overline{OE}$ = 0 and tri-state if $\overline{OE}$ = 1.
2. The clocks (RCLK, WCLK) can be free-running during reset.

6

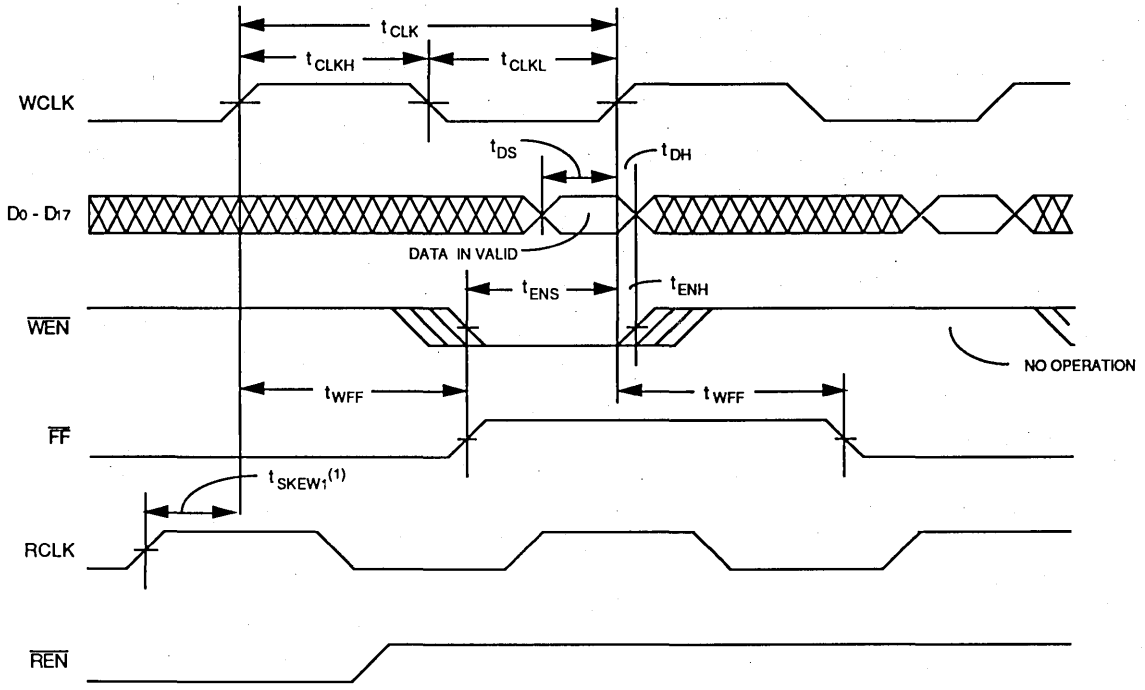


Figure 6. Write Cycle Timing

NOTE:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{FF}$ to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK edge.

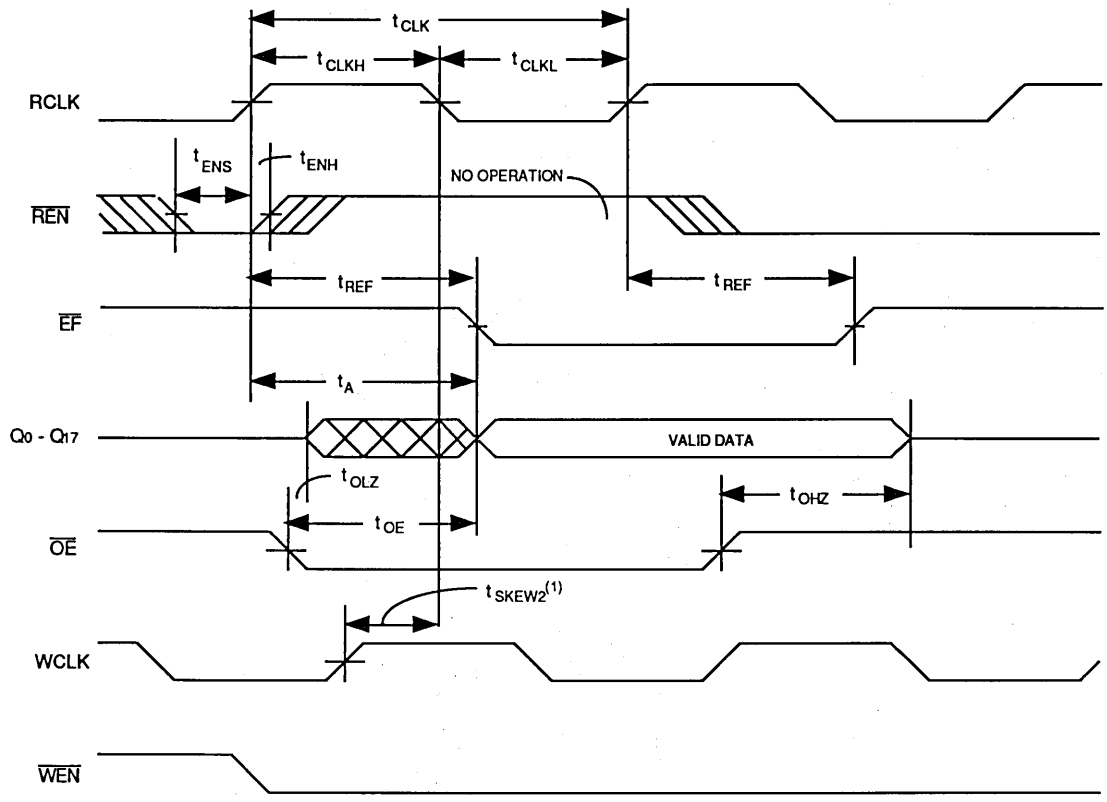


Figure 7. Read Cycle Timing

6

NOTE:
1. t_{SKEW2} is the minimum time between a rising WCLK edge and a falling RCLK edge for $\overline{EF}$ to change during the current clock cycle. If the time between the rising edge of WCLK and the falling edge of RCLK is less than t_{SKEW2}, then $\overline{EF}$ may not change state until the next RCLK edge.

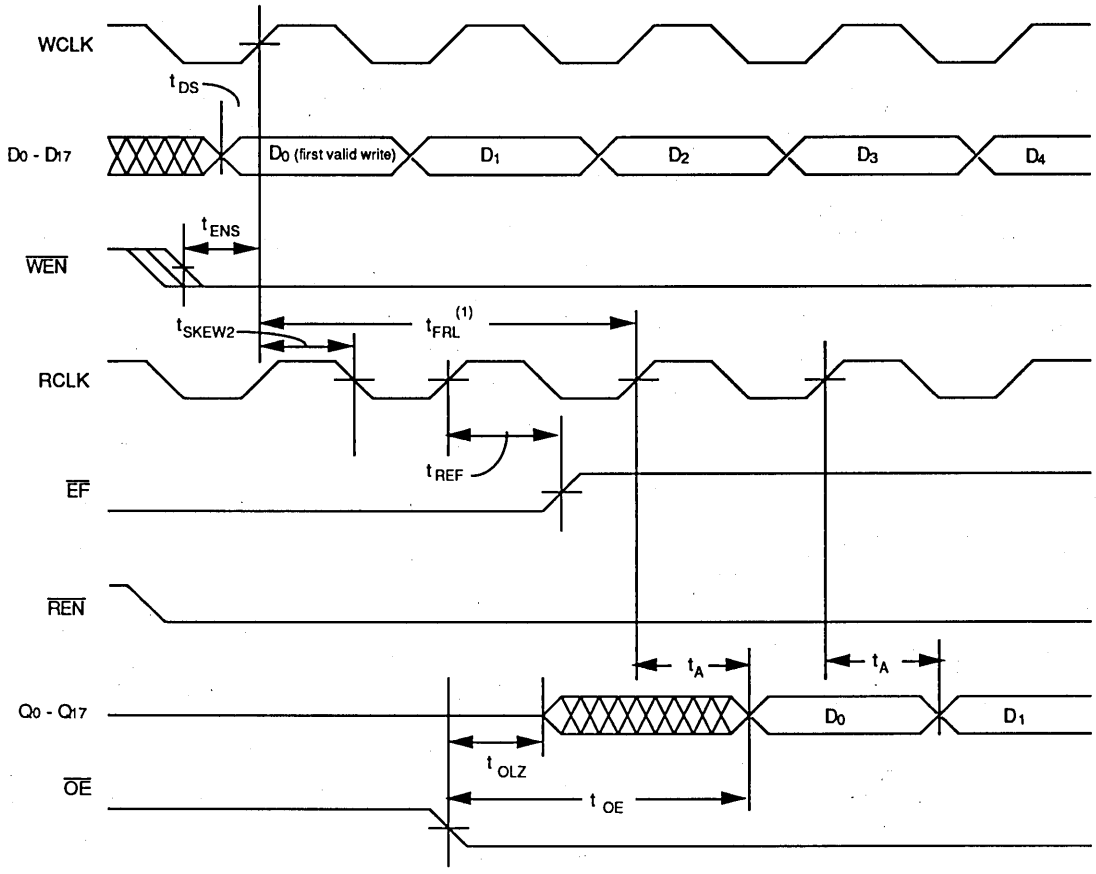


Figure 8. First Data Word Latency after Reset with Simultaneous Read and Write

NOTE:
1. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = 1.5 * t_{CLK} + t_{SKEW2}. t_{SKEW2} < minimum specification, t_{FRL} (maximum) = 2.5 * t_{CLK} + t_{SKEW2}. The Latency Timing apply only at the Empty Boundary ($\overline{EF}$ = LOW).

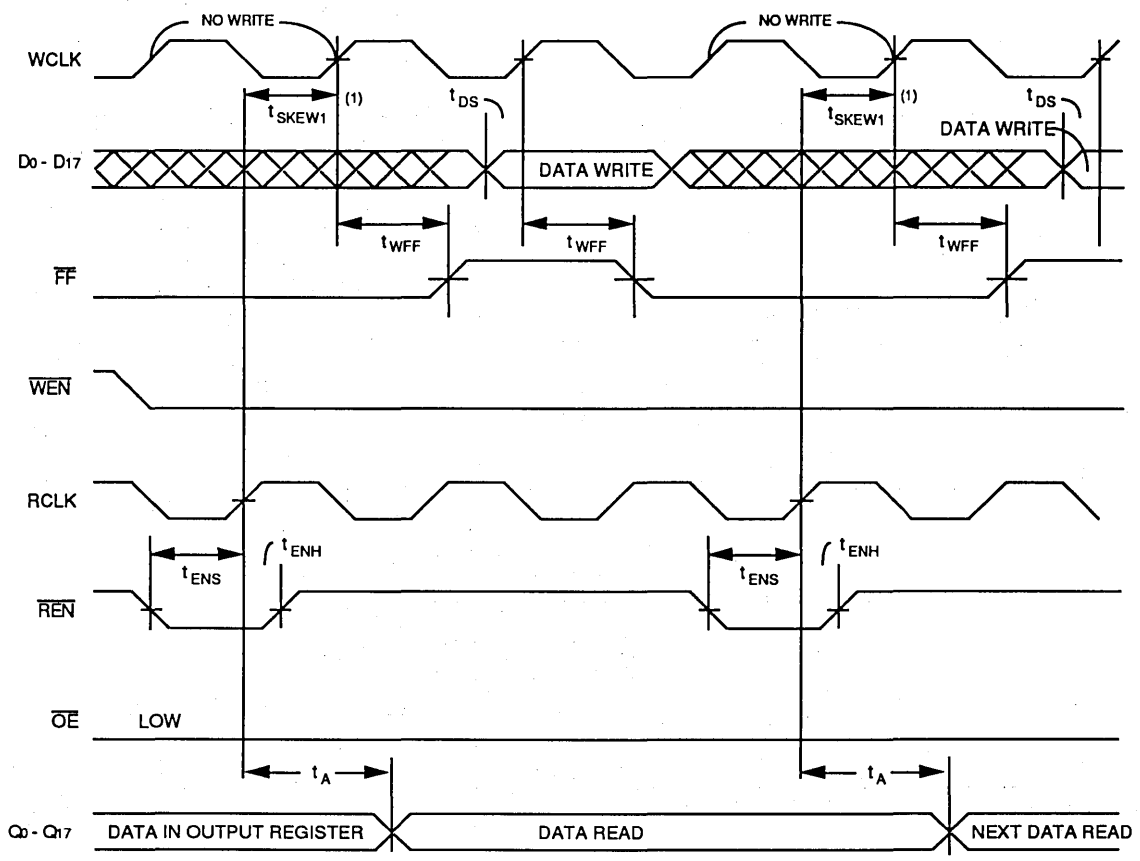


Figure 9. Full Flag Timing

NOTE:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{FF}$ to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK edge.

6

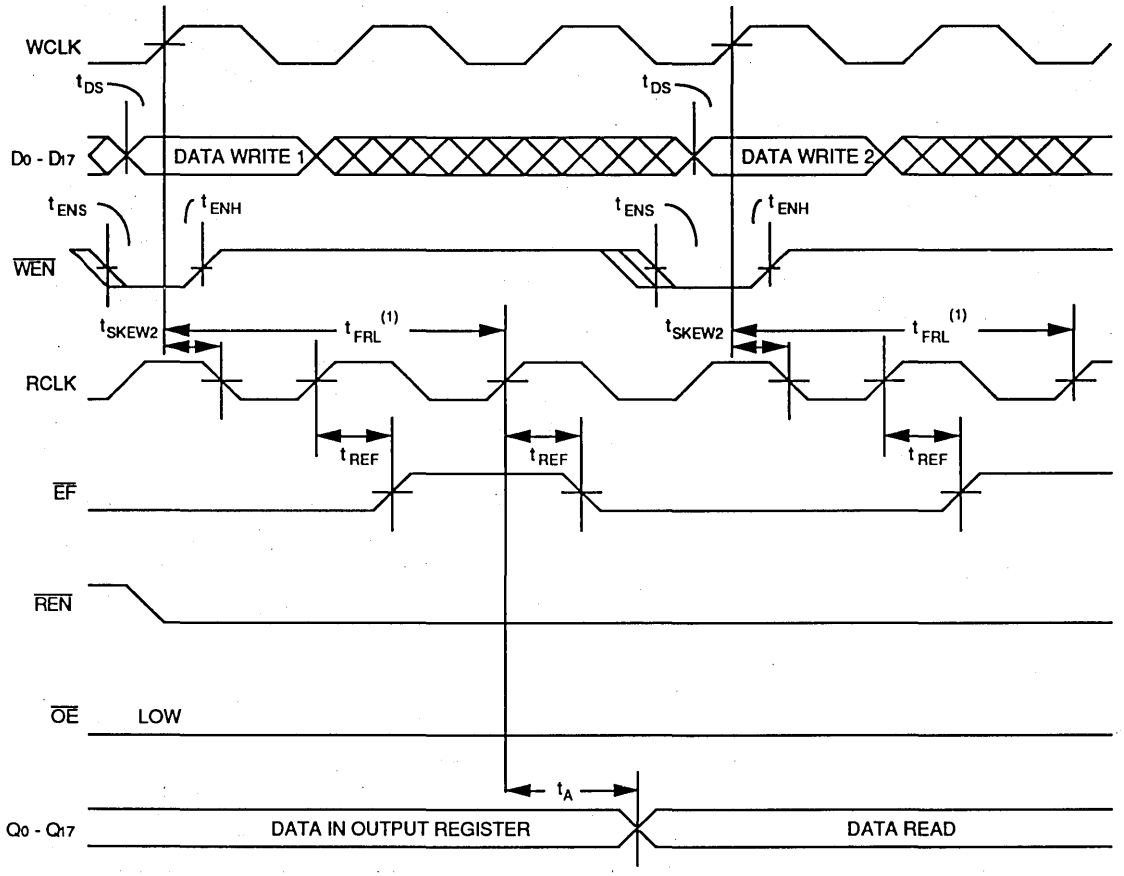


Figure 10. Empty Flag Timing

NOTE:
1. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = 1.5 * t_{CLK} + t_{SKEW2}. t_{SKEW2} < minimum specification, t_{FRL} (maximum) = 2.5 * t_{CLK} + t_{SKEW2}. The Latency Timing apply only at the Empty Boundary ($\overline{EF}$ = LOW).

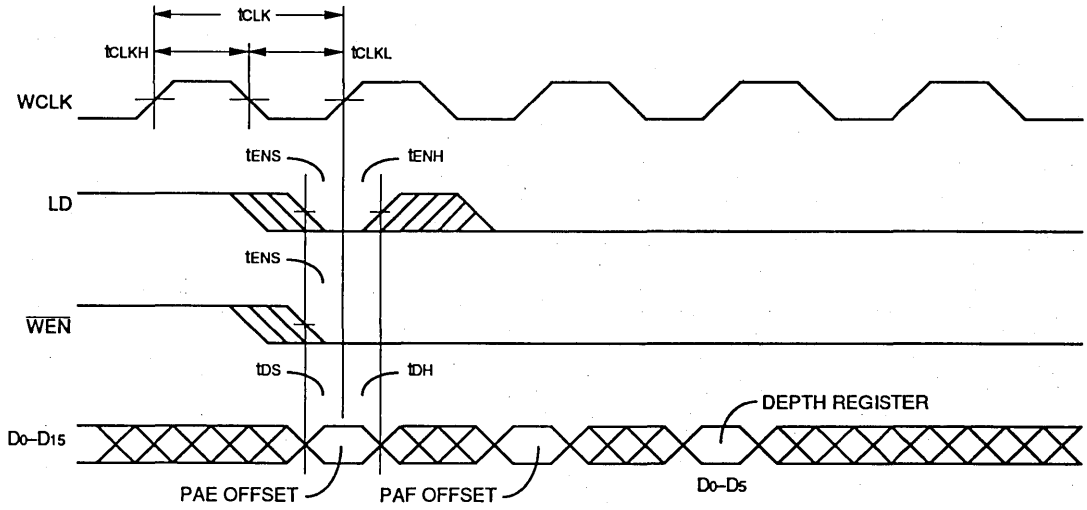


Figure 11. Write Programmable Registers

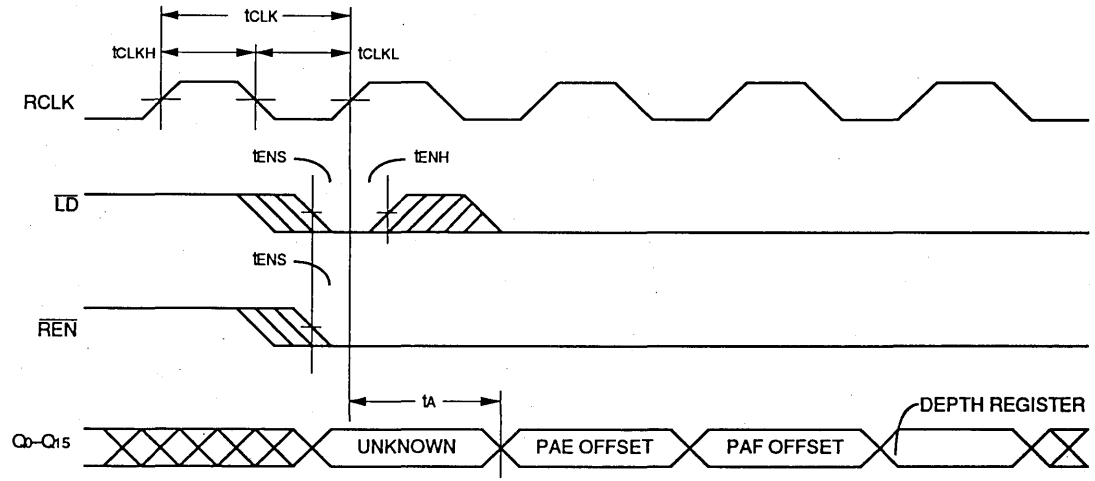


Figure 12. Read Programmable Registers

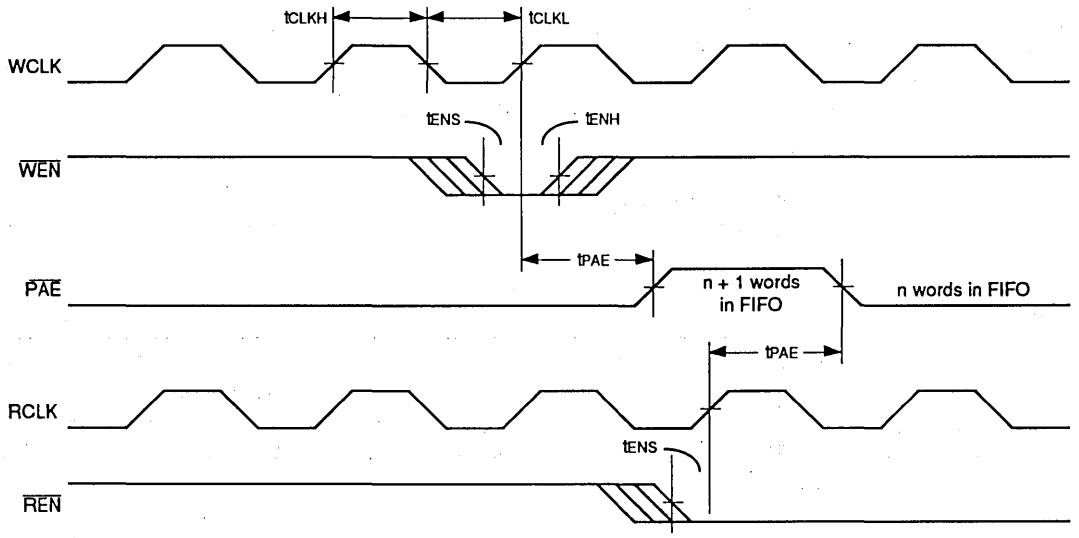


Figure 13. Programmable Almost Empty Flag Timing

NOTE:
1. PAE is offset = n. Number of data words written into FIFO already = n.

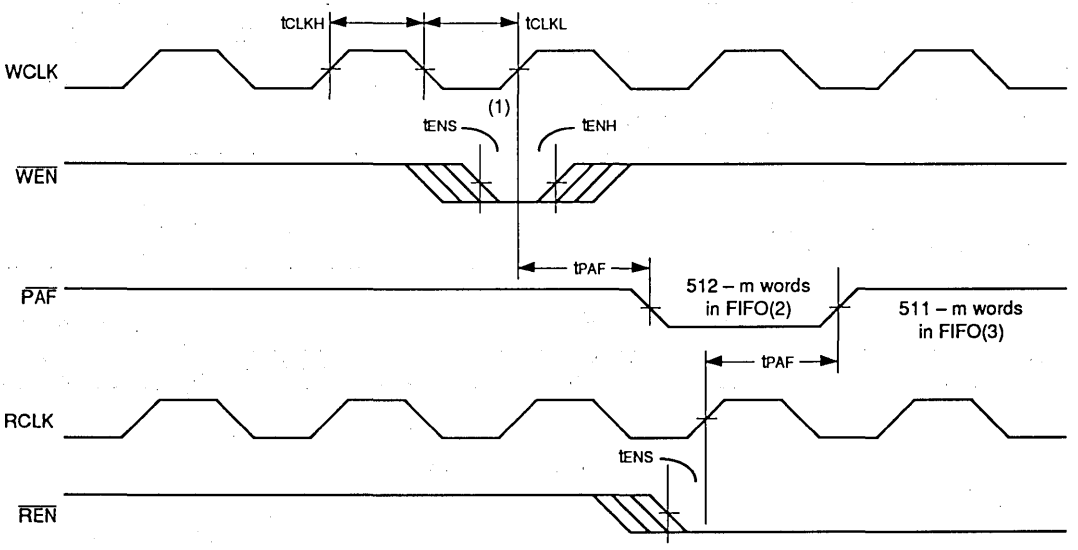


Figure 14. Programmable Almost-Full Flag Timing

NOTES:
1. PAF offset = m. Number of data words written into FIFO already = 511 – m for the IDT72215A and 1023 – m for the IDT72225A.
2. 512 – m words in FIFO for IDT72215A. 1024 – m word in FIFO for IDT72225A.
3. 511 – m words in FIFO for IDT72215A. 1023 – m word in FIFO for IDT72225A.

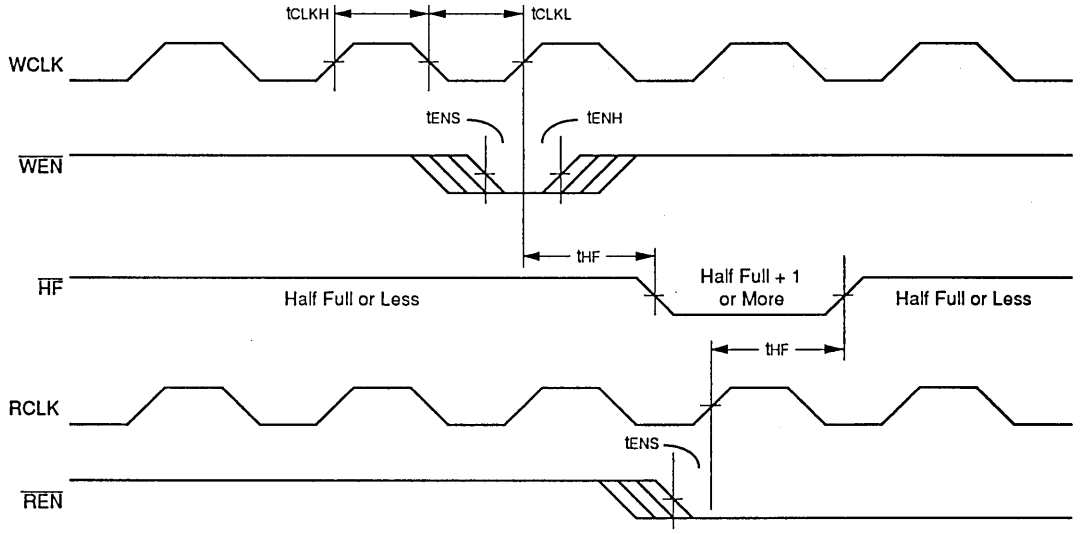


Figure 15. Half-Full Flag Timing

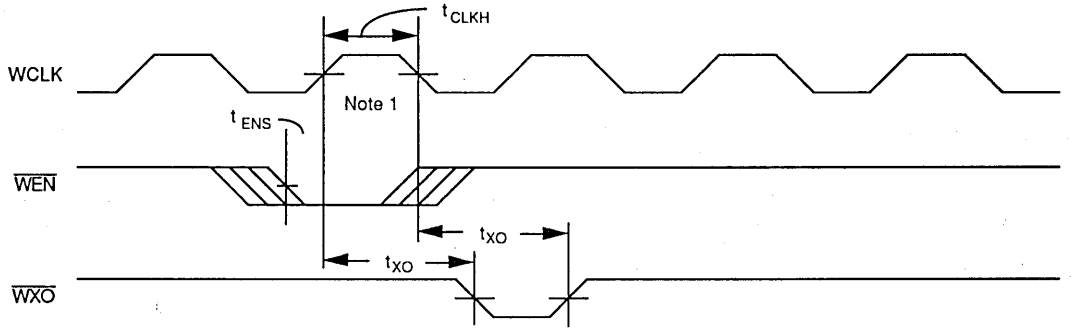


Figure 16. Write Expansion Out Timing

NOTE:
1. Write to Last Physical Location.

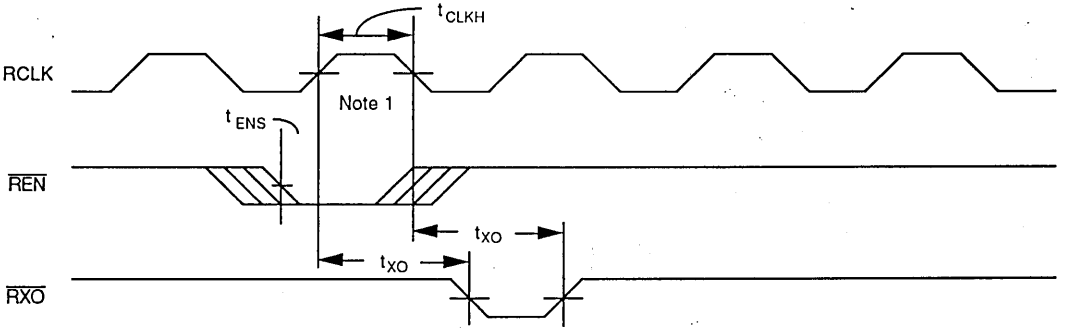


Figure 17. Read Expansion Out Timing

NOTE:
1. Read from Last Physical Location.

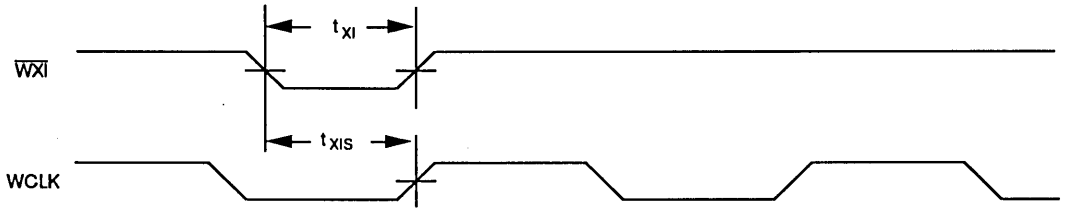


Figure 18. Write Expansion In Timing

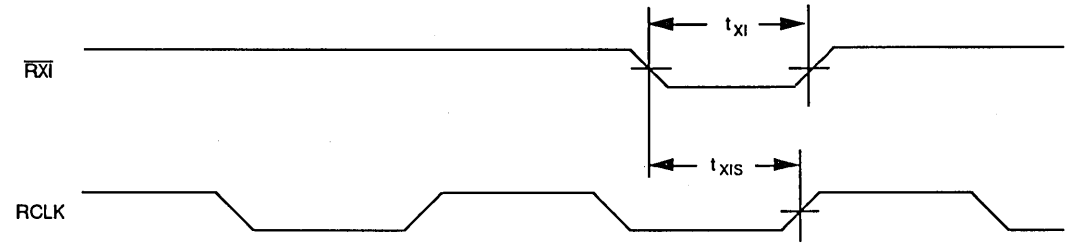


Figure 19. Read Expansion In Timing

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION

A single IDT72215A/72225A may be used when the application requirements are for 512/1024 words or less. The IDT72215A/72225A are in a single Device Configuration when the Write Exansion In ($\overline{WXI}$), Read Expansion In ($\overline{RXI}$), and First Load ($\overline{FL}$) control inputs are grounded . (See Figure 20.)

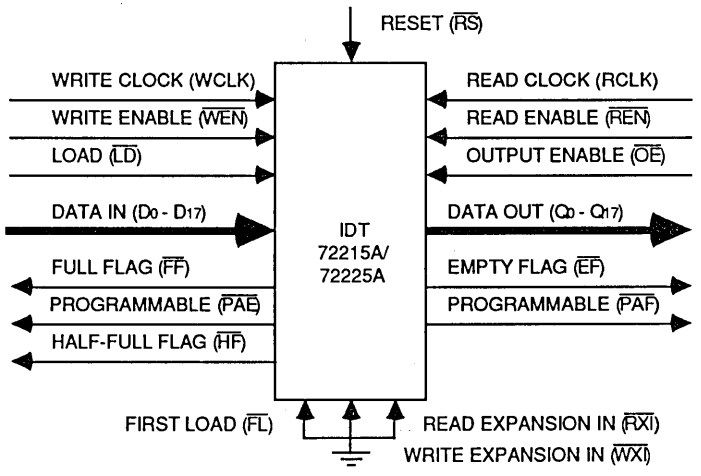
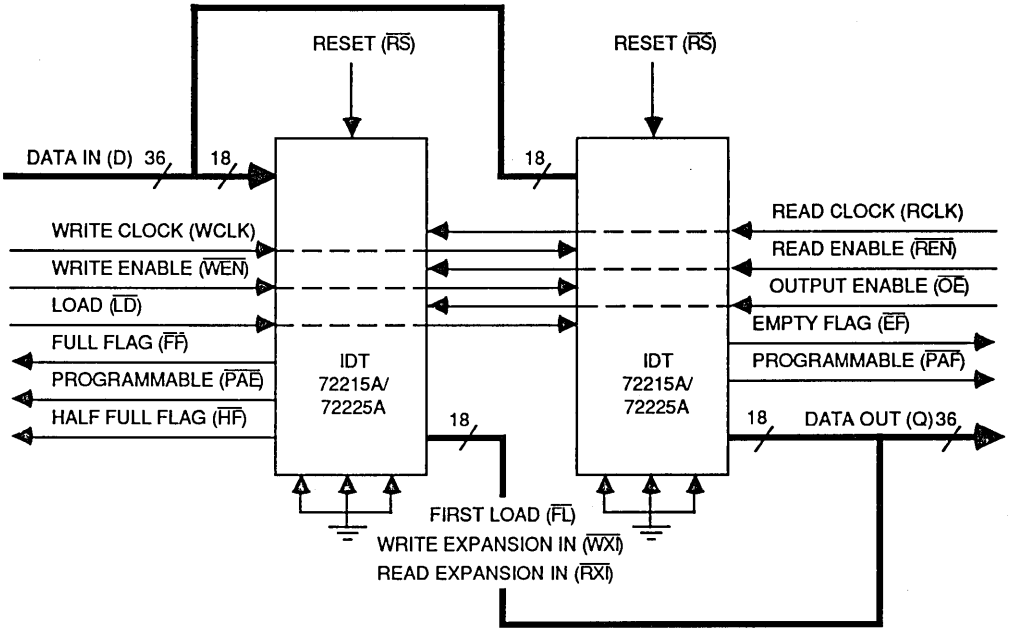


Figure 20. Block Diagram of Single 512 x 18/1024 x 18 Synchronous FIFO

WIDTH EXPANSION CONFIGURATION

Word width may be increased simply by connecting the corresponding control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{PAE}$, $\overline{HF}$, $\overline{PAF}$, and $\overline{FF}$) can be detected from any one device. Figure 21 demonstrates a 36-word width by using two IDT72215A.72225As. Any word width can be attained by adding additional IDT72215A/72225As.



NOTE:
1. Flag detection is accomplshed by monitoring the flag signals on either (any) device used in width expansion configuration. Do not connect any output control signals together.

Figure 21. Block Diagram of 512 x 36/1024 x 36 Synchronous FIFO Memory Used in a a Width Expansion Configuration

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DEPTH EXPANSION CONFIGURATION (WITH PROGRAMMABLE FLAGS)

The IDT72215A/72225A can easily be adapted to applications when the requirements are for greater than 512/1024 words. Figure 22 demonstrates Depth Expansion using three IDT72215A/72225As. Any depth up to 32768 can be attained by adding IDT72225As. The IDT72215A/72225A operates in the Depth Expansion configuration with programmable flags when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Write Expansion Out ($\overline{WXO}$) pin of each device must be tied to the Write Expansion In ($\overline{WXI}$) pin of the next device. See Figure 20.
4. The Read Expansion Out ($\overline{RXO}$) pin of each device must be tied to the Read Expansion In ($\overline{RXI}$) pin of the next device. See Figure 20.
5. To permit programmable flags, the first component controls the flags, and the flags are ignored on all other components. The total depth of the configuration is programmed in the master device by loading the total number of FIFOs into the depth register.
6. All Load ($\overline{LD}$) pins are tied together.
7. The Half-Full Flag ($\overline{HF}$) is not available in the Depth Expansion Configuration.

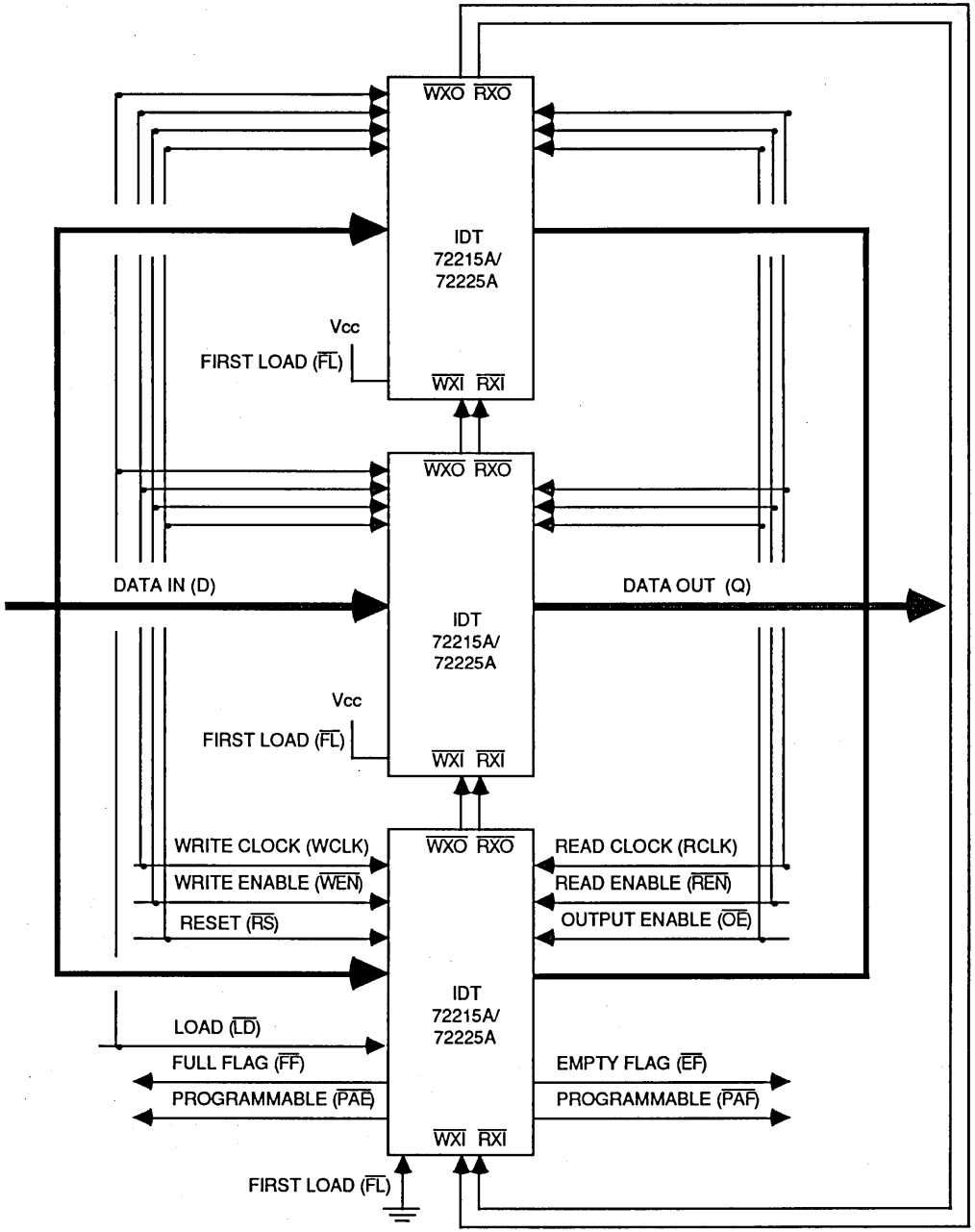
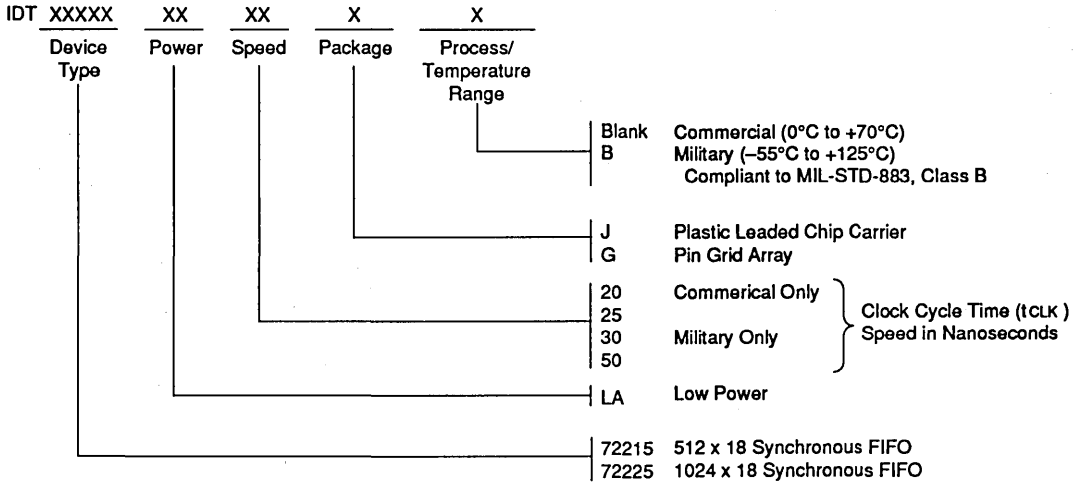


Figure 22. Block Diagram of 1536 x 18/3072 x 18 Synchronous FIFO Memory With Programmable Flags used in Depth Expansion Configuration

ORDERING INFORMATION



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6

Integrated Device Technology, Inc.

CMOS PARALLEL SyncFIFO™ (CLOCKED FIFO) 1024 x 8-BIT, 2048 x 8-BIT & 4096 x 8-BIT

ADVANCE INFORMATION
IDT72220
IDT72230
IDT72240

FEATURES:

- 1024, 2048, and 4096 x 8-bit memory array structures
- 15ns read / write cycle time
- Read and write clocks can be asynchronous or coincident
- Dual-ported zero fall-through time architecture
- Empty and Full flags signal FIFO status
- Almost-empty and almost-full flags set to Empty+7 and Full-7 respectively
- Output enable puts output data bus in high impedance state
- Produced with advanced submicron CEMOS™ technology
- Available in 28-pin 300 mil plastic DIP and 300 mil ceramic DIP
- For surface mount product please see the IDT72221/72231/72241 data sheet
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

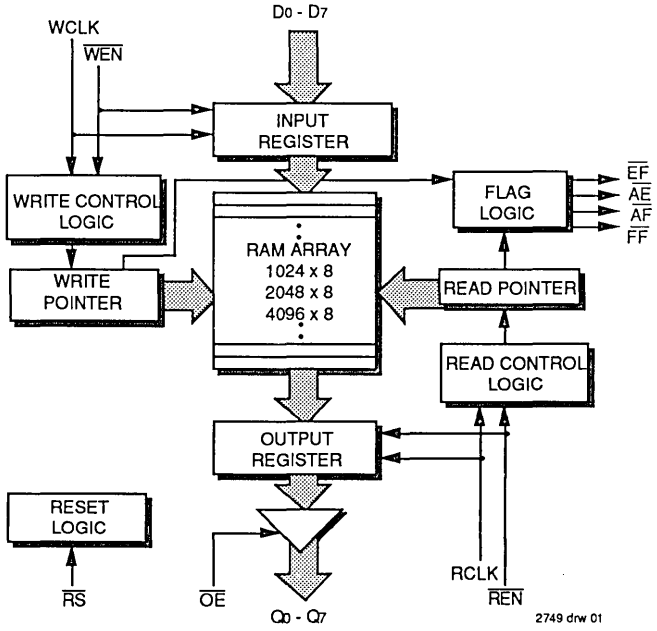
The IDT72220/72230/72240 SyncFIFO™ are very high speed, low-power first-in, first-out (FIFO) memories with clocked read and write controls. The IDT72220/72230/72240 have a 1024, 2048, and 4096 x 8-bit memory array, respectively. These FIFOs are applicable for a wide variety of data buffering needs, such as graphics, local area networks (LANs), and interprocessor communication.

These FIFOs have 8-bit input and output ports. The input port is controlled by a free-running clock (WCLK), and a write enable pin ($\overline{WEN}$). Data is read into the Synchronous FIFO on every clock when $\overline{WEN}$ is asserted. The output port is controlled by another clock pin (RCLK) and a read enable pin ($\overline{REN}$). The read clock can be tied to the write clock for single clock operation or the two clocks can run asynchronous of one another for dual clock operation. An output enable pin ($\overline{OE}$) is provided on the read port for three-state control of the output.

These Synchronous FIFOs have two end-point flags, Empty ($\overline{EF}$) and Full ($\overline{FF}$), and two partial flags, Almost-Empty ($\overline{AE}$) and Almost-Full ($\overline{AF}$), for improved system control. The partial flags are set to Empty+7 and Full-7 for $\overline{AE}$ and $\overline{AF}$, respectively.

The IDT72220/72230/72240 are fabricated using IDT's high speed submicron CEMOS™ technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



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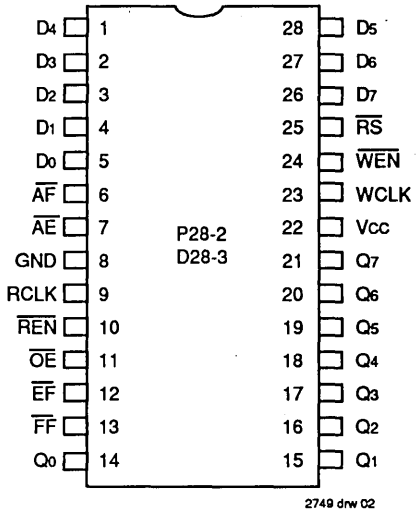
PIN CONFIGURATION



DIP
TOP VIEW

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D0 - D7	Data Inputs	I	Data inputs for a 8-bit bus.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal read and write pointers are set to the first location of the RAM array, $\overline{FF}$ and $\overline{AF}$ go high, and $\overline{AE}$ and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up.
WCLK	Write Clock	I	Data is written into the FIFO on a LOW-to-HIGH transition of WCLK when $\overline{WEN}$ is asserted.
$\overline{WEN}$	Write Enable	I	When $\overline{WEN}$ is LOW, data is written into the FIFO on every LOW-to-HIGH transition of WCLK. Data will not be written into the FIFO if the $\overline{FF}$ is LOW.
Q0 - Q7	Data Outputs	O	Data outputs for a 8-bit bus.
RCLK	Read Clock	I	Data is read from the FIFO on a LOW-to-HIGH transition of RCLK when $\overline{REN}$ is asserted.
$\overline{REN}$	Read Enable	I	When $\overline{REN}$ is LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the data output bus is active. If $\overline{OE}$ is HIGH, the output data bus will be in a high impedance state.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty and further data reads from the output are inhibited. When $\overline{EF}$ is HIGH, the FIFO is not empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{AE}$	Almost-Empty Flag	O	When $\overline{AE}$ is LOW, the FIFO is almost empty based on the offset Empty+7. $\overline{AE}$ is synchronized to RCLK.
$\overline{AF}$	Almost-Full Flag	O	When $\overline{AF}$ is LOW, the FIFO is almost full based on the offset Full-7. $\overline{AF}$ is synchronized to WCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full and further data writes into the input are inhibited. When $\overline{FF}$ is HIGH, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK.
Vcc	Power		One +5 volt power supply pin.
GND	Ground		One 0 volt ground pin.

2749 tbl 01

6

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +135	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2749 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage Commercial	2.0	—	—	V
VIH	Input High Voltage Military	2.2	—	—	V
VIL	Input Low Voltage Com'l. & Mil.	—	—	0.8	V

2749 tbl 04

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
CIN(2)	Input Capacitance	VIN = 0V	10	pF
COUT(1,2)	Output Capacitance	VOUT = 0V	10	pF

NOTE: 2749 tbl 03

1. With output deselected. ($\overline{OE}$ = high)
2. Characterized values, not currently tested.

DC ELECTRICAL CHARACTERISTICS

(Commercial: VCC = 5V ± 10%, TA = 0°C to +70°C; Military: VCC = 5V ± 10%, TA = -55°C to +125°C)

Symbol	Parameter	IDT72220, IDT72230 IDT72240 Commercial tCLK = 15, 20, 25, 50 ns			IDT72220, IDT72230, IDT72240 Military tCLK = 20, 25, 50 ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
ILI(1)	Input Leakage Current (any input)	–1	—	1	–10	—	10	µA
ILO(2)	Output Leakage Current	–10	—	10	–10	—	10	µA
VOH	Output Logic "1" Voltage, IOH = –2 mA	2.4	—	—	2.4	—	—	V
VOL	Output Logic "0" Voltage, IOL = 8 mA	—	—	0.4	—	—	0.4	V
ICC1(3)	Active Power Supply Current	—	—	140	—	—	160	mA

NOTES: 2749 tbl 05

1. Measurements with 0.4 ≤ VIN ≤ VOUT.
2. $\overline{OE}$ ≥ VIH, 0.4 ≤ VOUT ≤ VCC.
3. Measurements are made with outputs open.
   Tested at fCLK = 20 MHz.
   Typical ICC1 = 65 + (fCLK * 1.1 / MHz) + (fCLK * CL * 0.03 / MHz-pF) mA
   fCLK = 1 / tCLK
   CL = external capacitive load (30 pF typical)

AC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 5V ± 10%, TA = 0°C to +70°C; Military: Vcc = 5V ± 10%, TA = -55°C to +125°C)

		Com'l. IDT72220L15 IDT72230L15 IDT72240L15		Commercial and Military IDT72220L20 IDT72230L20 IDT72240L20		IDT72220L25 IDT72230L25 IDT72240L25		IDT72220L50 IDT72230L50 IDT72240L50		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
fS	Clock Cycle Frequency	—	66.7	—	50	—	40	—	20	MHz
tA	Data Access Time	2	10	2	12	3	15	3	25	ns
tCLK	Clock Cycle Time	15	—	20	—	25	—	50	—	ns
tCLKH	Clock High Time	6	—	8	—	10	—	20	—	ns
tCLKL	Clock Low Time	6	—	8	—	10	—	20	—	ns
tDS	Data Set-up Time	4	—	5	—	6	—	10	—	ns
tDH	Data Hold Time	1	—	1	—	1	—	2	—	ns
tENS	Enable Set-up Time	4	—	5	—	6	—	10	—	ns
tENH	Enable Hold Time	1	—	1	—	1	—	2	—	ns
tRS	Reset Pulse Width[1]	15	—	20	—	25	—	50	—	ns
tRSS	Reset Set-up Time	15	—	20	—	25	—	50	—	ns
tRSF	Reset to Flag and Output Time	—	15	—	20	—	25	—	50	ns
tOLZ	Output Enable to Output in Low Z[2]	0	—	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	3	8	3	10	3	13	3	28	ns
tOHZ	Output Enable to Output in High Z[2]	3	8	3	10	3	13	3	28	ns
tWFF	Write Clock to Full Flag	—	10	—	12	—	15	—	30	ns
tREF	Read Clock to Empty Flag	—	10	—	12	—	15	—	30	ns
tAF	Write Clock to Almost-Full Flag	—	10	—	12	—	15	—	30	ns
tAE	Read Clock to Almost-Empty Flag	—	10	—	12	—	15	—	30	ns
tSKEW1	Skew time between Read Clock & Write Clock for Empty Flag & Full Flag	6	—	8	—	10	—	15	—	ns
tSKEW2	Skew time between Read Clock & Write Clock for Almost-Empty Flag & Almost-Full Flag	15	—	18	—	20	—	30	—	ns

NOTES:
1. Pulse widths less than minimum are not allowed.
2. Values guaranteed by design, not currently tested.

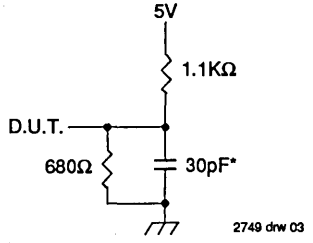
2749 tbl 06

6

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2749 tbl 07



or equivalent circuit

Figure 1. Output Load

*Includes jig and scope capabilities.

Integrated Device Technology, Inc.

CMOS PARALLEL SyncFIFO™ (CLOCKED FIFO) 1024 x 9-BIT, 2048 x 9-BIT & 4096 x 9-BIT

ADVANCE INFORMATION
IDT72221
IDT72231
IDT72241

FEATURES:

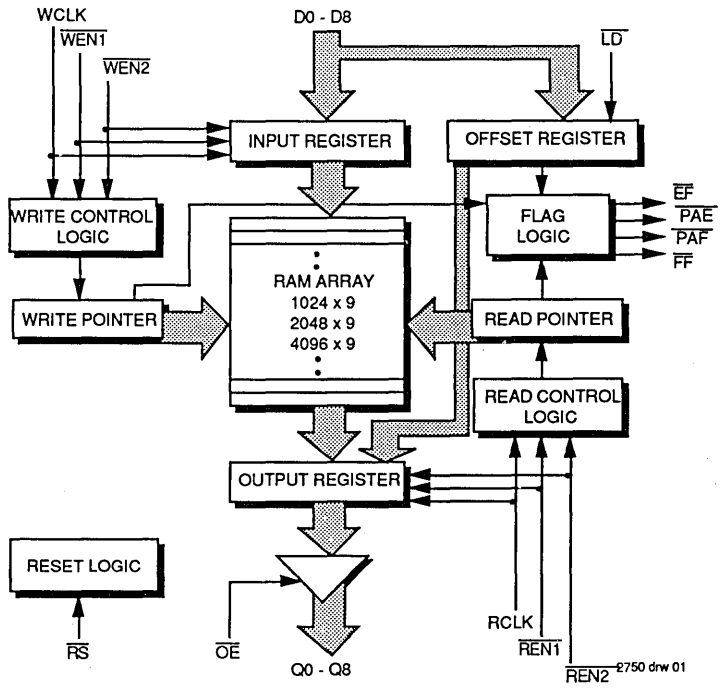
- 1024, 2048, and 4096 x 9-bit memory array structures
- 15ns read / write cycle time
- Read and write clocks can be asynchronous or coincident
- Dual-ported zero fall-through time architecture
- Empty and Full flags signal FIFO status
- Programmable almost-empty and almost-full flags can be set to any depth
- Programmable almost-empty and almost-full flags default to Empty+7 and Full-7 respectively
- Output enable puts output data bus in high impedance state
- Produced with advanced submicron CEMOS™ technology
- Available in 32-pin plastic leaded chip carrier (PLCC) and ceramic leadless chip carrier (LCC)
- For Through-Hole product please see the IDT72220/ 72230/72240 data sheet
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72221/72231/72241 SyncFIFO™ are very high speed, low-power first-in, first-out (FIFO) memories with clocked read and write controls. The IDT72221/72231/ 72241 have a 1024, 2048, and 4096 x 9-bit memory array, respectively. These FIFOs are applicable for a wide variety of data buffering needs, such as graphics, local area networks (LANs), and interprocessor communication.

These FIFOs have 9-bit input and output ports. The input port is controlled by a free-running clock (WCLK), and write enable pins ($\overline{WEN1}$, WEN2). Data is read into the Synchronous FIFO on every clock when the write enable pins are asserted. The output port is controlled by another clock pin (RCLK) and two read enable pins ($\overline{REN1}$, $\overline{REN2}$). The two enable pins on each port are provided to allow for depth expansion. The read clock can be tied to the write clock for single clock operation or the two clocks can run asynchronous of one another for dual clock operation. An output enable pin ($\overline{OE}$) is provided on the read port for three-state control of the output.

FUNCTIONAL BLOCK DIAGRAM



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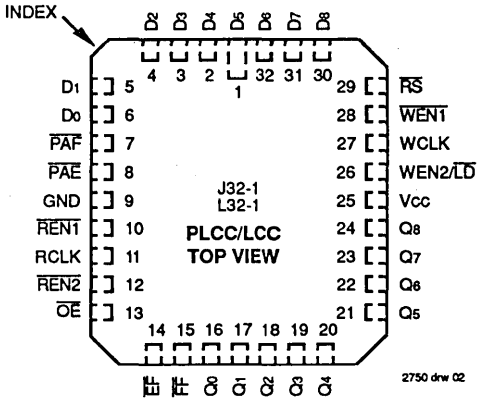
DESCRIPTION (Continued)

The Synchronous FIFOs have two fixed flags, Empty ($\overline{EF}$) and Full ($\overline{FF}$). Two programmable flags, Almost-Empty ($\overline{PAE}$) and Almost-Full ($\overline{PAF}$), are provided for improved system control. The programmable flags default to Empty+7 and Full-7 for $\overline{PAE}$ and $\overline{PAF}$ respectively. The programmable flag offset loading is controlled by a simple state machine, and is initiated by asserting the load pin ($\overline{LD}$).

The IDT72221/72231/72241 are fabricated using IDT's high speed submicron CEMOS™ technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

PIN CONFIGURATION



PIN DESCRIPTION

Symbol	Name	I/O	Description
D0 - D8	Data Inputs	I	Data inputs for a 9-bit bus.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal read and write pointers are set to the first location of the RAM array, $\overline{FF}$ and $\overline{PAF}$ go high, and $\overline{PAE}$ and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up.
WCLK	Write Clock	I	Data is written into the FIFO on a LOW-to-HIGH transition of WCLK when the Write Enable(s) are asserted.
$\overline{WEN1}$	Write Enable 1	I	If the FIFO is configured to have programmable flags, $\overline{WEN1}$ is the only write enable pin. When $\overline{WEN1}$ is LOW, data is written into the FIFO on every LOW-to-HIGH transition of WCLK. If the FIFO is configured to have two write enables, $\overline{WEN1}$ must be LOW & WEN2 must be HIGH to write data into the FIFO. Data will not be written into the FIFO if the $\overline{FF}$ is LOW.
WEN2/$\overline{LD}$	Write Enable 2 / Load	I	The FIFO is configured at reset to have two write enables or programmable flags. If WEN2/$\overline{LD}$ is HIGH at reset, this pin operates as a second write enable. If WEN2/$\overline{LD}$ is LOW at reset, this pin operates as a control to load and read the programmable flag offsets. If the FIFO is configured to have two write enables, $\overline{WEN1}$ must be LOW & WEN2 must be HIGH to write data into the FIFO. Data will not be written into the FIFO if the $\overline{FF}$ is LOW. If the FIFO is configured to have programmable flags, WEN2/$\overline{LD}$ is held LOW to write or read the programmable flag offsets.
Q0 - Q8	Data Outputs	O	Data outputs for a 9-bit bus.
RCLK	Read Clock	I	Data is read from the FIFO on a LOW-to-HIGH transition of RCLK when $\overline{REN1}$ & $\overline{REN2}$ are asserted.
$\overline{REN1}$	Read Enable 1	I	When $\overline{REN1}$ and $\overline{REN2}$ are LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{REN2}$	Read Enable 2	I	When $\overline{REN1}$ and $\overline{REN2}$ are LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the data output bus is active. If $\overline{OE}$ is HIGH, the output data bus will be in a high impedance state.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty and further data reads from the output are inhibited. When $\overline{EF}$ is HIGH, the FIFO is not empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{PAE}$	Programmable Almost-Empty Flag	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the offset programmed into the FIFO. The default offset at reset is Empty+7. $\overline{PAE}$ is synchronized to RCLK.
$\overline{PAF}$	Programmable Almost-Full Flag	O	When $\overline{PAF}$ is LOW, the FIFO is almost full based on the offset programmed into the FIFO. The default offset at reset is Full-7. $\overline{PAF}$ is synchronized to WCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full and further data writes into the input are inhibited. When $\overline{FF}$ is HIGH, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK.
Vcc	Power		One +5 volt power supply pin.
GND	Ground		One 0 volt ground pin.

6

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +135	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2750 tbl 02
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage Commercial	2.0	—	—	V
VIH	Input High Voltage Military	2.2	—	—	V
VIL	Input Low Voltage Com'l. & Mil.	—	—	0.8	V

2750 tbl 04

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN(2)	Input Capacitance	VIN = 0V	10	pF
COUT(1,2)	Output Capacitance	VOUT = 0V	10	pF

NOTE: 2750 tbl 03
1. With output deselected. ($\overline{OE}$ = high)
2. Characterized values, not currently tested.

DC ELECTRICAL CHARACTERISTICS

(Commercial: VCC = 5V ± 10%, TA = 0°C to +70°C; Military: VCC = 5V ± 10%, TA = -55°C to +125°C)

Symbol	Parameter	IDT72221, IDT72231, IDT72241 Commercial tCLK = 15, 20, 25, 50 ns			IDT72221, IDT72231, IDT72241 Military tCLK = 20, 25, 50 ns			Unit
		Min	Typ.	Max.	Min	Typ.	Max.	
ILI(1)	Input Leakage Current (any input)	–1	—	1	–10	—	10	µA
ILO(2)	Output Leakage Current	–10	—	10	–10	—	10	µA
VOH	Output Logic "1" Voltage, IOH = –2 mA	2.4	—	—	2.4	—	—	V
VOL	Output Logic "0" Voltage, IOL = 8 mA	—	—	0.4	—	—	0.4	V
ICC1(3)	Active Power Supply Current	—	—	140	—	—	160	mA

NOTES: 2750 tbl 05
1. Measurements with 0.4 ≤ VIN ≤ VOUT.
2. $\overline{OE}$ ≥ VIH, 0.4 ≤ VOUT ≤ VCC.
3. Measurements are made with outputs open.
   Tested at fCLK = 20 MHz.
   Typical ICC1 = 65 + (fCLK * 1.1 / MHz) + (fCLK * CL * 0.03 / MHz-pF) mA
   fCLK = 1 / tCLK
   CL = external capacitive load (30 pF typical)

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	Com'l. IDT72221L15 IDT72231L15 IDT72241L15		Commercial & Military IDT72221L20 IDT72231L20 IDT72241L20		IDT72221L25 IDT72231L25 IDT72241L25		IDT72221L50 IDT72231L50 IDT72241L50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
fS	Clock Cycle Frequency	—	66.7	—	50	—	40	—	20	MHz
tA	Data Access Time	2	10	2	12	3	15	3	25	ns
tCLK	Clock Cycle Time	15	—	20	—	25	—	50	—	ns
tCLKH	Clock High Time	6	—	8	—	10	—	20	—	ns
tCLKL	Clock Low Time	6	—	8	—	10	—	20	—	ns
tDS	Data Set-up Time	4	—	5	—	6	—	10	—	ns
tDH	Data Hold Time	1	—	1	—	1	—	2	—	ns
tENS	Enable Set-up Time	4	—	5	—	6	—	10	—	ns
tENH	Enable Hold Time	1	—	1	—	1	—	2	—	ns
tRS	Reset Pulse Width[1]	15	—	20	—	25	—	50	—	ns
tRSS	Reset Set-up Time	15	—	20	—	25	—	50	—	ns
tRSF	Reset to Flag and Output Time	—	15	—	20	—	25	—	50	ns
tOLZ	Output Enable to Output in Low Z[2]	0	—	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	3	8	3	10	3	13	3	28	ns
tOHZ	Output Enable to Output in High Z[2]	3	8	3	10	3	13	3	28	ns
tWFF	Write Clock to Full Flag	—	10	—	12	—	15	—	30	ns
tREF	Read Clock to Empty Flag	—	10	—	12	—	15	—	30	ns
tPAF	Write Clock to Programmable Almost-Full Flag	—	10	—	12	—	15	—	30	ns
tPAE	Read Clock to Programmable Almost-Empty Flag	—	10	—	12	—	15	—	30	ns
tSKEW1	Skew time between Read Clock & Write Clock for Empty Flag & Full Flag	6	—	8	—	10	—	15	—	ns
tSKEW2	Skew time between Read Clock & Write Clock for Programmable Almost-Empty Flag & Programmable Almost-Full Flag	15	—	18	—	20	—	30	—	ns

NOTES:

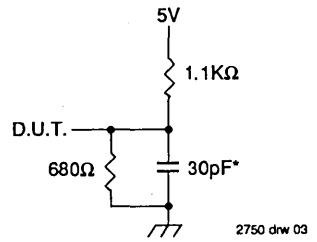
1. Pulse widths less than minimum are not allowed.
2. Values guaranteed by design, not currently tested.

2750 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2750 tbl 07



or equivalent circuit

Figure 1. Output Load

*Includes jig and scope capabilities.

Integrated Device Technology, Inc.

CMOS PARALLEL SyncFIFO™ (CLOCKED FIFO) 2048 x 18-BIT & 4096 x 18-BIT

ADVANCED INFORMATION
IDT72235
IDT72245

FEATURES:

- 2048 x 18-bit and 4096 x 18-bit memory array structures
- 20ns read / write cycle time
- Easily expandable in depth and width
- Read and write clocks can be asynchronous or coincident
- Dual-port zero fall-through time architecture
- Programmable almost-empty and almost-full flags
- Empty and Full flags signal FIFO status
- Half-Full flag capability in a single device configuration
- Output enable puts output data bus in high impedance state
- First device controls all flag logic in depth expansion
- Produced with advanced submicron CEMOS™ technology
- Available in a 68-lead pin grid array (PGA), and plastic leaded chip carrier (PLCC)
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72235 and IDT72245 are very high speed, low-power first-in, first-out (FIFO) memories with clocked read and write controls. The IDT72235 has a 2048 x 18-bit memory array, while the IDT72245 has a 4096 x 18-bit memory array. These FIFOs are applicable for a wide variety of data buffering needs, such as optical disk controllers, local area networks (LANs), and interprocessor communication.

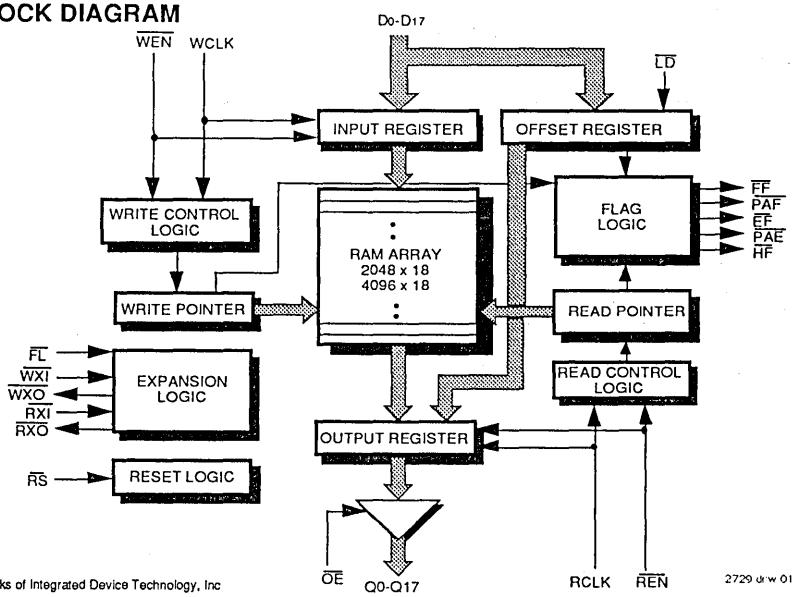
Both FIFOs have 18-bit input and output ports. The input port is controlled by a free-running clock (WCLK), and a data input enable pin ($\overline{WEN}$). Data is read into the synchronous FIFO on every clock when $\overline{WEN}$ is asserted. The output port is controlled by another clock pin (RCLK) and another enable pin ($\overline{REN}$). The read clock can be tied to the write clock for single clock operation or the two clocks can run asynchronous of one another for dual clock operation. An output enable pin ($\overline{OE}$) is provided on the read port for three-state control of the output.

The synchronous FIFOs have two fixed flags, Empty ($\overline{EF}$) and Full ($\overline{FF}$), and two programmable flags, Almost-Empty ($\overline{PAE}$) and Almost-Full ($\overline{PAF}$). The offset loading of the programmable flags is controlled by a simple state machine, and is initiated by asserting the load pin ($\overline{LD}$). A Half-Full flag ($\overline{HF}$) is available when the FIFO is used in a single device configuration.

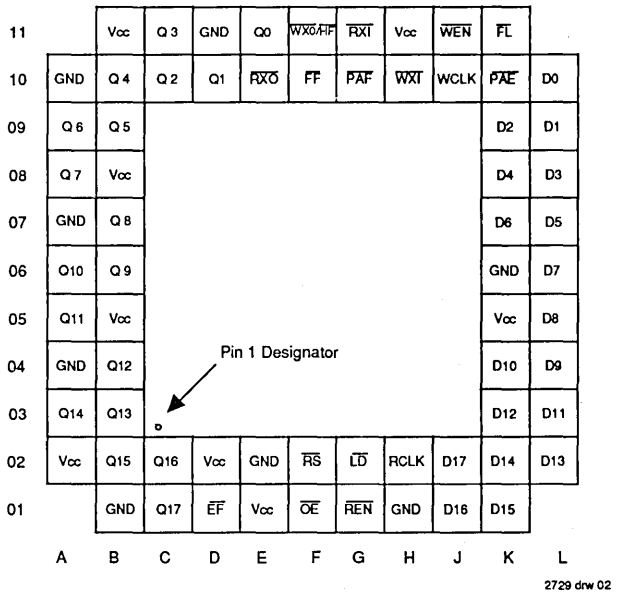
The IDT72235 and IDT72245 are depth expandable using a daisy-chain technique. The $\overline{XI}$ and $\overline{XO}$ pins are used to expand the FIFOs. To permit programmable flags in depth expansion, the first device, indicated by setting $\overline{FL}$ to low, controls the flags.

The IDT72235/72245 is fabricated using IDT's high speed submicron CEMOS™ technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

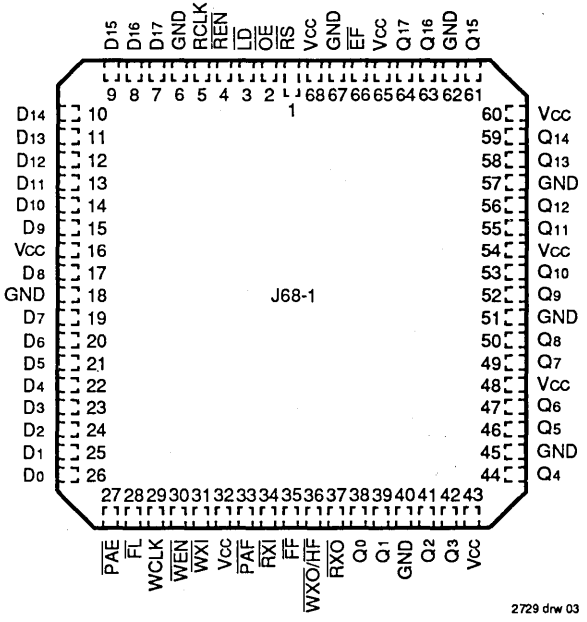
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



PGA
TOP VIEW



PLCC
TOP VIEW

PIN DESCRIPTION

Symbol	Name	I/O	Description
D_0–D_{17}	Data Inputs	I	Data inputs for a 18-bit bus.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal read and write pointers are set to the first location of the RAM array, $\overline{FF}$ and $\overline{PAF}$ go high, and $\overline{PAE}$ and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up.
WCLK	Write Clock	I	Data is written into the FIFO on a LOW-to-HIGH transition of WCLK when Write Enable $\overline{WEN}$ is asserted (LOW).
$\overline{WEN}$	Write Enable	I	When $\overline{WEN}$ is LOW, data is written into the FIFO on every LOW-to-HIGH transition of WCLK. When $\overline{WEN}$ is high, the FIFO holds the previous data. Data will not be written into the FIFO if the $\overline{FF}$ is LOW.
RCLK	Read Clock	I	Data is read from the FIFO on a LOW-to-HIGH transition of RCLK when Read Enable $\overline{REN}$ is asserted (LOW).
$\overline{REN}$	Read Enable	I	When $\overline{REN}$ is LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. When $\overline{REN}$ is high, the output register holds the previous data. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the data output bus is active. If $\overline{OE}$ is HIGH, the output data bus will be in a high impedance state.
$\overline{LD}$	Load	I	When $\overline{LD}$ is LOW, data on the inputs D_0–D_{15} is written to the offset and depth registers on the LOW-to-HIGH transition of the WCLK, when $\overline{WEN}$ is LOW. When $\overline{LD}$ is LOW, data on the outputs Q_0–Q_{15} is read from the offset and depth registers on the LOW-to-HIGH transition of the RCLK, when $\overline{REN}$ is LOW.
$\overline{FL}$	First Load	I	In the single device or width expansion configuration, $\overline{FL}$ is grounded. In the depth expansion configuration, $\overline{FL}$ is grounded on the first device (first load device) and set to high for all other devices in the daisy chain.
$\overline{WXI}$	Write Expansion Input	I	In the single device or width expansion configuration, $\overline{WXI}$ is grounded. In the depth expansion configuration, $\overline{WXI}$ is connected to $\overline{WXO}$ (Write Expansion Out) of the previous device.
$\overline{RXI}$	Read Expansion Input	I	In the single device or width expansion configuration, $\overline{RXI}$ is grounded. In the depth expansion configuration, $\overline{RXI}$ is connected to $\overline{RXO}$ (Read Expansion Out) of the previous device.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty and further data reads from the output are inhibited. When $\overline{EF}$ is HIGH, the FIFO is not empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{PAE}$	Programmable Almost-Empty Flag	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the offset programmed into the FIFO. The default offset at reset is 1/8 full.
$\overline{PAF}$	Programmable Almost-Full Flag	O	When $\overline{PAF}$ is LOW, the FIFO is almost full based on the offset programmed into the FIFO. The default offset at reset is 7/8 full.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full and further data writes into the input are inhibited. When $\overline{FF}$ is HIGH, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK.
$\overline{WXO/HF}$	Write Expansion Out/Half-Full Flag	O	In the single device or width expansion configuration, the device is more than half full when $\overline{HF}$ is LOW. In the depth expansion configuration, a pulse is sent from $\overline{WXO}$ to $\overline{WXI}$ of the next device when the last location in the FIFO is written.
$\overline{RXO}$	Read Expansion Out	O	In the depth expansion configuration, a pulse is sent from $\overline{RXO}$ to $\overline{RXI}$ of the next device when the last location in the FIFO is read.
Q_0–Q_{17}	Data Outputs	O	Data outputs for a 18-bit bus.
V_{CC}	Power		Eight +5 volt power supply pins.
GND	Ground		Eight 0 volt ground pins.

2729 tbl 01

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2729 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maimum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}[1]	Input Low Voltage Commercial & Military	—	—	0.8	V

NOTE: 2729 tbl 03

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

Symbol	Parameter	IDT72235 IDT72235 Commercial t_{CLK} = 20, 25, 50ns			IDT72245 IDT72245 Military t_{CLK} = 25, 30, 50ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI}[1]	Input Leakage Current (any input)	–1	—	1	–10	—	10	µA
I_{LO}[2]	Output Leakage Current	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = –2 mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8 mA	—	—	0.4	—	—	0.4	V
I_{CC1}[3]	Active Power Supply Current	—	—	250	—	—	300	mA
I_{CC2}[3]	Average Standby Current (All Input = VCC – 0.2V, except RCLK and WCLK which are free-running)	—	—	60	—	—	75	mA

NOTES: 2729 tbl 04

1. Measurements with 0.4 ≤ V_{IN} ≤ V_{OUT}.
2. $\overline{OE}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Tested at f = 20 MHz.

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AC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 5V ± 10%, TA = 0°C to +70°C; Military: Vcc = 5V ± 10%, TA = –55°C to +125°C)

Symbol	Parameter	IDT72235L20 IDT72245L20 Com'l.		IDT72235L25 IDT72245L25 Com'l. & Mil.		IDT72235L30 IDT72245L30 Mil.		IDT72235L50 IDT72245L50 Com'l. & Mil.		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
fS	Clock Cycle Frequency	—	50	—	40	—	33	—	20	MHz
tA	Data Access Time	2	14	3	15	3	18	3	25	ns
tCLK	Clock Cycle Time	20	—	25	—	30	—	50	—	ns
tCLKH	Clock High Time	8	—	10	—	12	—	20	—	ns
tCLKL	Clock Low Time	9	—	10	—	12	—	20	—	ns
tDG	Data Set-up Time	5	—	6	—	7	—	10	—	ns
tDH	Data Hold Time	1	—	1	—	1	—	2	—	ns
tENS	Enable Set-up Time	5	—	6	—	7	—	10	—	ns
tENH	Enable Hold Time	1	—	1	—	1	—	2	—	ns
tRS	Reset Pulse Width[1]	20	—	25	—	30	—	50	—	ns
tRSS	Reset Set-up Time[2]	12	—	15	—	18	—	30	—	ns
tRSF	Reset to Flag and Output Time	—	20	—	25	—	30	—	50	ns
tOLZ	Output Enable to Output in Low Z[2]	0	—	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	—	9	—	12	—	15	—	20	ns
tOHZ	Output Enable to Output in High Z[2]	1	9	1	12	1	15	1	20	ns
tWFF	Write Clock to Full Flag	—	14	—	16	—	18	—	30	ns
tREF	Read Clock to Empty Flag	—	12	—	15	—	18	—	30	ns
tPAF	Clock to Programmable Almost-Full Flag	—	20	—	22	—	24	—	35	ns
tPAE	Clock to Programmable Almost-Empty Flag	—	20	—	22	—	24	—	35	ns
tHF	Clock to Half-Full Flag	—	22	—	22	—	24	—	35	ns
tXO	Clock to Expansion Out	—	12	—	15	—	18	—	30	ns
tXI	Expansion In Pulse Width	8	—	10	—	12	—	20	—	ns
tXIS	Expansion In Set-Up Time	8	—	10	—	12	—	20	—	ns
tSKEW1	Skew time between Read Clock & Write Clock for Full Flag	14	—	16	—	18	—	20	—	ns
tSKEW2	Skew time between Read Clock & Write Clock for Empty Flag	14	—	16	—	18	—	20	—	ns

2729 tbl 05

NOTES:

1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

Integrated Device Technology, Inc.

CMOS PARALLEL FIFO 64 x 4-BIT AND 64 x 5-BIT

IDT72401
IDT72402
IDT72403
IDT72404

FEATURES:

- First-In/First-Out dual-port memory
- 64 x 4 organization (IDT72401/03)
- 64 x 5 organization (IDT72402/04)
- IDT72401/02 pin and functionally compatible with MMI67401/02
- RAM-based FIFO with low fall-through time
- Low power consumption
  — Active: 175mW (typ.)
- Maximum shift rate — 45MHz
- High data output drive capability
- Asynchronous and simultaneous read and write
- Fully expandable by bit width
- Fully expandable by word depth
- IDT72403/04 have Output Enable pin to enable output data
- High-speed data communications applications
- High-performance CEMOS™ technology
- Available in CERDIP, plastic DIP and SOIC
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-86846 and 5962-89523 is listed on this function.

DESCRIPTION:

The IDT72401 and IDT72403 are asynchronous high-performance First-In/First-Out memories organized 64 words by 4 bits. The IDT72402 and IDT72404 are asynchronous high-performance First-In/First-Out memories organized as 64 words by 5 bits. The IDT72403 and IDT72404 also have an Output Enable ($\overline{OE}$) pin. The FIFOs accept 4-bit or 5-bit data at the data input ($D_{0\text{-}D3,4}$). The stored data stack up on a first-in/first-out basis.

A Shift Out (SO) signal causes the data at the next to last word to be shifted to the output while all other data shifts down one location in the stack. The Input Ready (IR) signal acts like a flag to indicate when the input is ready for new data (IR = HIGH) or to signal when the FIFO is full (IR = LOW). The Input Ready signal can also be used to cascade multiple devices together. The Output Ready (OR) signal is a flag to indicate that the output remains valid data (OR = HIGH) or to indicate that the FIFO is empty (OR = LOW). The Output Ready can also be used to cascade multiple devices together.

Width expansion is accomplished by logically ANDing the Input Ready (IR) and Output Ready (OR) signals to form composite signals.

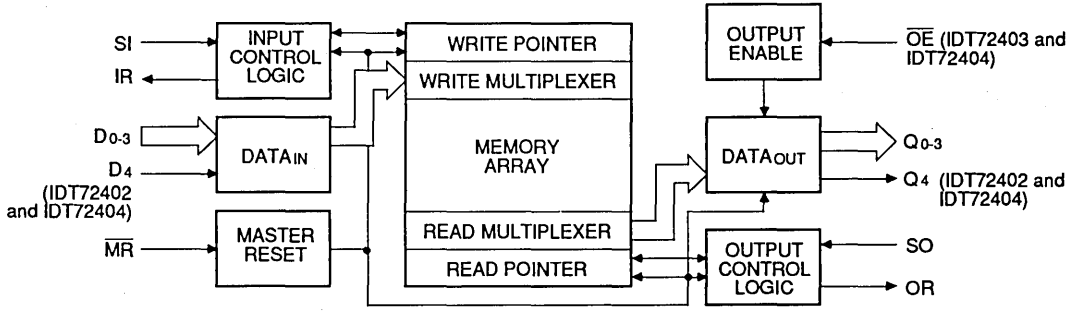
Depth expansion is accomplished by tying the data inputs of one device to the data outputs of the previous device. The Input Ready pin of the receiving device is connected to the Shift Out pin of the sending device and the Output Ready pin of the sending device is connected to the Shift In pin of the receiving device.

Reading and writing operations are completely asynchronous allowing the FIFO to be used as a buffer between two digital machines of widely varying operating frequencies. The 45MHz speed makes these FIFOs ideal for high-speed communication and controller applications.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

6

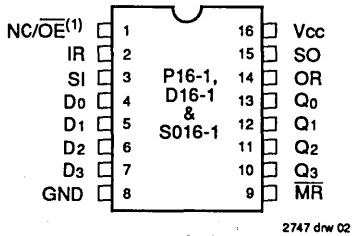
FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

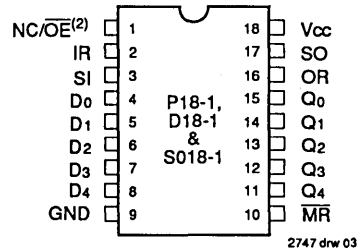
PIN CONFIGURATIONS

IDT72401
IDT72403



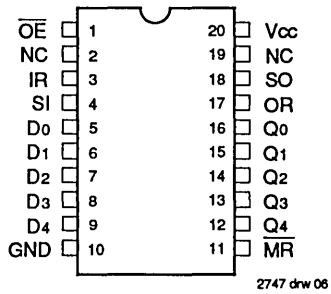
DIP/SOIC
TOP VIEW

IDT72402
IDT72404



DIP/SOIC
TOP VIEW

(IDT72404 Only)



CERPACK
TOP VIEW

NOTES:
1. Pin 1: NC - No Connection IDT72401
   $\overline{OE}$ - IDT72403
2. Pin 1: NC - No Connection IDT72402
   $\overline{OE}$ - IDT72404

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2747 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	—	V
V_{IL}(1)	Input High Voltage	—	—	0.8	V

NOTE: 2747 tbl 03

1. 1.5V undershoots are allowed for 10ns once per cycle.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2747 tbl 02

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{IC}(1)	Input Clamp Voltage		—	—	—
V_{IL}	Low-Level Input Current	V_{CC} = Max., GND ≤ V_I ≤ V_{CC}	-10	—	µA
V_{IH}	High-Level Input Current	V_{CC} = Max., GND ≤ V_I ≤ V_{CC}	—	10	µA
V_{OL}	Low-Level Output Current	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	High-Level Output Current	V_{CC} = Min., I_{OH} = -4mA	2.4	—	V
I_{OS}(2)	Output Short-Circuit Current	V_{CC} = Max., V_O = GND	-20	-90	mA
I_{HZ}	Off-State Output Current	V_{CC} = Max., V_O = 2.4V	—	20	µA
I_{LZ}	(IDT72403 and IDT72404)	V_{CC} = Max., V_O = 0.4V	-20	—	µA
I_{CC}(3, 4)	Supply Current	V_{CC} = Max., f = 10MHz Commercial Military	 — —	 35 45	mA

NOTES: 2747 tbl 04

1. FIFO is able to withstand a -1.5V undershoot for less than 10ns.
2. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. Guaranteed but not tested.
3. Icc measurements are made with outputs open. $\overline{OE}$ is HIGH for IDT72403/72404.
4. For frequencies greater than 10MHZ, Icc = 35mA + (1.5mA x [f - 10MHz]) commercial, and Icc = 45mA + (1.5mA x [f - 10MHz]) military.

6

OPERATING CONDITIONS

(Commercial: Vcc = 5.0V ± 10%, TA = 0°C to +70°C; Military: Vcc = 5.0V ± 10%, TA = -55°C to +125°C)

			Commercial		Military and Commercial								
			IDT72401L45 IDT72402L45 IDT72403L45 IDT72404L45		IDT72401L35 IDT72402L35 IDT72403L35 IDT72404L35		IDT72401L25 IDT72402L25 IDT72403L25 IDT72404L25		IDT72401L15 IDT72402L15 IDT72403L15 IDT72404L15		IDT72401L10 IDT72402L10 IDT72403L10 IDT72404L10		
Symbol	Parameters	Figure	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{SIH}[1]	Shift in HIGH Time	2	9	—	9	—	11	—	11	—	11	—	ns
t_{SIL}	Shift in LOW TIme	2	11	—	17	—	24	—	25	—	30	—	ns
t_{IDS}	Input Data Set-up	2	0	—	0	—	0	—	0	—	0	—	ns
t_{IDH}	Input Data Hold Time	2	13	—	15	—	20	—	30	—	40	—	ns
t_{SOH}[1]	Shift Out HIGH Time	5	9	—	9	—	11	—	11	—	11	—	ns
t_{SOL}	Shift Out LOW Time	5	11	—	17	—	24	—	25	—	25	—	ns
t_{MRW}	Master Reset Pulse	8	20	—	25	—	25	—	25	—	30	—	ns
t_{MRS}	Master Reset Pulse to SI	8	10	—	10	—	10	—	25	—	35	—	ns
t_{SIR}	Data Set-up to IR	4	3	—	3	—	5	—	5	—	5	—	ns
t_{HIR}	Data Hold from IR	4	13	—	15	—	20	—	30	—	30	—	ns
t_{SOR}[4]	Data Set-up to OR HIGH	7	0	—	0	—	0	—	0	—	0	—	ns

2747 tbl 05

AC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 5.0V ± 10%, TA = 0°C to +70°C; Military: Vcc = 5.0V ± 10%, TA = -55°C to +125°C)

			Commercial		Military and Commercial								
			IDT72401L45 IDT72402L45 IDT72403L45 IDT72404L45		IDT72401L35 IDT72402L35 IDT72403L35 IDT72404L35		IDT72401L25 IDT72402L25 IDT72403L25 IDT72404L25		IDT72401L15 IDT72402L15 IDT72403L15 IDT72404L15		IDT72401L10 IDT72402L10 IDT72403L10 IDT72404L10		
Symbol	Parameters	Figure	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{IN}	Shift In Rate	2	—	45	—	35	—	25	—	15	—	10	MHz
t_{IRL}[1]	Shift In to Input Ready LOW	2	—	18	—	18	—	21	—	35	—	40	ns
t_{IRH}[1]	Shift In to Input Ready HIGH	2	—	18	—	20	—	28	—	40	—	45	ns
t_{OUT}	Shift Out Rate	5	—	45	—	35	—	25	—	15	—	10	MHz
t_{ORL}[1]	Shift Out to Output Ready LOW	5	—	18	—	18	—	19	—	35	—	40	ns
t_{ORH}[1]	Shift Out to Output Ready HIGH	5	—	19	—	20	—	34	—	40	—	55	ns
t_{ODH}	Output Data Hold (Previous Word)	5	5	—	5	—	5	—	5	—	5	—	ns
t_{ODS}	Output Data Shift (Next Word)	5	—	19	—	20	—	34	—	40	—	55	ns
t_{PT}	Data Throughput or "Fall-Through"	4, 7	—	30	—	34	—	40	—	65	—	65	ns
t_{MRORL}	Master Reset to OR LOW	8	—	25	—	28	—	35	—	35	—	40	ns
t_{MRIRH}	Master Reset to IR HIGH	8	—	25	—	28	—	35	—	35	—	40	ns
t_{MRQ}	Master Reset to Data Output LOW	8	—	20	—	20	—	25	—	35	—	40	ns
t_{OOE}[3]	Output Valid from $\overline{OE}$ LOW	9	—	12	—	15	—	20	—	30	—	35	ns
t_{HZOE}[3,4]	Output HIGH-Z from $\overline{OE}$ HIGH	9	—	12	—	12	—	15	—	25	—	30	ns
t_{IPH}[2,4]	Input Ready Pulse HIGH	4	9	—	9	—	11	—	11	—	11	—	ns
t_{OPH}[2,4]	Ouput Ready Pulse HIGH	7	9	—	9	—	11	—	11	—	11	—	ns

NOTES:

2747 tbl 06

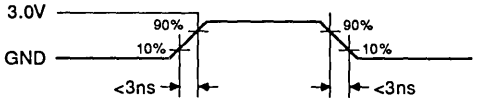
1. Since the FIFO is a very high-speed device, care must be excercised in the design of the hardware and timing utilized within the design. Device grounding and decoupling are crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. A monolithic ceramic capacitor of 0.1µF directly between Vcc and GND with very short lead length is recommended.
2. This parameter applies to FIFOs communicating with each other in a cascaded mode. IDT FIFOs are guaranteed to cascade with other IDT FIFOs of like speed grades.
3. IDT72403 and IDT72404 only.
4. Guaranteed by design but not currently tested.

AC TEST CONDITIONS

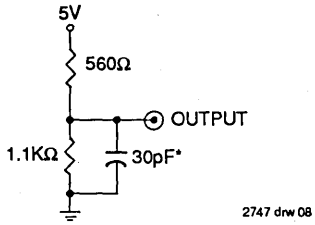
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2754 tbl 08

ALL INPUT PULSES:



2747 drw 07



2747 drw 08

or equivalent circuit

Figure 1. AC Test Load

*Including scope and jig

SIGNAL DESCRIPTIONS

INPUTS:

DATA INPUT ($D_{0-3, 4}$)

Data input lines. The IDT72401 and IDT72403 have a 4-bit data input. The IDT72402 and IDT72404 have a 5-bit data input.

CONTROLS:

SHIFT IN (SI)

Shift In controls the input of the data into the FIFO. When SI is HIGH, data can be written to the FIFO via the $D_{0-3, 4}$ lines.

SHIFT OUT (SO)

Shift Out controls the output of data of the FIFO. When SO is HIGH, data can be read from the FIFO via the Data Output ($Q_{0-3, 4}$) lines.

MASTER RESET ($\overline{MR}$)

Master Reset clears the FIFO of any data stored within. Upon power up, the FIFO should be cleared with a Master Reset. Master Reset is active LOW.

INPUT READY (IR)

When Input Ready is HIGH, the FIFO is ready for new input data to be written to it. When IR is LOW the FIFO is unavailable for new input data. Input Ready is also used to cascade many FIFOs together, as shown in Figures 10 and 11 in the Applications section.

OUTPUT READY (OR)

When Output Ready is HIGH, the output ($Q_{0-3, 4}$) contains valid data. When OR is LOW, the FIFO is unavailable for new output data. Output Ready is also used to cascade many FIFOs together, as shown in Figures 10 and 11.

OUTPUT ENABLE ($\overline{OE}$) (IDT72403 AND IDT72404 ONLY)

Output enable is used to read FIFO data onto a bus. Output Enable is active LOW.

OUTPUTS:

DATA OUTPUT ($Q_{0-3, 4}$)

Data Output lines. The IDT72401 and IDT72403 have a 4-bit data output. The IDT72402 and IDT72404 have a 5-bit data output.

FUNCTIONAL DESCRIPTION

These 64 x 4 and 64 x 5 FIFOs are designed using a dual port RAM architecture as opposed to the traditional shift register approach. This FIFO architecture has a write pointer, a read pointer and control logic, which allow simultaneous read and write operations. The write pointer is incremented by the falling edge of the Shift In (SI) control; the read pointer is incremented by the falling edge of the Shift Out (SO). The Input Ready (IR) signals when the FIFO has an available memory location; Output Ready (OR) signals when there is valid data on the output. Output Enable ($\overline{OE}$) provides the capability of three-stating the FIFO outputs.

FIFO Reset

The FIFO must be reset upon power up using the Master Reset ($\overline{MR}$) signal. This causes the FIFO to enter an empty state, signified by Output Ready (OR) being LOW and Input Ready (IR) being HIGH. In this state, the data outputs ($Q_{0-3, 4}$) will be LOW.

Data Input

Data is shifted in on the LOW-to-HIGH transition of Shift In (SI). This loads input data into the first word location of the FIFO and causes Input Ready to go LOW. On the HIGH-to-LOW transition of Shift In, the write pointer is moved to the next word position and Input Ready (IR) goes HIGH, indicating the readiness to accept new data. If the FIFO is full, Input Ready will remain LOW until a word of data is shifted out.

6

Data Output

Data is shifted out on the HIGH-to-LOW transition of Shift Out (SO). This causes the internal read pointer to be advanced to the next word location. If data is present, valid data will appear on the outputs and Output Ready (OR) will go HIGH. If data is not present, Output Ready will stay LOW indicating the FIFO is empty. The last valid word read from the FIFO will remain at the FIFOs output when it is empty. When the FIFO is not empty, Output Ready (OR) goes LOW on the LOW-to-HIGH transition of Shift Out. Previous data remains on the output until the HIGH-to-LOW transition of Shift Out (SO).

Fall-Through Mode

The FIFO operates in a fall-through mode when data gets shifted into an empty FIFO. After a fall-through delay the data propagates to the output. When the data reaches the output, the Output Ready (OR) goes HIGH. Fall-through mode also occurs when the FIFO is completely full. When data is shifted out of the full FIFO, a location is available for new data. After a fall-through delay, the Input Ready goes HIGH. If Shift In is HIGH, the new data can be written to the FIFO.

TIMING DIAGRAMS

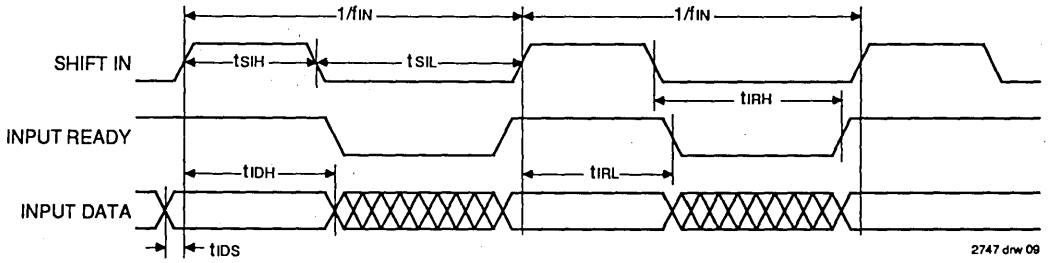
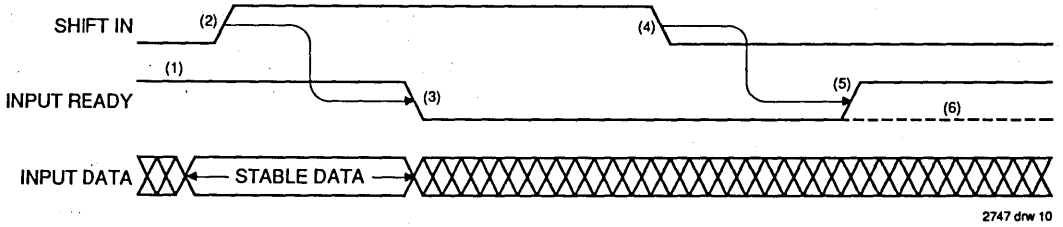


Figure 2. Input Timing

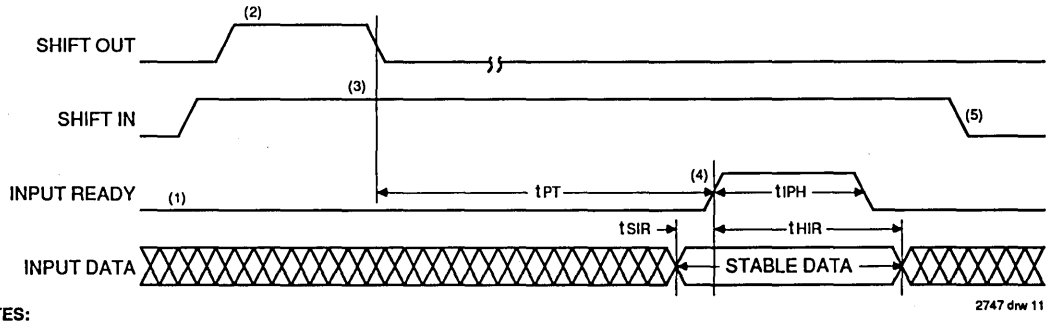


NOTES:
1. Input Ready HIGH indicates space is available and a Shift In pulse may be applied.
2. Input Data is loaded into the first word.
3. Input Ready goes LOW indicating the first word is full.
4. The write pointer is incremented.
5. The FIFO is ready for the next word.
6. If the FIFO is full then the Input Ready remains LOW.

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored (see Figure 4).

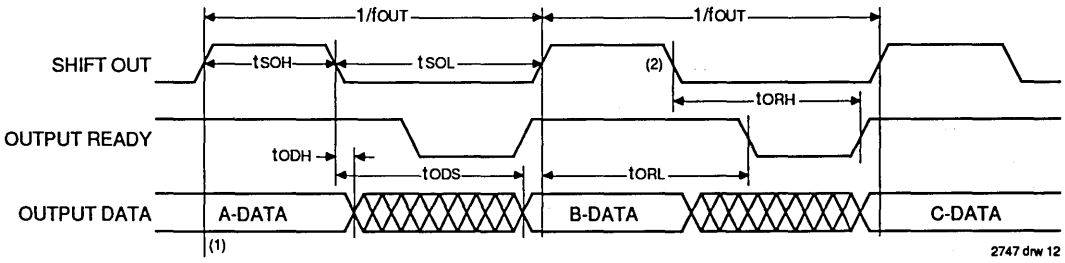
Figure 3. The Mechanism of Shifting Data Into the FIFO

TIMING DIAGRAMS (Continued)



NOTES:
1. FIFO is initially full.
2. Shift Out pulse is applied.
3. Shift In is held HIGH.
4. As soon as Input Ready becomes HIGH the Input Data is loaded into the FIFO.
5. The write pointer is incremented. Shift In should not go LOW until (t_{PT} + t_{IPH}).

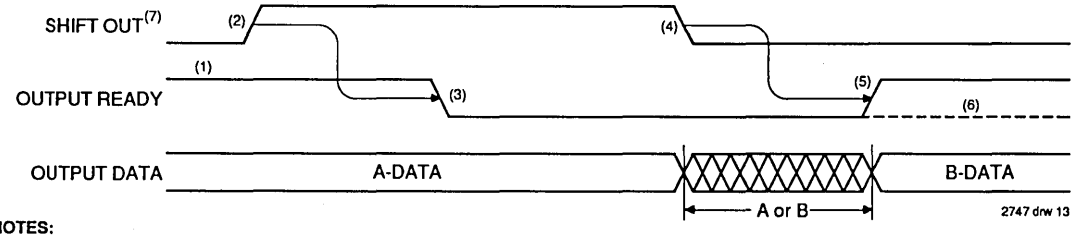
Figure 4. Data Is Shifted In Whenever Shift In and Input Ready are Both HIGH



NOTES:
1. This data is loaded consecutively A, B, C.
2. Data is shifted out when Shift Out makes a HIGH to LOW transition.

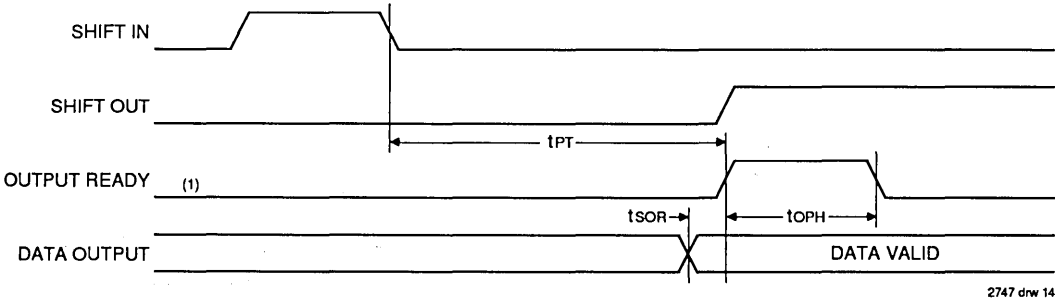
Figure 5. Output Timing

TIMING DIAGRAMS (Continued)



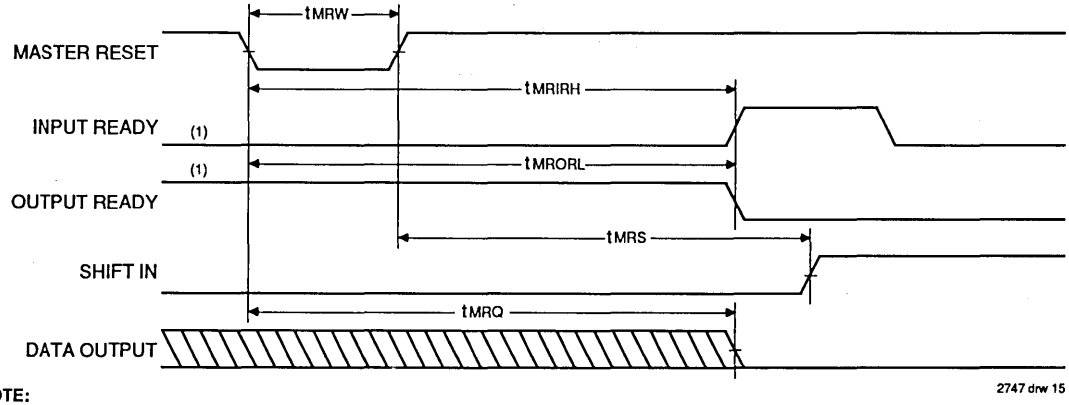
NOTES:
1. Input Ready HIGH indicates that data is available and a Shift In pulse may be applied.
2. Shift Out goes HIGH causing the next step.
3. Output Ready goes LOW.
4. The read pointer is incremented.
5. Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.
6. If the FIFO has only one word loaded (A DATA) then Output Ready stays LOW and the A DATA remains unchanged at the outputs.
7. Shift Out pulses applied when Output Ready is LOW will be ignored.

Figure 6. The Mechanism of Shifting Data Out of the FIFO



NOTE:
1. FIFO initially empty.

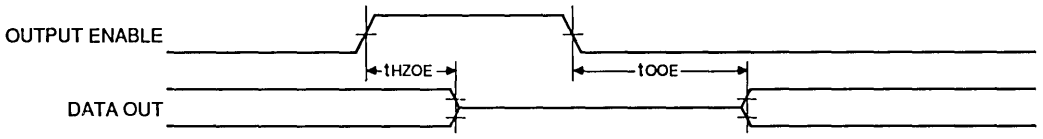
Figure 7. tPT and tOPH Specification



NOTE:
1. Worst case, FIFO initially full.

Figure 8. Master Reset Timing

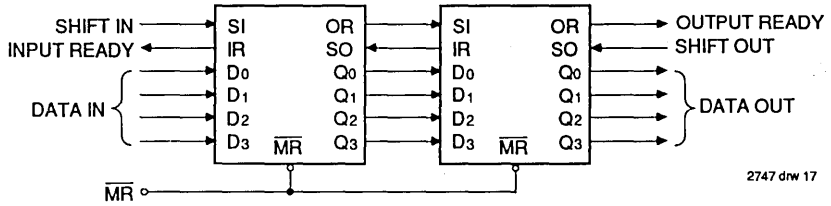
TIMING DIAGRAMS (Continued)



NOTE:
1. High-Z transitions are referenced to the steady-state V_{OH} -500mV and V_{OL} +500mV levels on the output. t_{HZOE} is tested with 5pF load capacitance instead of 30pF as shown in Figure 1.

Figure 9. Output Enable Timing, IDT72403 and IDT72404 Only

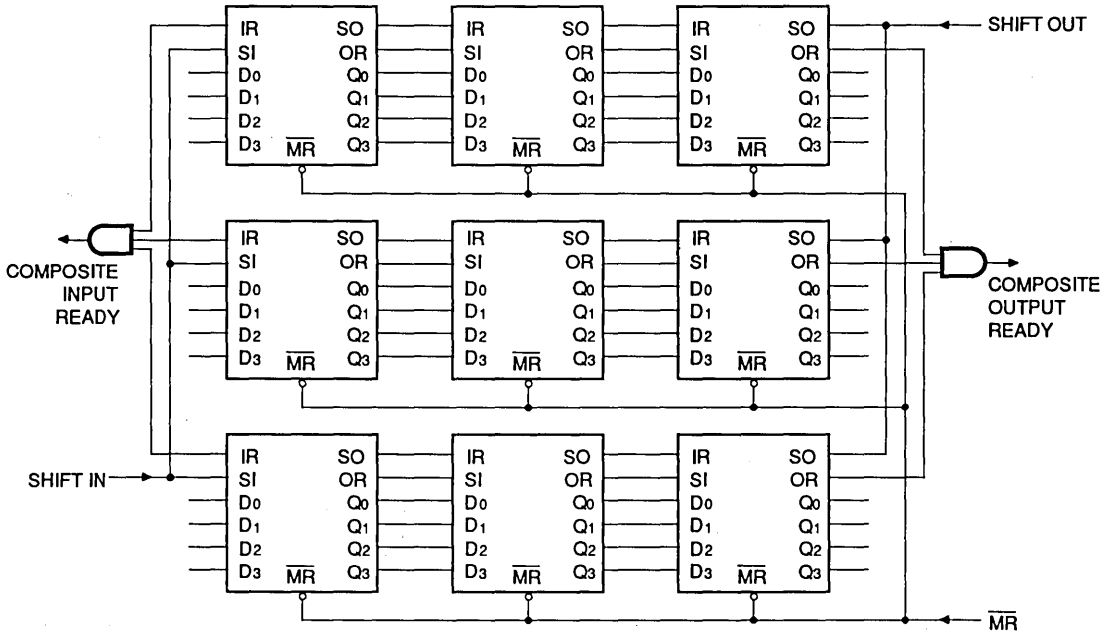
APPLICATIONS



NOTE:
1. FIFOs can be easily cascaded to any desired path. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.

Figure 10. 128 x 4 Depth Expansion

6

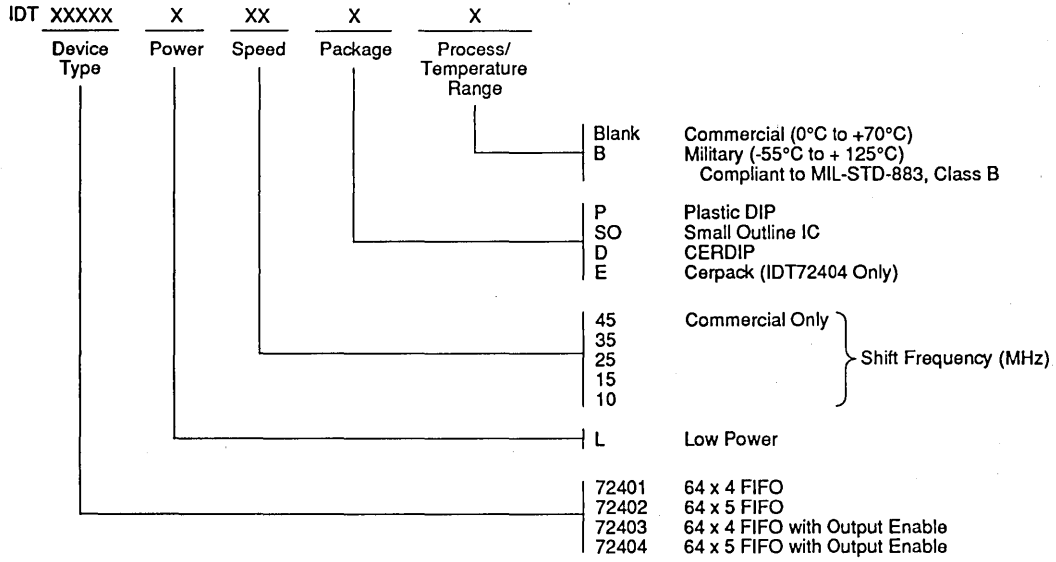


NOTES:

1. When the memory is empty, the last word will remain on the outputs until the Master Reset is strobed or a new data word falls through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data and stays LOW until the new data has appeared on the outputs. Anytime OR is HIGH, there is valid stable data on the outputs.
3. If SO is held HIGH while the memory is empty and a word is written into the input, that word will appear at the output after a fall-through time. OR will go HIGH for one internal cycle (at least t_{ORL}) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
4. When the Master Reset is brought Low, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW. If SI is HIGH when the Master Reset goes HIGH, the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the Master Reset is ended, IR will go HIGH, but the data in the inputs will not enter the memory until SI goes HIGH.
5. FIFOs are expandable on depth and width. However, in forming wider words, two external gates are required to generate composite Input and Output Ready flags. This is due to the variation of delays of the FIFOs.

Figure 11. 192 x 12 Depth and Width Expansion

ORDERING INFORMATION



2747 drw 19

6

Integrated Device Technology, Inc.

CMOS PARALLEL 64 x 5-BIT FIFO WITH FLAGS

IDT72413

FEATURES:

- First-In/First-Out dual-port memory—45MHz
- 64 x 5 organization
- Low power consumption
  — Active: 200mW (typical)
- RAM-based internal structure allows for fast fall-through time
- Asynchronous and simultaneous read and write
- Expandable by bit width
- Cascadable by word depth
- Half-Full and Almost-Full/Empty status flags
- IDT72413 is pin and functionally compatible with the MMI67413
- High-speed data communications applications
- Bidirectional and rate buffer applications
- High-performance CEMOS™ technology
- Available in plastic DIP, CERDIP and SOIC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72413 is a 64 x 5, high speed First-In/First-Out (FIFO) that loads and empties data on a first-in-first-out basis. It is expandable in bit width. All speed versions are cascadable in depth.

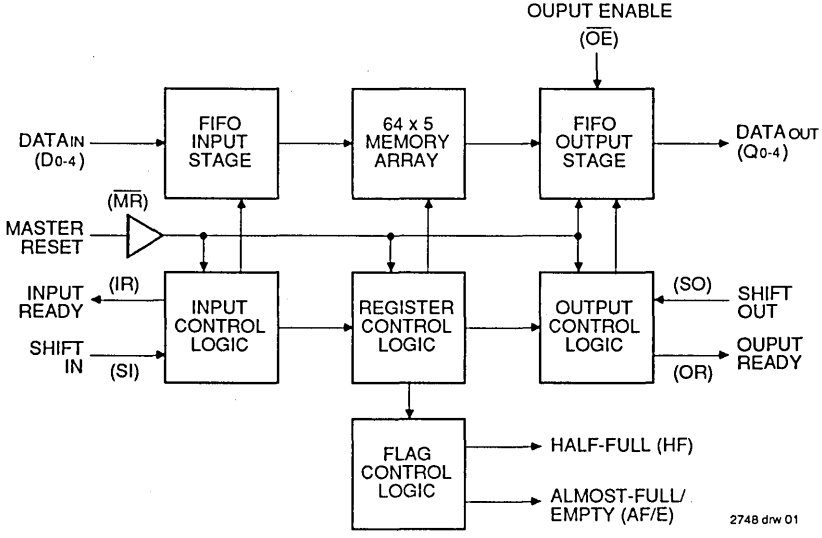
The FIFO has a Half-Full Flag, which signals when it has 32 or more words in memory. The Almost-Full/Empty Flag is active when there are 56 or more words in memory or when there are 8 or less words in memory.

The IDT72413 is pin and functionally compatible to the MMI67413. It operates at a shift rate of 45MHz. This makes it ideal for use in high-speed data buffering applications. The IDT72413 can be used as a rate buffer, between two digital systems of varying data rates, in high-speed tape drivers, hard disk controllers, data communications controllers and graphics controllers.

The IDT72413 is fabricated using IDTs high-performance CEMOS process. This process maintains the speed and high output drive capability of TTL circuits in low-power CMOS.

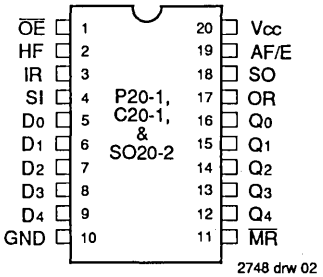
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



DIP/SOIC
TOP VIEW

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Military Supply Voltage	4.5	5.0	5.5	V
Vcc	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.0	—	—	V
VIL[1]	Input Low Voltage	—	—	0.8	V

2748 tbl 03

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

2748 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	5	pF
COUT	Output Capacitance	VOUT = 0V	7	pF

2748 tbl 02

NOTE:
1. This parameter is sampled and not 100% tested.
2. Characterized values, not currently listed.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	Test Conditions			Min.	Max.	Unit
V_{IC}[1]	Input Clamp Voltage				—	—	
I_{IL}	Low-Level Input Current	V_{CC} = Max., GND ≤ V_I ≤ V_{CC}			-10	—	µA
I_{IH}	High-Level Input Current	V_{CC} = Max., GND ≤ V_I ≤ V_{CC}			—	10	µA
V_{OL}	Low-Level Output Current	V_{CC} = Min.	I_{OL} (Q_{0-4})	Mil.	12mA	—	0.4	V
				Com'l.	24mA			
			I_{OL} (IR, OR)[2]		8mA			
			I_{OL} (HF, AF/E)		8mA			
V_{OH}	High-Level Output Current	V_{CC} = Min.	I_{OH} (Q_{0-4})		-4mA	2.4	—	V
			I_{OH} (IR, OR)		-4mA			
			I_{OH} (HF, AF/E)		-4mA			
I_{OS}[3]	Output Short-Circuit Current	V_{CC} = Max.	V_O = 0V			-20	-90	mA
I_{HZ}	Off-State Output Current	V_{CC} = Max.	V_O = 2.4V			—	20	µA
I_{LZ}		V_{CC} = Max.	V_O = 0.4V			-20	—	
I_{CC}[4]	Supply Current	V_{CC} = Max., $\overline{OE}$=HIGH		Mil.		—	70	mA
		Inputs LOW, f=25MHz		Com'l.		—	60	

NOTES: 2748 tbl 04

1. FIFO is able to withstand a -1.5V undershoot for less than 10ns.
2. Care should be taken to minimize as much as possible the DC and capactive load on IR and OR when operating at frequencies above 25mHz.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second. Guaranteed by design, but not currently tested.
4. For frequencies greater than 25MHz, I_{CC} = 60mA + (1.5mA x [f - 25MHz]) commercial and I_{CC} = 70mA + (1.5mA x [f - 25MHz]) military.

OPERATING CONDITIONS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)

			Military		Military & Commercial		Commercial		
			IDT72413L45		IDT72413L35		IDT72413L25		
Symbol	Parameters	Figure	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{SIH}[1]	Shift in HIGH Time	2	9	—	9	—	16	—	ns
t_{SIL}[1]	Shift in LOW TIme	2	11	—	17	—	20	—	ns
t_{IDS}	Input Data Set-up	2	0	—	0	—	0	—	ns
t_{IDH}	Input Data Hold Time	2	13	—	15	—	25	—	ns
t_{SOH}[1]	Shift Out HIGH Time	5	9	—	9	—	16	—	ns
t_{SOL}	Shift Out LOW Time	5	11	—	17	—	20	—	ns
t_{MRW}	Master Reset Pulse	8	20	—	30	—	35	—	ns
t_{MRS}[3]	Master Reset Pulse to SI	8	20	—	35	—	35	—	ns

NOTE: 2748 tbl 05

1. Since the FIFO is a very high-speed device, care must be excercised in the design of the hardware and timing utilized within the design. Device grounding and decoupling are crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. A monolithic ceramic capacitor of 0.1µF directly between VCC and GND with very short lead length is recommended.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)

			Military		Military & Commercial				
			IDT72413L45		IDT72413L35		IDT72413L25		
Symbol	Parameters	Figure	Min.	Max.	Min.	Max.	Min.	Max.	Unit
f_{IN}	Shift In Rate	2	—	45	—	35	—	25	MHz
t_{IRL}[1]	Shift In ↑ to Input Ready LOW	2	—	18	—	18	—	28	ns
t_{IRH}[1]	Shift In ↓ to Input Ready HIGH	2	—	18	—	20	—	25	ns
f_{OUT}	Shift Out Rate	5	—	45	—	35	—	25	MHz
t_{ORL}[1]	Shift Out ↓ to Output Ready LOW	5	—	18	—	18	—	28	ns
t_{ORH}[1]	Shift Out ↓ to Output Ready HIGH	5	—	19	—	20	—	25	ns
t_{ODH}[1]	Output Data Hold Previous Word	5	5	—	5	—	5	—	ns
t_{ODS}	Output Data Shift Next Word	5	—	19	—	20	—	20	ns
t_{PT}	Data Throughput or "Fall-Through"	4, 7	—	25	—	28	—	40	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	8	—	25	—	28	—	30	ns
t_{MRIRH}[3]	Master Reset ↑ to Input Ready HIGH	8	—	25	—	28	—	30	ns
t_{MRIRL}[2]	Master Reset ↓ to Input Ready LOW	8	—	25	—	28	—	30	ns
t_{MRQ}	Master Reset ↓ to Outputs LOW	8	—	20	—	25	—	35	ns
t_{MRHF}	Master Reset ↓ to Half-Full Flag	8	—	25	—	28	—	40	ns
t_{MRAFE}	Master Reset ↓ to AF/E Flag	8	—	25	—	28	—	40	ns
t_{IPH}[3]	Input Ready Pulse HIGH	4	5	—	5	—	5	—	ns
t_{OPH}[3]	Ouput Ready Pulse HIGH	7	5	—	5	—	5	—	ns
t_{ORD}[3]	Output Ready ↑ HIGH to Valid Data	5	—	5	—	5	—	7	ns
t_{AEH}	Shift Out ↑ to AF/E HIGH	9	—	28	—	28	—	40	ns
t_{AEL}	Shift In ↑ to AF/E	9	—	28	—	28	—	40	ns
t_{AFL}	Shift Out ↑ to AF/E LOW	10	—	28	—	28	—	40	ns
t_{AFH}	Shift In ↑ to AF/E HIGH	10	—	28	—	28	—	40	ns
t_{HFH}	Shift In ↑ to HF HIGH	11	—	28	—	28	—	40	ns
t_{HFL}	Shif Out ↑ to HF LOW	11	—	28	—	28	—	40	ns
t_{PHZ}[3]	Output Disable Delay	12	—	12	—	12	—	15	ns
t_{PLZ}[3]		12	—	12	—	12	—	15	
t_{PLZ}[3]	Output Enable Delay	12	—	15	—	15	—	20	ns
t_{PHZ}[3]		12	—	15	—	15	—	20	

2748 tbl 06

NOTES:

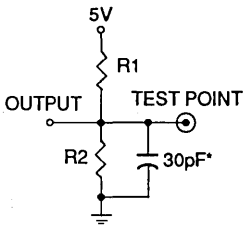
1. Since the FIFO is a very high-speed device, care must be taken in the design of the hardware and the timing utilized within the design. Device grounding and decoupling are crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. A monolithic ceramic capacitor of 0.1µF directly between VCC and GND with very short lead length is recommended.
2. If the FIFO is full, (IR = HIGH), $\overline{MR}$ ↓ forces IR to go LOW, and $\overline{MR}$ ↑ causes IR to go HIGH.
3. Guaranteed by design but not currently tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

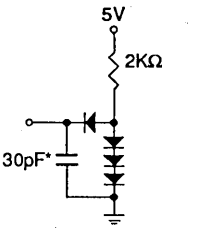
2754 tbl 08

STANDARD TEST LOAD



or equivalent circuit

DESIGN TEST LOAD



2748 drw 03

*Including scope and jig

RESISTOR VALUES FOR STANDARD TEST LOAD

I_{OL}	R1	R2
24mA	200Ω	300Ω
12mA	390Ω	760Ω
8mA	600Ω	1200Ω

Figure 1. Output Load

FUNCTIONAL DESCRIPTION:

The IDT72413, 65 x 5 FIFO is designed using a dual-port RAM architecture as opposed to the traditional shift register approach. This FIFO architecture has a write pointer, a read pointer and control logic, which allow simultaneous read and write operations. The write pointer is incremented by the falling edge of the Shift In (SI) control; the read pointer is incremented by the falling edge of the Shift Out (SO). The Input Ready (IR) signals when the FIFO has an available memory location; Output Ready (OR) signals when there is valid data on the output. Output Enable ($\overline{OE}$) provides the capability of three-stating the FIFO outputs.

FIFO RESET

The FIFO must be reset upon power up using the Master Reset ($\overline{MR}$) signal. This causes the FIFO to enter an empty state signified by Output Ready (OR) being LOW and Input Ready (IR) being HIGH. In this state, the data outputs (Q_{0-4}) will be LOW.

DATA INPUT

Data is shifted in on the LOW-to-HIGH transition of Shift In (SI). This loads input data into the first word location of the FIFO and causes the Input Ready to go LOW. On the HIGH-to-LOW transition of Shift In, the write pointer is moved to the next word position and Input Ready (IR) goes HIGH indicating the readiness to accept new data. If the FIFO is full, Input Ready will remain LOW until a word of data is shifted out.

DATA OUTPUT

Data is shifted out on the HIGH-to-LOW transition of Shift Out (SO). This causes the internal read pointer to be advanced to the next word location. If data is present, valid data will appear on the outputs and Output Ready (OR) will go HIGH. If data is not present, Output Ready will stay LOW indicating the FIFO is empty. The last valid word read from the FIFO will remain at the FIFOs output when it is empty. When the FIFO is not empty Output Ready (OR) goes LOW on the LOW-to-HIGH transition of Shift Out.

FALL-THROUGH MODE

The FIFO operates in a Fall-Through Mode when data gets shifted into an empty FIFO. After the fall-through delay the data propagates to the output. When the data reaches the output, the Output Ready (OR) goes HIGH.

A Fall-Through Mode also occurs when the FIFO is completely full. When data is shifted out of the full FIFO a location is available for new data. After a fall-through delay, the Input Ready goes HIGH. If Shift In is HIGH, the new data can be written to the FIFO. The fall-through delay of a RAM-based FIFO (one clock cycle) is far less than the delay of a Shift register-based FIFO.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA INPUT (D_{0-4})

Data input lines. The IDT72413 has a 5-bit data input.

CONTROLS:

SHIFT IN (SI)

Shift In controls the input of the data into the FIFO. When SI is HIGH, data can be written to the FIFO via the D0-4 lines. The data has to meet set-up and hold time requirements with respect to the rising edge of SI.

SHIFT OUT (SO)

Shift Out controls the outputs data from the FIFO.

MASTER RESET ($\overline{MR}$)

Master Reset clears the FIFO of any data stored within. Upon power up, the FIFO should be cleared with a Master Reset. Master Reset is active LOW.

HALF-FULL FLAG (HF)

Half-Full Flag signals when the FIFO has 32 or more words in it.

INPUT READY(IR)

When Input Ready is HIGH, the FIFO is ready for new input data to be written to it. When IR is LOW, the FIFO is unavailable for new input data, Input Ready is also used to cascade many FIFOs together, as shown in Figure 13 in the Applications section.

OUTPUT READY (OR)

When Output Ready is HIGH, the output (Q_{0-4}) contains valid data. When OR is LOW, the FIFO is unavailable for new output data. Output Ready is also used to cascade many FIFOs together, as shown in Figure 13 in the Applications section.

OUTPUT ENABLE ($\overline{OE}$)

Output Enable is used to enable the FIFO outputs onto a bus. Output Enable is active LOW.

ALMOST-FULL/EMPTY FLAG (AFE)

Almost-Full/Empty Flag signals when the FIFO is 7/8 full (56 or more words) or 1/8 from empty (8 or less words).

OUTPUTS:

DATA OUTPUT (Q_{0-4})

Data output lines, three-state. The IDT72413 has a 5-bit output.

TIMING DIAGRAMS

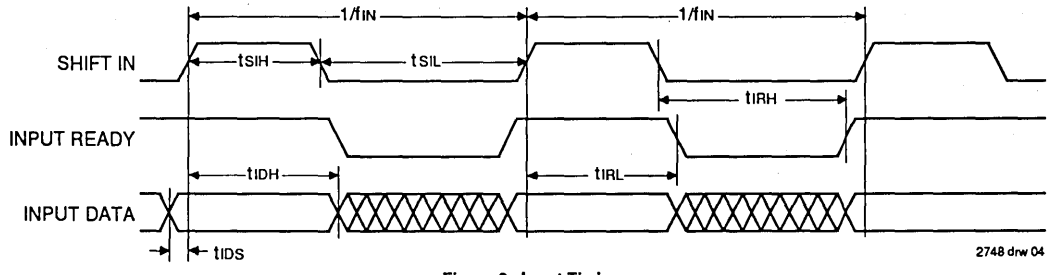
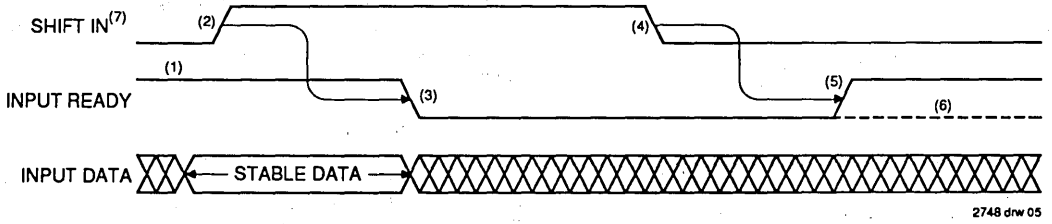


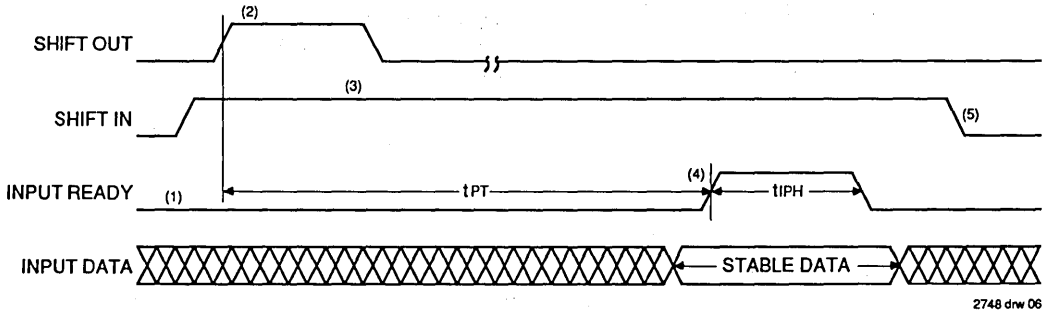
Figure 2. Input Timing

TIMING DIAGRAMS (Continued)



NOTES:
1. Input Ready HIGH indicates space is available and a Shift In pulse may be applied.
2. Input Data is loaded into the FIFO.
3. Input Ready goes LOW indicating the FIFO is unavailable for new data.
4. The write pointer is incremented.
5. The FIFO is ready for the next word.
6. If the FIFO is full, then the Input Ready remains LOW.
7. **Shift In pulses applied while Input Ready is LOW will be ignored (see Figure 4).**

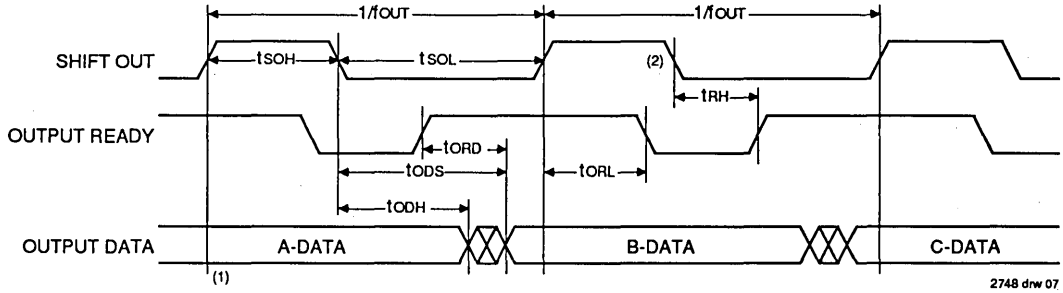
Figure 3. The Machanism of Shifting Data into the FIFO



NOTES:
1. FIFO is initially full.
2. Shift Out pulse is applied.
3. Shift In is held HIGH.
4. As soon as Input Ready becomes HIGH the Input Data is loaded into the FIFO.
5. The write pointer is incremented. Shift In should not go LOW until (t_{PT} + t_{IPH}).

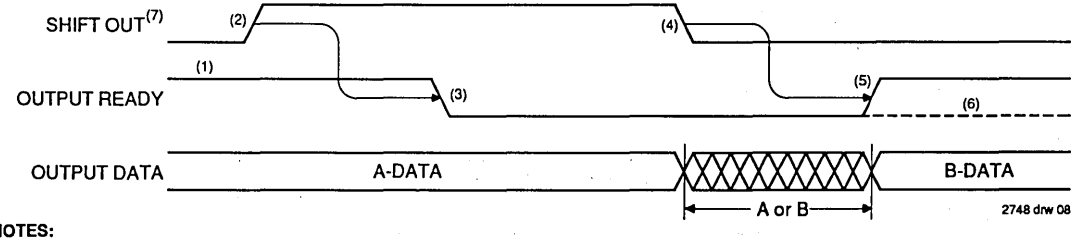
Figure 4. Data Is Shifted In Whenever Shift In and Input Ready are Both HIGH

TIMING DIAGRAMS (Continued)



NOTES:
1. This data is loaded consecutively A, B, C.
2. Output data changes on the falling edge of SO after a valid Shift Out sequence, i.e., OR and SO are both high together.

Figure 5. Output Timing

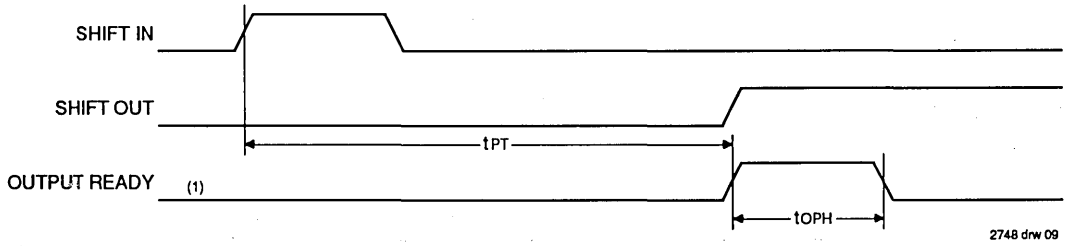


NOTES:
1. Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.
2. Shift Out goes HIGH causing the next step.
3. Output Ready goes LOW.
4. Read pointer is incremented.
5. Output Ready goes HIGH indicating that new data (B) will be available at the FIFO outputs after tORD ns.
6. If the FIFO has only one word loaded (A DATA) , Output Ready stays LOW and the A-DATA remains unchanged at the outputs.
7. Shift Out pulses applied when Output Ready is LOW will be ignored.

Figure 6. The Mechanism of Shifting Data Out of the FIFO

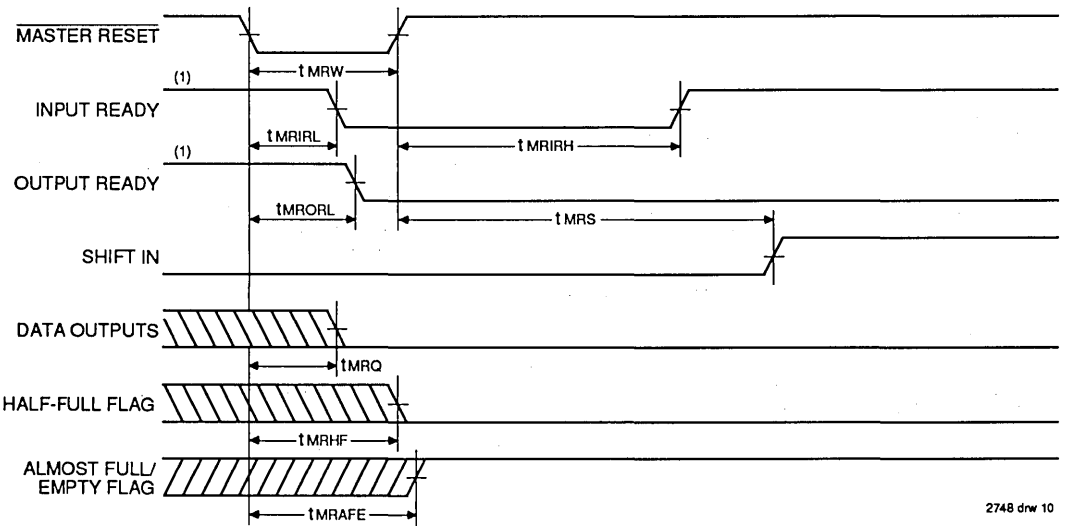
6

TIMING DIAGRAMS (Continued)



NOTE:
1. FIFO initailly empty.

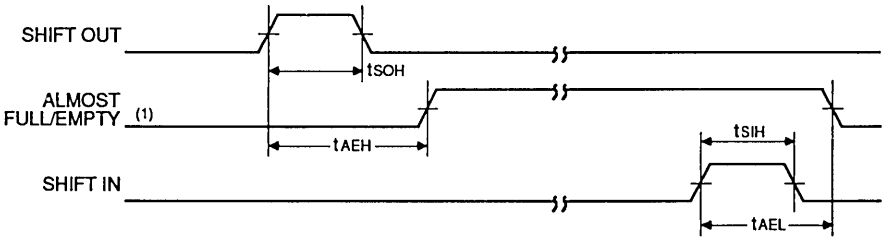
Figure 7. tPT and tOPH Specification



NOTE:
1. FIFO is partially full.

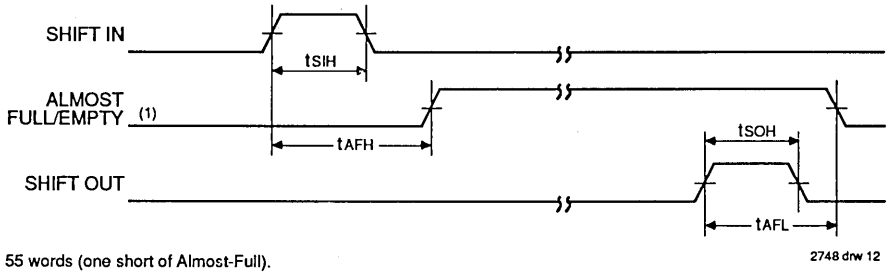
Figure 8. Master Reset Timing

TIMING DIAGRAMS (Continued)



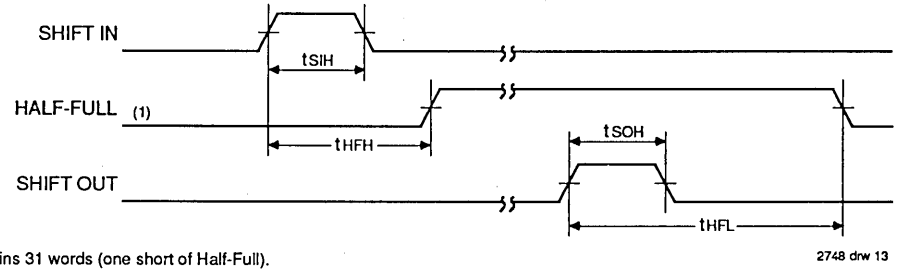
NOTE:
1. FIFO contains 9 words (one more than Almost-Empty).

Figure 9. tAEH and tAEL Specifications



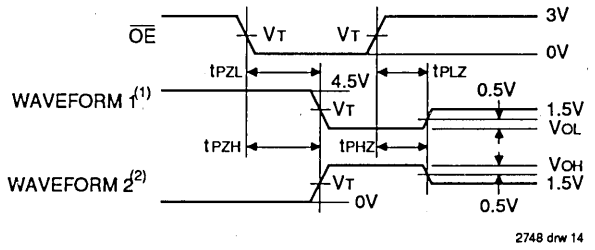
NOTE:
1. FIFO contains 55 words (one short of Almost-Full).

Figure 10. tAFH and tAFL Specifications



NOTE:
1. FIFO contains 31 words (one short of Half-Full).

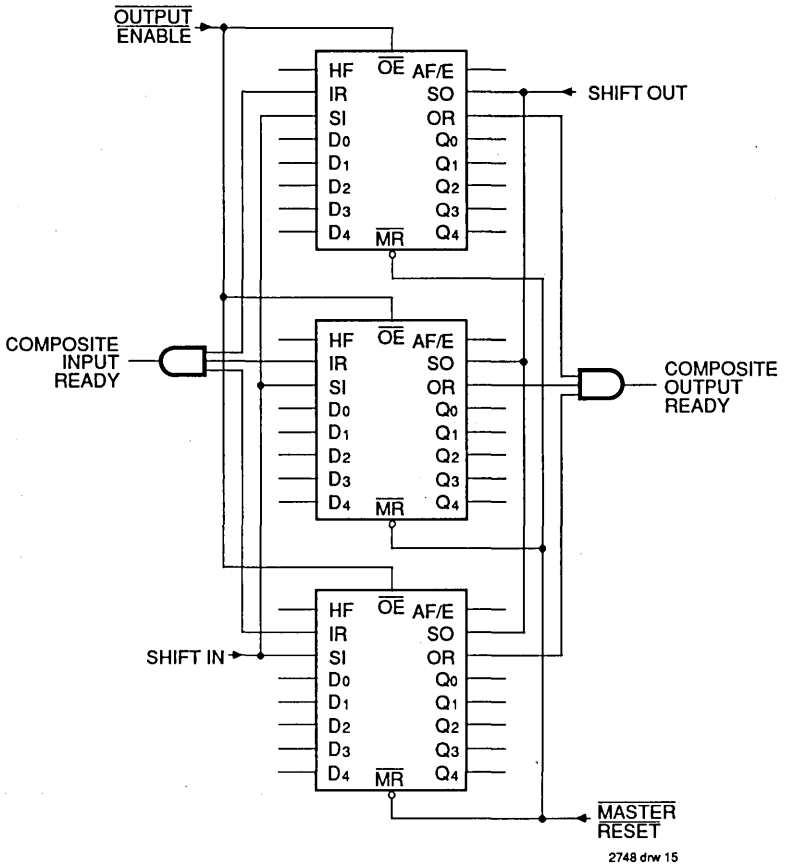
Figure 11. tHFL and tHFH Specifications



NOTES:
1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

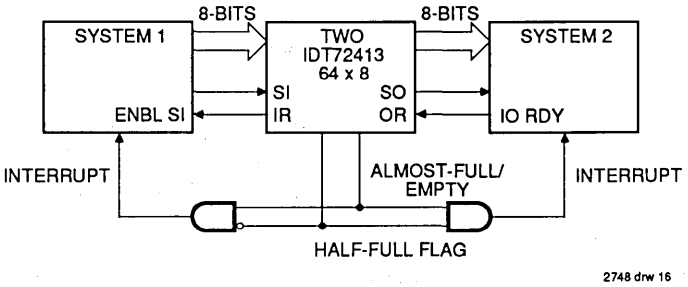
Figure 12. Enable and Disable

APPLICATIONS



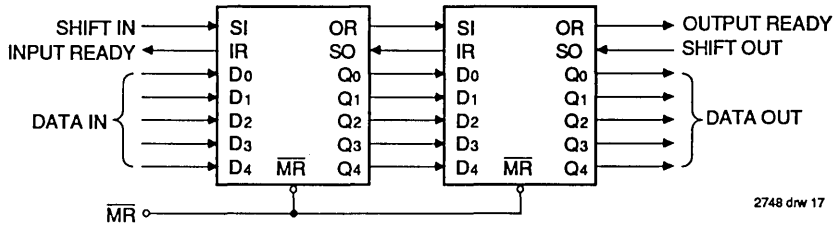
NOTE:
1. FIFOs are expandable in width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This requirement is due to the different fall-through times of the FIFOs.

Figure 13. 64 x 15 FIFO with IDT72413



NOTE:
1. Cascading the FIFOs in word width is done by ANDing the IR and OR as shown in Figure 13.

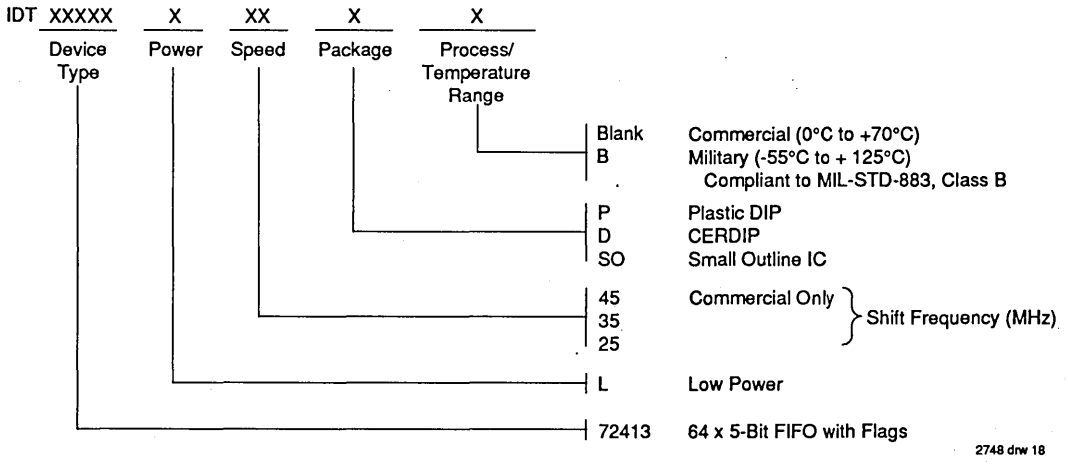
Figure 14. Application for IDT72413 for Two Asynchronous Systems



NOTE:
1. FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.

Figure 15. 128 x 5 Depth Expansion

ORDERING INFORMATION



6

Integrated Device Technology, Inc.

BUS-MATCHING BIDIRECTIONAL FIFO 512 x 18-BIT – 1024 x 9-BIT 1024 x 18-BIT – 2048 x 9-BIT

IDT7251
IDT7252
IDT72510
IDT72520

FEATURES:

- Two side-by-side FIFO memory arrays for bidirectional data transfers
- 512 x 18 - Bit – 1024 x 9 - Bit (IDT7251, IDT72510)
- 1024 x 18 - Bit – 2048 x 9 - Bit (IDT7252, IDT72520)
- 18 bit data bus on Port A side and 9 bit data bus on Port B side
- Can be configured for 18-to-9-bit, 36-to-9-bit, or 36-to-18-bit communication
- Fast 35ns access time
- Fully programmable standard microprocessor interface
- Built-in bypass path for direct data transfer between two ports
- Two fixed flags, Empty and Full, for both the A-to-B and the B-to-A FIFO
- Two programmable flags, Almost-Empty and Almost-Full for each FIFO
- Programmable flag offset can be set to any depth in the FIFO
- Any of the eight internal flags can be assigned to four external flag pins
- Flexible reread/rewrite capabilities.
- On-chip parity checking and generation
- Standard DMA control pins for data exchange with peripherals
- IDT7251 and IDT7252 available in 48-pin plastic or ceramic DIP
- IDT72510 and IDT72520 available in 52-pin PLCC packages (includes LDRER, LDREW, RESET, and one extra GND pin)
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7251, IDT72510, IDT7252, and IDT72520 are highly integrated first-in, first-out memories that enhance processor-to-processor and processor-to-peripheral communications. IDT BiFIFOs integrate two side-by-side memory arrays for data transfers in two directions.

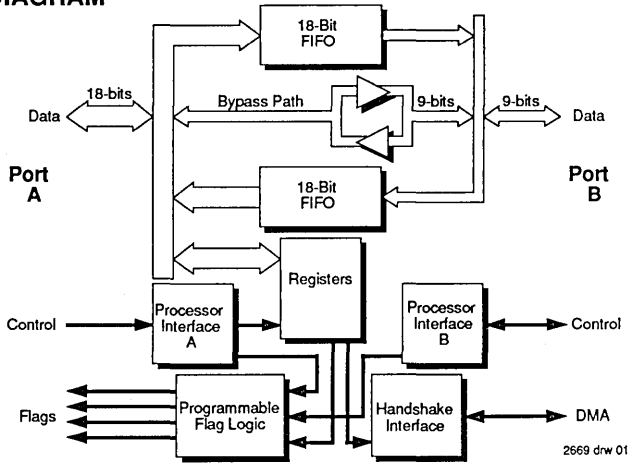
The BiFIFOs have two ports, A and B, that both have standard microprocessor interfaces. All BiFIFO operations are controlled from the 18-bit wide Port A. The BiFIFOs incorporate bus matching logic to convert the 18-bit wide memory data paths to the 9-bit wide Port B data bus. The BiFIFOs have a bypass path that allows the device connected to Port A to pass messages directly to the Port B device.

Ten registers are accessible through Port A, a Command Register, a Status Register, and eight Configuration Registers.

The IDT BiFIFOs have programmable flags. Each FIFO memory array has four internal flags, Empty, Almost-Empty, Almost-Full and Full, for a total of eight internal flags. The Almost-Empty and Almost-Full flag offsets can be set to any depth through the Configuration Registers. These eight internal flags can be assigned to any of four external flag pins (FLGA-FLGD) through one Configuration Register.

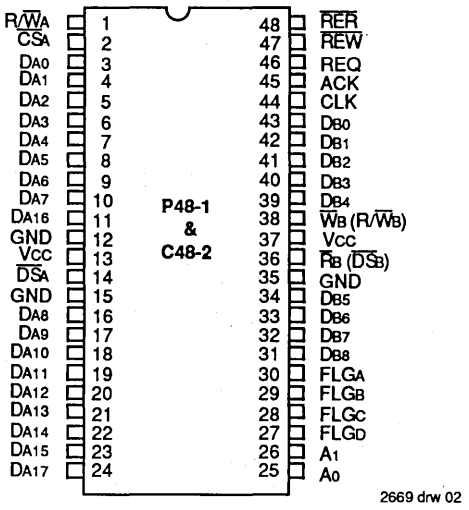
Port B has parity, reread/rewrite and DMA functions. Parity generation and checking can be done by the BiFIFO on data passing through Port B. The Reread and Rewrite controls will read or write Port B data blocks multiple times. The BiFIFOs have three pins, REQ, ACK and CLK, to control DMA transfers from Port B devices.

SIMPLIFIED BLOCK DIAGRAM



PIN CONFIGURATIONS

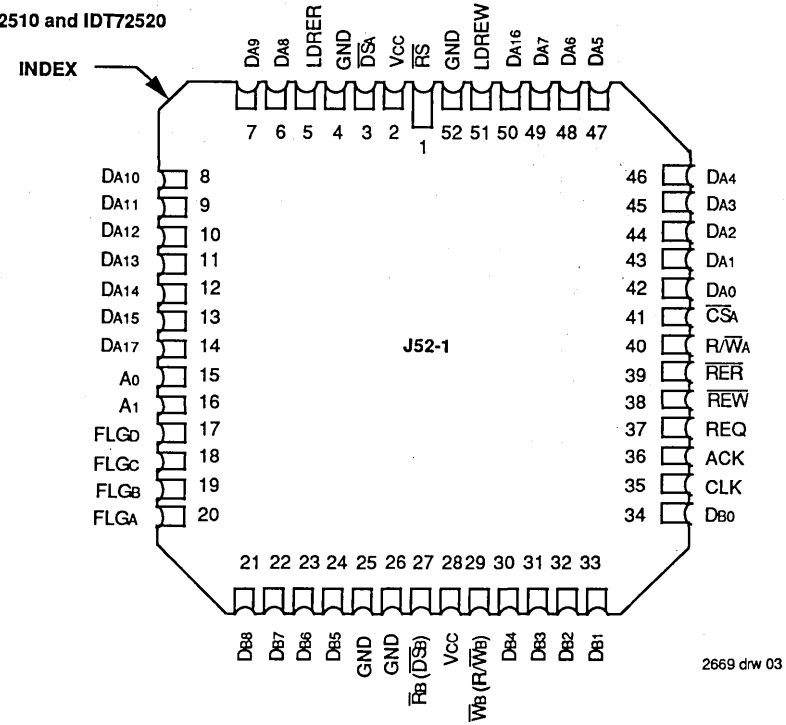
IDT7251 and IDT7252



2669 drw 02

DIP
TOP VIEW

IDT72510 and IDT72520



2669 drw 03

PLCC
TOP VIEW

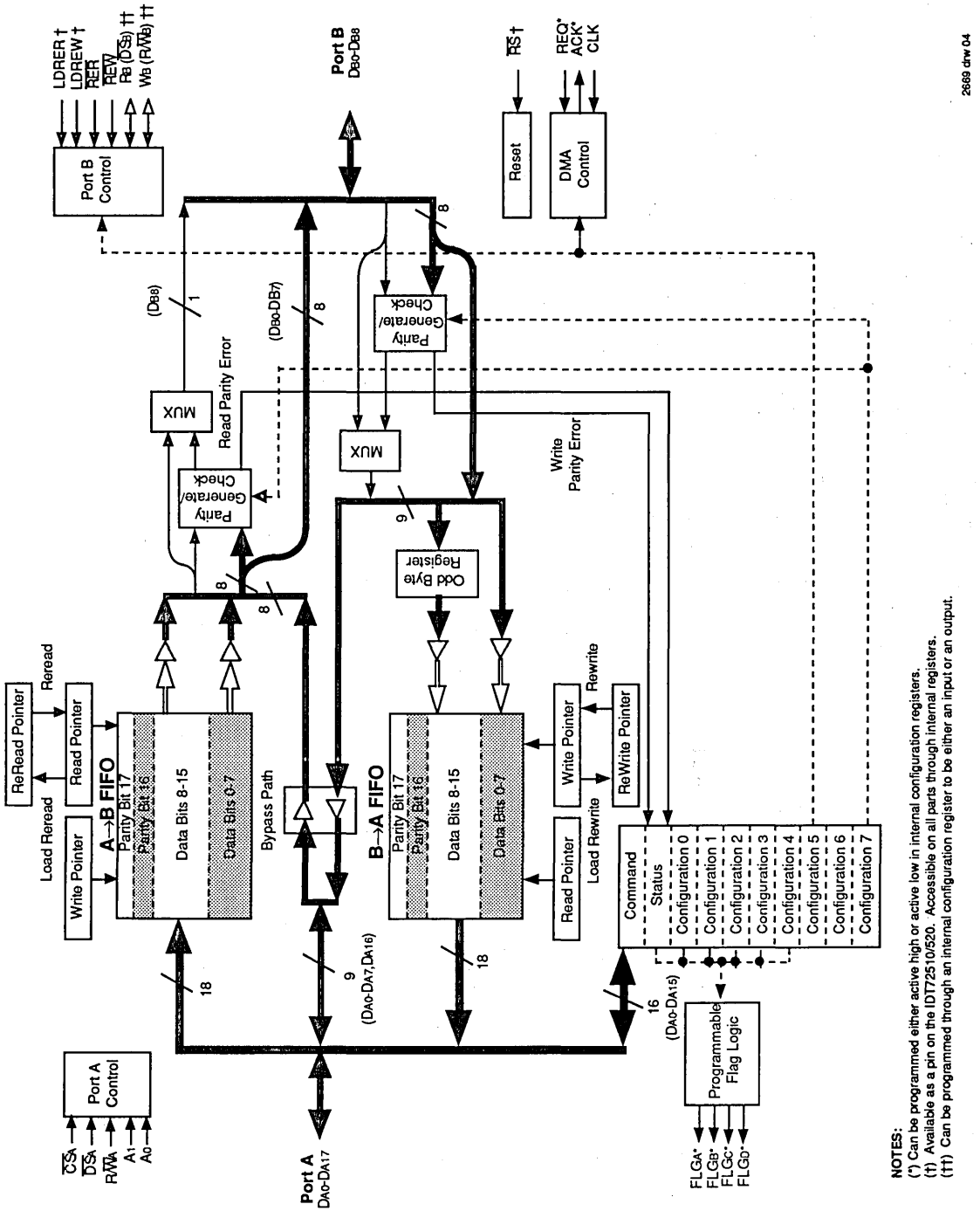
6

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D_{A0}-D_{A15}	Data A	I/O	Data inputs and outputs for 16 bits of the 18-bit Port A bus.
D_{A16}-D_{A17}	Parity A	I/O	D_{A16} is the parity bit for D_{A0}-D_{A7}. D_{A17} is the parity bit for D_{A8}-D_{A15}. D_{A16} and D_{A17} can be used as two extra data bits if the parity generate function is disabled.
$\overline{CS}_A$	Chip Select A	I	Port A is accessed when Chip Select A is LOW.
$\overline{DS}_A$	Data Strobe A	I	Data is written into Port A on the rising edge of Data Strobe when Chip Select is LOW. Data is read out of Port A on the falling edge of Data Strobe when Chip Select is LOW.
R/$\overline{W}_A$	Read/Write A	I	This pin controls the read or write direction of Port A. When $\overline{CS}_A$ is LOW and R/$\overline{W}_A$ is HIGH, data is read from Port A on the falling edge of $\overline{DS}_A$. When $\overline{CS}_A$ is LOW and R/$\overline{W}_A$ is LOW, data is written into Port A on the falling edge of $\overline{DS}_A$.
A_0, A_1	Addresses	I	When Chip Select A is asserted, A_0, A_1, and Read/Write A are used to select one of six internal resources.
D_{B0}-D_{B7}	Data B	I / O	Data inputs & outputs for 8 bits of the 9-bit Port B bus.
D_{B8}	Parity B	I / O	D_{B8} is the parity bit for D_{B0}-D_{B7}. D_{B8} can be used as a data bit if the parity generate function is disabled.
$\overline{R}_B$ ($\overline{DS}_B$)	Read B	I or O	If Port B is programmed to processor mode, this pin functions as an input. If Port B is programmed to peripheral mode this pin functions as an output. This pin can function as part of an Intel-style interface ($\overline{R}_B$) or as part of a Motorola-style interface ($\overline{DS}_B$). As an Intel-style interface, data is read from Port B on a falling edge of $\overline{R}_B$. As a Motorola-style interface, data is read on the falling edge of $\overline{DS}_B$ or written on the rising edge of $\overline{DS}_B$ through Port B. The Default is Intel-style processor mode ($\overline{R}_B$ as an input).
$\overline{W}_B$ (R/$\overline{W}_B$)	Write B	I or O	If Port B is programmed to processor mode, this pin functions as an input. If Port B is programmed to peripheral mode this pin functions as an output. This pin can function as part of an Intel-style interface ($\overline{W}_B$) or as part of a Motorola-style interface (R/$\overline{W}_B$). As an Intel-style interface, data is written to Port B on a rising edge of $\overline{W}_B$. As a Motorola-style interface, data is read (R/$\overline{W}_B$ = HIGH) or written (R/$\overline{W}_B$ = LOW) to Port B in conjunction with a Data Strobe B falling or rising edge. The Default is Intel-style processor mode ($\overline{W}_B$ as an input).
$\overline{RER}$	Reread	I	Loads A→B FIFO Read Pointer with the value of the Reread Pointer when LOW.
$\overline{REW}$	Rewrite	I	Loads B→A FIFO Write Pointer with the value of the Rewrite Pointer when LOW.
LDRER	Load Reread	I	Loads the Reread Pointer with the value of the A→B FIFO Read Pointer when HIGH. This signal is a pin on the IDT72510/520; it is accessible through the Command Register on all four parts.
LDREW	Load Rewrite	I	Loads the Rewrite Pointer with the value of the B→A FIFO Write Pointer when HIGH. This signal is a pin on the IDT72510/520; it is accessible through the Command Register on all four parts.
REQ	Request	I	When Port B is programmed in peripheral mode, asserting this pin begins a data transfer. Request can be programmed either active HIGH or active LOW.
ACK	Acknowledge	O	When Port B is programmed in peripheral mode, Acknowledge is asserted in response to a Request signal. This confirms that a data transfer may begin. Acknowledge can be programmed either active HIGH or active LOW.
CLK	Clock	I	This pin is used to generate timing for ACK, $\overline{R}_B$, $\overline{W}_B$, $\overline{DS}_B$ and R/$\overline{W}_B$ when Port B is in the peripheral mode.
FLG_A-FLG_D	Flags	O	These four outputs pins can be assigned any one of the eight internal flags in the BiFIFO. Each of the two internal FIFOs (A→B and B→A) has four internal flags: Empty, Almost-Empty, Almost-Full, and Full. If parity checking is enabled, the FLG_A pin can also be assigned as a parity error output.
$\overline{RS}$	Reset	I	A LOW on this pin will perform a reset of all BiFIFO functions. Hardware reset pin is only available for IDT72510/72520. Software reset can be achieved through command register for all four devices.
V_{CC}	Power		There are two +5V power pins on all four devices.
GND	Ground		There are three Ground pins at 0V for the IDT7251/52. There are four ground pins for the IDT72510/520.

2669 tbl 01

DETAILED BLOCK DIAGRAM



NOTES:
(*) Can be programmed either active high or active low in internal configuration registers.
(†) Available as a pin on the IDT72510/520. Accessible on all parts through internal registers.
(††) Can be programmed through an internal configuration register to be either an input or an output.

6

FUNCTIONAL DESCRIPTION

IDT's BiFIFO family is versatile for both multiprocessor and peripheral applications. Data can be sent through both FIFO memories concurrently, thus freeing both processors from laborious direct memory access (DMA) protocols and frequent interrupts.

Two full 18-bit wide FIFOs are integrated into the IDT BiFIFO, making simultaneous data exchange possible. Each FIFO is monitored by separate internal read and write pointers, so communication is not only bidirectional, it is also totally independent in each direction. The processor connected to Port A of the BiFIFO can send or receive messages directly to the Port B device using the BiFIFO's 9-bit bypass path.

The BiFIFOs can be used in three different bus configurations: 18 bits to 9 bits, 36 bits to 9 bits and 36 bits to 18 bits. One BiFIFO can be used for the 18- to 9-bit configuration, and two BiFIFOs are required for 36- to 9-bit or 36- to 18-bit configurations. Bits 11 and 12 of Configuration Register 5 determine the BiFIFO configuration (see Table 11 for Configuration Register 5 format).

The microprocessor or microcontroller connected to Port A controls all operations of the BiFIFOs. Thus, all Port A interface pins are inputs driven by the controlling processor. Port B can be programmed to interface either with a second processor or a peripheral device. When Port B is programmed in processor interface mode, the Port B interface pins are inputs driven by the second processor. If a peripheral device is connected to the BiFIFOs, Port B is programmed to peripheral interface mode and the interface pins are outputs.

18- to 9-bit Configurations

A single BiFIFO can be configured to connect an 18-bit processor to another 9-bit processor or a 9-bit peripheral. Bits 11 and 12 of Configuration Register 5 should be set to **00** for a stand-alone configuration. Figures 1 and 2 show the BiFIFO in 18- to 9-bit configurations for processor and peripheral interface modes respectively.

36- to 9-bit Configurations

Two BiFIFOs can be hooked together to create a 36-bit to 9-bit configuration. This means that a 36-bit processor can talk to a 9-bit processor or a 9-bit peripheral. Both BiFIFOs are programmed simultaneously through Port A by placing one command word on the most significant 16 data bits and one command word on the least significant 16 data bits (parity bits should be ignored).

One BiFIFO must be programmed as the master device and the other BiFIFO is the slave device. Bits 11 and 12 of Configuration Register 5 are set to 10 for the slave device and **11** for the master device. The first two 9-bit words on Port B are read from or written to the slave device and the next two 9-bit words go to the master device.

When both BiFIFOs are in peripheral interface mode, the Port B interface pins of the master device are outputs and this BiFIFO controls the bus. The Port B interface pins of the slave device are inputs driven by the master BiFIFO. Two BiFIFOs are connected in Figure 4 to create a 36- to 9-bit peripheral interface.

The two BiFIFOs shown in Figure 3 are configured to connect a 36-bit processor to a 9-bit processor.

36-BIT PROCESSOR to 18-BIT PROCESSOR CONFIGURATION

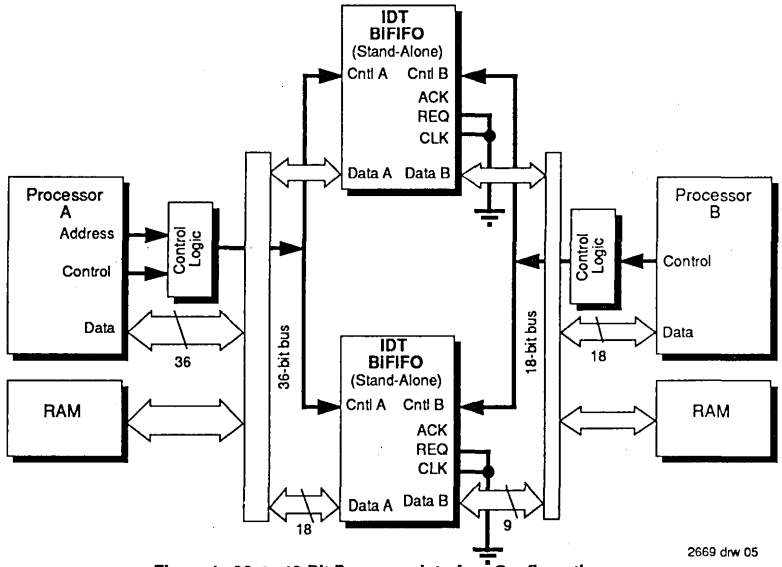


Figure 1. 36- to 18-Bit Processor Interface Configuration

NOTE:

1. Upper BiFIFO only is used in 18- to 9-bit configuration. Note that *Cntl A* refers to $\overline{CS}_A$, A_1, A_0, $R/\overline{W}_A$ and $\overline{DS}_A$; *Cntl B* refers to $R/\overline{W}_B$ and $\overline{DS}_B$ or $\overline{R}_B$ and $\overline{W}_B$.

36-BIT PROCESSOR to 18-BIT PERIPHERAL CONFIGURATION

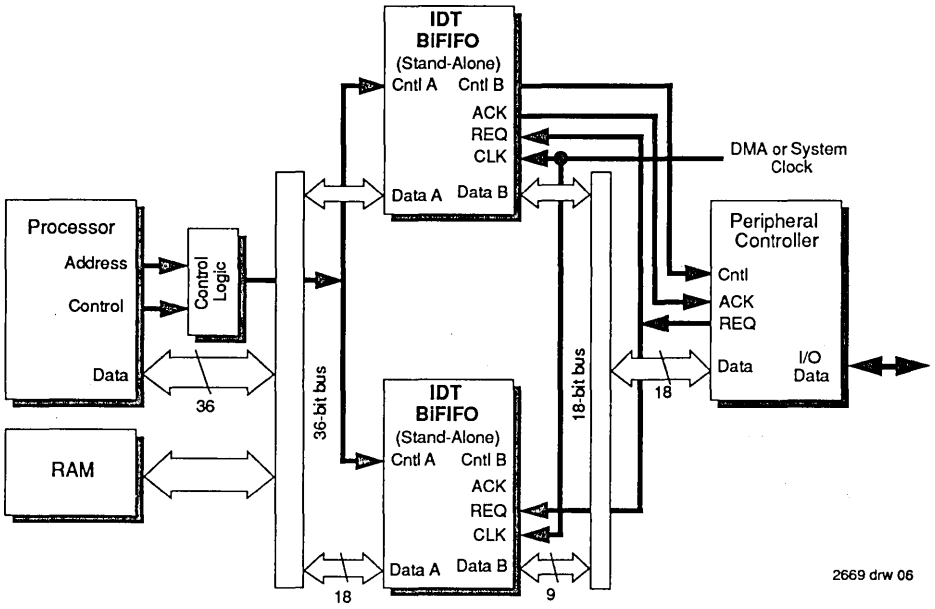


Figure 2. 36- to 18-Bit Peripheral Interface Configuration

NOTE:

1. Upper BiFIFO only is used in 18- to 9-bit configuration. Note that *Cntl A* refers to $\overline{CSA}$, A_1, A_0, R/$\overline{WA}$ and $\overline{DSA}$; *Cntl B* refers to R/$\overline{WB}$ and $\overline{DSB}$ or $\overline{RB}$ and $\overline{WB}$.

36- to 18-bit Configurations

In a 36- to 18-bit configuration, two BiFIFOs operate in parallel. Both BiFIFOs are programmed simultaneously, 16 data bits to each device with the 4 parity bits ignored.

Both BiFIFOs must be programmed into stand-alone mode for a 36-bit processor to communicate with an 18-bit processor or an 18-bit peripheral. This means that bits 11 and 12 of Configuration Register 5 must be set to **00**.

This configuration can be extended to wider bus widths (54- to 27-bits, 72- to 36-bits, ...) by adding more BiFIFOs to the configuration. Figures 1 and 2 show multiple BiFIFOs configured for processor and peripheral interface modes respectively.

Processor Interface Mode

When a microprocessor or microcontroller is connected to Port B, all BiFIFOs in the configuration must be programmed to processor interface mode. In this mode, all Port B interface controls are inputs. Both REQ and CLK pins should be pulled LOW to ensure that the set-up and hold time requirements for these pins are met during reset. Figures 1 and 3 show BiFIFOs in processor interface mode.

Peripheral Interface Mode

If Port B is connected to a peripheral controller, all BiFIFOs in the configuration must be programmed in the peripheral interface mode. To assure fixed high states for $\overline{RB}$ and $\overline{WB}$ before they are programmed into an output, both pins should be pulled-up to Vcc with 10K resistors.

If the BiFIFOs are in stand-alone configuration mode (18-to 9-bit, 36- to 18-bit, ...), then the Port B interface pins are all outputs. Of course, only one set of Port B interface pins should be used to control a single peripheral device, while the other interface pins are all ignored. Figure 2 shows stand-alone configuration BiFIFOs connected to a peripheral.

In a 36- to 9-bit configuration, the master device controls the bus. The Port B interface pins of the master device are outputs and the interface pins of the slave device are inputs. A 36- to 9-bit configuration of two BiFIFOs connected to a peripheral is shown in Figure 4.

Port A Interface

The BiFIFO is straightforward to use in microprocessor-based systems because each BiFIFO port has a standard microprocessor control set. Port A has access to six resources: the A→B FIFO, the B→A FIFO, the 9-bit direct data bus (bypass path), the configuration registers, status and command registers. The Port A Address and Read/Write pins determine the resource being accessed as shown in Table 1. Data Strobe is used to move data in and out of the BiFIFO.

When either of the internal FIFOs are accessed 18 bits of data are transferred across Port A. Since the bypass path is only 9 bits wide, the least significant byte with parity (DA_0-DA_7, DA_{16}) is used on Port A. All of the registers are 16 bits wide which means only the data bits (DA_0-DA_{15}) are passed by Port A.

36-BIT PROCESSOR to 9-BIT PROCESSOR CONFIGURATION

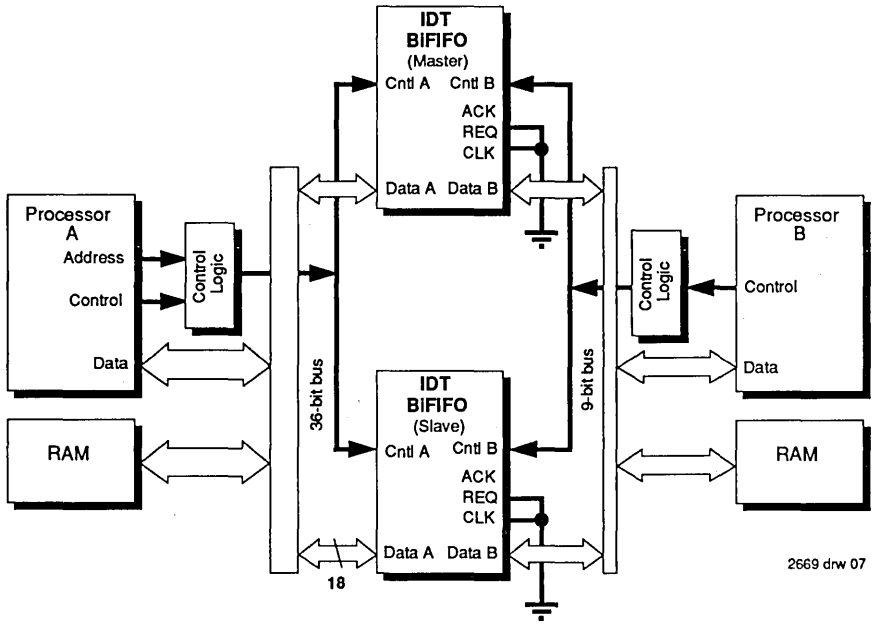


Figure 3. 36- to 9-Bit Processor Interface Configuration

NOTE:
1. *Cntl A* refers to $\overline{CS}_A$, A_1, A_0, $R/\overline{W}_A$ and $\overline{DS}_A$; *Cntl B* refers to $R/\overline{W}_B$ and $\overline{DS}_B$ or $\overline{R}_B$ and $\overline{W}_B$.

36-BIT PROCESSOR to 9-BIT PERIPHERAL CONFIGURATION

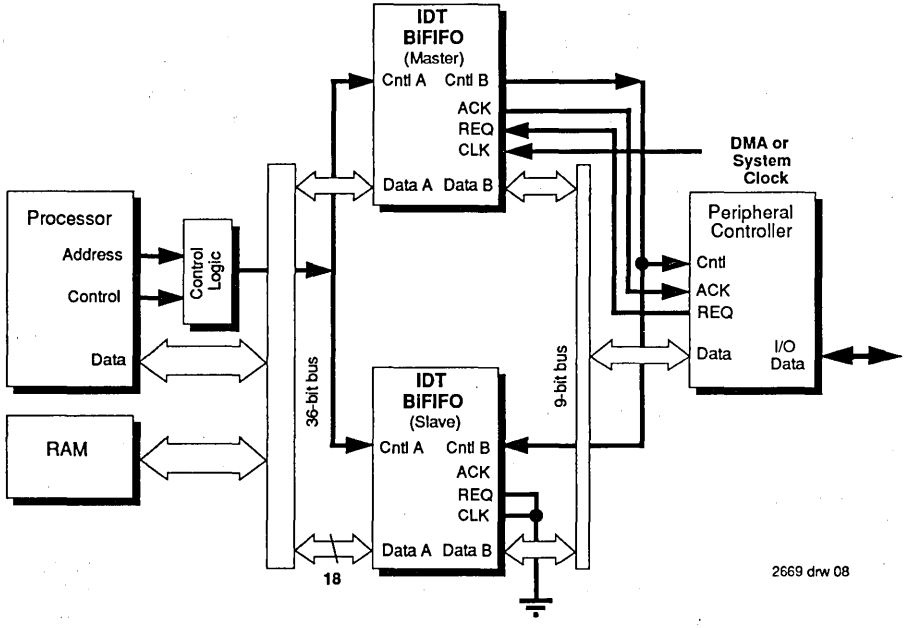


Figure 4. 36- to 9-Bit Peripheral Interface Configuration

NOTE:
1. *Cntl A* refers to $\overline{CS}_A$, A_1, A_0, $R/\overline{W}_A$ and $\overline{DS}_A$; *Cntl B* refers to $R/\overline{W}_B$ and $\overline{DS}_B$ or $\overline{R}_B$ and $\overline{W}_B$.

PORT A RESOURCES

$\overline{CS}_A$	A_1	A_0	Read	Write
0	0	0	B→A FIFO	A→B FIFO
0	0	1	9-bit Bypass Path	9-bit Bypass Path
0	1	0	Configuration Registers	Configuration Registers
0	1	1	Status Register	Command Register
1	X	X	Disabled	Disabled

2669 Tbl 02

Table 1. Accessing Port A Resources Using $\overline{CS}_A$, A_0, and A_1

Bypass Path

The bypass path acts as a bidirectional bus transceiver directly between Port A and Port B. The direct connection requires that the Port A interface pins are inputs and the Port B interface pins are outputs. The bypass path is 9 bits wide in an 18- to 9-bit configuration or in a 36- to 9-bit configuration. Only in the 36- to 18-bit configuration is the bypass path 18 bits wide.

During bypass operations, the BiFIFOs must be programmed into peripheral interface mode. Bit 10 of Configuration Register 5 (see Table 11) is set to 1 for peripheral interface mode. In a 36- to 9-bit configuration, both Port B data buses will be active. Data written into Port A will appear on both master and slave Port B buses concurrently. To avoid Port B bus contention, the data on DA_0-DA_7 and DA_{16} of both BiFIFOs should be exactly the same. Data read from Port A will appear on pins DA_0-DA_7 and DA_{16} of both BiFIFOs within the same 36-bit word.

Command Register

Ten registers are accessible through Port A, a Command Register, a Status Register, and eight Configuration Registers.

The Command Register is written by setting $\overline{CS}_A$ = 0, A_1 = 1, A_0 = 1. Commands written into the BiFIFO have a 4-bit opcode (bit 8 – bit 11) and a 3-bit operand (bit 0 – bit 2) as shown in Figure 5. The commands can be used to reset the BiFIFO, to select the Configuration Register, to perform intelligent reread/rewrite, to set the Port B DMA direction, to set the Status Register format, to modify the Port B Read and Write Pointers, and to clear Port B parity errors. The command opcodes are shown in Table 2.

The reset command initializes different portions of the BiFIFO depending on the command operand. Table 3 shows the reset command operands.

The Configuration Register address is set directly by the command operands shown in Table 4.

Intelligent reread/rewrite is performed by changing the Port B Read Pointer with the Reread Pointer or by changing the Port B Write Pointer with the Rewrite Pointer. No command operands are required to perform a reread/rewrite operation.

When Port B of the BiFIFO is in peripheral mode, the DMA direction is controlled by the Command Register. Table 5 shows the Port B read/write DMA direction operands.

The BiFIFO supports two Status Register formats. Status Register format 1 gives all the internal flag status, while Status Register format 0 provides the data in the Odd Byte Register. Table 6 gives the operands for selecting the appropriate Status Register format. See Table 8 for the details of the two Status Register formats.

Two commands are provided to increment the Port B Read and Write Pointers in case reread/rewrite is performed. Incrementing the pointers guarantees that pointers will be on a word boundary when an odd number of bytes is transmitted through Port B. No operands are required for these commands.

When parity check errors occur on Port B, a clear parity error command is needed to remove the parity error. There are no operands for these commands.

COMMAND OPERATIONS

Command Opcode	Function
0000	Reset BiFIFO (see Table 3)
0001	Select Configuration Register (see Table 4)
0010	Load Reread Pointer with Read Pointer Value
0011	Load Rewrite Pointer with Write Pointer Value
0100	Load Read Pointer with Reread Pointer Value
0101	Load Write Pointer with Rewrite Pointer Value
0110	Set DMA Transfer Direction (see Table 5)
0111	Set Status Register Format (see Table 6)
1000	Increment in byte for A→B FIFO Read Pointer (Port B)
1001	Increment in byte for B→A FIFO Write Pointer (Port B)
1010	Clear Write Parity Error Flag
1011	Clear Read Parity Error Flag

2669 tbl 03

Table 2. Functions Performed by Port A Commands

Reset

The IDT72510 and IDT72520 have a hardware reset pin ($\overline{RS}$) that resets all BiFIFO functions. A hardware reset requires the following four conditions: $\overline{R}_B$ and $\overline{W}_B$ must be HIGH, $\overline{RER}$ and $\overline{REW}$ must be HIGH, LDRER and LDREW must be LOW, and $\overline{DS}_A$ must be HIGH (Figure 9). After a hardware reset, the BiFIFO is in the following state: Configuration Registers 0-3 are 0000H, Configuration Register 4 is set

COMMAND FORMAT

15			12	11	8	7				3	2	0
X	X	X	X	Command Opcode		X	X	X	X	X	Command Operand	

2669 tbl 04

Figure 5. Format for Commands Written into Port A

RESET COMMAND FUNCTIONS

Reset Operands	Function
000	No Operation
001	Reset B→A FIFO (Read, Write, and Rewrite Pointers = 0)
010	Reset A→B FIFO (Read, Write, and Reread Pointers = 0)
011	Reset B→A and A→B FIFO
100	Reset Internal DMA Request Circuitry
101	No Operation
110	No Operation
111	Reset All

2669 tbl 05

Table 3. Reset Command Functions

to **6420H**, and Configuration Registers 5 and 7 are **0000H**. Additionally, Status Register format 0 is selected, all the pointers including the Reread and Rewrite Pointers are set to **0**, the odd byte register valid bit is cleared, the DMA direction is set to B→A write, the internal DMA request circuitry is cleared (set to its initial state), and all parity errors are cleared.

A software reset command can reset A→B pointers and the B→A pointers to **0** independently or together. The request (REQ) DMA circuitry can also be reset independently. A software Reset All command resets all the pointers, the DMA request circuitry, and sets all the Configuration Registers to their default condition. Note that a hardware reset is **NOT** the same as a software Reset All command. Table 7 shows the BiFIFO state after the different hardware and software resets.

SELECT CONFIGURATION REGISTER COMMAND FUNCTIONS

Operands	Function
000	Select Configuration Register 0
001	Select Configuration Register 1
010	Select Configuration Register 2
011	Select Configuration Register 3
100	Select Configuration Register 4
101	Select Configuration Register 5
110	Select Configuration Register 6
111	Select Configuration Register 7

2669 tbl 06

Table 4. Select Configuration Register Command Functions.

DMA DIRECTION COMMAND FUNCTIONS

Operands	Function
XX0	Write B→A FIFO
XX1	Read A→B FIFO

2669 tbl 07

Table 5. Set DMA Direction Command Functions. Command Only Operates in Peripheral Interface Mode

STATUS REGISTER FORMAT COMMAND FUNCTIONS

Operands	Function
XX0	Status Register Format 0
XX1	Status Register Format 1

2669 tbl 08

Table 6. Command Functions to Set the Status Register Format

STATE AFTER RESET

	Hardware Reset	Software Reset				
	($\overline{RS}$ asserted, IDT72510 & IDT72520 only)	B→A (001)	A→B (010)	B→A and A→B (011)	Internal Request (100)	All (111)
Configuration Registers 0-3	0000H	—	—	—	—	0000H
Configuration Register 4	6420H	—	—	—	—	6420H
Configuration Register 5	0000H	—	—	—	—	0000H
Configuration Register 7	0000H	—	—	—	—	0000H
Status Register format	0	—	—	—	—	—
B→A Read, Write, Rewrite Pointers	0	0	—	0	—	0
A→B Read, Write, Reread Pointers	0	—	0	0	—	0
Odd byte register valid bit	clear	clear	—	clear	—	clear
DMA direction	B→A write	—	—	—	—	—
DMA internal request	clear	—	—	—	clear	clear
Parity errors	clear	—	—	—	—	—

2669 tbl 09

Table 7. The BIFIFO State After a Reset Command

Status Register

The Status Register reports the state of the programmable flags, the DMA read/write direction, the Odd Byte Register valid bit, and parity errors. The Status Register is read by setting $\overline{CS}_A$ = 0, A_1 = 1, A_0 = 1 (see Table 1).

There are two Status Register formats that are set by a Status Register format command. Format **0** stores the Odd Byte Register data in the lower eight bits of the Status Register, while format **1** reports the flag states and the DMA read/write direction in the lower eight bits. The upper eight bits are identical for both formats. The flag states, the parity errors, the Odd Byte Register valid bit, and the Status Register format are all in the upper eight bits of the Status Register. See Table 8 for both Status Register formats.

Configuration Registers

The eight Configuration Register formats are shown in Table 9. Configuration Registers 0-3 contain the programmable flag offsets for the Almost Empty and Almost Full flags. These offsets are set to **0** when a hardware reset or a software reset all is applied. Note that Table 9 shows that Configuration Registers 0-3 are 10 bits wide to accommodate the 1024 locations in each FIFO memory of the IDT7252/520. Only 9 least significant bits are used for the 512 locations of the IDT7251/510; the most significant bit, bit 9, must be set to **0**.

Configuration Register 4 is used to assign the internal flags to the external flag pins (FLGA-FLGD). Each external flag pin is assigned an internal flag based on the four bit codes shown in Table 10. The default condition for Configuration Register 4 is **6420H** as shown in Table 7. The default flag assignments are: FLG_D is assigned B→A $\overline{Full}$, FLG_C is assigned B→A $\overline{Empty}$, FLG_B is assigned A→B $\overline{Full}$, FLG_A is assigned A→B $\overline{Empty}$.

Configuration Register 5 is a general control register. The format of Configuration Register 5 is shown in Table 11. Bit 0 sets the Intel-style interface ($\overline{R}_B$, $\overline{W}_B$) or Motorola-style interface ($\overline{DS}_B$, R/$\overline{W}_B$) for Port B. Bit 1 changes the byte order for data coming through Port B. Bits 2 and 3 redefine Full and Empty Flags for reread/rewrite data protection.

Bits 4-9 control the DMA interface and are only applicable in peripheral interface mode. In processor interface mode, these bits are don't care states. Bits 4 and 5 set the polarity of the DMA control pins REQ and ACK, respectively. An internal clock controls all DMA operations. This internal clock is derived from the external clock (CLK). Bit 9 determines the internal clock frequency: the internal clock = CLK or the internal clock = CLK divided by 2. Bit 8 sets whether $\overline{R}_B$, $\overline{W}_B$, and $\overline{DS}_B$ are asserted for either one or two internal clocks. Bits 6 and 7 set the number of internal clocks between REQ assertion and ACK assertion. The timing can be from 2 to 5 cycles as shown in Figure 17.

Bit 10 controls Port B processor or peripheral interface mode. In processor mode, the Port B control pins ($\overline{R}_B$, $\overline{W}_B$, $\overline{DS}_B$, R/$\overline{W}_B$) are inputs and the DMA controls are ignored. In peripheral mode, the Port B control pins are outputs and the DMA controls are active.

Bits 11 and 12 set the width expansion mode. For 18- to 9-bit configurations or 36- to 18-bit configurations, the BiFIFO should be set in stand-alone mode. For a 36- to 9-bit configuration, one BiFIFO must be in slave mode and the other BiFIFO must be in master mode. The master BiFIFO allows the first two bytes transferred across Port B to go to the slave BiFIFO, then the next two bytes go to the master BiFIFO.

Configuration Register 7 controls the parity functions of Port B as shown in Table 12. Either parity generation or parity

STATUS REGISTER FORMAT 0

Bit	Signal
0	Odd Byte Register
1	
2	
3	
4	
5	
6	
7	
8	Valid Bit
9	Write Parity Error
10	Read Parity Error
11	Status Register Format = 0
12	A→B Full Flag
13	A→B Almost-Full Flag
14	B→A Empty Flag
15	B→A Almost-Empty Flag

2669 tbl 10

STATUS REGISTER FORMAT 1

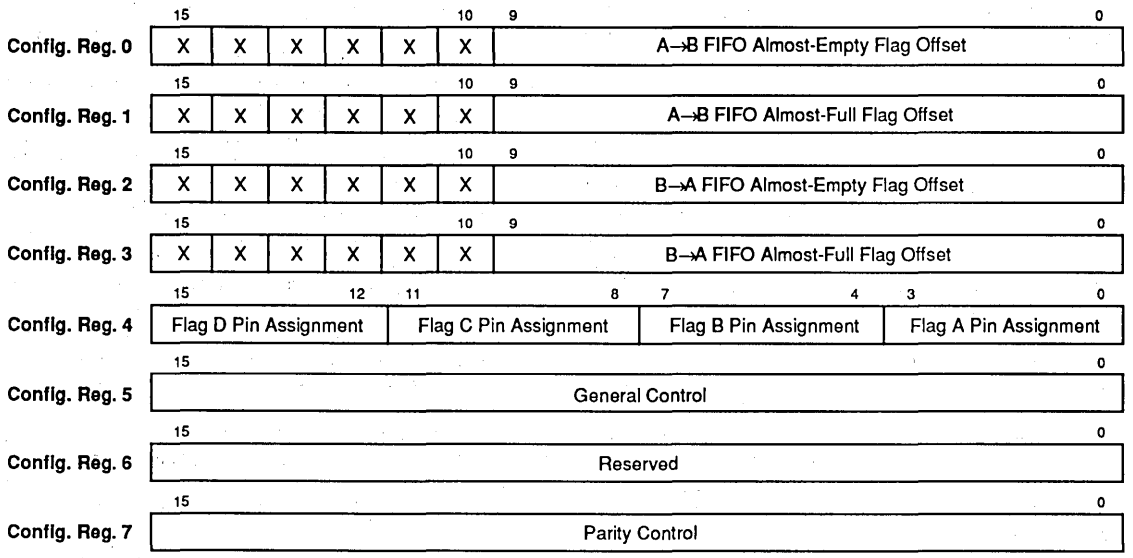
Bit	Signal
0	Reserved
1	Reserved
2	Reserved
3	DMA Direction
4	A→B Empty Flag
5	A→B Almost-Empty Flag
6	B→A Full Flag
7	B→A Almost-Full Flag
8	Valid Bit
9	Write Parity Error
10	Read Parity Error
11	Status Register Format = 1
12	A→B Full Flag
13	A→B Almost-Full Flag
14	B→A Empty Flag
15	B→A Almost-Empty Flag

2669 tbl 11

Table 8. The Two Status Register Formats

6

CONFIGURATION REGISTER FORMATS



NOTE:

1. Bit 9 of Configuration Registers 0-3 must be set to 0 on the IDT7251 and IDT72510.

2669 tbl 12

Table 9. The BIFIFO Configuration Register Formats

checking is enabled for data read and written through Port B. Bit 8 controls parity checking and generation for B→A write data. Bit 9 controls parity checking and generation for A→B read data. Bit 10 controls whether the parity is odd or even. Bit 11 is used to assign the internal parity checking error to the FLGA pin. When the parity error is assigned to FLGA, the Configuration Register 4 flag assignment for FLGA is ignored.

Programmable Flags

The IDT BiFIFO has eight internal flags; four of these flags have programmable offsets, the other four are empty or full. Associated with each FIFO memory array are four internal flags, Empty, Almost-Empty, Almost-Full and Full, for the total of eight internal flags. The Almost-Empty and Almost-Full offsets can be set to any depth through the Configuration Registers 0-3 (see Table 9). The offset (or depth) of FIFO RAM array is based on the unit of an 18-bit word. The flags are asserted at the depths shown in Table 13. After a hardware reset or a software reset all, the almost flag offsets are set to **0**. Even though the offsets are equivalent, the Empty and Almost-Empty flags have different timing which means that the flags are not coincident. Similarly, the Full and Almost-Full flags are not coincident because of timing.

These eight internal flags can be assigned to any of four external flag pins (FLGA-FLGD) through Configuration Register 4 (see Table 10). For the specific flag timings, see Figures 20-23.

The current state of all eight flags is available in the Status Register in Status Register format 1. In Status Register format 0, only four flags can be found in the Status Register (see Table 8).

EXTERNAL FLAG ASSIGNMENT CODES

Assignment Code	Internal Flag Assigned to Flag Pin
0000	A→B $\overline{\text{Empty}}$
0001	A→B $\overline{\text{Almost-Empty}}$
0010	A→B $\overline{\text{Full}}$
0011	A→B $\overline{\text{Almost-Full}}$
0100	B→A $\overline{\text{Empty}}$
0101	B→A $\overline{\text{Almost-Empty}}$
0110	B→A $\overline{\text{Full}}$
0111	B→A $\overline{\text{Almost-Full}}$
1000	A→B Empty
1001	A→B Almost-Empty
1010	A→B Full
1011	A→B Almost-Full
1100	B→A Empty
1101	B→A Almost-Empty
1110	B→A Full
1111	B→A Almost-Full

2669 tbl 13

Table 10. Configuration Register 4 Internal Flag Assignments to External Flag Pins.

Port B Interface

Port B also has parity, reread/rewrite and DMA functions. Port B can be configured to interface to either Intel-style ($\overline{R}_B$, $\overline{W}_B$) or Motorola-style ($\overline{DS}_B$, R/$\overline{W}_B$) devices in Configuration Register 5 (see Table 11). Port B can also be configured to talk to a processor or a peripheral device through Configuration Register 5. In processor interface mode, the Port B interface controls are inputs. In peripheral interface mode, the Port B interface controls are outputs. After a hardware reset or a software Reset All command, Port B defaults to an Intel-style processor interface; the controls are inputs.

Two 9-bit words are put together to create each 18-bit word stored in the internal FIFOs. The first 9-bit word written to Port B goes into the Odd Byte Register shown in the detailed block diagram. The Odd Byte Register valid bit (Bit 8) in the Status Register is 1 when this first 9-bit word is written. The data bits from Port B (DB_0-DB_7) are also stored in the lower 8 bits of the Status Register when Status Register format 0 is selected (see Table 8). The second write on Port B moves the 9-bits from Port B and the 9-bits in the Odd Byte Register into the B→A FIFO and advances the B→A Write Pointer. The Status Register valid bit is set to 0 after the second write.

When Port B reads data from the A→B FIFO, two buffers choose which 9 of the 18 memory bits are sent to Port B. These buffers alternate between the upper 9 bits (DA_8-DA_{15}, DA_{17}) and the lower 9 bits (DA_0-DA_7, DA_{16}). The A→B Read

CONFIGURATION REGISTER 5 FORMAT

Bit	Function		
0	Select Port B Interface $\overline{R}_B$ & $\overline{W}_B$ or $\overline{DS}_B$ & R/$\overline{W}_B$	0	Pins are $\overline{R}_B$ and $\overline{W}_B$ (Intel-style interface)
		1	Pins are $\overline{DS}_B$ and R/$\overline{W}_B$ (Motorola-style interface)
1	Byte Order of 18-bit Word	0	Lower byte DA_7-DA_0 and parity DA_{16} are read or written first on Port B
		1	Upper byte DA_{15}-DA_8 and parity DA_{17} are read or written first on Port B
2	Full Flag Definition	0	Full Flag is asserted when write pointer meets read pointer
		1	Full Flag is asserted when write pointer meets reread pointer
3	Empty Flag Definition	0	Empty Flag is asserted when read pointer meets write pointer
		1	Empty Flag is asserted when read pointer meets rewrite pointer
4	REQ Pin Polarity	0	REQ pin active HIGH
		1	REQ pin active LOW
5	ACK Pin Polarity	0	ACK pin active LOW
		1	ACK pin active HIGH
7-6	REQ / ACK Timing	00	2 internal clocks between REQ assertion and ACK assertion
		01	3 internal clocks between REQ assertion and ACK assertion
		10	4 internal clocks between REQ assertion and ACK assertion
		11	5 internal clocks between REQ assertion and ACK assertion
8	Port B Read and Write Timing Control for Peripheral Mode	0	$\overline{R}_B$, $\overline{W}_B$, and $\overline{DS}_B$ are asserted for 1 internal clock
		1	$\overline{R}_B$, $\overline{W}_B$, and $\overline{DS}_B$ are asserted for 2 internal clocks
9	Internal Clock Frequency Control	0	internal clock = CLK
		1	internal clock = CLK divided by 2
10	Port B Interface Mode Control	0	Processor interface mode (Port B controls are inputs)
		1	Peripheral interface mode (Port B controls are outputs)
12-11	Width Expansion Mode Control	00	Stand-alone mode (18- to 9-bits, 36- to 18-bits)
		01	Reserved
		10	Slave width expansion mode (36- to 9-bits)
		11	Master width expansion mode (36- to 9-bits)
13	Unused		
14	Unused		
15	Unused		

2669 tbl 14

Table 11. BiFIFO Configuration Register 5 Format

CONFIGURATION REGISTER 7 FORMAT

BIT	FUNCTION		
0-7	Unused		
8	Parity Input Control B→A	0	Disable Parity Generate, Enable Parity Check
		1	Enable Parity Generate, Disable Parity Check
9	Parity Output Control A→B	0	Disable Parity Generate, Enable Parity Check
		1	Enable Parity Generate, Disable Parity Check
10	Parity Odd/Even Control	0	Odd
		1	Even
11	Assign Parity Error to Flag A Pin	0	No Parity Error Output
		1	Parity Error on Flag A Pin
12-15	Unused		

2669 tbl 15

Table 12. BiFIFO Configuration Register 7 Format

Pointer is advanced after every two Port B reads.

The BiFIFO can be set to order the 9-bit data so the first 9-bits go to the LSB (D_{A0}-D_{A7}, D_{A16}) or the MSB (D_{A8}-D_{A15}, D_{A17}) of Port A. This data ordering is controlled by bit 1 of Configuration Register 5 (see Table 11).

DMA Control Interface

The BiFIFO has DMA control to simplify data transfers with peripherals. For the BiFIFO DMA controls (REQ, ACK and CLK) to operate, the BiFIFO must be in peripheral interface mode (Configuration Register 5, Table 11).

DMA timing is controlled by the external clock input, CLK. An internal clock is derived from this CLK signal to generate the $\overline{R}_B$, $\overline{W}_B$, $\overline{DS}_B$ and R/$\overline{W}_B$ output signals. The internal clock also determines the timing between REQ assertion and ACK assertion. Bit 9 of Configuration Register 5 determines whether the internal clock is the same as CLK or whether the internal clock is CLK divided by 2.

Bit 8 of Configuration Register 5 sets whether $\overline{R}_B$, $\overline{W}_B$ and $\overline{DS}_B$ are asserted for 1 or 2 internal clocks. Bits 6 and 7 of Configuration Register 5 set the number of clocks between REQ assertion and ACK assertion. The clocks between REQ assertion and ACK assertion can be 2, 3, 4 or 5.

Bits 4 and 5 of Configuration Register 5 set the polarity of the REQ and ACK pins, respectively.

A DMA transfer command sets the Port B read/write direction (see Table 5). The timing diagram for DMA transfers is shown in Figure 17. The basic DMA transfer starts with REQ assertion. After 2 to 5 internal clocks, ACK is asserted by the BiFIFO. ACK will not be asserted if a read is attempted on an Empty A→B FIFO or if a write is attempted on a Full B→A FIFO. If the BiFIFO is in Motorola-style interface mode, R/$\overline{W}_B$ is set at the same time that ACK is asserted. One internal clock later, $\overline{DS}_B$ is asserted. If the BiFIFO is in Intel-style interface mode, either $\overline{R}_B$ or $\overline{W}_B$ is asserted one internal clock after ACK assertion. These read/write controls stay asserted for 1 or 2 internal clocks, then ACK, $\overline{DS}_B$, $\overline{R}_B$ and $\overline{W}_B$ are made inactive. This completes the transfer of one 9-bit word.

On the next rising edge of CLK, REQ is sampled. If REQ is still asserted, another DMA transfer starts with the assertion of ACK. Data transfers will continue as long as REQ is asserted.

Parity Checking and Generation

Parity generation or checking is performed by the BiFIFO on data passing through Port B. Parity can either be odd or even as determined by Bit 10 of Configuration Register 7.

When parity checking is enabled, D_{B8} is treated as a data bit. D_{B8} data will be passed to D_{A16} (bypass operation) or stored in the RAM array (FIFO operation) for B->A operation;

INTERNAL FLAG TRUTH TABLE

Number of Words in FIFO					
From	To	Empty Flag	Almost-Empty Flag	Almost-Full Flag	Full Flag
0	0	Asserted	Asserted	Not Asserted	Not Asserted
1	n	Not Asserted	Asserted	Not Asserted	Not Asserted
n + 1	D - (m + 1)	Not Asserted	Not Asserted	Not Asserted	Not Asserted
D - m	D - 1	Not Asserted	Not Asserted	Asserted	Not Asserted
D	D	Not Asserted	Not Asserted	Asserted	Asserted

NOTE:

2669 tbl 16

1. BiFIFO flags can be assigned to external flag pins to be observed. D = FIFO depth (IDT7251/510 = 512, IDT7252/520 = 1024), n = Almost-Empty flag offset, m = Almost-Full flag offset.

Table 13. Internal Flag Truth Table.

similarly, DA16 or parity bits from the RAM array will be passed to DB8 for A->B operations. A->B read parity errors and B->A write parity errors are shown in Bit 9 and 10 in the Status Register. If an external parity error signal is required, a logical OR of the two parity error bits is brought out to FLGA pin by setting Bit 11 of Configuration Register 7.

Parity generation creates the ninth bit. This ninth bit is placed on DB8 for A->B read operation, and on DA16 or RAM array for B->A write operation.

It is recommended that if the parity pins (DB8, DA16, and DA17) are not used, they should be pulled down with 10K resistors for noise immunity.

Intelligent Reread/Rewrite

Intelligent reread/rewrite is a method the BiFIFO uses to help assure data integrity. Port B of the BiFIFO has two extra pointers, the Reread Pointer and the Rewrite Pointer. The Reread Pointer is associated with the A->B FIFO Read Pointer, while the Rewrite Pointer is associated with the B->A FIFO Write Pointer. The Reread Pointer holds the start address of a data block in the A->B FIFO RAM, and the Read Pointer is the current address of the same FIFO RAM array. By loading the Read Pointer with the value held in the Reread Pointer (RER asserted), reads will start over at the beginning of the data block. In order to mark the beginning of a data block, the Reread Pointer should be loaded with the Read Pointer value (LDRER asserted) before the first read is performed on this data block. Figure 6 shows a Reread operation.

Similarly, the Rewrite Pointer holds the start address of a data block in the B->A FIFO RAM, while the Write Pointer is the current address within the RAM array. The operation of the REW and LDREW is identical to the RER and LDRER discussed above. Figure 7 shows a Rewrite operation.

For the reread data protection, Bit 2 of Configuration Register 5 can be set to 1 to prevent the data block form being overwritten. In this way, the assertion of A->B full flag will occur when the write pointer meets the reread pointer instead of the read pointer as in the normal definition. For the rewrite data protection, Bit 3 of Configuration Register 5 can be set to 1 to prevent the data block from being read. In this case, the assertion of B->A empty flag will occur when the read pointer meets the rewrite pointer instead of the write pointer.

In conclusion, Bit 2 and 3 of Configuration Register 5 are used to redefine Full & Empty flags for data block partition. Although it can serve the purpose of data protection, the setting of these 2 bits is independent of the functions caused by RER/REW, or LDRER/LDREW assertions.

REREAD OPERATIONS

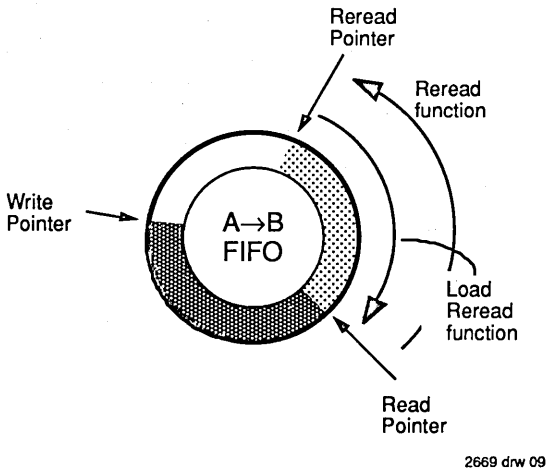


Figure 6. BIFIFO Reread Operations

REWRITE OPERATIONS

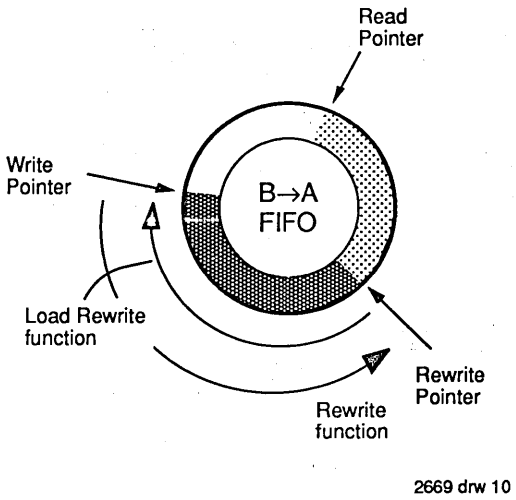


Figure 7. BIFIFO Rewrite Operations

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage With Respect To Ground	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2669 tbl 17

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input HIGH Voltage Commercial	2.0	—	—	V
V_{IH}	Input HIGH Voltage Military	2.2	—	—	V
V_{IL}(1)	Input LOW Voltage Commercial and Military	—	—	0.8	V

NOTE: 2669 tbl 18

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	IDT7251L IDT7252L IDT72510L IDT72520L Commercial t_A = 35, 50, 80ns			IDT7251L IDT7252L IDT72510L IDT72520L Military t_A = 40, 50, 80ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{IL}(1)	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	µA
I_{OL}(2)	Output Leakage Current	-10	—	10	-10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = -1mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4mA	—	—	0.4	—	—	0.4	V
I_{CC1}(3)	Average Vcc Power Supply Current	—	150	220	—	180	250	mA
I_{CC2}(3)	Average Standby Current ($\overline{FB}$ = $\overline{WB}$ = $\overline{DS_A}$ = V_{IH})	—	8	12	—	12	25	mA
I_{CC3}(3)	Power Down Current (All Inputs = V_{CC} - 0.2V)	—	—	2	—	—	4	mA

NOTES: 2669 tbl 19

1. Measurements with 0.4V ≤ V_{IN} ≤ V_{CC}, $\overline{DS_A}$ = $\overline{DS_B}$ ≥ V_{IH}. 2. Measurements with 0.4V ≤ V_{OUT} ≤ V_{CC}, $\overline{DS_A}$ = $\overline{DS_B}$ ≥ V_{IH}. 3. Icc measurements are made with outputs open.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 8

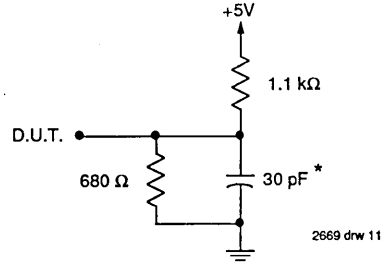
2669 tbl 20

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN} (2)	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT} (1,2)	Output Capacitance	V_{OUT} = 0V	12	pF

NOTES: 2669 tbl 21

1. With output deselected.
2. Characterized values, not currently tested.



or Equivalent Circuit

Figure 8. Output Load

* Includes jig and scope capacitances

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V±10%, T_A = -55°C to +125°C)

		Commercial		Military		Commercial and Military					
		IDT7251L35 IDT7252L35 IDT72510L35 IDT72520L35		IDT7251L40 IDT7252L40 IDT72510L40 IDT72520L40		IDT7251L50 IDT7252L50 IDT72510L50 IDT72520L50		IDT7251L80 IDT7252L80 IDT72510L80 IDT72520L80			Timing
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Figure
RESET TIMING (Port A and Port B)											
t_{RSC}	Reset cycle time	45	—	50	—	65	—	100	—	ns	9
t_{RS}	Reset pulse width	35	—	40	—	50	—	80	—	ns	9
t_{RSS}	Reset set-up time	35	—	40	—	50	—	80	—	ns	9
t_{RSR}	Reset recovery time	10	—	10	—	15	—	20	—	ns	9
t_{RSF}	Flag reset pulse width	—	45	—	50	—	65	—	100	ns	9
PORT A TIMING											
t_{AA}	Port A access time	—	35	—	40	—	50	—	80	ns	12, 14, 15
t_{ALZ}	Read or write pulse LOW to data bus at low Z	5	—	5	—	5	—	10	—	ns	12, 15, 16
t_{AHZ}	Read or write pulse HIGH to data bus at high Z	—	20	—	25	—	30	—	30	ns	12, 14, 15, 16
t_{ADV}	Data valid from read pulse HIGH	5	—	5	—	5	—	5	—	ns	12, 14, 16
t_{ARC}	Read cycle time	45	—	50	—	65	—	100	—	ns	12
t_{ARPW}	Read pulse width	35	—	40	—	50	—	80	—	ns	12, 14, 15
t_{ARR}	Read recovery time	10	—	10	—	15	—	20	—	ns	12
t_{AS}	$\overline{CS}_A$, A_0, A_1, R/$\overline{W}_A$ set-up time	5	—	5	—	5	—	10	—	ns	10, 12, 16
t_{AH}	$\overline{CS}_A$, A_0, A_1, R/$\overline{W}_A$ hold time	5	—	5	—	5	—	10	—	ns	10, 12
t_{ADS}	Data set-up time	18	—	20	—	30	—	40	—	ns	11, 12, 14, 15
t_{ADH}(1)	Data hold time	0	—	0	—	5	—	10	—	ns	11, 12, 14, 15
t_{AWC}	Write cycle time	45	—	50	—	65	—	100	—	ns	12
t_{AWPW}	Write pulse width	35	—	40	—	50	—	80	—	ns	11, 12, 14
t_{AWR}	Write recovery time	10	—	10	—	15	—	20	—	ns	12
t_{AWRCOM}	Write recovery time after a command	35	—	40	—	50	—	80	—	ns	11

NOTE:

1. The minimum data hold time is 5ns (10ns for the 80ns speed grade) when writing to the Command, Status or Configuration registers.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V±10%, T_A = -55°C to +125°C)

		Commercial		Military		Commercial and Military					
		IDT7251L35 IDT7252L35 IDT72510L35 IDT72520L35		IDT7251L40 IDT7252L40 IDT72510L40 IDT72520L40		IDT7251L50 IDT7252L50 IDT72510L50 IDT72520L50		IDT7251L80 IDT7252L80 IDT72510L80 IDT72520L80			Timing
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Figure
PORT B PROCESSOR INTERFACE TIMING											
t_{BA1}	Port B access time with no parity	—	35	—	40	—	50	—	80	ns	13, 14, 15
t_{BA2}	Port B access time with parity	—	42	—	48	—	60	—	90	ns	13, 14, 15
t_{BLZ}	Read or write pulse LOW to data bus at low Z	5	—	5	—	5	—	10	—	ns	13, 14, 15
t_{BHZ}	Read or write pulse HIGH to data bus at high Z	—	20	—	25	—	30	—	30	ns	13, 14, 15
t_{BDV}	Data valid from read pulse HIGH	5	—	5	—	5	—	10	—	ns	13, 14, 15, 16
t_{BRC}	Read cycle time	45	—	50	—	65	—	100	—	ns	13
t_{BRPW}	Read pulse width	35	—	40	—	50	—	80	—	ns	13
t_{BRR}	Read recovery time	10	—	10	—	15	—	20	—	ns	13
t_{BS}	$R/\overline{W}_B$ set-up time	5	—	5	—	5	—	10	—	ns	13
t_{BH}	$R/\overline{W}_B$ hold time	5	—	5	—	5	—	10	—	ns	13
t_{BDS1}	Data set-up time with no parity	18	—	20	—	30	—	40	—	ns	13, 14, 15
t_{BDH1}	Data hold time with no parity	0	—	0	—	5	—	10	—	ns	13, 14, 15
t_{BDS2}	Data set-up time with parity	22	—	25	—	35	—	45	—	ns	13, 14, 15
t_{BDH2}	Data hold time with parity	0	—	0	—	5	—	10	—	ns	13, 14, 15
t_{BWC}	Write cycle time	45	—	50	—	65	—	100	—	ns	13
t_{BWPW}	Write pulse width	35	—	40	—	50	—	80	—	ns	13, 15
t_{BWR}	Write recovery time	10	—	10	—	15	—	20	—	ns	13
PORT B PERIPHERAL INTERFACE TIMING											
t_{BCKC}	Clock cycle time	20	—	20	—	25	—	40	—	ns	17
t_{BCKH}	Clock pulse HIGH time	6	—	8	—	10	—	16	—	ns	17
t_{BCKL}	Clock pulse LOW time	6	—	8	—	10	—	16	—	ns	17
t_{BREQS}	Request set-up time	5	—	5	—	10	—	10	—	ns	17
t_{BREQH}	Request hold time	5	—	5	—	5	—	5	—	ns	17
t_{BACKL}	Delay from a rising clock edge to ACK switching	—	18	—	20	—	25	—	35	ns	17

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V±10%, T_A = -55°C to +125°C)

		Commercial		Military		Commercial and Military					
		IDT7251L35 IDT7252L35 IDT72510L35 IDT72520L35		IDT7251L40 IDT7252L40 IDT72510L40 IDT72520L40		IDT7251L50 IDT7252L50 IDT72510L50 IDT72520L50		IDT7251L80 IDT7252L80 IDT72510L80 IDT72520L80			Timing
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Figure
PORT B RETRANSMIT and PARITY TIMING											
t_{BDSBH}	$\overline{RER}$, $\overline{REW}$, LDRER, LDREW set-up and recovery time	10	—	10	—	15	—	15	—	ns	9, 18
t_{BPER}	Parity error time	25	—	25	—	30	—	30	—	ns	19
BYPASS TIMING											
t_{BYA}	Bypass access time	—	20	—	25	—	30	—	40	ns	16
t_{BYD}	Bypass delay	—	15	—	17	—	20	—	30	ns	16
t_{BYDV}	Bypass data valid time	20	—	20	—	20	—	20	—	ns	16
FLAG TIMING											
t_{REF}	Read clock edge to Empty Flag asserted	—	35	—	35	—	45	—	60	ns	14, 15, 20, 22
t_{WEF}	Write clock edge to Empty Flag not asserted	—	35	—	35	—	45	—	60	ns	14, 15, 20, 22
t_{RFF}	Read clock edge to Full Flag not asserted	—	35	—	35	—	45	—	60	ns	14, 15, 21, 23
t_{WFF}	Write clock edge to Full Flag asserted	—	35	—	35	—	45	—	60	ns	14, 15, 21, 23
t_{RAEF}	Read clock edge to Almost-Empty Flag asserted	—	50	—	50	—	60	—	75	ns	20, 22
t_{WAEF}	Write clock edge to Almost-Empty Flag not asserted	—	50	—	50	—	60	—	75	ns	20, 22
t_{RAFF}	Read clock edge to Almost-Full Flag not asserted	—	50	—	50	—	60	—	75	ns	21, 23
t_{WAFF}	Write clock edge to Almost-Full Flag asserted	—	50	—	50	—	60	—	75	ns	21, 23

NOTES:
1. Read and Write are internal signals derived from $\overline{DS}_A$, $R/\overline{W}_A$, $\overline{DS}_B$, $R/\overline{W}_B$, $\overline{R}_B$, and $\overline{W}_B$.
2. Although the flags, Empty, Almost-Empty, Almost-Full, and Full Flags are internal flags, the timing given is for those assigned to external pins.

6

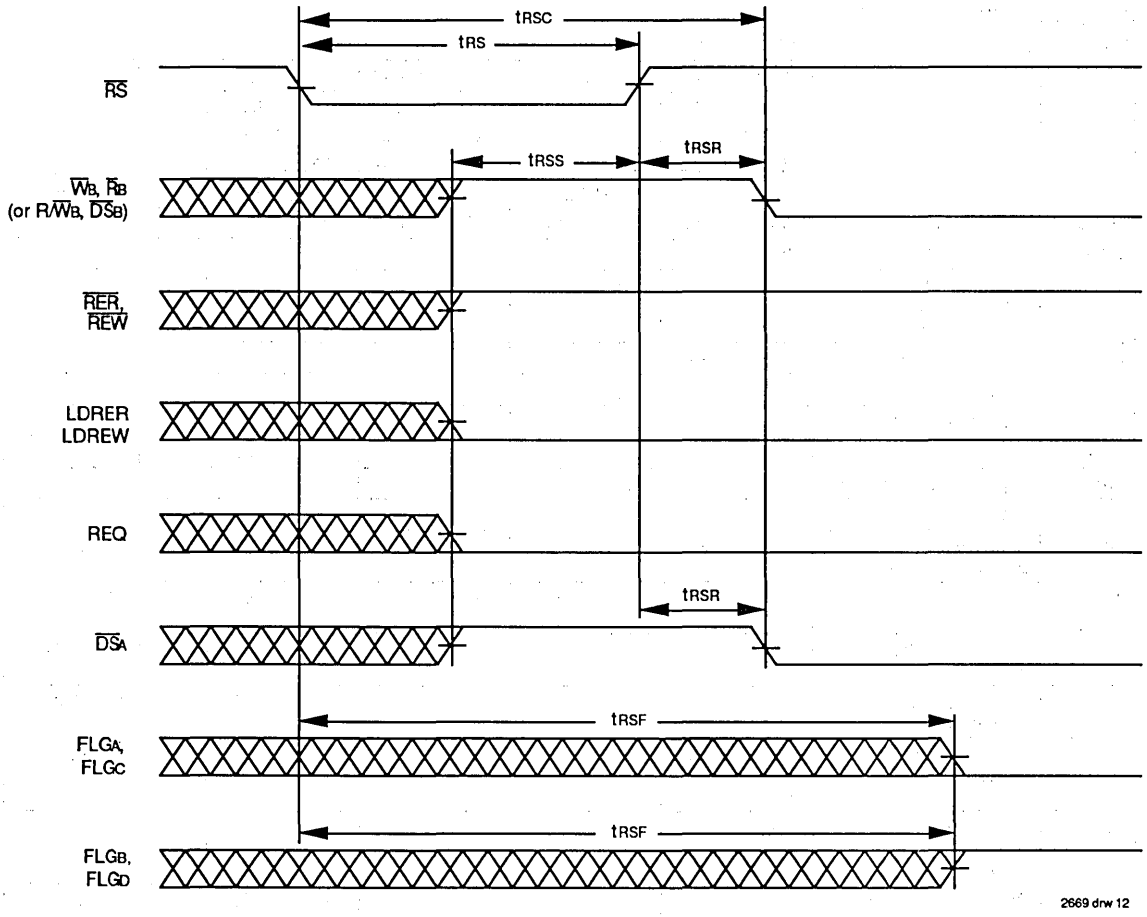


Figure 9. Hardware Reset Timing for IDT72510/520

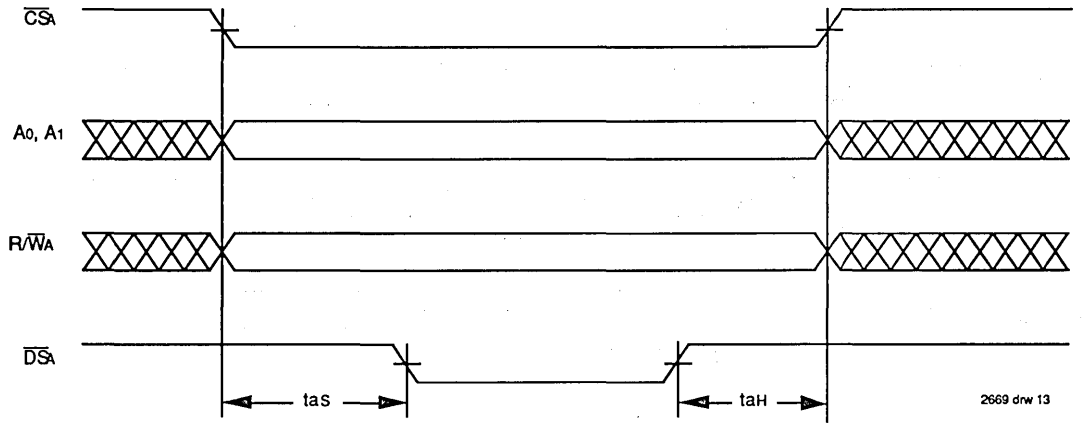


Figure 10. Basic Port A Control Signal Timing (Applies to All Port A Timing)

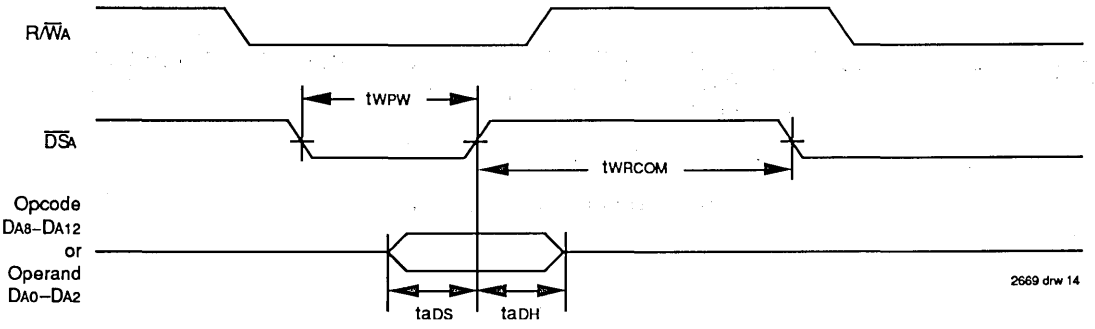
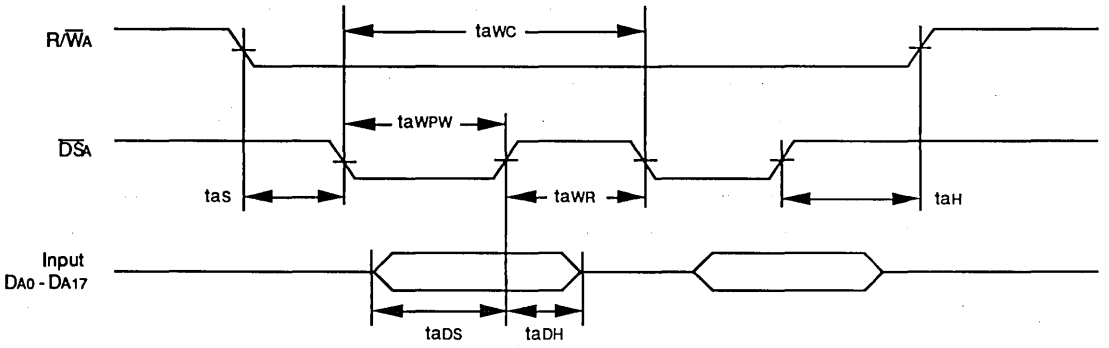


Figure 11. Port A Command Timing (Write)

WRITE



READ

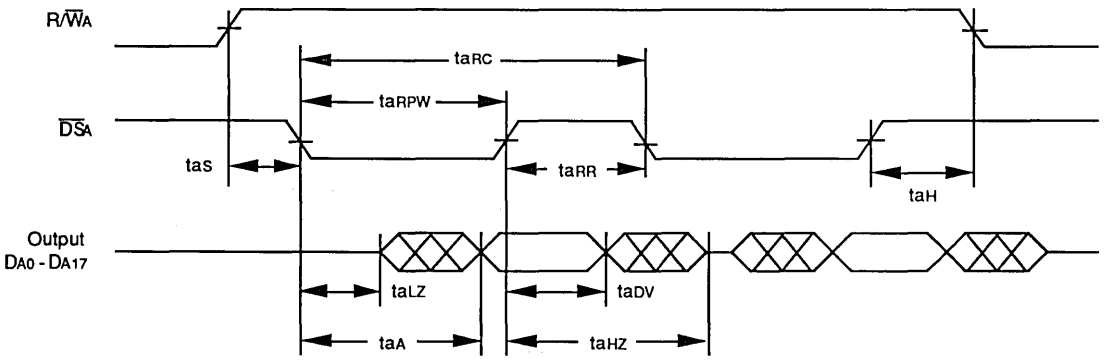
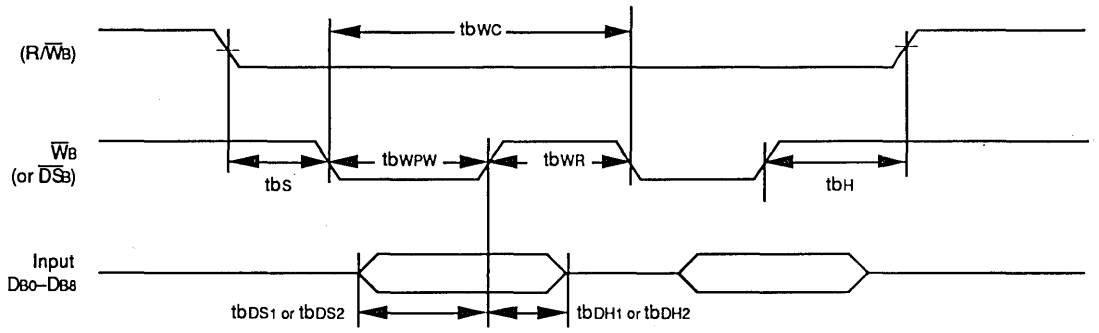


Figure 12. Read and Write Timing for Port A

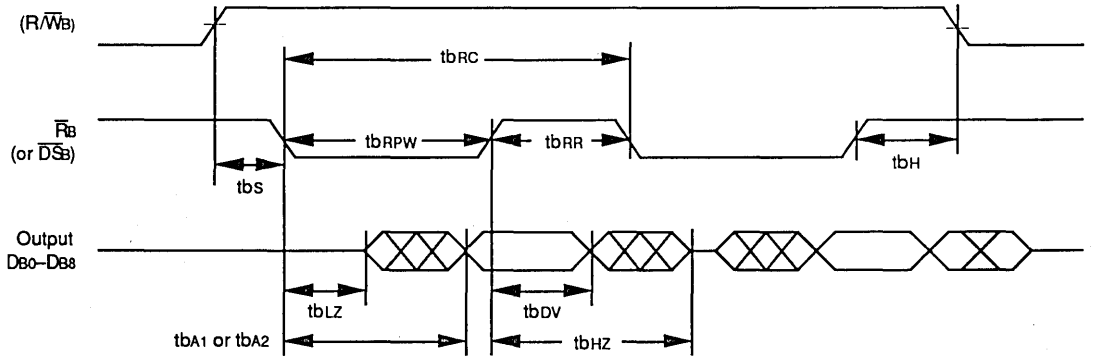
2669 drw 15

WRITE



NOTES:
1. tb_{DS1} and tb_{DH1} are with parity checking or if parity is ignored, tb_{DS2} and tb_{DH2} are with parity generation.
2. $\overline{P}_B = 1$

READ

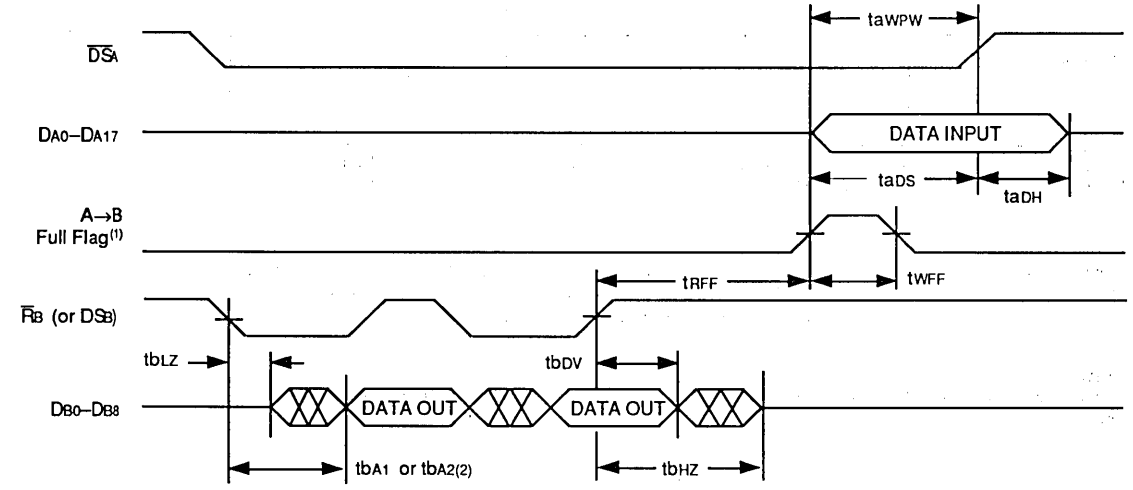


NOTES:
1. tb_{A1} is with parity checking or if parity is ignored, tb_{A2} is with parity generation.
2. $\overline{W}_B = 1$

2669 drw 18

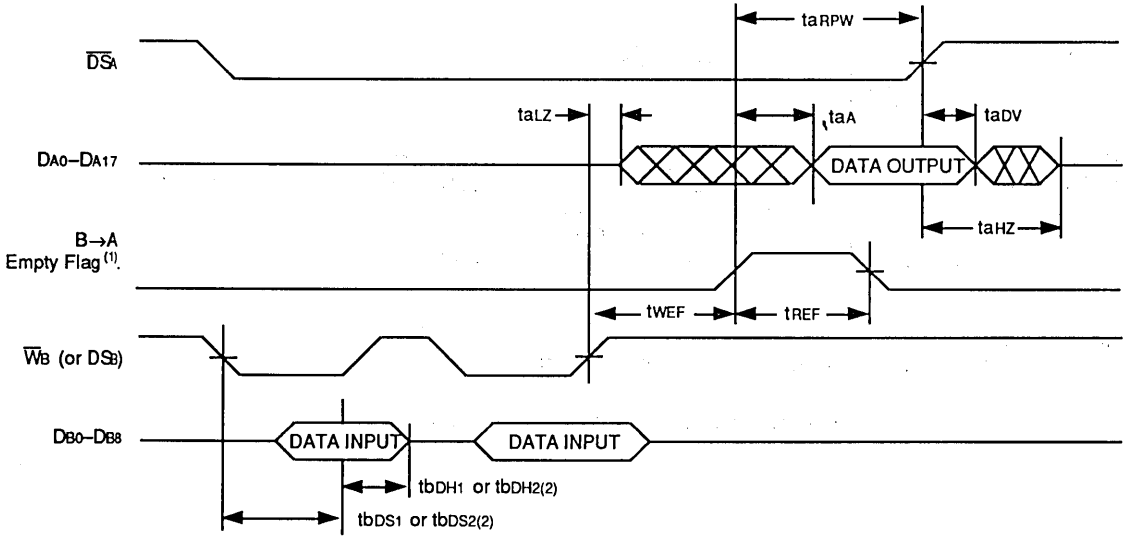
Figure 13. Port B Read and Write Timing. Processor Interface Mode Only

A→B FIFO WRITE FLOW-THROUGH



NOTES:
1. Assume the flag pin is programmed active low.
2. t_{bA1} is with parity checking or if parity is ignored, t_{bA2} is with parity generation.
3. R/$\overline{W}$A = 0.

B→A FIFO READ FLOW-THROUGH

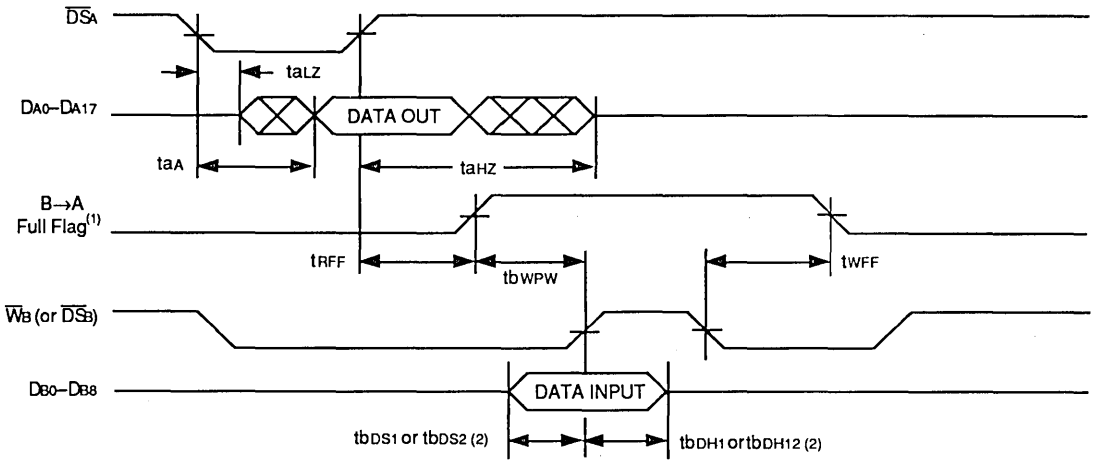


2669 drw 16

NOTES:
1. Assume the flag pin is programmed active low.
2. t_{bDS1} & t_{bDH1} is with parity checking or if parity is ignored, t_{bDS2} & t_{bDH2} is with parity generation.
3. R/$\overline{W}$A = 1.

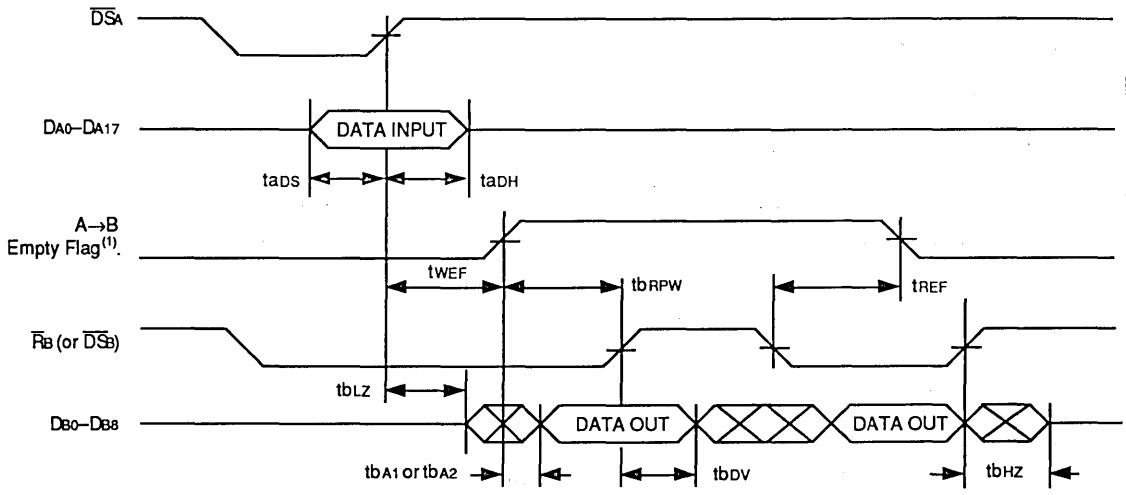
Figure 14. Port A Read and Write Flow-Through Timing. Processor Interface Mode Only

B→A FIFO WRITE FLOW-THROUGH



NOTES:
1. Assume the flag pin is programmed active low.
2. tb_{DS1} & tb_{DH1} are with parity checking or if parity is ignored, tb_{DS2} & tb_{DH2} are with parity generation.
3. $R/\overline{W}_A = 1$.

A→B FIFO READ FLOW-THROUGH

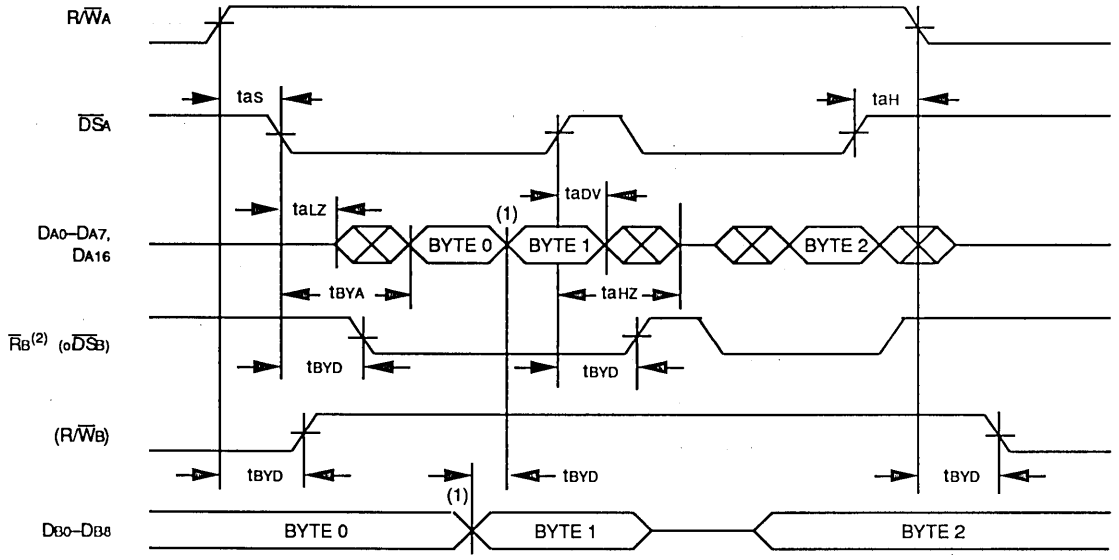


2669 drw 19

NOTES:
1. Assume the flag pin is programmed active low.
2. tb_{A1} are with parity checking or if parity is ignored, tb_{A2} are with parity generation.
3. $R/\overline{W}_A = 0$.

Figure 15. Port B Read and Write Flow-Through Timing

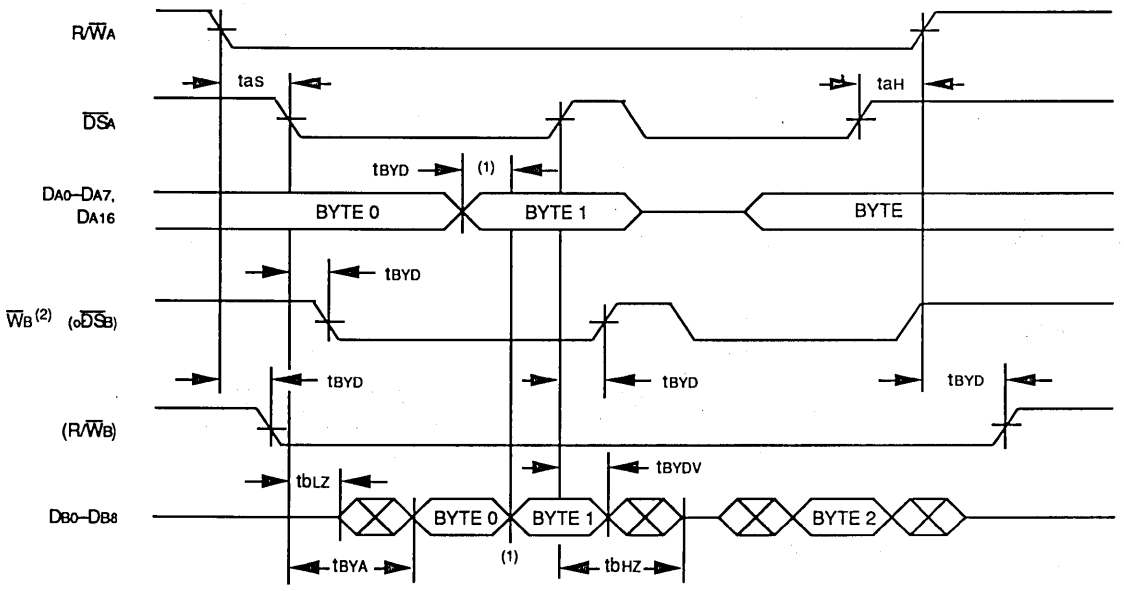
B→A READ BYPASS



NOTE:

1. Once the bypass starts, any data changes on Port B bus (Byte 0 → Byte 1) will be passed to Port A bus.
2. $\overline{WB}$ = 1.

A→B WRITE BYPASS



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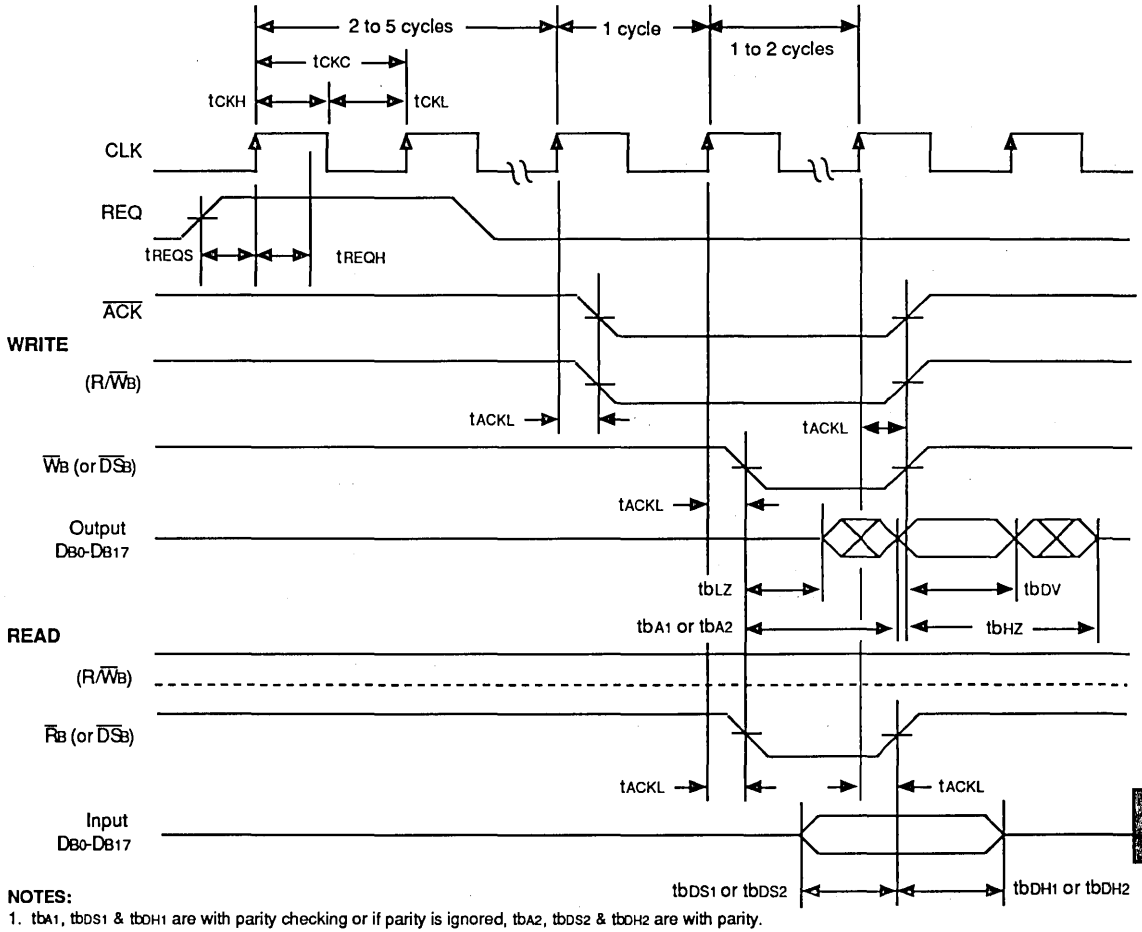
NOTE:

1. Once the bypass starts, any data changes on Port A bus (Byte 0 → Byte 1) will be passed to Port B bus.

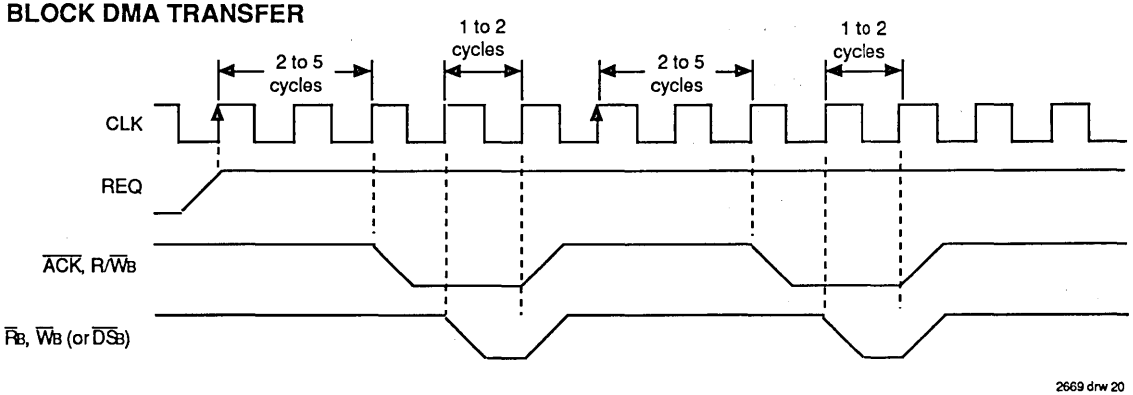
Figure 16. Bypass Path Timing. BIFIFO Must be in Peripheral Interface Mode

SINGLE WORD DMA TRANSFER



NOTES:
1. tbA1, tbDS1 & tbDH1 are with parity checking or if parity is ignored, tbA2, tbDS2 & tbDH2 are with parity.

BLOCK DMA TRANSFER



2669 drw 20

Figure 17. Port B Read and Write DMA Timing. Peripheral Interface Mode Only

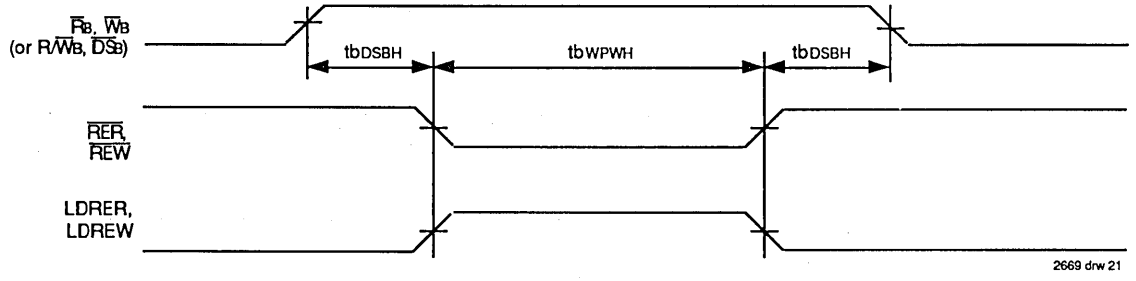
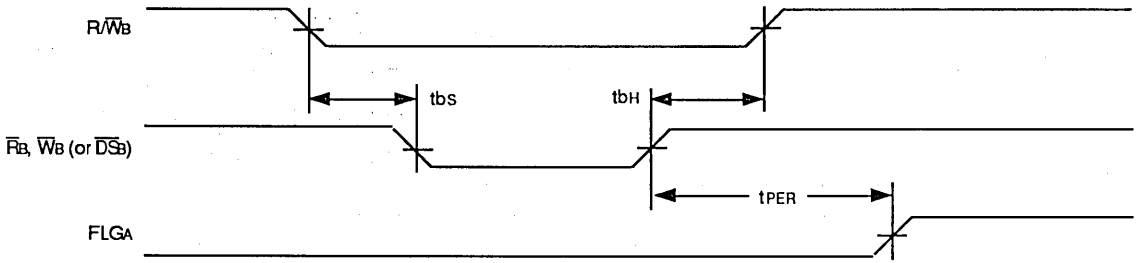
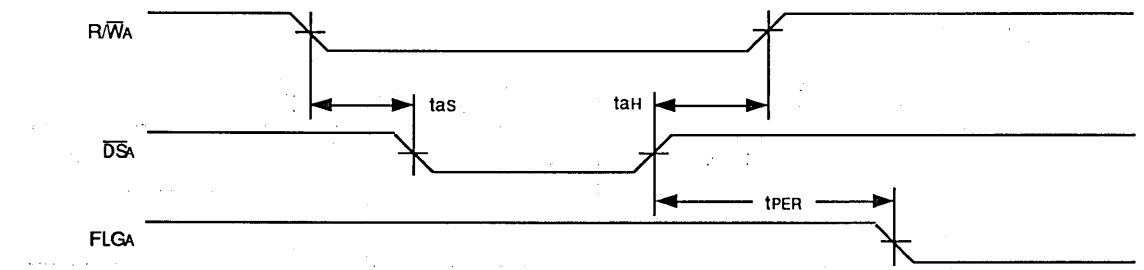


Figure 18. Port B Reread and Rewrite Timing for Intelligent Retransmit

Set Parity Error: FLGA is assigned as the parity error pin

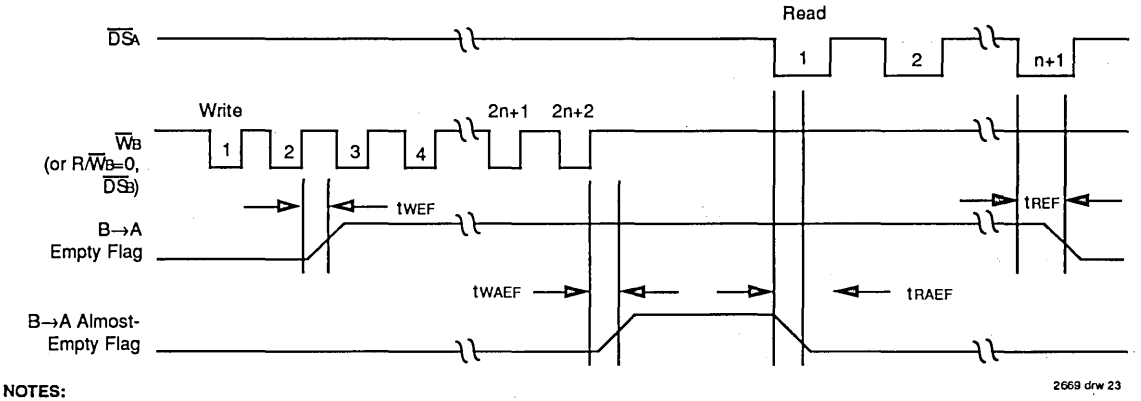


Clear Parity Error: Command written into Port A clears parity error on FLGA pin



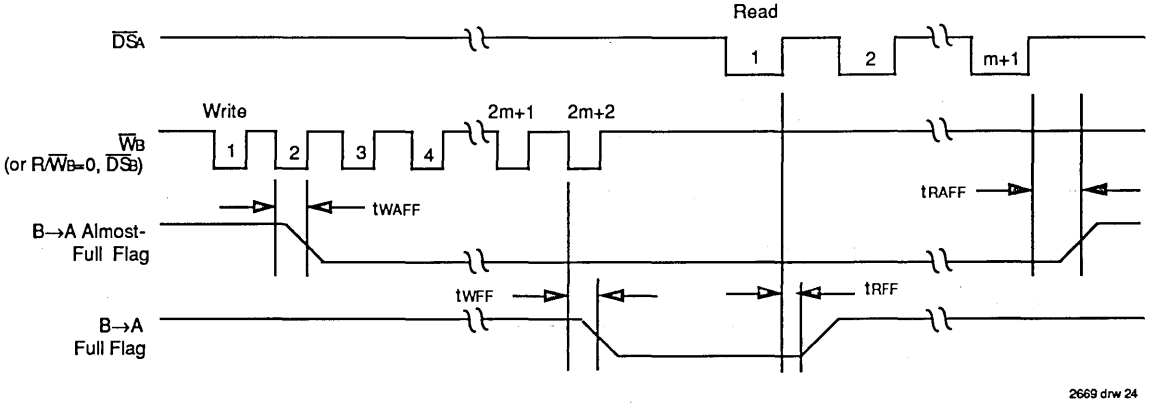
NOTE:
1. FLGA is the only pin that can be assigned as a parity error output.

Figure 19. Port B Parity Error Timing



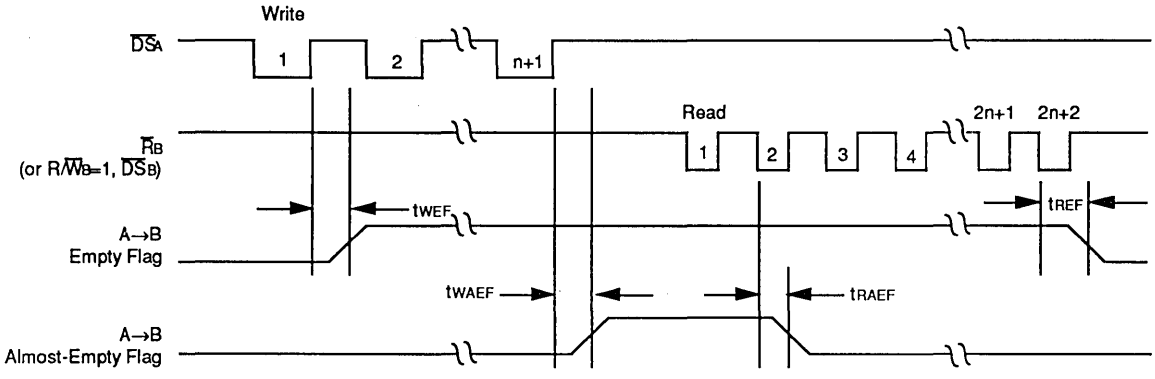
NOTES:
1. B→A FIFO is initially empty.
2. Assume the flag pins are programmed active low.
3. For stand-alone mode only; in a 36- to 9-bit configuration, Port B reads must be doubled.
4. R/$\overline{W_A}$ = 1

Figure 20. Empty and Almost-Empty Flag Timing for B→A FIFO. (n = Programmed Offset)



NOTES:
1. B→A FIFO initially contains D–(M+1) data words. D = 512 for IDT 7251/510; D = 1024 for IDT7252/520.
2. Assume the flag pins are programmed active low.
3. For stand-alone mode only; in a 36- to 9-bit configuration, Port B reads must be doubled.
4. R/$\overline{W_A}$ = 1

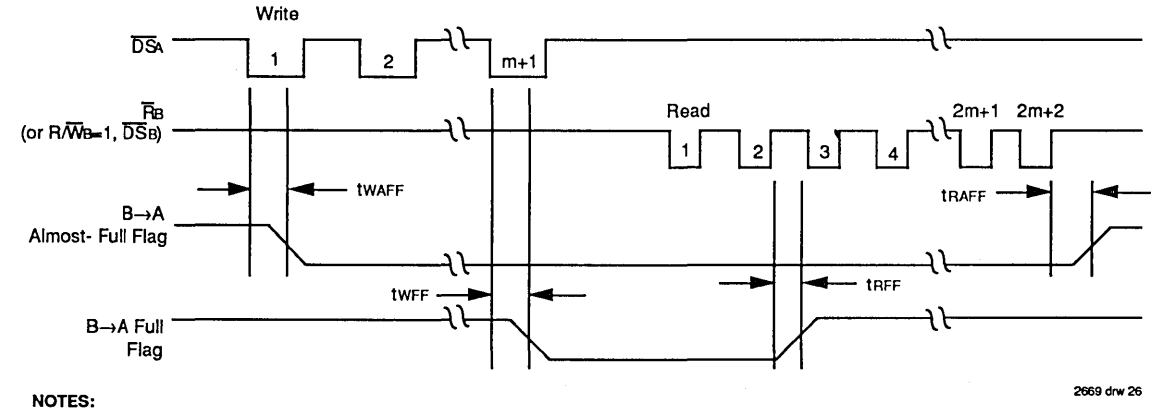
Figure 21. Full and Almost-Full Flag Timing for B→A FIFO. (m = Programmed Offset)



NOTES:

1. A→B FIFO is initially empty.
2. Assume the flag pins are programmed active low.
3. For stand-alone mode only; in a 36- to 9-bit configuration, Port B reads must be doubled.
4. R/$\overline{W_A}$ = 1

Figure 22. Empty and Almost-Empty Flag Timing for A→B FIFO. (n = Programmed Offset)

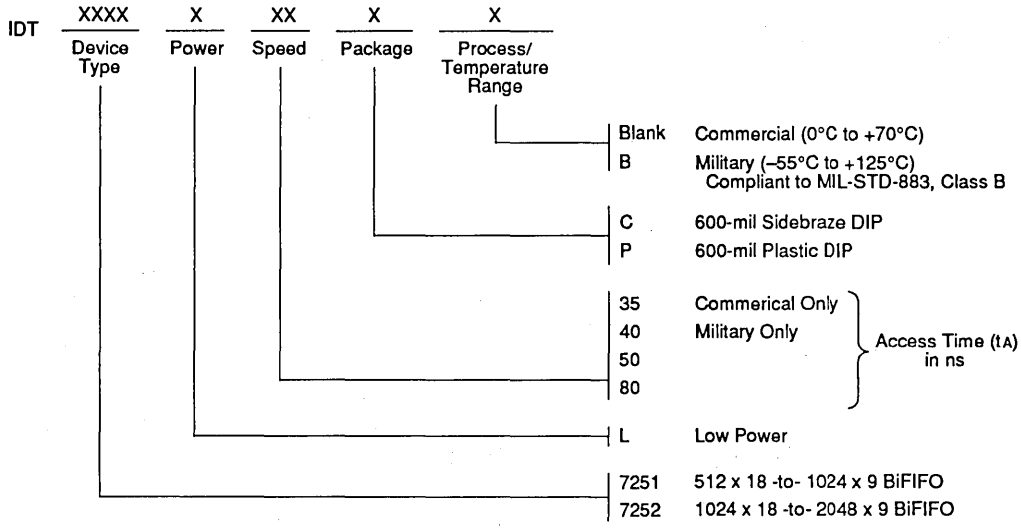


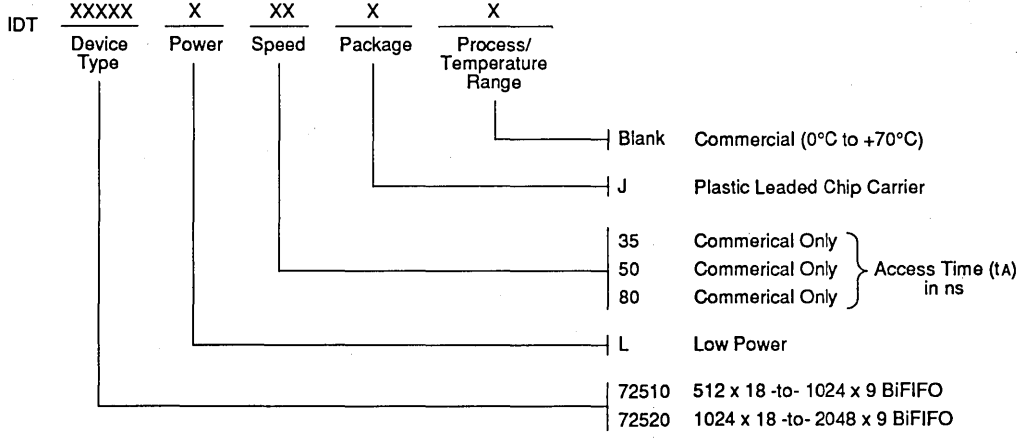
NOTES:

1. A→B FIFO initially contains D-(M+1) data words. D = 512 for IDT7251/510; D = 1024 for IDT7252/520.
2. Assume the flag pins are programmed active low.
3. For stand-alone mode only; in a 36- to 9-bit configuration, Port B reads must be doubled.
4. R/$\overline{W_A}$ = 0

Figure 23. Full and Almost-Full Flag Timing for A→B FIFO. (m = Programmed Offset)

ORDERING INFORMATION





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6

Integrated Device Technology, Inc.

PARALLEL BIDIRECTIONAL FIFO 512 x 18-BIT & 1024 x 18-BIT

IDT72511
IDT72521

FEATURES:

- Two side-by-side FIFO memory arrays for bidirectional data transfers
- 512 x 18 - Bit - 512 x 18 - Bit (IDT72511)
- 1024 x 18 - Bit - 1024 x 18 - Bit (IDT72521)
- 18-bit data buses on Port A side and Port B side
- Can be configured for 18-to-18-bit or 36-to-36-bit communication
- Fast 35ns access time
- Fully programmable standard microprocessor interface
- Built-in bypass path for direct data transfer between two ports
- Two fixed flags, Empty and Full, for both the A-to-B and the B-to-A FIFO
- Two programmable flags, Almost-Empty and Almost-Full for each FIFO
- Programmable flag offset can be set to any depth in the FIFO
- Any of the eight flags can be assigned to four external flag pins
- Flexible reread/rewrite capabilities
- Six general-purpose programmable I/O pins
- Standard DMA control pins for data exchange with peripherals
- 68-pin PGA and PLCC packages

DESCRIPTION:

The IDT72511 and IDT72521 are highly integrated first-in, first-out memories that enhance processor-to-processor and processor-to-peripheral communications. IDT BiFIFOs integrate two side-by-side memory arrays for data transfers in two directions.

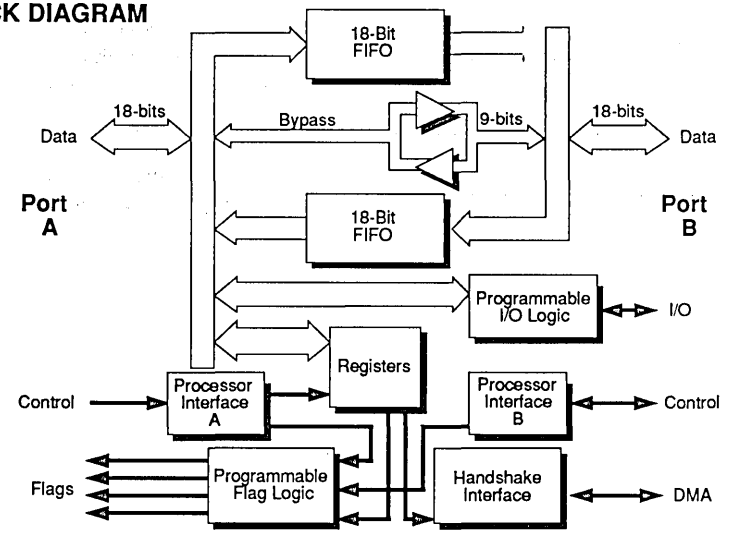
The BiFIFOs have two ports, A and B, that both have standard microprocessor interfaces. All BiFIFO operations are controlled from the 18-bit wide Port A. Port B is also 18 bits wide and can be connected to another processor or a peripheral controller. The BiFIFOs have a 9-bit bypass path that allows the device connected to Port A to pass messages directly to the Port B device.

Ten registers are accessible through Port A, a Command Register, a Status Register, and eight Configuration Registers.

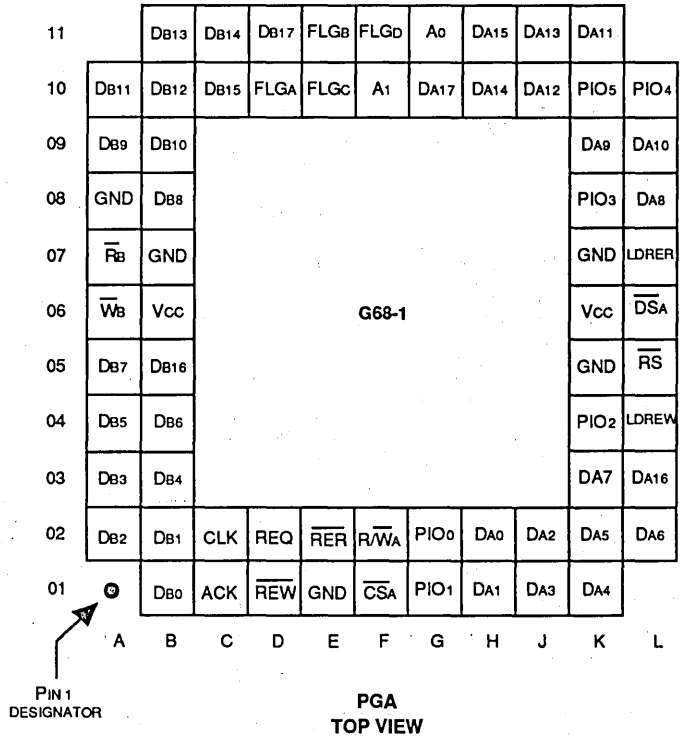
The IDT BiFIFO has programmable flags. Each FIFO memory array has four internal flags, Empty, Almost-Empty, Almost-Full and Full, for a total of eight internal flags. The Almost-Empty and Almost-Full flag offsets can be set to any depth through the Configuration Registers. These eight internal flags can be assigned to any of four external flag pins (FLG_A-FLG_D) through one Configuration Register.

Port B has programmable I/O, reread/rewrite and DMA functions. Six programmable I/O pins are manipulated through two Configuration Registers. The Reread and Rewrite controls will read or write Port B data blocks multiple times. The BiFIFO has three pins, REQ, ACK and CLK, to control DMA transfers from Port B devices.

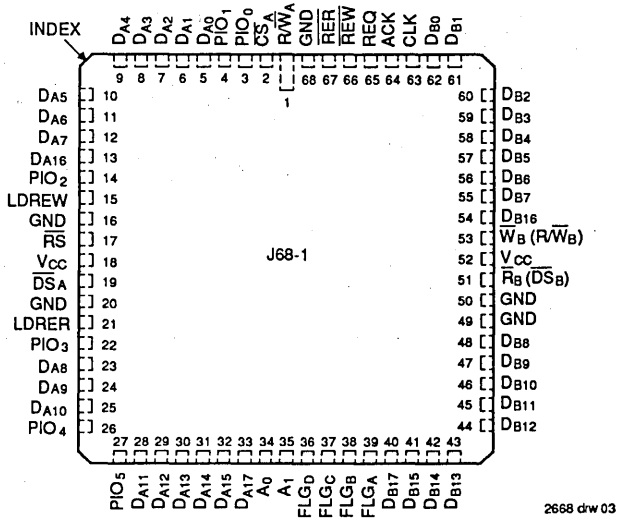
SIMPLIFIED BLOCK DIAGRAM



PIN CONFIGURATIONS



PGA
TOP VIEW



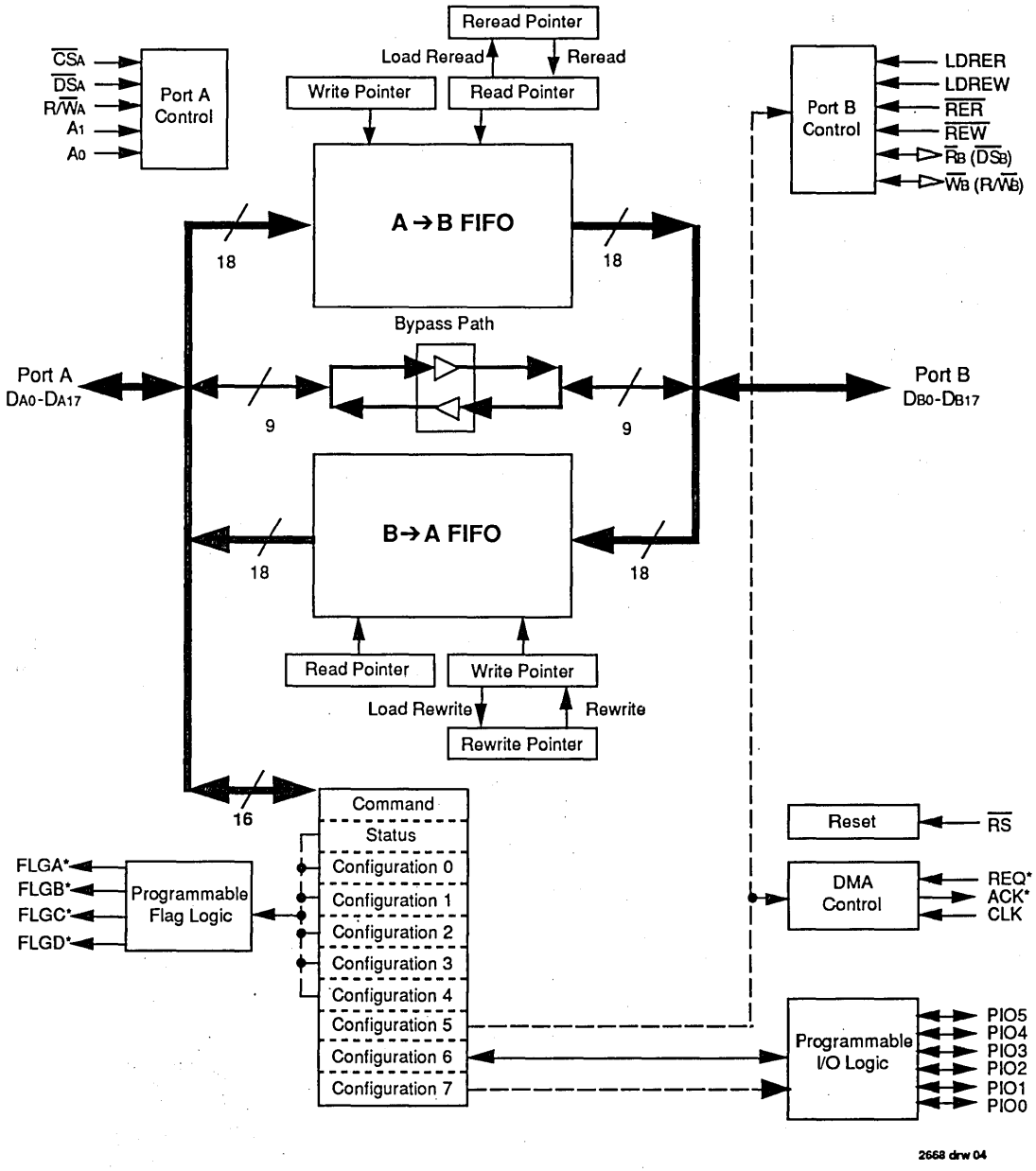
PLCC
TOP VIEW

PIN DESCRIPTION

Symbol	Name	I/O	Description
D_{A0}-D_{A17}	Data A	I/O	Data inputs and outputs for the 18-bit Port A bus.
$\overline{CS}_A$	Chip Select A	I	Port A is accessed when Chip Select A is LOW.
$\overline{DS}_A$	Data Strobe A	I	Data is written into Port A on the rising edge of Data Strobe when Chip Select is LOW. Data is read outof Port A on the falling edge of Data Strobe when Chip Select is LOW.
$R/\overline{W}_A$	Read/Write A	I	This pin controls the read or write direction of Port A. When $\overline{CS}_A$ is LOW and $R/\overline{W}_A$ is HIGH, data is read from Port A on the falling edge of $\overline{DS}_A$. When $\overline{CS}_A$ is LOW and $R/\overline{W}_A$ is LOW, data is written into Port A on the falling edge of $\overline{DS}_A$.
A_0, A_1	Addresses	I	When Chip Select A is asserted, A_0, A_1, and Read/Write A are used to select one of six internal resources.
D_{B0}-D_{B17}	Data B	I/O	Data inputs and outputs for the 18-bit Port B bus.
$\overline{R}_B$ ($\overline{DS}_B$)	Read B	I or O	If Port B is programmed to processor mode, this pin functions as an input. If Port B is programmed to peripheral mode this pin functions as an output. This pin can function as part of an Intel-style interface ($\overline{R}_B$) or as part of a Motorola-style interface ($\overline{DS}_B$). As an Intel-style interface, data is read from Port B on a falling edge of $\overline{R}_B$. As a Motorola-style interface, data is read on the falling edge of $\overline{DS}_B$ or written on the rising edge of $\overline{DS}_B$ through Port B. The default is Intel-style processor mode. ($\overline{R}_B$ as an input).
$\overline{W}_B$ ($R/\overline{W}_B$)	Write B	I or O	If Port B is programmed to processor mode, this pin functions as an input. If Port B is programmed to peripheral mode this pin functions as an output. This pin can function as part of an Intel-style interface ($\overline{W}_B$) or as part of a Motorola-style interface ($R/\overline{W}_B$). As an Intel-style interface, data is written to Port B on a rising edge of $\overline{W}_B$. As a Motorola-style interface, data is read ($R/\overline{W}_B$ = HIGH) or written ($R/\overline{W}_B$ = LOW) to Port B in conjunction with a Data Strobe B falling or rising edge. The default is Intel-style processor mode ($\overline{W}_B$ as an input.)
$\overline{RER}$	Reread	I	Loads A→B FIFO Read Pointer with the value of the Reread Pointer when LOW.
$\overline{REW}$	Rewrite	I	Loads B→A FIFO Write Pointer with the value of the Rewrite Pointer when LOW.
LDRER	Load Reread	I	Loads the Reread Pointer with the value of the A→B FIFO Read Pointer when HIGH.
LDREW	Load Rewrite	I	Loads the Rewrite Pointer with the value of the B→A FIFO Write Pointer when HIGH.
REQ	Request	I	When Port B is programmed in peripheral mode, asserting this pin begins a data transfer. Request can be programmed either active HIGH or active LOW.
ACK	Acknowledge	O	When Port B is programmed in peripheral mode, Acknowledge is asserted in response to a Request signal. This confirms that a data transfer may begin. Acknowledge can be programmed either active HIGH or active LOW.
CLK	Clock	I	This pin is used to generate timing for ACK, $\overline{R}_B$, $\overline{W}_B$, $\overline{DS}_B$ and $R/\overline{W}_B$ when Port B is in the peripheral mode.
FLGA-FLGD	Flags	O	These four outputs pins can be assigned any one of the eight internal flags in the BiFIFO. Each of the two internal FIFOs (A→B and B→A) has four internal flags: Empty, Almost-Empty, Almost-Full and Full.
PIO_0-PIO_5	Programmable Inputs/ Outputs	I/O	Six general purpose I/O pins. The input or output direction of each pin can be set independently.
$\overline{RS}$	Reset	I	A LOW on this pin will perform a reset of all BiFIFO functions.
V_{CC}	Power		There are two +5V power pins.
GND	Ground		There are five Ground pins at 0V.

2668 tbl 01

DETAILED BLOCK DIAGRAM



NOTES:

(*) Can be programmed either active high or active low in internal configuration registerers.

(††) Can be programmed through an internal configuration register to be either an input or an output.

FUNCTIONAL DESCRIPTION

IDT's BiFIFO family is versatile for both multiprocessor and peripheral applications. Data can be sent through both FIFO memories concurrently, thus freeing both processors from laborious direct memory access (DMA) protocols and frequent interrupts.

Two full 18-bit wide FIFOs are integrated into the IDT BiFIFO, making simultaneous data exchange possible. Each FIFO is monitored by separate internal read and write pointers, so communication is not only bidirectional, it is also totally independent in each direction. The processor connected to Port A of the BiFIFO can send or receive messages directly to the Port B device using the BiFIFO's 9-bit bypass path.

The BiFIFO can be used in different bus configurations: 18 bits to 18 bits and 36 bits to 36 bits. One BiFIFO can be used for the 18- to 18-bit configuration, and two BiFIFOs are required for 36- to 36-bit configuration. This configuration can be extended to wider bus widths (54- to 54-bits, 72- to 72-bits, ...) by adding more BiFIFOs to the configuration.

The microprocessor or microcontroller connected to Port A controls all operations of the BiFIFO. Thus, all Port A interface pins are inputs driven by the controlling processor. Port B can be programmed to interface either with a second processor or a peripheral device. When Port B is programmed in processor interface mode, the Port B interface pins are inputs driven by the second processor. If a peripheral device is connected to the BiFIFO, Port B is programmed to peripheral interface mode and the interface pins are outputs.

18- to 18-bit Configurations

A single BiFIFO can be configured to connect an 18-bit processor to another 18-bit processor or an 18-bit peripheral. The upper BiFIFO shown in each of the Figures 1 and 2 can be used in 18- to 18-bit configurations for processor and peripheral interface modes respectively.

36- to 36-bit Configurations

In a 36- to 36-bit configuration, two BiFIFOs operate in parallel. Both BiFIFOs are programmed simultaneously, 18 data bits to each device. Figures 1 and 2 show multiple BiFIFOs configured for processor and peripheral interface modes respectively.

Processor Interface Mode

When a microprocessor or microcontroller is connected to Port B, all BiFIFOs in the configuration must be programmed to processor interface mode. In this mode, all Port B interface controls are inputs. Both REQ and CLK pins should be pulled LOW to ensure that the setup and hold time requirements for these pins are met during reset. Figure 1 shows the BiFIFO in processor interface mode.

Peripheral Interface Mode

If Port B is connected to a peripheral controller, all BiFIFOs in the configuration must be programmed in peripheral interface mode. In this mode, all the Port B interface pins are all outputs. To assure fixed high states for $\overline{R}_B$ and $\overline{W}_B$ before they are programmed into an output, these two pins should be pulled up to Vcc with 10K resistors. Of course, only one set of Port B interface pins should be used to control a single peripheral device, while the other interface pins are all ignored. Figure 2 shows a BiFIFO configuration connected to a peripheral.

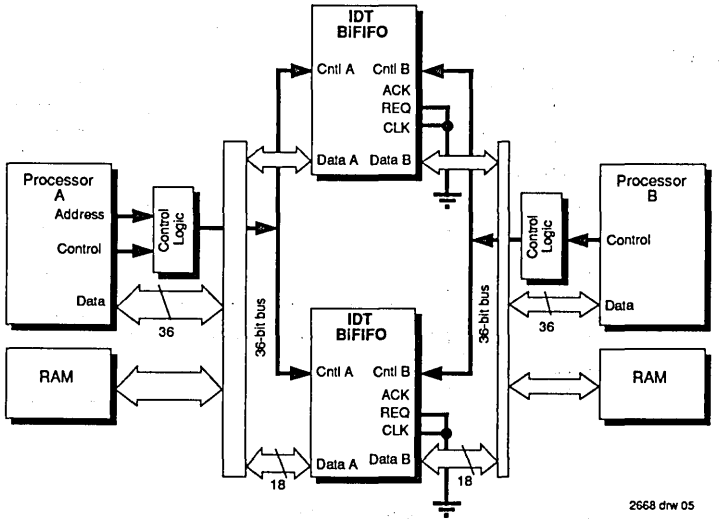


Figure 1. 36-Bit Processor to 36-Bit Processor Configuration

NOTE:
1. 36- to 36-bit processor interface configuration. Upper BiFIFO only is used in 18- to 18-bit configuration. Note that *Cntl A* refers to $\overline{CS}_A$, A_1, A_0, R/$\overline{W}_A$, and $\overline{DS}_A$; *Cntl B* refers to R/$\overline{W}_B$ and $\overline{DS}_B$ or $\overline{R}_B$ and $\overline{W}_B$.

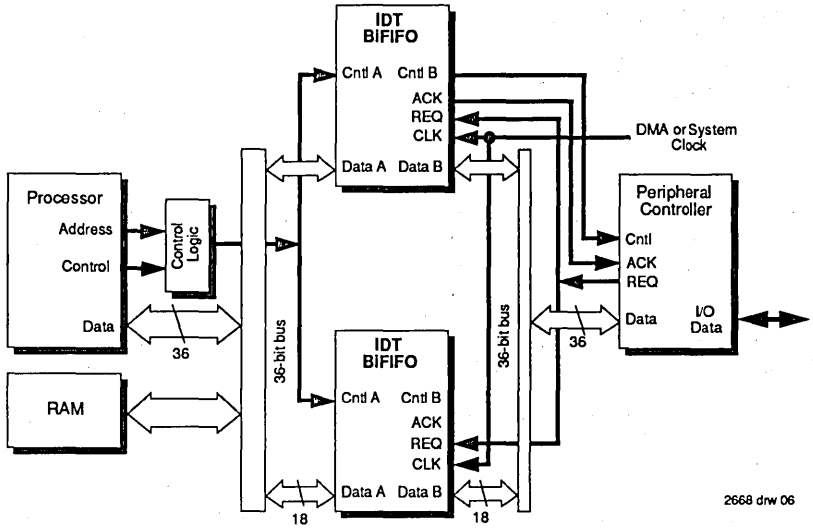


Figure 2. 36-Bit Processor to 36-Bit Peripheral Configuration

NOTE:
1. 36- to 36-bit peripheral interface configuration. Upper BiFIFO only is used in 18- to 18-bit configuration. Note that *Cntl A* refers to $\overline{CS}_A$, A_1, A_0, R/$\overline{W}_A$, and $\overline{DS}_A$; *Cntl B* refers to R/$\overline{W}_B$ and $\overline{DS}_B$ or $\overline{R}_B$ and $\overline{W}_B$.

Port A Interface

The BiFIFO is straightforward to use in microprocessor-based systems because each BiFIFO port has a standard microprocessor control set. Port A has access to six resources: the A→B FIFO, the B→A FIFO, the 9-bit direct data bus (bypass path), the configuration registers, status and command registers. The Port A Address and Read/Write pins determine the resource being accessed as shown in Table 1. Data Strobe is used to move data in and out of the BiFIFO.

When either of the internal FIFOs are accessed, 18 bits of data are transferred across Port A. Since the bypass path is only 9 bits wide, the least significant byte (DA_0-DA_7, DA_{16}) is used on Port A. All of the registers are 16 bits wide which means only the data bits (DA_0-DA_{15}) are passed by Port A.

Bypass Path

The bypass path acts as a bidirectional bus transceiver directly between Port A and Port B. The direct connection requires that the Port A interface pins are inputs and the Port B interface pins are outputs. The bypass path is 9 bits wide in an 18- to 18-bit configuration or 18 bits wide in a 36- to 36-bit configuration.

During bypass operations, the BiFIFOs must be programmed into peripheral interface mode. Bit 10 of Configuration Register 5 (see Table 10) is set to 1 for peripheral interface mode.

Command Register

Ten registers are accessible through Port A, a Command Register, a Status Register, and eight Configuration Registers.

The Command Register is written by setting $\overline{CS}_A$ = 0, A_1 = 1, A_0 = 1. Commands written into the BiFIFO have a 4-bit opcode (bit 8 – bit 11) and a 3-bit operand (bit 0 – bit 2) as shown in Figure 3. The commands can be used to reset the BiFIFO, to select the Configuration Register, to perform intelligent reread/rewrite, to set the Port B DMA direction, to set the Status Register format, and to modify the Port B Read and Write Pointers. The command opcodes are shown in Table 2.

The reset command initializes different portions of the BiFIFO depending on the command operand. Table 3 shows the reset command operands.

The Configuration Register address is set directly by the command operands shown in Table 4.

Intelligent reread/rewrite is performed by interchanging the Port B Read Pointer with the Reread Pointer or by interchanging the Port B Write Pointer with the Rewrite Pointer. No command operands are required to perform a reread/rewrite operation.

COMMAND FORMAT

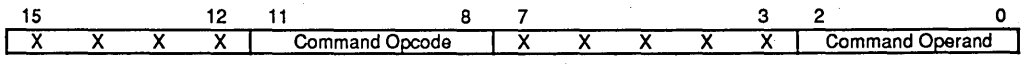


Figure 3. Format for Commands Written into Port A

When Port B of the BiFIFO is in peripheral mode, the DMA direction is controlled by the Command Register. Table 5 shows the Port B read/write DMA direction operands.

Two commands are provided to increment the Port B Read and Write Pointers. No operands are required for these commands.

Reset

The IDT72511 and IDT72521 have a hardware reset pin ($\overline{RS}$) that resets all BiFIFO functions. A hardware reset requires the following four conditions: $\overline{R}_B$ and $\overline{W}_B$ must be HIGH, $\overline{RER}$ and $\overline{REW}$ must be HIGH, LDRER and LDREW must be LOW, and $\overline{DS}_A$ must be HIGH (Figure 9). After a hardware reset, the BiFIFO is in the following state: Configuration Registers 0-3 are **0000H**, Configuration Register 4 is set to **6420H**, and Configuration Registers 5, 6 and 7 are **0000H**. Additionally, all the pointers including the Reread and Rewrite Pointers are set to **0**, the DMA direction is set to B→A write, and the internal DMA request circuitry is cleared (set to its initial state).

A software reset command can reset A→B pointers and the B→A pointers to **0** independently or together. The internal request DMA circuitry can also be reset independently. A software Reset All command resets all the pointers, the DMA request circuitry, and sets all the Configuration Registers to their default condition. Note that a hardware reset is **NOT** the same as a software Reset All command. Table 6 shows the BiFIFO state after the different hardware and software resets

Status Register

The Status Register reports the state of the programmable flags and the DMA read/write direction. The Status Register is read by setting $\overline{CS}_A$ = 0, A_1 = 1, A_0 = 1 (see Table 1). See Table 7 for the Status Register format.

Configuration Registers

The eight Configuration Register formats are shown in Table 8. Configuration Registers 0-3 contain the programmable

PORT A RESOURCE SELECTION

$\overline{CS}_A$	A_1	A_0	Read	Write
0	0	0	B→A FIFO	A→B FIFO
0	0	1	9-bit Bypass Path	9-bit Bypass Path
0	1	0	Configuration Registers	Configuration Registers
0	1	1	Status Register	Command Register
1	X	X	Disabled	Disabled

2668 tbl 03

Table 1. Accessing Port A Resources Using $\overline{CS}_A$, A_0 and A_1

COMMAND OPERATIONS

Command Opcode	Function
0000	Reset BiFIFO (see Table 3)
0001	Select Configuration Register (see Table 4)
0010	Load Reread Pointer with Read Pointer Value
0011	Load Rewrite Pointer with Write Pointer Value
0100	Load Read Pointer with Reread Pointer Value
0101	Load Write Pointer with Rewrite Pointer Value
0110	Set DMA Transfer Direction (see Table 5)
0111	Reserved
1000	Increment A→B FIFO Read Pointer (Port B)
1001	Increment B→A FIFO Write Pointer (Port B)
1010	Reserved
1011	Reserved

2668 tbl 04

Table 2. Functions Performed by Port A Commands

RESET COMMAND FUNCTIONS

Reset Operands	Function
000	No Operation
001	Reset B→A FIFO (Read, Write, and Rewrite Pointers = 0)
010	Reset A→B FIFO (Read, Write, and Reread Pointers = 0)
011	Reset B→A and A→B FIFO
100	Reset Internal DMA Request Circuitry
101	No Operation
110	No Operation
111	Reset All

2668 tbl 05

Table 3. Reset Command Functions

SELECT CONFIGURATION REGISTER/ COMMAND FUNCTIONS

Operands	Function
000	Select Configuration Register 0
001	Select Configuration Register 1
010	Select Configuration Register 2
011	Select Configuration Register 3
100	Select Configuration Register 4
101	Select Configuration Register 5
110	Select Configuration Register 6
111	Select Configuration Register 7

2668 tbl 06

Table 4. Select Configuration Register Functions.

DMA DIRECTION COMMAND FUNCTIONS

Operands	Function
XX0	Write B→A FIFO
XX1	Read A→B FIFO

2668 tbl 07

Table 5. Set DMA Direction Command Functions. Command Only Operates in Peripheral Interface Mode

STATE AFTER RESET

	Hardware Reset (RS asserted)	Software Reset				
		B→A(001)	A→B(010)	B→A and A→B(011)	Internal Request (100)	All(111)
Configuration Registers 0-3	0000H	—	—	—	—	0000H
Configuration Register 4	6420H	—	—	—	—	6420H
Configuration Register 5	0000H	—	—	—	—	0000H
Configuration Register 6-7	0000H	—	—	—	—	0000H
Status Register format	0	—	—	—	—	—
B→A Read, Write, Rewrite Pointers	0	0	—	0	—	0
A→B Read, Write, Reread Pointers	0	—	0	0	—	0
DMA direction	B→A write	—	—	—	—	—
DMA internal request	clear	—	—	—	clear	clear

2668 tbl 08

Table 6. The BIFIFO State After a Reset Command

flag offsets for the Almost-Empty and Almost-Full flags. These offsets are set to **0** when a hardware reset or a software Reset All is applied. Note that Table 8 shows that Configuration Registers 0-3 are 10 bits wide to accommodate the 1024 locations in each FIFO memory of the IDT7252/520. Only 9 least significant bits are used for the 512 locations of the IDT7251/510; the most significant bit, bit 9, must be set to **0**.

Configuration Register 4 is used to assign the internal flags to the external flag pins (FLG_A-FLG_D). Each external flag pin is assigned an internal flag based on the four bit codes shown in Table 9. The default condition for Configuration Register 4 is **6420H** as shown in Table 6. The default flag assignments are: FLG_D is assigned B→A $\overline{Full}$, FLG_C is assigned B→A $\overline{Empty}$, FLG_B is assigned A→B $\overline{Full}$, FLG_A is assigned A→B $\overline{Empty}$.

Configuration Register 5 is a general control register. The format of Configuration Register 5 is shown in Table 10.

Bit 0 sets the Intel-style interface ($\overline{R}_B$, $\overline{W}_B$) or Motorola-style interface ($\overline{DS}_B$, R/$\overline{W}_B$) for Port B. Bits 2 and 3 redefine Full and Empty Flags for reread/rewrite data protection.

Bits 4-9 control the DMA interface and are only applicable in peripheral interface mode. In processor interface mode, these bits are don't care states. Bits 4 and 5 set the polarity of the DMA control pins REQ and ACK respectively. An internal clock controls all DMA operations. This internal clock is derived from the external clock (CLK). Bit 9 determines the internal clock frequency: the internal clock = CLK or the internal clock = CLK divided by 2. Bit 8 sets whether $\overline{R}_B$, $\overline{W}_B$, and $\overline{DS}_B$ are asserted for either one or two internal clocks. Bits 6 and 7 set the number of internal clocks between REQ assertion and ACK assertion. The timing can be from 2 to 5 cycles as shown in Figure 17.

Bit 10 controls Port B processor or peripheral interface mode. In processor mode, the Port B control pins ($\overline{R}_B$, $\overline{W}_B$, $\overline{DS}_B$, R/$\overline{W}_B$) are inputs and the DMA controls are ignored. In peripheral mode, the Port B control pins are outputs and the DMA controls are active.

Six PIO pins can be programmed as an input or output by the corresponding mask bits in Configuration Register 7. The format of Configuration Register 7 is shown in Figure 5. Each bit of the register set the I/O direction independently. A logic **1** indicates that the corresponding PIO pin is an output, while a logic **0** indicates that the PIO pin is an input. This I/O mask register can be read or written.

A programmed output PIO_i pin (i = 0, 1, . . . 5) displays the data latched in Bit i of Configuration Register 6. A programmed input PIO_i pin allows Port A bus to sample the data on DA_i by reading Configuration Register 6.

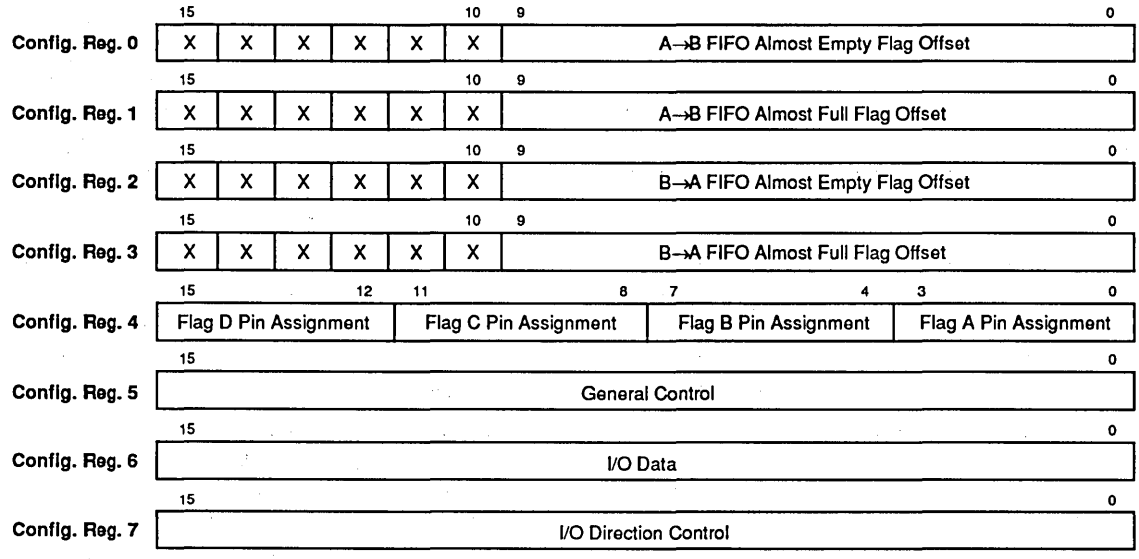
STATUS REGISTER FORMAT

Bit	Signal
0	Reserved
1	Reserved
2	Reserved
3	DMA Direction
4	A→B Empty Flag
5	A→B Almost-Empty Flag
6	B→A Full Flag
7	B→A Almost-Full Flag
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	A→B Full Flag
13	A→B Almost-Full Flag
14	B→A Empty Flag
15	B→A Almost-Empty Flag

2668 tbl 09

Table 7. The Status Register Format

CONFIGURATION REGISTER FORMATS



NOTE:
1. Bit 9 of Configuration Registers 0-3 must be set to 0 on the IDT72511.

2668 drw 02

Table 8. The BiFIFO Configuration Register Formats

Programmable Flags

The IDT BiFIFO has eight internal flags. Associated with each FIFO memory array are four internal flags, Empty, Almost-Empty, Almost-Full and Full, for the total of eight internal flags. The Almost-Empty and Almost-Full offsets can be set to any depth through the Configuration Registers 0-3 (see Table 8). The flags are asserted at the depths shown in Table 11. After a hardware reset or a software Reset All, the almost flag offsets are set to **0**. Even though the offsets are equivalent, the Empty and Almost-Empty flags have different timing which means that the flags are not coincident. Similarly, the Full and Almost-Full flags are not coincident after reset because of timing.

These eight internal flags can be assigned to any of four external flag pins (FLGA-FLGD) through Configuration Register 4 (see Table 9). For the specific flag timings, see Figures 20-23.

The current state of all eight flags is available in the Status Register.

EXTERNAL FLAG ASSIGNMENT CODES

Assignment Code	Internal Flag Assigned to Flag Pin
0000	A→B $\overline{\text{Empty}}$
0001	A→B $\overline{\text{Almost-Empty}}$
0010	A→B $\overline{\text{Full}}$
0011	A→B $\overline{\text{Almost-Full}}$
0100	B→A $\overline{\text{Empty}}$
0101	B→A $\overline{\text{Almost-Empty}}$
0110	B→A $\overline{\text{Full}}$
0111	B→A $\overline{\text{Almost-Full}}$
1000	A→B Empty
1001	A→B Almost-Empty
1010	A→B Full
1011	A→B Almost-Full
1100	B→A Empty
1101	B→A Almost-Empty
1110	B→A Full
1111	B→A Almost-Full

2668 tbl 11

Table 9. Configuration Register 4 Internal Flag Assignments to External Flag Pins

CONFIGURATION REGISTER 5 FORMAT

Bit	Function		
0	Select Port B Interface $\overline{R}_B$ and $\overline{W}_B$ or $\overline{DS}_B$ and R/$\overline{W}_B$	0	Pins are $\overline{R}_B$ and $\overline{W}_B$ (Intel-style interface)
		1	Pins are $\overline{DS}_B$ and R/$\overline{W}_B$ (Motorola-style interface)
1	Unused		
2	Full Flag Definition	0	Write pointer meets read pointer
		1	Write pointer meets reread pointer
3	Empty Flag Definition	0	Read pointer meets write pointer
		1	Read pointer meets rewrite pointer
4	REQ Pin Polarity	0	REQ pin active HIGH
		1	REQ pin active LOW
5	ACK Pin Polarity	0	ACK pin active LOW
		1	ACK pin active HIGH
7-6	REQ / ACK Timing	00	2 internal clocks between REQ assertion and ACK assertion
		01	3 internal clocks between REQ assertion and ACK assertion
		10	4 internal clocks between REQ assertion and ACK assertion
		11	5 internal clocks between REQ assertion and ACK assertion
8	Port B Read & Write Timing Control for Peripheral Mode	0	$\overline{R}_B$, $\overline{W}_B$, and $\overline{DS}_B$ are asserted for 1 internal clock
		1	$\overline{R}_B$, $\overline{W}_B$, and $\overline{DS}_B$ are asserted for 2 internal clocks
9	Internal Clock Frequency Control	0	Internal clock = CLK
		1	Internal clock = CLK divided by 2
10	Port B Interface Mode Control	0	Processor interface mode (Port B controls are inputs)
		1	Peripheral interface mode (Port B controls are outputs)
11	Unused		
12	Unused		
13	Unused		
14	Unused		
15	Unused		

2668 tbl 12

Table 10. BIFIFO Configuration Register 5 Format

CONFIGURATION REGISTER 6 FORMAT

15 ... 6	5	4	3	2	1	0
Unused	PIO5	PIO4	PIO3	PIO2	PIO1	PIO0

2668 tbl 13

Figure 4. BIFIFO Configuration Register 6 Format for Programmable I/O Data

CONFIGURATION REGISTER 7 FORMAT

15 ... 6	5	4	3	2	1	0
Unused	MIO5	MIO4	MIO3	MIO2	MIO1	MIO0

2668 tbl 23

Figure 5. BIFIFO Configuration Register 7 Format for Programmable I/O Direction Mask

Port B Interface

Port B has reread/rewrite and DMA functions. Port B can be configured to interface to either Intel-style ($\overline{R}_B$, $\overline{W}_B$) or Motorola-style ($\overline{DS}_B$, R/$\overline{W}_B$) devices in Configuration Register 5 (see Table 10). Port B can also be configured to talk to a processor or a peripheral device through Configuration Register 5. In processor interface mode, the Port B interface controls are inputs. In peripheral interface mode, the Port B interface controls are outputs. After a hardware reset or a software Reset All command, Port B defaults to an Intel-style processor interface; the controls are inputs.

DMA Control Interface

The BiFIFO has DMA control to simplify data transfers with peripherals. For the BiFIFO DMA controls (REQ, ACK and CLK) to operate, the BiFIFO must be in peripheral interface mode (Configuration Register 5, Table 10).

DMA timing is controlled by the external clock input, CLK. An internal clock is derived from this CLK signal to generate the $\overline{R}_B$, $\overline{W}_B$, $\overline{DS}_B$ and R/$\overline{W}_B$ output signals. The internal clock also determines the timing between REQ assertion and ACK assertion. Bit 9 of Configuration Register 5 determines whether the internal clock is the same as CLK or whether the internal clock is CLK divided by 2.

Bit 8 of Configuration Register 5 set whether $\overline{R}_B$, $\overline{W}_B$ and $\overline{DS}_B$ are asserted for 1 or 2 internal clocks. Bits 6 and 7 of Configuration Register 5 set the number of clocks between REQ assertion and ACK assertion. The clocks between REQ assertion and ACK assertion can be 2, 3, 4 or 5.

Bits 4 and 5 of Configuration Register 5 set the polarity of the REQ and ACK pins respectively.

A DMA transfer command sets the Port B read/write direction (see Table 5). The timing diagram for DMA transfers is shown in Figure 17. The basic DMA transfer starts with REQ assertion. After 2 to 5 internal clocks, ACK is asserted by the BiFIFO. ACK will not be asserted if a read is attempted on an empty A→B FIFO or if a write is attempted on a full B→A FIFO. If the BiFIFO is in Motorola-style interface mode, R/$\overline{W}_B$ is set at the same time that ACK is asserted. One internal clock later, $\overline{DS}_B$ is asserted. If the BiFIFO is in Intel-style interface mode, either $\overline{R}_B$ or $\overline{W}_B$ is asserted one internal clock after ACK assertion. These read/write controls stay asserted for 1 or 2 internal clocks, then ACK, $\overline{DS}_B$, $\overline{R}_B$ and $\overline{W}_B$ are made inactive. This completes the transfer of one 9-bit word.

On the next rising edge of CLK, REQ is sampled. If REQ is still asserted, another DMA transfer starts with the assertion of ACK. Data transfers will continue as long as REQ is asserted.

Intelligent Reread/Rewrite

Intelligent reread/rewrite is a method the BiFIFO uses to help assure data integrity. Port B of the BiFIFO has two extra pointers, the Reread Pointer and the Rewrite Pointer. The Reread Pointer is associated with the A->B FIFO Read Pointer, while the Rewrite Pointer is associated with the B->A FIFO Write Pointer. The Reread Pointer holds the start address of a data block in the A->B FIFO RAM, and the Read Pointer is the current address of the same FIFO RAM array. By loading the Read Pointer with the value held in the Reread Pointer (RER asserted), reads will start over at the beginning of the data block. In order to mark the beginning of a data block, the Reread Pointer should be loaded with the Read Pointer value (LDRER asserted) before the first read is performed on this data block. Figure 6 shows a Reread operation.

Similarly, the Rewrite Pointer holds the start address of a data block in the B->A FIFO RAM, while the Write Pointer is the current address within the RAM array. The operation of the REW and LDREW is identical to the RER and LDRER discussed above. Figure 7 shows a Rewrite operation.

For the reread data protection, Bit 2 of Configuration Register 5 can be set to 1 to prevent the data block from being overwritten. In this way, the assertion of A->B full flag will occur when the write pointer meets the reread pointer instead of the read pointer as in the normal definition. For the rewrite data protection, Bit 3 of Configuration Register 5 can be set to 1 to

INTERNAL FLAG TRUTH TABLE

Number of Words in FIFO					
From	To	Empty Flag	Almost-Empty Flag	Almost-Full Flag	Full Flag
0	0	Asserted	Asserted	Not Asserted	Not Asserted
1	n	Not Asserted	Asserted	Not Asserted	Not Asserted
n + 1	D – (m + 1)	Not Asserted	Not Asserted	Not Asserted	Not Asserted
D – m	D – 1	Not Asserted	Not Asserted	Asserted	Not Asserted
D	D	Not Asserted	Not Asserted	Asserted	Asserted

NOTE: 2668 tbl 14

1. BiFIFO flags must be assigned to external flag pins to be observed. D = FIFO depth (IDT72511 = 512, IDT72521 = 1024), n = Almost-Empty flag offset, m = Almost-Full flag offset.

Table 11. Internal Flag Truth Table

prevent the data block from being read. In this case the assertion of B->A empty flag will occur when the read pointer meets the rewrite pointer instead of the write pointer.

In conclusion, Bit 2 and 3 of Configuration Register 5 are used to redefine Full & Empty flags for data block partition. Although it can serve the purpose of data protection, the setting of these 2 bits is independent of the functions caused by RER/REW, or LDRER/LDREW assertions.

Programmable Input/Output

The BiFIFO has six programmable I/0 pins (PIO_0 - PIO_5) which are controlled by Port A through Configuration Registers 6 and 7. Data from the programmable I/O pins is mapped directly to the six least significant bits of Configuration Register 6. Figure 4 shows the format of Configuration Register 6. This data is read or written by Port A on the data pins (DA_0- DA_5). A programmed output PIO_i pin (i = 0, 1, . . . , 5) displays the data latched in Bit i of Configuration Register 6. A programmed input PIO_i pin allows Port A bus to sample its data on DA_i by reading Configuration Register 6. The read and write timing for the programmable I/O pins is shown in Figure 19. The direction of each programmable I/O pin can be set independently by programming the mask in Configuration Register 7. Each P10 pin has a corresponding input/output direction mask bit in Configuration Register 7. Figure 5 shows the format of Configuration Register 7. Setting a mask bit to a logic 1 makes the corresponding I/O pin an output. Mask bits set to logic 0 force the corresponding I/O pin to an input.

REREAD OPERATIONS

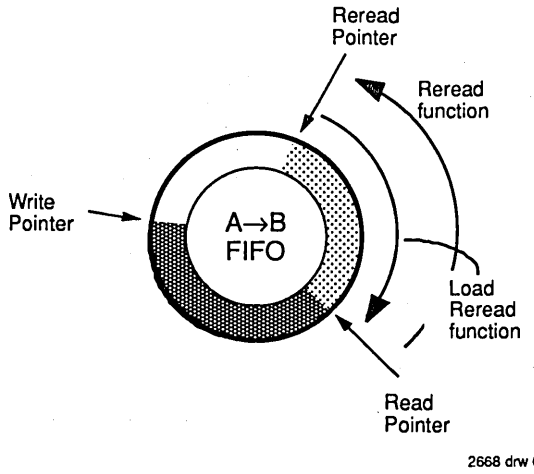


Figure 6. BIFIFO Reread Operations

REWRITE OPERATIONS

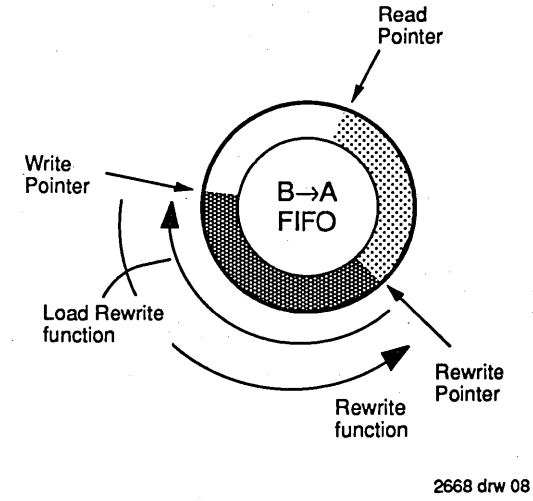


Figure 7. BIFIFO Rewrite Operations

6

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage With Respect To Ground	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2668 tbl 15

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input HIGH Voltage Commercial	2.0	—	—	V
V_{IH}	Input HIGH Voltage Military	2.2	—	—	V
V_{IL}(1)	Input LOW Voltage Commercial and Military	—	—	0.8	V

NOTE: 2668 tbl 16

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	IDT72511L IDT72521L Commercial t_A = 35, 50, 80ns			IDT72511L IDT72521L Military t_A = 40, 50, 80ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{IL}(1)	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	µA
I_{OL}(2)	Output Leakage Current	-10	—	10	-10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = -1mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4mA	—	—	0.4	—	—	0.4	V
I_{CC1}(3)	Average VCC Power Supply Current	—	150	230	—	180	250	mA
I_{CC2}(3)	Average Standby Current ($\overline{R}_B$ = $\overline{W}_B$ = $\overline{DS}_A$ = V_{IH})	—	8	12	—	12	25	mA
I_{CC3}(3)	Power Down Current (All Inputs = V_{CC} - 0.2V)	—	—	2	—	—	4	mA

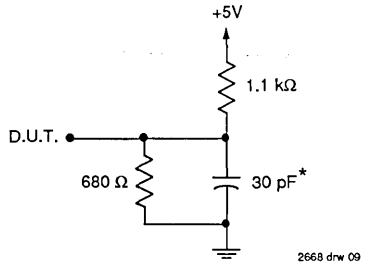
NOTES: 2668 tbl 17

1. Measurements with 0.4V ≤ V_{IN} ≤ V_{CC}, $\overline{DS}_A$ = $\overline{DS}_B$ ≥ V_{IH}
2. Measurements with 0.4V ≤ V_{OUT} ≤ V_{CC}, $\overline{DS}_A$ = $\overline{DS}_B$ ≥ V_{IH}
3. Icc measurements are made with outputs open.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 8

2668 tbl 18



or Equivalent Circuit

Figure 8. Output Load
*Includes jig and scope capacitances

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN} (2)	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT} (1,2)	Output Capacitance	V_{OUT} = 0V	12	pF

NOTES: 2668 tbl 19

1. With output deselected.
2. Characterized values, not currently tested.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to + 70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to + 125°C)

Symbol	Parameter	Commercial IDT72511L35 IDT72521L35 Min.	Max.	Military IDT72511L40 IDT72521L40 Min.	Max.	Commercial and Military IDT72511L50 IDT72521L50 Min.	Max.	IDT72511L80 IDT72521L80 Min.	Max.	Unit	Timing Figure
RESET TIMING (Port A and Port B)											
t_{RSC}	Reset cycle time	45	—	50	—	65	—	100	—	ns	9
t_{RS}	Reset pulse width	35	—	40	—	50	—	80	—	ns	9
t_{RSS}	Reset set-up time	35	—	40	—	50	—	80	—	ns	9
t_{RSR}	Reset recovery time	10	—	10	—	15	—	20	—	ns	9
t_{RSF}	Flag reset pulse width	—	45	—	50	—	65	—	100	ns	9
PORT A TIMING											
t_{aA}	Port A access time	—	35	—	40	—	50	—	80	ns	12, 14, 15
t_{aLZ}	Read or write pulse LOW to data bus at low Z	5	—	5	—	5	—	10	—	ns	12, 15, 16
t_{aHZ}	Read or write pulse HIGH to data bus at high Z	—	20	—	25	—	30	—	30	ns	12, 14, 15, 16
t_{aDV}	Data valid from read pulse HIGH	5	—	5	—	5	—	5	—	ns	12, 14, 16
t_{aRC}	Read cycle time	45	—	50	—	65	—	100	—	ns	12
t_{aRPW}	Read pulse width	35	—	40	—	50	—	80	—	ns	12, 14, 15
t_{aRR}	Read recovery time	10	—	10	—	15	—	20	—	ns	12
t_{aS}	$\overline{CS}_A$, A_0, A_1, $R/\overline{W}_A$ set-up time	5	—	5	—	5	—	10	—	ns	10, 12, 16
t_{aH}	$\overline{CS}_A$, A_0, A_1, $R/\overline{W}_A$ hold time	5	—	5	—	5	—	10	—	ns	10, 12
t_{aDS}	Data set-up time	18	—	20	—	30	—	40	—	ns	11, 12, 14, 15
t_{aDH}[1]	Data hold time	0	—	0	—	5	—	10	—	ns	11, 12, 14, 15
t_{aWC}	Write cycle time	45	—	50	—	65	—	100	—	ns	12
t_{aWPW}	Write pulse width	35	—	40	—	50	—	80	—	ns	11, 12, 14
t_{aWR}	Write recovery time	10	—	10	—	15	—	20	—	ns	12
t_{aWRCOM}	Write recovery time after a command	35	—	40	—	50	—	80	—	ns	11

NOTE:

2668 tbl 20

1. The minimum data hold time is 5ns (10ns for the 80ns speed grade) when writing to the Command, Status or Configuration registers.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to + 70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to + 125°C)

Symbol	Parameter	Commercial IDT72511L35 IDT72521L35 Min.	Max.	Military IDT72511L40 IDT72521L40 Min.	Max.	Commercial and Military IDT72511L50 IDT72521L50 Min.	Max.	IDT72511L80 IDT72521L80 Min.	Max.	Unit	Timing Figure
PORT B PROCESSOR INTERFACE TIMING											
t_{BA}	Port B access time	—	35	—	40	—	50	—	80	Z	13, 14, 15
t_{BLZ}	Read or write pulse LOW to data bus at low Z	5	—	5	—	5	—	10	—	ns	13, 14, 15
t_{BHZ}	Read or write pulse HIGH to data bus at high Z	—	20	—	25	—	30	—	30	ns	14, 13, 15
t_{BDV}	Data valid from read pulse HIGH	5	—	5	—	5	—	10	—	ns	13, 14, 15, 16
t_{BRC}	Read cycle time	45	—	50	—	65	—	100	—	ns	13
t_{BRPW}	Read pulse width	35	—	40	—	50	—	80	—	ns	13
t_{BRR}	Read recovery time	10	—	10	—	15	—	20	—	ns	13
t_{BS}	R/$\overline{W}_B$ set-up time	5	—	5	—	5	—	10	—	ns	13
t_{BH}	R/$\overline{W}_B$ hold time	5	—	5	—	5	—	10	—	ns	13
t_{BDS}	Data set-up time	18	—	20	—	30	—	40	—	ns	13, 14, 15
t_{BDH}	Data hold time	0	—	0	—	5	—	10	—	ns	13, 14, 15
t_{BWC}	Write cycle time	45	—	50	—	65	—	100	—	ns	13
t_{BWPW}	Write pulse width	35	—	40	—	50	—	80	—	ns	13, 15
t_{BWR}	Write recovery time	10	—	10	—	15	—	20	—	ns	13
PORT B PERIPHERAL INTERFACE TIMING											
t_{BCKC}	Clock cycle time	20	—	20	—	25	—	40	—	ns	17
t_{BCKH}	Clock pulse HIGH time	6	—	8	—	10	—	16	—	ns	17
t_{BCKL}	Clock pulse LOW time	6	—	8	—	10	—	16	—	ns	17
t_{BREQS}	Request set-up time	5	—	5	—	10	—	10	—	ns	17
t_{BREQH}	Request hold time	5	—	5	—	5	—	5	—	ns	17
t_{BACKL}	Delay from a rising clock edge to ACK switching	—	18	—	20	—	25	—	35	ns	17

2668 tbl 21

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to + 70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to + 125°C)

Symbol	Parameter	Commercial IDT72511L35 IDT72521L35 Min.	Max.	Military IDT72511L40 IDT72521L40 Min.	Max.	Commercial and Military IDT72511L50 IDT72521L50 Min.	Max.	IDT72511L80 IDT72521L80 Min.	Max.	Unit	Timing Figure
PORT B RETRANSMIT TIMING											
t_{BDSBH}	$\overline{RER}$, $\overline{REW}$, LDRER, LDREW set-up and recovery time	10	—	10	—	15	—	15	—	ns	9, 18
PROGRAMMABLE I/O TIMING											
t_{PIOA}	Programmable I/O access time	—	25	—	25	—	30	—	30	ns	19
t_{PIOS}	Programmable I/O set-up time	5	—	5	—	10	—	10	—	ns	19
t_{PIOH}	Programmable I/O hold time	5	—	5	—	10	—	10	—	ns	19
BYPASS TIMING											
t_{BYA}	Bypass access time	—	20	—	25	—	30	—	40	ns	16
t_{BYD}	Bypass delay	—	15	—	17	—	20	—	30	ns	16
t_{BYDV}	Bypass data valid time	20	—	20	—	20	—	20	—	ns	16
FLAG TIMING											
t_{REF}	Read clock edge to Empty Flag asserted	—	35	—	35	—	45	—	60	ns	14, 15, 20, 22
t_{WEF}	Write clock edge to Empty Flag not asserted	—	35	—	35	—	45	—	60	ns	14, 15, 20, 22
t_{RFF}	Read clock edge to Full Flag not asserted	—	35	—	35	—	45	—	60	ns	14, 15, 21, 23
t_{WFF}	Write clock edge to Full Flag asserted	—	35	—	35	—	45	—	60	ns	14, 15, 21, 23
t_{RAEF}	Read clock edge to Almost-Empty Flag asserted	—	50	—	50	—	60	—	75	ns	20, 22
t_{WAEF}	Write clock edge to Almost-Empty Flag not asserted	—	50	—	50	—	60	—	75	ns	20, 22
t_{RAFF}	Read clock edge to Almost-Full Flag not asserted	—	50	—	50	—	60	—	75	ns	21, 23
t_{WAFF}	Write clock edge to Almost-Full Flag asserted	—	50	—	50	—	60	—	75	ns	21, 23

NOTES:

2668 tbl 22

1. Read and write are internal signals derived from $\overline{DS_A}$, $R/\overline{W_A}$, $\overline{DS_B}$, $R/\overline{W_B}$, $\overline{R_B}$, and $\overline{W_B}$.
2. Although the flags, Empty, Almost-Empty, Almost-Full, and Full Flags are internal flags, the timing given is for those assigned to external pins.

6

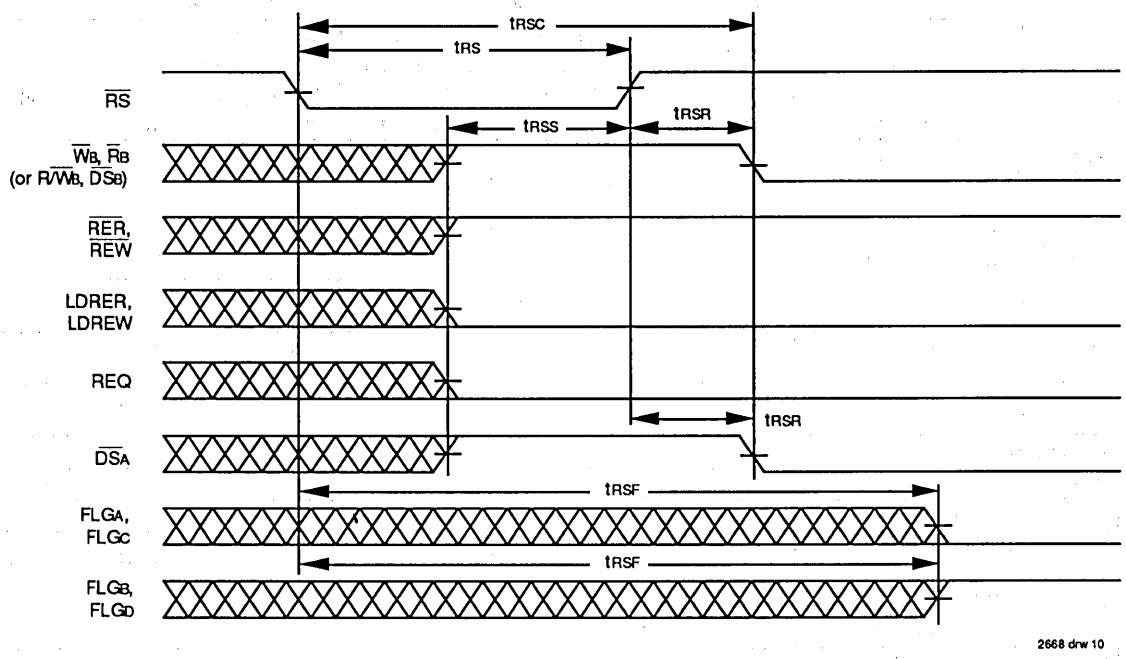


Figure 9. Hardware Reset Timing

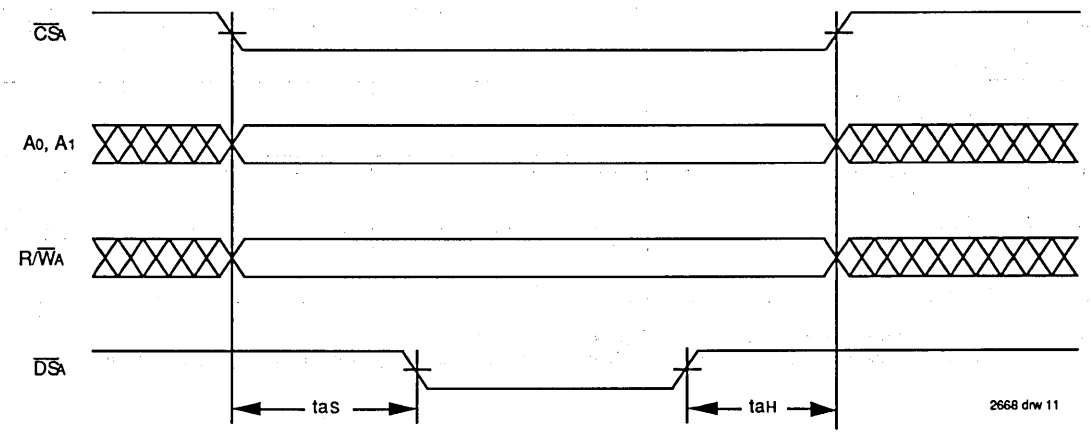


Figure 10. Basic Port A Control Signal Timing (Applies to All Port A Timing)

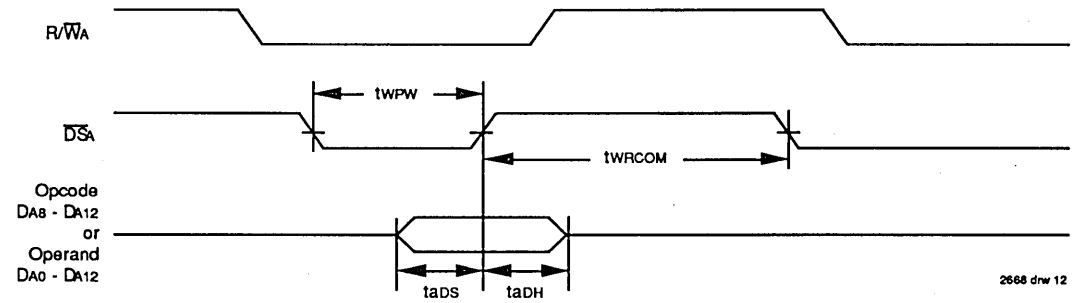


Figure 11. Port A Command Timing (write).

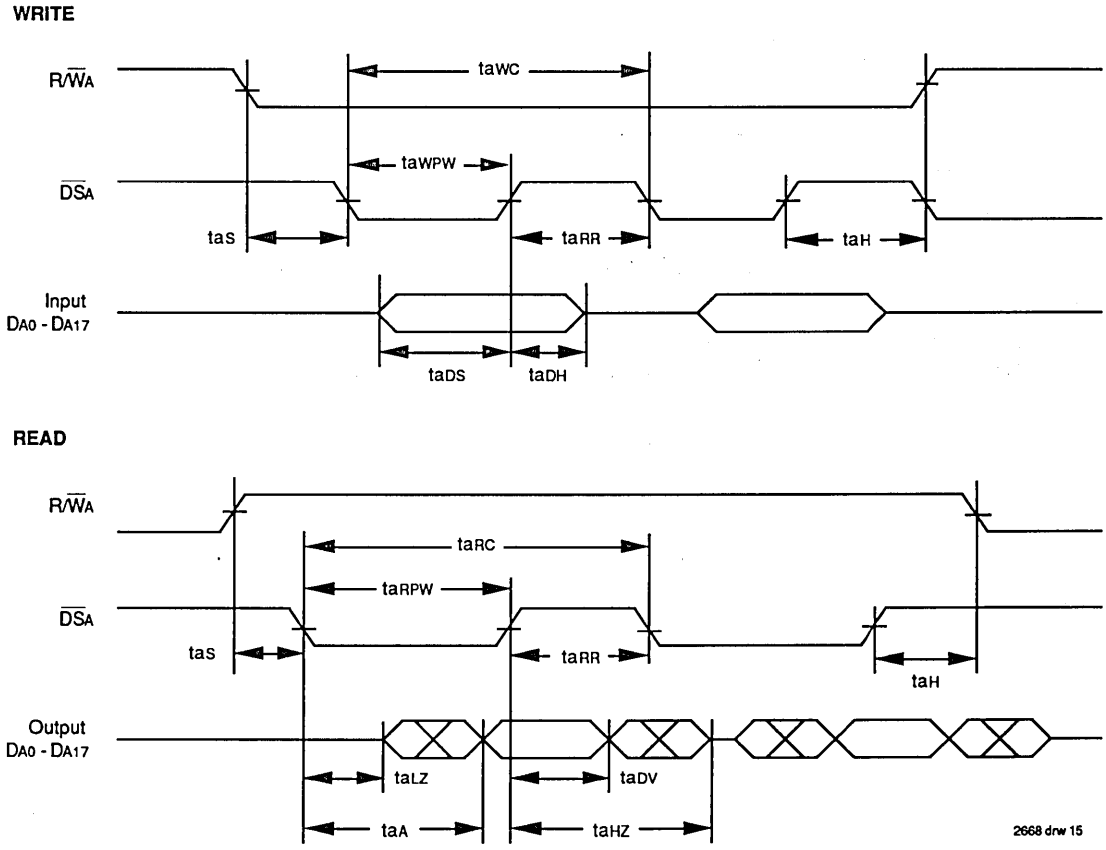
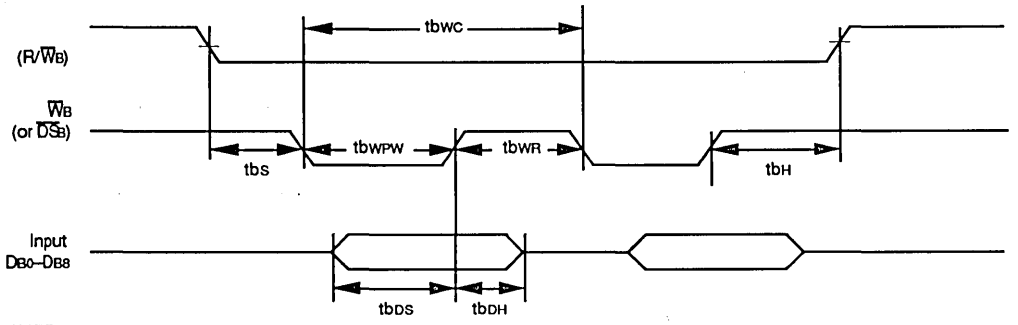


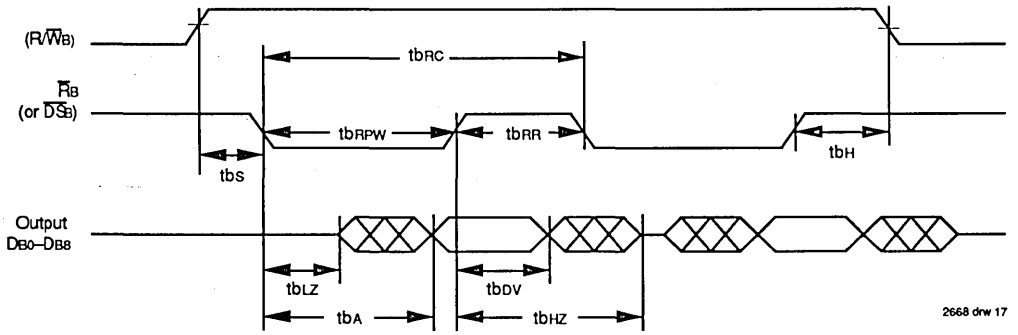
Figure 12. Read and Write Timing for Port A

WRITE



NOTE:
1. $\overline{F}_B$ = 1

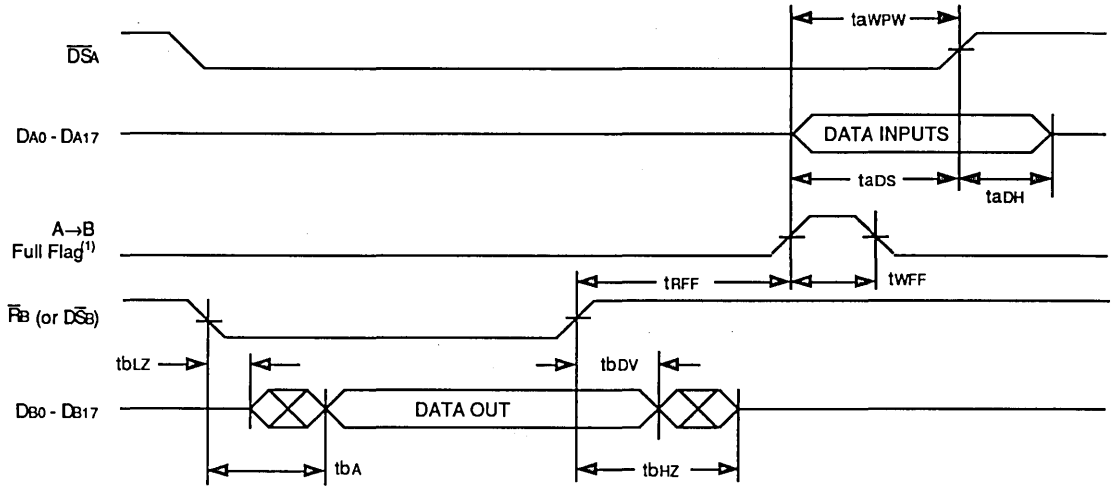
READ



NOTE:
1. $\overline{W}_B$ = 1

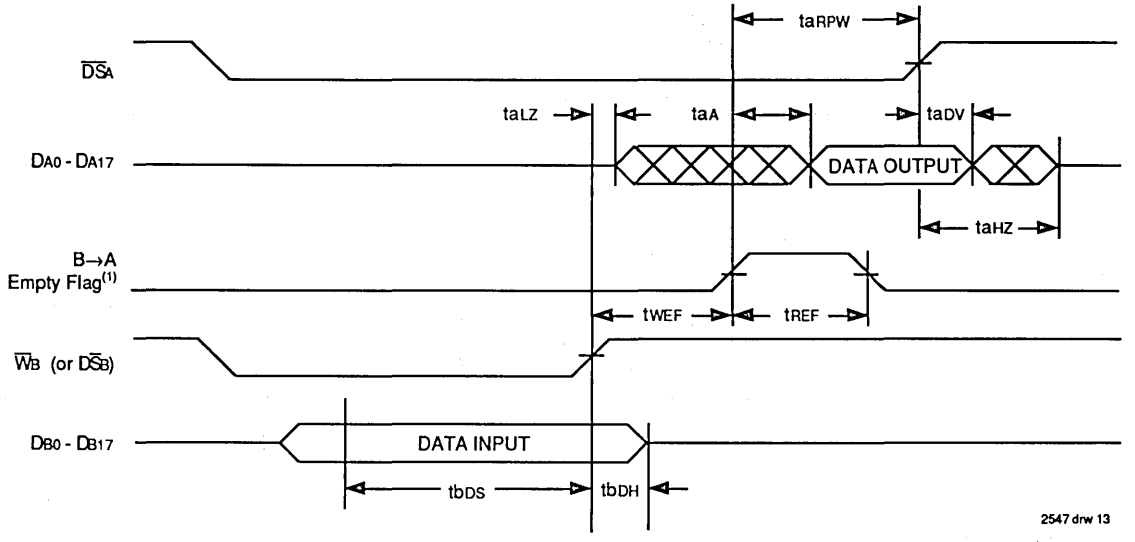
Figure 13. Port B Read and Write Timing, Processor Interface Mode Only

A→B FIFO WRITE FLOW-THROUGH



NOTES:
1. Assume the flag pin is programmed active low.
2. R/$\overline{W}$A = 0

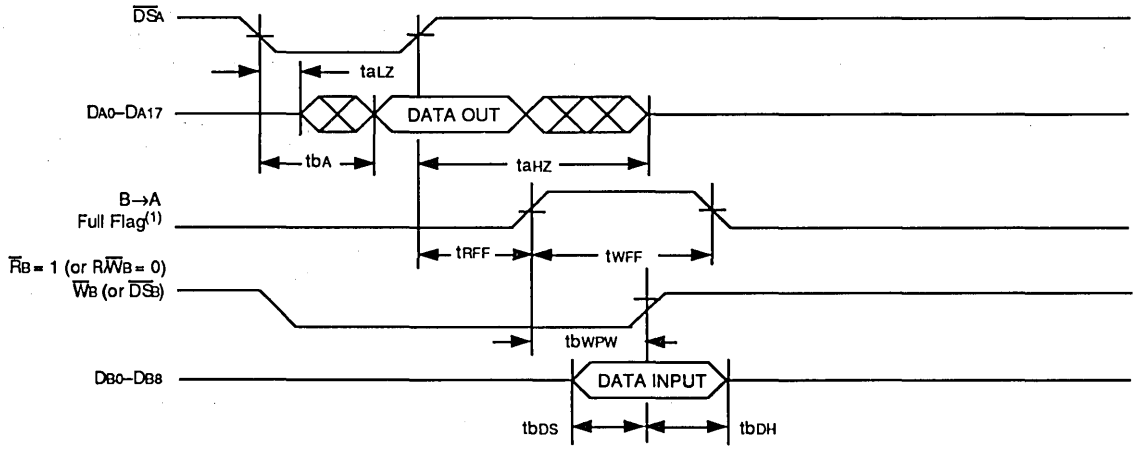
B→A FIFO READ FLOW-THROUGH



NOTES:
1. Assume the flag pin is programmed active low.
2. R/$\overline{W}$A = 1

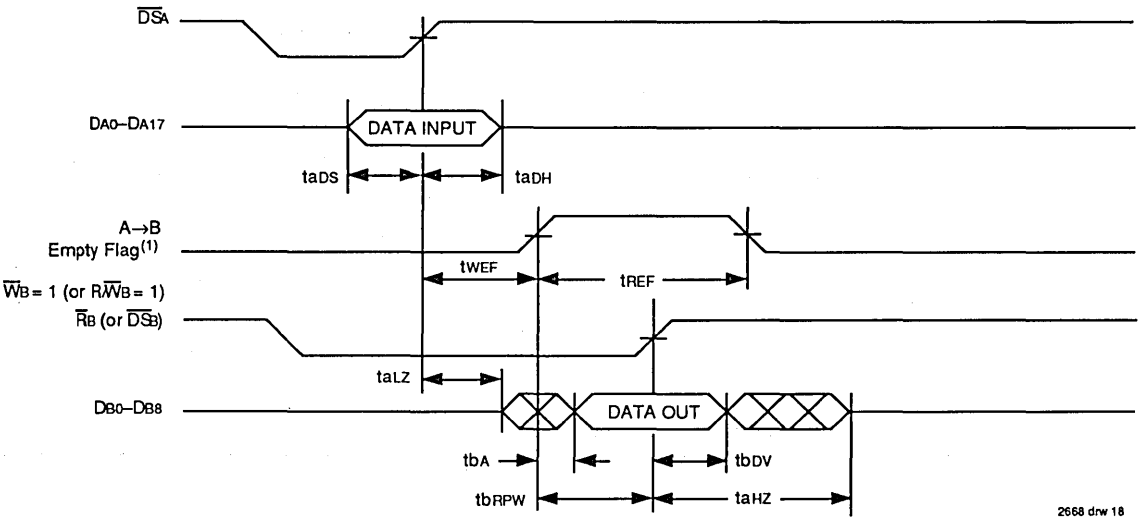
Figure 14. Port A Read and Write Flow-Through Timing, Processor Interface Mode Only

B→A FIFO WRITE FLOW-THROUGH



NOTES:
1. Assume the flag pin is programmed active low.
2. R/$\overline{W}_A$ = 1

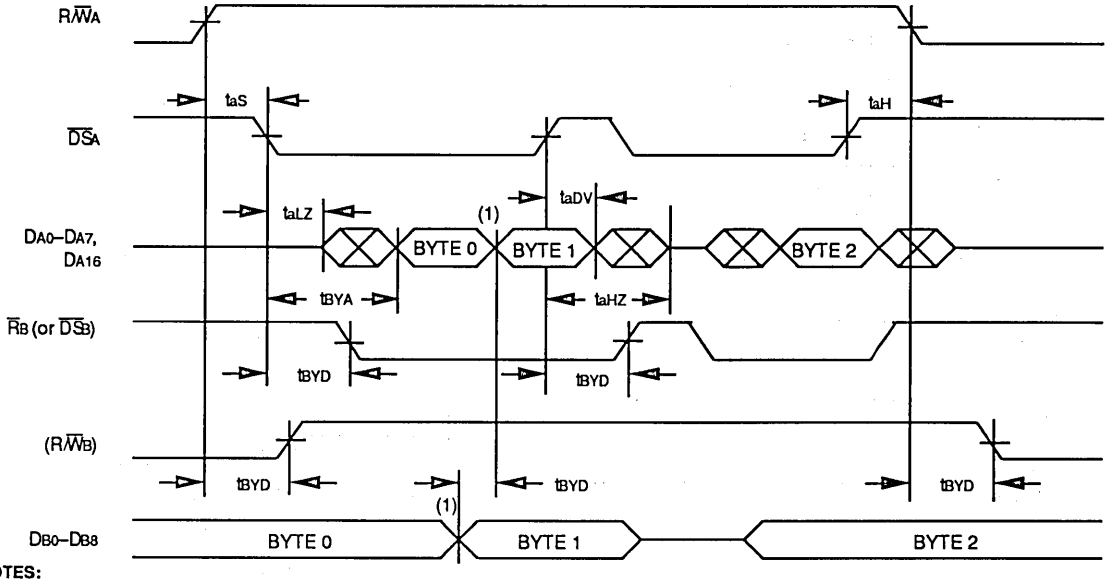
A→B FIFO READ FLOW-THROUGH



NOTES:
1. Assume the flag pin is programmed active low.
2. R/$\overline{W}_A$ = 0

Figure 15. Port B Read and Write Flow-Through Timing, Processor Interface Mode Only

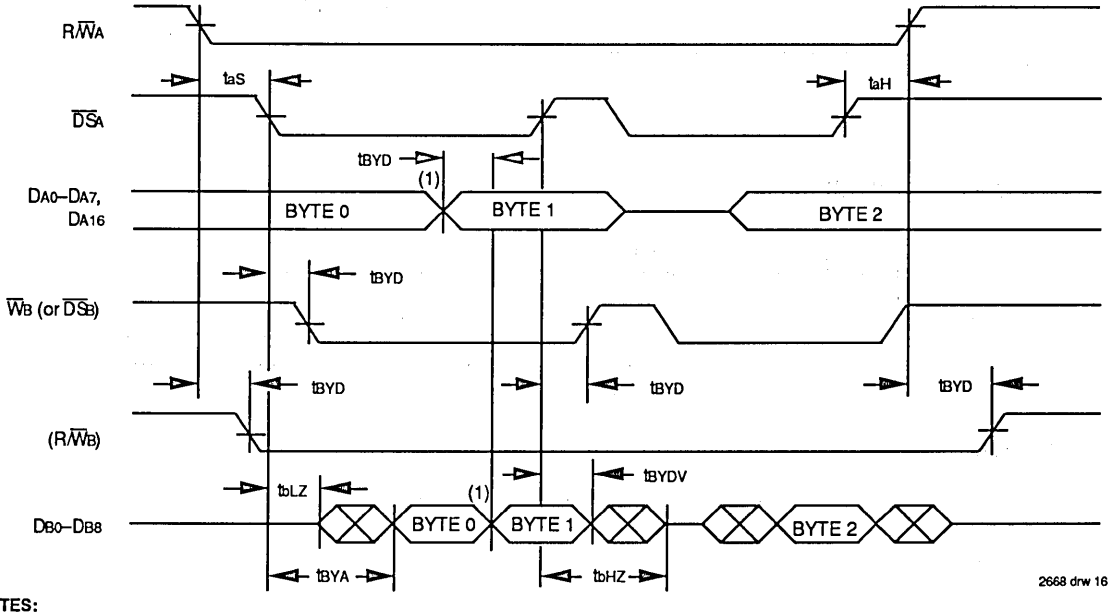
B→A READ BYPASS



NOTES:

1. Once the bypass mode starts, any data change on Port B bus (Byte 0 → Byte 1) will be passed to Port A bus.
2. $\overline{W}_B$ = 1

A→B WRITE BYPASS

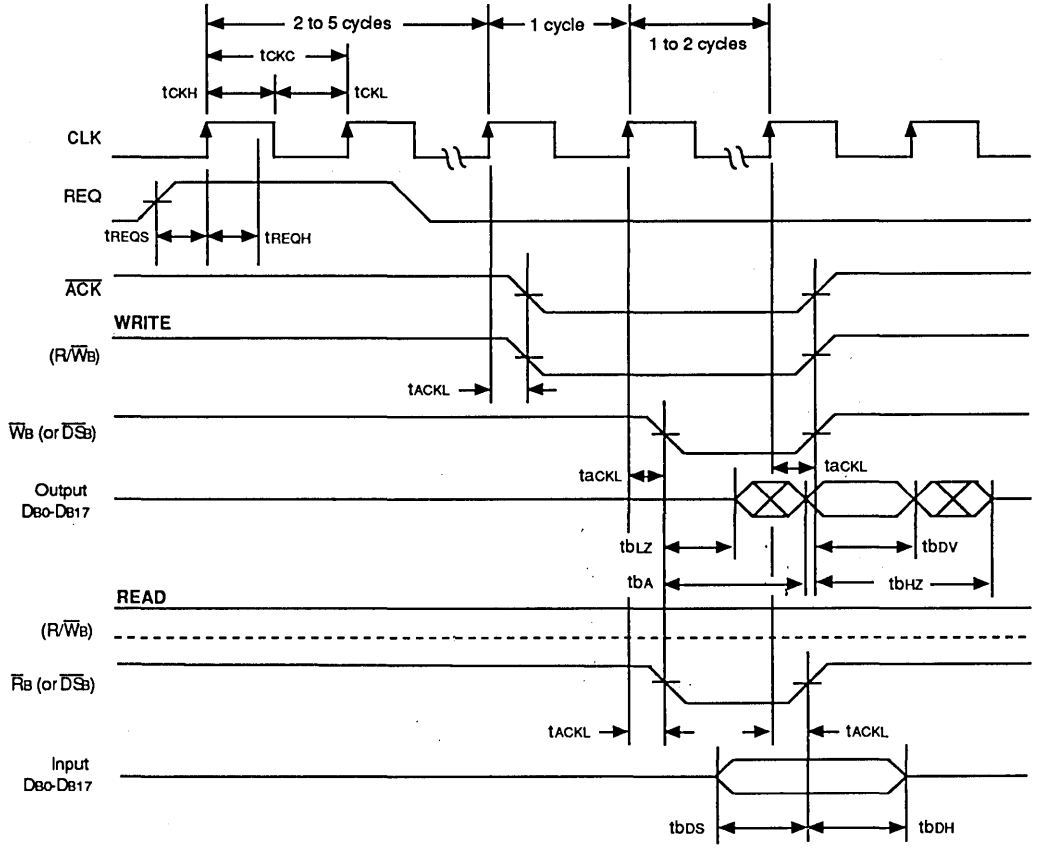


NOTES:

1. Once the bypass mode starts, any data change on Port A bus (Byte 0 → Byte 1) will be passed to Port B bus.
2. $\overline{R}_B$ = 1

Figure 16. Bypass Path Timing, BiFIFO Must Be In Peripheral Interface Mode

SINGLE WORD DMA TRANSFER



BLOCK DMA TRANSFER

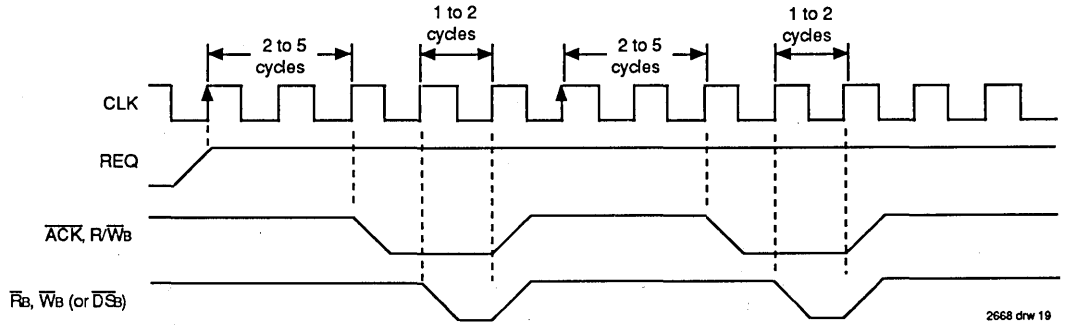


Figure 17. Port B Read and Write DMA timing. Peripheral Interface Mode Only

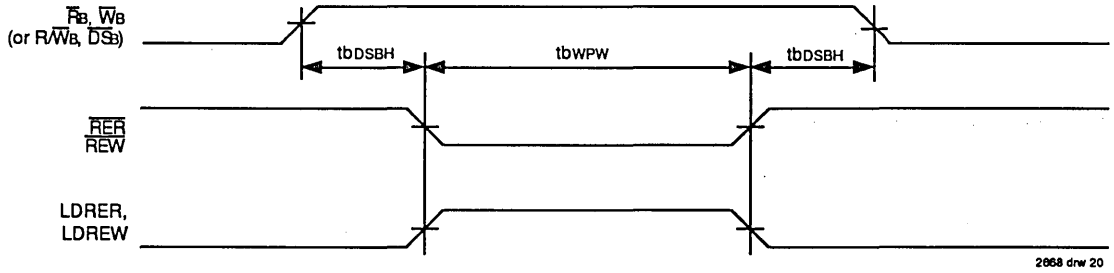
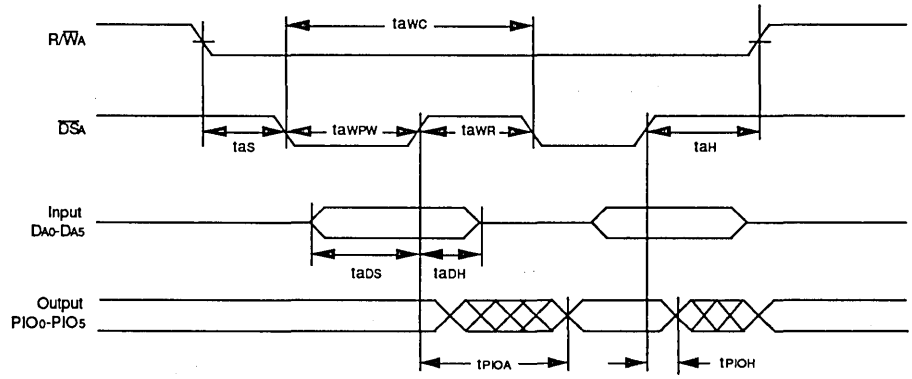


Figure 18. Port B Reread and Rewrite Timing for Intelligent Reread/Rewrite

Port A →PIO WRITE



PIO →Port A READ

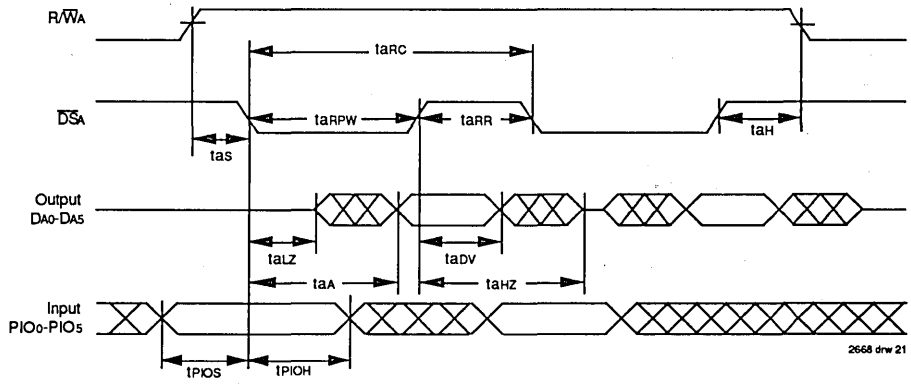
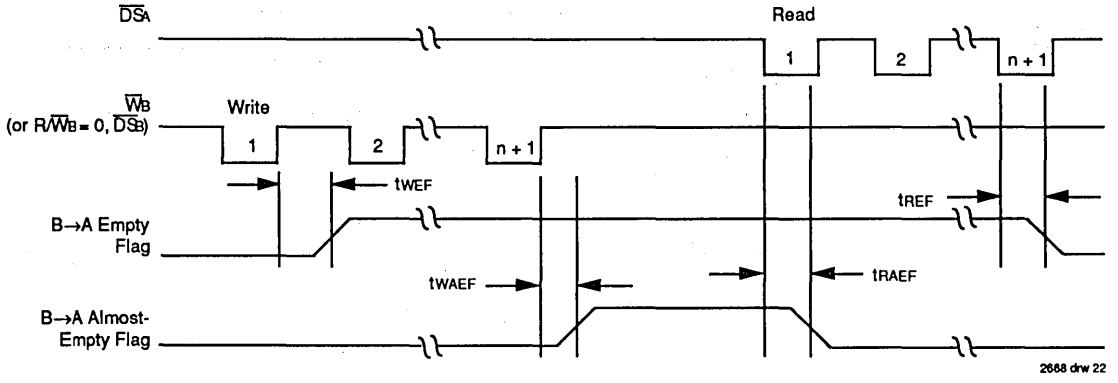
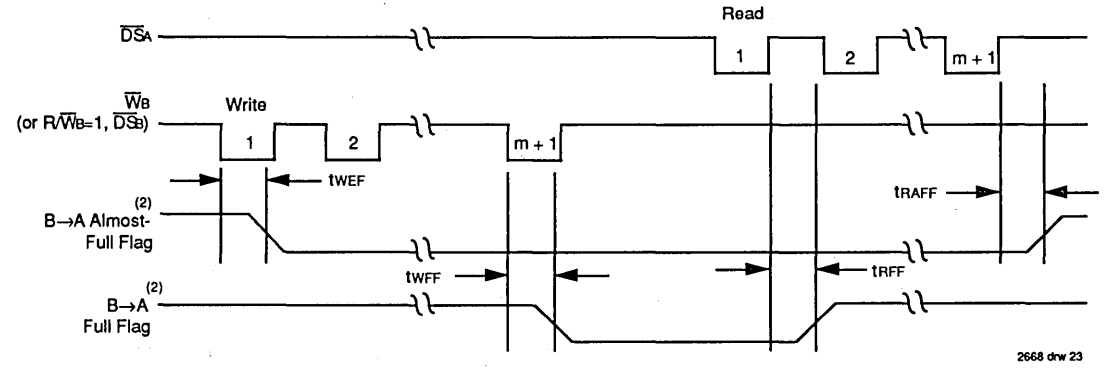


Figure 19. Programmable I/O Timing



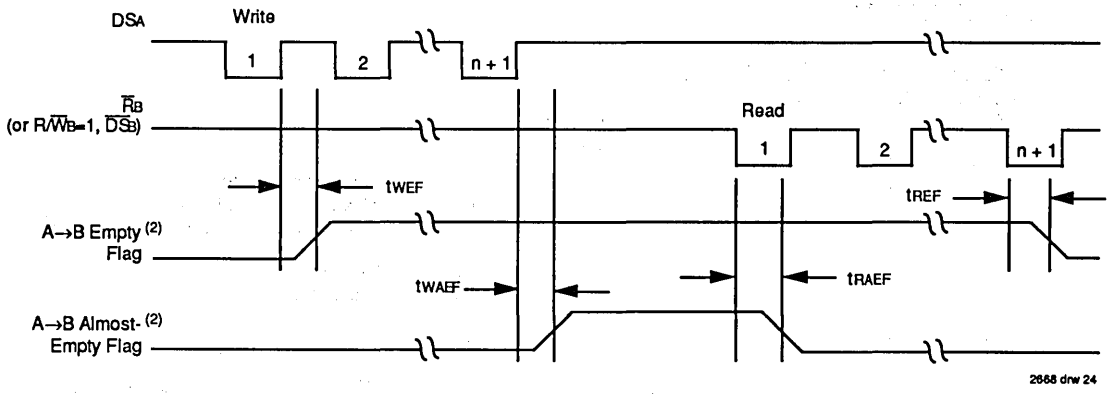
NOTES:
1. B→A FIFO is initially empty.
2. Assume the flag pins are programmed active low.
3. R/$\overline{W}_A$ = 1

Figure 20. Empty and Almost-Empty Flag Timing for B→A FIFO, (n = programmed offset)



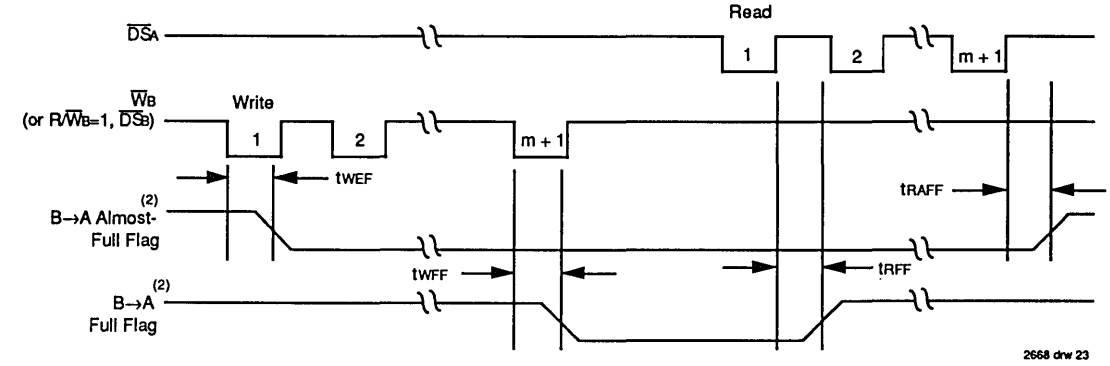
NOTES:
1. B→A FIFO initially contains D − (M + 1) data words. D = 512 for IDT72511; D = 1024 for IDT72521.
2. Assume the flag pins are programmed active low.
3. R/$\overline{W}_A$ = 1

Figure 21. Full and Almost-Full Flag Timing for B→A FIFO, (m = programmed offset)



NOTES:
1. A→B FIFO is initially empty.
2. Assume the flag pins are programmed active low.
3. RWA = 1

Figure 22. Empty and Almost-Empty Flag Timing for A→B FIFO, (n = programmed offset)

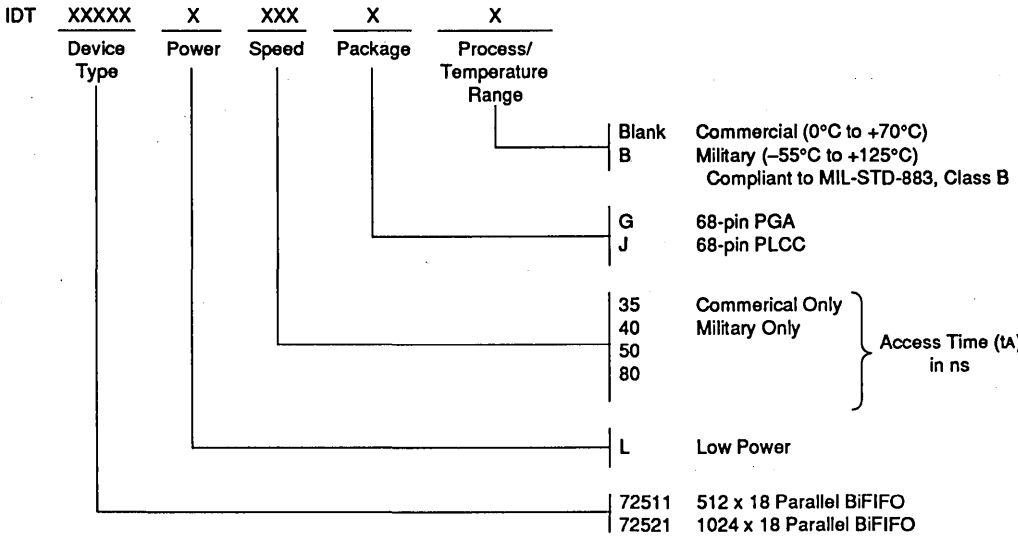


NOTES:
1. B→A FIFO initially contains D − (M + 1) data words. D = 512 for IDT72511; D = 1024 for IDT72521.
2. Assume the flag pins are programmed active low.
3. RWA = 1

Figure 23. Full and Almost-Full Flag Timing for A→B FIFO, (m = programmed offset)

6

ORDERING INFORMATION



2668 drw 26

Integrated Device Technology, Inc.

PARALLEL SyncBiFIFO™ (CLOCKED BIDIRECTIONAL FIFO) 256 x 18-BIT AND 512 x 18-BIT

PRELIMINARY
IDT72605
IDT72615

FEATURES:

- Two independent FIFO memories for fully bidirectional data transfers
- 256 x 18 organization (IDT 72605)
- 512 x 18 organization (IDT 72615)
- Synchronous interface for fast (25ns) read and write cycle times
- Each data port has an independent clock and read/write control
- Output enable is provided on each port as a three-state control of the data bus
- Built-in bypass path for direct data transfer between two ports
- Two fixed flags, Empty and Full, for both the A-to-B and the B-to-A FIFO
- Programmable flag offset can be set to any depth in the FIFO
- The synchronous BiFIFO is packaged in a 68-pin PGA and PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72605 and IDT72615 are very high speed, low power bidirectional FIFO memories with synchronous interface for fast read and write cycle times. The SyncBiFIFO™ is a data buffer that can store or retrieve information from two sources simultaneously. Two dual-port FIFO memory arrays are contained in the SyncBiFIFO; one data buffer for each direction.

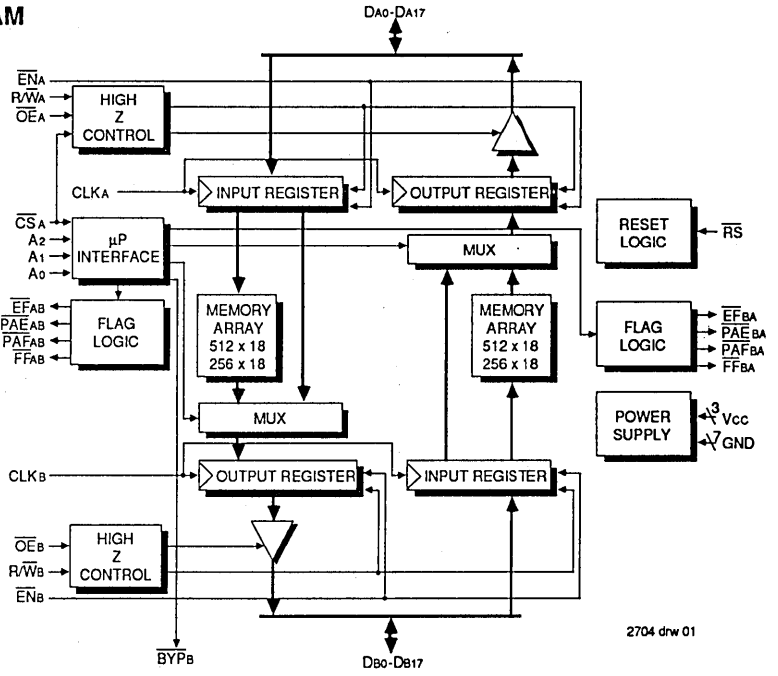
The SyncBiFIFO has registers on all inputs and outputs. Data is only transferred into the I/O registers on clock edges, hence the interfaces are synchronous. Each Port has its own independent clock. Data transfers to the I/O registers are gated by the enable signals. The transfer direction for each port is controlled independently by a read/write signal. Individual output enable signals control whether the SyncBiFIFO is driving the data lines of a port or whether those data lines are in a high impedance state.

Bypass control allows data to be directly transferred from input to output register in either direction.

The SyncBiFIFO has eight flags. The flag pins are full, empty, almost-full, or almost-empty for both FIFO memories. The offset depths of the almost-full and almost-empty flags can be programmed to any location.

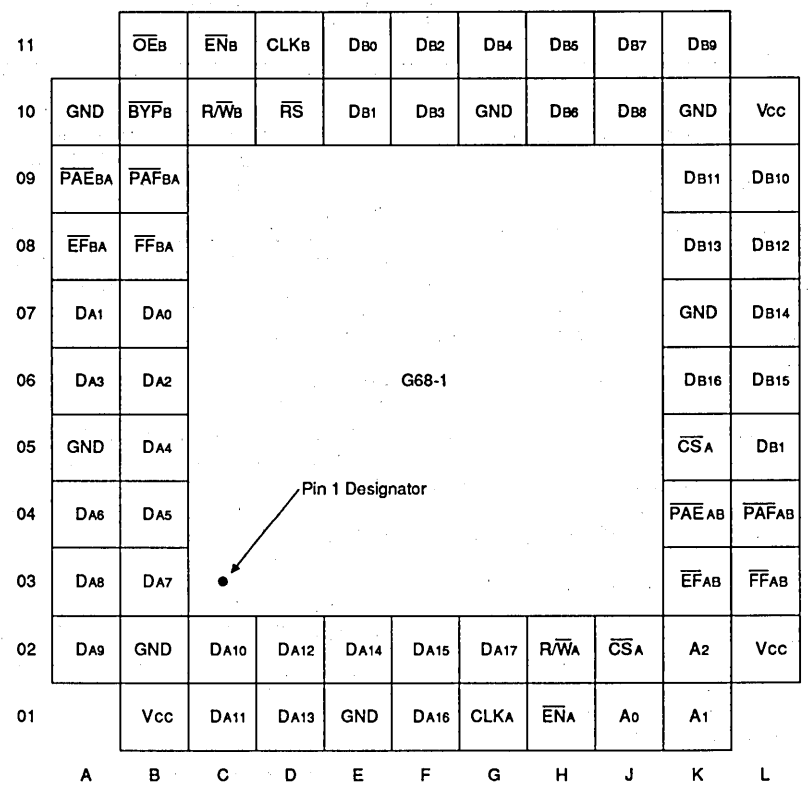
The SyncBiFIFO is fabricated using IDT's high speed submicron CEMOS™ technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



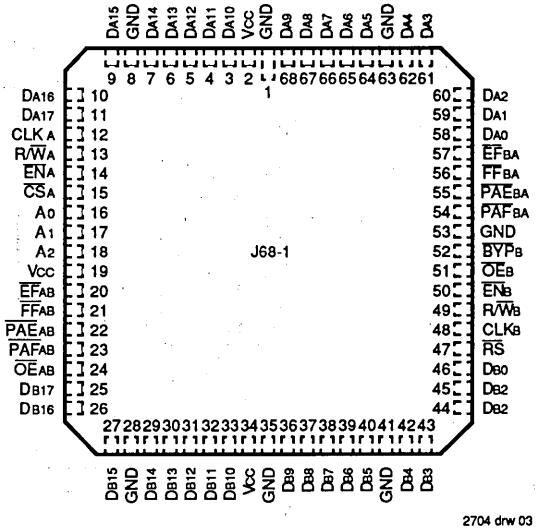
SyncFiFIFO and CEMOS are trademarks of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



2704 drw 02

PGA
Top View



2704 drw 03

PLCC
Top View

PIN DESCRIPTION

Symbol	Name	I/O	Description
D_{A0}-D_{A17}	Data A	I/O	Data inputs & outputs for the 18-bit Port A bus.
$\overline{CS}_A$	Chip Select A	I	Port A is accessed when $\overline{CS}_A$ is LOW. Port A is inactive if $\overline{CS}_A$ is HIGH.
$R/\overline{W}_A$	Read/Write A	I	This pin controls the read or write direction of Port A. If $R/\overline{W}_A$ is LOW, Data A input data is written into Port A. If $R/\overline{W}_A$ is HIGH, Data A output data is read from Port A. In bypass mode, when $R/\overline{W}_A$ is LOW, message is written into A→B output register. If $R/\overline{W}_A$ is HIGH, message is read from B→A output register.
CLK_A	Clock A	I	CLK_A is typically a free running clock. Data is read or written into Port A on the rising edge of CLK_A.
$\overline{EN}_A$	Enable A	I	When $\overline{EN}_A$ is LOW, data can be read or written to Port A. When $\overline{EN}_A$ is HIGH, no data transfers occur.
$\overline{OE}_A$	Output Enable A	I	When $R/\overline{W}_A$ is HIGH , Port A is an output bus and $\overline{OE}_A$ controls the high impedance state of D_{A0}-D_{A17}. If $\overline{OE}_A$ is HIGH, Port A is in a high impedance state. If $\overline{OE}_A$ is LOW while $\overline{CS}_A$ is LOW and $R/\overline{W}_A$ is HIGH, Port A is in an active (low impedance) state.
A_0, A_1, A_2	Addresses	I	When $\overline{CS}_A$ is asserted, A_0, A_1, A_2 and $R/\overline{W}_A$ are used to select one of six internal resources.
D_{B0}-D_{B17}	Data B	I/O	Data inputs & outputs for the 18-bit Port B bus.
$R/\overline{W}_B$	Read/Write B	I	This pin controls the read or write direction of Port B. If $R/\overline{W}_B$ is LOW, Data B input data is written into Port B. If R/W_B is HIGH, Data B output data is read from Port B. In bypass mode, when $R/\overline{W}_B$ is LOW, message is written into A→B output register. If $R/\overline{W}_B$ is HIGH, message is read from B→A output register.
CLK_B	Clock B	I	Clock B is typically a free running clock. Data is read or written into Port B on the rising edge of CLK_B.
$\overline{EN}_B$	Enable B	I	When $\overline{EN}_B$ is LOW, data can be read or written to Port B. When $\overline{EN}_B$ is HIGH, no data transfers occur.
$\overline{OE}_B$	Output Enable B	I	When $R/\overline{W}_B$ is HIGH , Port B is an output bus and $\overline{OE}_B$ controls the high impedance state of D_{B0}-D_{B17}. If $\overline{OE}_B$ is HIGH, Port B is in a high impedance state. If $\overline{OE}_B$ is LOW while $R/\overline{W}_B$ is HIGH, Port B is in an active (low impedance) state.
$\overline{EF}_{AB}$	A→B Empty Flag	O	When $\overline{EF}_{AB}$ is LOW, the A→B FIFO is empty and further data reads from Port B are inhibited. When $\overline{EF}_{AB}$ is HIGH, the FIFO is not empty. $\overline{EF}_{AB}$ is synchronized to CLK_B. In the bypass mode, $\overline{EF}_{AB}$ HIGH indicates that data D_{A0}-D_{A17} is available for passing through. After the data D_{B0}-D_{B17} has been read, $\overline{EF}_{AB}$ goes LOW.
$\overline{PAE}_{AB}$	A→B Programmable Almost-Empty Flag	O	When $\overline{PAE}_{AB}$ is LOW, the A→B FIFO is almost empty. An almost empty FIFO contains less than or equal to the offset programmed into $\overline{PAE}_{AB}$ Register. When $\overline{PAE}_{AB}$ is HIGH, the A→B FIFO contains more than offset in $\overline{PAE}_{AB}$ Register. The default offset value for $\overline{PAE}_{AB}$ Register is 8. $\overline{PAE}_{AB}$ is synchronized to CLK_B.
$\overline{PAF}_{AB}$	A→B Programmable Almost-Full Flag	O	When $\overline{PAF}_{AB}$ is LOW, the A→B FIFO is almost full. An almost full FIFO contains greater than the FIFO depth minus the offset programmed into $\overline{PAF}_{AB}$ Register. When $\overline{PAF}_{AB}$ is HIGH, the A→B FIFO contains less than or equal to the depth minus the offset in $\overline{PAF}_{AB}$ Register. The default offset value for $\overline{PAF}_{AB}$ Register is 8. $\overline{PAF}_{AB}$ is synchronized to CLK_A.
$\overline{FF}_{AB}$	A→B Full Flag	O	When $\overline{FF}_{AB}$ is LOW, the A→B FIFO is full and further data writes into Port A are inhibited. When $\overline{FF}_{AB}$ is HIGH, the FIFO is not full. $\overline{FF}_{AB}$ is synchronized to CLK_A. In bypass mode, $\overline{FF}_{AB}$ tells Port A that a message is waiting in Port B's output register. If $\overline{FF}_{AB}$ is LOW, a bypass message is in the register. If $\overline{FF}_{AB}$ is HIGH, Port B has read the message and another message can be written into Port A.
$\overline{EF}_{BA}$	B→A Empty Flag	O	When $\overline{EF}_{BA}$ is LOW, the B→A FIFO is empty and further data reads from Port A are inhibited. When $\overline{EF}_{BA}$ is HIGH, the FIFO is not empty. $\overline{EF}_{BA}$ is synchronized to CLK_A. In the bypass mode, $\overline{EF}_{BA}$ HIGH indicates that data D_{B0}-D_{B17} is available for passing through. After the data D_{A0}-D_{A17} has been read, $\overline{EF}_{BA}$ goes LOW on the following cycle.
$\overline{PAE}_{BA}$	B→A Programmable Almost-Empty Flag	O	When $\overline{PAE}_{BA}$ is LOW, the B→A FIFO is almost empty. An almost empty FIFO contains less than or equal to the offset programmed into $\overline{PAE}_{BA}$ Register. When $\overline{PAE}_{BA}$ is HIGH, the B→A FIFO contains more than offset in $\overline{PAE}_{BA}$ Register. The default offset value for $\overline{PAE}_{BA}$ Register is 8. $\overline{PAE}_{BA}$ is synchronized to CLK_A.
$\overline{PAF}_{BA}$	B→A Programmable Almost-Full Flag	O	When $\overline{PAF}_{BA}$ is LOW, the B→A FIFO is almost full. An almost full FIFO contains greater than the FIFO depth minus the offset programmed into $\overline{PAF}_{BA}$ Register. When $\overline{PAF}_{BA}$ is HIGH, the B→A FIFO contains less than or equal to the depth minus the offset in $\overline{PAF}_{BA}$ Register. The default offset value for $\overline{PAF}_{BA}$ Register is 8. $\overline{PAF}_{BA}$ is synchronized to CLK_B.

PIN DESCRIPTION (Continued)

Symbol	Name	I/O	Description
$\overline{FF}_{BA}$	B→A Full Flag	O	When $\overline{FF}_{BA}$ is LOW, the B→A FIFO is full and further data writes into Port B are inhibited. When $\overline{FF}_{BA}$ is HIGH, the FIFO is not full. $\overline{FF}_{BA}$ is synchronized to CLK_B. In bypass mode, $\overline{FF}_{BA}$ tells Port B that a message is waiting in Port A's output register. If $\overline{FF}_{BA}$ is LOW, a bypass message is in the register. If $\overline{FF}_{BA}$ is HIGH, Port A has read the message and another message can be written into Port B.
BYP_B	Port B Bypass Flag	O	This flag informs Port B that the Synchronous BiFIFO is in bypass mode. When BYP_B is LOW, Port A has placed the FIFO into bypass mode. If BYP_B is HIGH, the Synchronous BiFIFO passes data into memory. BYP_B is synchronized to CLK_B.
$\overline{RS}$	Reset	I	A LOW on this pin will perform a reset of all Synchronous BiFIFO functions.
V_{CC}	Power		There are three +5V power pins.
GND	Ground		There are seven Ground pins at 0V.

2704 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2704 tbl 34

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}(1)	Input Low Voltage Commercial and Military	—	—	0.8	V

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

2704 tbl 08

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}(2)	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}(1,2)	Output Capacitance	V_{OUT} = 0V	10	pF

NOTES:
1. With output deselected.
2. Characterized values, not currently tested.

2704 tbl 11

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	IDT72615L IDT72605L Commercial t_{CLK} = 25, 35, 50ns			IDT72615L IDT72605L Military t_{CLK} = 30, 35, 50ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{IL}(1)	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	µA
I_{OL}(2)	Output Leakage Current	-10	—	10	-10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = -2mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA	—	—	0.4	—	—	0.4	V
I_{CC}(3)	Average V_{CC} Power Supply Current	—	—	250	—	—	300	mA

NOTES:
1. Measurements with 0.4V ≤ V_{IN} ≤ V_{CC}.
2. $\overline{OE}$ ≥ V_{IH}; 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Tested with outputs open.

2704 tbl 09

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 2

2704 tbl 10

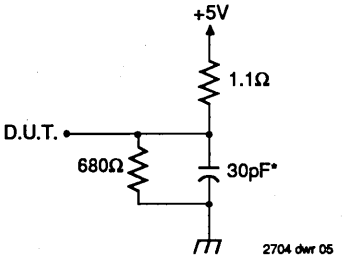


Figure 2. Output Load
* Includes jig and scope capacitances.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V±10%, T_A = -55°C to +125°C)

		Com'l.		Mil.		Com'l. and Mil.					
		IDT72615L25 IDT72605L25		IDT72615L30 IDT72605L30		IDT72615L35 IDT72605L35		IDT72615L50 IDT72605L50			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Timing
f_{CLK}	Clock frequency	—	40	—	33	—	28	—	20	MHz	—
t_{CLK}	Clock cycle time	25	—	30	—	35	—	50	—	ns	4,5,6,7
t_{CLKH}	Clock high time	10	—	12	—	14	—	20	—	ns	4,5,6,7,12,13,14,15
t_{CLKL}	Clock low time	10	—	12	—	14	—	20	—	ns	4,5,6,7,12,13,14,15
t_{RS}	Reset pulse width	25	—	30	—	35	—	50	—	ns	3
t_{RSS}	Reset set-up time	15	—	18	—	21	—	30	—	ns	3
t_{RSF}	Reset to flags in intial state	—	25	—	30	—	35	—	50	ns	3
t_A	Data access time	3	15	3	18	3	21	3	25	ns	5,7,8,9,10,11
t_{CS}	Control signal set-up time(1)	6	—	7	—	8	—	10	—	ns	4,5,6,7,8,9,10,11,12, 13,14,15
t_{CH}	Control signal hold time(1)	1	—	1	—	1	—	1	—	ns	4,5,6,7,10,11,12,13, 14,15
t_{DS}	Data set-up time	6	—	7	—	8	—	10	—	ns	4,6,8,9,10,11
t_{DH}	Data hold time	1	—	1	—	1	—	1	—	ns	4,6
t_{OE}	Output Enable LOW to output data valid(2)	3	13	3	16	3	20	3	28	ns	5,7,8,9,10,11
t_{OLZ}	Output Enable LOW to data bus at low Z(2)	0	—	0	—	0	—	0	—	ns	5,7,8,9,10,11
t_{OHZ}	Output Enable HIGH to data bus at high Z(2)	3	13	3	16	3	20	3	28	ns	5,7,10,11
t_{FF}	Clock to Full Flag time	—	15	—	18	—	21	—	30	ns	4,6,10,11
t_{EF}	Clock to Empty Flag time	—	15	—	18	—	21	—	30	ns	5,7,8,9,10,11
t_{PAE}	Clock to Programmable Almost Empty Flag time	—	15	—	18	—	21	—	30	ns	12,14
t_{PAF}	Clock to Programmable Almost Full Flag time	—	15	—	18	—	21	—	30	ns	13,15
t_{SKEW1}	Skew between CLK_A & CLK_B for Empty/Full Flags	12	—	15	—	17	—	20	—	ns	4,5,6,7,8,9,10,11
t_{SKEW2}	Skew between CLK_A & CLK_B for Programmable Flags	19	—	22	—	25	—	34	—	ns	4, 7,12,13,14,15

2704 tbl 12

NOTES
1. Control signals refer to $\overline{CS}_A$, $R/\overline{W}_A$, $\overline{EN}_A$, A_2, A_1, A_0, $R/\overline{W}_B$, $\overline{EN}_B$.
2. Minimum values are guaranteed by design.

FUNCTIONAL DESCRIPTION

IDT's SyncBiFIFO is versatile for both multiprocessor and peripheral applications. Data can be stored or retrieved from two sources simultaneously.

The SyncBiFIFO has registers on all inputs and outputs. Data is only transferred into the I/O registers on clock edges, hence the interfaces are synchronous. Two dual-port FIFO memory arrays are contained in the SyncBiFIFO; one data buffer for each direction. Each Port has its own independent clock. Data transfers to the I/O registers are gated by the enable signals. The transfer direction for each port is controlled independently by a read/write signal. Individual output enable signals control whether the SyncBiFIFO is driving the data lines of a port or whether those data lines are in a high impedance state. The processor connected to Port A of the BiFIFO can send or receive messages directly to the Port B device using the 18-bit bypass path.

The SyncBiFIFO can be used in multiples of 18-bits. The upper SyncBiFIFO shown in Figures 1 can be used in 18- to 18-bit configurations for processor interface mode. In a 36- to 36-bit configuration, two SyncBiFIFOs operate in parallel. Both devices are programmed simultaneously, 18 data bits to each device. This configuration can be extended to wider bus widths (54- to 54-bits, 72- to 72-bits, etc.) by adding more SyncBiFIFOs to the configuration. Figure 1 show multiple SyncBiFIFOs configured for multiprocessor communication.

The microprocessor or microcontroller connected to Port A controls all operations of the SyncBiFIFO. Thus, all Port A interface pins are inputs driven by the controlling processor. Port B interfaces with a second processor. The Port B control pins are inputs driven by the second processor.

RESET

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. The A→B and B→A FIFO Empty Flags ($\overline{EF}_{AB}$, $\overline{EF}_{BA}$) and Programmable Almost Empty Flags ($\overline{PAE}_{AB}$, $\overline{PAE}_{BA}$) will be set to low after t_{RSF}. The A→B and B→A FIFO Full Flags ($\overline{FF}_{AB}$, $\overline{FF}_{BA}$) and Programmable Almost Full Flags ($\overline{PAF}_{AB}$, $\overline{PAF}_{BA}$) will be set to high after t_{RSF}. After the reset, the offsets of the Almost-Empty Flags and Almost-Full Flags for the A→B and B→A FIFO offset default to 8.

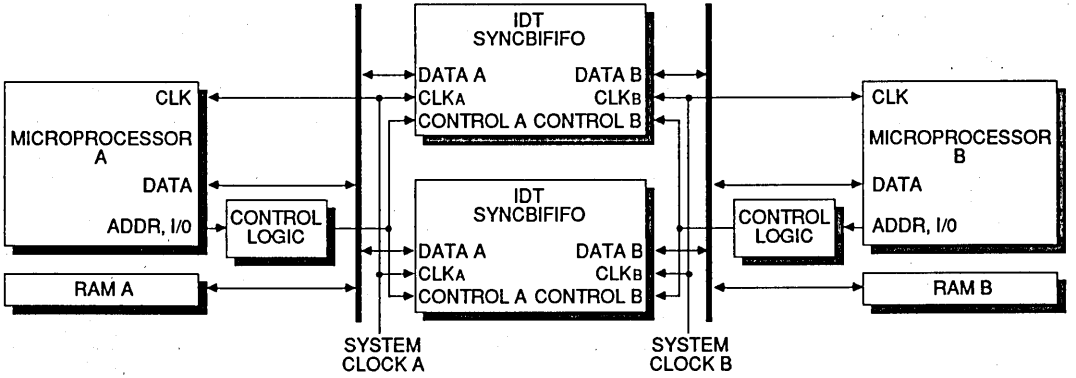
PORT A INTERFACE

The SyncBiFIFO™ is straightforward to use in microprocessor-based systems because each port has a standard microprocessor control set. Port A interfaces with microprocessor through the three address pins (A_2-A_0) and a Chip Select $\overline{CS}_A$ pins. When $\overline{CS}_A$ is asserted, A_2,A_1,A_0 and $R/\overline{W}_A$ are used to select one of six internal resources (Table 1).

With A_2=0 and A_1=0, A_0 determines whether data can be read out of output register or be written into the FIFO (A_0=0), or the data can pass through the FIFO through the bypass path (A_0=1).

With A_2=1, four programmable flags (two A→B FIFO programmable flags and two B→A FIFO programmable flags) can be selected: the A→B FIFO Almost-Empty Flag Offset (A_1=0, A_0=0), A→B FIFO Almost-Full Flag Offset (A_1=0, A_0=1), B→A FIFO Almost-Empty Flag Offset (A_1=1, A_0=0), B→A FIFO Almost-Full Flag Offset (A_1=1, A_0=1).

Port A is disabled when $\overline{CS}_A$ is deasserted and data A is in high impedance state.



NOTES:
1. Upper SyncBiFIFO only is used in 18- to 18-bit configuration.
2. Control A Consists of $R/\overline{W}_A$, $\overline{EN}_A$, $\overline{OE}_A$, $\overline{CS}_A$, A_2, A_1, A_0. Control B consists of $R/\overline{W}_B$, $\overline{EN}_B$, $\overline{OE}_B$.

Figure 1. 36- to 36-bit Processor Interface Configuration

$\overline{CS}_A$	R/$\overline{W}_A$	$\overline{EN}_A$	$\overline{OE}_A$	Data A I/O	Port A Operation
0	0	0	0	I	Data A is written on CLKA ↑. This write cycle immediately following low impedance cycle is prohibited.
0	0	0	1	I	Data A is written on CLKA ↑.
0	0	1	X	I	Data A is ignored
0	1	0	0	O	Data is read(1) from RAM array to output register on CLKA ↑, Data A is low impedance
0	1	0	1	O	Data is read(1) from RAM array to output register on CLKA ↑, Data A is high impedance
0	1	1	0	O	Output register does not change(2), Data A is low impedance
0	1	1	1	O	Output register does not change(2), Data A is high impedance
1	0	X	X	I	Data A is ignored(3)
1	1	X	X	O	Data A is high impedance(3)

NOTES
2704 tbl 02

1. When $A_2A_1A_0$ = 000, the next B→A FIFO value is read out of the output register and the read pointer advances. If $A_2A_1A_0$ = 001, the bypass path is selected and bypass data from the Port B input register is read from the Port A output register. If $A_2A_1A_0$ = 1XX, a flag offset register is selected and its offset is read out through Port A output register.
2. Regardless of the condition of $A_2A_1A_0$, the data in the Port A output register does not change and the B→A read pointer does not advance.
3. If $\overline{CS}_A$ is HIGH, then BYP_B is HIGH. No bypass occur under this condition.

Table 1. Port A Operation Control Signals

BYPASS PATH

The bypass paths provide direct communication between Port A and Port B. There are two full 18-bit bypass paths, one in each direction. During a bypass operation data is passed directly between the input and output registers, the FIFO memory is undisturbed.

Port A initiates and terminates all bypass operations. The bypass flag, BYP_B, is asserted to inform Port B that a bypass operation is beginning. The bypass flag state is controlled by the Port A controls, although the BYPB signal is synchronized to CLK_B. So, BYP_B is asserted on the next rising edge of CLK_B when $A_2A_1A_0$=001. When Port A returns to normal FIFO mode ($A_2A_1A_0$=000), BYP_B is deasserted on the next CLK_B rising edge.

Once the SyncBiFIFO is in bypass mode, all data transfers are controlled by the standard Port A ($\overline{CS}_A$, R/$\overline{W}_A$, CLK_A, $\overline{EN}_A$, $\overline{OE}_A$) and Port B (R/$\overline{W}_B$, CLK_B, $\overline{EN}_B$, $\overline{OE}_B$) interface pins. Each bypass path can be considered as a one word deep FIFO. Data is held in each output register until it is read. Since the controls of each port operates independently, Port A can be reading bypass data at the same time Port B is reading bypass data.

When R/$\overline{W}_A$ and $\overline{EN}_A$ is LOW, data on pins D_{A0}-D_{A17} is written into Port A through the input register. Following the rising edge of CLK_A for this write, the A→B Full Flag ($\overline{FF}_{AB}$) goes LOW. Subsequent writes into Port A are blocked by internal logic until $\overline{FF}_{AB}$ goes HIGH again. On the next CLK_B rising edge, the A→B Empty Flag ($\overline{EF}_{AB}$) goes HIGH indicating to Port B that data is available at its output register. Once R/$\overline{W}_B$ is HIGH and $\overline{EN}_B$ is LOW, data is read into the Port B output register. $\overline{OE}_B$ still controls whether Port B is in a high-impedance state. When $\overline{OE}_B$ is LOW, the output register data appears at D_{B0}-D_{B17}. $\overline{EF}_{AB}$ goes LOW following the CLK_B rising edge for this read. $\overline{FF}_{AB}$ is brought HIGH on the next CLK_A rising edge letting Port A know that another word can be written through the bypass path.

Bypass data transfers from Port B to Port A work in a similar manner with $\overline{EF}_{BA}$, $\overline{FF}_{BA}$ indicating the Port A output register state.

When the Port A address changes from bypass mode ($A_2A_1A_0$=001) to FIFO mode ($A_2A_1A_0$=000) on the rising edge of CLK_A, the data held in the Port B output register may be overwritten. Unless Port A monitors the BYP_B pin and waits for Port B to clock out the last bypass word, data from the A→B FIFO will overwrite data in the Port B output register. BYP_B will go HIGH on the rising edge of CLK_B signifying that Port B has finished its last bypass operation. Port B must read any bypass data in the output register on this last CLK_B clock or it is lost and the SyncBiFIFO returns to FIFO operations. It is especially important to monitor BYP_B when CLK_B is much slower than CLK_A to avoid this condition. BYP_B will also go HIGH after $\overline{CS}_A$ is brought HIGH; in this manner the Port B bypass data in the output register may also be lost.

Since the Port A processor controls $\overline{CS}_A$ and the bypass mode, this scenario can be handled for B→A bypass data. The Port A processor must be set up to read the last bypass word before leaving bypass mode.

PORT A CONTROL SIGNALS

The Port A control signals pins dictate the various operations shown in Table 2. Port A is accessed when $\overline{CS}_A$ is LOW, and is inactive if $\overline{CS}_A$ is HIGH. R/$\overline{W}_A$ and $\overline{EN}_A$ lines determine when Data A can be written or read. If R/$\overline{W}_A$ and $\overline{EN}_A$ are LOW, data is written into input register on the low-to-high transition of CLK_A. If R/$\overline{W}_A$ is HIGH and $\overline{OE}_A$ is LOW, data comes out of bus and is read from output register into three-state buffer. Refer to pin descriptions for more information.

$\overline{CS}_A$	A_2	A_1	A_0	Read	Write
0	0	0	0	B→A FIFO	A→B FIFO
0	0	0	1	18-bit Bypass Path	
0	1	0	0	A→B FIFO Almost-Empty Flag Offset	
0	1	0	1	A→B FIFO Almost-Full Flag Offset	
0	1	1	0	B→A FIFO Almost-Empty Flag Offset	
0	1	1	1	B→A FIFO Almost-Full Flag Offset	
1	X	X	X	Port A Disabled	

2704 tbl 03

Table 2. Accessing Port A Resources Using $\overline{CS}_A$, A_2, A_1, and A_0

PROGRAMMABLE FLAGS

The IDT SyncBiFIFO has eight flags: four flags for A→B FIFO ($\overline{EF}_{AB}$, $\overline{PAE}_{AB}$, $\overline{PAF}_{AB}$, $\overline{FF}_{AB}$), and four flags for B→A FIFO ($\overline{EF}_{BA}$, $\overline{PAE}_{BA}$, $\overline{PAF}_{BA}$, $\overline{FF}_{BA}$). The Empty and Full flags have fixed offsets, while the Almost Empty and Almost Full offsets can be set to any depth through the Flag Offset Registers (see Table 3). The flags are asserted at the depths shown in the Flag Truth Table (Table 4). After reset, the programmable flag offsets are set to 8. This means the Almost Empty flags are asserted at Empty + 8 words deep, and the Almost Full flags are asserted at Full - 8 words deep.

The $\overline{PAE}_{AB}$ is synchronized to CLK_B, while $\overline{PAF}_{AB}$ is synchronized to CLK_A; and $\overline{PAE}_{BA}$ is synchronized to CLK_A, while $\overline{PAF}_{BA}$ is synchronized to CLK_B. If the minimum time (t_{SKEW2}) between a rising CLK_B and a rising CLK_A is met, the flag will change state on the current clock; otherwise, the flag may not change state until the next clock rising edge. For the specific flag timings, refer to Figures 12-15.

	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$\overline{PAE}_{AB}$ Register	X	X	X	X	X	X	X	X	X	A→B FIFO Almost-Empty Flag Offset								
$\overline{PAF}_{AB}$ Register	X	X	X	X	X	X	X	X	X	A→B FIFO Almost-Full Flag Offset								
$\overline{PAE}_{BA}$ Register	X	X	X	X	X	X	X	X	X	B→A FIFO Almost-Empty Flag Offset								
$\overline{PAF}_{BA}$ Register	X	X	X	X	X	X	X	X	X	B→A FIFO Almost-Full Flag Offset								

2704 tbl 04

NOTE:
1. Bit 8 must be set to 0 for the IDT72605 (256 x 18) Synchronous BiFIFO.

Table 3. Flag Offset Register Format

Number of Words In FIFO					
From	To	$\overline{EF}$	$\overline{PAE}$	$\overline{PAF}$	$\overline{FF}$
0	0	Low	Low	High	High
1	n	High	Low	High	High
n+1	D-(m+1)	High	High	High	High
D-m	D-1	High	High	Low	High
D	D	High	High	Low	Low

n = Programmable Empty Offset ($\overline{PAE}_{AB}$ Register or $\overline{PAE}_{BA}$ Register)
m = Programmable Full Offset ($\overline{PAF}_{AB}$ Register or $\overline{PAF}_{BA}$ Register)
D = FIFO Depth (IDT72605 = 256 words, IDT72615= 512 words)

2704 tbl 05

Table 4. Internal Flag Truth Table

PORT B CONTROL SIGNALS

The Port B control signals pins dictate the various operations shown in Table 5. Port B is independent of $\overline{CS}_A$. $R/\overline{W}_B$ and $\overline{EN}_B$ lines determine when Data can be written or read in Port B. If $R/\overline{W}_B$ and $\overline{EN}_B$ are LOW, data is written into input register, and on low-to-high transition of CLK_B data is written into input register and the FIFO memory. If $R/\overline{W}_B$ is HIGH and $\overline{OE}_B$ is LOW, data comes out of bus and is read from output register into three-state buffer. In bypass mode, if $R/\overline{W}_B$ is LOW, bypass messages are transferred into B→A output register. If $R/\overline{W}_A$ is HIGH, bypass messages are transferred into A→B output register. Refer to pin descriptions for more information.

$R/\overline{W}_B$	$\overline{EN}_B$	$\overline{OE}_B$	Data B I/O	Port B Operation
0	0	0	I	Data B is written on CLK_B ↑. This write cycle immediately following output low impedance cycle is prohibited
0	0	1	I	Data B is written on CLK_B ↑.
0	1	X	I	Data B is ignored
1	0	0	O	Data is read(1) from RAM array to output register on CLK_B ↑, Data B is low impedance
1	0	1	O	Data is read(1) from RAM array to output register on CLK_B ↑, Data B is high impedance
1	1	0	O	Output register does not change(2), Data B is low impedance
1	1	1	O	Output register does not change(2), Data B is high impedance

2704 tbl 06

NOTES:

1. When $A_2A_1A_0$ = 000 or 1XX, the next A→B FIFO value is read out of the output register and the read pointer advances. If $A_2A_1A_0$ = 001, the bypass path is selected and bypass data is read from the Port B output register.
2. Regardless of the condition of $A_2A_1A_0$, the data in the Port B output register does not change and the A→B read pointer does not advance.

Table 5. Port B Operation Control Signals

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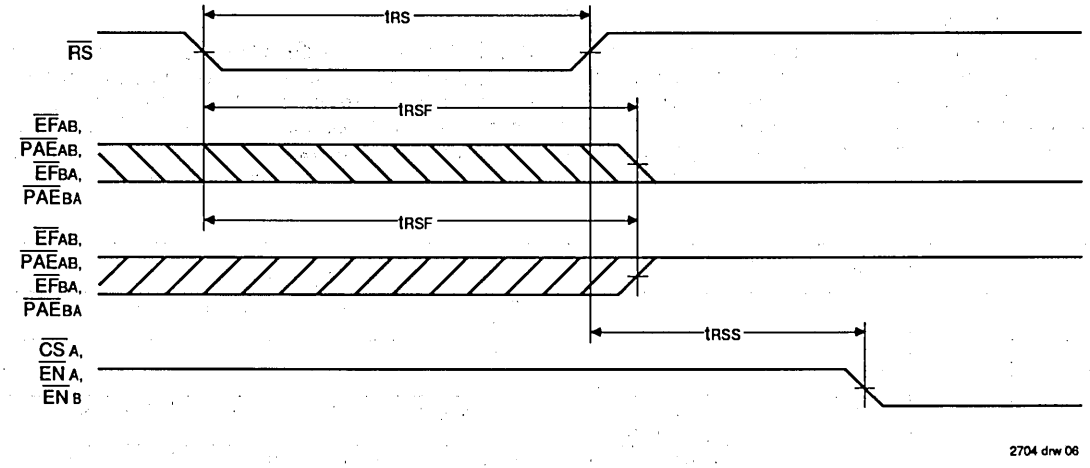


Figure 3. Reset Timing

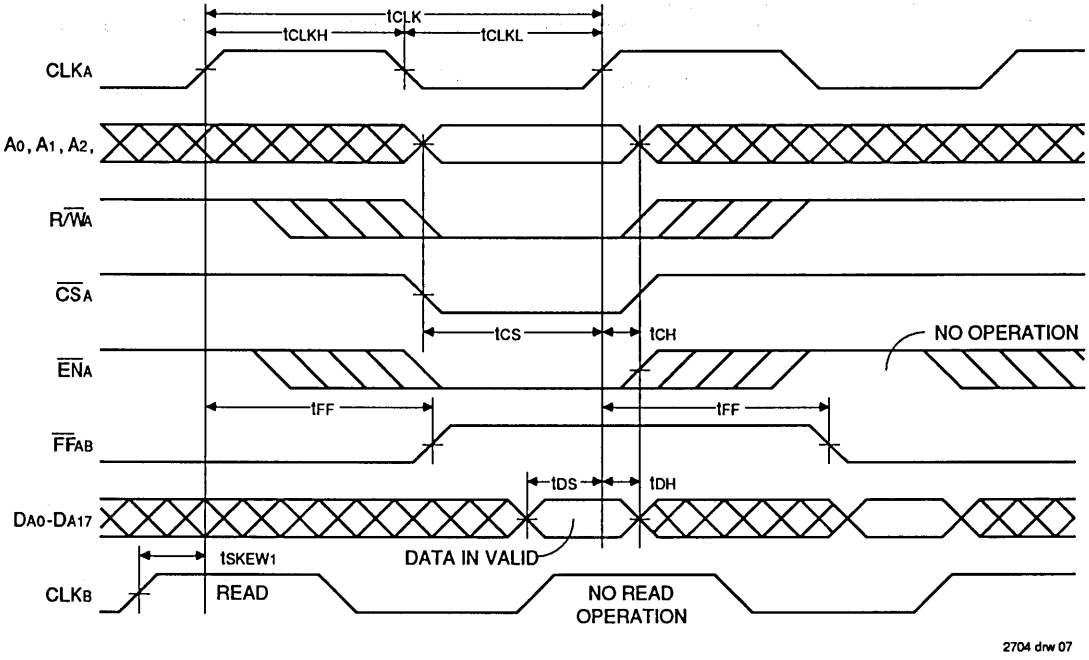


Figure 4. Port A (A→B) Write Timing

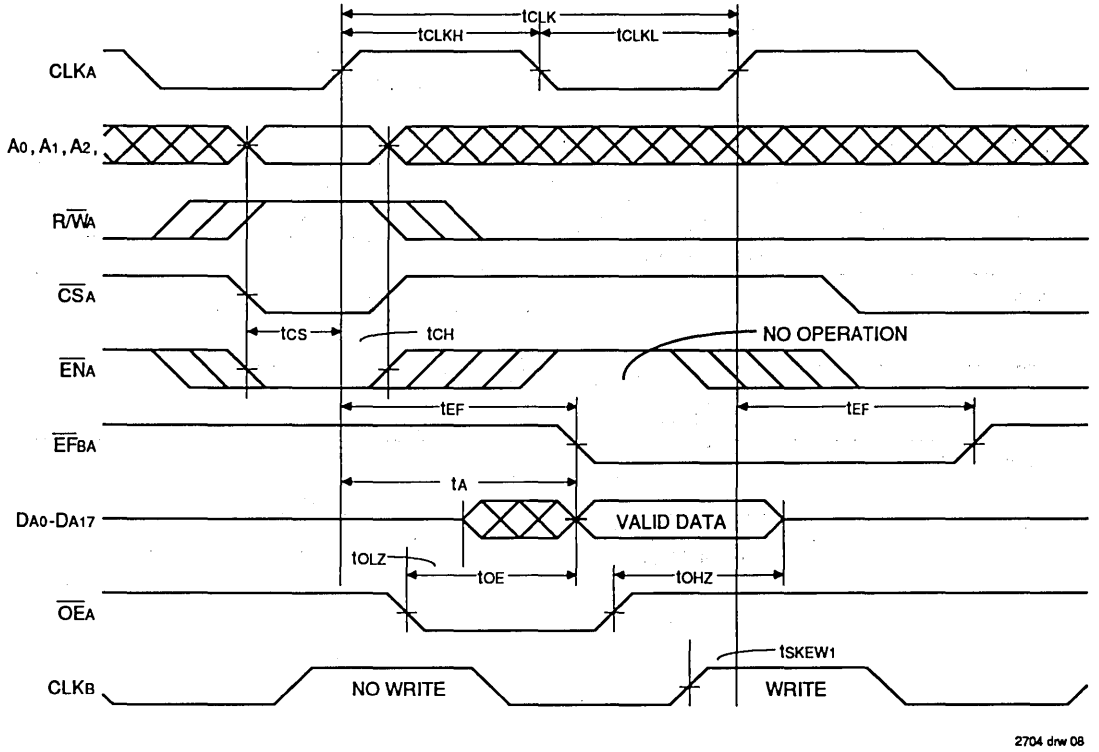


Figure 5. Port A (B→A) Read Timing

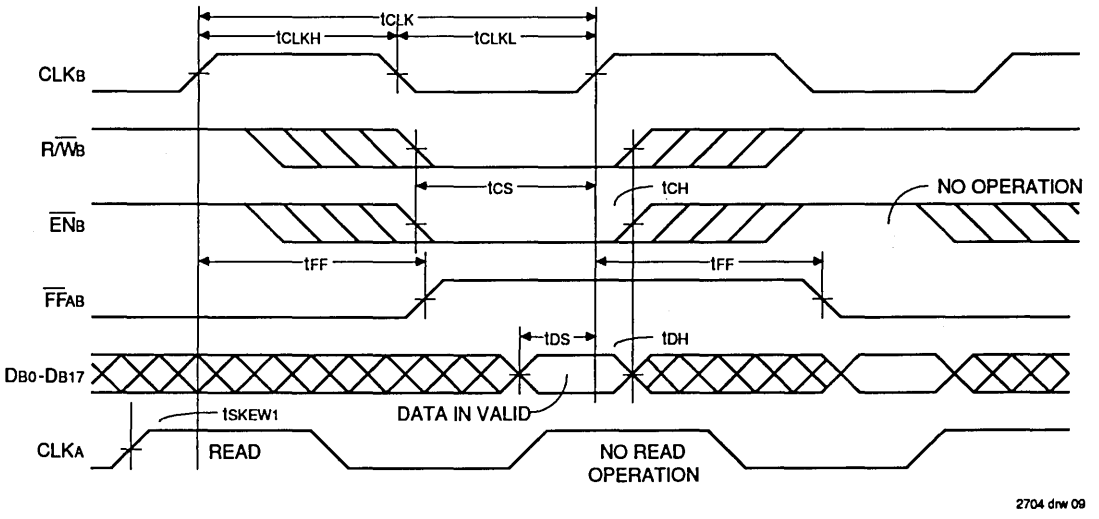


Figure 6. Port B (B→A) Write Timing

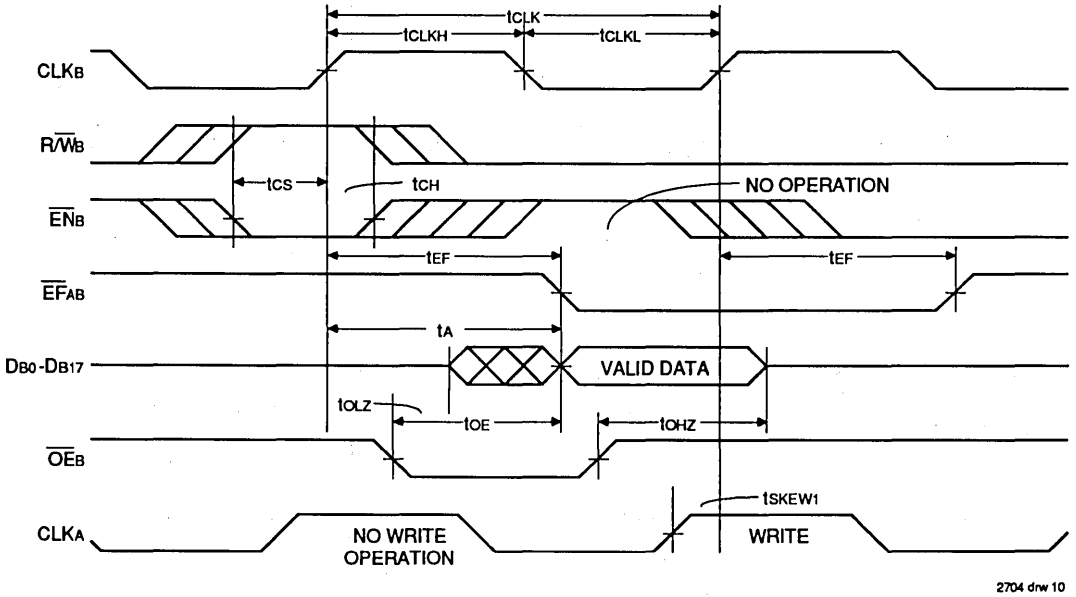
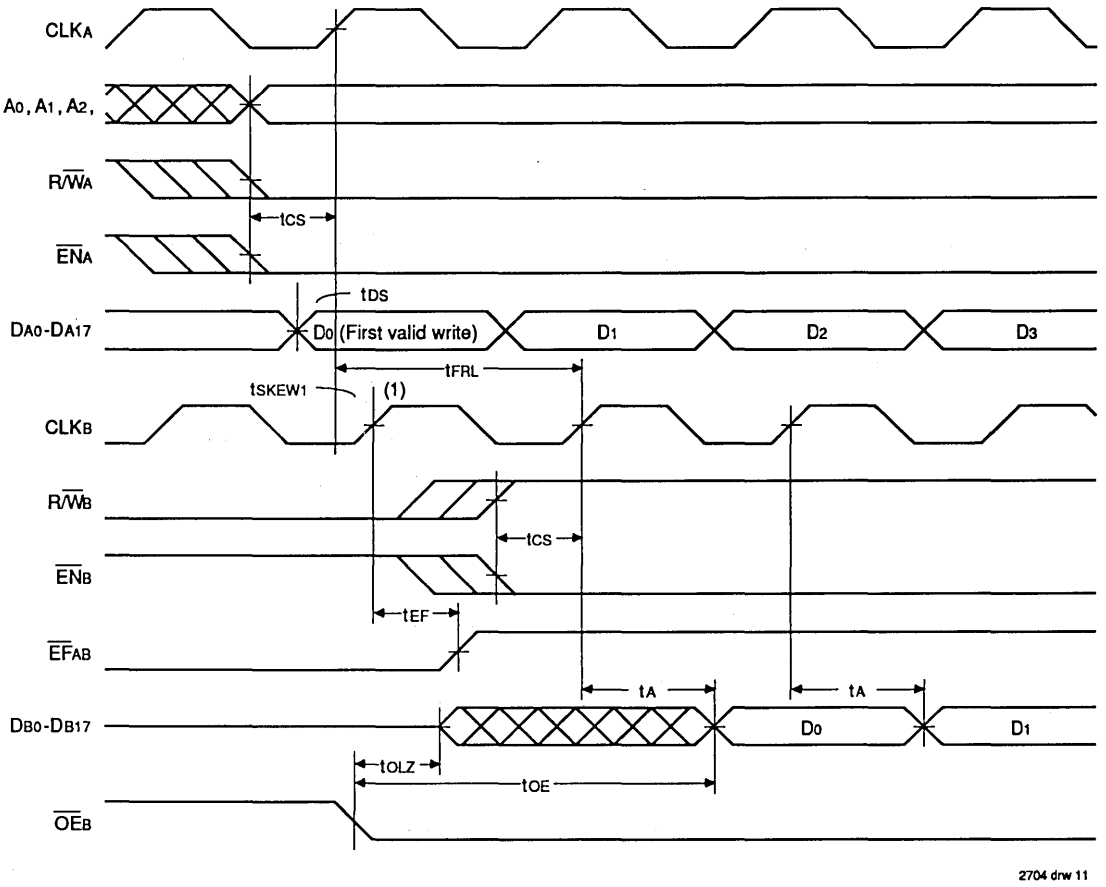
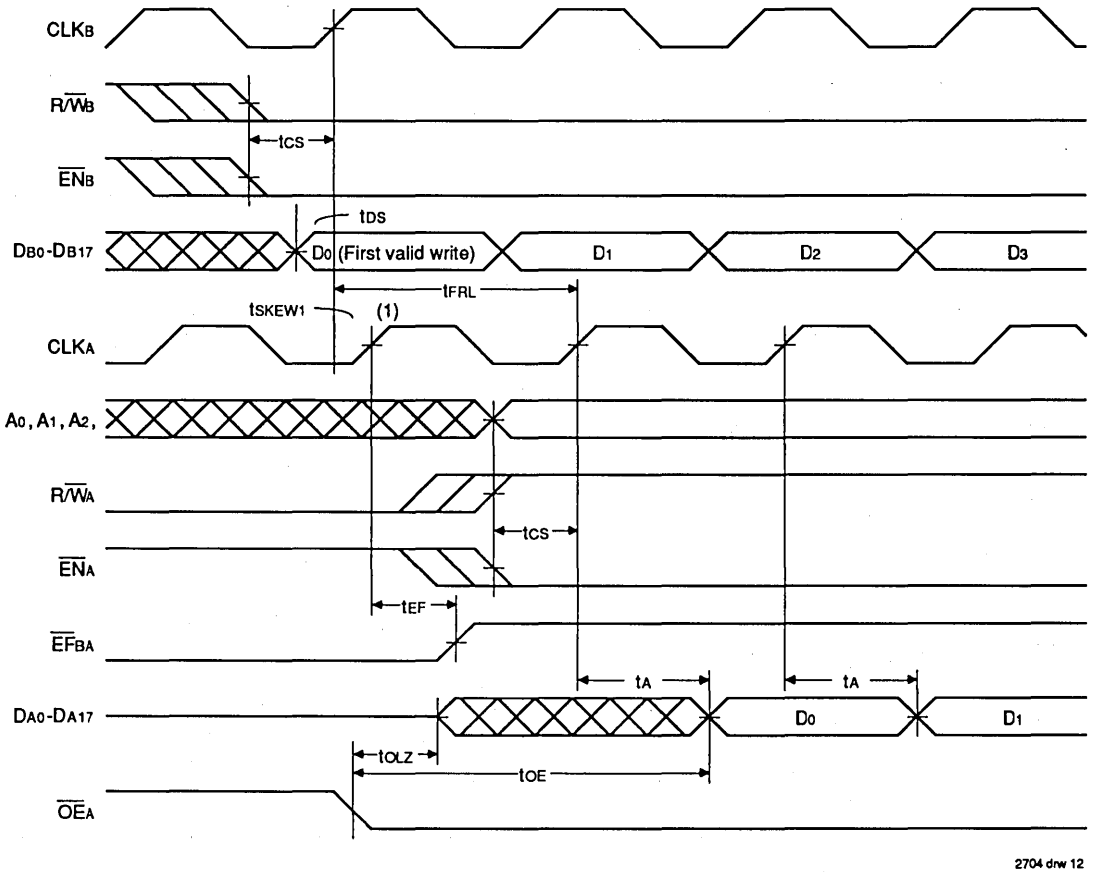


Figure 7. Port B (A→B) Read Timing



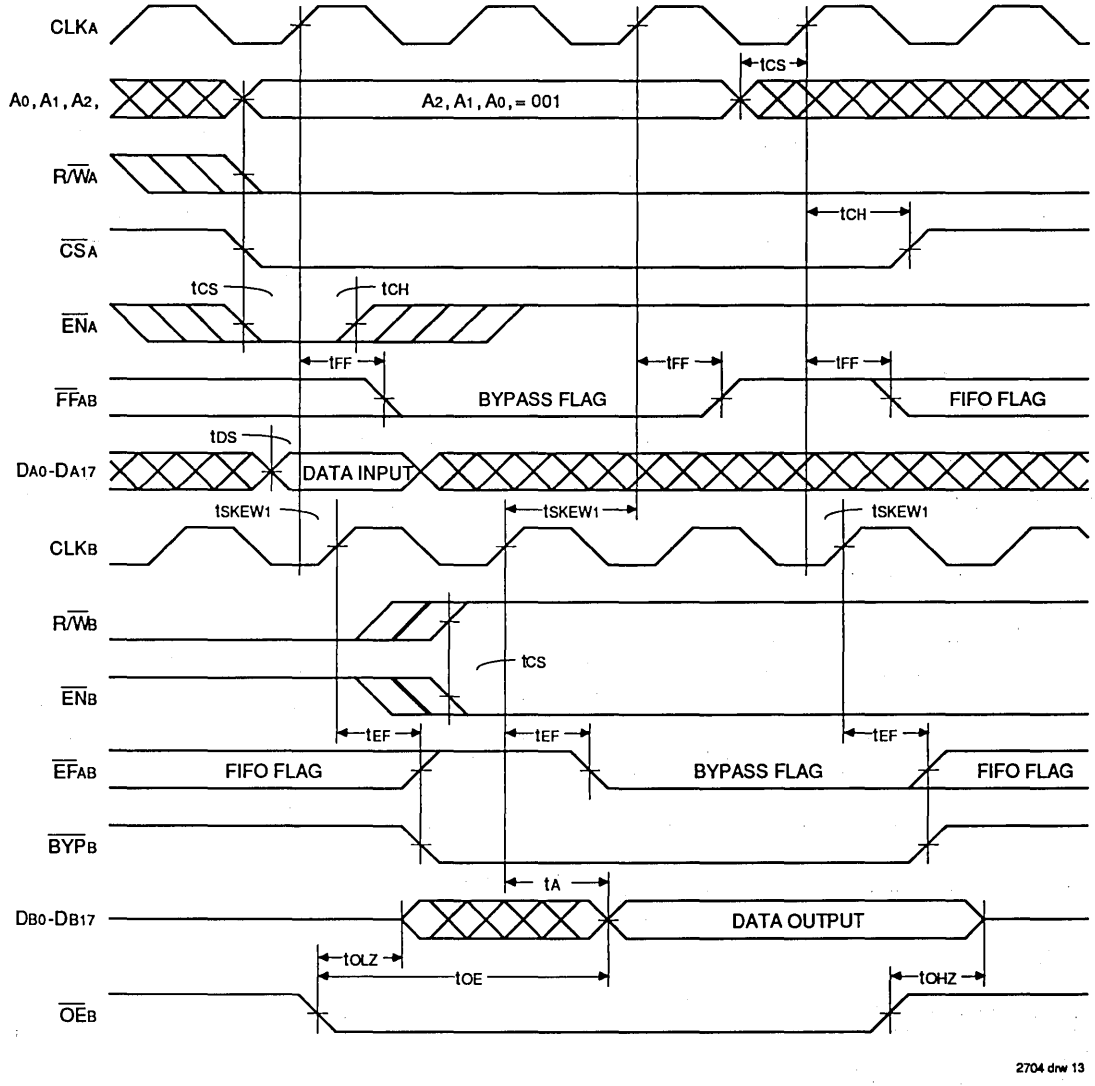
NOTE:
1. When $t_{SKEW1} \geq$ minimum specification, $t_{FRL(Max.)} = t_{CLK} + t_{SKEW1}$
   $t_{SKEW1} <$ minimum specification, $t_{FRL(Max.)} = 2t_{CLK} + t_{SKEW1}$
   The Latency Timing apply only at the Empty Boundary ($\overline{EF}$ = Low).

Figure 8. A→B First Data Word Latency after Reset for Simultaneous Read and Write



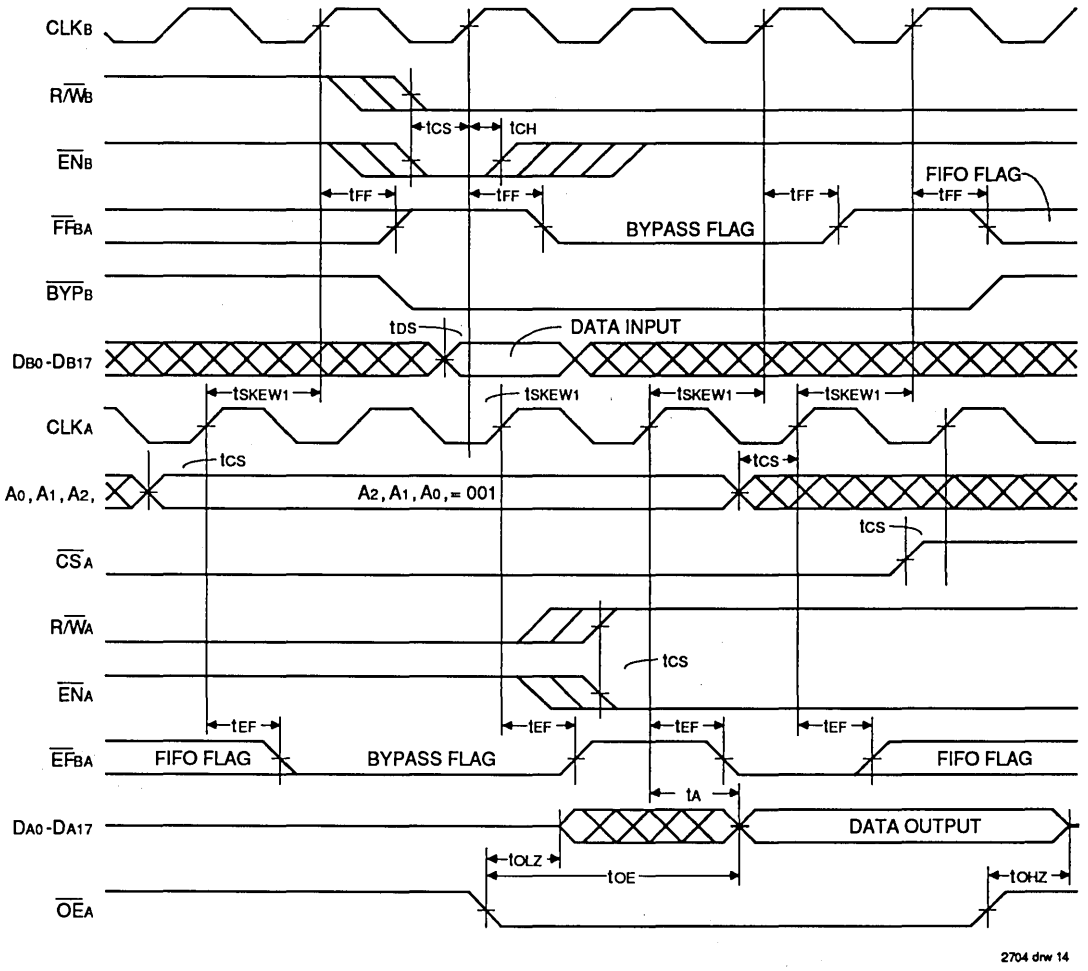
NOTE:
1. When $t_{SKEW1} \geq$ minimum specification, $t_{FRL(Max.)} = t_{CLK} + t_{SKEW1}$
   $t_{SKEW1} <$ minimum specification, $t_{FRL(Max.)} = 2t_{CLK} + t_{SKEW1}$
   The Latency Timing apply only at the Empty Boundary ($\overline{EF}$ = Low).

Figure 9. B→A First Data Word Latency after Reset for Simultaneous Read and Write



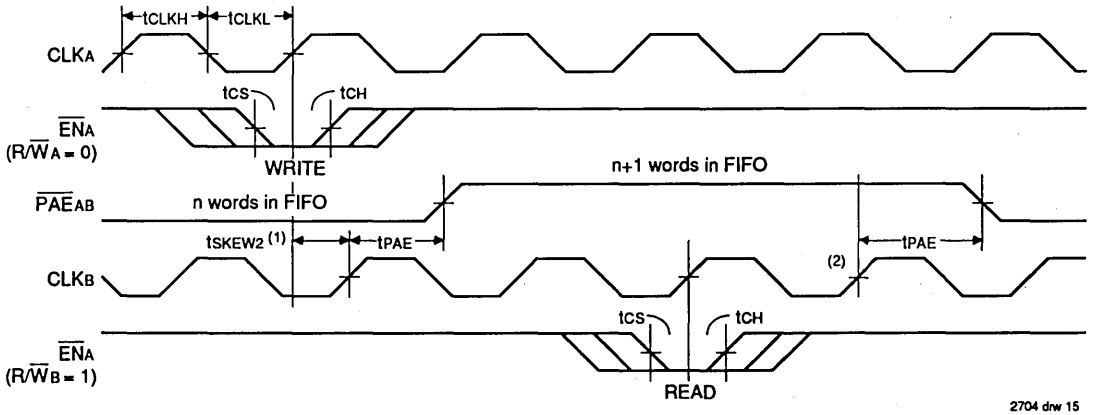
NOTES:
1. When $\overline{CS}_A$ is brought HIGH, A→B Bypass mode will switch to FIFO mode on the following CLKA going low-to-high.
2. After the bypass operation is completed, the $\overline{BYP}_B$ goes from low-to-high; this will reset all bypass flags. The bypass path becomes available for the next bypass operation.
3. When A-side changed from bypass mode into FIFO mode, B-side only has one cycle to read the bypass data. On the next cycle, B-side will be forced back to FIFO mode.

Figure 10. A→B Bypass Timing



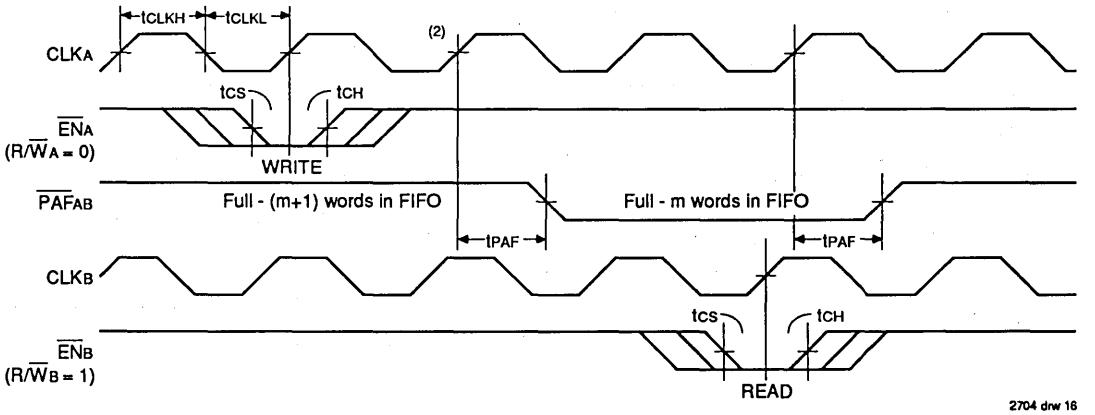
NOTES:
1. When $\overline{CS}_A$ is brought HIGH, A→B Bypass mode will switch to FIFO mode on the following CLKA going low-to-high.
2. After the bypass operation is completed, the $\overline{BYP}_B$ goes from low-to-high; this will reset all bypass flags. The bypass path becomes available for the next bypass operation.
3. When A-side changed from bypass mode into FIFO mode, B-side only has one cycle to read the bypass data. On the next cycle, B-side will be forced back to FIFO mode.

Figure 11. B→A Bypass Timing



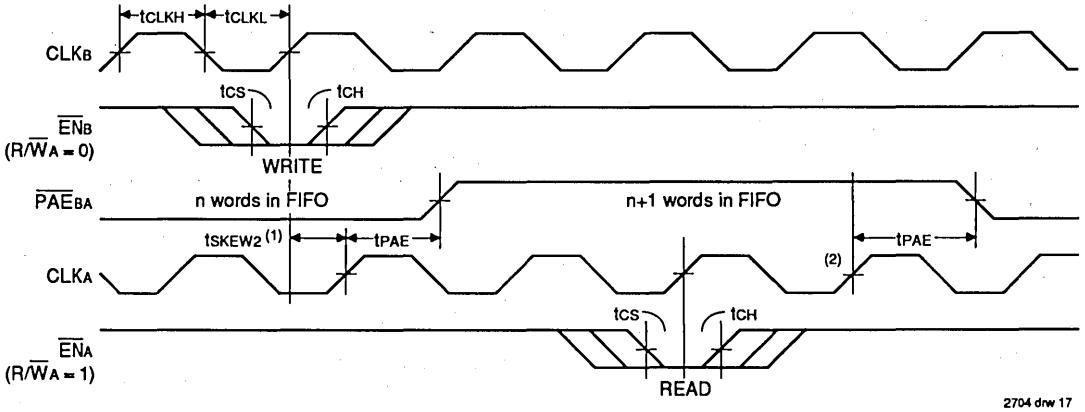
NOTES:
1. tSKEW the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{PAE}_{AB}$ to change during that clock cycle. If the time between the rising edge of CLKA and the rising edge of CLKB is less than tSKEW, then $\overline{PAE}_{AB}$ may not go HIGH until the next CLKB rising edge.
2. If a read is performed on this rising edge of the read clock, there will be Empty + (n + 1) words in the FIFO when $\overline{PAE}$ goes low.

Figure 12. A→B Programmable Almost-Empty Flag Timing



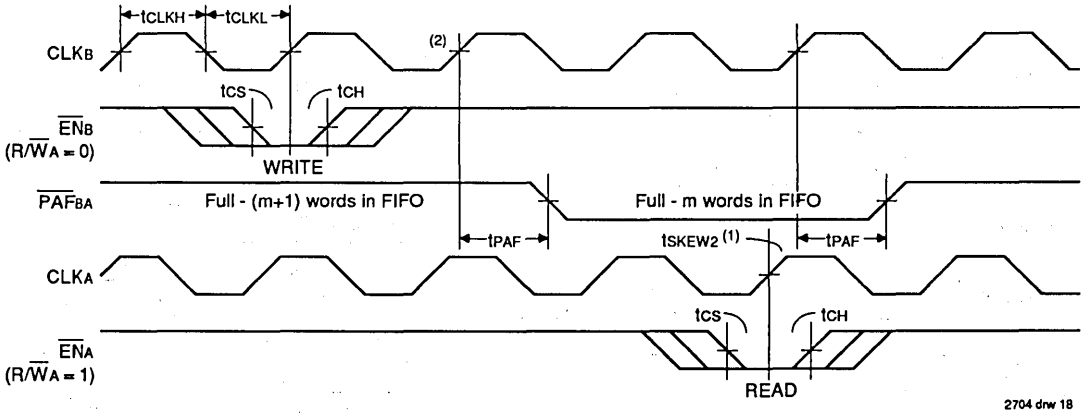
NOTES:
1. tSKEW2 is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{PAF}_{AB}$ to change during that clock cycle. If the time between the rising edge of CLKB and the rising edge of CLKA is less than tSKEW2, then $\overline{PAF}_{AB}$ may not go HIGH until the next CLKA rising edge.
2. If a write is performed on this rising edge of the write clock, there will be Full - (m + 1) words in the FIFO when $\overline{PAF}$ goes low.

Figure 13. A→B Programmable Almost-Full Flag Timing



NOTES:
1. tSKEW2 is the minimum time between a rising CLKB edge and a rising CLKA edge for PAEBA to change during that clock cycle. If the time between the rising edge of CLKB and the rising edge of CLKA is less than tSKEW2, then PAEBA may not go HIGH until the next CLKA rising edge.
2. If a read is performed on this rising edge of the read clock, there will be Empty + (n - 1) words in the FIFO when PAE goes low.

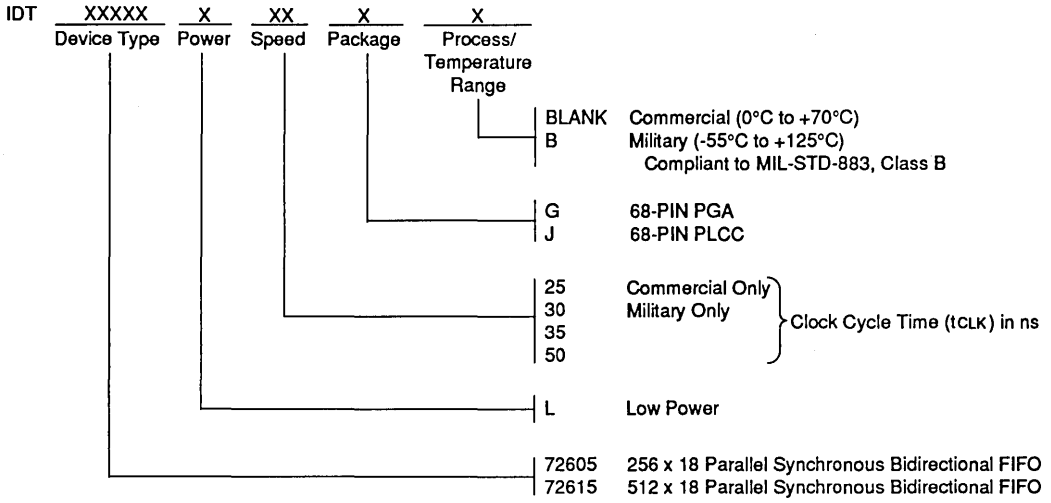
Figure 14. B→A Programmable Almost-Empty Flag Timing



NOTES:
1. tSKEW2 is the minimum time between a rising CLKB edge and a rising CLKA edge for PAFBA to change during that clock cycle. If the time between the rising edge of CLKB and the rising edge of CLKA is less than tSKEW2, then PAFBA may not go HIGH until the next CLKA rising edge.
2. If a write is performed on this rising edge of the write clock, there will be Full - (m + 1) words in the FIFO when PAF goes low.

Figure 15. B→A Programmable Almost-Full Flag Timing

ORDERING INFORMATION



2704 drw 19

6

MULTI-PORT RAMS

Integrated Device Technology has emerged as the leading multi-port RAM supplier by combining CEMOS technology with innovative circuit design. With system performance advantages as a goal, we have brought system design expertise together with circuit and technology expertise in defining dual-port and four-port RAM products. Our dual-port memories are now industry standards.

The synergistic relationship between advanced process technology, system expertise and unique design capability add value beyond that normally achieved. As an example, our dual-port memories provide arbitration along with a completely tested solution to the metastability problem. Various arbitration techniques are available to the designer to prevent contention and system wait states. On-chip hardware arbitration, "semaphore" token passing or software arbitration allow the most efficient memory to be selected for each application. At IDT, innovation counts only when it provides system advantages to the user.

Both commercial and military versions of all IDT memories are available. Our military devices are manufactured and processed strictly in conformance with all the administrative processing and performance requirements of MIL-STD-883. Because we anticipated increased military radiation resistance requirements, all devices are also offered with special radiation resistant processing and guarantees. As the leading supplier of military specialty RAMs, IDT provides performance and quality levels second to none.

Our commercial dual-port and four-port memories, in fact, share most processing steps with military devices.

TABLE OF CONTENTS

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 8K (1K x 8-BIT)

IDT7130SA/LA
IDT7140SA/LA

FEATURES

- High-speed access
  - —Military: 25/30/35/45/55/70/90/100/120ns (max.)
  - —Commercial: 20/25/30/35/45/55/70/90/100ns (max.)
- Low-power operation
  - —IDT7130/IDT7140SA
    - Active: 325mW (typ.)
    - Standby: 5mW (typ.)
  - —IDT7130/IDT7140LA
    - Active: 325mW (typ.)
    - Standby: 1mW (typ.)
- MASTER IDT7130 easily expands data bus width to 16-or-more-bits using SLAVE IDT7140
- On-chip port arbitration logic (IDT7130 Only)
- $\overline{BUSY}$ output flag on IDT7130; $\overline{BUSY}$ input on IDT7140
- $\overline{INT}$ flag for port-to-port communication
- Fully asynchronous operation from either port
- Battery backup operation–2V data retention
- TTL-compatible, single 5V ±10% power supply
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-86875

DESCRIPTION

The IDT7130/IDT7140 are high speed 1K x 8 dual-port static RAMs. The IDT7130 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7140 "SLAVE" dual-port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

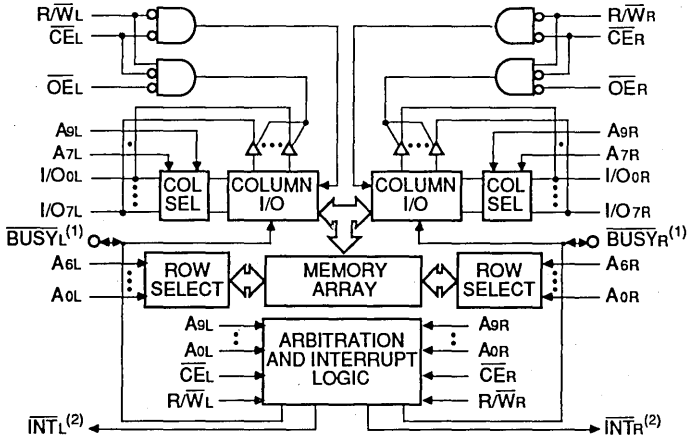
Both devices provide two independent ports with separate control, address and I/O pins that permit independent asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 325mW of power at maximum access times as fast as 20ns. Low-power (LA) versions offer battery backup data retention capability, with each dual-port typically consuming 200µw from a 2V battery.

The IDT7130/IDT7140 devices are packaged in 48-pin sidebraze or plastic DIPs, 48- or 52-pin LCCs, 52-pin PLCCs, and 48-Lead flatpacks.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM

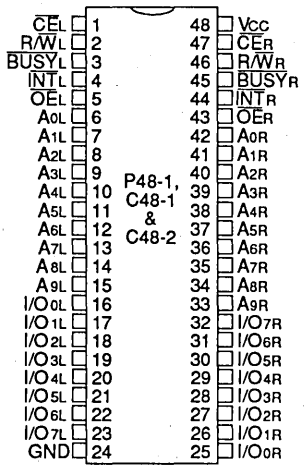


NOTES:

1. IDT7130 (MASTER): $\overline{BUSY}$ is open drain output and requires pullup resistor.
   IDT7140 (SLAVE): $\overline{BUSY}$ is input.
2. Open drain output: requires pullup resistor.

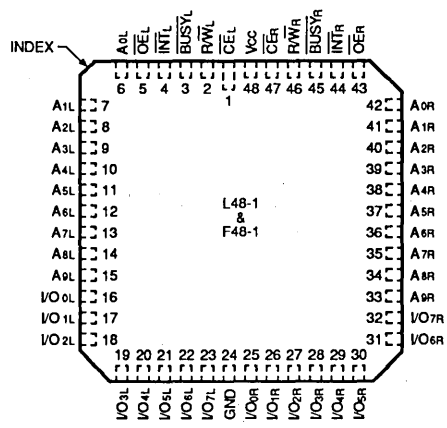
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGUARATIONS



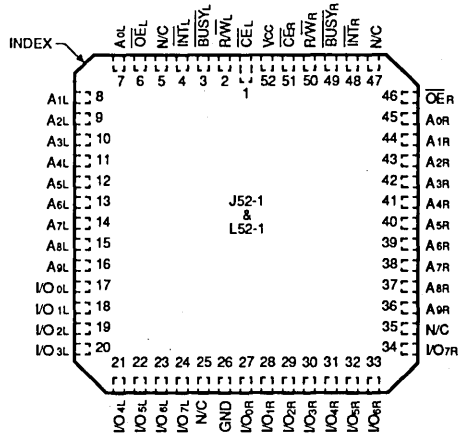
2689 drw 02

DIP
TOP VIEW



2689 drw 03

48-PIN LCC/FLATPACK
TOP VIEW



2689 drw 04

52-PIN LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

2689 tbl 01

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

2689 tbl 02

NOTE:

1. VIL (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0v ± 10%
Commercial	0°C to +70°C	0V	5.0v ± 10%

2689 tbl 03

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ±10%)

Symbol	Parameter	Test Conditions	IDT7130SA IDT7140SA Min.	IDT7130SA IDT7140SA Max.	IDT7130LA IDT7140LA Max.	IDT7130LA IDT7140LA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O_0-I/O_7)	I_{OL} = 4.0mA	—	0.4	—	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$, $\overline{INT}$)	I_{OL} = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2689 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version		7130 x 20[2,6] 7140 x 20[2,6] Typ.	7130 x 20[2,6] 7140 x 20[2,6] Max.	7130 x 25[6] 7140 x 25[6] Typ.	7130 x 25[6] 7140 x 25[6] Max.	7130 x 30[6] 7140 x 30[6] Typ.	7130 x 30[6] 7140 x 30[6] Max.	7130 x 35[7] 7140 x 35[7] Typ.	7130 x 35[7] 7140 x 35[7] Max.	7130 x 45 7140 x 45 Typ.	7130 x 45 7140 x 45 Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	Mil.	SA	—	—	75	300	75	290	75	280	75	230	mA
				LA	—	—	75	220	75	210	75	200	75	185	
			Com'l.	SA	75	260	75	250	75	240	75	195	75	190	
				LA	75	190	75	180	75	170	75	155	75	145	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE_L}$ and $\overline{CE_R}$ ≥ V_{IH} f = f_{MAX}[4]	Mil.	SA	—	—	25	75	25	75	25	75	25	65	mA
				LA	—	—	25	55	25	55	25	55	25	55	
			Com'l.	SA	25	65	25	65	25	65	25	65	25	65	
				LA	25	45	25	45	25	45	25	45	25	45	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE_L}$ or $\overline{CE_R}$ ≥ V_{IH} Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	—	—	50	180	46	175	40	170	40	135	mA
				LA	—	—	50	140	46	135	40	130	40	110	
			Com'l.	SA	50	180	50	170	46	155	40	130	40	120	
				LA	50	130	50	120	46	110	40	95	40	85	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE_L}$ and $\overline{CE_R}$ ≥ Vcc -0.2V V_{IN} ≥ Vcc -0.2V or V_{IN} ≤ 0.2V, f = 0[5]	Mil.	SA	—	—	1.2	40	1.2	40	1.2	35	1.0	30	mA
				LA	—	—	0.4	10	0.4	10	0.4	10	0.2	10	
			Com'l.	SA	1.2	15	1.2	15	1.2	15	1.0	15	1.0	15	
				LA	0.4	4	0.4	4	0.4	4	0.2	4	0.2	4	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs, f = 0[5])	One Port $\overline{CE_L}$ or $\overline{CE_R}$ ≥ Vcc -0.2V V_{IN} ≥ Vcc -0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	—	—	50	170	45	160	40	150	40	125	mA
				LA	—	—	46	135	42	125	35	115	35	95	
			Com'l.	SA	50	160	50	150	45	137	40	115	40	105	
				LA	46	125	46	115	42	105	35	90	35	80	

2689 tbl 05

NOTES:
1. "x" in part numbers indicates power rating (SA or LA).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of $1/t_{RC}$, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
6. Not available in DIP packages, see 7030/40 data sheet.
7. DIP packages for 0°C to +70°C only, see 7030/40 data sheet.

7

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (Continued) (V_{CC} = 5.0V ±10%)

Symbol	Parameter	Test Conditions	Version		7130 x 55 7140 x 55 Typ.	7130 x 55 7140 x 55 Max.	7130 x 70 7140 x 70 Typ.	7130 x 70 7140 x 70 Max.	7130 x 90 7140 x 90 Typ.	7130 x 90 7140 x 90 Max.	7130 x 100 7140 x 100 Typ.	7130 x 100 7140 x 100 Max.	7130 x 120[3] 7140 x 120[3] Typ.	7130 x 120[3] 7140 x 120[3] Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	Mil.	SA	65	230	65	225	65	200	65	190	65	190	mA
				LA	65	185	65	180	65	160	65	155	65	155	
			Com'l.	SA	65	180	65	180	65	180	65	180	—	—	
				LA	65	140	65	135	65	130	65	130	—	—	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ f = f_{MAX}[4]	Mil.	SA	25	65	25	65	25	65	25	65	25	65	mA
				LA	25	55	25	55	25	45	25	45	25	45	
			Com'l.	SA	25	65	25	60	25	55	25	55	—	—	
				LA	25	45	25	40	25	35	25	35	—	—	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	40	135	40	135	40	125	40	125	40	125	mA
				LA	40	110	40	110	40	100	40	100	40	100	
			Com'l.	SA	40	115	40	110	40	110	40	110	—	—	
				LA	40	85	40	85	40	75	40	75	—	—	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V, f = 0[5]	Mil.	SA	1.0	30	1.0	30	1.0	30	1.0	30	1.0	30	mA
				LA	0.2	10	0.2	10	0.2	10	0.2	10	0.2	10	
			Com'l.	SA	1.0	15	1.0	15	1.0	15	1.0	15	—	—	
				LA	0.2	4	0.2	4	0.2	4	0.2	4	—	—	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs, f = 0[5])	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	40	120	40	115	40	110	40	110	40	110	mA
				LA	35	90	35	85	35	80	35	80	35	80	
			Com'l.	SA	40	100	40	100	40	95	40	95	—	—	
				LA	35	75	35	75	35	70	35	70	—	—	

NOTES:
2689 tbl 06

1. "x" in part numbers indicates power rating (SA or LA).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.

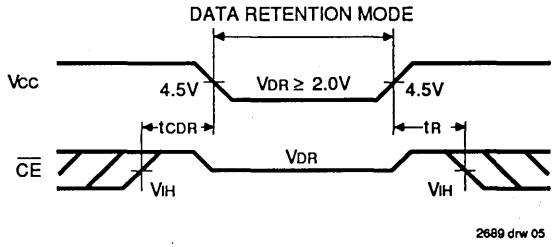
DATA RETENTION CHARACTERISTICS (LA Version Only)

Symbol	Parameter	Test Conditions		IDT7130LA/IDT7140LA Min.	Typ.	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V		2.0	—	0	V
I_{CCDR}	Data Retention Current		Mil.	—	100	4000	µA
			Com'l.	—	100	1500	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:
2689 tbl 07

1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM



2689 drw 05

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2, 3 and 4

2689 tbl 08

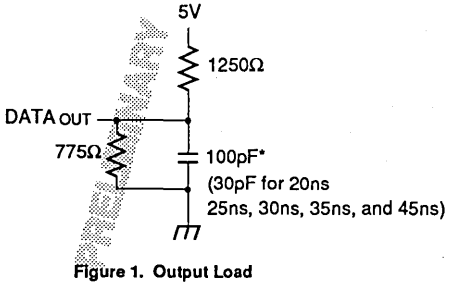


Figure 1. Output Load

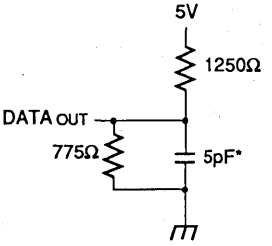


Figure 2. Output Load (for tHZ, tLZ, twz, and tow)

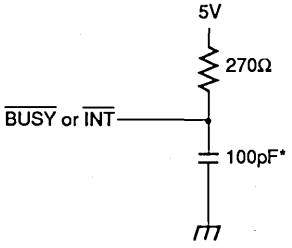


Figure 3. BUSY and INT Output Load

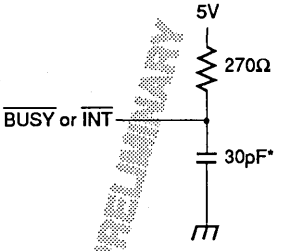


Figure 4. BUSY and INT Output Load (for 20ns, 25ns and 30ns versions)

* Including scope and jig

2689 drw 06

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AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(5)

Symbol	Parameter	7130 x 20(2,6) 7140 x 20(2,6) Min.	Max.	7130 x 25(6) 7140 x 25(6) Min.	Max.	7130 x 30(6) 7140 x 30(6) Min.	Max.	7130 x 35(7) 7140 x 35(7) Min.	Max.	7130 x 45 7140 x 45 Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
tAA	Address Access Time	—	20	—	25	—	30	—	35	—	45	ns
tACE	Chip Enable Access Time	—	20	—	25	—	30	—	35	—	45	ns
tAOE	Output Enable Access Time	—	10	—	12	—	15	—	25	—	30	ns
tOH	Output Hold From Address Change	0	—	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time(1,4)	0	—	0	—	0	—	5	—	5	—	ns
tHZ	Output High Z Time(1,4)	—	8	—	10	—	12	—	15	—	20	ns
tPU	Chip Enable to Power Up Time(4)	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time(4)	—	50	—	50	—	50	—	50	—	50	ns

2689 tbl 09

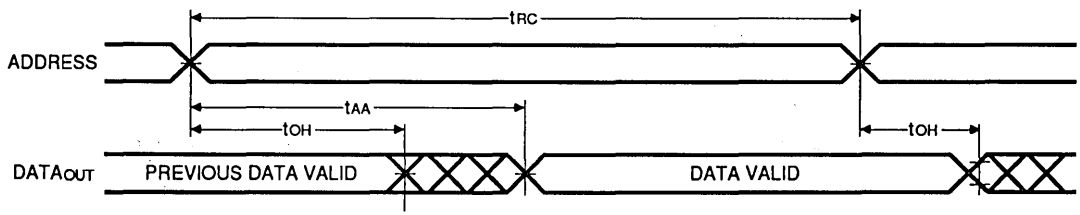
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(5) (Continued)

Symbol	Parameter	7130 x 55 7140 x 55 Min.	Max.	7130 x 70 7140 x 70 Min.	Max.	7130 x 90 7140 x 90 Min.	Max.	7130 x 100 7140 x 100 Min.	Max.	7130 x 120(3) 7140 x 120(3) Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	55	—	70	—	90	—	100	—	120	—	ns
tAA	Address Access Time	—	55	—	70	—	90	—	100	—	120	ns
tACE	Chip Enable Access Time	—	55	—	70	—	90	—	100	—	120	ns
tAOE	Output Enable Access Time	—	35	—	40	—	40	—	40	—	60	ns
tOH	Output Hold From Address Change	0	—	0	—	10	—	10	—	10	—	ns
tLZ	Output Low Z Time(1,4)	5	—	5	—	5	—	5	—	5	—	ns
tHZ	Output High Z Time(1,4)	—	30	—	35	—	40	—	40	—	40	ns
tPU	Chip Enable to Power Up Time(4)	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time(4)	—	50	—	50	—	50	—	50	—	50	ns

2689 tbl 10

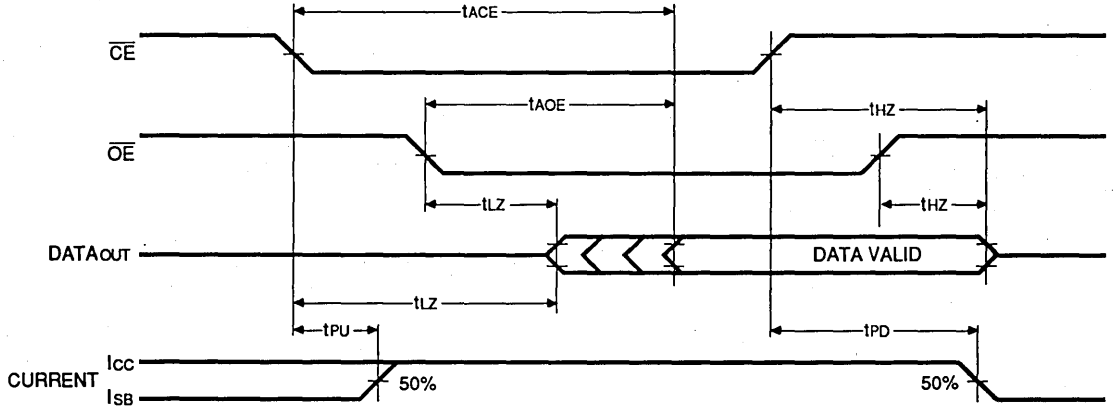
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2, 3 and 4).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. "x" in part numbers indicates power rating (SA or LA).
6. Not available in DIP packages, see 7030/40 data sheet.
7. DIP packages for 0°C to +70°C only, see 7030/40 data sheet.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE (1, 2, 4)



2689 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1, 3)



2689 drw 08

NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = VIL.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = VIL.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (7)

Symbol	Parameter	7130 x 20(2,8) 7140 x 20(2,8) Min.	Max.	7130 x 25(8) 7140 x 25(8) Min.	Max.	7130 x 30(8) 7140 x 30(8) Min.	Max.	7130 x 35(9) 7140 x 35(9) Min.	Max.	7130 x 45 7140 x 45 Min.	Max.	Unit
Write Cycle												
tWC	Write Cycle Time(5)	20	—	25	—	30	—	35	—	45	—	ns
tEW	Chip Enable to End of Write	15	—	20	—	25	—	30	—	35	—	ns
tAW	Address Valid to End of Write	15	—	20	—	25	—	30	—	35	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width (6)	15	—	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	10	—	12	—	15	—	20	—	20	—	ns
tHZ	Output High Z Time (1, 4)	—	8	—	10	—	12	—	15	—	20	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z (1, 4)	—	8	—	10	—	12	—	15	—	20	ns
tOW	Output Active From End of Write (1, 4)	0	—	0	—	0	—	0	—	0	—	ns

2689 tbl 11

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (7)

Symbol	Parameter	7130 x 55 7140 x 55 Min.	Max.	7130 x 70 7140 x 70 Min.	Max.	7130 x 90 7140 x 90 Min.	Max.	7130 x 100 7140 x 100 Min.	Max.	7130 x 120(3) 7140 x 120(3) Min.	Max.	Unit
Write Cycle												
tWC	Write Cycle Time(5)	55	—	70	—	90	—	100	—	120	—	ns
tEW	Chip Enable to End of Write	40	—	50	—	85	—	90	—	100	—	ns
tAW	Address Valid to End of Write	40	—	50	—	85	—	90	—	100	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width (6)	40	—	50	—	55	—	55	—	65	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	20	—	30	—	40	—	40	—	40	—	ns
tHZ	Output High Z Time (1, 4)	—	30	—	35	—	40	—	40	—	40	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z (1, 4)	—	30	—	35	—	40	—	40	—	50	ns
tOW	Output Active From End of Write (1, 4)	0	—	0	—	0	—	0	—	0	—	ns

2689 tbl 12

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2, 3 and 4).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, tWC = tBAA + tWP.
6. Specified for $\overline{OE}$ at high (Refer to "Timing Waveform of Write Cycle", Note 7)
7. "x" in part numbers indicates power rating (SA or LA).
8. Not available in DIP packages, see 7030/40 data sheet.
9. DIP packages for 0°C to +70°C only, see 7030/40 data sheet.

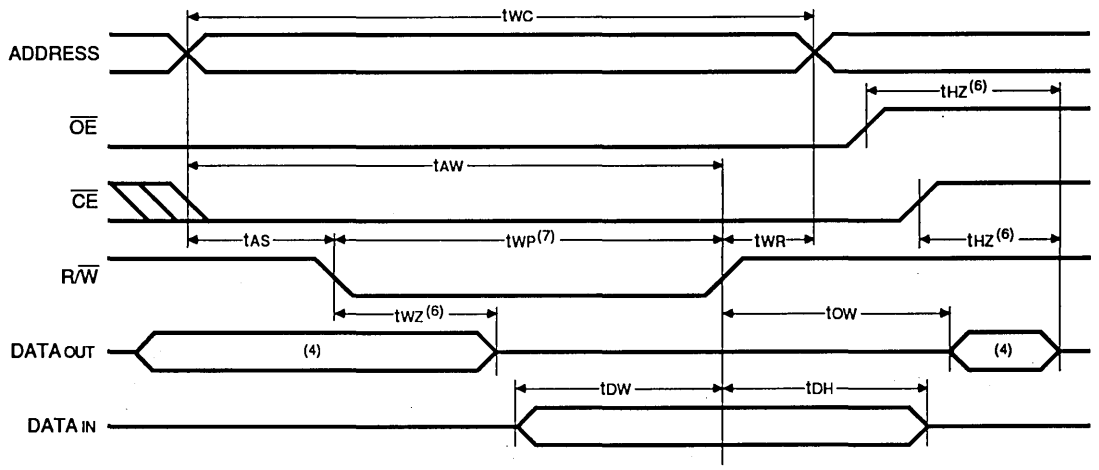
CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Output Capacitance	VIN = 0V	11	pF

2689 tbl 13

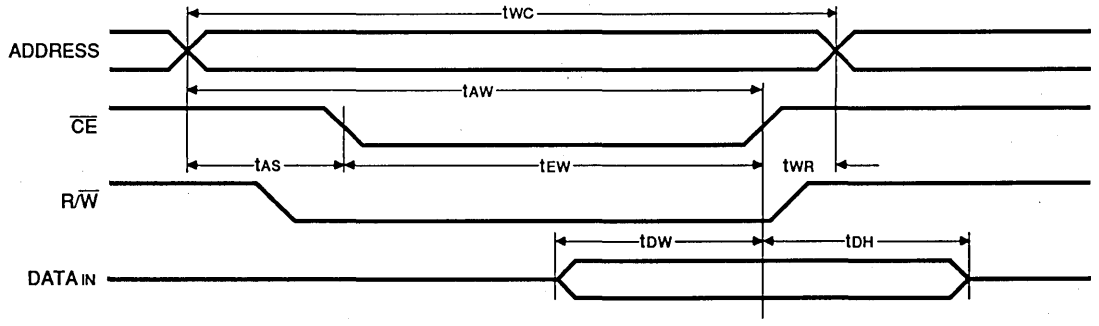
NOTE:
1. This parameter is determined by device characterization but is not production tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/$\overline{W}$ CONTROLLED TIMING)(1,2,3,7)



2689 drw 09

TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING)(1,2,3,5)



2689 drw 10

NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (8)

Symbol	Parameter	7130 x 20(1,10) 7140 x 20(1,10) Min.	Max.	7130 x 25(10) 7140 x 25(10) Min.	Max.	7130 x 30(10) 7140 x 30(10) Min.	Max.	7130 x 35(11) 7140 x 35(11) Min.	Max.	7130 x 45 7140 x 45 Min.	Max.	Unit
BUSY TIMING (FOR MASTER IDT7130 ONLY)												
tBAA	BUSY Access Time to Address	—	20	—	25	—	30	—	35	—	35	ns
tBDA	BUSY Disable Time to Address	—	18	—	20	—	25	—	30	—	35	ns
tBAC	BUSY Access Time to Chip Enable	—	20	—	20	—	25	—	30	—	30	ns
tBDC	BUSY Disable Time to Chip Enable	—	18	—	20	—	25	—	25	—	25	ns
tWDD	Write Pulse to Data Delay(3)	—	45	—	50	—	55	—	60	—	70	ns
tDDD	Write Data Valid to Read Data Delay(3)	—	30	—	33	—	33	—	35	—	45	ns
tAPS	Arbitration Priority Set-up Time (4)	5	—	5	—	5	—	5	—	5	—	ns
tBDD	BUSY Disable to Valid Data(5)	—	Note 5	—	Note 5	—	Note 5	—	Note 5	—	Note 5	ns
BUSY INPUT TIMING (FOR SLAVE IDT7140 ONLY)												
tWB	Write to BUSY Input(6)	0	—	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After BUSY(7)	12	—	15	—	20	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay(9)	—	45	—	50	—	55	—	60	—	70	ns
tDDD	Write Data Valid to Read Data Delay(9)	—	30	—	35	—	35	—	35	—	45	ns

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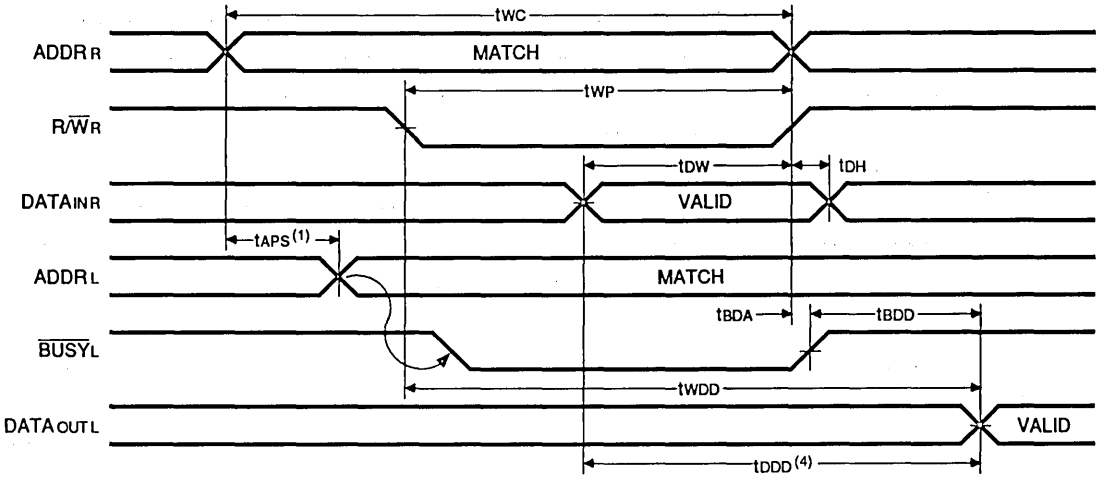
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (8)

Symbol	Parameter	7130 x 55 7140 x 55 Min.	Max.	7130 x 70 7140 x 70 Min.	Max.	7130 x 90 7140 x 90 Min.	Max.	7130 x 100 7140 x 100 Min.	Max.	7130 x 120(2) 7140 x 120(2) Min.	Max.	Unit
BUSY TIMING (FOR MASTER IDT7130 ONLY)												
tBAA	BUSY Access Time to Address	—	45	—	45	—	45	—	50	—	60	ns
tBDA	BUSY Disable Time to Address	—	40	—	40	—	45	—	50	—	60	ns
tBAC	BUSY Access Time to Chip Enable	—	35	—	35	—	45	—	50	—	60	ns
tBDC	BUSY Disable Time to Chip Enable	—	30	—	30	—	45	—	50	—	60	ns
tWDD	Write Pulse to Data Delay(3)	—	80	—	90	—	100	—	120	—	140	ns
tDDD	Write Data Valid to Read Data Delay(3)	—	55	—	70	—	90	—	100	—	120	ns
tAPS	Arbitration Priority Set-up Time(4)	5	—	5	—	5	—	5	—	5	—	ns
tBDD	BUSY Disable to Valid Data(5)	—	Note 5	—	Note 5	—	Note 5	—	Note 5	—	Note 5	ns
BUSY INPUT TIMING (FOR SLAVE IDT7140 ONLY)												
tWB	Write to BUSY Input(6)	0	—	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After BUSY(7)	20	—	20	—	20	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay(9)	—	80	—	90	—	100	—	120	—	140	ns
tDDD	Write Data Valid to Read Data Delay(9)	—	55	—	70	—	90	—	100	—	120	ns

2689 tbl 15

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (For Master IDT7130 only)".
4. To ensure that the earlier of the two ports wins.
5. tBDD is a calculated parameter and is the greater of 0, tWDD-tWP (actual) or tDDD-tDW (actual).
6. To ensure that the write cycle is inhibited during contention.
7. To ensure that a write cycle is completed after contention.
8. "x" in part numbers indicates power rating (SA or LA).
9. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With Port-to-Port Delay (For Slave IDT7140 Only)".
10. Not available in DIP packages, see 7030/40 data sheet.
11. DIP packages for 0°C to +70°C only, see 7030/40 data sheet.

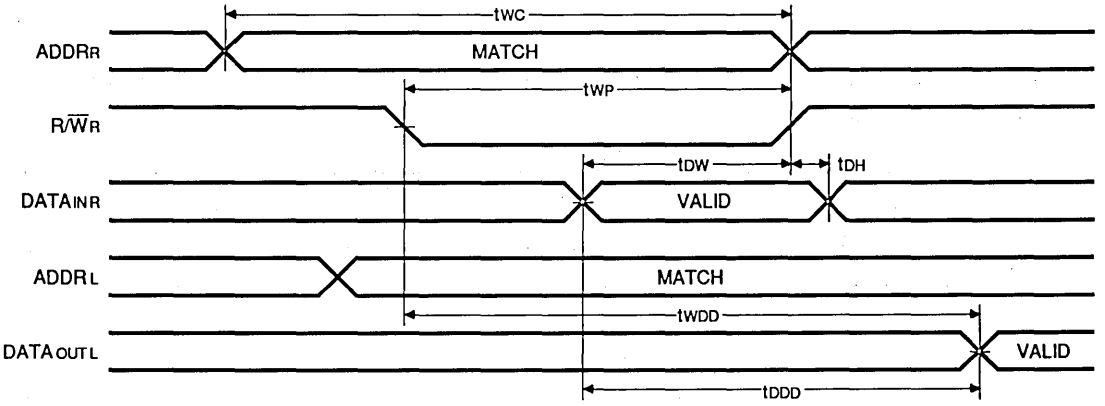
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$ (1,2,3) (FOR MASTER IDT7130 ONLY)



NOTES:
1. To ensure that the earlier of the two ports wins.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continously enabled for both ports.
4. $\overline{OE}$ at LO for the reading port.

2689 drw 11

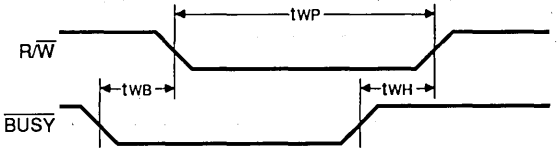
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY (1,2,3) (FOR SLAVE IDT7140 ONLY)



NOTES:
1. Assume $\overline{BUSY}$ input at HI for the writing port, and $\overline{OE}$ at LO for the reading port.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuosly enabled for both ports.

2689 drw 12

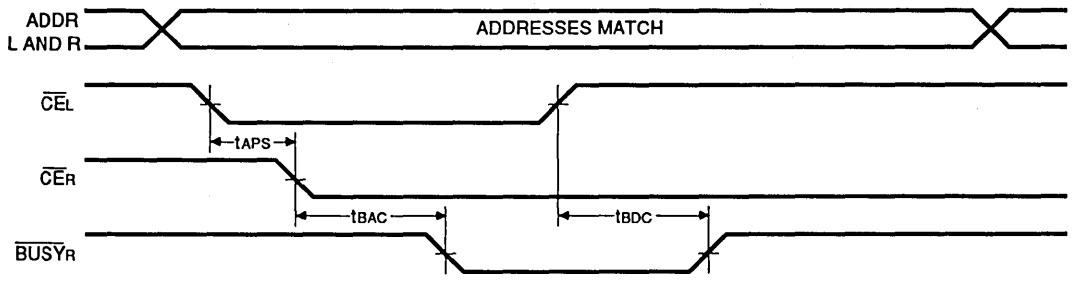
TIMING WAVEFORM OF WRITE WITH BUSY INPUT (FOR SLAVE IDT7140 ONLY)



2689 drw 13

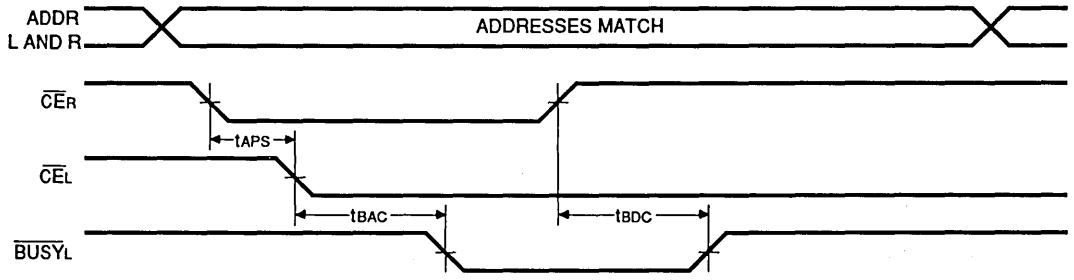
TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION

$\overline{CE}_L$ VALID FIRST:



2689 drw 14

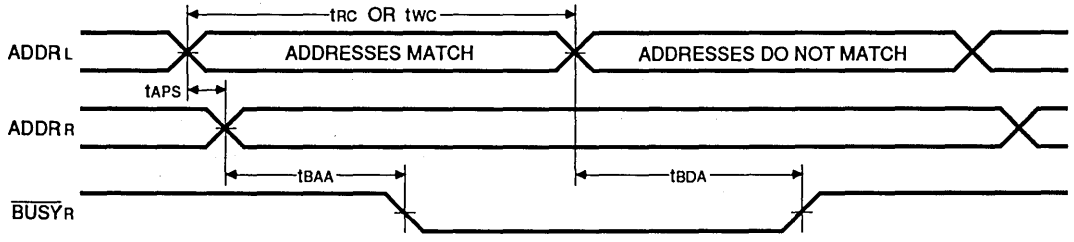
$\overline{CE}_R$ VALID FIRST:



2689 drw 15

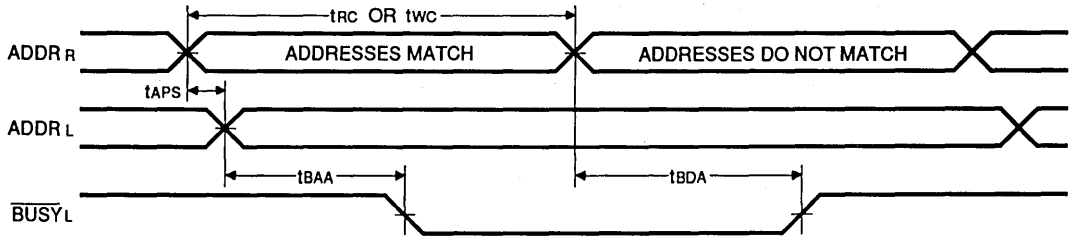
TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION(1)

LEFT ADDRESS VALID FIRST:



2689 drw 16

RIGHT ADDRESS VALID FIRST:



2689 drw 17

NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (3)

Symbol	Parameter	7130 x 20(1,4) 7140 x 20(1,4) Min.	Max.	7130 x 25(4) 7140 x 25(4) Min.	Max.	7130 x 30(4) 7140 x 30(4) Min.	Max.	7130 x 35(5) 7140 x 35(5) Min.	Max.	7130 x 45 7140 x 45 Min.	Max.	Unit
Interrupt Timing												
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	20	—	25	—	30	—	35	—	40	ns
tINR	Interrupt Reset Time	—	20	—	25	—	30	—	35	—	40	ns

2689 tbl 16

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

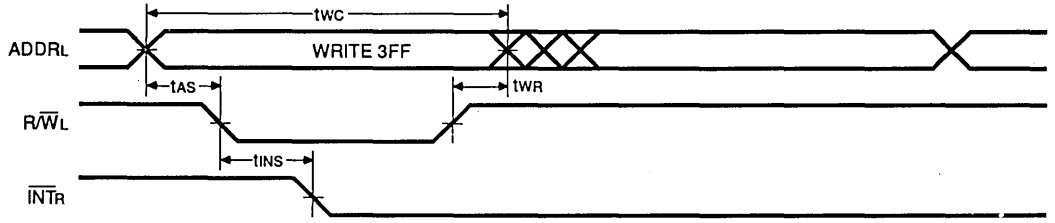
Symbol	Parameter	7130 x 55 7140 x 55 Min.	Max.	7130 x 70 7140 x 70 Min.	Max.	7130 x 90 7140 x 90 Min.	Max.	7130 x 100 7140 x 100 Min.	Max.	7130 x 120(2) 7140 x 120(2) Min.	Max.	Unit
Interrupt Timing												
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	45	—	50	—	55	—	60	—	70	ns
tINR	Interrupt Reset Time	—	45	—	50	—	55	—	60	—	70	ns

2689 tbl 17

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. "x" in part numbers indicates power rating (SA or LA).
4. Not available in DIP packages, see 7030/40 data sheet.
5. DIP packages for 0°C to +70°C only, see 7030/40 data sheet.

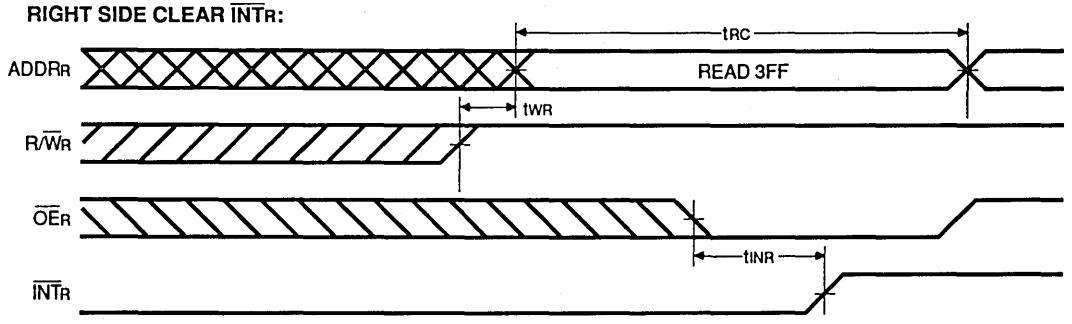
TIMING WAVEFORM OF INTERRUPT MODE (1, 2)

LEFT SIDE SETS $\overline{INT}_R$:



2689 drw 18

RIGHT SIDE CLEAR $\overline{INT}_R$:

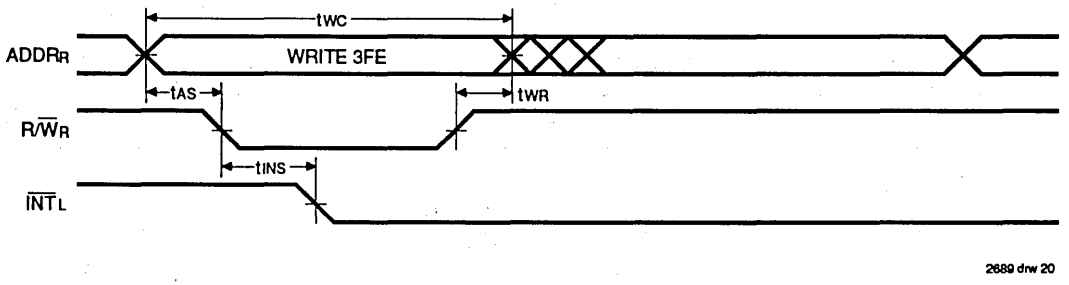


2689 drw 19

NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
2. $\overline{INT}_L$ and $\overline{INT}_R$ are reset (high) during power up.

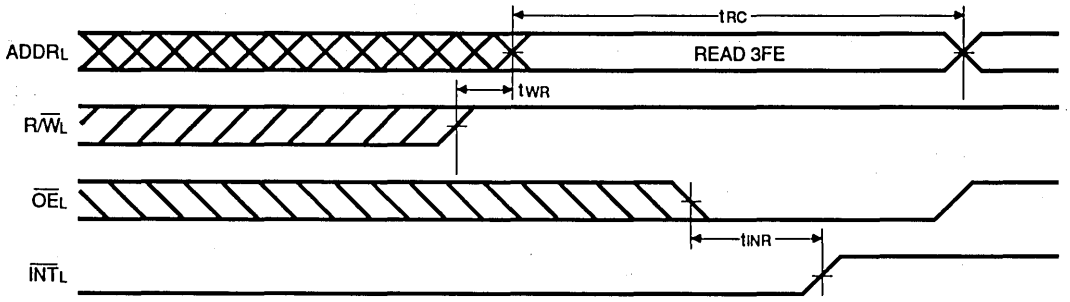
TIMING WAVEFORM OF INTERRUPT MODE(1, 2)

RIGHT SIDE SETS $\overline{INT}_L$:



2689 drw 20

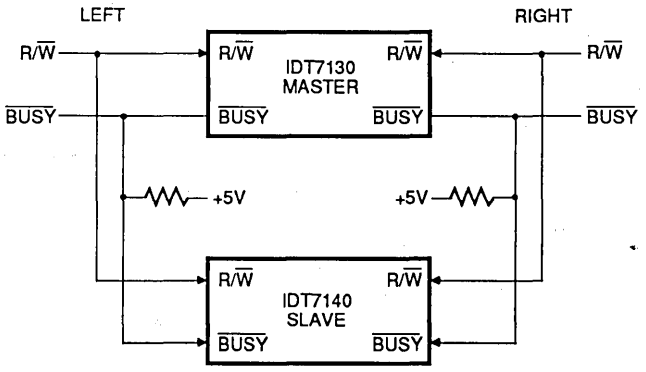
LEFT SIDE CLEAR $\overline{INT}_L$:



2689 drw 21

NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
2. $\overline{INT}_R$ and $\overline{INT}_L$ are reset (high) during power up.

16-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



2689 drw 22

NOTE:
1. No arbitration in IDT7140 (SLAVE). $\overline{BUSY}$-IN inhibits write in IDT7140 (SLAVE).

FUNCTIONAL DESCRIPTION:

The IDT7130/IDT7140 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any locations in memory. The IDT7130/IDT7140 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table 1.

The interrupt flag ($\overline{INT}$) permits communication between ports or systems. If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT_L}$) is set when the right port writes to memory location 3FE (HEX). The left port clears the interrupt by reading address location 3FE. Likewise, the right port interrupt flag ($\overline{INT_R}$) is set when the left port writes to memory location 3FF (HEX) and to clear the interrupt flag ($\overline{INT_R}$), the right port must read the memory location 3FF. The message (8-bits) at 3FE or 3FF is user defined. If the interrupt function is not used, address locations 3FE or 3FF are not used as mailboxes, but as part of the random access memory. Refer to Table II for the interrupt operation.

ARBITRATION LOGIC FUNCTIONAL DESCRIPTION:

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE_L}$ and $\overline{CE_R}$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table II). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION MASTER/SLAVE DESCRIPTION:

Expanding the data bus width to sixteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY_L}$ while another activates its $\overline{BUSY_R}$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one arbitrator, in the MASTER, is used. The SLAVE has BUSY inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed, until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

7

TRUTH TABLES

TABLE I – NON-CONTENTION READ/WRITE CONTROL(4)

Left Or Right Port(1)				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	Function
X	H	X	Z	Port Disabled and in Power Down Mode I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	DATAIN	Data on Port Written into Memory(2)
H	L	L	DATAOUT	Data in Memory Output on Port(3)
H	L	H	Z	High Impedance Outputs

2689 tbl 18

NOTES:
1. A_{0L}-$A_{9L} \neq A_{0R}$-A_{9R}
2. If $\overline{BUSY}$ = L, data is not written
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

TABLE II – INTERRUPT FLAG(1, 4)

Left Port					Right Port					
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{9L}	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0L}-A_{9R}	$\overline{INT}_R$	Function
L	L	X	3FF	X	X	X	X	X	L(2)	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	3FF	H(3)	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L(3)	L	L	X	3FE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	3FE	H(2)	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

2689 tbl 19

NOTES:
1. Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then NC.
3. If $\overline{BUSY}_R$ = L, then NC.
4. H = HIGH, L = LOW, X = DON'T CARE, NC = NO CHANGE

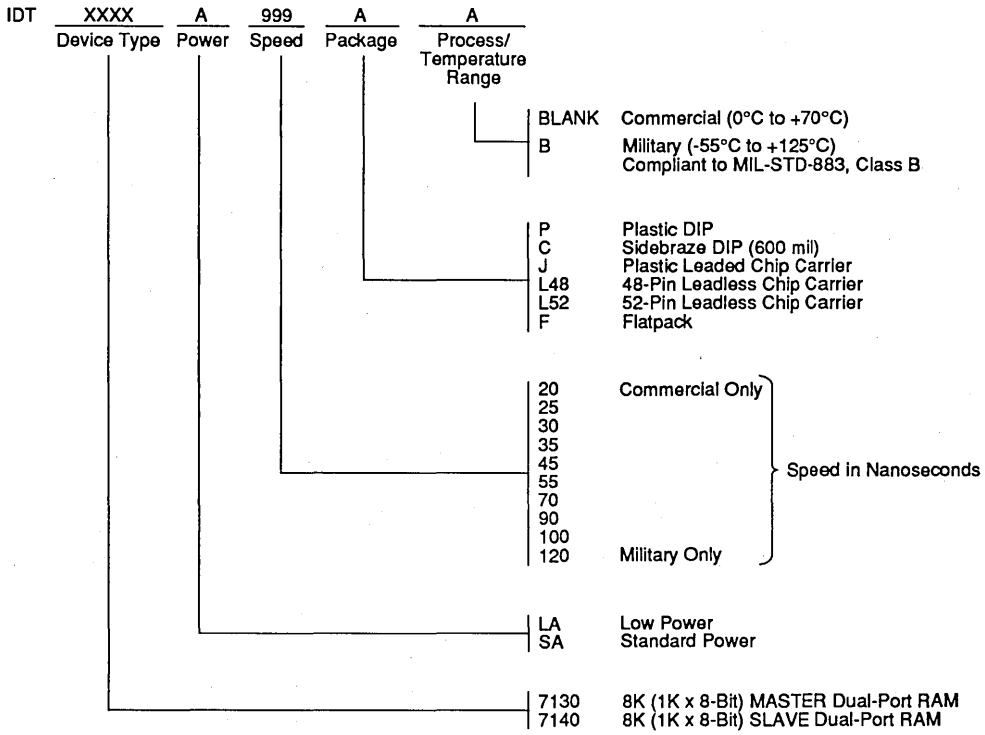
TABLE III – ARBITRATION (2)

Left Port		Right Port		Flags(1)		
$\overline{CE}_L$	A_{0L}-A_{9L}	$\overline{CE}_R$	A_{0R}-A_{9R}	$\overline{BUSY}_L$	$\overline{BUSY}_R$	Function
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	≠ A_{0R}-A_{9R}	L	≠ A_{0L}-A_{9L}	H	H	No Contention
Address Arbitration With $\overline{CE}$ Low Before Address Match						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ Arbitration With Address Match Before $\overline{CE}$						
LL5R	= A_{0R}-A_{9R}	LL5R	= A_{0L}-A_{9L}	H	L	L-Port Wins
RL5L	= A_{0R}-A_{9R}	RL5L	= A_{0L}-A_{9L}	L	H	R-Port Wins
LW5R	= A_{0R}-A_{9R}	LW5R	= A_{0L}-A_{9L}	H	L	Arbitration Resolved
LW5R	= A_{0R}-A_{9R}	LW5R	= A_{0L}-A_{9L}	L	H	Arbitration Resolved

2689 tbl 20

NOTES:
1. $\overline{INT}$ Flags Don't Care.
2. X = DON'T CARE, L = LOW, H = HIGH
   LV5R = Left Address Valid ≥ 5ns before right address.
   RV5L = Right Address Valid ≥ 5ns before left address.
   Same = Left and Right Addresses match within 5ns of each other.
   LL5R = Left $\overline{CE}$ = LOW ≥ 5ns before Right $\overline{CE}$.
   RL5L = Right $\overline{CE}$ = LOW ≥ 5ns before Left $\overline{CE}$.
   LW5R = Left and Right $\overline{CE}$ = LOW within 5ns of each other.

ORDERING INFORMATION



2689 drw 23

7

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 8K (1K x 8-BIT)

PRELIMINARY
IDT7030SA/LA
IDT7040SA/LA

FEATURES:

- High-speed access
  - —Military: 25/35/45ns (max.)
  - —Commercial: 20/25/35ns (max.)
- Low-power operation
  - —IDT7030/40SA
    - Active: 375mW (typ.)
    - Standby: 6mW (typ.)
  - —IDT7030/40LA
    - Active: 375mW (typ.)
    - Standby: 2mW (typ.)
- MASTER IDT7030 easily expands data bus width to 16-or-more-bits using SLAVE IDT7040
- On-chip port arbitration logic (IDT7030 only)
- $\overline{BUSY}$ output flag on IDT7030; $\overline{BUSY}$ input on IDT7040
- $\overline{INT}$ flag for port-to-port communication
- Fully asynchronous operation from either port
- Battery backup operation–2V data retention
- TTL-compatible, single 5V ±10% power supply
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7030/IDT7040 are high speed 1Kx8 dual-port static RAMs. The IDT7030 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7040 "SLAVE" dual-port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

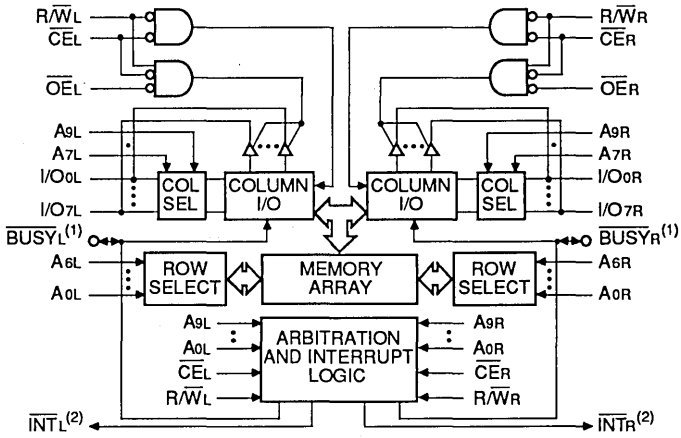
Both devices provide two independent ports with separate control, address and I/O pins that permit independent asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 375mW of power at maximum access times as fast as 20ns. Low-power (LA) versions offer battery backup data retention capability, with each dual-port typically consuming 200µw from a 2V battery.

The IDT7030/IDT7040 devices are packaged in 48-pin sidebraze or plastic DIPs.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



NOTE:

1. IDT7030 (MASTER): $\overline{BUSY}$ is open drain output and requires pullup resistor.
   IDT7040 (SLAVE): $\overline{BUSY}$ is input.
2. Open drain output: requires pullup resistor.

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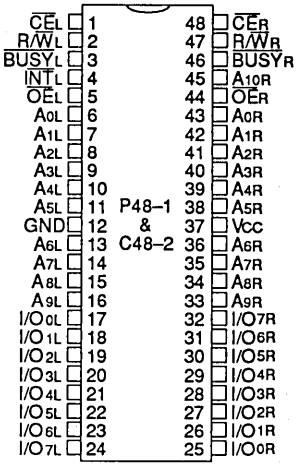
PIN CONFIGURATIONS



2690 drw 02

DIP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

2690 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

2690 tbl 02

NOTE:
1. VIL (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0v ± 10%
Commercial	0°C to +70°C	0V	5.0v ± 10%

2690 tbl 03

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Output Capacitance	VIN = 0V	11	pF

2690 tbl 04

NOTE:
1. This parameter is determined by device characterization but is not production tested.

7

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ±10%)

Symbol	Parameter	Test Conditions	IDT7030SA IDT7040SA Min.	IDT7030SA IDT7040SA Max.	IDT7030LA IDT7040LA Max.	IDT7030LA IDT7040LA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O_0-I/O_7)	I_{OL} = 4.0mA	—	0.4	—	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$, $\overline{INT}$)	I_{OL} = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2690 tbl 05

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version		7030 x 20[2] 7040 x 20[2] Typ.	7030 x 20[2] 7040 x 20[2] Max.	7030 x 25 7040 x 25 Typ.	7030 x 25 7040 x 25 Max.	7030 x 35 7040 x 35 Typ.	7030 x 35 7040 x 35 Max.	7030 x 45[3] 7040 x 45[3] Typ.	7030 x 45[3] 7040 x 45[3] Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	Mil.	SA	—	—	75	300	75	280	75	270	mA
				LA	—	—	75	220	75	200	75	190	
			Com'l.	SA	75	260	75	250	75	240	—	—	
				LA	75	190	75	180	75	180	—	—	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE_L}$ and $\overline{CE_R}$ ≥ V_{IH} f = f_{MAX}[4]	Mil.	SA	—	—	25	75	25	75	25	75	mA
				LA	—	—	25	55	25	55	25	55	
			Com'l.	SA	25	65	25	65	25	65	—	—	
				LA	25	45	25	45	25	45	—	—	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE_L}$ or $\overline{CE_R}$ ≥ V_{IH} Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	—	—	50	180	46	170	40	160	mA
				LA	—	—	50	140	46	130	40	125	
			Com'l.	SA	50	180	50	170	46	155	—	—	
				LA	50	130	50	120	46	110	—	—	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE_L}$ and $\overline{CE_R}$ ≥ Vcc -0.2V V_{IN} ≥ Vcc -0.2V or V_{IN} ≤ 0.2V, f = 0[5]	Mil.	SA	—	—	1.2	40	1.2	35	1.0	35	mA
				LA	—	—	0.4	10	0.4	10	0.2	10	
			Com'l.	SA	1.2	15	1.2	15	1.2	15	—	—	
				LA	0.4	4	0.4	4	0.4	4	—	—	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs, f = 0[5])	One Port $\overline{CE_L}$ or $\overline{CE_R}$ ≥ Vcc -0.2V V_{IN} ≥ Vcc -0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	—	—	50	170	45	150	40	140	mA
				LA	—	—	46	135	42	115	35	105	
			Com'l.	SA	50	160	50	150	45	135	—	—	
				LA	46	125	46	115	42	105	—	—	

2690 tbl 06

NOTES:
1. x in part numbers indicates power rating (SA or LA).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of $1/t_{RC}$, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.

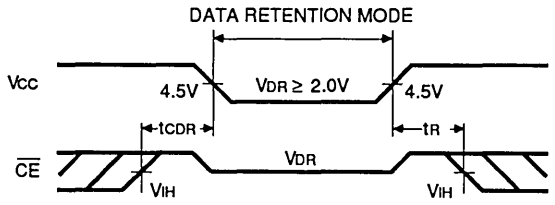
DATA RETENTION CHARACTERISTICS (LA Version Only)

Symbol	Parameter	Test Conditions		IDT7030LA/IDT7040LA Min.	Typ.[1]	Max.	Unit
V_{DR}	Vcc for Data Retention	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$		2.0	—	0	V
I_{CCDR}	Data Retention Current		Mil.	—	100	4000	µA
			Com'l.	—	100	1500	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

2690 tbl 07

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM



2690 drw 03

AC TEST CONDITIONS

Input Pulse Levels	GND TO 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 & 3

2690 tbl 08

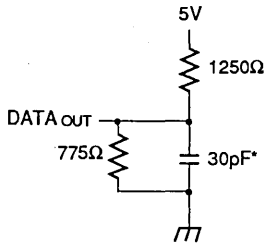


Figure 1. Output Load

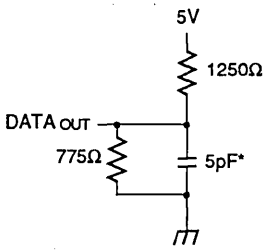


Figure 2. Output Load (for tHZ, tLZ, tWZ, and tOW)

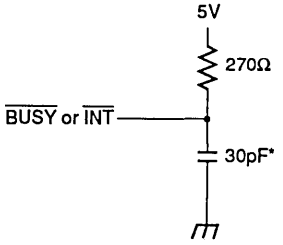


Figure 3. $\overline{BUSY}$ and $\overline{INT}$ Output Load

2690 drw 04

* Including scope and jig

7

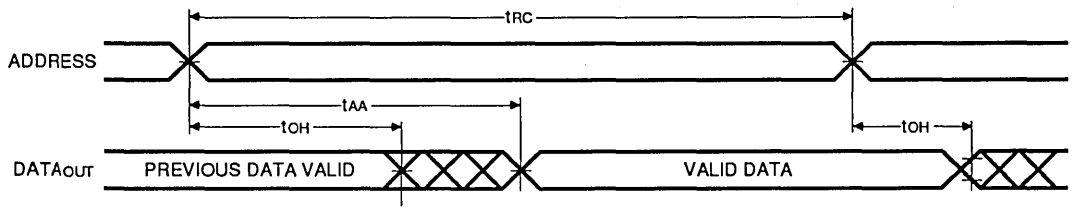
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[5]

Symbol	Parameter	7030 x 20[2] 7040 x 20[2] Min.	Max.	7030 x 25 7040 x 25 Min.	Max.	7030 x 35 7040 x 35 Min.	Max.	7030 x 45[3] 7040 x 45[3] Min.	Max.	Unit
Read Cycle										
tRC	Read Cycle Time	20	—	25	—	35	—	45	—	ns
tAA	Address Access Time	—	20	—	25	—	35	—	45	ns
tACE	Chip Enable Access Time	—	20	—	25	—	35	—	45	ns
tAOE	Output Enable Access Time	—	10	—	12	—	25	—	30	ns
tOH	Output Hold From Address Change	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time[1,4]	0	—	0	—	0	—	0	—	ns
tHZ	Output High Z Time[1,4]	—	8	—	10	—	15	—	20	ns
tPU	Chip Enable to Power Up Time[4]	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[4]	—	50	—	50	—	50	—	50	ns

2690 tbl 09

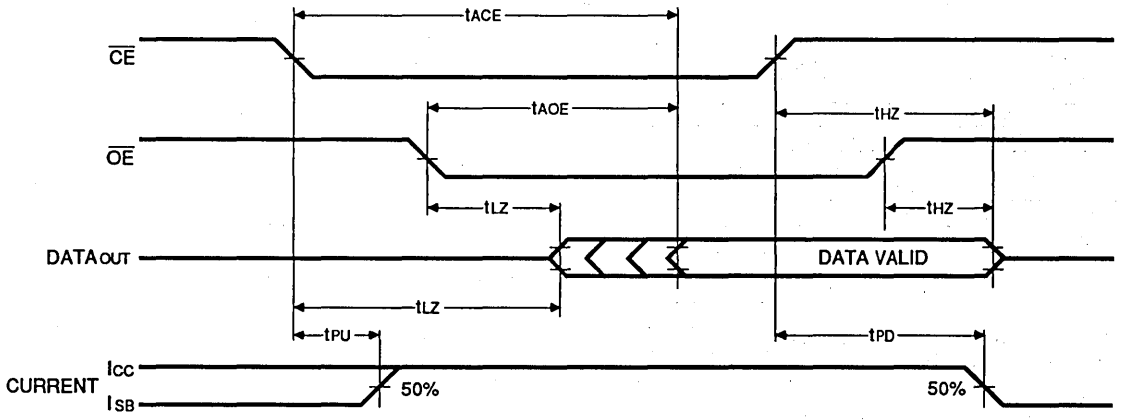
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. "x" in part numbers indicates power rating (SA or LA).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE [1,2,4]



2690 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1,3)



2690 drw 06

NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = VIL.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = VIL.

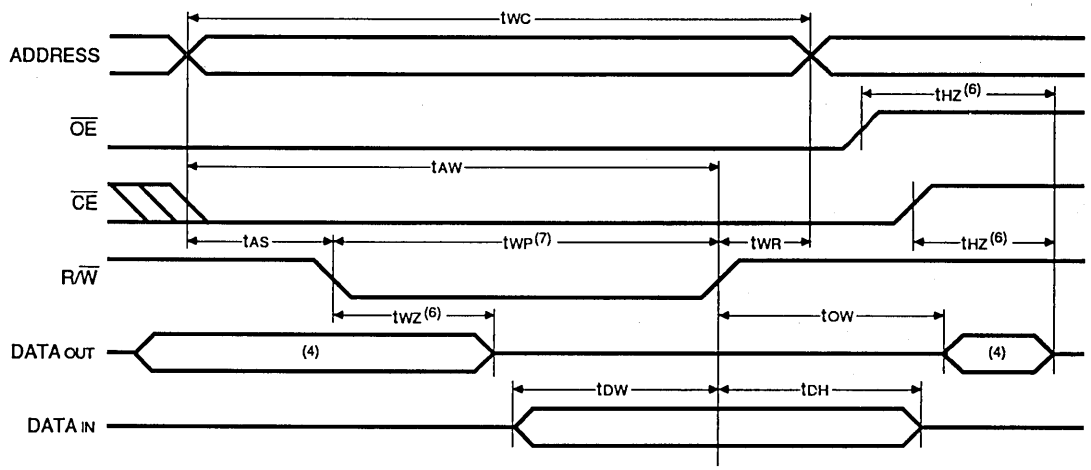
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[7]

Symbol	Parameter	7030 x 20[2] 7040 x 20[2] Min.	Max.	7030 x 25 7040 x 25 Min.	Max.	7030 x 35 7040 x 35 Min.	Max.	7030 x 45[3] 7040 x 45[3] Min.	Max.	Unit
Write Cycle										
tWC	Write Cycle Time[5]	20	—	25	—	35	—	45	—	ns
tEW	Chip Enable to End of Write	15	—	20	—	30	—	35	—	ns
tAW	Address Valid to End of Write	15	—	20	—	30	—	35	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width[6]	15	—	20	—	30	—	35	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	10	—	12	—	20	—	20	—	ns
tHZ	Output High Z Time[1,4]	—	8	—	10	—	15	—	20	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z[1,4]	—	8	—	10	—	15	—	20	ns
tOW	Output Active From End of Write[1,4]	0	—	0	—	0	—	0	—	ns

2690 tbl 10

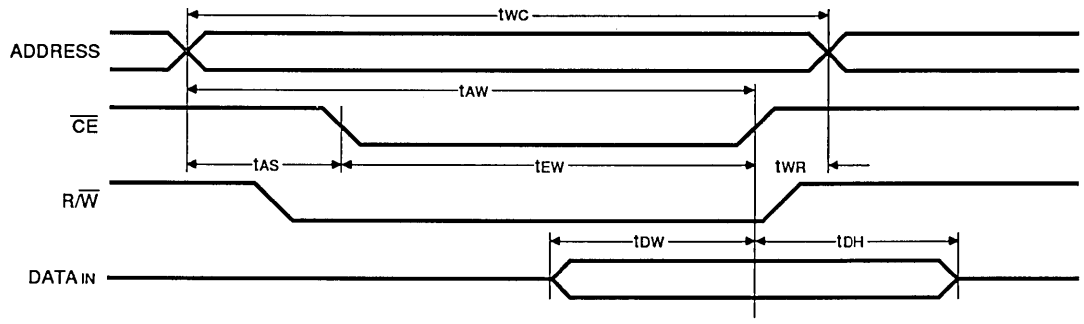
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, $t_{WC} = t_{BAA} + t_{WP}$.
6. Specified for $\overline{OE}$ at high (Refer to "Timing Waveform of Write Cycle", Note 7)
7. "x" in part numbers indicates power rating (SA or LA).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/$\overline{W}$ CONTROLLED TIMING)(1,2,3,7)



2690 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING)(1,2,3,5)



2690 drw 08

NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

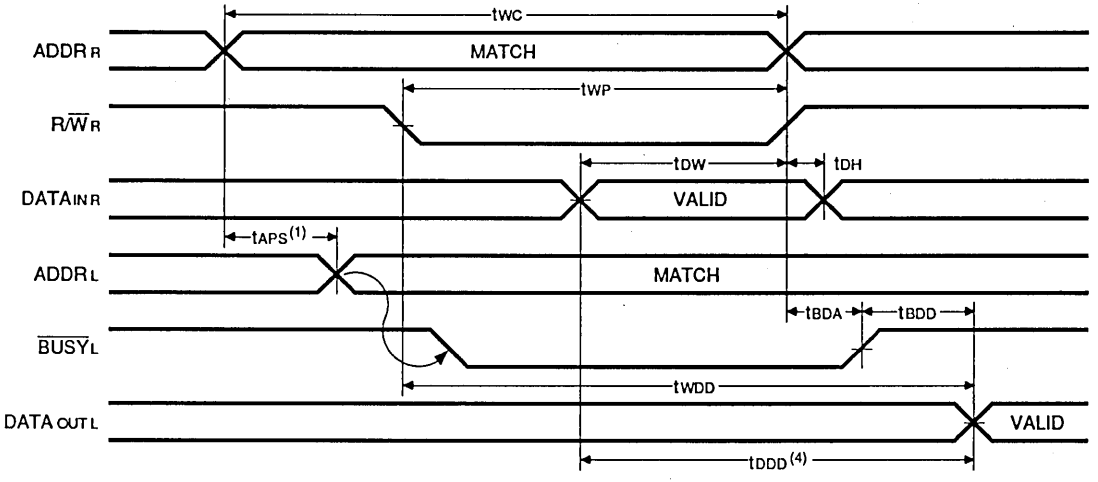
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(8)

Symbol	Parameter	7030 x 20(1) 7040 x 20(1) Min.	Max.	7030 x 25 7040 x 25 Min.	Max.	7030 x 35 7040 x 35 Min.	Max.	7030 x 45(2) 7040 x 45(2) Min.	Max.	Unit
Busy Timing (For Master IDT7030 Only)										
tBAA	$\overline{BUSY}$ Access Time to Address	—	20	—	25	—	35	—	35	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	18	—	20	—	30	—	35	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable	—	20	—	20	—	30	—	30	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable	—	18	—	20	—	25	—	25	ns
tWDD	Write Pulse to Data Delay (3)	—	45	—	50	—	60	—	70	ns
tDDD	Write Data Valid to Read Data Delay (3)	—	30	—	35	—	45	—	55	ns
tAPS	Arbitration Priority Set-up Time (4)	5	—	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data (5)	—	Note 5	—	Note 5	—	Note 5	—	Note 5	ns
Busy Input Timing (For Slave IDT7040 Only)										
tWB	Write to $\overline{BUSY}$ Input (6)	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$ (7)	12	—	15	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay (9)	—	45	—	50	—	60	—	70	ns
tDDD	Write Data Valid to Read Data Delay (9)	—	30	—	35	—	45	—	55	ns

2690 tbl 11

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (For Master IDT7030 only)".
4. To ensure that the earlier of the two ports wins.
5. tBDD is a calculated parameter and is the greater of 0, tWDD-tWP (actual) or tDDD-tDW (actual).
6. To ensure that the write cycle is inhibited during contention.
7. To ensure that a write cycle is completed after contention.
8. "x" in part numbers indicates power rating (SA or LA).
9. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With Port-to-Port Delay (For Slave IDT7040 Only)".

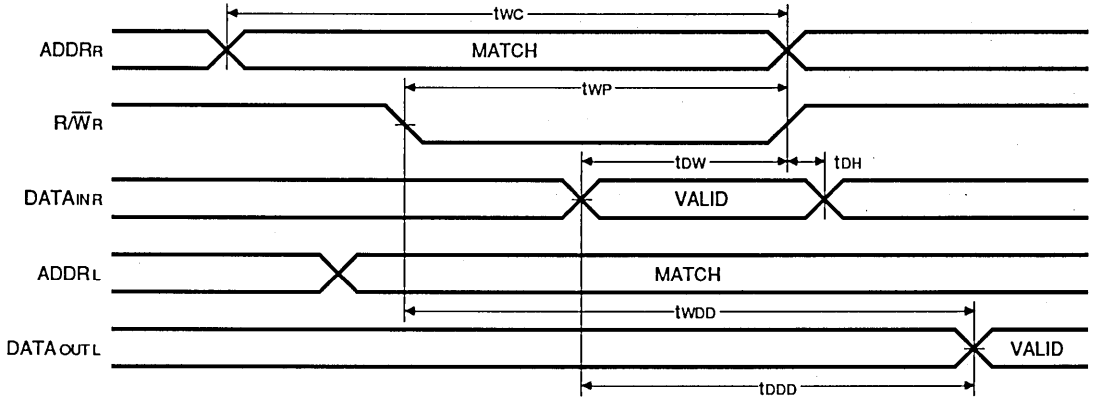
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$ (1,2,3) (FOR MASTER IDT7030 ONLY)



2690 drw 09

NOTES:
1. To ensure that the earlier of the two ports wins.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.
4. $\overline{OE}$ at LO for the reading port.

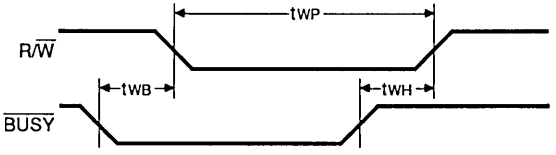
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY (1,2,3) (FOR SLAVE IDT7040 ONLY)



2690 drw 10

NOTES:
1. Assume $\overline{BUSY}$ input at HI for the writing port, and $\overline{OE}$ at LO for the reading port.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.

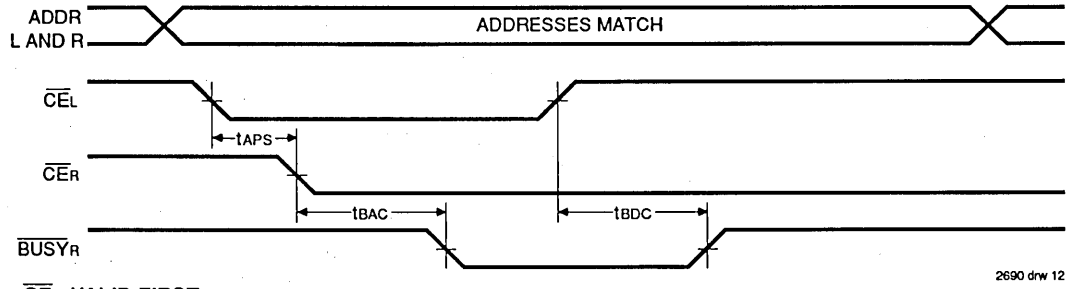
TIMING WAVEFORM OF WRITE WITH BUSY INPUT (FOR SLAVE IDT7040 ONLY)



2690 drw 11

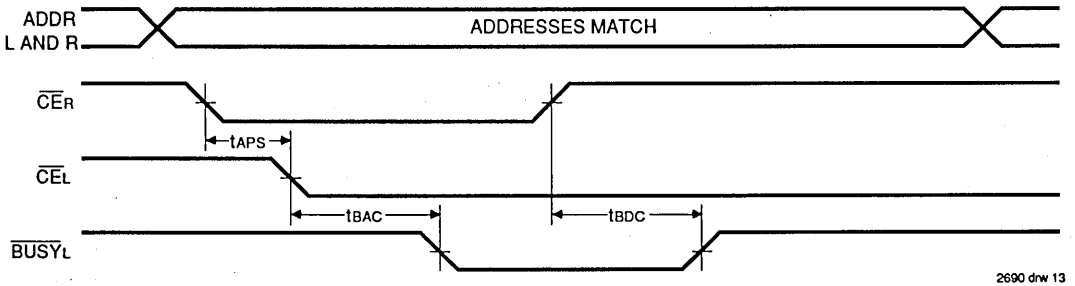
TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION (FOR MASTER IDT7030 ONLY)

$\overline{CE}_L$ VALID FIRST:



2690 drw 12

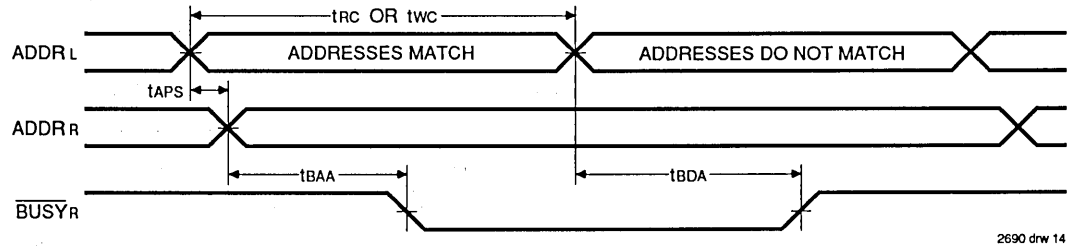
$\overline{CE}_R$ VALID FIRST:



2690 drw 13

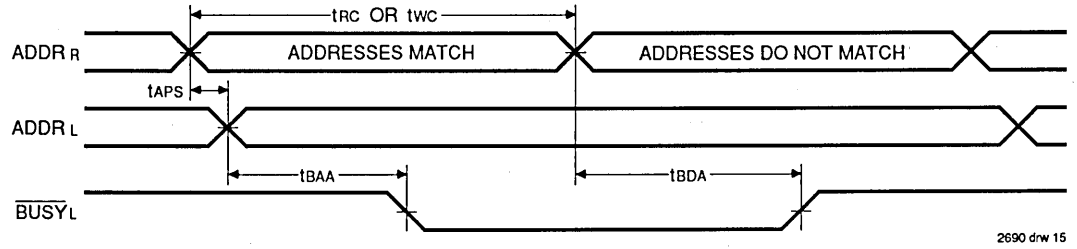
TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION (1) (FOR MASTER IDT7030 ONLY)

LEFT ADDRESS VALID FIRST:



2690 drw 14

RIGHT ADDRESS VALID FIRST:



2690 drw 15

NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (3)

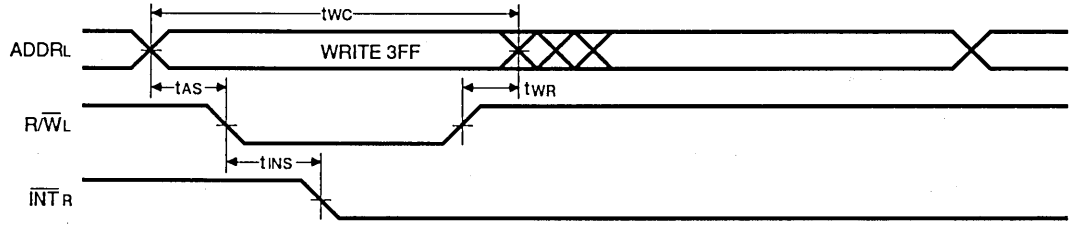
Symbol	Parameter	7030 x 20(1) 7040 x 20(1) Min.	Max.	7030 x 25 7040 x 25 Min.	Max.	7030 x 35 7040 x 35 Min.	Max.	7030 x 45(2) 7040 x 45(2) Min.	Max.	Unit
Interrupt Timing										
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tINS	Interupt Set Time	—	20	—	25	—	35	—	40	ns
tINR	Interupt Reset Time	—	20	—	25	—	35	—	40	ns

2690 tbl 12

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. "x" in part numbers indicates power rating (SA or LA).

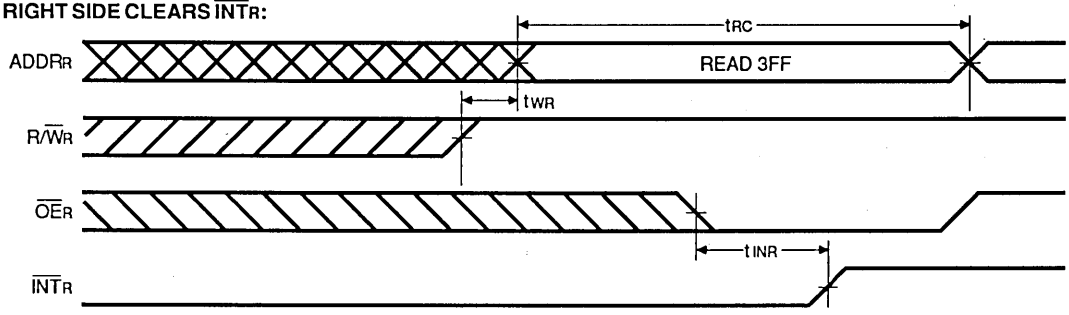
TIMING WAVEFORM OF INTERUPT MODE(1, 2)

LEFT SIDE SETS $\overline{INT}_R$:



2690 drw 16

RIGHT SIDE CLEARS $\overline{INT}_R$:



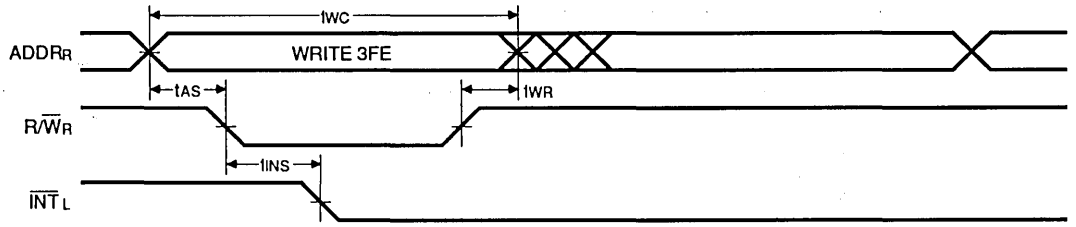
2690 drw 17

NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
2. $\overline{INT}_L$ and $\overline{INT}_R$ are reset (high) during power up.

7

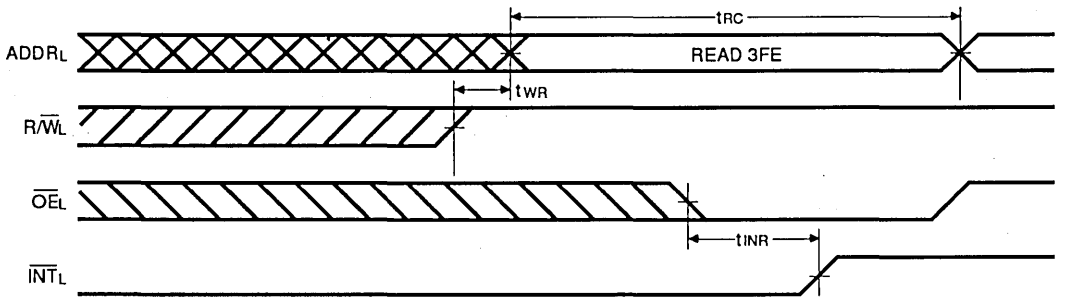
TIMING WAVEFORM OF INTERRUPT MODE (1, 2)

RIGHT SIDE SETS $\overline{INT}_L$:



2690 drw 18

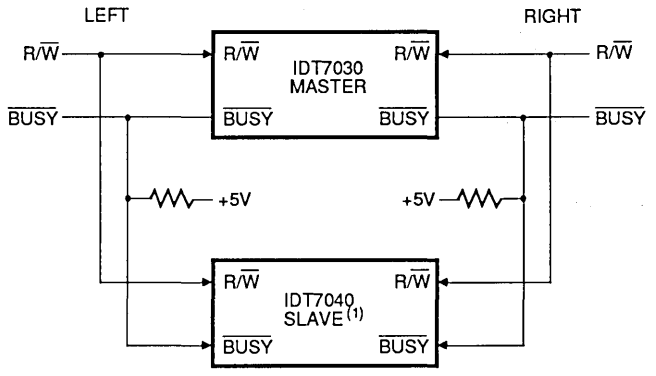
LEFT SIDE CLEARS $\overline{INT}_L$:



2690 drw 19

NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
2. $\overline{INT}_R$ and $\overline{INT}_L$ are reset (high) during power up.

16-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



2690 drw 20

NOTE:
1. No arbitration in IDT7040 (SLAVE). $\overline{BUSY}$-IN inhibits write in IDT7040 (SLAVE).

FUNCTIONAL DESCRIPTION

The IDT7030/IDT7040 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any locations in memory. The IDT7030/IDT7040 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table 1.

The interrupt flag ($\overline{INT}$) permits communication between ports or systems. If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is set when the right port writes to memory location 3FE (HEX). The left port clears the interrupt by reading address location 3FE (HEX). Likewise, the right port interrupt flag ($\overline{INT}_R$) is set when the left port writes to memory location 3FF (HEX) and to clear the interrupt flag ($\overline{INT}_R$) the right port must read the memory location 3FF. The message (8-bits) at 3FE or 3FF is user defined. If the interrupt function is not used, address locations 3FE or 3FF are not used as mailboxes, but as part of the random access memory. Refer to Table II for the interrupt operation.

ARBITRATION LOGIC FUNCTIONAL DESCRIPTION

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table II). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION MASTER/SLAVE DESCRIPTION

Expanding the data bus width to sixteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another acitivates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one arbitrator, in the MASTER, is used. The SLAVE has BUSY inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMS in width, the writing of the SLAVE RAMS must be delayed, until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than on chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

7

TRUTH TABLES

TABLE I – NON-CONTENTION READ/WRITE CONTROL[4]

Left Or Right Port[1]				Function
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	
X	H	X	Z	Port Disabled and in Power Down Mode I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R$ = $\overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	DATAIN	Data on Port Written into Memory[2]
H	L	L	DATAOUT	Data in Memory Output on Port[3]
H	L	H	Z	High Impedance Outputs

2690 tbl 13

NOTES:
1. $A_{0L} - A_{9L} \neq A_{0R} - A_{9R}$
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

TABLE II – INTERRUPT FLAG[1, 4]

Left Port					Right Port					Function
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{0L} - A_{9L}$	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{0L} - A_{9R}$	$\overline{INT}_R$	
L	L	X	3FF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	3FF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	3FE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	3FE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

2690 tbl 14

NOTES:
1. Assume $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then NC.
3. If $\overline{BUSY}_R$ = L, then NC.
4. H = HIGH, L = LOW, X = DON'T CARE, NC = NO CHANGE.

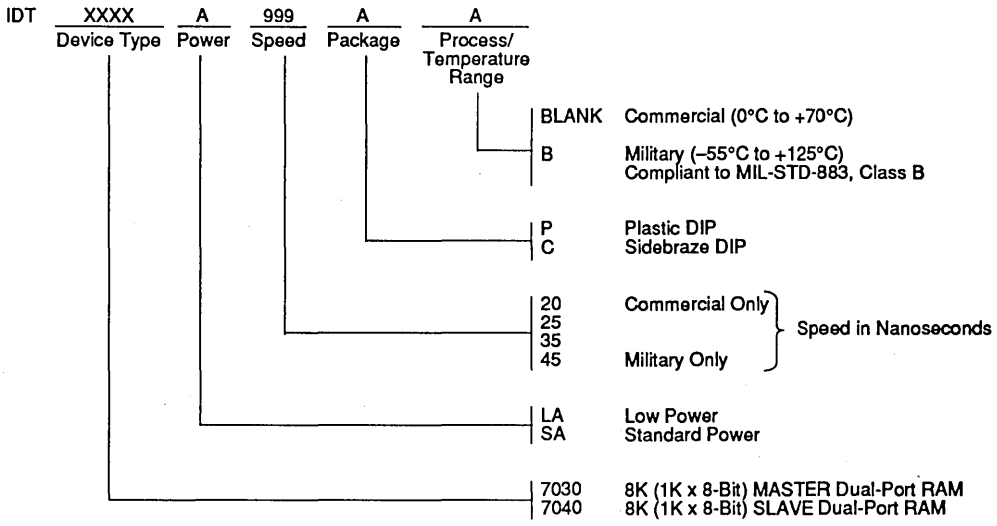
TABLE II – ARBITRATION[1, 2]

Left Port		Right Port		Flags[1]		Function
$\overline{CE}_L$	$A_{0L} - A_{9L}$	$\overline{CE}_R$	$A_{0R} - A_{9R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	≠ A_{0R} - A_{9R}	L	≠ A_{0L} - A_{9L}	H	H	No Contention
Address Arbitration With $\overline{CE}$ Low Before Address Match						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ Arbitration With Address Match Before $\overline{CE}$						
LL5R	= A_{0R} - A_{9R}	LL5R	= A_{0L} - A_{9L}	H	L	L-Port Wins
RL5L	= A_{0R} - A_{9R}	RL5L	= A_{0L} - A_{9L}	L	H	R-Port Wins
LW5R	= A_{0R} - A_{9R}	LW5R	= A_{0L} - A_{9L}	H	L	Arbitration Resolved
LW5R	= A_{0R} - A_{9R}	LW5R	= A_{0L} - A_{9L}	L	H	Arbitration Resolved

2690 tbl 15

NOTES:
1. $\overline{INT}$ Flags Don't Care.
2. X = DON'T CARE, L = LOW, H = HIGH
   LV5R = Left Address Valid ≥ 5ns before right address.
   RV5L = Right Address Valid ≥ 5ns before left address.
   Same = Left and Right Addresses match within 5ns of each other.
   LL5R = Left $\overline{CE}$ = LOW ≥ 5ns before Right $\overline{CE}$.
   RL5L = Right $\overline{CE}$ = LOW ≥ 5ns before Left $\overline{CE}$.
   LW5R = Left and Right $\overline{CE}$ = LOW within 5ns of each other.

ORDERING INFORMATION



2690 drw 21

7

Integrated Device Technology, Inc.

HIGH-SPEED 1K x 9 DUAL-PORT STATIC RAM WITH BUSY

PRELIMINARY
IDT7010S/L
IDT70104S/L

FEATURES:

- High-speed access
  - — Military: 35/45/55/70ns (max.)
  - — Commercial: 25/35/45/55ns (max.)
- Low-power operation
  - — IDT7010/70104S
    Active: 400mW (typ.)
    Standby: 7mW (typ.)
  - — IDT7010/70104L
    Active: 400mW (typ.)
    Standby: 2mW (typ.)
- Fully asynchronous operation from either port
- Each port has a 9-bit wide data path. The 9th bit could be used as the parity bit.
- MASTER IDT7010 easily expands data bus width to 18 bits or more using SLAVE IDT70104 chip.
- On-chip port arbitration logic (IDT7010 only)
- $\overline{BUSY}$ output flag on MASTER; $\overline{BUSY}$ input on SLAVE
- Battery backup operation — 2V data retention
- TTL compatible, signal 5V (±10%) power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7010/IDT70104 are high-speed 1K X 9 dual-port static RAMs. The IDT7010 is designed to be used as a stand-alone 9-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT70104 "SLAVE" dual-port in 18-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 18-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

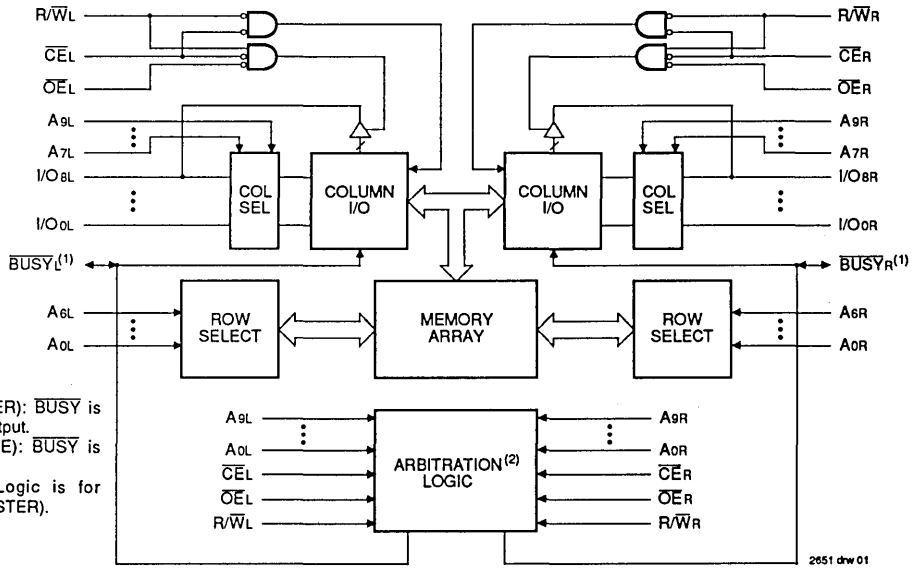
Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

The devices utilize a 9-bit wide data path to allow for control/data and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 400mW of power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability with each port typically consuming 200µW from a 2V battery.

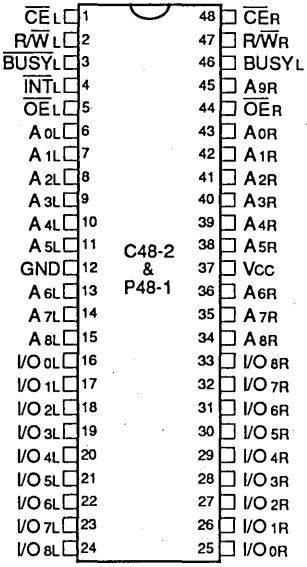
The IDT7010/IDT70104 devices are packaged in 48-pin sidebrazed or plastic DIPs, 48-pin LCCs and 48-pin flatpacks. The military devices are processed 100% in compliance to the test methods of MIL-STD-883, Method 5004.

FUNCTIONAL BLOCK DIAGRAM



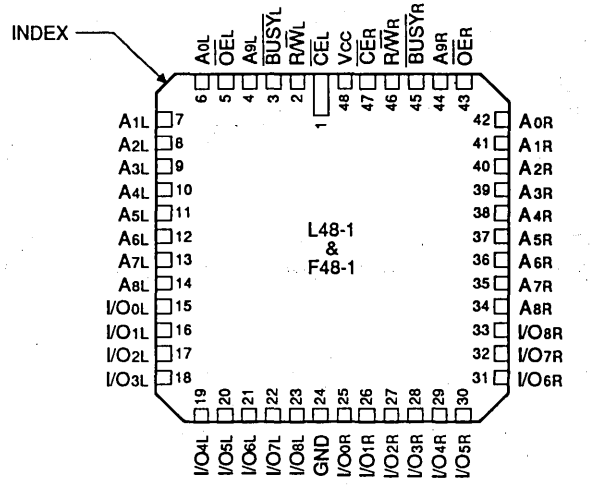
NOTE:
1. 7010 (MASTER): $\overline{BUSY}$ is totem-pole output.
   70104 (SLAVE): $\overline{BUSY}$ is input.
2. Arbitration Logic is for IDT7010 (MASTER).

PIN CONFIGURATIONS



2651 drw 02

48-PIN DIP
TOP VIEW



2651 drw 03

48-PIN LCC/FLATPACK
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2651 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0.0	V
VIH	Input High Votage	2.2	–	6.0	V
VIL	Input Low Voltage	–0.5(1)	–	0.8	V

NOTE: 2651 tbl 02

1. VIL (min.) = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2651 tbl 03

7

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	7010S 70104S Min.	7010S 70104S Max.	7010L 70104L Min.	7010L 70104L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O_0 – I/O_8), $\overline{BUSY}$	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage (I/O_0 – I/O_8), $\overline{BUSY}$	I_{OH} = –4mA	2.4	—	2.4	—	V

2651 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7010 x 25[2] 70104 x 25[2] Typ.	7010 x 25[2] 70104 x 25[2] Max.	7010 x 35 70104 x 35 Typ.	7010 x 35 70104 x 35 Max.	7010 x 45 70104 x 45 Typ.	7010 x 45 70104 x 45 Max.	7010 x 55 70104 x 55 Typ.	7010 x 55 70104 x 55 Max.	7010 x 70[3] 70104 x 70[3] Typ.	7010 x 70[3] 70104 x 70[3] Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \le V_{IL}$ Outputs Open f = f_{MAX}[4]	Mil.	S	—	—	80	300	75	290	70	285	65	275	mA
				L	—	—	80	220	75	210	70	205	65	200	
			Com'l.	S	75	260	75	250	75	245	70	235	—	—	
				L	75	190	75	180	75	170	70	160	—	—	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \ge V_{IH}$ f = f_{MAX}[4]	Mil.	S	—	—	25	80	25	80	25	80	25	65	mA
				L	—	—	25	60	25	60	25	60	25	55	
			Com'l.	S	25	65	25	65	25	65	25	65	—	—	
				L	25	45	25	45	25	45	25	45	—	—	
I_{SB2}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \ge V_{IH}$ Active Port Outputs Open, f = f_{MAX}[4]	Mil.	S	—	—	50	190	45	170	40	170	40	165	mA
				L	—	—	50	145	45	140	40	140	40	135	
			Com'l.	S	50	175	46	160	45	150	40	140	—	—	
				L	50	125	46	115	45	105	40	95	—	—	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \ge$ V_{CC} – 0.2V $V_{IN} \ge V_{CC}$ – 0.2V or $V_{IN} \le$ 0.2V, f = 0[5]	Mil.	S	—	—	1.2	30	1.0	30	1.0	30	1.0	30	mA
				L	—	—	0.4	10	0.2	10	0.2	10	0.2	10	
			Com'l.	S	1.2	15	1.0	15	1.0	15	1.0	15	—	—	
				L	0.4	5	0.4	5.0	0.2	5.0	0.2	5.0	—	—	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ – 0.2V, $V_{IN} \ge$ V_{CC} – 0.2V or $V_{IN} \le$ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	Mil.	S	—	—	47	170	45	160	40	155	40	150	mA
				L	—	—	44	130	42	125	35	120	35	115	
			Com'l.	S	50	155	45	142	45	132	45	127	—	—	
				L	46	120	42	110	42	100	42	95	—	—	

2651 tbl 05

NOTES:
1. "x" in part numbers indicates power rating (S or L).
2. 0°C to +70°C temperature range only.
3. –55°C to +125°C temperature range only.
4. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.

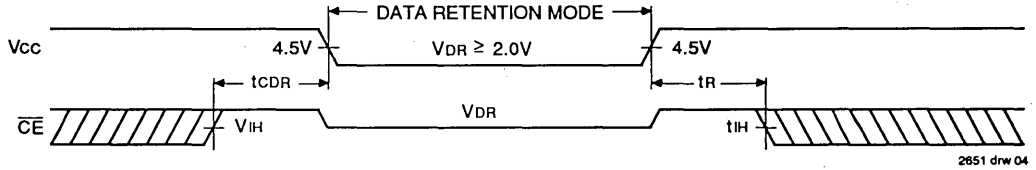
DATA RETENTION CHARACTERISTICS (L Version Only)

Symbol	Parameter	Test Condition		7010L/70104L Min.	Typ.(1)	Max.	Unit
V_{DR}	Vcc for Data Retention			2.0	—	—	V
I_{CCDR}	Data Retention Current	Vcc = 2.0V, $\overline{CE} \geq V_{CC} - 0.2V$	Mil.	—	100	4000	µA
			Com'l.	—	100	1500	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		0	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	ns

NOTES:
1. Vcc = 2V, TA = +25°C
2. tRC = Read Cycle Time
3. This parameter is guaranteed but not tested.

2651tbl 06

DATA RETENTION WAVEFORM



2651 drw 04

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 & 3

2651 tbl 07

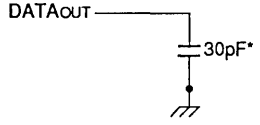
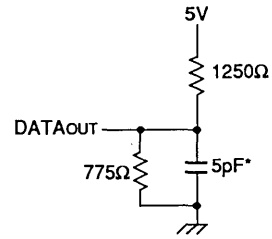


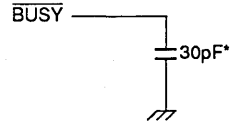
Figure 1. Output Load

2651 drw 05



2651 drw 06

Figure 2. Output Load (for tHZ, tLZ, tWZ, and tOW)



2651 drw 07

Figure 3. $\overline{BUSY}$ Output Load

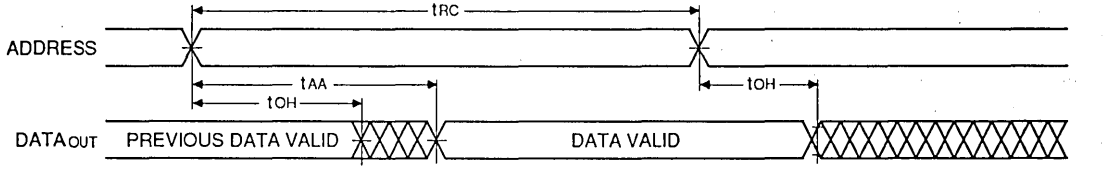
*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[5]

Symbol	Parameter	7010 x 25[2] 70104 x 25[2]		7010 x 35 70104 x 35		7010 x 45 70104 x 45		7010 x 55 70104 x 55		7010 x 70[3] 70104 x 70[3]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
tRC	Read Cycle Time	25	—	35	—	45	—	55	—	70	—	ns
tAA	Address Access Time	—	25	—	35	—	45	—	55	—	70	ns
tACE	Chip Enable Access Time	—	25	—	35	—	45	—	55	—	70	ns
tAOE	Output Enable Access Time	—	12	—	25	—	30	—	35	—	40	ns
tOH	Output Hold From Address Change	0	—	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time[1, 4]	0	—	0	—	0	—	0	—	0	—	ns
tHZ	Output High Z Time[1, 4]	—	10	—	15	—	20	—	30	—	35	ns
tPU	Chip Enable to Power Up Time[4]	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[4]	—	50	—	50	—	50	—	50	—	50	ns

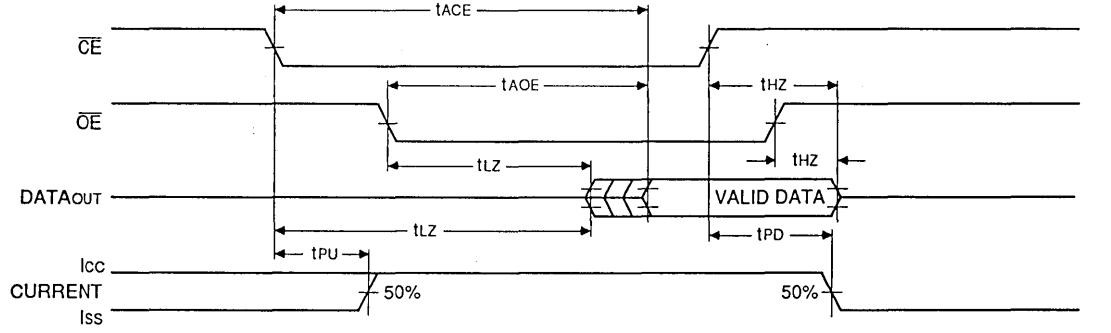
NOTES:
2651tbl 08
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. –55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. "x" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1, 2, 4]



2651 drw 09

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE[1, 3]



2651 drw 10

NOTES:
1. R/W is high for Read Cycles.
2. Device is continuously enabled, CE = VIL.
3. Addresses valid prior to or coincident with CE transition low.
4. OE = VIL.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[7]

Symbol	Parameter	7010 x 25[2] 70104 x 25[2]		7010 x 35 70104 x 35		7010 x 45 70104 x 45		7010 x 55 70104 x 55		7010 x 70[3] 70104 x 70[3]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle												
tWC	Write Cycle Time[5]	25	—	35	—	45	—	55	—	70	—	ns
tEW	Chip Enable to End of Write	20	—	30	—	35	—	40	—	50	—	ns
tAW	Address Valid to End of Write	20	—	30	—	35	—	40	—	50	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width[6]	20	—	30	—	35	—	40	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	12	—	20	—	20	—	20	—	30	—	ns
tHZ	Output High Z Time[1, 4]	—	10	—	15	—	20	—	30	—	35	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z[1, 4]	—	10	—	15	—	20	—	30	—	35	ns
tOW	Output Active From End of Write[1, 4]	0	—	0	—	0	—	0	—	0	—	ns

NOTES: 2651 tbl 09
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. –55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, tWC = tBAA + tWP.
6. Specified for $\overline{OE}$ at high (refer to "Timing Waveform of Write Cycle", Note 7).
7. "x" in part numbers indicates power rating (S or L).

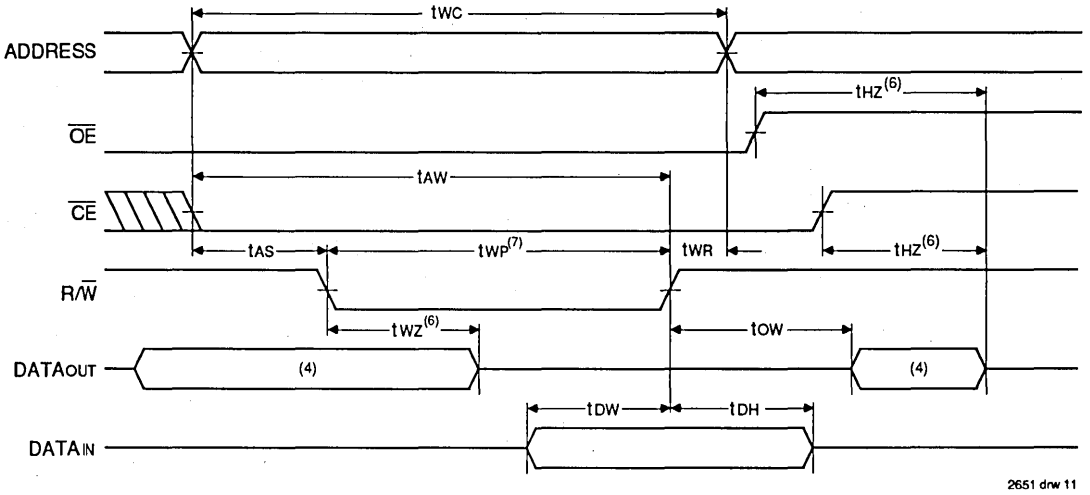
CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Output Capacitance	VOUT = 0V	11	pF

NOTE: 2651 tbl 10
1. This parameter is determined by device characterization but is not production tested.

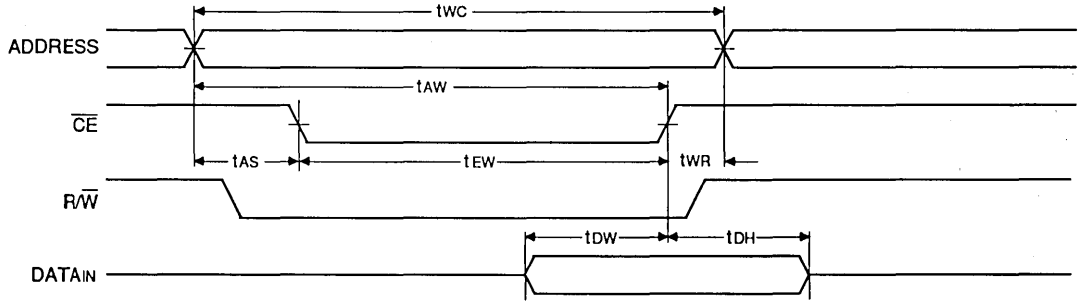
7

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/$\overline{W}$ CONTROLLED TIMING)(1, 2, 3, 7)



2651 drw 11

TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING)(1, 2, 3, 5)



2651 drw 12

NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or tWZ + tDW to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during as R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[8]

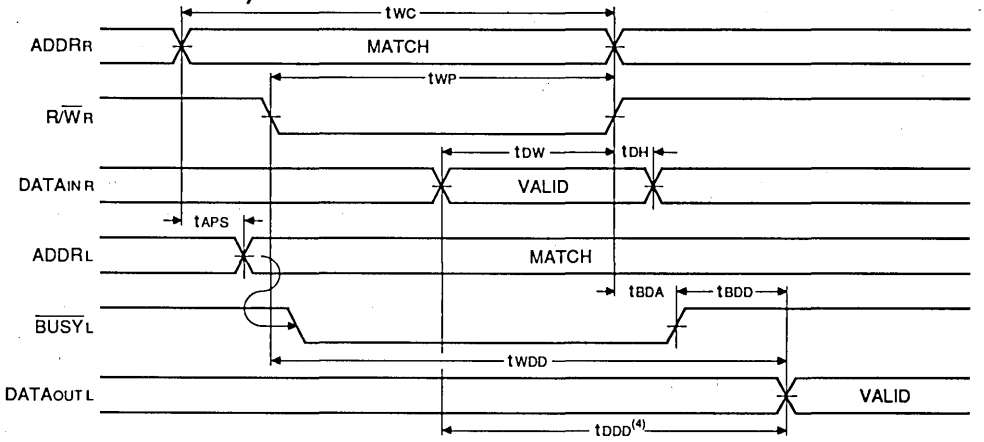
Symbol	Parameter	70101 x 25[1] 70105 x 25[1]		70101 x 35 70105 x 35		70101 x 45 70105 x 45		70101 x 55 70105 x 55		70101 x 70[2] 70105 x 70[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Busy Timing (For Master IDT7010 Only)												
tBAA	$\overline{BUSY}$ Access Time to Address	—	25	—	35	—	35	—	45	—	45	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	20	—	30	—	35	—	40	—	40	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable	—	20	—	30	—	30	—	35	—	35	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable	—	20	—	25	—	25	—	30	—	30	ns
tWDD	Write Pulse to Data Delay[3]	—	50	—	60	—	70	—	80	—	95	ns
tDDD	Write Data Valid to Read Data Delay[3]	—	35	—	45	—	55	—	65	—	80	ns
tAPS	Arbitration Priority Set-up Time[4]	5	—	5	—	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[5]	—	Note 5	—	Note 5	—	Note 5	—	Note 5	—	Note 5	ns
Busy Input Timing (For Slave IDT70104 Only)												
tWB	Write to $\overline{BUSY}$ Input[6]	0	—	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[7]	15	—	20	—	20	—	20	—	20	—	ns
tWDD	Write Pulse to Date Delay[9]	—	50	—	60	—	70	—	80	—	95	ns
tDDD	Write Data Valid to Read Data Delay[9]	—	35	—	45	—	55	—	65	—	80	ns

2651 tbl 11

NOTES:
1. 0°C to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (For MASTER IDT7010 only)".
4. To ensure that the earlier of the two ports wins.
5. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
6. To ensure that a write cycle is inhibited during contention.
7. To ensure that a write cycle is completed after contention.
8. "x" in part numbers indicates power rating (S or L).
9. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ Port-to-port Delay (For SLAVE IDT70104 only)".

7

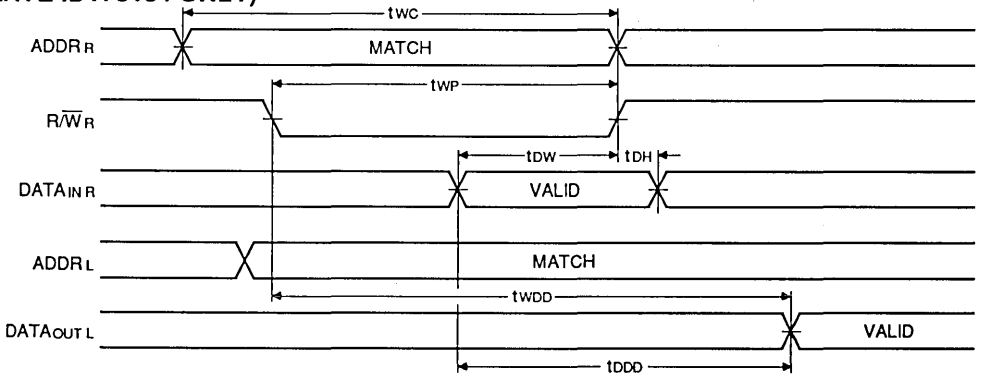
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$[1, 2, 3] (FOR MASTER IDT7010 ONLY)



2651 drw 13

NOTES:
1. To ensure that the earlier of the two ports wins.
2. Write Cycle parameters should be adhered to, in order to ensure proper writing.
3. Device is continuously enabled for both ports.
4. $\overline{OE}$ at LOW for the reading port.

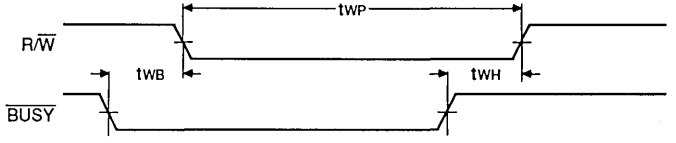
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY[1, 2, 3] (FOR SLAVE IDT70104 ONLY)



2651 drw 14

NOTES:
1. Assume $\overline{BUSY}$ input at HIGH for the writing port, and $\overline{OE}$ at LOW for the reading port.
2. Write Cycle parameters should be adhered to, in order to ensure proper writing.
3. Device is continuously enabled for both ports.

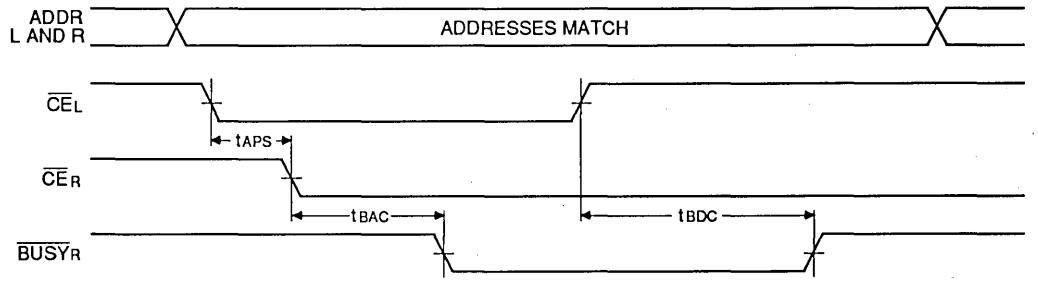
TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ INPUT (FOR SLAVE IDT70104 ONLY)



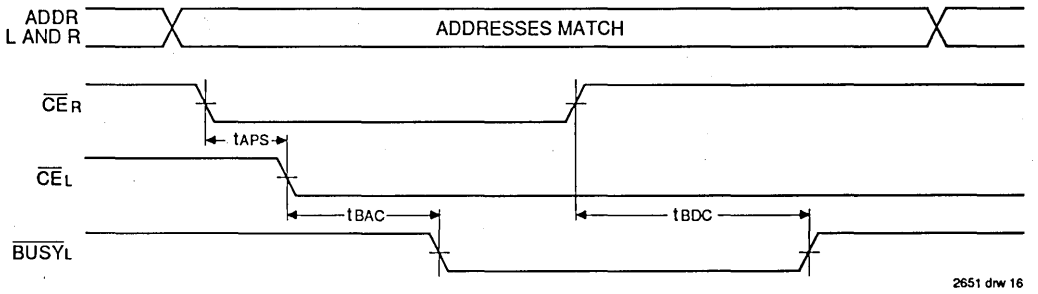
2651 drw 15

TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION

$\overline{CE}_L$ Valid First:



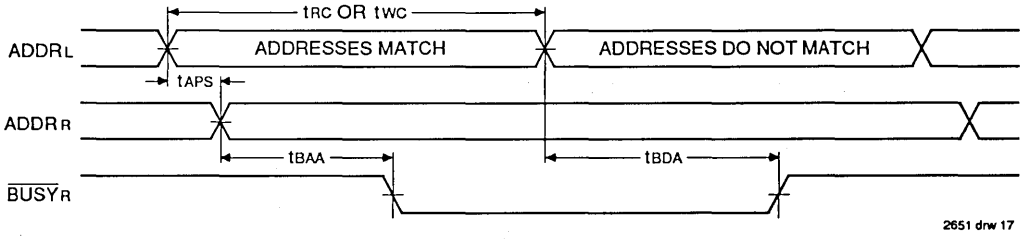
$\overline{CE}_R$ Valid First:



2651 drw 16

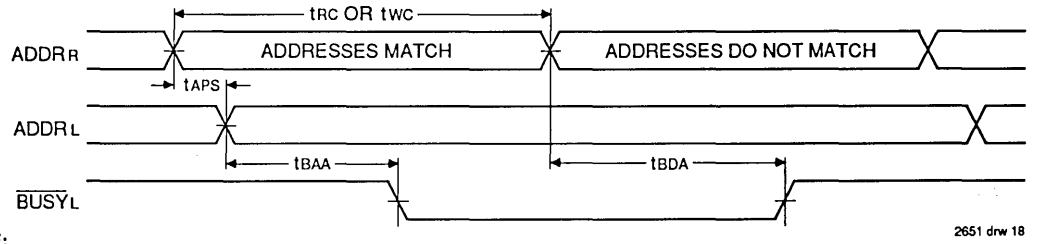
TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION(1)

Left Address Valid First:



2651 drw 17

Right Address Valid First:



2651 drw 18

NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$

FUNCTIONAL DESCRIPTION

The IDT7010/70104 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7010/70104 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table I.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION

The arbitration logic will resolve an address match or a chip enable match to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table II). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION

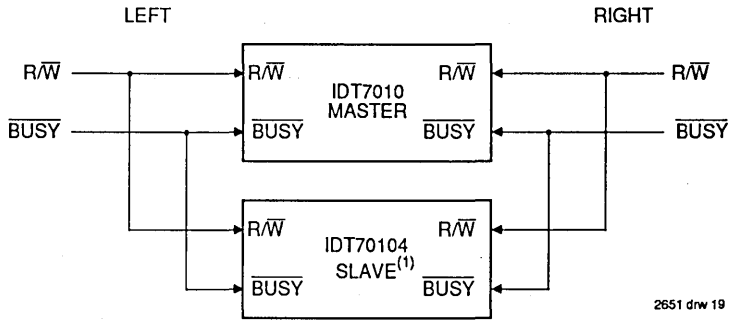
Expanding the data bus width to eighteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another activates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid this "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed, until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inherited due to $\overline{BUSY}$ from the MASTER.

18-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



NOTE:
1. No arbitration in IDT70104 (SLAVE). $\overline{BUSY}$-IN inhibits write in IDT70104 (SLAVE).

TRUTH TABLES

TABLE I. NON-CONTENTION READ/WRITE CONTROL[4]

Left or Right Port[1]				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-8}	Function
X	H	X	Z	Port Disabled and in Power Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	DATAIN	Data on Port Written Into Memory[2]
H	L	L	DATAOUT	Data in Memory Output on Port[3]
H	L	H	Z	High Impedance Outputs

2651 tbl 12

NOTES:
1. $A_{0L} - A_{9L} \neq A_{0R} - A_{9R}$
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

TABLE II. ARBITRATION[1]

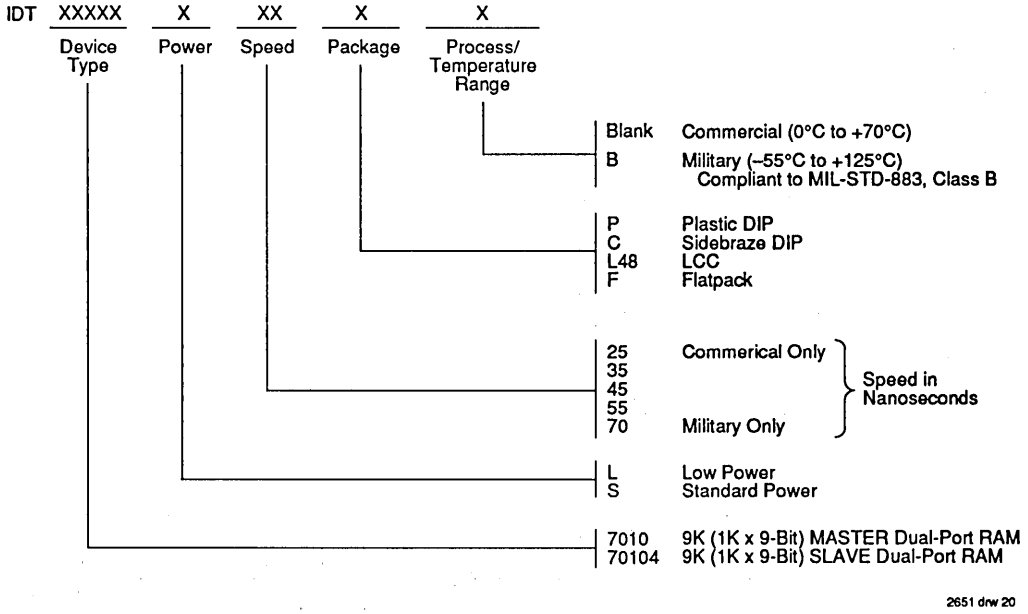
Left Port		Right Port		Flags		
$\overline{CE}_L$	$A_{0L} - A_{9L}$	$\overline{CE}_R$	$A_{0R} - A_{9R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	Function
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R} - A_{9R}$	L	$\neq A_{0L} - A_{9L}$	H	H	No Contention
Address Arbitration With $\overline{CE}$ Low Before Address Match						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ Arbitration With Address Match Before $\overline{CE}$						
LL5R	$= A_{0R} - A_{9R}$	LL5R	$= A_{0L} - A_{9L}$	H	L	L-Port Wins
RL5L	$= A_{0R} - A_{9R}$	RL5L	$= A_{0L} - A_{9L}$	L	H	R-Port Wins
LW5R	$= A_{0R} - A_{9R}$	LW5R	$= A_{0L} - A_{9L}$	H	L	Arbitration Resolved
LW5R	$= A_{0R} - A_{9R}$	LW5R	$= A_{0L} - A_{9L}$	L	H	Arbitration Resolved

2651 tbl 13

NOTES:
1. X = DON'T CARE, L = LOW, H = HIGH
   LV5R = Left Address Valid ≥ 5ns before right address.
   RV5L = Right Address Valid ≥ 5ns before left address.
   Same = Left and Right Addresses match within 5ns of each other.
   LL5R = Left $\overline{CE}$ = LOW > 5ns before Right $\overline{CE}$.
   RL5L = Right $\overline{CE}$ = LOW ≥ 5ns before Left $\overline{CE}$.
   LW5R = Left and right $\overline{CE}$ = LOW within 5ns of each other.

7

ORDERING INFORMATION



2651 drw 20

Integrated Device Technology, Inc.

HIGH-SPEED 1K x 9 DUAL-PORT STATIC RAM WITH INTERRUPT AND BUSY

PRELIMINARY
IDT70101S/L
IDT70105S/L

FEATURES:

- High-speed access
  - Military: 35/45/55/70ns (max.)
  - Commercial: 25/35/45/55ns (max.)
- Low-power operation
  - IDT70101/70105S
    Active: 400mW (typ.)
    Standby: 7mW (typ.)
  - IDT70101/70105L
    Active: 400mW (typ.)
    Standby: 2mW (typ.)
- Fully asynchronous operation from either port
- Each port has a 9-bit wide data path. The 9th bit could be used as the parity bit.
- MASTER IDT70101 easily expands data bus width to 18 bits or more using SLAVE IDT70105 chip.
- On-chip port arbitration logic (IDT70101 only)
- $\overline{BUSY}$ output flag on MASTER; $\overline{BUSY}$ input on SLAVE
- $\overline{INT}$ (INTERRUPT) flag for port-to-port communication
- Battery backup operation — 2V data retention
- TTL compatible, signal 5V (±10%) power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B

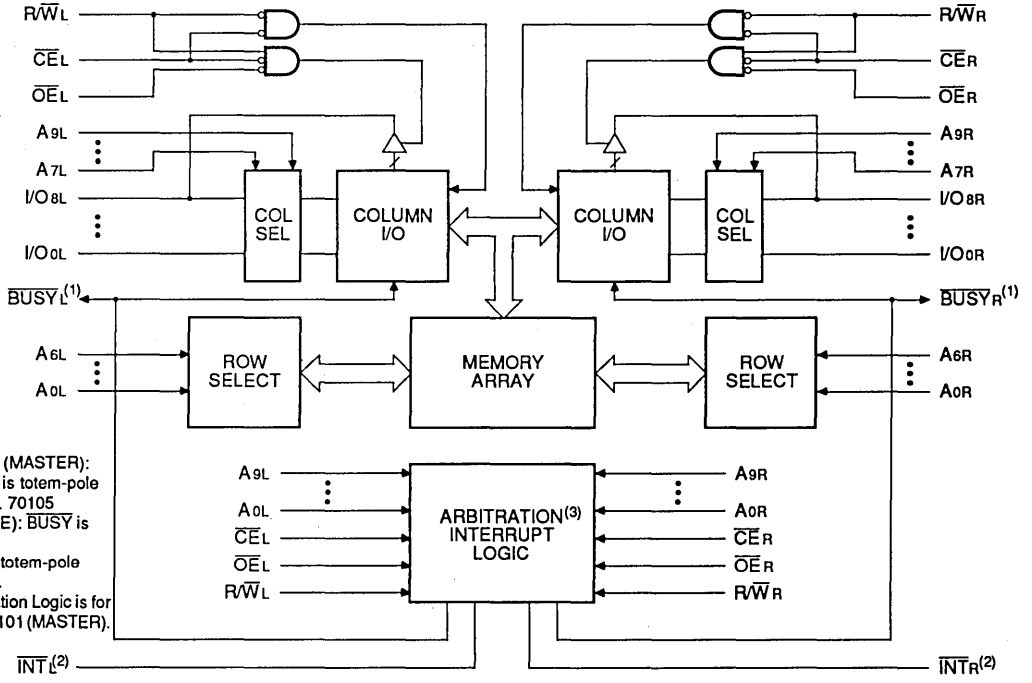
DESCRIPTION:

The IDT70101/IDT70105 are high-speed 1K x 9 dual-port static RAMs. The IDT70101 is designed to be used as a stand-alone 9-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT70105 "SLAVE" dual-port in 18-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 18-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

The devices utilize a 9-bit wide data path to allow for data/control and parity bits at the user's option. This feature is especially useful in data communications applications where

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. 70101 (MASTER): $\overline{BUSY}$ is totem-pole output. 70105 (SLAVE): $\overline{BUSY}$ is input.
2. $\overline{INT}$ is totem-pole output.
3. Arbitration Logic is for IDT70101 (MASTER).

CEMOS is a trademark of Integrated Device Technology, Inc.

2652 drw 01

MILITARY AND COMMERCIAL TEMPERATURE RANGES **SEPTEMBER 1990**

DESCRIPTION (Continued)

it is necessary to use a parity bit for transmission/reception error checking.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 400mW of power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability with each port typically consuming 200µW from a 2V battery.

The IDT70101/IDT70105 devices are packaged in 52-pin LCCs and 52-pin PLCCs. The military devices are processed 100% in compliance to the test methods of MIL-STD-883, Method 5004.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2652 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE: 2652 tbl 10

1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0.0	V
V_{IH}	Input High Votage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	–	0.8	V

NOTE: 2652 tbl 02

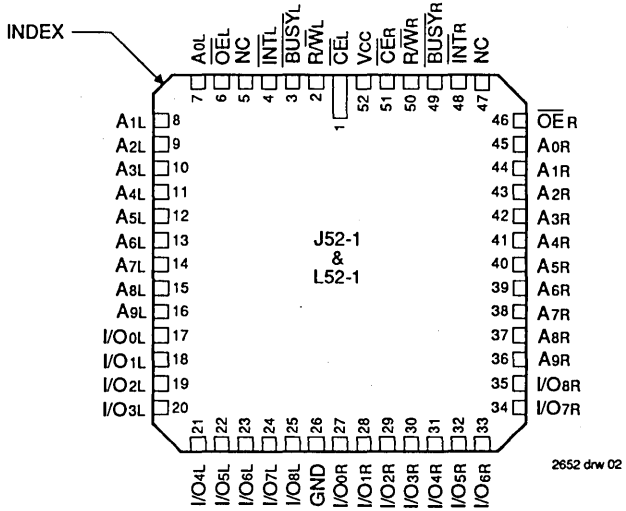
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2652 tbl 03

PIN CONFIGURATIONS



2652 drw 02

LCC/PLCC
TOP VIEW

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	70101S 70105S Min.	70101S 70105S Max.	70101L 70105L Min.	70101L 70105L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O_0 – I/O_8)	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4	—	2.4	—	V

2652 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 0.5V ± 10%)

Symbol	Parameter	Test Conditions	Version	70101 x 25[2] 70105 x 25[2] Typ.	70101 x 25[2] 70105 x 25[2] Max.	70101 x 35 70105 x 35 Typ.	70101 x 35 70105 x 35 Max.	70101 x 45 70105 x 45 Typ.	70101 x 45 70105 x 45 Max.	70101 x 55 70105 x 55 Typ.	70101 x 55 70105 x 55 Max.	70101 x 70[3] 70105 x 70[3] Typ.	70101 x 70[3] 70105 x 70[3] Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \le V_{IL}$ Outputs Open f = f_{MAX}[4]	Mil. S	—	—	80	300	75	290	70	285	65	275	mA
			Mil. L	—	—	80	220	75	210	70	205	65	200	
			Com'l. S	75	260	75	250	75	245	70	235	—	—	
			Com'l. L	75	190	75	180	75	170	70	160	—	—	
I_{SB1}	Standby Current (Both Ports—TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \ge V_{IH}$ f = f_{MAX}[4]	Mil. S	—	—	25	80	25	65	25	65	25	65	mA
			Mil. L	—	—	25	60	25	55	25	55	25	55	
			Com'l. S	25	65	25	65	25	65	25	65	—	—	
			Com'l. L	25	45	25	45	25	45	25	45	—	—	
I_{SB2}	Standby Current (One Port—TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \ge V_{IH}$ Active Port Outputs Open, f = f_{MAX}[4]	Mil. S	—	—	50	190	45	170	40	170	40	165	mA
			Mil. L	—	—	50	145	45	140	40	140	40	135	
			Com'l. S	50	175	46	160	45	150	40	140	—	—	
			Com'l. L	50	125	46	115	45	105	40	95	—	—	
I_{SB3}	Full Standby Current (Both Ports—All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \ge$ V_{CC} – 0.2V $V_{IN} \ge V_{CC}$ – 0.2V or $V_{IN} \le$ 0.2V, f = 0[5]	Mil. S	—	—	1.2	30	1.0	30	1.0	30	1.0	30	mA
			Mil. L	—	—	0.4	10	0.2	10	0.2	10	0.2	10	
			Com'l. S	1.2	15	1.2	15	1.0	15	1.0	15	—	—	
			Com'l. L	0.4	5	0.4	5	0.2	5	0.2	5	—	—	
I_{SB4}	Full Standby Current (One Port—All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ – 0.2V $V_{IN} \ge V_{CC}$ – 0.2V or $V_{IN} \le$ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	Mil. S	—	—	47	170	45	160	40	155	40	150	mA
			Mil. L	—	—	44	130	42	125	35	120	35	115	
			Com'l. S	50	155	45	142	45	132	45	127	—	—	
			Com'l. L	46	120	42	110	42	100	42	95	—	—	

2652 tbl 05

NOTES:
1. "x" in part numbers indicates power rating (S or L).
2. 0°C to +70°C temperature range only.
3. –55°C to +125°C temperature range only.
4. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.

7

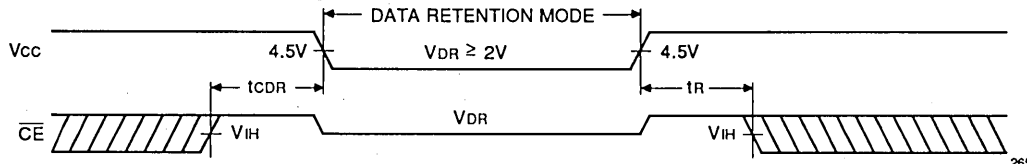
DATA RETENTION CHARACTERISTICS (L Version Only)

Symbol	Parameter	Test Conditions		70101L/70105L Min.	Typ.[1]	Max.	Unit
V_{DR}	Vcc for Data Retention			2.0	—	—	V
I_{CCDR}	Data Retention Current	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC} - 0.2V$	Mil.	—	100	4000	µA
			Com'l.	—	100	1500	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:
1. Vcc = 2V, TA = +25°C
2. tRC = Read Cycle Time
3. This parameter is guaranteed but not tested.

2652 tbl 06

DATA RETENTION WAVEFORM

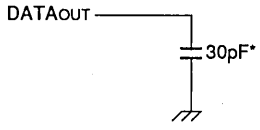


2652 drw 03

AC TEST CONDITIONS

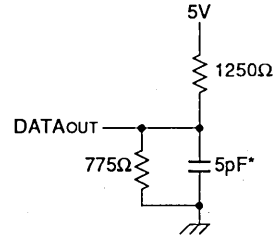
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 and 3

2652 tbl 07



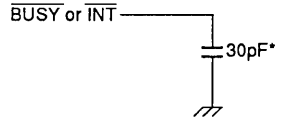
2652 drw 04

Figure 1. Output Load



2652drw 05

Figure 2. Output Load (for tHZ, tWZ, and tOW)



2652 drw 07

Figure 3. $\overline{BUSY}$ and $\overline{INT}$ Output Load

* Including scope and jig.

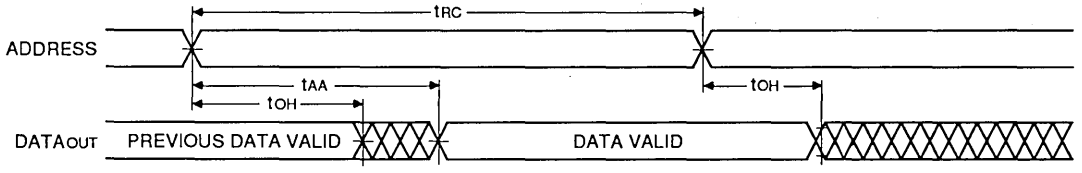
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[5]

Symbol	Parameter	70101 x 25[2] 70105 x 25[2] Min.	Max.	70101 x 35 70105 x 35 Min.	Max.	70101 x 45 70105 x 45 Min.	Max.	70101 x 55 70105 x 55 Min.	Max.	70101 x 70[3] 70105 x 70[3] Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	25	—	35	—	45	—	55	—	70	—	ns
tAA	Address Access Time	—	25	—	35	—	45	—	55	—	70	ns
tACE	Chip Enable Access Time	—	25	—	35	—	45	—	55	—	70	ns
tAOE	Output Enable Access Time	—	12	—	25	—	30	—	35	—	40	ns
tOH	Output Hold From Address Change	0	—	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time[1,4]	0	—	0	—	0	—	0	—	0	—	ns
tHZ	Output High Z Time[1,4]	—	10	—	15	—	20	—	30	—	35	ns
tPU	Chip Enable to Power Up Time[4]	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[4]	—	50	—	50	—	50	—	50	—	50	ns

2652 tbl 08

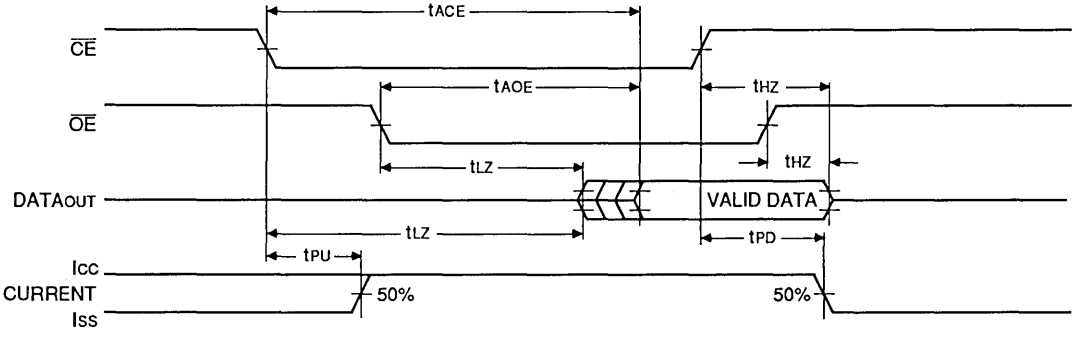
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. –55°C to +125°C range only.
4. This parameter guaranteed but not tested.
5. "x" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1, 2, 4]



2652 drw 08

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE[1, 3]



2652 drw 09

NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = VIL
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = VIL

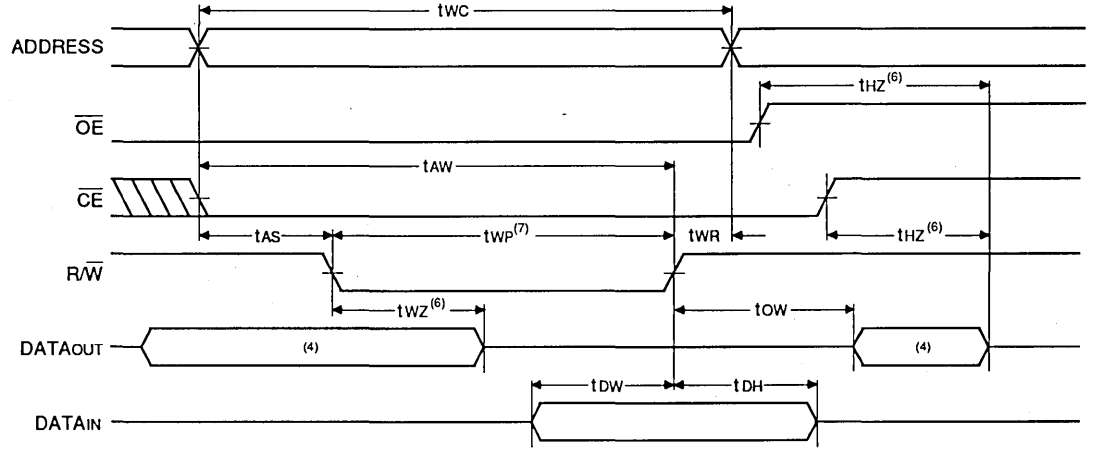
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[7]

Symbol	Parameter	70101 x 25[2] 70105 x 25[2]		70101 x 35 70105 x 35		70101 x 45 70105 x 45		70101 x 55 70105 x 55		70101 x 70[3] 70105 x 70[3]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle												
tWC	Write Cycle Time[5]	25	—	35	—	45	—	55	—	70	—	ns
tEW	Chip Enable to End of Write	20	—	30	—	35	—	40	—	50	—	ns
tAW	Address Valid to End of Write	20	—	30	—	35	—	40	—	50	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width[6]	20	—	30	—	35	—	40	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	12	—	20	—	20	—	20	—	30	—	ns
tHZ	Output High Z Time[1,4]	—	10	—	15	—	20	—	30	—	35	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z[1,4]	—	10	—	15	—	20	—	30	—	35	ns
tOW	Output Active From End of Write[1,4]	0	—	0	—	0	—	0	—	0	—	ns

2652 tbl 09

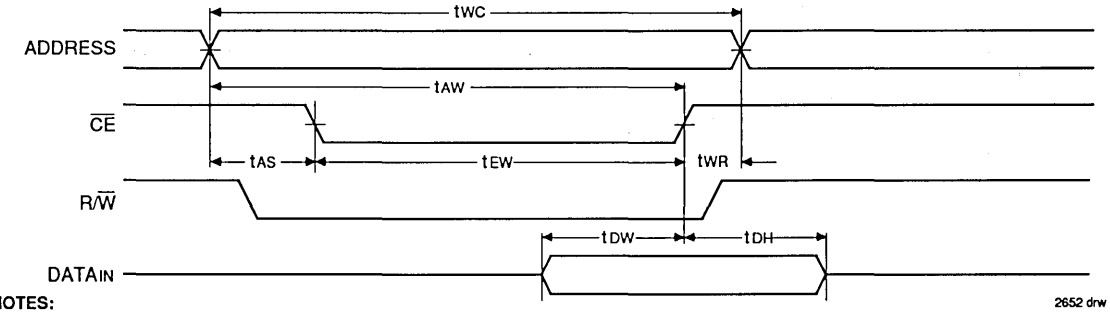
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. –55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, tWC = tBAA + tWP.
6. Specified for $\overline{OE}$ at high (refer to "Timing Waveform of Write Cycle", Note 7).
7. "x" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/$\overline{W}$ CONTROLLED TIMING)(1, 2, 3, 7)



2652 drw 10

TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING)(1, 2, 3, 5)



2652 drw 11

NOTES:

1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or tWZ + tDW to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

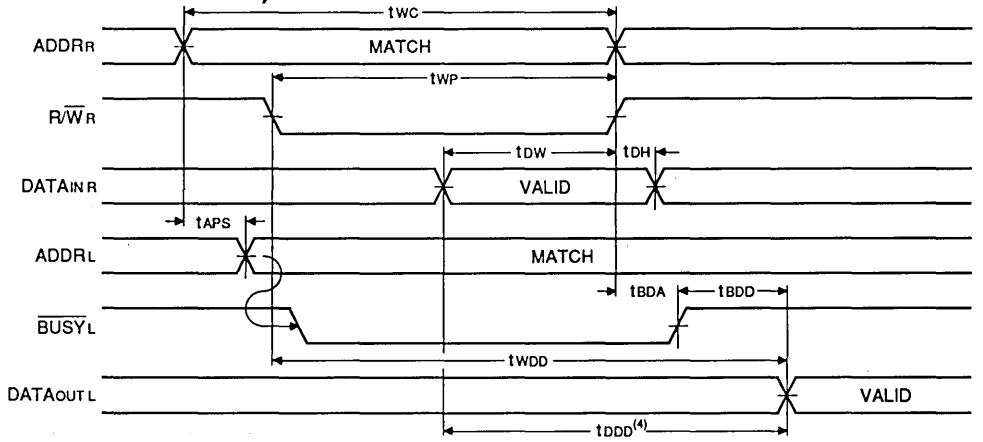
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[8]

Symbol	Parameter	70101 x 25[1] 70105 x 25[1]		70101 x 35 70105 x 35		70101 x 45 70105 x 45		70101 x 55 70105 x 55		70101 x 70[2] 70105 x 70[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Busy Timing (For Master IDT70101 Only)												
tBAA	$\overline{BUSY}$ Access Time to Address	—	25	—	35	—	35	—	45	—	45	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	20	—	30	—	35	—	40	—	40	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable	—	20	—	30	—	30	—	35	—	35	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable	—	20	—	25	—	25	—	30	—	30	ns
tWDD	Write Pulse to Data Delay[3]	—	50	—	60	—	70	—	80	—	95	ns
tDDD	Write Data Valid to Read Data Delay[3]	—	35	—	45	—	55	—	65	—	80	ns
tAPS	Arbitration Priority Set-up Time[4]	5	—	5	—	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[5]	—	Note 5	—	Note 5	—	Note 5	—	Note 5	—	Note 5	ns
Busy Input Timing (For Slave IDT70105 Only)												
tWB	Write to $\overline{BUSY}$ Input[6]	0	—	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[7]	15	—	20	—	20	—	20	—	20	—	ns
tWDD	Write Pulse to Date Delay[9]	—	50	—	60	—	70	—	80	—	95	ns
tDDD	Write Data Valid to Read Data Delay[9]	—	35	—	45	—	55	—	65	—	80	ns

2652 tbl 11

NOTES:
1. 0°C to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (For MASTER IDT70101 only)".
4. To ensure that the earlier of the two ports wins.
5. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
6. To ensure that a write cycle is inhibited during contention.
7. To ensure that a write cycle is completed after contention.
8. "x" in part numbers indicates power rating (S or L).
9. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ Port-to-port Delay (For SLAVE IDT70105 only)".

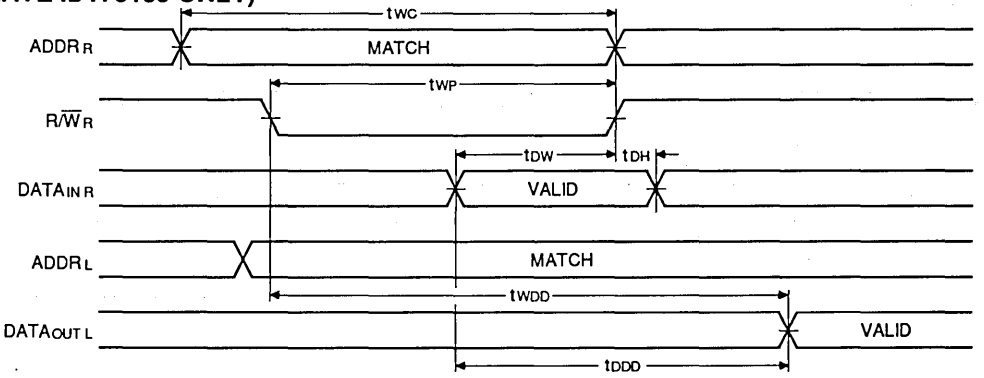
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$[1, 2, 3] (FOR MASTER IDT70101 ONLY)



2652 drw 12

NOTES:
1. To ensure that the earlier of the two ports wins.
2. Write Cycle parameters should be adhered to, in order to ensure proper writing.
3. Device is continuously enabled for both ports.
4. $\overline{OE}$ at LOW for the reading port.

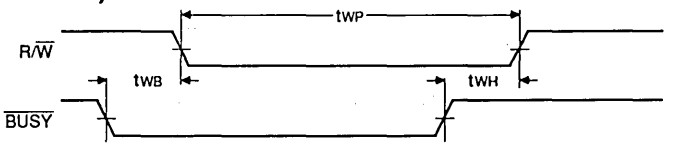
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY[1, 2, 3] (FOR SLAVE IDT70105 ONLY)



2652 drw 13

NOTES:
1. Assume $\overline{BUSY}$ input at HIGH for the writing port, and $\overline{OE}$ at LOW for the reading port.
2. Write Cycle parameters should be adhered to, in order to ensure proper writing.
3. Device is continuously enabled for both ports.

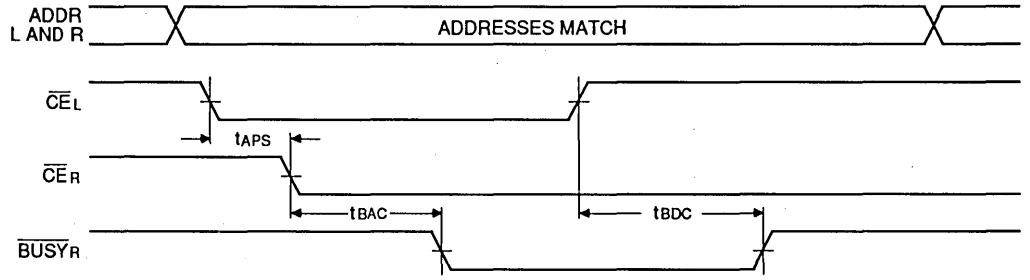
TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ INPUT (FOR SLAVE IDT70105 ONLY)



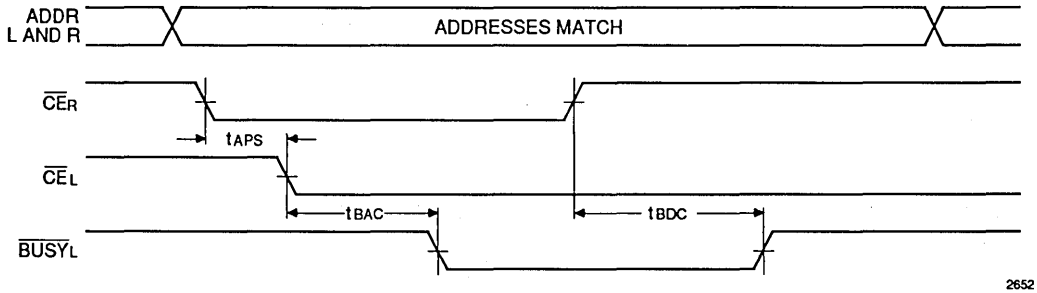
2652drw 14

TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION

$\overline{CE}_L$ VALID FIRST:



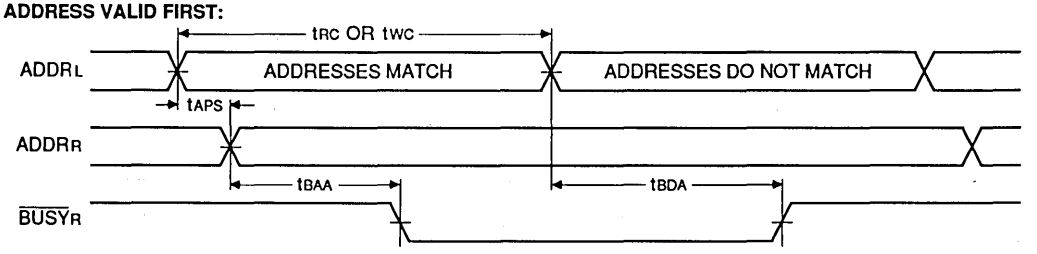
$\overline{CE}_R$ VALID FIRST:



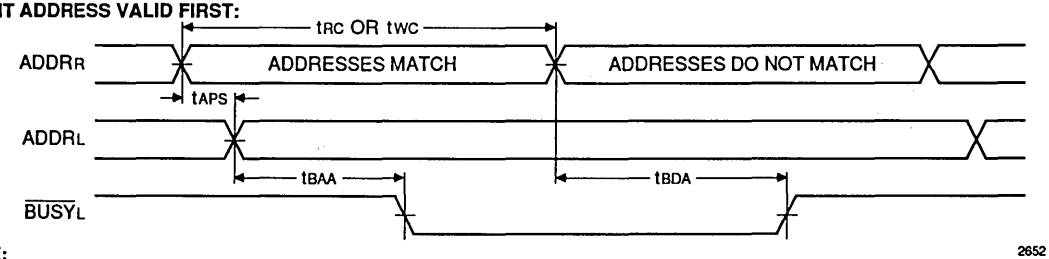
2652 drw 18

TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION(1)

LEFT ADDRESS VALID FIRST:



RIGHT ADDRESS VALID FIRST:



2652 drw 19

NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[3]

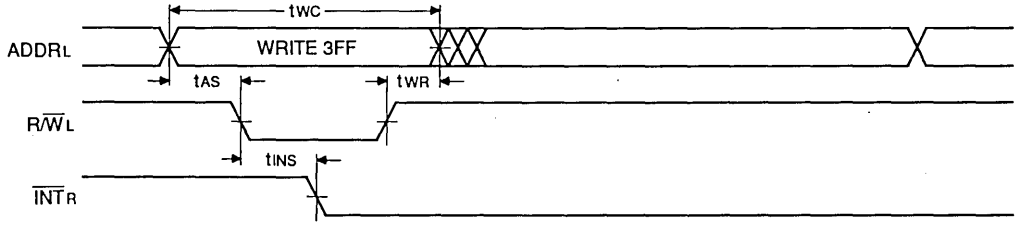
Symbol	Parameter	70101 x 25[1] 70105 x 25[1] Min.	Max.	70101 x 35 70105 x 35 Min.	Max.	70101 x 45 70105 x 45 Min.	Max.	70101 x 55 70105 x 55 Min.	Max.	70101 x 70[2] 70105 x 70[2] Min.	Max.	Unit
Interrupt Timing												
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	25	—	35	—	40	—	45	—	50	ns
t_{INR}	Interrupt Reset Time	—	25	—	35	—	40	—	45	—	50	ns

NOTES:
1. 0°C to –70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. "x" in part numbers indicates power rating (S or L).

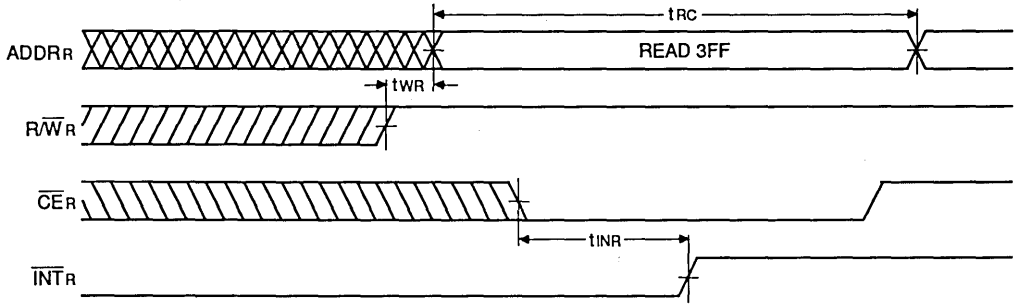
2652 tbl 13

TIMING WAVEFORM OF INTERRUPT MODE[1, 2]

LEFT SIDE SETS $\overline{INT}_R$:



RIGHT SIDE CLEARS $\overline{INT}_R$:

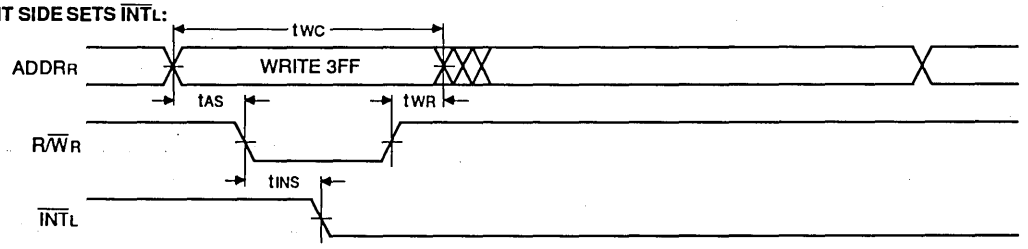


NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
2. $\overline{INT}_L$ and $\overline{INT}_R$ are reset (high) during power-up.

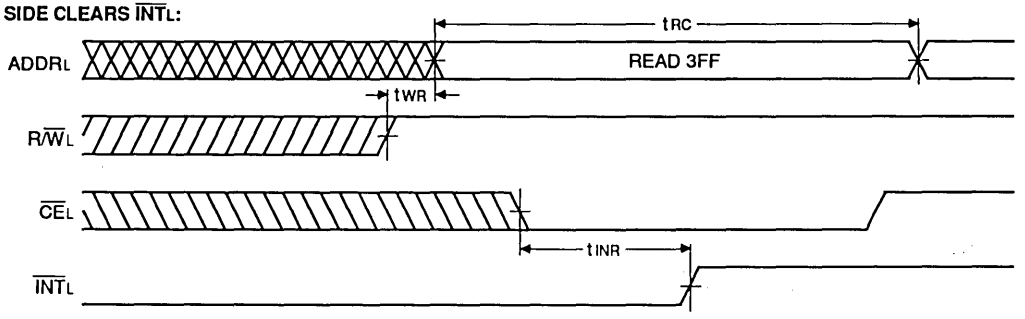
2652 drw 20

TIMING WAVEFORM OF INTERRUPT MODE[1, 2]

RIGHT SIDE SETS $\overline{INT}_L$:



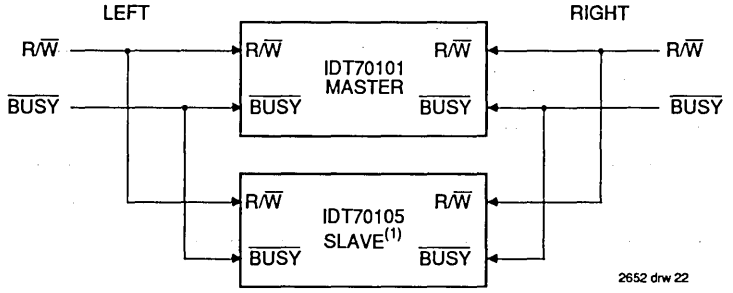
LEFT SIDE CLEARS $\overline{INT}_L$:



NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
2. $\overline{INT}_R$ and $\overline{INT}_L$ are reset (high) during power-up.

2652 drw 21

18-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



2652 drw 22

NOTE:
1. No arbitration in IDT70105 (SLAVE). $\overline{BUSY}$-IN inhibits write in IDT70105 (SLAVE).

FUNCTIONAL DESCRIPTION

The IDT70101/70105 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT70101/70105 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table 1.

The interrupt flag ($\overline{INT}$) permits communication between ports or systems. If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT_L}$) is set when the right port writes to memory location 3FE (HEX). The left port clears the interrupt by reading address location 3FE. Likewise, the right port interrupt flag ($\overline{INT_R}$) is set when the left port writes to memory location 3FF (HEX) and to clear the interrupt flag ($\overline{INT_R}$), the right port must read the memory location 3FF. The message (9-bits) at 3FE or a 3FF is user defined. If the interrupt function is not used, address location 3FE and 3FF are not used as mail boxes, but as part of the random access memory. Refer to Table II for the interrupt operation.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION

The arbitration logic will resolve an address match or a chip enable match to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE_L}$ and $\overline{CE_R}$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table III). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION

Expanding the data bus width to eighteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY_L}$ while another activates its $\overline{BUSY_R}$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid this "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed, until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than than one chip is active at the same time.

The write pulse to the SLAVE should by the maximum arbitration time of the MASTER. If, then a contention occurs, the write to the SLAVE will be inherited due to $\overline{BUSY}$ from the MASTER.

TRUTH TABLES

TABLE I. NON-CONTENTION READ/WRITE CONTROL[4]

Left or Right Port[1]				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-8}	Function
X	H	X	Z	Port Disabled and in Power Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	DATAIN	Data on Port Written Into Memory[2]
H	L	L	DATAOUT	Data in Memory Output on Port[3]
H	L	H	Z	High Impedance Outputs

NOTES:
1. $A_{0L} - A_{9L} \neq A_{0R} - A_{9R}$
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

2652 tbl 16

TABLE II. INTERRUPT FLAG[1,4]

Left Port					Right Port					
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{0L} - A_{9L}$	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{0L} - A_{9R}$	$\overline{INT}_R$	Function
L	L	X	3FF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	3FF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	3FE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	3FE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

NOTES:
1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then NC.
3. If $\overline{BUSY}_R$ = L, then NC.
4. H = HIGH,L = LOW, X = DON'T CARE, NC = NO CHANGE

2652 tbl 17

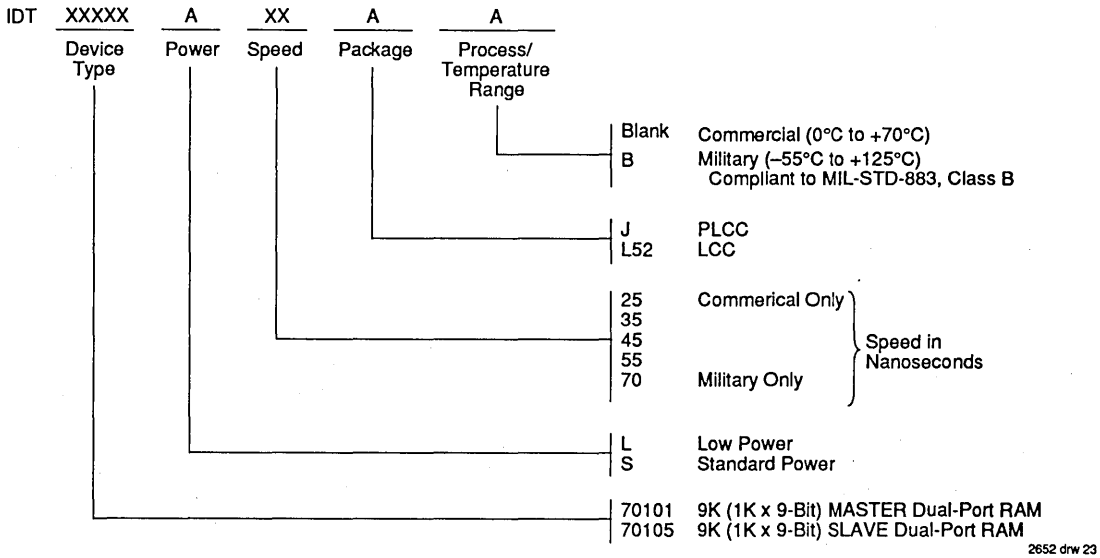
TABLE III. ARBITRATION[1]

Left Port		Right Port		Flags		
$\overline{CE}_L$	$A_{0L} - A_{9L}$	$\overline{CE}_R$	$A_{0R} - A_{9R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	Function
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R} - A_{9R}$	L	$\neq A_{0L} - A_{9L}$	H	H	No Contention
Address Arbitration With $\overline{CE}$ Low Before Address Match						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ Arbitration With Address Match Before $\overline{CE}$						
LL5R	= $A_{0R} - A_{9R}$	LL5R	= $A_{0L} - A_{9L}$	H	L	L-Port Wins
RL5L	= $A_{0R} - A_{9R}$	RL5L	= $A_{0L} - A_{9L}$	L	H	R-Port Wins
LW5R	= $A_{0R} - A_{9R}$	LW5R	= $A_{0L} - A_{9L}$	H	L	Arbitration Resolved
LW5R	= $A_{0R} - A_{9R}$	LW5R	= $A_{0L} - A_{9L}$	L	H	Arbitration Resolved

NOTES:
1. X = DON'T CARE, L = LOW, H = HIGH
   LV5R = Left Address Valid ≥ 5ns before right address.
   RV5L = Right Address Valid ≥ 5ns before left address.
   Same = Left and Right Addresses match within 5ns of each other.
   LL5R = Left $\overline{CE}$ = LOW > 5ns before Right $\overline{CE}$.
   RL5L = Right $\overline{CE}$ = LOW ≥ 5ns before Left $\overline{CE}$.
   LW5R = Left and right $\overline{CE}$ = LOW within 5ns of each other.

2652 tbl 18

ORDERING INFORMATION



2652 drw 23

7

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 16K (2K x 8-BIT)

IDT 7132SA/LA
IDT 7142SA/LA

FEATURES:

- High-speed access
  - — Military: 25/30/35/45/55/70/90/100/120ns (max.)
  - — Commercial: 20/25/30/35/45/55/70/90/100ns (max.)
- Low-power operation
  - — IDT7132/42SA
    Active: 325mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7132/42LA
    Active: 325mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- MASTER IDT7132 easily expands data bus width to 16-or-more bits using SLAVE IDT7142
- On-chip port arbitration logic (IDT7132 only)
- $\overline{BUSY}$ output flag on IDT7132; $\overline{BUSY}$ input on IDT7142
- Battery backup operation -2V data retention
- TTL-compatible, single 5v ±10% power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD, Class B
- Standard Military Drawing # 5962-87002

DESCRIPTION:

The IDT7132/IDT7142 are high-speed 2K x 8 dual-port static RAMs. The IDT7132 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7142 "SLAVE" dual-port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

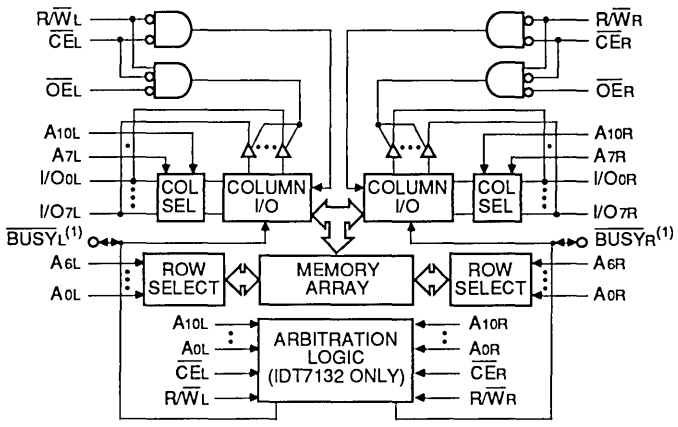
Both devices provide two independent ports with seperate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 325mW of power at maximum access times as fast as 20ns. Low-power (LA) versions offer battery backup data retention capability, with each dual-port typically consuming 200µW from a 2V battery.

The IDT7132/7142 devices are packaged in a 48-pin sidebraze or plastic DIPs, 48- or 52-pin LCCs, 52-pin PLCCs, and a 48-lead flatpacks.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



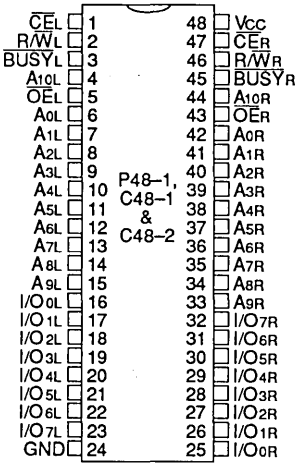
2692 drw 01

NOTE:

1. IDT7132 (MASTER): $\overline{BUSY}$ is open output and requires pullup resistor.
   IDT7142 (SLAVE): $\overline{BUSY}$ is input.

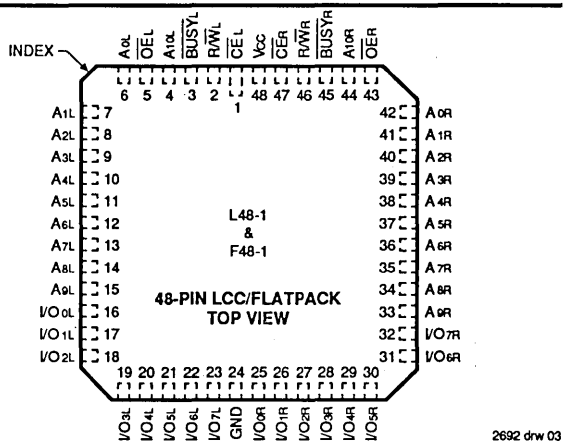
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGUARATIONS

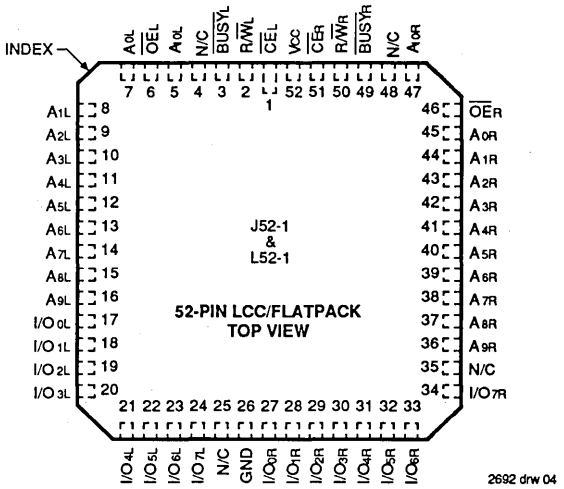


2692 drw 02

DIP
TOP VIEW



2692 drw 03



2692 drw 04

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

2692 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

2692 tbl 02

NOTE:
1. VIL (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0v ± 10%
Commercial	0°C to +70°C	0V	5.0v ± 10%

2692 tbl 03

7

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ±10%)

Symbol	Parameter	Test Conditions	IDT7132SA IDT7142SA Min.	IDT7132SA IDT7142SA Max.	IDT7132LA IDT7142LA Max.	IDT7132LA IDT7142LA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O_0-I/O_7)	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$)	I_{OL} = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2692 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLE VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version		7132 x 20[2,6] 7142 x 20[2,6] Typ.	7132 x 20[2,6] 7142 x 20[2,6] Max.	7132 x 25[6] 7142 x 25[6] Typ.	7132 x 25[6] 7142 x 25[6] Max.	7132 x 30[6] 7142 x 30[6] Typ.	7132 x 30[6] 7142 x 30[6] Max.	7132 x 35[7] 7142 x 35[7] Typ.	7132 x 35[7] 7142 x 35[7] Max.	7132 x 45 7142 x 45 Typ.	7132 x 45 7142 x 45 Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	Mil.	SA	—	—	75	300	75	290	75	280	75	230	mA
				LA	—	—	75	220	75	210	75	200	75	185	
			Com'l.	SA	75	260	75	250	75	240	75	195	75	190	
				LA	75	190	75	180	75	170	75	155	75	145	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE_L}$ and $\overline{CE_R}$ ≥ V_{IH} f = f_{MAX}[4]	Mil.	SA	—	—	25	75	25	75	25	75	25	65	mA
				LA	—	—	25	55	25	55	25	55	25	55	
			Com'l.	SA	25	65	25	65	25	65	25	65	25	65	
				LA	25	45	25	45	25	45	25	45	25	45	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE_L}$ or $\overline{CE_R}$ ≥ V_{IH} Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	—	—	50	180	46	175	40	170	40	135	mA
				LA	—	—	50	140	46	135	40	130	40	110	
			Com'l.	SA	50	180	50	170	46	155	40	130	40	120	
				LA	50	130	50	120	46	110	40	95	40	85	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs	Both Ports $\overline{CE_L}$ and $\overline{CE_R}$ ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V, f = 0[5]	Mil.	SA	—	—	1.2	40	1.2	40	1.2	35	1.0	30	mA
				LA	—	—	0.4	10	0.4	10	0.4	10	0.2	10	
			Com'l.	SA	1.2	15	1.2	15	1.2	15	1.0	15	1.0	15	
				LA	0.4	4	0.4	4	0.4	4	0.2	4	0.2	4	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs f = 0[5])	One Port $\overline{CE_L}$ or $\overline{CE_R}$ ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	—	—	50	170	45	160	45	150	40	125	mA
				LA	—	—	46	135	42	125	42	115	35	95	
			Com'l.	SA	50	160	50	150	45	137	40	115	40	105	
				LA	46	125	46	115	42	105	35	90	35	80	

2692 tbl 05

NOTES:
1. x in part numbers indicates power rating (SA or LA).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
6. Not available in DIP packages — see 7032/7042 data sheet.
7. DIP packages for 0°C to +70°C temperature range only — see 7032/7042 data sheet.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (Continued) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version	7132 x 55 7142 x 55 Typ.	Max.	7132 x 70 7142 x 70 Typ.	Max.	7132 x90 7142 x 90 Typ.	Max.	7132 x 100 7142 x 100 Typ.	Max.	7132 x 120[3] 7142 x 120 Typ.	Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}	Mil. SA	65	230	65	225	65	200	65	190	65	190	mA
			Mil. LA	65	185	65	180	65	160	65	155	65	155	
			Com'l. SA	65	180	65	180	65	180	65	180	—	—	
			Com'l. LA	65	140	65	135	65	130	65	130	—	—	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE_L}$ and $\overline{CE_R}$ ≥ V_{IH} f = f_{MAX}[4]	Mil. SA	25	65	25	65	25	65	25	65	25	65	mA
			Mil. LA	25	55	25	55	25	45	25	45	25	45	
			Com'l. SA	25	65	25	60	25	55	25	55	—	—	
			Com'l. LA	25	45	25	40	25	35	25	35	—	—	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE_L}$ or $\overline{CE_R}$ ≥ V_{IH} Active Port Outputs Open, f = f_{MAX}[4]	Mil. SA	40	135	40	135	40	125	40	125	40	125	mA
			Mil. LA	40	110	40	110	40	100	40	100	40	100	
			Com'l. SA	40	115	40	110	40	110	40	110	—	—	
			Com'l. LA	40	85	40	85	40	75	40	75	—	—	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE_L}$ and $\overline{CE_R}$ ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V, f = 0[5]	Mil. SA	1.0	30	1.0	30	1.0	30	1.0	30	1.0	30	mA
			Mil. LA	0.2	10	0.2	10	0.2	10	0.2	10	0.2	10	
			Com'l. SA	1.0	15	1.0	15	1.0	15	1.0	15	—	—	
			Com'l. LA	0.2	4	0.2	4	0.2	4	0.2	4	—	—	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs, f = 0[5])	One Port $\overline{CE_L}$ or $\overline{CE_R}$ ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	Mil. SA	40	120	40	115	40	110	40	110	40	110	mA
			Mil. LA	35	90	35	85	35	80	35	80	35	80	
			Com'l. SA	40	100	40	100	40	95	40	95	—	—	
			Com'l. LA	35	75	35	75	35	70	35	70	—	—	

2692 tbl 06

NOTES:
1. x in part numbers indicates power rating (SA or LA).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. At f = f_{Max}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
6. Not available in DIP packages — see 7032/7042 data sheet.
7. DIP packages for 0°C to +70°C temperature range only — see 7032/7042 data sheet.

DATA RETENTION CHARACTERISTICS (LA Version Only)

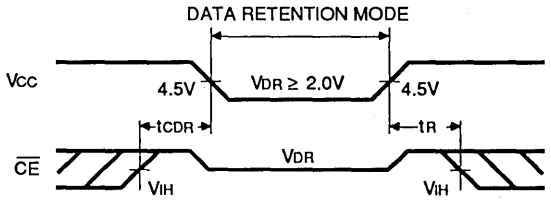
Symbol	Parameter	Test Conditions		IDT7132LA/IDT7142LA Min.	Typ.	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2.0V, $\overline{CE}$ ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V		2.0	—	0	V
I_{CCDR}	Data Retention Current		Mil.	—	100	4000	µA
			Com'l.	—	100	1500	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

2692 tbl 07

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

7

DATA RETENTION WAVEFORM



2692 drw 05

AC TEST CONDITIONS

Input Pulse Levels	GND TO 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2, 3 & 4

2692 tbl 08

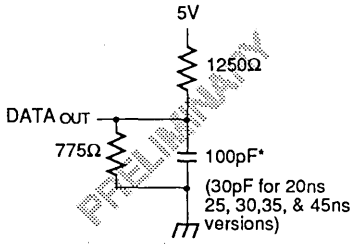


Figure 1. Output Load

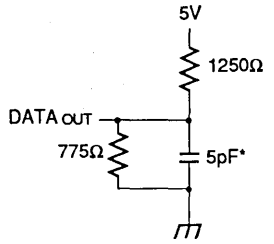


Figure 2. Output Load (for tHV, tLZ, tWZ, and tOW)

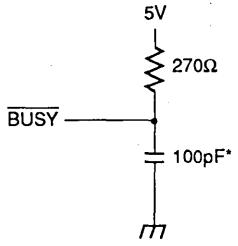


Figure 3. Busy Output Load (IDT7132 only)

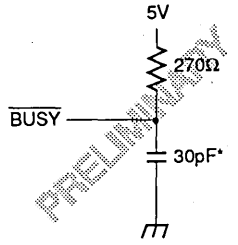


Figure 4. $\overline{BUSY}$ Output Load (for 20ns, 25ns and 30ns versions)

* Including scope and jig

2692 drw 06

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (5)

Symbol	Parameter	7132 x 20(2,6) 7142 x 20(2,6) Min.	Max.	7132 x 25(6) 7142 x 25(6) Min.	Max.	7132 x 30(6) 7142 x 30(6) Min.	Max.	7132 x 35(7) 7142 x 35(7) Min.	Max.	7132 x 45 7142 x 45 Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
tAA	Address Access Time	—	20	—	25	—	30	—	35	—	45	ns
tACE	Chip Enable Access Time	—	20	—	25	—	30	—	35	—	45	ns
tAOE	Output Enable Access Time	—	10	—	12	—	15	—	25	—	30	ns
tOH	Output Hold From Address Change	0	—	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time(1, 4)	0	—	0	—	0	—	5	—	5	—	ns
tHZ	Output High Z Time(1, 4)	—	8	—	10	—	12	—	15	—	20	ns
tPU	Chip Enable to Power Up Time(4)	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time(4)	—	50	—	50	—	50	—	50	—	50	ns

2692 tbl 09

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (5) (Continued)

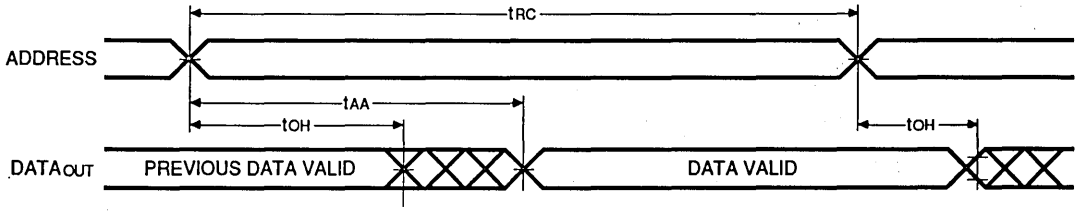
Symbol	Parameter	7132 x 55 7142 x 55 Min.	Max.	7132 x 70 7142 x 70 Min.	Max.	7132 x 90 7142 x 90 Min.	Max.	7132 x 100 7142 x 100 Min.	Max.	7132 x 120(3) 7142 x 120(3) Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	55	—	70	—	90	—	100	—	120	—	ns
tAA	Address Access Time	—	55	—	70	—	90	—	100	—	120	ns
tACE	Chip Enable Access Time	—	55	—	70	—	90	—	100	—	120	ns
tAOE	Output Enable Access Time	—	35	—	40	—	40	—	40	—	60	ns
tOH	Output Hold From Address Change	0	—	0	—	10	—	10	—	10	—	ns
tLZ	Output Low Z Time(1, 4)	5	—	5	—	5	—	5	—	5	—	ns
tHZ	Output High Z Time(1, 4)	—	30	—	35	—	40	—	40	—	40	ns
tPU	Chip Enable to Power Up Time(4)	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time(4)	—	50	—	50	—	50	—	50	—	50	ns

2692 tbl 10

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. "x" in part numbers indicates power rating (SA or LA).
6. Not available in DIP packages — see 7032/7042 data sheet.
7. DIP packages for 0°C to +70°C temperature range only — see 7032/7042 data sheet.

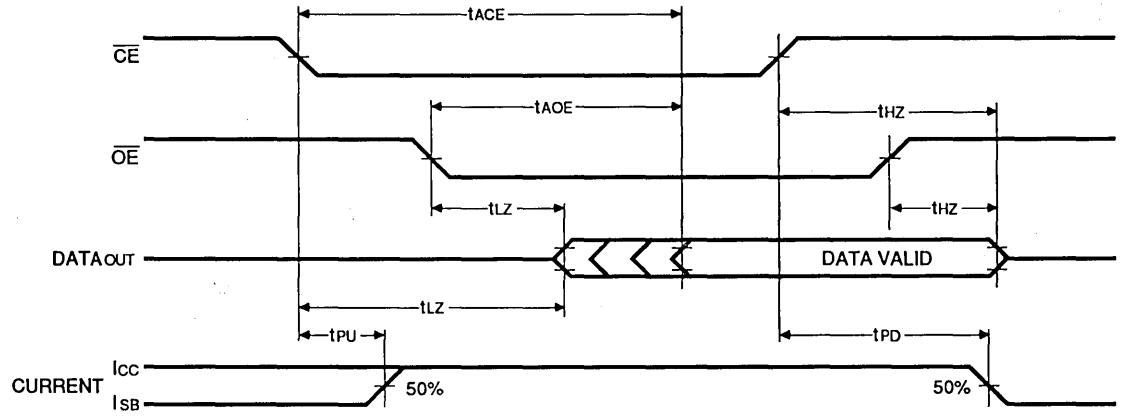
7

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE (1,2,4)



2692 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1,3)



2692 drw 08

NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = VIL.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = VIL.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLATAGE RANGE (7)

Symbol	Parameter	7132 x 20(2, 8) 7142 x 20(2, 8) Min.	Max.	7132 x 25(8) 7142 x 25(8) Min.	Max.	7132 x 30(8) 7142 x 30(8) Min.	Max.	7132 x 35(9) 7142 x 35(9) Min.	Max.	7132 x 45 7142 x 45 Min.	Max.	Unit
Write Cycle												
tWC	Write Cycle Time (5)	20	—	25	—	30	—	35	—	45	—	ns
tEW	Chip Enable to End of Write	15	—	20	—	25	—	30	—	35	—	ns
tAW	Address Valid to End of Write	15	—	20	—	25	—	30	—	35	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width (6)	15	—	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	10	—	12	—	15	—	20	—	20	—	ns
tHZ	Output High Z Time (1,4)	—	8	—	10	—	12	—	15	—	20	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z (1,4)	—	8	—	10	—	12	—	15	—	20	ns
tOW	Output Active From End of Write (1,4)	0	—	0	—	0	—	0	—	0	—	ns

2692 tbl 11

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2, 3 and 4).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, tWC = tBAA + tWP.
6. Specified for $\overline{OE}$ at high (Refer to "Timing Waveform of Write Cycle", Note 7)
7. "x" in part numbers indicates power rating (SA or LA).
8. Not available in DIP packages — see 7032/7042 data sheet.
9. DIP packages for 0°C to +70°C temperature range only — see 7032/7042 data sheet.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [7] (Continued)

Symbol	Parameter	7132 x 55 7142 x 55 Min.	Max.	7132 x 70 7142 x 70 Min.	Max.	7132 x 90 7142 x 90 Min.	Max.	7132 x 100 7142 x 100 Min.	Max.	7132 x 120[3] 7142 x 120[3] Min.	Max.	Unit
Write Cycle												
tWC	Write Cycle Time [5]	55	—	70	—	90	—	100	—	120	—	ns
tEW	Chip Enable to End of Write	40	—	50	—	85	—	90	—	100	—	ns
tAW	Address Valid to End of Write	40	—	50	—	85	—	90	—	100	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width [6]	40	—	50	—	55	—	55	—	65	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	20	—	30	—	40	—	40	—	40	—	ns
tHZ	Output High Z Time [1,4]	—	30	—	35	—	40	—	40	—	40	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z[1,4]	—	30	—	35	—	40	—	40	—	50	ns
tOW	Output Active From End of Write[1,4]	0	—	0	—	0	—	0	—	0	—	ns

2692 tbl 12

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, $t_{WC} = t_{BAA} + t_{WP}$.
6. Specified for $\overline{OE}$ at high (Refer to "Timing Waveform of Write Cycle", Note 7)
7. "x" in part numbers indicates power rating (SA or LA).

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

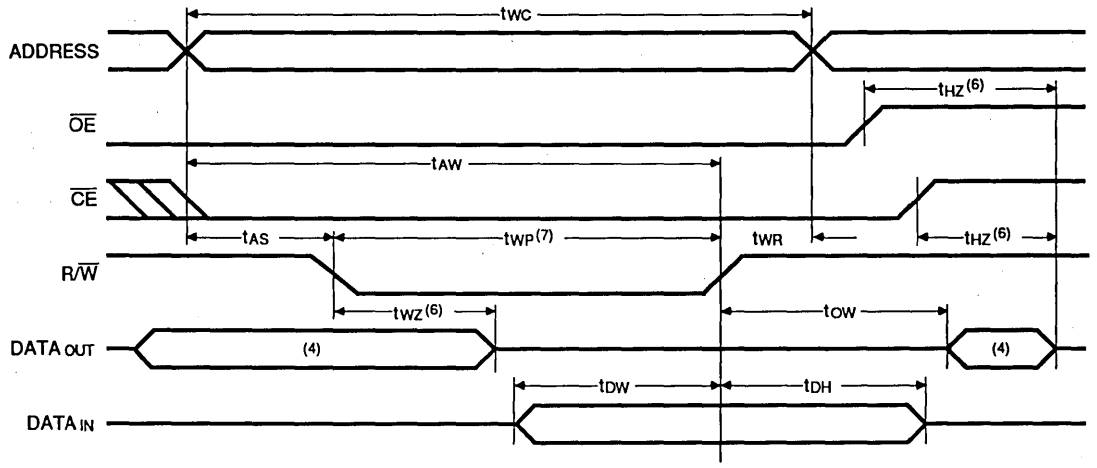
Symbol	Parameter [1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{IN} = 0V	11	pF

2692 tbl 13

NOTE:
1. This parameter is sampled and not 100% tested.

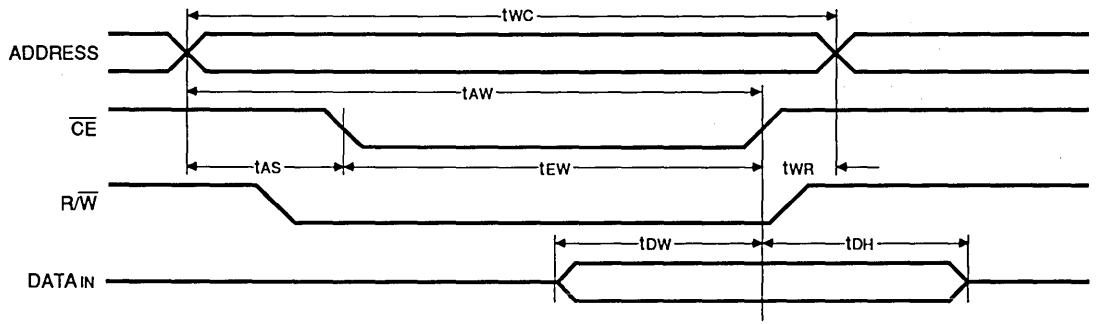
7

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/$\overline{W}$ CONTROLLED TIMING)(1,2,3,7)



2692 drw 09

TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING)(1,2,3,5)



2692 drw 10

NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[8]

Symbol	Parameter	7132 x 20 [1,10] 7142 x 20 [1,10] Min.	Max.	7132 x 25 [10] 7132 x 25 [10] Min.	Max.	7132 x 30 [10] 7142 x 30 [10] Min.	Max.	7132 x 35 [11] 7132 x 35 [11] Min.	Max.	7132 x 45 7142 x 45 Min.	Max.	Unit
Busy Timing (For Master IDT7132 Only)												
tBAA	$\overline{BUSY}$ Access Time to Address	—	20	—	25	—	30	—	35	—	35	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	18	—	20	—	25	—	30	—	35	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable	—	20	—	20	—	25	—	30	—	30	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable	—	18	—	20	—	25	—	25	—	25	ns
tWDD	Write Pulse to Data Delay [3]	—	45	—	50	—	55	—	60	—	70	ns
tDDD	Write Data Valid to Read Data Delay [3]	—	30	—	33	—	33	—	35	—	45	ns
tAPS	Arbitration Priority Set-up Time [4]	5	—	5	—	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data [5]	—	Note 5	—	Note 5	—	Note 5	—	Note 5	—	Note 5	ns
Busy Input Timing (For Slave IDT7142 Only)												
tWB	Write to $\overline{BUSY}$ Input [6]	0	—	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$ [7]	12	—	15	—	20	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay [9]	—	45	—	50	—	55	—	60	—	70	ns
tDDD	Write Data Valid to Read Data Delay [9]	—	30	—	35	—	40	—	35	—	45	ns

2692 tbl 14

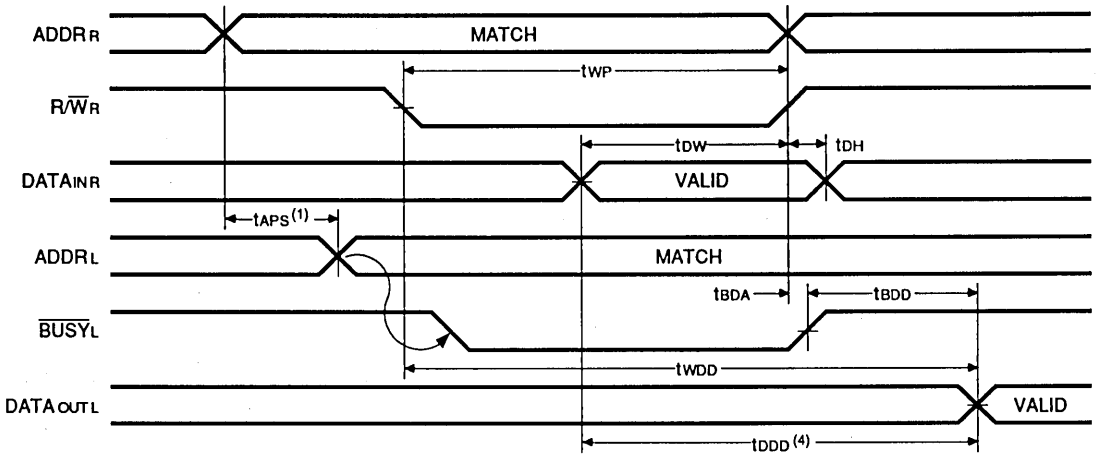
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[8]

Symbol	Parameter	7132 x 55 7142 x 55 Min.	Max.	7132 x 70 7142 x 70 Min.	Max.	7132 x 90 7142 x 90 Min.	Max.	7132 x 100 7142 x 100 Min.	Max.	7132 x 120 [2] 7142 x 120 [2] Min.	Max.	Unit
Busy Timing (For Master IDT7132 Only)												
tBAA	$\overline{BUSY}$ Access Time to Address	—	45	—	45	—	45	—	50	—	60	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	40	—	40	—	45	—	50	—	60	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable	—	35	—	35	—	45	—	50	—	60	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable	—	30	—	30	—	45	—	50	—	60	ns
tWDD	Write Pulse to Data Delay [3]	—	80	—	90	—	100	—	120	—	140	ns
tDDD	Write Data Valid to Read Data Delay [3]	—	55	—	70	—	90	—	100	—	120	ns
tAPS	Arbitration Priority Set-up Time [4]	5	—	5	—	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data [5]	—	Note 5	—	Note 5	—	Note 5	—	Note 5	—	Note 5	ns
Busy Input Timing (For Slave IDT7142 Only)												
tWB	Write to $\overline{BUSY}$ Input [6]	—	—	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$ [7]	20	—	20	—	20	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay [9]	—	80	—	90	—	100	—	120	—	140	ns
tDDD	Write Data Valid to Read Data Delay [9]	—	55	—	70	—	90	—	100	—	120	ns

2692 tbl 15

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (For Master IDT7132 only)".
4. To ensure that the earlier of the two ports wins.
5. tBDD is a calculated parameter and is the greater of 0, tWDD-tWP (actual) or tDDD - tDW (actual)
6. To ensure that the write cycle is inhibited during contention.
7. To ensure that a write cycle is completed after contention.
8. "x" in part numbers indicates power rating (SA or LA).
9. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With Port-to-Port Delay (For Slave IDT7142 Only)".
10. Not available in DIP packages — see 7032/7042 data sheet.
11. DIP packages for 0°C to +70°C temperature range only — see 7032/7042 data sheet.

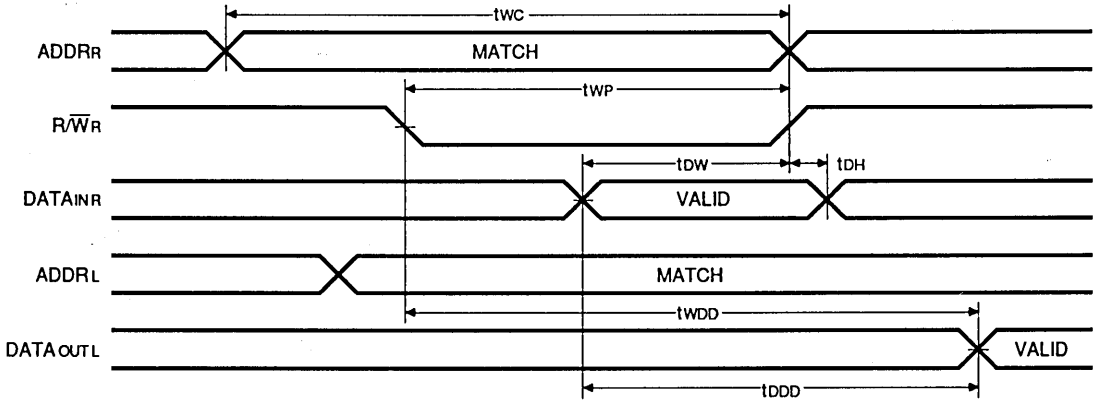
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$ (1,2,3) (FOR MASTER IDT7132 ONLY)



2692 drw 11

NOTES:
1. To ensure that the earlier of the two ports wins.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continously enabled for both ports.
4. $\overline{OE}$ at LO for the reading port.

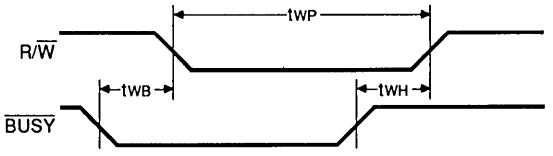
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY (1,2,3) (FOR SLAVE IDT7142 ONLY)



2692 drw 12

NOTES:
1. Assume $\overline{BUSY}$ input at HI for the writing port, and $\overline{OE}$ at LO for the reading port.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuosly enabled for both ports.

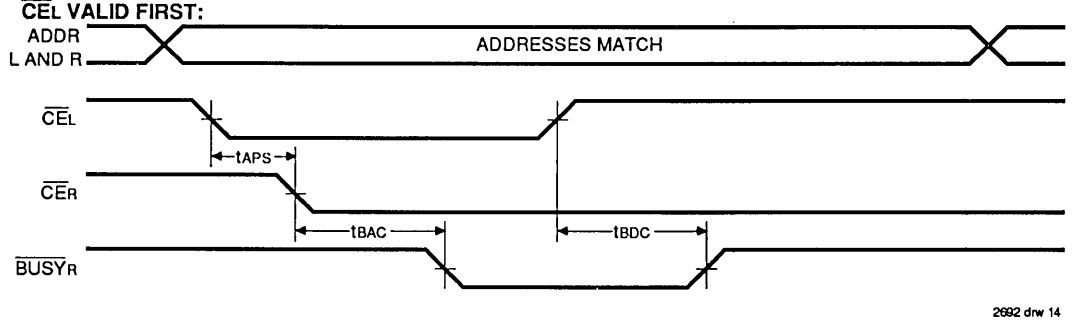
TIMING WAVEFORM OF WRITE WITH BUSY INPUT (FOR SLAVE IDT7142 ONLY)



2692 drw 13

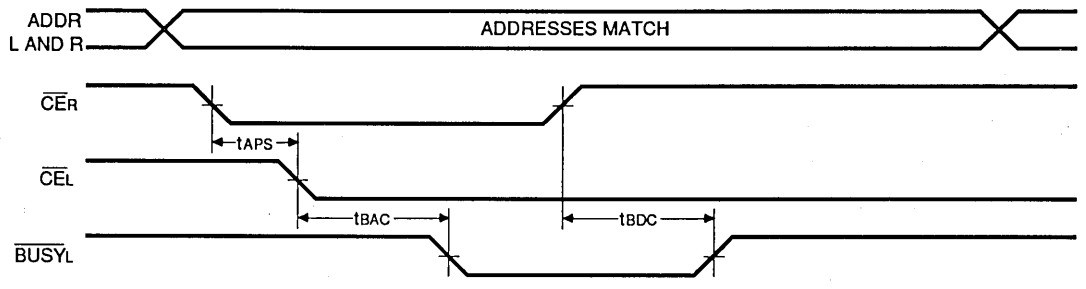
TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION

$\overline{CE}_L$ VALID FIRST:



2692 drw 14

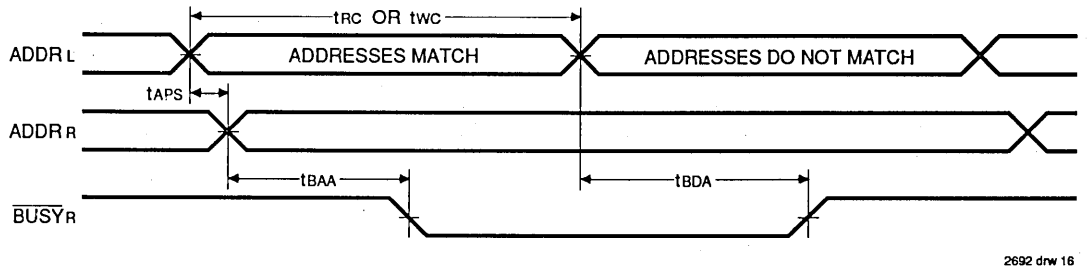
$\overline{CE}_R$ VALID FIRST:



2692 drw 15

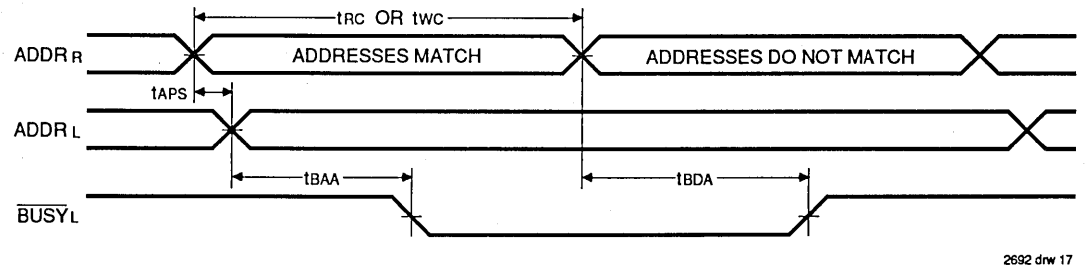
TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION (1)

LEFT ADDRESS VALID FIRST:



2692 drw 16

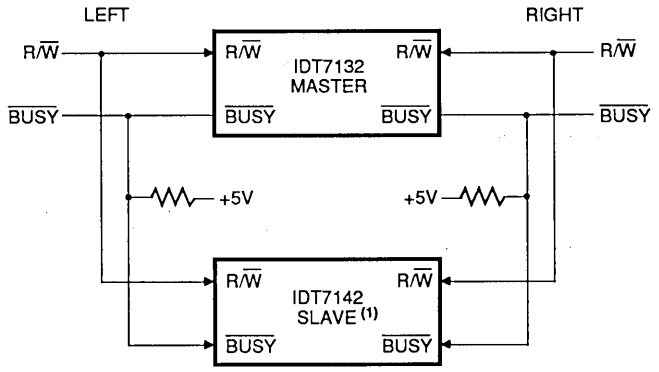
RIGHT ADDRESS VALID FIRST:



2692 drw 17

NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$

16-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



NOTE:
1. No arbitration in IDT7142 (SLAVE). BUSY-IN inhibits write in IDT7142 (SLAVE).

FUNCTIONAL DESCRIPTION:

The IDT7132/42 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any locations in memory. These devices have an automatic power-down feature controlled by CE. The CE controls on-chip power-down circuitry that permits the respective port to go into a standby mode when not selected (CE high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control (OE). In the read mode, the port's OE turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table 1.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION:

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active BUSY flag will be set for the delayed port.

The BUSY flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's BUSY flag. BUSY is set at speeds that permit the processor to hold the operation and its respective address data. It is important to note that the operation is invalid for the port that has BUSY set LOW. The delayed port will have access when BUSY goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before CE, on-chip control logic arbitrates between CEL and CER for access; or (2) if the CEs are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table II). In either mode of arbitration, the delayed port's BUSY flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION:

Expanding the data bus width to sixteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its BUSYL while another acitivates its BUSYR signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one arbitrator, in the MASTER, is used. The SLAVE has BUSY inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed, until after the BUSY input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past BUSY to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than on chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to BUSY from the MASTER.

TRUTH TABLES

TABLE I – NON-CONTENTION READ/WRITE CONTROL (4)

Left Or Right Port (1)				Function
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	
X	H	X	Z	Port Disabled and in Power Down Mode I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R$ = $\overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	DATAIN	Data on Port Written into Memory (2)
H	L	L	DATAOUT	Data in Memory Output on Port (3)
H	L	H	Z	High Impedance

2692 tbl 16

NOTES:
1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$
2. If $\overline{BUSY}$ = L, data is not written
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

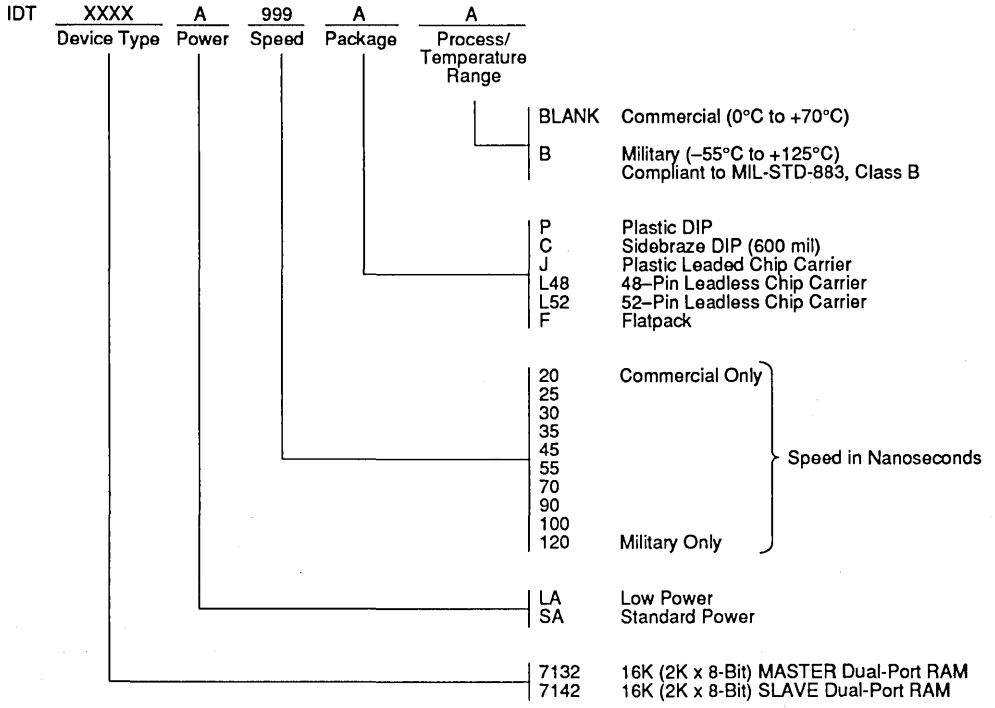
TABLE II – ARBITRATION (1,2)

Left Port		Right Port		Flags		Function
$\overline{CE}_L$	$A_{0L} - A_{10L}$	$\overline{CE}_R$	$A_{0R} - A_{10R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R} - A_{10R}$	L	$\neq A_{0L} - A_{10L}$	H	H	No Contention
Address Arbitration With $\overline{CE}$ Low Before Address Match						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ Arbitration With Address Match Before $\overline{CE}$						
LL5R	$= A_{0R} - A_{10R}$	LL5R	$= A_{0L} - A_{10L}$	H	L	L-Port Wins
RL5L	$= A_{0R} - A_{10R}$	RL5L	$= A_{0L} - A_{10L}$	L	H	R-Port Wins
LW5R	$= A_{0R} - A_{10R}$	LW5R	$= A_{0L} - A_{10L}$	H	L	Arbitration Resolved
LW5R	$= A_{0R} - A_{10R}$	LW5R	$= A_{0L} - A_{10L}$	L	H	Arbitration Resolved

2692 tbl 17

NOTES:
1. X = DON'T CARE, L = LOW, H = HIGH
2. LV5R = Left Address Valid ≥ 5ns before right address.
   RV5L = Right Address Valid ≥ 5ns before left address.
   Same = Left and Right Addresses match within 5ns of each other.
   LL5R = Left $\overline{CE}$ = LOW ≥ 5ns before Right $\overline{CE}$.
   RL5L = Right $\overline{CE}$ = LOW ≥ 5ns before Left $\overline{CE}$.
   LW5R = Left and Right $\overline{CE}$ = LOW within 5ns of each other.

ORDERING INFORMATION



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Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 16K (2K x 8-BIT)

PRELIMINARY
IDT7032SA/LA
IDT7042SA/LA

FEATURES

- High-speed access
  - —Military: 25/35/45ns (max.)
  - —Commercial: 20/25/35ns (max.)
- Low-power operation
  - —IDT7032/42SA
    - Active: 375mW (typ.)
    - Standby: 6mW (typ.)
  - —IDT7032/42LA
    - Active: 375mW (typ.)
    - Standby: 2mW (typ.)
- Fully asynchronous operation from either port
- MASTER IDT7032 easily expands data bus width to 16-or-more-bits using SLAVE IDT7042
- On-chip port arbitration logic (IDT7032 only)
- $\overline{BUSY}$ output flag on IDT7032; $\overline{BUSY}$ input on IDT7042
- Battery backup operation -2V data retention
- TTL-compatible, single 5V ±10% power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7032/IDT7042 are high speed 2Kx8 dual-port static RAMs. The IDT7032 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7042 "SLAVE" dual-port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

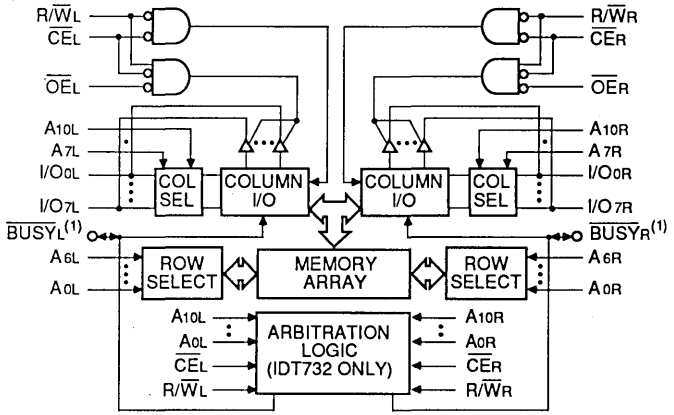
Both devices provide two independant ports with separate control, address and I/O pins that permit independent asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 375mW of power at maximum access times as fast as 20ns. Low-power (LA) versions offer battery backup data retention capability, with each dual-port typically consuming 200µw from a 2V battery.

The IDT7032/7042 devices are packaged in 48-pin sidebraze or plastic DIPs.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

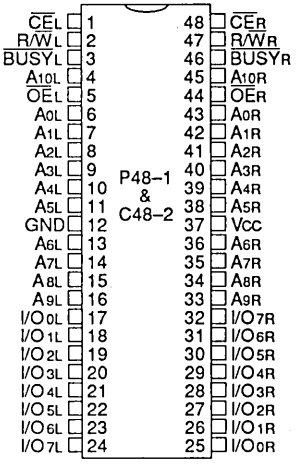
FUNCTIONAL BLOCK DIAGRAM



2693 drw 01

NOTE:
1. IDT7032 (MASTER): $\overline{BUSY}$ is open drain output and requires pullup resistor.
   IDT7042 (SLAVE): $\overline{BUSY}$ is input.

PIN CONFIGURATIONS



2693 drw 02

DIP
Top View

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

2693 tbl 01

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0v ± 10%
Commercial	0°C to +70°C	0V	5.0v ± 10%

2693 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

2693 tbl 03

NOTE:

1. VIL (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ±10%)

Symbol	Parameter	Test Conditions	IDT7032SA IDT7042SA Min.	IDT7032SA IDT7042SA Max.	IDT7032LA IDT7042LA Max.	IDT7032LA IDT7042LA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O_0-I/O_7)	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$)	I_{OL} = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2693 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version		7032 x 20[2] 7042 x 20[2] Typ.	7032 x 20[2] 7042 x 20[2] Max.	7032 x 25 7042 x 25 Typ.	7032 x 25 7042 x 25 Max.	7032 x 35 7042 x 35 Typ.	7032 x 35 7042 x 35 Max.	7032 x 45[3] 7042 x 45[3] Typ.	7032 x 45[3] 7042 x 45[3] Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	MIL.	SA	—	—	75	300	75	280	75	270	mA
				LA	—	—	75	220	75	200	75	190	
			COM'L.	SA	75	260	75	250	75	240	—	—	
				LA	75	190	75	180	75	180	—	—	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE_L}$ and $\overline{CE_R}$ ≥ V_{IH} f = f_{MAX}[4]	MIL.	SA	—	—	25	75	25	75	25	75	mA
				LA	—	—	25	55	25	55	25	55	
			COM'L.	SA	25	65	25	65	25	65	—	—	
				LA	25	45	25	45	25	45	—	—	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE_L}$ or $\overline{CE_R}$ ≥ V_{IH} Active Port Outputs Open, f = f_{MAX}[4]	MIL.	SA	—	—	50	180	46	170	40	160	mA
				LA	—	—	50	140	46	130	40	125	
			COM'L.	SA	50	180	50	170	40	155	—	—	
				LA	50	135	50	120	40	110	—	—	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE_L}$ and $\overline{CE_R}$ ≥ Vcc -0.2V V_{IN} ≥ Vcc -0.2V or V_{IN} ≤ 0.2V, f = 0[5]	MIL.	SA	—	—	1.2	40	1.2	35	1.0	35	mA
				LA	—	—	0.4	10	0.4	10	0.2	10	
			COM'L.	SA	1.2	15	1.2	15	1.0	15	—	—	
				LA	0.4	4	0.4	4	0.2	4	—	—	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs, f = 0[5])	One Port $\overline{CE_L}$ or $\overline{CE_R}$ ≥ Vcc -0.2V V_{IN} ≥ Vcc -0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	MIL.	SA	—	—	50	170	45	150	40	140	mA
				LA	—	—	46	135	42	115	35	105	
			COM'L.	SA	50	160	50	150	45	135	—	—	
				LA	46	125	46	115	42	105	—	—	

2693 tbl 05

NOTES:
1. x in part numbers indicates power rating (SA or LA).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.

7

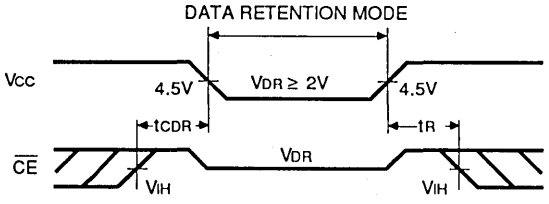
DATA RETENTION CHARACTERISTICS (LA Version Only)

Symbol	Parameter	Test Conditions		IDT7032LA/IDT7042LA Min.	Typ.	Max.	Unit
V_{DR}	Vcc for Data Retention	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC}$ -0.2V		2.0	—	0	V
I_{CCDR}	Data Retention Current		MIL.	—	100	4000	µA
			COM'L.	—	100	1500	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V		0	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	ns

2693 tbl 06

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM



2693 drw 03

AC TEST CONDITIONS

Input Pulse Levels	GND TO 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 & 3

2693 tbl 07

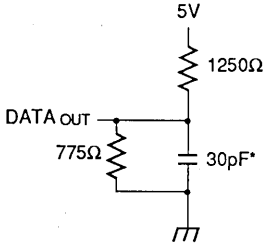


Figure 1. Output Load

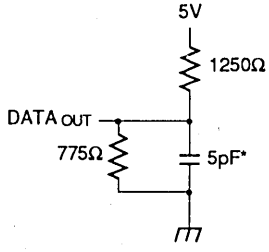


Figure 2. Output Load (for t_{HV}, t_{LZ}, t_{WZ}, and t_{OW})

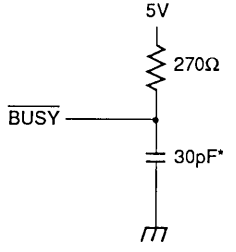


Figure 3. $\overline{BUSY}$ Output Load (IDT7032 only)

2693 drw 04

* Including scope and jig

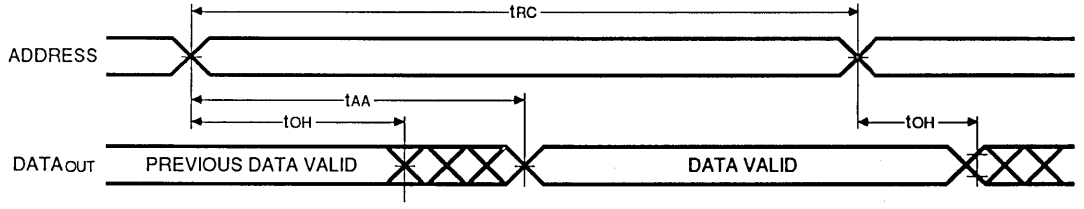
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (5)

Symbol	Parameter	7032 x 20 (2) 7042 x 20 (2) Min.	Max.	7032 x 25 7042 x 25 Min.	Max.	7032 x 35 7042 x 35 Min.	Max.	7032 x 45 (3) 7042 x 45 (3) Min.	Max.	Unit
Read Cycle										
tRC	Read Cycle Time	20	—	25	—	35	—	45	—	ns
tAA	Address Access Time	—	20	—	25	—	35	—	45	ns
tACE	Chip Enable Access Time	—	20	—	25	—	35	—	45	ns
tAOE	Output Enable Access Time	—	10	—	12	—	25	—	30	ns
tOH	Output Hold From Address Change	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time (1,4)	0	—	0	—	0	—	0	—	ns
tHZ	Output High Z Time (1,4)	—	8	—	10	—	15	—	20	ns
tPU	Chip Enable to Power Up Time (4)	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time (4)	—	50	—	50	—	50	—	50	ns

2693 tbl 08

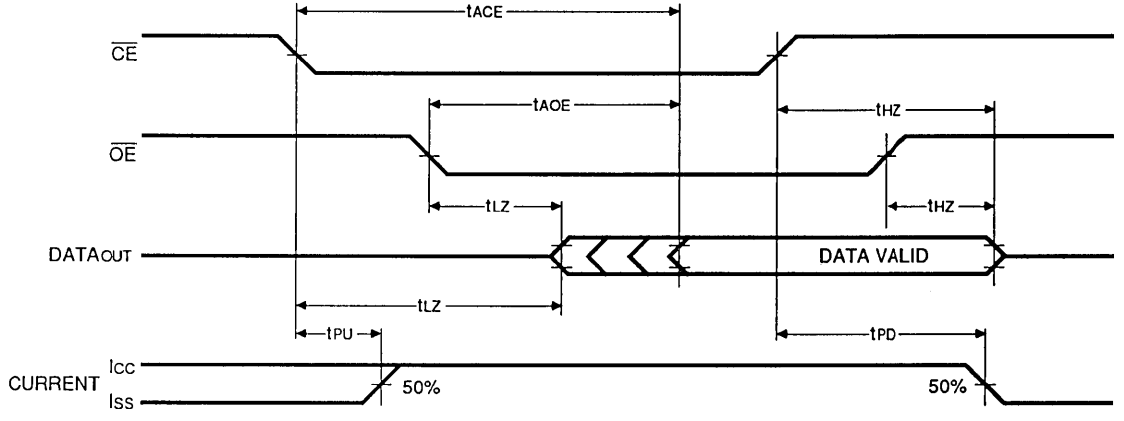
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. "x" in part numbers indicates power rating (SA or LA).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE (1,2,4)



2693 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1,3)



NOTES:
1. R/W is high for Read Cycles.
2. Device is continuously enabled, CE = VIL.
3. Addresses valid prior to or coincident with CE transition low.
4. OE = VIL.

2693 drw 06

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[7]

Symbol	Parameter	7032 x 20[2] 7042 x 20[2] Min.	Max.	7032 x 25 7042 x 25 Min.	Max.	7032 x 35 7042 x 35 Min.	Max.	7032 x 45[3] 7042 x 45[3] Min.	Max.	Unit
Write Cycle										
tWC	Write Cycle Time[5]	20	—	25	—	35	—	45	—	ns
tEW	Chip Enable to End of Write	15	—	20	—	30	—	35	—	ns
tAW	Address Valid to End of Write	15	—	20	—	30	—	35	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width[6]	15	—	20	—	30	—	35	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	10	—	12	—	20	—	20	—	ns
tHZ	Output High Z Time[1,4]	—	8	—	10	—	15	—	20	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z[1,4]	—	8	—	10	—	15	—	20	ns
tOW	Output Active From End of Write [1,4]	0	—	0	—	0	—	0	—	ns

2693 tbl 09

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, $t_{WC} = t_{BAA} + t_{WP}$.
6. Specified for $\overline{OE}$ at high (Refer to "Timing Waveform of Write Cycle", Note 7)
7. "x" in part numbers indicates power rating (SA or LA).

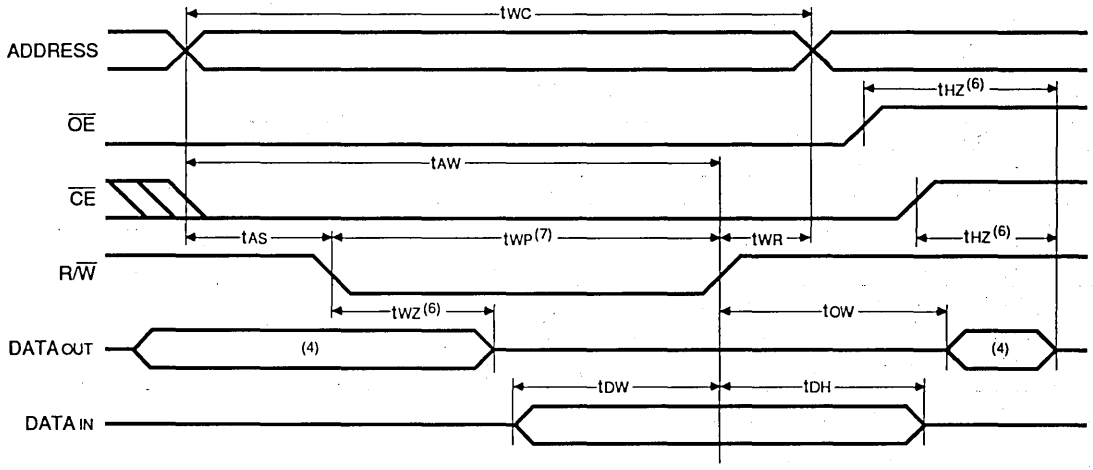
CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{IN} = 0V	11	pF

2693 tbl 10

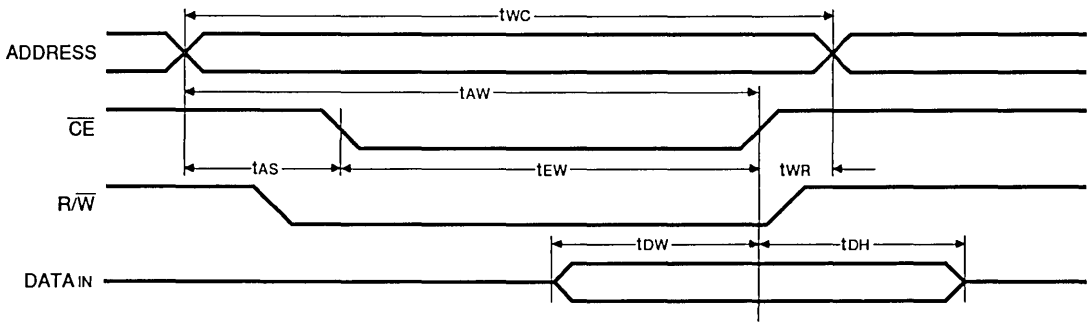
NOTE:
1. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/$\overline{W}$ CONTROLLED TIMING)(1,2,3,7)



2693 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING)(1,2,3,5)



2693 drw 08

NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

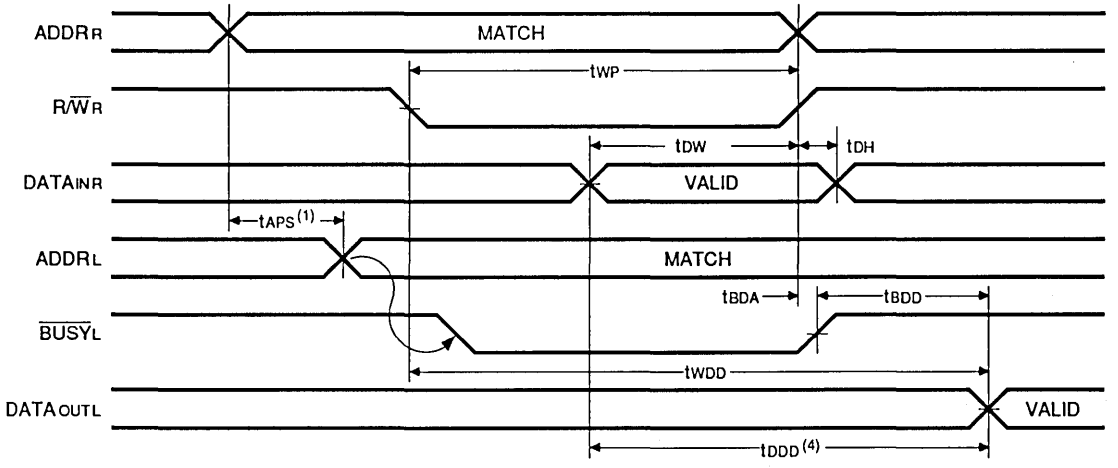
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(8)

Symbol	Parameter	7032 x 20(1) 7042 x 20(1) Min.	Max.	7032 x 25 7042 x 25 Min.	Max.	7032 x 35 7042 x 35 Min.	Max.	7032 x 45(2) 7042 x 45(2) Min.	Max.	Unit
Busy Timing (For Master IDT7032 Only)										
tBAA	$\overline{BUSY}$ Access Time to Address	—	20	—	25	—	35	—	35	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	18	—	20	—	30	—	35	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable	—	20	—	20	—	30	—	30	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable	—	18	—	20	—	25	—	25	ns
tWDD	Write Pulse to Data Delay(3)	—	45	—	50	—	60	—	70	ns
tDDD	Write Data Valid to Read Data Delay(3)	—	30	—	35	—	45	—	55	ns
tAPS	Arbitration Priority Set-up Time(4)	5	—	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data(5)	—	Note 5	—	Note 5	—	Note 5	—	Note 5	ns
Busy Input Timing (For Slave IDT7042 Only)										
tWB	Write to $\overline{BUSY}$ Input(6)	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$(7)	12	—	15	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay(9)	—	45	—	50	—	60	—	70	ns
tDDD	Write Data Valid to Read Data Delay(9)	—	30	—	35	—	45	—	55	ns

2693 tbl 11

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (For Master IDT7032 only)".
4. To ensure that the earlier of the two ports wins.
5. tBDD is a calculated parameter and is the greater of 0, tWDD-tWP (actual) or tDDD - tDW (actual).
6. To ensure that the write cycle is inhibited during contention.
7. To ensure that a write cycle is completed after contention.
8. "x" in part numbers indicates power rating (SA or LA).
9. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With Port-to-Port Delay (For Slave IDT7042 Only)".

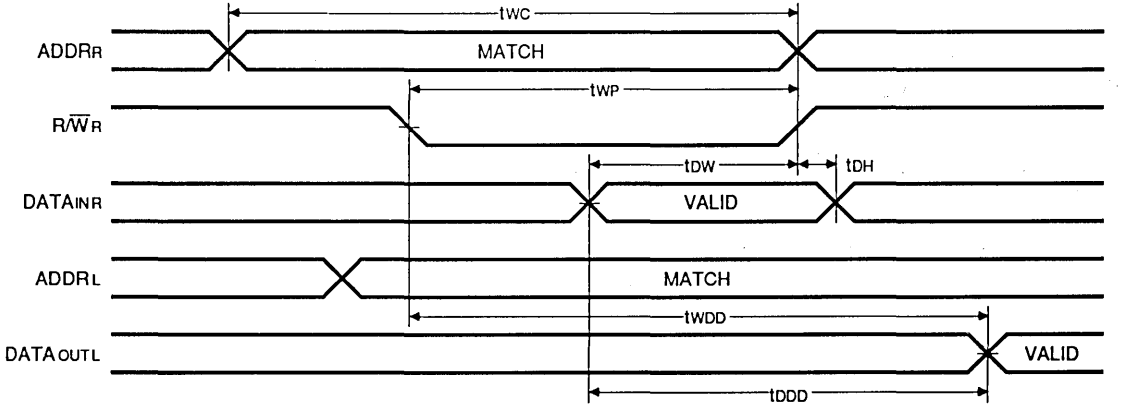
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$ (1,2,3) (FOR MASTER IDT7032 ONLY)



2693 drw 09

NOTES:
1. To ensure that the earlier of the two ports wins.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.
4. $\overline{OE}$ at LO for the reading port.

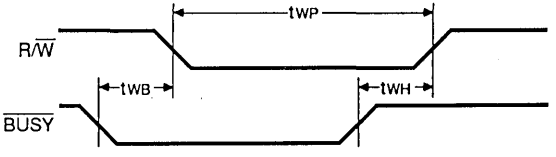
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY (1,2,3) (FOR SLAVE IDT7042 ONLY)



2693 drw 10

NOTES:
1. Assume $\overline{BUSY}$ input at HI for the writing port, and $\overline{OE}$ at LO for the reading port.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.

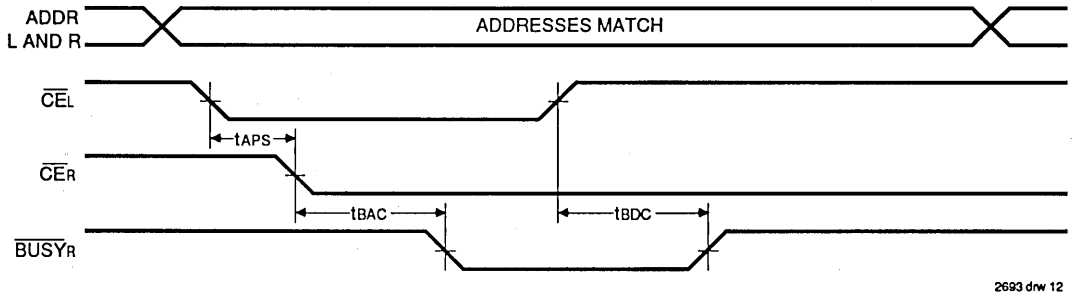
TIMING WAVEFORM OF WRITE WITH BUSY INPUT (FOR SLAVE IDT7042 ONLY)



2693 drw 11

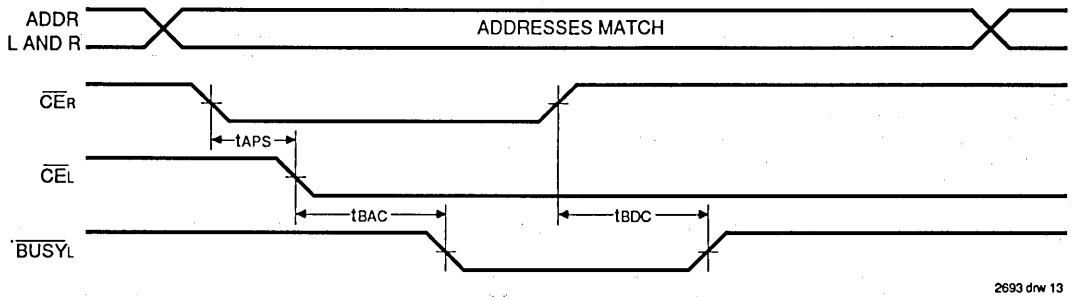
TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION (FOR MASTER IDT7032 ONLY)

$\overline{CE}_L$ VALID FIRST:



2693 drw 12

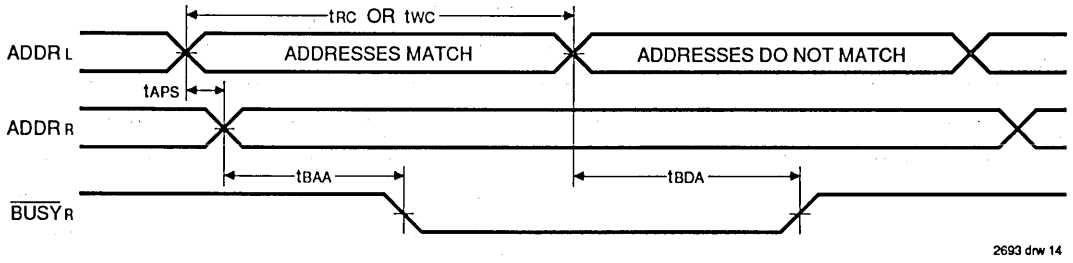
$\overline{CE}_R$ VALID FIRST:



2693 drw 13

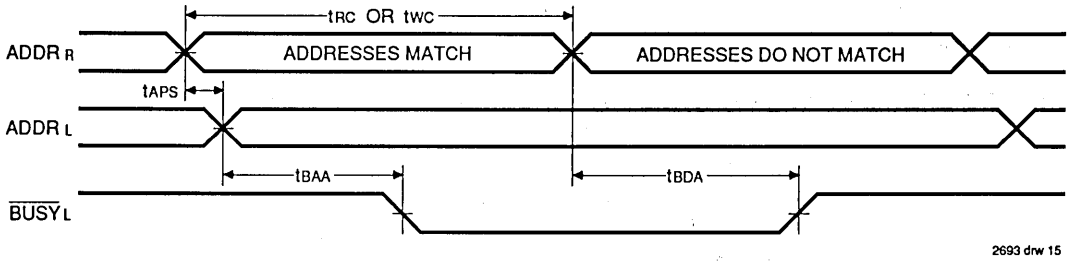
TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION (1) (FOR MASTER IDT7032 ONLY)

LEFT ADDRESS VALID FIRST:



2693 drw 14

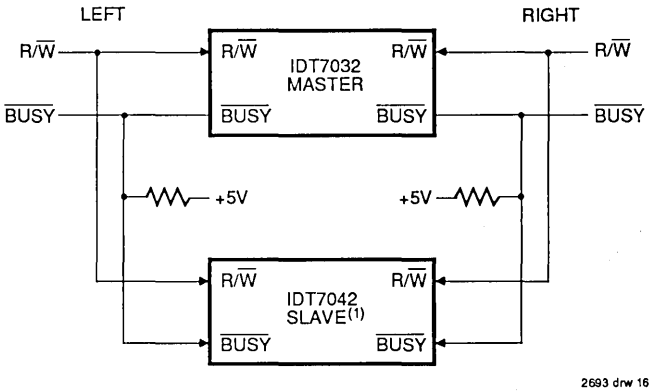
RIGHT ADDRESS VALID FIRST:



2693 drw 15

NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$

16-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



NOTE:
1. No arbitration in IDT7042 (SLAVE). BUSY-IN inhibits write in IDT7042 (SLAVE).

FUNCTIONAL DESCRIPTION

The IDT7032/42 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any locations in memory. These devices have an automatic power down feature controlled by CE. The CE controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected (CE high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control (OE). In the read mode, the port's OE turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table 1.

ARBITRATION LOGIC FUNCTIONAL DESCRIPTION

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active BUSY flag will be set for the delayed port.

The BUSY flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's BUSY flag. BUSY is set at speeds that permit the processor to hold the operation and its respective address data. It is important to note that the operation is invalid for the port that has BUSY set LOW. The delayed port will have access when BUSY goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before CE, on-chip control logic arbitrates between CEL and CER for access; or (2) if the CEs are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table II). In either mode of arbitration, the delayed port's BUSY flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION MASTER/SLAVE DESCRIPTION

Expanding the data bus width to sixteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its BUSYL while another aciti-vates its BUSYR signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one arbitrator, in the MASTER, is used. The SLAVE has BUSY inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMS in width, the writing of the SLAVE RAMS must be delayed, until after the BUSY input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past BUSY to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than on chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to BUSY from the MASTER.

TRUTH TABLES

TABLE I – NON-CONTENTION READ/WRITE CONTROL (4)

Left Or Right Port(1)				Function
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	
X	H	X	Z	Port Disabled and in Power Down Mode I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	DATAIN	Data on Port Written into Memory(2)
H	L	L	DATAOUT	Data in Memory Output on Port(3)
H	L	H	Z	High Impedance Outputs

2693 tbl 12

NOTES:
1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$
2. If $\overline{BUSY}$ = L, data is not written
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

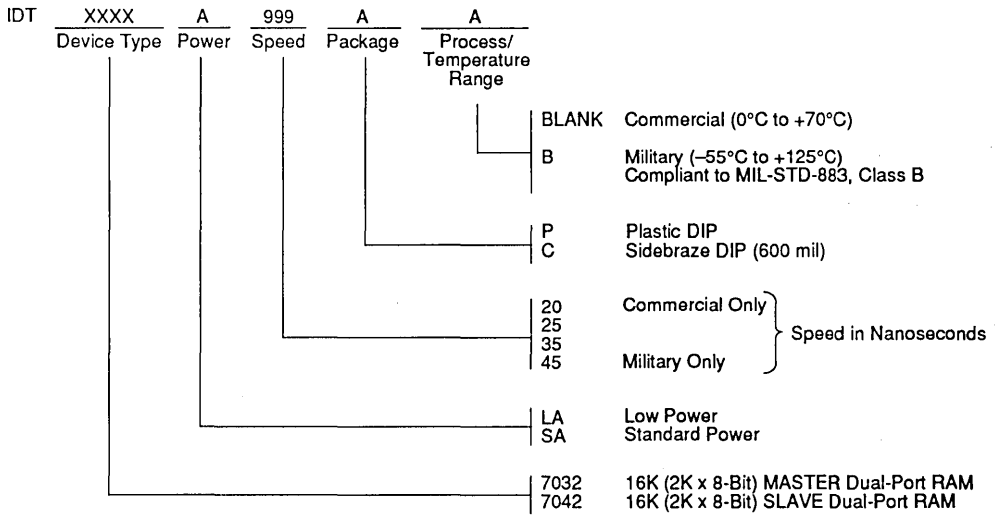
TABLE II – ARBITRATION (1,2)

Left Port		Right Port		Flags(2)		Function
$\overline{CE}_L$	$A_{0L} - A_{10L}$	$\overline{CE}_R$	$A_{0R} - A_{10R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R} - A_{10R}$	L	$\neq A_{0L} - A_{10L}$	H	H	No Contention
Address Arbitration With $\overline{CE}$ Low Before Address Match						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ Arbitration With Address Match Before $\overline{CE}$						
LL5R	$= A_{0R} - A_{10R}$	LL5R	$= A_{0L} - A_{10L}$	H	L	L-Port Wins
RL5L	$= A_{0R} - A_{10R}$	RL5L	$= A_{0L} - A_{10L}$	L	H	R-Port Wins
LW5R	$= A_{0R} - A_{10R}$	LW5R	$= A_{0L} - A_{10L}$	H	L	Arbitration Resolved
LW5R	$= A_{0R} - A_{10R}$	LW5R	$= A_{0L} - A_{10L}$	L	H	Arbitration Resolved

2693 tbl 13

NOTES:
1. X = DON'T CARE, L = LOW, H = HIGH
2. LV5R = Left Address Valid ≥ 5ns before right address.
   RV5L = Right Address Valid ≥ 5ns before left address.
   Same = Left and Right Addresses match within 5ns of each other.
   LL5R = Left $\overline{CE}$ = LOW ≥ 5ns before Right $\overline{CE}$.
   RL5L = Right $\overline{CE}$ = LOW ≥ 5ns before Left $\overline{CE}$.
   LW5R = Left and Right $\overline{CE}$ = LOW within 5ns of each other.

ORDERING INFORMATION



2693 drw 17

7

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 16K (2K x 8-BIT) WITH INTERRUPTS

IDT71321SA/LA
IDT71421SA/LA

FEATURES:

- High-speed access
  - —Military: 25/30/35/45/55/70ns (max.)
  - —Commercial: 20/25/30/35/45/55ns (max.)
- Low-power operation
  - —IDT71321/IDT71421SA
    - Active: 325mW (typ.)
    - Standby: 5mW (typ.)
  - —IDT71321/421LA
    - Active: 325mW (typ.)
    - Standby: 1mW (typ.)
- Two $\overline{INT}$ flags for port-to-port communications
- MASTER IDT71321 easily expands data bus width to 16-or-more-bits using SLAVE IDT71421
- On-chip port arbitration logic (IDT71321 only)
- $\overline{BUSY}$ output flag on IDT71321; $\overline{BUSY}$ input on IDT71421
- Fully asynchronous operation from either port
- Battery backup operation -2V data retention
- TTL-compatible, single 5V ±10% power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

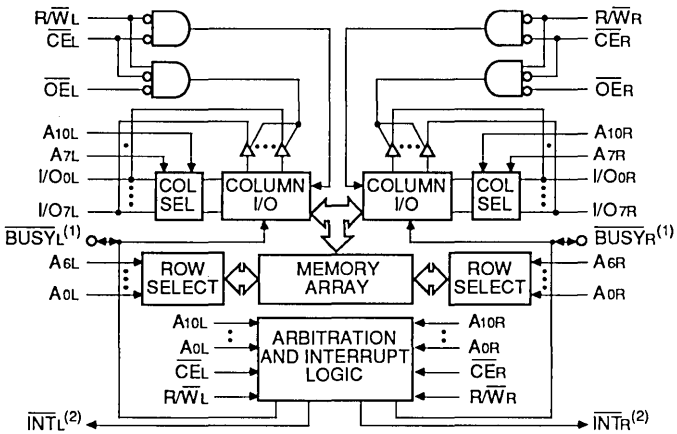
The IDT71321/IDT71421 are high-speed 2K x 8 dual-port static RAMs with internal interrupt logic for interprocessor communications. The IDT71321 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "MASTER" dual-port RAM, together with the IDT71421 "SLAVE" dual-port,in 16-or-more-bit memory systems applications results in full speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 325mW of power at maximum access times as fast as 20ns. Low-power (LA) versions offer battery backup data retention capability, with each dual-port typically consuming 200µw from a 2V battery.

The IDT71321/IDT71421 devices are packaged in 52-pin LCCs and PLCCs. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM

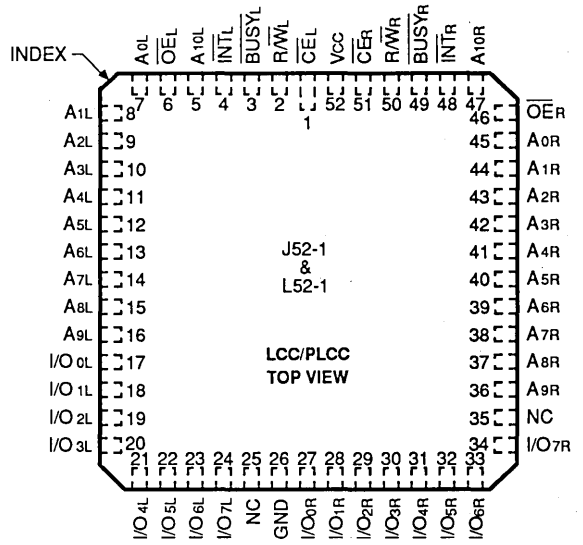


2691 drw 01

NOTES:
1. IDT71321 (MASTER): $\overline{BUSY}$ is open output and requires pullup resistor. IDT71421 (SLAVE): $\overline{BUSY}$ is input.
2. Open drain output: requires pullup resistor.

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



2691 drw 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

2691 tbl 01

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2691 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

2691 tbl 03

NOTE:

1. VIL (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (VCC = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT71321SA IDT71421SA Min.	IDT71321SA IDT71421SA Max.	IDT71321LA IDT71421LA Min.	IDT71321LA IDT71421LA Max.	Unit
|ILI|	Input Leakage Current	VCC = 5.5V, VIN = 0V to VCC	—	10	—	5	µA
|ILO|	Output Leakage Current	$\overline{CE}$ = VIH, VOUT = 0V to VCC	—	10	—	5	µA
VOL	Output Low Voltage (I/O0-I/O7)	IOL = 4mA	—	0.4	—	0.4	V
VOL	Open Drain Output Low Voltage ($\overline{BUSY}$/$\overline{INT}$)	IOL = 16mA	—	0.5	—	0.5	V
VOH	Output High Voltage	IOH = -4mA	2.4	—	2.4	—	V

2691 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version		71321x20[2] 71421x20[2] Typ.	71321x20[2] 71421x20[2] Max.	71321x25/30 71421x25/30 Typ.	71321x25/30 71421x25/30 Max.	71321x35 71421x35 Typ.	71321x35 71421x35 Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	Mil.	SA	—	—	75/75	300/290	75	280	mA
				LA	—	—	75/75	220/210	75	200	
			Com'l.	SA	75	260	75/70	250/240	75	195	
				LA	75	190	75/70	180/170	75	155	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ f = f_{MAX}[4]	Mil.	SA	—	—	25/25	75/75	25	75	mA
				LA	—	—	25/25	55/55	25	55	
			Com'l.	SA	25	65	25/25	65/65	25	65	
				LA	25	45	25/25	45/45	25	45	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	—	—	50/46	180/175	40	170	mA
				LA	—	—	50/46	140/135	40	130	
			Com'l.	SA	50	180	50/46	170/155	40	130	
				LA	50	130	50/46	120/110	40	95	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$, f = 0[5]	Mil.	SA	—	—	1.2/1.2	40/40	1.2	35	mA
				LA	—	—	0.4/0.4	10/10	0.4	10	
			Com'l.	SA	1.2	15	1.2/1.2	15/15	1.0	15	
				LA	0.4	4	0.4/0.4	4/4	0.2	4.0	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs, f = 0[5])	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$ Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	—	—	50/45	170/160	45	150	mA
				LA	—	—	46/42	135/125	42	115	
			Com'l.	SA	50	160	50/45	150/137	40	115	
				LA	46	125	46/42	115/105	35	90	

2691 tbl 05

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version		71321x45 71421x45 Typ.	71321x45 71421x45 Max.	71321x55 71421x55 Typ.	71321x55 71421x55 Max.	71321x70[3] 71421x70[3] Typ.	71321x70[3] 71421x70[3] Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	Mil.	SA	75	230	65	230	65	225	mA
				LA	75	185	65	185	65	180	
			Com'l.	SA	75	190	60	180	—	—	
				LA	75	145	60	140	—	—	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ f = f_{MAX}[4]	Mil.	SA	25	65	25	65	25	65	mA
				LA	25	55	25	55	25	55	
			Com'l.	SA	25	65	25	65	—	—	
				LA	25	45	25	45	—	—	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	40	135	40	135	40	135	mA
				LA	40	110	40	110	40	110	
			Com'l.	SA	40	120	40	115	—	—	
				LA	40	85	40	85	—	—	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$, f = 0[5]	Mil.	SA	1.0	30	1.0	30	1.0	30	mA
				LA	0.2	10	0.2	10	0.2	10	
			Com'l.	SA	1.0	15	1.0	15	—	—	
				LA	0.2	4.0	0.2	4.0	—	—	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs, f = 0[5])	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$ Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	40	125	40	120	40	110	mA
				LA	35	95	35	90	35	80	
			Com'l.	SA	40	115	40	100	—	—	
				LA	35	80	35	75	—	—	

2691 tbl 06

NOTES:
1. "x" in part numbers indicates power rating (SA or LA).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of $1/t_{RC}$, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.

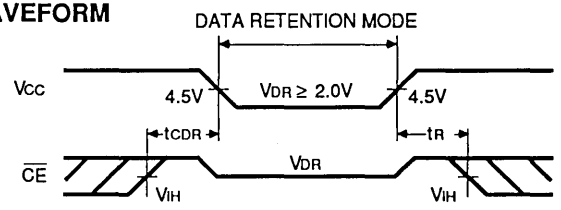
DATA RETENTION CHARACTERISTICS (LA Version Only)

Symbol	Parameter	Test Condition		IDT71321LA/IDT71421LA Min.	Typ.	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$		2.0	—	0	V
I_{CCDR}	Data Retention Current		MIL.	—	100	4000	µA
			COM'L.	—	100	1500	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	ns

2691 tbl 07

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM



2691 drw 03

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2, 3 and 4

2691 tbl 08

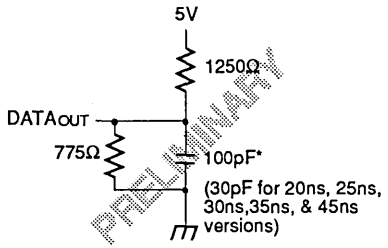


Figure 1. Output Load

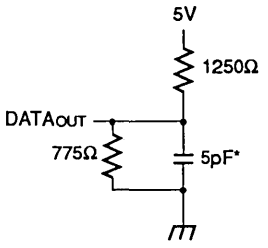


Figure 2. Output Load (for tHZ, tLZ, tWZ, and tow)

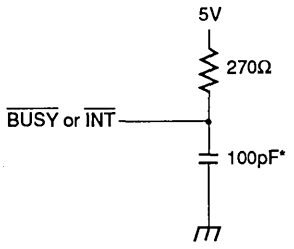


Figure 3. $\overline{BUSY}$ and $\overline{INT}$ Output Load

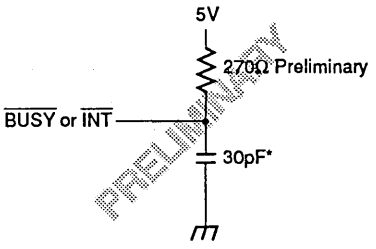


Figure 4. $\overline{BUSY}$ and $\overline{INT}$ Output Load (for 20ns,25ns and 30ns versions)

* Including scope and jig.

2691 drw 04

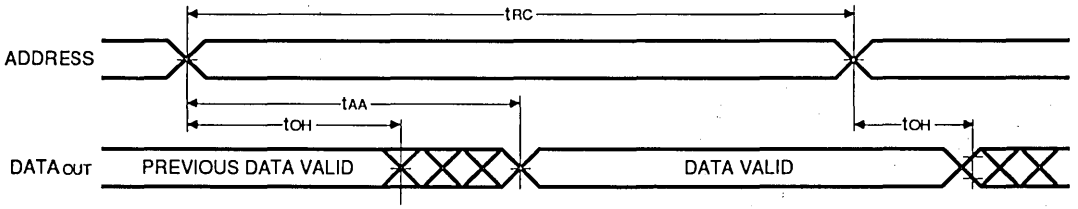
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

Symbol	Parameter	71321x20 (2) 71421x20 (2) Min.	Max.	71321x25/30 71421x25/30 Min.	Max.	71321x35 71421x35 Min.	Max.	71321x45 71421x45 Min.	Max.	71321x55 71421x55 Min.	Max.	71321x70(3) 71421x70(3) Min.	Max.	Unit
Read Cycle														
tRC	Read Cycle Time	20	—	25/30	—	35	—	45	—	55	—	70	—	ns
tAA	Address Access Time	—	20	—	25/30	—	35	—	45	—	55	—	70	ns
tACE	Chip Enable Access Time	—	20	—	25/30	—	35	—	45	—	55	—	70	ns
tAOE	Output Enable Access Time	—	10	—	12/15	—	25	—	30	—	35	—	40	ns
tOH	Output Hold From Address Change	0	—	0/0	—	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time(1,4)	0	—	0/0	—	5	—	5	—	5	—	5	—	ns
tHZ	Output High Z Time(1,4)	—	8	—	10/12	—	15	—	20	—	30	—	35	ns
tPU	Chip Enable to Power Up Time(4)	0	—	0/0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time(4)	—	50	—	50/50	—	50	—	50	—	50	—	50	ns

2691 tbl 09

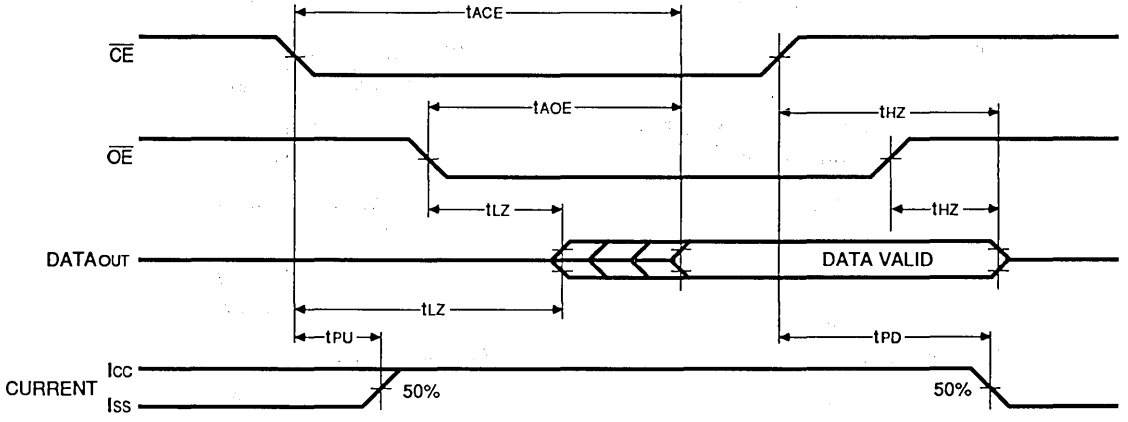
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2, 3 and 4).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. "x" in part numbers indicates power rating (SA or LA).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE (1,2,4)



2691 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1,3)



2691 drw 06

NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = VIL.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = VIL.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

Symbol	Parameter	71321x20 [2] 71421x20 [2] Min.	Max.	71321x25/30 71421x25/30 Min.	Max.	71321x35 71421x35 Min.	Max.	Unit
Write Cycle								
tWC	Write Cycle Time[5]	20	—	25/30	—	35	—	ns
tEW	Chip Enable to End of Write	15	—	20/25	—	30	—	ns
tAW	Address Valid to End of Write	15	—	20/25	—	30	—	ns
tAS	Address Set-up Time	0	—	0/0	—	0	—	ns
tWP	Write Pulse Width	15	—	20/25	—	30	—	ns
tWR	Write Recovery Time	0	—	0/0	—	0	—	ns
tDW	Data Valid to End of Write	10	—	12/15	—	20	—	ns
tHZ	Output High Z Time[1,4]	—	8	—	10/12	—	15	ns
tDH	Data Hold Time	0	—	0/0	—	0	—	ns
tWZ	Write Enabled to Output in High Z[1,4]	—	8	—	10/12	—	15	ns
tOW	Output Active From End of Write[1,4]	0	—	0/0	—	0	—	ns

2691 tbl 10

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (CONTINUED)

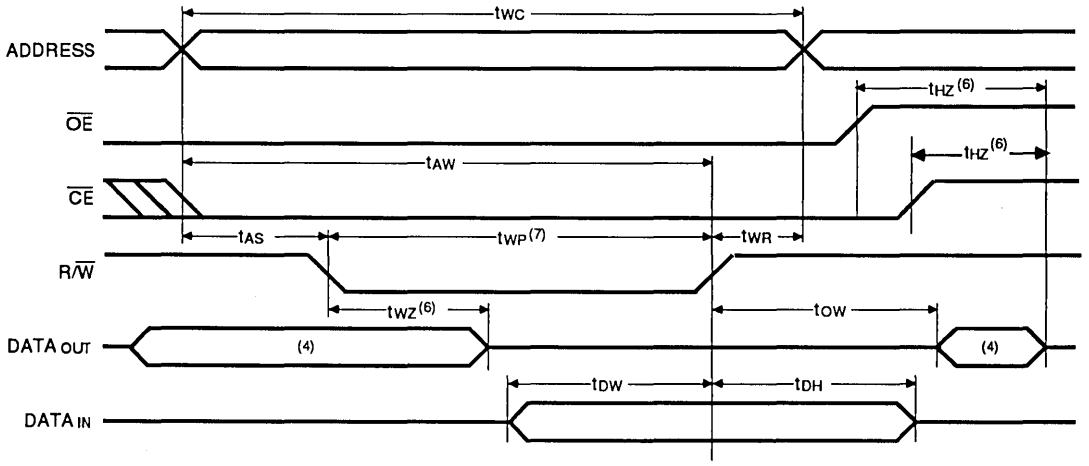
Symbol	Parameter	71321x45 71421x45 Min.	Max.	71321x55 71421x55 Min.	Max.	71321x70 [3] 71421x70 [3] Min.	Max.	Unit
Write Cycle								
tWC	Write Cycle Time[5]	45	—	55	—	70	—	ns
tEW	Chip Enable to End of Write	35	—	40	—	50	—	ns
tAW	Address Valid to End of Write	35	—	40	—	50	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width	35	—	40	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	20	—	20	—	30	—	ns
tHZ	Output High Z Time[1,4]	—	20	—	30	—	35	ns
tDH	Data Hold Time	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z[1,4]	—	20	—	30	—	35	ns
tOW	Output Active From End of Write[1,4]	0	—	0	—	0	—	ns

2691 tbl 11

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2, 3 and 4).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, tWC = tBAA + tWP.
6. "x" in part numbers indicates power rating (SA or LA).

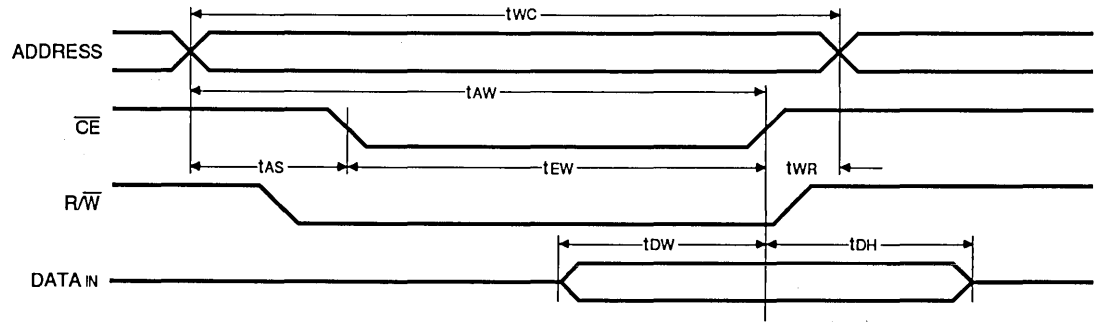
7

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING (1,2,3,7)



2691 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING (1,2,3,5)



2691 drw 08

NOTES:
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

Symbol	Parameter	71321x20 (1) 71421x20 (1) Min.	Max.	71321x25/30 71421x25/30 Min.	Max.	71321x35 71421x35 Min.	Max.	Unit
Busy Timing (For Master IDT71321 Only)								
tBAA	$\overline{BUSY}$ Access Time to Address	—	20	—	25/30	—	35	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	18	—	20/25	—	30	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable	—	20	—	20/25	—	30	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable	—	18	—	20/25	—	25	ns
tWDD	Write Pulse to Data Delay (3)	—	45	—	50/55	—	60	ns
tDDD	Write Data Valid to Read Data Delay (3)	—	30	—	33/33	—	35	ns
tAPS	Arbitration Priority Set-up Time (4)	5	—	5/5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data (5)	—	Note 5	—	Note 5	—	Note 5	ns
Busy Timing (For Slave IDT71421 Only)								
tWB	Write to $\overline{BUSY}$ Input (6)	0	—	0/0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$ (7)	12	—	15/20	—	20	—	ns
tWDD	Write Pulse to Data Delay (9)	—	45	—	50/55	—	60	ns
tDDD	Write Data Valid to Read Data Delay (9)	—	30	—	35/35	—	35	ns

2691 tbl 12

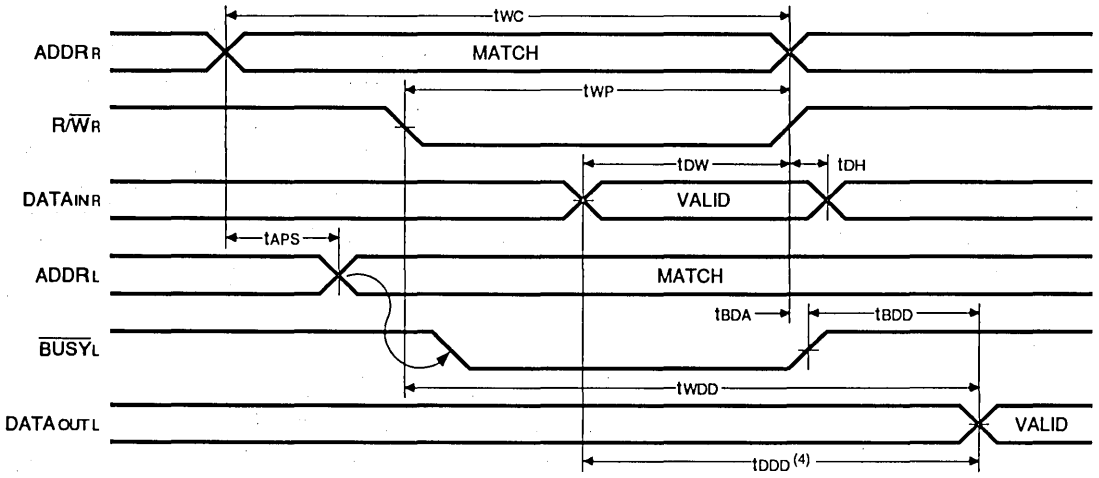
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (CONTINUED)

Symbol	Parameter	71321x45 71421x45 Min.	Max.	71321x55 71421x55 Min.	Max.	71321x70(2) 71421x70(2) Min.	Max.	Unit
Busy Timing (For Master IDT71321 Only)								
tBAA	$\overline{BUSY}$ Access Time to Address	—	35	—	45	—	45	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	35	—	40	—	40	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable	—	30	—	35	—	35	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable	—	25	—	30	—	30	ns
tWDD	Write Pulse to Data Delay (3)	—	70	—	80	—	90	ns
tDDD	Write Data Valid to Read Data Delay (3)	—	45	—	55	—	70	ns
tAPS	Arbitration Priority Set-up Time (4)	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data (5)	—	Note 5	—	Note 5	—	Note 5	ns
Busy Timing (For Slave IDT71421 Only)								
tWB	Write to $\overline{BUSY}$ Input (6)	0	—	0	—	—	—	ns
tWH	Write Hold After $\overline{BUSY}$ (7)	20	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay (9)	—	70	—	80	90	—	ns
tDDD	Write Data Valid to Read Data Delay (9)	—	45	—	55	—	70	ns

2691 tbl 13

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With BUSY (For Master IDT71321 only)".
4. To ensure that the earlier of the two ports wins.
5. tBDD is a calculated parameter and is the greater of 0, tWDD-tWP (actual) or tDDD - tDW (actual).
6. To ensure that the write cycle is inhibited during contention.
7. To ensure that a write cycle is completed after contention.
8. "x" in part numbers indicates power rating (SA or LA).
9. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With Port-to-Port Delay (For Slave IDT71421 Only)".

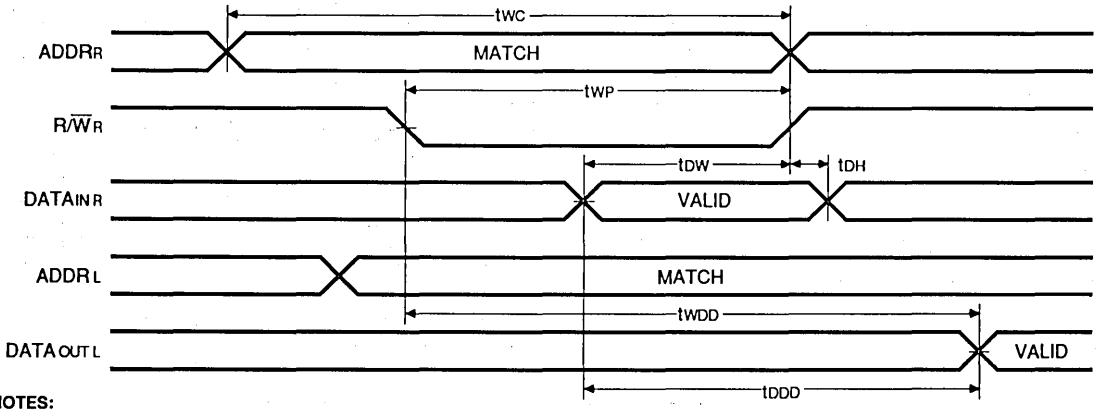
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$ (1,2,3) (FOR MASTER IDT71321)



2691 drw 09

NOTES:
1. To ensure that the earlier of the two ports wins.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.
4. $\overline{OE}$ at LO for the reading port.

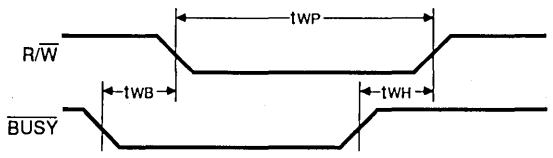
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY (1,2,3) (FOR SLAVE IDT71421 ONLY)



2691 drw 10

NOTES:
1. Assume $\overline{BUSY}$ input at HI for the writing port, and $\overline{OE}$ at LO for the reading port.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.

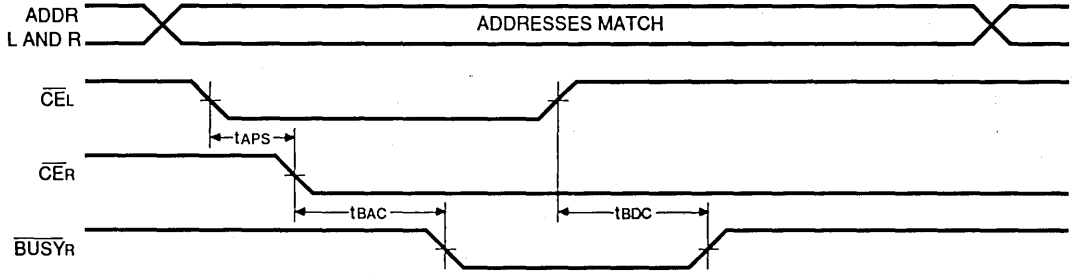
TIMING WAVEFORM OF WRITE WITH BUSY (FOR SLAVE IDT71421)



2691 drw 11

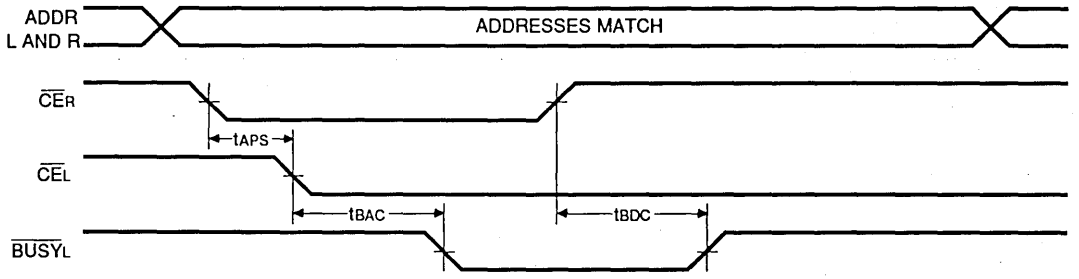
TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION (FOR MASTER IDT71321 ONLY)

$\overline{CE}_L$ VALID FIRST:



$\overline{CE}_R$ VALID FIRST:

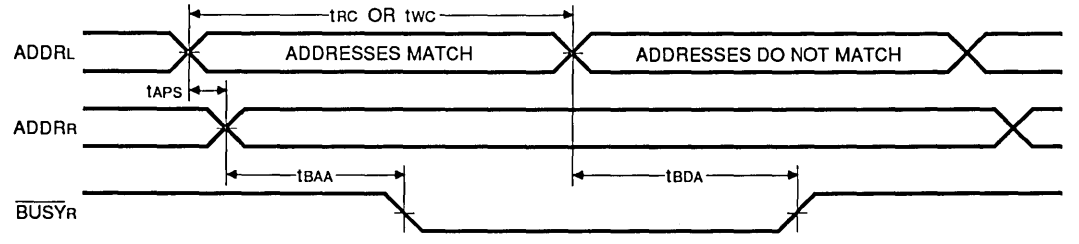
2691 drw 12



2691 drw 13

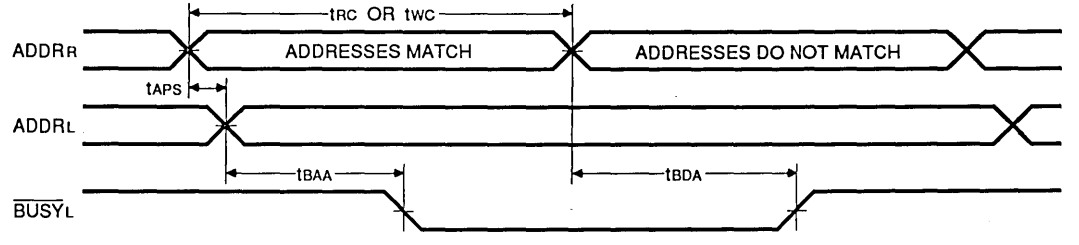
TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION (FOR MASTER IDT71321 ONLY)(1)

LEFT ADDRESS VALID FIRST:



2691 drw 14

RIGHT ADDRESS VALID FIRST:



NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$

2691 drw 15

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

Symbol	Parameter	71321SA/LA20(1) 71421SA/LA20(1) Min.	Max.	71321SA/LA25/30 71421SA/LA25/30 Min.	Max.	71321SA/LA35 71421SA/LA35 Min.	Max.	Unit
Interrupt Timing								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	20	—	25/30	—	35	ns
tINR	Interrupt Reset Time	—	20	—	25/30	—	35	ns

2691 tbl 14

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (CONTINUED)

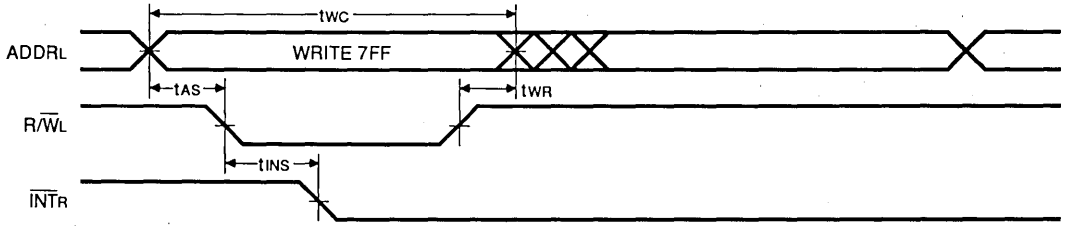
Symbol	Parameter	71321SA/LA45 71421SA/LA45 Min.	Max.	71321SA/LA55 71421SA/LA55 Min.	Max.	71321SA/LA70(2) 71421SA/LA70(2) Min.	Max.	Unit
Interrupt Timing								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	40	—	45	—	50	ns
tINR	Interrupt Reset Time	—	40	—	45	—	50	ns

2691 tbl 15

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.

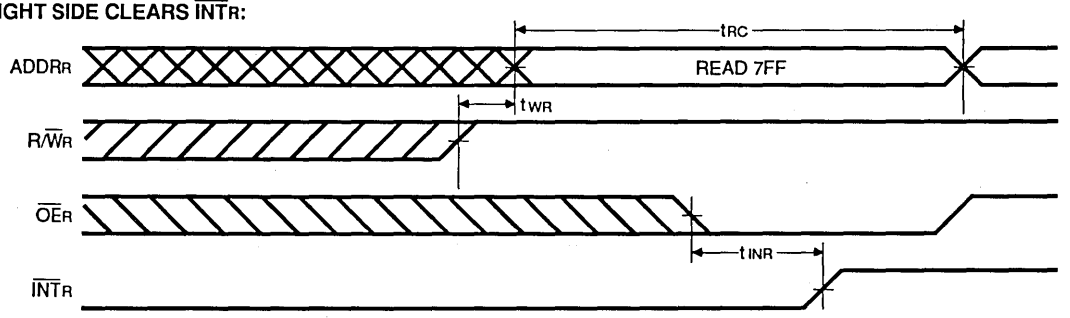
TIMING WAVEFORM OF INTERRUPT MODE (1, 2)

LEFT SIDE SETS $\overline{INT}_R$:



2691 drw 16

RIGHT SIDE CLEARS $\overline{INT}_R$:

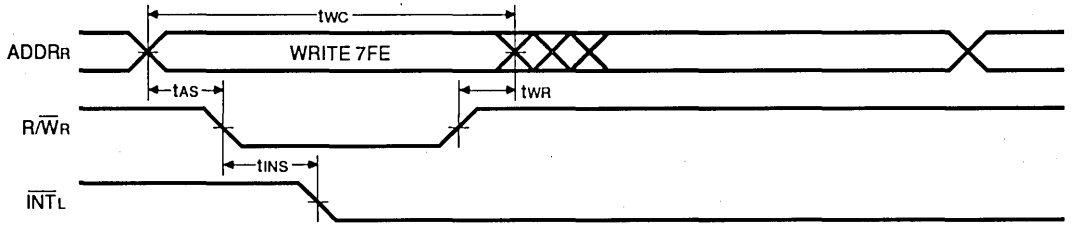


2691 drw 17

NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
2. $\overline{INT}_L$ and $\overline{INT}_R$ are reset (HIGH) during power up.

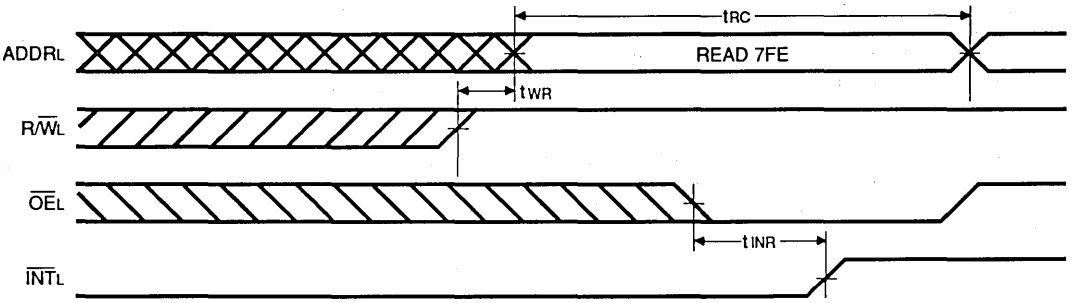
TIMING WAVEFORM OF INTERRUPT MODE (1, 2)

RIGHT SIDE SETS $\overline{INT}_L$:



2691 drw 18

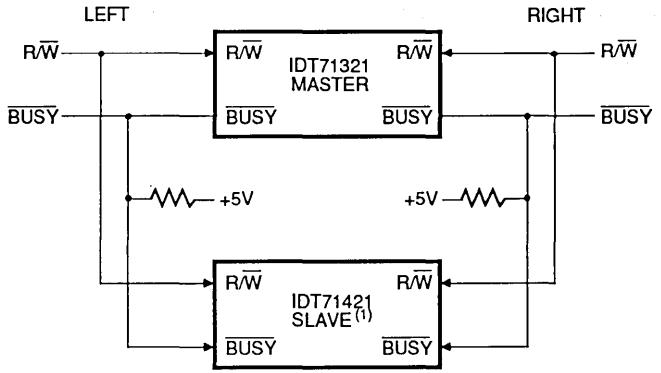
LEFT SIDE CLEARS $\overline{INT}_L$:



2691 drw 19

NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
2. $\overline{INT}_R$ and $\overline{INT}_L$ are reset (HIGH) during power up.

16-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



2691 drw 20

NOTE:
1. No arbitration in IDT71421 (SLAVE). $\overline{BUSY}$-IN inhibits write in IDT71421 (SLAVE).

FUNCTIONAL DESCRIPTION

The IDT71321/IDT71421 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any locations in memory. These devices have an automatic power-down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power-down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table 1.

The interrupt flag ($\overline{INT}$) permits communication between ports or systems. If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$)is set when the right port writes to memory location 7FE (HEX). The left port clears the interrupt by reading address location 7FE. Likewise, the right port interrupt flag (INT_R) is set when the left port writes to memory location 7FF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 7FF. The message (8 bits) at 7FE or 7FF is user-defined. If the interrupt function is not used, address locations 7FE and 7FF are not used as mail boxes but as part of the random access memory. Refer to Table II for the interrupt operation.

ARBITRATION LOGIC FUNCTIONAL DESCRIPTION

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table III). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION MASTER/SLAVE DESCRIPTION

Expanding the data bus width to sixteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another acitivates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMS in width, the writing of the SLAVE RAMs must be delayed, until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

TRUTH TABLES

TABLE I – NON-CONTENTION READ/WRITE CONTROL(4)

Left Or Right Port(1)				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	Function
X	H	X	Z	Port Disabled and in Power Down Mode I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	DATAIN	Data on Port Written into Memory(2)
H	L	L	DATAOUT	Data in Memory Output on Port(3)
H	L	H	Z	High Impedance Outputs

2691 tbl 16

NOTES:
1. A_{0L}-$A_{10L} \neq A_{0R}$-A_{10R}
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{BDD} timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter (1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{IN} = 0V	11	pF

2691 tbl 17

NOTE:
1. This parameter is determined by device characterization but is not 100% tested.

TABLE II – INTERRUPT FLAG(1, 4)

Left Port					Right Port					
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{10L}	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0L}-A_{10R}	$\overline{INT}_R$	Function
L	L	X	7FF	X	X	X	X	X	L(2)	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	7FF	H(3)	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L(3)	L	L	X	7FE	X(2)	Set Left $\overline{INT}_L$ Flag
X	L	L	7FE	H(2)	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

2691 tbl 18

NOTES:
1. Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then NC.
3. If $\overline{BUSY}_R$ = L, then NC.
4. H = HIGH, L = LOW, X = DON'T CARE, NC = NO CHANGE.

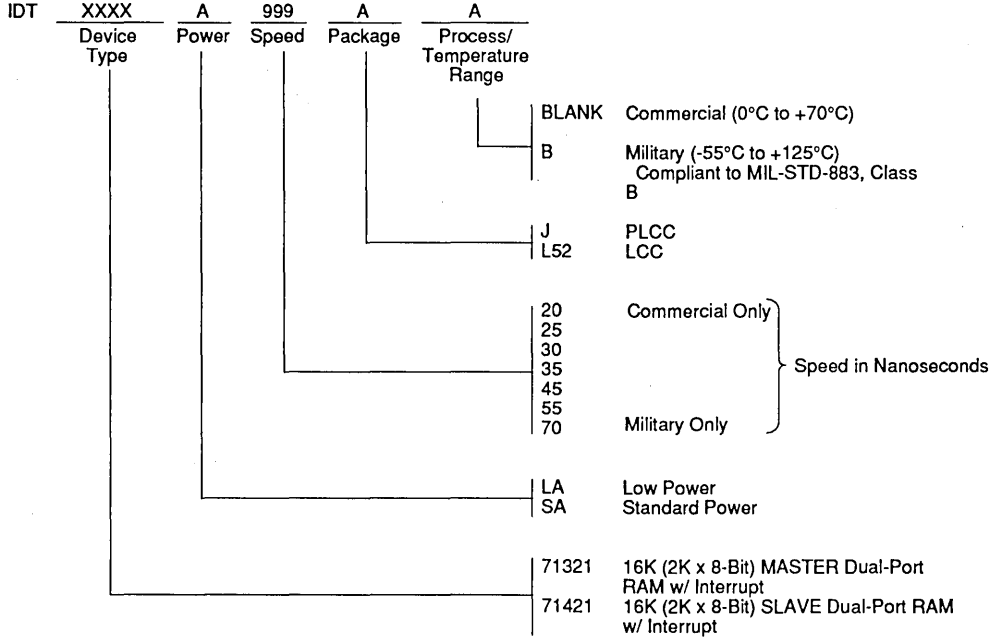
TABLE III – ARBITRATION(1, 2)

Left Port		Right Port		Flags		
$\overline{CE}_L$	A_{0L}-A_{10L}	$\overline{CE}_R$	A_{0R}-A_{10R}	$\overline{BUSY}_L$	$\overline{BUSY}_R$	Function
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	≠ A_{0R}-A_{10R}	L	≠ A_{0L}-A_{10L}	H	H	No Contention
Address Arbitration With $\overline{CE}$ Low Before Address Match						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ Arbitration With Address Match Before $\overline{CE}$						
LL5R	= A_{0R}-A_{10R}	LL5R	= A_{0L}-A_{10L}	H	L	L-Port Wins
RL5L	= A_{0R}-A_{10R}	RL5L	= A_{0L}-A_{10L}	L	H	R-Port Wins
LW5R	= A_{0R}-A_{10R}	LW5R	= A_{0L}-A_{10L}	H	L	Arbitration Resolved
LW5R	= A_{0R}-A_{10R}	LW5R	= A_{0L}-A_{10L}	L	H	Arbitration Resolved

2691 tbl 19

NOTES:
1. $\overline{INT}$ Flags Don't Care.
2. X = DON'T CARE, L = LOW, H = HIGH
   LV5R = Left Address Valid ≥ 5ns before right address.
   RV5L = Right Address Valid ≥ 5ns before left address.
   Same = Left and Right Addresses match within 5ns of each other.
   LL5R = Left $\overline{CE}$ = LOW ≥ 5ns before Right $\overline{CE}$.
   RL5L = Right $\overline{CE}$ = LOW ≥ 5ns before Left $\overline{CE}$.
   LW5R = Left and Right $\overline{CE}$ = LOW within 5ns of each other.

ORDERING INFORMATION



2691 drw 21

Integrated Device Technology, Inc.

HIGH-SPEED 2K x 9 DUAL-PORT STATIC RAM

PRELIMINARY
IDT7012

FEATURES:

- High-speed access
  - Military: 35/45/55/70ns (max.)
  - Commercial: 25/35/45/55ns (max.)
- Low-power operation
  - IDT7012S
    Active: 400mW (typ.)
    Standby: 7mW (typ.)
  - IDT7012L
    Active: 400mW (typ.)
    Standby: 2mW (typ.)
- Fully asychronous operation from either port
- Each port has a 9-bit wide data path. The 9th bit could be used as the parity bit
- Battery backup operation — 2V data retention
- TTL compatible, single 5V (±10%) power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7012 is a high-speed 2K x 9 dual-port static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when both sides simultaneously access the same dual-port location.

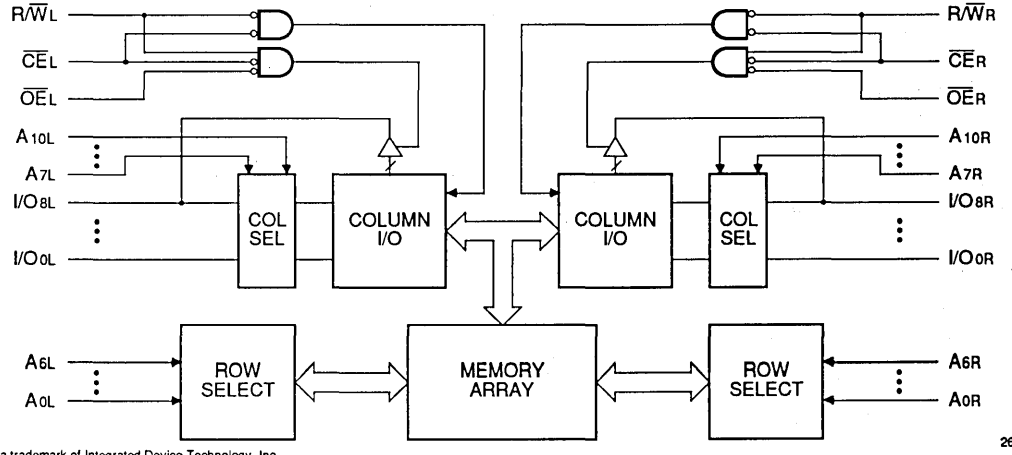
The IDT7012 provides two independent ports with separate control, address and I/O pins that permit independent, asychronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports. An automatic power-down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT7012 utilizes a 9-bit wide data path to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 400mW of power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 200µW from a 2V battery.

The IDT7012 is packaged in 48-pin sidebrazed or plastic DIPs, 48-pin LCCs and 48-pin flatpacks. The military devices are processed 100% in compliance to the test methods of MIL-STD-883, Method 5004.

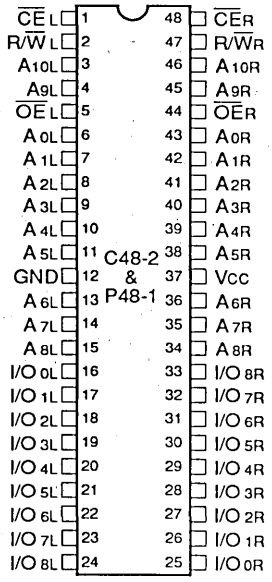
FUNCTIONAL BLOCK DIAGRAM



2653 drw 01

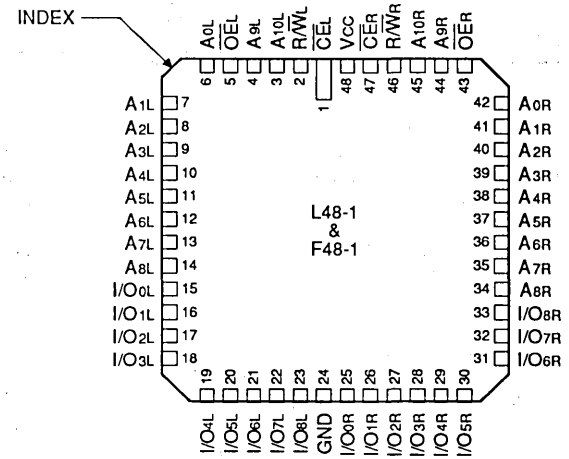
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



2653 drw 02

DIP
TOP VIEW



2653 drw 03

LCC/FLATPACK
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2653 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Condition	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Output Capacitance	VOUT = 0V	11	pF

NOTE: 2653 tbl 13

1. This parameter is sampled and not 100% tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2653 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0.0	V
VIH	Input High Votage	2.2	–	6.0	V
VIL	Input Low Voltage	–0.5(1)	–	0.8	V

NOTE: 2653 tbl 03

1. VIL = –3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	7012S		7012L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4	—	2.4	—	V

2653 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7012 x 25[2]		7012 x 35		7012 x 45		7012 x 55		7012 x 70[3]		Unit
					Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \le V_{IL}$ Outputs Open f = f_{MAX}[4]	Mil.	S	—	—	80	300	75	290	70	285	65	275	mA
				L	—	—	80	220	75	210	70	205	65	200	
			Com'l.	S	75	260	75	250	75	245	70	235	—	—	
				L	75	190	75	180	75	170	70	160	—	—	
I_{SB1}	Standby Current (Both Ports—TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \ge V_{IH}$ f = f_{MAX}[4]	Mil.	S	—	—	25	80	25	80	25	80	25	80	mA
				L	—	—	25	60	25	60	25	60	25	60	
			Com'l.	S	25	65	25	65	25	65	25	65	—	—	
				L	25	45	25	45	25	45	25	45	—	—	
I_{SB2}	Standby Current (One Port—TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \ge V_{IH}$ Active Port Outputs Open, f = f_{MAX}[4]	Mil.	S	—	—	50	190	45	180	40	170	40	165	mA
				L	—	—	50	145	45	140	40	140	40	135	
			Com'l.	S	50	175	46	160	45	150	40	140	—	—	
				L	50	125	46	115	45	105	40	95	—	—	
I_{SB3}	Full Standby Current (Both Ports—All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \ge V_{CC}$ – 0.2V $V_{IN} \ge V_{CC}$ – 0.2V or $V_{IN} \le$ 0.2V, f = 0[5]	Mil.	S	—	—	1.2	30	1.0	30	1.0	30	1.0	30	mA
				L	—	—	0.4	10	0.2	10	0.2	10	0.2	10	
			Com'l.	S	1.2	15	1.0	15	1.0	15	1.0	15	—	—	
				L	0.4	5	0.2	5	0.2	5	0.2	5	—	—	
I_{SB4}	Full Standby Current (One Port—All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ – 0.2V, $V_{IN} \ge V_{CC}$ – 0.2V or $V_{IN} \le$ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	Mil.	S	—	—	47	170	45	160	40	155	40	150	mA
				L	—	—	44	130	42	125	35	120	35	115	
			Com'l.	S	50	155	45	142	45	132	45	127	—	—	
				L	46	120	42	110	42	100	42	95	—	—	

2653 tbl 05

NOTES:
1. "x" in part numbers indicates power rating (S or L).
2. 0°C to +70°C temperature range only.
3. –55°C to +125°C temperature range only.
4. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.

7

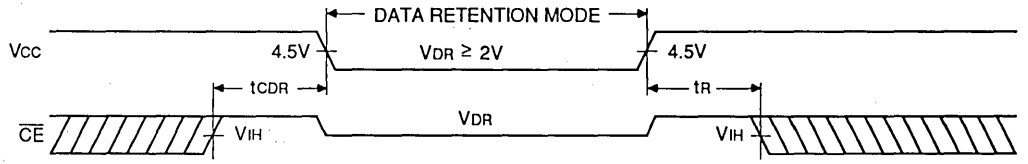
DATA RETENTION CHARACTERISTICS (L Version Only)

Symbol	Parameter	Test Condition		7012L Min.	7012L Typ.[1]	7012L Max.	Unit
V_{DR}	V_{CC} for Data Retention			2	—	—	V
I_{CCDR}	Data Retention Current	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC} - 0.2V$	Mil.	—	100	4000	µA
			Com'l.	—	100	1500	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but not tested.

2653 tbl 06

DATA RETENTION WAVEFORM

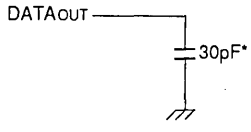


2653 drw 04

AC TEST CONDITIONS

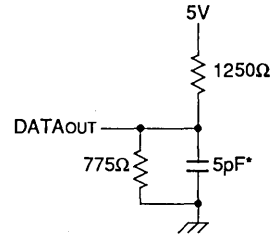
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2653 tbl 07



2653 drw 05

Figure 1. Output Load



2653 drw 06

Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})

* Including scope and jig.

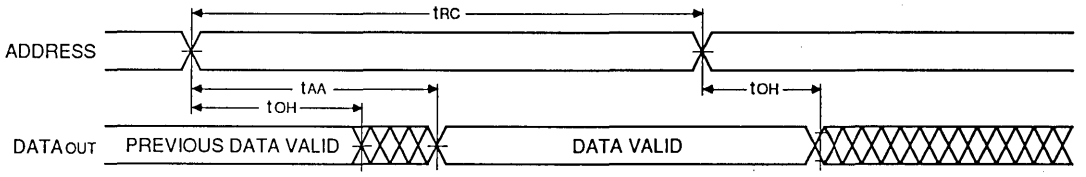
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[5]

Symbol	Parameter	7012 x 25[2] Min.	7012 x 25[2] Max.	7012 x 35 Min.	7012 x 35 Max.	7012 x 45 Min.	7012 x 45 Max.	7012 x 55 Min.	7012 x 55 Max.	7012 x 70[3] Min.	7012 x 70[3] Max.	Unit
Read Cycle												
tRC	Read Cycle Time	25	—	35	—	45	—	55	—	70	—	ns
tAA	Address Access Time	—	25	—	35	—	45	—	55	—	70	ns
tACE	Chip Enable Access Time	—	25	—	35	—	45	—	55	—	70	ns
tAOE	Output Enable Access Time	—	12	—	25	—	30	—	35	—	40	ns
tOH	Output Hold From Address Change	0	—	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time[1,4]	0	—	0	—	0	—	0	—	0	—	ns
tHZ	Output High Z Time[1,4]	—	10	—	15	—	20	—	30	—	35	ns
tPU	Chip Enable to Power-Up Time[4]	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power-Down Time[4]	—	50	—	50	—	50	—	50	—	50	ns

2653 tbl 08

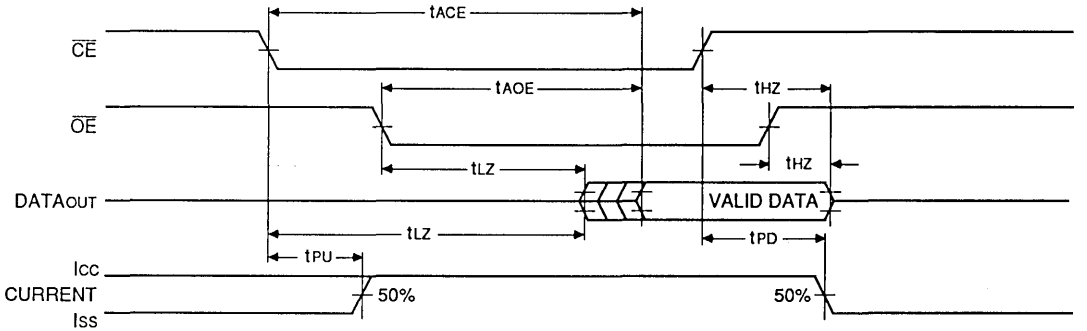
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. –55°C to +125°C range only.
4. This parameter guaranteed but not tested.
5. "x" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1, 2, 4]



2653 drw 09

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE[1, 3]



2653 drw 10

NOTES:
1. R/W is high for Read Cycles.
2. Device is continuously enabled, CE = VIL.
3. Addresses valid prior to coincident with CE transition low.
4. OE = VIL.

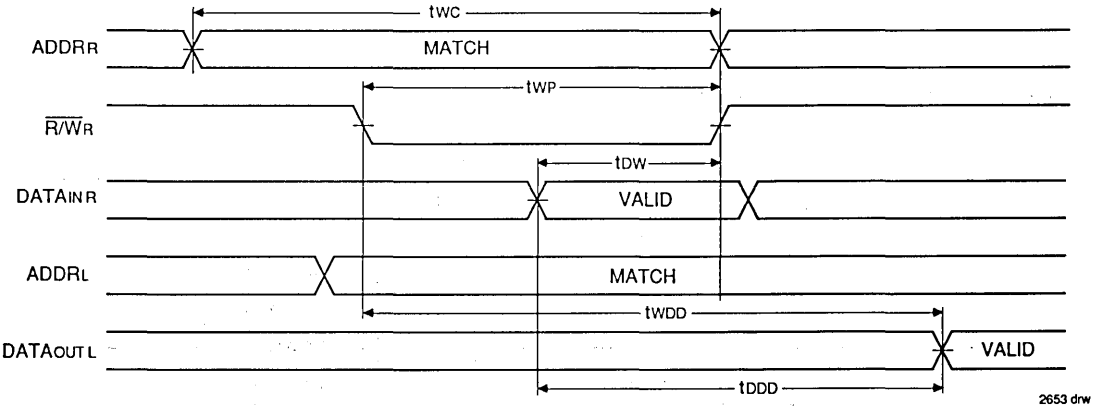
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[6]

Symbol	Parameter	7012 x 25[2]		7012 x 35		7012 x 45		7012 x 55		7012 x 70[3]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle												
tWC	Write Cycle Time	25	—	35	—	45	—	55	—	70	—	ns
tEW	Chip Enable to End of Write	20	—	30	—	35	—	40	—	50	—	ns
tAW	Address Valid to End of Write	20	—	30	—	35	—	40	—	50	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width[5]	20	—	30	—	35	—	40	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	12	—	20	—	20	—	20	—	30	—	ns
tHZ	Output High Z Time[1,4]	—	10	—	15	—	20	—	30	—	35	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z[1,4]	—	10	—	15	—	20	—	30	—	35	ns
tOW	Output Active From End of Write[1,4]	0	—	0	—	0	—	0	—	0	—	ns
tWDD	Write Pulse to Delay[4]	50	—	—	60	—	70	—	80	—	95	ns
tDDD	Write Data Valid to Read Data Delay[4]	—	35	—	45	—	55	—	65	—	80	ns

2653 tbl 09

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. 0°C to +70°C temperature range only.
3. –55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. Specified for $\overline{OE}$ at high (refer to "Timing Waveform of Write Cycle", Note 7).
6. "x" in part numbers indicates power rating (S or L).

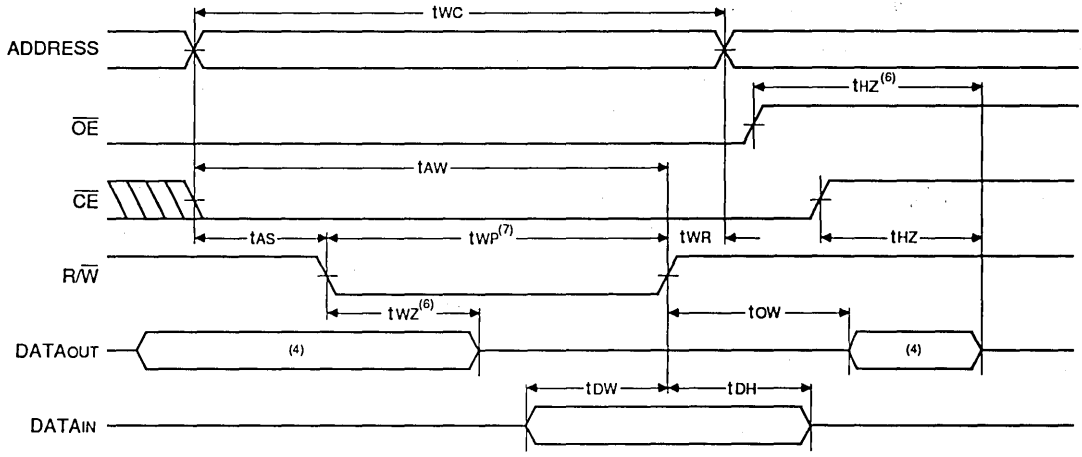
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY[1]



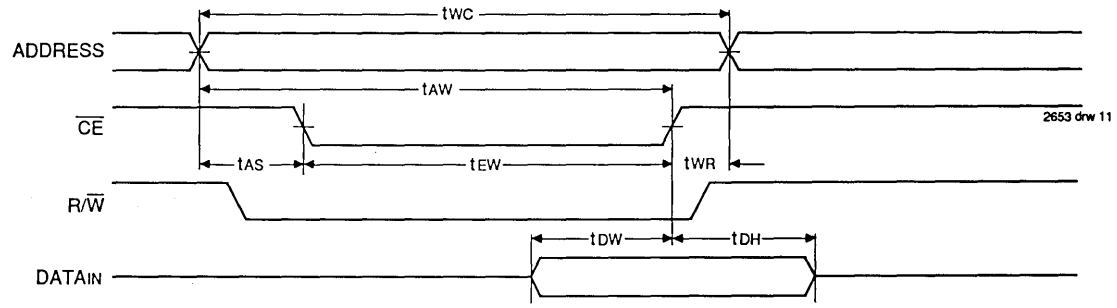
2653 drw 14

NOTE:
1. Write cycle parameters should be adhered to in order to ensure proper writing.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/$\overline{W}$ CONTROLLED TIMING)(1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ± 500mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

2653 drw 12

7

FUNCTIONAL DESCRIPTION

The IDT7012 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power-down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power-down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in the truth table below.

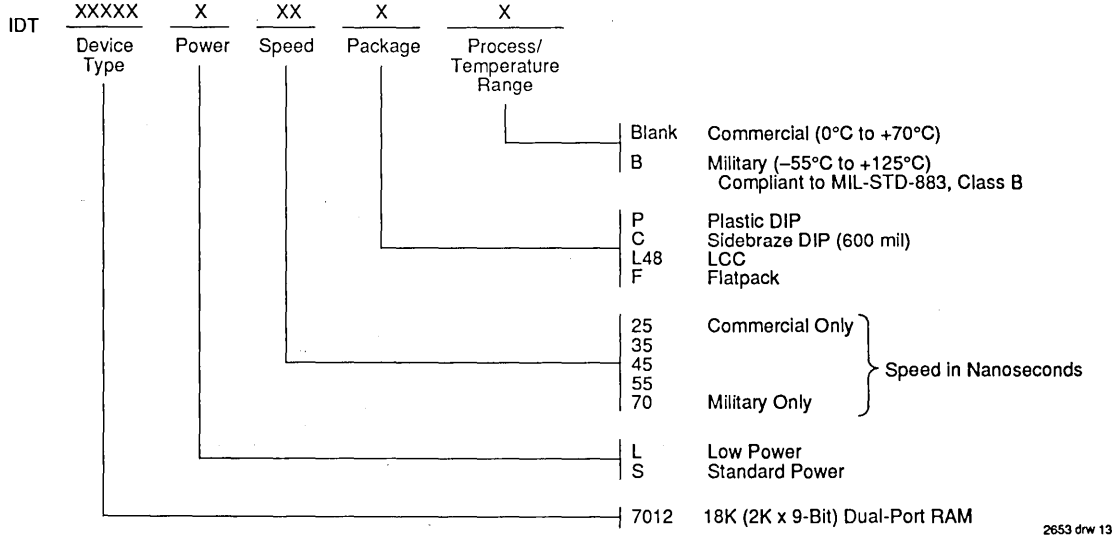
TRUTH TABLE NON-CONTENTION READ/WRITE CONTROL

Left or Right Port[1]				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-8}	Function
X	H	X	Z	Port Disabled and in Power-Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power-Down Mode, I_{SB1} or I_{SB3}
L	L	X	DATAIN	Data on Port Written Into Memory[2]
H	L	L	DATAOUT	Data in Memory Output on Port
X	X	H	Z	High Impedance Outputs

NOTES:
1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$
2. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

2653 tbl 11

ORDERING INFORMATION



2653 drw 13

Integrated Device Technology, Inc.

HIGH-SPEED 2K x 9 DUAL-PORT STATIC RAM WITH BUSY & INTERRUPT

PRELIMINARY
IDT70121S/L
IDT70125S/L

FEATURES:

- High-speed access
  - Military: 35/45/55/70ns (max.)
  - Commercial: 25/35/45/55ns (max.)
- Low-power operation
  - IDT70121/70125S
    Active: 400mW (typ.)
    Standby: 7mW (typ.)
  - IDT70121/70125L
    Active: 400mW (typ.)
    Standby: 7mW (typ.)
- Fully asychronous operation from either port
- MASTER IDT70121 easily expands data bus width to 18 bits or more using SLAVE IDT70125 chip
- On-chip port arbitration logic (IDT70121 only)
- $\overline{BUSY}$ output flag on Master; $\overline{BUSY}$ input on Slave
- $\overline{INT}$ flag for port-to-port communication
- Battery backup operation—2V data retention
- TTL compatible, signal 5V (±10%) power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

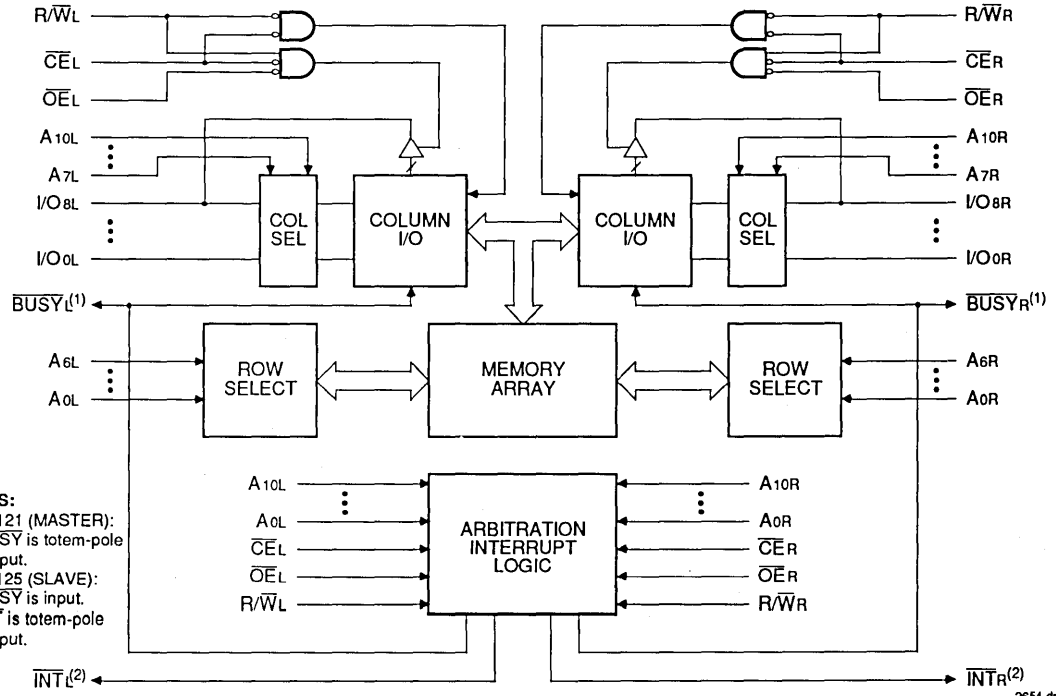
The IDT70121/IDT70125 are high-speed 2K x 9 dual-port static RAMs. The IDT70121 is designed to be used as a stand-alone 9-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT70125 "SLAVE" dual-port in 18-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 18-bit-or-wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power-down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT70121/IDT70125 utilizes a 9-bit wide data path to allow for Data/Control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

Fabricated using IDT's CEMOS™ high-performance

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. 70121 (MASTER): $\overline{BUSY}$ is totem-pole output.
   70125 (SLAVE): $\overline{BUSY}$ is input.
2. $\overline{INT}$ is totem-pole output.

2654 drw 01

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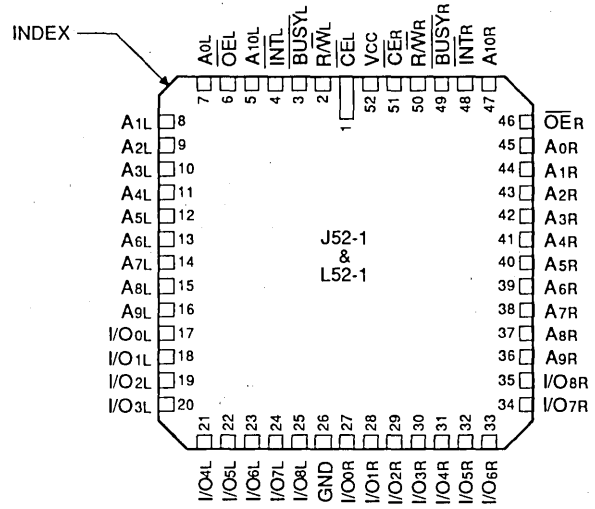
MILITARY AND COMMERCIAL TEMPERATURE RANGES **SEPTEMBER 1990**

DESCRIPTION (Continued):

technology, these devices typically operate on only 400mW of power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability with each port typically consuming 200µW from a 2V battery.

The IDT70121/IDT70125 devices are packaged in 52-pin LCCs and 52-pin PLCCs. The military devices are processed 100% in compliance to the test methods of MIL-STD-883, Method 5004.

PIN CONFIGURATIONS



2654 drw 02

LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2654 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2654 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0.0	V
VIH	Input High Votage	2.2	–	6.0	V
VIL	Input Low Voltage	–0.5(1)	–	0.8	V

NOTE: 2654 tbl 03

1. VIL = –3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	70121S 70125S Min.	70121S 70125S Max.	70121L 70125L Min.	70121L 70125L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4	—	2.4	—	V

2654 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Version		70121 x 25[2] 70125 x 25[2] Typ.	70121 x 25[2] 70125 x 25[2] Max.	70121 x 35 70125 x 35 Typ.	70121 x 35 70125 x 35 Max.	70121 x 45 70125 x 45 Typ.	70121 x 45 70125 x 45 Max.	70121 x 55 70125 x 55 Typ.	70121 x 55 70125 x 55 Max.	70121 x 70[3] 70125 x 70[3] Typ.	70121 x 70[3] 70125 x 70[3] Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \le V_{IL}$ Outputs Open f = f_{MAX}[4]	Mil.	S	—	—	80	300	75	290	70	285	65	275	mA
				L	—	—	80	220	75	210	70	205	65	200	
			Com'l.	S	75	260	75	250	75	245	70	235	—	—	
				L	75	190	75	180	75	170	70	160	—	—	
I_{SB1}	Standby Current (Both Ports—TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \ge V_{IH}$ f = f_{MAX}[4]	Mil.	S	—	—	25	80	25	80	25	80	25	80	mA
				L	—	—	25	60	25	60	25	60	25	60	
			Com'l.	S	25	65	25	65	25	65	25	65	—	—	
				L	25	45	25	45	25	45	25	45	—	—	
I_{SB2}	Standby Current (One Port—TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \ge V_{IH}$ Active Port Outputs Open, f = f_{MAX}[4]	Mil.	S	—	—	50	190	45	180	40	170	40	165	mA
				L	—	—	50	145	45	140	40	140	40	135	
			Com'l.	S	50	175	46	160	40	150	40	140	—	—	
				L	50	125	46	115	40	105	40	95	—	—	
I_{SB3}	Full Standby Current (Both Ports—CMOS Level Inputs)	Both Ports $\overline{CE}_R$ and $\overline{CE}_L \ge V_{CC}$ – 0.2V $V_{IN} \ge V_{CC}$ – 0.2V or $V_{IN} \le$ 0.2V, f = 0[5]	Mil.	S	—	—	1.2	30	1.0	30	1.0	30	1.0	30	mA
				L	—	—	0.4	10	0.2	10	0.2	10	0.2	10	
			Com'l.	S	1.2	15	1.2	15	1.0	15	1.0	15	—	—	
				L	0.4	5	0.4	5	0.2	5	0.2	5	—	—	
I_{SB4}	Full Standby Current (One Port—CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ – 0.2V, $V_{IN} \ge V_{CC}$ – 0.2V or $V_{IN} \le$ 0.2V, Active Port Outputs Open, f = f_{MAX}[4]	Mil.	S	—	—	47	170	45	160	40	155	40	150	mA
				L	—	—	44	130	42	125	35	120	35	115	
			Com'l.	S	50	155	45	142	45	132	45	127	—	—	
				L	45	120	42	110	42	100	42	95	—	—	

2654 tbl 05

NOTES:
1. "x" in part numbers indicates power rating (S or L).
2. 0°C to +70°C temperature range only.
3. –55°C to +125°C temperature range only.
4. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.

7

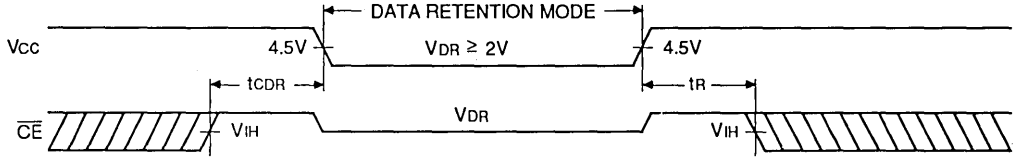
DATA RETENTION CHARACTERISTICS (L Version Only)

Symbol	Parameter	Test Condition		70121L/70125L Min.	Typ.(1)	Max.	Unit
V_{DR}	Vcc for Data Retention			2	—	—	V
I_{CCDR}	Data Retention Current	Vcc = 2.0V, $\overline{CE}$ ≥ Vcc – 0.2V	Mil.	—	100	4000	µA
			Com'l.	—	100	1500	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time	VIN ≥ Vcc – 0.2V or VIN ≤ 0.2V		0	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	ns

NOTES:
1. Vcc = 2V, TA = +25°C.
2. tRC = Read Cycle Time.
3. This parameter is guaranteed but not tested.

2654 tbl 06

DATA RETENTION WAVEFORM

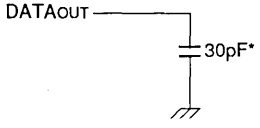


2654 drw 03

AC TEST CONDITIONS

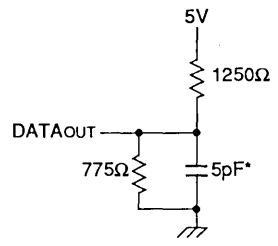
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 & 3

2654 tbl 07



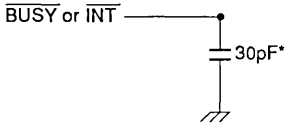
2654 drw 04

Figure 1. Output Load



2654 drw 05

Figure 2. Output Load (for tHZ, tLZ, tWZ, and tOW)



2654 drw 06

Figure 3. $\overline{BUSY}$ and $\overline{INT}$ Output Load

* Including scope and jig.

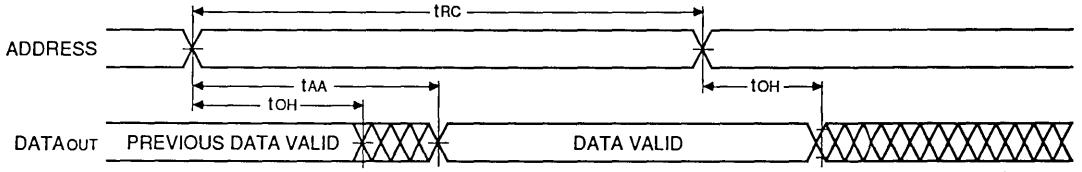
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(5)

Symbol	Parameter	70121 x 25(2) 70125 x 25(2) Min.	Max.	70121 x 35 70125 x 35 Min.	Max.	70121 x 45 70125 x 45 Min.	Max.	70121 x 55 70125 x 55 Min.	Max.	70121 x 70(3) 70125 x 70(3) Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	25	—	35	—	45	—	55	—	70	—	ns
tAA	Address Access Time	—	25	—	35	—	45	—	55	—	70	ns
tACE	Chip Enable Access Time	—	25	—	35	—	45	—	55	—	70	ns
tAOE	Output Enable Access Time	—	12	—	25	—	30	—	35	—	40	ns
tOH	Output Hold from Address Change	0	—	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time(1,4)	0	—	0	—	0	—	0	—	0	—	ns
tHZ	Output High Z Time(1,4)	—	10	—	15	—	20	—	30	—	35	ns
tPU	Chip Enable to Power-Up Time(4)	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power-Down Time(4)	—	50	—	50	—	50	—	50	—	50	ns

2654 tbl 08

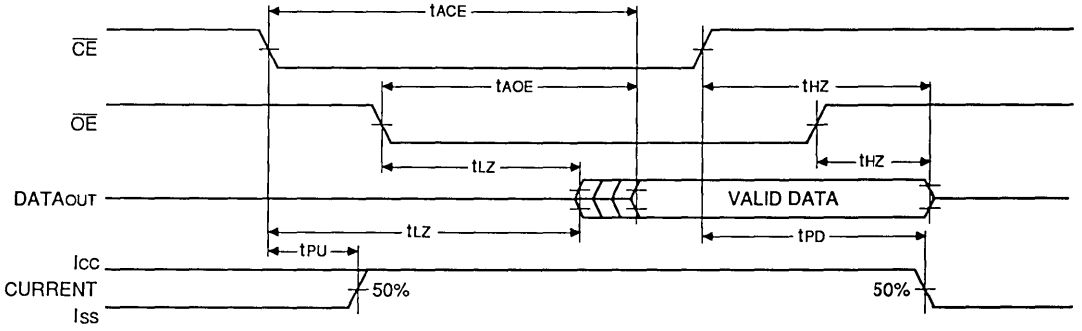
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. –55°C to +125°C range only.
4. This parameter guaranteed but not tested.
5. "x" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE(1,2,4)



2654 drw 08

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE(1,3)



2654 drw 09

NOTES:
1. R/W is high for Read Cycles.
2. Device is continuously enabled, CE = VIL.
3. Addresses valid prior to, or coincident with, CE transition low.
4. OE = VIL.

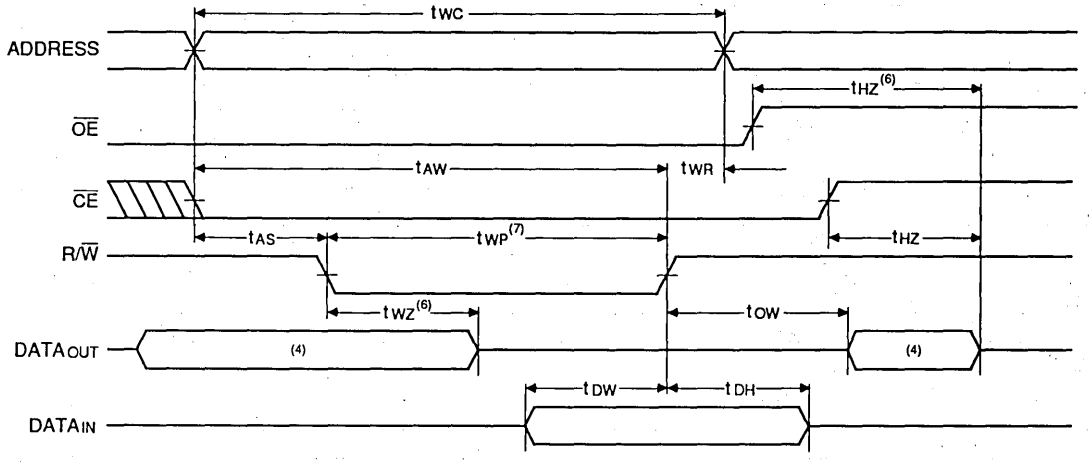
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[6]

Symbol	Parameter	70121 x 25[2] 70125 x 25[2]		70121 x 35 70125 x 35		70121 x 45 70125 x 45		70121 x 55 70125 x 55		70121 x 70[3] 70125 x 70[3]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle												
tWC	Write Cycle Time[5]	25	—	35	—	45	—	55	—	70	—	ns
tEW	Chip Enable to End of Write	20	—	30	—	35	—	40	—	50	—	ns
tAW	Address Valid to End of Write	20	—	30	—	35	—	40	—	50	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width[7]	20	—	30	—	35	—	40	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	12	—	20	—	20	—	20	—	30	—	ns
tHZ	Output High Z Time[1,4]	—	10	—	15	—	20	—	30	—	35	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z[1,4]	—	10	—	15	—	20	—	30	—	35	ns
tOW	Output Active from End of Write[1,4]	0	—	0	—	0	—	0	—	0	—	ns

NOTES:
2654 tbl 09

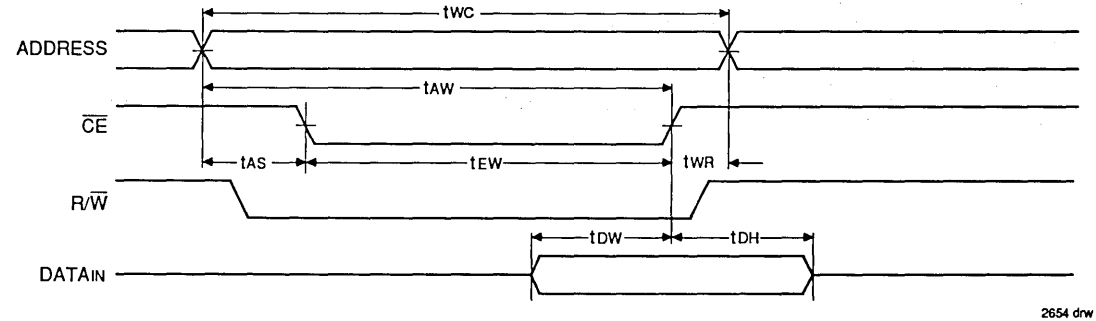
1. Transition is measured ±500mV from low or high voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. –55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, tWC = tBAA + tWP.
6. "x" in part numbers indicates power rating (S or L).
7. Specified for $\overline{OE}$ at high (Refer to "Timing Waveform of Write Cycle", Note 7).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,2,3,7)



2654 drw 10

TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1,2,3,5)



2654 drw 11

NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ± 500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

7

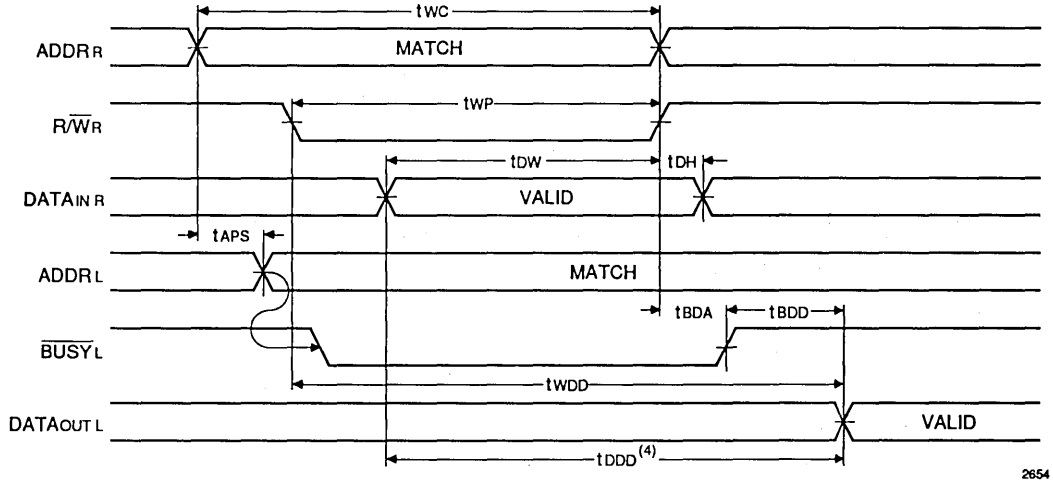
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[8]

Symbol	Parameter	70121 x 25[1] 70125 x 25[1] Min.	Max.	70121 x 35 70125 x 35 Min.	Max.	70121 x 45 70125 x 45 Min.	Max.	70121 x 55 70125 x 55 Min.	Max.	70121 x 70[2] 70125 x 70[2] Min.	Max.	Unit
Busy Timing (For Master IDT70121 Only)												
tBAA	$\overline{BUSY}$ Access Time to Address	—	25	—	35	—	35	—	45	—	45	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	20	—	30	—	35	—	40	—	40	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable	—	20	—	30	—	30	—	35	—	35	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable	—	20	—	25	—	25	—	30	—	30	ns
tWDD	Write Pulse to Data Delay[3]	—	50	—	60	—	70	—	80	—	95	ns
tDDD	Write Data Valid to Read Data Delay[3]	—	35	—	45	—	55	—	65	—	80	ns
tAPS	Arbitration Priority Set-up Time[4]	5	—	5	—	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[5]	—	Note 5	—	Note 5	—	Note 5	—	Note 5	—	Note 5	ns
Busy Timing (For Slave IDT70125 Only)												
tWB	Write to $\overline{BUSY}$ Input[6]	0	—	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[7]	15	—	20	—	20	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay[9]	—	50	—	60	—	70	—	80	—	95	ns
tDDD	Write Data Valid to Read Data Delay[9]	—	35	—	45	—	55	—	65	—	80	ns

2654 tbl 10

NOTES:
1. 0°C to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (For Master IDT70121 Only)."
4. To ensure that the earlier of the two ports wins.
5. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
6. To ensure that a write cycle is inhibited during contention.
7. To ensure that a write cycle is completed after contention.
8. "x" in part numbers indicates power rating (S or L).
9. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ Port-to-Port Delay (For SLAVE IDT70125 Only)."

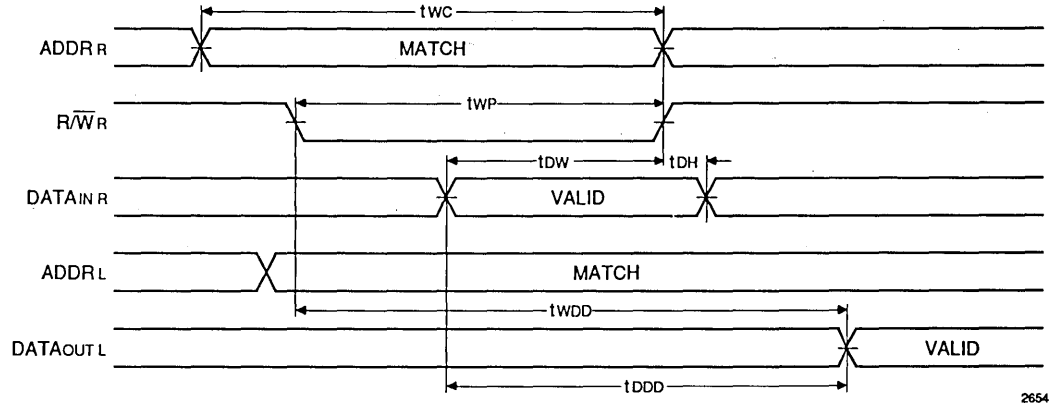
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$[1,2,3] (FOR MASTER IDT70121)



2654 drw 12

NOTES:
1. To ensure that the earlier of the two ports wins.
2. Write Cycle parameters should be adhered to, to ensure proper writing.
3. Device is continuously enabled for both ports.
4. $\overline{OE}$ at LOW for the reading port.

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY[1,2,3] (FOR SLAVE IDT70125 ONLY)

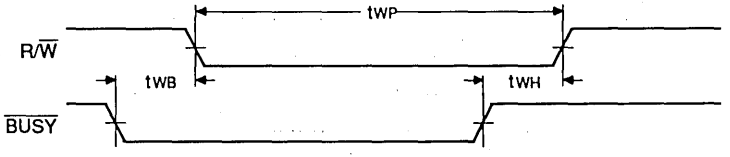


2654 drw 13

NOTES:
1. Assume $\overline{BUSY}$ input at HIGH for the writing port, and $\overline{OE}$ at LOW for the reading port.
2. Write Cycle parameters should be adhered to, to ensure proper writing.
3. Device is continuously enabled for both ports.

7

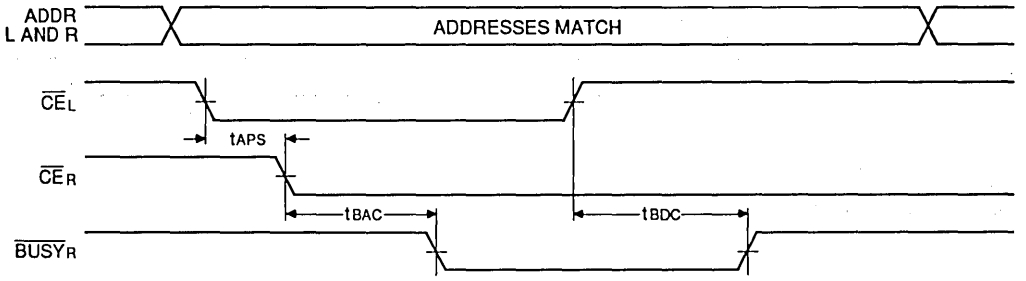
TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ (FOR SLAVE IDT70125 ONLY)



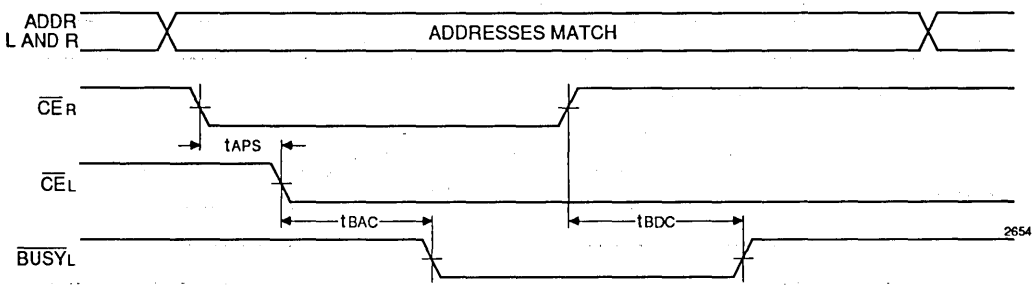
2654 drw 14

TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION (FOR MASTER IDT70121 ONLY)

$\overline{CE}_L$ VALID FIRST:



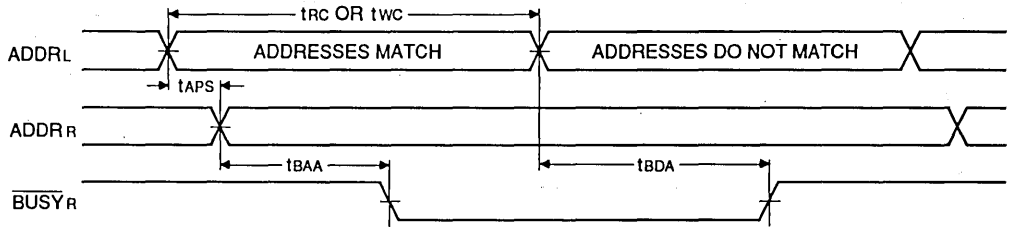
$\overline{CE}_R$ VALID FIRST:



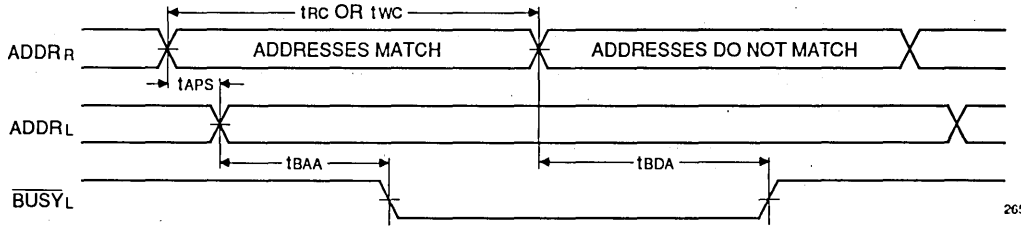
2654 drw 15

TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION (FOR MASTER IDT70121 ONLY)[1]

LEFT ADDRESS VALID FIRST:



RIGHT ADDRESS VALID FIRST:



2654 drw 16

NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[3]

Symbol	Parameter	70121 x 25[1] 70125 x 25[1] Min.	Max.	70121 x 35 70125 x 35 Min.	Max.	70121 x 45 70125 x 45 Min.	Max.	70121 x 55 70125 x 55 Min.	Max.	70121 x 70[2] 70125 x 70[2] Min.	Max.	Unit
Interrupt Timing												
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	25	—	35	—	40	—	45	—	50	ns
tINR	Interrupt Reset Time	—	25	—	35	—	40	—	45	—	50	ns

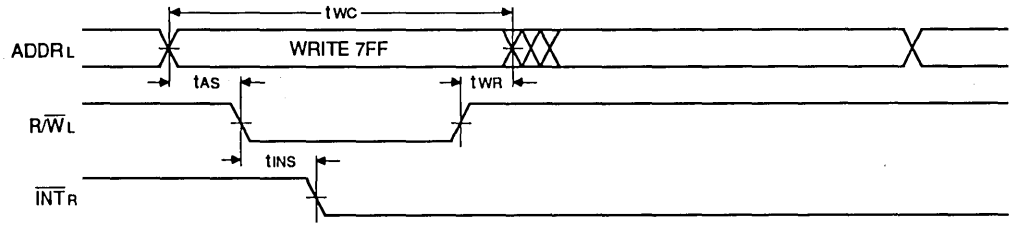
NOTES:
1. 0°C to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. "X" in part numbers indicates power rating (S or L).

2654 tbl 11

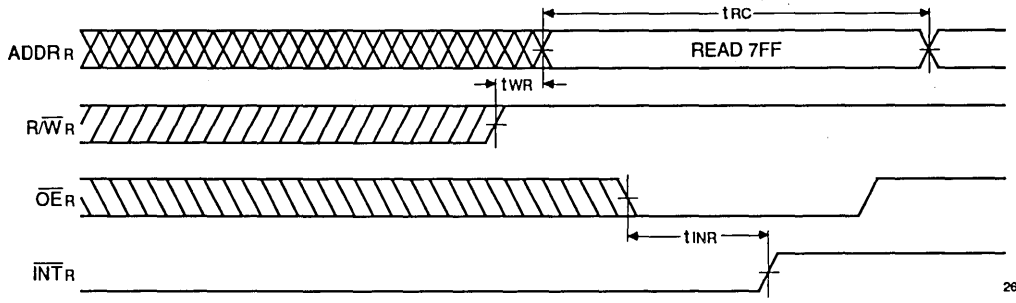
7

TIMING WAVEFORM OF INTERRUPT MODE[1,2]

LEFT SIDE SETS $\overline{INT}_R$:



RIGHT SIDE CLEARS $\overline{INT}_R$:

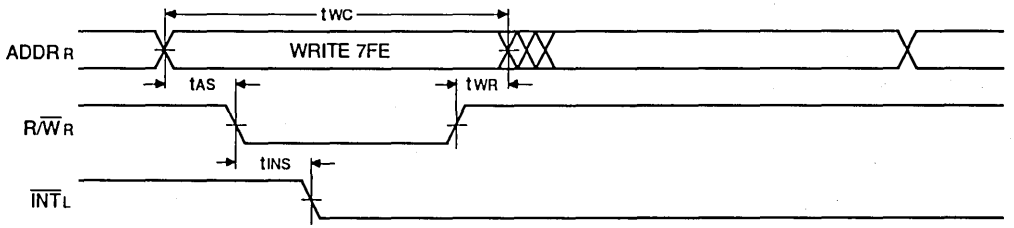


2654 drw 17

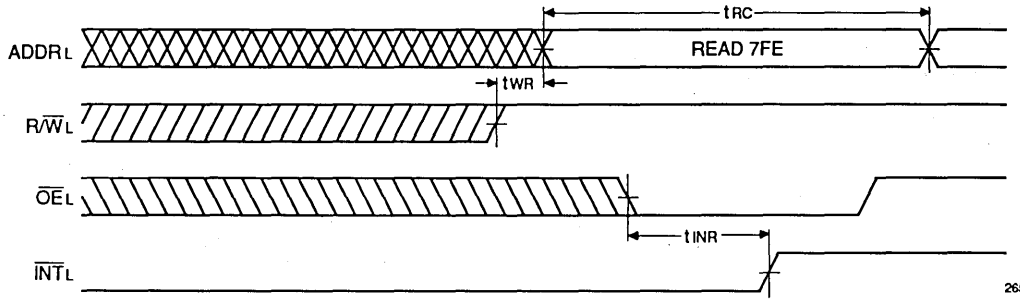
NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$.
2. $\overline{INT}_L$ and $\overline{INT}_R$ are reset (high) during power-up.

TIMING WAVEFORM OF INTERRUPT MODE[1,2]

RIGHT SIDE SETS $\overline{INT}_L$:



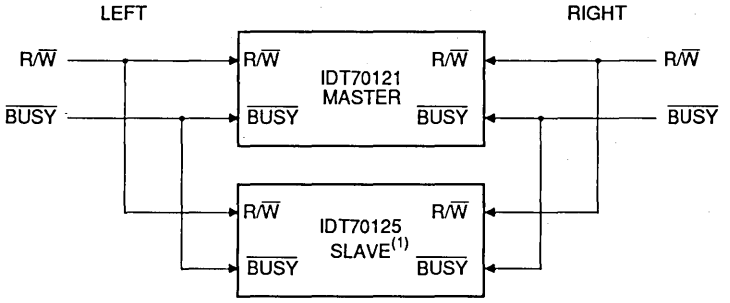
LEFT SIDE CLEARS $\overline{INT}_L$:



2654 drw 18

NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$.
2. $\overline{INT}_L$ and $\overline{INT}_R$ are reset to V_{OH} during power-up.

18-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



2654 drw 19

NOTE:
1. No arbitration in IDT70125 (SLAVE). $\overline{BUSY}_{IN}$ inhibits write in IDT70125 (SLAVE).

7

FUNCTIONAL DESCRIPTION

The IDT70121/IDT70125 provide two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power-down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power-down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table I.

The interrupt flag ($\overline{INT}$) permits communication between ports or systems. If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is set when the right port writes to memory location 7FE (HEX). The left port clears the interrupt by reading address location 7FE. Likewise, the right port interrupt flag ($\overline{INT}_R$) is set when the left port writes to memory location 7FF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 7FF. The message (9 bits) at 7FE or 7FF is user-defined. If the interrupt function is not used, address locations 7FE and 7FF are not used as mail boxes but as part of the random access memory. Refer to Table II for the interrupt operation.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table III). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION

Expanding the data bus width to eighteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another activates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid this "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

TRUTH TABLES

TABLE I. NON-CONTENTION READ/WRITE CONTROL[4]

Left or Right Port[1]				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-8}	Function
X	H	X	Z	Port Disabled and in Power-Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power-Down Mode, I_{SB1} or I_{SB3}
L	L	X	DATAIN	Data on Port Written Into Memory[2]
H	L	L	DATAOUT	Data in Memory Output on Port[3]
H	L	H	Z	High Impedance Outputs

NOTES: 2654 tbl 12
1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$.
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE: 2654 tbl 13
1. This parameter is determined by device characterization but is not production tested.

TABLE II. INTERRUPT FLAG[1,4]

Left Port					Right Port					
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{0L} - A_{10L}$	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{0L} - A_{10R}$	$\overline{INT}_R$	Function
L	L	X	7FF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	7FF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	7FE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	7FE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

NOTES: 2654 tbl 14
1. Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then NC.
3. If $\overline{BUSY}_R$ = L, then NC.
4. H = HIGH, L = LOW, X = DON'T CARE, NC = NO CHANGE

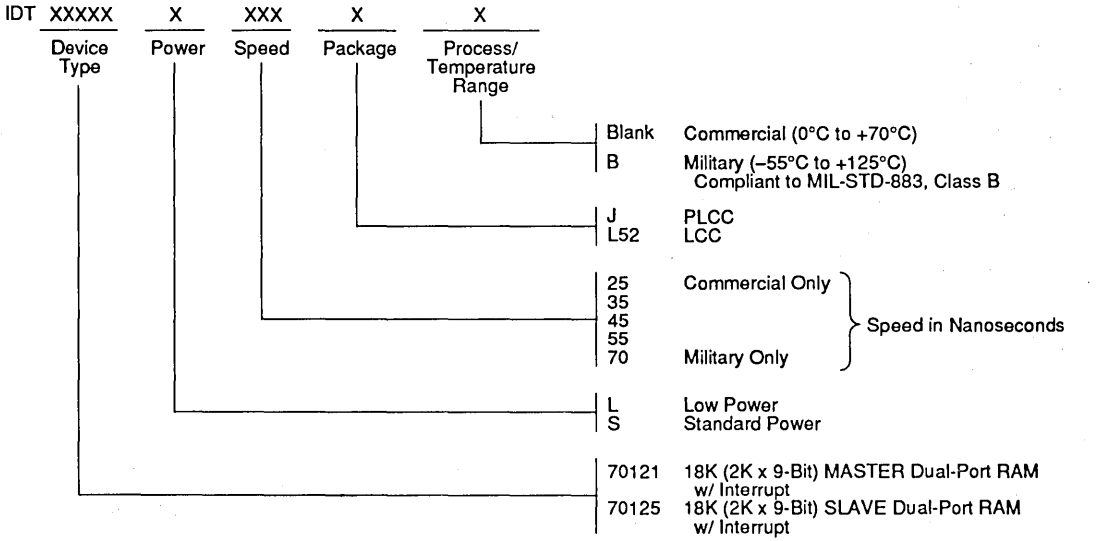
TABLE III. ARBITRATION[2]

Left Port		Right Port		Flags[1]		
$\overline{CE}_L$	$A_{0L} - A_{10L}$	$\overline{CE}_R$	$A_{0R} - A_{10R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	Function
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R} - A_{10R}$	L	$\neq A_{0L} - A_{10L}$	H	H	No Contention
Address Arbitration With $\overline{CE}$ Low Before Address Match						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ Arbitration With Address Match Before $\overline{CE}$						
LL5R	$= A_{0R} - A_{10R}$	LL5R	$= A_{0L} - A_{10L}$	H	L	L-Port Wins
RL5L	$= A_{0R} - A_{10R}$	RL5L	$= A_{0L} - A_{10L}$	L	H	R-Port Wins
LW5R	$= A_{0R} - A_{10R}$	LW5R	$= A_{0L} - A_{10L}$	H	L	Arbitration Resolved
LW5R	$= A_{0R} - A_{10R}$	LW5R	$= A_{0L} - A_{10L}$	L	H	Arbitration Resolved

NOTES: 2654 tbl 15
1. $\overline{INT}$ Flags Don't Care.
2. X = DON'T CARE, L = LOW, H = HIGH
   LV5R = Left Address Valid ≥ 5ns before right address.
   RV5L = Right Address Valid ≥ 5ns before left address.
   Same = Left and Right Addresses match within 5ns of each other.
   LL5R = Left $\overline{CE}$ = LOW ≥ 5ns before Right $\overline{CE}$.
   RL5L = Right $\overline{CE}$ = LOW ≥ 5ns before Left $\overline{CE}$.
   LW5R = Left and right $\overline{CE}$ = LOW within 5ns of each other.

7

ORDERING INFORMATION



2654 drw 20

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAMS 32K (2K x 16-BIT)

IDT7133S/L
IDT7143S/L

FEATURES:

- High-speed access
  - — Military: 55/70/90ns (max.)
  - — Commercial: 45/55/70/90ns (max.)
- Low-power operation
  - — IDT7133/43S
    Active: 375mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7133/43L
    Active: 375mW (typ.)
    Standby: 1mW (typ.)
- Versatile control for write: separate write control for lower and upper byte of each port
- MASTER IDT7133 easily expands data bus width to 32 bits or more using SLAVE IDT7143
- On-chip port arbitration logic (IDT7133 only)
- $\overline{BUSY}$ output flag on IDT7133; $\overline{BUSY}$ input on IDT7143
- Fully asynchronous operation from either port
- Battery backup operation–2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in 68-pin ceramic or plastic PGA, LCC, PLCC, and Flatpack
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7133/7143 are high-speed 2K x 16 dual-port static RAMs. The IDT7133 is designed to be used as a stand-alone 16-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7143 "SLAVE" dual-port in 32-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 32-bit-or-wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

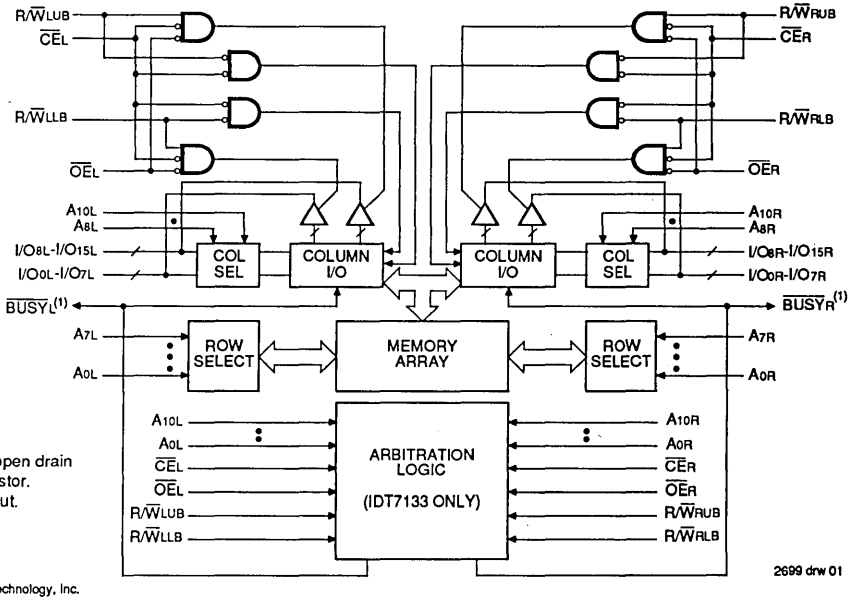
Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 375mW of power at maximum access times as fast as 45ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 1mW for a 2V battery.

The IDT7133/7143 devices have identical pinouts. Each is packed on a 68-pin ceramic or plastic PGA, 68-pin LCC, 68-pin flatpack, and 68-pin PLCC.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

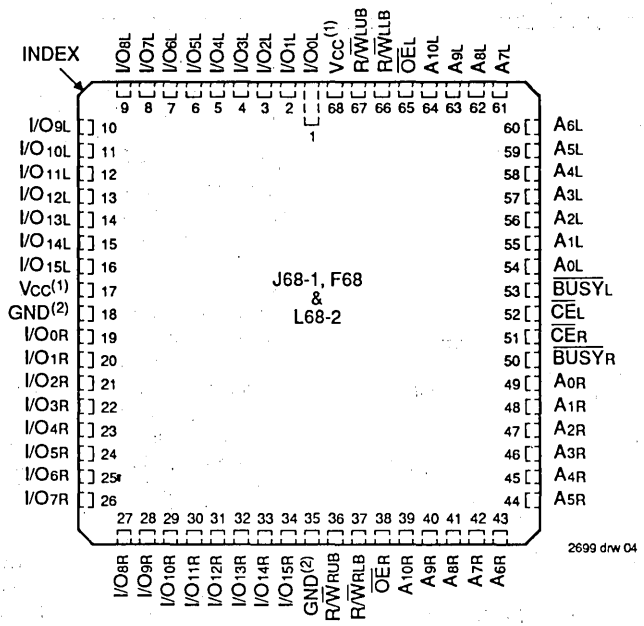


2699 drw 01

NOTES:
1. IDT7133 (MASTER): BUSY is open drain output and requires pull-up resistor. IDT7143 (SLAVE): BUSY is input.
2. LB = LOWER BYTE
3. UB = UPPER BYTE

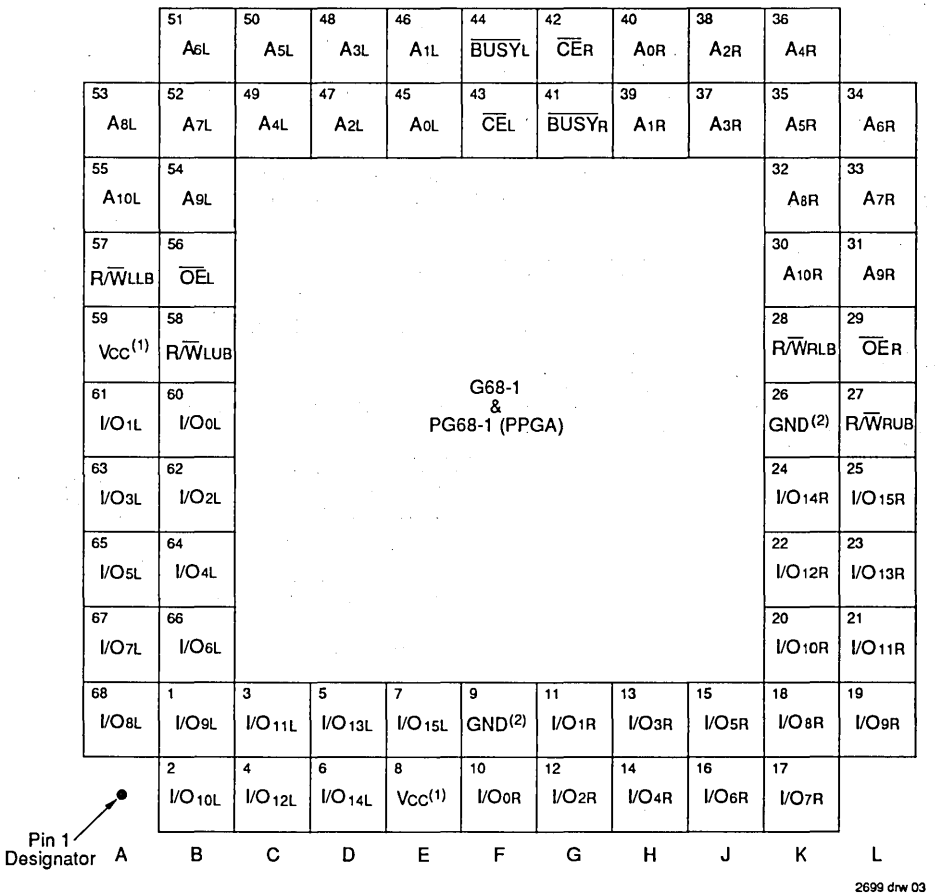
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



LCC/PLCC/FLATPACK
TOP VIEW

PIN CONFIGURATIONS (Continued)



2699 drw 03

PGA TOP VIEW (Ceramic or Plastic)

NOTES:
1. Both Vcc pins must be connected to the supply to assure reliable operation.
2. Both GND pins must be connected to the supply to assure reliable operation.
3. UB = Upper Byte, LB = Lower Byte.

7

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	2.0	2.0	W
IOUT	DC Output Current	50	50	mA

NOTE: 2699 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Input/Output Capacitance	VI/O = 0V	11	pF

NOTE: 2699 tbl 02

1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2699 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE: 2699 tbl 04

1. VIL (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (Either port, V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7133S IDT7143S		IDT7133L IDT7143L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O_0-I/O_{15})	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$)	I_{OL} = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2699 tbl 05

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[3] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		IDT7133x45[1] IDT7143x45[1]		IDT7133x55 IDT7143x55		IDT7133x70 IDT7143x70		IDT7133x90 IDT7143x90		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	MIL.	S	—	—	75	280	75	260	75	260	mA
				L	—	—	75	260	75	240	75	240	
			COM'L	S	—	260	75	240	75	240	75	235	
				L	—	240	75	220	75	220	75	215	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE_L}$ and $\overline{CE_R}$ ≥ V_{IH} f = f_{MAX}[4]	MIL.	S	—	—	25	80	25	75	25	75	mA
				L	—	—	25	70	25	65	25	65	
			COM'L	S	—	75	25	70	25	70	25	65	
				L	—	65	25	60	25	60	25	55	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE_L}$ or $\overline{CE_R}$ ≥ V_{IH} f = f_{MAX}[4] Active Port Outputs Open	MIL.	S	—	—	50	180	50	170	50	170	mA
				L	—	—	50	160	50	150	50	150	
			COM'L	S	—	160	50	150	50	150	50	145	
				L	—	140	50	130	50	130	50	125	
I_{SB3}	Full Standby Current (Both Ports — CMOS Level Inputs)	Both Ports $\overline{CE_L}$ & $\overline{CE_R}$ ≥ V_{CC} - 0.2V	MIL.	S	—	—	30	30	1	30	1	30	mA
				L	—	—	10	10	0.2	10	0.2	10	
		V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[5]	COM'L	S	—	15	1	15	1	15	1	15	
				L	—	4	0.2	4	0.2	4	0.2	4	
I_{SB4}	Full Standby Current (OnePort — All CMOS Level Inputs f = 0[5])	One Port $\overline{CE_L}$ or $\overline{CE_R}$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or	MIL.	S	—	—	45	170	45	160	45	155	mA
				L	—	—	40	150	40	140	40	135	
		V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	COM'L	S	—	150	45	140	45	140	45	135	
				L	—	130	40	120	40	120	40	115	

NOTES:

2699 tbl 06

1. 0°C to +70°C temperature range only.
2. V_{CC} = 5V, T_A = +25°C.
3. "x" in part number indicates power rating (S or L).
4. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of $1/t_{RC}$, and using "AC Test Conditions" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.

7

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES(1)

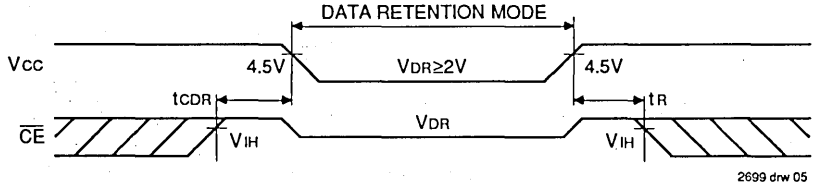
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		IDT7133/IDT7143 Min.	IDT7133/IDT7143 Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V		2.0	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$	MIL.	—	4000	µA
		$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	COM'L.	—	1500	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	ns
I_{LI}(3)	Input Leakage Current			—	2	µA

2699 tbl 07

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



2699 drw 05

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 & 3

2699 tbl 08

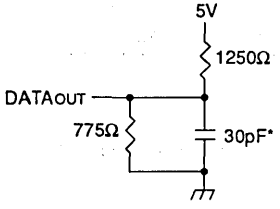


Figure 1. Output Load

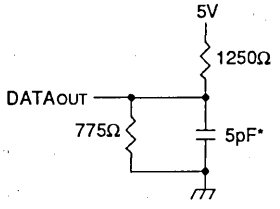


Figure 2. Output Load (for tLZ, tHZ, twz, tow)

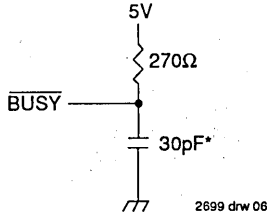


Figure 3. $\overline{BUSY}$ Output Load (IDT7133 only)

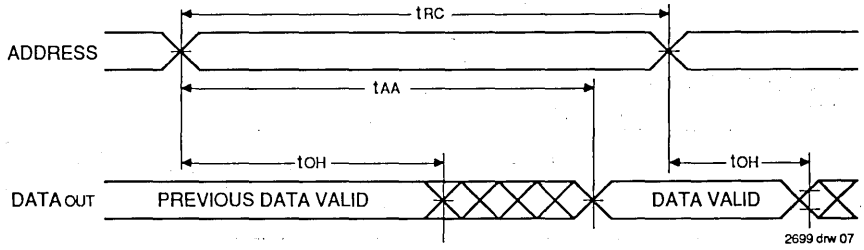
*Including scope and jig

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

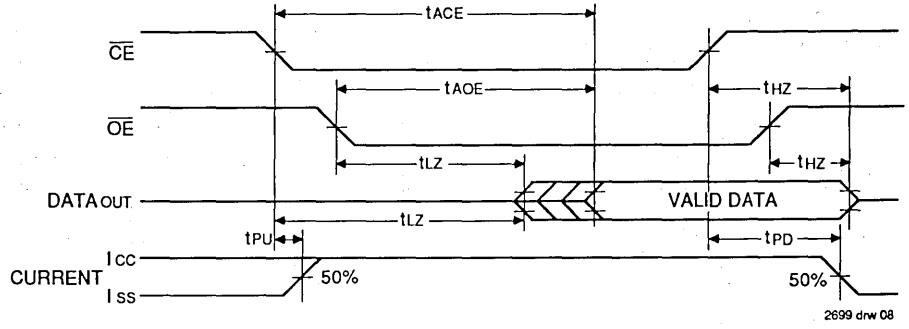
Symbol	Parameter	IDT7133S/L45[2] IDT7143S/L45[2] Min.	Max.	IDT7133S/L55 IDT7143S/L55 Min.	Max.	IDT7133S/L70 IDT7143S/L70 Min.	Max.	IDT7133S/L90 IDT7143S/L90 Min.	Max.	Unit
READ CYCLE										
tRC	Read Cycle Time	45	—	55	—	70	—	90	—	ns
tAA	Address Access Time	—	45	—	55	—	70	—	90	ns
tACE	Chip Enable Access Time	—	45	—	55	—	70	—	90	ns
tAOE	Output Enable Access Time	—	30	—	35	—	40	—	40	ns
tOH	Output Hold from Address Change	0	—	0	—	0	—	10	—	ns
tLZ	Output Low Z Time[1, 3]	0	—	5	—	5	—	5	—	ns
tHZ	Output High Z Time[1, 3]	—	20	—	20	—	25	—	25	ns
tPU	Chip Enable to Power Up Time[3]	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[3]	—	50	—	50	—	50	—	50	ns

NOTES: 2699 tbl 09
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. This parameter is guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1, 2, 4]



TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE[1, 3]



NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = VIL.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = VIL.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Symbol	Parameter	IDT7133S/L45[2] IDT7143S/L45[2]		IDT7133S/L55 IDT7143S/L55		IDT7133S/L70 IDT7143S/L70		IDT7133S/L90 IDT7143S/L90		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
tWC	Write Cycle Time[4]	45	—	55	—	70	—	90	—	ns
tEW	Chip Enable to End of Write	30	—	40	—	50	—	85	—	ns
tAW	Address Valid to End of Write	30	—	40	—	50	—	85	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width[6]	30	—	40	—	50	—	55	—	ns
tWR	Write Recovery Time	5	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	15	—	20	—	25	—	30	—	ns
tHZ	Output High Z Time[1, 3]	—	20	—	20	—	25	—	25	ns
tDH	Data Hold Time[5]	5	—	5	—	5	—	5	—	ns
tWZ	Write Enable to Output in High Z[1, 3]	—	20	—	20	—	25	—	25	ns
tOW	Output Active from End of Write[1, 3, 5]	5	—	5	—	5	—	5	—	ns

2699 tbl 10

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. This parameter is guaranteed but not tested.
4. For MASTER/SLAVE combination, tWC = tBAA + tWR + tWP.
5. The specification for tDH must be met by the device supplying write data to the RAM under all operation conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
6. Specified for $\overline{OE}$ at high (refer to "Timing Waveform of Write Cycle", Note 7).

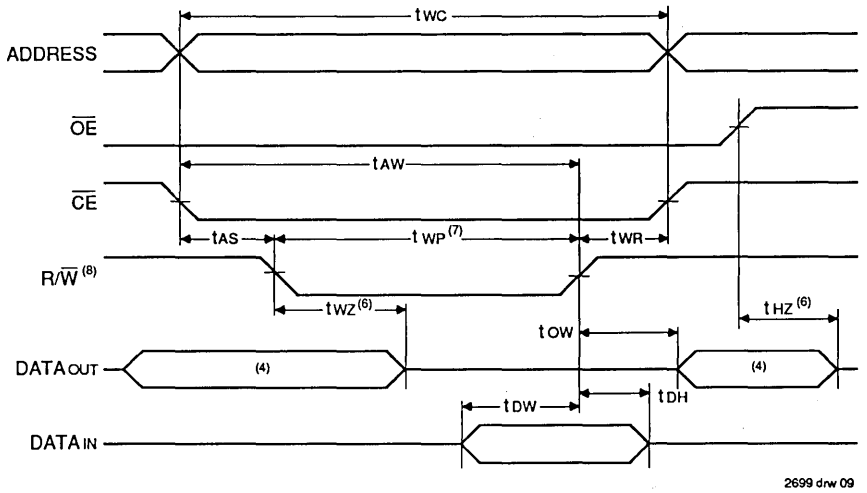
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Symbol	Parameter	IDT7133S/L45[1] IDT7143S/L45[1]		IDT7133S/L55 IDT7143S/L55		IDT7133S/L70 IDT7143S/L70		IDT7133S/L90 IDT7143S/L90		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
BUSY TIMING (FOR MASTER IDT7133)										
tBAA	$\overline{BUSY}$ Access Time to Address	—	45	—	50	—	55	—	55	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	40	—	40	—	45	—	45	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable	—	30	—	35	—	35	—	45	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable	—	25	—	30	—	30	—	45	ns
tWDD	Write Pulse to Data Delay[2]	—	80	—	80	—	90	—	100	ns
tDDD	Write Data Valid to Read Data Delay[2]	—	55	—	55	—	70	—	90	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	Note 4	—	Note 4	—	Note 4	—	Note 4	ns
tAPS	Arbitration Priority Set Up Time[4]	5	—	5	—	5	—	10	—	ns
BUSY INPUT TIMING (For SLAVE IDT7143)										
tWB	Write to $\overline{BUSY}$[5]	0	—	—	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[6]	30	—	30	—	30	—	30	—	ns
tWDD	Write Pulse to Data Delay[7]	—	80	—	80	—	90	—	100	ns
tDDD	Write Data Valid to Read Data Delay[7]	—	55	—	55	—	70	—	90	ns

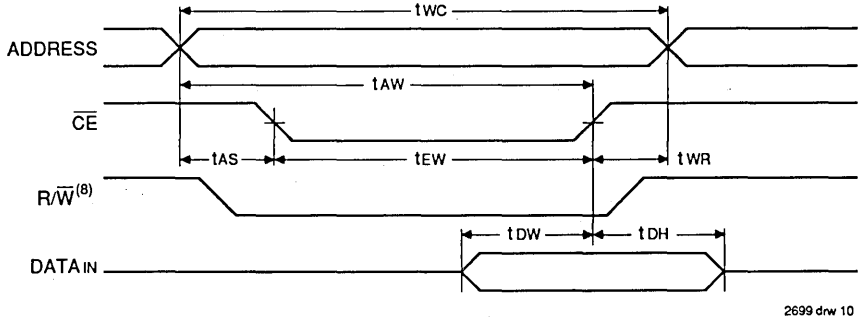
2699 tbl 11

NOTES:
1. 0°C to +70°C temperature range only.
2. Port-to-port delay through RAM cells from writing port to reading port, refer to "TIMING WAVEFORM OF READ WITH BUSY (For Master IDT7133)"
3. tBDD is calculated parameter and is greater of 0, tWDD - tWP (actual) or tDDD - tDW (actual).
4. To ensure that the earlier of the two ports wins.
5. To ensure that the write cycle is inhibited during contention.
6. To ensure that a write cycle is completed after contention.
7. Port-to-port delay through RAM cells from writing port to reading port, refer to "TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY (For Slave IDT7143)"

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING)(1, 2, 3, 7)



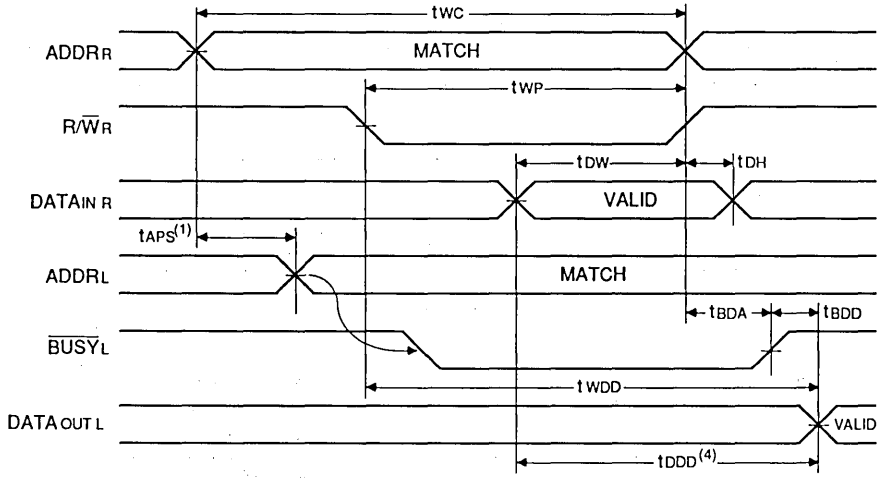
WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
8. R/$\overline{W}$ for either upper or lower byte.

7

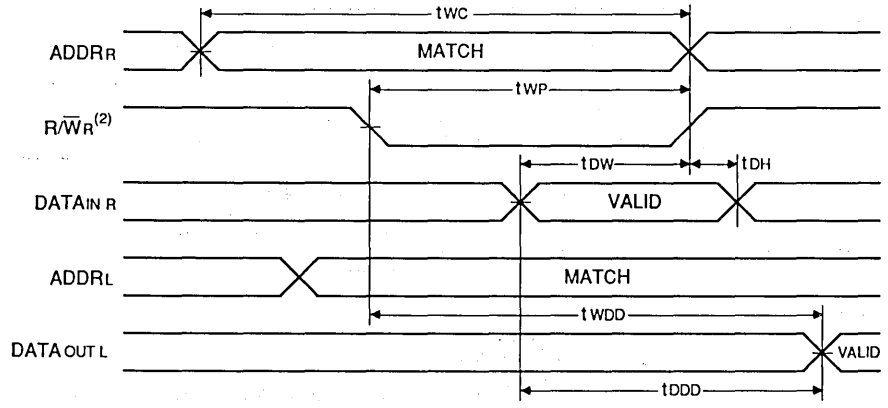
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$[1, 2, 3] (For MASTER IDT7133)



2699 drw 11

NOTES:
1. To ensure that the earlier of the two ports wins.
2. Write cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.
4. $\overline{OE}$ at LO for the reading port.

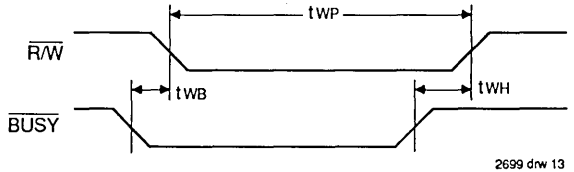
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY[1, 2, 3] (For SLAVE IDT7143)



2699 drw 12

NOTES:
1. Assume $\overline{BUSY}$ input at HI for the writing port, and $\overline{OE}$ at LO for the reading port.
2. Write cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.

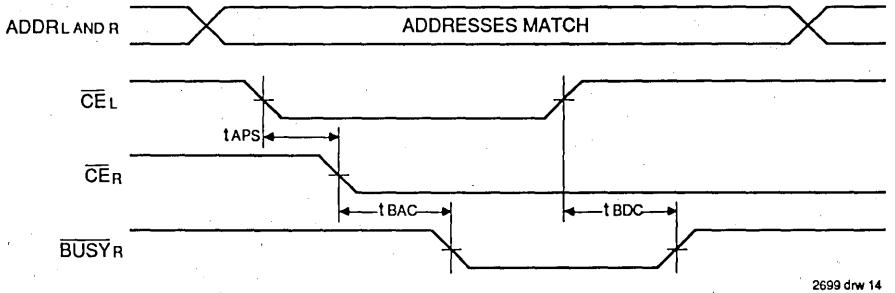
TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ INPUT (For SLAVE IDT7143)



2699 drw 13

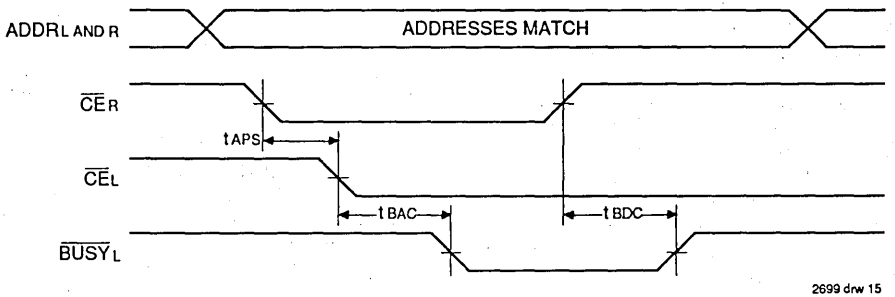
TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION

$\overline{CE}_L$ VALID FIRST:



2699 drw 14

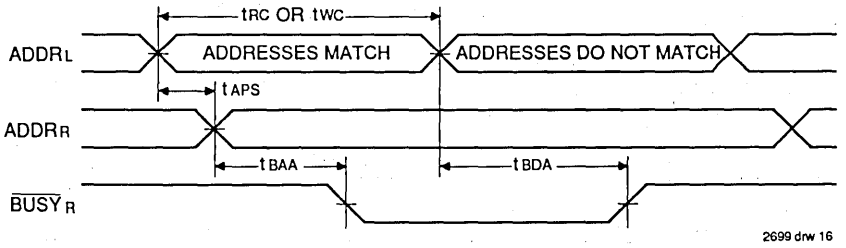
$\overline{CE}_R$ VALID FIRST:



2699 drw 15

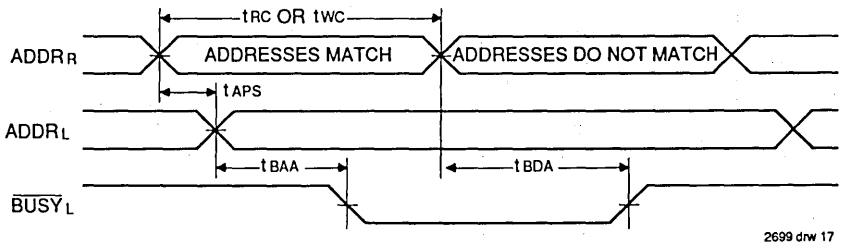
TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION(1)

LEFT ADDRESS VALID FIRST:



2699 drw 16

RIGHT ADDRESS VALID FIRST:



2699 drw 17

NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$

FUNCTIONAL DESCRIPTION:

The IDT7133/43 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The devices have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is pemitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table 1.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION:

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table II). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION:

Expanding the data bus width to 32 bits or more in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another activates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will await indefinately for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

TABLE I – NON-CONTENTION READ/WRITE CONTROL[4]

LEFT OR RIGHT PORT[1]						
$R/\overline{W}_{LB}$	$R/\overline{W}_{UB}$	$\overline{CE}$	$\overline{OE}$	I/O_{0-7}	I/O_{8-15}	Function
X	X	H	X	Z	Z	Port Disabled and in Power Down Mode, I_{SB2}, I_{SB4}
X	X	H	X	Z	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	L	X	$DATA_{IN}$	$DATA_{IN}$	Data on Lower Byte and Upper Byte Written into Memory[2]
L	H	L	L	$DATA_{IN}$	$DATA_{OUT}$	Data on Lower Byte Written into Memory[2], Data in Memory Output on Upper Byte[3]
H	L	L	L	$DATA_{OUT}$	$DATA_{IN}$	Data in Memory Output on Lower Byte[3], Data on Upper Byte Written into Memory[2]
L	H	L	H	$DATA_{IN}$	Z	Data on Lower Byte Written into Memory[2]
H	L	L	H	Z	$DATA_{IN}$	Data on Upper Byte Written into Memory[2]
H	H	L	L	$DATA_{OUT}$	$DATA_{OUT}$	Data in Memory Output on Lower Byte and Upper Byte
H	H	L	H	Z	Z	High Impedance Outputs

NOTES: 2699 tbl 12

1. A_{0L} - $A_{10L} \neq A_{0R}$ - A_{10R}
2. If $\overline{BUSY}$ = LOW, data is not written.
3. If $\overline{BUSY}$ = LOW, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance, LB = Lower Byte, UB = Upper Bytle

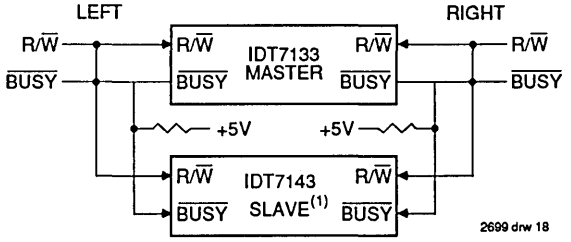
TABLE II — ARBITRATION

LEFT PORT		RIGHT PORT		FLAGS[1]		
$\overline{CE}_L$	$A_{0L} - A_{10L}$	$\overline{CE}_R$	$A_{0R} - A_{10R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	Function
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R} - A_{10R}$	L	$\neq A_{0L} - A_{10L}$	H	H	No Contention
ADDRESS ARBITRATION WITH $\overline{CE}$ LOW BEFORE ADDRESS MATCH						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CE}$						
LL5R	$= A_{0R} - A_{10R}$	LL5R	$= A_{0L} - A_{10L}$	H	L	L-Port Wins
RL5L	$= A_{0R} - A_{10R}$	RL5L	$= A_{0L} - A_{10L}$	L	H	R-Port Wins
LW5R	$= A_{0R} - A_{10R}$	LW5R	$= A_{0L} - A_{10L}$	H	L	Arbitration Resolved
LW5R	$= A_{0R} - A_{10R}$	LW5R	$= A_{0L} - A_{10L}$	L	H	Arbitration Resolved

2699 tbl 12

NOTES:
1. H = HIGH, L = LOW, X = Don't Care
   LV5R = Left Address Valid ≥ 5ns before right address
   RV5L = Right Address Valid ≥ 5ns before left address
   Same = Left and Right Address match within 5ns of each other
   LL5R = Left $\overline{CE}$ = LOW ≥ 5ns before Right $\overline{CE}$
   RL5L = Right $\overline{CE}$ = LOW ≥ 5ns before Left $\overline{CE}$
   LW5R = Left and Right $\overline{CE}$ = LOW within 5ns of each other

32-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



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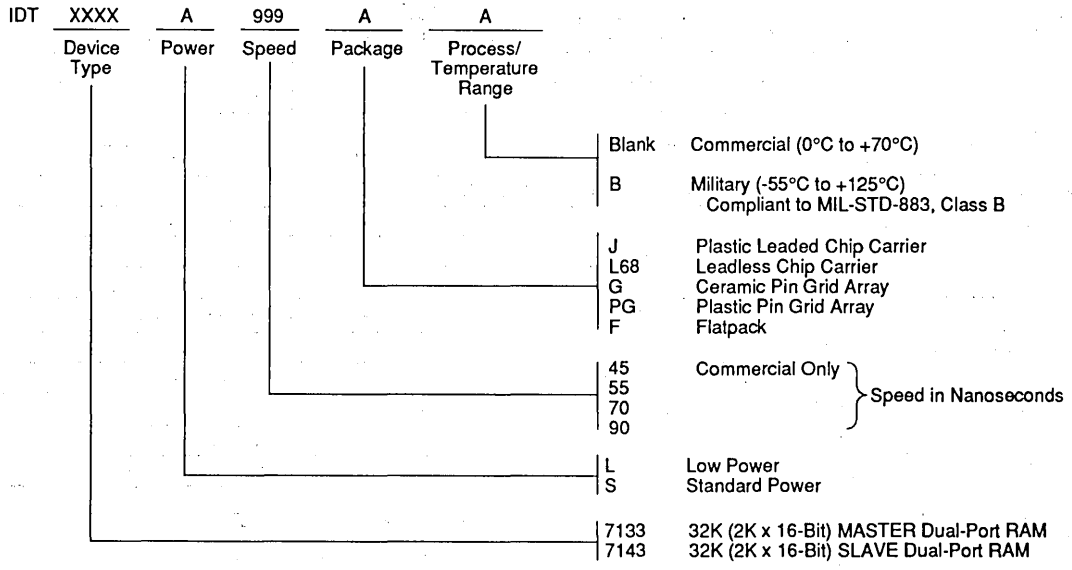
NOTES:
1. No arbitration in IDT7143 (SLAVE). $\overline{BUSY}$-IN inhibits write in IDT7143 (SLAVE).

7

ORDERING INFORMATION



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Integrated Device Technology, Inc.

CMOS DUAL-PORT RAMS 32K (2K x 16-BIT)

PRELIMINARY
IDT7133SA/LA
IDT7143SA/LA

FEATURES:

- High-speed access
  - — Military: 35/45/55/70ns (max.)
  - — Commercial: 25/35/45/55/70/ns (max.)
- Low-power operation
  - — IDT7133/43SA
    Active: 500 mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7133/43LA
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- Versatile control for write: separate write control for lower and upper byte of each port
- MASTER IDT7133 easily expands data bus width to 32 bits or more using SLAVE IDT7143
- On-chip port arbitration logic (IDT7133 only)
- $\overline{BUSY}$ output flag on IDT7133; $\overline{BUSY}$ input on IDT7143
- Fully asynchronous operation from either port
- Battery backup operation–2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in 68-pin ceramic or plastic PGA, Flatpack, LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7133/7143 are high-speed 2K x 16 dual-port static RAMs. The IDT7133 is designed to be used as a stand-alone 16-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7143 "SLAVE" dual-port in 32-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 32-bit-or-wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

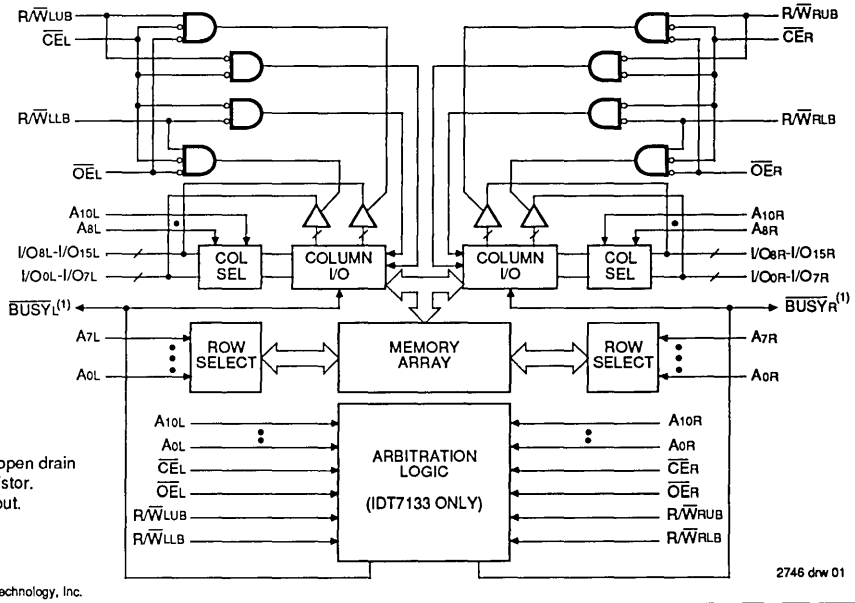
Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 500mW of power at maximum access times as fast as 25ns. Low-power (LA) versions offer battery backup data retention capability, with each port typically consuming 1mW for a 2V battery.

The IDT7133/7143 devices have identical pinouts. Each is packed on a 68-pin ceramic or plastic PGA, 68-pin LCC, 68-pin flatpack, and 68-pin PLCC.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. IDT7133 (MASTER): BUSY is open drain output and requires pull-up resistor. IDT7143 (SLAVE): BUSY is input.
2. LB = LOWER BYTE
3. UB = UPPER BYTE

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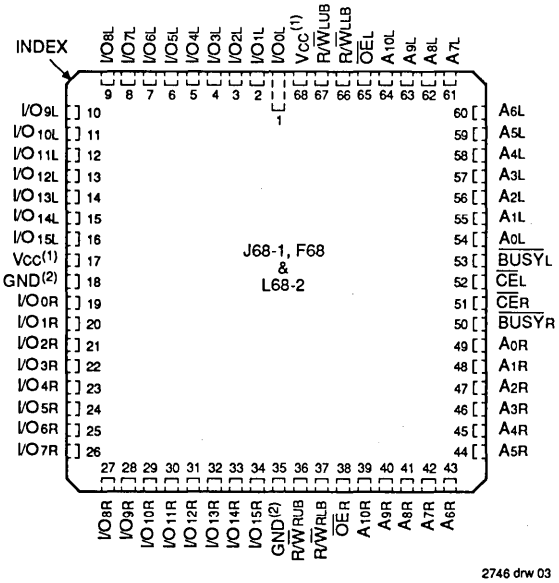
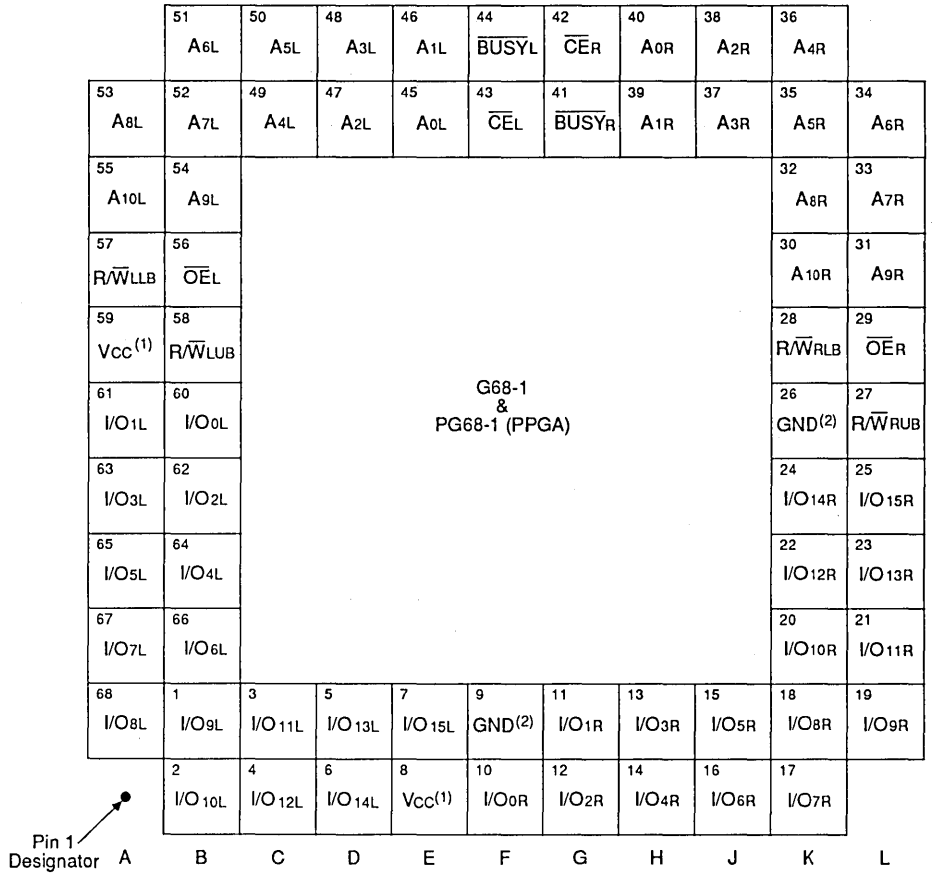
PIN CONFIGURATIONS



2746 drw 03

LCC/PLCC/FLATPACK
TOP VIEW

NOTES:
1. Both Vcc pins must be connected to the supply to assure reliable operation.
2. Both GND pins must be connected to the supply to assure reliable operation.
3. UB = Upper Byte, LB = Lower Byte



PGA (Ceramic or Plastic)
TOP VIEW

NOTES:
1. Both Vcc pins must be connected to the supply to assure reliable operation.
2. Both GND pins must be connected to the supply to assure reliable operation.
3. UB = Upper Byte, LB = Lower Byte

7

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	2.0	2.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2746 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Input/Output Capacitance	$V_{I/O}$ = 0V	11	pF

NOTE: 2746 tbl 02

1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2746 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2746 tbl 04

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (Either port, V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7133SA IDT7143SA		IDT7133LA IDT7143LA		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O_0-I/O_{15})	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$)	I_{OL} = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2746 tbl 05

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[3] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7133x25[1] 7143x25[1]		7133x35 7143x35		7133x45 7143x45		7133x55 7143x55		7133x70 7143x70		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \le V_{IL}$ Outputs Open f = f_{MAX}[4]	MIL.	S	—	—	75	290	75	280	75	280	75	260	mA
				L	—	—	75	270	75	260	75	260	75	240	
			COM'L.	S	100	280	80	260	75	260	75	240	75	240	
				L	100	260	80	240	75	240	75	220	75	220	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \ge V_{IH}$ f = f_{MAX}[4]	MIL.	S	—	—	25	85	25	80	25	80	25	75	mA
				L	—	—	25	75	25	70	25	70	25	65	
			COM'L.	S	25	80	25	75	25	75	25	70	25	70	
				L	25	70	25	65	25	65	25	60	25	60	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \ge V_{IH}$ f = f_{MAX}[4] Active Port Outputs Open	MIL.	S	—	—	50	190	50	180	50	180	50	170	mA
				L	—	—	50	170	50	160	50	160	50	150	
			COM'L.	S	50	170	50	160	50	160	50	150	50	150	
				L	50	150	50	140	50	140	50	130	50	130	
I_{SB3}	Full Standby Current (Both Ports — CMOS Level Inputs)	Both Ports $\overline{CE}_L$ & $\overline{CE}_R \ge V_{CC}$ - 0.2V	MIL.	S	—	—	1	30	1	30	1	30	1	30	mA
				L	—	—	0.2	10	0.2	10	0.2	10	0.2	10	
		$V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le$ 0.2V, f = 0[5]	COM'L.	S	1	15	1	15	1	15	1	15	1	15	
				L	0.2	4	0.2	4	0.2	4	0.2	4	0.2	4	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ - 0.2V $V_{IN} \ge V_{CC}$ - 0.2V or	MIL.	S	—	—	45	180	45	170	45	170	45	160	mA
				L	—	—	40	160	40	150	40	150	40	140	
		$V_{IN} \le$ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	COM'L.	S	45	160	45	150	45	140	45	140	45	140	
				L	40	140	40	130	40	120	40	120	40	120	

NOTES:

2746 tbl 06

1. 0°C to +70°C temperature range only.
2. V_{CC} = 5V, T_A = +25°C.
3. "x" in part number indicates power rating (SA or LA).
4. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES[1]

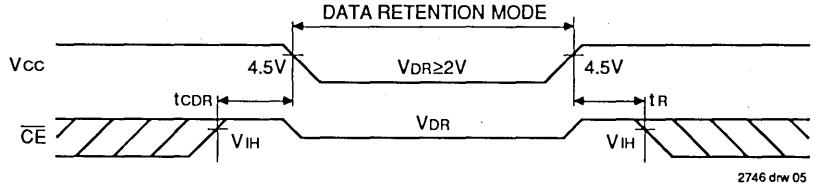
(LA Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		IDT7133LA/IDT7143LA Min.	IDT7133LA/IDT7143LA Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V		2.0	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$	MIL.	—	4000	µA
		$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	COM'L.	—	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	ns
I_{LI}[3]	Input Leakage Current			—	2	µA

2746 tbl 07

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW Vcc DATA RETENTION WAVEFORM



2746 drw 05

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 & 3

2746 tbl 08

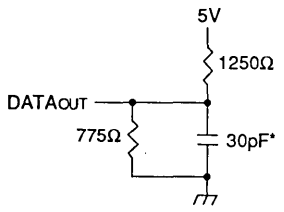


Figure 1. Output Load

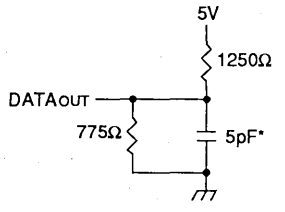


Figure 2. Output Load (for tLZ, tHZ, tWZ, tOW)

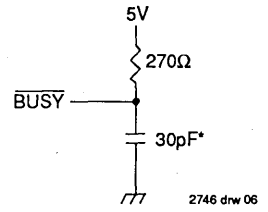


Figure 3. $\overline{BUSY}$ Output Load (IDT7133 only)

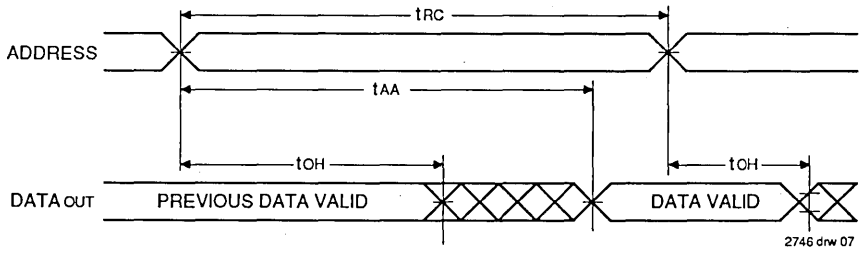
*Including scope and jig

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[4]

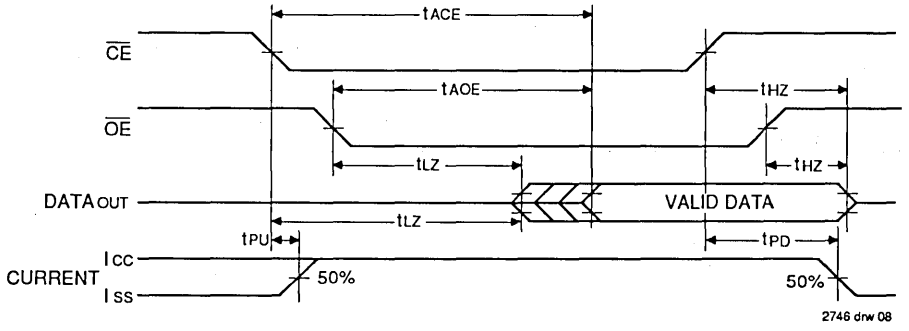
Symbol	Parameter	IDT7133x25[2] IDT7143x25[2] Min.	Max.	IDT7133x35 IDT7143x35 Min.	Max.	IDT7133x45 IDT7143x45 Min.	Max.	IDT7133x55 IDT7143x55 Min.	Max.	IDT7133x70 IDT7143x70 Min.	Max.	Unit
READ CYCLE												
tRC	Read Cycle Time	25	—	35	—	45	—	55	—	70	—	ns
tAA	Address Access Time	—	25	—	35	—	45	—	55	—	70	ns
tACE	Chip Enable Access Time	—	25	—	35	—	45	—	55	—	70	ns
tAOE	Output Enable Access Time	—	15	—	20	—	25	—	30	—	40	ns
tOH	Output Hold from Address Change	0	—	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time[1, 3]	3	—	3	—	5	—	5	—	5	—	ns
tHZ	Output High Z Time[1, 3]	—	15	—	20	—	20	—	25	—	30	ns
tPU	Chip Enable to Power Up Time[3]	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[3]	—	50	—	50	—	50	—	50	—	50	ns

NOTES: 2746 tbl 09
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. This parameter is guaranteed but not tested.
4. "x" in part number indicates power rating (SA or LA).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1, 2, 4]



TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE[1, 3]



NOTES:
1. R/W is high for Read Cycles.
2. Device is continuously enabled, CE = VIL.
3. Addresses valid prior to or coincident with CE transition low.
4. OE = VIL.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[7]

Symbol	Parameter	IDT7133x25[2] IDT7143x25[2] Min.	Max.	IDT7133x35 IDT7143x35 Min.	Max.	IDT7133x45 IDT7143x45 Min.	Max.	IDT7133x55 IDT7143x55 Min.	Max.	IDT7133x70 IDT7143x70 Min.	Max.	Unit
WRITE CYCLE												
tWC	Write Cycle Time[4]	25	—	35	—	45	—	55	—	70	—	ns
tEW	Chip Enable to End of Write	20	—	25	—	35	—	45	—	55	—	ns
tAW	Address Valid to End of Write	20	—	25	—	35	—	45	—	55	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width[6]	20	—	25	—	35	—	45	—	55	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	15	—	20	—	20	—	25	—	30	—	ns
tHZ	Output High Z Time[1, 3]	—	15	—	20	—	20	—	20	—	25	ns
tDH	Data Hold Time[5]	0	—	0	—	5	—	5	—	5	—	ns
tWZ	Write Enable to Output in High Z[1, 3]	—	15	—	20	—	20	—	20	—	25	ns
tOW	Output Active from End of Write[1, 3, 5]	3	—	3	—	3	—	3	—	3	—	ns

NOTES: 2746 tbl 10

1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. This parameter is guaranteed but not tested.
4. For MASTER/SLAVE combination, tWC = tBAA + tWR + tWP.
5. The specification for tDH must be met by the device supplying write data to the RAM under all operation conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
6. Specified for $\overline{OE}$ at high (refer to "Timing Waveform of Write Cycle", Note 7).
7. "x" in part number indicates power rating (SA or LA).

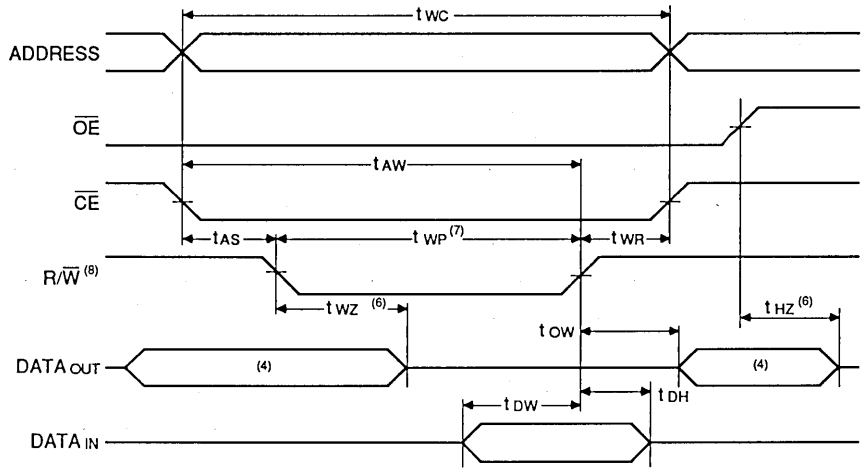
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[8]

Symbol	Parameter	IDT7133x25[1] IDT7143x25[1] Min.	Max.	IDT7133x35 IDT7143x35 Min.	Max.	IDT7133x45 IDT7143x45 Min.	Max.	IDT7133x55 IDT7143x55 Min.	Max.	IDT7133x70 IDT7143x70 Min.	Max.	Unit
BUSY TIMING (For MASTER IDT7133)												
tBAA	$\overline{BUSY}$ Access Time to Address	—	25	—	35	—	45	—	50	—	55	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	20	—	30	—	40	—	40	—	45	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable	—	20	—	25	—	30	—	35	—	35	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable	—	20	—	20	—	25	—	30	—	30	ns
tWDD	Write Pulse to Data Delay[2]	—	50	—	60	—	70	—	80	—	90	ns
tDDD	Write Data Valid to Read Data Delay[2]	—	35	—	45	—	55	—	65	—	80	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	Note 4	—	Note 4	—	Note 4	—	Note 4	—	Note 4	ns
tAPS	Arbitration Priority Set Up Time[4]	5	—	5	—	5	—	5	—	5	—	ns
BUSY INPUT TIMING (For SLAVE IDT7143)												
tWB	Write to $\overline{BUSY}$[5]	0	—	0	—	0	—	—	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[6]	20	—	25	—	30	—	30	—	30	—	ns
tWDD	Write Pulse to Data Delay[7]	—	50	—	60	—	70	—	80	—	90	ns
tDDD	Write Data Valid to Read Data Delay[7]	—	35	—	45	—	55	—	65	—	80	ns

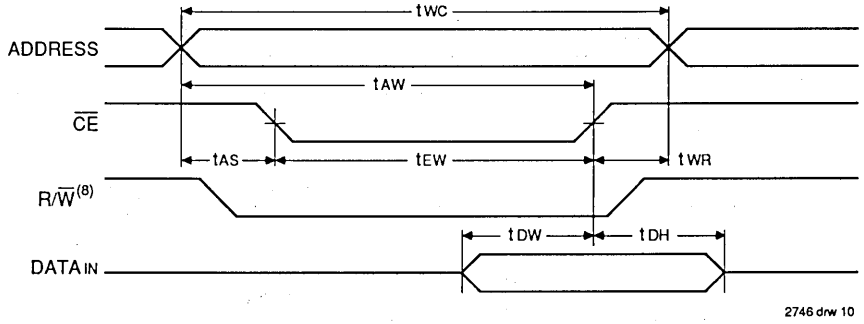
NOTES: 2746 tbl 11

1. 0°C to +70°C temperature range only.
2. Port-to-port delay through RAM cells from writing port to reading port, refer to "TIMING WAVEFORM OF READ WITH BUSY (For Master IDT7133)"
3. tBDD is calculated parameter and is greater of 0, tWDD - tWP (actual) or tDDD - tDW (actual).
4. To ensure that the earlier of the two ports wins.
5. To ensure that the write cycle is inhibited during contention.
6. To ensure that a write cycle is completed after contention.
7. Port-to-port delay through RAM cells from writing port to reading port, refer to "TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY (For Slave IDT7143)"
8. "x" in part number indicates power rating (SA or LA).

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING)(1, 2, 3, 7)

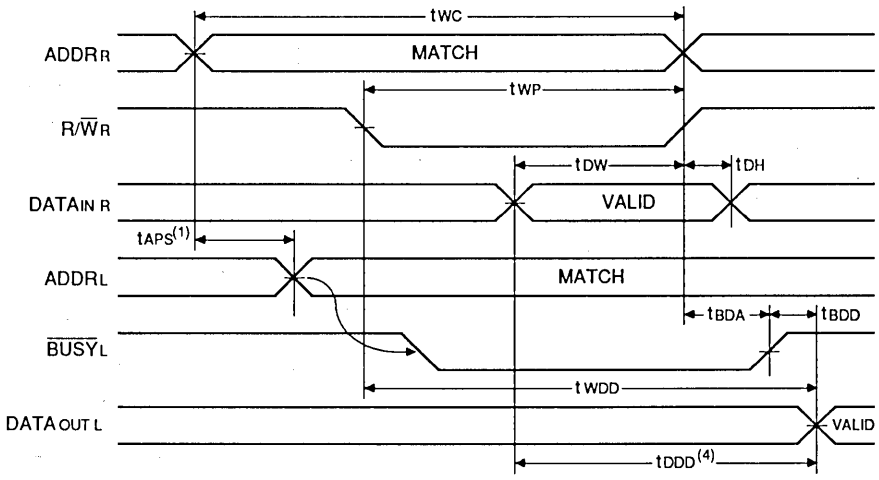


WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
8. R/$\overline{W}$ for either upper or lower byte.

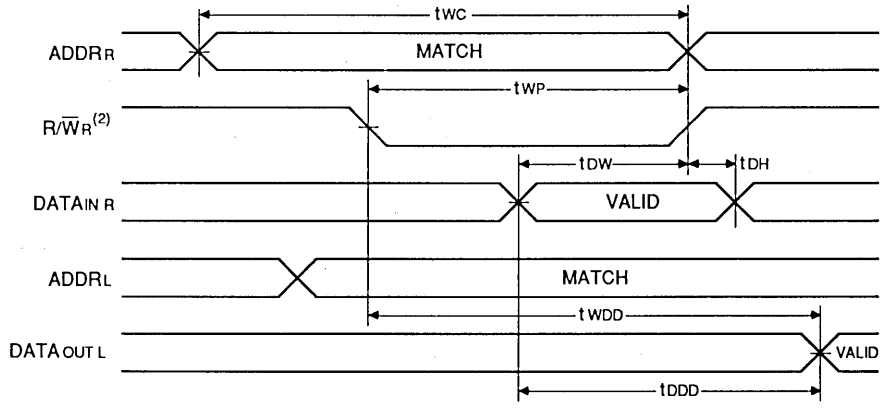
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$[1, 2, 3] (For MASTER IDT7133)



2746 drw 11

NOTES:
1. To ensure that the earlier of the two ports wins.
2. Write cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.
4. $\overline{OE}$ at LO for the reading port.

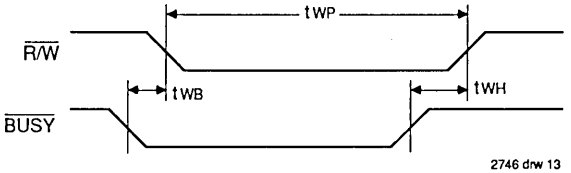
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY[1, 2, 3] (For SLAVE IDT7143)



2746 drw 12

NOTES:
1. Assume $\overline{BUSY}$ input at HI for the writing port, and $\overline{OE}$ at LO for the reading port.
2. Write cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.

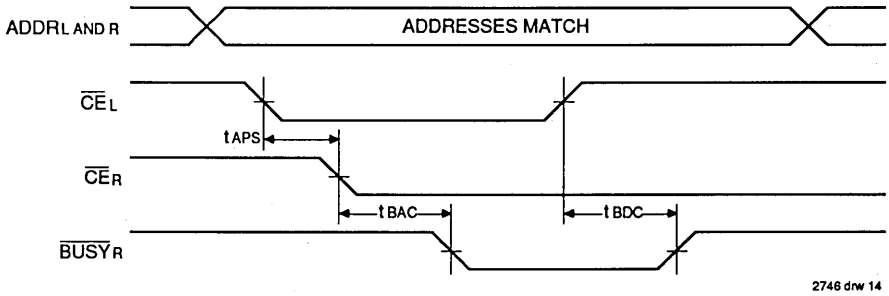
TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ INPUT (For SLAVE IDT7143)



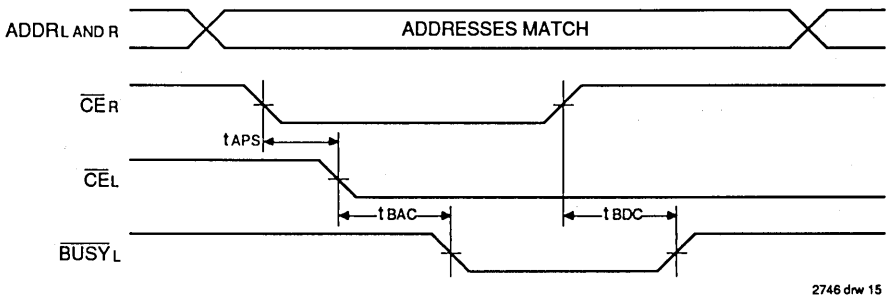
2746 drw 13

TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION

$\overline{CE}_L$ VALID FIRST:

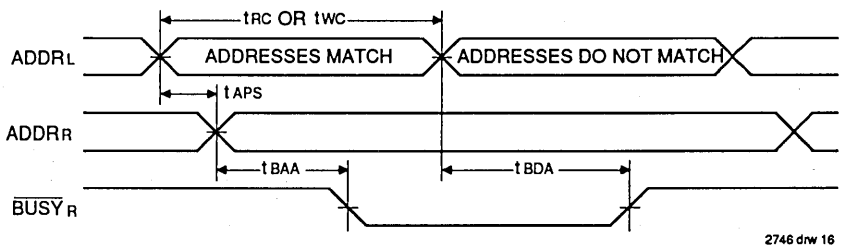


$\overline{CE}_R$ VALID FIRST:

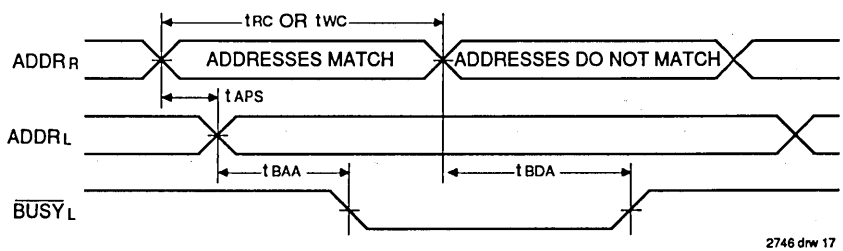


TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION(1)

LEFT ADDRESS VALID FIRST:



RIGHT ADDRESS VALID FIRST:



NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$

FUNCTIONAL DESCRIPTION:

The IDT7133/43 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The devices have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is pemitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table 1.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION:

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table II). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION:

Expanding the data bus width to 32 bits or more in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another activates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will await indefinately for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

TABLE I – NON-CONTENTION READ/WRITE CONTROL[4]

LEFT OR RIGHT PORT[1]						
$R/\overline{W}_{LB}$	$R/\overline{W}_{UB}$	$\overline{CE}$	$\overline{OE}$	I/O_{0-7}	I/O_{8-15}	Function
X	X	H	X	Z	Z	Port Disabled and in Power Down Mode, I_{SB2}, I_{SB4}
X	X	H	X	Z	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	L	X	$DATA_{IN}$	$DATA_{IN}$	Data on Lower Byte and Upper Byte Written into Memory[2]
L	H	L	L	$DATA_{IN}$	$DATA_{OUT}$	Data on Lower Byte Written into Memory[2], Data in Memory Output on Upper Byte[3]
H	L	L	L	$DATA_{OUT}$	$DATA_{IN}$	Data in Memory Output on Lower Byte[3], Data on Upper Byte Written into Memory[2]
L	H	L	H	$DATA_{IN}$	Z	Data on Lower Byte Written into Memory[2]
H	L	L	H	Z	$DATA_{IN}$	Data on Upper Byte Written into Memory[2]
H	H	L	L	$DATA_{OUT}$	$DATA_{OUT}$	Data in Memory Output on Lower Byte and Upper Byte
H	H	L	H	Z	Z	High Impedance Outputs

NOTES: 2746 tbl 12

1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$
2. If $\overline{BUSY}$ = LOW, data is not written.
3. If $\overline{BUSY}$ = LOW, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance, LB = Lower Byte, UB = Upper Bytle

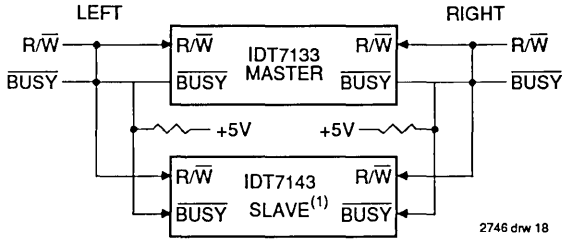
TABLE II — ARBITRATION[1]

LEFT PORT		RIGHT PORT		FLAGS		
$\overline{CE}_L$	$A_{0L} - A_{10L}$	$\overline{CE}_R$	$A_{0R} - A_{10R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	Function
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R} - A_{10R}$	L	$\neq A_{0L} - A_{10L}$	H	H	No Contention
ADDRESS ARBITRATION WITH $\overline{CE}$ LOW BEFORE ADDRESS MATCH						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CE}$						
LL5R	$= A_{0R} - A_{10R}$	LL5R	$= A_{0L} - A_{10L}$	H	L	L-Port Wins
RL5L	$= A_{0R} - A_{10R}$	RL5L	$= A_{0L} - A_{10L}$	L	H	R-Port Wins
LW5R	$= A_{0R} - A_{10R}$	LW5R	$= A_{0L} - A_{10L}$	H	L	Arbitration Resolved
LW5R	$= A_{0R} - A_{10R}$	LW5R	$= A_{0L} - A_{10L}$	L	H	Arbitration Resolved

NOTES:
1. H = HIGH, L = LOW, X = Don't Care
   LV5R = Left Address Valid ≥ 5ns before right address
   RV5L = Right Address Valid ≥ 5ns before left address
   Same = Left and Right Address match within 5ns of each other
   LL5R = Left $\overline{CE}$ = LOW ≥ 5ns before Right $\overline{CE}$
   RL5L = Right $\overline{CE}$ = LOW ≥ 5ns before Left $\overline{CE}$
   LW5R = Left and Right $\overline{CE}$ = LOW within 5ns of each other

2746 tbl 12

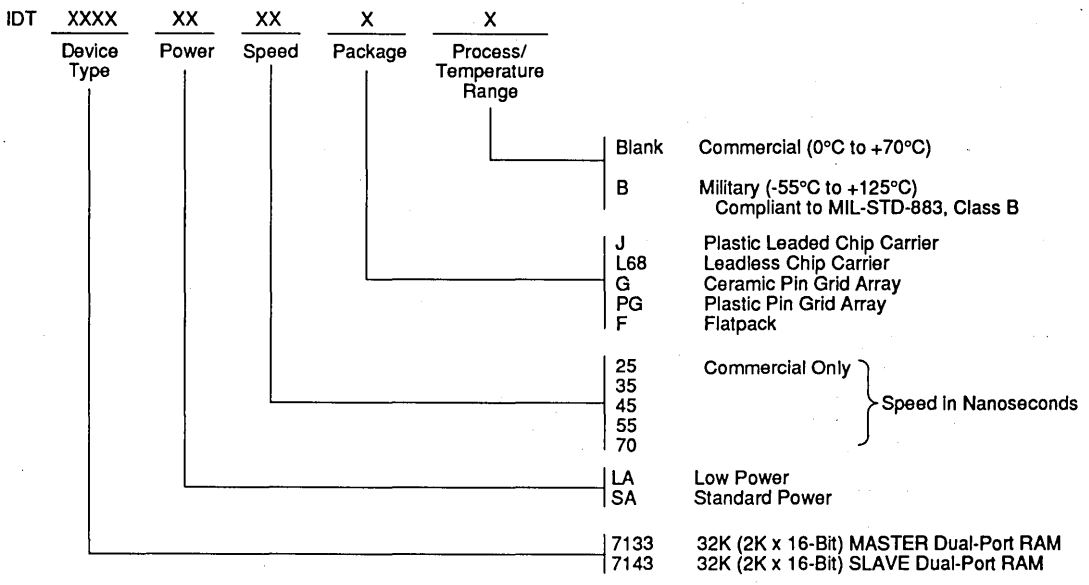
32-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



2746 drw 18

NOTES:
1. No arbitration in IDT7143 (SLAVE). $\overline{BUSY}$-IN inhibits write in IDT7143 (SLAVE).

ORDERING INFORMATION



2746 drw 19

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 32K (4K x 8-BIT)

IDT7134S
IDT7134L

FEATURES:

- High-speed access
  - — Military: 45/55/70ns (max.)
  - — Commercial: 35/45/55/70ns (max.)
- Low-power operation
  - — IDT7134S
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7134L
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in several popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

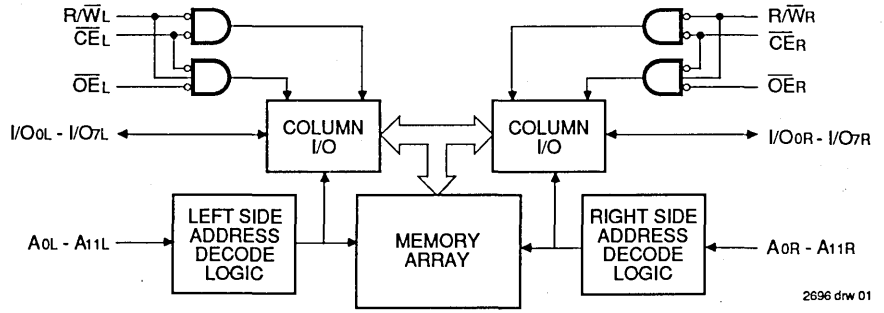
The IDT7134 is a high-speed 4K x 8 dual-port static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when both sides simultaneously access the same dual-port RAM location.

The IDT7134 provides two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these dual-ports typically operate on only 500mW of power at maximum access times as fast as 35ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 200µW from a 2V battery.

The IDT7134 is packaged on either a sidebraze or plastic 48-pin DIP, 48-pin or 52-pin LCC, and 52-pin PLCC. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



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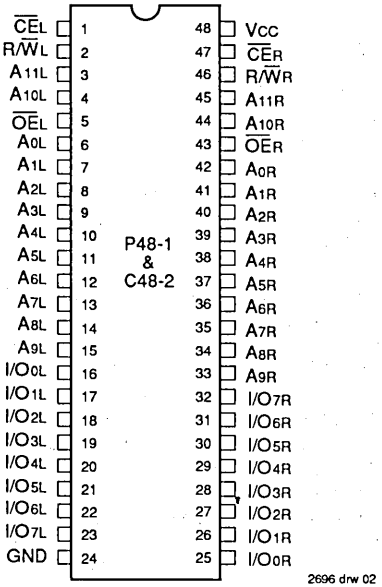
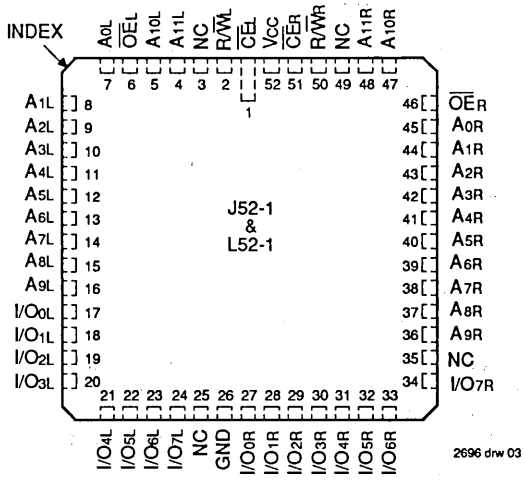
CEMOS is a trademark of Integrated Device Technology, Inc.

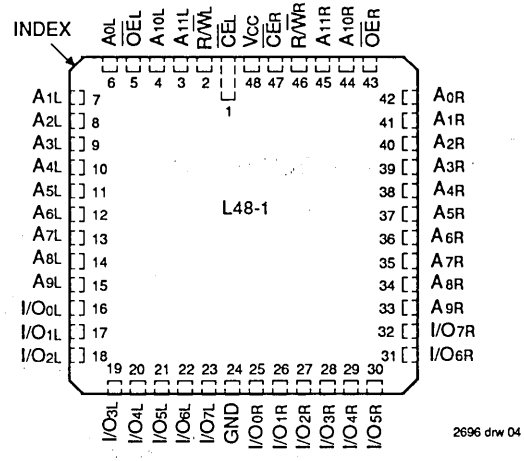
PIN CONFIGURATIONS



DIP
TOP VIEW



LCC/PLCC
TOP VIEW



LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.5	1.5	W
IOUT	DC Output Current	50	50	mA

2696 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Output Capacitance	VOUT = 0V	11	pF

2696 tbl 02

NOTE:
1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2696 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:
1. VIL (min.) = -3.0V for pulse width less than 20ns.

2696 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (Vcc = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7134S		IDT7134L		Unit
			Min.	Max.	Min.	Max.	
|ILI|	Input Leakage Current	Vcc = 5.5V, VIN = 0V to Vcc	—	10	—	5	µA
|ILO|	Output Leakage Current	$\overline{CE}$ = VIH, VOUT = 0V to Vcc	—	10	—	5	µA
VOL	Output Low Voltage	IOL = 6mA	—	0.4	—	0.4	V
		IOL = 8mA	—	0.5	—	0.5	
VOH	Output High Voltage	IOH = -4mA	2.4	—	2.4	—	V

2696 tbl 05

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1) (Vcc = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		IDT7134x35(4)		IDT7134x45		IDT7134x55		IDT7134x70		Unit
					Typ.(2)	Max.	Typ.(2)	Max.	Typ.(2)	Max.	Typ.(2)	Max.	
ICC	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = VIL, Outputs Open, f = fMAX(3)	MIL.	S	—	—	100	240	100	230	100	230	mA
				L	—	—	100	200	100	180	100	180	
			COM'L.	S	100	220	100	200	100	200	100	200	
				L	100	180	100	160	100	160	100	160	
ISB1	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ VIH, f = fMAX(3)	MIL.	S	—	—	25	70	25	70	25	70	mA
				L	—	—	25	50	25	50	25	50	
			COM'L.	S	25	75	25	70	25	70	25	70	
				L	25	45	25	40	25	40	25	40	
ISB2	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ VIH, Active Port Outputs Open, f = fMAX(3)	MIL.	S	—	—	50	160	50	150	50	150	mA
				L	—	—	50	130	50	120	50	120	
			COM'L.	S	50	140	50	130	50	130	50	130	
				L	50	110	50	100	50	100	50	100	
ISB3	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ & $\overline{CE}_R$ ≥ Vcc - 0.2V	MIL.	S	—	—	1.0	30	1.0	30	1.0	30	mA
				L	—	—	0.2	10	0.2	10	0.2	10	
		VIN ≥ Vcc - 0.2V or VIN ≤ 0.2V, f = 0(3)	COM'L.	S	1.0	15	1.0	15	1.0	15	1.0	15	
				L	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	
ISB4	Full Standby Current (One Port — All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ Vcc - 0.2V, VIN ≥ Vcc - 0.2V or VIN ≤ 0.2V, Active Port Outputs Open, f = fMAX(3)	MIL.	S	—	—	50	130	50	120	50	120	mA
				L	—	—	45	100	45	90	45	90	
			COM'L.	S	45	120	45	110	45	110	45	110	
				L	45	100	45	90	45	90	45	90	

NOTES:
1. "x" in part number indicates power rating (S or L).
2. Vcc = 5V, TA = +25°C.
3. fMAX = 1/tRC = All inputs cycling at f = 1/tRC (except Output Enable). f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby ISB3.
4. 0°C to +70°C temperature range.

2696 tbl 06

7

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES[1]

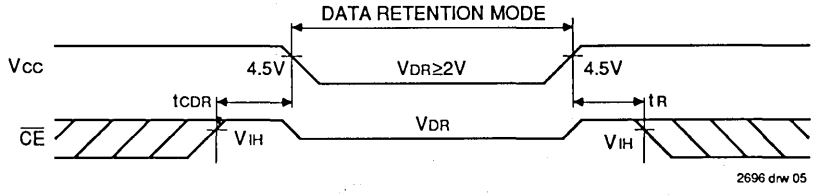
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$	MIL.	—	100	4000	µA
		$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	COM'L.	—	100	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

2696 tbl 07

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



2696 drw 05

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2696 tbl 08

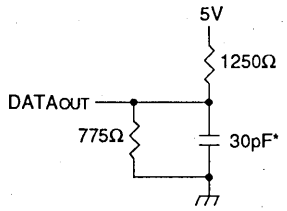
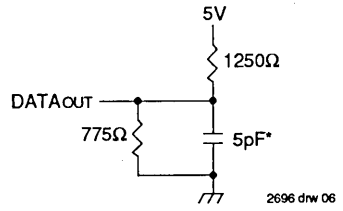


Figure 1. Output Load



2696 drw 06

Figure 2. Output Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})

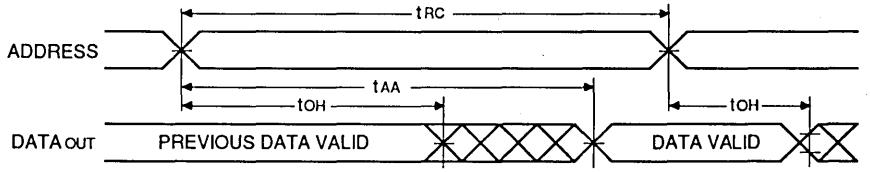
*Including scope and jig

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Symbol	Parameter	IDT7134S35[3] IDT7134L35[3] Min.	Max.	IDT7134S45 IDT7134L45 Min.	Max.	IDT7134S55 IDT7134L55 Min.	Max.	IDT7134S70 IDT7134L70 Min.	Max.	Unit
READ CYCLE										
tRC	Read Cycle Time	35	—	45	—	55	—	70	—	ns
tAA	Address Access Time	—	35	—	45	—	55	—	70	ns
tACE	Chip Enable Access Time	—	35	—	45	—	55	—	70	ns
tAOE	Output Enable Access Time	—	20	—	25	—	30	—	40	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
tLZ	Output Low Z Time[1, 2]	5	—	5	—	5	—	5	—	ns
tHZ	Output High Z Time[1, 2]	—	20	—	20	—	25	—	30	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	50	—	50	—	50	—	50	ns

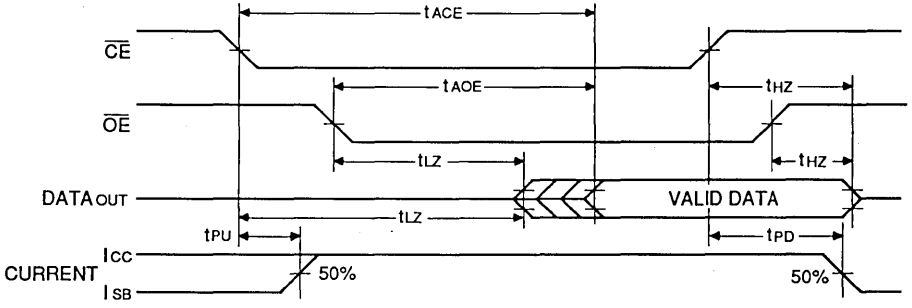
NOTES: 2698 tbl 10
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. 0°C to +70°C temperature range only.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1, 2, 4]



2696 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE[1, 3]



2696 drw 08

NOTES:
1. R/W is high for Read Cycles.
2. Device is continuously enabled, CE = VIL.
3. Addresses valid prior to or coincident with CE transition low.
4. OE = VIL.

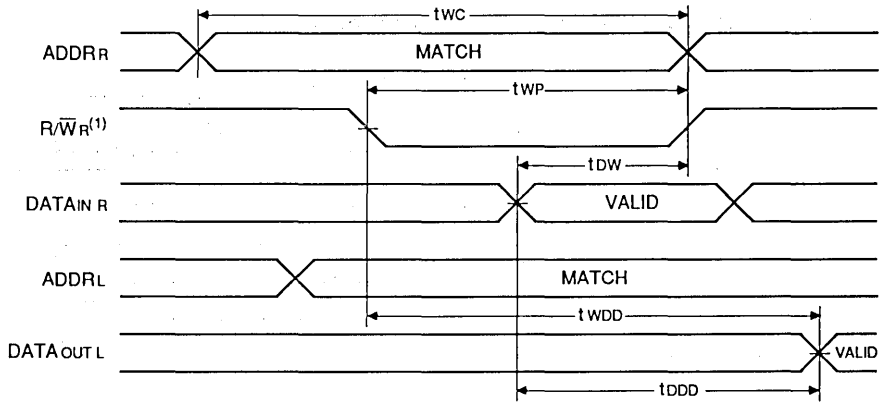
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Symbol	Parameter	IDT7134S35[5] IDT7134L35[5]		IDT7134S45 IDT7134L45		IDT7134S55 IDT7134L55		IDT7134S70 IDT7134L70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
tWC	Write Cycle Time	35	—	45	—	55	—	70	—	ns
tEW	Chip Enable to End of Write	30	—	40	—	50	—	60	—	ns
tAW	Address Valid to End of Write	30	—	40	—	50	—	60	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	30	—	40	—	50	—	60	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	20	—	20	—	25	—	30	—	ns
tHZ	Output High Z Time[1, 2]	—	20	—	20	—	25	—	30	ns
tDH	Data Hold Time[3]	3	—	3	—	3	—	3	—	ns
tWZ	Write Enabled to Output in High Z[1, 2]	—	20	—	20	—	25	—	30	ns
tOW	Output Active from End of Write[1, 2, 3]	3	—	3	—	3	—	3	—	ns
tWDD	Write Pulse to Data Delay[4]	—	80	—	80	—	80	—	90	ns
tDDD	Write Data Valid to Read Data Delay[4]	—	55	—	55	—	55	—	70	ns

2696 tbl 10

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read with Port-to-Port Delay".
5. 0°C to +70°C temperature range only.
6. Specified for $\overline{OE}$ at high (refer to "Timing Waveform of Write Cycle", Note 7).

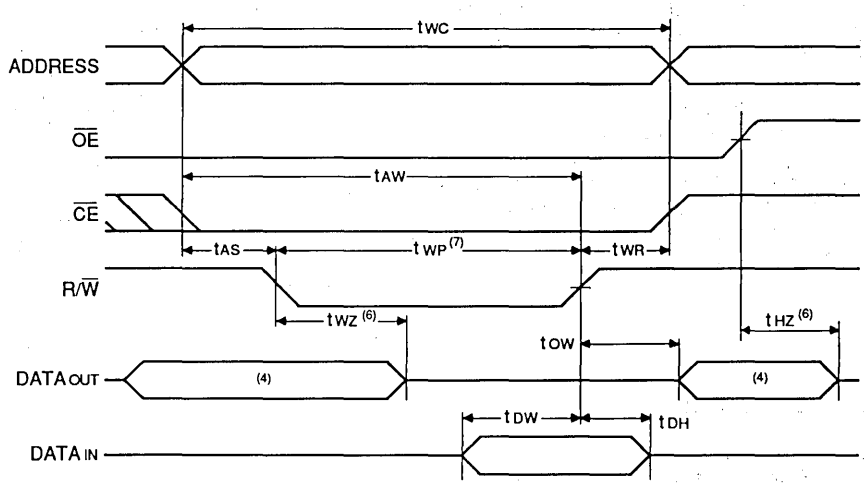
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY[1]



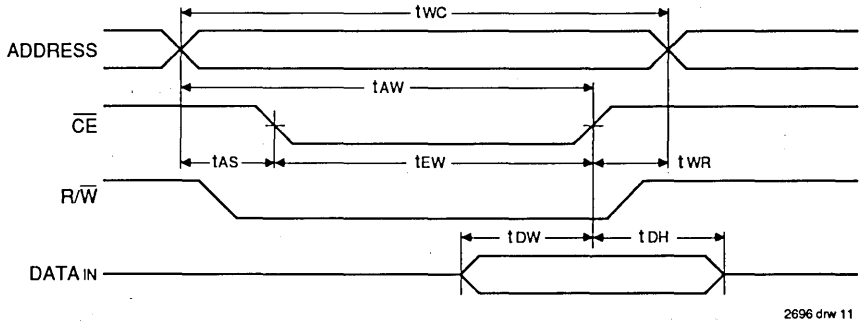
2696 drw 09

NOTES:
1. Write cycle parameters should be adhered to in order to ensure proper writing.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1, 2, 3, 4, 6, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1, 2, 3, 5)



NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP .

FUNCTIONAL DESCRIPTION:

The IDT7134 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in the table below.

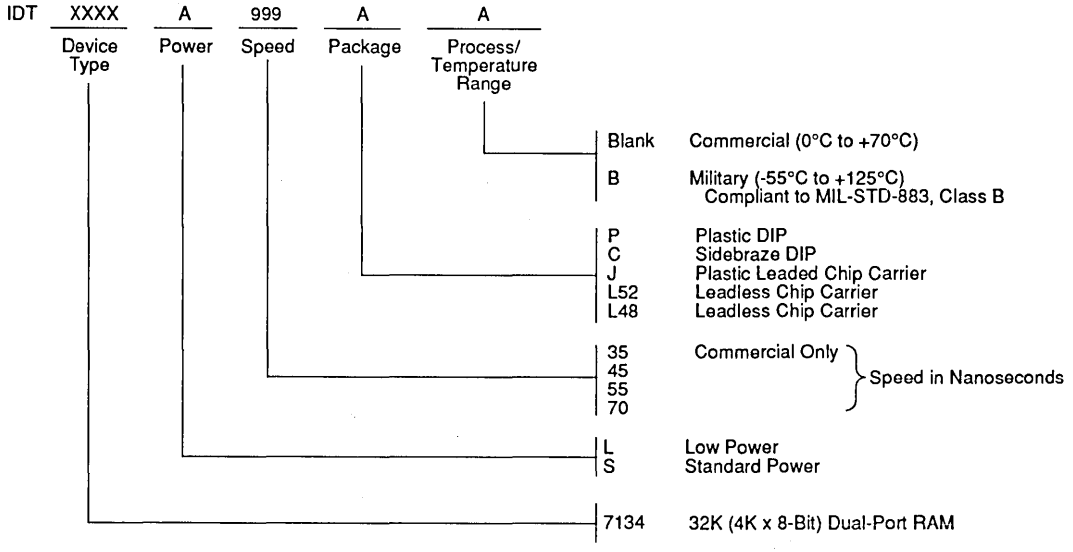
TABLE I – READ/WRITE CONTROL

Left or Right Port(1)				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	Function
X	H	X	Z	Port Disabled and in Power Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	$DATA_{IN}$	Data on port written into memory
H	L	L	$DATA_{OUT}$	Data in memory output on port
X	X	H	Z	High impedance outputs

NOTES: 2696 tbl 11

1. A_{0L} - $A_{11L} \neq A_{0R}$ - A_{11R}
   H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

ORDERING INFORMATION



2696 drw 12

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 32K (4K x 8-BIT)

PRELIMINARY
IDT7134SA
IDT7134LA

FEATURES:

- High-speed access
  - — Military: 35/45/55/70ns (max.)
  - — Commercial: 25/35/45/55/70ns (max.)
- Low-power operation
  - — IDT7134SA
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7134LA
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in several popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

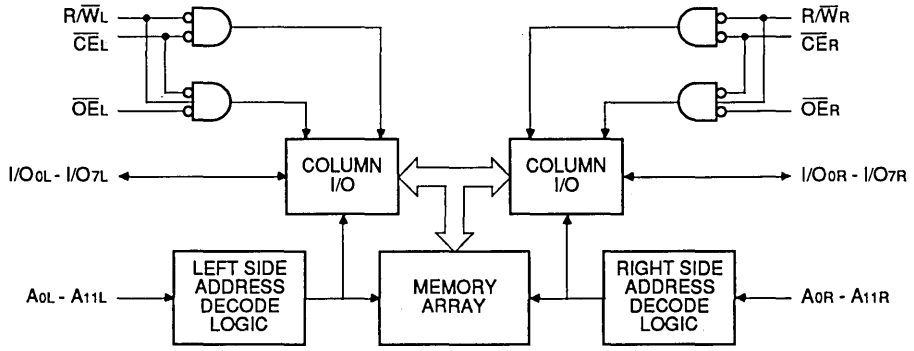
The IDT7134 is an extremely high-speed 4K x 8 dual-port static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when both sides simultaneously access the same dual-port RAM location.

The IDT7134 provides two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these dual-port typically on only 500mW of power at maximum access times as fast as 25ns. Low -power (LA) versions offer battery backup data retention capability, with each port typically consuming 1mW from a 2V battery.

The IDT7134 is packaged on either a sidebraze or plastic 48-pin DIP, 48-pin or 52-pin LCC, and 52-pin PLCC. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM

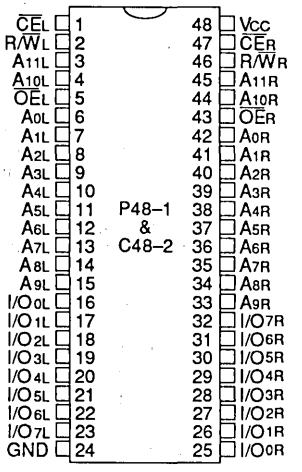


2720 drw 01

7

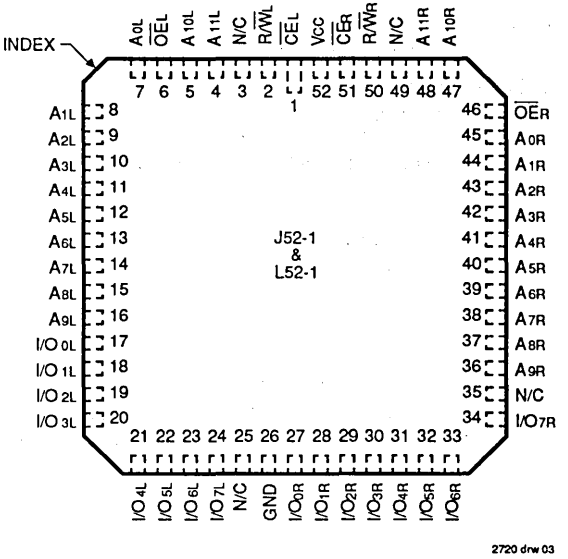
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



2720 drw 02

DIP
TOP VIEW



2720 drw 03

LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to Ground	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	1.5	1.5	W
IOUT	DC Output Current	50	50	mA

2720 tbl 01

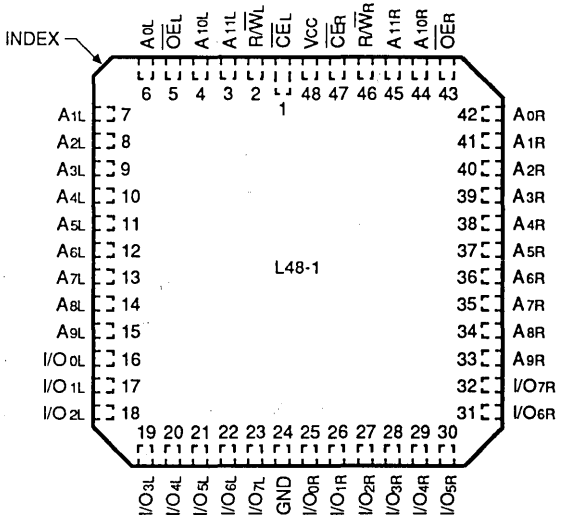
NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE(1) (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Output Capacitance	VOUT = 0V	11	pF

2720 tbl 02

NOTE:
1. This parameter is determined by device characterization but is not production tested.



2720 drw 04

LCC
TOP VIEW

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	−55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2720 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2720 tbl 04

NOTE:
1. V_{IL} (min.) = −3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (Vcc = 5V ± 10%)

Symbol	Parameter	Test Conditions	IDT7134SA		IDT7134LA		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	Vcc = 5.5V, V_{IN} = 0V to Vcc	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to Vcc	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 6mA	—	0.4	—	0.4	V
		I_{OL} = 8mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = −4mA	2.4	—	2.4	—	V

2720 tbl 05

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1) (Vcc = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version		7134x25(4)		7134x35		7134x45		7134x55		7134x70		Unit
					Typ.(2)	Max.	Typ.(2)	Max.	Typ.(2)	Max.	Typ.(2)	Max.	Typ.(2)	Max.	
Icc	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ ≤ V_{IL} Outputs Open f = f_{MAX}(3)	MIL.	S	—	—	100	260	100	240	100	230	100	230	mA
				L	—	—	100	220	100	200	100	180	100	180	
			COM'L.	S	100	240	100	220	100	200	100	200	100	200	
				L	100	200	100	180	100	160	100	160	100	160	
I_{SB1}	Standby Current (Both Ports—TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH} f = f_{MAX}(3)	MIL.	S	—	—	25	75	25	70	25	70	25	70	mA
				L	—	—	25	55	25	50	25	50	25	50	
			COM'L.	S	25	80	25	75	25	70	25	70	25	70	
				L	25	50	25	45	25	40	25	40	25	40	
I_{SB2}	Standby Current (One Port—TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH} Active Port Outputs Open, f = f_{MAX}(3)	MIL.	S	—	—	50	170	50	160	50	150	50	150	mA
				L	—	—	50	140	50	130	50	120	50	120	
			COM'L.	S	50	150	50	140	50	130	50	130	50	130	
				L	50	120	50	110	50	100	50	100	50	100	
I_{SB3}	Full Standby Current (Both Ports—All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ Vcc - 0.2V	MIL.	S	—	—	1.0	30	1.0	30	1.0	30	1.0	30	mA
				L	—	—	0.2	10	0.2	10	0.2	10	0.2	10	
		V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ 0.2V, f = 0(3)	COM'L.	S	1.0	15	1.0	15	1.0	15	1.0	15	1.0	15	
				L	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	
I_{SB4}	Full Standby Current (One Port—All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ Vcc - 0.2V	MIL.	S	—	—	50	140	50	130	50	120	50	120	mA
				L	—	—	45	110	45	100	45	90	45	90	
		V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX}(3)	COM'L.	S	45	130	45	120	45	110	45	110	45	110	
				L	45	110	45	100	45	90	45	90	45	90	

2720 tbl 06

NOTES:
1. "x" in part number indicates power rating (SA or LA).
2. Vcc = 5V, Ta = +25°C.
3. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except Output Enable). f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby I_{SB3}.
4. 0°C to +70°C temperature range.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES[1]

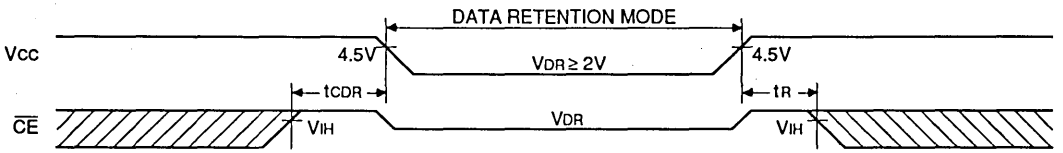
(LA Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	VCC for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$	MIL.	—	100	4000	µA
		$V_{IN} \geq V_{HC}$ or V_{LC}	COM'L.	—	100	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

2720 tbl 07

NOTES:
1. V_{CC} = 2V, T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



2720 drw 05

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2720 tbl 08

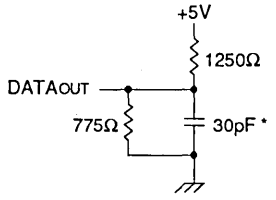
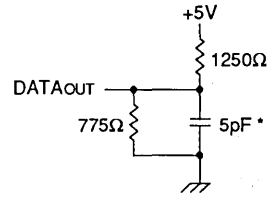


Figure 1. Output Load



2720 drw 06

Figure 2. Output Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})

*Including scope and jig

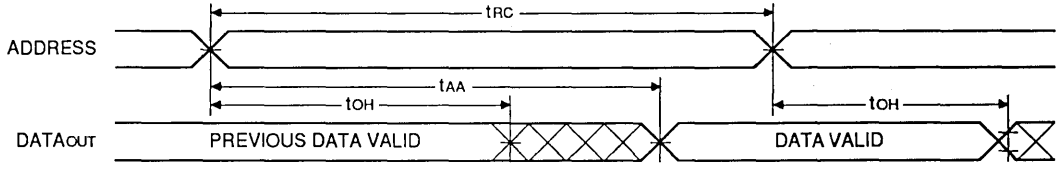
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[4]

Symbol	Parameter	7134X25[3]		7134X35		7134X45		7134X55		7134X70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
tRC	Read Cycle Time	25	—	35	—	45	—	55	—	70	—	ns
tAA	Address Access Time	—	25	—	35	—	45	—	55	—	70	ns
tACE	Chip Enable Access Time	—	25	—	35	—	45	—	55	—	70	ns
tAOE	Output Enable Access Time	—	15	—	20	—	25	—	30	—	40	ns
tOH	Output Hold from Address Change	0	—	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time[1, 2]	0	—	0	—	5	—	5	—	5	—	ns
tHZ	Output High Z Time[1, 2]	—	15	—	20	—	25	—	30	—	40	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	50	—	50	—	50	—	50	—	50	ns

2720 tbl 09

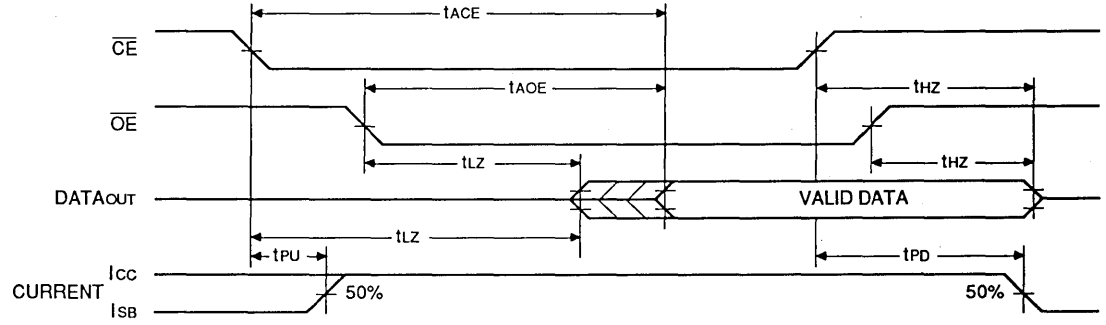
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. 0°C to +70°C temperature range only.
4. "X" in part number indicates power rating (SA or LA).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1, 2, 4]



2720 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE[1, 3]



2720 drw 08

NOTES:
1. R/W is high for Read Cycles.
2. Device is continuously enabled, CE = VIL.
3. Addresses valid prior to or coincident with CE transition low.
4. OE = VIL.

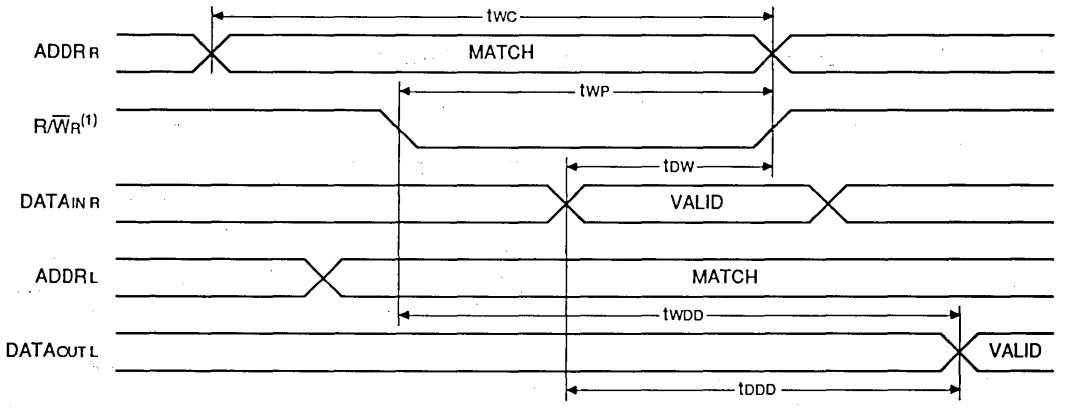
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[7]

Symbol	Parameter	7134X25[5]		7134X35		7134X45		7134X55		7134X70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
	WRITE CYCLE											
t_{WC}	Write Cycle Time	25	—	35	—	45	—	55	—	70	—	ns
t_{EW}	Chip Enable to End of Write	20	—	30	—	40	—	50	—	60	—	ns
t_{AW}	Address Valid to End of Write	20	—	30	—	40	—	50	—	60	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	30	—	40	—	50	—	60	—	ns
t_{WR}	Write RecoveryTime	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	15	—	20	—	20	—	25	—	30	—	ns
t_{HZ}	Output High Z Time[1, 2]	—	15	—	20	—	20	—	25	—	30	ns
t_{DH}	Data Hold Time[3]	0	—	3	—	3	—	3	—	3	—	ns
t_{WZ}	Write Enabled to Output in High Z[1, 2]	—	15	—	20	—	20	—	25	—	30	ns
t_{OW}	Output Active from End of Write[1, 2, 3]	3	—	3	—	3	—	3	—	3	—	ns
t_{WDD}	Write Pulse to Data Delay[4]	—	50	—	60	—	70	—	80	—	90	ns
t_{DDD}	Write Data Valid to Read Data Delay[4]	—	35	—	45	—	55	—	65	—	80	ns

2720 tbl 10

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read with Port-to-Port Delay"
5. 0°C to +70°C temperature range only.
6. Specified for $\overline{OE}$ at high (refer to "Timing Waveform of Write Cycle", Note 7).
7. "X" in part number indicates power rating (SA or LA).

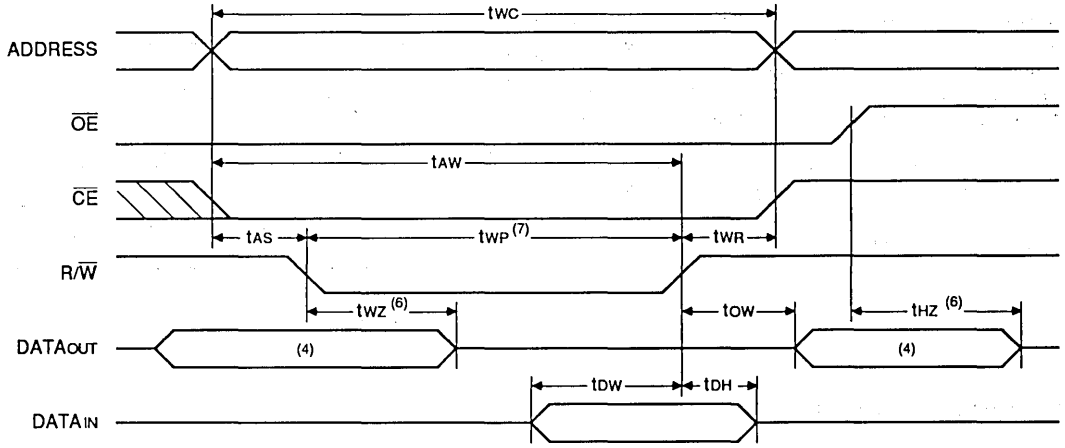
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY[1]



2720 drw 09

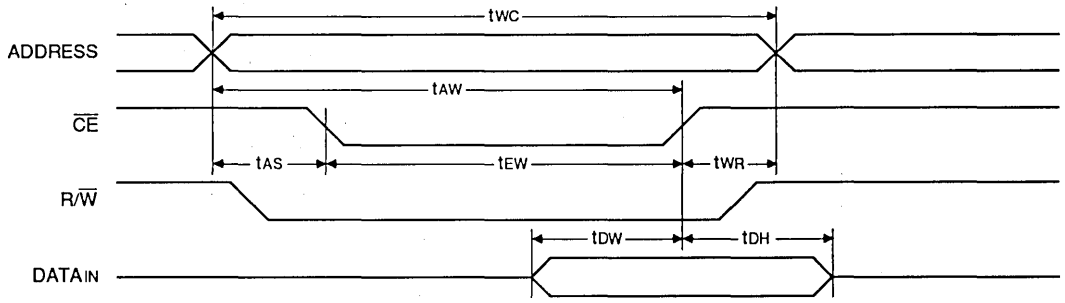
NOTE:
1. Write cycle parameters should be adhered to, in order to ensure proper writing.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1, 2, 3, 4, 6, 7)



2720 drw 10

TIMING WAVEFORM OF WRITE CYCLE NO. 1, $\overline{CE}$ CONTROLLED TIMING(1, 2, 3, 5)



2720 drw 11

NOTE:S

1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

FUNCTIONAL DESCRIPTION

The IDT7134 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in the table below.

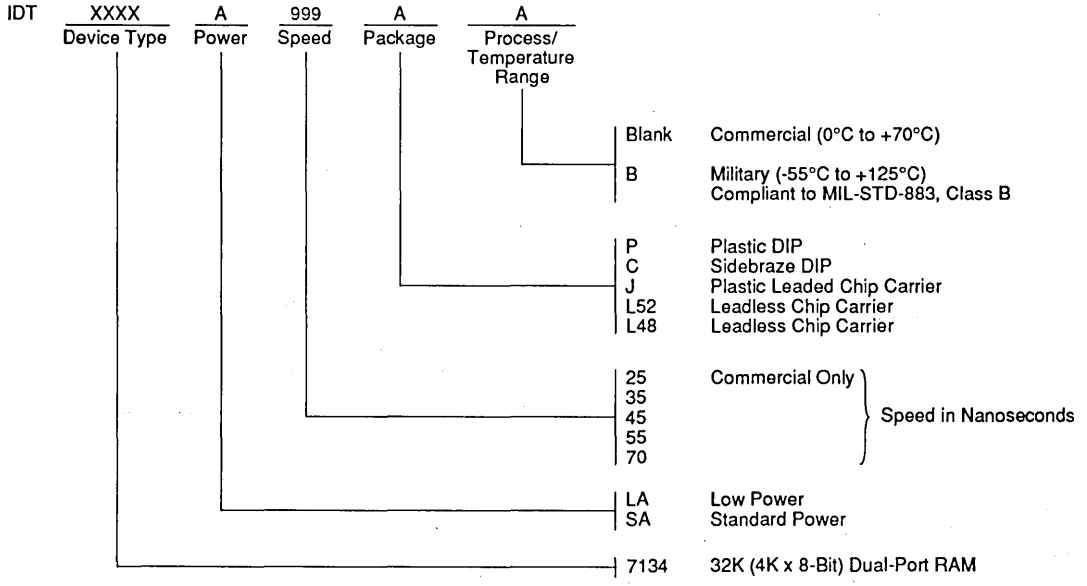
TABLE I – READ/WRITE CONTROL

Left or Right Port(1)				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	Function
X	H	X	Z	Port Disabled and in Power Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	$DATA_{IN}$	Data on port written into memory
H	L	L	$DATA_{OUT}$	Data in memory output on port
X	X	H	Z	High impedance outputs

2720 tbl 11

NOTE:
1. $A_{0L} - A_{11L} \neq A_{0R} - A_{11R}$
H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

ORDERING INFORMATION



2720 drw 12

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 32K (4K x 8-BIT) WITH SEMAPHORE

IDT71342S
IDT71342L

FEATURES

- High-speed access
  - — Military: 45/55/70ns (max.)
  - — Commercial: 35/45/55/70ns (max.)
- Low-power operation
  - — IDT71342S
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - — IDT71342L
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- Full on-chip hardware support of semaphore signalling between ports
- Battery backup operation—2V data retention
- TTL-compatible; single +5V (±10%) power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION

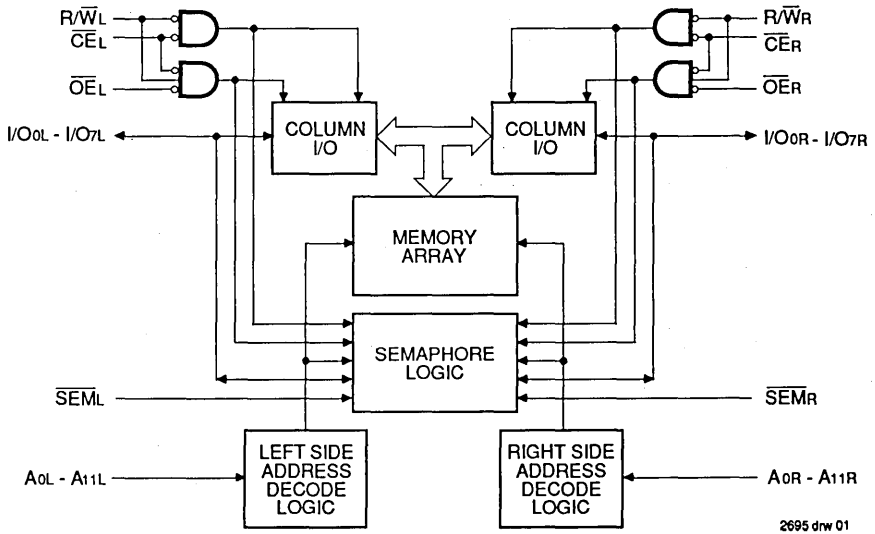
The IDT71342 is an extremely high-speed 4K x 8 dual-port static RAM with full on-chip hardware support of semaphore signalling between the two ports.

The IDT71342 provides two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads and writes to any location in memory. To assist in arbitrating between ports, a fully independent semaphore logic block is provided. This block contains unassigned flags which can be accessed by either side; however, only one side can control the flag at any time. An automatic power down feature, controlled by $\overline{CE}$ and $\overline{SEM}$, permits the on-chip circuitry of each port to enter a very low standby power mode (both $\overline{CE}$ and $\overline{SEM}$ high).

Fabricated using IDT's CEMOS™ high-performance technology, this device typically operates on only 500mW of power at maximum access times as fast as 35ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 200µW from a 2V battery. The device is packaged in either a hermetic 52-pin leadless chip carrier or a 52-pin PLCC.

The IDT 71342 military devices are manufactured in compliance with the latest revision of MIL-STD-883, Class B.

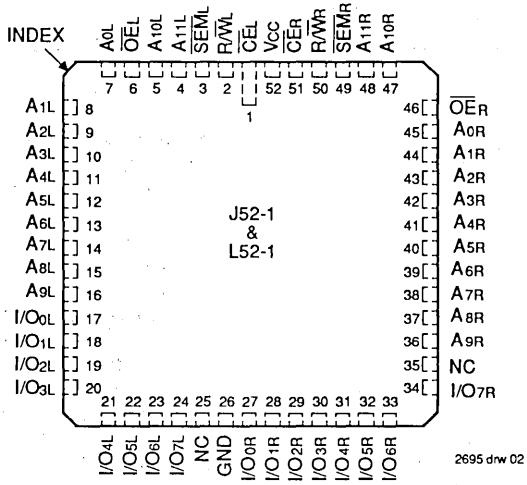
FUNCTIONAL BLOCK DIAGRAM



7

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.5	1.5	W
IOUT	DC Output Current	50	50	mA

NOTE: 2695 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Output Capacitance	VOUT = 0V	11	pF

NOTE: 2695 tbl 02

1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2695 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE: 2695 tbl 04

1. VIL (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT71342S		IDT71342L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 6mA	—	0.4	—	0.4	V
		I_{OL} = 8mA	—	0.5	—	0.5	
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2695 tbl 05

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		IDT71342x35[4]		IDT71342x45		IDT71342x55		IDT71342x70		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \le V_{IL}$ Outputs Open	MIL.	S	—	—	100	240	100	230	100	230	mA
				L	—	—	100	200	100	180	100	180	
		$\overline{SEM} \ge V_{IH}$ f = f_{MAX}[3]	COM'L.	S	100	220	100	200	100	200	100	200	
				L	100	180	100	160	100	160	100	160	
I_{CC1}	Dynamic Operation Current (Semaphores Both Sides)	$\overline{CE} \ge V_{IH}$ $\overline{SEM} \le V_{IL}$ Outputs Open f = f_{MAX}[3]	MIL.	S	—	—	85	130	85	130	85	130	mA
				L	—	—	85	110	85	110	85	110	
			COM'L.	S	85	145	85	130	85	130	85	130	
				L	85	115	85	100	85	100	85	100	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE_L}$ and $\overline{CE_R} \ge V_{IH}$ $\overline{SEM_L} = \overline{SEM_R} \ge V_{IH}$ f = f_{MAX}[3]	MIL.	S	—	—	25	70	25	70	25	70	mA
				L	—	—	25	50	25	50	25	50	
			COM'L.	S	25	75	25	70	25	70	25	70	
				L	25	45	25	40	25	40	25	40	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE_L}$ or $\overline{CE_R} \ge V_{IH}$ Active Port Outputs Open, f = f_{MAX}[3] $\overline{SEM_L} = \overline{SEM_R} \ge V_{IH}$	MIL.	S	—	—	50	160	50	150	50	150	mA
				L	—	—	50	130	50	120	50	120	
			COM'L.	S	50	140	50	130	50	130	50	130	
				L	50	110	50	100	50	100	50	100	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE_L}$ & $\overline{CE_R} \ge V_{CC}$ - 0.2V $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le 0.2V$ $\overline{SEM_L} = \overline{SEM_R} \ge$ V_{CC}-0.2V, f = 0[3]	MIL.	S	—	—	1.0	30	1.0	30	1.0	30	mA
				L	—	—	0.2	10	0.2	10	0.2	10	
			COM'L.	S	1	15	1.0	15	1.0	15	1.0	15	
				L	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	One Port $\overline{CE_L}$ or $\overline{CE_R} \ge V_{CC}$ - 0.2V $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le 0.2V$ Active Port Outputs Open, f = f_{MAX}[3]	MIL.	S	—	—	50	130	50	120	50	120	mA
				L	—	—	45	100	45	90	45	90	
			COM'L.	S	45	120	45	110	45	110	45	110	
				L	45	100	45	90	45	90	45	90	

NOTES:

2695 tbl 06

1. "x" in part number indicates power rating (S or L).
2. V_{CC} = 5V, T_A = +25°C.
3. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except Output Enable). f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby I_{SB3}.
4. 0°C to +70°C temperature range only.

7

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES[1]

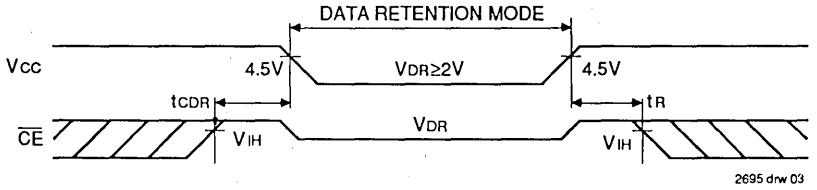
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	V
I_{CCDR}	Data Retention Current	V_{CC} = 2V	MIL.	—	100	4000	µA
		$\overline{CE} \geq V_{HC}$	COM'L.	—	100	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$		0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

2695 tbl 07

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2696 tbl 08

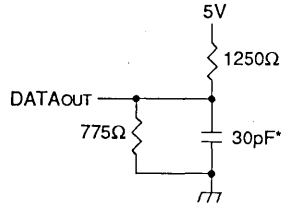


Figure 1. Output Load

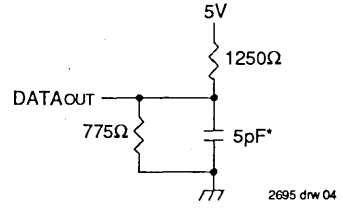


Figure 2. Output Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})

*Including scope and jig

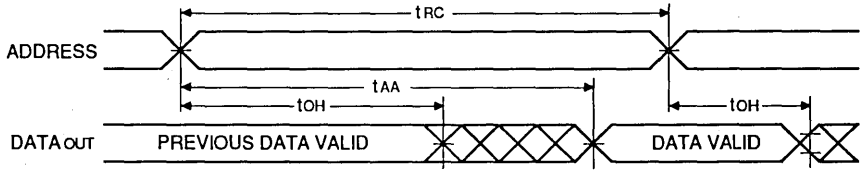
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

Symbol	Parameter	IDT71342S35[5] IDT71342L35[5] Min.	Max.	IDT71342S45 IDT71342L45 Min.	Max.	IDT71342S55 IDT71342L55 Min.	Max.	IDT71342S70 IDT71342L70 Min.	Max.	Unit
READ CYCLE										
tRC	Read Cycle Time	35	—	45	—	55	—	70	—	ns
tAA	Address Access Time	—	35	—	45	—	55	—	70	ns
tACE	Chip Enable Access Time[3]	—	35	—	45	—	55	—	70	ns
tAOE	Output Enable Access Time	—	20	—	25	—	30	—	40	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
tLZ	Output Low Z Time[1, 2]	5	—	5	—	5	—	5	—	ns
tHZ	Output High Z Time[1, 2]	—	20	—	20	—	25	—	30	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	50	—	50	—	50	—	50	ns
tSOP	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay[4]	—	80	—	80	—	80	—	90	ns
tDDD	Write Data Valid to Read Data Delay[4]	—	55	—	55	—	55	—	70	ns

2695 tbl 09

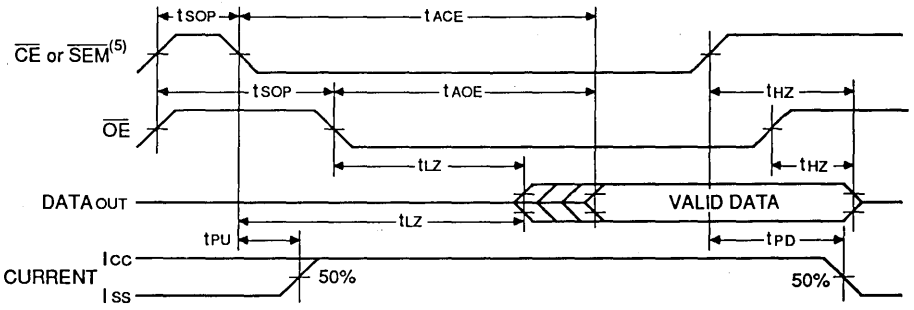
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = VIL, $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH, $\overline{SEM}$ = VIL.
4. Port to Port delay through RAM cells from writing port to a reading port.
5. 0°C to +70°C temperature range only.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1, 2, 4]



2695 drw 05

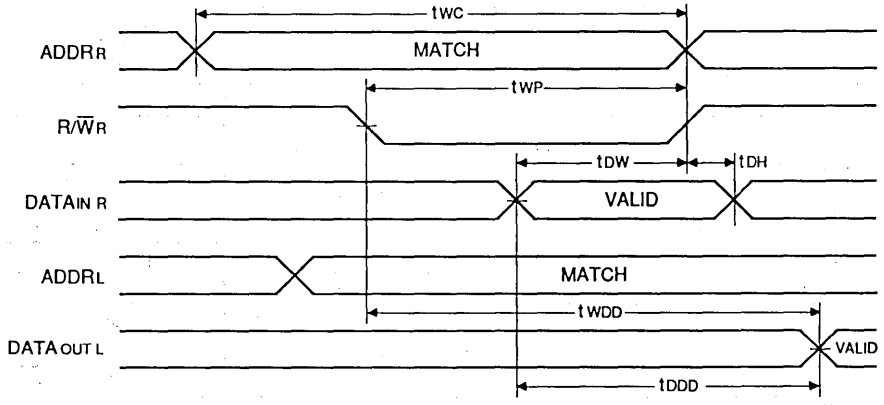
TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE[1, 3]



2695 drw 06

NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = VIL. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = VIL.
5. To access RAM, $\overline{CE}$ = VIH, $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH, $\overline{SEM}$ = VIL.

TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY(1, 2)



2695 drw 07

NOTES:
1. Write cycle parameters should be adhered to, to ensure proper writing.
2. Device is continously enabled for both ports.

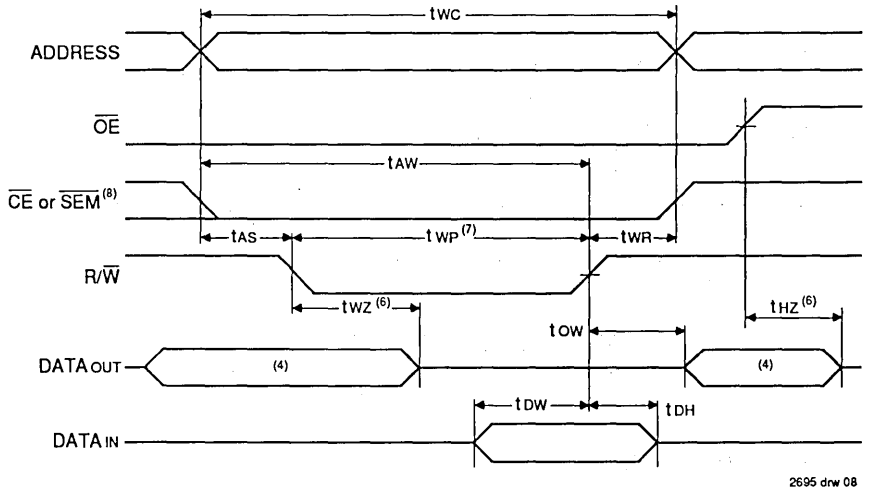
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

Symbol	Parameter	IDT71342S35(5) IDT71342L35(5) Min.	Max.	IDT71342S45 IDT71342L45 Min.	Max.	IDT71342S55 IDT71342L55 Min.	Max.	IDT71342S70 IDT71342L70 Min.	Max.	Unit
WRITE CYCLE										
tWC	Write Cycle Time	35	—	45	—	55	—	70	—	ns
tEW	Chip Enable to End of Write(3)	30	—	40	—	50	—	60	—	ns
tAW	Address Valid to End of Write	30	—	40	—	50	—	60	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	30	—	40	—	50	—	60	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	20	—	20	—	25	—	30	—	ns
tHZ	Output High Z Time(1, 2)	—	20	—	20	—	25	—	30	ns
tDH	Data Hold Time(4)	3	—	3	—	3	—	3	—	ns
tWZ	Write Enabled to Output in High Z(1, 2)	—	20	—	20	—	25	—	30	ns
tOW	Output Active from End of Write(1, 2, 4)	3	—	3	—	3	—	3	—	ns
tSWR	SEM Flag Write to Read Time	10	—	10	—	10	—	10	—	ns
tSPS	SEM Flag Contention Window	10	—	10	—	10	—	10	—	ns

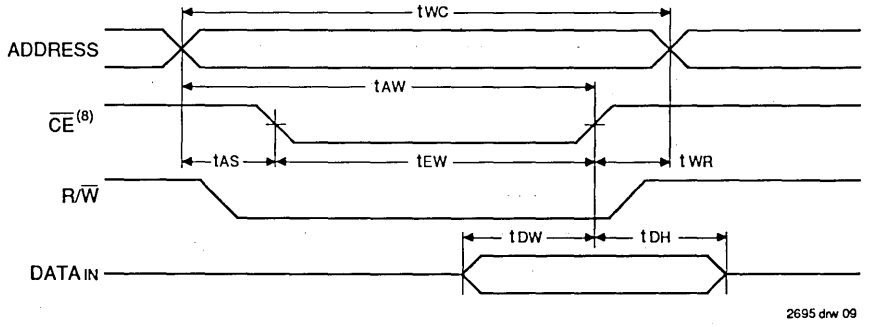
2695 tbl 10

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = VIL, $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH, $\overline{SEM}$ = VIL. This condition must be valid for the entire tEW time.
4. The specification for tDH must be met by the device supplying data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
5. 0°C to +70°C temperature range only.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1, 2, 3, 7)

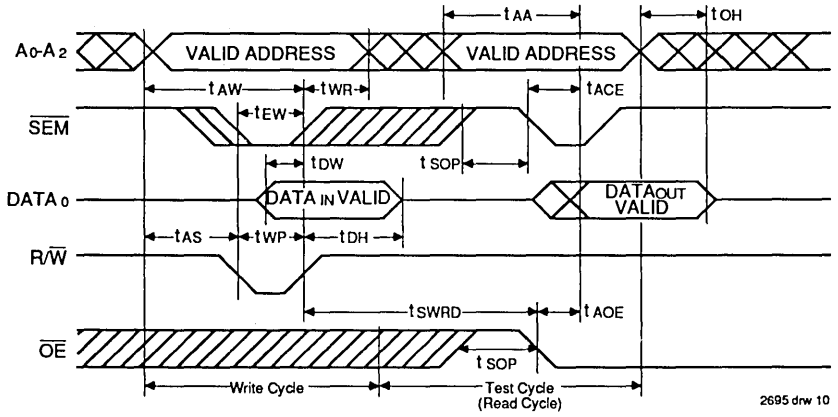


TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1, 2, 3, 5)



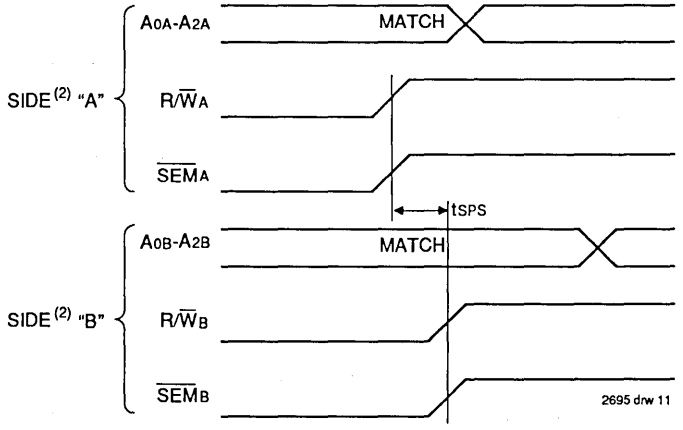
NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ or $\overline{SEM}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
8. To access RAM, $\overline{CE}$ = VIL, $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH, $\overline{SEM}$ = VIL. Either condition must be valid for the entire tEW time.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



NOTE:
1. $\overline{CE}$ = VIH for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE CONTENTION[1, 3, 4]



NOTE:
1. DOR = DOL = VIL, $\overline{CE}$R = $\overline{CE}$L = VIH, Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. Either side "A" = left and side "B" = right, or side "A" = right and side "B" = left.
3. This parameter is measured from the point where R/$\overline{W}$A or $\overline{SEM}$A goes high until R/$\overline{W}$B or $\overline{SEM}$B goes high.
4. If tSPS is violated, the semaphore will fall positively to one side or the other,but there is no guarantee which side will obtain the flag.

FUNCTIONAL DESCRIPTION

The IDT71342 is an extremely fast dual-port 4K x 8 CMOS static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the dual-port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the dual-port RAM or any other shared resource.

The dual-port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS static RAMs and can be read from or written to at the same time, with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the dual-port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the dual-port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the repective port to go into standby mode when not selected. This is the condition which is shown in Table 1 where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT71342 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT71342's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT71342 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the dual-port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that a shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor had set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT71342 in a separate memory space from the dual-port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard static RAM. Each of the flags has a unique address which can be accessed by either side through address pins $A_0 - A_2$. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D_0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other (see Table II). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence of WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as a one, a fact which the processor will verify by the subsequent read (see Table II). As an example, assume a

processor writes a zero the the left prot at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during a subsequent read. Had a seqence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 3. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

TABLE I – NON-CONTENTION READ/WRITE CONTROL

Left or Right Port[1]					
R/$\overline{W}$	$\overline{CE}$	$\overline{SEM}$	$\overline{OE}$	D_{0-7}	Function
X	H	H	X	Z	Port Disabled and in Power Down Mode
H	H	L	L	$DATA_{OUT}$	Data in Semaphore Flag Output on Port
X	X	X	H	Z	Output Disabled
⌐	H	L	X	$DATA_{IN}$	Port Data Bit D_0 Written Into Semaphore Flag
H	L	H	L	$DATA_{OUT}$	Data in memory output on port
L	L	H	X	$DATA_{IN}$	Data on port written into memory
X	L	L	X	—	Not Allowed

NOTES: 2695tbl 11

1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$
   H = HIGH, L = LOW, X = Don't Care, Z = High Impedance
   ⌐ = Low-to-High transition.

TABLE II – EXAMPLE SEMAPHORE PROCUREMENT SEQUENCE

Function	$D_0 - D_7$ Left	$D_0 - D_7$ Right	STATUS
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left side has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

NOTE: 2695 tbl 12

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT71342.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen. Code integrity is of the utmost importance when semaphores are used instead of slower, more restrictive hardware intensive schemes.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES – Some examples

Perhaps the simplest application of semaphores is their application as resource markers for the IDT71342's dual-port RAM. Say the 4K x 8 RAM was to be divided into two 2K x 8 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 2K of dual-port RAM, the processor on the left port could write and then read a zero into Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 2K. Meanwhile, the right processor would attempt to perform the same function. Since this processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 2K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control , it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 2K blocks of dual-port RAM with each other.

The blocks do not have to by any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the dual-port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices had determined which memory area was "off limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

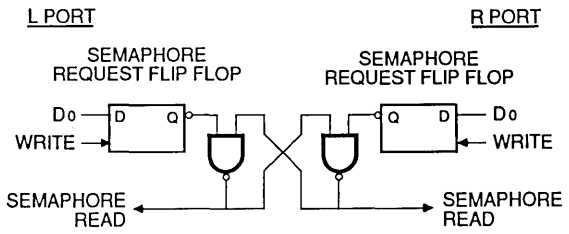
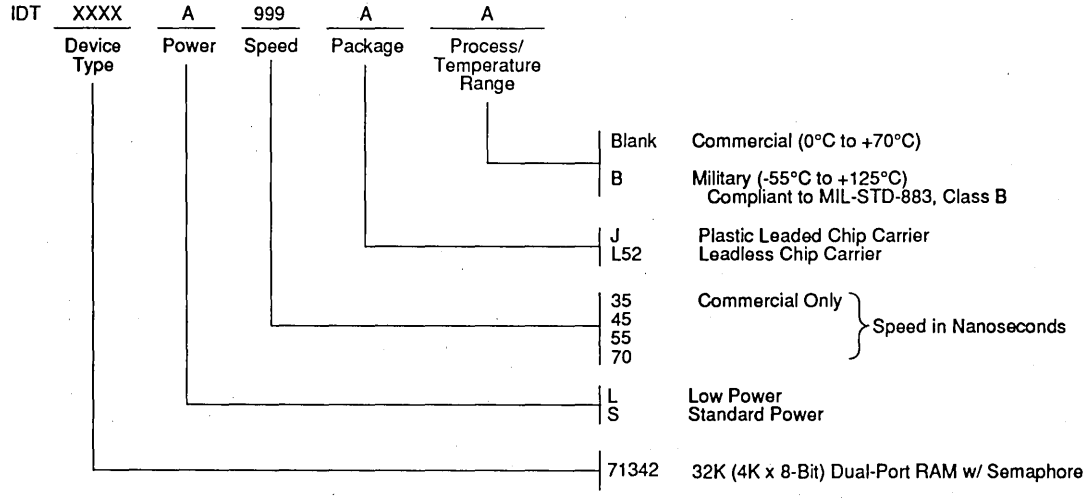


Figure 3. IDT71342 Semaphore Logic

ORDERING INFORMATION



2695 drw 13

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 32K (4K x 8-BIT) WITH SEMAPHORE

PRELIMINARY
IDT71342SA
IDT71342LA

FEATURES:

- High-speed access
  - — Military: 35/45/55/70ns (max.)
  - — Commercial: 25/35/45/55/70ns (max.)
- Low-power operation
  - — IDT71342SA
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - — IDT71342LA
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- Full on-chip hardware support of semaphore signalling between ports
- Battery backup operation—2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

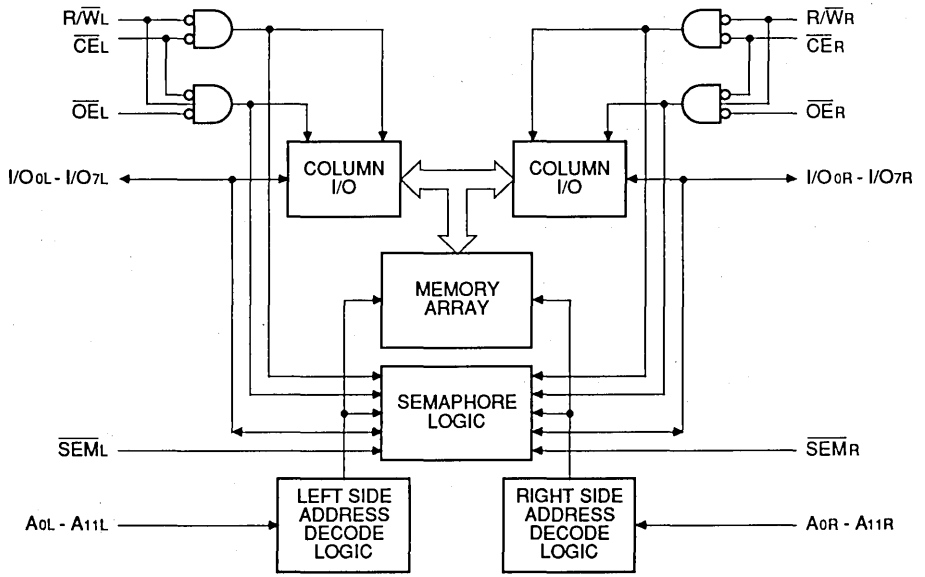
The IDT71342 is an extremely high-speed 4K x 8 dual-port static RAM with full on-chip hardware support of semaphore signalling between the two ports.

The IDT71342 provides two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. To assist in arbitrating between ports, a fully independent semaphore logic block is provided. This block contains unassigned flags which can be accessed by either side; however, only one side can control the flag at any time. An automatic power down feature, controlled by $\overline{CE}$ and $\overline{SEM}$, permits the on-chip circuitry of each port to enter a very low standby power mode (both $\overline{CE}$ and $\overline{SEM}$ high).

Fabricated using IDT's CEMOS™ high-performance technology, this device typically operates on only 500mW of power at maximum access times as fast as 25ns. Low-power (LA) versions offer battery backup data retention capability, with each port typically consuming 1mW from a 2V battery. The device is packaged in either a hermetic 52-pin leadless chip carrier or a 52-pin PLCC.

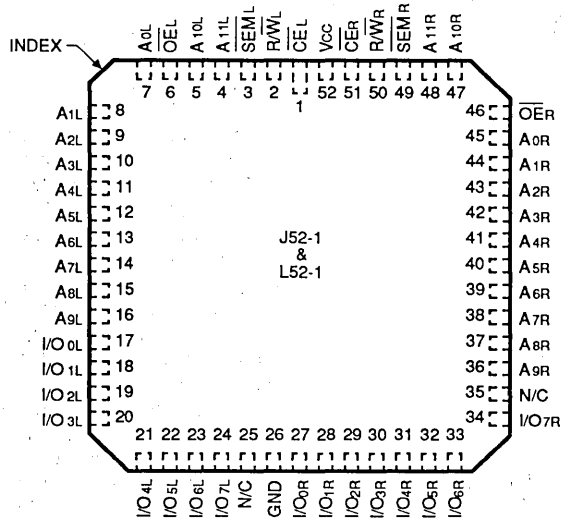
The IDT71342 military devices are manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



LCC/PLCC
TOP VIEW

2721 drw 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to Ground	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	1.5	1.5	W
IOUT	DC Output Current	50	50	mA

2721 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE(1) (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Output Capacitance	VOUT = 0V	11	pF

2721 tbl 02

NOTE:
1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2721 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

2721 tbl 04

NOTE:
1. VIL (min.) = –3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Conditions	IDT71342SA		IDT71342LA		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 6mA	—	0.4	—	0.4	V
		I_{OL} = 8mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4	—	2.4	—	V

2721 tbl 05

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version		71342x25[4]		71342x35		71342x45		71342x55		71342x70		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \le V_{IL}$ Outputs Open	MIL.	S	—	—	100	260	100	240	100	230	100	230	mA
				L	—	—	100	220	100	200	100	180	100	180	
		$\overline{SEM}$ = Don't Care f = f_{MAX}[3]	COM'L.	S	100	240	100	220	100	200	100	200	100	200	
				L	100	200	100	180	100	160	100	160	100	160	
I_{CC1}	Dynamic Operating Current (Semaphores Both Sides)	$\overline{CE} \ge V_H$ Outputs Open	MIL.	S	—	—	85	150	85	130	85	130	85	130	mA
				L	—	—	85	130	85	110	85	110	85	110	
		$\overline{SEM} \le V_L$ f = f_{MAX}[3]	COM'L.	S	85	160	85	145	85	130	85	130	85	130	
				L	85	130	85	115	85	100	85	100	85	100	
I_{SB1}	Standby Current (Both Ports—TTL Level Inputs)	$\overline{CE_L}$ and $\overline{CE_R} \ge V_{IH}$ $\overline{SEM_L}$ = $\overline{SEM_R} \ge V_{IH}$	MIL.	S	—	—	25	75	25	70	25	70	25	70	mA
				L	—	—	25	55	25	50	25	50	25	50	
		f = f_{MAX}[3]	COM'L.	S	25	80	25	75	25	70	25	70	25	70	
				L	25	50	25	45	25	40	25	40	25	40	
I_{SB2}	Standby Current (One Port—TTL Level Inputs)	$\overline{CE_L}$ or $\overline{CE_R} \ge V_{IH}$ Active Port Outputs	MIL.	S	—	—	50	170	50	160	50	150	50	150	mA
				L	—	—	50	140	50	130	50	120	50	120	
		Open, f = f_{MAX}[3] $\overline{SEM_L}$ = $\overline{SEM_R} \ge V_{IH}$	COM'L.	S	50	150	50	140	50	130	50	130	50	130	
				L	50	120	50	110	50	100	50	100	50	100	
I_{SB3}	Full Standby Current (Both Ports—All CMOS Level Inputs)	Both Ports $\overline{CE_L}$ and $\overline{CE_R} \ge$ Vcc - 0.2V	MIL.	S	—	—	1.0	30	1.0	30	1.0	30	1.0	30	mA
				L	—	—	0.2	10	0.2	10	0.2	10	0.2	10	
		$V_{IN} \ge$ Vcc - 0.2V or $V_{IN} \le$ 0.2V $\overline{SEM_L}$ = $\overline{SEM_R} \ge$ Vcc - 0.2V, f = 0[3]	COM'L.	S	1.0	15	1.0	15	1.0	15	1.0	15	1.0	15	
				L	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	
I_{SB4}	Full Standby Current (One Port—All CMOS Level Inputs)	One Port $\overline{CE_L}$ or $\overline{CE_R} \ge$ Vcc - 0.2V	MIL.	S	—	—	50	140	50	130	50	120	50	120	mA
				L	—	—	45	110	45	100	45	90	45	90	
		$V_{IN} \ge$ Vcc - 0.2V or $V_{IN} \le$ 0.2V $\overline{SEM_L}$ = $\overline{SEM_R} \ge$ Vcc — 0.2V Active Port Outputs Open, f = f_{MAX}[3]	COM'L.	S	45	130	45	120	45	110	45	110	45	110	
				L	45	110	45	100	45	90	45	90	45	90	

2721 tbl 06

NOTES:
1. "x" in part number indicates power rating (SA or LA).
2. V_{CC} = 5V, T_A = +25°C.
3. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except Output Enable). f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby I_{SB3}.
4. 0°C to +70°C temperature range.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES[1]

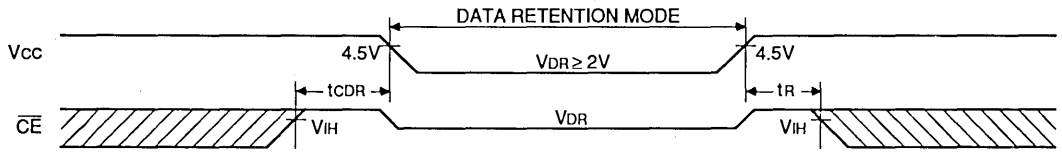
(LA Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	VCC for Data Retention	—		2.0	—	—	V
I_{CCDR}	Data Retention Current	V_{CC} = 2V	MIL.	—	100	4000	µA
		$\overline{CE} \geq V_{HC}$	COM'L.	—	100	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$		0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

2721 tbl 07

NOTES:
1. V_{CC} = 2V, T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



2721 drw 03

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2721 tbl 08

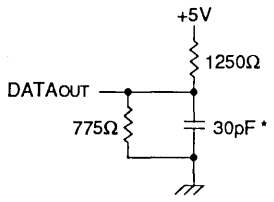
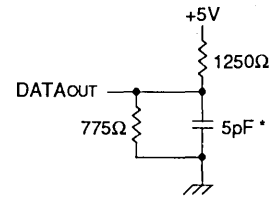


Figure 1. Output Load



2721 drw 04

Figure 2. Output Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})

*Including scope and jig

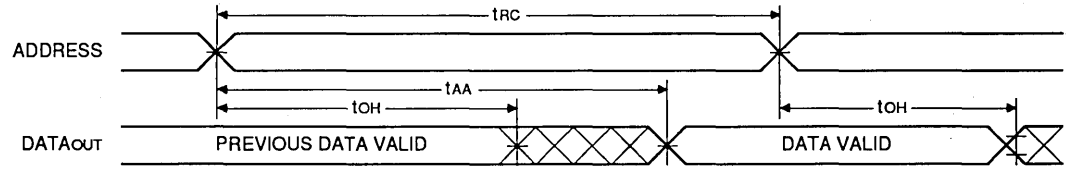
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE(6)

Symbol	Parameter	71342x25(5)		71342x35		71342x45		71342x55		71342x70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
tRC	Read Cycle Time	25	—	35	—	45	—	55	—	70	—	ns
tAA	Address Access Time	—	25	—	35	—	45	—	55	—	70	ns
tACE	Chip Enable Access Time(3)	—	25	—	35	—	45	—	55	—	70	ns
tAOE	Output Enable Access Time	—	15	—	20	—	25	—	30	—	40	ns
tOH	Output Hold from Address Change	0	—	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time(1, 2)	0	—	0	—	5	—	5	—	5	—	ns
tHZ	Output High Z Time(1, 2)	—	15	—	20	—	25	—	30	—	40	ns
tPU	Chip Enable to Power Up Time(2)	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time(2)	—	50	—	50	—	50	—	50	—	50	ns
tSOP	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10	—	15	—	15	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay(4)	—	80	—	80	—	70	—	80	—	90	ns
tDDD	Write Data Valid to Read Data Delay(4)	—	55	—	55	—	55	—	65	—	80	ns

2721 tbl 09

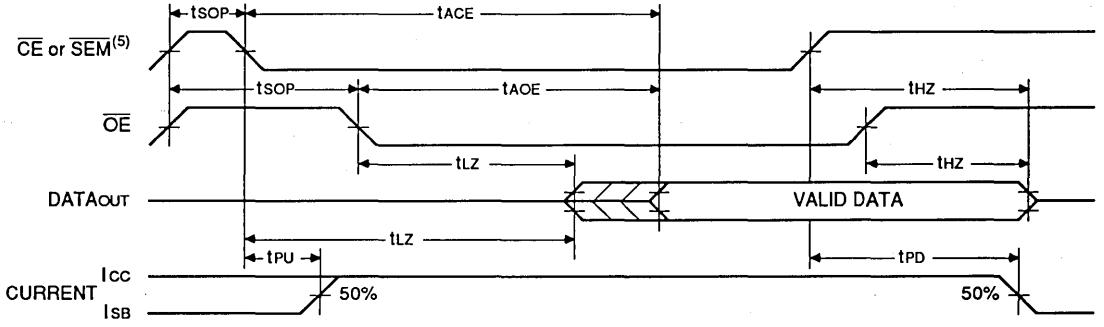
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = VIL, $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH, $\overline{SEM}$ = VIL.
4. Port to Port delay through RAM cells from writing port to a reading port.
5. 0°C to +70°C temperature range only.
6. "x" in part number indicates power rating (SA or LA).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE(1, 2, 4)



2721 drw 05

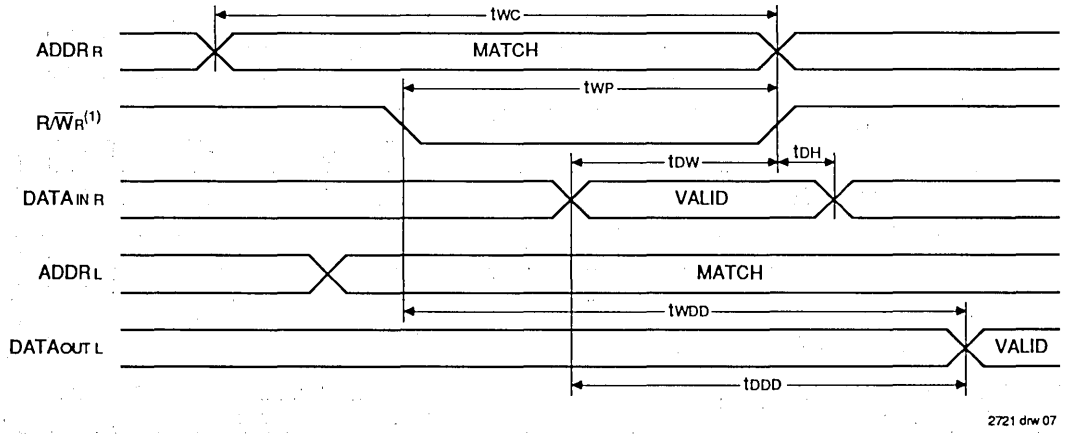
TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE(1, 3)



2721 drw 06

NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = VIL. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = VIL.
5. To access RAM, $\overline{CE}$ = VIL, $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH, $\overline{SEM}$ = VIL.

TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY(1, 2)



NOTES:
1. Write cycle parameters should be adhered to, in order to ensure proper writing.
2. Device is continuously enabled for both ports.

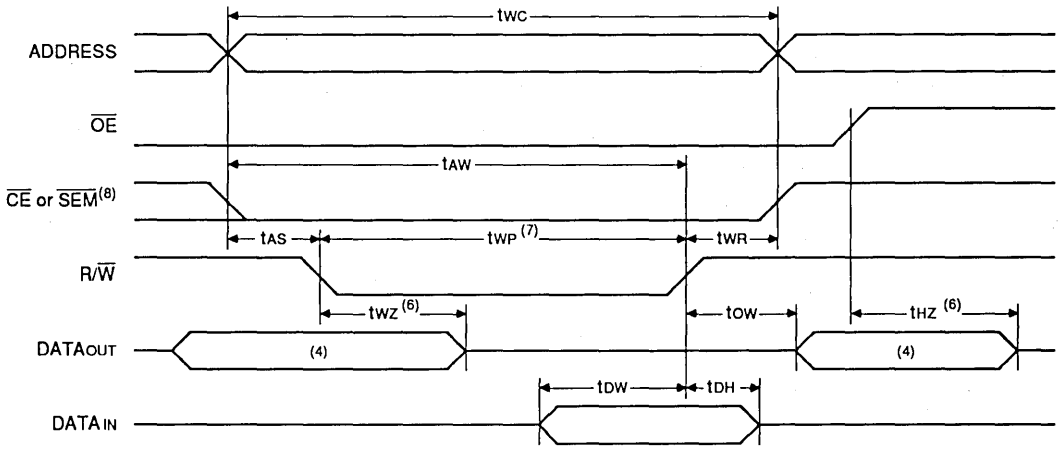
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE(6)

Symbol	Parameter	7134X25(5)		7134X35		7134X45		7134X55		7134X70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE												
tWC	Write Cycle Time	25	—	35	—	45	—	55	—	70	—	ns
tEW	Chip Enable to End of Write(3)	20	—	30	—	40	—	50	—	60	—	ns
tAW	Address Valid to End of Write	20	—	30	—	40	—	50	—	60	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	20	—	30	—	40	—	50	—	60	—	ns
tWR	Write RecoveryTime	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	15	—	20	—	20	—	25	—	30	—	ns
tHZ	Output High Z Time(1, 2)	—	15	—	20	—	20	—	25	—	30	ns
tDH	Data Hold Time(4)	0	—	3	—	3	—	3	—	3	—	ns
tWZ	Write Enabled to Output in High Z(1, 2)	—	15	—	20	—	20	—	25	—	30	ns
tOW	Output Active from End of Write(1, 2, 4)	3	—	3	—	3	—	3	—	3	—	ns
tSWR	SEM Flag Write to Read Time	10	—	10	—	10	—	10	—	10	—	ns
tSPS	SEM Flag Contention Window	10	—	10	—	10	—	10	—	10	—	ns

2721 tbl 10

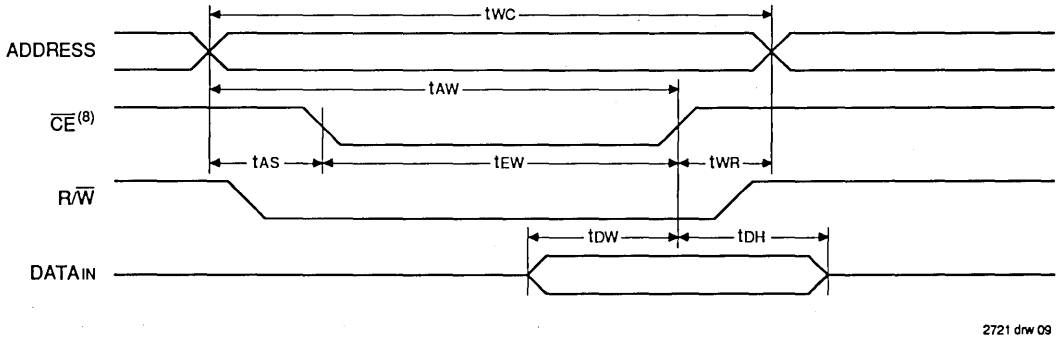
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = VIL, $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH, $\overline{SEM}$ = VIL. This condition must be valid for the entire tEW time.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
5. 0°C to +70°C temperature range only.
6. "X" in part number indicates power rating (SA or LA).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1, 2, 3, 7)



2721 drw 08

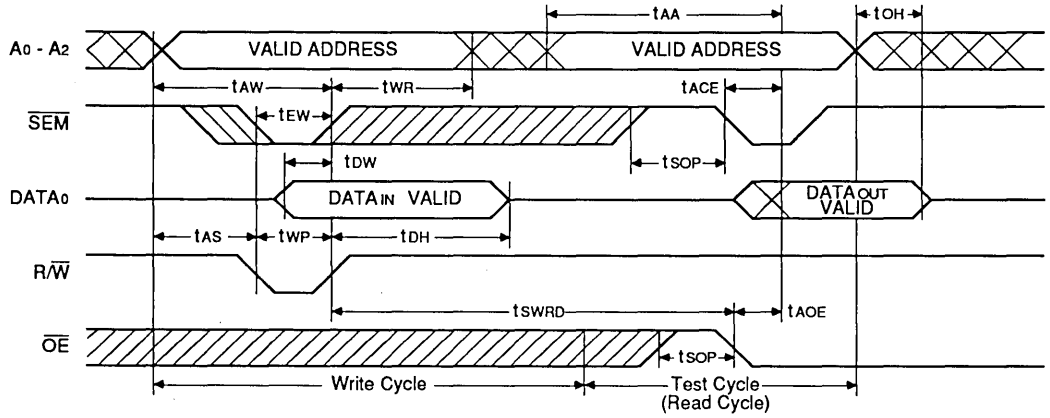
TIMING WAVEFORM OF WRITE CYCLE NO. 1, $\overline{CE}$ CONTROLLED TIMING(1, 2, 3, 5)



2721 drw 09

NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ or $\overline{SEM}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
8. To access RAM, $\overline{CE}$ = VIL, $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH, $\overline{SEM}$ = VIL. Either condition must be valid for the entire tEW time.

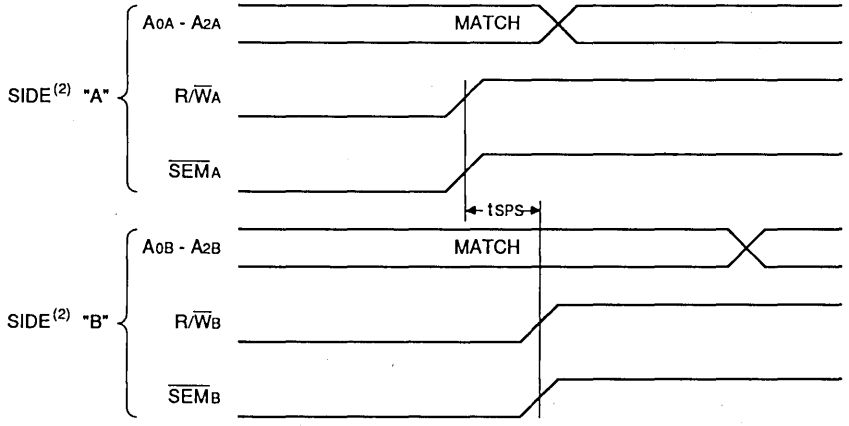
TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



2721 drw 10

NOTE:
1. $\overline{CE}$ = VIH for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE CONTENTION[1, 3, 4]



2721 drw 11

NOTES:
1. DOR = DOL = VIL, $\overline{CE}_R$ = $\overline{CE}_L$ = VIH, Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. Either side "A" = left and side "B" = right, or side "A" = right and side "B" = left.
3. This parameter is measured from the point where R/WA or $\overline{SEM}_A$ goes high until R/WB or $\overline{SEM}_B$ goes high.
4. If tSPS is violated, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

FUNCTIONAL DESCRIPTION

The IDT71342 is an extremely fast dual-port 4K x 8 CMOS static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the dual-port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the dual-port RAM or any other shared resource.

The dual-port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS static RAMs and can be read from or written to at the same time, with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the dual-port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the dual-port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Table 1 where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT71342 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT71342's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT71342 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the dual-port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that a shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor had set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT71342 in a separate memory space from the dual-port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard static RAM. Each of the flags has a unique address which can be accessed by either side through the address pins A_0–A_2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D_0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other (see Table II). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence of WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as a one, a fact which the processor will verify by the subsequent read (see Table II). As an example, assume a processor writes a zero in the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume

control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during a subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 3. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

TABLE I — NON-CONTENTION READ/WRITE CONTROL

Left or Right Port(1)					
R/$\overline{W}$	$\overline{CE}$	$\overline{SEM}$	$\overline{OE}$	D_{0-7}	Function
X	H	H	X	Z	Port Disabled and in Power Down Mode
H	H	L	L	$DATA_{OUT}$	Data in Semaphore Flag Output on Port
X	X	X	H	Z	Output Disabled
↑	H	L	X	$DATA_{IN}$	Port Data Bit D0 Written Into Semaphore Flag
H	L	H	L	$DATA_{OUT}$	Data in Memory Output on Port
L	L	H	X	$DATA_{IN}$	Data on Port Written Into Memory
X	L	L	X	—	Not Allowed

2721 tbl 11

NOTE:
1. $A_{OL} = A_{10L} \neq A_{OR} - A_{10R}$
   H = HIGH, L = LOW, X = Don't Care, Z = High Impedance
   ↑ = Low-to-High transition.

TABLE II — EXAMPLE SEMAPHORE PROCUREMENT SEQUENCE(1)

Function	$D_0 - D_7$ Left	$D_0 - D_7$ Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left side has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

2721 tbl 12

NOTE:
1. This table denotes a sequence of events for only one of the eight semaphores on the IDT71342.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen. Code integrity is of the utmost importance when semaphores are used instead of slower, more restrictive hardware intensive schemes.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES–Some examples

Perhaps the simplest application of semaphores is their application as resource markers for the IDT71342's dual-port RAM. Say the 4K x 8 RAM was to be divided into two 2K x 8 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of the memory.

To take a resource, in this example the lower 2K of dual-port RAM, the processor on the left port could write and then read a zero into Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 2K. Meanwhile, the right processor would attempt to perform the same function. Since this processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 2K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 2K blocks of dual-port RAM with each other.

The blocks do not have to by any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the dual-port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices had determined which memory area was "off limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

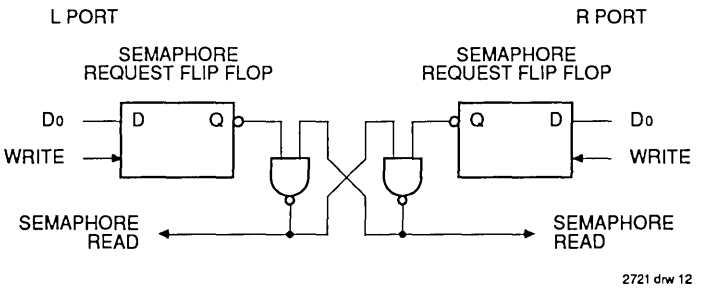
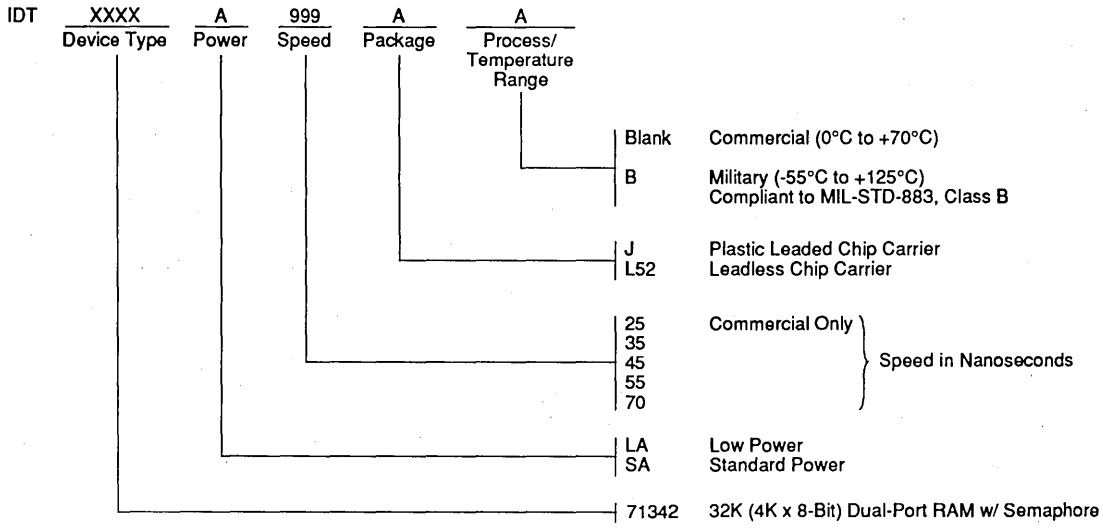


Figure 3. IDT71342 Semaphore Logic

ORDERING INFORMATION



2721 drw 13

Integrated Device Technology, Inc.

HIGH SPEED 36K (4K x 9-BIT) DUAL-PORT RAM

ADVANCE INFORMATION
IDT7014S
IDT7014L

FEATURES:

- High-speed access
  - — Military: 20/25/35/45ns (max.)
  - — Commercial: 15/20/25/35ns (max.)
- Low-power operation
  - — IDT7014S
    Active: 375mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7134L
    Active: 375mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in several popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7014 is an extremely high-speed 4K x 9 dual-port static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when both sides simultaneously access the same dual-port RAM location.

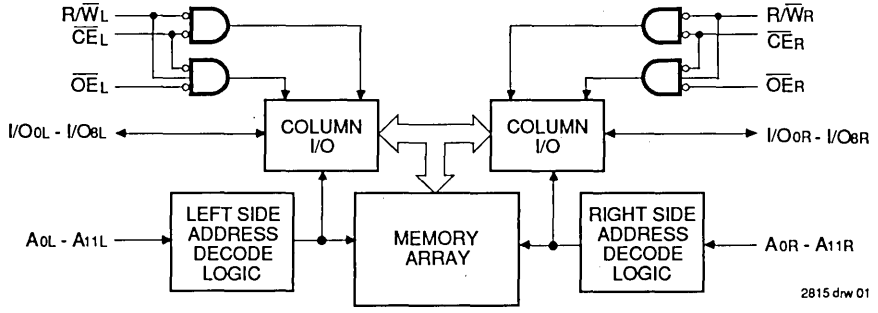
The IDT7014 provides two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT 7014 utilities a 9-bit wide data path to allow for control and parity bits at the user's option. This feature is especiall useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

Fabricated using IDT's BiCEMOS™ high-performance technology, these dual-ports typically operate on only 375mW of power at maximum access times as fast as 15ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 300µW from a 2V battery.

The IDT7014 is packaged on a 52-pin LCC or 52-pin PLCC. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



7

BiCEMOS is a trademark of Integrated Device Technology, Inc.

Integrated Device Technology, Inc.

HIGH-SPEED 4K x 16 DUAL-PORT STATIC RAM

PRELIMINARY
IDT7024S/L

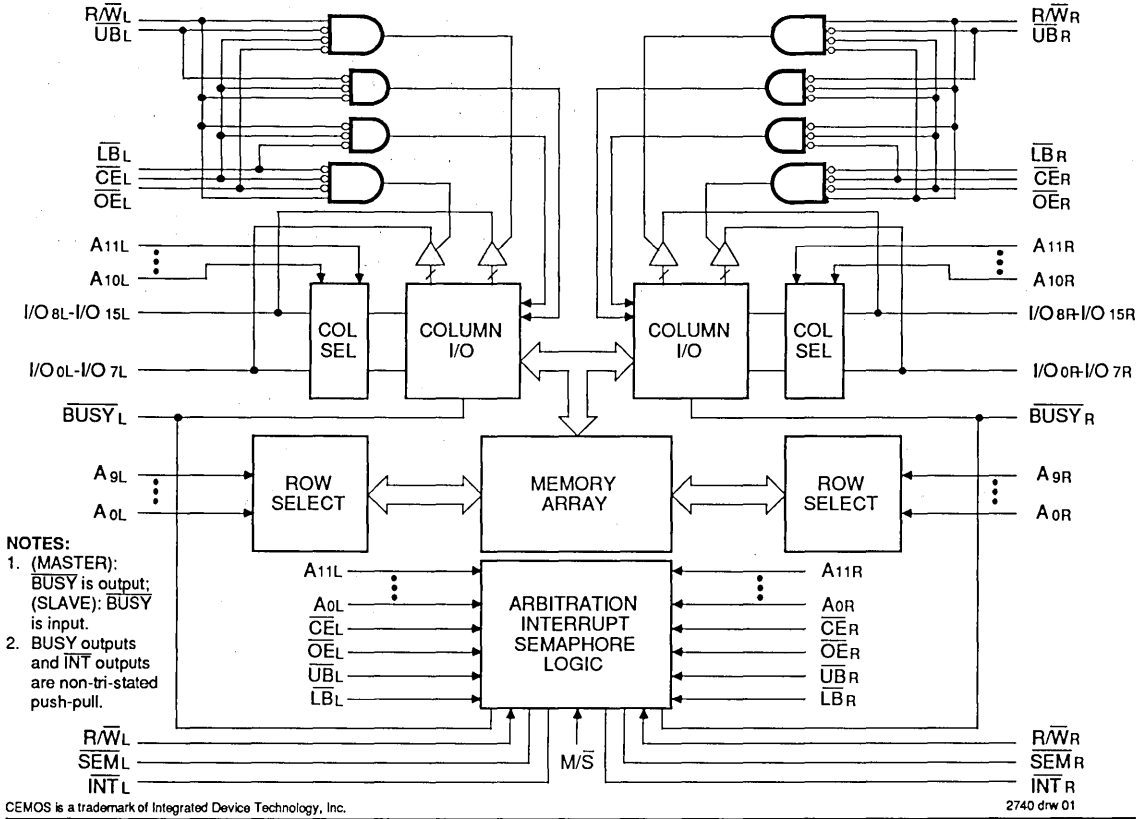
FEATURES:

- True dual-ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Military: 35/45/55/70ns (max.)
  - — Commercial: 25/30/35/45/55ns (max.)
- Low-power operation
  - — IDT7024S
    Active: —mW (typ.)
    Standby: —mW (typ.)
  - — IDT7024L
    Active: —mW (typ.)
    Standby: —mW (typ.)
- Separate upper-byte and lower-byte control for multiplexed bus compatibility
- IDT7024 easily expands data bus width to 32 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- Interrupt Flag
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL compatible, single 5V (±10%) power supply
- Available in 84-pin PGA, quad flatpack and PLCC

DESCRIPTION:

The IDT7024 is a high-speed 4K x 16 dual-port static RAM. The IDT7024 is designed to be used as a stand-alone 64K-bit dual-port RAM or as a combination MASTER/SLAVE dual-port RAM for 32-bit-or-more word systems. Using the IDT

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.
2. BUSY outputs and $\overline{INT}$ outputs are non-tri-stated push-pull.

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2740 drw 01

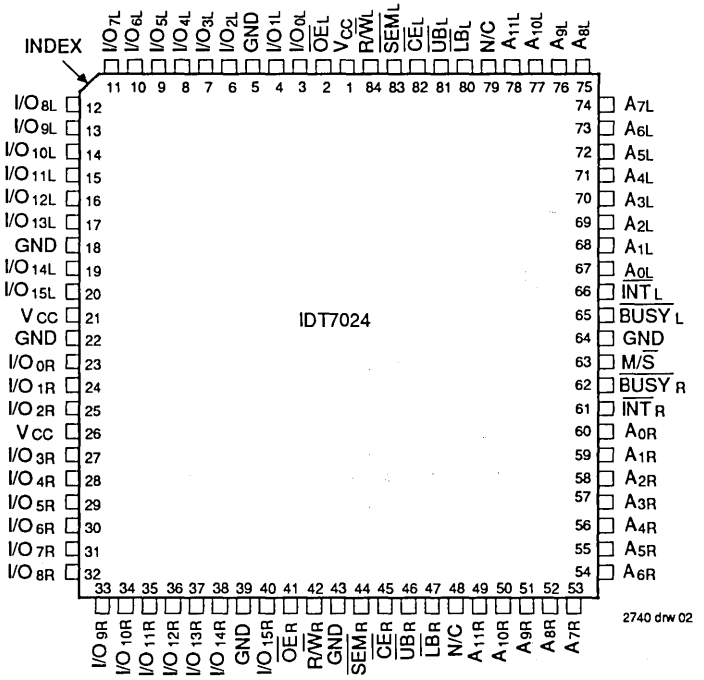
MASTER/SLAVE dual-port RAM approach in 32-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only —mW or power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability with each port typically consuming —mW from a 2V battery.

The IDT7024 is packaged in plastic as well as ceramic 84-pin PGA and 84-pin quad flatpack and PLCC. The military devices are processed 100% in compliance to the test methods of MIL-STD-883, Method 5004.

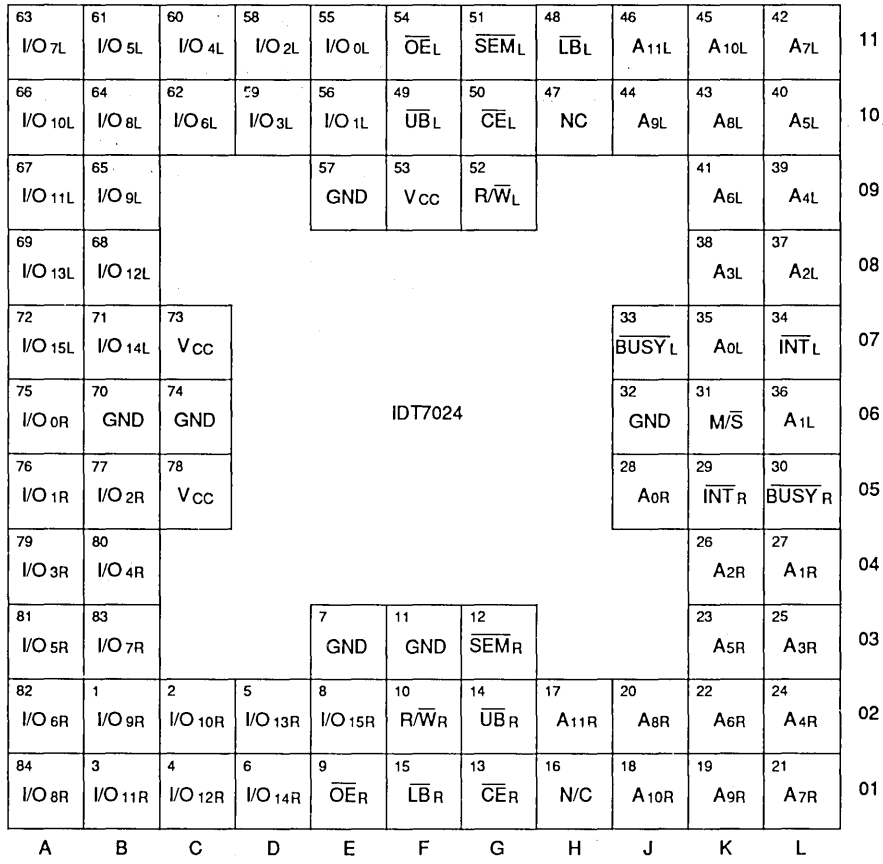
PIN CONFIGURATIONS



PLCC/FLATPACK
TOP VIEW

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.

PIN CONFIGURATIONS (Continued)



2740 drw 03

84-PIN PGA
TOP VIEW

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.

PIN NAMES

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} - A_{11L}$	$A_{0R} - A_{11R}$	Address
$I/O_{0L} - I/O_{15L}$	$I/O_{0R} - I/O_{15R}$	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

2740 tbl 18

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

Inputs[1]						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-15	I/O0-7	Mode
H	X	X	X	X	H	Hi-Z	Hi-Z	Deselected: Power Down
X	X	X	H	H	H	Hi-Z	Hi-Z	Both Bytes Deselected: Power Down
L	L	X	L	H	H	DATAIN	Hi-Z	Write to Upper Byte Only
L	L	X	H	L	H	Hi-Z	DATAIN	Write to Lower Byte Only
L	L	X	L	L	H	DATAIN	DATAIN	Write to Both Bytes
L	H	L	L	H	H	DATAOUT	Hi-Z	Read Upper Byte Only
L	H	L	H	L	H	Hi-Z	DATAOUT	Read Lower Byte Only
L	H	L	L	L	H	DATAOUT	DATAOUT	Read Both Bytes
X	X	H	X	X	X	Hi-Z	Hi-Z	Outputs Disabled

NOTE:
1. $A_{0L} - A_{11L} \neq A_{0R} - A_{11R}$

2740 tbl 01

TRUTH TABLE: SEMAPHORE READ/WRITE CONTROL

Inputs						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-15	I/O0-7	Mode
H	H	L	X	X	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
X	H	L	H	H	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
H	↓	X	X	X	L	DATAIN	DATAIN	Write DIN0 into Semaphore Flag
X	↓	X	H	H	L	DATAIN	DATAIN	Write DIN0 into Semaphore Flag
L	X	X	L	X	L	—	—	Not Allowed
L	X	X	X	L	L	—	—	Not Allowed

2740 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2740 tbl 04

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Output Capacitance	VOUT = 0V	11	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

2740 tbl 03

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2740 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE:
1. $V_{IL} \geq$ -3.0V for pulse width less than 20ns.

2740 tbl 06

7

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7024S		IDT7024L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[5]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2740 tbl 07

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7024X25 COM'L ONLY		7024X30 COM'L ONLY		7024X35		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \le V_{IL}$, Outputs Open $\overline{SEM} \ge V_{IH}$ f = f_{MAX}[3]	MIL.	S	—	—	—	—	—	400	mA
				L	—	—	—	—	—	340	
			COM'L.	S	—	360	—	350	—	340	
				L	—	310	—	300	—	290	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_R = \overline{CE}_L \ge V_{IH}$ $\overline{SEM}_R = \overline{SEM}_L \ge V_{IH}$ f = f_{MAX}[3]	MIL.	S	—	—	—	—	—	85	mA
				L	—	—	—	—	—	65	
			COM'L.	S	—	70	—	70	—	70	
				L	—	50	—	50	—	50	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \ge V_{IH}$ Active Port Outputs Open f = f_{MAX}[3] $\overline{SEM}_R = \overline{SEM}_L \ge V_{IH}$	MIL.	S	—	—	—	—	—	290	mA
				L	—	—	—	—	—	250	
			COM'L.	S	—	250	—	250	—	240	
				L	—	220	—	215	—	210	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \ge V_{CC}$ - 0.2V $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le$ 0.2V, f = 0[4] $\overline{SEM}_R = \overline{SEM}_L \ge V_{CC}$ - 0.2V	MIL.	S	—	—	—	—	—	30	mA
				L	—	—	—	—	—	10	
			COM'L.	S	—	15	—	15	—	15	
				L	—	5	—	5	—	5	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ - 0.2V $\overline{SEM}_R = \overline{SEM}_L \ge V_{CC}$ - 0.2V $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le$ 0.2V Active Port Outputs Open, f = f_{MAX}[3]	MIL.	S	—	—	—	—	—	260	mA
				L	—	—	—	—	—	215	
			COM'L.	S	—	230	—	230	—	220	
				L	—	190	—	190	—	180	

NOTES:

2740 tbl 08

1. X in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C.
3. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. At $V_{CC} \le$ 1.0V input leakages are undefined.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1](Continued) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7024X45 Typ.[2]	7024X45 Max.	7024X55 Typ.[2]	7024X55 Max.	7024X70 MIL ONLY Typ.[2]	7024X70 MIL ONLY Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \le V_{IL}$, Outputs Open, $\overline{SEM} \ge V_{IH}$, $f = f_{MAX}$[3]	MIL.	S	—	400	—	395	—	390	mA
				L	—	340	—	335	—	330	
			COM'L.	S	—	340	—	335	—	—	
				L	—	290	—	285	—	—	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R \ge V_{IH}$, $\overline{SEM}_R = \overline{SEM}_L \ge V_{IH}$, $f = f_{MAX}$[3]	MIL.	S	—	85	—	85	—	85	mA
				L	—	65	—	65	—	65	
			COM'L.	S	—	70	—	70	—	—	
				L	—	50	—	50	—	—	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_R$ or $\overline{CE}_L \ge V_{IH}$, Active Port Outputs Open, $f = f_{MAX}$[3], $\overline{SEM}_R = \overline{SEM}_L \ge V_{IH}$	MIL.	S	—	290	—	290	—	290	mA
				L	—	250	—	250	—	250	
			COM'L.	S	—	240	—	240	—	—	
				L	—	210	—	210	—	—	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \ge V_{CC}$ - 0.2V, $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le 0.2V$, $f = 0$[4], $\overline{SEM}_R = \overline{SEM}_L \ge V_{CC}$ - 0.2V	MIL.	S	—	30	—	30	—	30	mA
				L	—	10	—	10	—	10	
			COM'L.	S	—	15	—	15	—	—	
				L	—	5	—	5	—	—	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ - 0.2V, $\overline{SEM}_R = \overline{SEM}_L \ge V_{CC}$ - 0.2V	MIL.	S	—	260	—	260	—	260	mA
				L	—	215	—	215	—	215	
		$V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le 0.2V$, Active Port Outputs Open, $f = f_{MAX}$[3]	COM'L.	S	—	220	—	220	—	—	
				L	—	180	—	180	—	—	

NOTES:
2740 tbl 08

1. X in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C.
3. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. At $V_{CC} \le 1.0V$ input leakages are undefined.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES (L Version Only)

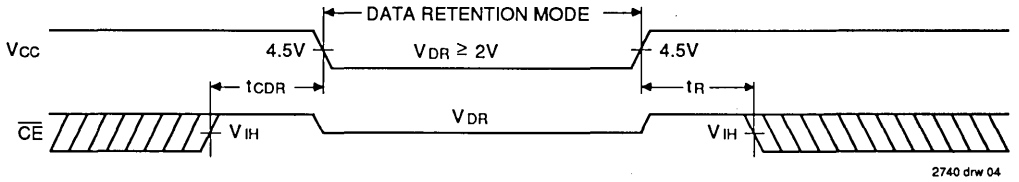
(V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	Vcc for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$	MIL.	—	—	4000	µA
		$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	COM'L.	—	—	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:
1. T_A = +25°C, V_{CC} = 2V
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

2740 tbl 09

DATA RETENTION WAVEFORM

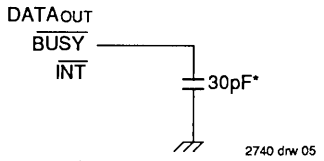


2740 drw 04

AC TEST CONDITIONS

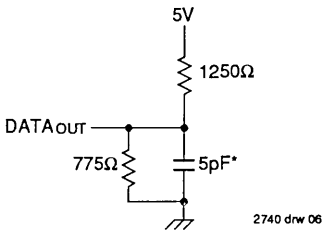
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2740 tbl 10



2740 drw 05

Figure 1. Output Load



2740 drw 06

Figure 2. Output Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})

* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[4]

Symbol	Parameter	IDT7024X25 COM'L ONLY		IDT7024X30 COM'L ONLY		IDT7024X35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
tRC	Read Cycle Time	25	—	30	—	35	—	ns
tAA	Address Access Time	—	25	—	30	—	35	ns
tACE	Chip Enable Access Time[3]	—	25	—	30	—	35	ns
tABE	Byte Enable Access Time[3]	—	25	—	30	—	35	ns
tAOE	Output Enable Access Time	—	13	—	15	—	20	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low Z Time[1, 2]	3	—	3	—	3	—	ns
tHZ	Output High Z Time[1, 2]	—	15	—	15	—	15	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	50	—	50	—	50	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	12	—	15	—	15	—	ns

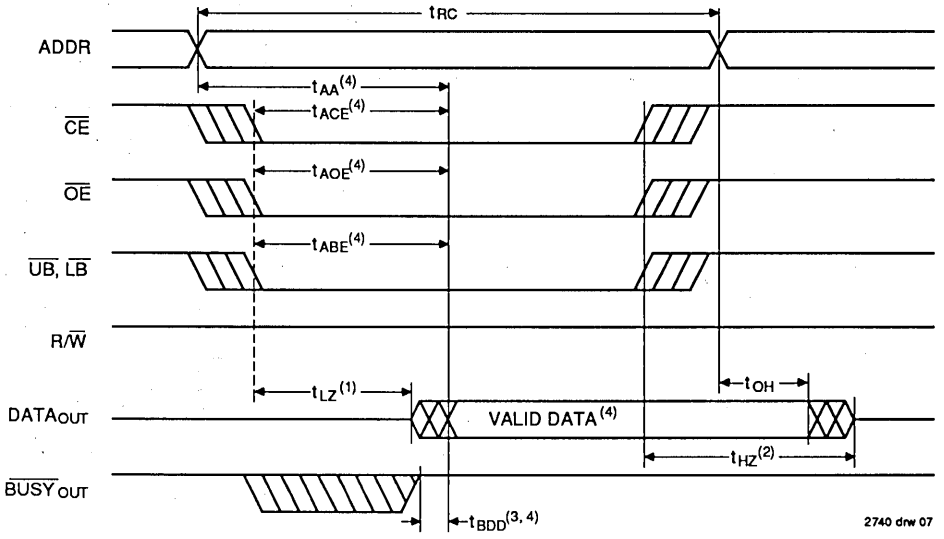
Symbol	Parameter	IDT7024X45		IDT7024X55		IDT7024X70 MIL ONLY		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
tRC	Read Cycle Time	45	—	55	—	70	—	ns
tAA	Address Access Time	—	45	—	55	—	70	ns
tACE	Chip Enable Access Time[3]	—	45	—	55	—	70	ns
tABE	Byte Enable Access Time[3]	—	45	—	55	—	70	ns
tAOE	Output Enable Access Time	—	25	—	30	—	35	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low Z Time[1, 2]	5	—	5	—	5	—	ns
tHZ	Output High Z Time[1, 2]	—	20	—	25	—	30	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	50	—	50	—	50	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	15	—	ns

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = L, $\overline{UB}$ or $\overline{LB}$ = L, $\overline{SEM}$ = H.
4. X in part numbers indicates power rating (S or L).

2740 tbl 11

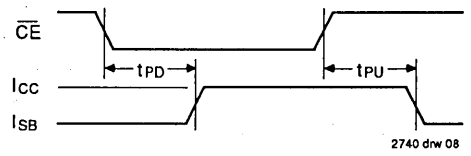
7

WAVEFORM OF READ CYCLES(5)



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$, $\overline{CE}$, $\overline{LB}$, or $\overline{UB}$.
2. Timing depends on which signal is de-asserted firs $\overline{CE}$, $\overline{OE}$, $\overline{LB}$, or $\overline{UB}$.
3. Required only if busy logic is being used to prevent read data corruption, during simultaneous accesses to the same location, in masters and master-slave width expansions.
4. Start of valid data depends on which timing becomes effective last tABE, tAOE, tACE, tAA or tBDD.
5. $\overline{SEM}$ = H.

TIMING OF POWER-UP POWER-DOWN



AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (5)

Symbol	Parameter	IDT7024X25 COM'L ONLY		IDT7024X30 COM'L ONLY		IDT7024X35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
tWC	Write Cycle Time	25	—	30	—	35	—	ns
tEW	Chip Enable to End of Write(3)	20	—	25	—	30	—	ns
tAW	Address Valid to End of Write	20	—	25	—	30	—	ns
tAS	Address Set-up Time(3)	0	—	0	—	0	—	ns
tWP	Write Pulse Width	20	—	25	—	30	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	15	—	20	—	25	—	ns
tHZ	Output High Z Time(1, 2)	—	15	—	15	—	15	ns
tDH	Data Hold Time(4)	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High Z(1, 2)	—	15	—	15	—	15	ns
tOW	Output Active from End of Write(1, 2, 4)	0	—	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	10	—	10	—	10	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	10	—	10	—	10	—	ns

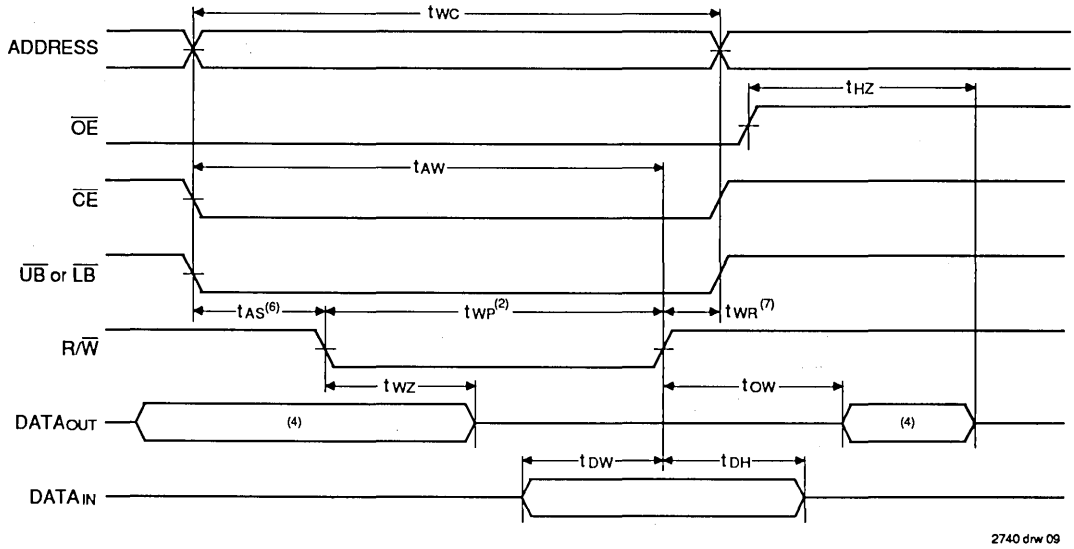
Symbol	Parameter	IDT7024X45		IDT7024X55		IDT7024X70 MIL. ONLY		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
tWC	Write Cycle Time	45	—	55	—	70	—	ns
tEW	Chip Enable to End of Write(3)	40	—	45	—	50	—	ns
tAW	Address Valid to End of Write	40	—	45	—	50	—	ns
tAS	Address Set-up Time(3)	0	—	0	—	0	—	ns
tWP	Write Pulse Width	35	—	40	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	25	—	30	—	40	—	ns
tHZ	Output High Z Time(1, 2)	—	20	—	25	—	30	ns
tDH	Data Hold Time(4)	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High Z(1, 2)	—	20	—	25	—	30	ns
tOW	Output Active from End of Write(1, 2, 4)	0	—	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	10	—	10	—	10	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	10	—	10	—	10	—	ns

NOTES:

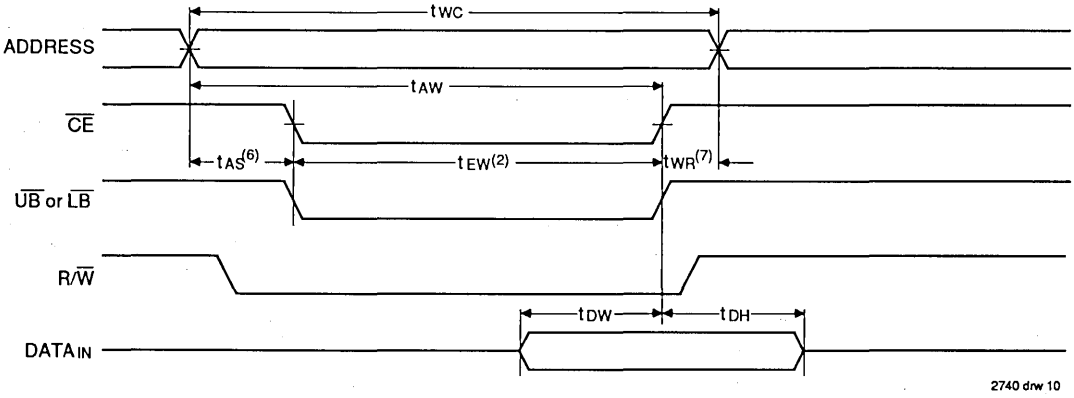
2740 tbl 12

1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = L, $\overline{UB}$ or $\overline{LB}$ = L, $\overline{SEM}$ = H. To access semaphore, $\overline{CE}$ = H and $\overline{SEM}$ = L. Either condition must be valid for the entire tEW time.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
5. X in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,3,5,8)

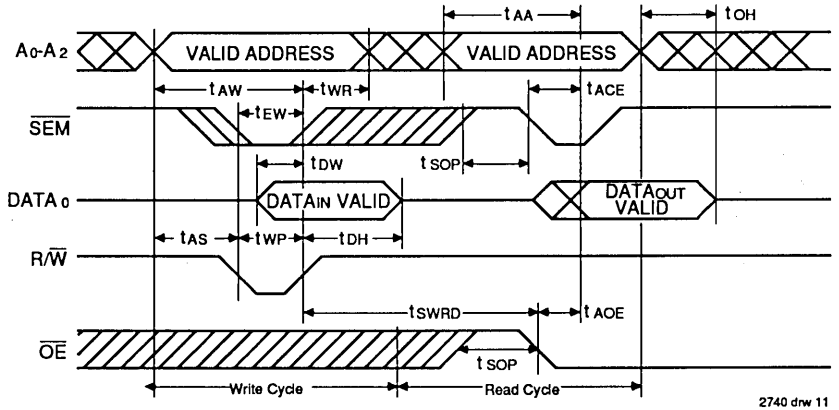


TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$ CONTROLLED TIMING(1,3,5,8)



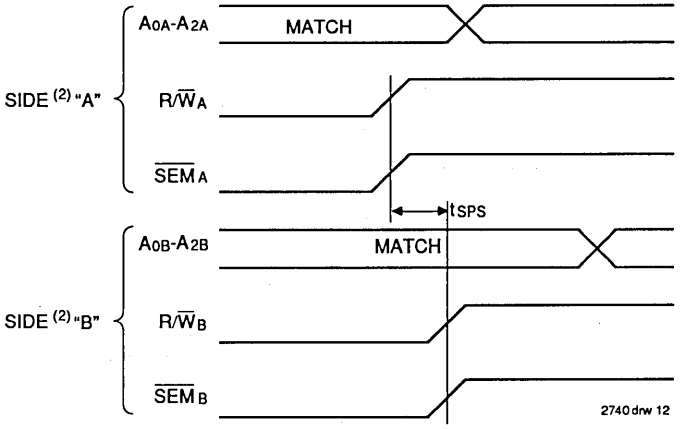
NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{UB}$ or $\overline{LB}$ and a low $\overline{CE}$ and a low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is low during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



NOTE:
1. $\overline{CE}$ = H for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE WRITE CONTENTION[1,3,4]



NOTES:
1. D_{OR} = D_{OL} = L, $\overline{CE}_R$ = $\overline{CE}_L$ = H, Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from R/$\overline{W}$A or $\overline{SEM}$A going high to R/$\overline{W}$B or $\overline{SEM}$B going high.
4. If t_{SPS} is violated, the semaphore will fall positively to one side or the other, but there is not guarantee which side will obtain the flag.

7

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(6)

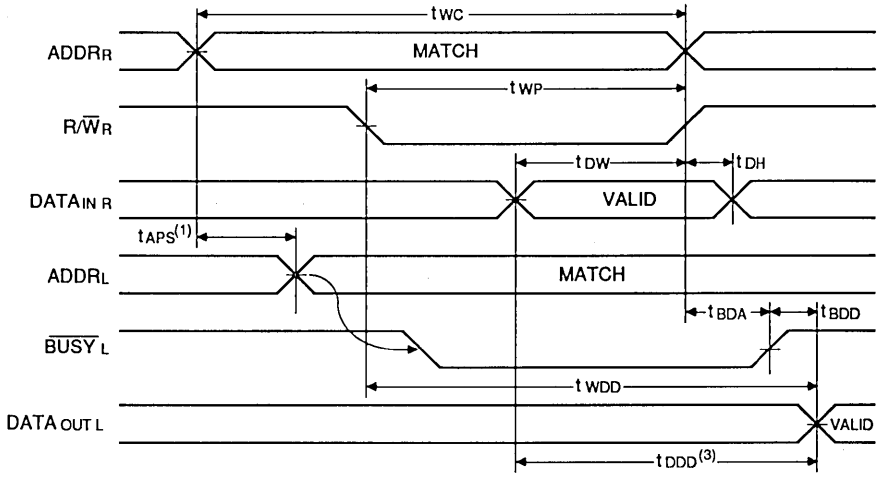
Symbol	Parameter	IDT7024X25 COM'L ONLY		IDT7024X30 COM'L ONLY		IDT7024X35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
BUSY TIMING (M/$\overline{S}$ = H)								
tBAA	$\overline{BUSY}$ Access Time to Address	—	25	—	30	—	35	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	20	—	25	—	30	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable or Byte Enable	—	20	—	25	—	30	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable or Byte Disable	—	17	—	20	—	25	ns
tAPS	Arbitration Priority Set-up Time(2)	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data(5)	—	Note 3	—	Note 3	—	Note 3	ns
BUSY TIMING (M/$\overline{S}$ = L)								
tWB	$\overline{BUSY}$ Input to Write(4)	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$(5)	17	—	20	—	25	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay(7)	—	50	—	55	—	60	ns
tDDD	Write Data Valid to Read Data Delay(7)	—	35	—	40	—	45	ns

Symbol	Parameter	IDT7024X45		IDT7024X55		IDT7024X70 MIL. ONLY		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
BUSY TIMING (M/$\overline{S}$ = H)								
tBAA	$\overline{BUSY}$ Access Time to Address	—	35	—	45	—	45	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	30	—	40	—	40	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable or Byte Enable	—	30	—	40	—	40	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable or Byte Disable	—	25	—	35	—	35	ns
tAPS	Arbitration Priority Set-up Time(2)	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data(5)	—	Note 3	—	Note 3	—	Note 3	ns
BUSY TIMING (M/$\overline{S}$ = L)								
tWB	$\overline{BUSY}$ Input to Write(4)	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$(5)	25	—	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay(7)	—	70	—	80	—	95	ns
tDDD	Write Data Valid to Read Data Delay(7)	—	55	—	65	—	80	ns

NOTES: 2740 tbl 13

1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (M/$\overline{S}$ = H)".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
4. To ensure that the write cycle is inhibited during contention.
5. To ensure that a write cycle is completed after contention.
6. "x" is part numbers indicates power rating (S or L).
7. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (M/$\overline{S}$ = L)".

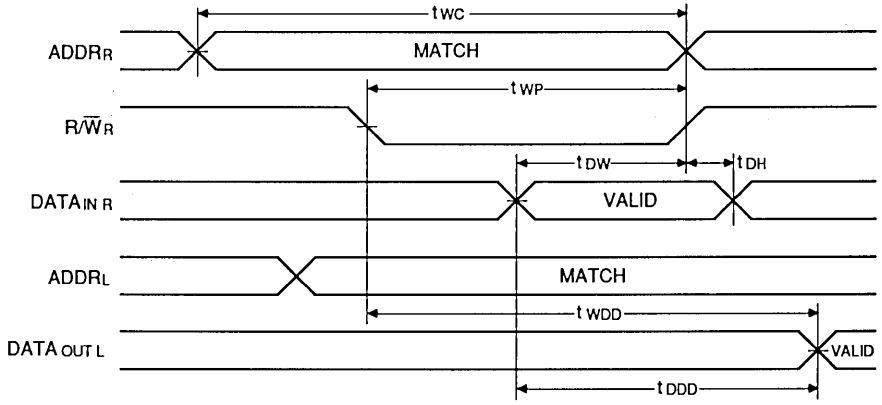
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$[2] (M/$\overline{S}$ = H)



2740 drw 13

NOTES:
1. To ensure that the earlier of the two ports wins.
2. $\overline{CE}_L$ = $\overline{CE}_R$ = L
3. $\overline{OE}$ = L for the reading port.

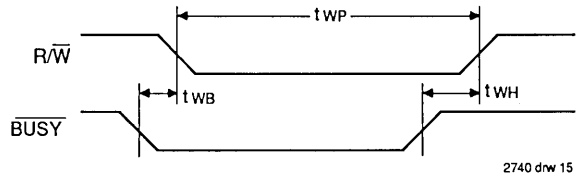
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY[1,2] (M/$\overline{S}$ = L)



2740 drw 14

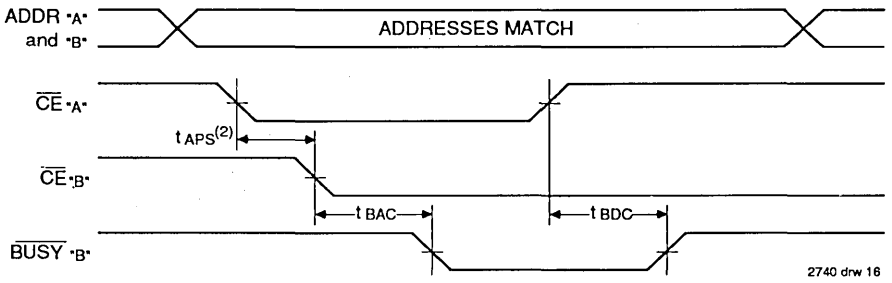
NOTES:
1. $\overline{BUSY}$ input equals H for the writing port.
2. $\overline{CE}_L$ = $\overline{CE}_R$ = L

TIMING WAVEFORM OF SLAVE WRITE (M/$\overline{S}$ = L)

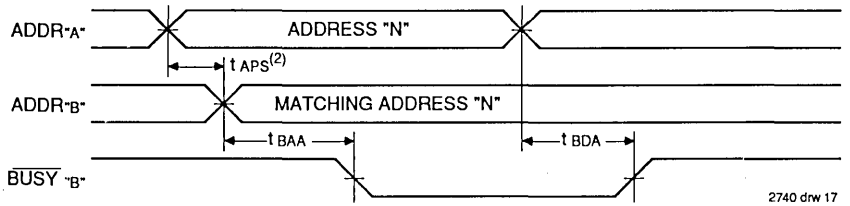


2740 drw 15

WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING[1] (M/$\overline{S}$ = H)



WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING[1](M/$\overline{S}$ = H)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If tAPS is violated, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1]

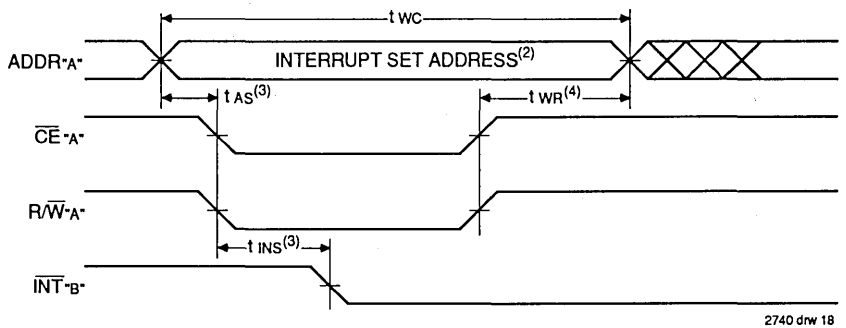
Symbol	Parameter	IDT7024X25 COM'L ONLY		IDT7024X30 COM'L ONLY		IDT7024X35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	20	—	25	—	30	ns
tINR	Interrupt Reset Time	—	20	—	25	—	30	ns

Symbol	Parameter	IDT7024X45		IDT7024X55		IDT7024X70 MIL. ONLY		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	35	—	40	—	50	ns
tINR	Interrupt Reset Time	—	35	—	40	—	50	ns

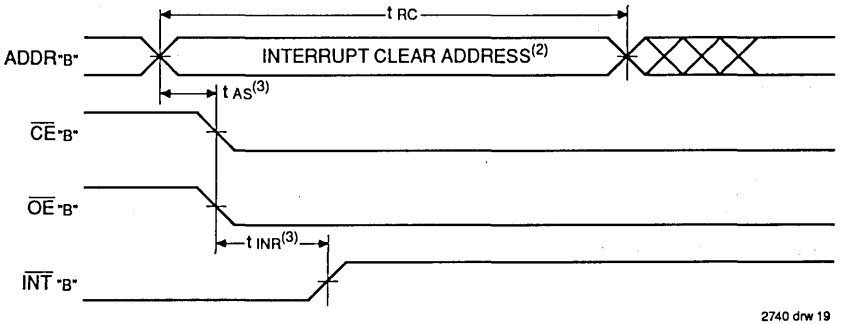
NOTE:
1. "x" in part numbers indicates power rating (S or L).

2740 tbl 14

WAVEFORM OF INTERRUPT TIMING[1]



2740 drw 18



2740 drw 19

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See Interrupt truth table.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable signal is de-asserted first.

TRUTH TABLES

TRUTH TABLE I — INTERRUPT FLAG[1]

Left Port					Right Port					
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{11L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R}-A_{11R}	$\overline{INT}_R$	Function
L	L	X	FFF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	FFF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	FFE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	FFE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

NOTES: 2740 tbl 15

1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then no change.
3. If $\overline{BUSY}_R$ = L, then no change.

TRUTH TABLE II — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{11L} A_{0R}-A_{11R}	$\overline{BUSY}_L$[1]	$\overline{BUSY}_R$[1]	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit[3]

NOTES: 2740 tbl 16

1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}_X$ outputs on the IDT7024 are push pull, not open drain outputs. On slaves the $\overline{BUSY}_X$ input internally inhibits writes.
2. L if the inputs to the opposite port were stable prior to the address and enable inputs of this port. H if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = Low will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs cannot be low simultaneouly.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving low regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving low regardless of actual logic level on the pin.

TRUTH TABLE III — EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE[1]

Functions	D_0 - D_{15} Left	D_0 - D_{15} Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Right port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

NOTE: 2740 tbl 17

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT7024.

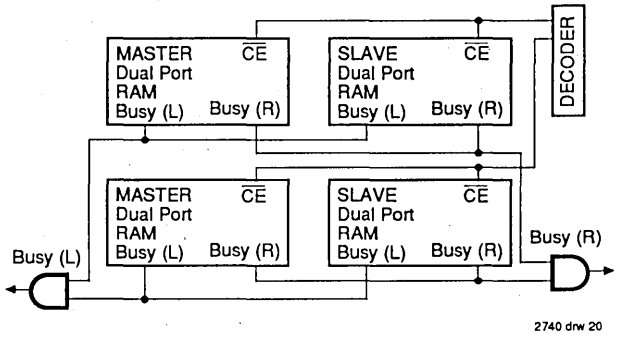


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7024 RAMs.

FUNCTIONAL DESCRIPTION

The IDT7024 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7024 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is set when the right port writes to memory location FFE (HEX). The left port clears the interrupt by reading address location FFE. Likewise, the right port interrupt flag ($\overline{INT}_R$) is set when the left port writes to memory location FFF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location FFF. The message (16 bits) at FFE or FFF is user-defined. If the interrupt function is not used, address locations FFE and FFF are not used as mail boxes, but as part of the random access memory. Refer to Table I for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by placing the part in slave mode with the $M/\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low.

The busy outputs on the IDT 7024 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT7024 RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT7024 RAM the busy pin is an output if the part is used as a master ($M/\overline{S}$ pin = H), and the busy pin is an input if the part used as a slave ($M/\overline{S}$ pin = L).

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with either the $R/\overline{W}$ signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

SEMAPHORES

The IDT7024 is an extremely fast dual-port 4K x 16 CMOS static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the dual-port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the dual-port RAM or any other shared resource.

The dual-port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the dual-port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the dual-port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT7024 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT7024's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT7024 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the dual-port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT7024 in a separate memory space from the dual-port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0 – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin Do is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussing on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from

that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—SOME EXAMPLES

Perhaps the simplest application of semaphores is their application as resource markers for the IDT7024's dual-port RAM. Say the 4K x 16 RAM was to be divided into two 2K x 16 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 2K of dual-port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 2K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 2K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 2K blocks of dual-port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the dual-port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

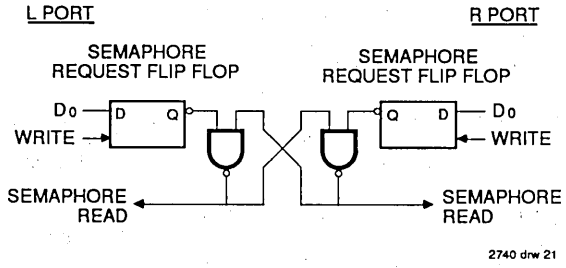
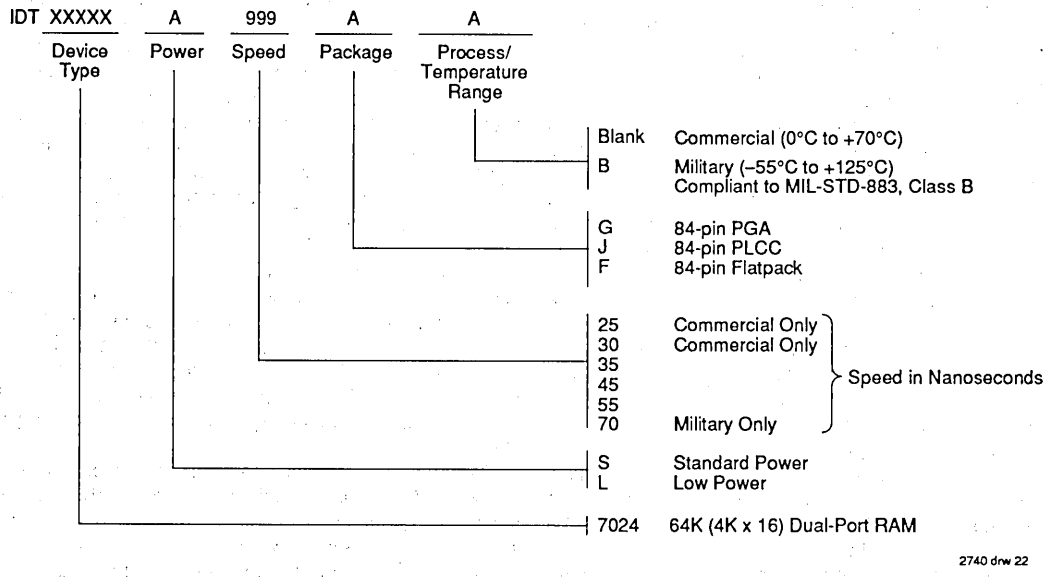


Figure 4. IDT7024 Semaphore Logic

ORDERING INFORMATION



Integrated Device Technology, Inc.

HIGH-SPEED 8K x 8 DUAL-PORT STATIC RAM

PRELIMINARY
IDT7005S/L

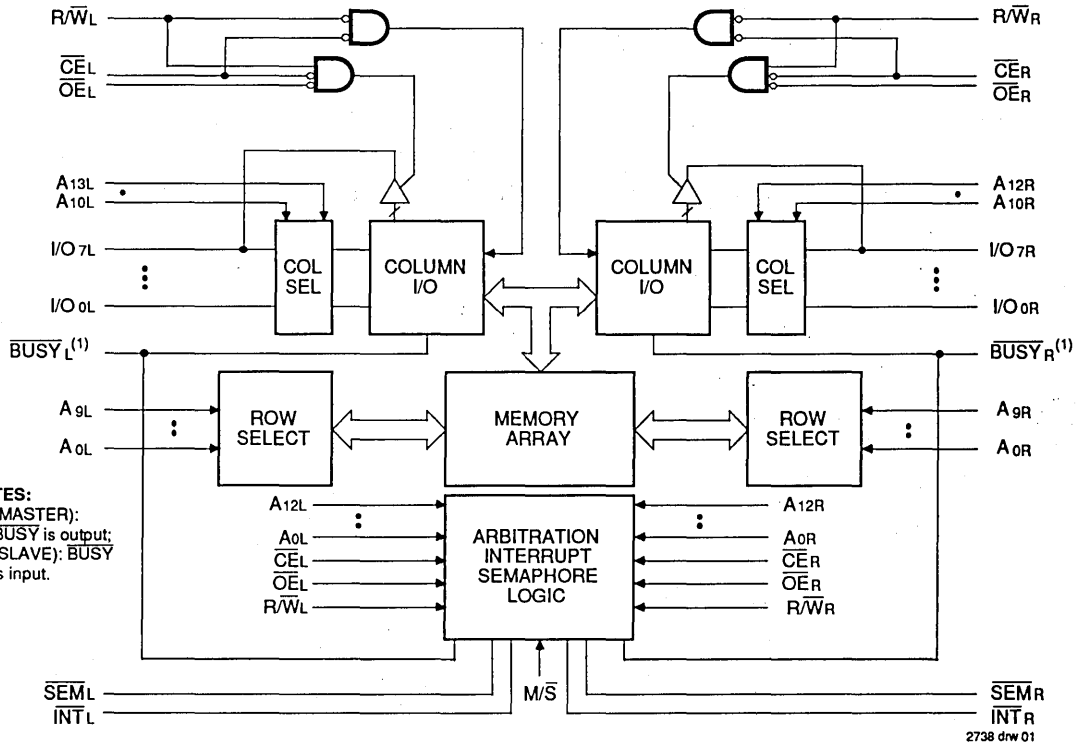
FEATURES:

- True dual-ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Military: 45/55/70ns (max.)
  - — Commercial: 35/45/55ns (max.)
- Low-power operation
  - — IDT7005S
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7005L
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- IDT7005 easily expands data bus width to 16 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- Interrupt Flag
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL compatible, single 5V (±10%) power supply
- Available in 68-pin PGA, quad flatpack, LCC and PLCC

DESCRIPTION:

The IDT7005 is a high-speed 8K x 8 dual-port static RAM. The IDT7005 is designed to be used as a stand-alone 64K-bit dual-port RAM or as a combination MASTER/SLAVE dual-port RAM for 16-bit-or-more word systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-bit or wider memory system applications results in full-speed, error-free

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.

2738 drw 01

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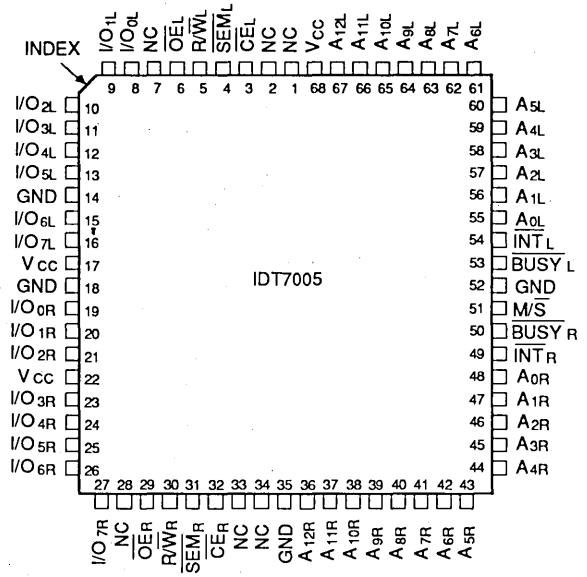
operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 500mW or power at maximum access times as fast as 35ns. Low-power (L) versions offer battery backup data retention capability with each port typically consuming 500µW from a 2V battery.

The IDT7005 is packaged in plastic as well as ceramic 68-pin PGA and 68-pin quad flatpack, LCC and PLCC. The military devices are processed 100% in compliance to the test methods of MIL-STD-883, Method 5004.

PIN CONFIGURATIONS

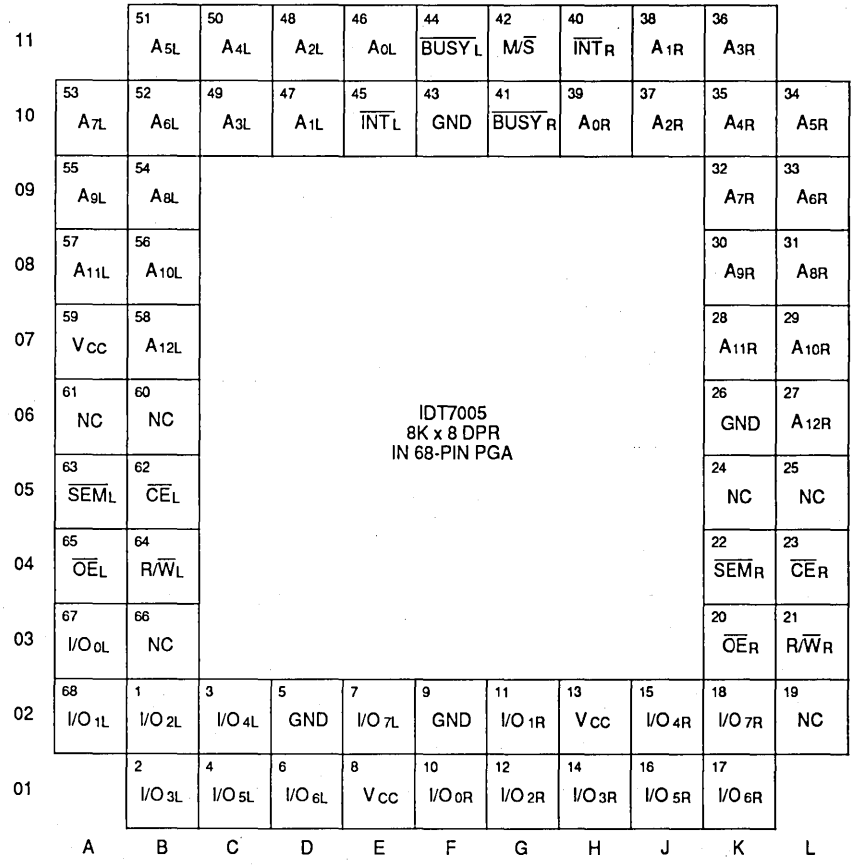


2738 drw 02

LCC/PLCC/FLATPACK
TOP VIEW

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.

PIN CONFIGURATIONS (Continued)



2738 drw 03

68-PIN PGA
TOP VIEW

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.

PIN NAMES

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
R/$\overline{W}_L$	R/$\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} - A_{12L}$	$A_{0R} - A_{12R}$	Address
$I/O_{0L} - I/O_{7L}$	$I/O_{0R} - I/O_{7R}$	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
M/$\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

2738 tbl 18

7

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

Inputs[1]				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0-7	Mode
H	X	X	H	Hi-Z	Deselected: Power Down
L	L	X	H	DATAIN	Write to Memory
L	H	L	H	DATAOUT	Read Memory
X	X	H	X	Hi-Z	Outputs Disabled

NOTE:
1. $A_{0L} — A_{12L} \neq A_{0R} — A_{12R}$

2738 tbl 01

TRUTH TABLE: SEMAPHORE READ/WRITE CONTROL

Inputs				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O07	Mode
H	H	L	L	DATAOUT	Read Data in Semaphore Flag
H	⎍	X	L	DATAIN	Write DIN0 into Semaphore Flag
L	X	X	L	—	Not Allowed

2738 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2738 tbl 04

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Output Capacitance	VOUT = 0V	11	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

2738 tbl 03

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2738 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE:
1. $V_{IL} \geq$ -3.0V for pulse width less than 20ns.

2738 tbl 06

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7005S		IDT7005L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[5]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2738 tbl 07

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7005X35 COM'L ONLY Typ.[2]	7005X35 COM'L ONLY Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \le V_{IL}$, Outputs Open, $\overline{SEM} \ge V_{IH}$, f = f_{MAX}[3]	MIL.	S	—	—	mA
				L	—	—	
			COM'L.	S	—	340	
				L	—	290	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_R$ = $\overline{CE}_L \ge V_{IH}$, $\overline{SEM}_R$ = $\overline{SEM}_L \ge V_{IH}$, f = f_{MAX}[3]	MIL.	S	—	—	mA
				L	—	—	
			COM'L.	S	—	70	
				L	—	50	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \ge V_{IH}$, Active Port Outputs Open, f = f_{MAX}[3], $\overline{SEM}_R$ = $\overline{SEM}_L \ge V_{IH}$	MIL.	S	—	—	mA
				L	—	—	
			COM'L.	S	—	240	
				L	—	210	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \ge V_{CC}$ - 0.2V, $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le$ 0.2V, f = 0[4], $\overline{SEM}_R$ = $\overline{SEM}_L \ge V_{CC}$ - 0.2V	MIL.	S	—	—	mA
				L	—	10	
			COM'L.	S	—	15	
				L	—	5	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ - 0.2V, $\overline{SEM}_R$ = $\overline{SEM}_L \ge V_{CC}$ - 0.2V, Active Port Outputs Open, f = f_{MAX}[3]	MIL.	S	—	—	mA
				L	—	—	
		$V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le$ 0.2V	COM'L.	S	—	220	
				L	—	180	

NOTES:
1. X in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C.
3. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. At $V_{CC} \le$ 1.0V input leakages are undefined.

2738 tbl 08

7

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1](Continued) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7005X45 Typ.[2]	7005X45 Max.	7005X55 Typ.[2]	7005X55 Max.	7005X70 MIL ONLY Typ.[2]	7005X70 MIL ONLY Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \le V_{IL}$, Outputs Open $\overline{SEM} \ge V_{IH}$ $f = f_{MAX}$[3]	MIL.	S	—	400	—	395	—	390	mA
				L	—	340	—	335	—	330	
			COM'L.	S	—	340	—	335	—	—	
				L	—	290	—	285	—	—	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE_L} = \overline{CE_R} \ge V_{IH}$ $\overline{SEM_R} = \overline{SEM_L} \ge V_{IH}$ $f = f_{MAX}$[3]	MIL.	S	—	85	—	85	—	85	mA
				L	—	65	—	65	—	65	
			COM'L.	S	—	70	—	70	—	—	
				L	—	50	—	50	—	—	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE_R}$ or $\overline{CE_L} \ge V_{IH}$ Active Port Outputs Open $f = f_{MAX}$[3] $\overline{SEM_R} = \overline{SEM_L} \ge V_{IH}$	MIL.	S	—	290	—	290	—	290	mA
				L	—	250	—	250	—	250	
			COM'L.	S	—	240	—	240	—	—	
				L	—	210	—	210	—	—	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE_L}$ and $\overline{CE_R} \ge V_{CC}$ - 0.2V $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le 0.2V$, $f = 0$[4] $\overline{SEM_R} = \overline{SEM_L} \ge V_{CC}$ - 0.2V	MIL.	S	—	30	—	30	—	30	mA
				L	—	10	—	10	—	10	
			COM'L.	S	—	15	—	15	—	—	
				L	—	5	—	5	—	—	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	One Port $\overline{CE_L}$ or $\overline{CE_R} \ge V_{CC}$ - 0.2V $\overline{SEM_R} = \overline{SEM_L} \ge V_{CC}$ - 0.2V	MIL.	S	—	260	—	260	—	260	mA
				L	—	215	—	215	—	215	
		$V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le 0.2V$ Active Port Outputs Open, $f = f_{MAX}$[3]	COM'L.	S	—	220	—	220	—	—	
				L	—	180	—	180	—	—	

NOTES:
1. X in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C.
3. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of $1/t_{RC}$, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. At $V_{CC} \le 1.0V$ input leakages are undefined.

2738 tbl 08

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES (L Version Only)

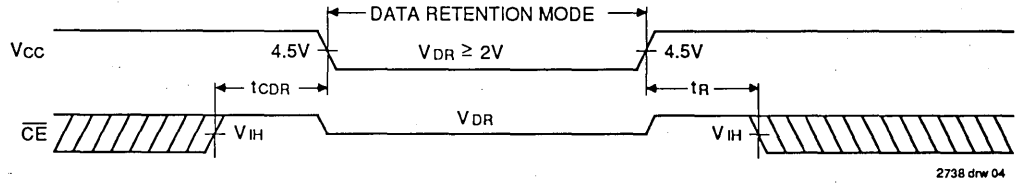
(V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$	MIL.	—	—	4000	µA
		$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	COM'L.	—	—	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:
1. T_A = +25°C, V_{CC} = 2V
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

2738 tbl 09

DATA RETENTION WAVEFORM

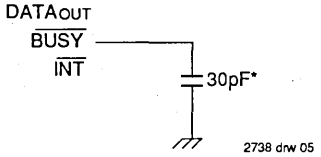


2738 drw 04

AC TEST CONDITIONS

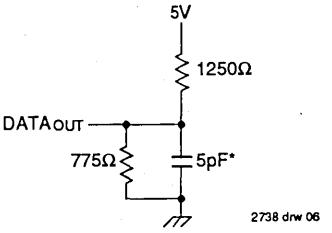
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2738 tbl 10



2738 drw 05

Figure 1. Output Load



2738 drw 06

Figure 2. Output Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})

* Including scope and jig.

7

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[4]

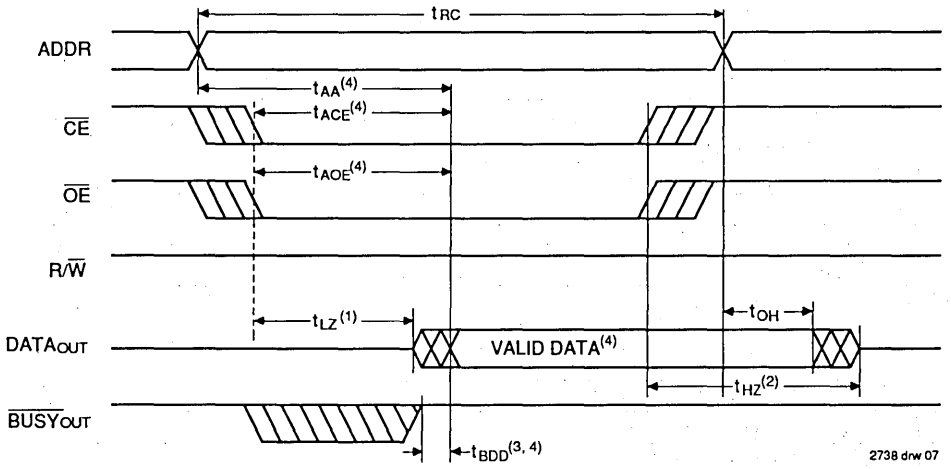
Symbol	Parameter	IDT7005X35 COM'L ONLY Min.	IDT7005X35 COM'L ONLY Max.	Unit
READ CYCLE				
tRC	Read Cycle Time	35	—	ns
tAA	Address Access Time	—	35	ns
tACE	Chip Enable Access Time[3]	—	35	ns
tAOE	Output Enable Access Time	—	20	ns
tOH	Output Hold from Address Change	3	—	ns
tLZ	Output Low Z Time[1, 2]	3	—	ns
tHZ	Output High Z Time[1, 2]	—	15	ns
tPU	Chip Enable to Power Up Time[2]	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	50	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	ns

Symbol	Parameter	IDT7005X45 Min.	IDT7005X45 Max.	IDT7005X55 Min.	IDT7005X55 Max.	IDT7005X70 MIL ONLY Min.	IDT7005X70 MIL ONLY Max.	Unit
READ CYCLE								
tRC	Read Cycle Time	45	—	55	—	70	—	ns
tAA	Address Access Time	—	45	—	55	—	70	ns
tACE	Chip Enable Access Time[3]	—	45	—	55	—	70	ns
tAOE	Output Enable Access Time	—	25	—	30	—	35	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low Z Time[1, 2]	5	—	5	—	5	—	ns
tHZ	Output High Z Time[1, 2]	—	20	—	25	—	30	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	50	—	50	—	50	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	15	—	ns

NOTES:
2738 tbl 11

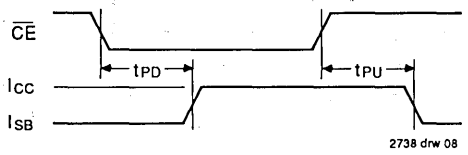
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = L, $\overline{SEM}$ = H.
4. X in part numbers indicates power rating (S or L).

WAVEFORM OF READ CYCLES[5]



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first $\overline{CE}$ or $\overline{OE}$.
3. Required only if busy logic is being used to prevent read data corruption, during simultaneous accesses to the same location, in masters and master-slave width expansions.
4. Start of valid data depends on which timing becomes effective last tABE, tAOE, tACE, tAA or tBDD.
5. $\overline{SEM}$ = H.

TIMING OF POWER-UP POWER-DOWN



AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (5)

Symbol	Parameter	IDT7005X35 COM'L ONLY Min.	IDT7005X35 COM'L ONLY Max.	Unit
WRITE CYCLE				
tWC	Write Cycle Time	35	—	ns
tEW	Chip Enable to End of Write(3)	30	—	ns
tAW	Address Valid to End of Write	30	—	ns
tAS	Address Set-up Time(3)	0	—	ns
tWP	Write Pulse Width	30	—	ns
tWR	Write Recovery Time	0	—	ns
tDW	Data Valid to End of Write	25	—	ns
tHZ	Output High Z Time(1, 2)	—	15	ns
tDH	Data Hold Time(4)	0	—	ns
tWZ	Write Enable to Output in High Z(1, 2)	—	15	ns
tOW	Output Active from End of Write(1, 2, 4)	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	10	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	10	—	ns

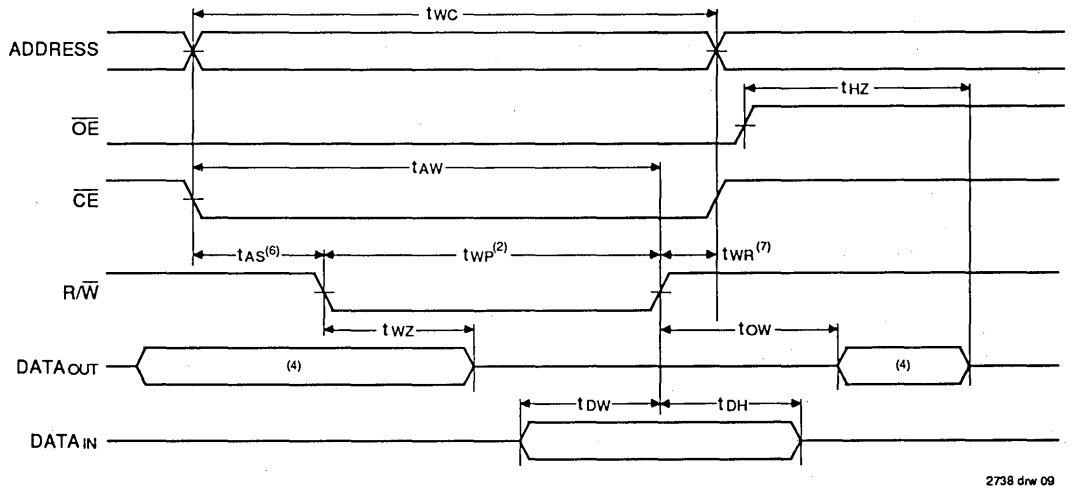
Symbol	Parameter	IDT7005X45 Min.	IDT7005X45 Max.	IDT7005X55 Min.	IDT7005X55 Max.	IDT7005X70 MIL. ONLY Min.	IDT7005X70 MIL. ONLY Max.	Unit
WRITE CYCLE								
tWC	Write Cycle Time	45	—	55	—	70	—	ns
tEW	Chip Enable to End of Write(3)	40	—	45	—	50	—	ns
tAW	Address Valid to End of Write	40	—	45	—	50	—	ns
tAS	Address Set-up Time(3)	0	—	0	—	0	—	ns
tWP	Write Pulse Width	35	—	40	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	25	—	30	—	40	—	ns
tHZ	Output High Z Time(1, 2)	—	20	—	25	—	30	ns
tDH	Data Hold Time(4)	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High Z(1, 2)	—	20	—	25	—	30	ns
tOW	Output Active from End of Write(1, 2, 4)	0	—	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	10	—	10	—	10	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	10	—	10	—	10	—	ns

NOTES:

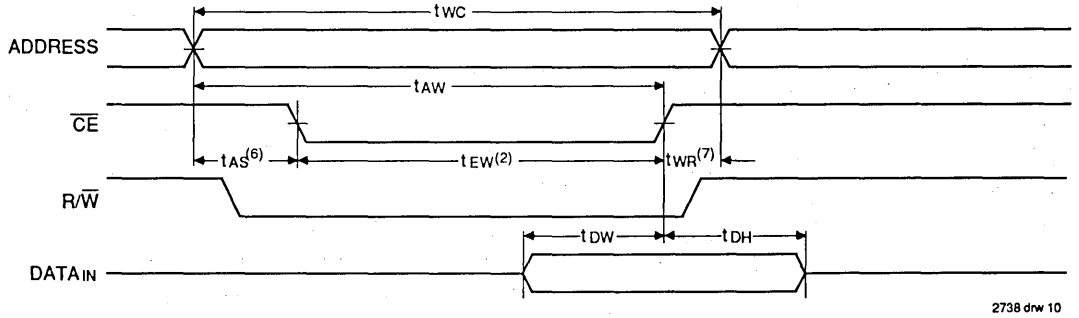
2738 tbl 12

1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = L, $\overline{SEM}$ = H. To access semaphore, $\overline{CE}$ = H and $\overline{SEM}$ = L. Either condition must be valid for the entire tEW time.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
5. X in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,3,5,8)



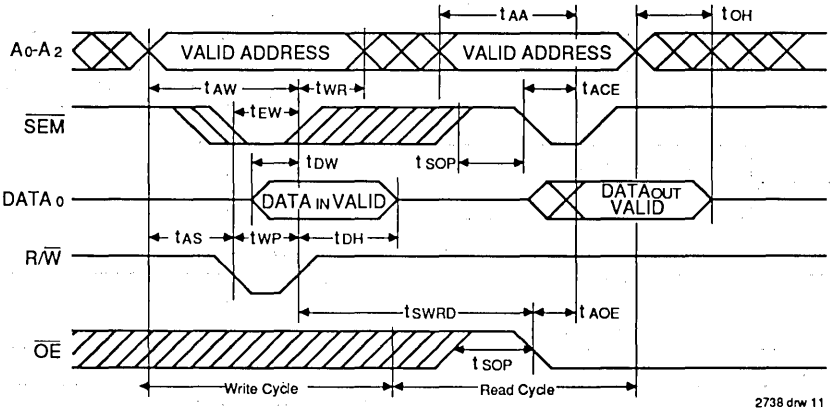
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1,3,5,8)



NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is low during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

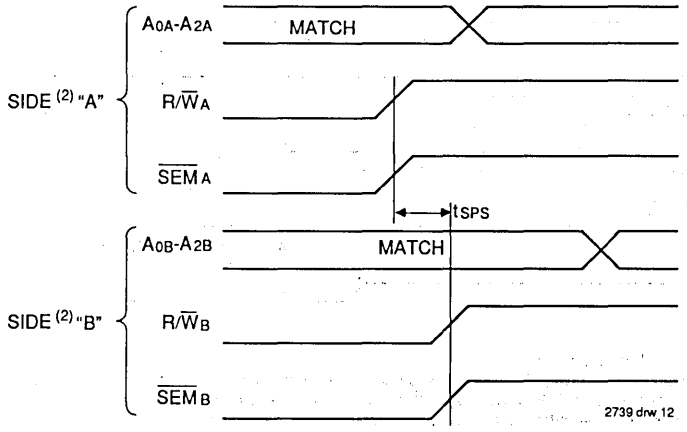
7

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



NOTE:
1. $\overline{CE}$ = H for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE WRITE CONTENTION[1,3,4]



NOTES:
1. DOR = DOL = L, $\overline{CE}_R$ = $\overline{CE}_L$ = H, Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from R/$\overline{W}_A$ or $\overline{SEM}_A$ going high to R/$\overline{W}_B$ or $\overline{SEM}_B$ going high.
4. If tSPS is violated, the semaphore will fall positively to one side or the other, but there is not guarantee which side will obtain the flag.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[6]

Symbol	Parameter	IDT7005X35 COM'L ONLY Min.	IDT7005X35 COM'L ONLY Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)				
tBAA	$\overline{BUSY}$ Access Time to Address	—	35	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	30	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable	—	30	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable	—	25	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[5]	—	Note 3	ns
BUSY TIMING (M/$\overline{S}$ = L)				
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	25	—	ns
PORT-TO-PORT DELAY TIMING				
tWDD	Write Pulse to Data Delay[7]	—	60	ns
tDDD	Write Data Valid to Read Data Delay[7]	—	45	ns

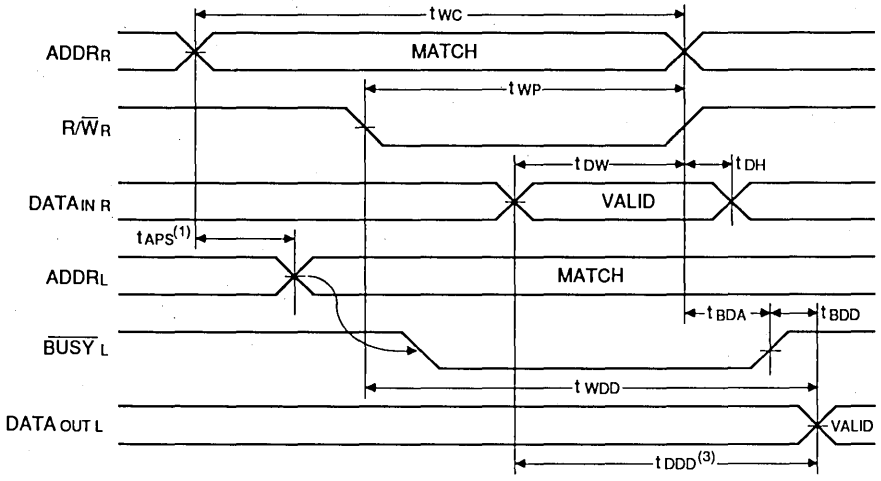
Symbol	Parameter	IDT7005X45 Min.	IDT7005X45 Max.	IDT7005X55 Min.	IDT7005X55 Max.	IDT7005X70 MIL. ONLY Min.	IDT7005X70 MIL. ONLY Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)								
tBAA	$\overline{BUSY}$ Access Time to Address	—	35	—	45	—	45	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	30	—	40	—	40	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable	—	30	—	40	—	40	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable	—	25	—	35	—	35	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[5]	—	Note 3	—	Note 3	—	Note 3	ns
BUSY TIMING (M/$\overline{S}$ = L)								
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	25	—	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay[7]	—	70	—	80	—	95	ns
tDDD	Write Data Valid to Read Data Delay[7]	—	55	—	65	—	80	ns

NOTES: 2738 tbl 13

1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (M/$\overline{S}$ = H)".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
4. To ensure that the write cycle is inhibited during contention.
5. To ensure that a write cycle is completed after contention.
6. "x" is part numbers indicates power rating (S or L).
7. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (M/$\overline{S}$ = L)".

7

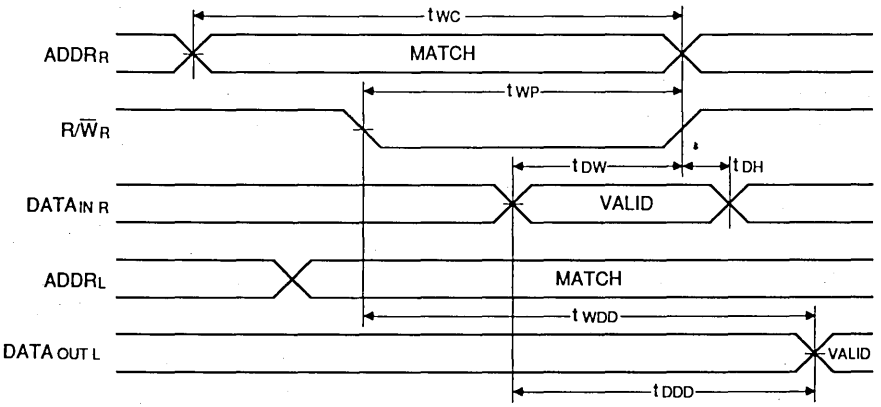
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$[2] (M/$\overline{S}$ = H)



2738 drw 13

NOTES:
1. To ensure that the earlier of the two ports wins.
2. $\overline{CE}_L = \overline{CE}_R = L$
3. $\overline{OE}$ = L for the reading port.

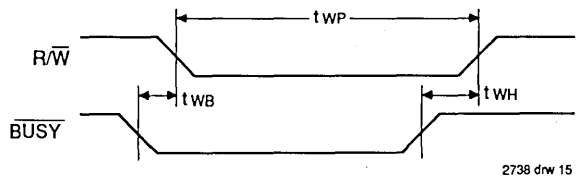
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY[1,2] (M/$\overline{S}$ = L)



2738 drw 14

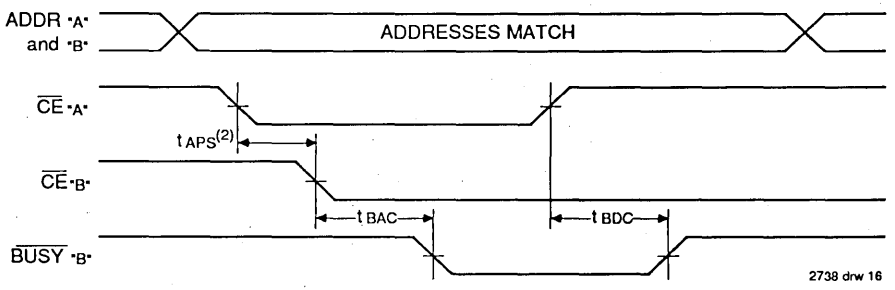
NOTES:
1. $\overline{BUSY}$ input equals H for the writing port.
2. $\overline{CE}_L = \overline{CE}_R = L$

TIMING WAVEFORM OF SLAVE WRITE (M/$\overline{S}$ = L)

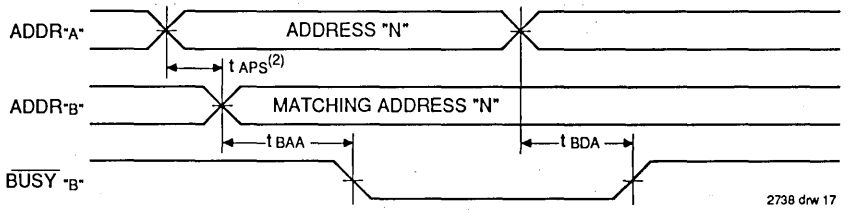


2738 drw 15

WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING[1] (M/$\overline{S}$ = H)



WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING[1](M/$\overline{S}$ = H)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If tAPS is violated, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

7

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1]

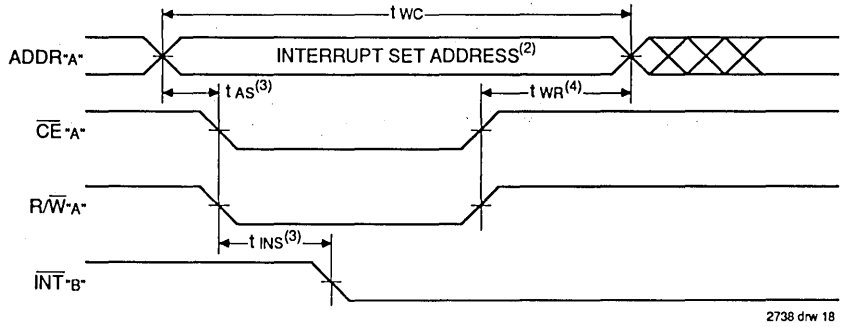
Symbol	Parameter	IDT7005X35 COM'L ONLY Min.	Max.	Unit
INTERRUPT TIMING				
tAS	Address Set-up Time	0	—	ns
tWR	Write Recovery Time	0	—	ns
tINS	Interrupt Set Time	—	30	ns
tINR	Interrupt Reset Time	—	30	ns

Symbol	Parameter	IDT7005X45 Min.	Max.	IDT7005X55 Min.	Max.	IDT7005X70 MIL. ONLY Min.	Max.	Unit
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	35	—	40	—	50	ns
tINR	Interrupt Reset Time	—	35	—	40	—	50	ns

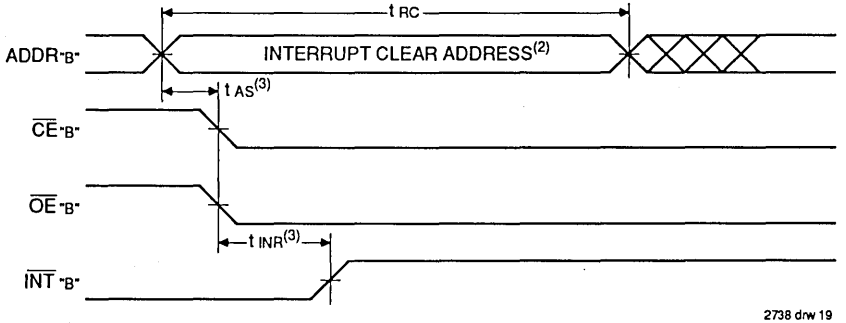
2738 tbl 14

NOTE:
1. "x" in part numbers indicates power rating (S or L).

WAVEFORM OF INTERRUPT TIMING[1]



2738 drw 18



2738 drw 19

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See Interrupt truth table.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable signal is de-asserted first.

TRUTH TABLES

TRUTH TABLE I — INTERRUPT FLAG[1]

Left Port					Right Port					
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{12L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R}-A_{12R}	$\overline{INT}_R$	Function
L	L	X	1FFF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	1FFF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	1FFE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	1FFE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

NOTES: 2738 tbl 15

1. Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then no change.
3. If $\overline{BUSY}_R$ = L, then no change.

TRUTH TABLE II — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{12L} A_{0R}-A_{12R}	$\overline{BUSY}_L$[1]	$\overline{BUSY}_R$[1]	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit[3]

NOTES: 2738 tbl 16

1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}$x outputs on the IDT7005 are push pull, not open drain outputs. On slaves the $\overline{BUSY}$x input internally inhibits writes.
2. L if the inputs to the opposite port were stable prior to the address and enable inputs of this port. H if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = Low will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs cannot be low simultaneouly.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving low regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving low regardless of actual logic level on the pin.

TRUTH TABLE III — EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE[1]

Functions	D_0 - D_7 Left	D_0 - D_7 Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Right port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

NOTE: 2738 tbl 17

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT7005.

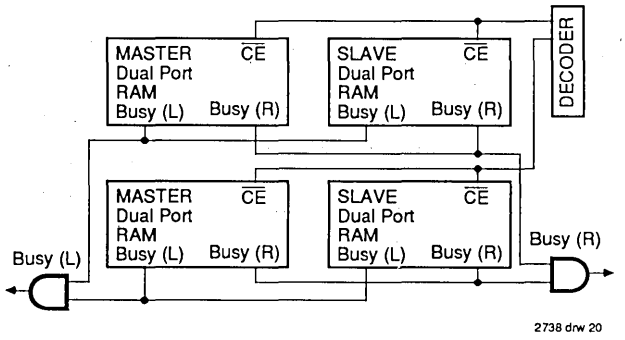


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7005 RAMs.

FUNCTIONAL DESCRIPTION

The IDT7005 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7005 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is set when the right port writes to memory location 1FFE (HEX). The left port clears the interrupt by reading address location 1FFE. Likewise, the right port interrupt flag ($\overline{INT}_R$) is set when the left port writes to memory location 1FFF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 1FFF. The message (8 bits) at 1FFE or 1FFF is user-defined. If the interrupt function is not used, address locations 1FFE and 1FFF are not used as mail boxes, but as part of the random access memory. Refer to Table I for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by placing the part in slave mode with the M/$\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low.

The busy outputs on the IDT 7005 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT7005 RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT7005 RAM the busy pin is an output if the part is used as a master (M/$\overline{S}$ pin = H), and the busy pin is an input if the part used as a slave (M/$\overline{S}$ pin = L).

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with the R/$\overline{W}$ signal. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

SEMAPHORES

The IDT7005 is an extremely fast dual-port 8K x 8 CMOS static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the dual-port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the dual-port RAM or any other shared resource.

The dual-port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the dual-port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the dual-port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT7005 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT7005's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT7005 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the dual-port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT7005 in a separate memory space from the dual-port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0 – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin Do is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussing on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from

that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—SOME EXAMPLES

Perhaps the simplest application of semaphores is their application as resource markers for the IDT7005's dual-port RAM. Say the 8K x 8 RAM was to be divided into two 4K x 8 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 4K of dual-port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 4K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 4K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 4K blocks of dual-port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the dual-port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

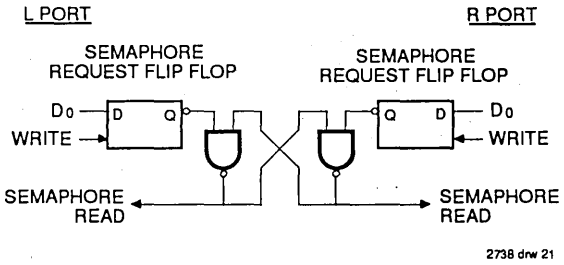
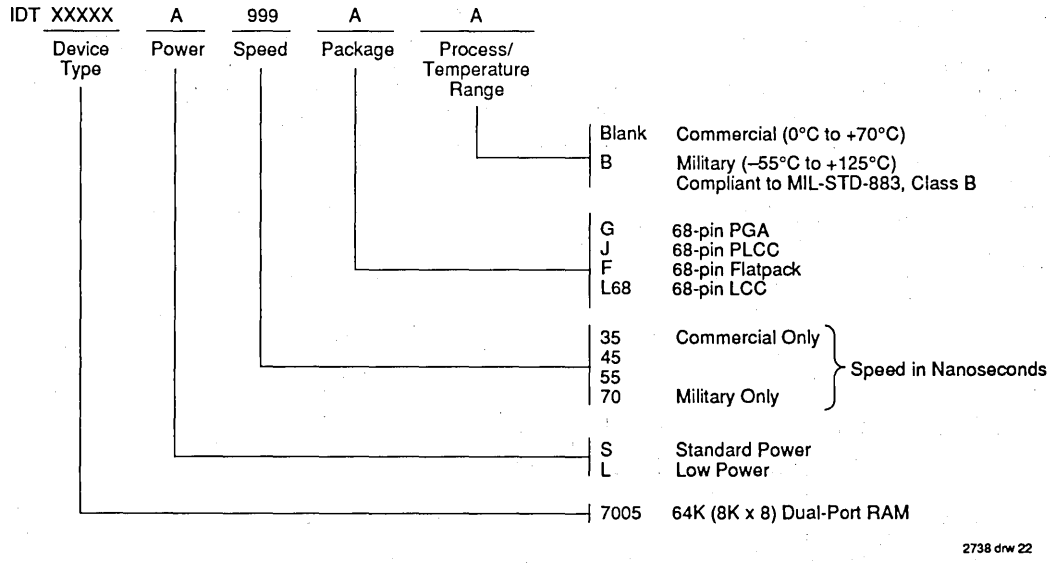


Figure 4. IDT7005 Semaphore Logic

ORDERING INFORMATION



7

Integrated Device Technology, Inc.

HIGH-SPEED 8K x 16 DUAL-PORT STATIC RAM

PRELIMINARY
IDT7025S/L

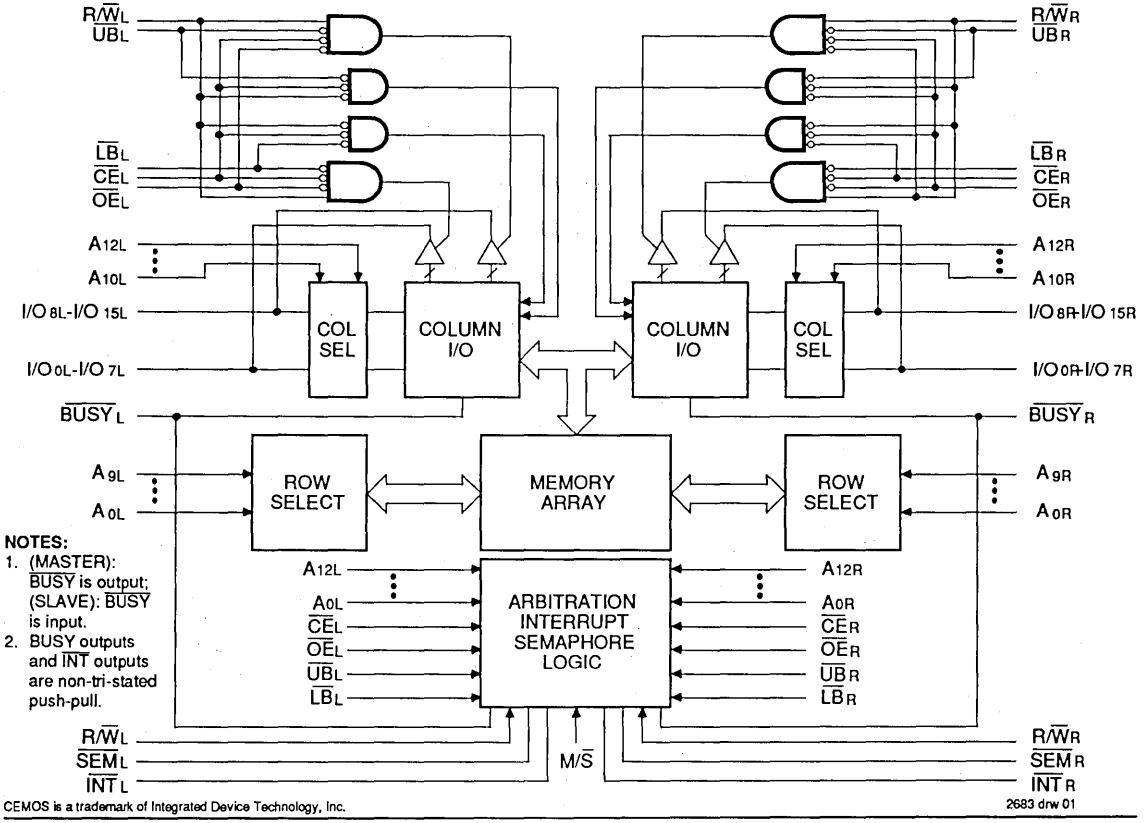
FEATURES:

- True dual-ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Military: 35/45/55/70ns (max.)
  - — Commercial: 25/30/35/45/55ns (max.)
- Low-power operation
  - — IDT7025S
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7025L
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- Separate upper-byte and lower-byte control for multiplexed bus compatibility
- IDT7025 easily expands data bus width to 32 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- Interrupt Flag
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL compatible, single 5V (±10%) power supply
- Available in 84-pin PGA, quad flatpack and PLCC

DESCRIPTION:

The IDT7025 is a high-speed 8K x 16 dual-port static RAM. The IDT7025 is designed to be used as a stand-alone 128K-bit dual-port RAM or as a combination MASTER/SLAVE dual-port RAM for 32-bit-or-more word systems. Using the IDT

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.
2. BUSY outputs and $\overline{INT}$ outputs are non-tri-stated push-pull.

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2683 drw 01

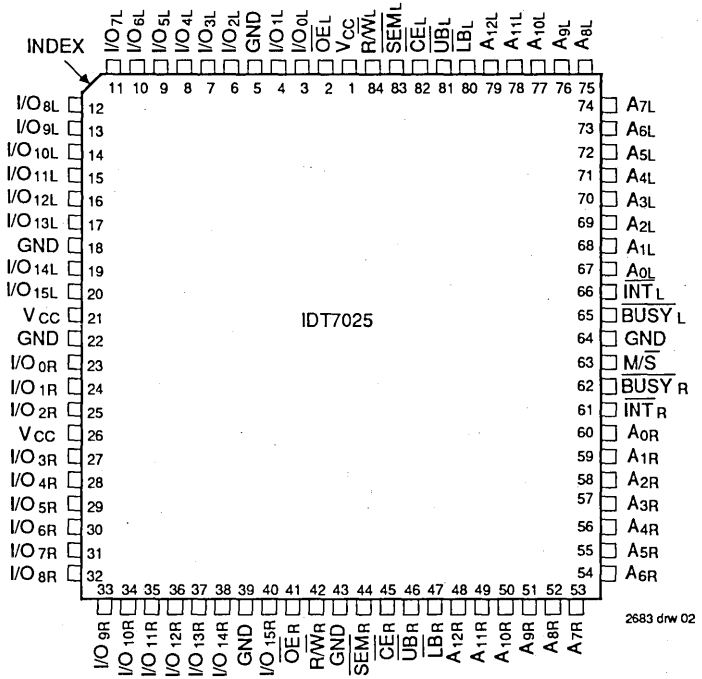
MASTER/SLAVE dual-port RAM approach in 32-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 500mW or power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability with each port typically consuming 500µW from a 2V battery.

The IDT7025 is packaged in plastic as well as ceramic 84-pin PGA and 84-pin quad flatpack and PLCC. The military devices are processed 100% in compliance to the test methods of MIL-STD-883, Method 5004.

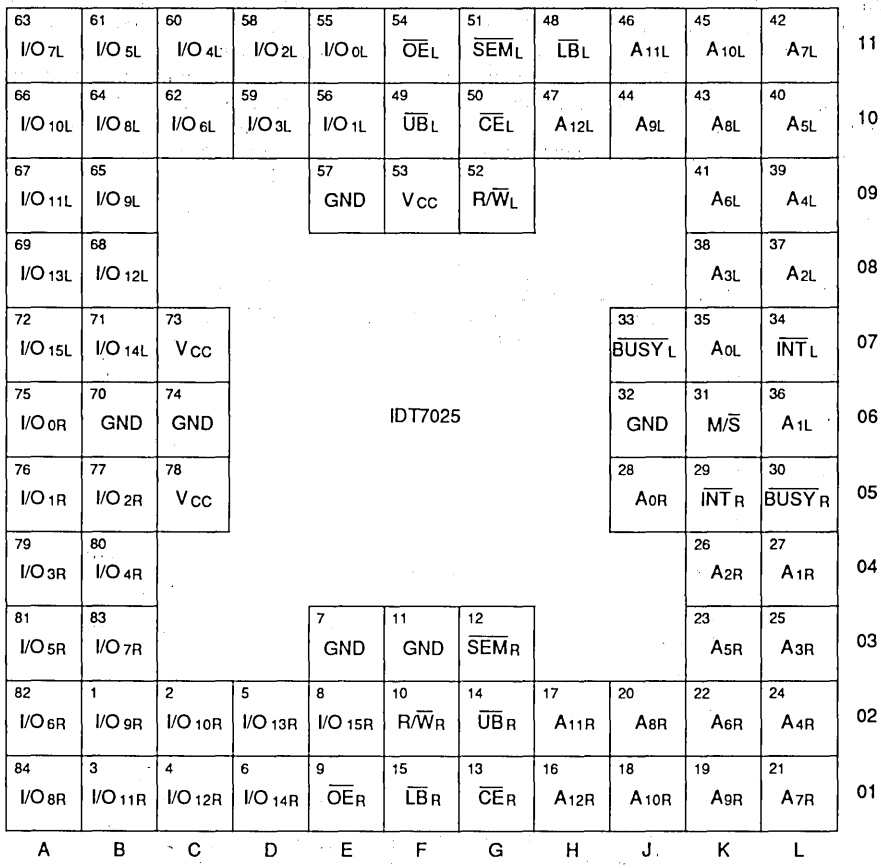
PIN CONFIGURATIONS



PLCC/FLATPACK
TOP VIEW

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.

PIN CONFIGURATIONS (Continued)



2683 drw 03

84-PIN PGA
TOP VIEW

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.

PIN NAMES

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} - A_{12L}$	$A_{0R} - A_{12R}$	Address
$I/O_{0L} - I/O_{15L}$	$I/O_{0R} - I/O_{15R}$	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

2683 tbl 18

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

Inputs[1]						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-15	I/O0-7	Mode
H	X	X	X	X	H	Hi-Z	Hi-Z	Deselected: Power Down
X	X	X	H	H	H	Hi-Z	Hi-Z	Both Bytes Deselected: Power Down
L	L	X	L	H	H	DATAIN	Hi-Z	Write to Upper Byte Only
L	L	X	H	L	H	Hi-Z	DATAIN	Write to Lower Byte Only
L	L	X	L	L	H	DATAIN	DATAIN	Write to Both Bytes
L	H	L	L	H	H	DATAOUT	Hi-Z	Read Upper Byte Only
L	H	L	H	L	H	Hi-Z	DATAOUT	Read Lower Byte Only
L	H	L	L	L	H	DATAOUT	DATAOUT	Read Both Bytes
X	X	H	X	X	X	Hi-Z	Hi-Z	Outputs Disabled

NOTE:
1. $A_{0L} — A_{12L} \neq A_{0R} — A_{12R}$

2683 tbl 01

TRUTH TABLE: SEMAPHORE READ/WRITE CONTROL

Inputs						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-15	I/O0-7	Mode
H	H	L	X	X	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
X	H	L	H	H	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
H	↓	X	X	X	L	DATAIN	DATAIN	Write DIN0 into Semaphore Flag
X	↓	X	H	H	L	DATAIN	DATAIN	Write DIN0 into Semaphore Flag
L	X	X	L	X	L	—	—	Not Allowed
L	X	X	X	L	L	—	—	Not Allowed

2683 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2683 tbl 04

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Output Capacitance	VOUT = 0V	11	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

2682 tbl 03

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2683 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE:
1. $V_{IL} \geq$ -3.0V for pulse width less than 20ns.

2683 tbl 06

7

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7025S		IDT7025L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[5]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2683 tbl 07

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7025X25 COM'L ONLY Typ.[2]	7025X25 COM'L ONLY Max.	7025X30 COM'L ONLY Typ.[2]	7025X30 COM'L ONLY Max.	7025X35 Typ.[2]	7025X35 Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ ≤ V_{IL}, Outputs Open $\overline{SEM}$ ≥ V_{IH} f = f_{MAX}[3]	MIL.	S	—	—	—	—	—	400	mA
				L	—	—	—	—	—	340	
			COM'L.	S	—	360	—	350	—	340	
				L	—	310	—	300	—	290	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_R$ = $\overline{CE}_L$ ≥ V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{IH} f = f_{MAX}[3]	MIL.	S	—	—	—	—	—	85	mA
				L	—	—	—	—	—	65	
			COM'L.	S	—	70	—	70	—	70	
				L	—	50	—	50	—	50	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH} Active Port Outputs Open f = f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{IH}	MIL.	S	—	—	—	—	—	290	mA
				L	—	—	—	—	—	250	
			COM'L.	S	—	250	—	250	—	240	
				L	—	220	—	215	—	210	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V	MIL.	S	—	—	—	—	—	30	mA
				L	—	—	—	—	—	10	
			COM'L.	S	—	15	—	15	—	15	
				L	—	5	—	5	—	5	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} - 0.2V $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX}[3]	MIL.	S	—	—	—	—	—	260	mA
				L	—	—	—	—	—	215	
			COM'L.	S	—	230	—	230	—	220	
				L	—	190	—	190	—	180	

NOTES:

2683 tbl 08

1. X in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C.
3. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. At V_{CC} ≤ 1.0V input leakages are undefined.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1](Continued) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7025X45 Typ.[2]	7025X45 Max.	7025X55 Typ.[2]	7025X55 Max.	7025X70 MIL ONLY Typ.[2]	7025X70 MIL ONLY Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \le V_{IL}$, Outputs Open $\overline{SEM} \ge V_{IH}$ $f = f_{MAX}$[3]	MIL.	S	—	400	—	395	—	390	mA
				L	—	340	—	335	—	330	
			COM'L.	S	—	340	—	335	—	—	
				L	—	290	—	285	—	—	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R \ge V_{IH}$ $\overline{SEM}_R = \overline{SEM}_L \ge V_{IH}$ $f = f_{MAX}$[3]	MIL.	S	—	85	—	85	—	85	mA
				L	—	65	—	65	—	65	
			COM'L.	S	—	70	—	70	—	—	
				L	—	50	—	50	—	—	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_R$ or $\overline{CE}_L \ge V_{IH}$ Active Port Outputs Open $f = f_{MAX}$[3] $\overline{SEM}_R = \overline{SEM}_L \ge V_{IH}$	MIL.	S	—	290	—	290	—	290	mA
				L	—	250	—	250	—	250	
			COM'L.	S	—	240	—	240	—	—	
				L	—	210	—	210	—	—	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \ge V_{CC}$ - 0.2V $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le 0.2V$, $f = 0$[4] $\overline{SEM}_R = \overline{SEM}_L \ge V_{CC}$ - 0.2V	MIL.	S	—	30	—	30	—	30	mA
				L	—	10	—	10	—	10	
			COM'L.	S	—	15	—	15	—	—	
				L	—	5	—	5	—	—	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ - 0.2V $\overline{SEM}_R = \overline{SEM}_L \ge V_{CC}$ - 0.2V	MIL.	S	—	260	—	260	—	260	mA
				L	—	215	—	215	—	215	
		$V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le 0.2V$ Active Port Outputs Open, $f = f_{MAX}$[3]	COM'L.	S	—	220	—	220	—	—	
				L	—	180	—	180	—	—	

NOTES:

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1. X in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C.
3. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of $1/t_{RC}$, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. At $V_{CC} \le 1.0V$ input leakages are undefined.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES (L Version Only)

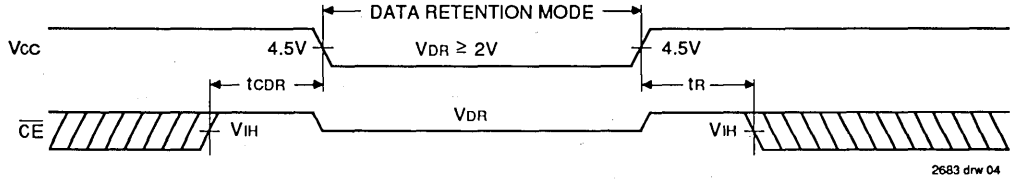
(V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$	MIL.	—	—	4000	µA
		$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	COM'L.	—	—	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:
1. T_A = +25°C, V_{CC} = 2V
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

2683 tbl 09

DATA RETENTION WAVEFORM

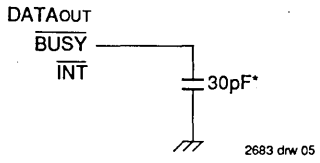


2683 drw 04

AC TEST CONDITIONS

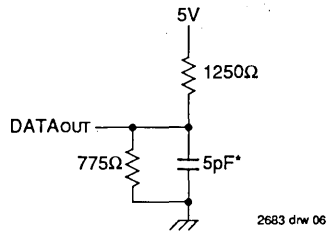
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2683 tbl 10



2683 drw 05

Figure 1. Output Load



2683 drw 06

Figure 2. Output Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})

* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[4]

Symbol	Parameter	IDT7025X25 COM'L ONLY		IDT7025X30 COM'L ONLY		IDT7025X35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
tRC	Read Cycle Time	25	—	30	—	35	—	ns
tAA	Address Access Time	—	25	—	30	—	35	ns
tACE	Chip Enable Access Time[3]	—	25	—	30	—	35	ns
tABE	Byte Enable Access Time[3]	—	25	—	30	—	35	ns
tAOE	Output Enable Access Time	—	13	—	15	—	20	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low Z Time[1, 2]	3	—	3	—	3	—	ns
tHZ	Output High Z Time[1, 2]	—	15	—	15	—	15	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	50	—	50	—	50	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	12	—	15	—	15	—	ns

Symbol	Parameter	IDT7025X45		IDT7025X55		IDT7025X70 MIL ONLY		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
tRC	Read Cycle Time	45	—	55	—	70	—	ns
tAA	Address Access Time	—	45	—	55	—	70	ns
tACE	Chip Enable Access Time[3]	—	45	—	55	—	70	ns
tABE	Byte Enable Access Time[3]	—	45	—	55	—	70	ns
tAOE	Output Enable Access Time	—	25	—	30	—	35	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low Z Time[1, 2]	5	—	5	—	5	—	ns
tHZ	Output High Z Time[1, 2]	—	20	—	25	—	30	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	50	—	50	—	50	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	15	—	ns

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = L, $\overline{UB}$ or $\overline{LB}$ = L, $\overline{SEM}$ = H.
4. X in part numbers indicates power rating (S or L).

2683 tbl 11

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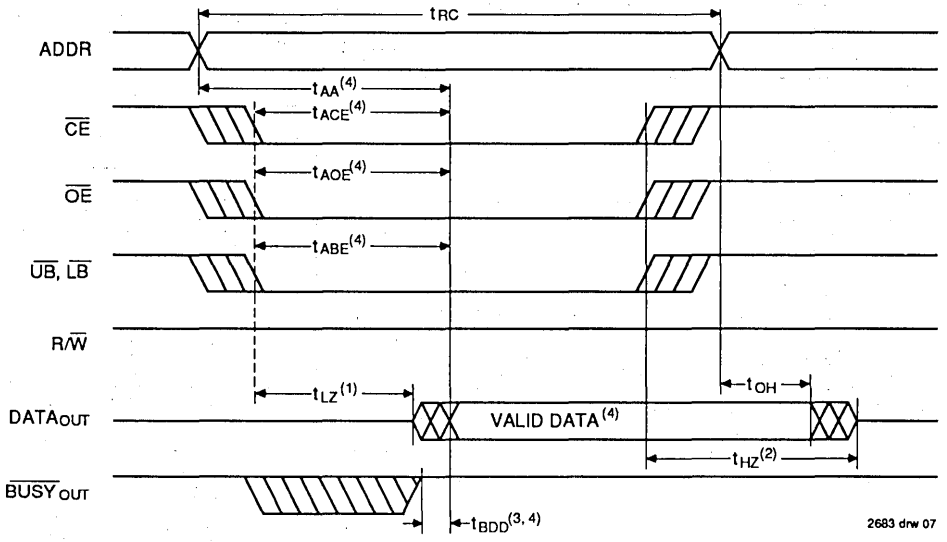
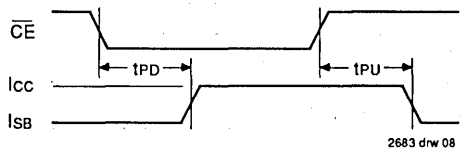
WAVEFORM OF READ CYCLES(5)



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$, $\overline{CE}$, $\overline{LB}$, or $\overline{UB}$.
2. Timing depends on which signal is de-asserted first $\overline{CE}$, $\overline{OE}$, $\overline{LB}$, or $\overline{UB}$.
3. Required only if busy logic is being used to prevent read data corruption, during simultaneous accesses to the same location, in masters and master-slave width expansions.
4. Start of valid data depends on which timing becomes effective last tABE, tAOE, tACE, tAA or tBDD.
5. $\overline{SEM}$ = H.

TIMING OF POWER-UP POWER-DOWN



AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (5)

Symbol	Parameter	IDT7025X25 COM'L ONLY		IDT7025X30 COM'L ONLY		IDT7025X35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
tWC	Write Cycle Time	25	—	30	—	35	—	ns
tEW	Chip Enable to End of Write(3)	20	—	25	—	30	—	ns
tAW	Address Valid to End of Write	20	—	25	—	30	—	ns
tAS	Address Set-up Time(3)	0	—	0	—	0	—	ns
tWP	Write Pulse Width	20	—	25	—	30	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	15	—	20	—	25	—	ns
tHZ	Output High Z Time(1, 2)	—	15	—	15	—	15	ns
tDH	Data Hold Time(4)	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High Z(1, 2)	—	15	—	15	—	15	ns
tOW	Output Active from End of Write(1, 2, 4)	0	—	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	10	—	10	—	10	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	10	—	10	—	10	—	ns

Symbol	Parameter	IDT7025X45		IDT7025X55		IDT7025X70 MIL. ONLY		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
tWC	Write Cycle Time	45	—	55	—	70	—	ns
tEW	Chip Enable to End of Write(3)	40	—	45	—	50	—	ns
tAW	Address Valid to End of Write	40	—	45	—	50	—	ns
tAS	Address Set-up Time(3)	0	—	0	—	0	—	ns
tWP	Write Pulse Width	35	—	40	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	25	—	30	—	40	—	ns
tHZ	Output High Z Time(1, 2)	—	20	—	25	—	30	ns
tDH	Data Hold Time(4)	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High Z(1, 2)	—	20	—	25	—	30	ns
tOW	Output Active from End of Write(1, 2, 4)	0	—	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	10	—	10	—	10	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	10	—	10	—	10	—	ns

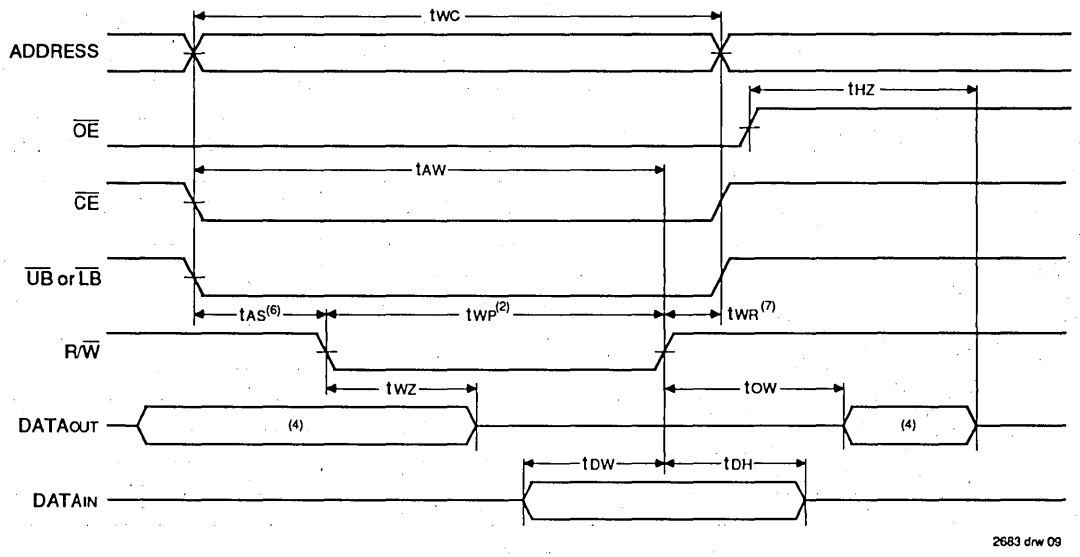
NOTES:

2683 tbl 12

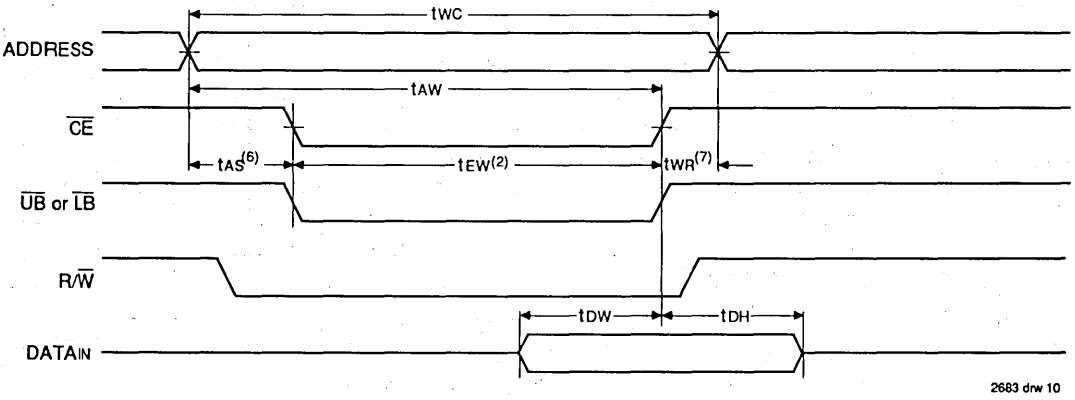
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = L, $\overline{UB}$ or $\overline{LB}$ = L, $\overline{SEM}$ = H. To access semaphore, $\overline{CE}$ = H and $\overline{SEM}$ = L. Either condition must be valid for the entire tEW time.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
5. X in part numbers indicates power rating (S or L).

7

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,3,5,8)

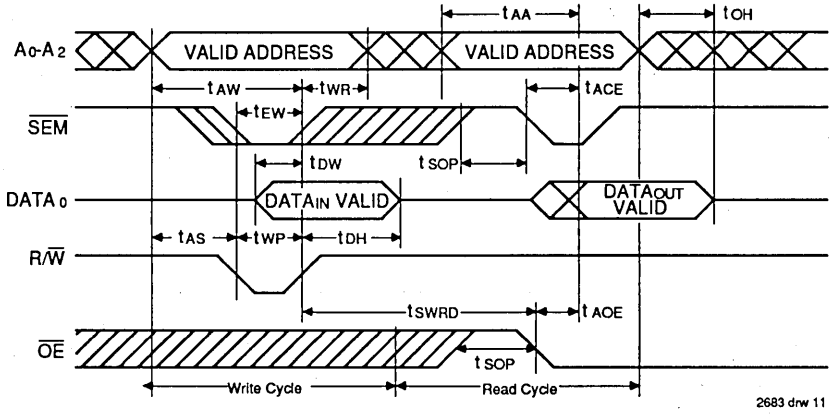


TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$ CONTROLLED TIMING(1,3,5,8)



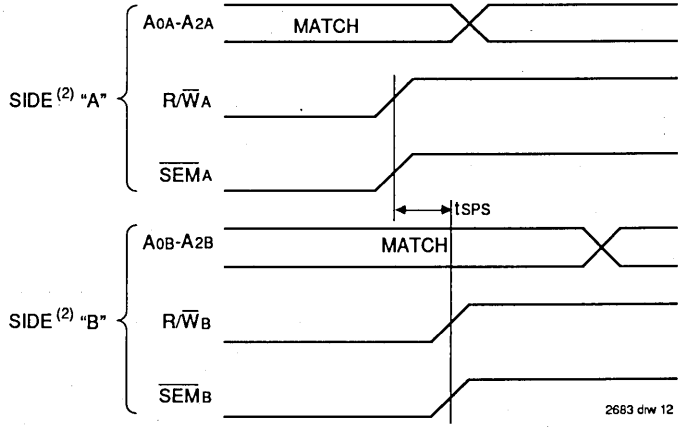
NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{UB}$ or $\overline{LB}$ and a low $\overline{CE}$ and a low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is low during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



NOTE:
1. $\overline{CE}$ = H for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE WRITE CONTENTION[1,3,4]



NOTES:
1. $D_{OR} = D_{OL}$ = L, $\overline{CE}_R = \overline{CE}_L$ = H, Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from $R/\overline{W}_A$ or $\overline{SEM}_A$ going high to $R/\overline{W}_B$ or $\overline{SEM}_B$ going high.
4. If t_{SPS} is violated, the semaphore will fall positively to one side or the other, but there is not guarantee which side will obtain the flag.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[6]

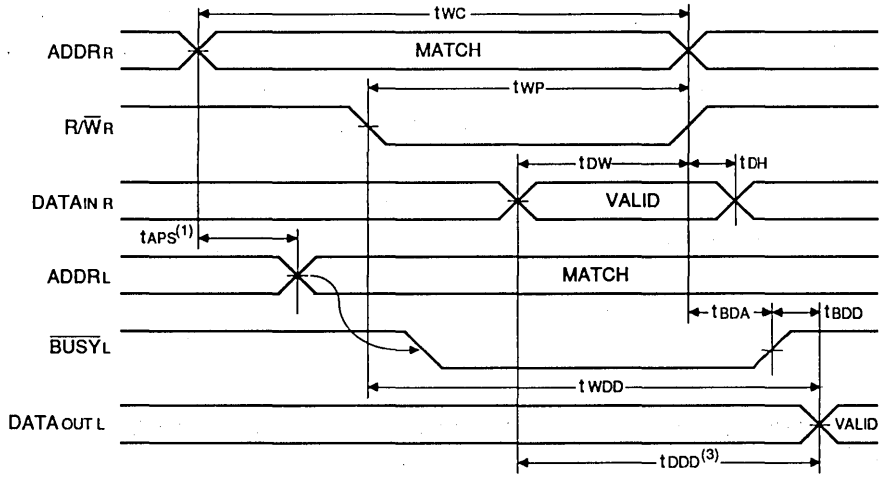
Symbol	Parameter	IDT7025X25 COM'L ONLY Min.	IDT7025X25 COM'L ONLY Max.	IDT7025X30 COM'L ONLY Min.	IDT7025X30 COM'L ONLY Max.	IDT7025X35 Min.	IDT7025X35 Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)								
tBAA	$\overline{BUSY}$ Access Time to Address	—	25	—	30	—	35	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	20	—	25	—	30	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable or Byte Enable	—	20	—	25	—	30	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable or Byte Disable	—	17	—	20	—	25	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[5]	—	Note 3	—	Note 3	—	Note 3	ns
BUSY TIMING (M/$\overline{S}$ = L)								
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	17	—	20	—	25	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay[7]	—	50	—	55	—	60	ns
tDDD	Write Data Valid to Read Data Delay[7]	—	35	—	40	—	45	ns

Symbol	Parameter	IDT7025X45 Min.	IDT7025X45 Max.	IDT7025X55 Min.	IDT7025X55 Max.	IDT7025X70 MIL. ONLY Min.	IDT7025X70 MIL. ONLY Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)								
tBAA	$\overline{BUSY}$ Access Time to Address	—	35	—	45	—	45	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	30	—	40	—	40	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable or Byte Enable	—	30	—	40	—	40	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable or Byte Disable	—	25	—	35	—	35	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[5]	—	Note 3	—	Note 3	—	Note 3	ns
BUSY TIMING (M/$\overline{S}$ = L)								
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	25	—	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay[7]	—	70	—	80	—	95	ns
tDDD	Write Data Valid to Read Data Delay[7]	—	55	—	65	—	80	ns

NOTES: 2683 tbl 13

1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (M/$\overline{S}$ = H)".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0, tWDD – tDW (actual) or tDDD – tWP (actual).
4. To ensure that the write cycle is inhibited during contention.
5. To ensure that a write cycle is completed after contention.
6. "x" is part numbers indicates power rating (S or L).
7. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (M/$\overline{S}$ = L)".

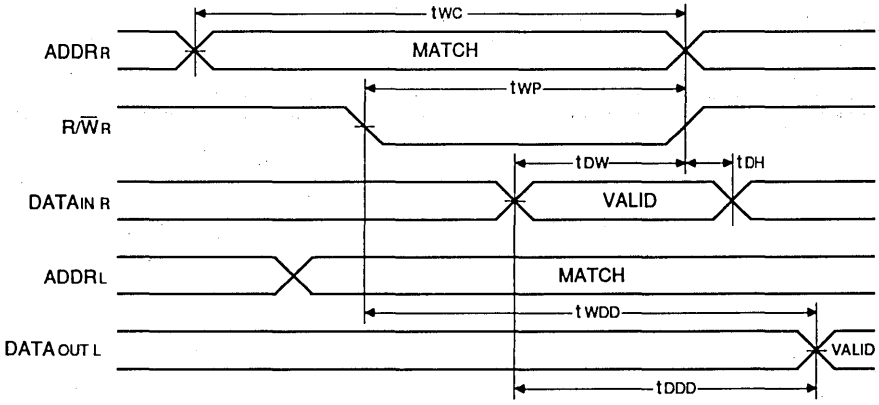
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$[2] (M/$\overline{S}$ = H)



2683 drw 13

NOTES:
1. To ensure that the earlier of the two ports wins.
2. $\overline{CE}_L$ = $\overline{CE}_R$ = L
3. $\overline{OE}$ = L for the reading port.

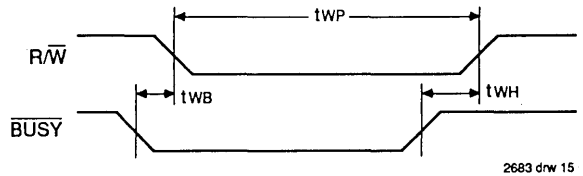
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY[1,2] (M/$\overline{S}$ = L)



2683 drw 14

NOTES:
1. $\overline{BUSY}$ input equals H for the writing port.
2. $\overline{CE}_L$ = $\overline{CE}_R$ = L

TIMING WAVEFORM OF SLAVE WRITE (M/$\overline{S}$ = L)



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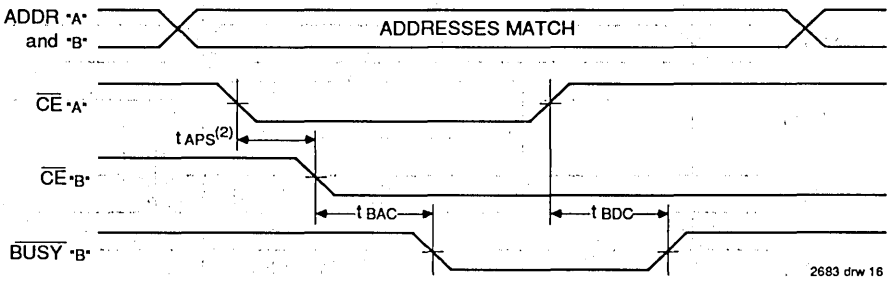
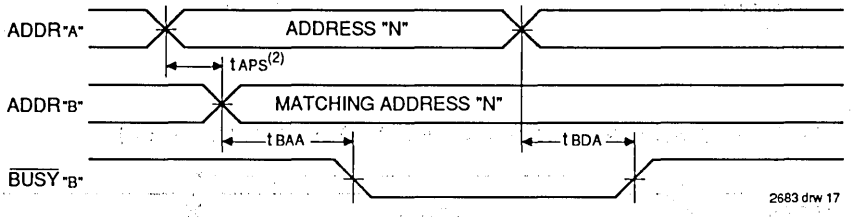
WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING[1] (M/$\overline{S}$ = H)



WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING[1](M/$\overline{S}$ = H)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If tAPS is violated, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1]

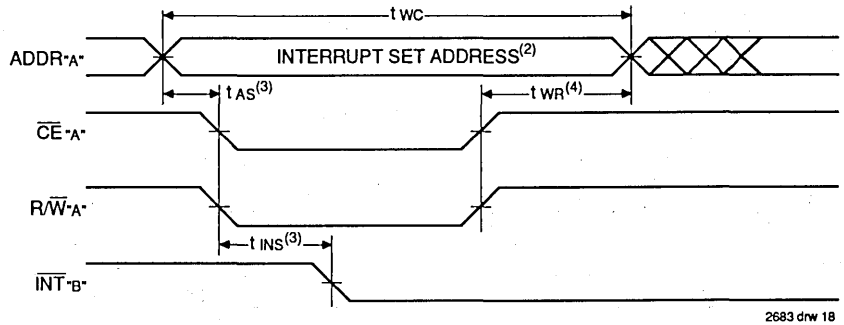
Symbol	Parameter	IDT7025X25 COM'L ONLY Min.	IDT7025X25 COM'L ONLY Max.	IDT7025X30 COM'L ONLY Min.	IDT7025X30 COM'L ONLY Max.	IDT7025X35 Min.	IDT7025X35 Max.	Unit
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	20	—	25	—	30	ns
tINR	Interrupt Reset Time	—	20	—	25	—	30	ns

Symbol	Parameter	IDT7025X45 Min.	IDT7025X45 Max.	IDT7025X55 Min.	IDT7025X55 Max.	IDT7025X70 MIL. ONLY Min.	IDT7025X70 MIL. ONLY Max.	Unit
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	35	—	40	—	50	ns
tINR	Interrupt Reset Time	—	35	—	40	—	50	ns

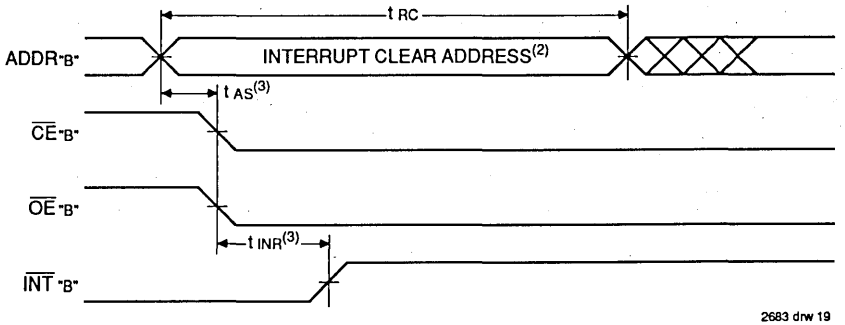
NOTE:
1. "x" in part numbers indicates power rating (S or L).

2683 tbl 14

WAVEFORM OF INTERRUPT TIMING[1]



2683 drw 18



2683 drw 19

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See Interrupt truth table.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable signal is de-asserted first.

TRUTH TABLES

TRUTH TABLE I — INTERRUPT FLAG[1]

Left Port					Right Port					
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{12L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R}-A_{12R}	$\overline{INT}_R$	Function
L	L	X	1FFF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	1FFF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	1FFE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	1FFE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

NOTES: 2683 tbl 15

1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then no change.
3. If $\overline{BUSY}_R$ = L, then no change.

TRUTH TABLE II — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{12L} A_{0R}-A_{12R}	$\overline{BUSY}_L$[1]	$\overline{BUSY}_R$[1]	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit[3]

NOTES: 2683 tbl 16

1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}x$ outputs on the IDT7025 are push pull, not open drain outputs. On slaves the $\overline{BUSY}x$ input internally inhibits writes.
2. L if the inputs to the opposite port were stable prior to the address and enable inputs of this port. H if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = Low will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs cannot be low simultaneouly.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving low regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving low regardless of actual logic level on the pin.

TRUTH TABLE III — EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE[1]

Functions	D_0 - D_{15} Left	D_0 - D_{15} Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Right port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

NOTE: 2683 tbl 17

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT7025.

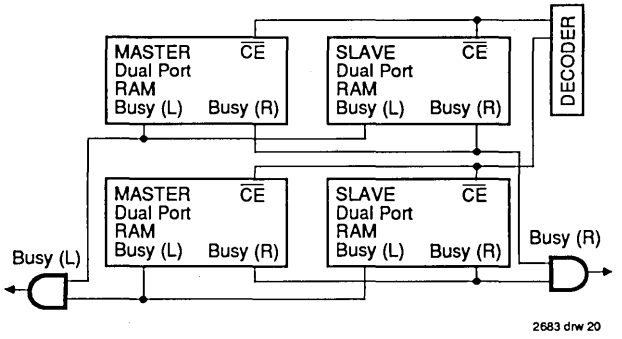


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7025 RAMs.

FUNCTIONAL DESCRIPTION

The IDT7025 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7025 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is set when the right port writes to memory location 1FFE (HEX). The left port clears the interrupt by reading address location 1FFE. Likewise, the right port interrupt flag ($\overline{INT}_R$) is set when the left port writes to memory location 1FFF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 1FFF. The message (16 bits) at 1FFE or 1FFF is user-defined. If the interrupt function is not used, address locations 1FFE and 1FFF are not used as mail boxes, but as part of the random access memory. Refer to Table I for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by placing the part in slave mode with the $M/\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low.

The busy outputs on the IDT 7025 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT7025 RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT7025 RAM the busy pin is an output if the part is used as a master ($M/\overline{S}$ pin = H), and the busy pin is an input if the part used as a slave ($M/\overline{S}$ pin = L).

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with either the $R/\overline{W}$ signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

7

SEMAPHORES

The IDT7025 is an extremely fast dual-port 8K x 16 CMOS static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the dual-port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the dual-port RAM or any other shared resource.

The dual-port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the dual-port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the dual-port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT7025 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT7025's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT7025 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the dual-port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT7025 in a separate memory space from the dual-port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0 – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin Do is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussing on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from

that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—SOME EXAMPLES

Perhaps the simplest application of semaphores is their application as resource markers for the IDT7025's dual-port RAM. Say the 8K x 16 RAM was to be divided into two 4K x 16 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 4K of dual-port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 4K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 4K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 4K blocks of dual-port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the dual-port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

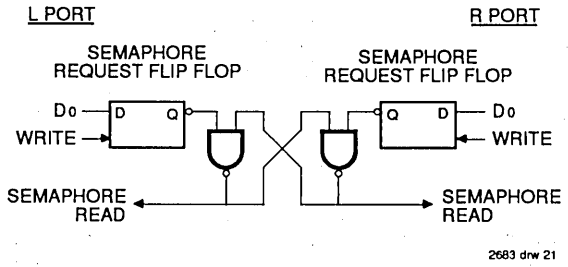
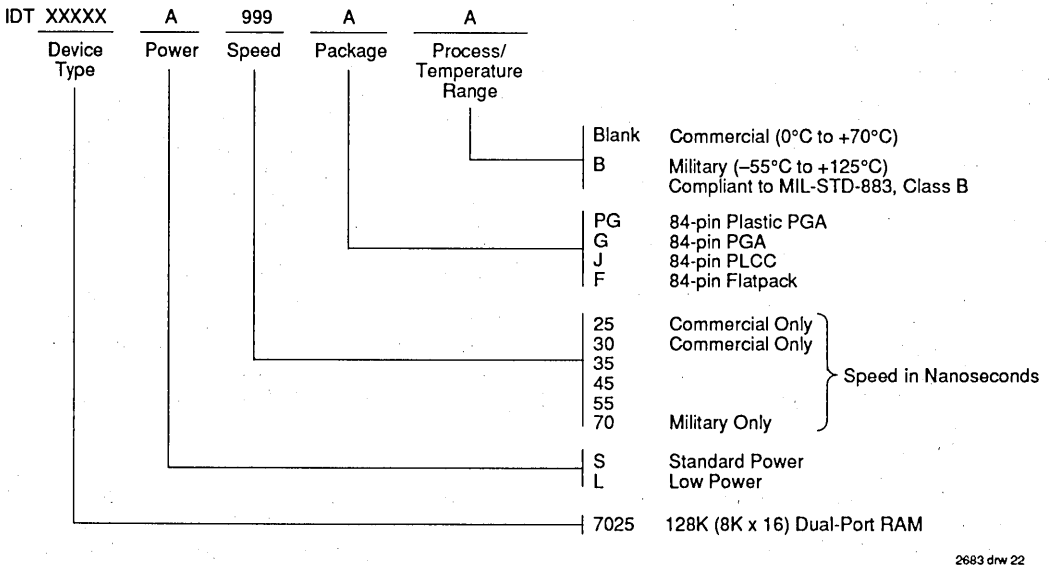


Figure 4. IDT7025 Semaphore Logic

ORDERING INFORMATION



Integrated Device Technology, Inc.

HIGH-SPEED 16K x 8 DUAL-PORT STATIC RAM

PRELIMINARY IDT7006S/L

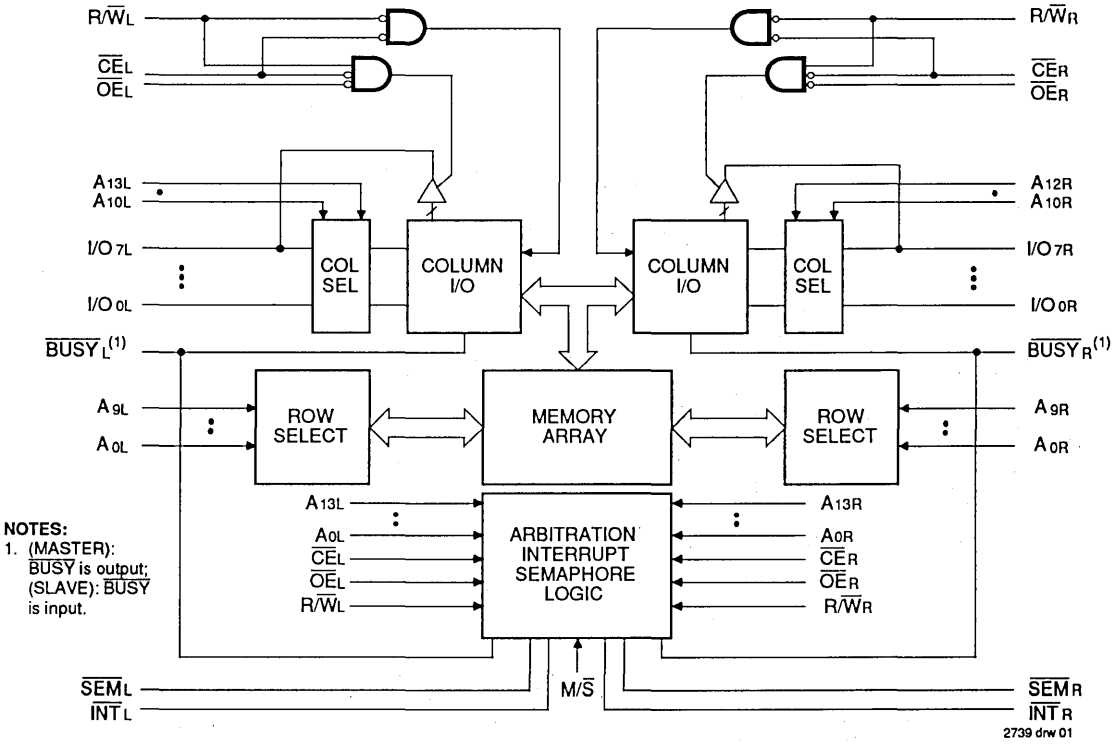
FEATURES:

- True dual-ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Military: 45/55/70ns (max.)
  - — Commercial: 35/45/55ns (max.)
- Low-power operation
  - — IDT7006S
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7006L
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- IDT7006 easily expands data bus width to 16 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- Interrupt Flag
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL compatible, single 5V (±10%) power supply
- Available in 68-pin PGA, quad flatpack, LCC and PLCC

DESCRIPTION:

The IDT7006 is a high-speed 16K x 8 dual-port static RAM. The IDT7006 is designed to be used as a stand-alone 128K-bit dual-port RAM or as a combination MASTER/SLAVE dual-port RAM for 16-bit-or-more word systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-bit or wider memory system applications results in full-speed, error-free

FUNCTIONAL BLOCK DIAGRAM



2739 drw 01

NOTES:
1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.

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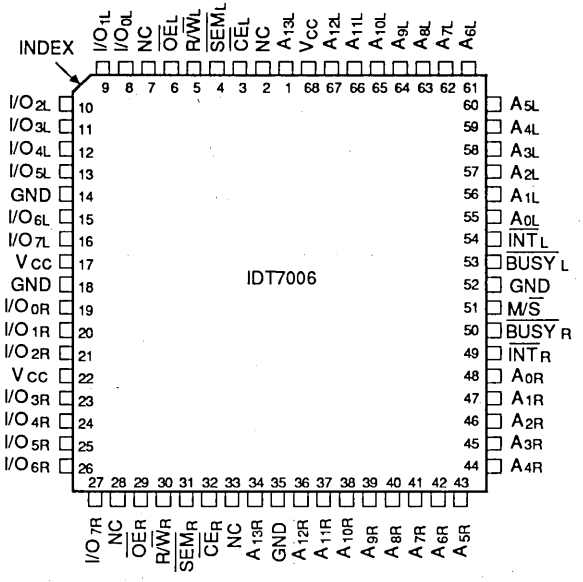
operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 500mW or power at maximum access times as fast as 35ns. Low-power (L) versions offer battery backup data retention capability with each port typically consuming 500µW from a 2V battery.

The IDT7006 is packaged in plastic as well as ceramic 68-pin PGA and 68-pin quad flatpack, LCC and PLCC. The military devices are processed 100% in compliance to the test methods of MIL-STD-883, Method 5004.

PIN CONFIGURATIONS

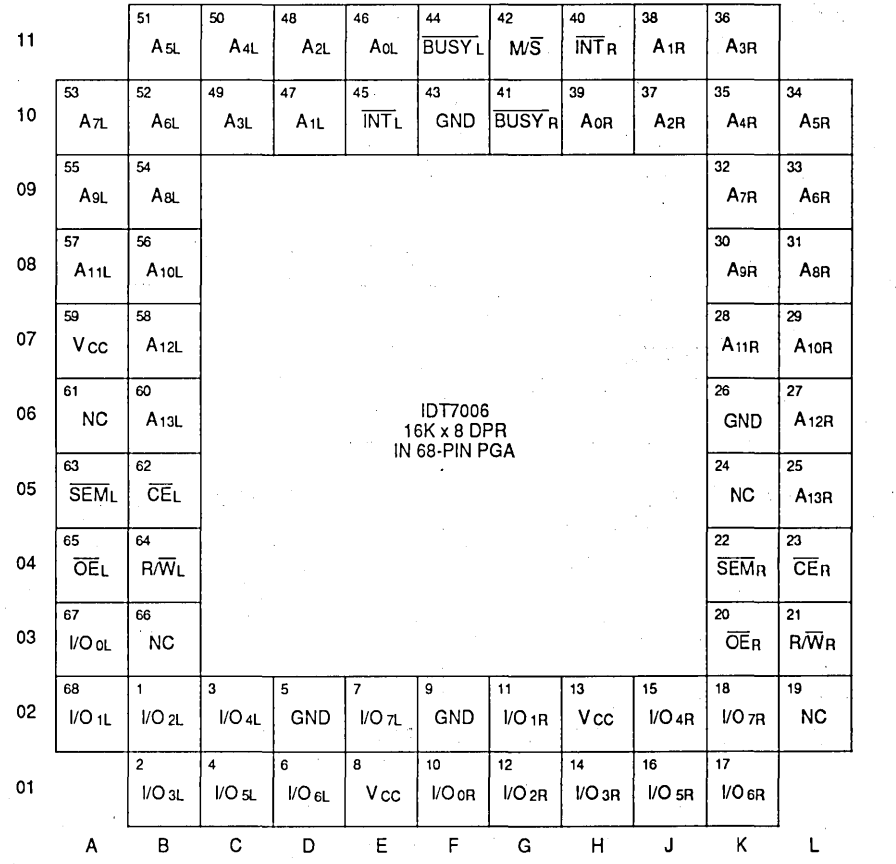


2739 drw 02

LCC/PLCC/FLATPACK
TOP VIEW

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.

PIN CONFIGURATIONS (Continued)



2739 drw 03

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.

68-PIN PGA
TOP VIEW

PIN NAMES

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} - A_{13L}$	$A_{0R} - A_{13R}$	Address
$I/O_{0L} - I/O_{7L}$	$I/O_{0R} - I/O_{7R}$	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

2739 tbl 18

7

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

Inputs[1]				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0-7	Mode
H	X	X	H	Hi-Z	Deselected: Power Down
L	L	X	H	DATAIN	Write to Memory
L	H	L	H	DATAOUT	Read Memory
X	X	H	X	Hi-Z	Outputs Disabled

NOTE:
1. $A_{0L} - A_{13L} \neq A_{0R} - A_{13R}$

2739 tbl 01

TRUTH TABLE: SEMAPHORE READ/WRITE CONTROL

Inputs				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0-7	Mode
H	H	L	L	DATAOUT	Read Data in Semaphore Flag
H	↓	X	L	DATAIN	Write DIN0 into Semaphore Flag
L	X	X	L	—	Not Allowed

2739 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2739 tbl 04

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Output Capacitance	VOUT = 0V	11	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

2739 tbl 03

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2739 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE:
1. $V_{IL} \geq$ -3.0V for pulse width less than 20ns.

2739 tbl 06

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7006S		IDT7006L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[5]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2739 tbl 07

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7006X35 COM'L ONLY Typ.[2]	7006X35 COM'L ONLY Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \le V_{IL}$, Outputs Open $\overline{SEM} \ge V_{IH}$ f = f_{MAX}[3]	MIL.	S	—	—	mA
				L	—	—	
			COM'L.	S	—	340	
				L	—	290	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_R$ = $\overline{CE}_L \ge V_{IH}$ $\overline{SEM}_R$ = $\overline{SEM}_L \ge V_{IH}$ f = f_{MAX}[3]	MIL.	S	—	—	mA
				L	—	—	
			COM'L.	S	—	70	
				L	—	50	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \ge V_{IH}$ Active Port Outputs Open f = f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L \ge V_{IH}$	MIL.	S	—	—	mA
				L	—	—	
			COM'L.	S	—	240	
				L	—	210	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \ge V_{CC}$ - 0.2V $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le$ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L \ge V_{CC}$ - 0.2V	MIL.	S	—	—	mA
				L	—	—	
			COM'L.	S	—	15	
				L	—	5	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ - 0.2V $\overline{SEM}_R$ = $\overline{SEM}_L \ge V_{CC}$ - 0.2V $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le$ 0.2V Active Port Outputs Open, f = f_{MAX}[3]	MIL.	S	—	—	mA
				L	—	—	
			COM'L.	S	—	220	
				L	—	180	

NOTES:
1. X in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C.
3. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. At $V_{CC} \le$ 1.0V input leakages are undefined.

2739 tbl 08

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DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1](Continued) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7006X45 Typ.[2]	7006X45 Max.	7006X55 Typ.[2]	7006X55 Max.	7006X70 MIL ONLY Typ.[2]	7006X70 MIL ONLY Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \le V_{IL}$, Outputs Open $\overline{SEM} \ge V_{IH}$ $f = f_{MAX}$[3]	MIL.	S	—	400	—	395	—	390	mA
				L	—	340	—	335	—	330	
			COM'L.	S	—	340	—	335	—	—	
				L	—	290	—	285	—	—	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R \ge V_{IH}$ $\overline{SEM}_R = \overline{SEM}_L \ge V_{IH}$ $f = f_{MAX}$[3]	MIL.	S	—	85	—	85	—	85	mA
				L	—	65	—	65	—	65	
			COM'L.	S	—	70	—	70	—	—	
				L	—	50	—	50	—	—	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_R$ or $\overline{CE}_L \ge V_{IH}$ Active Port Outputs Open $f = f_{MAX}$[3] $\overline{SEM}_R = \overline{SEM}_L \ge V_{IH}$	MIL.	S	—	290	—	290	—	290	mA
				L	—	250	—	250	—	250	
			COM'L.	S	—	240	—	240	—	—	
				L	—	210	—	210	—	—	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \ge V_{CC}$ - 0.2V $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le 0.2V$, f = 0[4] $\overline{SEM}_R = \overline{SEM}_L \ge V_{CC}$ - 0.2V	MIL.	S	—	30	—	30	—	30	mA
				L	—	10	—	10	—	10	
			COM'L.	S	—	15	—	15	—	—	
				L	—	5	—	5	—	—	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ - 0.2V $\overline{SEM}_R = \overline{SEM}_L \ge V_{CC}$ - 0.2V	MIL.	S	—	260	—	260	—	260	mA
				L	—	215	—	215	—	215	
		$V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le 0.2V$ Active Port Outputs Open, $f = f_{MAX}$[3]	COM'L.	S	—	220	—	220	—	—	
				L	—	180	—	180	—	—	

NOTES:

2739 tbl 08

1. X in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C.
3. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. At $V_{CC} \le 1.0V$ input leakages are undefined.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES (L Version Only)

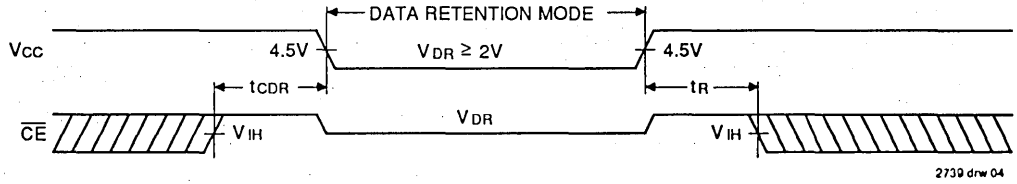
(V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$	MIL.	—	—	4000	µA
		$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	COM'L.	—	—	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:
1. T_A = +25°C, V_{CC} = 2V
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

2739 tbl 09

DATA RETENTION WAVEFORM

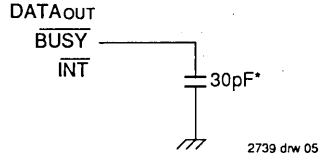


2739 drw 04

AC TEST CONDITIONS

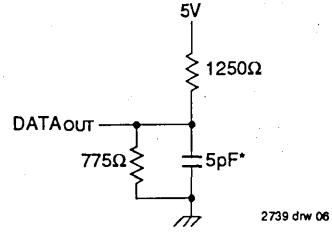
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2739 tbl 10



2739 drw 05

Figure 1. Output Load



2739 drw 06

Figure 2. Output Load (for tLZ, tHZ, tWZ, tOW)

* Including scope and jig.

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AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[4]

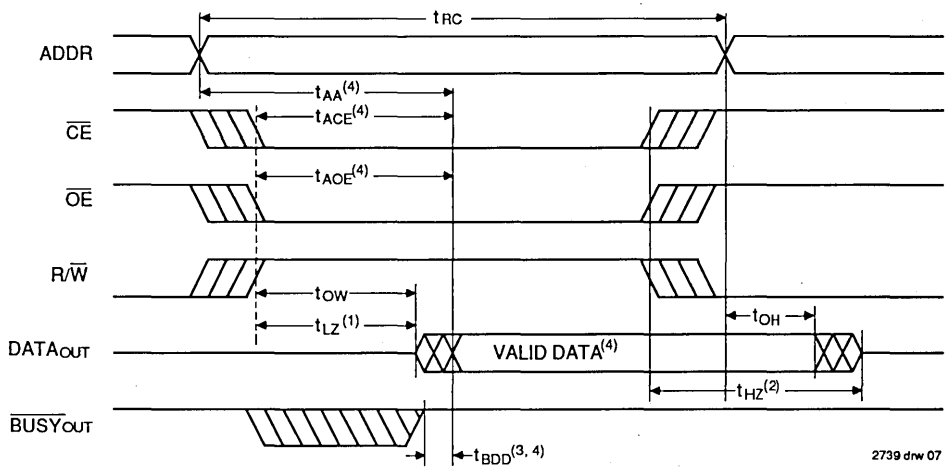
Symbol	Parameter	IDT7006X35 COM'L ONLY Min.	IDT7006X35 COM'L ONLY Max.	Unit
READ CYCLE				
tRC	Read Cycle Time	35	—	ns
tAA	Address Access Time	—	35	ns
tACE	Chip Enable Access Time[3]	—	35	ns
tAOE	Output Enable Access Time	—	20	ns
tOH	Output Hold from Address Change	3	—	ns
tLZ	Output Low Z Time[1, 2]	3	—	ns
tHZ	Output High Z Time[1, 2]	—	15	ns
tPU	Chip Enable to Power Up Time[2]	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	50	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	ns

Symbol	Parameter	IDT7006X45 Min.	IDT7006X45 Max.	IDT7006X55 Min.	IDT7006X55 Max.	IDT7006X70 MIL ONLY Min.	IDT7006X70 MIL ONLY Max.	Unit
READ CYCLE								
tRC	Read Cycle Time	45	—	55	—	70	—	ns
tAA	Address Access Time	—	45	—	55	—	70	ns
tACE	Chip Enable Access Time[3]	—	45	—	55	—	70	ns
tAOE	Output Enable Access Time	—	25	—	30	—	35	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low Z Time[1, 2]	5	—	5	—	5	—	ns
tHZ	Output High Z Time[1, 2]	—	20	—	25	—	30	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	50	—	50	—	50	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	15	—	ns

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = L, $\overline{SEM}$ = H.
4. X in part numbers indicates power rating (S or L).

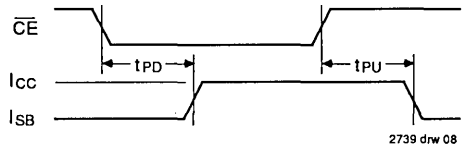
2739 tbl 11

WAVEFORM OF READ CYCLES(5)



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first $\overline{CE}$ or $\overline{OE}$.
3. Required only if busy logic is being used to prevent read data corruption, during simultaneous accesses to the same location, in masters and master-slave width expansions.
4. Start of valid data depends on which timing becomes effective last tABE, tAOE, tACE, tAA or tBDD.
5. $\overline{SEM}$ = H.

TIMING OF POWER-UP POWER-DOWN



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AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (5)

Symbol	Parameter	IDT7006X35 Min.	IDT7006X35 Max.	Unit
WRITE CYCLE				
tWC	Write Cycle Time	35	—	ns
tEW	Chip Enable to End of Write(3)	30	—	ns
tAW	Address Valid to End of Write	30	—	ns
tAS	Address Set-up Time(3)	0	—	ns
tWP	Write Pulse Width	30	—	ns
tWR	Write Recovery Time	0	—	ns
tDW	Data Valid to End of Write	25	—	ns
tHZ	Output High Z Time(1, 2)	—	15	ns
tDH	Data Hold Time(4)	0	—	ns
tWZ	Write Enable to Output in High Z(1, 2)	—	15	ns
tOW	Output Active from End of Write(1, 2, 4)	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	10	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	10	—	ns

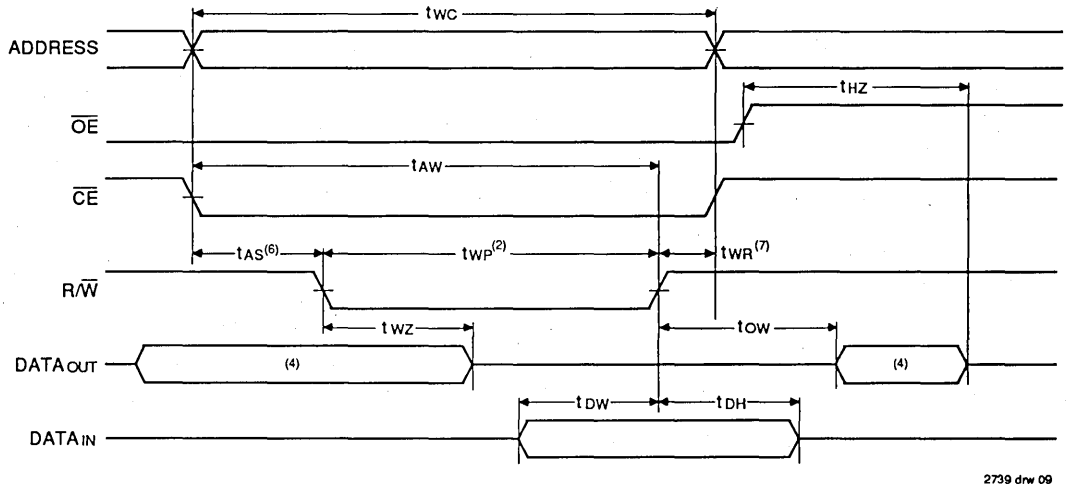
Symbol	Parameter	IDT7006X45 Min.	IDT7006X45 Max.	IDT7006X55 Min.	IDT7006X55 Max.	IDT7006X70 MIL. ONLY Min.	IDT7006X70 MIL. ONLY Max.	Unit
WRITE CYCLE								
tWC	Write Cycle Time	45	—	55	—	70	—	ns
tEW	Chip Enable to End of Write(3)	40	—	45	—	50	—	ns
tAW	Address Valid to End of Write	40	—	45	—	50	—	ns
tAS	Address Set-up Time(3)	0	—	0	—	0	—	ns
tWP	Write Pulse Width	35	—	40	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	25	—	30	—	40	—	ns
tHZ	Output High Z Time(1, 2)	—	20	—	25	—	30	ns
tDH	Data Hold Time(4)	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High Z(1, 2)	—	20	—	25	—	30	ns
tOW	Output Active from End of Write(1, 2, 4)	0	—	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	10	—	10	—	10	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	10	—	10	—	10	—	ns

NOTES:

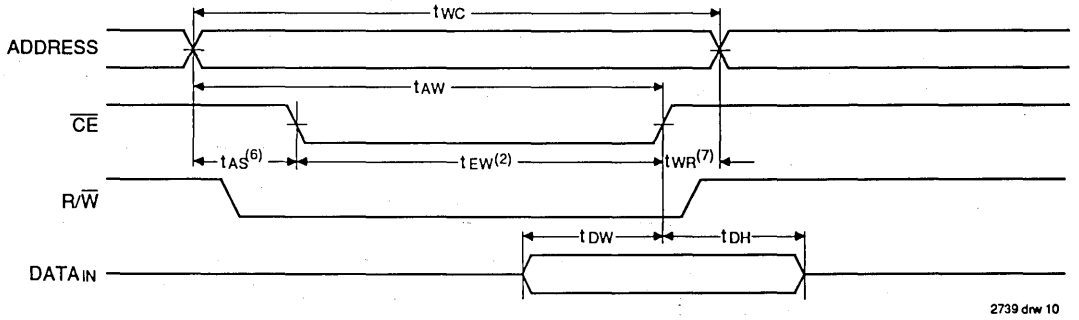
2739 tbl 12

1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = L, $\overline{SEM}$ = H. To access semaphore, $\overline{CE}$ = H and $\overline{SEM}$ = L. Either condition must be valid for the entire tEW time.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
5. X in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,3,5,8)

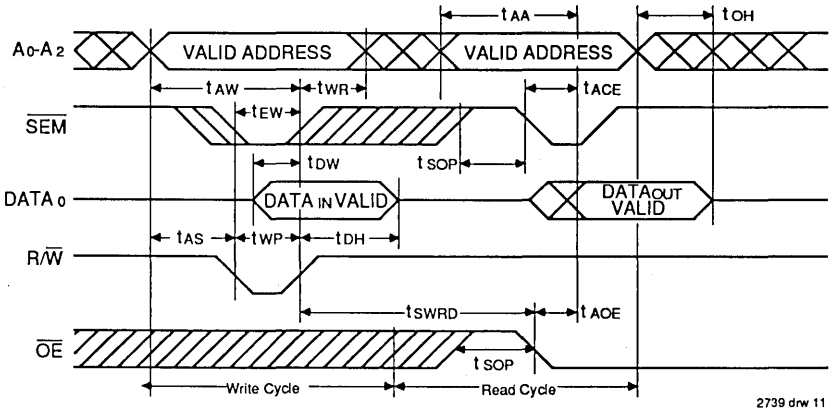


TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1,3,5,8)



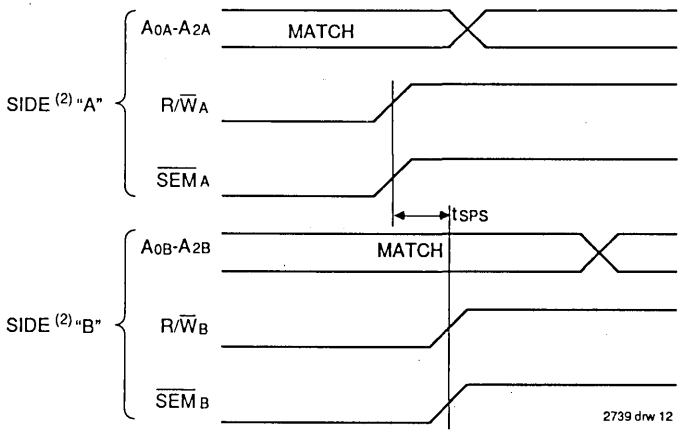
NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or twp) of a low $\overline{CE}$ and a low R/$\overline{W}$ for memory array writing cycle.
3. twR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is low during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of twp or (twz + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified twp.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



NOTE:
1. $\overline{CE}$ = H for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE WRITE CONTENTION[1,3,4]



NOTES:
1. D_{OR} = D_{OL} = L, $\overline{CE}_R$ = $\overline{CE}_L$ = H, Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from $R/\overline{W}_A$ or $\overline{SEM}_A$ going high to $R/\overline{W}_B$ or $\overline{SEM}_B$ going high.
4. If t_{SPS} is violated, the semaphore will fall positively to one side or the other, but there is not guarantee which side will obtain the flag.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[6]

Symbol	Parameter	IDT7006X35 COM'L ONLY Min.	IDT7006X35 COM'L ONLY Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)				
tBAA	$\overline{BUSY}$ Access Time to Address	—	35	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	30	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable	—	30	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable	—	25	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[5]	—	Note 3	ns
BUSY TIMING (M/$\overline{S}$ = L)				
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	25	—	ns
PORT-TO-PORT DELAY TIMING				
tWDD	Write Pulse to Data Delay[7]	—	60	ns
tDDD	Write Data Valid to Read Data Delay[7]	—	45	ns

Symbol	Parameter	IDT7006X45 Min.	IDT7006X45 Max.	IDT7006X55 Min.	IDT7006X55 Max.	IDT7006X70 MIL. ONLY Min.	IDT7006X70 MIL. ONLY Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)								
tBAA	$\overline{BUSY}$ Access Time to Address	—	35	—	45	—	45	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	30	—	40	—	40	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable	—	30	—	40	—	40	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable	—	25	—	35	—	35	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[5]	—	Note 3	—	Note 3	—	Note 3	ns
BUSY TIMING (M/$\overline{S}$ = L)								
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	25	—	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay[7]	—	70	—	80	—	95	ns
tDDD	Write Data Valid to Read Data Delay[7]	—	55	—	65	—	80	ns

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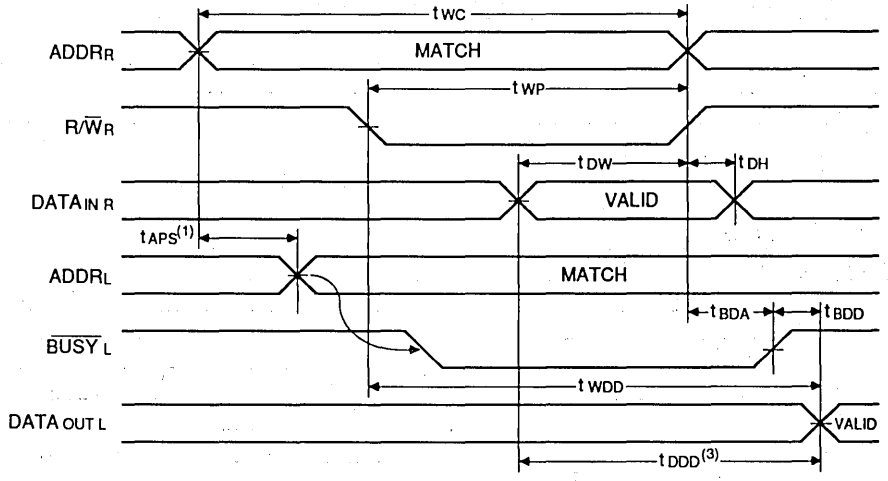
NOTES: 2739 tbl 13

1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (M/$\overline{S}$ = H)".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
4. To ensure that the write cycle is inhibited during contention.
5. To ensure that a write cycle is completed after contention.
6. "x" is part numbers indicates power rating (S or L).
7. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (M/$\overline{S}$ = L)".

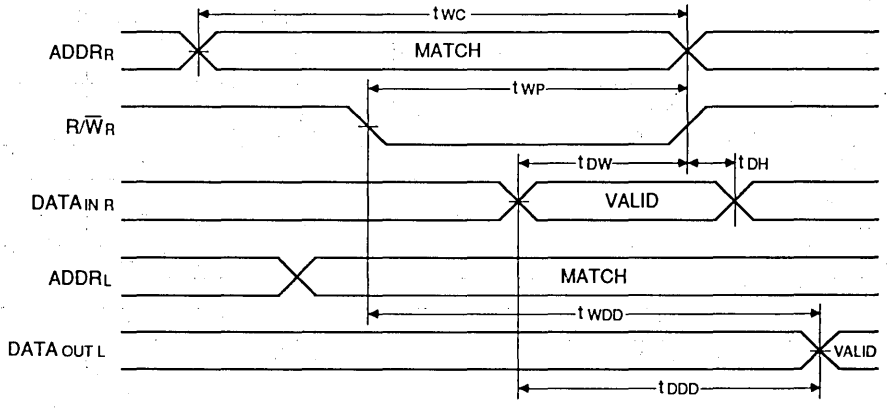
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$[2] (M/$\overline{S}$ = H)



2739 drw 13

NOTES:
1. To ensure that the earlier of the two ports wins.
2. $\overline{CE}_L = \overline{CE}_R = L$
3. $\overline{OE}$ = L for the reading port.

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY[1,2] (M/$\overline{S}$ = L)



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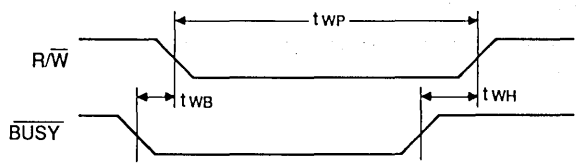
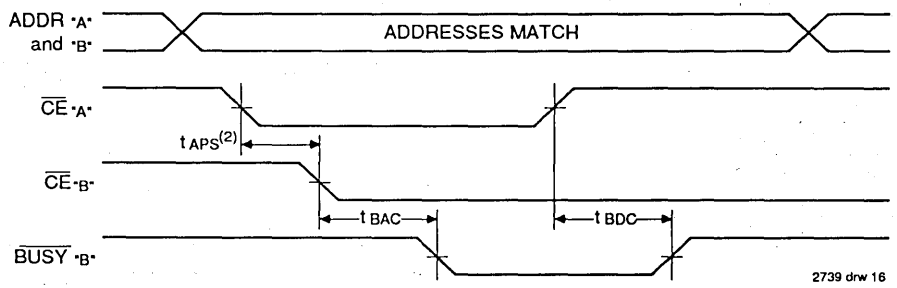
NOTES:
1. $\overline{BUSY}$ input equals H for the writing port.
2. $\overline{CE}_L = \overline{CE}_R = L$

TIMING WAVEFORM OF SLAVE WRITE (M/$\overline{S}$ = L)

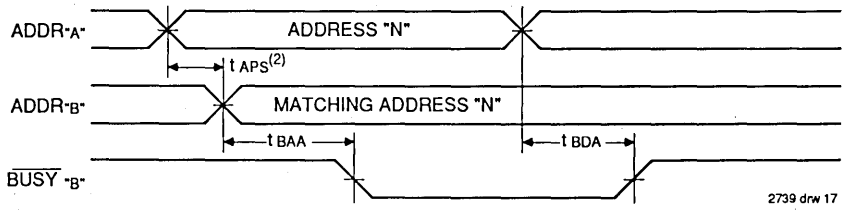


2739 drw 15

WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING[1] (M/$\overline{S}$ = H)



WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING[1](M/$\overline{S}$ = H)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If tAPS is violated, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1]

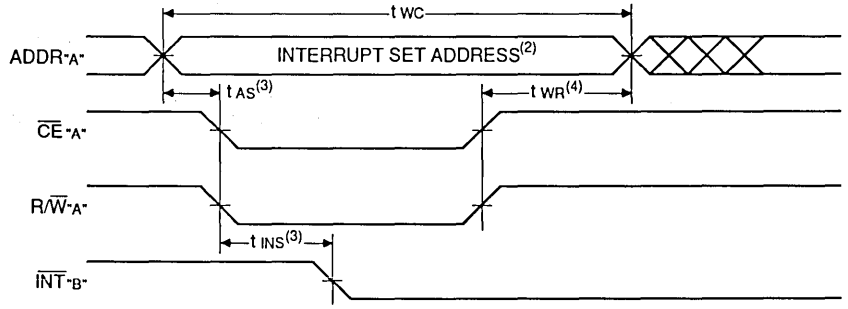
Symbol	Parameter	IDT7006X35 COM'L ONLY Min.	IDT7006X35 COM'L ONLY Max.	Unit
INTERRUPT TIMING				
tAS	Address Set-up Time	0	—	ns
tWR	Write Recovery Time	0	—	ns
tINS	Interrupt Set Time	—	30	ns
tINR	Interrupt Reset Time	—	30	ns

Symbol	Parameter	IDT7006X45 Min.	IDT7006X45 Max.	IDT7006X55 Min.	IDT7006X55 Max.	IDT7006X70 MIL. ONLY Min.	IDT7006X70 MIL. ONLY Max.	Unit
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	35	—	40	—	50	ns
tINR	Interrupt Reset Time	—	35	—	40	—	50	ns

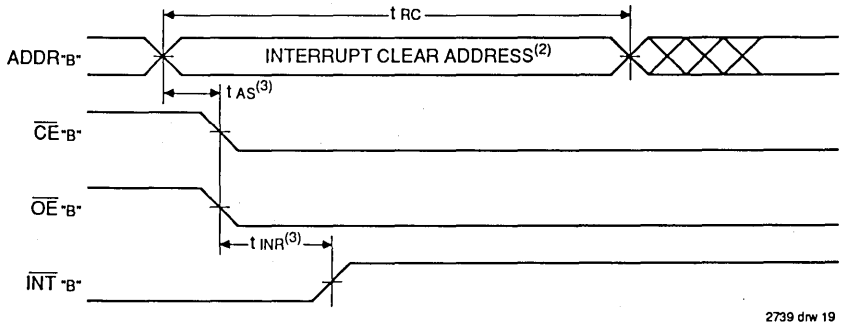
2739 tbl 14

NOTE:
1. "x" in part numbers indicates power rating (S or L).

WAVEFORM OF INTERRUPT TIMING[1]



2739 drw 18



2739 drw 19

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See Interrupt truth table.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable signal is de-asserted first.

TRUTH TABLES

TRUTH TABLE I — INTERRUPT FLAG[1]

Left Port					Right Port					
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{13L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R}-A_{13R}	$\overline{INT}_R$	Function
L	L	X	3FFF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	3FFF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	3FFE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	3FFE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

NOTES:

2739 tbl 15

1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then no change.
3. If $\overline{BUSY}_R$ = L, then no change.

TRUTH TABLE II — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{13L} A_{0R}-A_{13R}	$\overline{BUSY}_L$[1]	$\overline{BUSY}_R$[1]	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit[3]

NOTES:

2739 tbl 16

1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}$x outputs on the IDT7006 are push pull, not open drain outputs. On slaves the $\overline{BUSY}$x input internally inhibits writes.
2. L if the inputs to the opposite port were stable prior to the address and enable inputs of this port. H if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = Low will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs cannot be low simultaneouly.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving low regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving low regardless of actual logic level on the pin.

TRUTH TABLE III — EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE[1]

Functions	D_0 - D_7 Left	D_0 - D_7 Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Right port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

NOTE:

2739 tbl 17

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT7006.

7

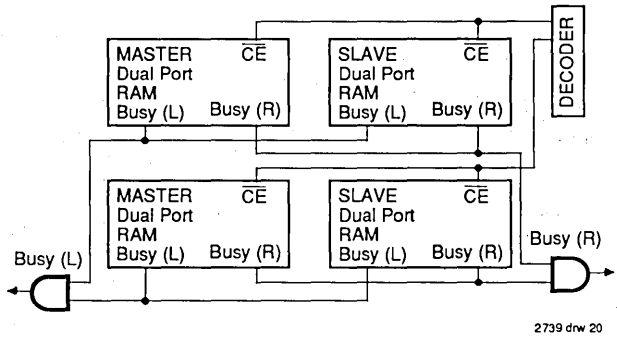


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7006 RAMs.

FUNCTIONAL DESCRIPTION

The IDT7006 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7006 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is set when the right port writes to memory location 3FFE (HEX). The left port clears the interrupt by reading address location 3FFE. Likewise, the right port interrupt flag ($\overline{INT}_R$) is set when the left port writes to memory location 3FFF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 3FFF. The message (8 bits) at 3FFE or 3FFF is user-defined. If the interrupt function is not used, address locations 3FFE and 3FFF are not used as mail boxes, but as part of the random access memory. Refer to Table 1 for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by placing the part in slave mode with the $M/\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low.

The busy outputs on the IDT 7006 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT7006 RAM array in width while using busy logic, one master part is used to decide which side of the RAMs array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT7006 RAM the busy pin is an output if the part is used as a master ($M/\overline{S}$ pin = H), and the busy pin is an input if the part used as a slave ($M/\overline{S}$ pin = L).

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with the $R/\overline{W}$ signal. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

SEMAPHORES

The IDT7006 is an extremely fast dual-port 16K x 8 CMOS static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the dual-port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the dual-port RAM or any other shared resource.

The dual-port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the dual-port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the dual-port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT7006 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT7006s hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT7006 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the dual-port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT7006 in a separate memory space from the dual-port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0 – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin Do is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussing on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from

that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—SOME EXAMPLES

Perhaps the simplest application of semaphores is their application as resource markers for the IDT7006's dual-port RAM. Say the 16K x 8 RAM was to be divided into two 8K x 8 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 8K of dual-port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 8K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 8K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 8K blocks of dual-port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the dual-port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

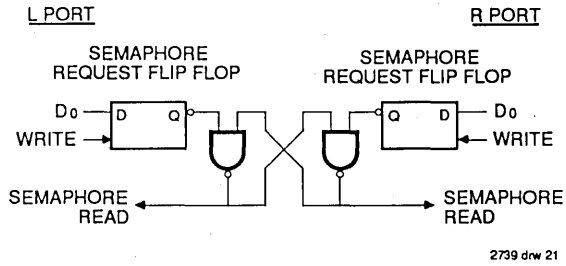
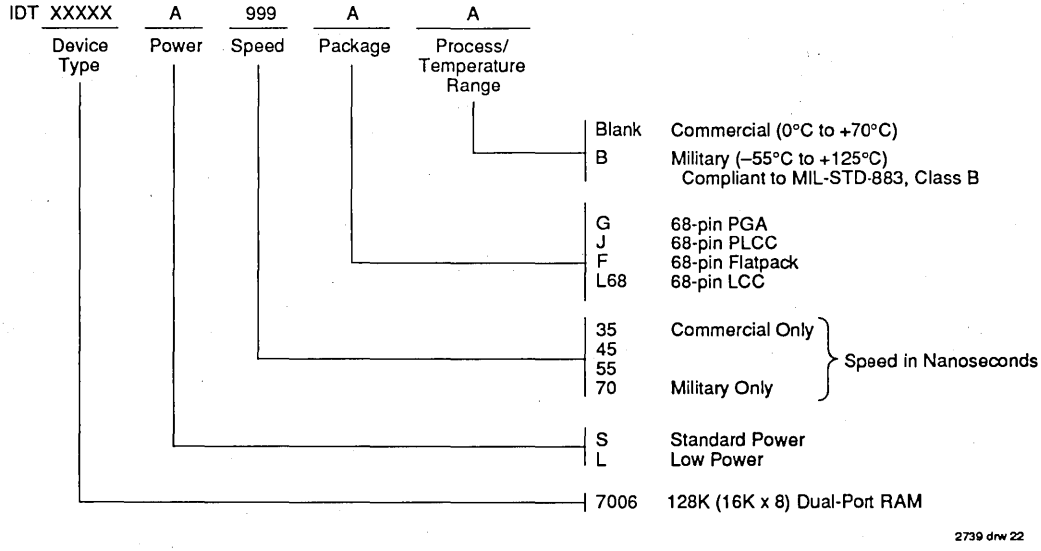


Figure 4. IDT7006 Semaphore Logic

ORDERING INFORMATION



Integrated Device Technology, Inc.

HIGH-SPEED 1K x 8 FourPort™ STATIC RAM

PRELIMINARY
IDT7050S
IDT7050L

FEATURES:

- High-speed access
  - — Military: 30/35/45ns (max.)
  - — Commercial: 25/30/35/45ns (max.)
- Low-power operation
  - — IDT7050S
    Active: 750mW (typ.)
    Standby: 10mW (typ.)
  - — IDT7050L
    Active: 750mW (typ.)
    Standby: 1.5mW (typ.)
- Fully asynchronous operation from each of the four ports: P1, P2, P3, P4
- Versatile control for write-inhibit: separate $\overline{BUSY}$ input to control write-inhibit for each of the four ports
- Battery backup operation—2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in several popular hermetic and plastic packages for both through-hole and surface mount
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7050 is a high-speed 1K x 8 FourPort static RAM designed to be used in systems where multiple access in a common RAM is required. This FourPort static RAM offers increased system performance in multiprocessed systems that have a need to communicate in real time and also offers added benefit for high-speed systems in which multiple access is required in the same cycle.

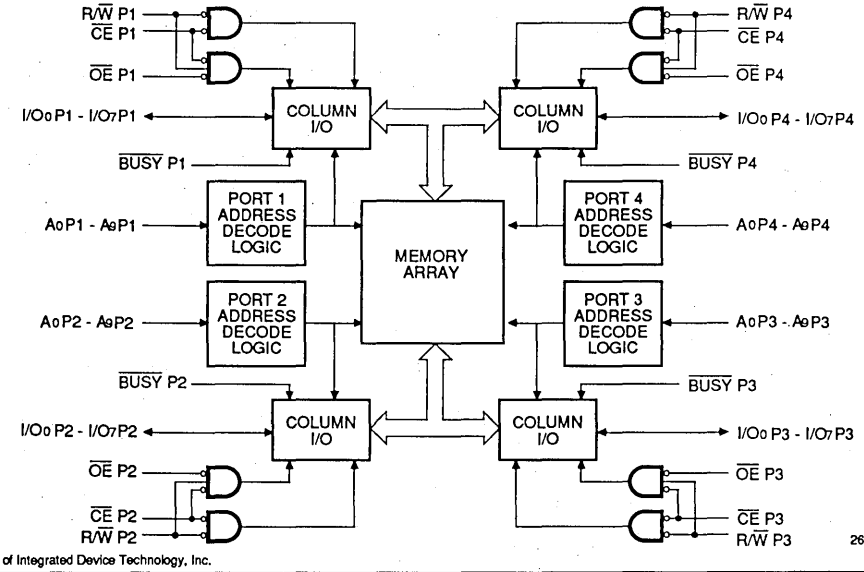
The IDT7050 is also an extremely high-speed 1K x 8 FourPort static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when all ports simultaneously access the same FourPort RAM location.

The IDT7050 provides four independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from all ports. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low power standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, this four port RAM typically operates on only 750mW of power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 50µW from a 2V battery.

The IDT7050 is packaged in either a ceramic or plastic 108-pin PGA and 132-pin quad flatpack. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM

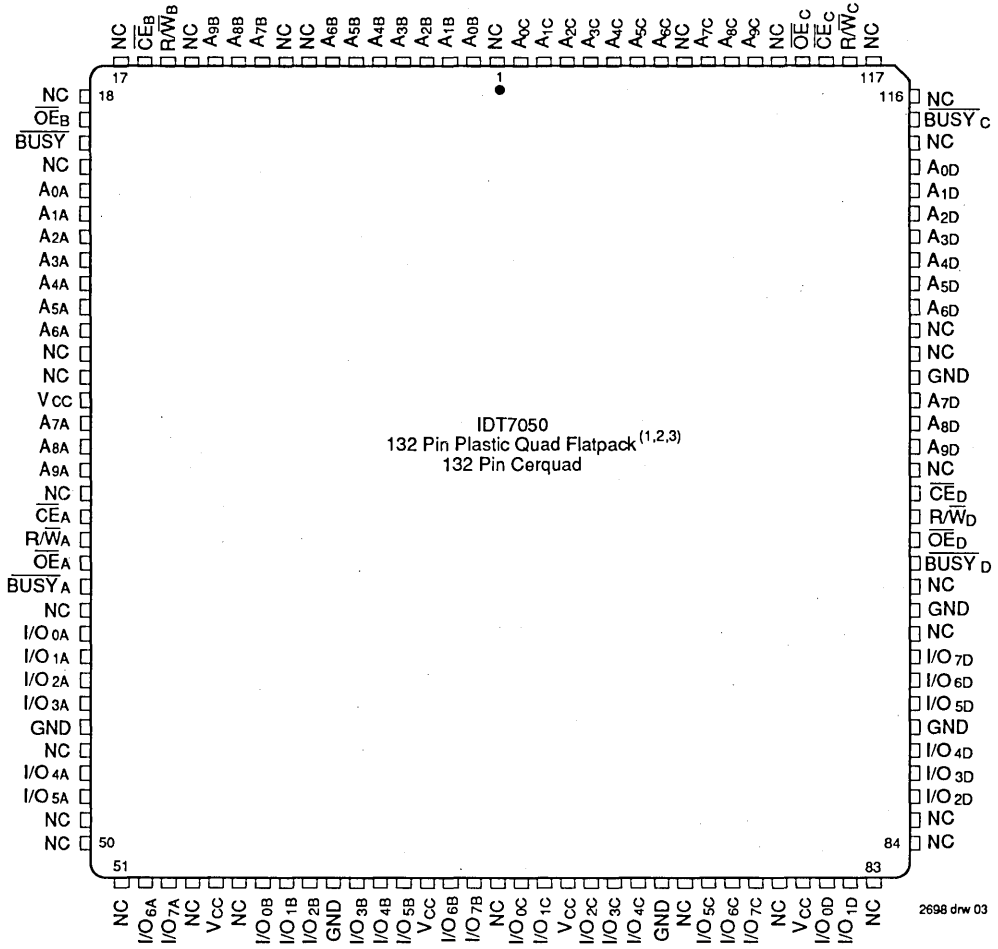


FourPort is a trademark of Integrated Device Technology, Inc.

81 $R/\overline{W}$ P2	80 NC	77 A_7 P2	74 A_5 P2	72 A_3 P2	69 A_0 P2	68 A_0 P3	65 A_3 P3	63 A_5 P3	60 A_7 P3	57 NC	54 $R/\overline{W}$ P3	12
84 $\overline{BUSY}$ P2	83 $\overline{OE}$ P2	78 A_8 P2	76 NC	73 A_4 P2	70 A_1 P2	67 A_1 P3	64 A_4 P3	61 NC	59 A_8 P3	56 $\overline{OE}$ P3	53 $\overline{BUSY}$ P3	11
87 A_2 P1	86 A_1 P1	82 $\overline{CE}$ P2	79 A_9 P2	75 A_6 P2	71 A_2 P2	66 A_2 P3	62 A_6 P3	58 A_9 P3	55 $\overline{CE}$ P3	51 A_1 P4	50 A_2 P4	10
90 A_5 P1	88 A_3 P1	85 A_0 P1							52 A_0 P4	49 A_3 P4	47 A_5 P4	09
92 NC	91 A_6 P1	89 A_4 P1							48 A_4 P4	46 A_6 P4	45 NC	08
95 A_8 P1	94 A_7 P1	93 V_{CC}			IDT7050 108 Pin PGA (1,2,3)				44 GND	43 A_7 P4	42 A_8 P4	07
96 A_9 P1	97 NC	98 $\overline{CE}$ P1			TOP VIEW				39 $\overline{CE}$ P4	40 NC	41 A_9 P4	06
99 $R/\overline{W}$ P1	100 $\overline{OE}$ P1	102 I/O_0 P1							35 V_{SS}	37 $\overline{OE}$ P4	38 $R/\overline{W}$ P4	05
101 $\overline{BUSY}$ P1	103 I/O_1 P1	106 GND							31 GND	34 I/O_7 P4	36 $\overline{BUSY}$ P4	04
104 I/O_2 P1	105 I/O_3 P1	1 I/O_6 P1	4 V_{CC}	8 GND	12 V_{CC}	17 V_{CC}	21 GND	25 V_{CC}	28 I/O_2 P4	32 I/O_5 P4	33 I/O_6 P4	03
107 I/O_4 P1	2 I/O_7 P1	5 I/O_0 P2	7 I/O_2 P2	10 I/O_4 P2	13 I/O_6 P2	16 I/O_1 P3	19 I/O_3 P3	22 I/O_5 P3	24 I/O_7 P3	29 I/O_3 P4	30 I/O_4 P4	02
108 I/O_5 P1	3 NC	6 I/O_1 P2	9 I/O_3 P2	11 I/O_5 P2	14 I/O_7 P2	15 I/O_0 P3	18 I/O_2 P3	20 I/O_4 P3	23 I/O_6 P3	26 I/O_0 P4	27 I/O_1 P4	01
A	B	C	D	E	F	G	H	J	K	L	M	

2698 drw 02

NOTES:
1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. NC denotes no - connect pin.



NOTES:
1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. NC denotes no - connect pin.

PIN CONFIGURATIONS

Symbol	Pin Name
A_0 P1 – A_9 P1	Address Lines – Port 1
A_0 P2 – A_9 P2	Address Lines – Port 2
A_0 P3 – A_9 P3	Address Lines – Port 3
A_0 P4 – A_9 P4	Address Lines – Port 4
I/O_0 P1 – I/O_7 P1	Data I/O – Port 1
I/O_0 P2 – I/O_7 P2	Data I/O – Port 2
I/O_0 P3 – I/O_7 P3	Data I/O – Port 3
I/O_0 P4 – I/O_7 P4	Data I/O – Port 4
$R/\overline{W}$ P1	Read/Write – Port 1
$R/\overline{W}$ P2	Read/Write – Port 2
$R/\overline{W}$ P3	Read/Write – Port 3
$R/\overline{W}$ P4	Read/Write – Port 4
GND	Ground
$\overline{CE}$ P1	Chip Enable – Port 1
$\overline{CE}$ P2	Chip Enable – Port 2
$\overline{CE}$ P3	Chip Enable – Port 3
$\overline{CE}$ P4	Chip Enable – Port 4
$\overline{OE}$ P1	Output Enable – Port 1
$\overline{OE}$ P2	Output Enable – Port 2
$\overline{OE}$ P3	Output Enable – Port 3
$\overline{OE}$ P4	Output Enable – Port 4
$\overline{BUSY}$ P1	Write Disable – Port 1
$\overline{BUSY}$ P2	Write Disable – Port 2
$\overline{BUSY}$ P3	Write Disable – Port 3
$\overline{BUSY}$ P4	Write Disable – Port 4
Vcc	Power
GND	Ground

2698 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2698 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE: 2698 tbl 03

1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2698 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE: 2698 tbl 05

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

7

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7050S		IDT7050L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2698 tbl 06

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1, 2, 6] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		IDT7050x25[3]		IDT7050x30		IDT7050x35		IDT7050x45		Unit
					Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
I_{CC1}	Operating Power Supply Current (All Ports Active)	$\overline{CE} \le V_{IL}$ Outputs Open f = 0[4]	MIL.	S	—	—	150	360	150	360	150	360	mA
				L	—	—	150	300	150	300	150	300	
			COM'L.	S	150	300	150	300	150	300	150	300	
				L	150	250	150	250	150	250	150	250	
I_{CC2}	Dynamic Operating Current (All Ports Active)	$\overline{CE} \le V_{IL}$ Outputs Open f = f_{MAX}[5]	MIL.	S	—	—	220	400	210	395	195	390	mA
				L	—	—	190	335	180	330	170	325	
			COM'L.	S	225	350	220	340	210	335	195	330	
				L	195	305	190	295	180	290	170	285	
I_{SB}	Standby Current (All Ports — TTL Level Inputs)	$\overline{CE} \ge V_{IH}$ f = f_{MAX}[5]	MIL.	S	—	—	45	115	40	110	35	105	mA
				L	—	—	40	85	35	80	30	75	
			COM'L.	S	60	85	45	80	40	75	35	70	
				L	50	70	40	65	35	60	30	55	
I_{SB1}	Full Standby Current (All Ports — All CMOS Level Inputs)	All Ports $\overline{CE} \ge V_{CC}$ - 0.2V	MIL.	S	—	—	1.5	30	1.5	30	1.5	30	mA
				L	—	—	.3	4.5	.3	4.5	.3	4.5	
		$V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le$ 0.2V, f = 0[4]	COM'L.	S	1.5	15	1.5	15	1.5	15	1.5	15	
				L	.3	1.5	.3	1.5	.3	1.5	.3	1.5	

2698 tbl 07

NOTES:
1. "x" in part number indicates power rating (S or L).
2. V_{CC} = 5V, T_A = +25°C for Typ.
3. 0°C to +70°C temperature range only.
4. f = 0 means no address or control lines change.
5. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
6. For the case of one port, divide the appropriate current by four.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES[1]

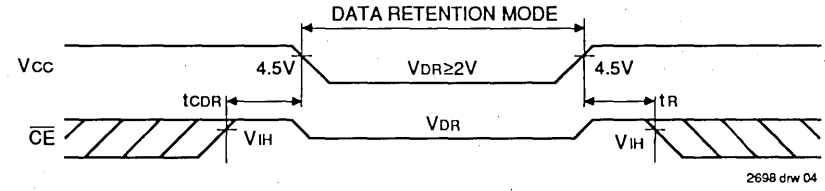
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \ge V_{HC}$	MIL.	—	25	1800	µA
		$V_{IN} \ge V_{HC}$ or $\le V_{LC}$	COM'L.	—	25	600	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

2698 tbl 08

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW Vcc DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2698 tbl 09

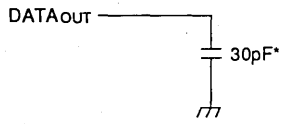


Figure 1. Output Load

*Including scope and jig

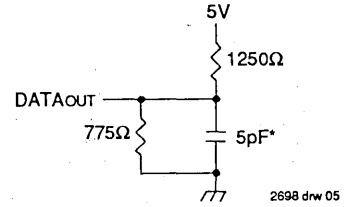


Figure 2. Output Load
(for tLZ, tHZ, twz, tow)

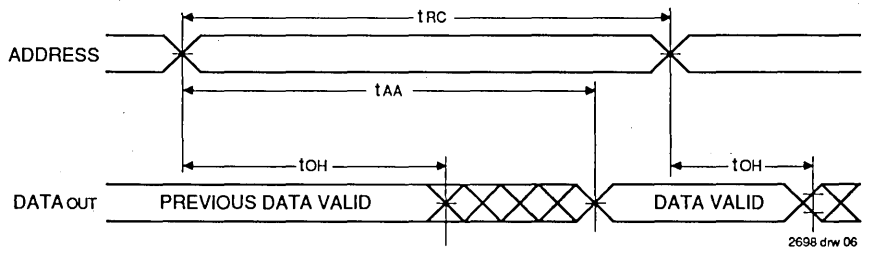
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Symbol	Parameter	IDT7050S25[1,3] IDT7050L25[1,3] Min.	Max.	IDT7050S30 IDT7050L30 Min.	Max.	IDT7050S35 IDT7050L35 Min.	Max.	IDT7050S45 IDT7050L45 Min.	Max.	Unit
READ CYCLE										
tRC	Read Cycle Time	25	—	30	—	35	—	45	—	ns
tAA	Address Access Time	—	25	—	30	—	35	—	45	ns
tACE	Chip Enable Access Time	—	25	—	30	—	35	—	45	ns
tAOE	Output Enable Access Time	—	15	—	20	—	25	—	30	ns
tOH	Output Hold from Address Change	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time[1, 2]	3	—	3	—	5	—	5	—	ns
tHZ	Output High Z Time[1, 2]	—	15	—	15	—	15	—	20	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	20	—	30	—	50	—	50	ns

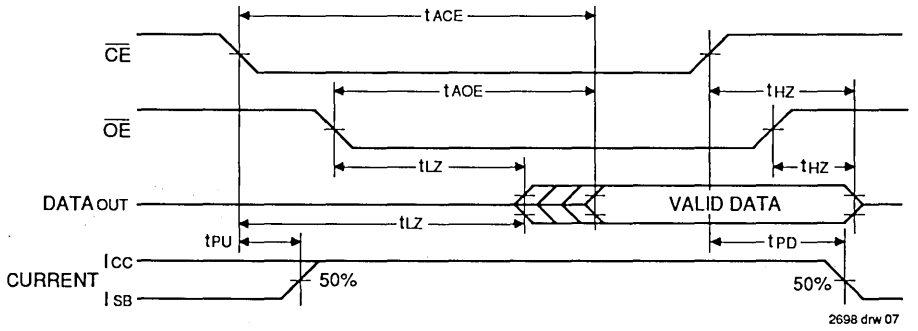
2698 tbl 10

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. 0°C to +70°C temperature range only.

TIMING WAVEFORM OF READ CYCLE NO. 1, ANY PORT(1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 2, ANY PORT(1, 3)



NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = V_{IL}.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

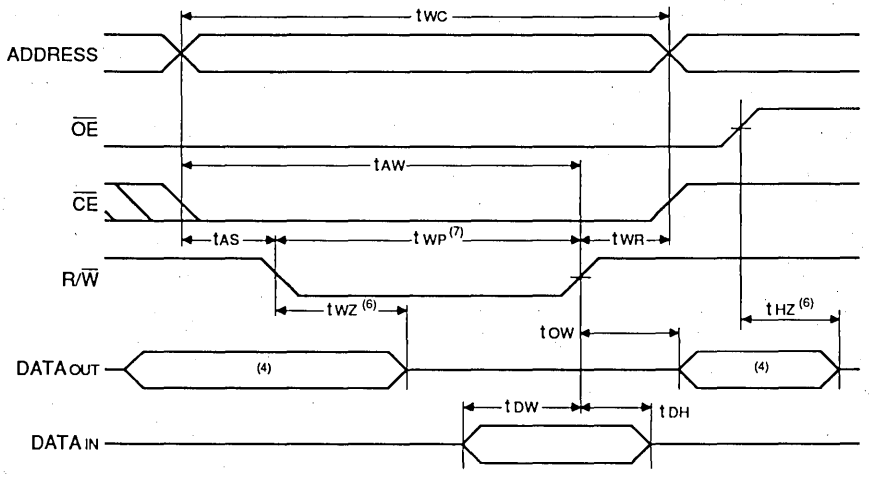
Symbol	Parameter	IDT7050S25[7] IDT7050L25[7]		IDT7050S30 IDT7050L30		IDT7050S35 IDT7050L35		IDT7050S45 IDT7050L45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
tWC	Write Cycle Time	25	—	30	—	35	—	45	—	ns
tEW	Chip Enable to End of Write	20	—	25	—	30	—	35	—	ns
tAW	Address Valid to End of Write	20	—	25	—	30	—	35	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width[3]	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	5	—	5	—	5	—	5	—	ns
tDW	Data Valid to End of Write	15	—	15	—	20	—	20	—	ns
tHZ	Output High Z Time[1, 2]	—	15	—	15	—	15	—	20	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z[1, 2]	—	15	—	15	—	15	—	20	ns
tOW	Output Active from End of Write[1, 2]	0	—	0	—	0	—	0	—	ns
tWDD	Write Pulse to Data Delay[4]	—	45	—	50	—	55	—	65	ns
tDDD	Write Data Valid to Read Data Delay[4]	—	35	—	40	—	45	—	55	ns
BUSY INPUT TIMING										
tWB	Write to $\overline{BUSY}$[5]	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[6]	15	—	20	—	20	—	20	—	ns

NOTES:

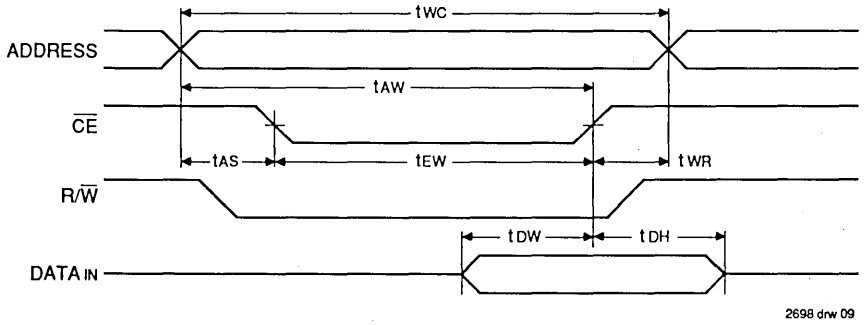
2698 tbl 11

1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. Specified for $\overline{OE}$ at high (refer to "Timing Waveform of Write Cycle", Note 7).
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read with Port-to-Port Delay".
5. To ensure that the write cycle is inhibited during contention.
6. To ensure that a write cycle is completed after contention.
7. 0°C to +70°C temperature range only.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1, 2, 3, 7)

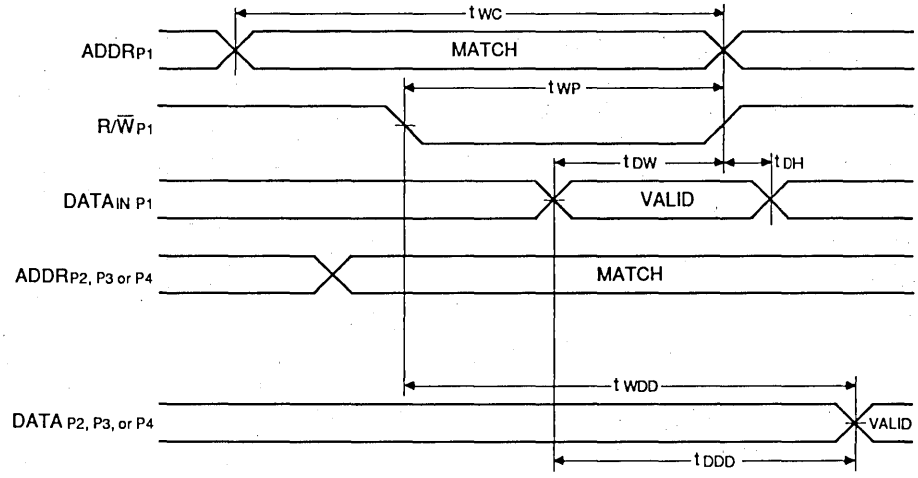


TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1, 2, 3, 5)



NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP .

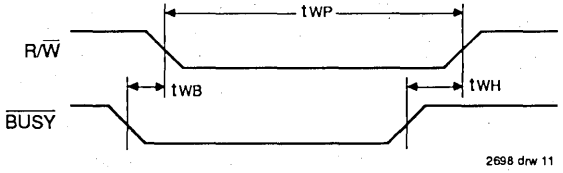
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY(1, 2, 3)



2698 drw 10

NOTES:
1. Assume $\overline{BUSY}$ input at HI and $\overline{CE}$ at LO for the writing port.
2. Write cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for any of the reading ports which has its $\overline{OE}$ at LO.

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ INPUT



2698 drw 11

7

FUNCTIONAL DESCRIPTION

The IDT7050 provides four ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. READ/WRITE conditions are illustrated in the table below.

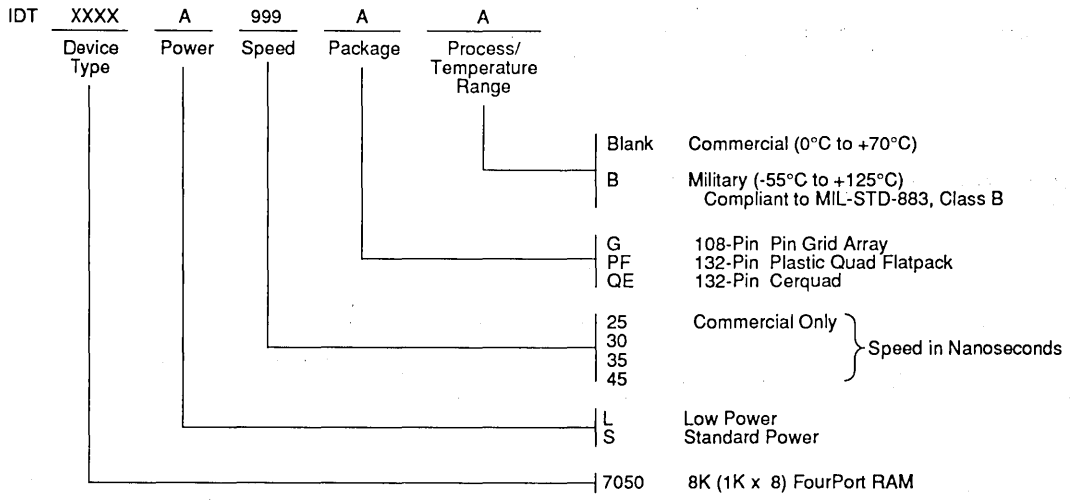
TABLE I – READ/WRITE CONTROL

Any Port[1]				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	Function
X	H	X	Z	Port Disabled and in Power Down Mode
X	H	X	Z	$\overline{CE}_{P1} = \overline{CE}_{P2} = \overline{CE}_{P3} = \overline{CE}_{P4}$ = H Power Down Mode, I_{SB1} or I_{SB}
L	L	X	$DATA_{IN}$	Data on port written into memory[2, 3]
H	L	L	$DATA_{OUT}$	Data in memory output on port
X	X	H	Z	High impedance outputs

2698 tbl 12

NOTES:
1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance
2. If $\overline{BUSY}$ = LOW, data is not written.
3. For valid write operation, no more than one port can write to the same address location at the same time.

ORDERING INFORMATION



2698 drw 12

Integrated Device Technology, Inc.

HIGH-SPEED 2K x 8 FourPort™ STATIC RAM

PRELIMINARY
IDT7052S
IDT7052L

FEATURES:

- High-speed access
  - — Military: 30/35/45ns (max.)
  - — Commercial: 25/30/35/45ns (max.)
- Low-power operation
  - — IDT7052S
    Active: 750mW (typ.)
    Standby: 10mW (typ.)
  - — IDT7052L
    Active: 750mW (typ.)
    Standby: 1.5mW (typ.)
- Fully asynchronous operation from each of the four ports: P1, P2, P3, P4
- Versatile control for write-inhibit: separate $\overline{BUSY}$ input to control write-inhibit for each of the four ports
- Battery backup operation—2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in several popular hermetic and plastic packages for both through-hole and surface mount
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7052 is a high-speed 2K x 8 FourPort static RAM designed to be used in systems where multiple access in a common RAM is required. This FourPort static RAM offers increased system performance in multiprocessed systems that have a need to communicate in real time and also offers added benefit for high-speed systems in which multiple access is required in the same cycle.

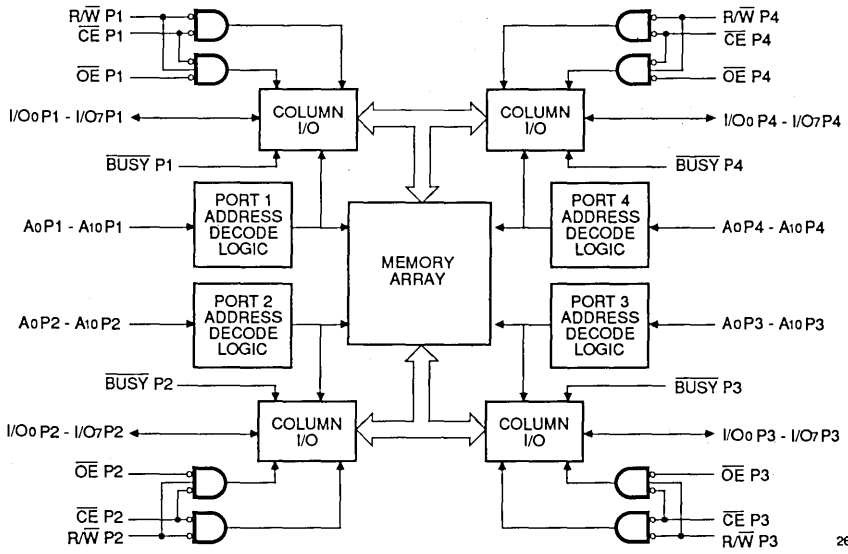
The IDT7052 is also an extremely high-speed 2K x 8 FourPort static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when all ports simultaneously access the same FourPort RAM location.

The IDT7052 provides four independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from all ports. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low power standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, this four port RAM typically operates on only 750mW of power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 50µW from a 2V battery.

The IDT7052 is packaged in either a ceramic or plastic 108-pin PGA and 132-pin quad flatpack. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM

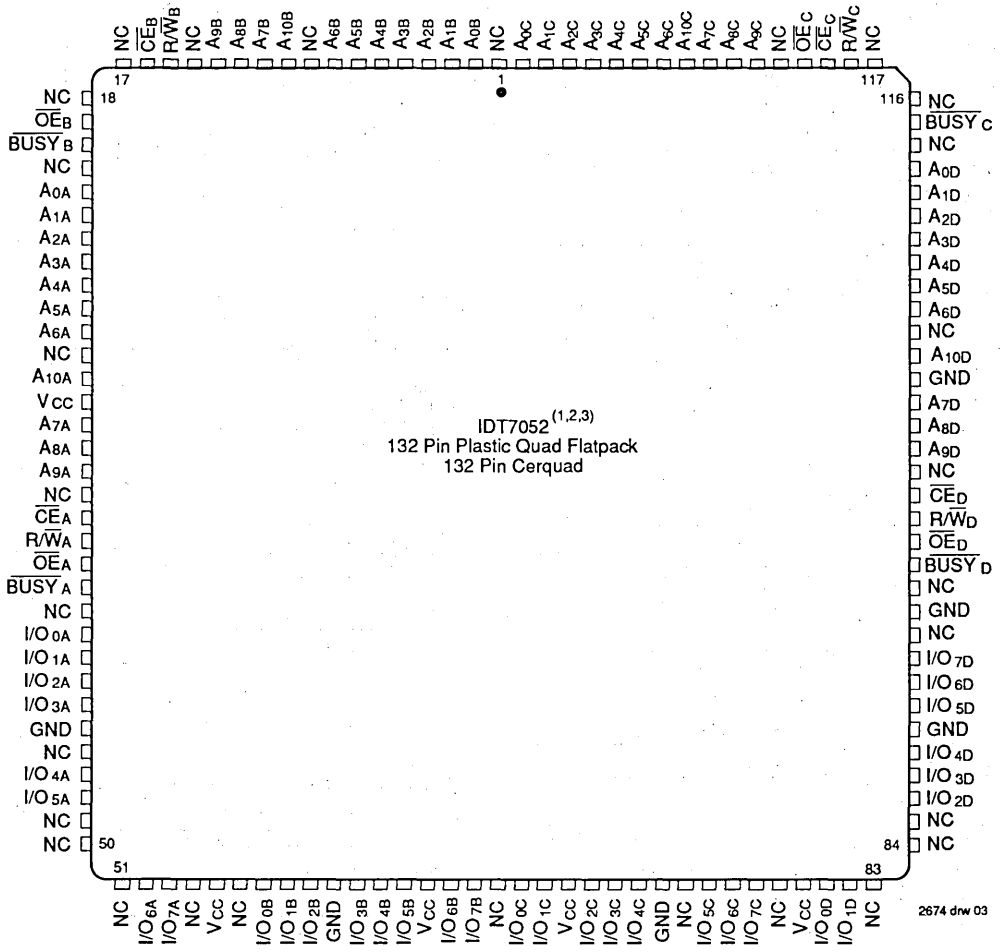


FourPort is a trademark of Integrated Device Technology, Inc.

A	B	C	D	E	F	G	H	J	K	L	M	
81 R/$\overline{W}$ P2	80 NC	77 A_7 P2	74 A_5 P2	72 A_3 P2	69 A_0 P2	68 A_0 P3	65 A_3 P3	63 A_5 P3	60 A_7 P3	57 NC	54 R/$\overline{W}$ P3	12
84 $\overline{BUSY}$ P2	83 $\overline{OE}$ P2	78 A_8 P2	76 A_{10} P2	73 A_4 P2	70 A_1 P2	67 A_1 P3	64 A_4 P3	61 A_{10} P3	59 A_8 P3	56 $\overline{OE}$ P3	53 $\overline{BUSY}$ P3	11
87 A_2 P1	86 A_1 P1	82 $\overline{CE}$ P2	79 A_9 P2	75 A_6 P2	71 A_2 P2	66 A_2 P3	62 A_6 P3	58 A_9 P3	55 $\overline{CE}$ P3	51 A_1 P4	50 A_2 P4	10
90 A_5 P1	88 A_3 P1	85 A_0 P1							52 A_0 P4	49 A_3 P4	47 A_5 P4	09
92 A_{10} P1	91 A_6 P1	89 A_4 P1							48 A_4 P4	46 A_6 P4	45 A_{10} P4	08
95 A_8 P1	94 A_7 P1	93 V_{CC}			IDT7052 108-Pin PGA(1,2,3)				44 GND	43 A_7 P4	42 A_8 P4	07
96 A_9 P1	97 NC	98 $\overline{CE}$ P1			TOP VIEW				39 $\overline{CE}$ P4	40 NC	41 A_9 P4	06
99 R/$\overline{W}$ P1	100 $\overline{OE}$ P1	102 I/O_0 P1							35 GND	37 $\overline{OE}$ P4	38 R/$\overline{W}$ P4	05
101 $\overline{BUSY}$ P1	103 I/O_1 P1	106 GND							31 GND	34 I/O_7 P4	36 $\overline{BUSY}$ P4	04
104 I/O_2 P1	105 I/O_3 P1	1 I/O_6 P1	4 V_{CC}	8 GND	12 V_{CC}	17 V_{CC}	21 GND	25 V_{CC}	28 I/O_2 P4	32 I/O_5 P4	33 I/O_6 P4	03
107 I/O_4 P1	2 I/O_7 P1	5 I/O_0 P2	7 I/O_2 P2	10 I/O_4 P2	13 I/O_6 P2	16 I/O_1 P3	19 I/O_3 P3	22 I/O_5 P3	24 I/O_7 P3	29 I/O_3 P4	30 I/O_4 P4	02
108 I/O_5 P1	3 NC	6 I/O_1 P2	9 I/O_3 P2	11 I/O_5 P2	14 I/O_7 P2	15 I/O_0 P3	18 I/O_2 P3	20 I/O_4 P3	23 I/O_6 P3	26 I/O_0 P4	27 I/O_1 P4	01

2674 drw 02

NOTES:
1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. NC denotes no-connect pin.



NOTES:
1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. NC denotes no-connect pin.

7

PIN CONFIGURATIONS

Symbol	Pin Name
A_0 P1 – A_{10} P1	Address Lines – Port 1
A_0 P2 – A_{10} P2	Address Lines – Port 2
A_0 P3 – A_{10} P3	Address Lines – Port 3
A_0 P4 – A_{10} P4	Address Lines – Port 4
I/O_0 P1 – I/O_7 P1	Data I/O – Port 1
I/O_0 P2 – I/O_7 P2	Data I/O – Port 2
I/O_0 P3 – I/O_7 P3	Data I/O – Port 3
I/O_0 P4 – I/O_7 P4	Data I/O – Port 4
$R/\overline{W}$ P1	Read/Write – Port 1
$R/\overline{W}$ P2	Read/Write – Port 2
$R/\overline{W}$ P3	Read/Write – Port 3
$R/\overline{W}$ P4	Read/Write – Port 4
GND	Ground
$\overline{CE}$ P1	Chip Enable – Port 1
$\overline{CE}$ P2	Chip Enable – Port 2
$\overline{CE}$ P3	Chip Enable – Port 3
$\overline{CE}$ P4	Chip Enable – Port 4
$\overline{OE}$ P1	Output Enable – Port 1
$\overline{OE}$ P2	Output Enable – Port 2
$\overline{OE}$ P3	Output Enable – Port 3
$\overline{OE}$ P4	Output Enable – Port 4
$\overline{BUSY}$ P1	Write Disable – Port 1
$\overline{BUSY}$ P2	Write Disable – Port 2
$\overline{BUSY}$ P3	Write Disable – Port 3
$\overline{BUSY}$ P4	Write Disable – Port 4
Vcc	Power
GND	Ground

2674 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2674 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE: 2674 tbl 03

1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2674 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE: 2674 tbl 05

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7052S		IDT7052L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2674 tbl 06

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1, 2, 6] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		IDT7052x25[3]		IDT7052x30		IDT7052x35		IDT7052x45		Unit
					Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
I_{CC1}	Operating Power Supply Current (All Ports Active)	$\overline{CE} \le V_{IL}$ Outputs Open f = 0[4]	MIL.	S	—	—	150	360	150	360	150	360	mA
				L	—	—	150	300	150	300	150	300	
			COM'L.	S	150	300	150	300	150	300	150	300	
				L	150	250	150	250	150	250	150	250	
I_{CC2}	Dynamic Operating Current (All Ports Active)	$\overline{CE} \le V_{IL}$ Outputs Open f = f_{MAX}[5]	MIL.	S	—	—	220	400	210	395	195	390	mA
				L	—	—	190	335	180	330	170	325	
			COM'L.	S	225	350	220	340	210	335	195	330	
				L	195	305	190	295	180	290	170	285	
I_{SB}	Standby Current (All Ports — TTL Level Inputs)	$\overline{CE} \ge V_{IH}$ f = f_{MAX}[5]	MIL.	S	—	—	45	115	40	110	35	105	mA
				L	—	—	40	85	35	80	30	75	
			COM'L.	S	60	85	45	80	40	75	35	70	
				L	50	70	40	65	35	60	30	55	
I_{SB1}	Full Standby Current (All Ports — All CMOS Level Inputs)	All Ports $\overline{CE} \ge V_{CC}$ - 0.2V	MIL.	S	—	—	1.5	30	1.5	30	1.5	30	mA
				L	—	—	.3	4.5	.3	4.5	.3	4.5	
		$V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le$ 0.2V, f = 0[4]	COM'L.	S	1.5	15	1.5	15	1.5	15	1.5	15	
				L	.3	1.5	.3	1.5	.3	1.5	.3	1.5	

NOTES:
2674 tbl 07

1. "x" in part number indicates power rating (S or L).
2. V_{CC} = 5V, T_A = +25°C for Typ.
3. 0°C to +70°C temperature range only.
4. f = 0 means no address or control lines change.
5. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
6. For the case of one port, divide the above appropriate current by four.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES[1]

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

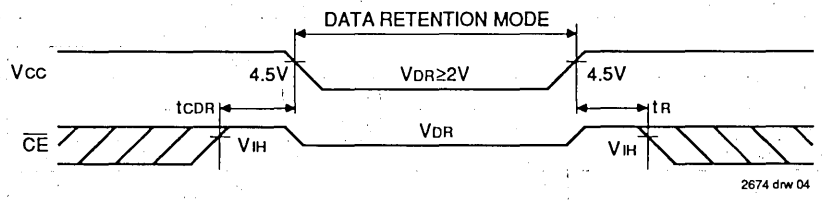
Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \ge V_{HC}$	MIL.	—	25	1800	µA
		$V_{IN} \ge V_{HC}$ or $\le V_{LC}$	COM'L.	—	25	600	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:
2674 tbl 08

1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

7

LOW Vcc DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2674 tbl 09

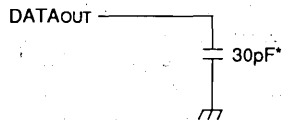


Figure 1. Output Load

*Including scope and jig

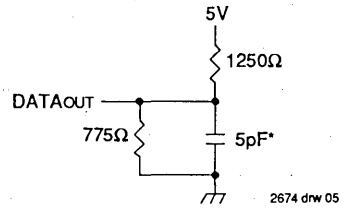


Figure 2. Output Load
(for tLZ, tHZ, tWZ, tOW)

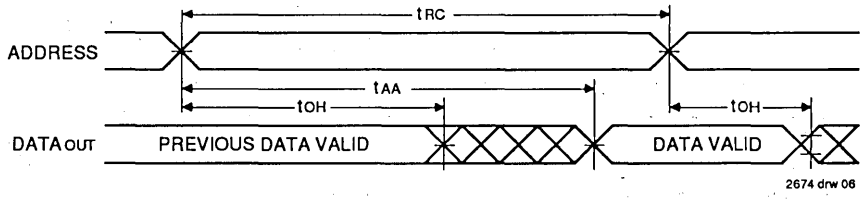
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Symbol	Parameter	IDT7052S25[1] IDT7052L25[1] Min.	Max.	IDT7052S30 IDT7052L30 Min.	Max.	IDT7052S35 IDT7052L35 Min.	Max.	IDT7052S45 IDT7052L45 Min.	Max.	Unit
READ CYCLE										
tRC	Read Cycle Time	25	—	30	—	35	—	45	—	ns
tAA	Address Access Time	—	25	—	30	—	35	—	45	ns
tACE	Chip Enable Access Time	—	25	—	30	—	35	—	45	ns
tAOE	Output Enable Access Time	—	15	—	20	—	25	—	30	ns
tOH	Output Hold from Address Change	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time[1, 2]	3	—	3	—	5	—	5	—	ns
tHZ	Output High Z Time[1, 2]	—	15	—	15	—	15	—	20	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	20	—	30	—	50	—	50	ns

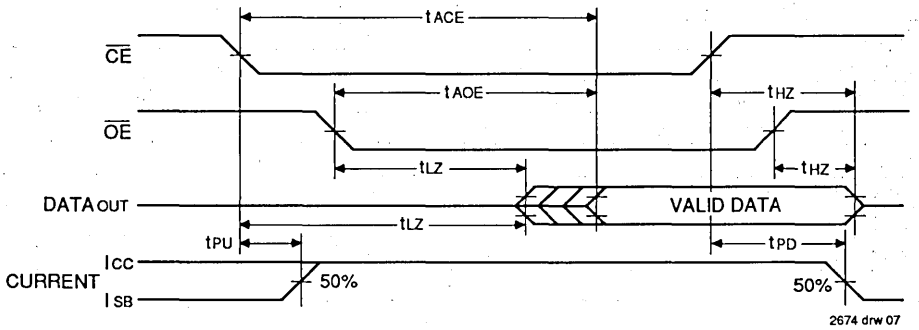
2674 tbl 10

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. 0°C to +70°C temperature range only.

TIMING WAVEFORM OF READ CYCLE NO. 1, ANY PORT(1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 2, ANY PORT(1, 3)



NOTES:
1. R/W is high for Read Cycles.
2. Device is continuously enabled, CE = VIL.
3. Addresses valid prior to or coincident with CE transition low.
4. OE = VIL.

7

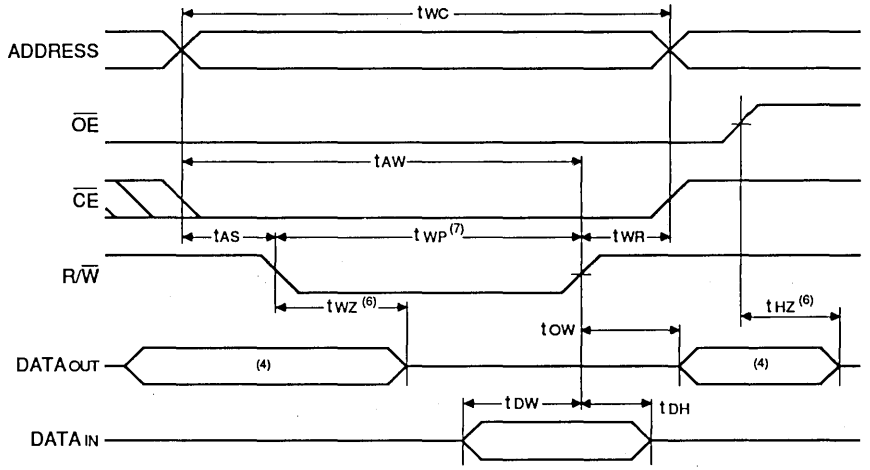
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Symbol	Parameter	IDT7052S25[7] IDT7052L25[7]		IDT7052S30 IDT7052L30		IDT7052S35 IDT7052L35		IDT7052S45 IDT7052L45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
tWC	Write Cycle Time	25	—	30	—	35	—	45	—	ns
tEW	Chip Enable to End of Write	20	—	25	—	30	—	35	—	ns
tAW	Address Valid to End of Write	20	—	25	—	30	—	35	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width[3]	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	5	—	5	—	5	—	5	—	ns
tDW	Data Valid to End of Write	15	—	15	—	20	—	20	—	ns
tHZ	Output High Z Time[1, 2]	—	15	—	15	—	15	—	20	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z[1, 2]	—	15	—	15	—	15	—	20	ns
tOW	Output Active from End of Write[1, 2]	0	—	0	—	0	—	0	—	ns
tWDD	Write Pulse to Data Delay[4]	—	45	—	50	—	55	—	65	ns
tDDD	Write Data Valid to Read Data Delay[4]	—	35	—	40	—	45	—	55	ns
BUSY INPUT TIMING										
tWB	Write to $\overline{BUSY}$[5]	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[6]	15	—	20	—	20	—	20	—	ns

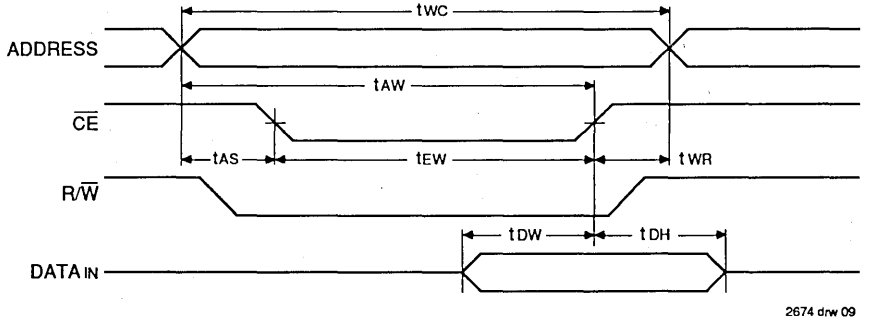
NOTES:
2698 tbl 11

1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. Specified for $\overline{OE}$ at high (refer to "Timing Waveform of Write Cycle", Note 7).
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read with Port-to-Port Delay".
5. To ensure that the write cycle is inhibited during contention.
6. To ensure that a write cycle is completed after contention.
7. 0°C to +70°C temperature range only.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1, 2, 3, 7)



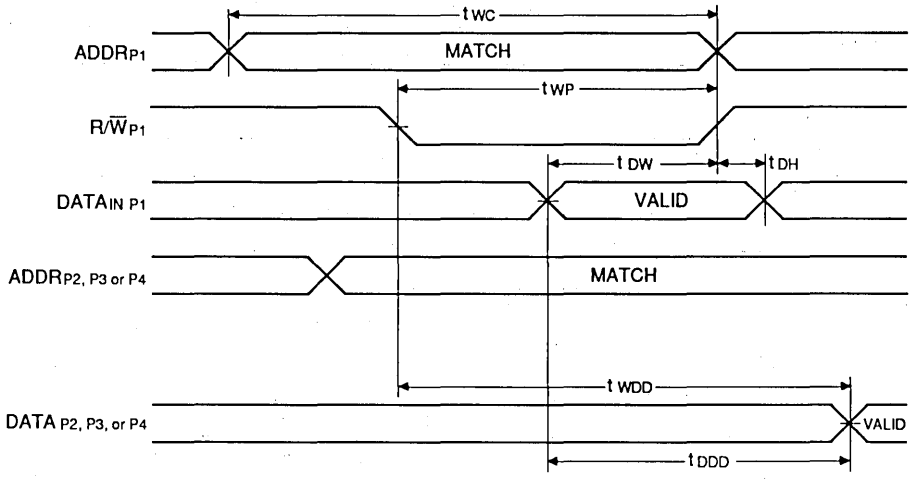
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1, 2, 3, 5)



NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

7

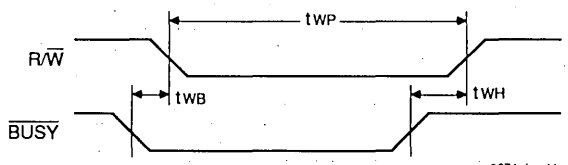
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY(1, 2, 3)



2698 drw 10

NOTES:
1. Assume $\overline{BUSY}$ input at HI and $\overline{CE}$ at LO for the writing port.
2. Write cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for any of the reading ports which has its $\overline{OE}$ at LO.

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ INPUT



2674 drw 11

FUNCTIONAL DESCRIPTION

The IDT7052 provides four ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. READ/WRITE conditions are illustrated in the table below.

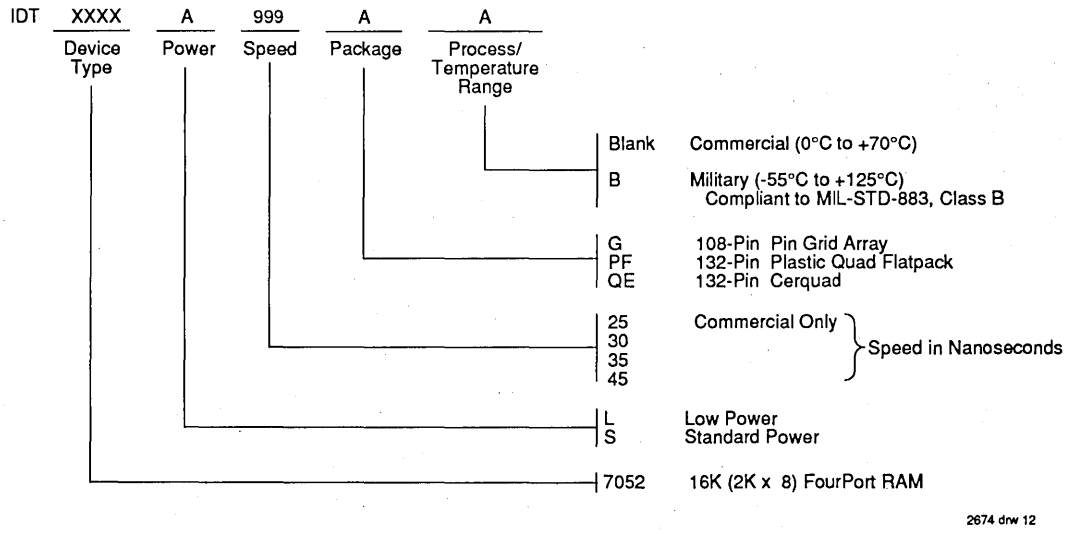
TABLE I – READ/WRITE CONTROL

Any Port[1]				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	Function
X	H	X	Z	Port Disabled and in Power Down Mode
X	H	X	Z	$\overline{CE}_{P1} = \overline{CE}_{P2} = \overline{CE}_{P3} = \overline{CE}_{P4}$ = H Power Down Mode, I_{SB} or I_{SB1}
L	L	X	$DATA_{IN}$	Data on port written into memory[2, 3]
H	L	L	$DATA_{OUT}$	Data in memory output on port
X	X	H	Z	High impedance outputs

NOTES: 2698 tbl 12

1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance
2. If $\overline{BUSY}$ = LOW, data is not written.
3. For valid write operation, no more than one port can write to the same address location at the same time.

ORDERING INFORMATION



2674 drw 12

7

Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (4K x 16-BIT) REGISTERED RAM w/SPC™

IDT 71502S
IDT 71502L

FEATURES:

- 4K x 16 RAM with registered outputs, serial or parallel load and readback capability in only 48 pins
- Serial Protocol Channel allows serial load and readback of RAM over a 4-wire channel
- RAM address counter speeds RAM load and readback
- Outputs may be programmed to be registered or non-registered in groups of 8 bits
- Initialize register allows initial microword selection
- Synchronous and asynchronous output enables allow for depth expansion and bus driving
- Programmable chip selects enable depth & width expansion without any external decode logic
- Breakpoint comparator supports system diagnostics
- Parity check on outputs for high reliability designs
- High-speed (address set-up before clock)
  - Military: 35/45/55ns (max.)
  - Commercial: 25/35/45ns (max.)
- Low-power consumption
  - IDT71502S - Active: 750mW (typ.)
  - IDT71502L - Active: 600mW (typ.)
- Input and output directly TTL-compatible
- Standard 48-pin DIP, 48-pin LCC and 52-pin PLCC.
- Military product 100% compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71502 Registered RAM is a 65,536 bits high speed static RAM organized as 4K x 16, with a high speed register at the RAM outputs and serial load and readback capability using the IDT Serial Protocol Channel, SPC™.

This device is the first in a family of multifeatured RAM's with a built-in Serial Protocol Channel SPC™ letting the user set the best configuration for his system:

- SELF-ADDRESSING RAM
- WRITABLE CONTROL STORE
- LOGIC ANALYZER/RECORDER

The 71502 is fabricated using IDT's high-performance, high-reliability technology—CEMOS™. This technology gives the 71502 the combination of low power, high speed, and high density that makes it a cost effective solution.

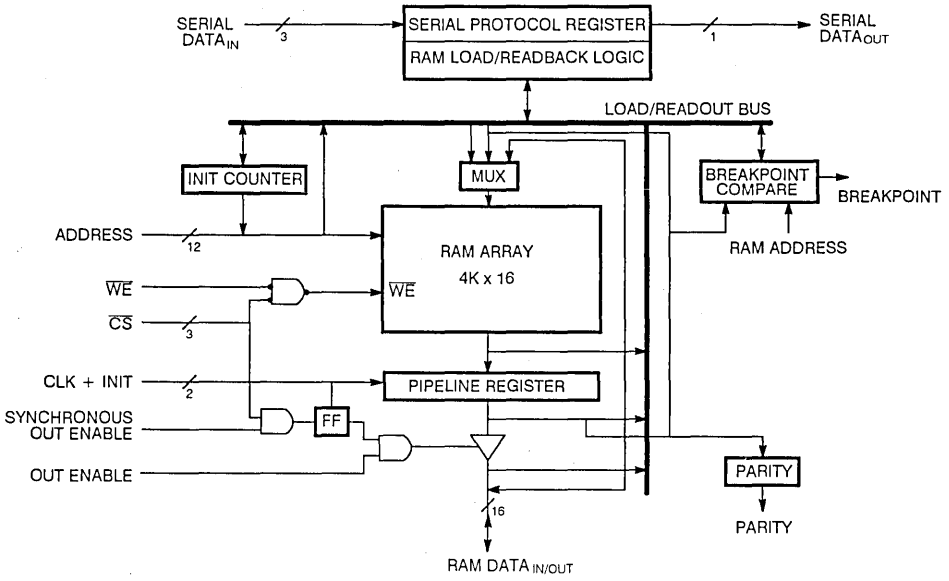
The IDT71502 is available with address set up before clock times as fast as 25ns. These times are available with a maximum power consumption of only 1.6W.

All inputs and outputs of the IDT71502 are TTL-compatible, and the device operates from a single 5V supply. Fully static, asynchronous circuitry is used, requiring no clocks (with the exception of the register clock) or refreshing for operation.

The IDT71502 is packaged in plastic and ceramic versions of either a 48-pin, 600 mil DIP; a 48-pin leadless chip carrier, or a 52-pin plastic leadless chip carrier providing high board level packing densities.

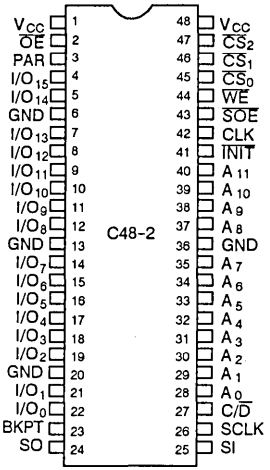
The IDT71502 is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004.

FUNCTIONAL BLOCK DIAGRAM



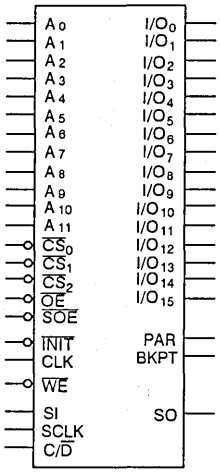
CEMOS is a trademark of Integrated Device Technology, Inc.

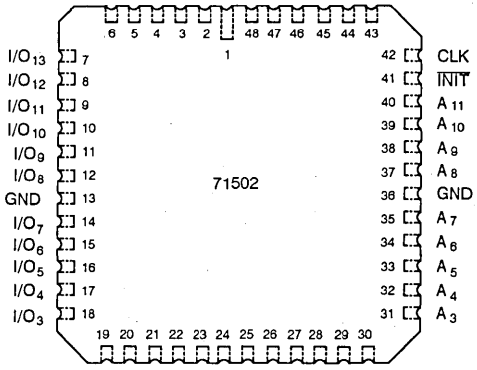
PIN CONFIGURATION



DIP
TOP VIEW

LOGIC SYMBOL



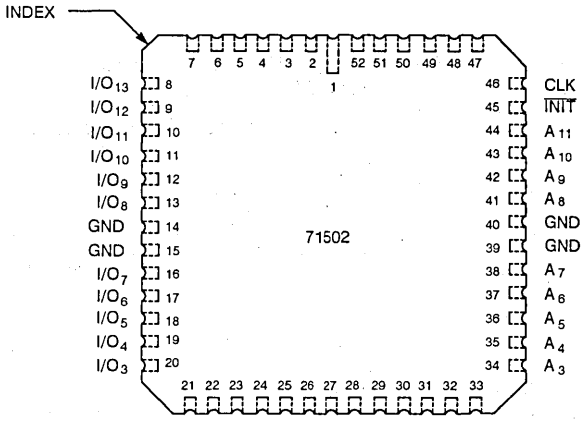


LCC PINOUT
TOP VIEW

PIN NAMES

NAME	FUNCTION
A_{0-11}	Address
I/O_{0-15}	Data Input/Output
$\overline{CS}_{0-2}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{SOE}$	Synchronous Output Enable
CLK	Clock (to register)
$\overline{INIT}$	Initialize
BKPT	Breakpoint Detect
PAR	Parity
SI	SPC Serial $DATA_{IN}$ (1)
SO	SPC Serial $DATA_{OUT}$ (1)
SCLK	SPC Clock (1)
$C/\overline{D}$	SPC Command/$\overline{Data}$ (1)
GND	Ground
V_{CC}	Power

NOTE:
1. The Serial Protocol Channel (SPC) is discussed at length in IDT Application Note 16.



PLCC PINOUT
TOP VIEW

7

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE(1) (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:

1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

TRUTH TABLE - READ/WRITE OPERATIONS STANDARD PIPELINED MODE

MODE	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{SOE}$	CLK	I/O OPERATION
Deselected	H	X	L	X	↓	High Z
Read	L	H	H	X	X	High Z
Read	L	H	L	H	↓	High Z
Read	L	H	L	L	↓	$DATA_{OUT}$ @ Address
Write	L	L	X	X	X	$DATA_{IN}$ @ Address

TRUTH TABLE - SPC OPERATIONS

MODE	C/$\overline{D}$	SCLK	FUNCTION
Command	H	↓	Shift bit into command register
Data	L	↓	Shift bit into data register
Execute	↓	↓	Execute command during time between C/$\overline{D}$ and SCLK

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS		IDT71502S MIN.	IDT71502S TYP.(1)	IDT71502S MAX.	IDT71502L MIN.	IDT71502L TYP.(1)	IDT71502L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage(2)	I_{OL} = 16mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
V_{OH}	Output High Voltage(2)	I_{OH} = -8mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V
V_{OL}	Output Low Voltage, BKPT	I_{OL} = 24mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V

NOTES:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.
2. All outputs except BKPT, which is open drain.

DC ELECTRICAL CHARACTERISTICS (1)

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	POWER	IDT71502S25(2, 4) IDT71502L25(2, 4) COM'L.	IDT71502S35(4) IDT71502L35(4) COM'L.	IDT71502S35(4) IDT71502L35(4) MIL.	IDT71502S45(4) IDT71502L45(4) COM'L.	IDT71502S45(4) IDT71502L45(4) MIL.	IDT71502S55(3, 4) IDT71502L55(3, 4) COM'L.	IDT71502S55(3, 4) IDT71502L55(3, 4) MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0	S	155	155	170	155	170	155	170	mA
		L	135	135	150	135	150	135	150	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX} = 1/TRC	S	280	255	270	230	245	220	235	mA
		L	250	225	240	200	215	190	205	

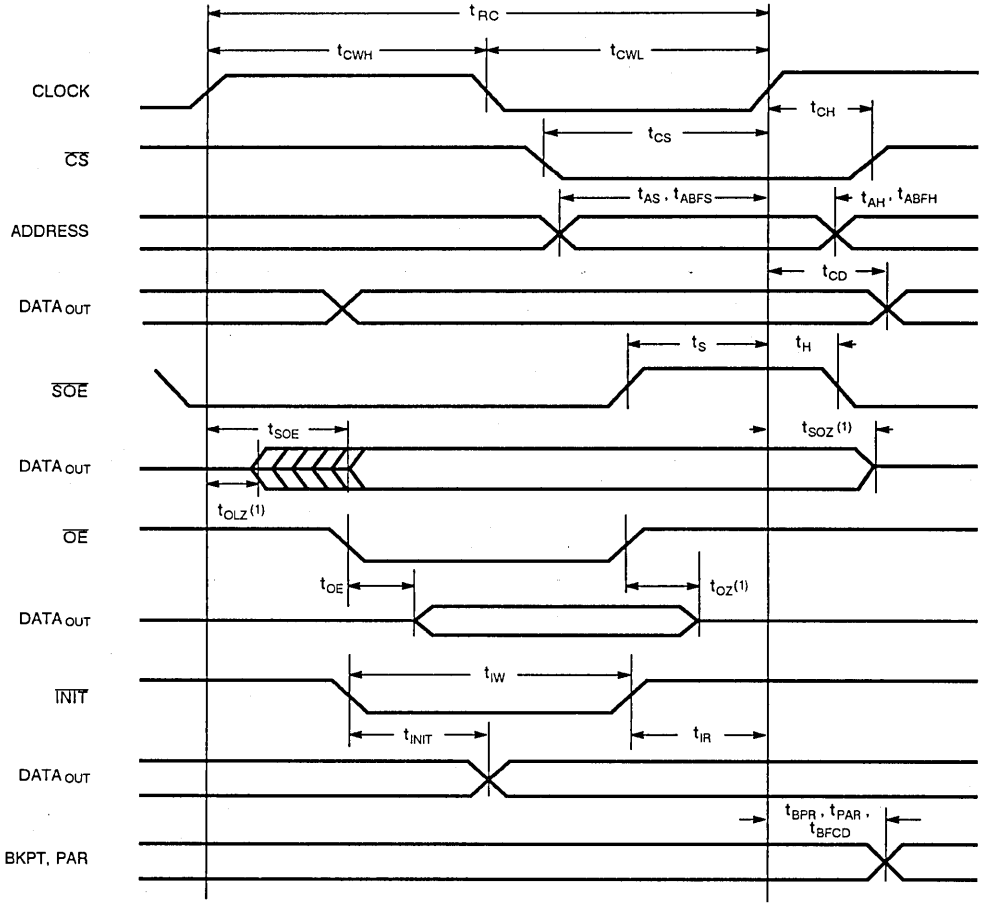
NOTES:
1. All values are guaranteed maximums.
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. Pipelined address access set-up time.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT71502S25[1,4] IDT71502L25[1,4] MIN.	MAX.	IDT71502S35[4] IDT71502L35[4] MIN.	MAX.	IDT71502S45[4] IDT71502L45[4] MIN.	MAX.	IDT71502S55[2,4] IDT71502L55[2,4] MIN.	MAX.	UNIT
READ CYCLE – PIPELINED										
t_{RC}	Read Cycle Time	40	–	50	–	65	–	80	–	ns
t_{AS}	Address Set-up Time	25	–	35	–	45	–	55	–	ns
t_{CS}	Chip Select Set-up Time	10	–	12	–	15	–	20	–	ns
t_S	Set-up Time: $\overline{SOE}$	10	–	12	–	15	–	20	–	ns
t_{AH}	Address Hold Time	0	–	0	–	0	–	0	–	ns
t_{CH}	Chip Select Hold Time	2	–	2	–	2	–	2	–	ns
t_H	Hold Time: $\overline{SOE}$	2	–	2	–	2	–	2	–	ns
t_{CD}	Clock to Output Delay	–	12	–	15	–	20	–	25	ns
t_{CWH}	Clock Width, High	15	–	15	–	20	–	20	–	ns
t_{CWL}	Clock Width, Low	15	–	15	–	20	–	20	–	ns
t_{OE}	Asynchronous Output Enable To Data Valid Time	–	12	–	15	–	20	–	25	ns
t_{OZ}	Asynchronous Output Disable Time[3,5]	–	11	–	14	–	19	–	24	ns
t_{SOE}	Synchronous Output Enable To Data Valid Time	–	12	–	15	–	20	–	25	ns
t_{SOZ}	Synchronous Output Disable Time[3,5]	–	11	–	14	–	19	–	24	ns
t_{INIT}	Initialize to Output Delay	–	45	–	50	–	65	–	80	ns
t_{IR}	Initialize Recovery Time	30	–	35	–	45	–	55	–	ns
t_{IW}	Initialize Pulse Width	30	–	35	–	45	–	55	–	ns
t_{PAR}	Parity Generation Time	–	30	–	35	–	45	–	55	ns
t_{BPR}	Breakpoint Delay From Register	–	35	–	35	–	45	–	55	ns
t_{BPA}	Breakpoint Delay From Address	–	35	–	35	–	45	–	55	ns
t_{ABFS}	Address to BKPT FF Set-up	30	–	35	–	40	–	50	–	ns
t_{ABFH}	Address to BKPT FF Hold	0	–	0	–	0	–	0	–	ns
t_{BFCD}	BKPT FF Clock to Data	–	16	–	20	–	25	–	30	ns
READ CYCLE – NON-PIPELINED										
t_{AAN}	Address Access Time	–	30	–	35	–	65	–	80	ns
t_{OLZ}	Asynchronous Output Enable Time[3,5]	2	–	2	–	2	–	2	–	ns
t_{SOEN}	Synchronous Output Enable To Data Valid Time	–	12	–	15	–	20	–	25	ns
t_{CAN}	Chip Select Access Time	–	15	–	20	–	30	–	35	ns
t_{ASPN}	Address Set-up Parity Time	40	–	50	–	65	–	80	–	ns
t_{AABN}	Address Access to Breakpoint	–	55	–	65	–	80	–	95	ns
t_{AABFS}	Address Access to BKPT FF Set-up	40	–	50	–	65	–	80	–	ns
t_{AABFH}	Address Access to BKPT FF Hold	0	–	0	–	0	–	0	–	ns
t_{PFCD}	Parity Flip-Flop Clock to data	–	12	–	15	–	20	–	25	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. Pipelined address access set-up time.
5. Transition is measured ±500mW from steady state with 5pF load (including scope and jig).

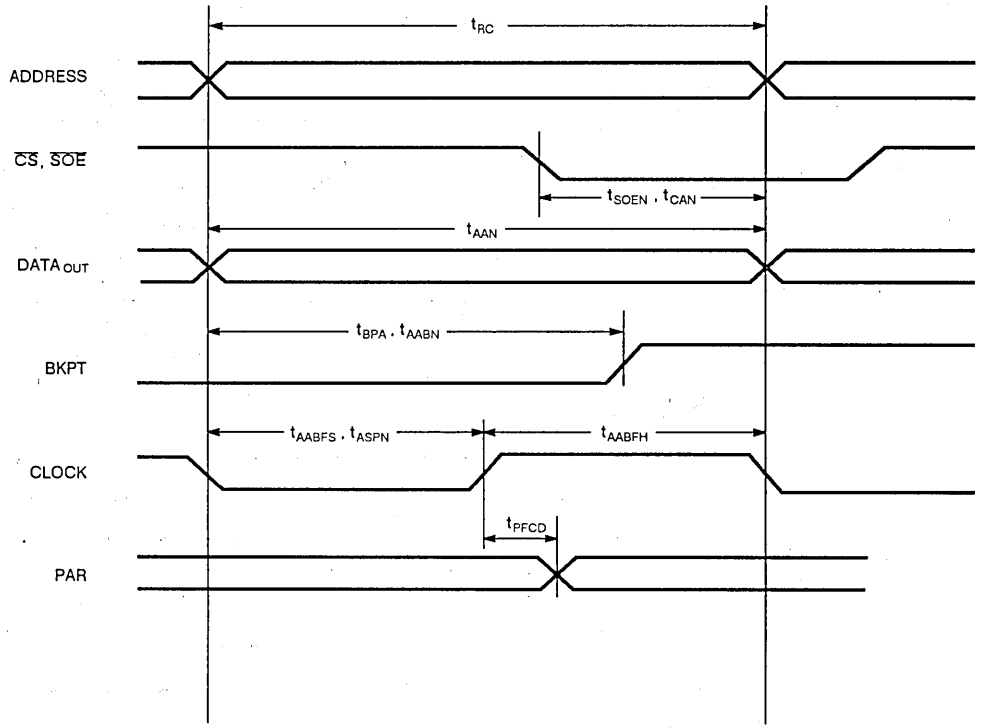
TIMING WAVEFORM OF READ CYCLE NO. 1



NOTE:

1. Transition is measured ±500mV from steady state with 5pF load (including scope and jig).

TIMING WAVEFORM OF READ CYCLE NO. 2 – NON-PIPELINED



NOTE:

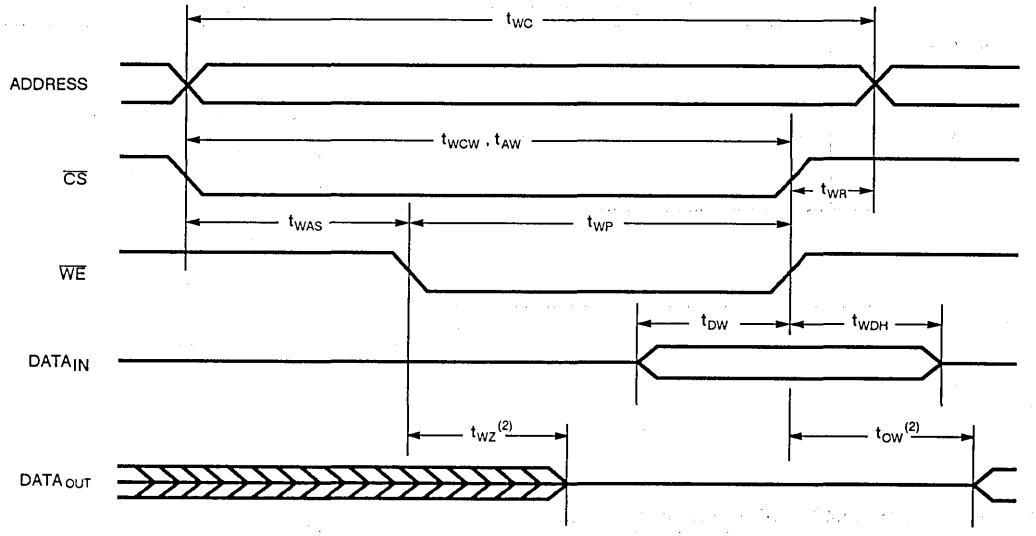
1. Transition is measured ±500mV from steady state with 5pF load (including scope and jig).

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT71502S25 (1, 4) IDT71502L25 (1, 4) MIN.	MAX.	IDT71502S35 (4) IDT71502L35 (4) MIN.	MAX.	IDT71502S45 (4) IDT71502L45 (4) MIN.	MAX.	IDT71502S55 (2, 4) IDT71502L55 (2, 4) MIN.	MAX.	UNIT
RAM WRITE CYCLE										
t_{WC}	RAM Write Cycle Time	40	–	50	–	65	–	80	–	ns
t_{WAS}	RAM Write Address Set-up Time	0	–	0	–	0	–	0	–	ns
t_{WP}	RAM Write Pulse Width (5)	20	–	25	–	35	–	45	–	ns
t_{DW}	RAM Write Data Set-up Before End Of Write	15	–	17	–	25	–	30	–	ns
t_{AW}	Address Valid to End of Write	25	–	30	–	50	–	60	–	ns
t_{WCW}	Chip Select To End Of Write	25	–	30	–	50	–	60	–	ns
t_{WDH}	RAM Write Data Hold Time	0	–	0	–	0	–	0	–	ns
t_{WR}	Write Recovery Time	5	–	5	–	5	–	5	–	ns
t_{WZ}	Write Enable to Output Hi-Z (3, 6)	–	15	–	15	–	20	–	20	ns
t_{OW}	Output Active from End of Write (3, 6)	5	–	5	–	5	–	5	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed but not tested.
4. Pipelined address access set-up time.
5. $\overline{OE}$ = V_{IH}.
6. Transition is measured ±500mV from steady state with 5pF load (including scope and jig).

TIMING WAVEFORM OF WRITE CYCLE (1)



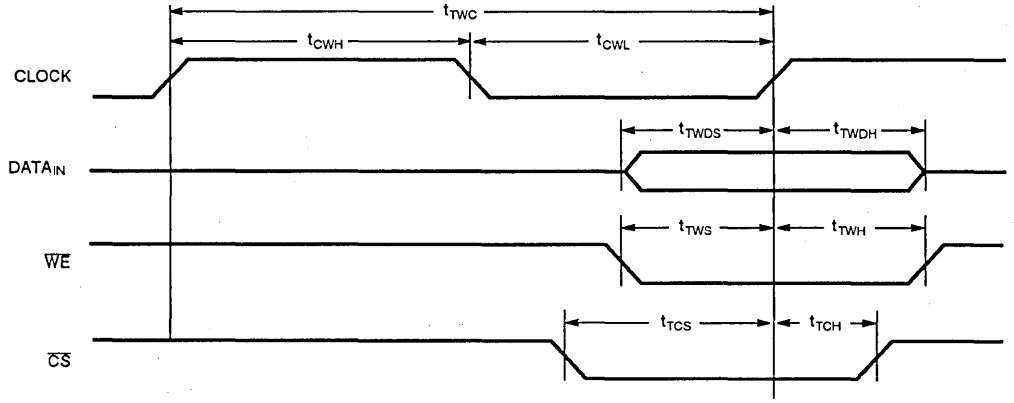
NOTE:
1. A write occurs during the overlap of both $\overline{CS}$ and $\overline{WE}$ low.
2. Transition is measured ±500mV from steady state with 5pF load (including scope and jig).

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT71502S25[1,4] IDT71502L25[1,4] MIN.	MAX.	IDT71502S35[4] IDT71502L35[4] MIN.	MAX.	IDT71502S45[4] IDT71502L45[4] MIN.	MAX.	IDT71502S55[2,4] IDT71502L55[2,4] MIN.	MAX.	UNIT
TRACE WRITE CYCLE										
t_{TWC}	Trace Write Cycle Time	40	–	50	–	65	–	80	–	ns
t_{TWDS}	Trace Write Data Set-up Time	8	–	10	–	12	–	15	–	ns
t_{TWDH}	Trace Write Data Hold Time	2	–	2	–	2	–	2	–	ns
t_{TWS}	Trace Write Enable Set-up Time	8	–	10	–	12	–	15	–	ns
t_{TCS}	Trace Write Chip Select Set-up Time	8	–	10	–	12	–	15	–	ns
t_{TWH}	Trace Write Enable Hold Time	2	–	2	–	2	–	2	–	ns
t_{TCH}	Trace Write Chip Select Hold Time	2	–	2	–	2	–	2	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed but not tested.
4. Pipelined address access set-up time.

TIMING WAVEFORM OF TRACE WRITE CYCLE[1]



NOTE:
1. A write occurs if both $\overline{CS}$ and $\overline{WE}$ are low at the clock low-to-high transition

AC TEST CONDITIONS (Read and Write Cycles)

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

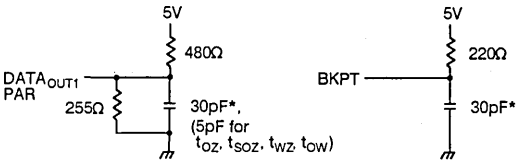


Figure 1. Output Load, Parity Output

Figure 2. Output Load (for BKPT pin)

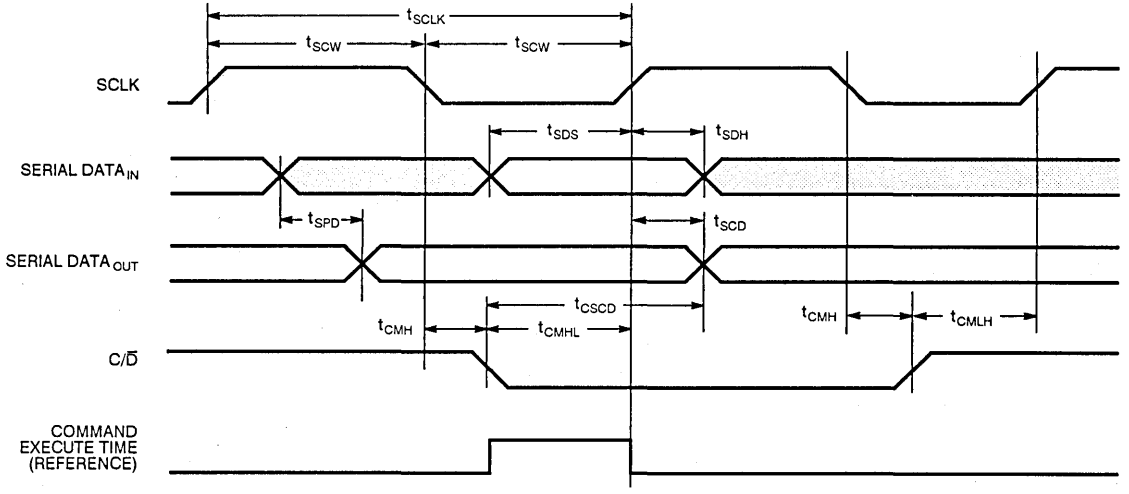
*Includes scope and jig.

SPC AC ELECTRICAL CHARACTERISTICS [1] V_{CC} = 5V ±10%, All Temperature Ranges

SYMBOL	PARAMETER	IDT71502S/L[1] MIN.	MAX.	UNIT
t_{SCLK}	SCLK Period	100	–	ns
t_{SCW}	SCLK Pulse Width	40	–	ns
t_{SDS}	Serial Data Set-up Time	20	–	ns
t_{SDH}	Serial Data Hold Time	2	–	ns
t_{SCD}	Clock to serial Data Output Delay	–	30	ns
t_{SPD}	Serial Data-In-to-Out Delay, Stub Mode	–	20	ns
t_{CMLH}	Command/Data Set-up Time, Low-to-High[2]	20	–	ns
t_{CMHL}	Command Set-up Time, High-to-Low (Execution Time)[2]	35	–	ns
t_{CMH}	Command/Data Hold Time[2]	5	–	ns
t_{CSCD}	Command/Data to Serial Data Output Delay (1st Bit Only)	–	45	ns

NOTES:
1. These specifications apply to all speed grades of the product.
2. C/$\overline{D}$ cannot change while SCLK is high.

TIMING WAVEFORM OF SPC CHANNEL



AC TEST CONDITIONS (SPC)

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 3

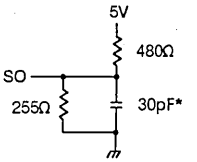
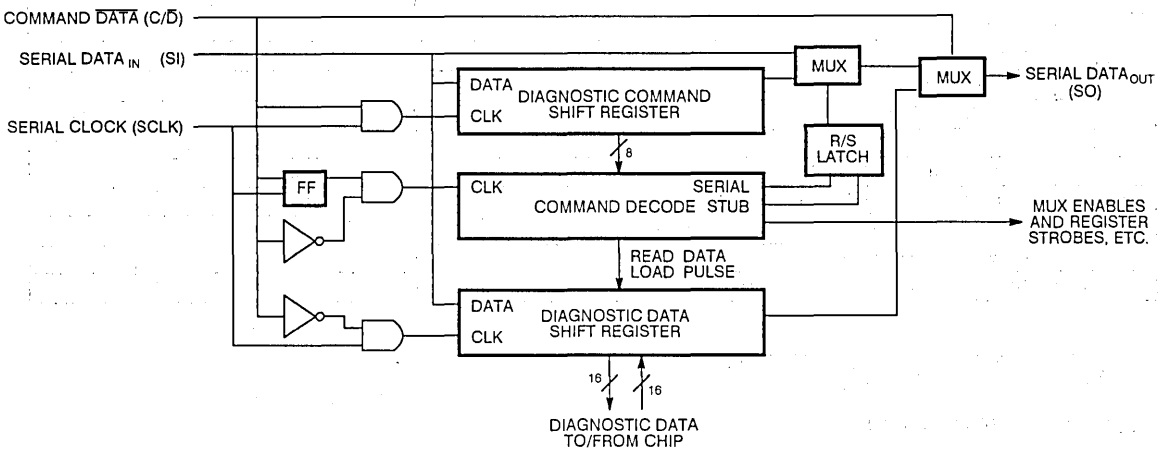


Figure 3. Output Load for Serial Output

*Includes scope and jig.

SPC FUNCTIONAL BLOCK DIAGRAM



SPC COMMAND FORMAT

7 — 4	3 — 0
SPC Command Code 4 bits	SPC Register Code 4 bits

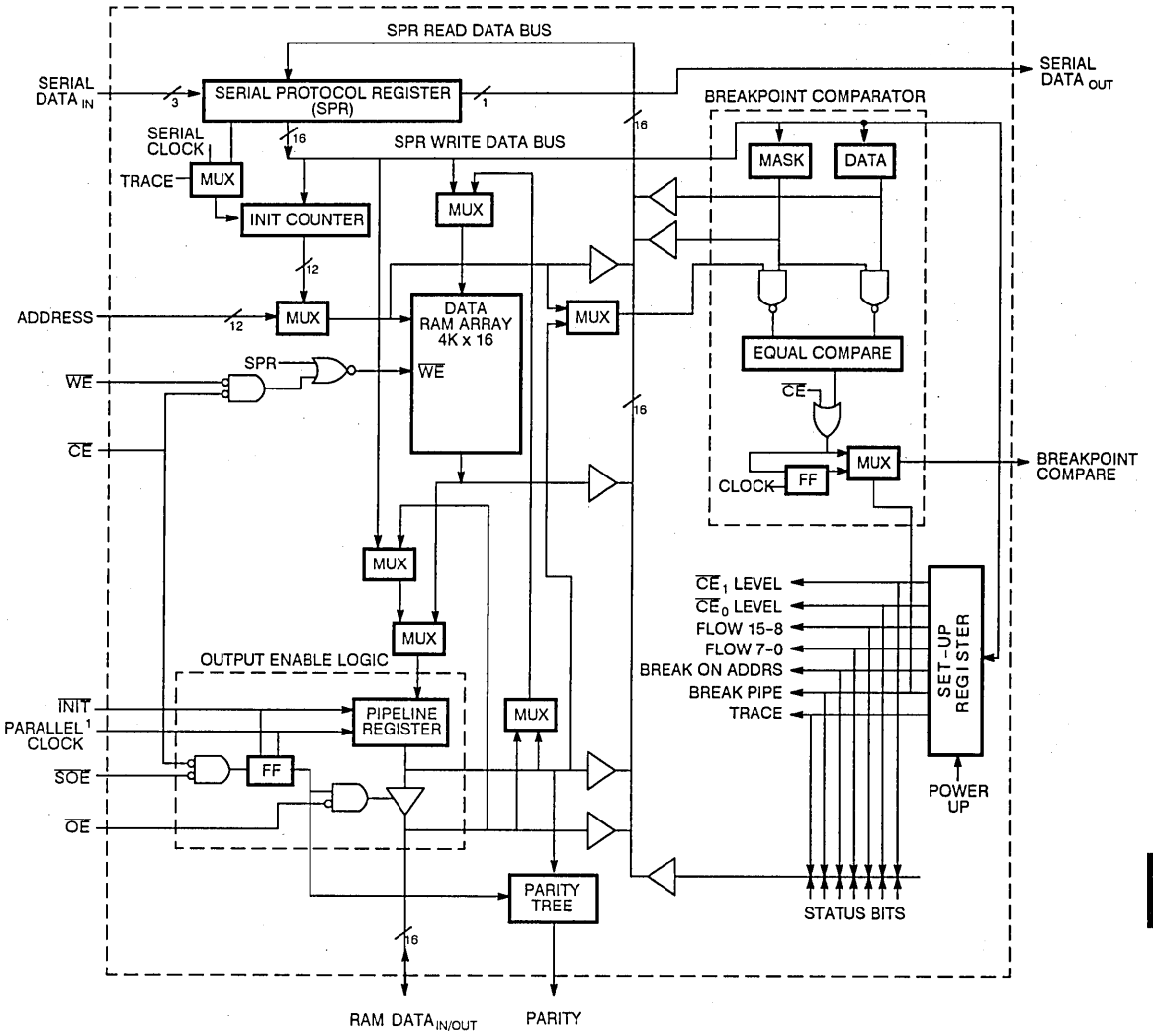
SPC COMMAND CODES

COMMAND CODE	READ/WRITE FUNCTION	ACTION	NOTES
0	Read	Read Register	Uses Register Select Field
1	Write	Write Register	Uses Register Select Field
2	Read	Read Register and Increment Initialize Counter	Serial RAM Read
3	Write	Write Register and Increment Initialize Counter	Serial RAM Write
4-C	–	Reserved (No-Op)	–
D	Write	Stub Diagnostic	Broadcast Commands
E	Write	Serial Diagnostic	Serial Commands
F	–	No-Op	Guaranteed No-Op

SPC REGISTER CODES

REGISTER CODE	READ/WRITE FUNCTION	REGISTER	NOTES
0	R/W	Initialize Counter	–
1	R/W	RAM Output (or Input if reading)	–
2	R/W	Pipeline Register	–
3	R/W	Break Mask Register	–
4	R/W	Break Data Register	–
5	R/W	Set-up + Status Register	Break Multiplexer, Trace Mode, etc.
6	Rd Only	I/O_{15} - I/O_0 (Data Pins)	Data Pins of Chip
7	Rd Only	RAM Address	Address Going into RAM
8-F	–	Reserved (unused)	–

REGISTERED RAM DATA FLOW BLOCK DIAGRAM



NOTE:

1. SPC and RAM accesses are mutually exclusive. Hence, these two operations must not occur simultaneously. During SPC accesses, the content of the pipeline register will change if the parallel clock is active.

SET-UP REGISTER FORMAT

BIT	NAME	TYPE [1]	FUNCTION	POWER-UP VALUE
15	CE	RO	Chip Enable State: NOR of All Chip Enable Pins	0
14	$\overline{SOE}$ FF	RO	$\overline{SOE}$ FF State: 1 = Output Enabled, 0 = Output Disabled	0
13	$\overline{SOE}$ Pin	RO	$\overline{SOE}$ Pin State: 1 = High, 0 = Low	0
12	$\overline{OE}$ Pin	RO	$\overline{OE}$ Pin State: 1 = High, 0 = Low	0
11	$\overline{WE}$ Pin	RO	$\overline{WE}$ Pin State: 1 = High, 0 = Low	0
10	$\overline{INIT}$ Pin	RO	$\overline{INIT}$ Pin State: 1 = High, 0 = Low	0
9	BP Compare	RO	Breakpoint Comparator Output: 1 = Compare Valid	0
8	BP Pin	RO	BP Pin State: 1 = High, 0 = Low	0
7	$\overline{CS}_1$ Level	R/W	0 = $\overline{CS}_1$ is Low Active; 1 = CS_1 is High Active	0
6	$\overline{CS}_0$ Level	R/W	0 = $\overline{CS}_0$ is Low Active; 1 = CS_0 is High Active	0
5	Non-Reg High	R/W	Set Pipeline Register Bits 15-8 to Flow-Through Mode	0
4	Non-Reg Low	R/W	Set Pipeline Register Bits 7-0 to Flow-Through Mode	0
3	–	–	(Unused)	0
2	BC Address	R/W	0 = Breakpoint on Pipeline Register Output, 1 = Breakpoint on RAM Address Inputs	0
1	BC Pipelined	R/W	Set Breakpoint Output MUX for Pipeline FF Output	0
0	Trace Mode	R/W	Set for Trace Mode: I/O_{15-0} to Pipeline Register, Pipeline Register to RAM, Initialize Counter as Address, Write with Clock Pulse	0

NOTE:
1. RO means Read Only. R/W means Read/Write.

GENERAL DESCRIPTION

The IDT71502 Registered RAM consists of a 4K x 16-bit RAM plus a 16-bit pipeline register and is designed for microcode writable control store use. A serial shift register system, the Serial Protocol Channel (SPC), is included on-chip for serial load and read-back of the RAM data. A RAM address counter is also provided to speed up RAM load and read-back. The SPC serial shift register is also configured to be used as a diagnostic register. The shift register can read all status conditions on the chip such as the RAM output, pipeline register output, data output pin state and RAM load/read counter value. A breakpoint comparator is included to support the diagnostic function. This breakpoint comparator can be used to detect a particular bit pattern in the RAM address or pipeline register outputs.

The IDT71502 Registered RAM includes features to support control store applications. These include synchronous output enable and an initialize register for selecting the initial value of the pipeline register. A parity output is provided which indicates the parity of the contents of the pipeline register. The parity output can be used to provide parity check control for high-reliability systems.

The IDT71502 Registered RAM can also be used as a trace RAM for recording external data. In this mode, the data I/O pins are inputs and data is clocked into the RAM using the Initialize register as the address counter. The Trace mode, in combination with the breakpoint comparator, allows the IDT71502 Registered RAM to be used as a one-chip logic analyzer.

RAM Operation

After power up, and in its typical operating mode, the IDT71502 Registered RAM is set for pipelined read and direct (non-pipelined) write. Data may be directly written into the RAM by driving the address and data inputs and strobing the Write Enable input. Data is read from the RAM by driving the address lines and clocking the pipeline register.

The RAM may also be read and written by the Serial Protocol Channel (SPC). This is the typical path for loading the RAM after power up. SPC and RAM accesses are mutually exclusive. Hence, these two operations must not occur simultaneously. During SPC accesses, the content of the pipeline register will change if the parallel clock is active.

Serial Protocol Channel

The Serial Protocol Channel (SPC) logic consists of a 16-bit data shift register, an 8-bit command register and clock logic consisting of gates and a flip-flop. A block diagram of the command decode logic is shown for reference. The command decode logic decodes and executes the command in the command shift register using the clock from the clock logic. The command is divided into two four-bit fields. The most significant four bits of the command register define the command to be executed: read, write, etc. The least significant four bits define the register to be read or written. (NOTE: The data to the SPC is shifted in LSB first.)

The SPC is connected to the outside world through four wires. These wires consist of serial data in and out, a shift clock and a command/$\overline{\text{data}}$ line. When the command/$\overline{\text{data}}$ line is high, commands are shifted from the serial data in to the command register by the clock. When the command/$\overline{\text{data}}$ line is low, data is shifted into the data shift register by the clock. When the command/data line transitions from high (command) to low (data), a clock pulse is generated internally to the command decode logic. This pulse lasts from the beginning of the high-to-low transition to the next serial clock pulse and is used to execute the command in the command register.

Two of the defined commands are Serial and Stub. These commands control a latch which determines the source of the serial data out in the command mode. The Serial command causes the data output to be taken from the last stage of the command shift register. This is the normal operating mode, where all the shift registers in a system are connected into one long shift register. The SPC logic in the IDT71502 is automatically set to the Serial mode by power up. The Stub command sets the latch and causes the serial output data to be taken from the serial input. In this mode, the serial data is passed directly from one chip to the next so that all command registers have the same data at their serial inputs. This allows a broadcast mode where all command registers in a system can be loaded with the same command at the same time.

RAM Load/Readback Logic

The RAM write pulse is generated by an internal one-shot triggered by the clock. Data is written into the RAM immediately following pipeline register load and the Initialize Counter is incremented by the trailing edge of the write pulse. Using an internally generated write pulse makes RAM writing independent of clock high and low times. A timing diagram of the RAM clocking is shown in the Trace Mode Clock Timing Diagram (Figure 5).

A detailed block diagram of the IDT71502 Registered RAM, showing the various internal registers and the load and readback paths, is shown in the Registered RAM Data Flow Block Diagram. In addition to the logic shown in the Functional Block Diagram on the first page of the data sheet, there is an Initialize Counter for loading and initializing the RAM, Break Data and Mask registers for the Breakpoint Comparator and multiplexers at the input to the Pipeline register for allowing data from the data I/O pins to be clocked into the Pipeline register in the Trace mode before being written into the RAM. The data flow block diagram also shows the various multiplexers for routing data for breakpoint and readback use.

Initialize Counter

The Initialize Counter provides the initial address to the RAM after reset of the part. A pulse applied to the Initialize pin causes the Initialize Counter to be gated to the RAM address and the RAM data to be preset into the pipeline register. This provides an initial value in the pipeline register before the first clock pulse arrives. The Initialize Counter can be reset to zero at power up of the chip and can be loaded with a value other than zero by the SPC. Once loaded with a value by the SPC, this value is used in further chip reset operations.

Set-up Register

The Set-up Register is a 16-bit register used to set the chip operating mode and to read back chip operating status conditions. A command word written into the Set-up Register sets 7 latches which control the chip operating conditions. Reading the Set-up Register provides the current status of these 7 latches and various other signals on the chip. At power up, the 7 latches are cleared to zero and the Initialize counter is cleared to zero. The format of the Set-up Register is shown in the Set-up Register Format table.

The Set-up Register has 7 latches which determine the operating mode of the chip. These are $\overline{\text{CS}}_1$, $\overline{\text{CS}}_0$, Non-Reg High, Non-Reg Low, BC RAM, Break Pipe and Trace. The $\overline{\text{CS}}_1$ and $\overline{\text{CS}}_0$ bits determine the polarity of the $\overline{\text{CS}}_1$ and $\overline{\text{CS}}_0$ chip enables. The Non-Reg High and Low bits set the upper and lower bytes of the Pipeline Register to a flow-through mode, respectively. The BC RAM bit determines the source of the data for breakpoint comparison, either the Pipeline Register or the RAM address. The Break Pipe latch switches the breakpoint pin multiplexer from the comparator to the buffer flip-flop. The trace latch sets the chip into the Trace mode.

7

Power Up State

Power up is defined as taking V_{CC} from below 1.0 volts to 5.0 volts nominal. This generates power up reset, an internal signal which resets several registers on the chip. After power up, the IDT71502 is in the following state:

- Set-up Register cleared to zero
- Initialize Counter cleared to zero
- Breakpoint Mask Register cleared to equal (Breakpoint output high)
- $\overline{SOE}$ Flip-Flop cleared to outputs off

Note that taking V_{CC} from 5.0 volts to 2.0 volts and back to 5.0 volts will not cause power up reset.

Set-up Register: Programmable Chip Enable

The chip enable function is programmable by bits in the Set-up Register. The logic for this is shown in Figure 1. The bits in the Set-up Register define the active state of each chip enable: high or low. This allows up to four RAMs to be cascaded in depth with no external decoders required (16K x 16 bits of RAM).

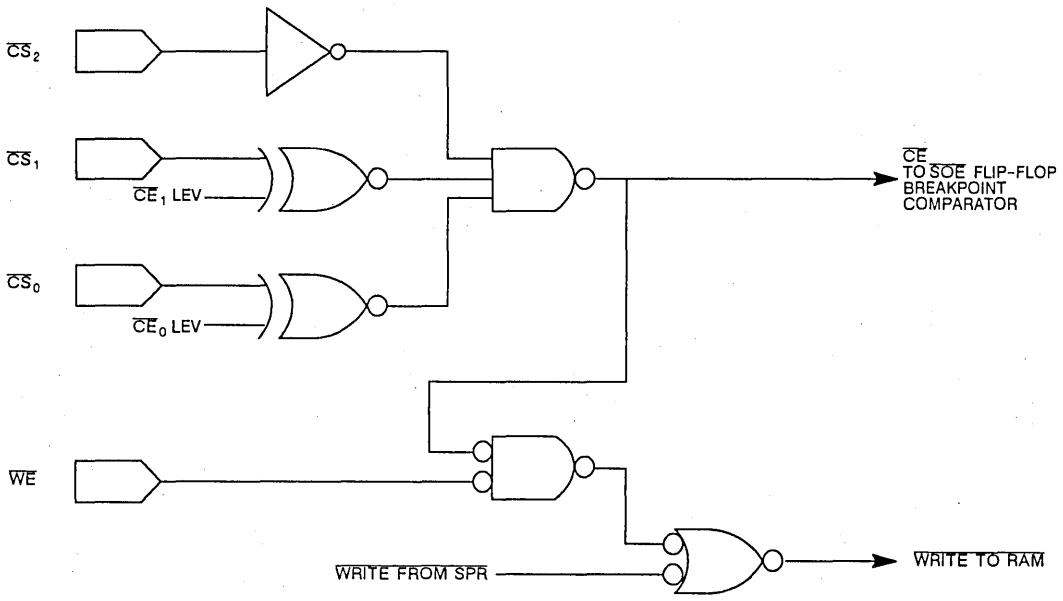


Figure 1. Chip Enable Logic Block Diagram

Set-up Register: Non-Registered Outputs

Two bits of the Set-up Register, Non-Reg Hi and Non-Reg Lo, can be set to cause the Pipeline Register bits 15-9 and 7-0, respectively, to be set to the flow-through mode. In the flow-through mode, both latches of the register are open and the register acts like a simple buffer with its output following its input. This allows the user to have some non-registered bits in microcode applications. The output circuit consisting of the Pipeline Register, the Synchronous Output Enable ($\overline{SOE}$), and the Output Enable ($\overline{OE}$), has some special logic to support this mode, as shown in Figure 2.

Also, activating the Initialize pin causes the Pipeline Register to be put in the flow-through mode. Figure 2 shows the Pipeline Register as two latches operated in the MASTER/SLAVE configuration. The clock input will cause the latch pair to work as a register. If the Initialize pin is activated, both registers will be placed in the flow-through mode by the OR gates. Also, if either Non-Reg bit is set, its corresponding 8-bit portion of the register will be placed in the flow-through mode.

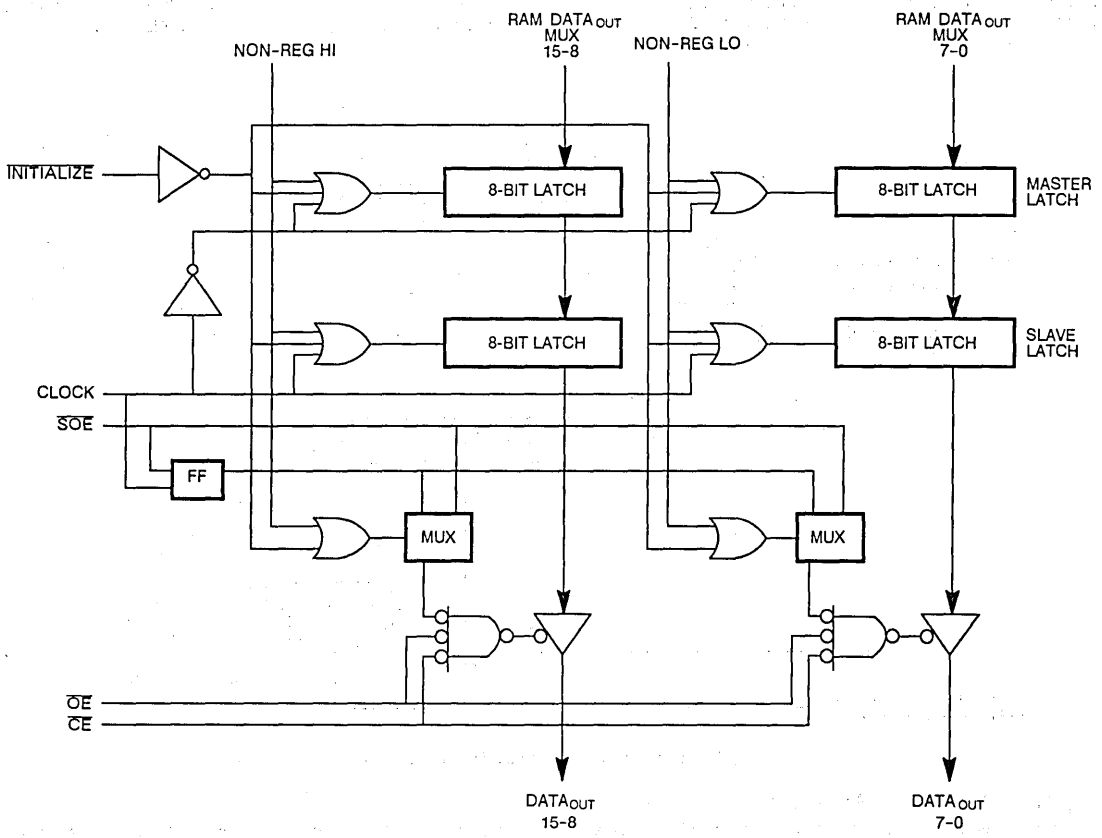


Figure 2. Output Logic Block Diagram

When in the flow-through mode, the output enable flip-flop for that half must also be in the flow-through mode for external chip expansion to work properly. A non-registered RAM bit must be enabled by a non-registered output enable, while a registered bit must be enabled by a synchronous output enable. This is done by using the non-registered bit to control a multiplexer which selects between the $\overline{SOE}$ flip-flop input and output as the source of the output enable.

Set-up Register: Breakpoint Comparator Control

The Breakpoint Comparator (BC) provides a masked 16-bit comparison of the various data paths that can be read by the SPC. It consists of an equal-comparator and the Break Data and Mask registers, as shown in Breakpoint Comparator Logic Block Diagram (Figure 3). The BC compares the data from the chip against the data in the Break Data Register and activates the Breakpoint Compare output if the two are equal. The Mask Register enables comparison: if a bit in the Mask Register is a one, comparison is enabled on the corresponding bit in the Break Data Register. If it is zero, the comparison on the that bit is disabled: i.e., forced to equal.

The Breakpoint output is an open drain type to allow width expansion of the Breakpoint Comparison. For example, if two IDT71502 chips have their breakpoint pins tied together to the same load resistor, both breakpoint comparators must be valid before the output can rise. The result is a 32-bit comparison.

A selectable flip-flop is provided for the Breakpoint Output. This allows pipeline registered bits, non-registered bits and address bits to be used in comparison with the same timing. Breakpoint comparison is commonly performed on the pipeline register outputs. These outputs are valid after the clock; i.e. for the current cycle. Address inputs and non-pipelined outputs are valid before the clock, representing address and data for the next cycle, respectively. If address or non-pipelined outputs are to be used in breakpoint comparison, a flip-flop delay must be added so that they will be valid after the clock in the same manner as pipelined bits. The selectable flip-flop provides this delay so that all breakpoint comparison outputs are valid in the current cycle.

The Breakpoint output driver is enabled by the $\overline{SOE}$ Flip-Flop to allow depth expansion of the comparison. $\overline{SOE}$ must be low prior to clock going high whether in pipelined mode or not.

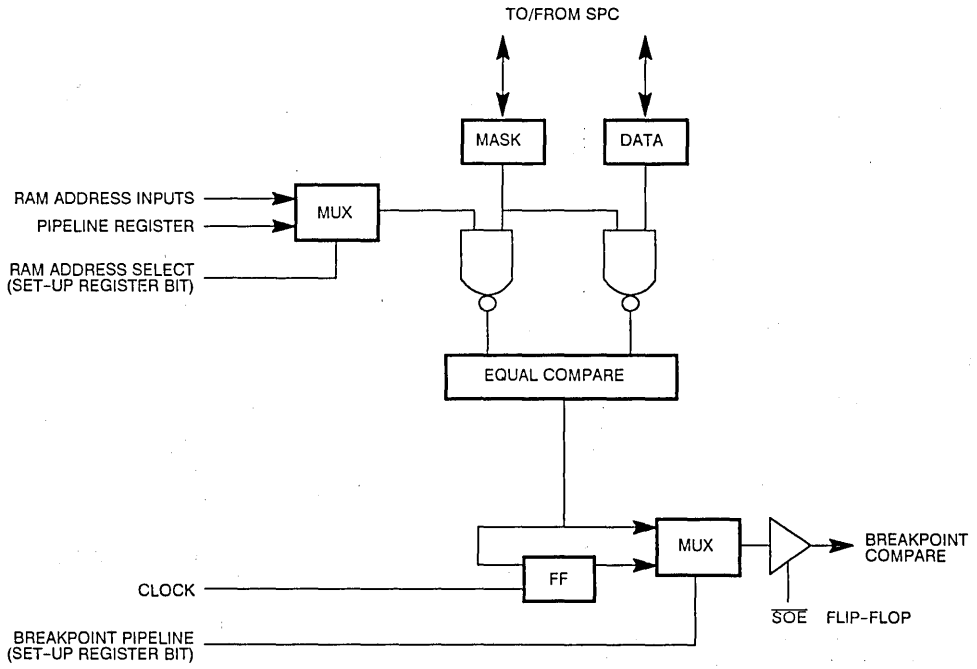


Figure 3. Breakpoint Comparator Logic Block Diagram

Set-up Register: Trace Mode Operation

When the trace bit in the Set-up Register is set, the chip is in the Trace mode. In this mode, data from the chip data pins, I/O_{15}- I/O_0, is written into sequential locations in the RAM . The address for the RAM comes from the Initialize Counter, which is incremented after each RAM write. The Trace mode is used to record external data events in the same manner as a logic analyzer. The Trace mode recording sequence is as follows:

1. Data from the I/O pins is written into the Pipeline Register by the clock.
2. Data in the Pipeline Register is written into the RAM by a one-shot driven by the trailing edge of the clock. The RAM address comes from the Initialize Counter.
3. The Initialize Counter is incremented by the trailing edge of the RAM write pulse.

Trace operation requires both $\overline{WE}$ and $\overline{CS}$ to be active. If either is inactive (high), the Initialize Register will not be incremented and data will not be written into the RAM. The Pipeline Register will be loaded, however. This allows the write enable to be used for skipping words. A timing diagram of this logic is shown in the Trace Mode Sequence Timing Diagram (Figure 4).

The RAM write pulse is generated by an internal one-shot triggered by the clock. Data is written into the RAM immediately following pipeline register load and the Initialize Counter is incremented by the trailing edge of the write pulse. Using an internally generated write pulse makes RAM writing independent of clock high and low times. A timing diagram of the RAM clocking is shown in the Trace Mode Clock Timing Diagram (Figure 5).

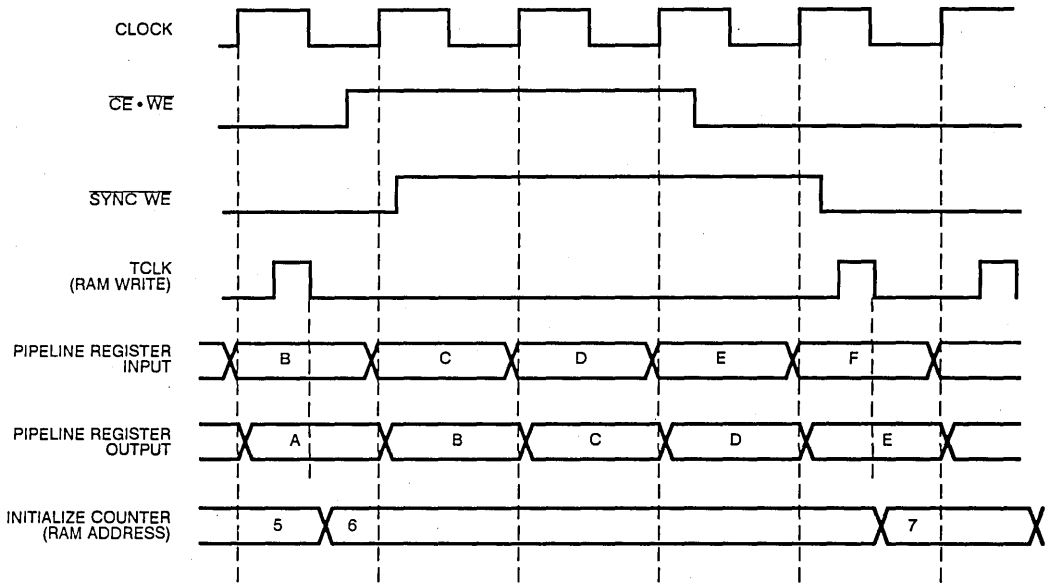


Figure 4. Trace Mode Sequence Timing Diagram

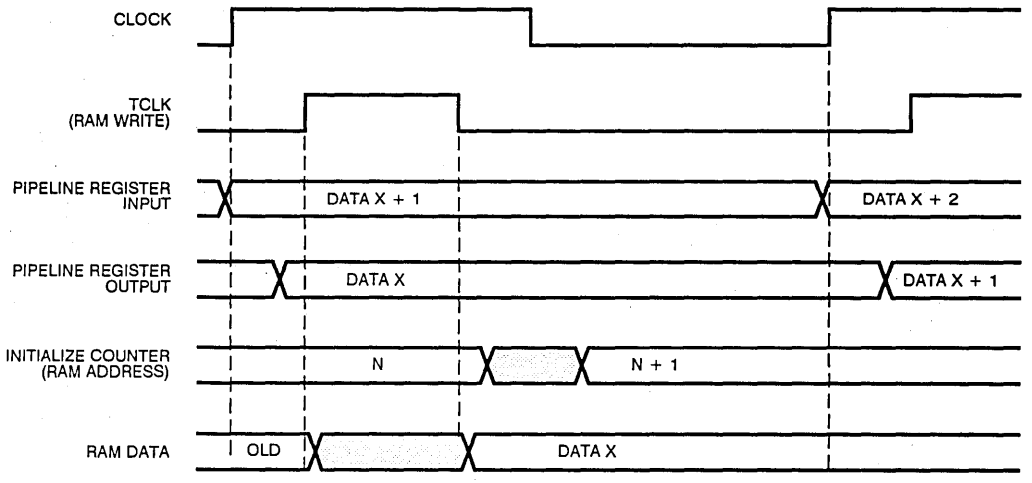


Figure 5. Trace Mode Clock Timing Diagram

Parity Output

The Parity Output pin is generated from a 16-bit parity tree, as shown in the Parity Tree Logic Block Diagram (Figure 6). Even parity is used. Parity is generated on the contents of the Pipeline Register. The parity output driver is three-state and is enabled by the $\overline{SOE}$ Flip-Flop to allow depth expansion of the parity output.

The Parity Output always reflects the parity of the registered value. Additional flip-flops and multiplexers are included in the parity tree to cover the case of non-registered outputs. If one or both bytes of the Pipeline Register are set to the Non-Registered mode, a flip-flop pipeline delay is added to the corresponding byte parity chain to make the result of that byte parity calculation the same as if the Pipeline Register was not in the Non-Pipelined mode. $\overline{SOE}$ must be low prior to the clock going high in pipelined or non-pipelined mode.

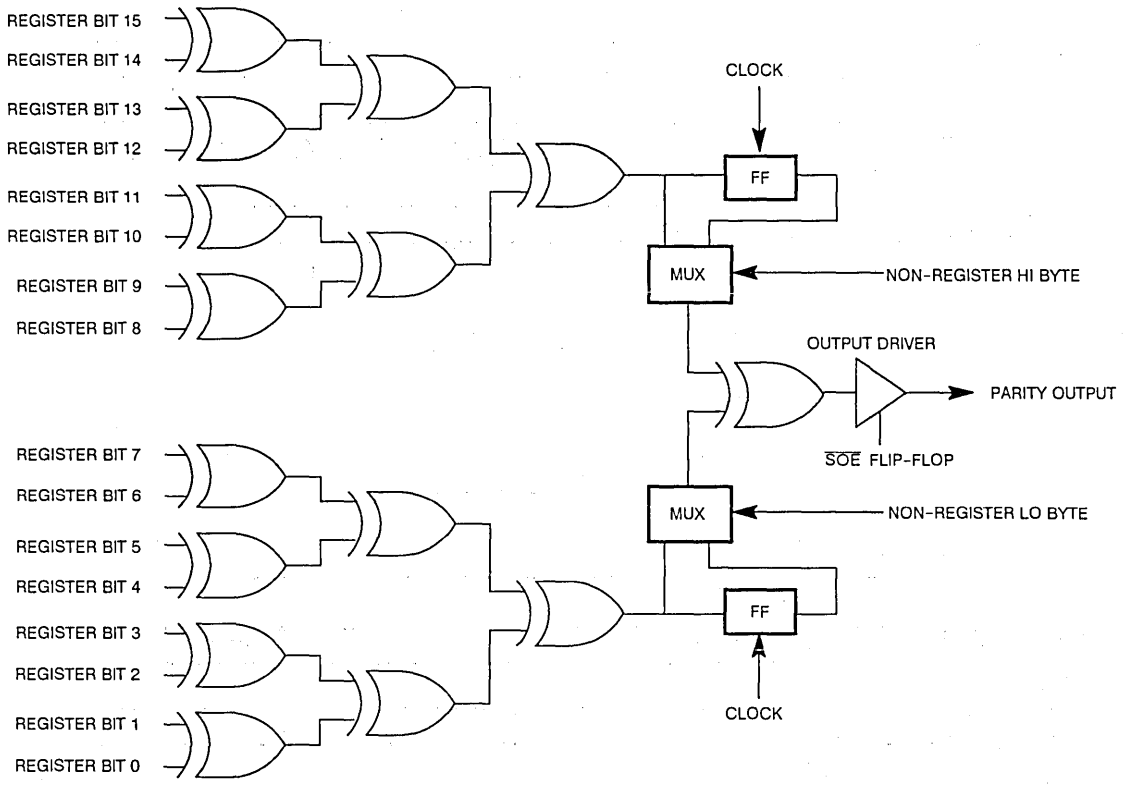


Figure 6. Parity Tree Logic Block Diagram

REGISTERED RAM APPLICATIONS

Using the Registered RAM in Writable Control Stores

The IDT71502 Registered RAM is designed expressly for efficient use in writable control stores. A simplified block diagram of a 16-bit microprogram-controlled system using the IDT71502 is shown in Writable Control Store Using Registered RAM (Figure 7). The system shown uses four IDT71502 Registered RAM chips to provide 4K x 64 bits of microcode writable control store.

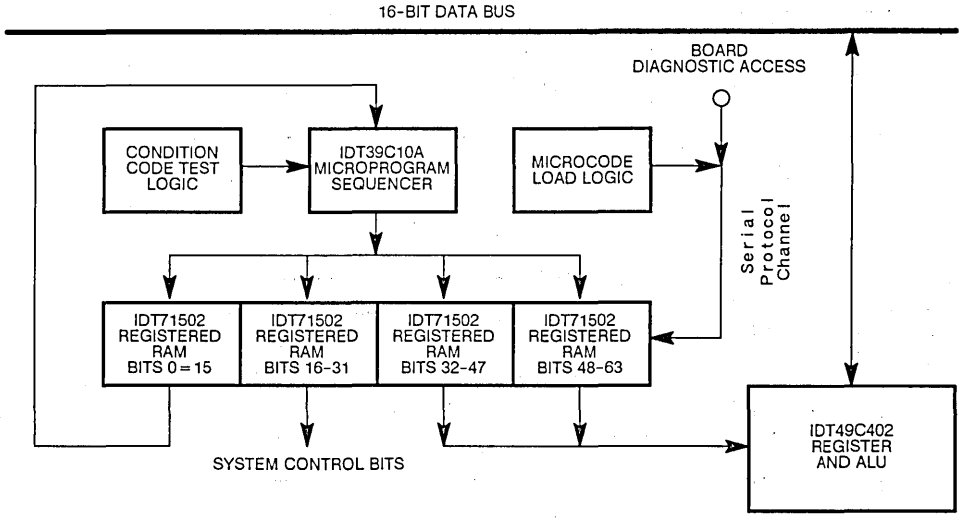


Figure 7. Writable Control Store Using Registered RAM

Using the Parity Output

The parity output can be used in conjunction with an additional IDT71502 Registered RAM to provide parity checking for control stores. This is shown in the Parity Check in a Writable Control Store System (Figure 8) block diagram. The parity output driver is gated by the $\overline{SOE}$ Flip-Flop. This allows simple depth expansion of the parity function by paralleling the parity outputs in the same manner as the data outputs, as shown in the Parity Check in a Depth Expanded Writable Control Store System (Figure 9) block diagram.

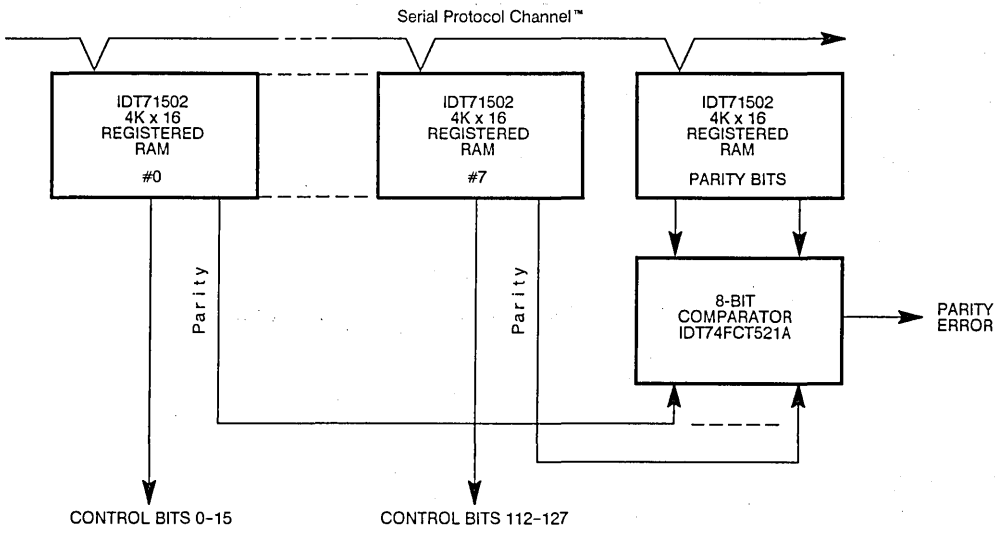


Figure 8. Parity Check in a Writable Control Store System

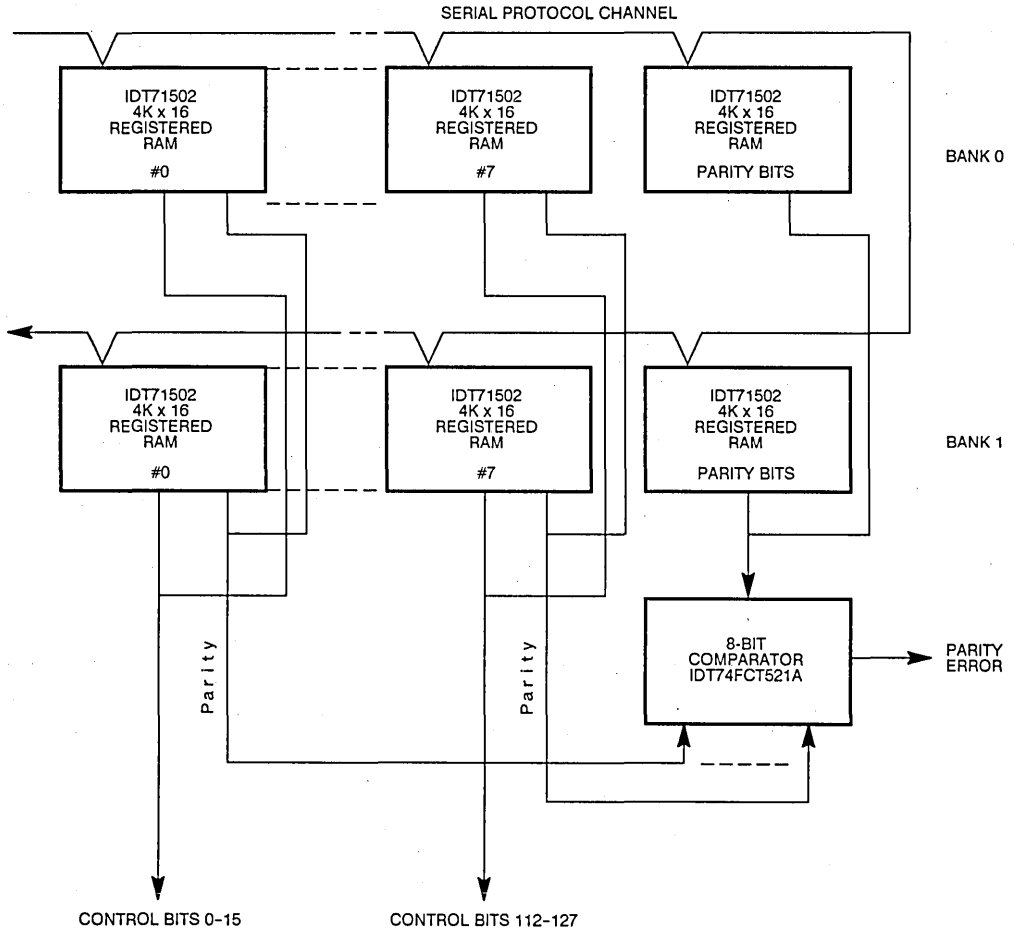


Figure 9. Parity Check in a Depth Expanded Writable Control Store System

Using Trace Mode as a Logic Analyzer

The Trace mode allows the IDT71502 to be used as an on-board logic analyzer for system diagnostics. It is particularly powerful when used in conjunction with the Breakpoint function. In the Trace mode, data is recorded in sequential locations in the RAM as controlled by the Trace Counter. Since the incoming data is clocked into the pipeline register, the set-up and hold times are short and compatible with capturing changing bus data, for example. A block diagram of a system with an IDT71502 used in the Trace mode is shown in Diagnostic Bus Monitoring Using Trace Mode (Figure 10).

The Breakpoint outputs from the IDT71502 devices in a system can be used to control the Trace mode writing. The Breakpoint outputs are open drain types which provide a wire-AND function when connected together to a single pull-up resistor. By tying the Breakpoint outputs for the writable control store RAMs and the trace RAM, a breakpoint comparison can be made over the full microcode word plus the data bus contents. This comparison can be used to enable the trace write so that only data which occurred at the Breakpoint times is recorded. This allows recording the data that was on the bus during each instance of an I/O write, for example.

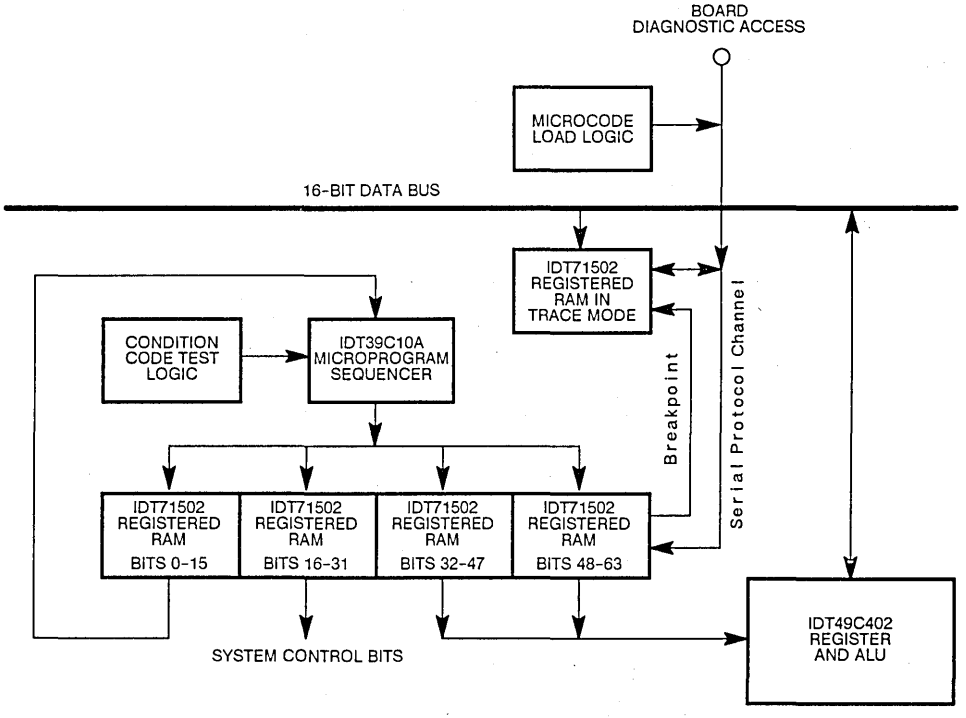


Figure 10. Diagnostic Bus Monitoring Using Trace Mode

7

Serial Loading of the IDT71502 Using the SPC

In order to use the IDT71502 in writable control store applications, it must be loaded with the microprogram before use. This is done using the Serial Protocol Channel (SPC). Loading the RAM over the SPC can be done in several ways. The microcode can be loaded from a central microprocessor, which can perform both microcode load and system diagnostics at power up, or it can be loaded using dedicated load logic.

An example of a design of this dedicated load logic is shown in the Microcode Load Logic Example (Figure 11). The purpose of this example is to show how one goes about designing this logic. This example shows an approach which loads the RAMs with data from a single EPROM. The load logic gets the SPC command and data information from the EPROM. It is controlled by single byte instructions from the same EPROM. The format of these instructions is shown in Microcode Load Logic Instruction Formats (Figure 12), and a map of the typical contents of the EPROM is shown in Microcode Load EPROM Memory Map (Figure 13).

The load logic consists of a 16-bit address counter, an 8-bit shift register, a 4-bit byte counter and a PAL containing a 2-bit instruction register. The logic in the PAL interprets the 2-bit load instructions to cause bytes of command or data information to be loaded into the IDT74FCT299 shift register and shifted to the SPC. The two IDT74FCT161 counters are used to count the bytes being sent and the 8 bits in each byte.

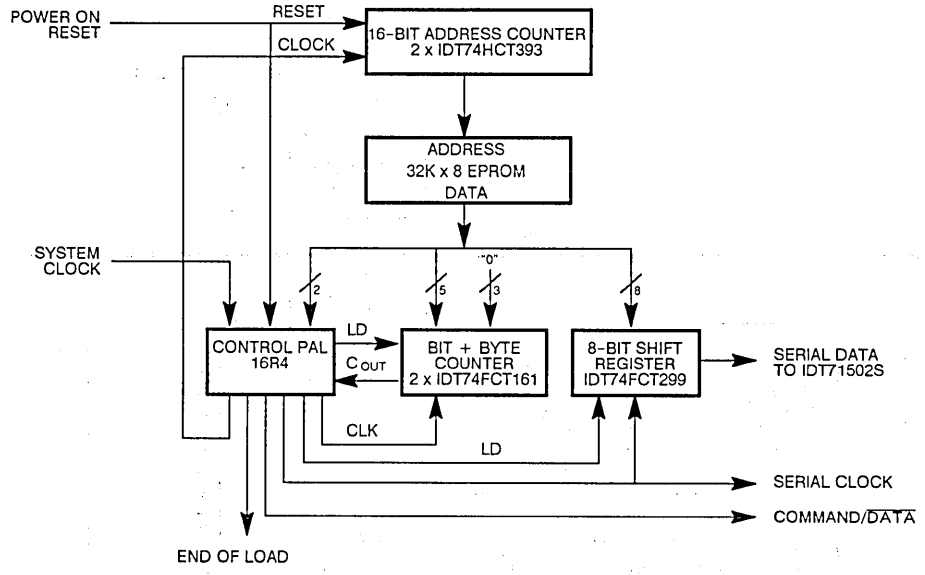


Figure 11. Microcode Load Logic Example

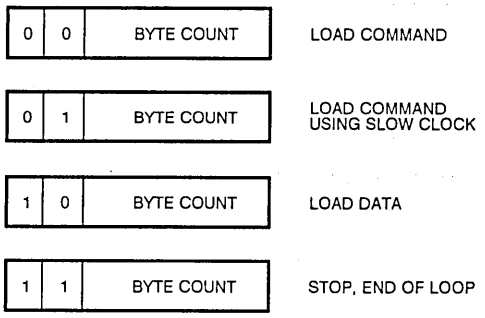


Figure 12. Microcode Load Logic Instruction Formats

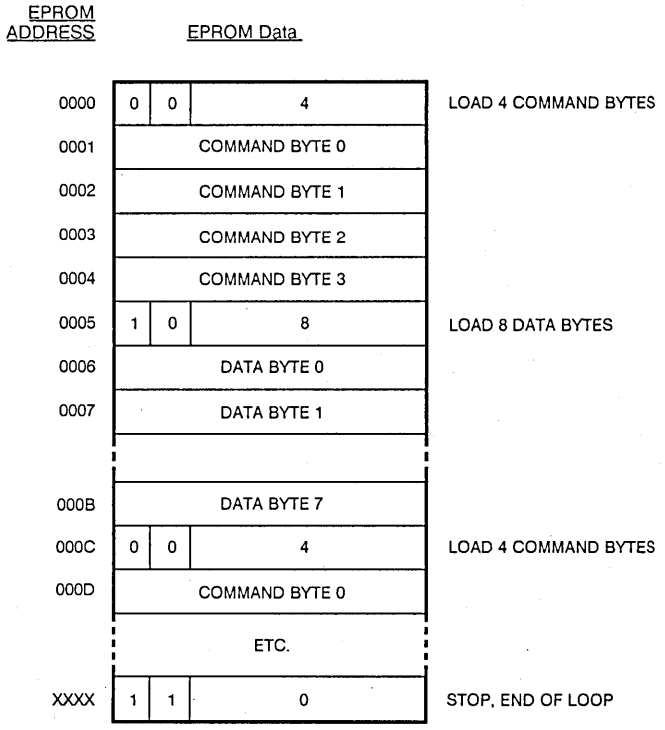
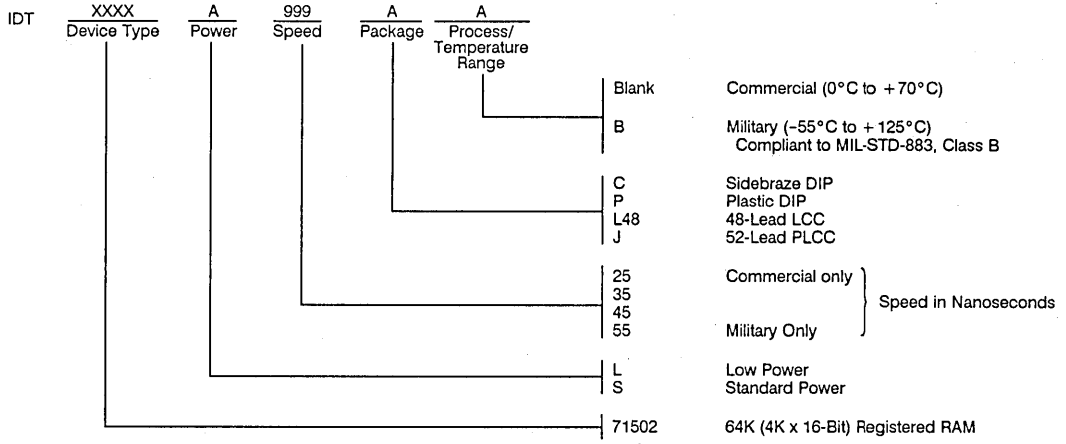


Figure 13. Microcode Load EPROM Memory Map

ORDERING INFORMATION



7

SUBSYSTEM PRODUCTS

IDT Subsystems Division has the resources and experience to deliver the highest quality RAM module products. IDT's combination of advanced design, assembly, and test capabilities give customers the highest levels of quality, service and performance. Product offerings include a number JEDEC standards as well as specialized and application specific RAM modules, including the world's highest performance and densest SRAMs, Dual-Port RAMs, and FIFOs. Custom capabilities allow our customers to enjoy the benefits of parametically tested complete memory-based subsystems including extremely high performance caches for a wide range of processors and complete memory subsystems including multi-megabyte microprocessor main memories.

DT modules products provide a number of benefits to the high performance system designer:

For system designers of high performance systems, modules solve a number of major problems through the benefits they provide. The biggest benefit of modules is that they save significant amounts of space for designers packing ever more performance in less space by utilizing double sided surface mount technology (SMT). Modules allow designers to take advantage of SMT for performance critical memory paths without the investments or the volume necessary to justify employing SMT for an entire system. Since systems at the high performance end of the spectrum tend to be lower volume, it makes sense to take advantage of module technology to enjoy the space savings and performance advantages of SMT without the cost. In addition, decoupling capacitors are mounted next to or underneath the active memory components on the module, thus eliminating the need to consider them or the real estate they consume.

Numerous module packaging options are available which allow designers to tradeoff board area, height and mechanical stability. Vertical mount module options (modules in which mounted components are oriented in a vertical fashion) such as single in-line packages (SIPs), dual-row SIPs (DSIPs), zig-zag in-line packages (ZIPs) and single-in-line memory modules (SIMMs) are ideal packages for applications requiring the highest density. Many of these vertical mount modules are maximum 0.5 inch tall, which is well within the board space requirements for card rack type systems. Horizontal mount module options include dual in-line packages (DIPs), quad in-line packages (QIPs), and hex in-line packages (HIPs). These modules are ideal for those applications requiring the most in mechanical stability and those with many I/O pins.

Design, manufacturing, and marketing often disagree on the size of memory that their high performance system will offer. By allowing the decision to made at manufacturing time by having module solutions with different memory sizes and common pinouts, the module user lets the market dictate memory requirements. JEDEC has defined standards for memory pinouts including 128K x 8 and 512K x 8 SRAM in the same 600 mil wide 32 lead DIP and 16K x 32, 64K x 32 and 256K x 32 SRAM in the same 64 lead SIMM/ZIP which are among the most common industry standard SRAM modules.

Testing is both a design and manufacturing problem that is often an afterthought. By providing a pretested higher level block, modules simplify the test issue for both design and manufacturing. Since the module is tested using full parametric AC/DC guardbanded test patterns over the specified operating temperature range, designers are guaranteed a level of performance for a larger block of their system versus a spec for an individual component. System board test is simplified because a major block of memory has been fully tested at the module level, thus simplifying the test method and debug cycle at the board level.

Time to market is always a very important issue. Studies have shown that a major portion of profits are made in the early part of the product life cycle before competition drives down prices to a level based on manufacturing costs rather than a unique level of value. Integrating the high performance memory into an module shortens the design cycle by simplifying board design by leveraging off the module manufacturer's design expertise. System board layout and the design cycle are simplified because the number of input/outputs (I/Os) are reduced by combining common component address, data, control, and power pins.

Module solutions help reduce hidden costs that are not often taken into account. Since active and passive components necessary to realize an module solution are combined onto a single substrate, the module user reduces inventory and handling costs by combining a number of diverse components into one single component.

IDT Subsystems products provide an ideal solution for system designers to integrate high performance RAM in order to maximize density, performance and cost-effectiveness for both commercial and military applications.

TABLE OF CONTENTS

1990-91 SPECIALIZED MEMORIES DATA BOOK (CONTINUED)

8

Integrated Device Technology, Inc.

8K x 8
16K x 8 CMOS
CMOS DUAL-PORT STATIC
RAM MODULE (MASTER)

IDT7M134S
IDT7M135S

FEATURES:

- High-density 64K/128K CMOS Dual-Port RAM modules
- 16K x 8 (IDT7M135) or 8K x 8 (IDT7M134)option
- Fully asynchronous read/write operation from either port
- Fast access time
  - commercial: 30ns (max.)
  - military: 40ns (max.)
- Low power consumption
- On-chip port arbitration logic
- $\overline{BUSY}$ flags
- Single 5V (±10%) power supply
- Dual Vcc and GND pins for maximum noise immunity
- On-chip pull up resistors for open-drain $\overline{BUSY}$ flag option
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

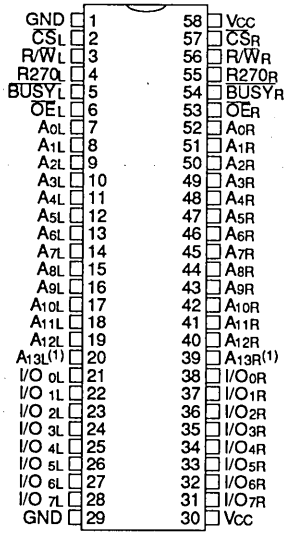
The IDT7M134/IDT7M135 are 64K/128K high-speed CMOS Dual-Port static RAM modules constructed on a multi-layered ceramic substrate using four IDT7132 2K x 8 dual-port static RAMs (IDT7M134) or eight IDT7132 dual-port static RAMs (IDT7M135) in leadless chip carriers. Dual-port function is achieved by utilization of the two on-board IDT54/IDT74FCT138 decoder circuits that interpret the higher order addresses A_{L11-13} and A_{R11-13} to select one of the eight 2K x 8 dual-port static RAMs. (On IDT7M134 8K x 8 option, A_{L13} and A_{R13} need to be externally grounded and the selection becomes one of the four 2K x 8 dual-port static RAMs). Extremely high speeds are achieved in this fashion due to the use of the IDT7132 dual-port static RAM, fabricated in IDT's high-performance CEMOS™ technology.

The IDT7M134/IDT7M135 provide two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in the memory. The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. The on-chip arbitration logic will determine which port has access and sets the $\overline{BUSY}$ flag of the delayed port. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. The delayed port will have access when $\overline{BUSY}$ goes high (inactive).

The IDT7M134/IDT7M135 are available with access times as fast as 30ns commercial and 40ns military temperature range, with operating power consumption of only 2.1W/3.5W (max.). The module also offers a standby power mode of 1.4W/2.8W (max.) and a full standby mode of 660mW/1.3W (max.).

All IDT mililtary module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION (2)



DIP
TOP VIEW

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PIN NAMES

Left Port	Right Port	Names
A_{0L}-A_{13L}	A_{0R}-A_{13R}	Address
I/O0L-IO7L	I/O0R-I/O7R	Data Input/Output
$\overline{CS}_L$	$\overline{CS}_R$	Chip Select
R/$\overline{W}_L$	R/$\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$\overline{BUSY}_L$	$\overline{BUSY}_R$	$\overline{BUSY}$ Flag (Open Drain)
R270L	R270R	PULL-UP Resistors for Open-drain $\overline{BUSY}$ Flag option
Vcc	Vcc	Power
GND	GND	Ground

NOTES:
1. On 8K x 8 IDT7M134 option A_{13L} and A_{13R} need to be externally connected to ground for proper operation.
2. For module dimensions, please refer to module drawing M12 in the packaging section.

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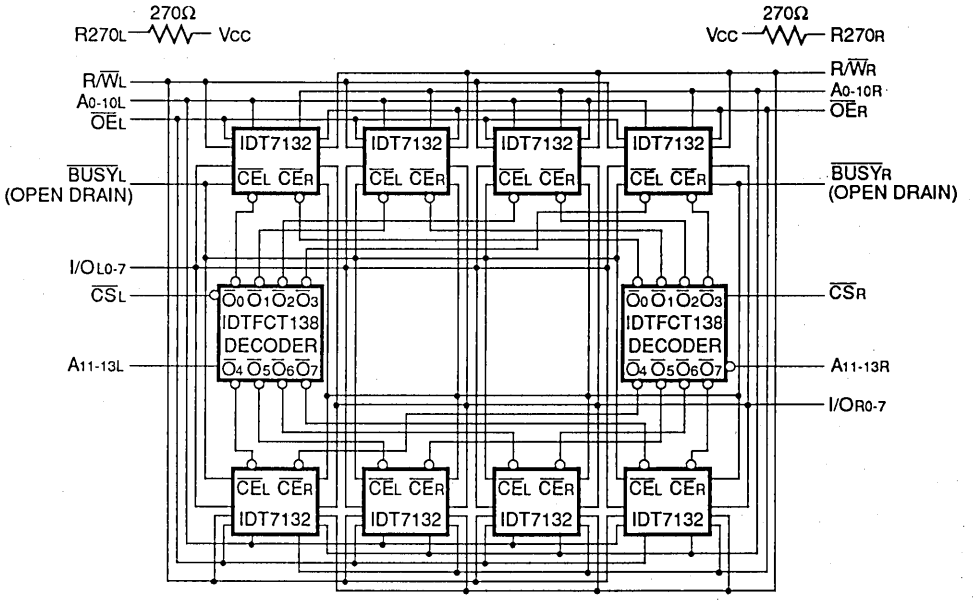
FUNCTIONAL BLOCK DIAGRAMS

IDT7M135 (16K x 8)



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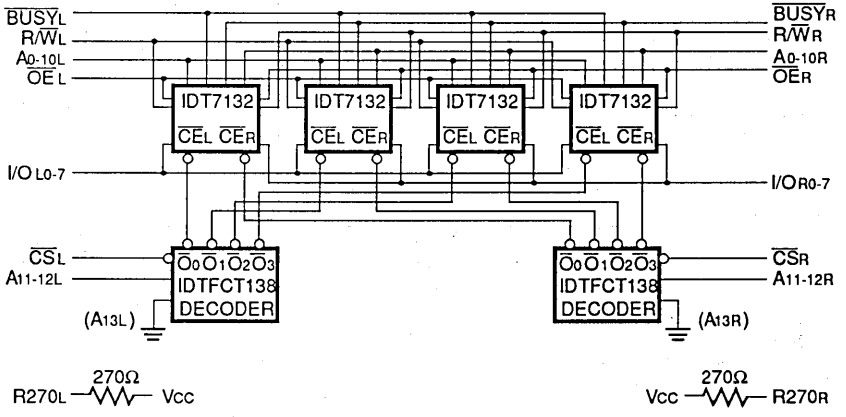
IDT7M134 (8K x 8)



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8

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:
1. V_{IL} = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS(4)

(Vcc = 5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7M134S Min.	IDT7M134S Typ.(1)	IDT7M134S Max.	IDT7M135S Min.	IDT7M135S Typ.(1)	IDT7M135S Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	Vcc = 5.5V, V_{IN} = 0V to Vcc	—	—	15	—	—	20	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to Vcc	—	—	15	—	—	20	µA
V_{IH}	Input High Voltage	—	2.2	—	6.0	2.2	—	6.0	V
V_{IL}	Input Low Voltage	—	-1.0(2)	—	0.8	-1.0(2)	—	0.8	V
Icc	Dynamic Operating Current (Both Ports Active)	$\overline{CS}$ = V_{IL}, Outputs Open, f = f_{MAX}	—	190	380	—	320	640	mA
I_{SB}	Standby Current (Both Ports Standby)	$\overline{CS_L}$ and $\overline{CS_R}$ ≥ V_{IH}, Vcc = Max., Both Ports Output Open	—	130	260	—	260	520	mA
I_{SB1}	Standby Current (One Port Standby)	$\overline{CS_L}$ or $\overline{CS_R}$ ≥ V_{IH}, Vcc = Max. Active Port Outputs Open	—	160	320	—	290	580	mA
I_{SB2}	Full Standby Current (Both Ports Full Standby)	Both Ports $\overline{CS_L}$ and $\overline{CE_R}$ ≥ Vcc -0.2V V_{IN} ≥ Vcc -0.2V or V_{IN} ≤ 0.2V	—	4	120(3)	—	10	240(3)	mA
V_{OL}	Output Low Voltage (I/O_0-I/O_7)	I_{OL} = 4mA, Vcc = 4.5V I_{OL} = 8mA, Vcc = 4.5V	— —	— —	0.4 0.5	— —	— —	0.4 0.5	V V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$)	I_{OL} = 16mA, Vcc = 4.5V	—	—	0.5	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, Vcc = 4.5V	2.4	—	—	2.4	—	—	V

NOTES:
1. Vcc = 5V, T_A = +25°C.
2. V_{IL} min. = -3.0V for pulse width less than 20ns.
3. I_{SB2} max. of IDT7M134/IDT7M135 at commercial temperature = 80mA/150mA.
4. For tAA = 30, 35, 40ns versions all D.C. parameters are preliminary only.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 and 3

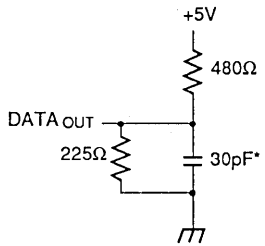

Figure 1. Output Load

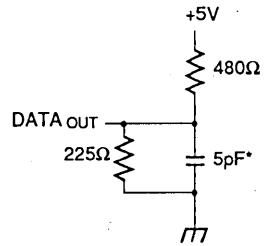

Figure 2. Output Load
(for t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ}, t_{OW})

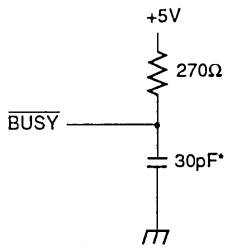

Figure 3. $\overline{BUSY}$ Output Load

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* Including scope and jig. 30pF for fast speed versions. Consult factory for further details.

8

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	7M134S30 7M135S30 (Com'l. Only) Min.	Max.	7M134S35 7M135S35 (Com'l. Only) Min.	Max.	7M134S40 7M135S40 Min.	Max.	7M134S45 7M135S45 Min.	Max.	Unit
READ CYCLE										
t_{RC}	Read Cycle Time	30	—	35	—	40	—	45	—	ns
t_{AA}	Address Access Time	—	30	—	35	—	40	—	45	ns
t_{ACS}	Chip Select Access Time	—	30	—	35	—	40	—	45	ns
t_{OE}	Output Enable Access Time	—	15	—	20	—	25	—	30	ns
t_{OH}	Output Hold From Address Change	0	—	0	—	0	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	10	—	ns
t_{CHZ}[1]	Chip Select to Output in High Z	—	10	—	15	—	15	—	20	ns
t_{OHZ}[1]	Output Enable to Output in High Z	—	10	—	15	—	15	—	30	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Down Time	—	50	—	50	—	50	—	50	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	30	—	35	—	40	—	45	—	ns
t_{CW}	Chip Select to End of Write	25	—	30	—	35	—	40	—	ns
t_{AW}	Address Valid to End of Write	25	—	30	—	35	—	40	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	5	—	ns
t_{DW}	Data Valid to End of Write	20	—	20	—	22	—	25	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	5	—	ns
t_{OHZ}[1]	Output Enable to Output in High Z	—	10	—	15	—	15	—	20	ns
t_{WHZ}[1]	Write Enabled to Output in High Z	—	10	—	15	—	15	—	20	ns
t_{OW}[1]	Output Active From End of Write	0	—	0	—	0	—	0	—	ns
$\overline{BUSY}$ TIMING										
t_{BAA}	$\overline{BUSY}$ Access Time to Address	—	35	—	35	—	40	—	40	ns
t_{BDA}	$\overline{BUSY}$ Disable Time to Address	—	30	—	35	—	35	—	35	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Select	—	30	—	35	—	35	—	40	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Select	—	30	—	30	—	30	—	35	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data	—	20	—	25	—	30	—	30	ns
t_{WDD}	Write Pulse to Data Delay	—	50	—	55	—	60	—	65	ns
t_{DDD}	Write Data Valid to Read Data	—	25	—	30	—	35	—	40	ns
t_{APS}	Arbitration Priority Set-up Time	10	—	10	—	10	—	10	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

AC ELECTRICAL CHARACTERISTICS (Continued)

(V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	IDTM134S50 IDTM135S50		IDTM134S60 IDTM135S60		IDTM134S70 IDTM135S70 (Mil. Only)		IDTM134S90 IDTM135S90 (Mil. Only)		IDTM134S100 IDTM135S100 (Mil. Only)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	50	—	60	—	70	—	90	—	100	—	ns
t_{AA}	Address Access Time	—	50	—	60	—	70	—	90	—	100	ns
t_{ACS}	Chip Select Access Time	—	50	—	60	—	70	—	90	—	100	ns
t_{OE}	Output Enable Access Time	—	35	—	40	—	40	—	45	—	50	ns
t_{OH}	Output Hold From Address Change	0	—	0	—	5	—	10	—	10	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	10	—	10	—	10	—	15	—	15	—	ns
t_{CHZ}[1]	Chip Select to Output in High Z	—	25	—	35	—	35	—	45	—	50	ns
t_{OHZ}[1]	Output Enable to Output in High Z	—	40	—	40	—	30	—	40	—	40	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Down Time	—	50	—	50	—	50	—	50	—	50	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	50	—	60	—	70	—	90	—	100	—	ns
t_{CW}	Chip Select to End of Write	45	—	50	—	60	—	80	—	95	—	ns
t_{AW}	Address Valid to End of Write	45	—	50	—	60	—	80	—	95	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	40	—	45	—	45	—	50	—	55	—	ns
t_{WR}	Write Recovery Time	5	—	5	—	5	—	5	—	5	—	ns
t_{DW}	Data Valid to End of Write	25	—	25	—	30	—	40	—	40	—	ns
t_{DH}	Data Hold Time	5	—	5	—	10	—	10	—	10	—	ns
t_{OHZ}[1]	Output Enable to Output in High Z	—	25	—	35	—	35	—	40	—	40	ns
t_{WHZ}[1]	Write Enabled to Output in High Z	—	25	—	35	—	35	—	40	—	40	ns
t_{OW}[1]	Output Active From End of Write	0	—	0	—	0	—	0	—	0	—	ns
$\overline{BUSY}$ TIMING												
t_{BAA}	$\overline{BUSY}$ Access Time to Address	—	40	—	45	—	45	—	45	—	50	ns
t_{BDA}	$\overline{BUSY}$ Disable Time to Address	—	40	—	45	—	45	—	45	—	50	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Select	—	40	—	40	—	40	—	40	—	50	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Select	—	35	—	35	—	35	—	35	—	50	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data	—	35	—	40	—	50	—	50	—	60	ns
t_{WDD}	Write Pulse to Data Delay	—	75	—	85	—	90	—	100	—	120	ns
t_{DDD}	Write Data Valid to Read Data	—	50	—	60	—	70	—	80	—	100	ns
t_{APS}	Arbitration Priority Set-up Time	10	—	10	—	10	—	10	—	10	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

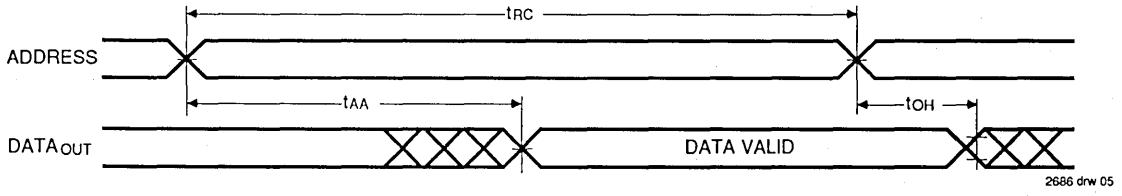
8

CAPACITANCE[1,2] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	IDT7M134S	IDT7M135S	Unit
$C_{IN(D)}$	Input Capacitance (Data)	V_{IN} = 0V	50	95	pF
$C_{IN(A)}$	Input Capacitance (Address)	V_{IN} = 0V	50	100	pF
$C_{IN(C)}$	Input Capacitance ($\overline{CS}$)	V_{IN} = 0V	14	14	pF
$C_{IN(C)}$	Input Capacitance ($\overline{BUSY}$, $\overline{OE}$)	V_{IN} = 0V	50	95	pF
$C_{IN(C)}$	Input Capacitance (R/$\overline{W}$)	V_{IN} = 0V	50	95	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	50	95	pF

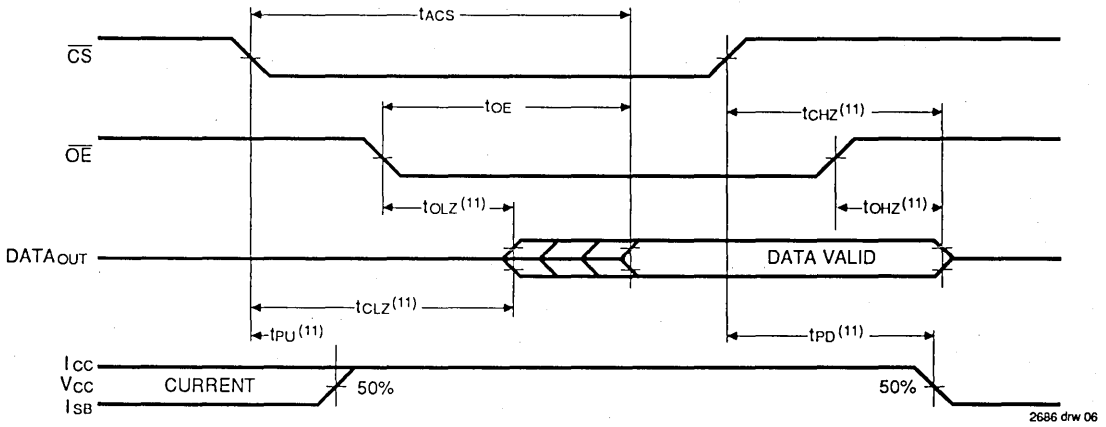
NOTES:
1. This parameter is guaranteed by design but not tested.
2. Typical values.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1,2,6]



2686 drw 05

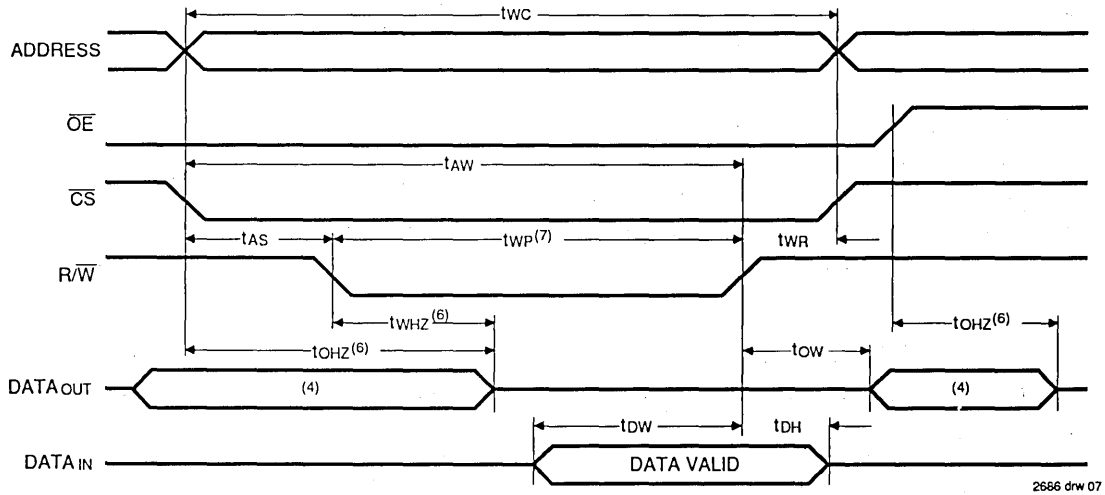
TIMING WAVEFORM OF READ CYCLE NO. 2 EITHER SIDE[1,3]



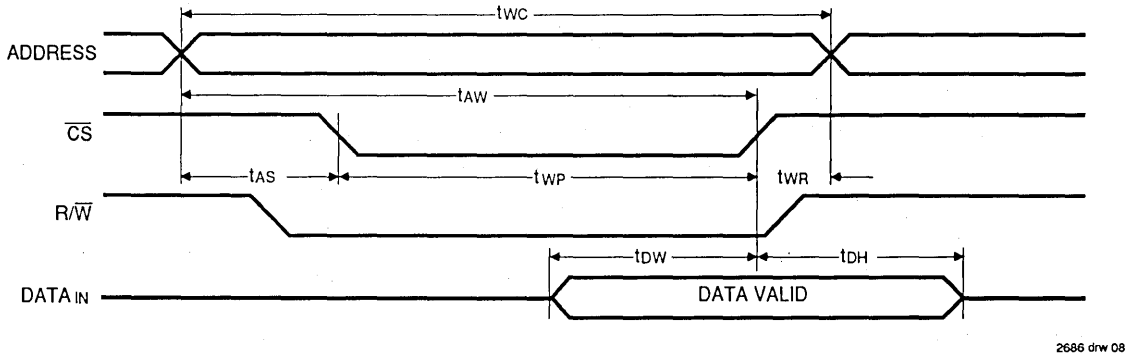
2686 drw 06

NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CS}$ = V_{IL}.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. If $\overline{CS}$ goes high simultaneously with R/$\overline{W}$ high, the outputs remain in the high impedance state.
5. $\overline{CS}_L$ = $\overline{CS}_R$ ≤ V_{IL}
6. $\overline{OE}$ = V_{IL}
7. R/$\overline{W}$ = V_{IH} during address transition.
8. Transition is measured at +500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
9. For SLAVE port (IDT7M144/IDT7M145) only.
10. Port-to-port delay through RAM cells from writing port to reading port.
11. This parameter guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING)(1,2,3,7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,3,5)

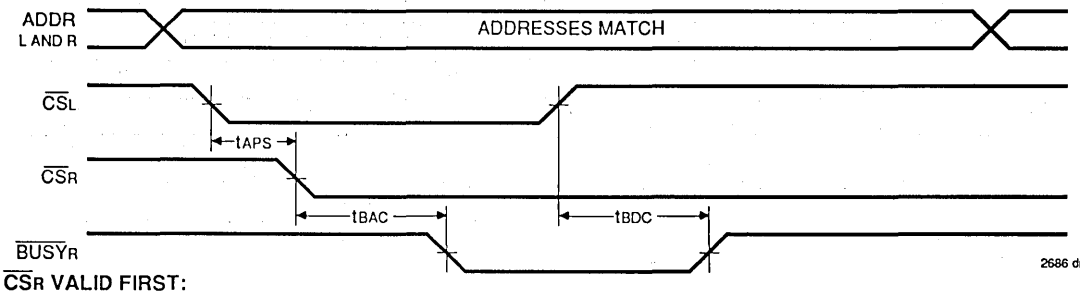


NOTES:
1. R/$\overline{W}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a R/$\overline{W}$ controlled write cycle, write pulse (tWP > tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

8

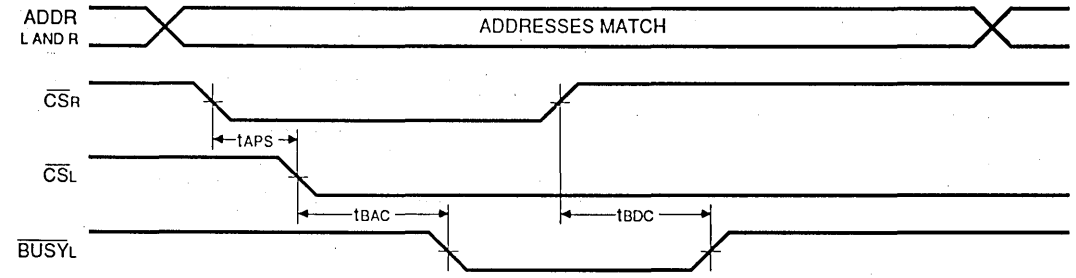
TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CS}$ ARBITRATION

$\overline{CS}_L$ VALID FIRST:



2686 drw 09

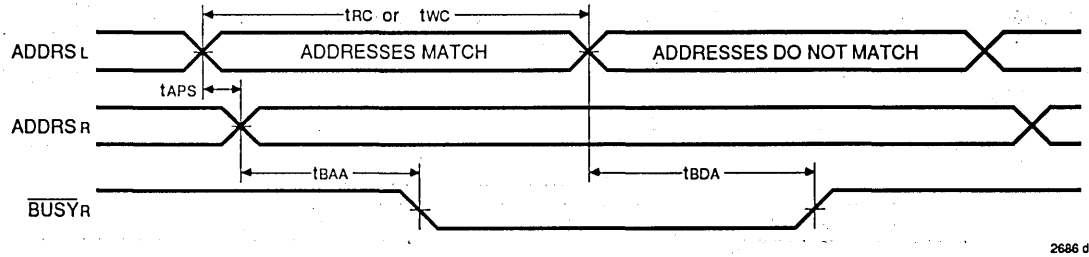
$\overline{CS}_R$ VALID FIRST:



2686 drw 10

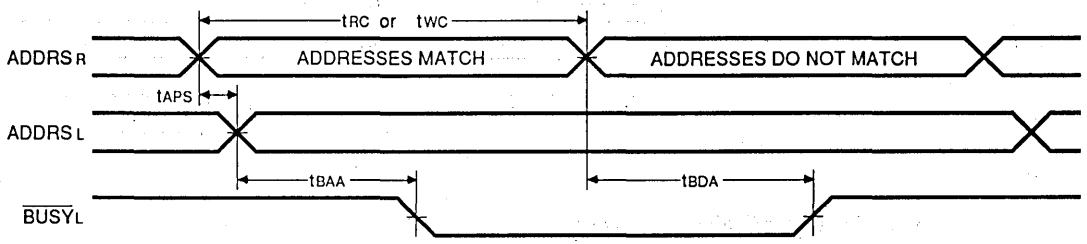
TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION(5)

LEFT ADDRESS VALID FIRST:



2686 drw 11

RIGHT ADDRESS VALID FIRST:

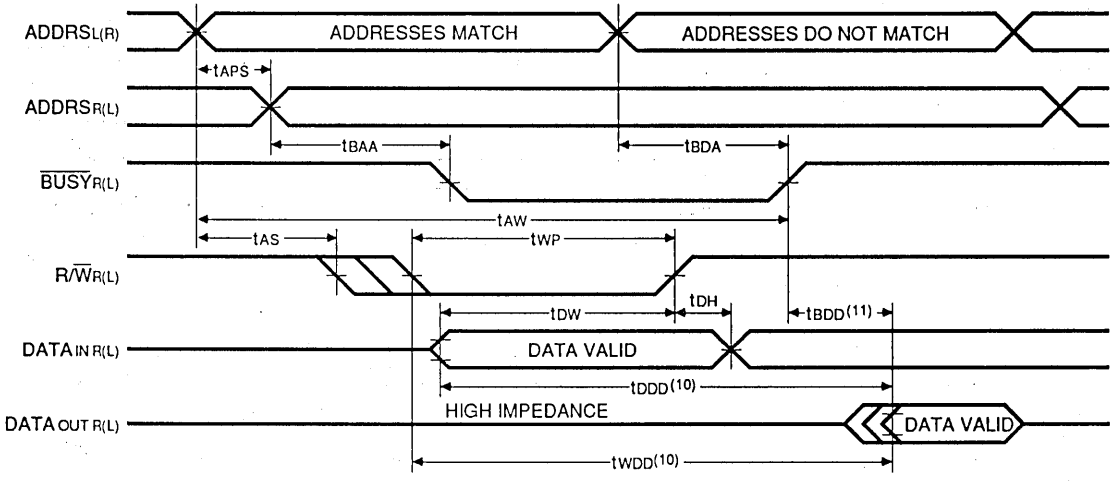


2686 drw 12

NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CS}$ = VIL.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. If $\overline{CS}$ goes high simultaneously with R/$\overline{W}$ high, the outputs remain in the high impedance state.
5. $\overline{CS}_L$ = $\overline{CS}_R$ ≤ VIL
6. $\overline{OE}$ = VIL
7. R/$\overline{W}$ = VIH during address transition.
8. Transition is measured at +500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
9. For SLAVE port (IDT7M144/IDT7M145) only.
10. Port-to-port delay through RAM cells from writing port to reading port.
11. This parameter guaranteed by design, but not tested.

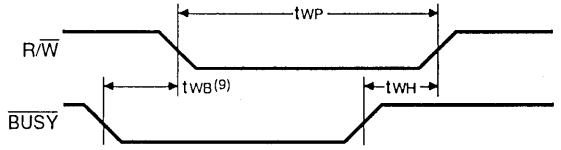
8

TIMING WAVEFORM OF READ WITH BUSY(5)



2686 drw 13

TIMING WAVEFORM OF WRITE WITH BUSY(5)



2686 drw 14

NOTES:
1. R/W is high for Read Cycles.
2. Device is continuously enabled, CS = VIL.
3. Addresses valid prior to or coincident with CS transition low.
4. If CS goes high simultaneously with R/W high, the outputs remain in the high impedance state.
5. CSL = CSR ≤ VIL
6. OE = VIL
7. R/W = VIH during address transition.
8. Transition is measured at +500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
9. For SLAVE port (IDT7M144/IDT7M145) only.
10. Port-to-port delay through RAM cells from writing port to reading port.
11. This parameter guaranteed by design, but not tested.

FUNCTIONAL DESCRIPTION

The IDT7M134/IDT7M135 provide two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7M134/IDT7M135 have an automatic power down feature controlled by $\overline{CS}$. The $\overline{CS}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CS}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table I.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION

The arbitration logic will resolve an address match or a chip select match down to 10ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and set the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CS}$, on-chip control logic arbitrates between $\overline{CS}_L$ and $\overline{CS}_R$ for access; or (2) if the $\overline{CS}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table III, Address Arbitration). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access complete its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION

Expanding the data bus width to sixteen-or-more-bits in a dual-port static RAM system implies that several modules will be active at the same time. If each module includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another activates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid this "busy lock-out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port static RAMs in width, the writing of the SLAVE modules must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE module may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems when more than one module is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

TRUTH TABLES

TABLE I — NON-CONTENTION READ/WRITE CONTROL, LEFT OR RIGHT PORT[1]

$R/\overline{W}$	$\overline{CS}$	$\overline{OE}$	I/O_{0-7}	FUNCTION
X	H	X	Z	Port Disabled and in Power Down Mode, I_{SB}
X	H	X	Z	$\overline{CS}_R = \overline{CS}_L$ = H, Power Down Mode, I_{SB} or I_{SB2}
L	L	X	$DATA_{IN}$	Data on Port Written into Memory[2]
H	L	L	$DATA_{OUT}$	Data in Memory Output on Port[3]
H	L	H	Z	High Impedance Outputs

NOTES:
1. A_{0L}-$A_{13L} \neq A_{0R}$-A_{13R}
2. If BUSY = L, data is not written.
3. If BUSY = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

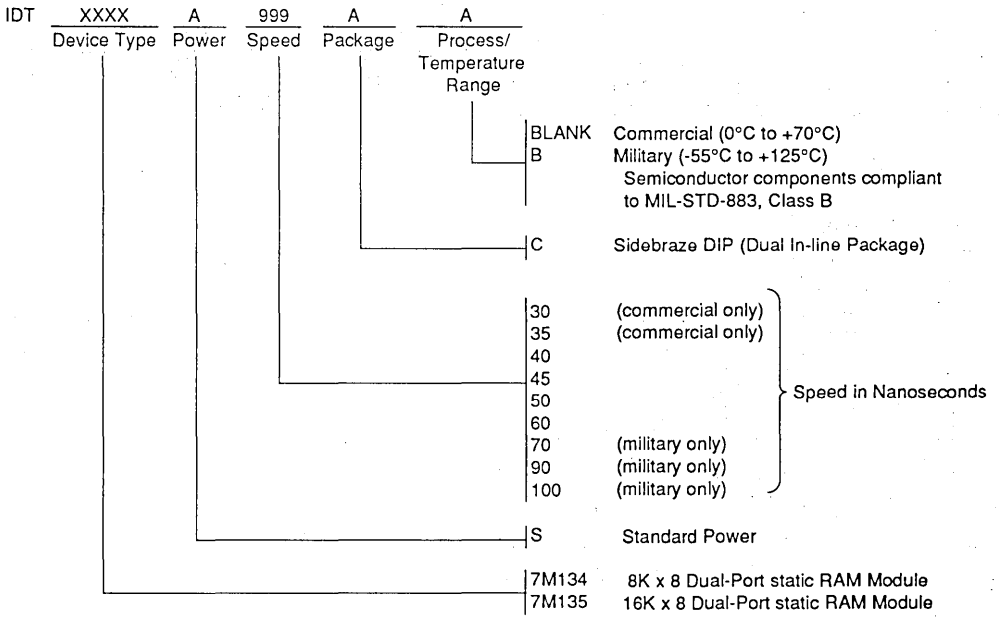
8

TABLE III — ARBITRATION

LEFT PORT		RIGHT PORT		FLAGS(1)		
$\overline{CS}_L$	A_{0L}-A_{13L}	$\overline{CS}_R$	A_{0L}-A_{13R}	$\overline{BUSY}_L$	$\overline{BUSY}_R$	FUNCTION
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	≠A_{0R}-A_{13R}	L	≠A_{0L}-A_{13L}	H	H	No Contention
ADDRESS ARBITRATION WITH $\overline{CS}$ LOW BEFORE ADDRESS MATCH						
L	LV10R	L	LV10R	H	L	Left-Port Wins
L	RV10L	L	LV10L	L	H	Right-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CS}$ ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CS}$						
LL10R	= A_{0R}-A_{13R}	LL10R	= A_{0L}-A_{13L}	H	L	Left-Port Wins
RL10L	= A_{0R}-A_{13R}	RL10R	= A_{0L}-A_{13L}	L	H	Right-Port Wins
LW10R	= A_{0R}-A_{13R}	LW10R	= A_{0L}-A_{13L}	H	L	Arbitration Resolved
LW10R	= A_{0R}-A_{13R}	LW10R	= A_{0L}-A_{13L}	L	H	Arbitration Resolved

NOTE:
1. X = DON'T CARE, L = LOW, H = HIGH, Same = Left and Right Addresses match within 10ns of each other.
   LV10R = Left Address Valid ≥ 10ns before Right Address.
   RV10L = Right Address Valid ≥ 10ns before Left Address.
   LL10R = Left $\overline{CS}$ = LOW ≥ 10ns before Right $\overline{CS}$.
   RL10L = Right $\overline{CS}$ = LOW ≥ 10ns before left $\overline{CS}$.
   LW10R = Left and Right $\overline{CS}$ = LOW within 10ns of each other.

ORDERING INFORMATION



2686 drw 15

Integrated Device Technology, Inc.

8K x 8
16K x 8
CMOS DUAL-PORT STATIC RAM MODULE (SLAVE)

IDT7M144S
IDT7M145S

FEATURES:

- High-density 64K/128K CMOS SLAVE Dual-Port static RAM modules
- 16K x 8 (IDT7M145) or 8K x 8 (IDT7M144) option
- Easily expands data bus width to 16-or-more-bits when used with MASTER IDT7M134 or IDT7M135 modules
- Fully asynchronous read/write operation from either port
- Fast access time
  - commercial: 30ns (max.)
  - military: 40ns (max.)
- Low-power consumption
- $\overline{BUSY}$ output flags
- Dual Vcc and GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Single 5V (±10%) power supply

DESCRIPTION:

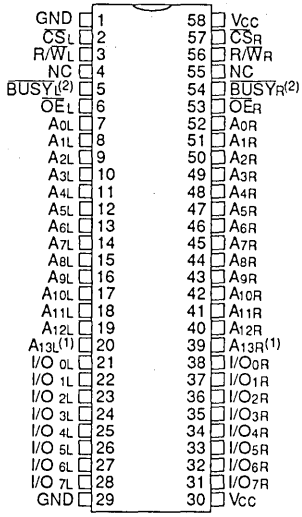
The IDT7M144/IDT7M145 are 64K/128K high-speed CEMOS™ SLAVE Dual-Port static RAM modules constructed on a multi-layered, co-fired, ceramic substrate using four IDT7142 2K x 8 SLAVE dual-port static RAMs (IDT7M144) or eight IDT7142 SLAVE dual-port static RAMs (IDT7M145) in leadless chip carriers. Dual-port function is achieved by utilization of the two on-board IDT54/IDT74FCT138 decoder circuits that interpret the higher order addresses A_{L11-13} and A_{R11-13} to select one of the eight 2K x 8 dual-port static RAMs. (On IDT7M144 8K x 8 option, the A_{L13} and A_{R13} need to be externally grounded and the selection becomes one of the four 2K x 8 dual-port static RAMs).

The IDT7M144/IDT7M145 are designed as "SLAVE" dual-port static RAM modules to be used together with the IDT7M135/IDT7M135 "MASTER" dual-port RAM modules in 16-or-more-bit systems, whereas the IDT7M134/IDT7M135 are designed to be used as stand-alone 8-bit dual-port static RAM modules. Using the IDT MASTER/SLAVE dual-port static RAM module approach in 16-or-more-bit memory system applications results in full speed operation without the need for additional discrete logic.

Both SLAVE IDT7M144/IDT7M145 and MASTER IDT7M134/IDT7M135 modules provide two ports with separate control, address and I/O pins that permit independent asynchronous access for reads or writes to any location in the memory. The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. The delayed port will have access when $\overline{BUSY}$ goes high (inactive). The $\overline{BUSY}$ pins are outputs on the MASTER and inputs on the SLAVE.

All military module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883 Class B, making them ideally suited for applications demanding the highest level of performance and reliability.

PIN CONFIGURATION (3)



DIP
TOP VIEW

2687 dwg 01

PIN NAMES

Left Port	Right Port	Names
A_{0L}-A_{13L}	A_{0R}-A_{13R}	Address Input
I/O_{0L}-IO_{7L}	I/O_{0R}-I/O_{7R}	Data Input/Output
$\overline{CS_L}$	$\overline{CS_R}$	Chip Select
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$\overline{BUSY}_L$	$\overline{BUSY}_R$	$\overline{BUSY}$ Input
Vcc	Vcc	Power
GND	GND	Ground

NOTES:

1. On 8K x 8 IDT7M144 option, A_{13L} and A_{13R} need to be externally connected to ground for proper operation.
2. IDT7M134/IDT7M135 (MASTER): $\overline{BUSY}$ is open drain output and requires pull up resistor. IDT7M144/IDT7M145 (SLAVE): $\overline{BUSY}$ is input.
3. For module dimensions, please refer to module drawing M12 in the packaging section.

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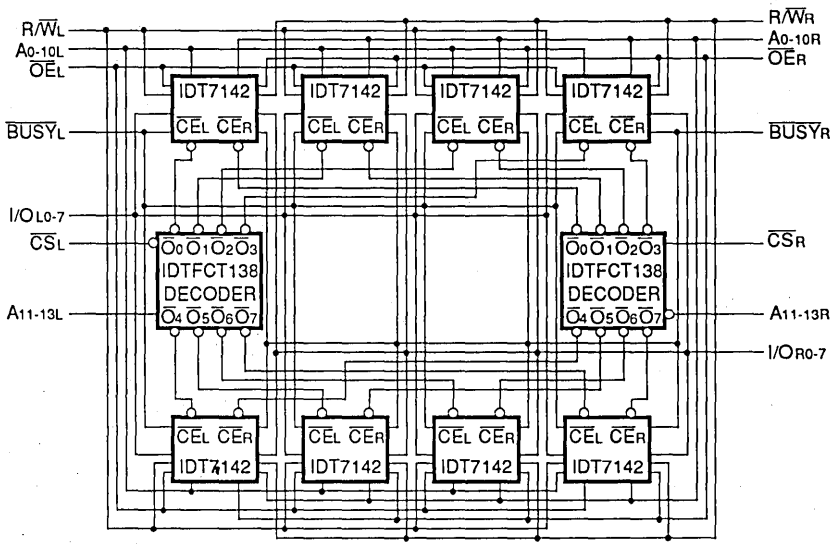
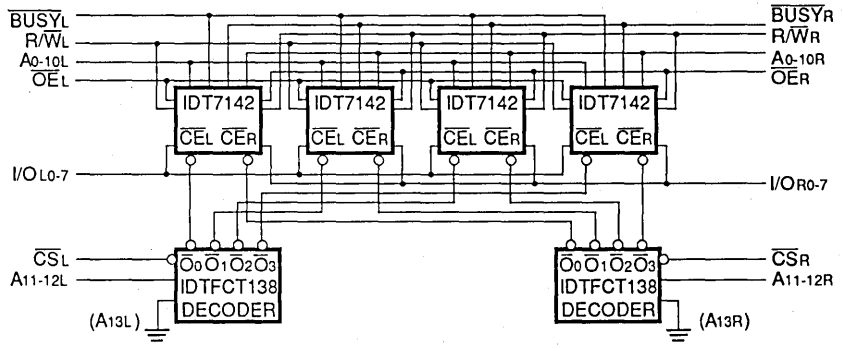
FUNCTIONAL BLOCK DIAGRAMS

IDT7M145 (16K x 8)



2687 dwg 02

IDT7M144 (8K x 8)



2687 dwg 03

(GROUND A_{13L} AND A_{13R} EXTERNALLY)

DC ELECTRICAL CHARACTERISTICS
OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

(DC electricals for the IDT7M144/IDT7M145 SLAVE module are identical to the IDT7M134/IDT7M135 MASTER module. Reference the IDT7M134/IDT7M135 CMOS Dual-Port static RAM data sheet.)

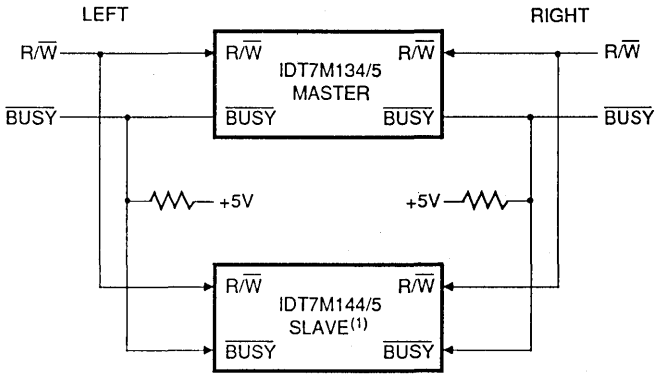
AC ELECTRICAL CHARACTERISTICS
OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

(AC electricals for the IDT7M144/IDT7M145 SLAVE module are identical to the IDT7M134/IDT7M135 MASTER module except where noted below.)

Symbol	Parameter	IDTM144S30 IDTM145S30 (Com'l. Only) Min.	Max.	IDTM144S35 IDTM145S35 (Com'l. Only) Min.	Max.	IDTM144S40 IDTM145S40 Min.	Max.	IDTM144S45 IDTM145S45 Min.	Max.	Unit
tWB	Write to $\overline{BUSY}$	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$	20	—	20	—	20	—	20	—	ns

Symbol	Parameter	IDTM144S50 IDTM145S50 Min.	Max.	IDTM144S60 IDTM145S60 Min.	Max.	IDTM144S70 IDTM145S70 (Mil. Only) Min.	Max.	IDTM144S90 IDTM145S90 (Mil. Only) Min.	Max.	IDTM144S100 IDTM145S100 (Mil. Only) Min.	Max.	Unit
tWB	Write to $\overline{BUSY}$	0	—	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$	20	—	20	—	20	—	20	—	20	—	ns

16-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEM

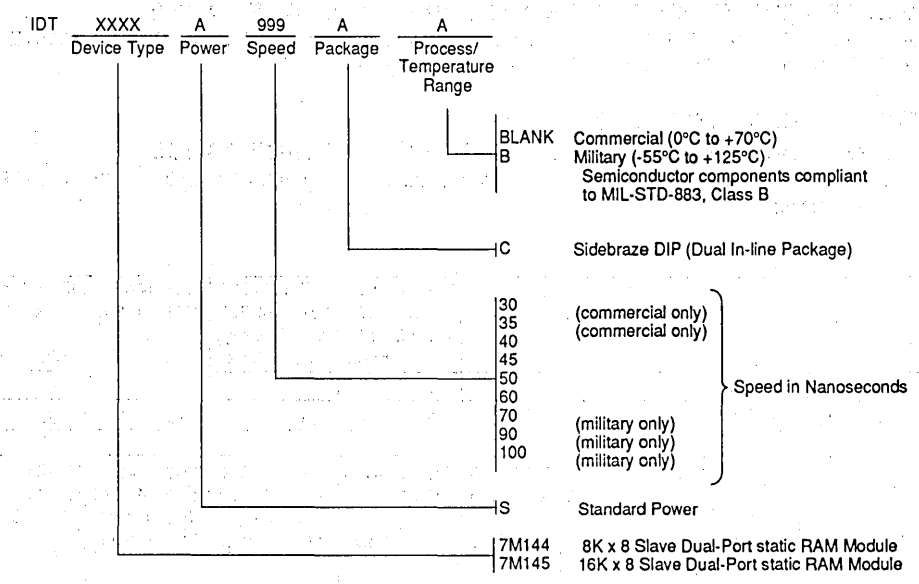


2687 dwg 04

NOTE:
1. No arbitration in IDT7M144/IDT7M145 (SLAVE): $\overline{BUSY}$ in inhibits write in IDT7M144/IDT7M145.

8

ORDERING INFORMATION



Integrated Device Technology, Inc.

32K X 8 CMOS DUAL-PORT STATIC RAM MODULE

IDT7M137

FEATURES:

- High-density 256K CMOS Dual-Port static RAM module
- 32K x 8 organization
- Fully asynchronous read/write operation from either port
- Fast access time
  - commercial: 30ns (max.)
  - military: 40ns (max.)
- Low power consumption
- Dual Vcc and GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Single 5V (±10%) power supply

DESCRIPTION:

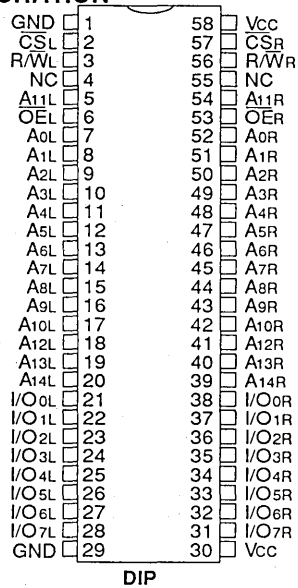
The IDT7M137 is a 256K high-speed CMOS Dual-Port static RAM module constructed on a multi-layered ceramic substrate using eight IDT7134 dual-port static RAMs in leadless chip carriers. The full 32K bytes of dual-port static RAM are directly addressable by utilization of the two on-board IDT54/IDT74FCT138 decoder circuits that interpret the higher order addresses A_{L12-14} and A_{R12-14} to select one of the eight 4K x 8 dual-port static RAMs. Extremely high speeds are achieved in this fashion due to the use of the IDT7134 dual-port static RAM, fabricated in IDT's high-performance CEMOS™ technology.

The IDT7M137 provides two ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in the memory. The IDT7M137 is designed to be used in systems where on-chip hardware port arbitration is not needed. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports.

The IDT7M137 is available with access times as fast as 30ns commercial and 40ns military temperature range. The module fits into a 58-pin sidebrazed DIP (Dual In-line Package).

All IDT7M137 military module semiconductor components are manufactured in compliance to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION(1)



2685 drw 01

DIP
TOP VIEW

NOTE:

1. For module dimensions, please refer to module drawing M12 in the packaging section.

PIN NAMES

LEFT PORT	RIGHT PORT	NAMES
Vcc	Vcc	Power
GND	GND	Ground
$\overline{CS}_L$	$\overline{CS}_R$	Chip Select
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L-14L}	A_{0R-14R}	Address
I/O_{0L-7L}	I/O_{0R-7R}	Data Input/Output
NC	NC	No Connect

2685 tbl 01

8

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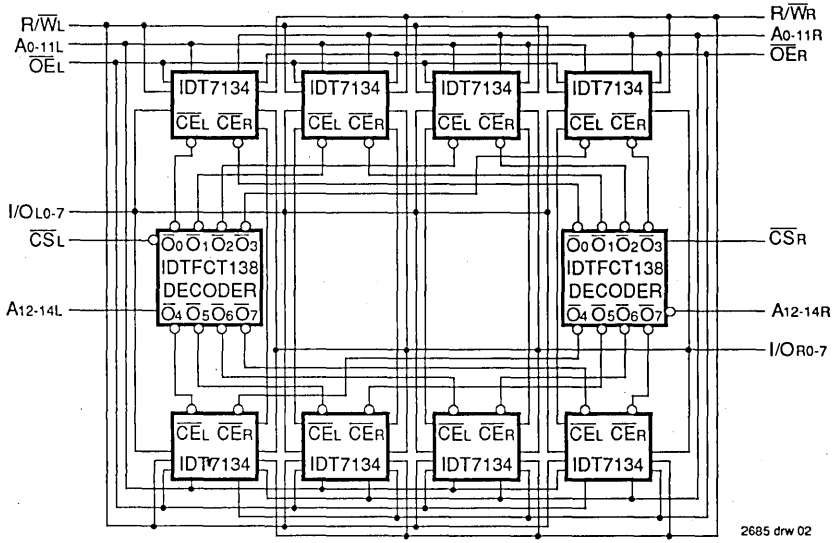


FUNCTIONAL DESCRIPTION:

The IDT7M137 provides two ports with separate controls, address and I/O that permit independent access for reads or writes to any location in memory. The IDT7M137 has an automatic power down feature controlled by $\overline{CS}$. The $\overline{CS}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CS}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2685 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2685 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:
1. V_{IL} = -3.0V for pulse width less than 20ns.

2685 tbl 04

CAPACITANCE (1) (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C_{OUT}	Output Capacitance	V_{IN} = 0V	120	pF
C_{IN}	Input Capacitance	V_{OUT} = 0V	50	pF

NOTE:
1. This parameter is guaranteed by design, but not tested.

2685 tbl 09

DC ELECTRICAL CHARACTERISTICS (4)

(Vcc = 5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7M137 Min.	Typ.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	Vcc = 5.5V, V_{IN} = 0V to Vcc	—	—	20	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to Vcc	—	—	20	µA
V_{IH}	Input High Voltage		2.2	—	6.0	V
V_{IL}	Input Low Voltage		-1.0(2)	—	0.8	V
Icc	Dynamic Operating Current (Both Ports Active)	$\overline{CS}$= V_{IL}, Outputs Open	—	275	730	mA
I_{SB}	Standby Current (Both Ports Standby)	$\overline{CS_L}$ and $\overline{CS_R}$ ≥ V_{IH}, Vcc = Max., Both Ports Outputs Open	—	200	560	mA
I_{SB1}	Standby Current (One Port Standby)	$\overline{CS_L}$ or $\overline{CS_R}$ ≥ V_{IH}, Vcc = Max., Active Port Outputs Open	—	225	650	mA
I_{SB2}	Full Standby Current (Both Ports Full Standby)	Both Ports $\overline{CS_L}$ and $\overline{CS_R}$ ≥ Vcc -0.2V V_{IN} ≥ Vcc -0.2V or V_{IN} ≤ 0.2V	—	8	240(3)	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA I_{OL} = 10mA	— —	— —	0.4 0.5	V V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	—	V

2685 tbl 05

NOTES:
1. Vcc = 5V, T_A = +25°C
2. V_{IL} min. = -3.0V for pulse width less than 30ns.
3. I_{SB2} max. of IDTM137 at commercial temperature = 150mA.4. For tAA = 30, 35, 40, 45ns versions all DC parameters are preliminary only.

8

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1,2 and 3

2685 tbl 08

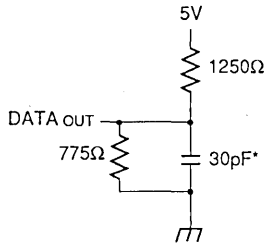
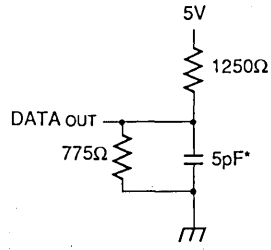


Figure 1.
Output Load



2685 drw 07

Figure 2.
Output Load
(for tHZ, tLZ, tWZ, and tOW)

* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V ±10%, TA = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	7M137S30 (Com'l. Only) Min.	Max.	7M137S35 (Com'l. Only) Min.	Max.	7M137S40 Min.	Max.	7M137S45 Min.	Max.	Unit
READ CYCLE										
tRC	Read Cycle Time	30	—	35	—	40	—	45	—	ns
tAA	Address Access Time	—	30	—	35	—	40	—	45	ns
tACS	Chip Select Access Time	—	30	—	35	—	40	—	45	ns
tOE	Output Enable Access Time	—	15	—	20	—	25	—	30	ns
tOH	Output Hold From Address Change	0	—	0	—	0	—	0	—	ns
tCLZ(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	ns
tCHZ(1)	Chip Select to Output in High Z	—	10	—	15	—	15	—	25	ns
tOHZ(1)	Output Enable to Output in High Z	—	10	—	15	—	15	—	25	ns
tOLZ(1)	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	ns
tPU(1)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
tPD(1)	Chip Deselect to Power Down Time	—	50	—	50	—	50	—	60	ns
WRITE CYCLE										
tWC	Write Cycle Time	30	—	35	—	40	—	45	—	ns
tCW	Chip Select to End of Write	25	—	30	—	35	—	40	—	ns
tAW	Address Valid to End of Write	25	—	30	—	35	—	40	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	20	—	25	—	30	—	40	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	20	—	20	—	22	—	22	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tOHZ(1)	Output Enable to Output in High Z	—	10	—	15	—	15	—	20	ns
tWHZ(1)	Write Enabled to Output in High Z	—	10	—	15	—	15	—	20	ns
tOW(1)	Output Active From End of Write	0	—	0	—	0	—	0	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.

2685 tbl 06

AC ELECTRICAL CHARACTERISTICS

(Vcc = 5.0V± 10%, TA = -55°C to + 125°C and 0°C to + 70°C) (Continued)

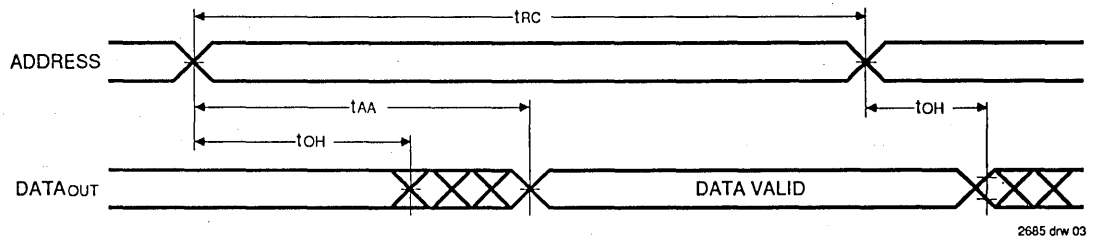
Symbol	Parameter	IDTM137S55 Min.	IDTM137S55 Max.	IDTM137S60 Min.	IDTM137S60 Max.	IDTM137S70 (Mil. Only) Min.	IDTM137S70 (Mil. Only) Max.	IDTM137S90 (Mil. Only) Min.	IDTM137S90 (Mil. Only) Max.	IDTM137S100 (Mil. Only) Min.	IDTM137S100 (Mil. Only) Max.	Unit
READ CYCLE												
tRC	Read Cycle Time	55	—	60	—	70	—	90	—	100	—	ns
tAA	Address Access Time	—	55	—	60	—	70	—	90	—	100	ns
tACS	Chip Select Access Time	—	55	—	60	—	70	—	90	—	100	ns
tOE	Output Enable Access Time	—	35	—	35	—	40	—	40	—	40	ns
tOH	Output Hold From Address Change	0	—	0	—	0	—	10	—	10	—	ns
tCLZ (1)	Chip Select to Output in Low Z	15	—	15	—	15	—	15	—	15	—	ns
tCHZ (1)	Chip Select to Output in High Z	—	35	—	40	—	40	—	40	—	40	ns
tOLZ (1)	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
tOHZ (1)	Output Enable to Output in High Z	—	30	—	35	—	40	—	40	—	40	ns
tPU (1)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
tPD (1)	Chip Deselect to Power Down Time	—	60	—	60	—	60	—	60	—	60	ns
WRITE CYCLE												
tWC	Write Cycle Time	55	—	60	—	70	—	90	—	100	—	ns
tCW	Chip Select to End of Write	50	—	55	—	60	—	80	—	90	—	ns
tAW	Address Valid to End of Write	50	—	55	—	60	—	80	—	90	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	45	—	50	—	55	—	70	—	80	—	ns
tWR	Write Recovery Time	5	—	5	—	5	—	10	—	10	—	ns
tDW	Data Valid to End of Write	25	—	30	—	35	—	45	—	50	—	ns
tDH	Data Hold Time	5	—	5	—	5	—	10	—	10	—	ns
tOHZ (1)	Output Enable to Output in High Z	—	35	—	40	—	40	—	40	—	50	ns
tWHZ (1)	Write Enabled to Output in High Z	0	35	0	40	0	40	0	40	0	50	ns
tOW (1)	Output Active From End of Write	0	—	0	—	0	—	0	—	0	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.

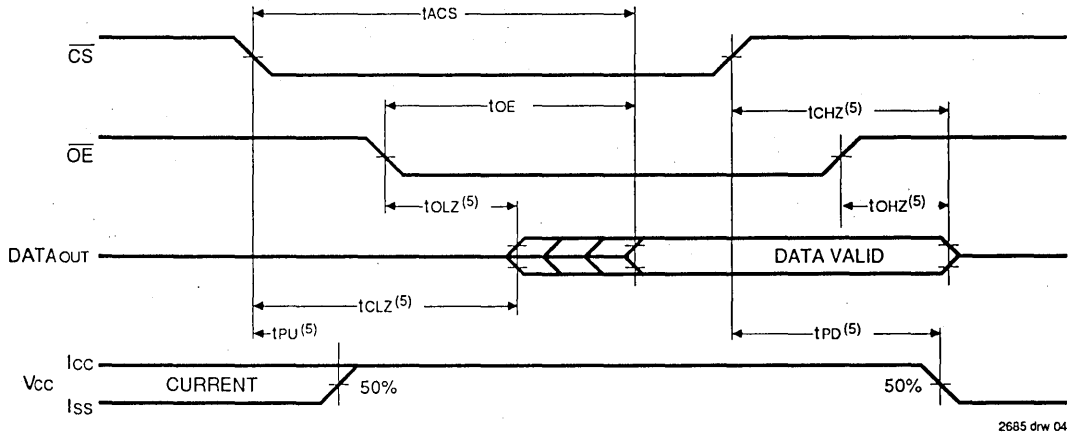
2685 tbl 07

8

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE (1, 2, 4)

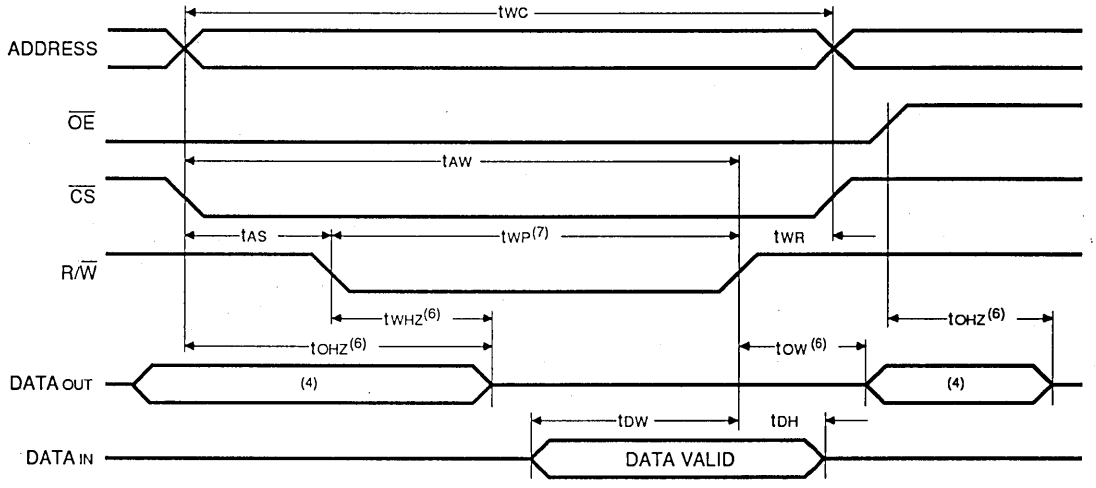


TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1, 3)



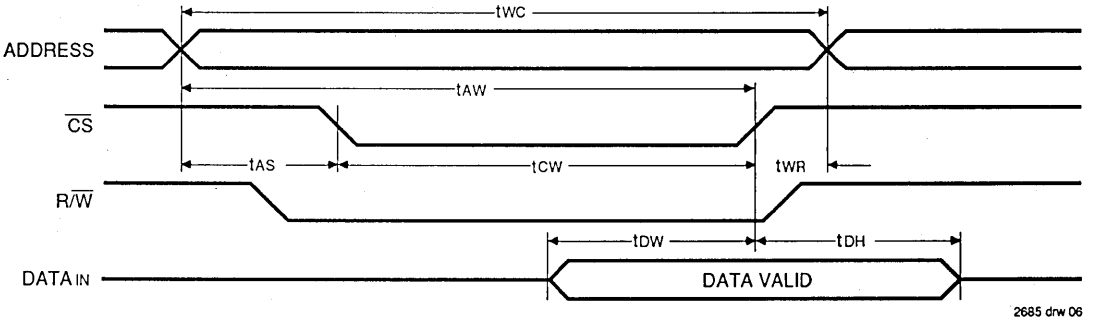
NOTES:
1. R/$\overline{W}$ is High for Read Cycles.
2. Device is continuously enabled, $\overline{CS}$ = VIL.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING)[1, 2, 3, 7]



2685 drw 05

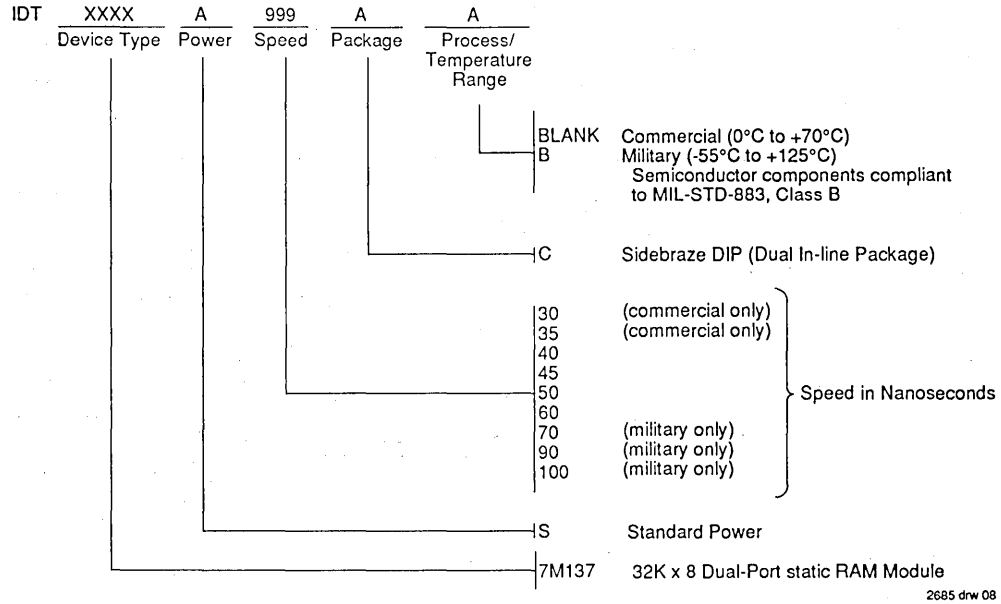
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 5]



2685 drw 06

NOTES:
1. R/$\overline{W}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a R/$\overline{W}$ controlled write cycle, write pulse (tWP) > (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

8


IDT
XXXX
Device Type
A
Power
999
Speed
A
Package
A
Process/
Temperature
Range
BLANK
Commercial (0°C to +70°C)
B
Military (-55°C to +125°C)
Semiconductor components compliant
to MIL-STD-883, Class B
C
Sidebraze DIP (Dual In-line Package)
30
(commercial only)
35
(commercial only)
40
45
50
60
70
(military only)
90
(military only)
100
(military only)
Speed in Nanoseconds
S
Standard Power
7M137
32K x 8 Dual-Port static RAM Module
2685 drw 08

Integrated Device Technology, Inc.

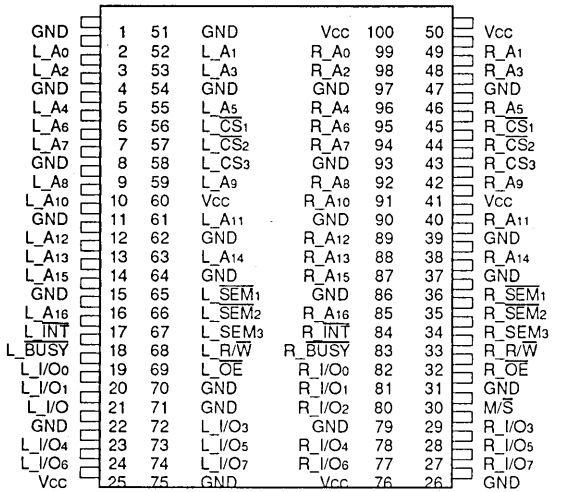
128K x 8
64K x 8
CMOS DUAL-PORT RAM MODULE

ADVANCE INFORMATION
IDT7M1001
IDT7M1003

FEATURES:

- High density 1 megabit/512K CMOS Dual-Port static RAM modules
- Fast access times
  - commercial: 40, 45, 55, 65, 80ns
  - military: 45, 55, 65, 80, 100ns
- Fully asynchronous read/write operation from either port
- Easy to expand data bus width to 16-bits or more using the Master/Slave function
- On-chip port arbitration logic and $\overline{BUSY}$ output flag
- $\overline{INT}$ flag for port-to-port communication
- Full on-chip hardware support of semaphore signaling between ports
- Surface mounted fine pitch (25 mil) LCC packages allow a through-hole module to fit onto 2.5 sq. inches of board space
- Single 5V (± 10%) power supply
- Inputs/outputs directly TTL compatible

PIN CONFIGURATION (1)



QIP
TOP VIEW

2804 drw 01

NOTE:
1. For module dimensions, please refer to drawing M18 (7M1001) and M19 (7M1003) in the packaging section.

DESCRIPTION:

The IDT7M1001/1003 are 1 megabit/512K high-speed CMOS Dual-Port RAM modules constructed on a co-fired ceramic substrate using 8 IDT7006 (16K X 8) Dual-Port RAMs or depopulated with only 4 IDT7006 Dual-Port RAMs. The IDT7M1001/1003 modules are designed to be used as stand-alone 1 megabit/512K dual-port RAM or as a combination master/slave dual-port RAM for 16-bit or more word width systems. Using the IDT Master/Slave in that system application results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory. System performance is enhanced by facilitating port-to-port communication via additional control signals $\overline{SEM}$ & $\overline{INT}$.

The IDT7M1001/1003 modules are packaged in an 80 pin ceramic QIP (Quad In-line Package) only 1.0 inches wide. Maximum access times as fast as 40ns are available over the commercial temperature range and 45ns over the military temperature range.

All IDT military modules are constructed with semiconductor components manufactured in compliance with the latest revision of MIL-STD-883 Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

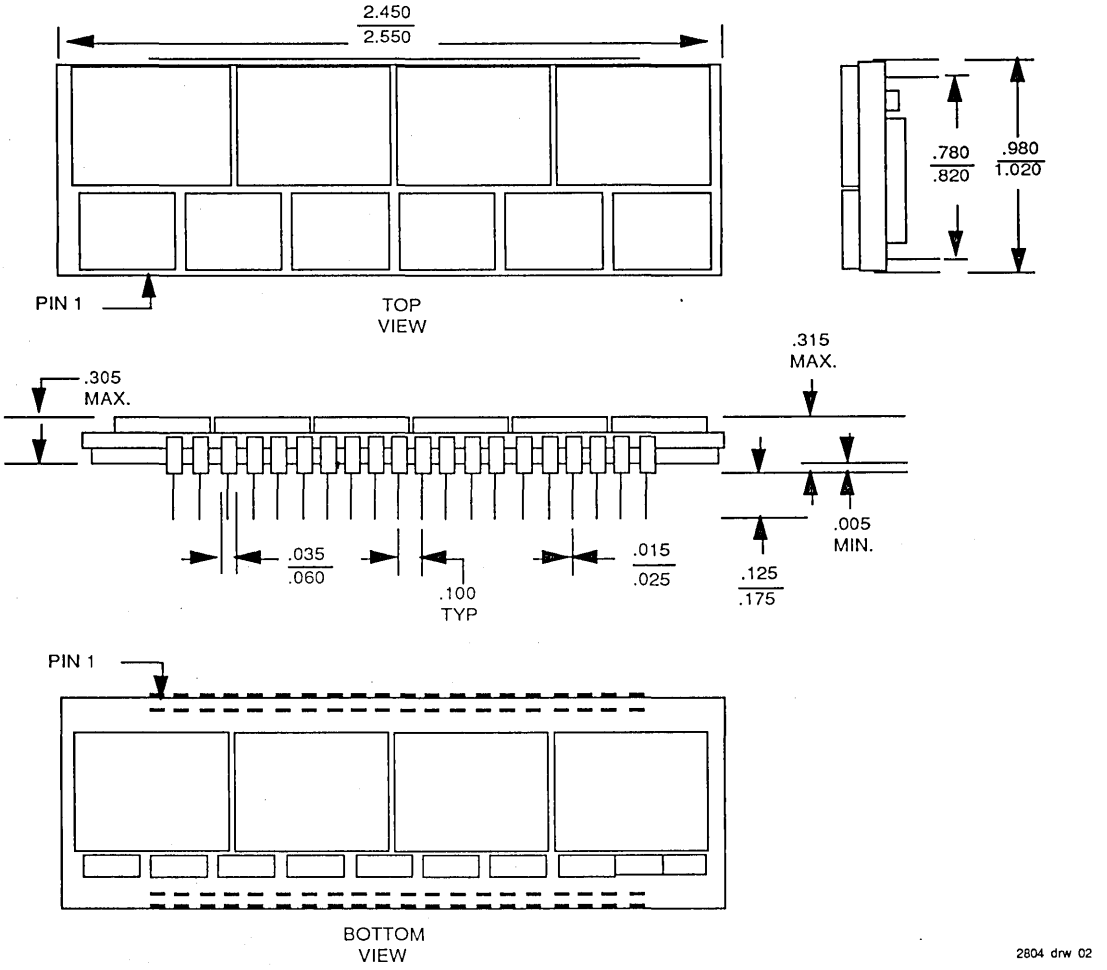
PIN NAMES

L_A0 - 16	Left Port Address Lines
R_A0 - 16	Right Port Address Lines
L_I/O0 - 7	Left Port Data Input/Output
R_I/O0 - 7	Right Port Data Input/Output
L_R/$\overline{W}$	Left Port Read/Write Select
R_R/$\overline{W}$	Right Port Read/Write Select
L_$\overline{CS}$1-3	Left Port Chip Selects
R_$\overline{CS}$1-3	Right Port Chip Selects
L_$\overline{OE}$	Left Port Output Enable
R_$\overline{OE}$	Right Port Output Enable
L_$\overline{BUSY}$	Left Port Busy Flag
R_$\overline{BUSY}$	Right Port Busy Flag
L_$\overline{INT}$	Left Port Interrupt Line
R_$\overline{INT}$	Right Port Interrupt Line
L_$\overline{SEM}$1-3	Left Port Semaphore Control
R_$\overline{SEM}$1-3	Right Port Semaphore Control
M/$\overline{S}$	Master/Slave Control
VCC	Power
GND	Ground

2804 tbl 01

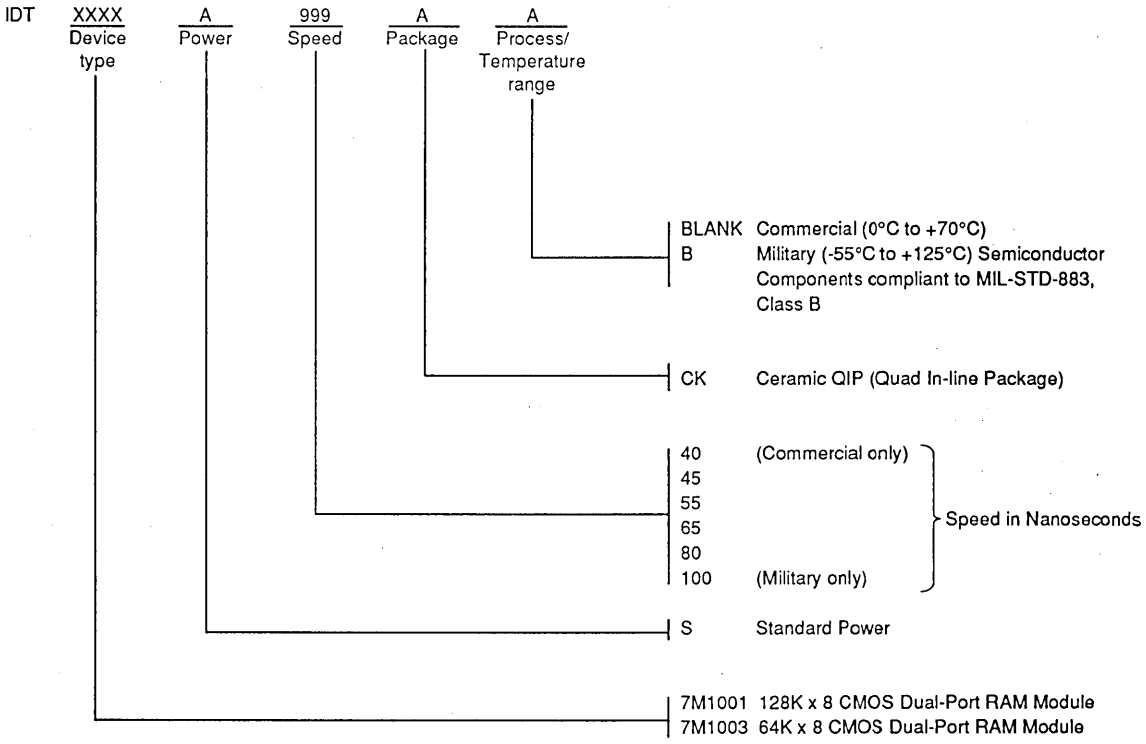
8

PACKAGE DIMENSIONS



2804 drw 02

ORDERING INFORMATION



8

Integrated Device Technology, Inc.

8K x 9
16K x 9
CMOS DUAL-PORT
STATIC RAM MODULES

PRELIMINARY
IDT7M1004
IDT7M1005

FEATURES:

- High density 8K/16K x 9 CMOS Dual-Port Static RAM modules
- Fast access times
  —commercial: 30, 35, 45, 55, 65ns
  —military: 40, 45, 55, 65, 80, 100ns
- Fully asynchronous read/write operation from either port
- Slave configuration only
- Expand data bus width to 18 bits or more using external arbitration
- Surface mounted LCC packages allow through-hole module to fit on a 60-pin sidebrazed DIP
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible

DESCRIPTION:

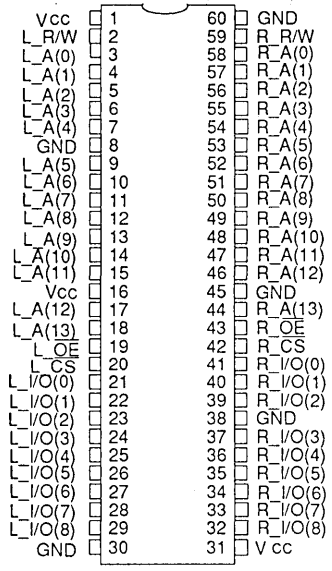
The IDT7M1004/1005 are 8K/16K x 9 high speed CMOS Dual-Port static RAM modules constructed on a co-fired ceramic substrate using 8 IDT7012 (2K x 9) Dual-Port RAMs or depopulated using only 4 IDT7012 Dual-Port RAMs. The IDT7M1004/1005 modules are designed to be used as stand alone dual-port RAM Slaves or as dual-port RAM slaves for 18-bit or more word width systems.

This module provides two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory. The IDT7M1004/1005 modules are configured only as Slaves. If contention (simultaneous access from both ports to the same exact address) is a possible occurance in this application, and data integrity is required, external logic must be used to compare address and control signals between the two sides to prevent a data conflict. Most often, users are able to assure by other means (such as software handshaking or interrupts) that such a contention between sides does not occur.

The IDT7M1004/1005 modules are packaged in a 60-pin ceramic sidebrazed DIP (Dual In-line Package). Maximum access times as fast as 30ns are available over the commercial temperature range and 40ns over the military temperature range.

All IDT military modules are constructed with semiconductor components manufactured in compliance with the latest revision of MIL-STD-883, Class B making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



DIP
TOP VIEW 2797 drw 14

PIN NAMES

Left Port	Right Port	Names
L_$\overline{CS}$	R_$\overline{CS}$	Chip Selects
L_R/$\overline{W}$	R_R/$\overline{W}$	Read/Write Enables
L_$\overline{OE}$	R_$\overline{OE}$	Output Enables
L_A (0–13)	R_A (0–13)	Address Inputs
L_I/O (0–8)	R_I/O (0–8)	Data Input/Outputs
Vcc		Power
GND		Ground

2797 tbl 01

NOTE:
1. On the IDT7M1004 option (8K x 9) L_A_{13} and R_A_{13} need to be connected to GND for proper operation of the module.

NOTE:
1. For module dimensions, please refer to drawing M14 in the packaging section.

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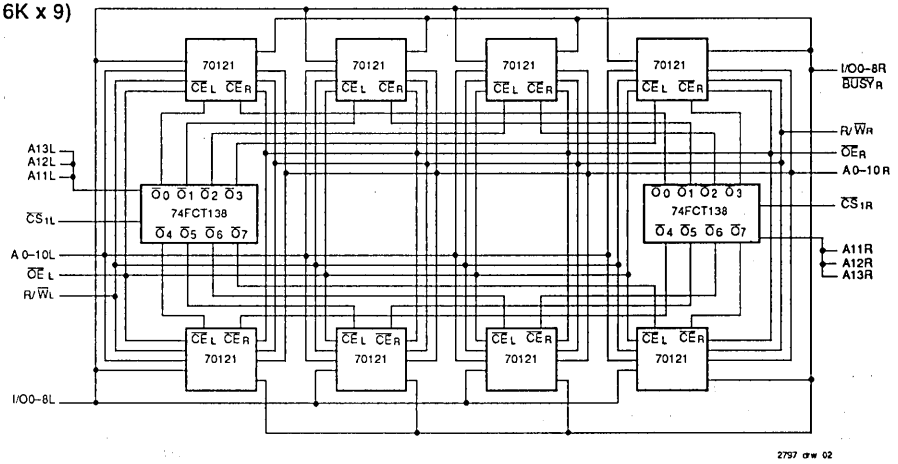
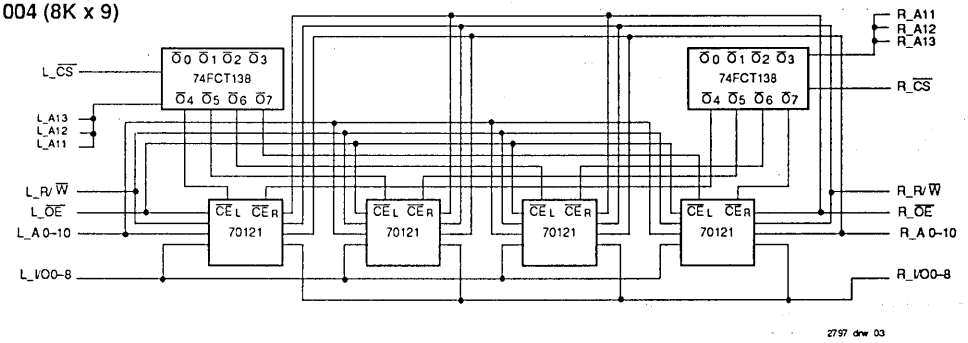
FUNCTIONAL BLOCK DIAGRAMS

IDT7M1005 (16K x 9)



IDT7M1004 (8K x 9)



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
TA	Operating Temperature	0 to +70	−55 to +125	°C
TBIAS	Temperature Under Bias	−55 to +125	−65 to +135	°C
TSTG	Storage Temperature	−55 to +125	−65 to +150	°C
IOUT	DC Output Current	50	50	mA

2797 tbl 02

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	−0.5(1)	—	0.8	V

NOTE:

1. VIL ≥ −3.0V for pulse width less than 20ns.

2797 tbl 03

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	−55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2797 tbl 04

CAPACITANCE TABLE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	IDT7M1004 Max.	IDT7M1005 Max.	Unit
C_IN(1)	Input Capacitance (A(0–10), $\overline{BUSY}$, $\overline{OE}$, R/$\overline{W}$)	V_IN = 0V	80	40	pF
C_IN(2)	Input Capacitance (Data)	V_IN = 0V	90	45	pF
C_IN(3)	Input Capacitance (A(11–13), $\overline{CS}$, $\overline{INT}$)	V_IN = 0V	12	12	pF
COUT	Output Capacitance (Data)	V_OUT = 0V	90	45	pF

NOTE:
1. This parameter is guaranteed by design but not tested.

2797 tbl 05

DC ELECTRICAL CHARACTERISTICS

(VCC = 5V ± 10%, TA = –55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7M1004 Min.	IDT7M1004 Max.	IDT7M1005 Min.	IDT7M1005 Max.	Unit
|ILI|	Input Leakage	VCC = Max. VIN = GND to VCC	—	40	—	80	µA
|ILO|	Output Leakage	VCC = Max. $\overline{CS}$ ≥ VIH, VOUT = GND to VCC	—	40	—	80	µA
VOL	Output Low Voltage	VCC = Min. IOL = 4mA	—	0.4	—	0.4	V
VOH	Output High Voltage	VCC = Min. IOH = -4mA	2.4	—	2.4	—	V

2797 tbl 06

DC ELECTRICAL CHARACTERISTICS

(VCC = 5V ± 10%, TA = –55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7M1004/5 (Com'l.) Min.	IDT7M1004/5 (Com'l.) Max.(1)	IDT7M1004/5 (Com'l.) Max.(2)	IDT7M1004/5 (Mil.) Min.	IDT7M1004/5 (Mil.) Max.(1)	IDT7M1004/5 (Mil.) Max.(2)	Unit
ICC2	Dynamic Operating Current (Both Ports Active)	VCC = Max., $\overline{CS}$ ≤ VIL, $\overline{SEM}$ = Don't Care Outputs Open, f = fMAX	—	500	870	—	560	860	mA
ISB	Standby Supply Current (Both Ports Inactive)	VCC = Max., $\overline{CS}$_L and $\overline{CS}$_R ≥ VIH Outputs Open, f = fMAX	—	280	560	—	280	560	mA
ISB1	Standby Supply Current (One Port Inactive)	VCC = Max., $\overline{CS}$_L or $\overline{CS}$ ≥ VIH Outputs Open, f = fMAX	—	370	650	—	430	750	mA
ISB2	Full Standby Supply Current (Both Ports Inactive)	$\overline{CS}$_L and $\overline{CS}$_R ≥ VCC –0.2V VIN > VCC 0.2V or < 0.2V $\overline{SEM}$_L and $\overline{SEM}$_R ≥ VCC –0.2V	—	60	120	—	120	240	mA

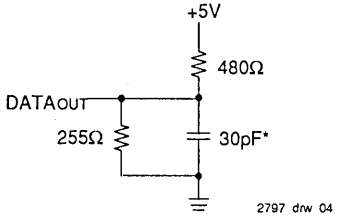
NOTES:
1. For IDT7M1004 (8K x 9) version only.
2. For IDT7M1005 (16K x 9) version only.

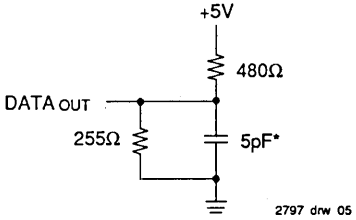
2797 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2797 tbl 08





*Including scope and jig.

Figure 1. Output Load

Figure 2. Output Load (For t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ}, t_{OW})

8

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

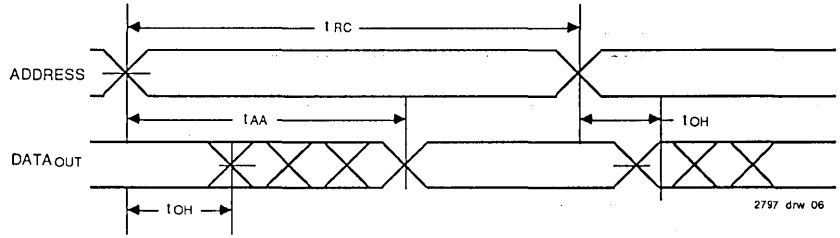
Symbol	Parameter	7M1004S30 7M1005S30 (Com'l. Only)		7M1004S35 7M1005S35 (Com'l. Only)		7M1004S40 7M1005S40		7M1004S45 7M1005S45		7M1004S55 7M1005S55		7M1004S65 7M1005S65		7M1004S80 7M1005S80 (Mil. Only)		7M1004S100 7M1005S100 (Mil. Only)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle																		
t_{RC}	Read Cycle Time	30	—	35	—	40	—	45	—	55	—	65	—	80	—	100	—	ns
t_{AA}	Address Access Time	—	30	—	35	—	40	—	45	—	55	—	65	—	80	—	100	ns
t_{ACS}[2]	Chip Select Access Time	—	30	—	35	—	40	—	45	—	55	—	65	—	80	—	100	ns
t_{OE}	Output Enable Access Time	—	15	—	20	—	20	—	25	—	30	—	35	—	40	—	45	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	3	—	3	—	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	15	—	15	—	15	—	20	—	25	—	30	—	35	—	40	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	3	—	3	—	3	—	5	—	5	—	5	—	5	—	5	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	15	—	15	—	15	—	20	—	25	—	30	—	35	—	40	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Up Time	—	50	—	50	—	50	—	50	—	50	—	50	—	50	—	50	ns
Write Cycle																		
t_{WC}	Write Cycle Time	30	—	35	—	40	—	45	—	55	—	65	—	80	—	100	—	ns
t_{CW}[2]	Chip Select to End of Write	25	—	30	—	35	—	40	—	45	—	50	—	55	—	60	—	ns
t_{AW}	Address Valid to End of Write	25	—	30	—	35	—	40	—	45	—	50	—	55	—	60	—	ns
t_{AS}	Address Set-Up Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	30	—	35	—	35	—	40	—	50	—	55	—	60	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	20	—	25	—	25	—	25	—	30	—	40	—	45	—	50	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	15	—	15	—	15	—	20	—	25	—	30	—	35	—	40	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	15	—	15	—	15	—	20	—	25	—	30	—	35	—	40	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns

NOTES:

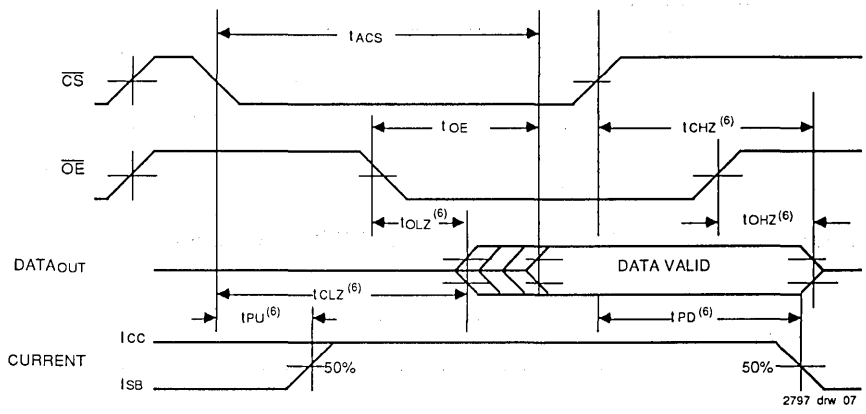
2797 tbl 09

1. This parameter is guaranteed by design but not tested.
2. To access RAM array, $\overline{CS} \leq V_{IL}$.
3. Master mode is not available on this module.
4. The module is always in the Slave Mode.
5. Port-to-Port delay through the RAM cells from the writing port to the reading port.
6. To ensure that the earlier of the two ports wins.
7. To ensure that the write cycle is inhibited during contention.
8. To ensure that a write cycle is completed after contention.

TIMING WAVEFORM OF READ CYCLE NO. 1 (EITHER SIDE) (1, 2, 4)



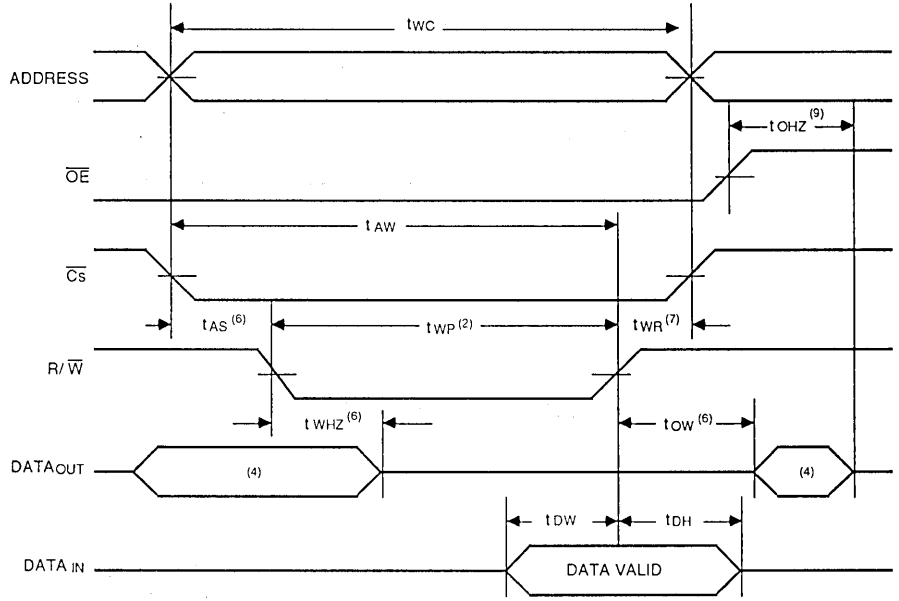
TIMING WAVEFORM OF READ CYCLE NO. 2 (EITHER SIDE) (1, 3, 5)



NOTES:
1. R/$\overline{W}$ is high for Read Cycles
2. Device is continuously enabled, $\overline{CS}$ = L. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low
4. $\overline{OE}$ = L
5. To access RAM, $\overline{CS}$ = L. To access semaphore, $\overline{CS}$ = H.
6. This parameter is guaranteed by design but not tested.

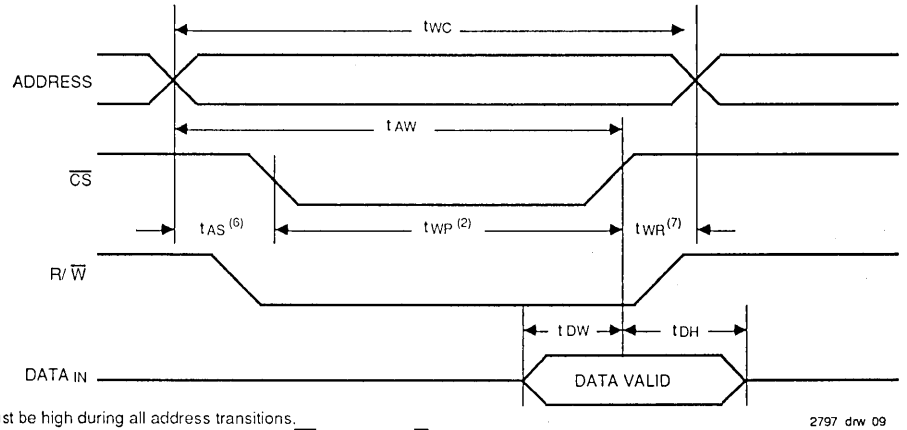
8

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING) (1, 3, 5, 8)



2797 drw 08

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING) (1, 3, 5, 8)

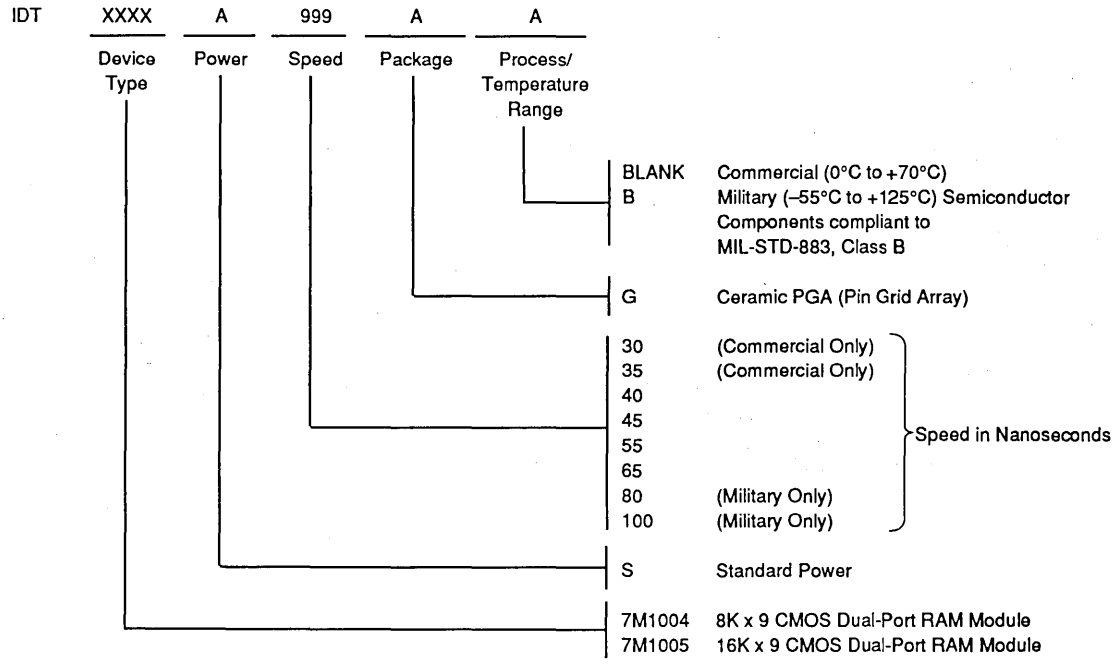


2797 drw 09

NOTES:

1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
9. This parameter is guaranteed by design but not tested.

ORDERING INFORMATION



8

Integrated Device Technology, Inc.

128K X 16, 64K X 16, 32K X 16 CMOS DUAL-PORT RAM

(SHARED MEMORY MODULE)

IDT7MB6036
IDT7MB6046
IDT7MB6056

FEATURES:

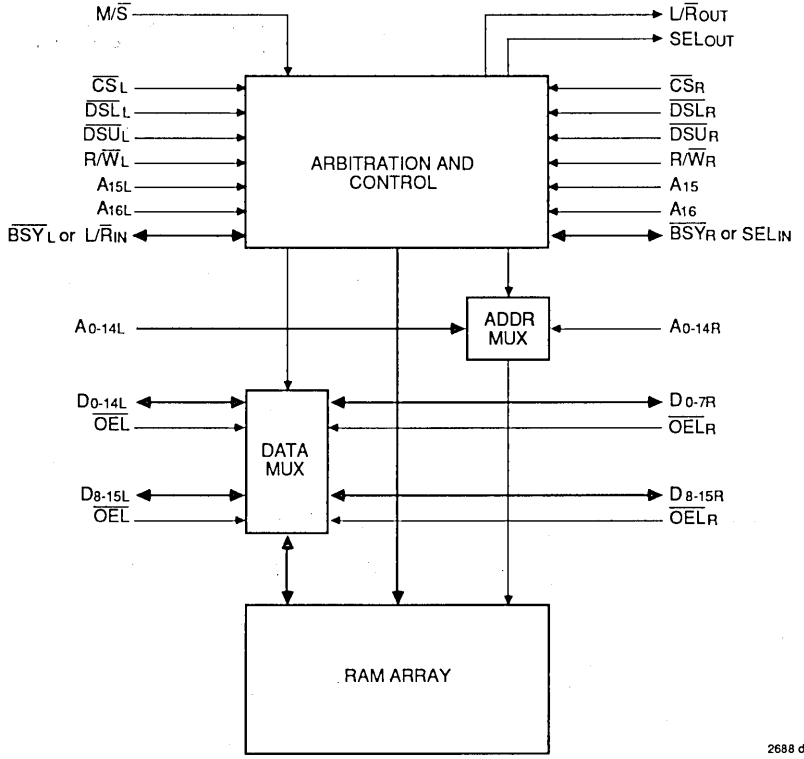
- High density 2 megabit/1 megabit/512K-bit CMOS Dual-Port static RAM (shared memory modules)
- Fully asynchronous read/write operation from either port
- Port arbitration/multiplexing logic by custom FCT chip set
- Memory array comprised of industry standard static RAM component
- Fast access time
  - 50ns (max.)
- Versatile controls: $\overline{BUSY}$ output flag and separate controls for lower and upper byte writes on each port
- Master/Slave control on-board for expanding word width
- Multiple GND and Vcc pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Single 5V (±10%) power supply

DESCRIPTION:

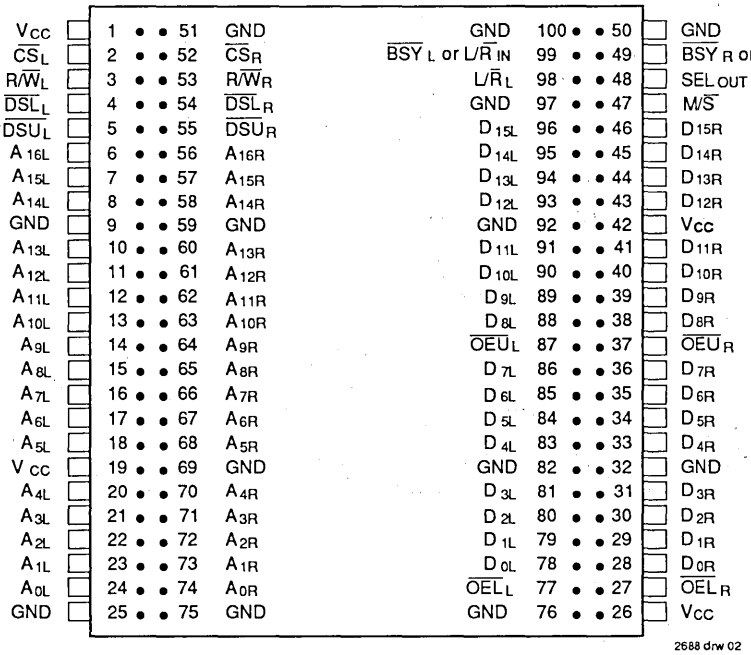
The Shared Memory Module provides two ports with separate control, address and Data I/O pins that permit independent access for read or writes to any location in the memory array. Using the on-board Master/Slave input allows these modules to be used as building blocks in 32-bit or more-bit systems requiring full speed operation without additional discrete logic.

In the Master Mode, the Shared Memory Module arbitrates asynchronously between the left and right ports $\overline{CS}$ inputs. The first to arrive is granted exclusive access to the entire RAM array for as long as its $\overline{CS}$ is asserted. If both ports attempt simultaneous access, the losing port will have its $\overline{BUSY}$ asserted until the winning port completes it access, at which time the second port will be granted its own exclusive access to the entire RAM array. See application note AN-74 for more details regarding proper module operating modes.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (1, 2, 3, 4, 5)



2688 drw 02

NOTES:
1. For module dimensions (7MB6036), please refer to drawing M20 in the packaging section.
2. For module dimensions (7MB6046), please refer to drawing M21 in the packaging section.
3. For module dimensions (7MB6056), please refer to drawing M22 in the packaging section.
4. Pins 7 and 57 must be grounded for proper operation of the 7MB6046 module.
5. Pins 6, 7, 56 and 57 must be grounded for proper operation of the 7MB6056 module.

PIN DESCRIPTION

Symbol	Description
VCC	Power
GND	Ground
A0-16L	Left Port Address
D0-15L	Left Port Data
A0-16R	Right Port Address
D0-15L	Right Port Data
R/$\overline{W}$	Read/Write Control
$\overline{CS}$	Active Low Chip Select
$\overline{DSL}$	Data Strobe for Lower Byte
$\overline{DSU}$	Data Strobe for Upper Byte
$\overline{OEL}$	Output Enable for Lower Byte
$\overline{OEU}$	Output Enable for Upper Byte
$\overline{BSY}$L or L/$\overline{R}$IN	Left Busy Output for Stand Alone or Master Mode. Left or Right Port Select Input for Slave Mode.
$\overline{BSY}$R or SELIN	Right Busy Output for Stand Alone or Master Mode. RAM Array Select Input for Slave Mode.
L/$\overline{R}$OUT	Left or Right Port Select Output on Master to be Connected to L/$\overline{R}$_IN Input on One or More Slaves when Width Expansion is Required.
SELOUT	RAM Array Select Output on Master to be Connected to SEL_IN Input on One or More Slaves when Width Expansion is Required.
M/$\overline{S}$	Master/Slave signal for cascading master w/one or more slaves.

8

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	-55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE

Symbol	Parameter	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	100	pF
COUT	Output Capacitance	VOUT = 0V	40	pF

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.0	—	6.0	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE:
1. VIL = -3.5V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V ± 10%, TA = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
|ILI|	Input Leakage Current	VCC = Max. VIN = GND to VCC	—	15	µA
|ILO|	Output Leakage Current	VCC = Max. $\overline{CS}$ = VIH, VOUT = GND to VCC	—	15	µA
ICC	Dynamic Operating Current	VCC = Max., $\overline{CS}$ ≤ VIL, f = fMAX, Output Open	—	520	mA
ISB	Standby Power Supply Current	$\overline{CS}$ ≥ VIH, VCC= MAX. Outputs Open, f = fMAX.	—	200	mA
VOH	Output Low Voltage	VCC = Min. IOH = –8mA	2.4	—	V
VOL	Output High Voltage	VCC = Min. IOL = 16mA		0.4	V

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

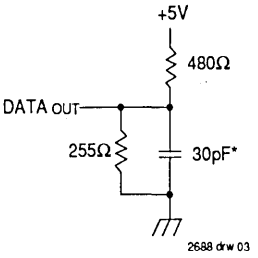


Figure 1. Output Load

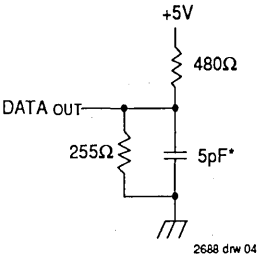


Figure 2. Output Load (for tOHZ and tOLZ)

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

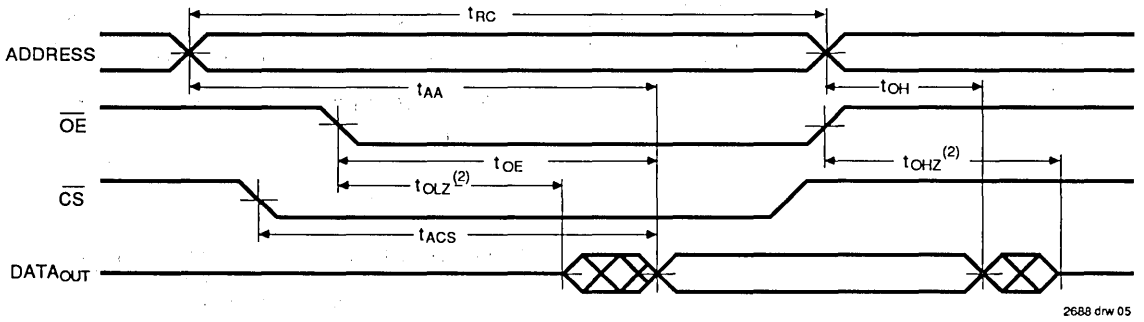
(VCC = 5.0V + 10%, TA = 0°C to +70°C)

Symbol	Parameter	7MB6036S50 7MB6046S50 7MB6056S50 Min.	Max.	7MB6036S60 7MB6046S60 7MB6056S60 Min.	Max.	7MB6036S70 7MB6046S70 7MB6056S70 Min.	Max.	7MB6036S85 7MB6046S85 7MB6056S85 Min.	Max.	7MB6036S100 7MB6046S100 7MB6056S100 Min.	Max.	7MB6036S120 7MB6046S120 7MB6056S120 Min.	Max.	Unit
No Contention Read														
tRC	Read Cycle Time	50	—	60	—	70	—	85	—	100	—	120	—	ns
tAA	Address Access Time	—	50	—	60	—	70	—	85	—	100	—	120	ns
tACS	Chip Select Access Time	—	50	—	60	—	70	—	85	—	100	—	120	ns
tOE	Output Enable to Data Valid	—	27	—	32	—	37	—	42	—	47	—	52	ns
tOH	O/P Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
tOLZ(1)	$\overline{OE}$ to Output in Low-Z	8	—	8	—	8	—	8	—	8	—	8	—	ns
tOHZ(1)	$\overline{OE}$ to Output in High-Z	—	7.5	—	7.5	—	7.5	—	7.5	—	7.5	—	7.5	ns
No Contention Write														
tWC	Write Cycle Time	50	—	60	—	70	—	85	—	100	—	120	—	ns
tAW	Address Valid to End of Write	45	—	50	—	60	—	75	—	90	—	110	—	ns
tCW	$\overline{CS}$ to End of Write	45	—	50	—	60	—	75	—	90	—	110	—	ns
tAS	Address Set-Up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tCDS	$\overline{CS}$ to Data Strobe	15	—	15	—	15	—	15	—	15	—	15	—	ns
tDS	Data Strobe Width	25	—	30	—	35	—	50	—	60	—	70	—	ns
tWR	Write Recovery Time	3	—	5	—	5	—	5	—	5	—	5	—	ns
tDW	Data Valid to End of Write	22	—	25	—	30	—	45	—	50	—	55	—	ns
tDH	Data Hold from End of Write	5	—	5	—	5	—	10	—	10	—	10	—	ns
Contention Read														
tCB	$\overline{CS}$ to BUSY	—	12	—	12	—	15	—	20	—	20	—	20	ns
tBD	Busy Negate to Data Valid	—	50	—	60	—	70	—	85	—	100	—	120	ns
Contention Write														
tCB	$\overline{CS}$ to BUSY	—	12	—	2	—	15	—	20	—	20	—	20	ns
tBDS	Busy Negate to Data Strobe	7	—	7	—	10	—	15	—	15	—	15	—	ns
Slave Timing														
tLR	$\overline{CS}$ to L/R Output	—	11	—	11	—	15	—	20	—	20	—	20	ns
tSEL	$\overline{CS}$ to Select Output	—	14	—	14	—	15	—	20	—	20	—	20	ns
tAPS	Arbitration Priority Set-up Time	5	—	5	—	5	—	5	—	5	—	5	—	ns

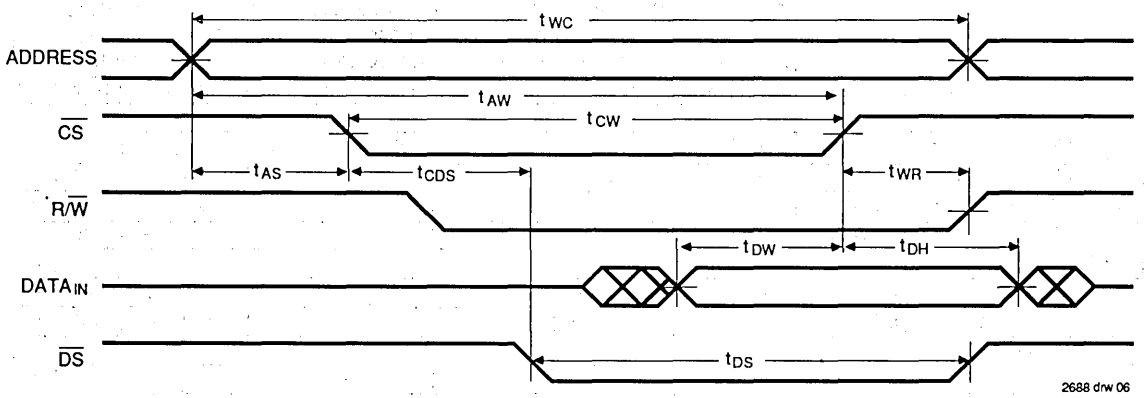
NOTE:
1. This parameter guaranteed by design but not tested.

8

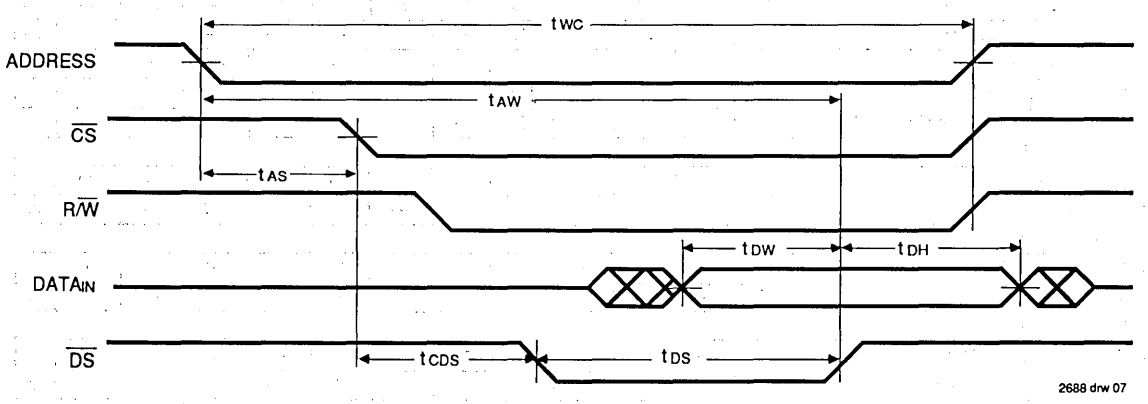
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF WRITE CYCLE (CS CONTROLLED)



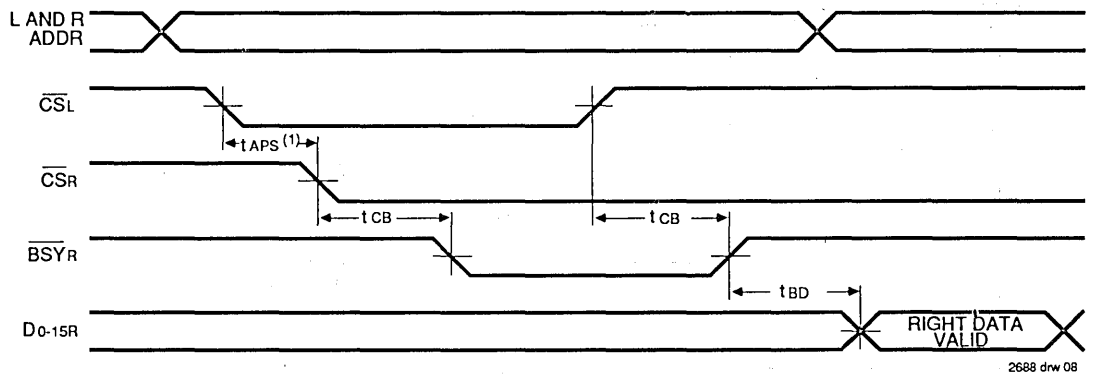
TIMING WAVEFORM OF WRITE CYCLE (DS CONTROLLED)



NOTES:
1. R/W = VIH.
2. Transition is measured +200mV from steady state with 5pF load (including scope and jig. This parameter guaranteed by design, but not tested.

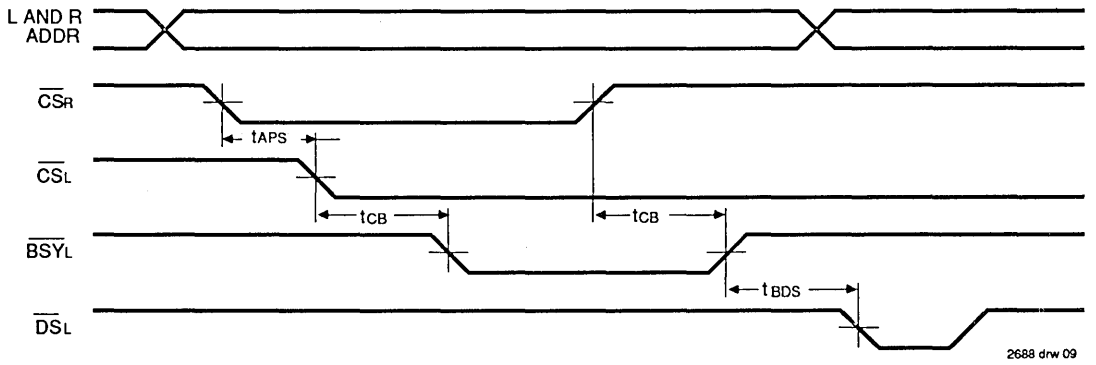
TIMING WAVEFORM OF CONTENTION READ, ($\overline{CS}$ ARBITRATION)

$\overline{CS}_L$ VALID FIRST:

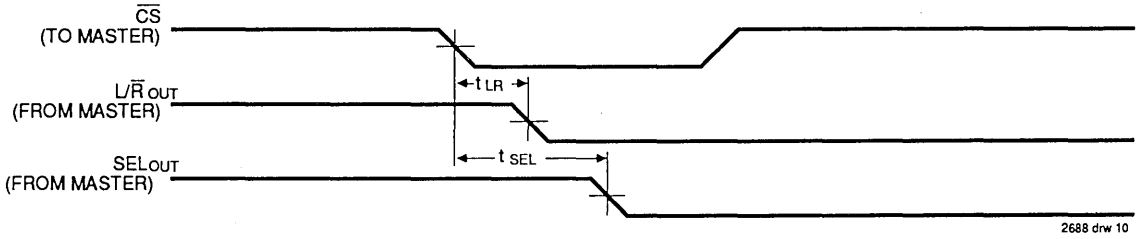


TIMING WAVEFORM OF CONTENTION WRITE, ($\overline{CS}$ ARBITRATION)

$\overline{CS}_R$ VALID FIRST:

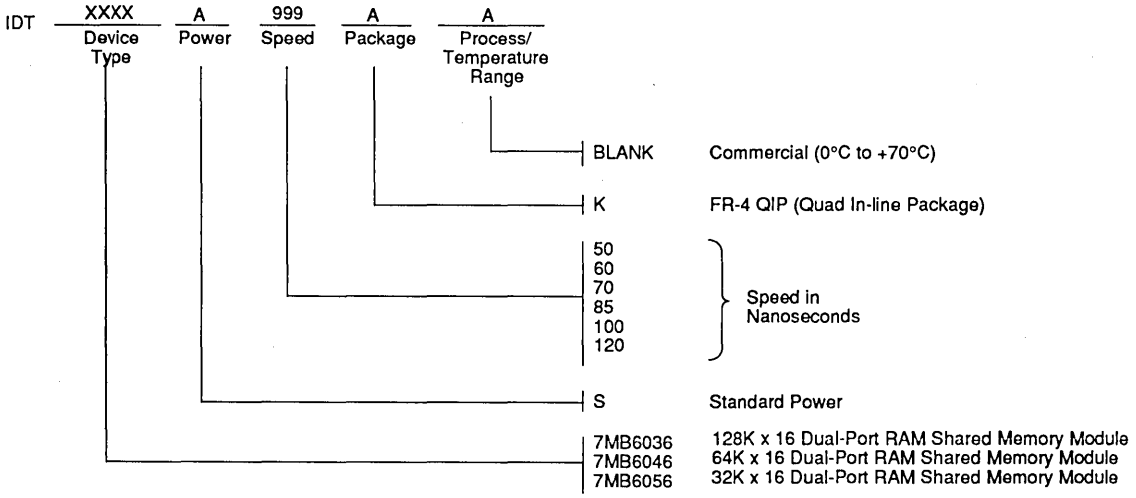


TIMING WAVEFORM OF SLAVE(2)



NOTES:
1. t_{APS} is only necessary to guarantee left side access. Within this set-up time, one side or the other will gain access, but neither will have priority.
2. $\overline{CS}$ inputs are ignored when configured as a Slave, allowing the Master to control port selection with L/R_OUT and SEL_OUT signals.

ORDERING INFORMATION



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Integrated Device Technology, Inc.

64K x 16
32K x 16
CMOS DUAL-PORT
STATIC RAM MODULE

PRELIMINARY
IDT7MB1006
IDT7MB1008

FEATURES

- High density 1 megabit/512K CMOS Dual-Port static RAM module
- Fast access times
  - commercial: 40, 45, 55, 65, 80 ns
  - military: 45, 55, 65, 80, 100 ns
- Fully asynchronous read/write operation from either port
- Easy to expand data bus width to 32 bits or more using the master/slave function
- Separate upper and lower byte control
- On-chip port arbitration logic
- $\overline{INT}$ flag for port-to-port communication
- Full on-chip hardware support of semaphore signaling between ports
- Surface mounted PQFP (plastic quad flatpack) components allow a through-hole module to fit into a 132-pin FR-4 QIP (Quad In-line Package)
- Single 5V (±10%) power supply
- Input/outputs directly TTL compatible

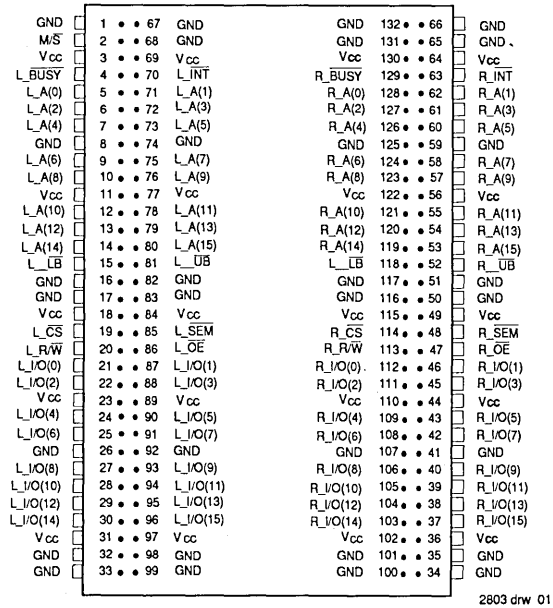
DESCRIPTION:

The IDT7MB1006/IDT7M1008 is a 64K x 16/32K x 16 high-speed CMOS dual-port static RAM module constructed on a multilayer epoxy laminate (FR-4) substrate using eight IDT7025 (8K x 16) dual-port RAMs or depopulated with four IDT7025 dual-port RAMs. The IDT7MB1006/1008 module is designed to be used as stand-alone dual-port RAM or as a combination master/slave dual-port RAM for 32-bit or more word width systems. Using the IDT master/slave approach in such system applications results in full-speed, errorj-free operation without the need for additional discrete logic.

This module provides two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory. System performance is enhanced by facilitating port-to-port communication via additional control signals $\overline{SEM}$ and $\overline{INT}$.

The IDT7MB1006/1008 module is packaged on a FR-4 132-pin QIP (Quad In-line Package). Maximum access times as fast as 40ns are available over the commercial temperature range.

PIN CONFIGURATION (1)



2803 drw 01

PIN NAMES

A_0 - A_{15}	Address Lines
I/O_0 - I/O_7	Data Inputs/Outputs
R/$\overline{W}$	Read/Write Selects
$\overline{CS}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{BUSY}$	$\overline{BUSY}$ Flag
$\overline{INT}$	Interrupt Line
$\overline{SEM}$	Semaphore Control
$\overline{UB}$	Upper Byte Select
$\overline{LB}$	Lower Byte Select
M/$\overline{S}$	Master/Slave Control
Vcc	Power Supply
GND	Ground

2803 tbl 01

NOTE:
1. Dimensions for these modules are currently not available, please consult the factory.

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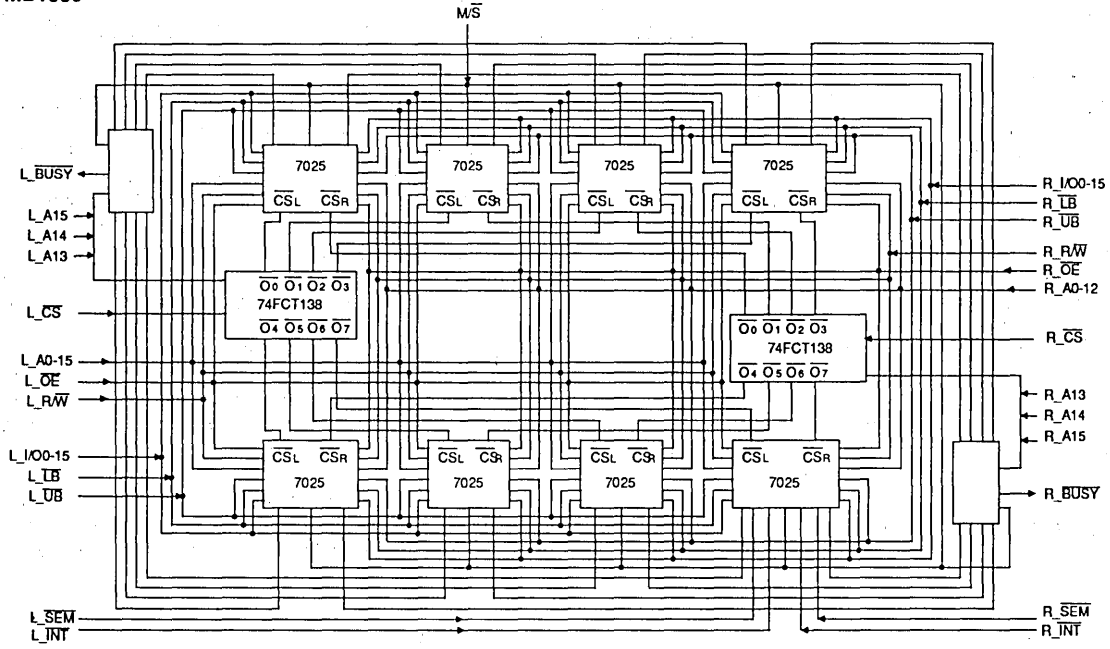
8

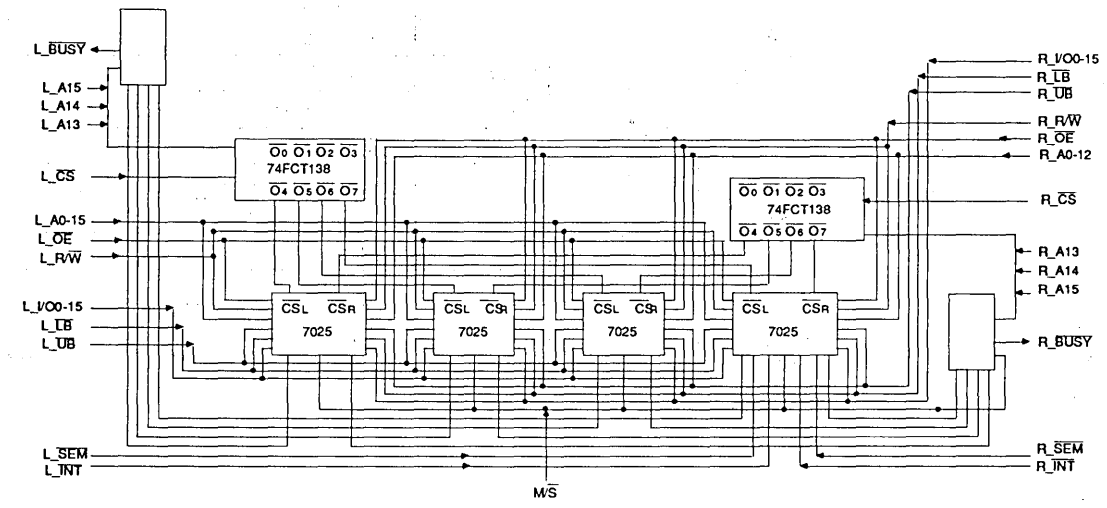
FUNCTIONAL BLOCK DIAGRAM

7MB1006



2803 drw 02

7MB1008



2803 drw 03

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to ± 7.0	-0.5 to ± 7.0	V
TA	Operating Temperature	0 to +70	-55 to + 125	°C
TBIAS	Temperature Under Bias	-55 to + 125	-65 to + 135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

2803 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE(2) (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Test Conditions	Max.	Unit
CIN1	Input Capacitance ($\overline{CS}$, $\overline{BUSY}$)	VIN = 0V	5	pF
CIN1	Input Capacitance (SEM, $\overline{INT}$)	VIN = 0V	15	pF
CIN2	Input Capacitance (Data, Address, All Other Controls)	VIN = 0V	40	pF
COUT	Output Capacitance (Data)	VOUT = 0V	40	pF

2803 tbl 05

NOTE:
1. This parameter is guaranteed by design but not tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to + 70°C	OV	5.0V± 10%

2803 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	-	6.0	V
VIL	Input Low Voltage	-0.5(1)	-	0.8	V

2803 tbl 04

NOTE:
1. VIL (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS

(Vcc=5.0V ± 10%, TA = 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7MB1006 Min.	IDT7MB1006 Max.	IDT7MB1008 Min.	IDT7MB1008 Max.	Unit
ICC2	Dynamic Operating Current (Both Ports Active)	Vcc = Max., $\overline{CS}$ ≥ VIL, SEM = Don't Care Outputs Open, f = fMAX	—	900	—	620	mA
ISB	Standby Supply Current	Vcc = Max., L_$\overline{CS}$ and R_$\overline{CS}$ ≥ VIH, Outputs Open, f = fMAX	—	580	—	300	mA
ISB1	Standby Supply Current (One Port Active)	Vcc = Max., L_$\overline{CS}$ or R_$\overline{CS}$ ≥ VIH Outputs Open, f = fMAX	—	760	—	480	mA
ISB2	Full Standby Supply Current	L_$\overline{CS}$ and R_$\overline{CS}$ ≥ Vcc - 0.2V VIN > Vcc - 0.2V or < 0.2V L_$\overline{SEM}$ and R_$\overline{SEM}$ ≥ Vcc - 0.2V	—	125	—	65	mA

2803 tbl 06

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DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7MB1006 Min.	IDT7MB1006 Max.	IDT7MB1008 Min.	IDT7MB1008 Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address & Control)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	80	—	40	mA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	20	—	20	mA
$\|I_{LO}\|$	Output Leakage (Data)	V_{CC} = Max. $\overline{CS} \geq V_{IH}$, V_{OUT} = GND to V_{CC}	—	20	—	20	mA
V_{OL}	Output Low Voltage	V_{CC} = Min. I_{OL} = 4mA	—	0.4	—	0.4	mA
V_{OH}	Output High Voltage	V_{CC} = Min. I_{OH} = -4mA	2.4	—	2.4	—	mA

2803 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2803 tbl 08

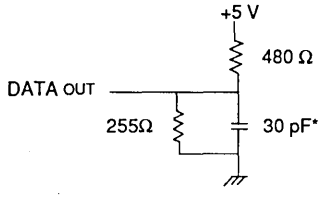

Figure 1. Output Load

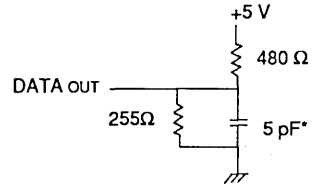

Figure 2. Output Load
(for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{WHZ}, t_{OW})

*Including scope and jig.

2803 drw 04

AC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V ± 10%, TA = 0°C to +70°C)

Symbol	Parameter	IDT7MB1006S40 IDT7MB1008S40		IDT7MB1006S45 IDT7MB1008S45		IDT7MB1006S55 IDT7MB1008S55		DT7MB1006S65 DT7MB1008S65		IDT7MB1006S80 IDT7MB1008S80		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
tRC	Read Cycle Time	40	—	45	—	55	—	65	—	80	—	ns
tAA	Address Access Time	—	40	—	45	—	55	—	65	—	80	ns
tACS(2)	Chip Select Access Time	—	40	—	45	—	55	—	65	—	80	ns
tOE	Output Enable Access Time	—	20	—	25	—	30	—	35	—	40	ns
tOH	Output Hold From Address Change	3	—	3	—	3	—	3	—	3	—	ns
tCLZ(1)	Chip Select to Output in Low Z	3	—	5	—	5	—	5	—	5	—	ns
tCHZ(1)	Chip Deselect to Output in High Z	—	18	—	20	—	25	—	30	—	35	ns
tOLZ(1)	Output Enable to Output in Low Z	3	—	3	—	5	—	5	—	5	—	ns
tOHZ(1)	Output Disable to Output in High Z	—	18	—	20	—	25	—	30	—	35	ns
tPU(1)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
tPD(1)	Chip Disable to Power Down Time	—	50	—	50	—	50	—	50	—	50	ns
tSOP	$\overline{SEM}$ Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	20	—	20	—	20	—	20	—	20	—	ns
Write Cycle												
tWC	Write Cycle Time	40	—	45	—	55	—	65	—	80	—	ns
tCW(2)	Chip Select to End of Write	35	—	40	—	45	—	50	—	55	—	ns
tAW	Address Valid to End of Write	35	—	40	—	45	—	50	—	55	—	ns
tAS1	Address Set-up to Write Pulse Time	5	—	5	—	5	—	5	—	5	—	ns
tAS2	Address Set-up to $\overline{CS}$ Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	30	—	35	—	40	—	45	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	25	—	27	—	30	—	40	—	45	—	ns
tDH(1)	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tOHZ(1)	Output Disable to Output in High Z	—	18	—	20	—	25	—	30	—	35	ns
tWHZ(1)	Write Disable to Output in High Z	—	18	—	20	—	25	—	30	—	35	ns
tOW	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	15	—	15	—	15	—	15	—	15	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	15	—	15	—	15	—	15	—	15	—	ns

NOTES:

1. This parameter is guaranteed by design but not tested.
2. To access RAM, $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.

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2803 tbl 09

AC ELECTRICAL CHARACTERISTICS

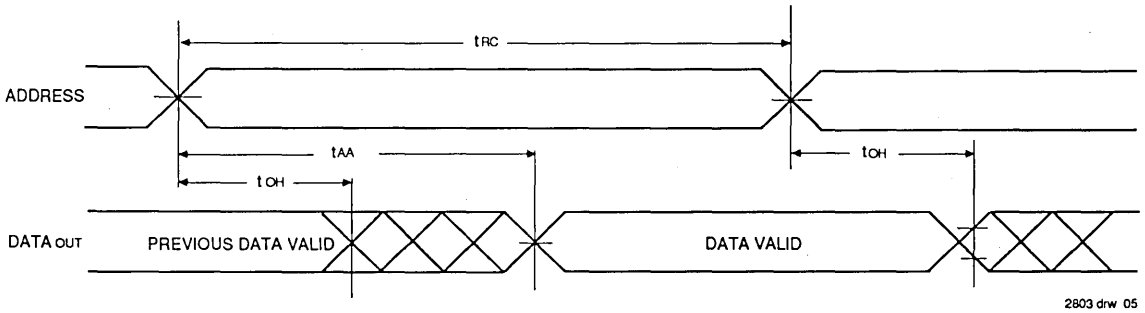
(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameters	IDT7MB1006S40 IDT7MB1008S40		IDT7MB1006S45 IDT7MB1008S45		IDT7MB1006S55 IDT7MB1008S55		IDT7MB1006S65 IDT7MB1008S65		IDT7MB1006S80 IDT7MB1008S80		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{BUSY}$ Cycle - MASTER MODE[3]												
t_{BAA}	$\overline{BUSY}$ Access Time from Address	—	40	—	45	—	45	—	55	—	55	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address	—	30	—	35	—	40	—	45	—	45	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Select	—	35	—	40	—	40	—	50	—	55	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Select	—	30	—	35	—	35	—	45	—	45	ns
t_{WDD}[5]	Write Pulse to Data Delay	—	60	—	70	—	80	—	85	—	95	ns
t_{DDD}	Write Data Valid to Read Data Delay	—	40	—	45	—	55	—	70	—	80	ns
t_{APS}[6]	Arbitration Priority Set-up Time	5	—	5	—	5	—	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Time	—	Note 9	—	Note 9	—	Note 9	—	Note 9	—	Note 9	ns
$\overline{BUSY}$ Cycle - Slave Mode[4]												
t_{WB}[7]	Write to $\overline{BUSY}$ Input	0	—	0	—	0	—	0	—	0	—	ns
t_{WH}[8]	Write Hold After $\overline{BUSY}$	25	—	30	—	30	—	30	—	30	—	ns
t_{WDD}[5]	Write Pulse to Data Delay	—	60	—	70	—	80	—	85	—	100	ns
t_{DDD}[5]	Write Data Valid to Read Data Valid	—	45	—	50	—	60	—	70	—	85	ns
Interrupt Timing												
t_{AS}	Address Set-up Time	5	—	5	—	5	—	5	—	5	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	30	—	35	—	40	—	45	—	55	ns
t_{INR}	Interrupt Reset Time	—	30	—	35	—	40	—	45	—	55	ns

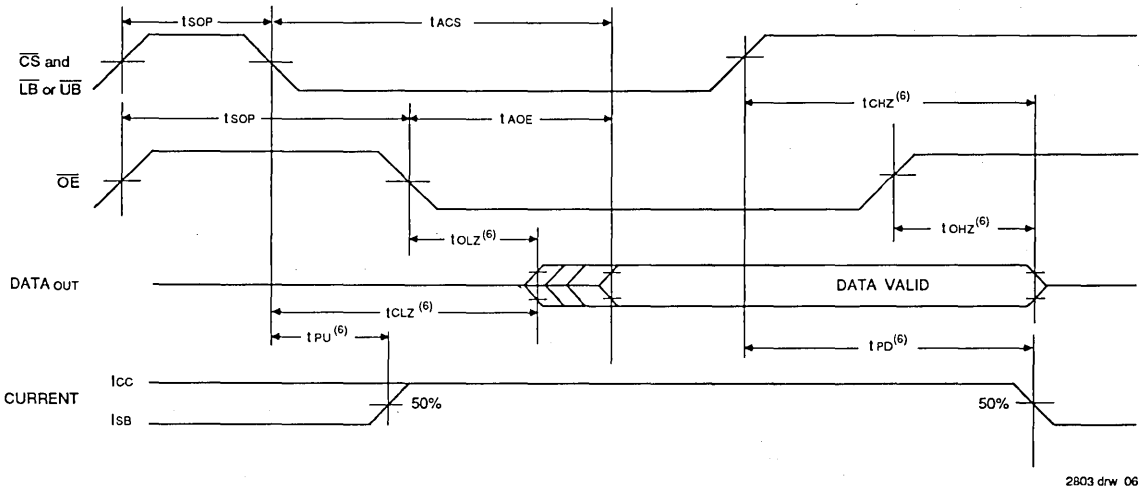
NOTES:
1. This parameter is guaranteed by design but not tested.
2. To access RAM, $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
3. When the module is being used in the Master Mode ($M/\overline{S} \geq V_{IH}$).
4. When the module is being used in the Slave Mode ($M/\overline{S} \leq V_{IL}$).
5. Port-to-Port delay through the RAM cells from the writing port to the reading port.
6. To ensure that the earlier of the two ports wins.
7. To ensure that the write cycle is inhibited during contention.
8. To ensure that a write cycle is completed after contention.
9. t_{BDD} is a calculated parameter and is the greater of 0, t_{WDD} - t_{WP} (actual), or t_{DDD} - t_{WP} (actual).

2803 tbl 11

TIMING WAVEFORM OF READ CYCLE NO. 1 (EITHER SIDE)(1,2,4)



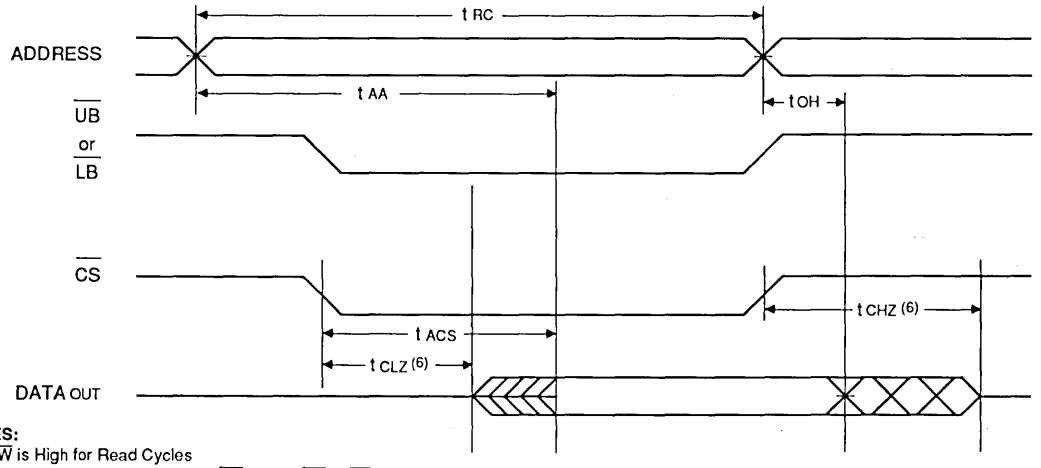
TIMING WAVEFORM OF READ CYCLE NO. 2 (EITHER SIDE)(1,3,5)



NOTES:
1. R/W is High for Read Cycles
2. Device is continuously enabled. CS = Low, UB or LB = Low. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with CS transition low.
4. OE = Low.
5. To access RAM, CS = Low, UB or LB = Low, SEM = H. To access semaphore, CS = H and SEM = Low.
6. This parameter is guaranteed by design but not tested.

8

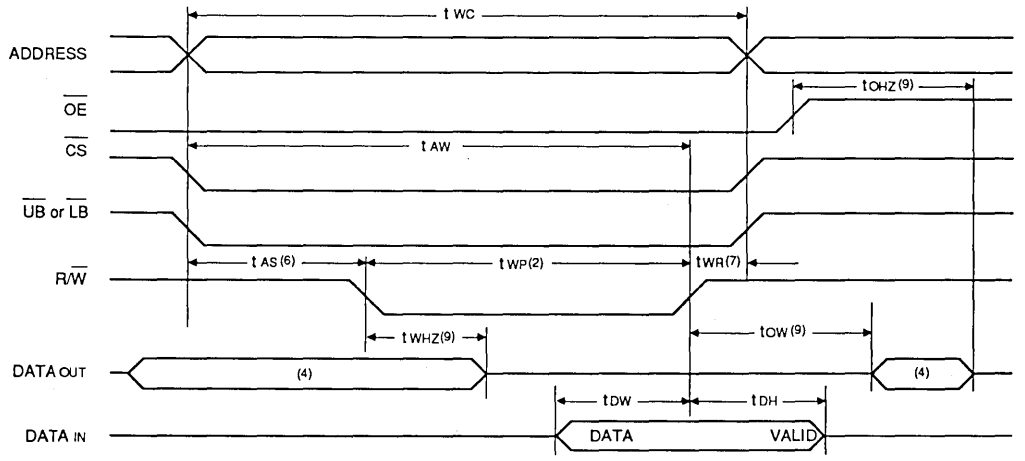
TIMING WAVEFORM OF READ CYCLE NO. 3 ($\overline{UB}$ OR $\overline{LB}$ CONTROLLED TIMING)(1,3,4,5)



NOTES:
1. R/$\overline{W}$ is High for Read Cycles
2. Device is continuously enabled. $\overline{CS}$ = Low. $\overline{UB}$ or $\overline{LB}$ = Low. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = Low.
5. To access RAM, $\overline{CS}$ = Low $\overline{UB}$ or $\overline{LB}$ = Low, $\overline{SEM}$ = H. To access semaphore, $\overline{CS}$ = H and $\overline{SEM}$ = Low.
6. This parameter is guaranteed by design but not tested.

2803 drw 07

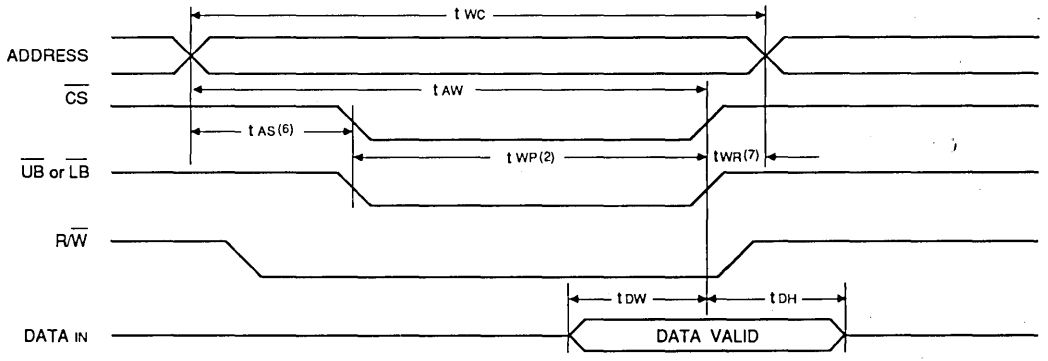
TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING)(1,3,5,8)



2803 drw 08

NOTES:
1. R/$\overline{W}$ is High for Read Cycles
2. Device is continuously enabled. $\overline{CS}$ = Low. $\overline{UB}$ or $\overline{LB}$ = Low. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = Low.
5. To access RAM, $\overline{CS}$ = Low, $\overline{UB}$ or $\overline{LB}$ = Low, $\overline{SEM}$ = H. To access semaphore, $\overline{CS}$ = H and $\overline{SEM}$ = Low.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is Low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is High during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse width be as short as the specified t_{WP}.
9. This parameter is guaranteed by design but not tested.

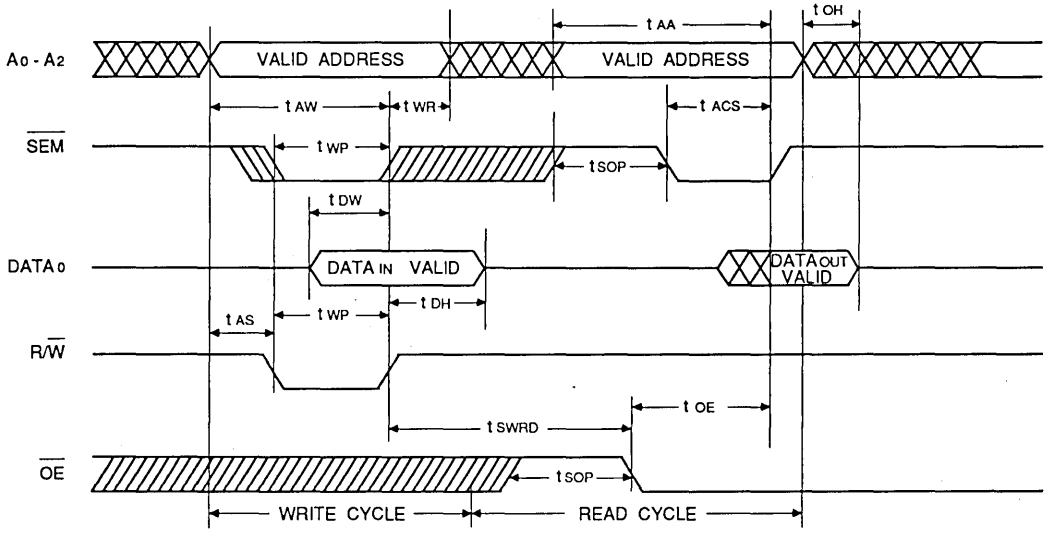
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$, $\overline{UB}$, $\overline{LB}$ CONTROLLED TIMING)(1,3,5,8)



2803 drw 09

NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a Low $\overline{UB}$ or $\overline{LB}$ and a Low $\overline{CS}$ and a Low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CS}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
9. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING (EITHER SIDE)(1)

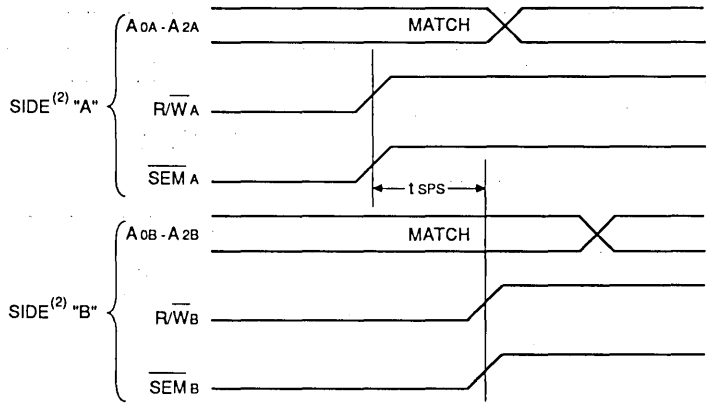


2803 drw 10

NOTE:
1. $\overline{CS}$ = High for the duration of the above timing (both write and read cycle).

8

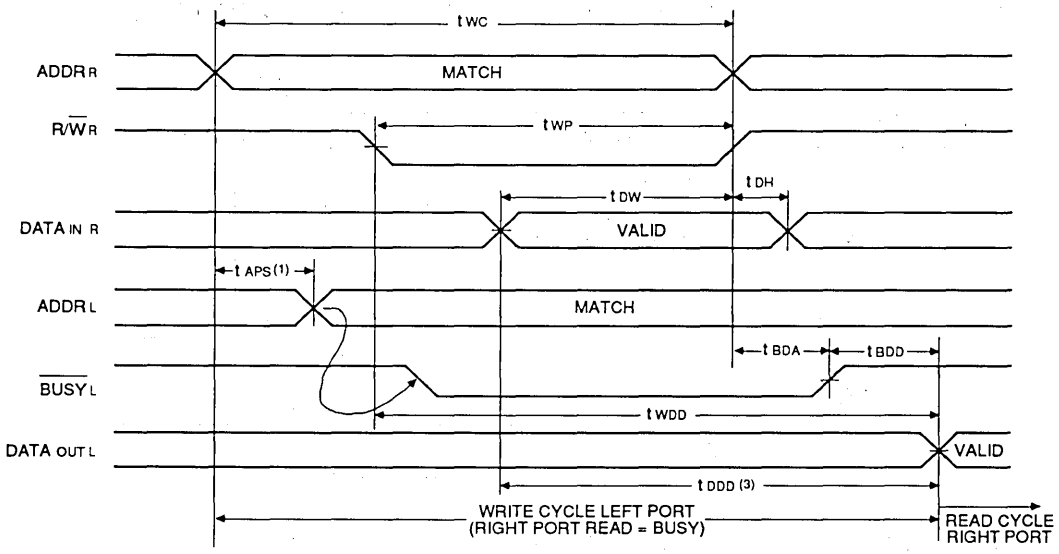
TIMING WAVEFORM OF SEMAPHORE CONTENTION(1,3,4)



2803 drw 11

NOTES:
1. $D_{0R} = D_{0L}$ = Low, $L\_\overline{CE} = R\_\overline{CE}$ = High. Semaphore Flag is released form both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from $R/\overline{W}_A$ or $\overline{SEM}_A$ going High to $R/\overline{W}_B$ or $\overline{SEM}_B$ going High.
4. If t_{SPS} is violated, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

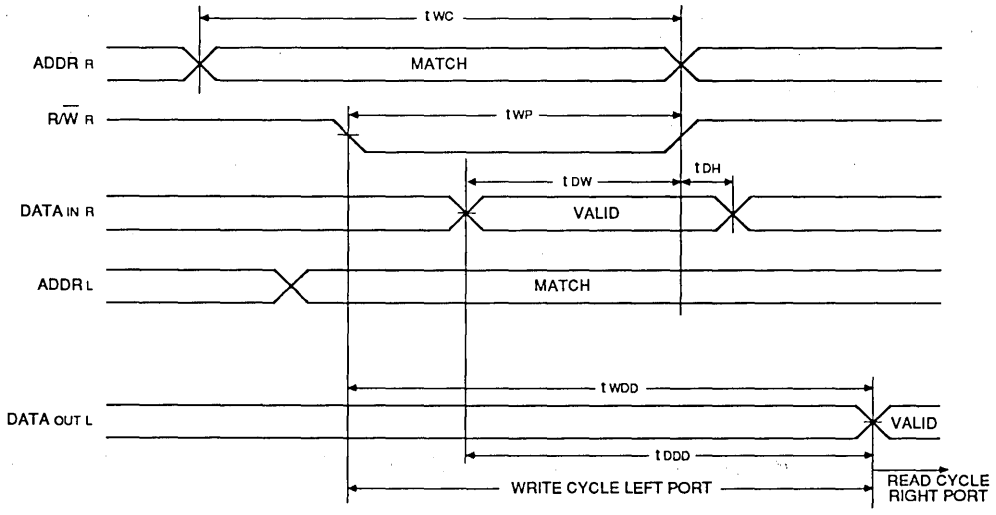
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$ ($M/\overline{S} \geq V_{IH}$)(2)



2803 drw 12

NOTES:
1. To ensure that the earlier of the two ports wins.
2. $L\_\overline{CE} = R\_\overline{CE}$ = Low
3. $\overline{OE}$ = Low for the reading port.

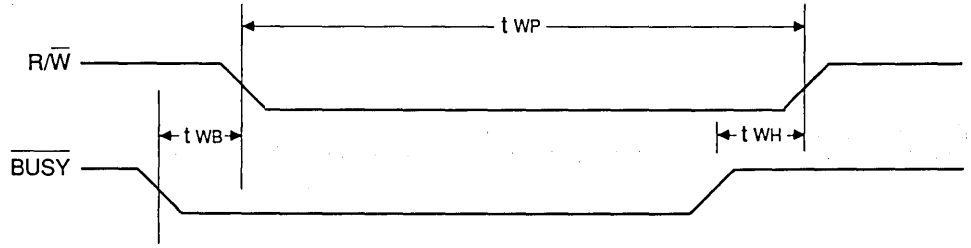
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY ($M/\overline{S} \leq V_{IL}$)(1,2)



2803 drw 13

NOTES:
1. $\overline{BUSY}$ input equals High for the writing port.
2. L_$\overline{CS}$ = R_$\overline{CS}$ = Low

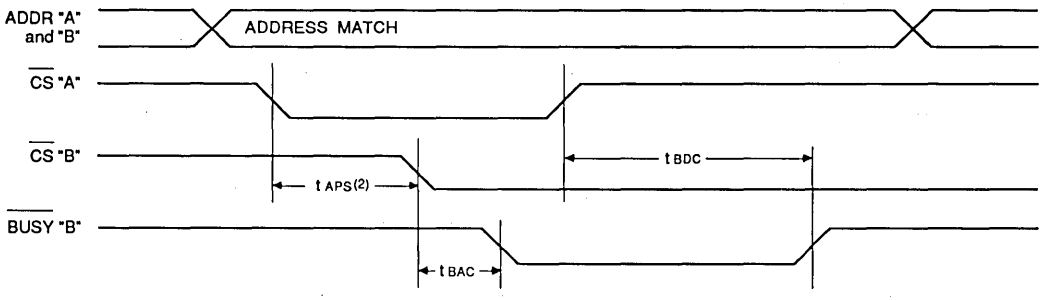
TIMING WAVEFORM OF WRITE WITH BUSY INPUT ($M/\overline{S} \leq V_{IL}$)



2803 drw 13a

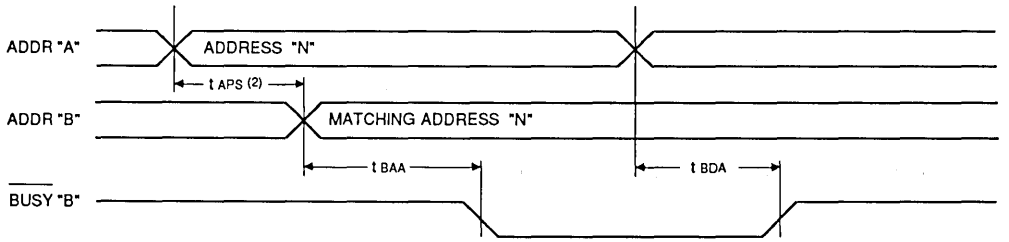
8

WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CS}$ TIMING(1)



2803 drw 14

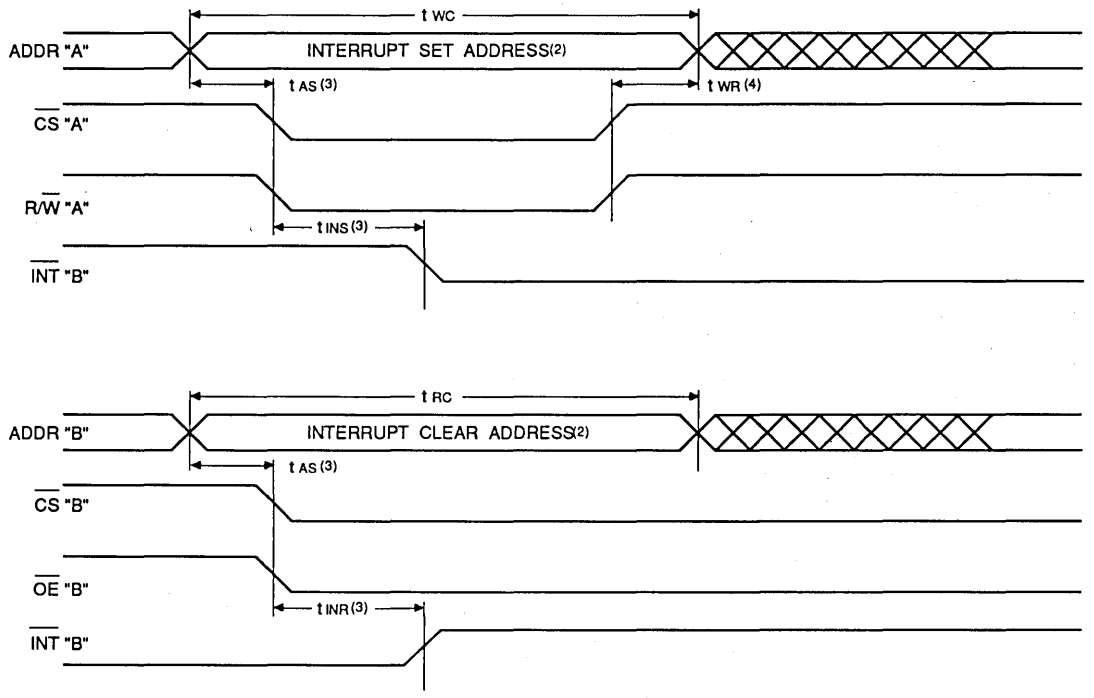
WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING(1)



2803 drw 15

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If t_{APS} is violated, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

WAVEFORM OF INTERRUPT TIMING[1]



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NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See InterruptTruth Table.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable is de-asserted first.

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TRUTH TABLES

TABLE I: NON-CONTENTION READ/WRITE CONTROL[1,2,3]

Inputs[1]						Outputs		
$\overline{CS}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8 - I/O15	I/O0 - I/O7	Mode
F	X	X	X	X	H	Hi-Z	Hi-Z	Deselected: Power Down
X	X	X	H	H	H	Hi-Z	Hi-Z	Both Bytes Deselected
T	L	X	L	H	H	DATAIN	Hi-Z	Write to Upper Byte Only
T	L	X	H	L	H	Hi-Z	DATAIN	Write to Lower Byte Only
T	L	X	L	L	H	DATAIN	DATAIN	Write to Both Bytes
T	H	L	L	H	H	DATAOUT	Hi-Z	Read Upper Byte Only
T	H	L	H	L	H	Hi-Z	DATAOUT	Read Lower Byte Only
T	H	L	L	L	H	DATAOUT	DATAOUT	Read Both Bytes
X	X	H	X	X	X	Hi-Z	Hi-Z	Outputs Disabled

NOTES: 2803 tbl 12
1. AOL — A12 ≠ AOR — A12R
2. $\overline{CS}$ = True represents L_$\overline{CS}$ = R_$\overline{CS}$ = Low.
3. $\overline{CS}$ = False represents L_$\overline{CS}$ = R_$\overline{CS}$ = High.

TABLE II: SEMAPHORE READ/WRITE CONTROL

Inputs						Outputs		
$\overline{CS}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8 - I/O15	I/O0 - I/O7	Mode
F	H	L	X	X	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
X	H	L	H	H	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
F	↓	X	X	X	L	DATAIN	DATAIN	Write DIN0 into Semaphore Flag
X	↓	X	H	H	L	DATAIN	DATAIN	Write DIN0 into Semaphore Flag
T	X	X	L	X	L	—	—	Not Allowed
T	X	X	X	L	L	—	—	Not Allowed

NOTES: 2803 tbl 13
1. AOL — A12 ≠ AOR — A12R
2. $\overline{CS}$ = True represents L_$\overline{CS}$ = R_$\overline{CS}$ = Low.
3. $\overline{CS}$ = False represents L_$\overline{CS}$ = R_$\overline{CS}$ = High.

TABLE III: INTERRUPT FLAG[1]

Left Port					Right Port					
R/$\overline{W}$	$\overline{CS}$	$\overline{OE}$	A0 - A15	$\overline{INT}$L	R/$\overline{W}$	$\overline{CS}$	$\overline{OE}$	A0 - A15R	$\overline{INT}$	Function
L	L	X	1FFF	X	X	X	X	X	L[2]	Set Right $\overline{INT}$R Flag
X	X	X	X	X	X	L	L	1FFF	H[3]	Reset Right $\overline{INT}$R Flag
X	X	X	X	L[2]	L	L	X	1FFE	X	Set Left $\overline{INT}$L Flag
X	L	L	1FFE	H[3]	X	X	X	X	X	Reset Left $\overline{INT}$L Flag

NOTES: 2803 tbl 14
1. Assumes L_$\overline{BUSY}$ = R_$\overline{BUSY}$ = High
2. If L_$\overline{BUSY}$ = Low then no change.
3. If R_$\overline{BUSY}$ = Low then no change.
4. At the interrupt addresses 1FFE and 1FFF, address bits 13 - 15 are zero.

TRUTH TABLES

TABLE IV: ADDRESS BUSY ARBITRATION

Inputs			Outputs		
L_$\overline{CS}$	R_$\overline{CS}$	A_{0L} - A_{15L} A_{0R} - A_{15R}	L_$\overline{BUSY}$[1]	R_$\overline{BUSY}$[1]	Function
X	X	No Match	H	H	Normal
H	X	Match	H	H	Normal
X	H	Match	H	H	Normal
L	L	Match	Note 2	Note 2	Write Inhibit[3]

NOTES: 2803 tbl 15

1. Pins L_$\overline{BUSY}$ and R_$\overline{BUSY}$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. X_$\overline{BUSY}$ outputs on the IDT7MB10016/1008 are push pull, not open drain outputs. On slaves the X_$\overline{BUSY}$ input internally inhibits writes.
2. L if the inputs to the opposite port were stable prior to the address and enable inputs of this port. H if the inputs to the opposite port became stable after the address and enable inputs of this port. If the primacy of stable inputs cannot be resolved, either L_$\overline{BUSY}$ = Low or R_$\overline{BUSY}$ = Low will result. L_$\overline{BUSY}$ and R_$\overline{BUSY}$ outputs cannot be low simultaneously.
3. Writes to the left port are internally ignored when L_$\overline{BUSY}$ outputs are driving low regardless of actual logic level the pin. Writes to the right port are internally ignored when R_$\overline{BUSY}$ outputs are driving low regardless of actual logic level on the pin.

TABLE V: EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE[2]

Function	D0 - D15 Left	D0 - D15 Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains sempahore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to SEmaphore	0	1	Left port obtains sempahore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has sempahore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

NOTE: 2803 tbl 16

1. This table denotes a sequence of events for only one of the eight semaphores available on the IDT7MB1006/1008

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FUNCTIONAL DESCRIPTIONAL

The IDT7MB1006/1008 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7MB1006/1008 has an automatic power down feature controlled by $\overline{CS}$. The $\overline{CS}$ controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{CS}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. NON-CONTENTION READ/WRITE conditions are illustrated in the Truth Tables.

INTERRUPTS

The interrupt flag ($\overline{INT}$) permits communictaion between ports or systems. If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is set when the right port writes to memory location 1FFE (HEX). The left port clears the interrupt by reading address location 1FFE. Likewise, the right port interrupt flag ($\overline{INT}_R$) is set when the left port writes to memory location 1FFF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 1FFF. The message (16 bits) at 1FFE or 1FFF is user-defined. If the interrupt function is not used, address locations 1FFE and 1FFF are not used as mail boxes, but as part of the random access memory. Refer to Table III for the interrupt operation. Interrupts in the least significant IDT7025 of the module are used. To address them, the most significant address bits (A_{13-15}) must be 0.

BUSY LOGIC

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CS}$, on-chip control logic arbitrates between $\overline{CS}_L$ and $\overline{CS}_R$ for access; or (2) if the $\overline{CS}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table II). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION

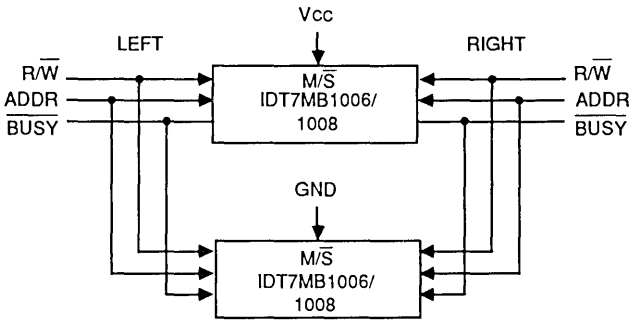
Expanding the data bus width to thirtytwo-or-more-bits in a dual-port RAM system implies that several modules will be active at the same time. If each module includes a hardware arbitrator, and the addresses for each module arrive at the same time, it is possible that one will activate its L_$\overline{BUSY}$ while another activates its R_$\overline{BUSY}$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid this "Busy Lock-out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RMs in width, the writing of the SLAVE modules must be delayed, until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE module may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one module is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

32-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



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SEMAPHORES

The IDT7MB1006/1008 is an extremely fast dual-port 64K/32K x 16 CMOS static RAM module with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the dual-port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the dual-port RAM or any shared resource.

The dual-port RAM module features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS static RAM modules and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultanious READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the dual-port RAM. These devices have an automatic power-down feature controlled by $\overline{CS}$ the dual-port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CS}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table where $\overline{CS}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT7MB1006/1008 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT7MB1006/1008's hardware semaphores which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT7MB1006/1008 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW SEMPAHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the dual-port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that a shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor had set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side had relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT7MB1006/1008 in a separate memory space from the dual-port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A_0 - A_2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D_0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other (Table V). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that flag this is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go active or the output will never change.

A sequence of WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the samaphore flag will appear as a one, a fact which the processor will verify by the subsequent read. (see Table V). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right

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side attempts to write a zero to the same samaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during a subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 1. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore latch have been written to a zero in the meantime, the samaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The ciritcal case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is especially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a recource secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen. Code integrity is of the utmost importance when semaphores are used instead of slower, more restrictive hardware intensive schemes.

Initialization of the samaphores is not automatic and must be handled via the initialization program at power-up. Since any sempahore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES — SOME EXAMPLES

Perhaps the simplest application of semaphores is their application as resource markers for the IDT7MB1006/1008's dual-port RAM module. Say that a 8K x 16 RAM block was to be divided into two 4K x 16 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 4K of dual-port RAM, the processor on the left port could write and then read a zero into Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 4K. Meanwhile the right processor would attempt to perform the same function. Since this processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 4K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 4K blocks of dual-port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the dual-port RAM or other shared resources into eight parts. Semaphore can even assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interface where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices had determined which memory area was "off limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available to one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application, one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

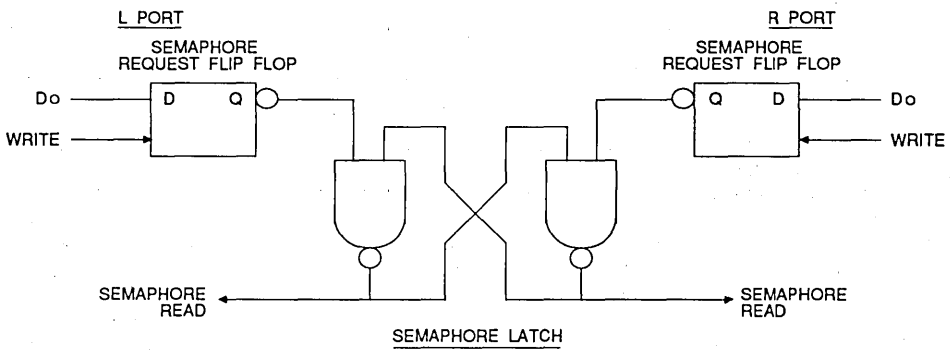

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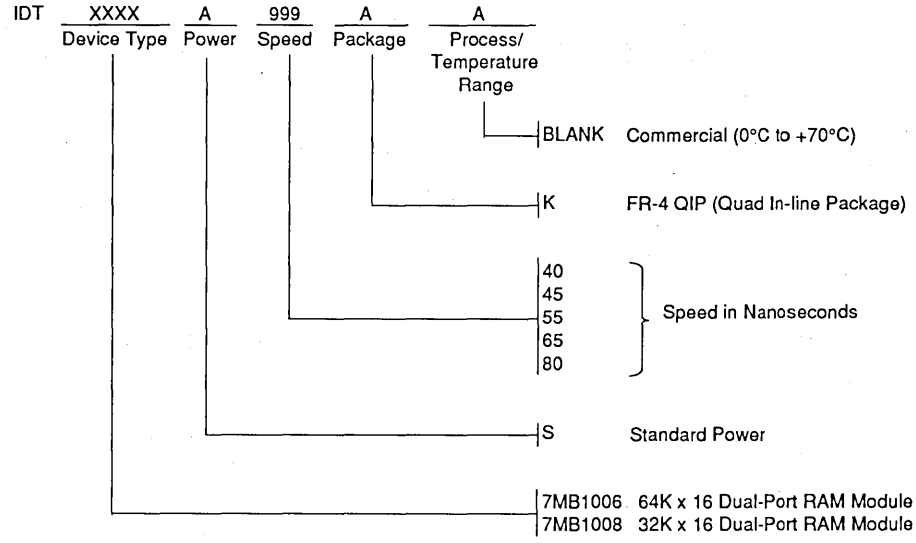
Figure 1. IDT7MB1006/1008 Semaphore Logic

ORDERING INFORMATION



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Integrated Device Technology, Inc.

128K x 18, 64K x 18 , 32K x 18 CMOS DUAL-PORT RAM

(SHARED MEMORY MODULE)

PRELIMINARY
IDT7MB6136
IDT7MB6146
IDT7MB6156

FEATURES:

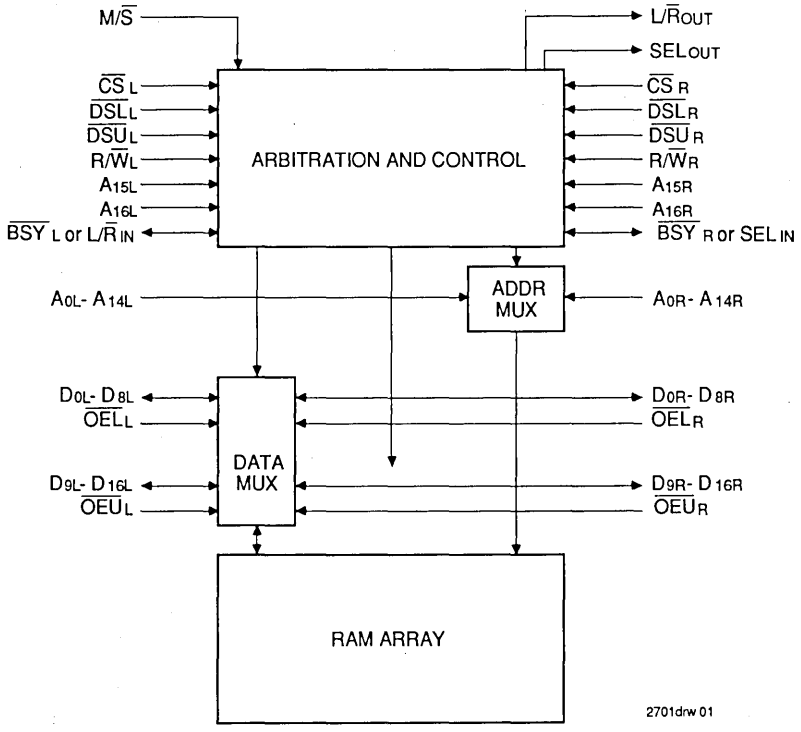
- High density 2 megabit/1 megabit/512K-bit CMOS Dual-Port static RAM (shared memory modules)
- 18-bit wide shared memory array for those applications requiring parity, tags, or extra width
- Fully asynchronous read/write operation from either port
- Port arbitration/multiplexing logic by custom FCT chip set
- Memory array comprised of industry standard static RAM components
- Versatile controls: $\overline{BUSY}$ ouput flag and separate write controls for lower and upper byte on each port
- Master/Slave control on-board for expanding word width
- Multiple GND and Vcc pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Single 5V (±10%) power supply

DESCRIPTION:

The Shared Memory Module provides two ports with separate control, address and data I/O pins that permit independent access for reads or writes to any location in the memory array. Using the on-board Master/Slave input allows these module to be used as building blocks in 32-bit or more-bit systems requiring full speed operation without additional discrete logic.

In the Master Mode, the Shared Memory Module arbitrates asynchronously between the left and right port $\overline{CS}$ inputs. The first to arrive is granted exclusive access to the entire RAM array for as long as its $\overline{CS}$ is asserted. If both ports attempt simultaneous access, the losing port will have its $\overline{BUSY}$ asserted until the winning port completes its access, at which time the second port will be granted its own exclusive access to the entire RAM array. See application note AN-74 for more details regarding proper module operating modes.

FUNCTIONAL BLOCK DIAGRAM



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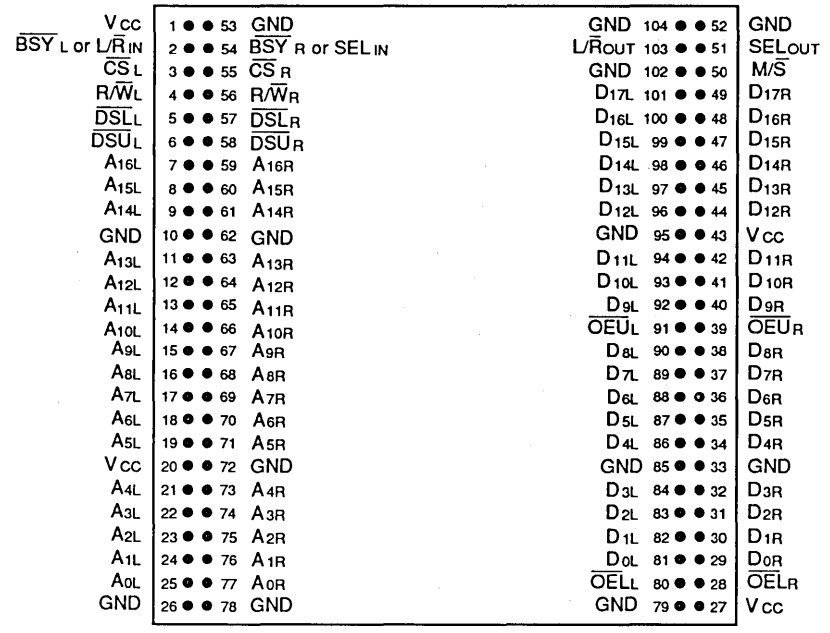
PIN CONFIGURATION[1, 2, 3]



QIP
TOP VIEW

2701 drw 02

NOTES:
1. For module dimensions, please refer to drawing M23, M24, and M25 in the packaging section.
2. Pins (8 and 60) must be grounded for proper operation of the IDT7MB6146 module (64K x 18 version). Pins 7 and 59 become A15L and A15R respectively.
3. Pins (7, 8, 59, and 60) must be grounded for proper operation of the IDT7MB6156 module (32K x 18 version).

PIN DESCRIPTIONS

Symbol	Description
VCC	Power
GND	Ground
A0L-A16L	Left Port Address
D0L-D17L	Left Port Data
A0R-A16R	Right Port Address
D0R-D17R	Right Port Data
R/$\overline{W}$	Read/Write Control
$\overline{CS}$	Chip Select
$\overline{DSL}$	Data Strobe for lower byte
$\overline{DSU}$	Data Strobe for upper byte
$\overline{OEL}$	Output Enable for lower byte
$\overline{OEU}$	Output Enable for upper byte
$\overline{BSY}$L or L/$\overline{R}$IN	Left Busy Output for Stand Alone or Master Mode. Left or Right Port Select Input for Slave Mode
$\overline{BSY}$R or SELIN	Right Busy Output for Stand Alone or Master Mode. RAM Array Select Input for Slave Mode
L/$\overline{R}$OUT	Left or Right Port Select Output on Master to be connected to L/$\overline{R}$IN Input on one or more slaves when width expansion is required
SELOUT	RAM Array Select Output on Master to be connected to SELIN Input on one or more slaves when width expansion is required
M/$\overline{S}$	Master/Slave signal for cascading master with one or more slaves

2701 tbl 01

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2701 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}(1)	Input Low Voltage	-0.5	—	0.8	V

NOTE: 2700 tbl 03

1. V_{IL} = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2701 tbl 04

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, T_A = 0°C TO +70°C)

Symbol	Description	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{IN} = GND to V_{CC}	—	15	µA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -15mA	2.4	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 32mA	—	0.4	V
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS} \leq V_{IL}$ f = f_{MAX}, Outputs Open	—	520	mA
I_{SB}	Standby Supply Current (TTL)	V_{CC} = Max., $\overline{CS} \geq V_{IH}$ f = f_{MAX}, Outputs Open	—	170	mA

2701 tbl 05

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 & 3

2701 tbl 06

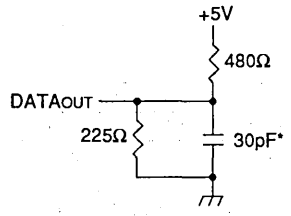


Figure 1. Output Load

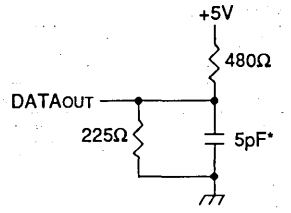


Figure 2. Output Load (for t_{OHZ} and t_{OLZ})

*Includes scope and jig

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

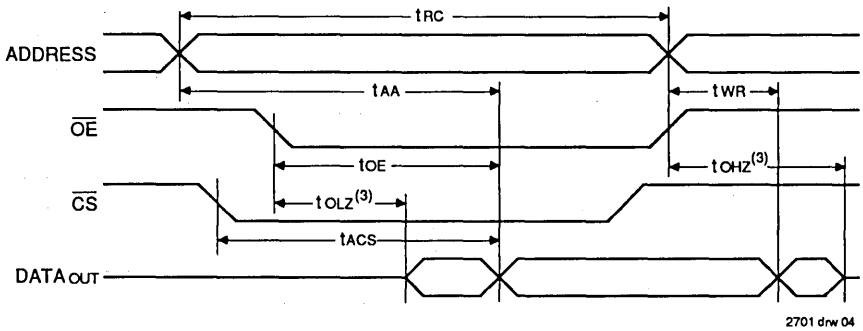
Symbol	Parameter	IDT7MB6136S40 IDT7MB6146S40 IDT7MB6156S40		IDT7MB6136S45 IDT7MB6146S45 IDT7MB6156S45		IDT7MB6136S55 IDT7MB6146S55 IDT7MB6156S55		IDT7MB6136S70 IDT7MB6146S70 IDT7MB6156S70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
No Contention Read										
t_{RC}	Read Cycle Time	40	—	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	40	—	45	—	55	—	70	ns
t_{ACS}	Chip Select Access Time	—	40	—	45	—	55	—	70	ns
t_{OE}	Output Enable to Data Valid	—	31	—	33	—	36	—	41	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{OLZ}[1]	$\overline{OE}$ to Output to Low Z	11	—	11	—	11	—	11	—	ns
t_{OHZ}[1]	$\overline{OE}$ to Output to High Z	—	9	—	9	—	9	—	9	ns
No Contention Write										
t_{WC}	Write Cycle Time	40	—	45	—	55	—	70	—	ns
t_{AW}	Address Valid to End of Write	35	—	40	—	50	—	65	—	ns
t_{CW}	$\overline{CS}$ to End of Write	35	—	40	—	50	—	65	—	ns
t_{AS}	Address Set Up Time	0	—	0	—	0	—	0	—	ns
t_{CDS}	$\overline{CS}$ to Data Strobe	15	—	15	—	15	—	15	—	ns
t_{DS}	Data Strobe Width	19	—	22	—	26	—	33	—	ns
t_{WR}	Write Recovery Time	2	—	2	—	2	—	2	—	ns
t_{DW}	Data Valid to End of Write	19	—	21	—	24	—	29	—	ns
t_{DH}	Data Hold from End of Write	2	—	2	—	2	—	2	—	ns
Contention Read										
t_{CB}	$\overline{CS}$ to BUSY	—	12	—	12	—	12	—	12	ns
t_{BD}	$\overline{BUSY}$ Negate to Data Valid	—	40	—	45	—	55	—	55	ns
Contention Write										
t_{CB}	$\overline{CS}$ to BUSY	—	12	—	12	—	12	—	12	ns
t_{BDS}	$\overline{BUSY}$ Negate to Data Strobe	7	—	7	—	7	—	7	—	ns
Slave Timing										
t_{LR}	$\overline{CS}$ to $L/\overline{R}_{OUT}$	—	11	—	11	—	11	—	11	ns
t_{SEL}	$\overline{CS}$ to SEL_{OUT}	—	14	—	14	—	14	—	14	ns
t_{APS}	Arbitration Prioity Set-Up Time	5	—	5	—	5	—	5	—	ns

NOTE:

1. This parameter is guaranteed by design, but not tested.

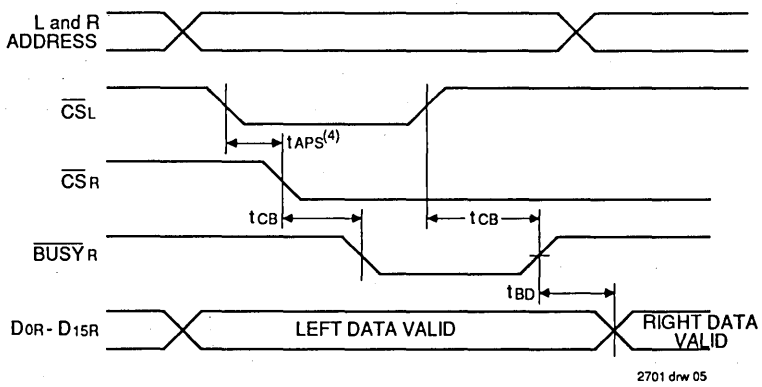
2701 tbl 07

TIMING WAVEFORM OF READ CYCLE[1]



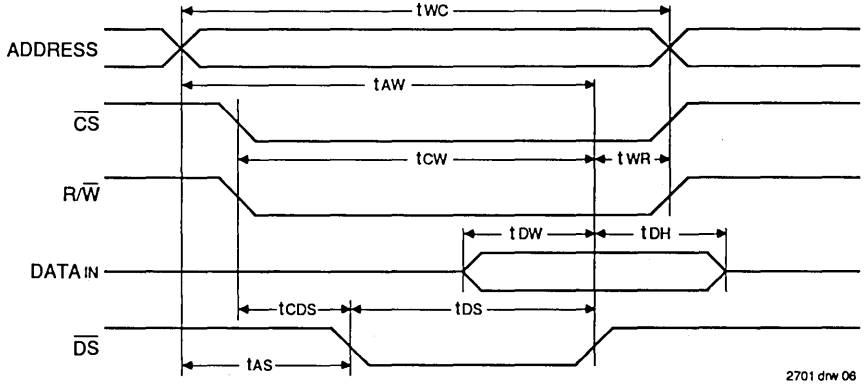
TIMING WAVEFORM OF READ CYCLE ($\overline{CS}$ ARBITRATION)

$\overline{CS}_L$ Valid First:

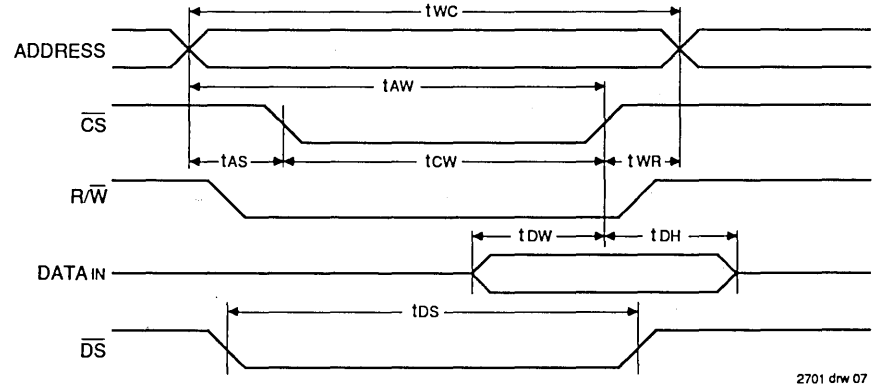


NOTES:
1. R/$\overline{W}$ = VIH for all address transitions.
2. Transitions is measured ±200mV from steady state with 5pF load (including scope and jig).
3. This parameter is garanteed by design, but not tested.
4. tAPS is only necessary to guarantee left side access (in this example). Within this set-uptime, one side or the other will gain access, but neither will have priority.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{DS}$ CONTROLLED)(1)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ CONTROLLED)(1)



NOTE:
1. $R/\overline{W}$ = V_{IH} for all address transitions.

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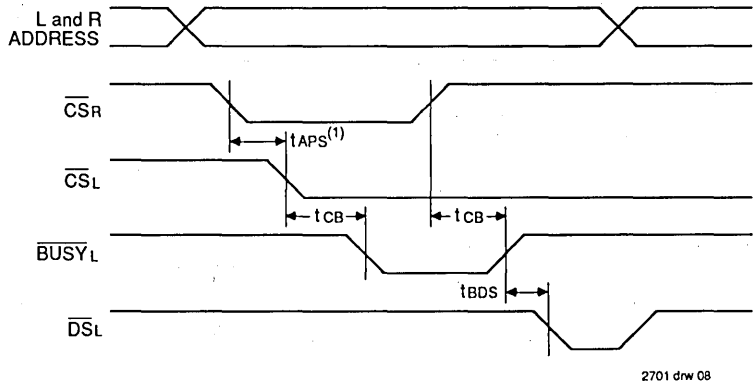
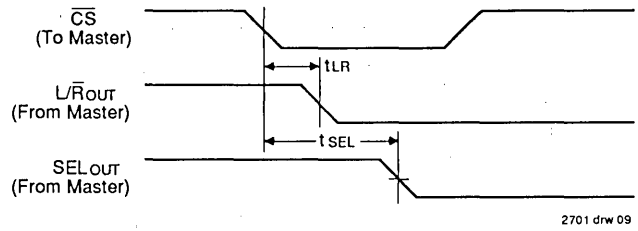
TIMING WAVEFORM OF CONTENTION WRITE CYCLE

$\overline{CS}_R$ Valid First:



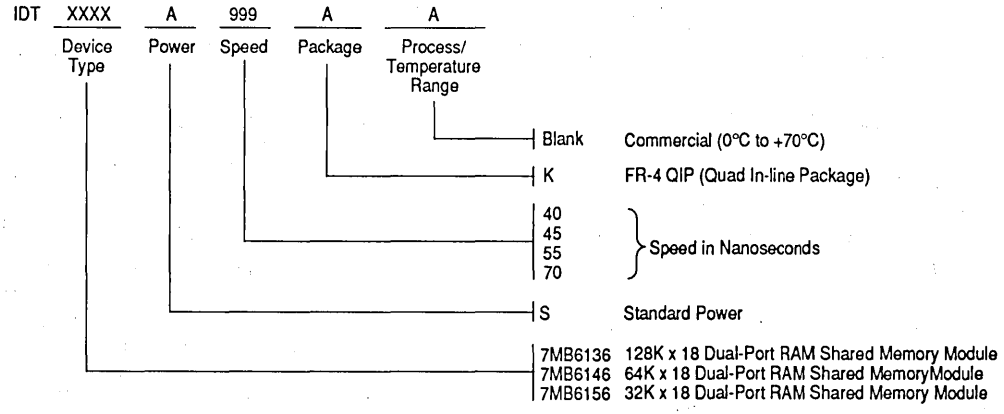
TIMING WAVEFORM OF SLAVE(2)



NOTES:

1. t_{APS} is only necessary to guarantee right side access (in this example). Within this set-up time, one side or the other will gain access, but neither will have priority.
2. $\overline{CS}$ inputs to the Slave are ingnored when configured as a Slave. This allows the Master to control port selection of the Slave with the L/$\overline{R}_{OUT}$ and SEL_{OUT} signals.

ORDERING INFORMATION



2701 drw 11

8

Integrated Device Technology, Inc.

16K x 32 CMOS DUAL-PORT STATIC RAM MODULE

PRELIMINARY
IDT7M1002

FEATURES

- High density 512K CMOS dual-port RAM modules
- Fast access times
  —commercial: 40, 45, 55, 65, 80ns
  —military: 45, 55, 65, 80, 100ns
- Fully asynchronous read/write operation from either port
- Easy to expand data bus width to 64 bits or more using the Master/Slave function
- Separate byte read/write signals for byte control
- On-chip port arbitration logic
- $\overline{INT}$ flag for port-to-port communication
- Full on-chip hardware support of semaphore signaling between ports
- Surface mounted fine pitch (25 mil) LCC packages allow through-hole module to fit into 121 pin PGA footprint
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible

DESCRIPTION

The IDT7M1002 is a 16K x 32 high speed CMOS Dual-Port static RAM Module constructed on a co-fired ceramic substrate using four 16K x 8 (IDT7006) Dual-Port static RAMs in surface-mounted LCC packages. The IDT7M1002 module is designed to be used as stand-alone 512K dual-port RAM or as a combination Master/Slave dual-port RAM for 64-bit or more word width systems. Using the IDT Master/Slave approach in such system applications results in full-speed, error-free operation without the need for additional discreet logic.

The module provides two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory. System performance is enhanced by facilitating port-to-port communication via additional control signals $\overline{SEM}$ & $\overline{INT}$.

The IDT7M1002 module is packaged in a ceramic 121 pin PGA (Pin Grid Array)1.3 inchs square . Maximum access times as fast as 40ns are available over the commercial temperature range and 45ns over the military temperature range.

All IDT military modules are constructed with semiconductor components manufactured in compliance with the latest revision of MIL-STD-883, Class B making them ideally suited to applications demanding the highest level of performance and reliability.

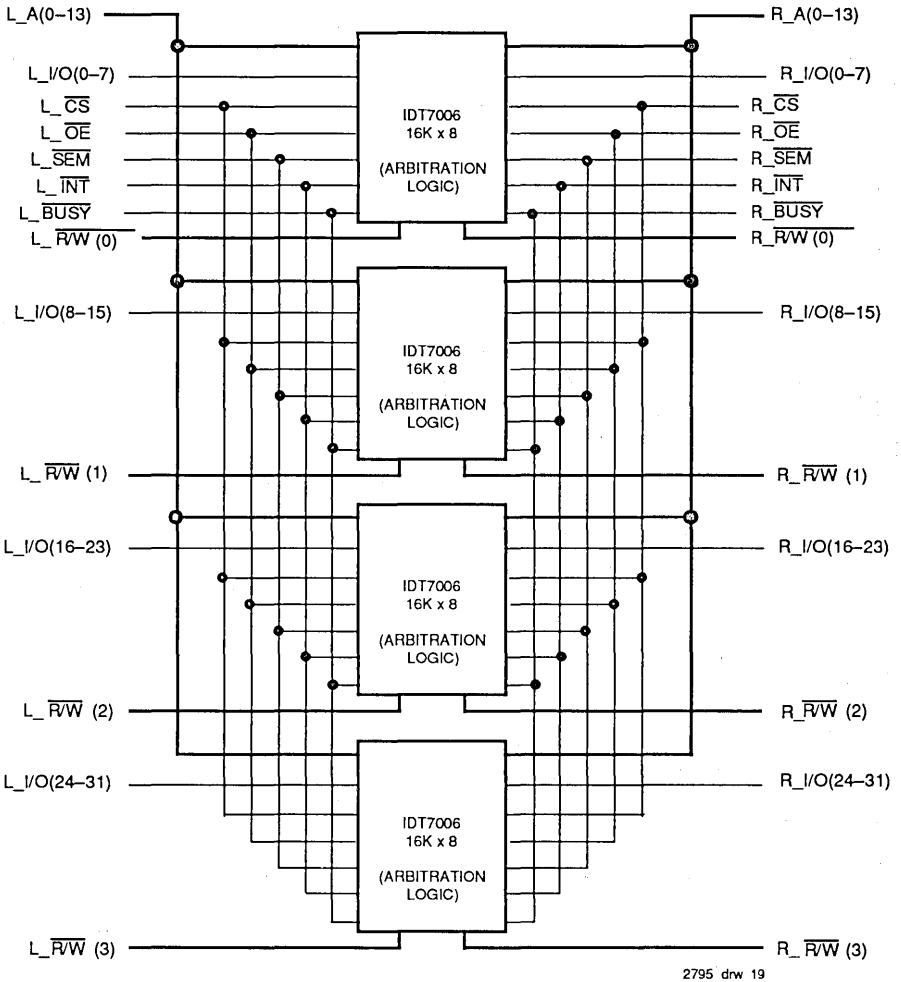
PIN CONFIGURATION (1)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	L_I/O(24)	L_I/O(26)	L_I/O(28)	L_I/O(30)	L_$\overline{CS}$	L_$\overline{OE}$	L_R/$\overline{W}$(3)	R_$\overline{OE}$	R_$\overline{CS}$	R_I/O(30)	R_I/O(28)	R_I/O(26)	R_I/O(24)
B	L_I/O(23)	L_I/O(25)	L_I/O(27)	L_I/O(29)	L_I/O(31)	L_A(0)	L_R/$\overline{W}$(4)	R_A(0)	R_I/O(31)	R_I/O(29)	R_I/O(27)	R_I/O(25)	R_I/O(23)
C	L_I/O(21)	L_I/O(22)	VCC	L_A(3)	L_A(2)	L_A(1)	GND	R_A(1)	R_A(2)	R_A(3)	GND	R_I/O(22)	R_I/O(21)
D	L_I/O(19)	L_I/O(20)	L_A(4)	GND							R_A(4)	R_I/O(20)	R_I/O(19)
E	L_I/O(17)	L_I/O(18)	L_A(5)								R_A(5)	R_I/O(18)	R_I/O(17)
F	L_$\overline{SEM}$	L_I/O(16)	L_A(6)								R_A(6)	R_I/O(16)	R_$\overline{SEM}$
G	L_$\overline{BUSY}$	L_$\overline{INT}$	GND				PGA TOP VIEW				GND	R_$\overline{INT}$	R_$\overline{BUSY}$
H	L_R/$\overline{W}$(1)	L_R/$\overline{W}$(2)	L_A(7)								R_A(7)	R_R/$\overline{W}$ (2)	R_R/$\overline{W}$ (1)
I	L_I/O(15)	L_I/O(14)	L_A(8)								R_A(8)	R_I/O(14)	R_I/O(15)
J	L_I/O(13)	L_I/O(12)	L_A(9)								R_A(9)	R_I/O(12)	R_I/O(14)
K	L_I/O(11)	M/$\overline{S}$	GND	L_A(10)	L_A(11)	L_A(12)	GND	R_A(12)	R_A(11)	R_A(10)	VCC	GND	R_I/O(13)
L	L_I/O(10)	L_I/O(8)	L_I/O(6)	L_I/O(4)	L_I/O(2)	L_A(13)	R_R/$\overline{W}$ (4)	R_A(13)	R_I/O(2)	R_I/O(4)	R_I/O(6)	R_I/O(8)	R_I/O(10)
M	L_I/O(9)	L_I/O(7)	L_I/O(5)	L_I/O(3)	L_I/O(1)	L_I/O(0)	R_R/$\overline{W}$ (3)	R_I/O(0)	R_I/O(1)	R_I/O(3)	R_I/O(5)	R_I/O(7)	R_I/O(9)

NOTE:

1. For module dimensions, please refer to drawing M33 in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



2795 drw 19

PIN NAMES

Left Port	Right Port	Description
L_A (0–13)	R_A (0–13)	Address Inputs
L_I/O (0–31)	R_I/O (0–13)	Data Inputs/Outputs
L_R/W (1–4)	R_R/W (1–4)	Read/Write Enables
L_CS	R_CS	Chip Select
L_OE	R_OE	Output Enable
L_BUSY	R_BUSY	Busy Flag
L_INT	R_INT	Interrupt Flag
L_SEM	R_SEM	Semaphore Control
M/S		Master/Slave Control
Vcc		Power
GND		Ground

2795 tbl 01

8

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Rating	Commerical	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2795 tbl 02

NOTE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2795 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

2795 tbl 04

NOTE:
1. $V_{IL} \geq -3.0V$ for pulse width less than 20ns

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7M1002 Min.	IDT7M1002 Max.	Units
$\|I_{LI}\|$	Input Leakage (Address & Control)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	40	µA
$\|I_{LI}\|$	Input Leakage (DATA)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage (DATA)	V_{CC} = Max. $\overline{CS} \geq V_{IH}$, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min. I_{OL} = 4mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = –4mA	2.4	—	V

2795 tbl 05

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7M1002 (Commercial) Min.	IDT7M1002 (Commercial) Max.	IDT7M1002 (Military) Min.	IDT7M1002 (Military) Max.	Units
I_{CC2}	Dynamic Operating Current (Both Ports Active)	V_{CC} = Max., $\overline{CS} \leq V_{IL}$, $\overline{SEM}$ = Don't Care Outputs Open, f = f_{MAX}	—	1360	—	1400	mA
I_{SB}	Standby Supply Current (Both Ports Inactive)	V_{CC} = Max., L_$\overline{CS}$ and R_$\overline{CS} \geq V_{IH}$ Outputs Open, f = f_{MAX}	—	280	—	340	mA
I_{SB1}	Standby Suppy Current (One Port Inactive)	V_{CC} = Max., L_$\overline{CS}$ or R_$\overline{CS} \geq V_{IH}$ Outputs Open, f = f_{MAX}	—	1000	—	1160	mA
I_{SB2}	Full Standby Supply Current (Both Ports Inactive)	L_$\overline{CS}$ and R_$\overline{CS} \geq V_{CC}$ – 0.2V $V_{IN} > V_{CC}$ – 0.2V or < 0.2V L_$\overline{SEM}$ and R_$\overline{SEM} \geq V_{CC}$ – 0.2V	—	60	—	120	mA

2795 tbl 05

CAPACITANCE [1] (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
CIN (1)	Input Capacitance ($\overline{CS}$, $\overline{OE}$, $\overline{SEM}$, Address)	VIN = 0V	40	pF
CIN(2)	Input Capacitance (R/$\overline{W}$, $\overline{I/O}$, $\overline{INT}$)	VIN = 0V	12	pF
CIN(3)	Input Capacitance ($\overline{BUSY}$, M/$\overline{S}$)	VIN = 0V	45	pF
COUT	Output Capacitance (I/O)	VOUT = 0V	12	pF

2795 tbl 07

NOTE:
1. This parameter is guaranteed by design but not tested.

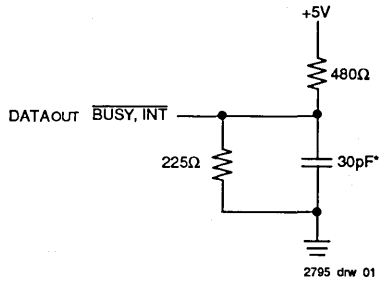


Figure 1. Output Load

*Including scope and jig.

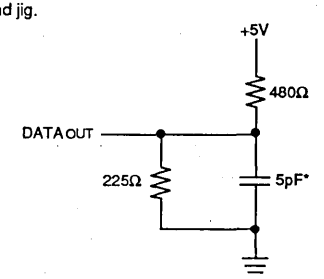


Figure 2. Output Load

(For tCHZ, tCLZ, tOHZ, tOLZ, tWHZ, tOW)

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2795 tbl 08

AC ELECTRICAL CHARACTERISTICS

(VCC = 5V ± 10%, TA = –55°C to +125°C or 0°C to +70°C)

		7M1002S40 (Com'l Only)		7M1002S45		7M1002S55		7M1002S65		7M1002S80		7M1002S100 (Mil Only)		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle														
tRC	Read Cycle Time	40	—	45	—	55	—	65	—	80	—	100	—	ns
tAA	Address Access Time	—	40	—	45	—	55	—	65	—	80	—	100	ns
tACS [2]	Chip Select Access Time	—	40	—	45	—	55	—	65	—	80	—	100	ns
tOE	Output Enable Access Time	—	20	—	25	—	30	—	35	—	40	—	45	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	3	—	ns
tCLZ [1]	Chip Select to Output in Low Z	3	—	5	—	5	—	5	—	5	—	5	—	ns
tCHZ [1]	Chip Deselect to Output in High Z	—	15	—	20	—	25	—	30	—	35	—	40	ns
tOLZ [1]	Output Enable to Output in Low Z	3	—	5	—	5	—	5	—	5	—	5	—	ns
tOHZ [1]	Output Disable to Output in High Z	—	15	—	20	—	25	—	30	—	35	—	40	ns
tPU [1]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tPD [1]	Chip Deselect to Power Up Time	—	50	—	50	—	50	—	50	—	50	—	50	ns
tSOP	Sem. Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	15	—	15	—	15	—	15	—	ns
Write Cycle														
tWC	Write Cycle Time	40	—	45	—	55	—	65	—	80	—	100	—	ns
tCW [2]	Chip Select to End of Write	35	—	40	—	45	—	50	—	55	—	60	—	ns
tAW	Address Valid to End of Write	35	—	40	—	45	—	50	—	55	—	60	—	ns
tAS	Address Set-Up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	35	—	35	—	40	—	50	—	55	—	60	—	ns

2795 tbl 09

(Continued on next page)

8

AC ELECTRICAL CHARACTERISTICS

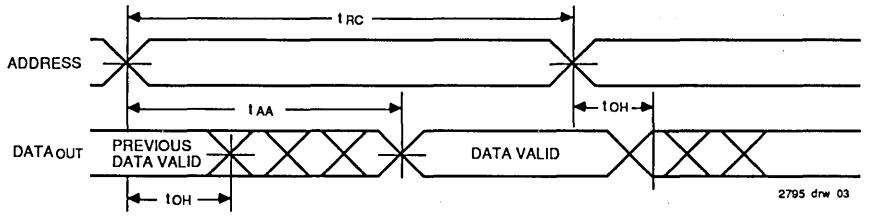
(VCC = 5V ± 10%, T_A = 55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	7M1002S40 (Com'l Only)		7M1002S45		7M1002S55		7M1002S65		7M1002S80		7M1002S100 (Mil Only)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle (continued)														
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	25	—	25	—	30	—	40	—	45	—	50	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tOHZ (1)	Output Disable to Output in High Z	—	15	—	20	—	25	—	30	—	35	—	40	ns
tWHZ (1)	Write Disable to Output in High Z	—	15	—	20	—	25	—	30	—	35	—	40	ns
tOW (1)	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	10	—	10	—	10	—	10	—	10	—	10	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	10	—	10	—	10	—	10	—	10	—	10	—	ns
Busy Cycle-Master Mode (3)														
tBAA	$\overline{BUSY}$ Access Time to Address	—	30	—	35	—	45	—	45	—	50	—	50	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	30	—	30	—	40	—	40	—	45	—	45	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Select	—	30	—	30	—	40	—	40	—	45	—	45	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Deselect	—	25	—	25	—	35	—	35	—	40	—	40	ns
tWDD (5)	Write Pulse to Data Delay	—	60	—	70	—	80	—	85	—	90	—	100	ns
tDDD	Write Data Valid to Read Data Delay	—	40	—	50	—	60	—	70	—	75	—	85	ns
tAPS (6)	Arbitration Priority Set-Up Time	5	—	5	—	5	—	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Time	—	NOTE 9	—	NOTE 9	—	NOTE 9	—	NOTE 9	—	NOTE 9	—	NOTE 9	ns
Busy Cycle-Slave Mode (4)														
tWB (7)	Write to BUSY Input	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWH (8)	Write Hold after BUSY	25	—	25	—	25	—	25	—	25	—	25	—	ns
tWDD (5)	Write Pulse to Data Delay	—	60	—	70	—	80	—	85	—	100	—	120	ns
tDDD (5)	Write Data Valid to Read Data Valid	—	45	—	50	—	60	—	70	—	85	—	105	ns
Interrupt Timing														
tAS	Address Set-Up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	30	—	35	—	40	—	45	—	55	—	65	ns
tINR	Interrupt Reset Time	—	30	—	35	—	40	—	45	—	55	—	65	ns

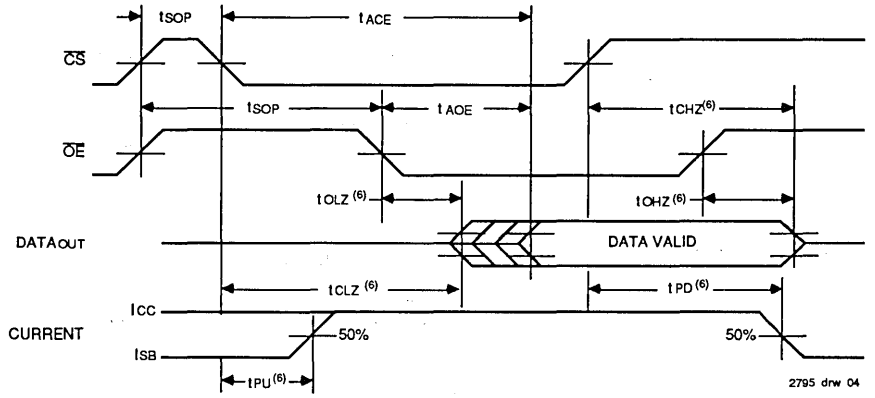
2795 tbl 10

NOTE:
1. This parameter is guaranteed by design but not tested.
2. To access RAM, $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
3. When the module is being used in the Master Mode ($M/\overline{S} \geq V_{IH}$).
4. When the module is being used in the Slave Mode ($M/\overline{S} \leq V_{IL}$).
5. Port-to-Port delay through the RAM cells from the writing port to the reading port.
6. To ensure that the earlier of the two ports wins.
7. To ensure that the write cycle is inhibited during contention.
8. To ensure that a write cycle is completed after contention.
9. tBDD is a calculated parameter and is the greater of 0, tWDD - tWP (actual), or tDDD - tWP (actual).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE (1, 2, 4)



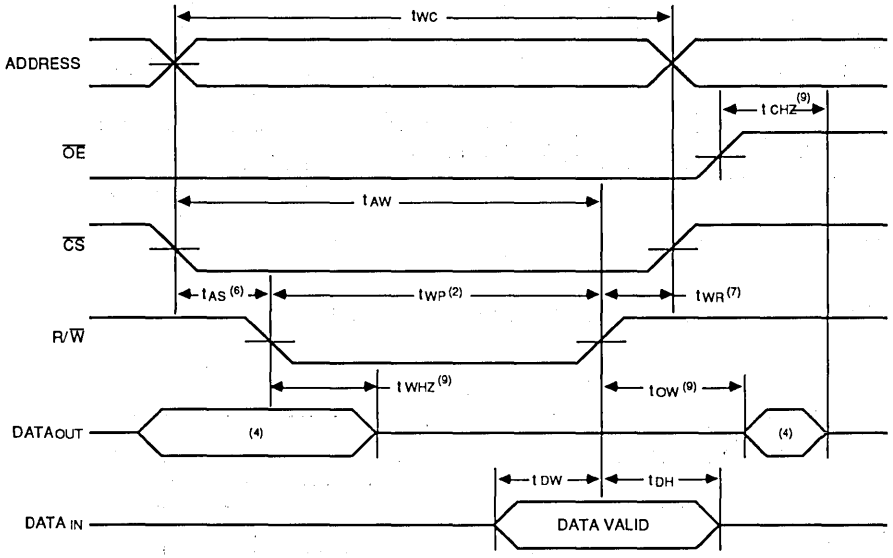
TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1, 3, 5)



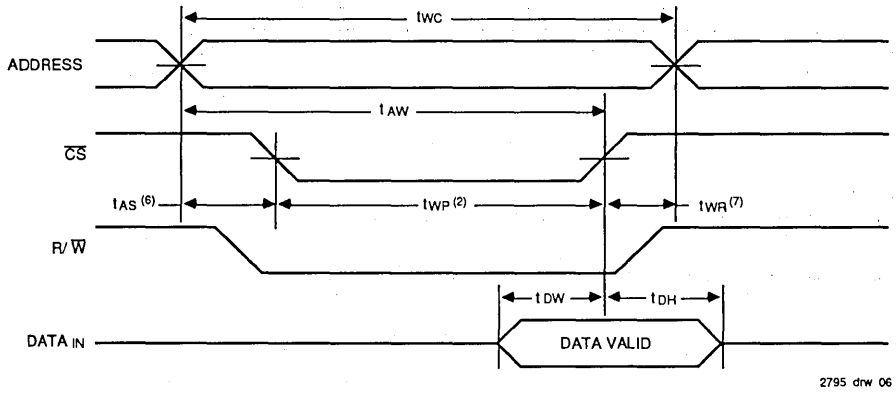
NOTES:
1. R/$\overline{W}$ is high for Read Cycles
2. Device is continuously enabled $\overline{CS} \leq V_{IL}$. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} \leq V_{IL}$
5. To access RAM, $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To accesss semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
6. This parameter is guaranteed by design but not tested.

8

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING) (1, 2, 4)

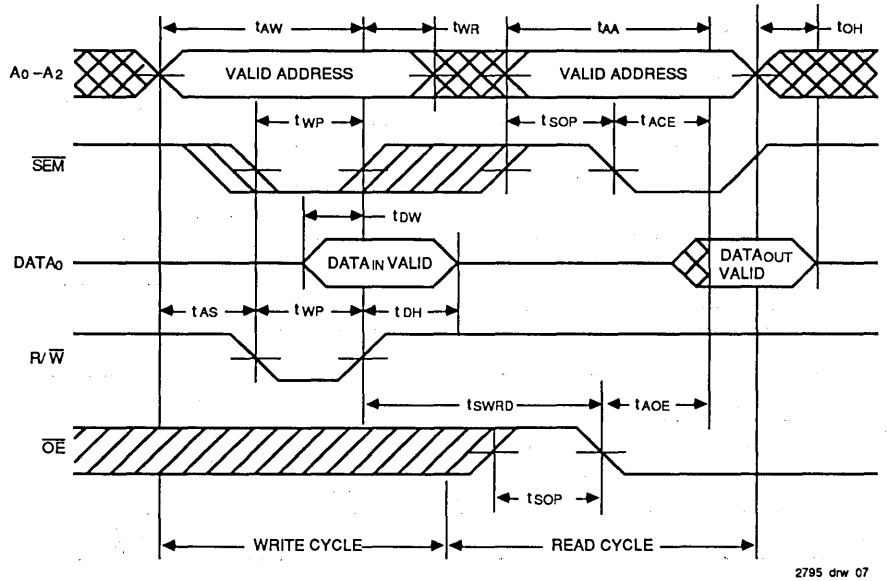


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING) (1, 2, 4)



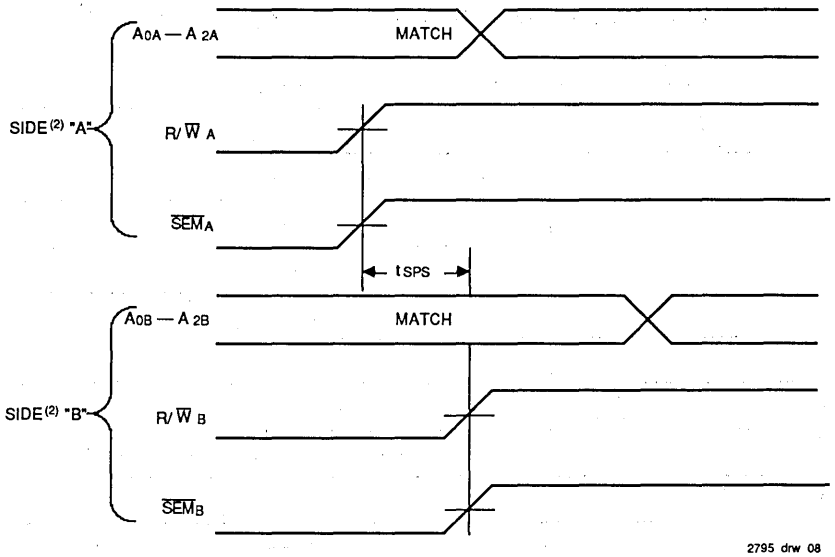
NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must be applied.
5. If the $\overline{CS}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE, EITHER SIDE (1)



NOTE:
1. $\overline{CS} \geq V_{IH}$ for the duration of the above timing (both write and read cycle).

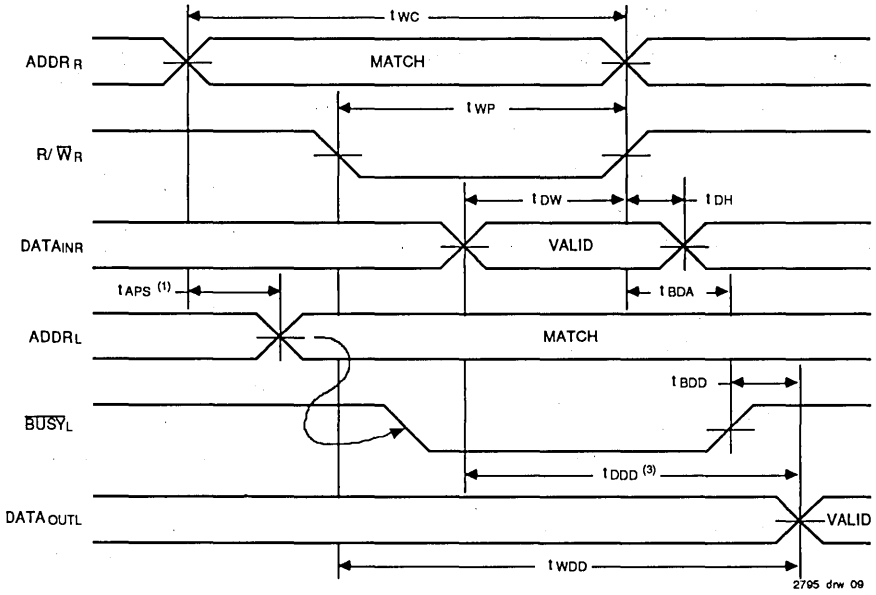
TIMING WAVEFORM OF SEMAPHORE CONTENTION (1, 3, 4)



NOTES:
1. $D_{OR} = D_{OL} \leq V_{IL}$, ($L\_\overline{CS} = R\_\overline{CS}$) $\geq V_{IH}$ Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from $R/\overline{W}_A$ or $\overline{SEM}_A$ going high to $R/\overline{W}_B$ or $\overline{SEM}_B$ going high.
4. If tSPS is violated, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

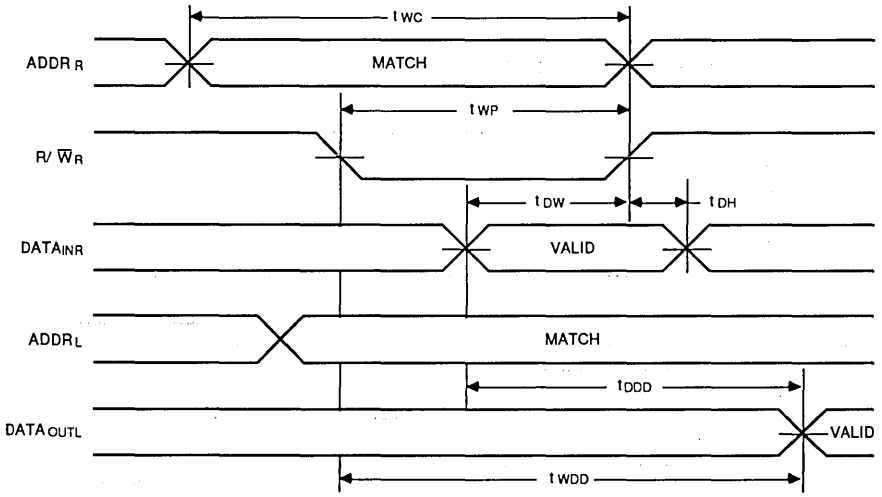
8

TIMING WAVEFORM OF READ WITH $\overline{BUSY}$ (M/$\overline{S}$ ≥ VIH)(2)



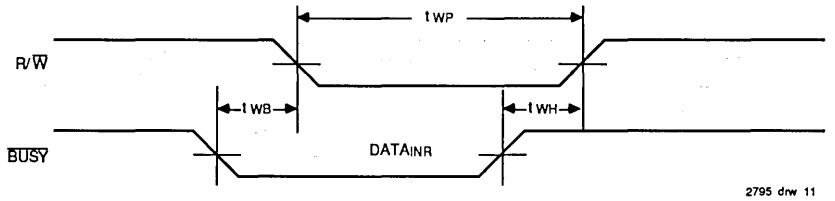
NOTES:
1. To ensure that the earlier of the two ports wins.
2. (L_ $\overline{CS}$ = R_ $\overline{CS}$) ≤ VIL
3. $\overline{OE}$ ≤ VIL for the reading port.

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY (M/$\overline{S}$ ≤ VIH) (1, 2)

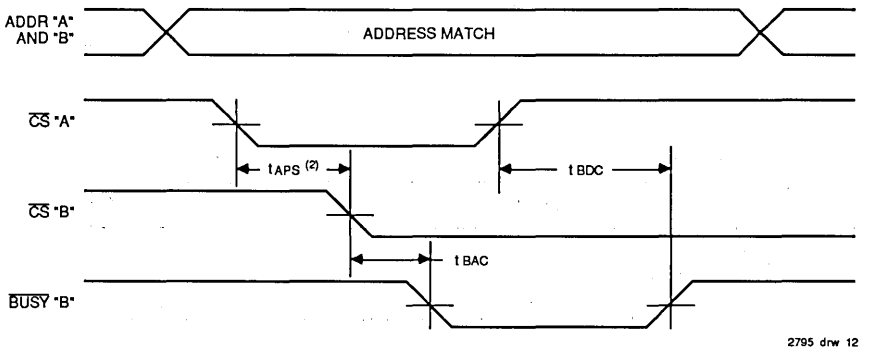


NOTES:
1. $\overline{BUSY}$ input equals High for the writing port.
2. (L_ $\overline{CS}$ = R_ $\overline{CS}$) ≤ VIL

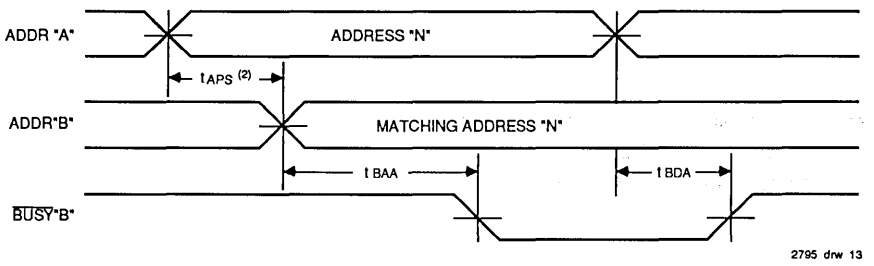
TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ INPUT (M/$\overline{S}$ ≤ VIL)



TIMING WAVEFORM OF BUSY ARBITRATION ($\overline{CS}$ CONTROLLED TIMING) (1)



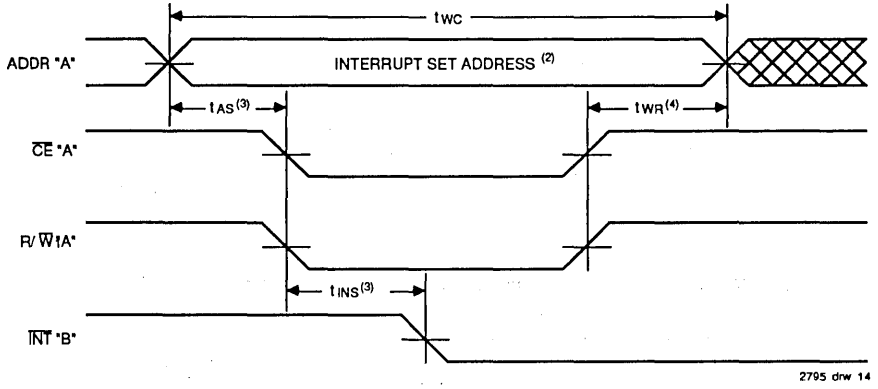
TIMING WAVEFORM OF BUSY ARBITRATION (CONTROLLED BY ADDRESS MATCH TIMING) (1)

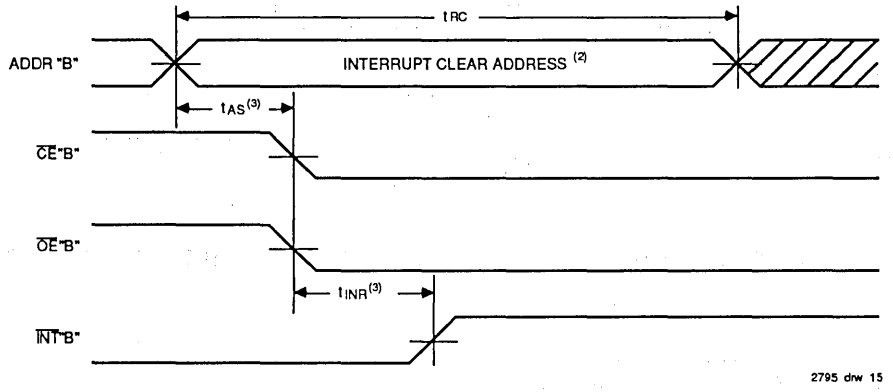


NOTES:
1. All timing is the same for the left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If tAPS is violated, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

8

TIMING WAVEFORM OF INTERRUPT CYCLE (1)





NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See Interrupt truth table.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable signal is de-asserted first.

TRUTH TABLE I: Non-Contention Read/Write Control (1)

Inputs				Outputs	Mode
$\overline{CS}$	$\overline{R/W}$	$\overline{OE}$	$\overline{SEM}$	$\overline{I/O}$	Description
H	X	X	H	High-Z	Deselected or Power Down
L	L	X	H	Data_In	Write
L	H	L	H	Data_OUT	Read
X	X	H	X	High-Z	Outputs Disabled

2795 tbl 11

NOTE:
1. The conditions for non-contention are L_A (0–13) ≠ R_A (0–13).

TRUTH TABLE II: Semaphore Read/Write Control

Inputs(1)				Outputs	Mode
$\overline{CS}$	$\overline{R/W}$	$\overline{OE}$	$\overline{SEM}$	$\overline{I/O}$	Description
H	H	L	L	Data_OUT	Read Data in Semaphore Flag
H	⎽⎽⌐	X	L	Data_IN	Write Data_IN (0, 8, 16, 24)
L	X	X	L	—	Not Allowed

2795 tbl 12

NOTE:
1. ⎽⎽⌐ denotes a LOW to HIGH waveform transition.

TABLE III: Interrupt Flag (1)

Left Port					Right Port					Function
$\overline{R/W}$ (1)	$\overline{CS}$	$\overline{OE}$	A (0–13)	$\overline{INT}$	$\overline{R/W}$ (1)	$\overline{CS}$	$\overline{OE}$	A (0–13)	$\overline{INT}$	
L	L	X	1FFF	X	X	X	X	X	L (2)	Set Right $\overline{INT}$ Flag
X	X	X	X	X	X	L	L	1FFF	H (3)	Reset Right $\overline{INT}$ Flag
X	X	X	X	L (3)	L	L	X	1FFE	X	Set Left $\overline{INT}$ Flag
X	L	L	1FFE	H (2)	X	X	X	X	X	Reset Left $\overline{INT}$ Flag

2795 tbl 13

NOTE:
1. Assuming L_$\overline{BUSY}$ = R_$\overline{BUSY}$ ≥ V_{IH}.
2. If L_$\overline{BUSY}$ ≤ V_{IL} then no change.
3. If R_$\overline{BUSY}$ ≤ V_{IL} then no change.

8

TRUTH TABLE IV: Address BUSY Arbitration

Inputs			Outputs [1]		
L_$\overline{CS}$	R_$\overline{CS}$	L_A (0-13) R_A (0-13)	L_$\overline{BUSY}$	R_$\overline{BUSY}$	Function
X	X	No Match	H	H	Normal
H	X	Match	H	H	Normal
X	H	Match	H	H	Normal
L	L	Match	Note 2	Note 2	Write Inhibit [3]

2795 tbl 14

NOTES:
1. Pins L_$\overline{BUSY}$ and R_$\overline{BUSY}$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}$ outputs on the IDT7M1002 are push pull, not open drain outputs. On slaves the $\overline{BUSY}$ input internally inhibits writes.
2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If the primacy of stable inputs cannot be resolved, either L_$\overline{BUSY}$ ≤ V_{IL} or R_$\overline{BUSY}$ ≤ V_{IL} will result in L_$\overline{BUSY}$ and R_$\overline{BUSY}$ outputs cannot be low simultaneously.
3. Writes to the left port are internallly ignored when L_$\overline{BUSY}$ outputs are driving low regardless of the actual logic levels on the pin. Writes to the right port are internally ignored when R_$\overline{BUSY}$ outputs are driving low regardless of the actual logic levels on the pin.

TABLE V: Example of Semaphore Procurement Sequence [1]

Functions	I/O Left	I/O Right	Status
No Action	1	1	Semaphore is free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore is free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore is free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore is free

2795 tbl 15

NOTE:
1. This table denotes a hypothetical sequence of events for only one of the eight semaphores available on the IDT7M1002.

FUNCTIONAL DESCRIPTION

The IDT7M1002 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7M1002 has an automatic power down feature controlled by $\overline{CS}$. The $\overline{CS}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CS}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in the Truth Tables.

INTERRUPTS

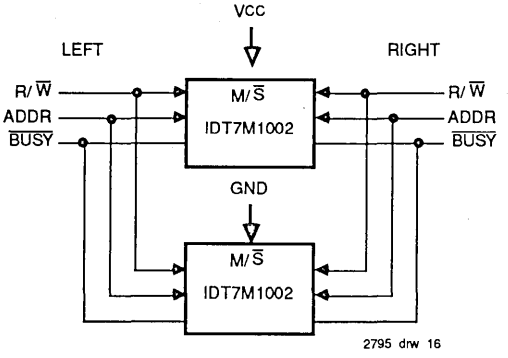
The interrupt flag ($\overline{INT}$) permits communication between ports or systems. If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is set when the right port writes to memory location 1FFE (HEX). The left port clears the interrupt by reading address location 1FFE. Likewise, the right port interrupt flag ($\overline{INT}_R$) is set when the left port writes to memory location 1FFF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 1FFF. The message (16 bits) at 1FFE or 1FFF is user-defined. If the interrupt function is not used, address locations 1FFE and 1FFF are not used as mail boxes, but as part of the random access memory. Refer to Table 1 for the interrupt operation. These interrupts are set by either L_R/$\overline{W}$1 or R_R/$\overline{W}$1 All other R/$\overline{W}$ controls have no affect on the interrupt function.

BUSY LOGIC

The arbitration logic will resolve an address match or a chip select match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CS}$, on-chip control logic arbitrates between $\overline{CS}_L$ and $\overline{CS}_R$ for access; or (2) if the $\overline{CS}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table II). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.



64-Bit Master/Slave Dual-Port Memory Systems

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION

Expanding the data bus width to sixtyfour-or-more-bits in a dual-port RAM system implies that several modules will be active at the same time. If each module includes a hardware arbitrator, and the addresses for each module arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another activates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid this "Busy Lock-Out" problem, IDT had developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE modules must be delayed, until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE module may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one module is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

SEMAPHORES

The IDT7M1002 is an extremely fast dual-port 16K x 32 CMOS Static RAM Module with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the dual-port RAM module to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the dual-port RAM or any other shared resource.

The dual-port RAM module features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS static RAM and can be read from,

or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphores portion of the dual-port RAM. These devices have an automatic power-down feature controlled by $\overline{CS}$ and $\overline{SEM}$. The $\overline{CS}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in the Truth Table where $\overline{CS}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT7M1002 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT7M1002's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT7M1002 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the dual-port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that a shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor had set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

There are 4 semaphores at each of 8 addresses. Write to the semaphores at I/O_0, I/O_8, I/O_{16}, and I/O_{24}. Read the semaphores at I/O_{0-7}, I/O_{8-15}, I/O_{16-23}, and I/O_{24-31}.

The eight semaphore flags reside within the IDT7M1002 in a separate memory space from the dual-port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$ and $R/\overline{W}$) as they would be used in accessing a standard static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A_0–A_2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin I/O_0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other (see Table V). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence of WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as a one, a fact which the processor will verify by the subsequent read (see Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during a subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 1. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one

is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request , the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen. Code integrity is of the utmost importance when semaphores are used instead of slower, more restrictive hardware intensive schemes.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—Some Examples

Perhaps the simplest application of semaphors is their application as resource markers for the IDT7M1002's Dual-Port RAM Module. Say that 8K x 16 of RAM was to be divided into two 4K x 16 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 4K of dual-port RAM, the processor on the left port could write and then read a zero into Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 4K. Meanwhile, the right processor would attempt to perform the same function. Since this processor was attempting to gain control of the resource after the left processor it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 4K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 4K blocks of dual-port RAM with each other.

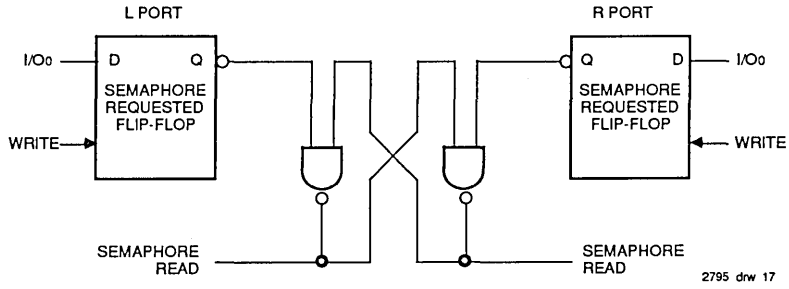


Figure 1. IDT7M1002 Semaphore Logic

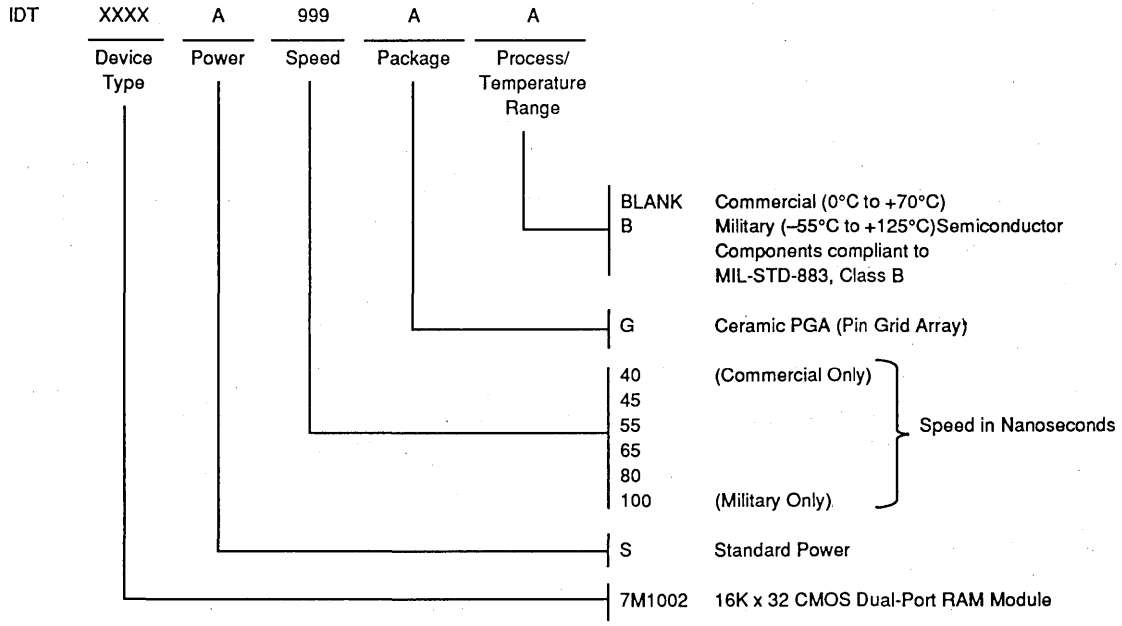
The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the dual-port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices had determined which memory area was "off limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

ORDERING INFORMATION



8

Integrated Device Technology, Inc.

8K x 8
4K x 8
CMOS FourPort™ RAM MODULE

PRELIMINARY
IDT7MB1041
IDT7MB1042

FEATURES:

- High-density 64K/32K-bit CMOS FourPort RAM Modules
- 8K x 8 (IDT7MB1041) or 4K x 8 (IDT7MB1042) option
- Fast access times
  - maximum: 35, 40, 45, 55, 65, 80, 100ns
- Fully asynchronous operation from any four ports: P1, P2, P3, P4
- Versatile control for write-inhibit: separate $\overline{BUSY}$ input to control write-inhibit for each of the other 3 ports
- Battery backup operation - 2V data retention (low power version only)
- Surface mounted fine pitch (25 mil) PQFP (Plastic Quad FlatPack) components on a FR-4 120-pin QIP (Quad In-line Package) substrate
- TTL compatible I/Os
- Single 5V (± 10%) power supply
- Multiple ground pins provide maximum noise immunity
- Input/outputs directly TTL compatible

DESCRIPTION:

The IDT7MB1041/1042 are 64/32K-bit high-speed CMOS FourPort RAM modules constructed on a multi-layer FR-4 substrate using 4 IDT7052 (2K x 8) FourPort RAMs or a depopulated version with 2 IDT7052 FourPort RAMs. The IDT7MB1041/1042 modules are designed to be used as stand-alone 64K/32K-bit fourport RAM. Using the IDT FourPort Module in such system applications as multiprocessor or real time data acquisition result in dramatically increased system performance by providing four independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory. Upper and lower byte module signals for each port provide the system additional memory control capability.

The IDT7MB1041/1042 modules are packaged in a 120-pin FR-4 QIP (Quad In-line Package) and have maximum access times of 35ns over the commercial temperature range.

PIN NAMES (1, 2)

P1-4A0 - 12	Ports 1-4, Address Inputs
P1-4I/O0 - 7	Port 1-4, Data Inputs/Outputs
R/$\overline{W}$ P1	ReadWrite - Port 1
R/$\overline{W}$ P2	Read/Write - Port 2
R/$\overline{W}$ P3	Read/Write - Port 3
R/$\overline{W}$ P4	Read/Write - Port 4
$\overline{CS}$ P1	Chip Select - Port 1
$\overline{CS}$ P2	Chip Select - Port 2
$\overline{CS}$ P3	Chip Select - Port 3
$\overline{CS}$ P4	Chip Select - Port 4
$\overline{OE}$ P1	Output Enable - Port 1
$\overline{OE}$ P2	Output Enable - Port 2
$\overline{OE}$ P3	Output Enable - Port 3
$\overline{OE}$ P4	Output Enable - Port 4
$\overline{BUSY}$ P1	Port Busy Write Disable - Port 1
$\overline{BUSY}$ P2	Port Busy Write Disable - Port 2
$\overline{BUSY}$ P3	Port Busy Write Disable - Port 3
$\overline{BUSY}$ P4	Port Busy Write Disable - Port 4
Vcc	Power
GND	Ground

2802 tbl 01

PIN CONFIGURATION

Note: Pin configurations for these modules are currently not available, please consult the factory.

Notes:
1. For valid read operation, no other part may write to the same address location at the same time.
2. For the IDT7MB1042 (4K x 8) version, P1A12, P2A12, P3A12, P4A12 must be connected to GND for proper operation of the module.

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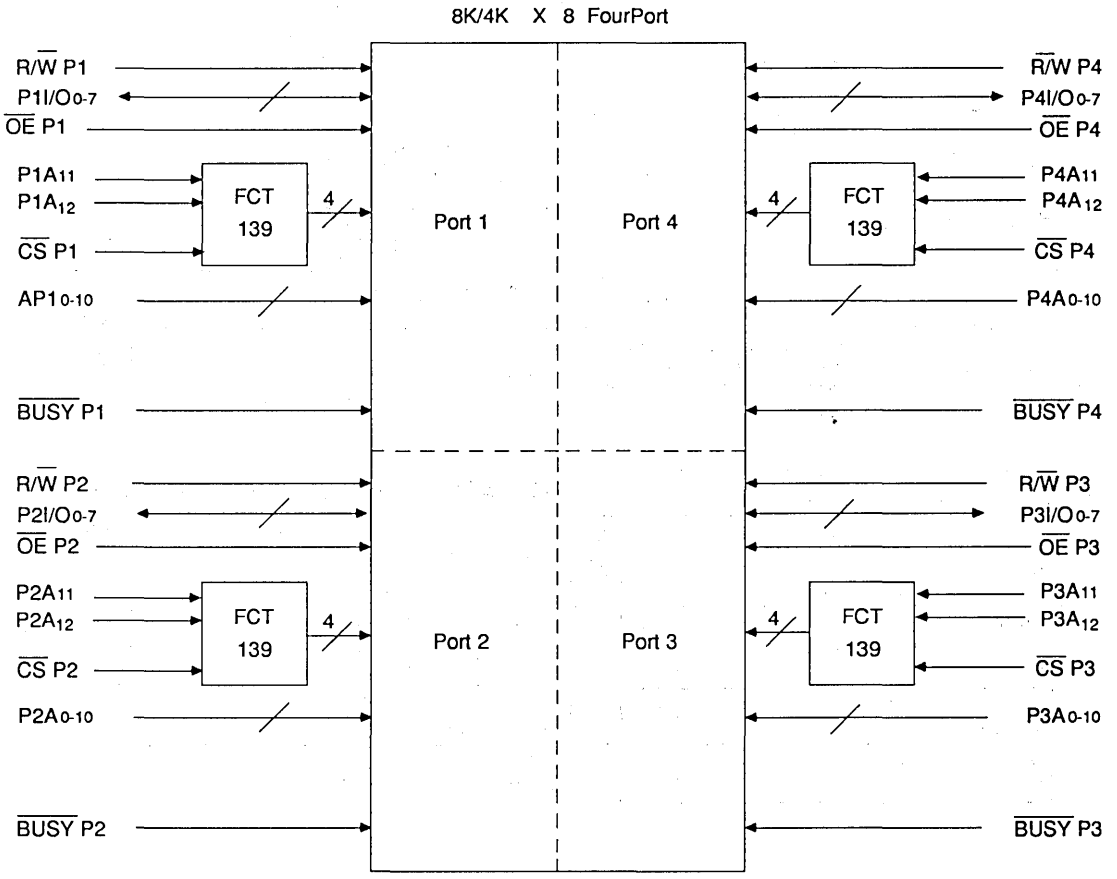
FUNCTIONAL BLOCK DIAGRAM



2802 drw 01

8

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to ± 7.0	-0.5 to ± 7.0	V
TA	Operating Temperature	0 to +70	-55 to + 125	°C
TBIAS	Temperature Under Bias	-55 to + 125	-65 to + 135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2802 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to + 70°C	OV	5.0V± 10%

2801 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE: 2802 tbl 04

1. VIL (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS

(Vcc=5.0V ± 10%, TA = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
|ILI|	Input Leakage Current	Vcc = 5.5V, VIN = 0V to Vcc	—	40	µA
|ILO|	Output Leakage Current	$\overline{CS}$ = VIH, VOUT = 0V to Vcc	—	40	µA
VOL	Output Low Voltage	IOL = 4mA	—	0.4	V
VOH	Output High Voltage	IOH = -4mA	2.4	—	V

2802 tbl 05

CAPACITANCE(1) (TA= +25°C, F = 1.0 MHz)

Symbol	Parameter	Test Conditions	IDT7MB1041/1042 Max.	Max.	Unit
CIN1	Input Capacitance	VIN = 0V	12	12	pF
CIN2	Input Capacitance (Data, Address, All Other Controls)	VIN = 0V	50	25	pF
COUT	Output Capacitance (Data)	VOUT = 0V	45	25	pF

NOTE: 2802 tbl 06

1. This parameter is guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS

(Vcc=5.0V ± 10%, TA = 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7MB1041 Min.	Max.	IDT7MB1042 Min.	Max.	Unit
ICC1	Operating Power Supply Current (All Ports Active)	$\overline{CS}$ ≥ VIL, Outputs Open f = 0	—	550	—	400	mA
ICC2	Dynamic Operating Current	$\overline{CS}$ ≥VIL, Outputs Open f = fMAX	—	600	—	430	mA
ISB	Standby current (All Ports - TTL Level Inputs)	$\overline{CS}$ = VIH, Outputs Open f = fMAX	—	340	—	170	mA
ISB1	Full Standby Current (All Ports - All CMOS Level Inputs)	All Ports $\overline{CS}$ ≥ Vcc -0.2V VIN ≥Vcc -0.2V or VIN ≤ 0.2V, f = 0	—	20	—	10	mA

2802 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2802 tbl 08

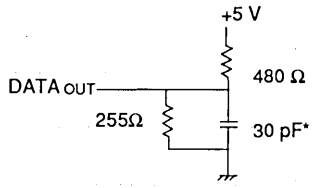


Figure 1. Output Load

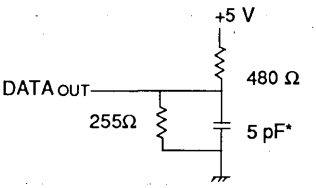


Figure 2. Output Load (for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{WHZ}, t_{OW})

*Including scope and jig.

2802 drw 02

AC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MB1041S35 7MB1042S35 Min.	Max.	7MB1041S40 7MB1042S40 Min.	Max.	7MB1041S45 7MB1042S45 Min.	Max.	7MB1041S55 7MB1042S55 Min.	Max.	7MB1041S65 7MB1042S65 Min.	Max.	7MB1041S80 7MB1042S80 Min.	Max.	7MB1041S100 7MB1042S100 Min.	Max.	Unit
Read Cycle																
t_{RC}	Read Cycle Time	35	—	40	—	45	—	55	—	65	—	80	—	100	—	ns
t_{AA}	Address Access Time	—	35	—	40	—	45	—	55	—	65	—	80	—	100	ns
t_{ACS}	Chip Select Access Time	—	35	—	40	—	45	—	55	—	65	—	80	—	100	ns
t_{OE}	Output Enable Access Time	—	25	—	25	—	30	—	40	—	50	—	65	—	85	ns
t_{OH}	Output Hold From Address Change	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{CLZ}(2)	Chip Select to Output in Low Z	3	—	5	—	5	—	5	—	5	—	10	—	10	—	ns
t_{OLZ}(2)	Output Enable to Output in Low Z	3	—	5	—	5	—	5	—	5	—	10	—	10	—	ns
t_{CHZ}(2)	Chip Deselect to Output in High Z	20	—	20	—	25	—	25	—	25	—	30	—	30	—	ns
t_{OHZ}(2)	Output Disable to Output in High Z	20	—	20	—	25	—	25	—	25	—	30	—	30	—	ns
t_{PU}(2)	Chip Enable to Power Up Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}(2)	Chip Disable to Power Down Time	—	35	—	55	—	55	—	50	—	70	—	70	—	70	ns

NOTES:

2802 tbl 09

1. Transition is measured by ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed by design but not tested.

8

AC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

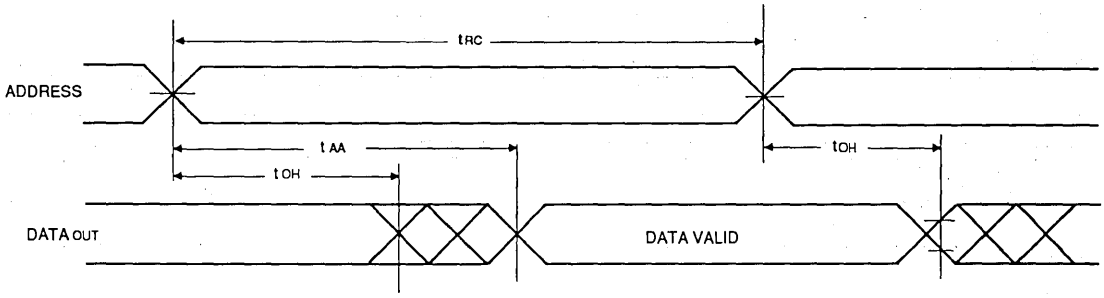
Symbol	Parameter	7MB1041S35 7MB1042S35 Min.	Max.	7MB1041S40 7MB1042S40 Min.	Max.	7MB1041S45 7MB1042S45 Min.	Max.	7MB1041S55 7MB1042S55 Min.	Max.	7MB1041S65 7MB1042S65 Min.	Max.	7MB1041S80 7MB1042S80 Min.	Max.	7MB1041S100 7MB1042S100 Min.	Max.	Unit
Write Cycle																
t_{WC}	Write Cycle Time	35	—	40	—	45	—	55	—	65	—	80	—	100	—	ns
t_{CW}	Chip Select to End of Write	30	—	35	—	35	—	45	—	55	—	70	—	90	—	ns
t_{AW}	Address Valid to End of Write	30	—	35	—	35	—	45	—	55	—	70	—	90	—	ns
t_{AS1}	Address Set-up to $\overline{CS}$ Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{AS2}	Address Set-up to R/$\overline{W}$ Time	5	—	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{WP}	Write Pulse Width	25	—	30	—	35	—	45	—	45	—	45	—	45	—	ns
t_{WR}	Write Recovery Time	5	—	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{DW}	Data Valid to End of Write	20	—	20	—	20	—	20	—	20	—	30	—	30	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}[2]	Write Enabled to Output in High Z	—	18	—	18	—	20	—	20	—	20	—	30	—	30	ns
t_{OW}	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WDD}	Write Pulse to Data Delay	—	50	—	65	—	70	—	80	—	80	—	90	—	100	ns
t_{DDD}	Write Data Valid to Read Data Delay	—	40	—	45	—	45	—	55	—	65	—	80	—	100	ns
Busy Input Timing																
t_{WB}	Write to $\overline{BUSY}$	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$	20	—	20	—	25	—	25	—	25	—	30	—	30	—	ns

NOTES:

2802 tbl 10

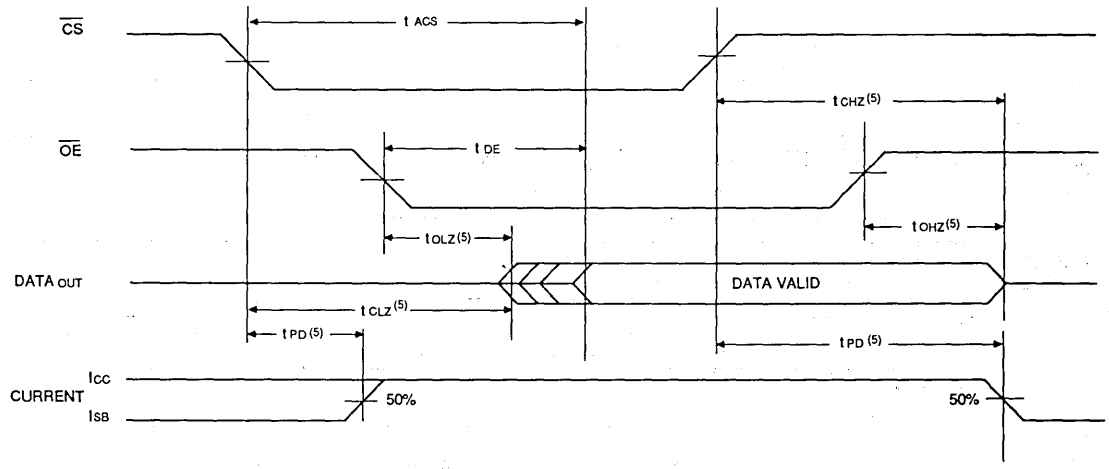
1. Transition is measured by ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is quaranteed by design but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1, ANY PORT(1,2,4)



2802 drw 03

TIMING WAVEFORM OF READ CYCLE NO. 2, ANY PORT(1,3)

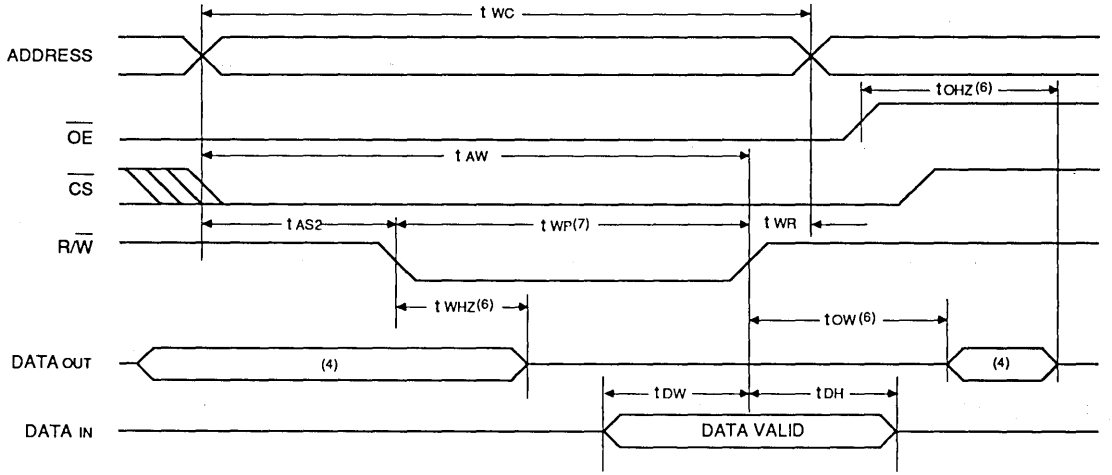


2802 drw 04

NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled. $\overline{CS} \geq V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} \geq V_{IL}$.
5. This parameter is guaranteed by design but not tested.

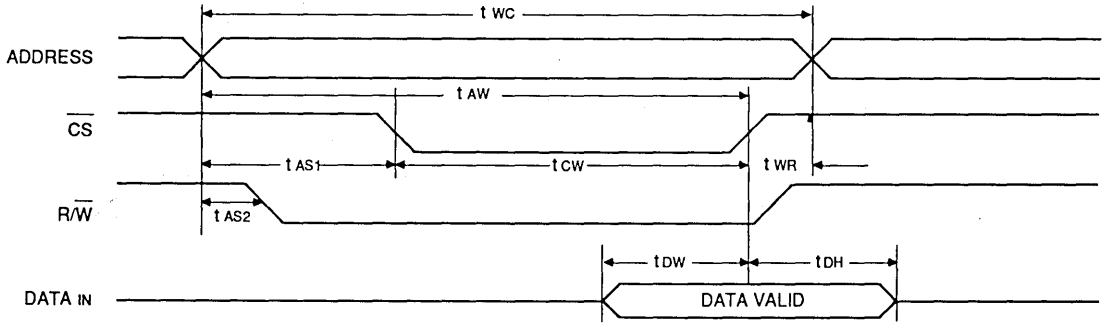
8

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,2,3,7)



2802 drw 05

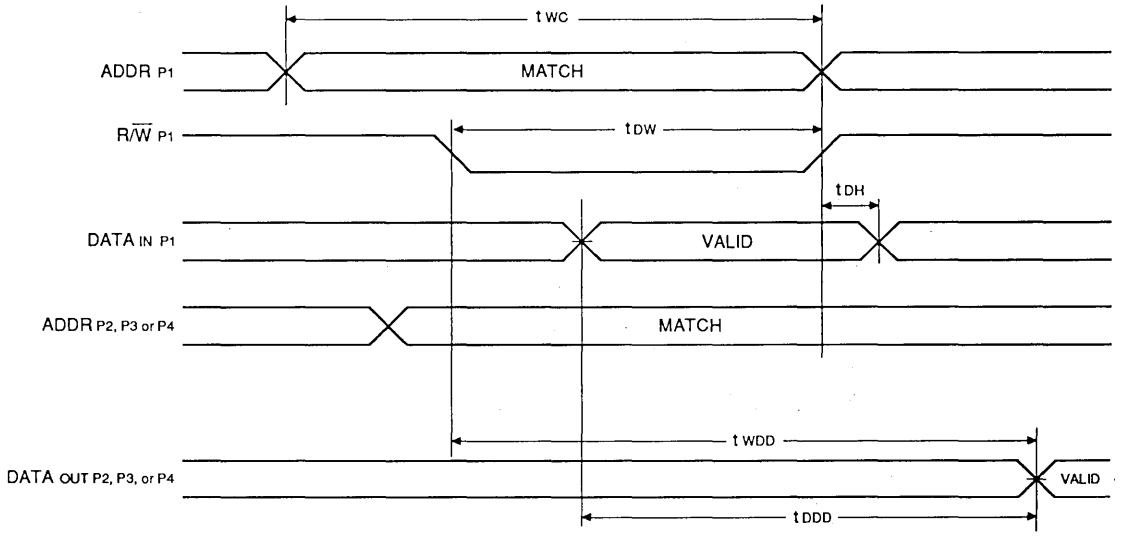
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CS}$ CONTROLLED TIMING(1,2,3,5)



2802 drw 06

NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the ouputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design but not tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the busfor the required tDW. If $\overline{OE}$ is high during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

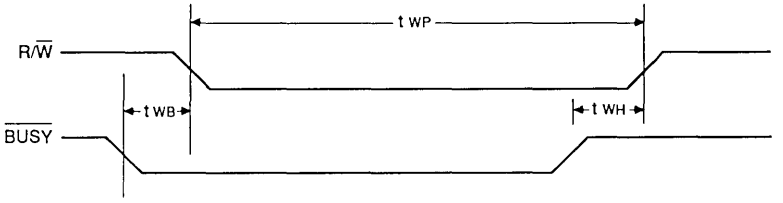
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY(1,2,3)



NOTES:
1. Assume $\overline{BUSY}$ input at High and $\overline{CS}$ at Low for the writing port.
2. Write cycle parameters should be adhered to, to ensure proper writing.
3. Device is continuously enabled for any of the reading ports which has its $\overline{OE}$ at Low.

2802 drw 07

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ INPUT



2802 drw 08

FUNCTIONAL DESCRIPTION

The IDT7MB1041/1042 provides four ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by $\overline{CS}$. The $\overline{CS}$ controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{CS}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. READ/WRITE conditions are illustrated in the table below.

READ/WRITE CONTROL

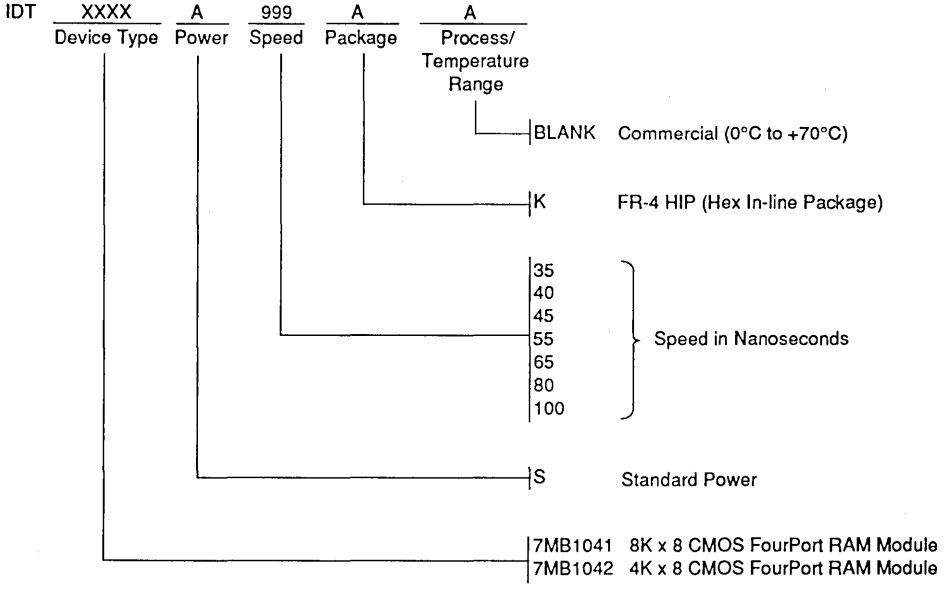
ANY PORT					
$\overline{CS}$	R/$\overline{W}$	$\overline{OE}$	$\overline{BUSY}$	I/O0-7	FUNCTION
H	X	X	X	HI-Z	Port Disabled and in Power Down Mode
L	L	X	H	DATAIN	Write Cycle
X	L	X	L	HI-Z	Write is Blocked
L	H	L	X	DATAOUT	Read Cycle
X	X	H	X	HI-Z	High Impedance Outputs

2802 drw 11

NOTES:

1. H = High, L - Low, X = Don't Care, Z = High Impedance.
2. If $\overline{BUSY}$ = Low, Data is not written.
3. For valid write operation, no more than one port can write to the same address location at the same time.

ORDERING INFORMATION



Integrated Device Technology, Inc.

4K x 16
2K x 16
CMOS FourPort™ RAM MODULE

PRELIMINARY
IDT7MB1043
IDT7MB1044

FEATURES:

- High density 64K/32K CMOS FourPort RAM Modules
- 4K x 16 (IDT7MB1043) or 2K x 16 (IDT7MB1044) option
- Fast access times
  - maximum: 35, 40, 45, 55, 65, 80, 100ns
- Fully asynchronous operation from any four ports: P1, P2, P3, P4
- Versatile control for write-inhibit: separate $\overline{BUSY}$ input to control write-inhibit for each of the other 3 ports
- Battery backup operation - 2V data retention (low power version only)
- Surface mounted fine pitch (25 mil) PQFP (Plastic Quad FlatPack) components on a FR-4 162-pin HIP (Hex In-line Package) substrate
- TTL compatible I/Os
- Single 5V (± 10%) power supply
- Multiple ground pins provide maximum noise immunity
- Input/outputs directly TTL compatible

DESCRIPTION:

The IDT7MB1043/1044 are 64/32K-bit high speed CMOS FourPort RAM modules constructed on a multi-layer FR-4 substrate using 4 IDT7052 (2K x 8) FourPort RAMs or a depopulated version with 2 IDT7052 FourPort RAMs. The IDT7MB1043/1044 modules are designed to be used as stand-alone 64K/32K-bit fourport RAM. Using the IDT FourPort Module in such system applications as multiprocessor or real time data acquistion result in dramatically increased system performance by providing four independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory. Upper and lower byte module signals for each port provide the system additional memory control capability.

The IDT7MB1043/1044 modules are packaged in a 162 pin FR-4 HIP (Hex In-line Package) and have maximum access times of 30ns over the commercial temperature range.

PIN NAMES (1, 2)

$P1\text{-}4A_{0-11}$	Ports 1-4, Address Inputs
$P1\text{-}4I/O_{0-15}$	Port 1-4, Data Inputs/Outputs
$R/\overline{W}$ UP1, LP1	ReadWrite - Upper/Lower Byte Port 1
$R/\overline{W}$ UP2, LP2	Read/Write - Upper/Lower Byte Port 2
$R/\overline{W}$ UP3, LP3	Read/Write - Upper/Lower Byte Port 3
$R/\overline{W}$ UP4, LP4	Read/Write - Upper/Lower Byte Port 4
$\overline{CS}$ UP1, LP1	Chip Select - Upper/Lower Byte Port 1
$\overline{CS}$ UP2, LP2	Chip Select - Upper/Lower Byte Port 2
$\overline{CS}$ UP3, LP3	Chip Select - Upper/Lower Byte Port 3
$\overline{CS}$ UP4, LP4	Chip Select - Upper/Lower Byte Port 4
$\overline{OE}$ UP1, LP1	Output Enable - Upper/Lower Byte Port 1
$\overline{OE}$ UP2, LP2	Output Enable - Upper/Lower Byte Port 2
$\overline{OE}$ UP3, LP3	Output Enable - Upper/Lower Byte Port 3
$\overline{OE}$ UP4, LP4	Output Enable - Upper/Lower Byte Port 4
$\overline{BUSY}$ P1	Port Busy Write Disable - Port 1
$\overline{BUSY}$ P2	Port Busy Write Disable - Port 2
$\overline{BUSY}$ P3	Port Busy Write Disable - Port 3
$\overline{BUSY}$ P4	Port Busy Write Disable - Port 4
V_{CC}	Power
GND	Ground

2801 tbl 01

PIN CONFIGURATION

Note: Pin configurations for these modules are currently not available, please consult the factory.

Notes:

1. For valid read operation, no other part may write to the same address location at the same time.
2. For the IDT7MB1044 (2K x 16) version, $P1A_{11}$, $P2A_{11}$, $P3A_{11}$, $P4A_{11}$ must be connected to GND for proper operation of the module.

8

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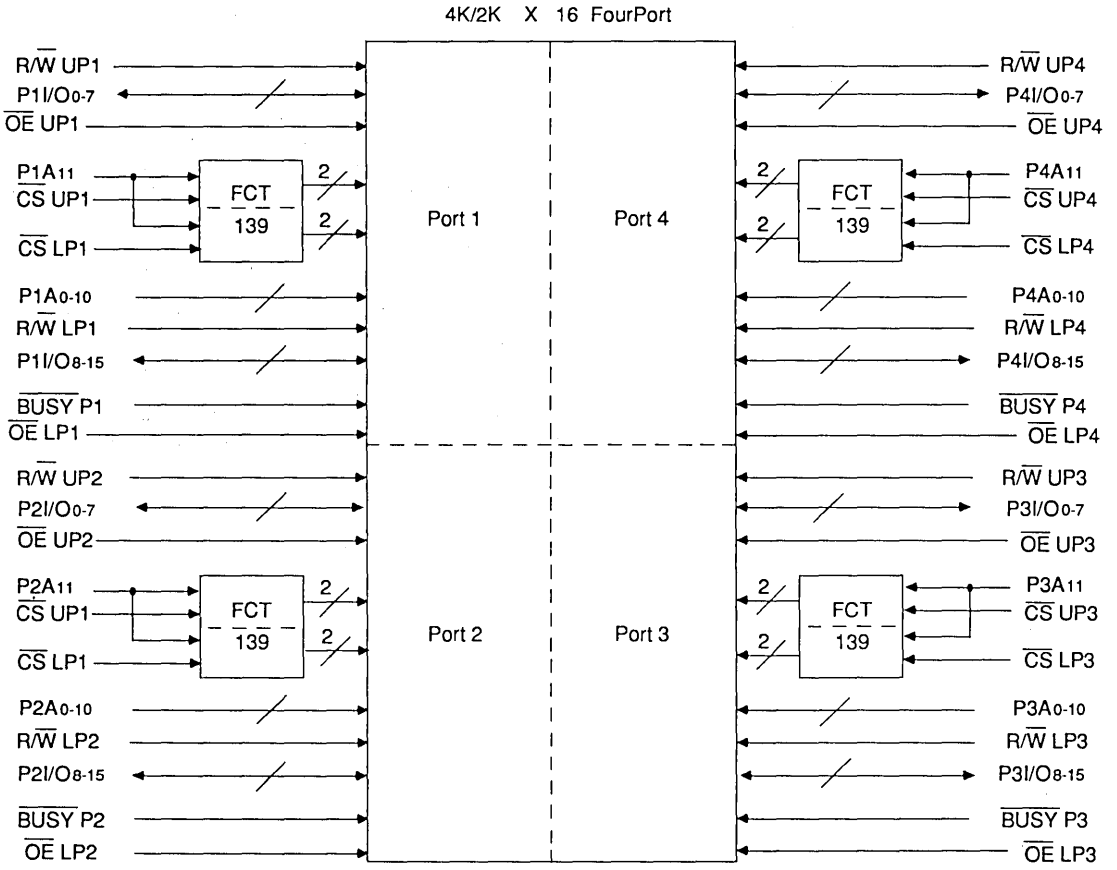
FUNCTIONAL BLOCK DIAGRAM



2801 drw 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to ± 7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	-55 to + 125	°C
TSTG	Storage Temperature	-55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE: 2801 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to + 70°C	0V	5.0V± 10%

2801 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE: 2801 tbl 04

1. VIL (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS

(Vcc = 5.0V ± 10%, TA = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
ILI	Input Leakage Current	Vcc = 5.5V, VIN = 0V to Vcc	—	40	µA
ILO	Output Leakage Current	$\overline{CS}$ = VIH, VOUT = 0V to Vcc	—	10	µA
VOL	Output Low Voltage	IOL = 4mA	—	0.4	V
VOH	Output High	IOH = 4mA	2.4	0.4	V

2801 tbl 05

CAPACITANCE(1) (TA = +25°C, f = 1.0 MHz)

Symbol	Parameter	Test Conditions	IDT7MB1043/1044 Max.	Max.	Unit
CIN1	Input Capacitance	VIN = 0V	12	12	pF
CIN2	Input Capacitance (Data, Address, All Other Controls)	VIN = 0V	40	20	pF
COUT	Output Capacitance (Data)	VOUT = 0V	45	25	pF

NOTE: 2801 tbl 06

1. This parameter is guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS

(Vcc = 5.0V ± 10%, TA = 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7MB1043 Min.	Max.	IDT7MB1044 Min.	Max.	Unit
ICC1	Operating Power Supply Current (All Ports Active)	$\overline{CS}$ ≥ VIL, Outputs Open f = 0	—	750	—	600	mA
ICC2	Dynamic Operating Current	$\overline{CS}$ ≥ VIL, Outputs Open f = fMAX	—	850	—	700	mA
ISB	Standby current (All Ports - TTL Level Inputs)	$\overline{CS}$ = VIH, Outputs Open f = fMAX	—	340	—	170	mA
ISB1	Full Standby Current (All Ports - All CMOS Level Inputs)	All Ports $\overline{CS}$ ≥ Vcc -0.2V VIN ≥ Vcc - 0.2V or VIN ≤ 0.2V, f = 0	—	20	—	10	mA

2801 tbl 07

8

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2801 tbl 08

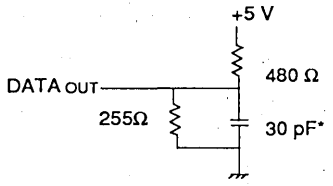


Figure 1. Output Load

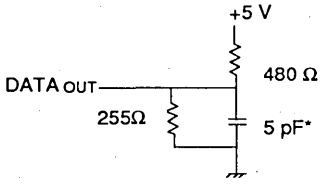


Figure 2. Output Load (for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{WHZ}, t_{OW})

* Including scope and jig.

2801 drw 02

AC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameters	7MB1043S35 7MB1044S35 Min.	Max.	7MB1043S40 7MB1044S40 Min.	Max.	7MB1043S45 7MB1044S45 Min.	Max.	7MB1043S55 7MB1044S55 Min.	Max.	7MB1043S65 7MB1044S65 Min.	Max.	7MB1043S80 7MB1044S80 Min.	Max.	7MB1043S100 7MB1044S100 Min.	Max.	Unit
Read Cycle																
t_{RC}	Read Cycle Time	35	—	40	—	45	—	55	—	65	—	80	—	100	—	ns
t_{AA}	Address Access Time	—	35	—	40	—	45	—	55	—	65	—	80	—	100	ns
t_{ACS}	Chip Select Access Time	—	35	—	40	—	45	—	55	—	65	—	80	—	100	ns
t_{OE}	Output Enable Access Time	—	25	—	25	—	30	—	40	—	50	—	65	—	85	ns
t_{OH}	Output Hold From Address Change	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{CLZ}(2)	Chip Select to Output in Low Z	3	—	5	—	5	—	5	—	5	—	10	—	10	—	ns
t_{OLZ}(2)	Output Enable to Output in Low Z	3	—	5	—	5	—	5	—	5	—	10	—	10	—	ns
t_{CHZ}(2)	Chip Deselect to Output in High Z	20	—	20	—	25	—	25	—	25	—	30	—	30	—	ns
t_{OHZ}(2)	Output Disable to Output in High Z	20	—	20	—	25	—	25	—	25	—	30	—	30	—	ns
t_{PU}(2)	Chip Enable to Power Up Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}(2)	Chip Disable to Power Down Time	—	35	—	55	—	55	—	50	—	70	—	70	—	70	ns

NOTES:

2801 tbl 09

1. Transition is measured by ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is quaranteed by design but not tested.

AC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameters	7MB1043S35 7MB1044S35 Min.	Max.	7MB1043S40 7MB1044S40 Min.	Max.	7MB1043S45 7MB1044S45 Min.	Max.	7MB1043S55 7MB1044S55 Min.	Max.	7MB1043S65 7MB1044S65 Min.	Max.	7MB1043S80 7MB1044S80 Min.	Max.	7MB1043S100 7MB1044S100 Min.	Max.	Unit
Write Cycle																
t_{WC}	Write Cycle Time	35	—	40	—	45	—	55	—	65	—	80	—	100	—	ns
t_{CW}	Chip Select to End of Write	30	—	35	—	35	—	45	—	55	—	70	—	90	—	ns
t_{AW}	Address Valid to End of Write	30	—	35	—	35	—	45	—	55	—	70	—	90	—	ns
t_{AS1}	Address Set-up to $\overline{CS}$ Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{AS2}	Address Set-up to R/$\overline{W}$ Time	5	—	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{WP}	Write Pulse Width	25	—	30	—	35	—	45	—	45	—	45	—	45	—	ns
t_{WR}	Write Recovery Time	5	—	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{DW}	Data Valid to End of Write	20	—	20	—	20	—	20	—	20	—	30	—	30	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}[2]	Write Enabled to Output in High Z	—	18	—	18	—	20	—	20	—	20	—	30	—	30	ns
t_{OW}	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WDD}	Write Pulse to Data Delay	—	50	—	65	—	70	—	80	—	80	—	90	—	100	ns
t_{DDD}	Write Data Valid to Read Data Delay	—	40	—	45	—	45	—	55	—	65	—	80	—	100	ns
Busy Input Timing																
t_{WB}	Write to $\overline{BUSY}$	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$	20	—	20	—	25	—	25	—	25	—	30	—	30	—	ns

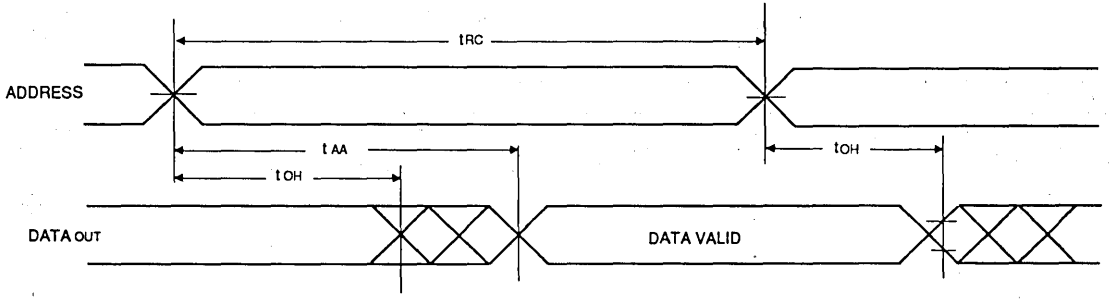
NOTES:

2801 tbl 10

1. Transition is measured by ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is quaranteed by design but not tested.

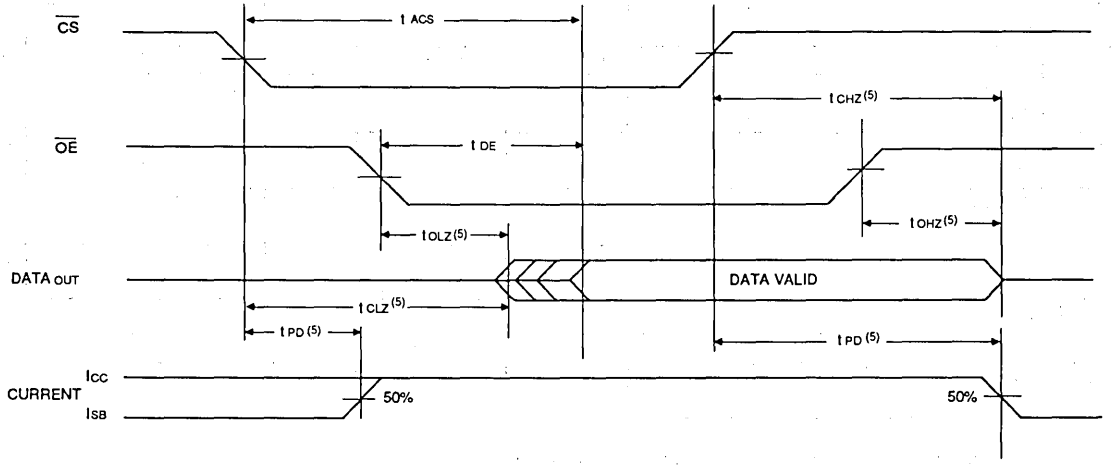
8

TIMING WAVEFORM OF READ CYCLE NO. 1, ANY PORT (1, 2, 4)



2801 drw 03

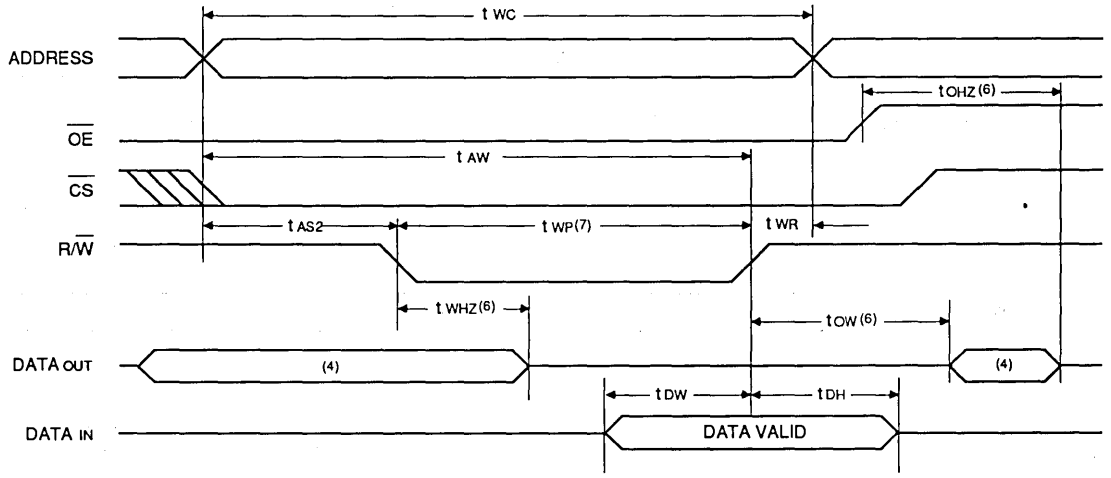
TIMING WAVEFORM OF READ CYCLE NO. 2, ANY PORT (1, 3)



2801 drw 04

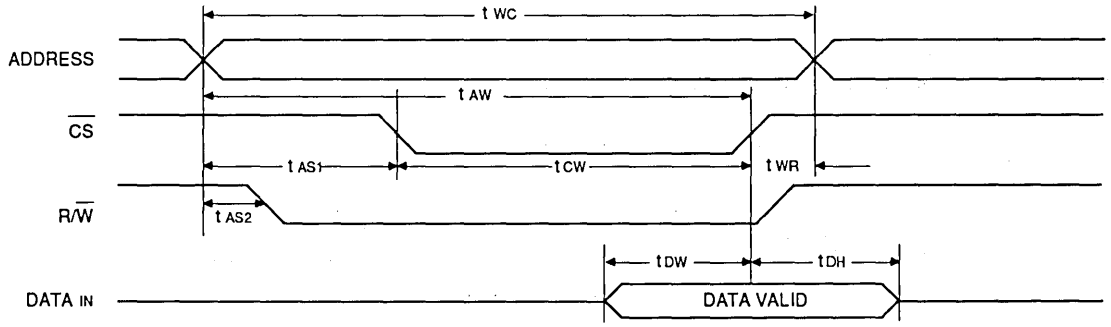
NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled. $\overline{CS} \geq V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} \geq V_{IL}$.
5. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING (1, 2, 3, 7)



2801 drw 05

TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CS}$ CONTROLLED TIMING (1, 2, 3, 5)

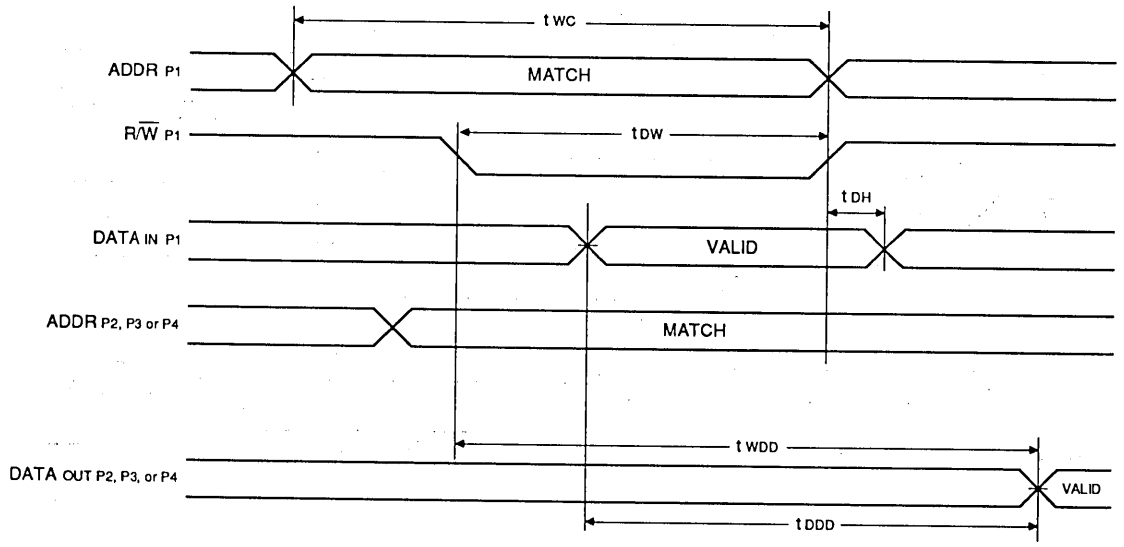


2801 drw 06

NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the ouputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design but not tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the busfor the required tDW. If $\overline{OE}$ is high during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

8

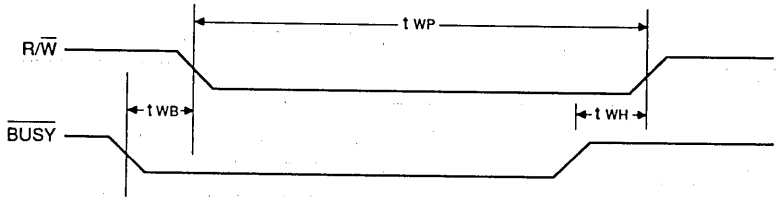
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY (1, 2, 3)



NOTES:
1. Assume $\overline{BUSY}$ input at High and $\overline{CS}$ at Low for the writing port.
2. Write cycle parameters should be adhered to, to ensure proper writing.
3. Device is continuously enabled for any of the reading ports which has its $\overline{OE}$ at Low.

2801 drw 07

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ INPUT



2801 drw 08

FUNCTIONAL DESCRIPTION

The IDT7MB1043/1044 provides four ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by $\overline{CS}$. The $\overline{CS}$ controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{CS}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. READ/WRITE conditions are illustrated in the table below.

READ/WRITE CONTROL

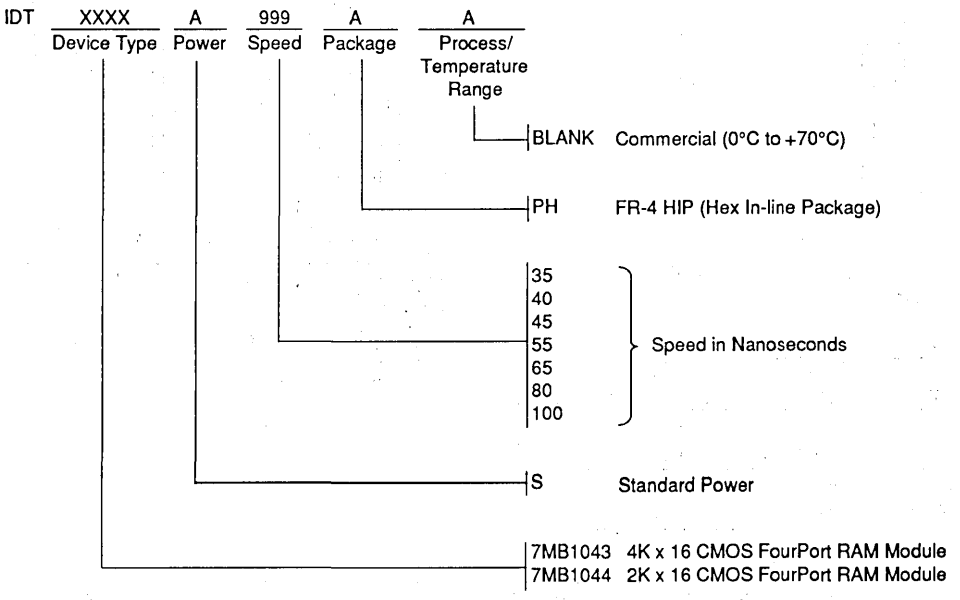
ANY PORT								FUNCTION
$\overline{CS}$	LBYTE	UBYTE	R/$\overline{W}$	$\overline{OE}$	$\overline{BUSY}$	I/O0:7	I/O8:15	
H	X	X	X	X	X	HI-Z	HI-Z	Port Disabled and in Power Down Mode
H	X	X	X	X	X	HI-Z	HI-Z	CSP1 = CSP2 = CSP3 = CSP4 = H Power Down Mode, ISB or ISB1
L	L	L	L	X	H	DATAIN	DATAIN	Write Cycle - Upper & Lower Bytes
L	L	H	L	X	H	DATAIN	HI-Z	Write Cycle - Lower Byte only
L	H	L	L	X	H	HI-Z	DATAIN	Write Cycle - Upper Byte only
X	X	X	L	X	L	HI-Z	HI-Z	Write is Blocked
L	L	L	H	L	X	DATAOUT	DATAOUT	Read Cycle - Upper & Lower Bytes
L	L	H	H	L	X	DATAOUT	HI-Z	Read Cycle - Lower Byte only
L	H	L	H	L	X	HI-Z	DATAOUT	Read Cycle - Upper Byte only
X	X	X	X	H	X	HI-Z	HI-Z	High Impedance Outputs

NOTES:

2801 drw 11

1. H = High, L - Low, X = Don't Care, Z = High Impedance.
2. If $\overline{BUSY}$ = Low, Data is not written.
3. For valid write operation, no more than one port can write to the same address location at the same time.

ORDERING INFORMATION



8

Integrated Device Technology, Inc.

8K X 9 & 16K X 9 CEMOS™ PARALLEL IN-OUT FIFO MODULE

IDT7M205S
IDT7M206S

FEATURES:

- First-In/First-Out memory module
- 8K x 9 organization (IDT7M205S)
- 16K x 9 organization (IDT7M206S)
- High speed: 20ns (max.) access time
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- MASTER/SLAVE multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and Full warning-flags
- High-performance CEMOS technology
- Single 5V (±10%) power supply

DESCRIPTION:

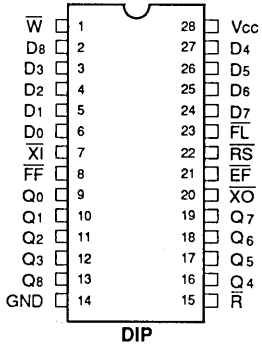
IDT7M205S/206S are FIFO memory modules constructed on a multi-layered ceramic substrate using four IDT7203 (2K x 9) or four IDT7204 (4K x 9) FIFOs in leadless chip carriers. Extremely high speeds are achieved in this fashion due to the use of IDT7203s and IDT7204s fabricated in IDT's high performance CEMOS technology. These devices utilize an algorithm that loads and empties data on a first-In/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The devices have a read/write cycle time of 30ns (min.) for commercial and 40ns (min.) for military temperature ranges.

The devices utilize a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

IDT's Military FIFO modules have semiconductor components manufactued in compliance with the latest revision of MIL-STD-883 Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

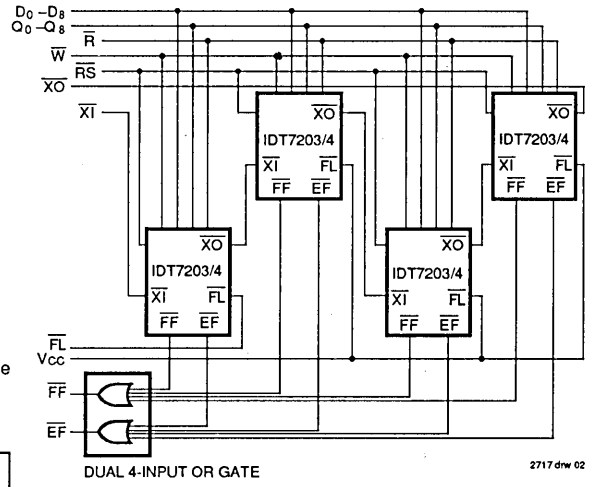
PIN CONFIGURATION[1]



DIP
TOP VIEW

NOTE:
1. For module dimensions, please refer to drawing M1 in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

$\overline{W}$ = WRITE	$\overline{FL}$ = FIRST LOAD	$\overline{XI}$ = EXPANSION IN	$\overline{EF}$ = EMPTY FLAG
$\overline{R}$ = READ	D = DATAIN	$\overline{XO}$ = EXPANSION OUT	Vcc = POWER
$\overline{RS}$ = RESET	Q = DATAOUT	$\overline{FF}$ = FULL FLAG	GND = GROUND

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2717 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}(1)	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}(1)	Input Low Voltage Commercial and Military	—	—	0.8	V

NOTE: 2717 tbl 03

1. 1.5V undershoots are allowed for 10ns once per cycle.

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	40	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	60	pF

NOTE: 2717 tbl 04

1. This parameter is guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C and –55°C to +125°C)

Symbol	Parameter	IDT7M205S(5) IDT7M206S(5) Min.	IDT7M205S(5) IDT7M206S(5) Max.	IDT7M205S(4) IDT7M206S(4) Min.	IDT7M205S(4) IDT7M206S(4) Max.	Unit
$\|I_{LI}\|$(1)	Input Leakage Current (Any Input)	—	5	—	10	µA
$\|I_{OL}\|$(2)	Output Leakage Current	—	10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = –2mA	2.4	—	2.4	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA	—	0.4	—	0.4	V
I_{CC1}(3)	Average Vcc Power Supply Current	—	640	—	350	mA
I_{CC2}(3)	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RST}$ = $\overline{FL}/\overline{RT}$ = V_{IH})	—	60	—	100	mA
I_{CC3}(3)	Power Down Current (All Input = Vcc – 0.2V)	—	32	—	48	mA

NOTES: 2717 tbl 04

1. Measurements with 0.4 ≤ V_{IN} ≤ V_{OUT}.
2. $\overline{R}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ Vcc.
3. Icc measurements are made with outputs open.
4. t_{AA} = 40, 50, 60, 70, 85, 120ns
5. t_{AA} = 20, 25, 30, 35ns

8

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1, 2 & 3

2717 tbl 06

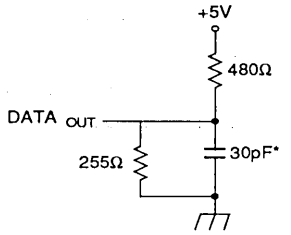


Figure 1. Output Load

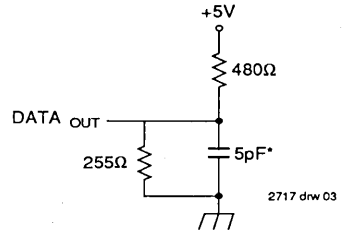


Figure 2. Output Load
(for tRLZ, tWLZ, and tRHZ)

* Includes scope and jig capacitances.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C and –55°C to +125°C)

		7M205S20 7M206S20 (Com'l Only)		7M205S25 7M206S25 (Com'l Only)		7M205S30 7M206S30		7M205S35 7M206S35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
tRC	Read Cycle Time	30	—	35	—	40	—	45	—	ns
tA	Access Time	—	20	—	25	—	30	—	35	ns
tRR	Read Recovery Time	10	—	10	—	10	—	10	—	ns
tRPW(1)	Read Pulse Width	20	—	25	—	30	—	35	—	ns
tRLZ(2)	Read Pulse Low to Data Bus at Low Z	5	—	5	—	5	—	5	—	ns
tWLZ(2)	Write Pulse High to Data Bus at Low Z	5	—	5	—	10	—	10	—	ns
tDV	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	ns
tRHZ(2)	Read Pulse High to Data Bus at High Z	—	13	—	20	—	20	—	20	ns
tWC	Write Cycle Time	30	—	35	—	40	—	45	—	ns
tWPW(1)	Write Pulse Width	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	10	—	10	—	10	—	10	—	ns
tDS	Data Set-up Time	15	—	18	—	18	—	20	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tRSC	Reset Cycle Time	30	—	35	—	40	—	45	—	ns
tRS(1)	Reset Pulse Width	20	—	25	—	30	—	35	—	ns
tRSR	Reset Recovery Time	10	—	10	—	10	—	10	—	ns
tEFL	Reset to Empty Flag Low	—	30	—	35	—	40	—	45	ns
tREF	Read Low to Empty Flag Low	—	20	—	25	—	30	—	35	ns
tRFF	Read High to Full Flag High	—	23	—	25	—	30	—	35	ns
tWEF	Write High to Empty Flag High	—	23	—	25	—	30	—	35	ns
tWFF	Write Low to Full Flag Low	—	20	—	25	—	30	—	35	ns

NOTES:
1. Pulse widths less than minimum value are not allowed.
2. This parameter is guaranteed by design but not tested.

2717 tbl 05

AC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V ±10%, TA = 0°C to +70°C and –55°C to +125°C)

Symbol	Parameter	7M205S40 7M206S40		7M205S50 7M206S50		7M205S60 7M206S60		7M205S70 7M206S70		7M205S85 7M206S85		7M205S120 7M206S120		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tRC	Read Cycle Time	50	—	65	—	75	—	85	—	105	—	140	—	ns
tA	Access Time	—	40	—	50	—	60	—	70	—	85	—	120	ns
tRR	Read Recovery Time	10	—	15	—	15	—	15	—	20	—	20	—	ns
tRPW(1)	Read Pulse Width	40	—	50	—	60	—	70	—	85	—	120	—	ns
tRLZ(2)	Read Pulse Low to Data Bus at Low Z	5	—	10	—	10	—	10	—	10	—	10	—	ns
tWLZ(2)	Write Pulse High to Data Bus at Low Z	10	—	15	—	15	—	15	—	20	—	20	—	ns
tDV	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	5	—	5	—	ns
tRHZ(2)	Read Pulse High to Data Bus at High Z	—	25	—	30	—	30	—	30	—	30	—	35	ns
tWC	Write Cycle Time	50	—	65	—	75	—	85	—	105	—	140	—	ns
tWPW(1)	Write Pulse Width	40	—	50	—	60	—	70	—	85	—	120	—	ns
tWR	Write Recovery Time	10	—	15	—	15	—	15	—	20	—	20	—	ns
tDS	Data Set-up Time	20	—	30	—	30	—	30	—	40	—	40	—	ns
tDH	Data Hold Time	0	—	5	—	5	—	10	—	10	—	10	—	ns
tRSC	Reset Cycle Time	50	—	65	—	75	—	85	—	105	—	140	—	ns
tRS(1)	Reset Pulse Width	40	—	50	—	60	—	70	—	85	—	120	—	ns
tRSR	Reset Recovery Time	10	—	15	—	15	—	15	—	20	—	20	—	ns
tEFL	Reset to Empty Flag Low	—	55	—	65	—	75	—	85	—	105	—	140	ns
tREF	Read Low to Empty Flag Low	—	40	—	50	—	60	—	70	—	85	—	120	ns
tRFF	Read High to Full Flag High	—	40	—	50	—	60	—	70	—	85	—	120	ns
tWEF	Write High to Empty Flag High	—	40	—	50	—	60	—	70	—	85	—	120	ns
tWFF	Write Low to Full Flag Low	—	40	—	50	—	60	—	70	—	85	—	120	ns

NOTES:
1. Pulse widths less than minimum value are not allowed.
2. This parameter is guaranteed by design but not tested.

2717 tbl 08

8

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D_0-D_8)
Data Inputs for 9-bit wide data path.

CONTROLS:

RESET ($\overline{RS}$)
Reset is accomplished whenever the RESET ($\overline{RS}$) input is taken to a low state. During RESET, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. Both the READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) inputs must be in the high state during reset.

WRITE ENABLE ($\overline{W}$)
A write cycle is initiated on the falling edge of this input if the FULL FLAG ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect the the rising edge of the WRITE ENABLE ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

To prevent data overflow, the FULL FLAG ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the FULL FLAG ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin.

READ ENABLE ($\overline{R}$)
A read cycle is initiated on the falling edge of the READ ENABLE ($\overline{R}$) provided the EMPTY FLAG ($\overline{EF}$) is not set. The data is accessed on a first-in/first-out basis independent of any ongoing write operations. After READ ENABLE ($\overline{R}$) goes high, the Data Outputs (Q_0 through Q_8) will return to a high impedance condition until the next READ operation. When all the data has been read from the FIFO, the EMPTY FLAG ($\overline{EF}$) will go low, inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the EMPTY FLAG ($\overline{EF}$) will go high after t_{WEF} and a valid READ can then begin.

FIRST LOAD ($\overline{FL}$)
This pin is grounded to indicate that it is the first device. In the multiple module (depth expansion mode) application, this pin on the rest of devices should connect to V_{CC} for proper operation.

EXPANSION IN ($\overline{XI}$)
EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous (in depth expansion) or same device for proper applications.

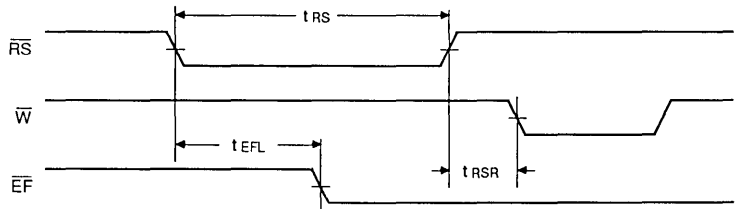
OUTPUTS:

FULL FLAG ($\overline{FF}$)
The FULL FLAG ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location from the read pointer, indicating that the device is full. If the read pointer is not moved after RESET ($\overline{RS}$), the FULL FLAG ($\overline{FF}$) will go low after 8,192 writes for the IDT7M205 and 16,384 writes for the IDT7M206.

EXPANSION OUT ($\overline{XO}$)
EXPANSION OUT ($\overline{XO}$) is connected to the EXPANSION IN ($\overline{XI}$) of the same device (single device mode) or the EXPANSION IN ($\overline{XI}$) of the next device (multiple device, depth expansion mode) for proper operation. This output acts as a signal to the next device by providing a pulse to the next device when the current device reaches the last location of memory.

DATA OUTPUTS (Q_0-Q_8)
Data outputs for a 9-bit wide data. This output is in a high impedance condition whenever READ ($\overline{R}$) is in a high state.

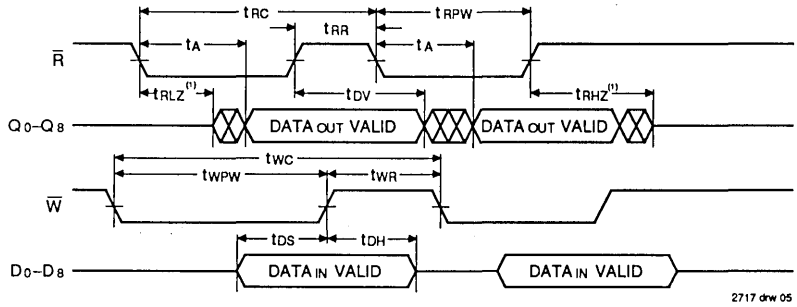
TIMING WAVEFORM OF RESET CYCLE(1,2)



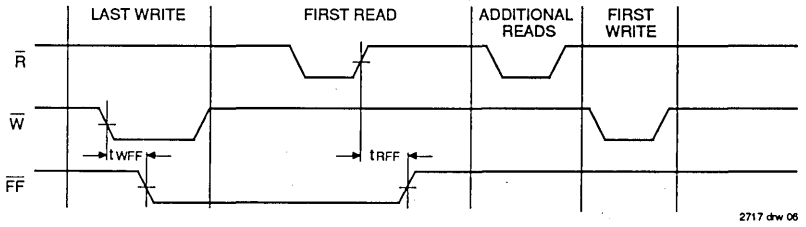
2717 drw 04

NOTES:
1. $t_{RSC} = t_{RS} + t_{RSR}$
2. $\overline{W}$ and $\overline{R}$ = V_{IH} during RESET.

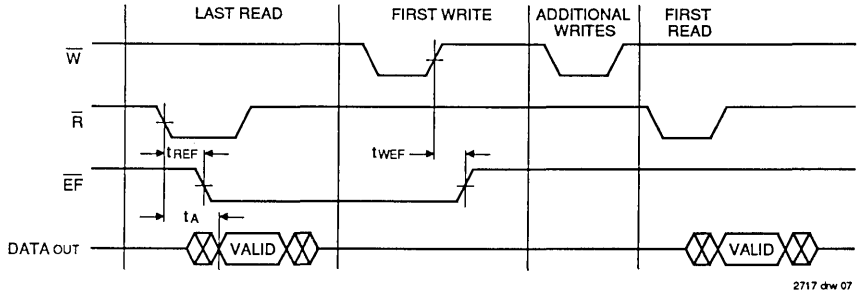
TIMING WAVEFORM FOR ASYNCHRONOUS WRITE AND READ OPERATION



TIMING WAVEFORM OF THE FULL FLAG FROM LAST WRITE TO FIRST READ



TIMING WAVEFORM OF THE EMPTY FLAG FROM LAST READ TO FIRST WRITE



NOTE:
1. This parameter is guaranteed by design but not tested.

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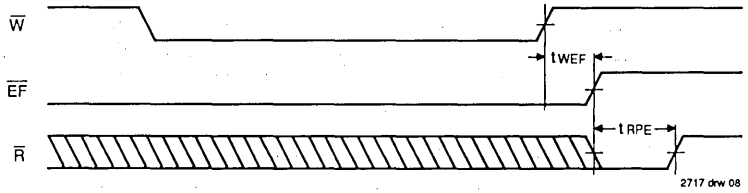
TIMING WAVEFORM FOR THE EMPTY FLAG

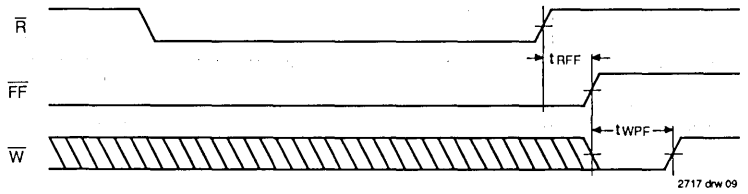
t_{RPE} EFFECTIVE READ PULSE WIDTH AFTER FULL FLAG HIGH (1)



NOTE:
1. (t_{RPE} = t_{RPW})

TIMING WAVEFORM FOR THE FULL FLAG

t_{RPE} EFFECTIVE READ PULSE WIDTH AFTER FULL FLAG HIGH (1)



NOTE:
1. (t_{WPF} = t_{WPW})

OPERATING MODES

SINGLE DEVICE MODE

A single IDT7M205/206 may be used when the application requirements are for 8,192/16,384 words or less. The IDT7M205/206 is in a Single Device Configuration when the EXPANSION IN ($\overline{XI}$) control input is connected to the EXPANSION OUT ($\overline{XO}$) of the device and the FIRST LOAD ($\overline{FL}$) control pin is grounded (see Figure 8).

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 9 demonstrates an 18-bit word width by using two IDT7M205/206s. Any word width can be attained by adding additional IDT7M205/206s.

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT7M205/206 can easily be adapted to applications when the requirements are for greater than 8,192/16,384 words. Figure 10 demonstrates Depth Expansion using three IDT7M205/206s. Any depth can be attained by adding additional IDT7M205/206s. The IDT7M205/206 operate in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the FIRST LOAD ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The EXPANSION OUT ($\overline{XO}$) pin of each device must be tied to the EXPANSION IN ($\overline{XI}$) pin of the next device. (See Figure 10.)
4. External logic is needed to generate a composite FULL FLAG ($\overline{FF}$) and EMPTY FLAG ($\overline{EF}$). This requires the logical ANDing of all $\overline{EF}$s and logical ANDing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). (See Figure 10.)

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see Figure 11).

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT7M205/206s as shown in Figure 12. Care must be taken to assure that the appropriate flag is monitored by each system (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted with the IDT7M205/206: a read flow-through mode and write flow-through mode. For the read flow-through mode (Figure 13), the FIFO permits a reading of a single word of data immediately after writing one word of data into the completely empty FIFO.

In the write flow-through mode (Figure 14), the FIFO permits a writing of a single word of data immediately after reading one word of data from a completely full FIFO.

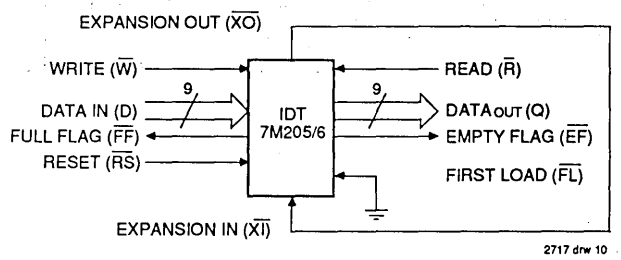


Figure 8. Block Diagram of Single IDT7M205/206 FIFO

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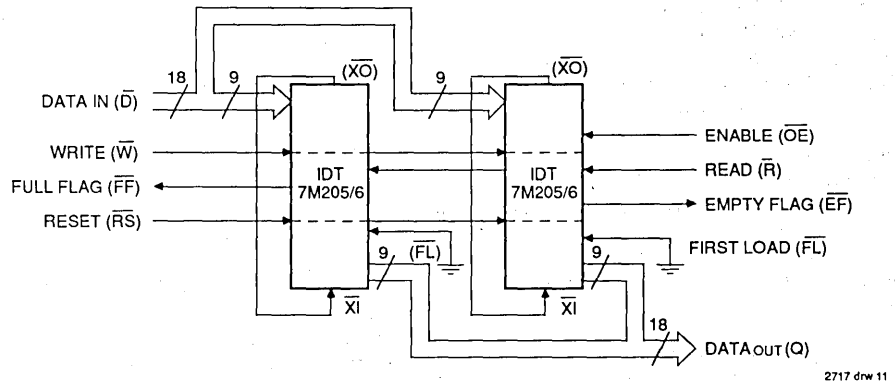

NOTE:
1. Flag detection is accomplished by monitoring the FF and EF signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 9. Block Diagram of 8,192 x 18/16,384 x 18 FIFO Memory Used In Width Expansion Mode

TRUTH TABLES
TABLE I—RESET
Single Device Configuration/Width Expansion Mode

Mode	Inputs		Internal Status		Outputs	
	RS	XI	Read Pointer	Write Pointer	EF	FF
Reset	0	0	Location Zero	Location Zero	0	1
Read/Write	1	0	Increment(1)	Increment(1)	X	X

NOTE: 2717 tbl 08
1. Pointer will increment if flag is High.

TABLE II—RESET AND FIRST LOAD TRUTH TABLE
Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	RS	FL	XI	Read Pointer	Write Pointer	EF	FF
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTE: 2717 tbl 09
1. XI is connected to XO of previous device. See Figure 10.
2. RS = Reset Input FL = First Load, EF = Empty Flag Output, FF = Flag Full Output, XI = Expansion Input.

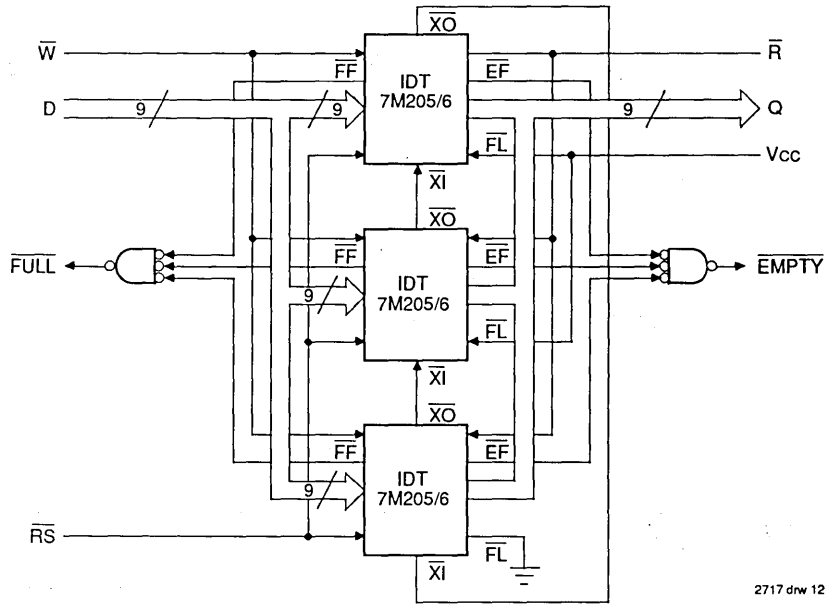

Figure 10. Block Diagram of 24,576 x 9/49,152 x 9 FIFO Memory (Depth Expansion)

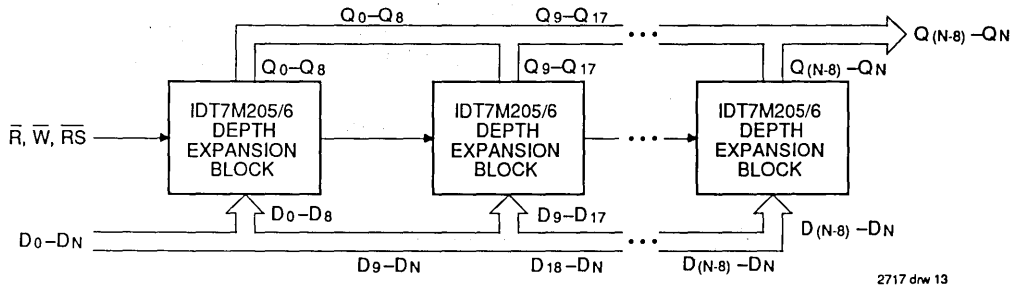

Figure 11. Compound FIFO Expansion

NOTES:
1. For depth expansion block see DEPTH EXPANSION Section and Figure 10.
2. For Flag detection see WIDTH EXPANSION Section and Figure 9.

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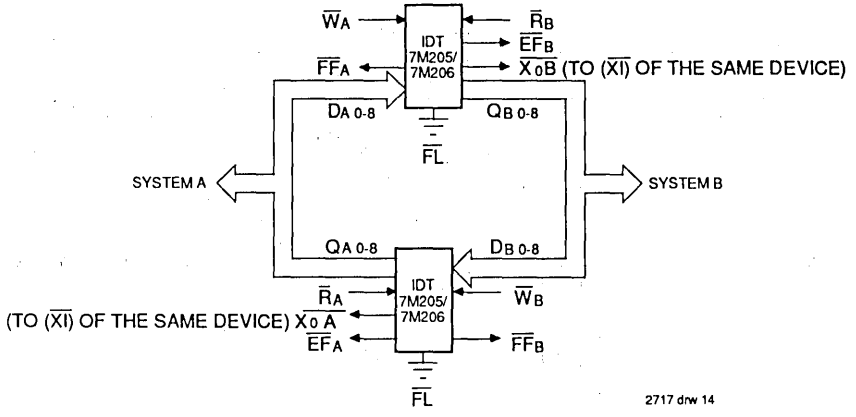


Figure 12. Bidirectional FIFO Mode

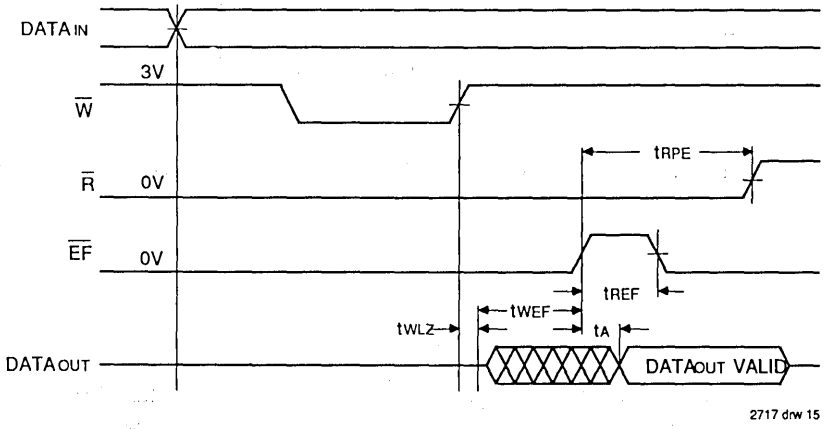


Figure 13. Read Data Flow-Through Mode

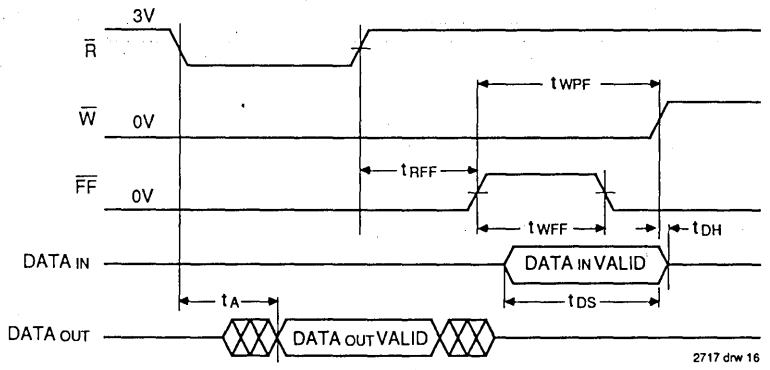
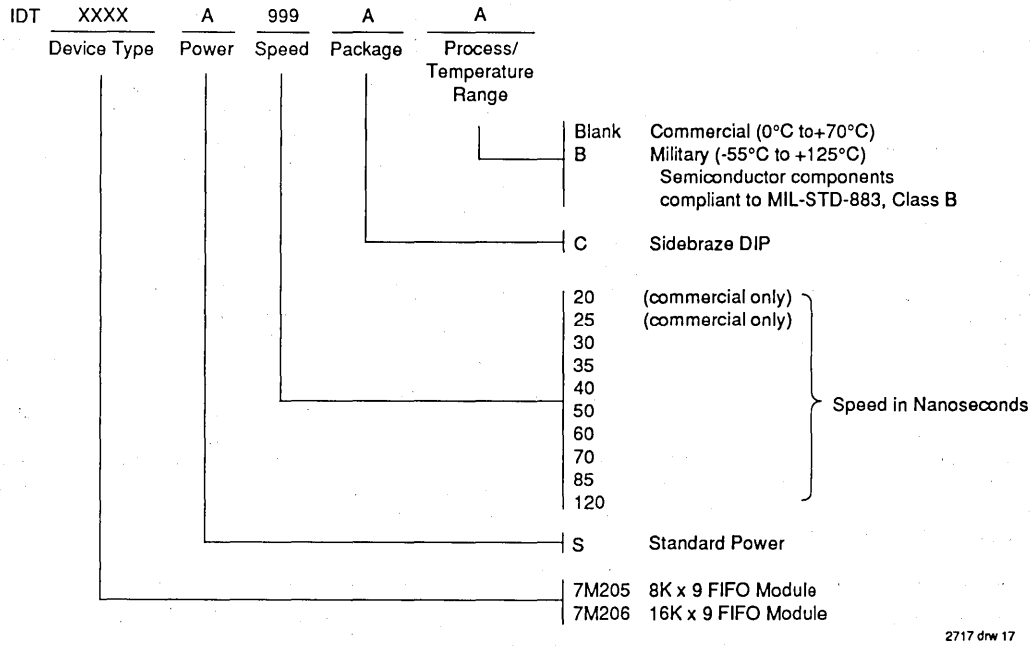


Figure 14. Write Data Flow-Through Mode

ORDERING INFORMATION



8

Integrated Device Technology, Inc.

8K x 9 & 16K x 9 CMOS PARALLEL IN-OUT FIFO MODULE

IDT7MP2005
IDT7MP2011

FEATURES:

- First-In/First-Out memory module
- 8K x 9 organization (IDT7MP2005)
- 16K x 9 organization (IDT7MP2011)
- High speed: 20ns (max.) access time
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- MASTER/SLAVE multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and Full warning-flags
- High-performance CEMOS™ technology
- Single 5V (±10%) power supply

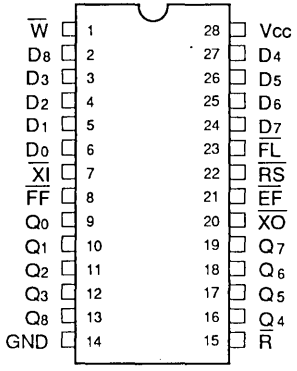
DESCRIPTION:

IDT7MP2005/7MP2011 are FIFO memory modules constructed on multi-layered epoxy laminate (FR-4) substrate by mounting two IDT7204 (4K x 9) or IDT7205 (8K x 9) FIFOs in plastic leaded chip carriers. Extremely high speeds are achieved in this fashion due to the use of IDT7203s and IDT7204s fabricated in IDT's high performance CEMOS technology. These devices utilize an algorithm that loads and empties data on a first-In/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The devices have a read/write cycle time of 30ns (min.) for commercial temperature ranges.

The devices utilize a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

PIN CONFIGURATION[1]



DSIP
TOP VIEW

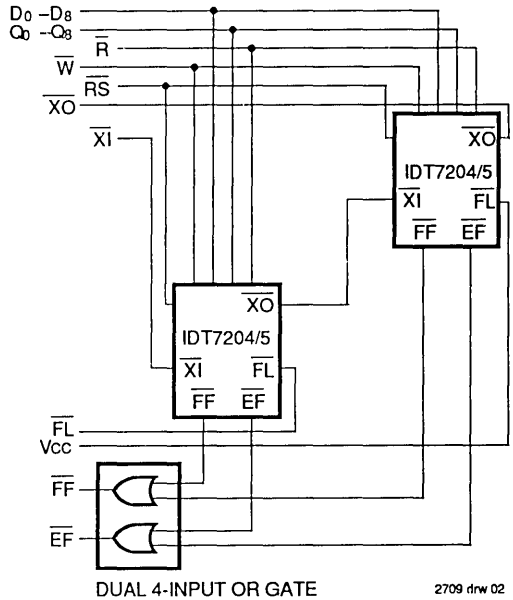
2709 drw 01

NOTE:
1. For module dimensions, please refer to drawing M34 in the packaging section.

PIN NAMES

$\overline{W}$ = WRITE	$\overline{FL}$ = FIRST LOAD	$\overline{XI}$ = EXPANSION IN	$\overline{EF}$ = EMPTY FLAG
$\overline{R}$ = READ	D = DATAIN	$\overline{XO}$ = EXPANSION OUT	Vcc = POWER
$\overline{RS}$ = RESET	Q = DATAOUT	$\overline{FF}$ = FULL FLAG	GND = GROUND

FUNCTIONAL BLOCK DIAGRAM



DUAL 4-INPUT OR GATE

2709 drw 02

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Unit
VTERM	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	−55 to +125	°C
TSTG	Storage Temperature	−55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE: 2709 tbl 02
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vccc	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH(1)	Input High Voltage Commercial	2.0	—	—	V
VIL(1)	Input Low Voltage Commercial	—	—	0.8	V

NOTE: 2709 tbl 03
1. 1.5V undershoots are allowed for 10ns once per cycle.

CAPACITANCE (TA = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	20	pF
COUT	Output Capacitance	VOUT = 0V	25	pF

NOTE: 2709 tbl 04
1. This parameter is guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V ±10%, TA = 0°C to +70°C)

Symbol	Parameter	IDT7MP2005(4) Min.	IDT7MP2005(4) Max.	IDT7MP2011(5) Min.	IDT7MP2011(5) Max.	IDT7MP2005(6) Min.	IDT7MP2005(6) Max.	Unit
|ILI|(1)	Input Leakage Current (Any Input)	—	20	—	20	—	20	µA
|ILO|(2)	Output Leakage Current	—	20	—	20	—	20	µA
VOH	Output Logic "1" Voltage IOUT = −2mA	2.4	—	2.4	—	2.4	—	V
VOL	Output Logic "0" Voltage IOUT = 8mA	—	0.4	—	0.4	—	0.4	V
ICC1(3)	Operating Current	—	320	—	300	—	132	mA
ICC2(3)	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = VIH)	—	30	—	24	—	24	mA
ICC3(3)	Power Down Current (All Input = VCC − 0.2V)	—	16	—	16	—	16	mA

NOTES: 2709 tbl 04
1. Measurements with 0.4 ≤ VIN ≤ VOUT.
2. $\overline{R}$ ≥ VIH, 0.4 ≤ VOUT ≤ VCC.
3. Icc measurements are made with outputs open.
4. tAA = 20, 25, 30, 35ns.
5. tAA = 30, 35, 40, 50, 60, 70, 85, 120ns.
6. tAA = 40, 50, 60, 70, 85, 120ns.

8

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1, 2 & 3

2709 tbl 06

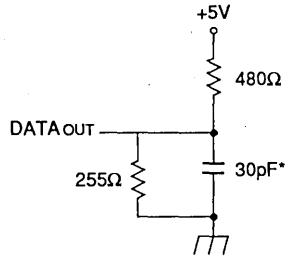
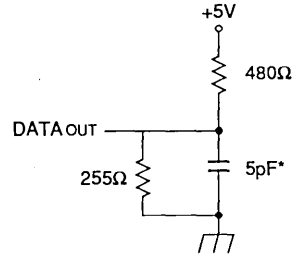


Figure 1. Output Load



2709 drw 03

Figure 2. Output Load (for tRLZ, tWLZ, and tRHZ)

* Includes scope and jig capacitances.

AC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V±10%, TA = 0°C to +70°C)

Symbol	Parameter	7MP2005S20 Min.	7MP2005S20 Max.	7MP2005S25 Min.	7MP2005S25 Max.	7MP2005S30 7MP2011S30 Min.	7MP2005S30 7MP2011S30 Max.	7M205SS35 7M2011S35 Min.	7M205SS35 7M2011S35 Max.	Unit
tRC	Read Cycle Time	30	—	35	—	40	—	45	—	ns
tA	Access Time	—	20	—	25	—	30	—	35	ns
tRR	Read Recovery Time	10	—	10	—	10	—	10	—	ns
tRPW(1)	Read Pulse Width	20	—	25	—	30	—	35	—	ns
tRLZ(2)	Read Pulse Low to Data Bus at Low Z	5	—	5	—	5	—	5	—	ns
tWLZ(2)	Write Pulse High to Data Bus at Low Z	5	—	5	—	10	—	10	—	ns
tDV	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	ns
tRHZ(2)	Read Pulse High to Data Bus at High Z	—	13	—	20	—	20	—	20	ns
tWC	Write Cycle Time	30	—	35	—	40	—	45	—	ns
tWPW(1)	Write Pulse Width	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	10	—	10	—	10	—	10	—	ns
tDS	Data Set-up Time	15	—	18	—	18	—	20	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tRSC	Reset Cycle Time	30	—	35	—	40	—	45	—	ns
tRS(1)	Reset Pulse Width	20	—	25	—	30	—	35	—	ns
tRSR	Reset Recovery Time	10	—	10	—	10	—	10	—	ns
tEFL	Reset to Emtpy Flag Low	—	30	—	35	—	40	—	45	ns
tREF	Read Low to Emtpy Flag Low	—	20	—	25	—	30	—	35	ns
tRFF	Read High to Full Flag High	—	23	—	25	—	30	—	35	ns
tWEF	Write High to Empty Flag High	—	23	—	25	—	30	—	35	ns
tWFF	Write Low to Full Flag Low	—	20	—	25	—	30	—	35	ns

NOTES:

2709 tbl 05

1. Pulse widths less than minimum value are not allowed.
2. This parameter is guaranteed by design but not tested.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V±10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP2005S40 7MP2011S40		7MP2005S50 7MP2011S50		7MP2005S60 7MP2011S60		7MP2005S70 7MP2011S70		7MP2005S85 7MP2011S85		7MP2005S120 7MP2011S120		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	50	—	65	—	75	—	85	—	105	—	140	—	ns
t_A	Access Time	—	40	—	50	—	60	—	70	—	85	—	120	ns
t_{RR}	Read Recovery Time	10	—	15	—	15	—	15	—	20	—	20	—	ns
t_{RPW}[1]	Read Pulse Width	40	—	50	—	60	—	70	—	85	—	120	—	ns
t_{RLZ}[2]	Read Pulse Low to Data Bus at Low Z	5	—	10	—	10	—	10	—	10	—	10	—	ns
t_{WLZ}[2]	Write Pulse High to Data Bus at Low Z	10	—	15	—	15	—	15	—	20	—	20	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{RHZ}[2]	Read Pulse High to Data Bus at High Z	—	25	—	30	—	30	—	30	—	30	—	35	ns
t_{WC}	Write Cycle Time	50	—	65	—	75	—	85	—	105	—	140	—	ns
t_{WPW}[1]	Write Pulse Width	40	—	50	—	60	—	70	—	85	—	120	—	ns
t_{WR}	Write Recovery Time	10	—	15	—	15	—	15	—	20	—	20	—	ns
t_{DS}	Data Set-up Time	20	—	30	—	30	—	30	—	40	—	40	—	ns
t_{DH}	Data Hold Time	0	—	5	—	5	—	10	—	10	—	10	—	ns
t_{RSC}	Reset Cycle Time	50	—	65	—	75	—	85	—	105	—	140	—	ns
t_{RS}[1]	Reset Pulse Width	40	—	50	—	60	—	70	—	85	—	120	—	ns
t_{RSR}	Reset Recovery Time	10	—	15	—	15	—	15	—	20	—	20	—	ns
t_{EFL}	Reset to Emtpy Flag Low	—	50	—	65	—	75	—	85	—	105	—	140	ns
t_{REF}	Read Low to Emtpy Flag Low	—	40	—	50	—	60	—	70	—	85	—	120	ns
t_{RFF}	Read High to Full Flag High	—	40	—	50	—	60	—	70	—	85	—	120	ns
t_{WEF}	Write High to Empty Flag High	—	40	—	50	—	60	—	70	—	85	—	120	ns
t_{WFF}	Write Low to Full Flag Low	—	40	—	50	—	60	—	70	—	85	—	120	ns

2709 tbl 08

NOTES:
1. Pulse widths less than minimum value are not allowed.
2. This parameter is guaranteed by design but not tested.

8

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D_0-D_8)
Data Inputs for 9-bit wide data path.

CONTROLS:

RESET ($\overline{RS}$)
Reset is accomplished whenever the RESET ($\overline{RS}$) input is taken to a low state. During RESET, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. Both the READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) inputs must be in the high state during reset.

WRITE ENABLE ($\overline{W}$)
A write cycle is initiated on the falling edge of this input if the FULL FLAG ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect the the rising edge of the WRITE ENABLE ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

To prevent data overflow, the FULL FLAG ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the FULL FLAG ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin.

READ ENABLE ($\overline{R}$)
A read cycle is initiated on the falling edge of the READ ENABLE ($\overline{R}$) provided the EMPTY FLAG ($\overline{EF}$) is not set. The data is accessed on a first-in/first-out basis independent of any ongoing write operations. After READ ENABLE ($\overline{R}$) goes high, the Data Outputs (Q_0 through Q_8) will return to a high impedance condition until the next READ operation. When all the data has been read from the FIFO, the EMPTY FLAG ($\overline{EF}$) will go low, inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the EMPTY FLAG ($\overline{EF}$) will go high after t_{WEF} and a valid READ can then begin.

FIRST LOAD ($\overline{FL}$)
This pin is grounded to indicate that it is the first device. In the multiple module (depth expansion mode) application, this pin on the rest of devices should connect to Vcc for proper operation.

EXPANSION IN ($\overline{XI}$)
EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous (in depth expansion) or same device for proper applications.

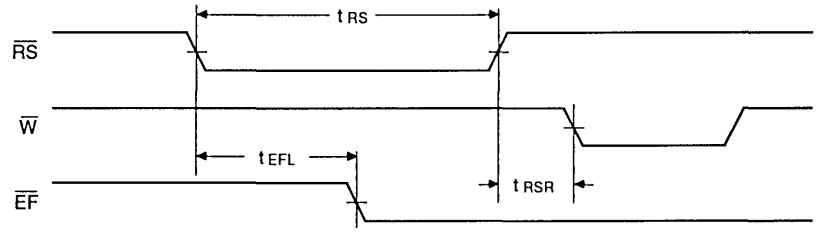
OUTPUTS:

FULL FLAG ($\overline{FF}$)
The FULL FLAG ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location from the read pointer, indicating that the device is full. If the read pointer is not moved after RESET ($\overline{RS}$), the FULL FLAG ($\overline{FF}$) will go low after 8,192 writes for the IDT7MP2005 and 16,384 writes for the IDT7MP2011.

EXPANSION OUT ($\overline{XO}$)
EXPANSION OUT ($\overline{XO}$) is connected to the EXPANSION IN ($\overline{XI}$) of the same device (single device mode) or the EXPANSION IN ($\overline{XI}$) of the next device (multiple device, depth expansion mode) for proper operation. This output acts as a signal to the next device by providing a pulse to the next device when the current device reaches the last location of memory.

DATA OUTPUTS (Q_0-Q_8)
Data outputs for a 9-bit wide data path. This output is in a high impedance condition whenever READ ($\overline{R}$) is in a high state.

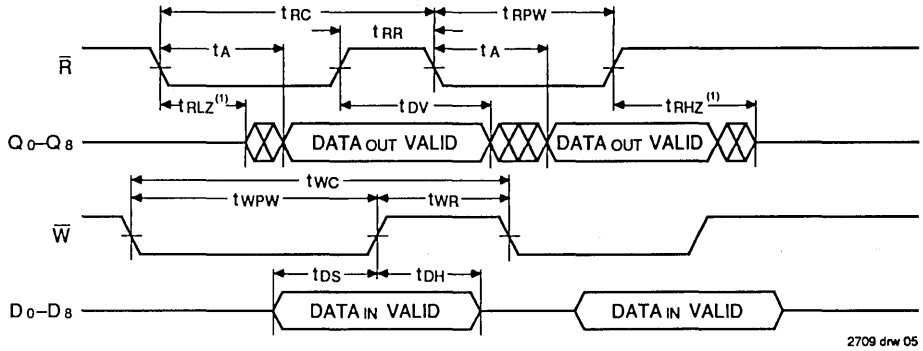
TIMING WAVEFORM OF RESET CYCLE(1,2)



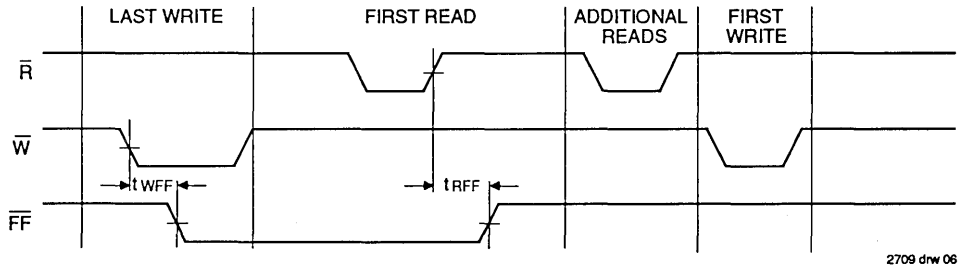
2709 drw 04

NOTES:
1. $t_{RSC} = t_{RS} + t_{RSR}$
2. $\overline{W}$ and $\overline{R}$ = V_{IH} during RESET.

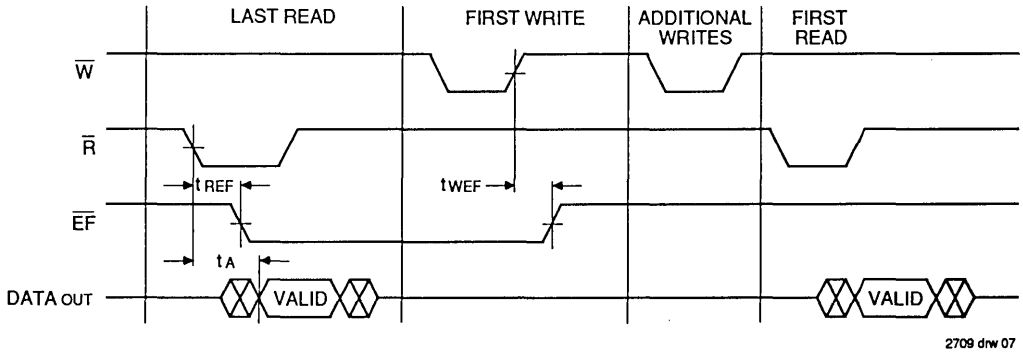
TIMING WAVEFORM OF ASYNCHRONOUS WRITE AND READ OPERATION



TIMING WAVEFORM FOR THE FULL FLAG FROM LAST WRITE TO FIRST READ



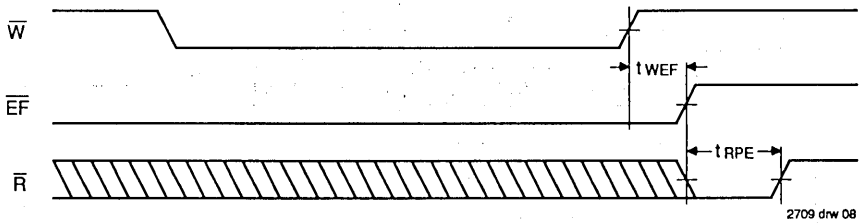
TIMING WAVEFORM FOR THE EMPTY FLAG FROM LAST READ TO FIRST WRITE



NOTE:
1. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF THE EMPTY FLAG CYCLE

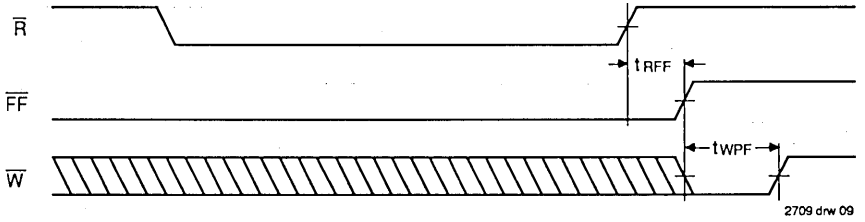
t_{RPE} EFFECTIVE READ PULSE WIDTH AFTER FULL FLAG HIGH (1)



NOTE:
1. (t_{RPE} = t_{RPW})

TIMING WAVEFORM OF THE FULL FLAG CYCLE

t_{RPE} EFFECTIVE READ PULSE WIDTH AFTER FULL FLAG HIGH (1)



NOTE:
1. (t_{WPF} = t_{WPW})

OPERATING MODES

SINGLE DEVICE MODE

A single IDT7MP2005/2011 may be used when the application requirements are for 8,192/16,384 words or less. The IDT7MP2005/2011 is in a Single Device Configuration when the EXPANSION IN ($\overline{XI}$) control input is connected to the EXPANSION OUT ($\overline{XO}$) of the device and the FIRST LOAD ($\overline{FL}$) control pin is grounded (see Figure 8).

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 9 demonstrates an 18-bit word width by using two IDT7MP2005/2011. Any word width can be attained by adding additional IDT7MP2005/2011s.

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT7MP2005/2011 can easily be adapted to applications when the requirements are for greater than 8,192/16,384 words. Figure 10 demonstrates Depth Expansion using three IDT7MP2005/2011. Any depth can be attained by adding additional IDT7MP2005/2011s. The IDT7MP2005/2011 operate in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the FIRST LOAD ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The EXPANSION OUT ($\overline{XO}$) pin of each device must be tied to the EXPANSION IN ($\overline{XI}$) pin of the next device. (See Figure 10.)
4. External logic is needed to generate a composite FULL FLAG ($\overline{FF}$) and EMPTY FLAG ($\overline{EF}$). This requires the logical ANDing of all $\overline{EF}$s and logical ANDing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). (See Figure 10.)

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straight forward manner to achieve large FIFO arrays. (See Figure 11.)

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of READ and WRITE operations) can be achieved by pairing IDT7MP2005/2011s as shown in Figure 12. Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted with the IDT7MP2005/2011: a read flow-through mode and write flow-through mode. For the read flow-through mode (Figure 13), the FIFO permits a reading of a single word of data immediately after writing one word of data into the completely empty FIFO.

In the write flow-through mode (Figure 14), the FIFO permits a writing of a single word of data immediately after reading one word of data from a completely full FIFO.

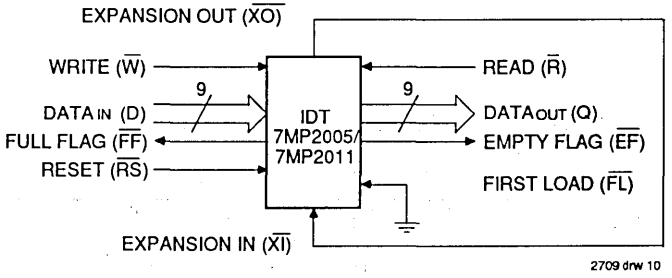
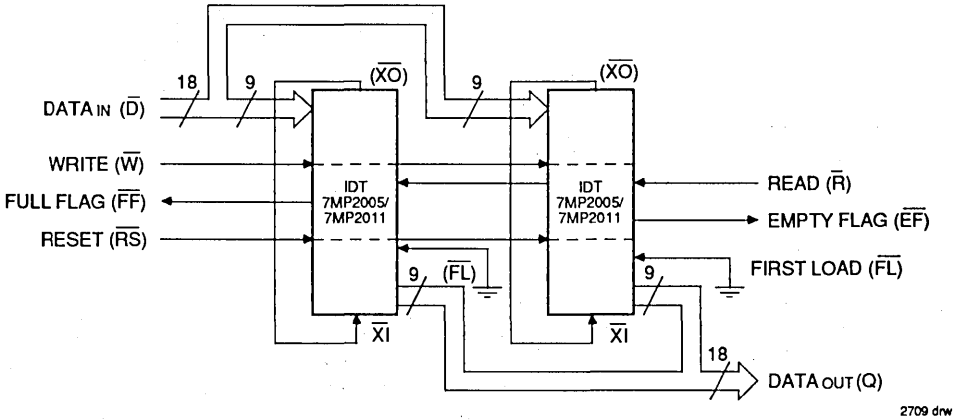


Figure 8. Block Diagram of Single IDT7MP2005/7MP2011 FIFO



NOTE:
1. Flag detection is accomplished by monitoring the FF and EF signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 9. Block Diagram of 8,192 x 18/16,384 x 18 FIFO Memory Used in Width Expansion Mode

TRUTH TABLES
TABLE I—RESET
Single Device Configuration/Width Expansion Mode

Mode	Inputs		Internal Status		Outputs	
	RS	XI	Read Pointer	Write Pointer	EF	FF
Reset	0	0	Location Zero	Location Zero	0	1
Read/Write	1	0	Increment(1)	Increment(1)	X	X

NOTE: 2709 tbl 08
1. Pointer will increment if flag is High.

TABLE II—RESET AND FIRST LOAD TRUTH TABLE
Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	RS	FL	XI	Read Pointer	Write Pointer	EF	FF
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTE: 2709 tbl 09
1. XI is connected to XO of previous device. See Figure 10.
2. RS = Reset Input, FL = First Load, EF = Empty Flag Output, FF = Flag Full Output, XI = Expansion Input.

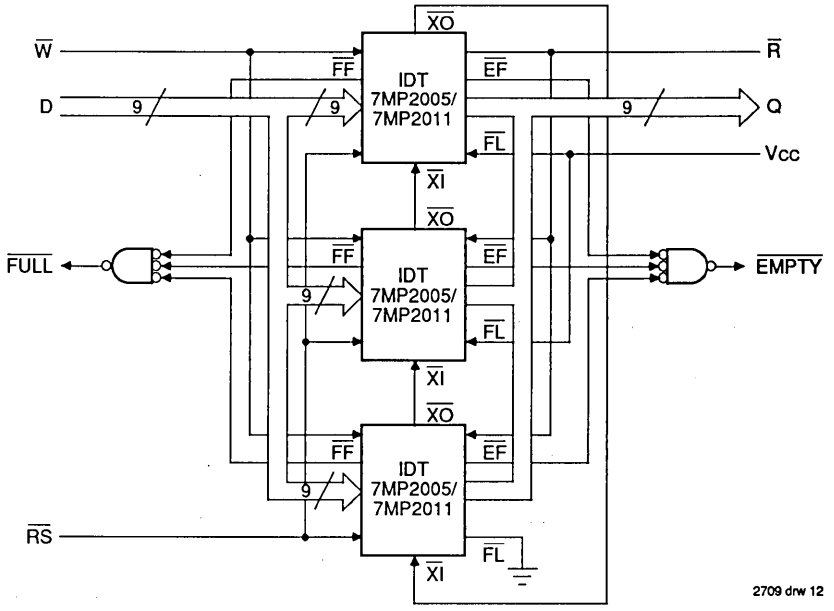


Figure 10. Block Diagram of 24,576 x 9/49,152 x 9 FIFO Memory (Depth Expansion)

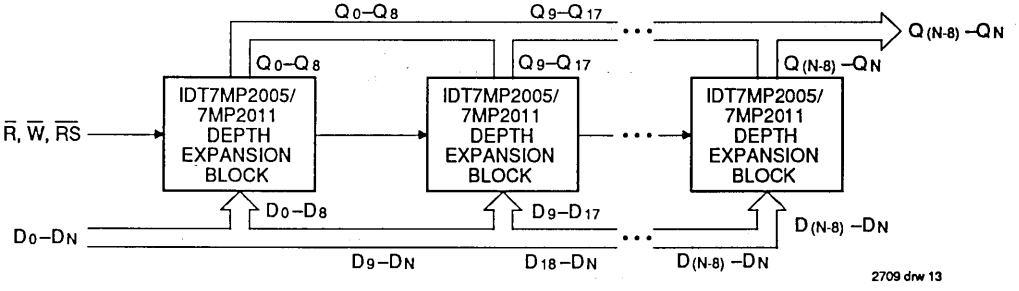


Figure 11. Compound FIFO Expansion

NOTES:
1. For depth expansion block see DEPTH EXPANSION Section and Figure 10.
2. For Flag detection see WIDTH EXPANSION Section and Figure 9.

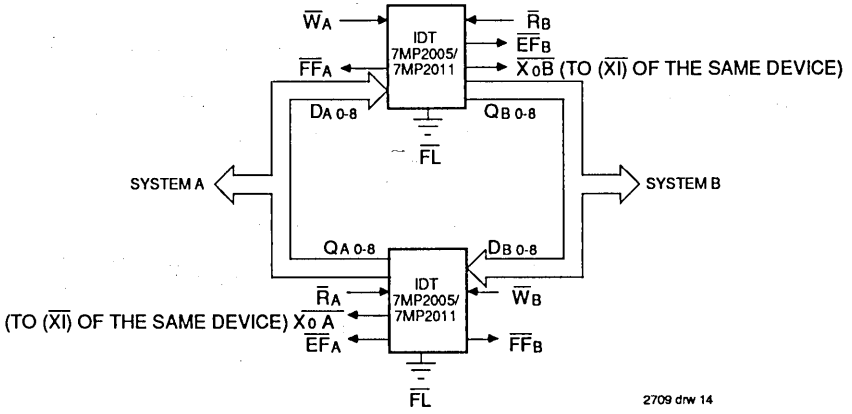


Figure 12. Bidirectional FIFO Mode

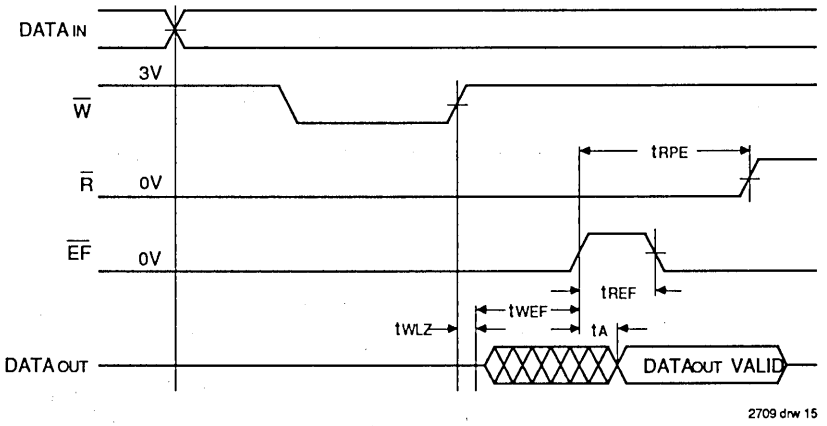


Figure 13. Read Data Flow-Through Mode

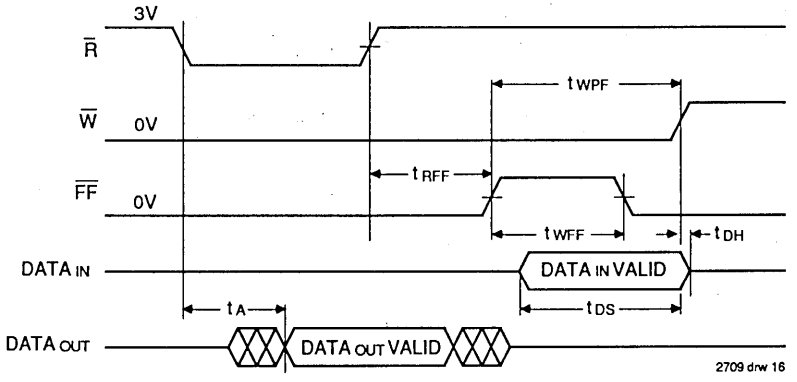
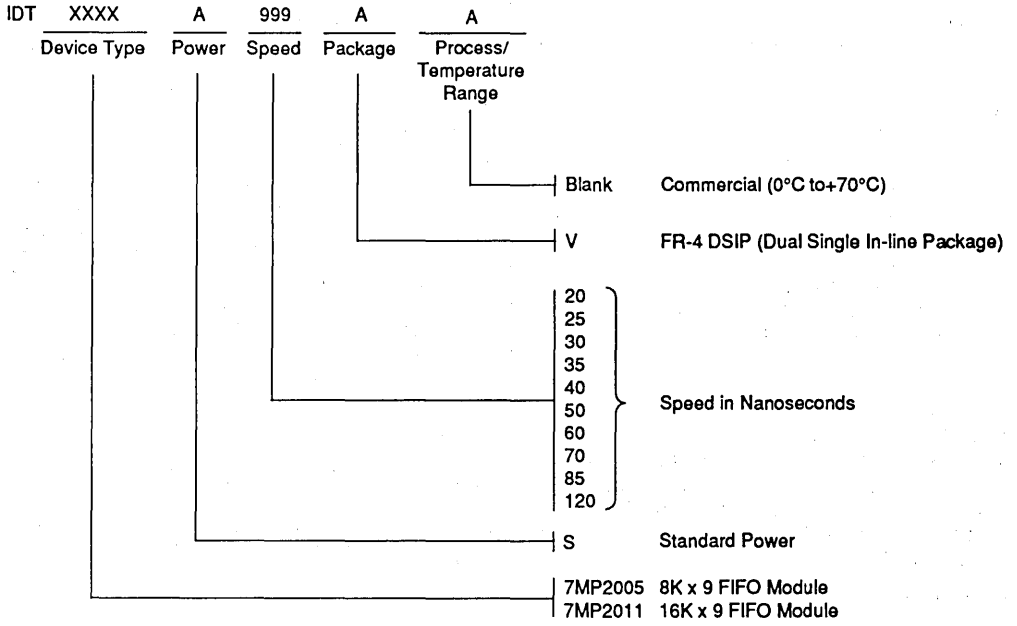


Figure 14. Write Data Flow-Through Mode

ORDERING INFORMATION



2709 drw 17

8

Integrated Device Technology, Inc.

32K x 9 CMOS PARALLEL IN-OUT FIFO MODULE

IDT7M207S

FEATURES:

- First-In/First-Out memory module
- 32K x 9 organization
- High speed: 30ns (max.) access time
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- MASTER/SLAVE multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and Full warning-flags
- High-performance CEMOS™ technology
- Single 5V (±10%) power supply

DESCRIPTION:

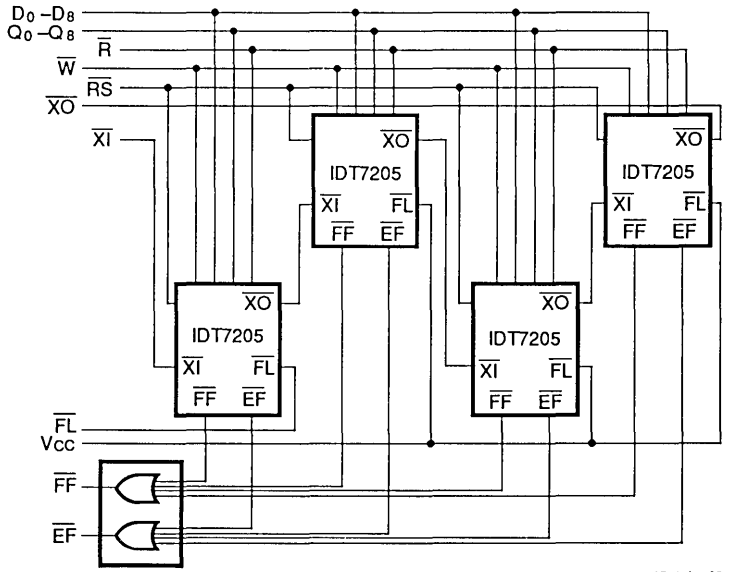
IDT7M207S is a FIFO memory modules constructed on a multi-layered ceramic substrate using four IDT7205 (8K x 9) FIFOs in leadless chip carriers. Extremely high speeds are achieved in this fashion due to the use of IDT7205s fabricated in IDT's high performance CEMOS technology. These devices utilize a algorithm that loads and empties data on a first-in/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The devices have a read/write cycle time of 30ns (min.) for commercial and 35ns (min.) for military temperature ranges.

The devices utilize a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

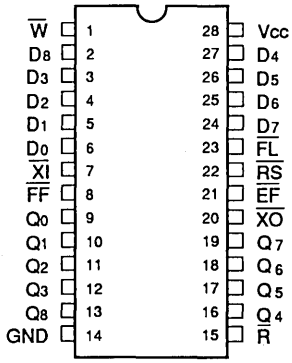
IDT's Military FIFO modules have semicondutor components manufactued in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION[1]



2718 drw 01

DIP
TOP VIEW

PIN NAMES

W = WRITE	FL = FIRST LOAD	XI = EXPANSION IN	EF = EMPTY FLAG
R = READ	D = DATAIN	XO = EXPANSION OUT	Vcc = POWER
RS = RESET	Q = DATAOUT	FF = FULL FLAG	GND = GROUND

2718 tbl 01

NOTE:
1. For module dimensions, please refer to drawing M1 in the packaging section.

8

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2718 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}(1)	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}(1)	Input Low Voltage Commercial and Military	—	—	0.8	V

NOTE: 2718 tbl 03

1. 1.5V undershoots are allowed for 10ns once per cycle.

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	40	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	60	pF

NOTE: 2718 tbl 04

1. This parameter is guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; and –55°C to +125°C)

Symbol	Parameter	IDT7M207S Commercial		IDT7M207S Military		Unit
		Min.	Max.	Min.	Max.	
I_{LI}(1)	Input Leakage Current (Any Input)	–5	5	-10	10	µA
I_{OL}(2)	Output Leakage Current	–10	10	-10	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = –2mA	2.4	—	2.4	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA	—	0.4	—	0.4	V
I_{CC1}(3)	Average Vcc Power Supply Current	—	600	—	720	mA
I_{CC2}(3)	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH})	—	48	—	100	mA
I_{CC3}(3)	Power Down Current (All Input = V_{CC} – 0.2V)	—	32	—	48	mA

NOTES: 2718 tbl 04

1. Measurements with 0.4 ≤ V_{IN} ≤ V_{OUT}.
2. $\overline{R}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Icc measurements are made with outputs open.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1, 2 & 3

2718 tbl 06

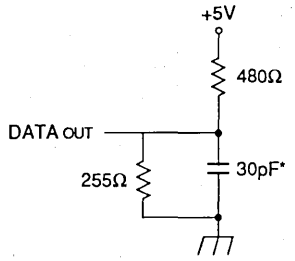


Figure 1. Output Load

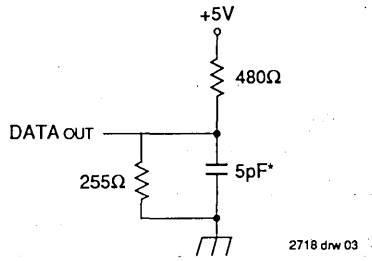


Figure 2. Output Load (for tRLZ, tWLZ, and tRHZ)

* Includes scope and jig capacitances.

AC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V±10%, TA = 0°C to +70°C and –55°C to +125°C)

Symbol	Parameter	7M207S30 (Com'l. Only) Min.	Max.	7M207S35 Min.	Max.	7M207S40 Min.	Max.	7M207S50 Min.	Max.	Unit
tRC	Read Cycle Time	40	—	45	—	50	—	65	—	ns
tA	Access Time	—	30	—	35	—	40	—	50	ns
tRR	Read Recovery Time	10	—	10	—	10	—	15	—	ns
tRPW(1)	Read Pulse Width	30	—	35	—	40	—	50	—	ns
tRLZ(2)	Read Pulse Low to Data Bus at Low Z	5	—	5	—	5	—	10	—	ns
tWLZ(2)	Write Pulse High to Data Bus at Low Z	10	—	10	—	10	—	15	—	ns
tDV	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	ns
tRHZ(2)	Read Pulse High to Data Bus at High Z	—	20	—	20	—	25	—	30	ns
tWC	Write Cycle Time	40	—	45	—	50	—	65	—	ns
tWPW(1)	Write Pulse Width	30	—	35	—	40	—	50	—	ns
tWR	Write Recovery Time	10	—	10	—	10	—	15	—	ns
tDS	Data Set-up Time	18	—	20	—	23	—	30	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	5	—	ns
tRSC	Reset Cycle Time	40	—	45	—	50	—	65	—	ns
tRS(1)	Reset Pulse Width	30	—	35	—	40	—	50	—	ns
tRSR	Reset Recovery Time	10	—	10	—	10	—	15	—	ns
tEFL	Reset to Emtpy Flag Low	—	40	—	45	—	55	—	65	ns
tREF	Read Low to Emtpy Flag Low	—	30	—	35	—	40	—	50	ns
tRFF	Read High to Full Flag High	—	30	—	35	—	40	—	50	ns
tWEF	Write High to Empty Flag High	—	30	—	35	—	40	—	50	ns
tWFF	Write Low to Full Flag Low	—	30	—	35	—	40	—	50	ns

2718 tbl 05

NOTES:
1. Pulse widths less than minimum value are not allowed.
2. Values guaranteed by design, not currently tested.

8

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V±10%, T_A = 0°C to +70°C and –55°C to +125°C)

Symbol	Parameter	7M207S60 Min.	7M207S60 Max.	7M207S70 Min.	7M207S70 Max.	7M207S85 Min.	7M207S85 Max.	7M207S120 Min.	7M207S120 Max.	Unit
t_{RC}	Read Cycle Time	75	—	85	—	105	—	140	—	ns
t_A	Access Time	—	60	—	70	—	85	—	120	ns
t_{RR}	Read Recovery Time	15	—	15	—	20	—	20	—	ns
t_{RPW}[1]	Read Pulse Width	60	—	70	—	85	—	120	—	ns
t_{RLZ}[2]	Read Pulse Low to Data Bus at Low Z	10	—	10	—	10	—	10	—	ns
t_{WLZ}[2]	Write Pulse High to Data Bus at Low Z	15	—	15	—	20	—	20	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	ns
t_{RHZ}[2]	Read Pulse High to Data Bus at High Z	—	30	—	30	—	30	—	35	ns
t_{WC}	Write Cycle Time	75	—	85	—	105	—	140	—	ns
t_{WPW}[1]	Write Pulse Width	60	—	70	—	85	—	120	—	ns
t_{WR}	Write Recovery Time	15	—	15	—	20	—	20	—	ns
t_{DS}	Data Set-up Time	30	—	30	—	40	—	40	—	ns
t_{DH}	Data Hold Time	5	—	10	—	10	—	10	—	ns
t_{RSC}	Reset Cycle Time	75	—	85	—	105	—	140	—	ns
t_{RS}[1]	Reset Pulse Width	60	—	70	—	85	—	120	—	ns
t_{RSR}	Reset Recovery Time	15	—	15	—	20	—	20	—	ns
t_{EFL}	Reset to Emtpy Flag Low	—	75	—	85	—	105	—	140	ns
t_{REF}	Read Low to Emtpy Flag Low	—	60	—	70	—	85	—	120	ns
t_{RFF}	Read High to Full Flag High	—	60	—	70	—	85	—	120	ns
t_{WEF}	Write High to Empty Flag High	—	60	—	70	—	85	—	120	ns
t_{WFF}	Write Low to Full Flag Low	—	60	—	70	—	85	—	120	ns

NOTES:
1. Pulse widths less than minimum value are not allowed
2. Values guaranteed by design, not currently tested.

2718 tbl 08

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D_0-D_8)
Data Inputs for 9-bit wide data path.

CONTROLS:

RESET ($\overline{RS}$)
Reset is accomplished whenever the RESET ($\overline{RS}$) input is taken to a low state. During RESET, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. Both the READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) inputs must be in the high state during reset.

WRITE ENABLE ($\overline{W}$)
A write cycle is initiated on the falling edge of this input if the FULL FLAG ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect the the rising edge of the WRITE ENABLE ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

To prevent data overflow, the FULL FLAG ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the FULL FLAG ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin.

READ ENABLE ($\overline{R}$)
A read cycle is initiated on the falling edge of the READ ENABLE ($\overline{R}$) provided the EMPTY FLAG ($\overline{EF}$) is not set. The data is accessed on a first-in/first-out basis independent of any ongoing write operations. After READ ENABLE ($\overline{R}$) goes high, the Data Outputs (Q_0 through Q_8) will return to a high impedance condition until the next READ operation. When all the data has been read from the FIFO, the EMPTY FLAG ($\overline{EF}$) will go low, inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the EMPTY FLAG ($\overline{EF}$) will go high after t_{WEF} and a valid READ can then begin.

FIRST LOAD ($\overline{FL}$)
This pin is grounded to indicate that it is the first device. In the multiple module (depth expansion mode) application, this pin on the rest of devices should connect to Vcc for proper operation.

EXPANSION IN ($\overline{XI}$)
EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous (in depth expansion) or same device for proper applications.

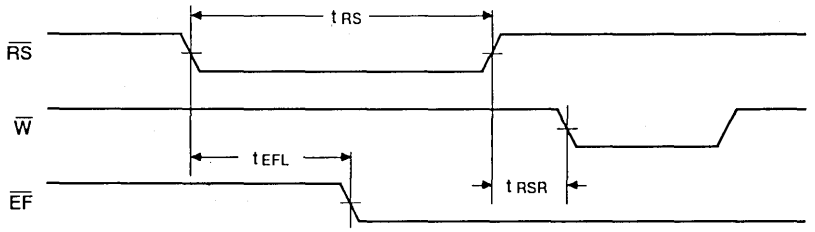
OUTPUTS:

FULL FLAG ($\overline{FF}$)
The FULL FLAG ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location from the read pointer, indicating that the device is full. If the read pointer is not moved after RESET ($\overline{RS}$), the FULL FLAG ($\overline{FF}$) will go low after 32,768 writes for the IDT7M207.

EXPANSION OUT ($\overline{XO}$)
EXPANSION OUT ($\overline{XO}$) is connected to the EXPANSION IN ($\overline{XI}$) of the same device (single device mode) or the EXPANSION IN ($\overline{XI}$) of the next device (multiple device, depth expansion mode) for proper operation. This output acts as a signal to the next device by providing a pulse to the next device when the current device reaches the last location of memory.

DATA OUTPUTS (Q_0-Q_8)
Data outputs for a 9-bit wide data path. This output is in a high impedance condition whenever READ ($\overline{R}$) is in a high state.

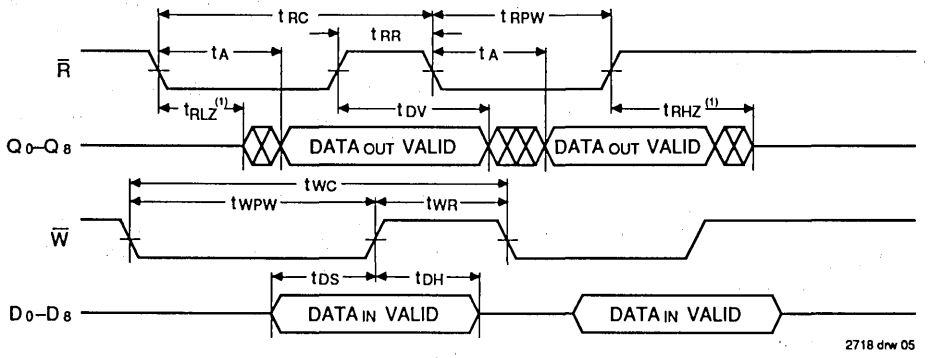
TIMING WAVEFORM OF RESET CYCLE(1,2)



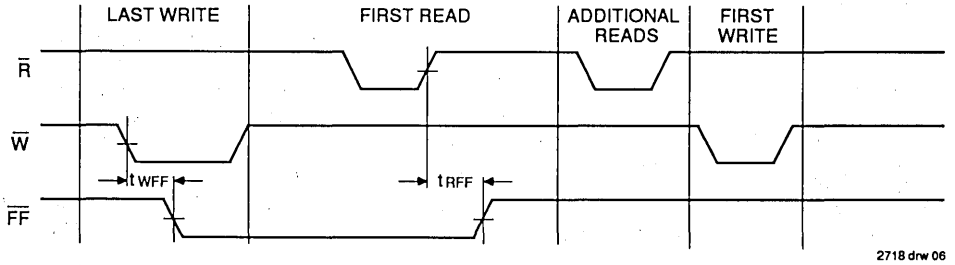
2718 drw 04

NOTES:
1. $t_{RSC} = t_{RS} + t_{RSR}$
2. $\overline{W}$ and $\overline{R}$ = V_{IH} during RESET.

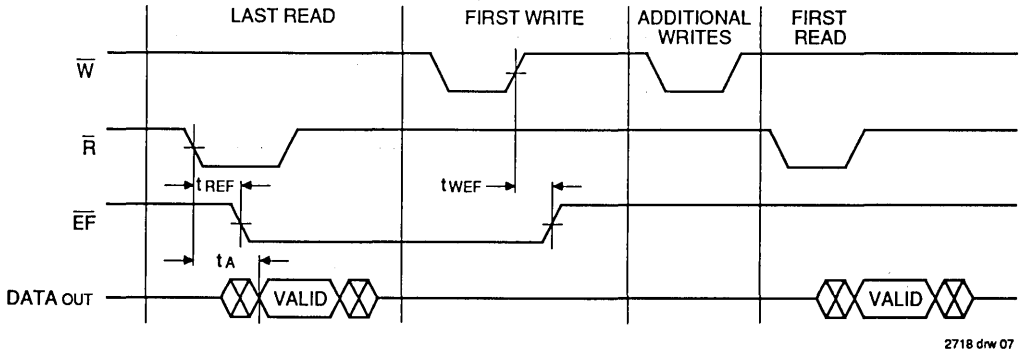
TIMING WAVEFORM OF ASYNCHRONOUS WRITE AND READ OPERATION



TIMING WAVEFORM FOR THE FULL FLAG FROM LAST WRITE TO FIRST READ



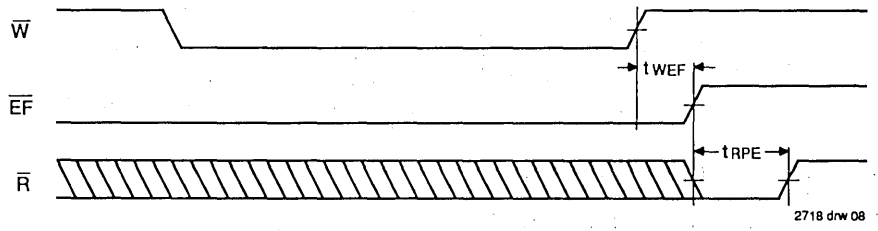
TIMING WAVEFORM FOR THE EMPTY FLAG FROM LAST READ TO FIRST WRITE



NOTE:
1. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM FOR THE EMPTY FLAG CYCLE

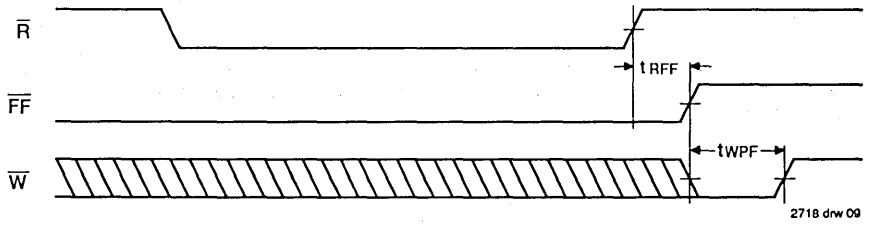
t_{RPE} EFFECTIVE READ PULSE WIDTH AFTER FULL FLAG HIGH (1)



NOTE:
1. (t_{RPE} = t_{RPW})

TIMING WAVEFORM FOR THE FULL FLAG CYCLE

t_{RPE} EFFECTIVE READ PULSE WIDTH AFTER FULL FLAG HIGH (1)



NOTE:
1. (t_{WPF} = t_{WPW})

8

OPERATING MODES

SINGLE DEVICE MODE

A single IDT7M207 may be used when the application requirements are for 32,768 words or less. The IDT7M207 is in a Single Device Configuration when the EXPANSION IN ($\overline{XI}$) control input is connected to the EXPANSION OUT ($\overline{XO}$) of the device and the FIRST LOAD ($\overline{FL}$) control pin is grounded (see Figure 8).

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 9 demonstrates an 18-bit word width by using two IDT7M207s. Any word width can be attained by adding additional IDT7M207s.

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT7M207 can easily be adapted to applications when the requirements are for greater than 32,768 words. Figure 10 demonstrates Depth Expansion using three IDT7M207s. Any depth can be attained by adding additional IDT7M207s. The IDT7M207 operate in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the FIRST LOAD ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The EXPANSION OUT ($\overline{XO}$) pin of each device must be tied to the EXPANSION IN ($\overline{XI}$) pin of the next device. (See Figure 10.)
4. External logic is needed to generate a composite FULL FLAG ($\overline{FF}$) and EMPTY FLAG ($\overline{EF}$). This requires the logical ANDing of all $\overline{EF}$s and logical ANDing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). (See Figure 10.)

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see Figure 11).

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of READ and WRITE operations) can be achieved by pairing IDT7M207s as shown in Figure 12. Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted with the IDT7M207: a read flow-through mode and write flow-through mode. For the read flow-through mode (Figure 13), the FIFO permits a reading of a single word of data immediately after writing one word of data into the completely empty FIFO.

In the write flow-through mode (Figure 14), the FIFO permits a writing of a single word of data immediately after reading one word of data from a completely full FIFO.

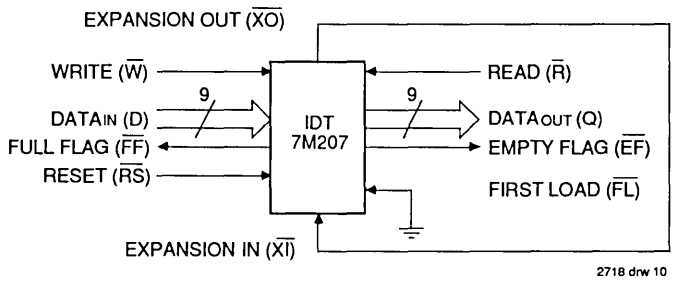
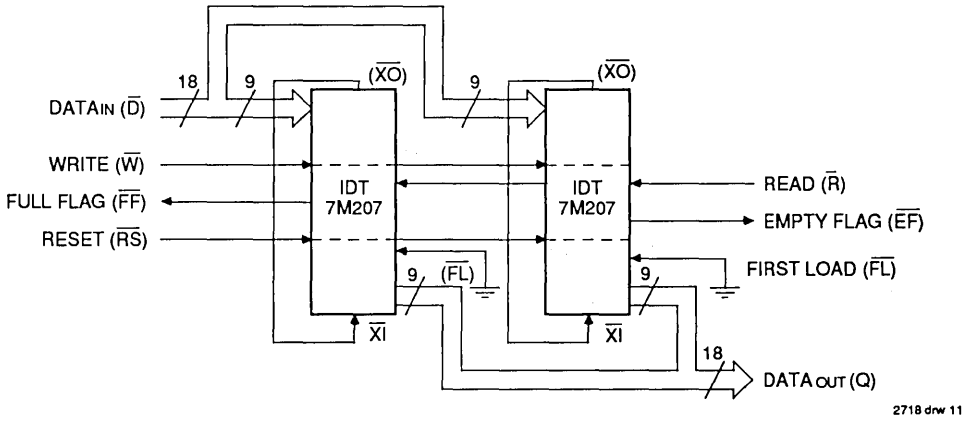


Figure 8. Block Diagram of Single IDT7M207 FIFO



NOTE:
1. Flag detection is accomplished by monitoring the FF and EF signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 9. Block Diagram of 32,768 x 18 FIFO Memory Used in Width Expansion Mode

TRUTH TABLES
TABLE I—RESET

Single Device Configuration/Width Expansion Mode

Mode	Inputs		Internal Status		Outputs	
	RS	XI	Read Pointer	Write Pointer	EF	FF
Reset	0	0	Location Zero	Location Zero	0	1
Read/Write	1	0	Increment(1)	Increment(1)	X	X

NOTE: 2718 tbl 08
1. Pointer will increment if flag is High.

TABLE II—RESET AND FIRST LOAD TRUTH TABLE

Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	RS	FL	XI	Read Pointer	Write Pointer	EF	FF
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTE: 2718 tbl 09
1. XI is connected to XO of previous device. See Figure 10.
2. RS = Reset Input, FL = First Load, EF = Empty Flag Output, FF = Flag Full Output, XI = Expansion Input.

8

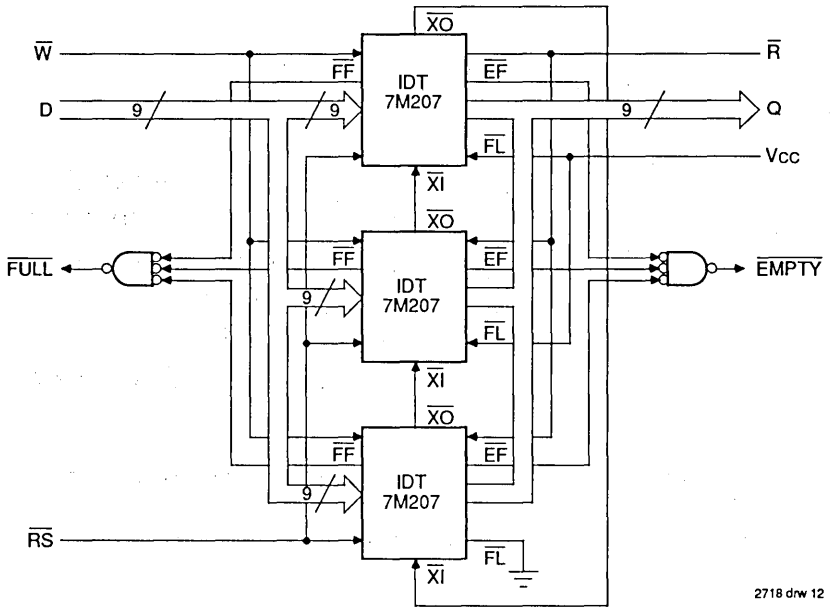


Figure 10. Block Diagram of 98,304 x 9 FIFO Memory (Depth Expansion)

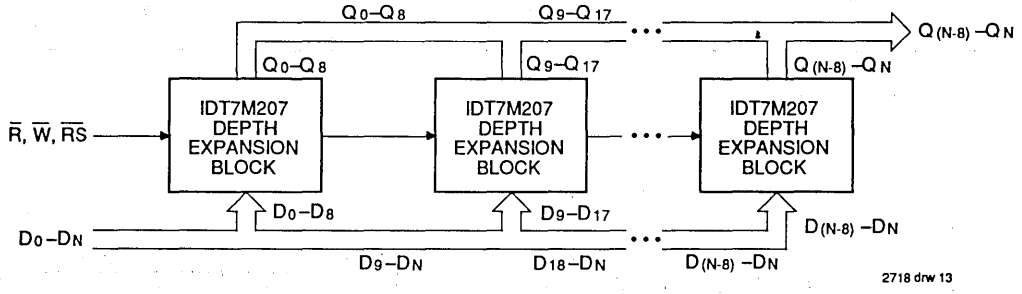


Figure 11. Compound FIFO Expansion

NOTES:
1. For depth expansion block see DEPTH EXPANSION Section and Figure 10.
2. For Flag detection see WIDTH EXPANSION Section and Figure 9.

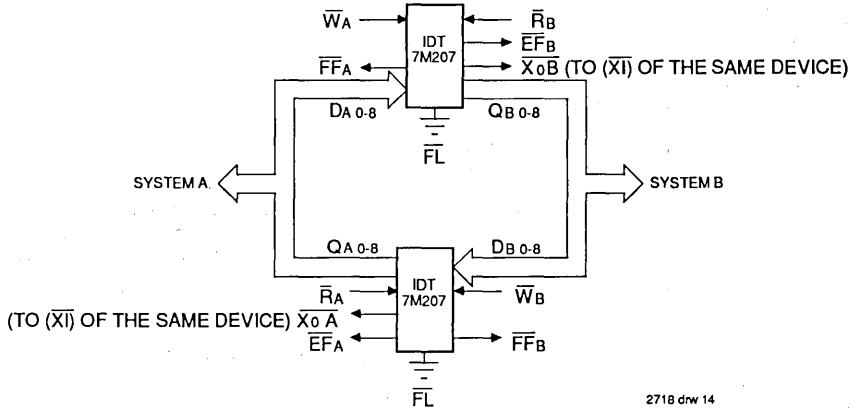


Figure 12. Bidirectional FIFO Mode

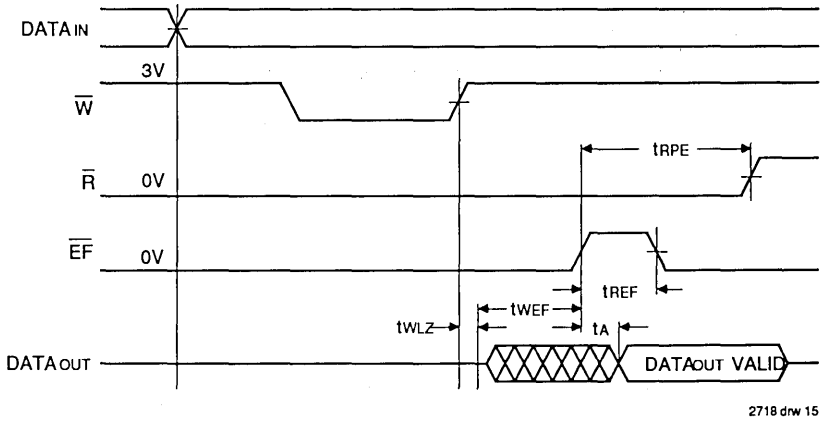


Figure 13. Read Data Flow-Through Mode

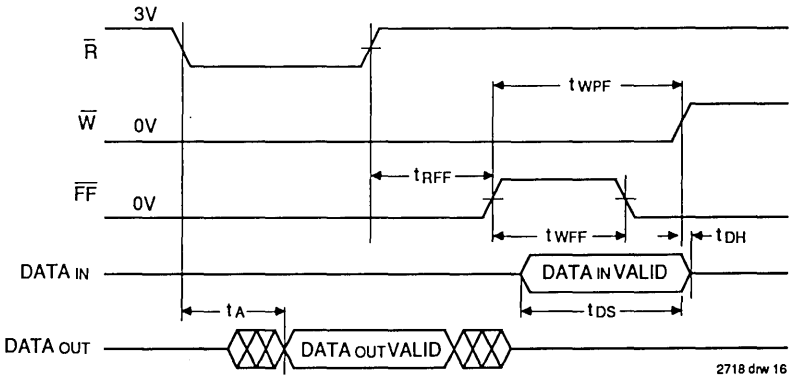
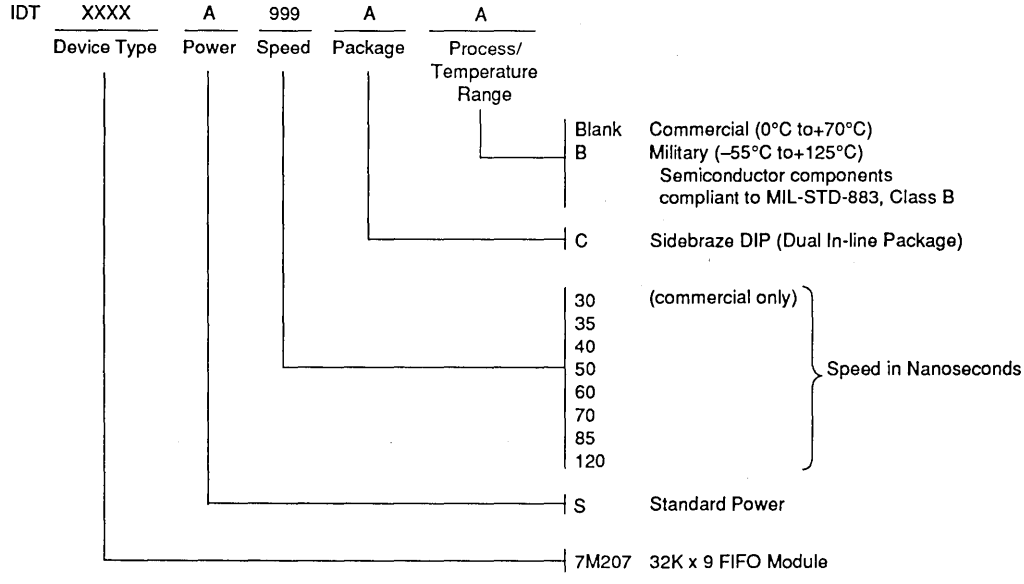


Figure 14. Write Data Flow-Through Mode

ORDERING INFORMATION



2718 drw 17

Integrated Device Technology, Inc.

32K x 18 & 16K x 18 CEMOS™ PARALLEL IN-OUT FIFO MODULE

PRELIMINARY
IDT7MP2009
IDT7MP2010

FEATURES:

- First-In/First-Out memory module
- 32K x 18 organization (IDT7MP2009)
- 16K x 18 organization (IDT7MP2010)
- High speed: 20ns (max.) access time
- Separate upper and lower 9-bit $\overline{XI}$ and $\overline{XO}$
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- MASTER/SLAVE multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and Full warning-flags
- High-performance CEMOS™ technology
- Single 5V (±10%) power supply

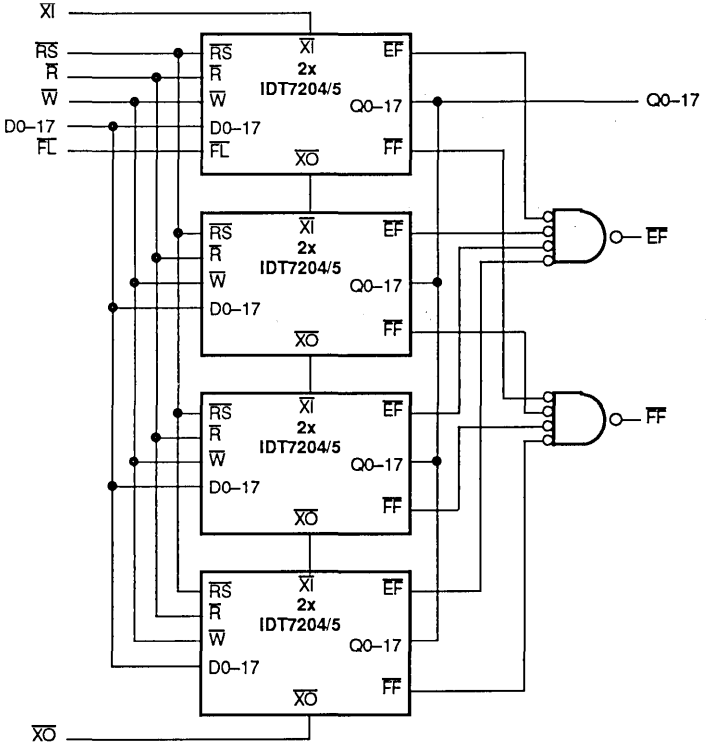
DESCRIPTION:

IDT7MP2009/7MP2010 are FIFO memory modules constructed on multi-layered epoxy laminate (FR-4) substrate by mounting eight IDT7205 (8K x 9) or IDT7204 (4K x 9) FIFOs in plastic leaded chip carriers. Extremely high speeds are achieved in this fashion due to the use of IDT7205s and IDT7204s fabricated in IDT's high performance CEMOS technology. These devices utilize an algorithm that loads and empties data on a first-in/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The devices have a read/write cycle time of 30ns (min.) for commercial temperature ranges.

The devices utilize a 18-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

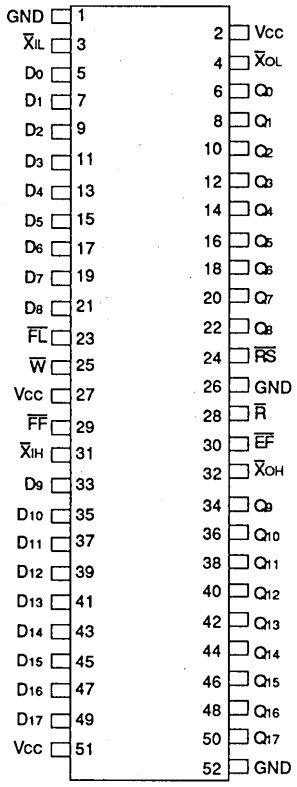
FUNCTIONAL BLOCK DIAGRAM



2799 drw 01

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION[1]



ZIP
TOP VIEW

2799 drw 02

PIN NAMES

$\overline{W}$ = WRITE	$\overline{FL}$ = FIRST LOAD	$\overline{X}_{IH}$, $\overline{X}_{IL}$ = EXPANSION IN	$\overline{EF}$ = EMPTY FLAG
$\overline{R}$ = READ	D_{0-17} = DATAIN	$\overline{X}_{OH}$, $\overline{X}_{OL}$ = EXPANSION OUT	Vcc = POWER
$\overline{RS}$ = RESET	Q_{0-17} = DATAOUT	$\overline{FF}$ = FULL FLAG	GND = GROUND

NOTE:
1. For module dimensions, please refer to drawing M45 in the packaging section.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2709 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}(1)	Input High Voltage Commercial	2.0	—	—	V
V_{IL}(1)	Input Low Voltage Commercial	—	—	0.8	V

NOTE: 2709 tbl 03

1. 1.5V undershoots are allowed for 10ns once per cycle.

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	80	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	120	pF

NOTE: 2709 tbl 04

1. This parameter is guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	IDT7MP2010(4) Min.	IDT7MP2010(4) Max.	IDT7MP2009(5) Min.	IDT7MP2009(5) Max.	IDT7MP2010(6) Min.	IDT7MP2010(6) Max.	Unit
$\|I_{LI}\|$(1)	Input Leakage Current (Any Input)	—	20	—	20	—	20	µA
$\|I_{OL}\|$(2)	Output Leakage Current	—	20	—	20	—	20	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = –2mA	2.4	—	2.4	—	2.4	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA	—	0.4	—	0.4	—	0.4	V
I_{CC1}(3)	Operating Current	—	1280	—	1200	—	975	mA
I_{CC2}(3)	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH})	—	115	—	100	—	100	mA
I_{CC3}(3)	Power Down Current (All Input = V_{CC} – 0.2V)	—	65	—	65	—	65	mA

NOTES: 2709 tbl 04

1. Measurements with 0.4 ≤ V_{IN} ≤ V_{OUT}.
2. $\overline{R}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. I_{CC} measurements are made with outputs open.
4. t_{AA} = 20, 25, 30, 35ns.
5. t_{AA} = 30, 35, 40, 50, 60, 70, 85, 120ns.
6. t_{AA} = 40, 50, 60, 70, 85, 120ns.

8

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1, 2 & 3

2709 tbl 06

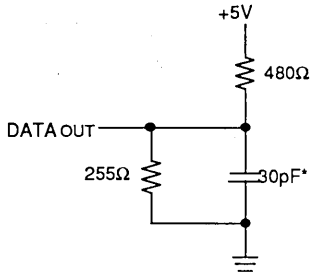


Figure 1. Output Load

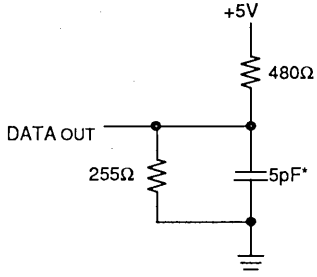


Figure 2. Output Load
(for t_{RLZ}, t_{WLZ}, and t_{RHZ})

* Includes scope and jig capacitances.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP2010S20 Min.	7MP2010S20 Max.	7MP2010S25 Min.	7MP2010S25 Max.	7MP2010S30 7MP2009S30 Min.	7MP2010S30 7MP2009S30 Max.	7MP2010S35 7MP2009S35 Min.	7MP2010S35 7MP2009S35 Max.	Unit
t_{RC}	Read Cycle Time	30	—	35	—	40	—	45	—	ns
t_A	Access Time	—	20	—	25	—	30	—	35	ns
t_{RR}	Read Recovery Time	10	—	10	—	10	—	10	—	ns
t_{RPW}(1)	Read Pulse Width	20	—	25	—	30	—	35	—	ns
t_{RLZ}(2)	Read Pulse Low to Data Bus at Low Z	5	—	5	—	5	—	5	—	ns
t_{WLZ}(2)	Write Pulse High to Data Bus at Low Z	5	—	5	—	10	—	10	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	ns
t_{RHZ}(2)	Read Pulse High to Data Bus at High Z	—	13	—	20	—	20	—	20	ns
t_{WC}	Write Cycle Time	30	—	35	—	40	—	45	—	ns
t_{WPW}(1)	Write Pulse Width	20	—	25	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	10	—	10	—	10	—	10	—	ns
t_{DS}	Data Set-up Time	15	—	18	—	18	—	20	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{RSC}	Reset Cycle Time	30	—	35	—	40	—	45	—	ns
t_{RS}(1)	Reset Pulse Width	20	—	25	—	30	—	35	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	10	—	10	—	ns
t_{EFL}	Reset to Empty Flag Low	—	30	—	35	—	40	—	45	ns
t_{REF}	Read Low to Empty Flag Low	—	20	—	25	—	30	—	35	ns
t_{RFF}	Read High to Full Flag High	—	23	—	25	—	30	—	35	ns
t_{WEF}	Write High to Empty Flag High	—	23	—	25	—	30	—	35	ns
t_{WFF}	Write Low to Full Flag Low	—	20	—	25	—	30	—	35	ns

NOTES:
1. Pulse widths less than minimum value are not allowed.
2. This parameter is guaranteed by design but not tested.

2709 tbl 05

AC ELECTRICAL CHARACTERISTICS (Continued)

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP2010S40 7MP2009S40 Min.	Max.	7MP2010S50 7MP2009S50 Min.	Max.	7MP2010S60 7MP2009S60 Min.	Max.	7MP2010S70 7MP2009S70 Min.	Max.	Unit
t_{RC}	Read Cycle Time	50	—	65	—	75	—	85	—	ns
t_A	Access Time	—	40	—	50	—	60	—	70	ns
t_{RR}	Read Recovery Time	10	—	15	—	15	—	15	—	ns
t_{RPW}[1]	Read Pulse Width	40	—	50	—	60	—	70	—	ns
t_{RLZ}[2]	Read Pulse Low to Data Bus at Low Z	5	—	10	—	10	—	10	—	ns
t_{WLZ}[2]	Write Pulse High to Data Bus at Low Z	10	—	15	—	15	—	15	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	ns
t_{RHZ}[2]	Read Pulse High to Data Bus at High Z	—	25	—	30	—	30	—	30	ns
t_{WC}	Write Cycle Time	50	—	65	—	75	—	85	—	ns
t_{WPW}[1]	Write Pulse Width	40	—	50	—	60	—	70	—	ns
t_{WR}	Write Recovery Time	10	—	15	—	15	—	15	—	ns
t_{DS}	Data Set-up Time	20	—	30	—	30	—	30	—	ns
t_{DH}	Data Hold Time	0	—	5	—	5	—	10	—	ns
t_{RSC}	Reset Cycle Time	50	—	65	—	75	—	85	—	ns
t_{RS}[1]	Reset Pulse Width	40	—	50	—	60	—	70	—	ns
t_{RSR}	Reset Recovery Time	10	—	15	—	15	—	15	—	ns
t_{EFL}	Reset to Empty Flag Low	—	50	—	65	—	75	—	85	ns
t_{REF}	Read Low to Empty Flag Low	—	40	—	50	—	60	—	70	ns
t_{RFF}	Read High to Full Flag High	—	40	—	50	—	60	—	70	ns
t_{WEF}	Write High to Empty Flag High	—	40	—	50	—	60	—	70	ns
t_{WFF}	Write Low to Full Flag Low	—	40	—	50	—	60	—	70	ns

NOTES:
1. Pulse widths less than minimum value are not allowed.
2. This parameter is guaranteed by design but not tested.

2709 tbl 08

8

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D_0-D_{17})
Data Inputs for 18-bit wide data path.

CONTROLS:

RESET ($\overline{RS}$)
Reset is accomplished whenever the RESET ($\overline{RS}$) input is taken to a low state. During RESET, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. Both the READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) inputs must be in the high state during reset.

WRITE ENABLE ($\overline{W}$)
A write cycle is initiated on the falling edge of this input if the FULL FLAG ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect the the rising edge of the WRITE ENABLE ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

To prevent data overflow, the FULL FLAG ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the FULL FLAG ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin.

READ ENABLE ($\overline{R}$)
A read cycle is initiated on the falling edge of the READ ENABLE ($\overline{R}$) provided the EMPTY FLAG ($\overline{EF}$) is not set. The data is accessed on a first-in/first-out basis independent of any ongoing write operations. After READ ENABLE ($\overline{R}$) goes high, the Data Outputs (Q_0 through Q_{17}) will return to a high impedance condition until the next READ operation. When all the data has been read from the FIFO, the EMPTY FLAG ($\overline{EF}$) will go low, inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the EMPTY FLAG ($\overline{EF}$) will go high after t_{WEF} and a valid READ can then begin.

FIRST LOAD ($\overline{FL}$)
This pin is grounded to indicate that it is the first device. In the multiple module (depth expansion mode) application, this pin on the rest of devices should connect to Vcc for proper operation.

EXPANSION IN ($\overline{XI}$)
EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous (in depth expansion) or same device for proper applications.

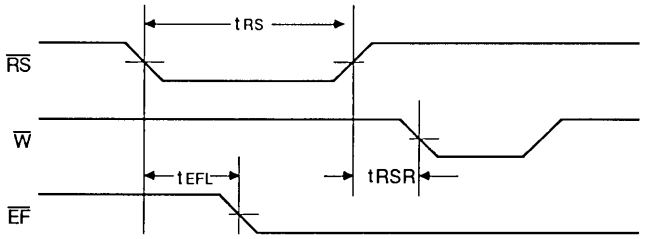
OUTPUTS:

FULL FLAG ($\overline{FF}$)
The FULL FLAG ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location from the read pointer, indicating that the device is full. If the read pointer is not moved after RESET ($\overline{RS}$), the FULL FLAG ($\overline{FF}$) will go low after 32,768 writes for the IDT7MP2009 and 16,384 writes for the IDT7MP2010.

EXPANSION OUT ($\overline{XO}$)
EXPANSION OUT ($\overline{XO}$) is connected to the EXPANSION IN ($\overline{XI}$) of the same device (single device mode) or the EXPANSION IN ($\overline{XI}$) of the next device (multiple device, depth expansion mode) for proper operation. This output acts as a signal to the next device by providing a pulse to the next device when the current device reaches the last location of memory.

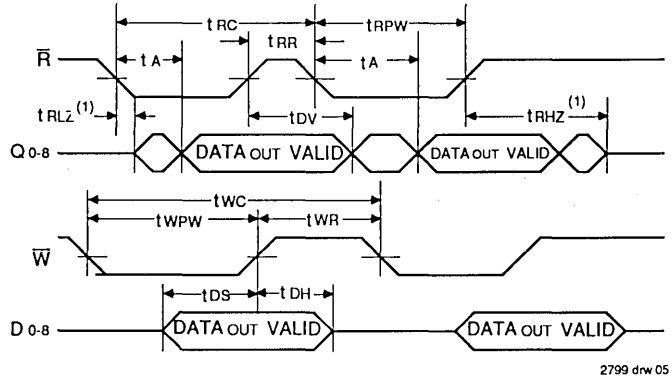
DATA OUTPUTS (Q_0-Q_{17})
Data outputs for a 18-bit wide data path. This output is in a high impedance condition whenever READ ($\overline{R}$) is in a high state.

TIMING WAVEFORM OF RESET CYCLE(1,2)

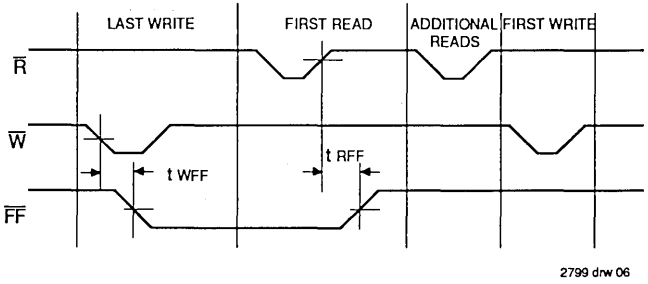


NOTES:
1. $t_{RSC} = t_{RS} + t_{RSR}$
2. $\overline{W}$ and $\overline{R}$ = V_{IH} during RESET.

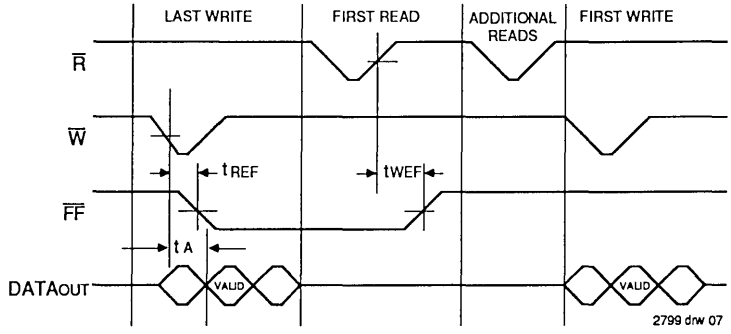
TIMING WAVEFORM OF ASYNCHRONOUS WRITE AND READ OPERATION



TIMING WAVEFORM FOR THE FULL FLAG FROM LAST WRITE TO FIRST READ

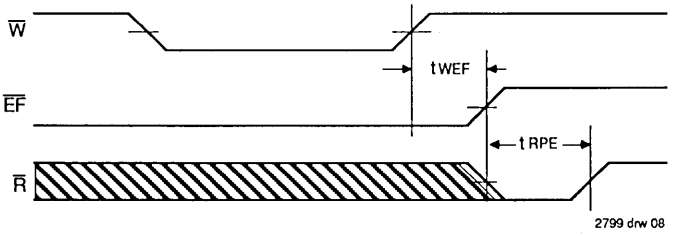


TIMING WAVEFORM FOR THE EMPTY FLAG FROM LAST READ TO FIRST WRITE



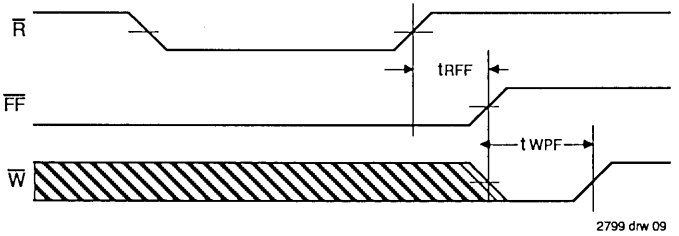
NOTE:
1. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF THE EMPTY FLAG CYCLE



NOTE:
1. ($t_{RPE} = t_{RPW}$)

TIMING WAVEFORM OF THE FULL FLAG CYCLE



NOTE:
1. ($t_{WPF} = t_{WPW}$)

OPERATING MODES

SINGLE DEVICE MODE

A single IDT7MP2009/2010 may be used when the application requirements are for 32,768/16,384 words or less. The IDT7MP2009/2010 is in a Single Device Configuration when the EXPANSION IN ($\overline{XI}$) control input is connected to the EXPANSION OUT ($\overline{XO}$) of the device and the FIRST LOAD ($\overline{FL}$) control pin is grounded (see Figure 8).

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 9 demonstrates an 36-bit word width by using two IDT7MP2009/2010. Any word width can be attained by adding additional IDT7MP2009/2010s.

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT7MP2009/2010 can easily be adapted to applications when the requirements are for greater than 32,768/16,384 words. Figure 10 demonstrates Depth Expansion using three IDT7MP2009/2010. Any depth can be attained by adding additional IDT7MP2009/2010s. The IDT7MP2009/2010 operate in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the FIRST LOAD ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The EXPANSION OUT ($\overline{XO}$) pin of each device must be tied to the EXPANSION IN ($\overline{XI}$) pin of the next device. (See Figure 10.)
4. External logic is needed to generate a composite FULL FLAG ($\overline{FF}$) and EMPTY FLAG ($\overline{EF}$). This requires the logical ANDing of all $\overline{EF}$s and logical ANDing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). (See Figure 10.)

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see Figure 11).

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of READ and WRITE operations) can be achieved by pairing IDT7MP2005/2011s as shown in Figure 12. Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted with the IDT7MP2009/2010: a read flow-through mode and write flow-through mode. For the read flow-through mode (Figure 13), the FIFO permits a reading of a single word of data immediately after writing one word of data into the completely empty FIFO.

In the write flow-through mode (Figure 14), the FIFO permits a writing of a single word of data immediately after reading one word of data from a completely full FIFO.

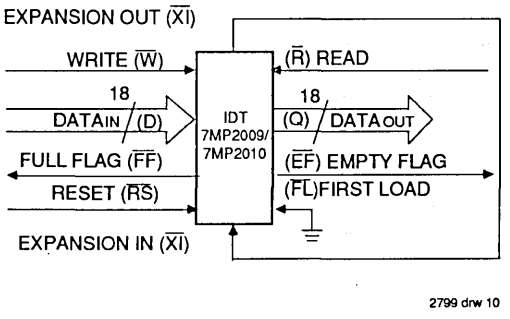
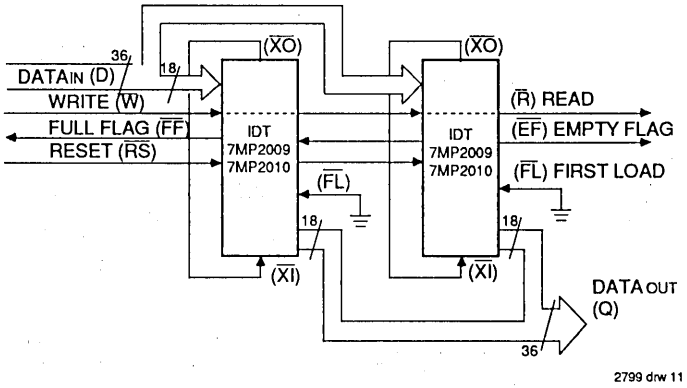


Figure 8. Block Diagram of Single IDT7MP2009/7MP2010 FIFO



NOTE:
1. Flag detection is accomplished by monitoring the $\overline{FF}$ and $\overline{EF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 9. Block Diagram of 32,768/16,384 x 36 FIFO Memory Used in Width Expansion Mode

TRUTH TABLES
TABLE I—RESET
Single Device Configuration/Width Expansion Mode

Mode	Inputs		Internal Status		Outputs	
	$\overline{RS}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset	0	0	Location Zero	Location Zero	0	1
Read/Write	1	0	Increment(1)	Increment(1)	X	X

NOTE:
1. Pointer will increment if flag is High.

2709 tbl 08

TABLE II—RESET AND FIRST LOAD TRUTH TABLE
Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTE:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 10.
2. $\overline{RS}$ = Reset Input, $\overline{FL}$ = First Load, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Flag Full Output, $\overline{XI}$ = Expansion Input.

2709 tbl 09

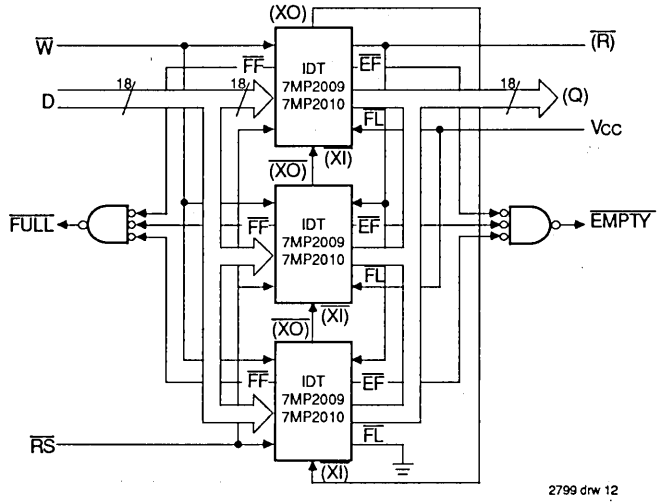


Figure 10. Block Diagram of 93,304/49,152 x 18 FIFO Memory (Depth Expansion)

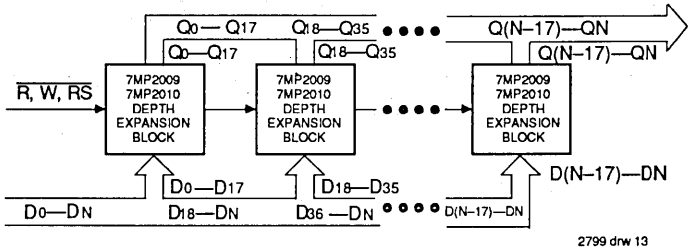


Figure 11. Compound FIFO Expansion

NOTES:
1. For depth expansion block see DEPTH EXPANSION Section and Figure 10.
2. For Flag detection see WIDTH EXPANSION Section and Figure 9.

8

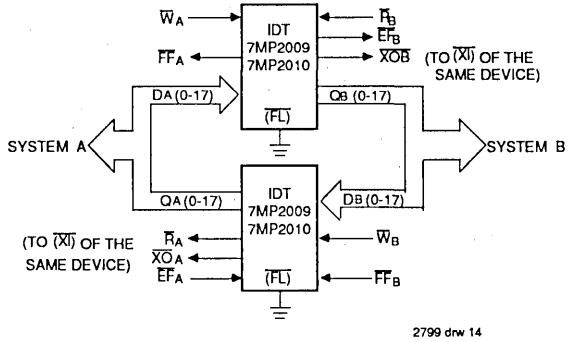


Figure 12. Bidirectional FIFO Mode

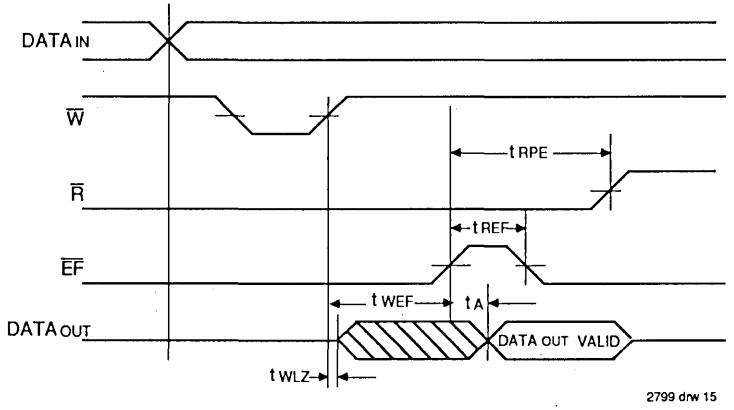


Figure 13. Read Data Flow-Through Mode

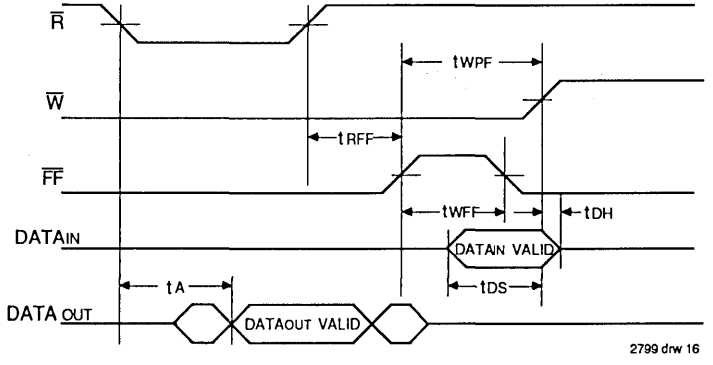
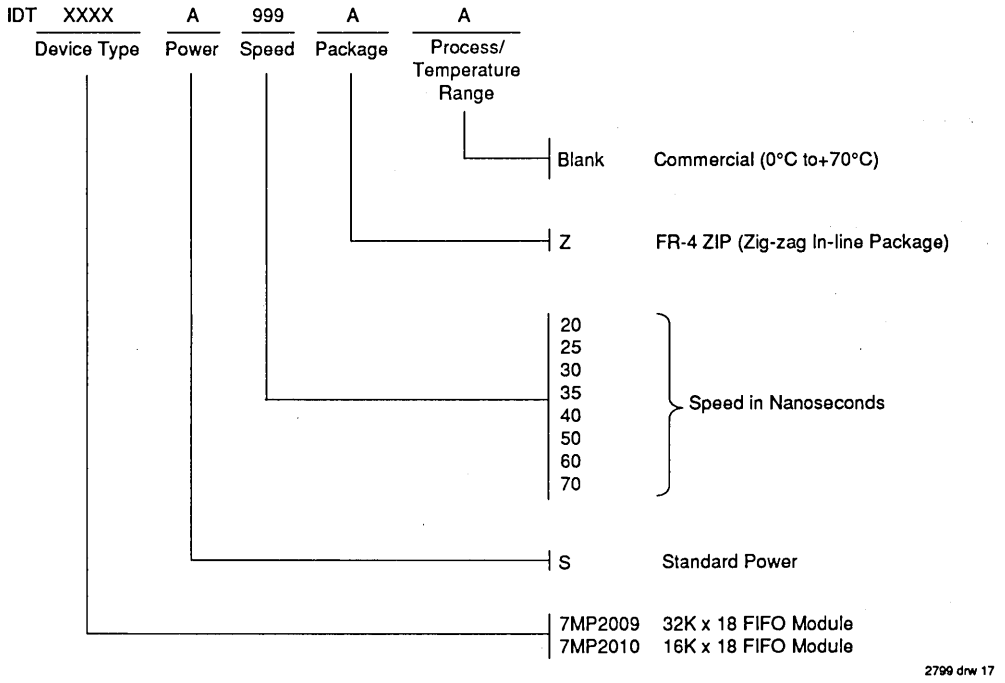


Figure 14. Write Data Flow-Through Mode

ORDERING INFORMATION



8

Integrated Device Technology, Inc.

1024K x 1 CMOS STATIC RAM MODULE

IDT7MC4001

FEATURES:

- High-density separate I/O, 1 megabit CMOS static RAM module
- Fast access times: 35ns (max.)
- Surface mounted LCC components mounted on a co-fired ceramic substrate
- Available in low profile 30-pin ceramic SIP (Single In-line Package)
- Low power consumption
- Single 5V(±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

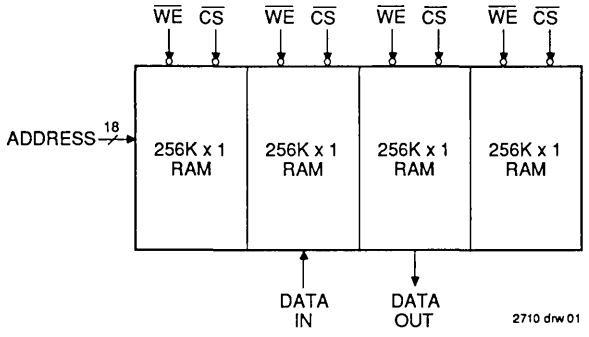
The IDT7MC4001 is a 1024K x 1 high-speed static RAM module with separate I/O. The module is constructed on a co-fired ceramic substrate using four 256K x 1 static RAMs in surface mount packages. Extremely fast speeds can be achieved by using RAMs fabricated in IDT's high-performance, high-reliability CEMOS™ technology.

The IDT7MC family of ceramic SIPs offers the optimum in packing density and profile height. The IDT7MC4001 is offered in a 30-pin ceramic SIP (Single In-line Package). At only 420 mils high, this low profile package is ideal for systems with minimal board spacing.

The IDT7MC4001 is available with maximum access times as fast as 35ns, with maximum power consumption of 1.35 watts. The module also offers a full standby mode of 330mW (max.).

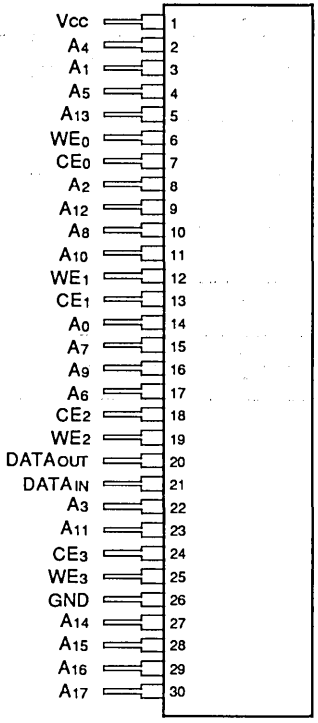
All inputs and outputs of the IDT7MC4001 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION[1]



2710 drw 02

SIP
FRONT VIEW

NOTE:
1. For module dimensions, please refer to module drawing M35 in the packaging section.

PIN NAMES

A_0–A_{17}	Address
$DATA_{IN}$	Data Input
$DATA_{OUT}$	Data Output
$\overline{CS}_{0-3}$	Chip Select
$\overline{WE}_{0-3}$	Write Enable
V_{CC}	Power
GND	Ground

2710 tbl 01

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	HighZ	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	High Z	Active

2710 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	TemperatureUnder Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2710 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Test	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	20	pF

NOTE: 2710 tbl 04
1. This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2710 tbl 05
1. V_{IL} = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2710 tbl 06

8

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	20	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	20	µA
I_{CC1}	Operating Power Supply Current	f = 0, $\overline{CS}$ = V_{IL}, V_{CC} = Max., Output Open	—	225	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ = V_{IL}, f = f_{MAX}, Output Open	—	245	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} or TTL Level, V_{CC} = Max., f=f_{MAX}, Output Open	—	180	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}$ ≥ V_{HC}, V_{IN} ≥ V_{HC} or ≤ V_{LC} V_{CS} = Max., Output Open	—	60	mA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	—	V

2710 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2710 tbl 08

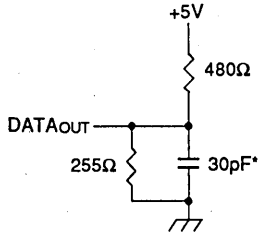


Figure 1. Output Load

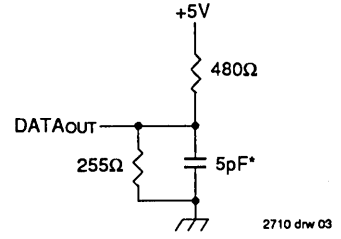


Figure 2. Output Load (for t_{CLZ}, t_{CHZ}, t_{OW}, and t_{WHZ})

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

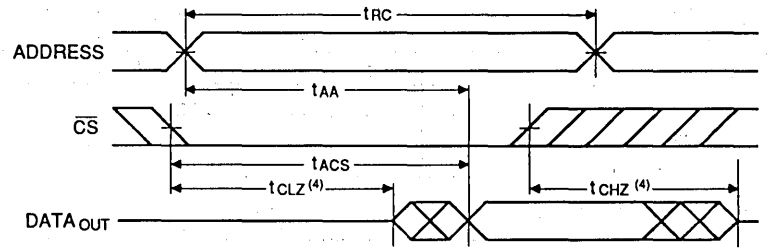
Symbol	Parameters	IDT7MC4001S35		IDT7MC4001S45		IDT7MC4001S55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	35	—	45	—	55	—	ns
t_{AA}	Address Access Time	—	35	—	45	—	55	ns
t_{ACS}	Chip Select Access Time	—	35	—	45	—	55	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	10	—	10	—	10	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	—	25	—	35	—	45	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	ns
t_{PU}(1)	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power Down Time	—	35	—	45	—	55	ns
Write Cycle								
t_{WC}	Write Cycle Time	35	—	45	—	55	—	ns
t_{CW}	Chip Selection to End of Write	30	—	40	—	50	—	ns
t_{AW}	Address Valid to End of Write	30	—	40	—	50	—	ns
t_{AS}	Address Set-up Time	5	—	5	—	5	—	ns
t_{WP}	Write Pulse Width	25	—	35	—	45	—	ns
t_{WR}	Write Recovery Time	5	—	5	—	5	—	ns
t_{WHZ}(1)	Write Enable to Ouput in High Z	—	25	—	30	—	40	ns
t_{DW}	Data Valid to End of Write	20	—	25	—	35	—	ns
t_{DH}	Data Hold from Write Time	5	—	5	—	5	—	ns
t_{OW}(1)	Output Active from End of Write	5	—	5	—	5	—	ns

NOTE:
1. This parameter is guaranteed by design but not tested.

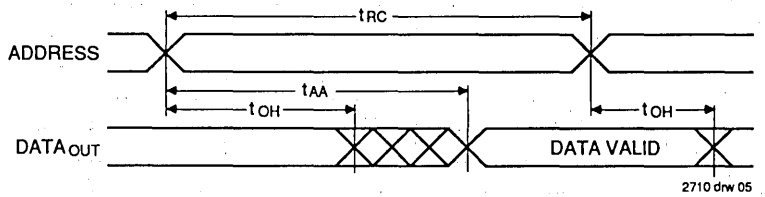
2710 tbl 09

8

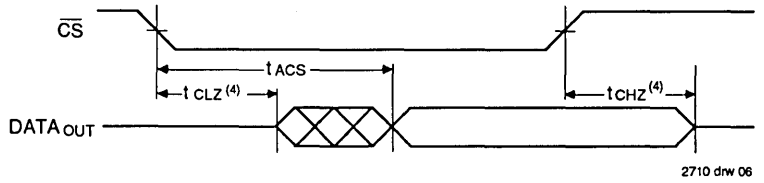
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2)

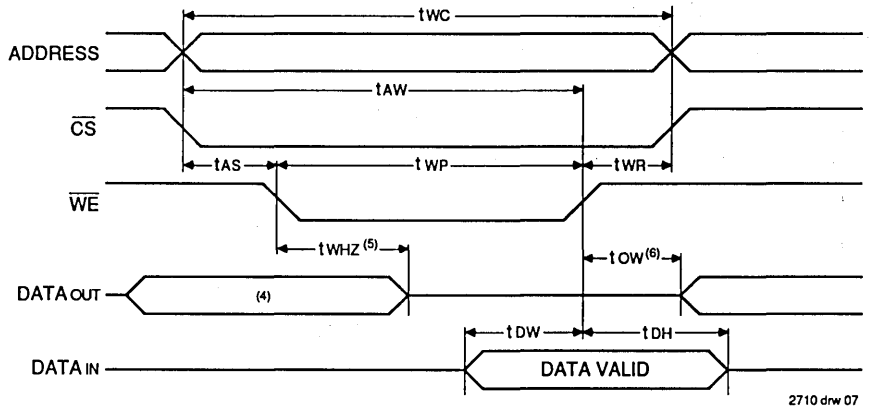


TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3)

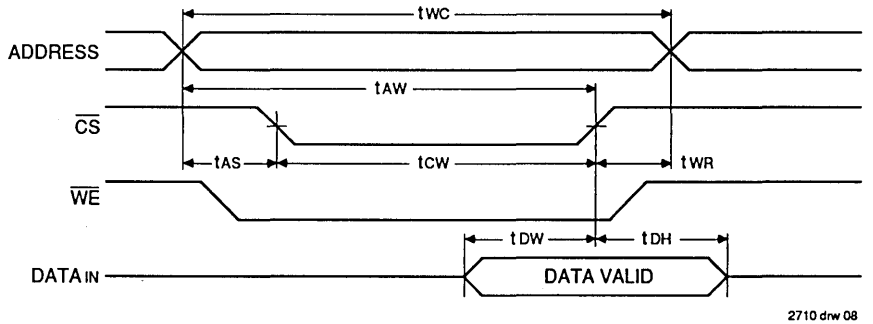


NOTES:
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



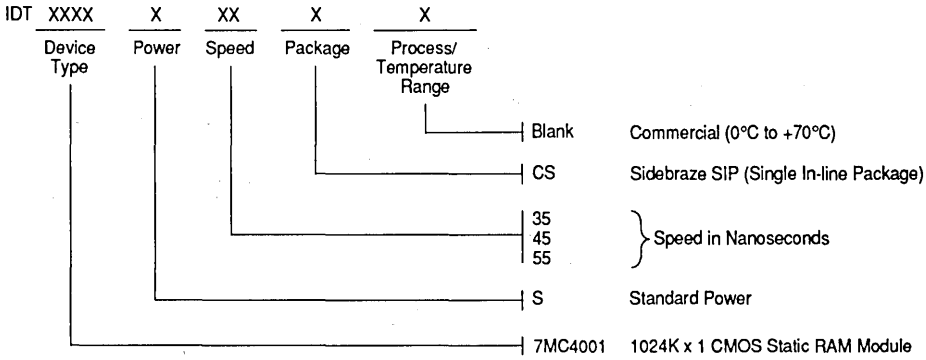
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (twp) of a low $\overline{CS}$and a low $\overline{WE}$.
3. twr is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going High to the end of write cycle.
4. During this period, I/O pins are in the output state and inputs signals must not be applied.
5. If the $\overline{CS}$ Low transition occurs simultaneously with or after the $\overline{WE}$ Low transitions, the outputs remain in a high impedance state.
6. Transition is measured ±500mV from steady state. This parameter is graranteed by design, but not tested.

8

ORDERING INFORMATION



2710 drw 09

Integrated Device Technology, Inc.

256K X 4 CMOS STATIC RAM MODULE

PRELIMINARY
IDT7M4042

FEATURES:

- High density 1 megabit CMOS static RAM module
- Equivalent to the JEDEC standard for future monolithic 256K x 4 with output enable static RAMs
- Fast access time
  - — Commercial: 30ns (max.)
  - — Military: 35ns (max.)
- Surface mounted leadless chip carriers on an 28-pin 400 mil ceramic DIP substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B

DESCRIPTION:

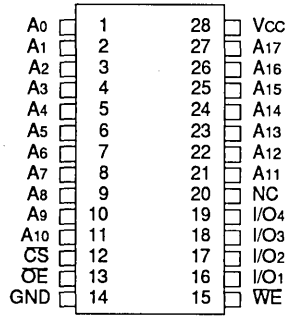
The IDT7M4042 is a (256K x 4 with output enable) static RAM module constructed on a co-fired ceramic substrate using four (64K x 4) static RAMs and an IDT74FCT139 decoder in leadless chip carriers. Extremely fast speeds can be achieved using 256K static RAMs and logic fabricated in IDT's high performance, high-reliability CEMOS™ technology. The IDT7M4042 is available with access times as fast as 30ns commercial and 35ns military with minimal power consumption.

The IDT7M4042 is packaged in a 28-pin ceramic DIP. This results in a package 1.6 inches long, 400 mils wide and only 280 mils thick.

All inputs and outputs of the IDT7M4042 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation.

All IDT7M4042 military module semiconductor components are compliant to the latest revision of MIL-STD-883, Class B, making them ideally suited for applications demanding the highest levels of performance and reliability.

PIN CONFIGURATION[1]



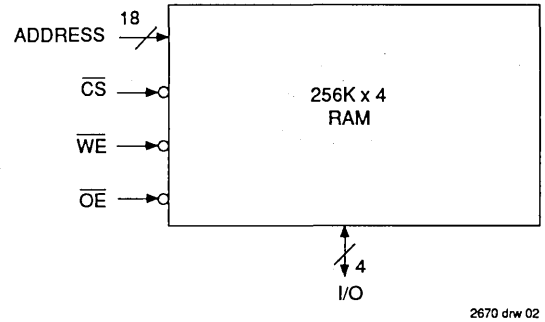
DIP
TOP VIEW

2670 drw 01

NOTE:

1. For module dimensions, please refer to module drawing M2 in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



2670 drw 02

PIN NAMES

I/O1-4	Data Inputs/Outputs
A0-17	Addresses
CS	Chip Select
WE	Write Enable
OE	Output Enable
VCC	Power
GND	Ground

2670 tbl 01

8

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

2670 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

2670 tbl 03

NOTE:
1. VIL = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2670 tbl 04

DC ELECTRICAL CHARACTERISTICS

(Vcc = 5V ± 10%, TA = -55°C to + 125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
ILI	Input Leakage	Vcc = Max. VIN = GND to Vcc	—	40	uA
ILO	Output Leakage	Vcc = Max. $\overline{CS}$ = VIH, VOUT = GND to Vcc	—	40	uA
VOL	Output Low Voltage	Vcc = Min. IOL = 8mA Vcc = Min. IOL = 10mA	— —	0.4 0.5	V V
VOH	Output High Voltage	Vcc = Min. IOH = -4mA	2.4	—	V

2670 tbl 05

Symbol	Parameter	Test Conditions	Max.	Unit
ICC	Dynamic Operating Current	Vcc = Max. $\overline{CS}$ = VIL f = fMAX; Outputs Open	320	mA
ISB	Standby Supply Current	Vcc = Max. $\overline{CS}$ = VIH f = fMAX; Outputs Open	148	mA
ISB1	Full Standby Supply Current	$\overline{CS}$ ≥ Vcc -0.2V VIN > Vcc -0.2V or < 0.2V	122	mA

2670 tbl 06

TRUTH TABLE

Mode	$\overline{CS}$xx	$\overline{WE}$	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	DATAOUT	Active
Write	L	L	High Z	Active

2670 tbl 10

CAPACITANCE(1) (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
CIN(1)	Input Capacitance	VIN = 0V	40	pF
CIN(2)	Input Capacitance ($\overline{CS}$, A16-17)	VIN = 0V	10	pF
COUT	Output Capacitance	VOUT = 0V	40	pF

2670 tbl 11

NOTE:
1. This parameter guaranteed by design, but not tested.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to + 125°C or 0°C to +70°C)

Symbol	Parameters	7M4042S30 Min.	Max.	7M4042S35 Min.	Max.	7M4042S45 Min.	Max.	7M4042S55 Min.	Max.	7M4042S65 Min.	Max.	7M4042S80 Min.	Max.	Unit
Read Cycle														
t_{RC}	Read Cycle Time	30	—	35	—	45	—	55	—	65	—	80	—	ns
t_{AA}	Address Access Time	—	30	—	35	—	45	—	55	—	65	—	80	ns
t_{ACS}	Chip Select Access Time	—	30	—	35	—	45	—	55	—	65	—	80	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	12	—	15	—	27	—	32	—	37	—	47	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Select to Output in High Z	—	18	—	21	—	23	—	28	—	33	—	38	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	10	—	13	—	15	—	15	—	20	—	25	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	3	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	30	—	35	—	45	—	55	—	65	—	80	ns
Write Cycle														
t_{WC}	Write Cycle Time	30	—	35	—	45	—	55	—	65	—	80	—	ns
t_{CW}	Chip Select to End of Write	30	—	30	—	40	—	50	—	60	—	70	—	ns
t_{AW}	Address Valid to End of Write	30	—	30	—	40	—	50	—	60	—	70	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	22	—	30	—	40	—	50	—	60	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	2	—	2	—	2	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	13	—	13	—	15	—	20	—	25	—	30	ns
t_{DW}	Data to Write Time Overlap	15	—	17	—	22	—	27	—	32	—	40	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	5	—	ns

2670 tbl 07

NOTE:
1. This parameter is guaranteed by design, but not tested.

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2670 tbl 08

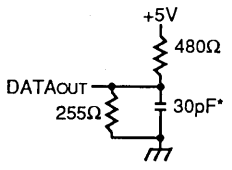
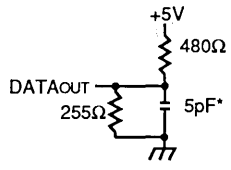


Figure 1. Output Load



2670 drw 03

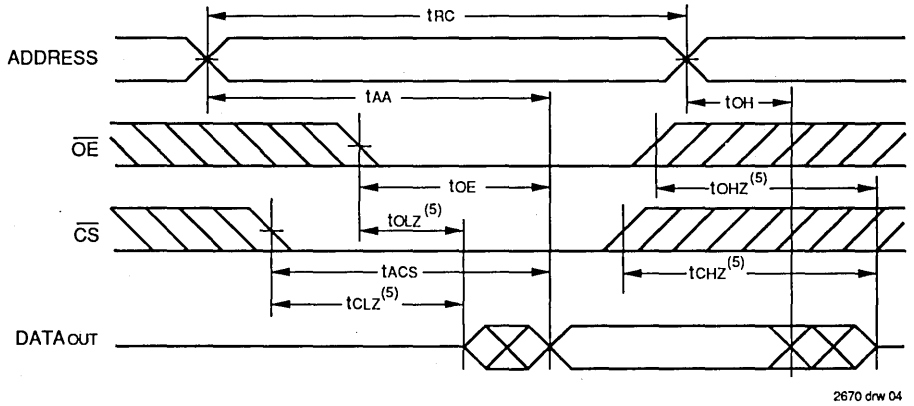
Figure 2. Output Load

(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

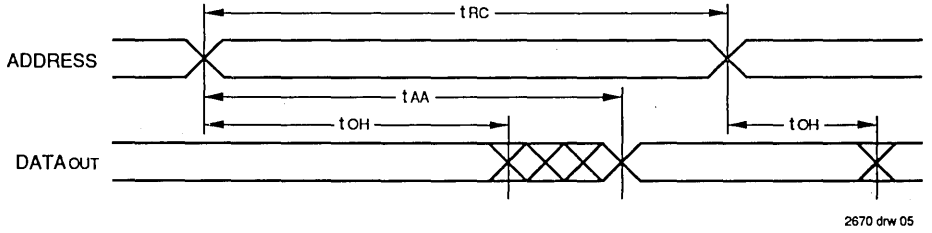
*** Including scope and jig.**

8

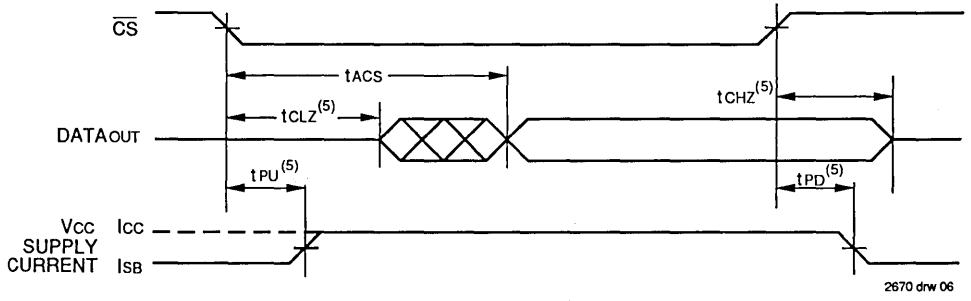
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)

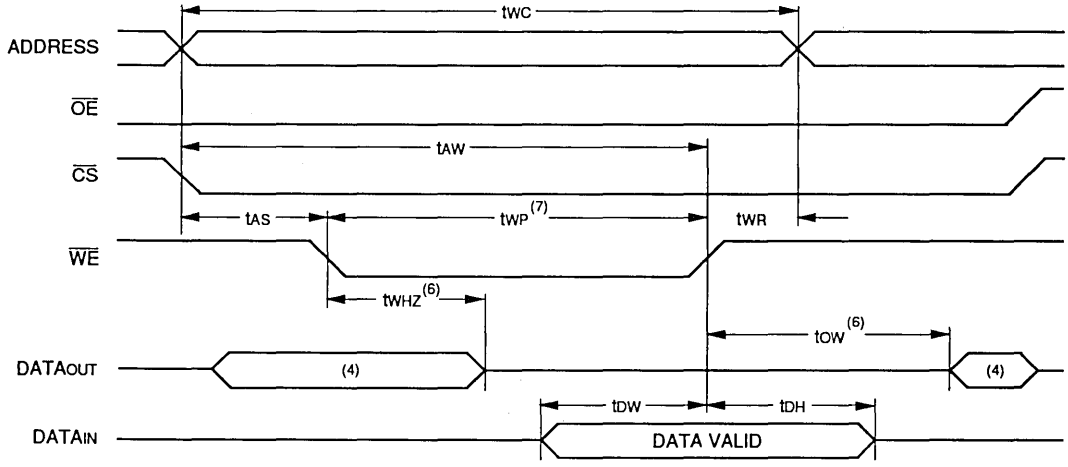


TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



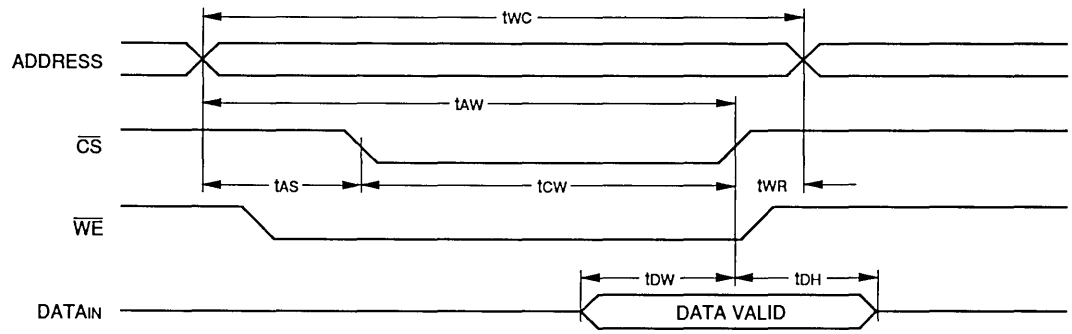
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING) (1, 2, 3, 7)



2670 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING) (1, 2, 3, 5)

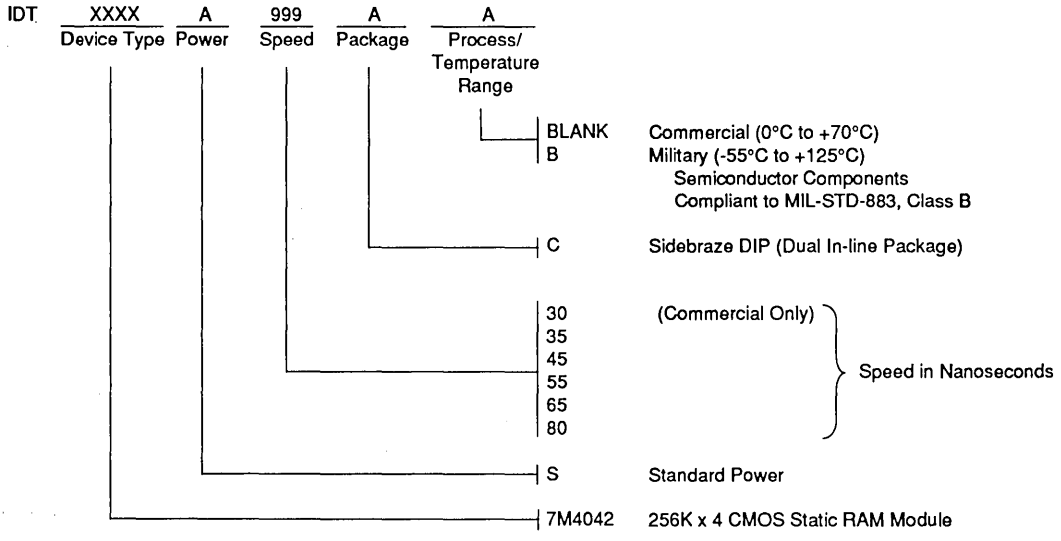


2670 drw 08

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tCW or tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter guaranteed by design, but not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

8

ORDERING INFORMATION



2670 drw 10

Integrated Device Technology, Inc.

64K x 8
64K x 9
CMOS STATIC RAM MODULE

IDT7M812
IDT7M912

FEATURES:

- High-density 512K CMOS static RAM module
- 64K x 8 (IDT7M812) or 64K x 9 (IDT7M912) configuration
- Fast access times
  - — Military: 25ns (max.)
  - — Commercial: 15ns (max.)
- Low power consumption
  - — Active: 2.4W (typ. in 64K x 8 organization)
  - — Standby: 240µW (typ. in 64K x 8 organization)
- Available in 40–pin, 600 mil center sidebraze DIP
- Single 5V (±10%) power supply
- Dual Vcc and GND pins for maximum noise immunity
- Inputs and outputs directly TTL– compatible

DESCRIPTION:

The IDT7M812/IDT7M912 are 512K high-speed CMOS static RAMs constructed on a multi-layered co-fired ceramic substrate using 8 IDT7187 (64K x 1) static RAMs (IDT7M812) or 9 IDT7187 static RAMs (IDT7M912) in leadless chip carriers. Extremely high speeds can be achieved by the use of IDT7187s fabricated in IDT's high-performance, high-reliability technology, CEMOS™.

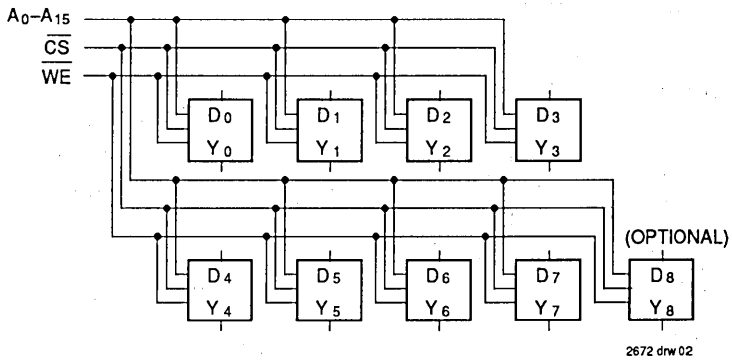
The IDT7M812/IDT7M912 are available with maximum access times as fast as 15ns commercial and 25ns military temperature ranges, with maximum operating power consumption of only 8.9W (IDT7M912, 25ns, 64K x 9 option). The module also offers a standby power mode of 3.2W (max.) and a full standby mode of 1.2W (max.).

The IDT7M812/IDT7M912 are offered in a high-density 40-pin, 600 mil center sidebraze DIP to take full advantage of the compact IDT7187s in leadless chip carriers. The IDT7M912 (64K x 9) option can provide more flexibility in system application for error detection, parity bit, etc.

All inputs and outputs of the IDT7M812/IDT7M912 are TTL–compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

All IDT military module semiconductor components are compliant to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

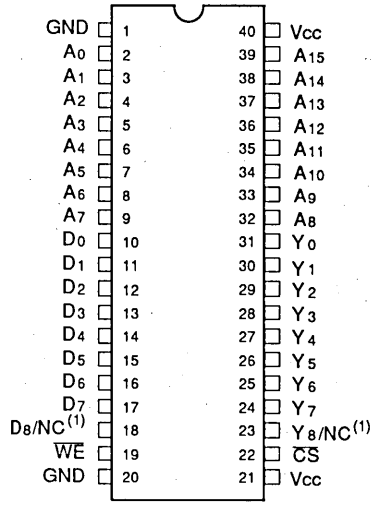
FUNCTIONAL BLOCK DIAGRAM



8

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION (1, 2)



2672 drw 01

TOP VIEW
DIP

NOTES:
1. For the IDT7M912 (64K x 9 version)Pin 18 and Pin 23 are D8 and Y8 respectively. For the IDT7M812 (64K x 8 version), these pins are No Connects.
2. For module dimensions, please refer to drawing M9 and M10 in the packaging section.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	−55°C to +125°C	0V	5.0V ± 10%
Commerical	0°C to +70°C	0V	5.0V ± 10%

2672 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	−0.5(1)	—	0.8	V

NOTE:
1. VIL = −3.0V for pulse width less than 20ns.

2672 tbl 03

PIN NAMES

A0–A15	Address
D0–D8	Data Input
Y0–Y8	Data Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
Vcc	Power
GND	Ground
NC	No Connect

2672 tbl 08

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	DATAOUT	Active
Write	L	L	High Z	Active

2672 tbl 06

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
TA	Operating Temperature	0 to +70	−55 to +125	°C
TBIAS	Temperature Under Bias	−55 to +125	−65 to +135	°C
TSTG	Storage Temperature	−55 to +125	−65 to +155	°C
IOUT	DC Output Current	50	50	mA

NOTE:

2672 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE(1) (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	7M812(2)	7M912(2)	Unit
CIN(D)	Input Capacitance (Data)	VIN = 0V	12	12	pF
CIN(A)	Input Capacitance (Address)	VIN = 0V	72	80	pF
CIN(C)	Input Capacitance ($\overline{CS}$, $\overline{WE}$)	VIN = 0V	72	80	pF
COUT	Output Capacitance	VOUT = 0V	12	12	pF

NOTES:

2672 tbl 07

1. This parameter is guaranteed by design but not tested.
2. Maximum rated values

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address & Control)	V_{CC} = Max.; V_{IN} =GND to V_{CC}	—	40	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max.; V_{IN} =GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max.; $\overline{CS}$ =V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	V_{CC} = Min.; I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min.; I_{OH} = −4mA	2.4	—	V

2672 tbl 09

Symbol	Parameter	Test Conditions	IDT7M812				IDT7M912				Unit
			Min.	Typ.[1]	Max.[3]	Max.[2]	Min.	Typ.[1]	Max.[3]	Max.[2]	
I_{CC1}	Operating Current	f = 0; $\overline{CS}$ = V_{IL} V_{CC} = Max.; Output Open	—	520	1080	1120	—	580	1215	1260	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max.; $\overline{CS}$ = V_{IL}; f = f_{MAX} Output Open	—	520	1440	1400	—	580	1620	1575	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max. f = f_{MAX}, Outputs Open	—	280	520	520	—	310	585	585	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} − 0.2V; V_{IN} > V_{CC} − 0.2V or < 0.2V	—	0.1	200	200	—	0.4	225	225	mA

NOTES:

2672 tbl 04

1. V_{CC} = 5.0V, T_A = +25°C.
2. t_{AA} = 20, 25, 30, 35, 45, 55, 65ns.
3. t_{AA} = 15ns.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 and 3

2672 tbl 10

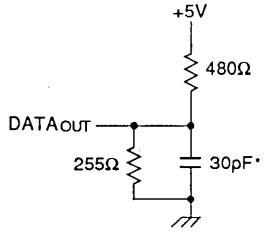


Figure 1. Output Load

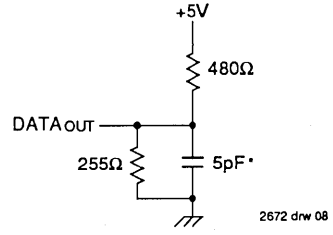


Figure 2. Output Load
(for t_{OHZ}, t_{OLZ}, t_{WHZ}, and t_{OW})

* Including scope and jig.

8

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = −55°C to +125°C and 0° to +70°C)

Symbol	Parameter	7M812S15 7M912S15 (Com'l. Only)		7M812S20 7M912S20 (Com'l. Only)		7M812S25 7M912S25		7M812S30 7M912S30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	15	—	20	—	25	—	30	—	ns
t_{AA}	Address Access Time	—	15	—	20	—	25	—	30	ns
t_{ACS}	Chip Select Access Time	—	15	—	20	—	25	—	30	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{OLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{OHZ}[1]	Chip Deselect to Output in High Z	—	6	—	6	—	20	—	25	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	15	—	20	—	25	—	30	ns
Write Cycle										
t_{WC}	Write Cycle Time	12	—	15	—	25	—	30	—	ns
t_{CW}	Chip Select to End of Write	12	—	15	—	23	—	28	—	ns
t_{AW}	Address Valid to End of Write	12	—	15	—	23	—	28	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	3	—	3	—	ns
t_{WP}	Write Pulse Width	12	—	15	—	20	—	25	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data to Write Time Overlap	8	—	10	—	15	—	20	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	5	—	5	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	6	—	8	0	20	0	25	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

AC ELECTRICAL CHARACTERISTICS (Cont'd.)

(V_{CC} = 5V ±10%, T_A = −55°C to +125°C and 0° to +70°C)

Symbol	Parameter	7M812S35 7M912S35		7M812S45 7M912S45		7M812S55 7M912S55		7M812S65 7M912S65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	35	—	45	—	55	—	65	—	ns
t_{AA}	Address Access Time	—	35	—	45	—	55	—	65	ns
t_{ACS}	Chip Select Access Time	—	35	—	45	—	55	—	65	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{OLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{OHZ}[1]	Chip Deselect to Output in High Z	—	25	—	30	—	30	—	30	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	35	—	35	—	35	—	35	ns
Write Cycle										
t_{WC}	Write Cycle Time	35	—	45	—	55	—	65	—	ns
t_{CW}	Chip Select to End of Write	35	—	40	—	50	—	55	—	ns
t_{AW}	Address Valid to End of Write	35	—	40	—	50	—	55	—	ns
t_{AS}	Address Set-up Time	5	—	5	—	5	—	5	—	ns
t_{WP}	Write Pulse Width	30	—	30	—	35	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data to Write Time Overlap	20	—	25	—	25	—	30	—	ns
t_{DH}	Data Hold from Write Time	5	—	5	—	5	—	5	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	0	25	0	30	0	30	0	35	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

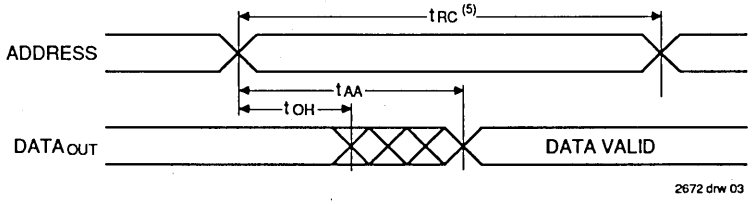
NOTE:

1. This parameter is guaranteed by design, but not tested.

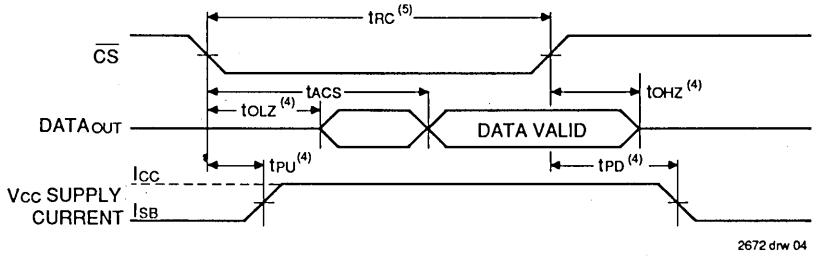
2672 tbl 05

8

TIMING WAVEFORM OF READ CYCLE NO. 1(1,2)

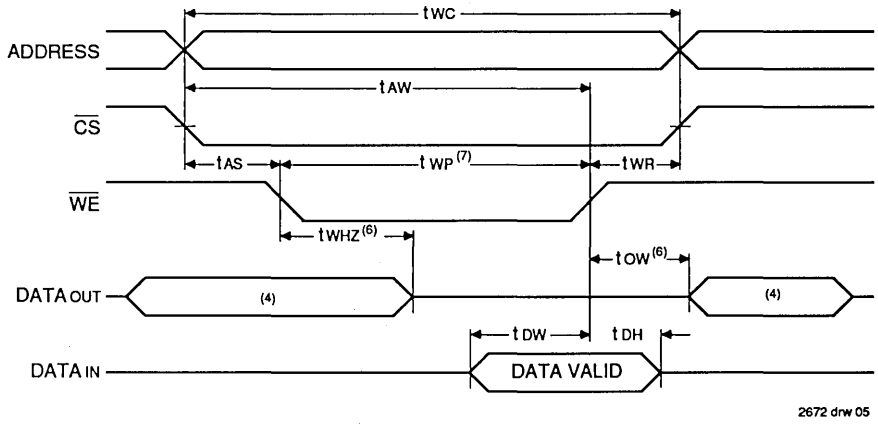


TIMING WAVEFORM OF READ CYCLE NO. 2(1,3)

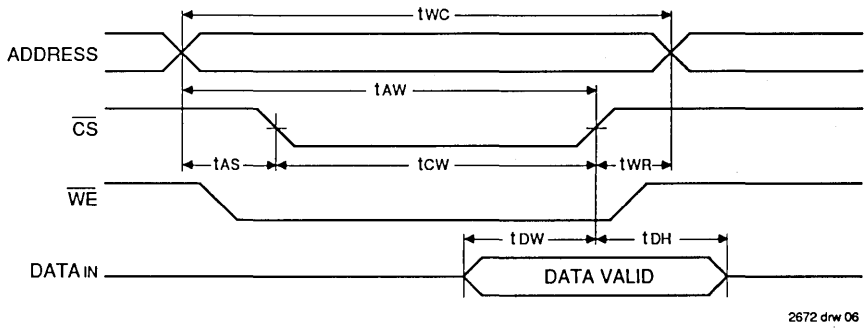


NOTES:
1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is guaranteed by design, but not tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1,2,3,7)



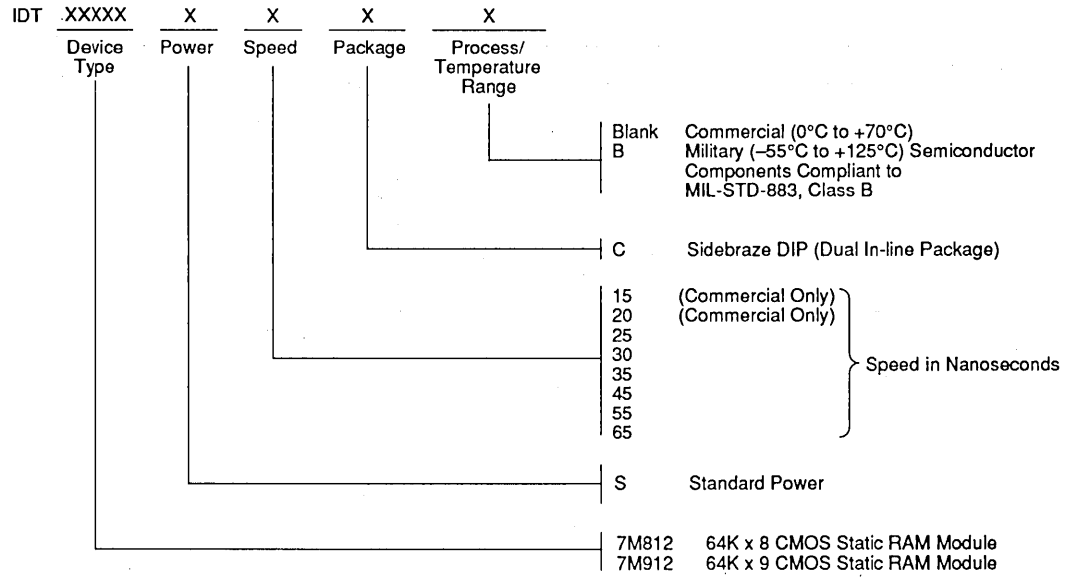
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,3,5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transactions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.

8

ORDERING INFORMATION



Integrated Device Technology, Inc.

128K X 8 CMOS STATIC RAM MODULE

IDT8M824S

FEATURES:

- High-density 1 megabit (128K x 8)CMOS static RAM module
- High-speed
  - — Military: 35ns (max.)
  - — Commercial: 25ns (max.)
- Low power consumption
  - — Active: less than 550mW (typ.)
  - — Standby: less than 20mW (typ.)
- Offered in the JEDEC standard 32-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

The IDT8M824S is a 128K x 8 high-speed CMOS static RAM constructed on a co-fired ceramic substrate using four 32K x 8 static RAMs and a FCT139 decoder in leadless chip carriers. Functional equivalence to monolithic one megabit static RAMs is achieved by utilization of an on board decoder that interprets the higher order address A_{15} and A_{16} to select one of the four 32K x 8 RAMs. Extremely fast speeds can be achieved with this technique due to use of 256K static RAMs and the decoder fabricated in IDT's high-performance, high-reliability CEMOS technology.

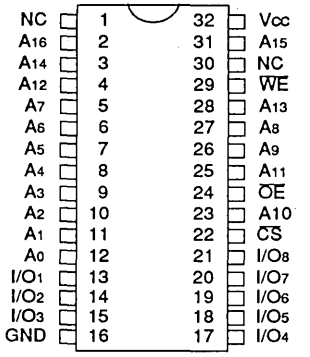
The IDT8M824S is available with maximum access times as fast as 25ns for commercial temperature range, with maximum power consumption of 2.5 watts. The module offers a full standby mode of 440mW (max.).

The IDT8M824S is offered in a 32-pin, 600 mil center sidebraze DIP, adhering to JEDEC standards for one megabit monolithic pinouts.

All inputs and outputs of the IDT8M824S are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

All IDT military module semiconductor components are manufactured in compliance to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION (1)



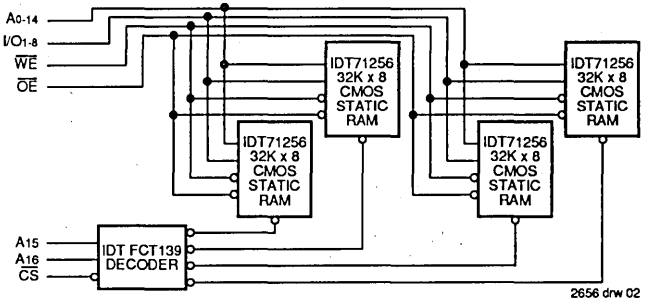
DIP
TOP VIEW

2656 drw 01

2656 drw 01

NOTE:
1. For module dimensions, please refer to module drawing M6 and M7 in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



2656 drw 02

PIN NAMES

A_{0-16}	Addresses
I/O_{1-8}	Data Input/Output
$\overline{CS}$	Chip Select
Vcc	Power
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground

2656 tbl 01

8

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2656 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2656 tbl 03

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2656 tbl 04

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to + 125°C and 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	IDT8M824S Typ.(1)	IDT8M824S Max.(2)	IDT8M824S Max.(3)	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	—	20	40	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	—	20	40	uA
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ = V_{IL}, f = f_{MAX}, Output Open	—	150	450	265	mA
I_{SB}	Standby Supply Current	V_{CC} = MAX. $\overline{CS}$ = V_{IH} f = fmax, Outputs open	—	10	280	85	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} -0.2V V_{IN} > V_{CC} -0.2V or < 0.2V	—	10	80	80	mA
V_{OL}	Output Low Voltage	V_{CC} = Min. I_{OL} = 8mA	—	—	0.4	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min. I_{OH} = -4mA	2.4	—	—	—	V

2656 tbl 05

NOTES:
1. V_{CC} = 5V, T_A = +25°C.
2. tAA = 25ns.
3. tAA = 30, 35, 40, 45, 50, 60, 70, 85, 100ns.

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2656 tbl 06

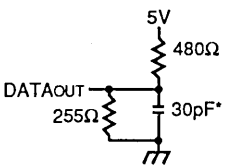
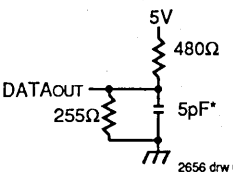


Figure 1. Output Load



2656 drw 03

Figure 2. Output Load
(for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

(VCC = 5V ± 10%, TA = -55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	8M824S25 (Com'l. Only) Min.	Max.	8M824S30 (Com'l. Only) Min.	Max.	8M824S35 Min.	Max.	8M824S40 Min.	Max.	8M824S45 Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
tAA	Address Access Time	—	25	—	30	—	35	—	40	—	45	ns
tACS	Chip Select Access Time	—	25	—	30	—	35	—	40	—	45	ns
tCLZ1,2[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	10	—	11	—	13	—	25	—	25	ns
tOLZ[1]	Output Enable to Output in Low Z	2	—	2	—	2	—	5	—	5	—	ns
tCHZ[1]	Chip Select to Output in High Z	—	15	—	16	—	20	—	20	—	20	ns
tOHZ[1]	Output Disable to Output in High Z	—	8	—	10	—	15	—	20	—	20	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
tPU[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
tPD[1]	Chip Deselect to Power-Down Time	—	25	—	30	—	35	—	40	—	45	ns
Write Cycle												
tWC	Write Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
tCW	Chip Select to End of Write	20	—	25	—	30	—	35	—	40	—	ns
tAW	Address Valid to End of Write	20	—	25	—	30	—	35	—	40	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	5	—	5	—	ns
tWP	Write Pulse Width	15	—	20	—	23	—	30	—	35	—	ns
tWR	Write Recovery Time	0	—	0	—	2	—	5	—	5	—	ns
tWHZ[1]	Write Enable to Output in High Z	—	10	—	11	—	15	—	15	—	15	ns
tDW	Data to Write Time Overlap	11	—	13	—	14	—	15	—	20	—	ns
tDH	Data Hold from Write Time	3	—	3	—	3	—	3	—	5	—	ns
tOW[1]	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

2656 tbl 07

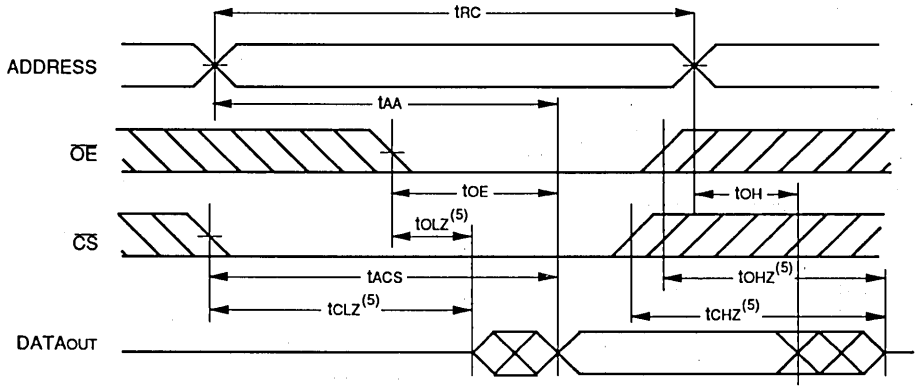
Symbol	Parameter	8M824S50 Min.	Max.	8M824S60 (Mil. Only) Min.	Max.	8M824S70 (Mil. Only) Min.	Max.	8M824S85 (Mil. Only) Min.	Max.	8M824S100 (Mil. Only) Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	50	—	60	—	70	—	85	—	100	—	ns
tAA	Address Access Time	—	50	—	60	—	70	—	85	—	100	ns
tACS	Chip Select Access Time	—	50	—	60	—	70	—	85	—	100	ns
tCLZ1,2[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	30	—	35	—	40	—	50	—	60	ns
tOLZ[1]	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
tCHZ[1]	Chip Select to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
tOHZ[1]	Output Disable to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
tPU[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
tPD[1]	Chip Deselect to Power-Down Time	—	50	—	60	—	70	—	85	—	100	ns
Write Cycle												
tWC	Write Cycle Time	50	—	60	—	70	—	85	—	100	—	ns
tCW	Chip Select to End of Write	45	—	55	—	65	—	75	—	90	—	ns
tAW	Address Valid to End of Write	45	—	55	—	65	—	75	—	90	—	ns
tAS	Address Set-up Time	5	—	5	—	5	—	5	—	5	—	ns
tWP	Write Pulse Width	40	—	50	—	60	—	70	—	80	—	ns
tWR	Write Recovery Time	5	—	5	—	5	—	10	—	10	—	ns
tWHZ[1]	Write Enable to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
tDW	Data to Write Time Overlap	20	—	25	—	30	—	35	—	40	—	ns
tDH	Data Hold from Write Time	5	—	5	—	5	—	5	—	5	—	ns
tOW[1]	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

2656 tbl 08

NOTE:
1. This parameter guaranteed by design but not tested.

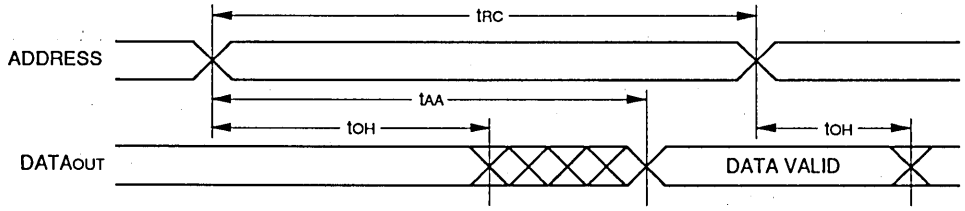
8

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



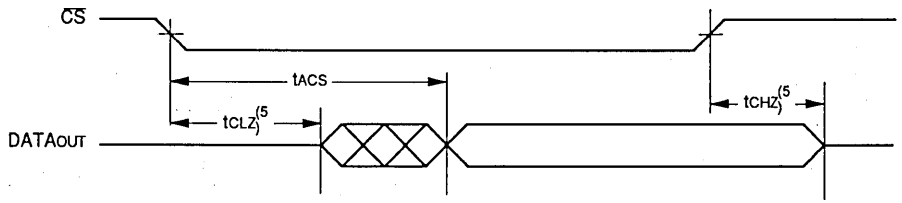
TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)

2656 drw 04



2656 drw 05

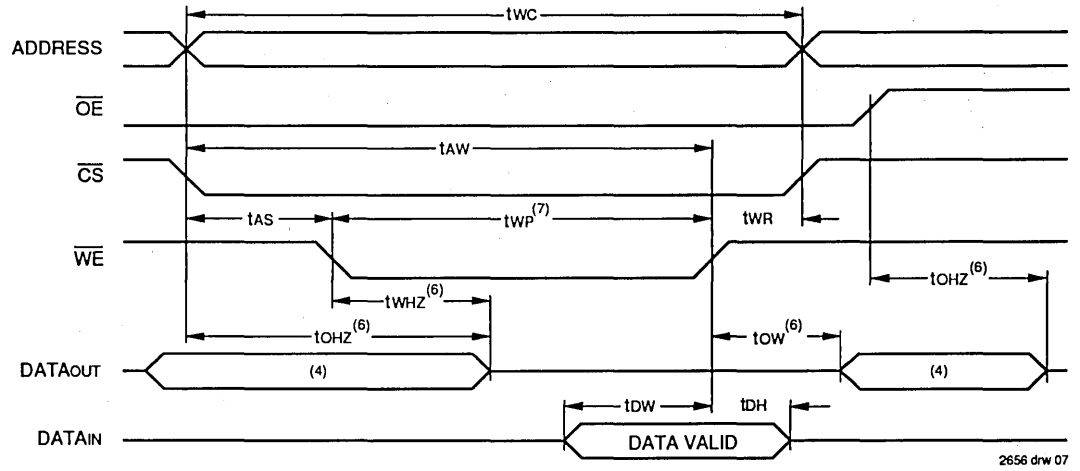
TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)



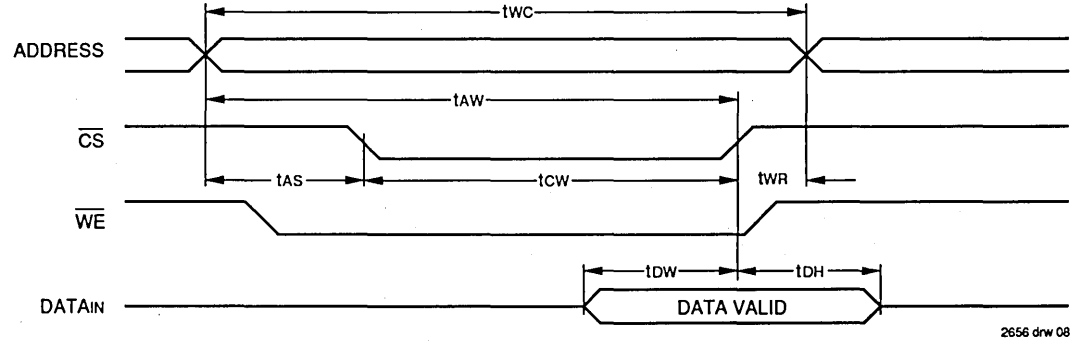
2656 drw 06

NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1,2,3,7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,3,5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter guaranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse (tWP > tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

8

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	DOUT	Active
Read	L	H	H	High Z	Active
Write	L	X	L	DIN	Active

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
CIN(D)	Input Capacitance (data)	VIN = 0V	35	50	pF
CIN(AC1)	Input Capacitance (A0-14, $\overline{OE}$, $\overline{WE}$)	VIN = 0V	35	50	pF
CIN(AC2)	Input Capacitance (A15-16, $\overline{CS}$)	VOUT = 0V	—	14	pF
COUT	Output Capacitance	VOUT = 0V	35	50	pF

NOTE:
1. This parameter is guaranteed by design but not tested.

ORDERING INFORMATION

IDT XXXX / Device Type — A / Power — 999 / Speed — A / Package — A / Process/ Temperature Range

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Semiconductor Components Compliant to MIL-STD-883, Class B
C	LCCs on a Sidebraze DIP (Dual In-line Package)
N	SOICs on a Sidebraze DIP (Dual In-line Package)
25	(Commercial Only) — Speed in Nanoseconds
30	(Commercial Only) — Speed in Nanoseconds
35	Speed in Nanoseconds
40	Speed in Nanoseconds
45	Speed in Nanoseconds
50	Speed in Nanoseconds
60	(Military Only) — Speed in Nanoseconds
70	(Military Only) — Speed in Nanoseconds
85	(Military Only) — Speed in Nanoseconds
100	(Military Only) — Speed in Nanoseconds
S	Standard Power
8M824	128K x 8 CMOS Static RAM Module

2656 Drw 09

Integrated Device Technology, Inc.

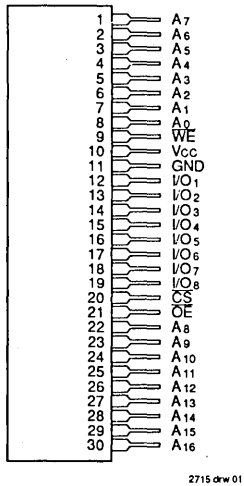
128K x 8 CMOS STATIC RAM MODULE

IDT8MP824S

FEATURES:

- High-density 1 megabit CMOS static RAM module
- Fast access time
  — 25ns (max.)
- Low-power consumption
  — Active: less than 500mW (typ.)
  — Standby: less than 8.8mW (typ.)
- Cost-effective plastic surface-mounted RAM packages on an epoxy laminate (FR-4) substrate
- Offered in a 30-pin SIP (Single In-line Package) for maximum space-saving
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

PIN CONFIGURATION[1]



2715 drw 01

SIP
BACK VIEW

DESCRIPTION:

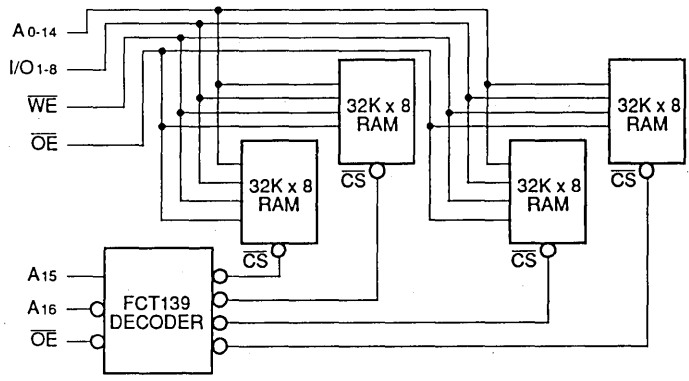
The IDT8MP824S is (128K x 8) high-speed CMOS static RAM module constructed on an epoxy laminate substrate using four 32K x 8 static RAMs in plastic surface mount packages. Functional equivalence to proposed monolithic one megabit static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A15 and A16 to select one of the four 32K x 8 RAMs. Extremely fast speeds can be achieved with this technique due to use of 256K static RAMs and decoder fabricated in IDT's high-performance, high-reliability CEMOS™ technology.

The IDT8MP824S is available with maximum access times as fast as 25ns over the commercial temperature range, with maximum operating power consumption of 825mW. The module also offers a full standby mode of 330mW (max.).

The IDT8MP824S is offered in a 30-pin SIP (single in-line) package. For the 32-pin JEDEC standard DIP, refer to the IDT8M824S module.

All inputs and outputs of the IDT8MP824S are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



2715 drw 02

8

NOTE:
1. For module dimensions, please refer to module drawing M36 in the packaging section.

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN NAMES

A_{0-16}	Addresses
I/O_{1-8}	Data Input/Output
$\overline{CS}$	Chip Select
V_{CC}	Power
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground

2715 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

2715 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2715 tbl 03

NOTE:
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND VOLTAGE SUPPLY

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2715 tbl 04

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT8MP824S Min.	IDT8MP824S Typ.(1)	IDT8MP824S Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	—	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	—	15	µA
I_{CC}	Dynamic Operating Current	$\overline{CS}$ = V_{IL} V_{CC} = Max., Output Open f = f_{MAX}	—	100	200	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} V_{CC} = Max. Output Open	—	2	80	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}$ ≥ V_{HC}, V_{IN} ≥ V_{HC} or ≤ V_{LC} V_{CC} = Max., Output Open	—	1.6	60	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	—	V

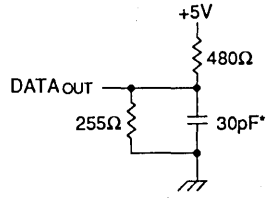
2715 tbl 05

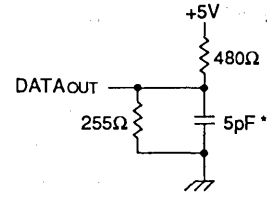
NOTE:
1. V_{CC} = 5V, T_A = +25°C

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2715 tbl 06





2715 drw 03

Figure 1. Output Load

Figure 2. Output Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

* Including scope and jig

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

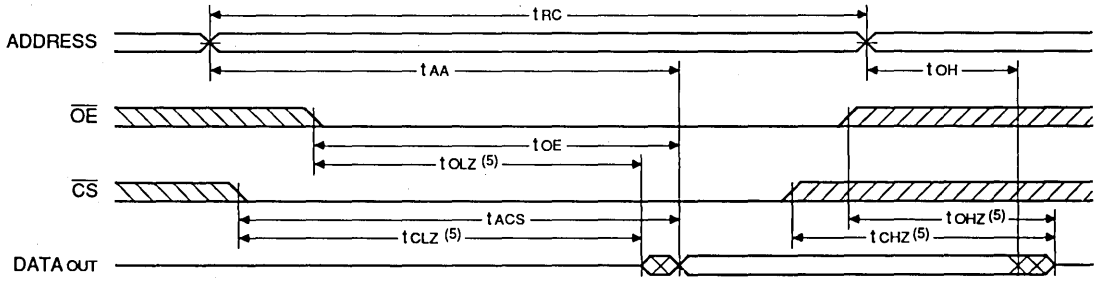
Symbol	Parameters	8MP824S25 Min.	8MP824S25 Max.	8MP824S30 Min.	8MP824S30 Max.	8MP824S35 Min.	8MP824S35 Max.	8MP824S40 Min.	8MP824S40 Max.	8MP824S45 Min.	8MP824S45 Max.	8MP824S50 Min.	8MP824S50 Max.	Unit
READ CYCLE														
t_{RC}	Read Cycle Time	25	—	30	—	35	—	40	—	45	—	50	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	—	40	—	45	—	50	ns
t_{ACS}	Chip Select Access Time	—	25	—	30	—	35	—	40	—	45	—	50	ns
t_{CLZ} (1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	10	—	11	—	13	—	25	—	25	—	30	ns
t_{OLZ} (1)	Output Enable to Output in Low Z	2	—	2	—	2	—	5	—	5	—	5	—	ns
t_{CHZ} (1)	Chip Select to Output in High Z	—	15	—	16	—	20	—	20	—	20	—	20	ns
t_{OHZ} (1)	Output Disable to Output in High Z	—	8	—	10	—	15	—	20	—	20	—	20	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{PU} (1)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD} (1)	Chip Deselect to Power Down Time	—	25	—	30	—	35	—	40	—	45	—	50	ns
WRITE CYCLE														
t_{WC}	Write Cycle Time	25	—	30	—	35	—	40	—	45	—	50	—	ns
t_{CW}	Chip Select to End of Write	20	—	25	—	30	—	35	—	40	—	45	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	30	—	35	—	40	—	45	—	ns
t_{AS}	Address Setup Time	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	23	—	30	—	35	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	2	—	5	—	5	—	5	—	ns
t_{WHZ} (1)	Write Enable to Output in High Z	—	10	—	11	—	15	—	15	—	15	—	20	ns
t_{DW}	Data to Write Time Overlap	11	—	13	—	14	—	15	—	20	—	20	—	ns
t_{DH}	Data Hold from Write Time	3	—	3	—	3	—	3	—	5	—	5	—	ns
t_{OW} (1)	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	5	—	ns

2715 tbl 07

NOTE:
1. This parameter is guaranteed by design but not tested.

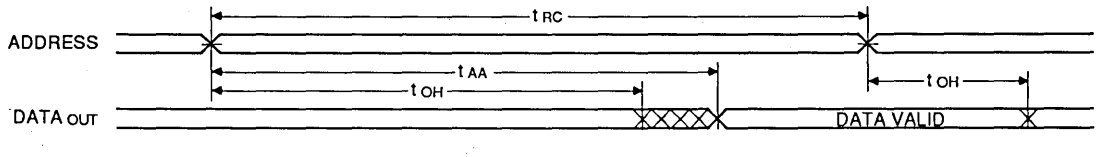
8

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



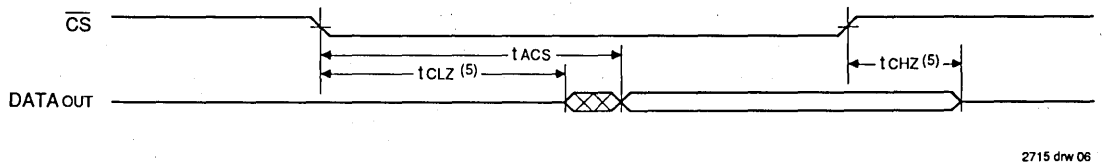
2715 drw 04

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2715 drw 05

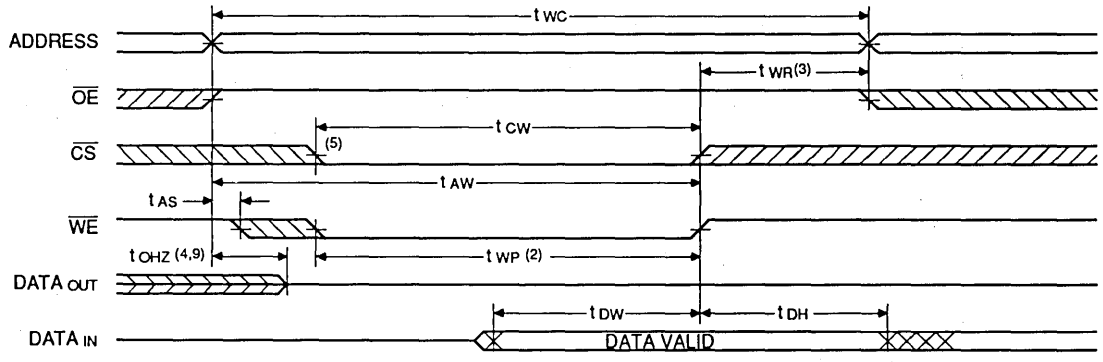
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



2715 drw 06

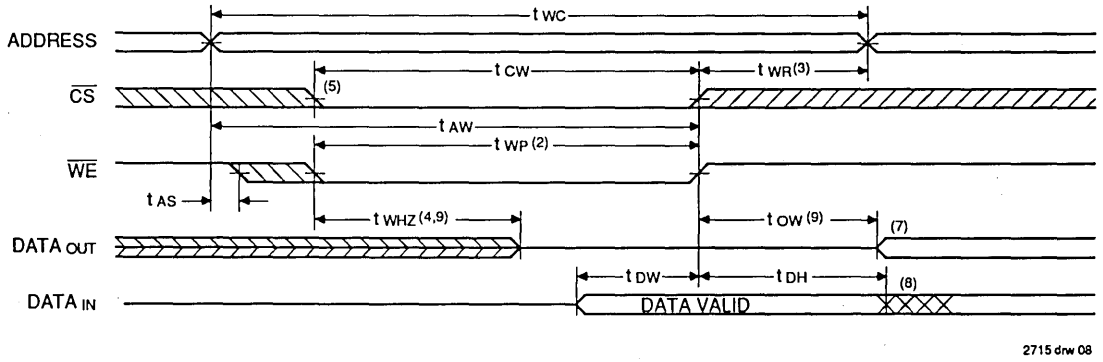
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1)



2715 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 2(1, 6)



2715 drw 08

NOTES:
1. $\overline{WE}$, $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWP is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = VIL).
7. DOUT is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state. This parameter is guaranteed by design but not tested.

8

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	DOUT	Active
Read	L	H	H	High Z	Active
Write	L	X	L	DIN	Active

2715 tbl 08

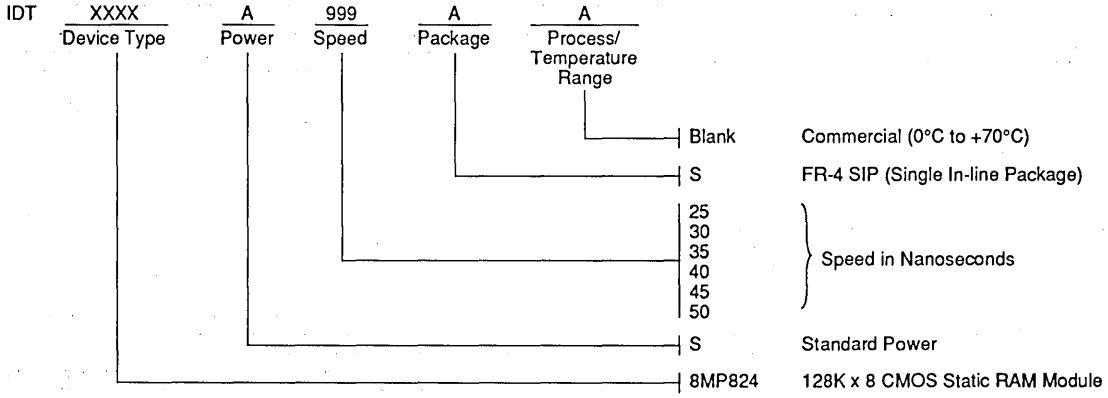
CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	35	pF
COUT	Output Capacitance	VOUT = 0V	40	pF

2715 tbl 09

NOTE:
1. This parameter is guaranteed by design but not tested.

ORDERING INFORMATION



2715 drw 10

Integrated Device Technology, Inc.

128K x 8 CMOS STATIC RAM MODULE

IDT8MP824L

FEATURES:

- High-density 1 megabit CMOS static RAM module
- Fast access time
  — 70ns (max.)
- Low-power consumption
  — Active: less than 400mW (typ.)
  — Standby: less than 50µW (typ.)
- Cost-effective plastic surface-mounted RAM packages on an epoxy laminate (FR-4) substrate
- Offered in a 30-pin SIP (Single In-line Package) for maximum space-savings
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

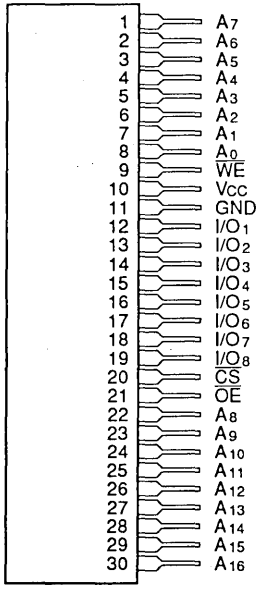
The IDT8MP824L is 128K x 8 high-speed CMOS static RAM constructed on an epoxy laminate substrate using four 32K x 8 static RAMs in plastic surface mount packages. Functional equivalence to proposed monolithic one megabit static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A_{15} and A_{16} to select one of the four 32K x 8 RAMs.

The IDT8MP824L is available with maximum access times as fast as 70ns for commercial range, with maximum power consumption of 660mW. The module also offers a full standby mode of 2.2mW (max.).

The IDT8MP824L is offered in a 30-pin SIP (Single In-line Package). For the 32-pin JEDEC sidebrazed DIP, refer to the IDT8M824S module.

All inputs and outputs of the IDT8MP824L are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

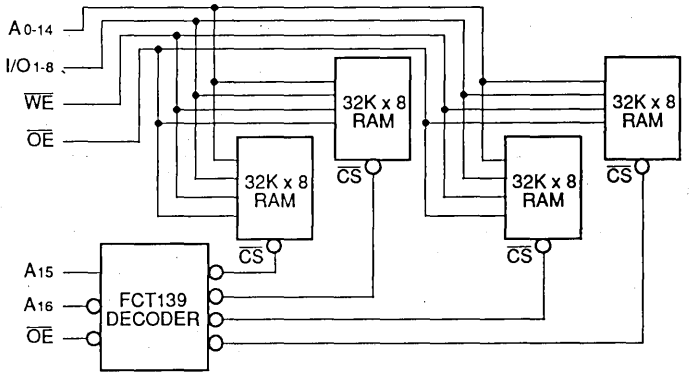
PIN CONFIGURATION[1]



2716 drw 01

SIP
BACK VIEW

FUNCTIONAL BLOCK DIAGRAM



2716 drw 02

PIN NAMES

A_{0-16}	Addresses
I/O_{1-8}	Data Input/Output
$\overline{CS}$	Chip Select
Vcc	Power Supply
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground

2716 tbl 01

NOTE:
1. For module dimensions, please refer to module drawing M36 in the packaging section.

8

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE: 2716 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2716 tbl 03

1. V_{IL} (min.) = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND VOLTAGE SUPPLY

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2716 tbl 04

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT8MP824L Min.	Typ.[1]	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	—	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	—	15	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS} \le V_{IL}$ V_{CC} = Max., Output Open f = 0	—	10	80	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS} \le V_{IL}$ V_{CC} = Max., Output Open f = f_{MAX}	—	80	120	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \ge V_{IH}$ V_{CC} = Max., Output Open f = f_{MAX}	—	6	12	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} > V_{CC}$ - 0.2V $V_{IN} > V_{CC}$ - 0.2V or < 0.2V	—	10	400	µA
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA, V_{CC} = Min.	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA, V_{CC} = Min.	2.4	—	—	V

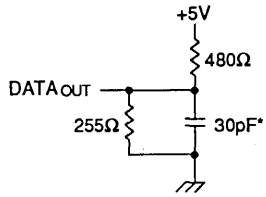
NOTE: 2716 tbl 05

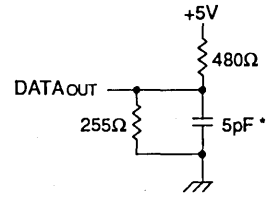
1. V_{CC} = 5V, T_A = +25°C

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2716 tbl 06





2716 drw 03

Figure 1. Output Load

Figure 2. Output Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

* Including scope and jig

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameters	IDT8MP824L70 Min.	IDT8MP824L70 Max.	IDT8MP824L85 Min.	IDT8MP824L85 Max.	IDT8MP824L100 Min.	IDT8MP824L100 Max.	Unit
READ CYCLE								
t_{RC}	Read Cycle Time	70	—	85	—	100	—	ns
t_{AA}	Address Access Time	—	70	—	85	—	100	ns
t_{ACS}	Chip Select Access Time	—	70	—	85	—	100	ns
t_{CLZ} (1)	Chip Select to Output in Low Z	10	—	10	—	10	—	ns
t_{OE}	Output Enable to Output Valid	—	40	—	50	—	60	ns
t_{OLZ} (1)	Output Enable to Output in Low Z	5	—	5	—	5	—	ns
t_{CHZ} (1)	Chip Select to Output in High Z	—	30	—	35	—	40	ns
t_{OHZ} (1)	Output Disable to Output in High Z	—	30	—	35	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	ns
t_{PU} (1)	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD} (1)	Chip Deselect to Power Down Time	—	70	—	85	—	100	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	70	—	85	—	100	—	ns
t_{CW}	Chip Select to End of Write	65	—	75	—	90	—	ns
t_{AW}	Address Valid to End of Write	65	—	75	—	90	—	ns
t_{AS}	Address Setup Time	5	—	5	—	5	—	ns
t_{WP}	Write Pulse Width	60	—	70	—	80	—	ns
t_{WR}	Write Recovery Time	5	—	5	—	5	—	ns
t_{WHZ} (1)	Write Enable to Output in High Z	—	30	—	35	—	40	ns
t_{DW}	Data to Write Time Overlap	30	—	35	—	40	—	ns
t_{DH}	Data Hold from Write Time	5	—	5	—	5	—	ns
t_{OW} (1)	Output Active from End of Write	5	—	5	—	5	—	ns

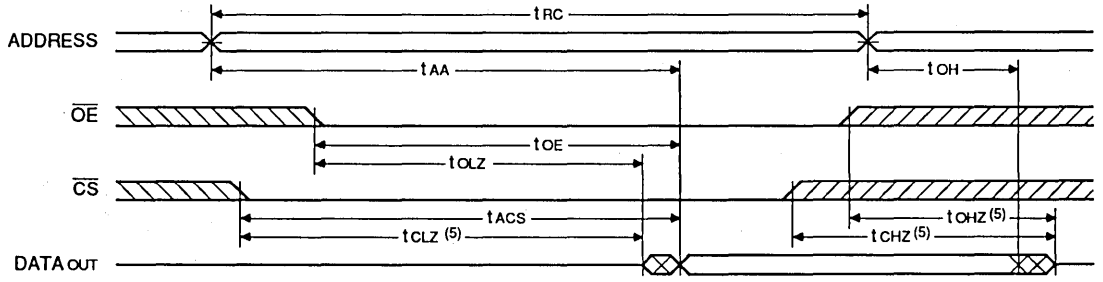
NOTE:

1. This parameter is guaranteed by design but not tested.

2716 tbl 07

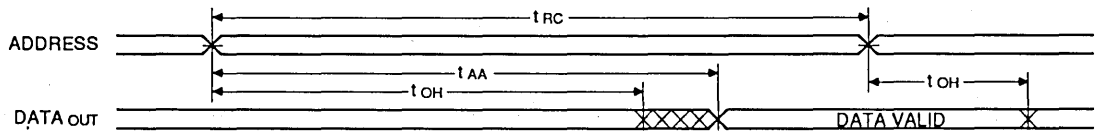
8

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



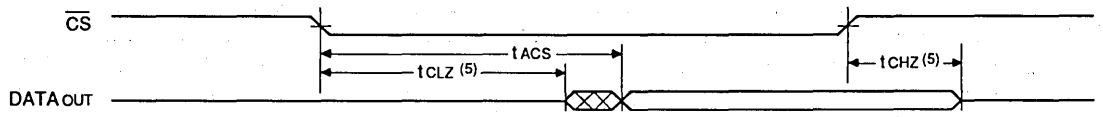
2716 drw 04

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2716 drw 05

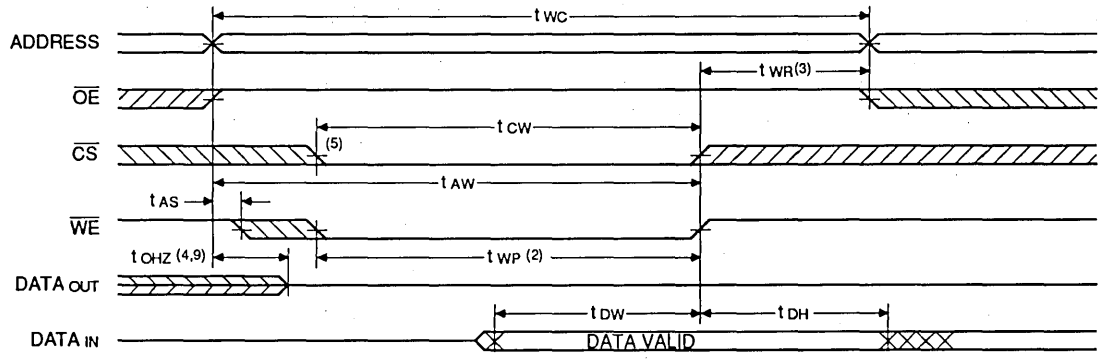
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



2716 drw 06

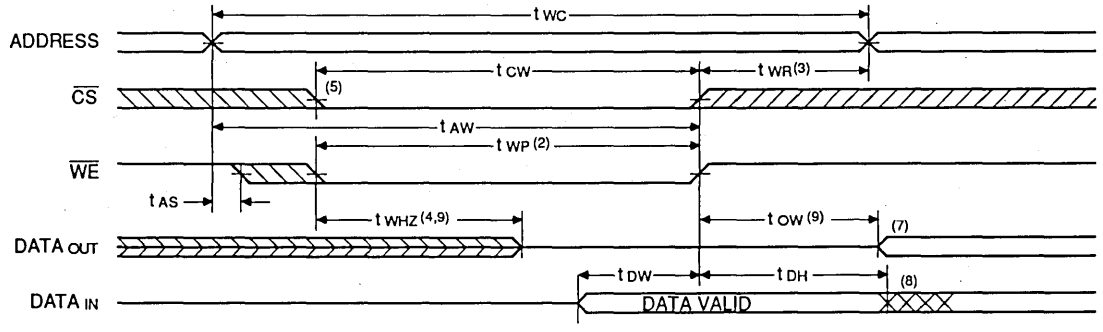
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1)



2716 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 2(1, 6)



2716 drw 08

NOTES:
1. $\overline{WE}$, $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$.
3. tWP is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = VIL).
7. DOUT is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state. This parameter is guaranteed by design but not tested.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	DOUT	Active
Read	L	H	H	High Z	Active
Write	L	X	L	DIN	Active

2716 tbl 08

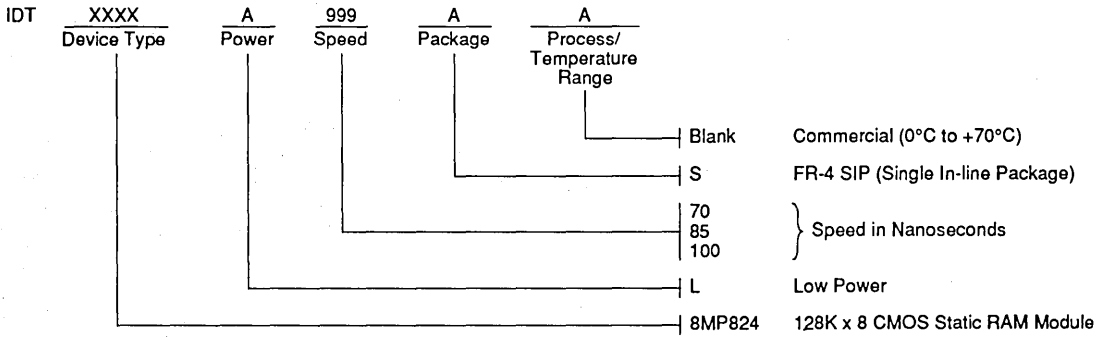
CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	35	pF
COUT	Output Capacitance	VOUT = 0V	40	pF

NOTE:
1. This parameter is guaranteed by design but not tested.

2716 tbl 09

ORDERING INFORMATION



2716 drw 10

Integrated Device Technology, Inc.

256K x 8 CMOS STATIC RAM MODULE

PRELIMINARY
IDT7MP4034

FEATURES:

- High density separate I/O, 2 megabit CMOS static RAM module
- Fast access time: 20ns (max.)
- Low profile 42-pin ZIP (Zig-zag In-line Package)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (+10%) power supply
- Inputs/outputs directly TTL compatible
- Multiple GND pins for maximum noise immunity

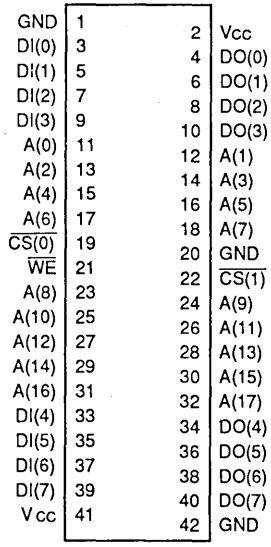
DESCRIPTION:

The IDT7MP4034 is a separate I/O 2 megabit CMOS static RAM module constructed on an epoxy laminate (FR-4) substrate using 8 256K x 1 static RAMs in plastic SOJ packages. Availability of two chip select lines (one for each group of four RAM) provides nibble access and allows the user to configure the memory into a 256K x 8 or a 512K x 4 organization. Extremely fast speeds can be achieved using 256K static RAMs fabricated in IDT's high performance, high reliability CEMOS™ technology. The IDT7MP4034 is available with access times as fast as 20ns with minimal power consumption.

The 7MP family of ZIPs, DSIPs and SIPs offers the optimum in packing density and profile height. The IDT7MP4034 is packaged in a 42 pin FR-4 ZIP (Zig-zag In-line vertical Package). The memory configuration results in a package 2.65 inches long and 0.35 inches wide. At only 0.50 inches high, this low profile package is ideal for high performance systems with minimum board spacing.

All inputs and outputs of the IDT7MP4034 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation.

PIN CONFIGURATION(1)

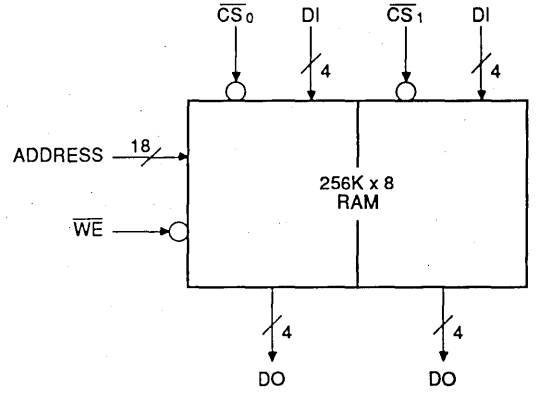


2745 drw 01

ZIP
TOP VIEW

NOTE:
1. For module dimensions, please refer to drawing M44 in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



2745 drw 02

PIN NAMES

DI_{0-7}	Data Inputs
DO_{0-7}	Data Outputs
A_{0-17}	Addresses
$\overline{CS}_{0-1}$	Chip Selects
$\overline{WE}$	Write Enable
Vcc	Power
GND	Ground

2745 tbl 01

8

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

2745 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2745 tbl 03

NOTE:
1. V_{IL} = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2745 tbl 04

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C TO +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	40	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V
I_{CC}	Dynamic Operating Current	$\overline{CS}$ = V_{IL}, Output Open V_{CC} = Max., F = F_{MAX}	—	1,280	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max. Outputs Open, F = F_{MAX}	—	280	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} - 0.2V, V_{IN} > V_{CC} - 0.2V or < 0.2V, F = 0	—	240	mA

2745 tbl 05

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 and 3

2745 tbl 06

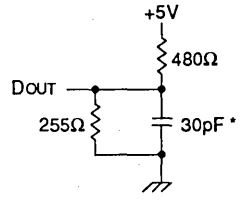
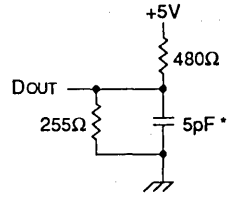


Figure 1. Output Load



2745 drw 03

Figure 2. Output Load (for t_{CHZ}, t_{CLZ}, t_{OW} and t_{WHZ})

* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

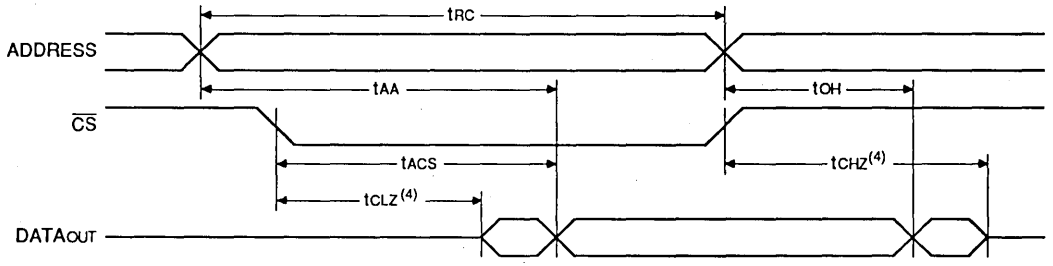
Symbol	Parameter	7MP4034S20 Min.	7MP4034S20 Max.	7MP4034S25 Min.	7MP4034S25 Max.	7MP4034S35 Min.	7MP4034S35 Max.	7MP4034S45 Min.	7MP4034S45 Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	20	—	25	—	35	—	45	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	—	45	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	—	35	—	45	ns
t_{CLZ} (1)	Chip Select to Output in Low Z	3	—	5	—	5	—	5	—	ns
t_{CHZ} (1)	Chip Deselect to Output in High Z	—	10	—	13	—	20	—	25	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{PU} (1)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD} (1)	Chip Deselect to Power Down Time	—	20	—	25	—	35	—	45	ns
Write Cycle										
t_{WC}	Write Cycle Time	20	—	25	—	35	—	45	—	ns
t_{CW}	Chip Select to End of Write	17	—	22	—	30	—	40	—	ns
t_{AW}	Address Valid to End of Write	17	—	22	—	30	—	40	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	17	—	22	—	30	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	3	—	3	—	3	—	ns
t_{WHZ} (1)	Write Enable to Output in High Z	—	10	—	13	—	20	—	25	ns
t_{DW}	Data to Write Time Overlap	13	—	15	—	20	—	25	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
t_{OW} (1)	Output Active from End of Write	0	—	5	—	5	—	5	—	ns

2745 tbl 07

NOTE:
1. This parameter is guaranteed by design but not tested.

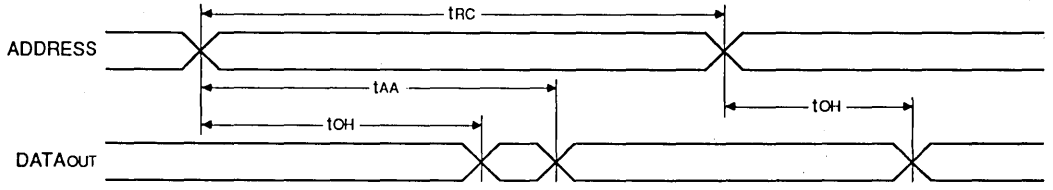
8

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



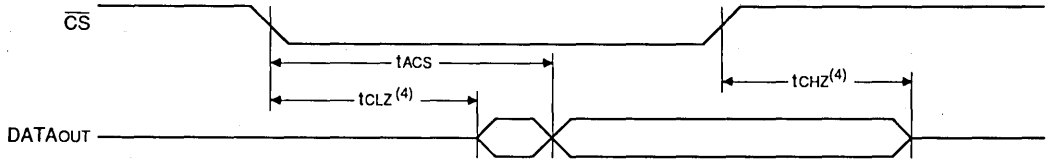
2745 drw 04

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2)



2745 drw 05

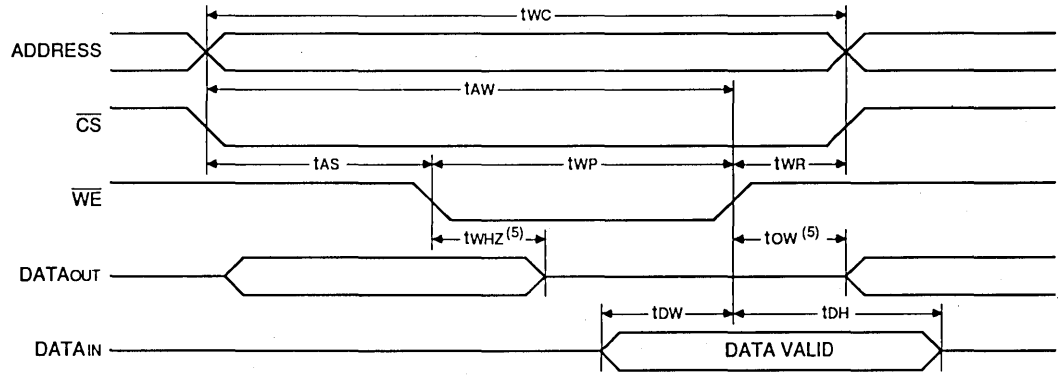
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3)



2745 drw 06

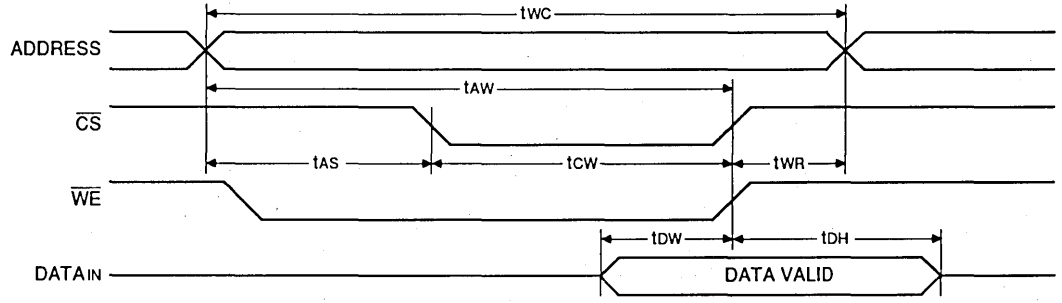
NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state with 5pF load (including scope and jig). This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1, 2, 3) ($\overline{WE}$ CONTROLLED TIMING)



2745 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1, 2, 3, 4) ($\overline{CS}$ CONTROLLED TIMING)



2745 drw 08

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tCW or tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneous with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
5. Transition is measured ±200mV from steady state with 5pF load (including scope and jig). This parameter is guaranteed by design but not tested.

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TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	DATAOUT	Active
Write	L	L	DATAIN	Active

2745 tbl 08

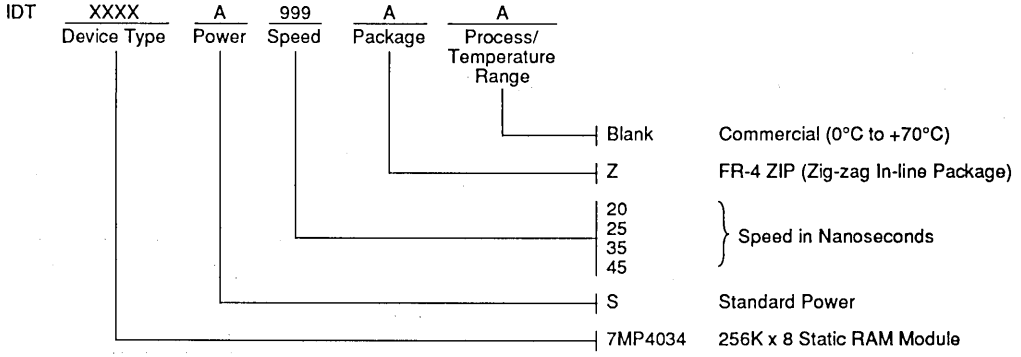
CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	V_{IN} = 0V	15	pF
$C_{IN(A)}$	Input Capacitance (Address and Control)	V_{IN} = 0V	92	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	15	pF

2745 tbl 09

NOTE:
1. This parameter is guaranteed by design but not tested.

ORDERING INFORMATION



2745 drw 12

Integrated Device Technology, Inc.

512K x 8 CMOS STATIC RAM MODULE

PRELIMINARY
IDT7M4048
IDT7MB4048

FEATURES:

- High density 4 megabit (512K x 8) static RAM module
- Equivalent to the JEDEC standard for future monolithic 512K x 8 static RAMs
- Fast access time: 30ns (max.)
- Low power consumption (commercial grade L version)
  - — Active: 110mA (max.)
  - — CMOS Standby: 8mA (max.)
- Very low power version (commercial grade SCD 4591)
  - — Data Retention: 200µA (max.) Vcc = 2V
  - — CMOS Standby: 400µA (max.)
- Surface mounted plastic packages or leadless chip carriers on a 32-pin, 600 mil ceramic DIP substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible

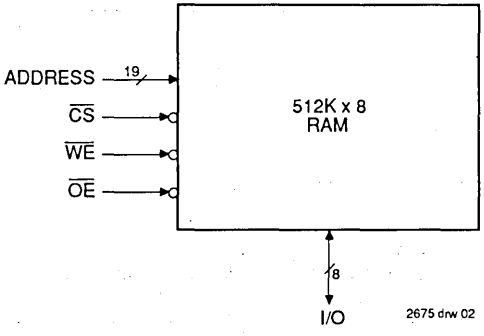
DESCRIPTION:

The IDT7M4048/7MB4048 is a 4 megabit (512K x 8) static RAM module constructed on a co-fired ceramic or multilayer epoxy laminate (FR-4) substrate using four 1 Megabit static RAMS and a decoder. The IDT7M4048/7MB4048 is available with access times as fast as 30ns. For battery backup applications, a very low power version is available, offering a data retention current of 200µA.

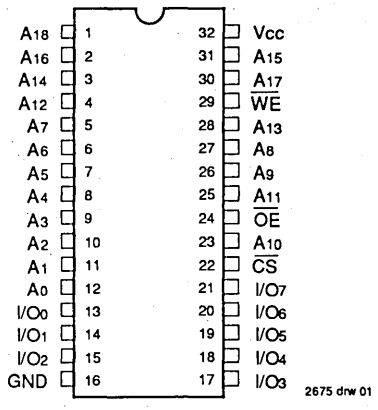
The IDT7M4048 is packaged in a 32-pin ceramic DIP. This results in a package 1.7 inches long and 600 mils wide, packing 4 megabits into the JEDEC DIP footprint. The IDT7MB4048 likewise is packaged in a 32-pin FR-4 DIP resulting in the same JEDEC footprint in a package 1.6 inches long and 600 mils wide.

All inputs and outputs of the IDT7M4048 and 7MB4048 are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use. All IDT military module semiconductor components are manufactured in compliance to the latest revision of MIL-STD-883 Class B, making them ideally suited for applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION(1)



DIP
TOP VIEW

PIN NAMES

I/O0-7	Data Inputs/Outputs
A0-18	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power
GND	Ground

2675 tbl 01

NOTE:
1. For module dimensions, please refer to module drawing M3, M4, or M5 (7M4048L, 7M4048S, 7MB4048S) in the packaging section.

8

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TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	DOUT	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	DIN	Active

2675 tbl 09

CAPACITANCE[1] (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	35	pF
CIN(C)	Input Capacitance ($\overline{CS}$)	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	35	pF

NOTE: 2675 tbl 10
1. This parameter is guaranteed by design, but not tested.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2675 tbl 02
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2675 tbl 03
1. VIL = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%
Military	-55°C to +125°C	0V	5V ±10%

2675 tbl 04

DC ELECTRICAL CHARACTERISTICS

(VCC = 5V ± 10%, TA = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameter	Test Conditions	7M4048LxxN		7MB4048SxxP 7M4048SxxC 7M4048SxxCB				Unit
			(COM'L ONLY)		(COM'L)		(MILITARY)		
			Min.	Max.	Min.	Max.	Min.	Max.	
|ILI|	Input Leakage	VCC = Max., VIN = GND to VCC	—	4	—	8	—	40	µA
|ILO|	Output Leakage	VCC = Max., $\overline{CS}$ = VIH, VOUT = GND to VCC	—	4	—	8	—	40	µA
VOL	Output Low Voltage	VCC = Min., IOL = 2mA[2], IOL = 8mA[3]	—	0.4	—	0.4	—	0.4	V
VOH	Output High Voltage	VCC = Min., IOH = -1mA[2], IOH = –4mA[3]	2.4	—	2.4	—	2.4	—	V
ICC	Dynamic Operating Current	VCC = Max., $\overline{CS}$ ≤ VIL; f = fMAX, Outputs Open	—	110	—	360	—	480	mA
ISB	Standby Supply Current (TTL Levels)	$\overline{CS}$ ≥ VIH, VCC = Max., f = fMAX, Outputs Open	—	12	—	240	—	240	mA
ISB1[1]	Full Standby Supply Current (CMOS Levels)	$\overline{CS}$ ≥ VCC - 0.2V, VIN ≥ VCC - 0.2V or ≤ 0.2V	—	8	—	40	—	80	mA

NOTES: 2675 tbl 05
1. For low power version ISB1 = 400µA, refer to SCD4591 when ordering. For Commercial grade 7M4048L version only
2. For Commercial grade 7M4048L version only.
3. For 7MB4048SxxP, 7M4048SxxC, and 7M4048SxxCB versions.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2675 tbl 07

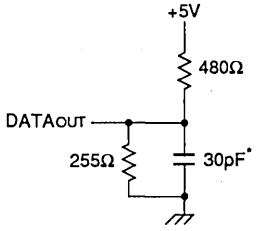


Figure 1. Output Load

* Including scope and jig

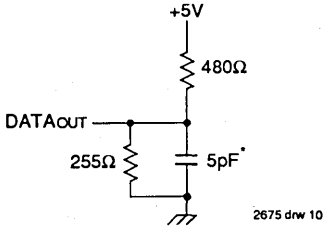


Figure 2. Output Load
(for t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, t_{OW} and t_{CLZ})

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

		7M4048S30C 7MB4048S30P		7M4048S35C 7MB4048S35P		7M4048S40C 7M4048S40CB 7MB4048S40P		7M4048S45C 7M4048S45CB 7MB4048S45P		7M4048S50C 7M4048S50CB 7MB4048S50P		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
Read Cycle												
t_{RC}	Read Cycle Time	30	—	35	—	40	—	45	—	50	—	ns
t_{AA}	Address Access Time	—	30	—	35	—	40	—	45	—	50	ns
t_{ACS}	Chip Select Access Time	—	30	—	35	—	40	—	45	—	50	ns
t_{OE}	Output Enable to Output Valid	—	11	—	15	—	20	—	25	—	30	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	10	—	15	—	20	—	20	—	20	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	2	—	2	—	5	—	5	—	5	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	16	—	20	—	20	—	20	—	20	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	5	—	5	—	5	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	30	—	35	—	40	—	45	—	50	ns
Write Cycle												
t_{WC}	Write Cycle Time	30	—	35	—	40	—	45	—	50	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	30	—	35	—	40	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	5	—	5	—	5	—	ns
t_{AW}	Address Valid to End of Write	25	—	30	—	35	—	40	—	45	—	ns
t_{CW}	Chip Select to End of Write	25	—	30	—	35	—	40	—	45	—	ns
t_{DS}	Data Set-up Time	—	—	—	—	—	—	—	—	—	—	ns
t_{DH}	Data Hold Time	3	—	3	—	3	—	5	—	5	—	ns
t_{WR}	Write Recovery Time	3	—	3	—	5	—	5	—	5	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	11	—	15	—	15	—	15	—	20	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

2675 tbl 08

8

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameter	7M4048S60C 7M4048S60CB 7MB4048S60P		7M4048S70C 7M4048S70CB 7M4048L70N		7M4048S85C 7M4048S85CB 7M4048L85N		7M4048S100C 7M4048S100CB 7M4048L100N		7M4048S120C 7M4048S120CB 7M4048L120N		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t_{RC}	Read Cycle Time	60	—	70	—	85	—	100	—	120	—	ns
t_{AA}	Address Access Time	—	60	—	70	—	85	—	100	—	120	ns
t_{ACS}	Chip Select Access Time	—	60	—	70	—	85	—	100	—	120	ns
t_{OE}	Output Enable to Output Valid	—	35	—	45	—	48	—	50	—	60	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	25	—	30	—	33	—	35	—	40	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	5	—	0	—	0	—	0	—	0	—	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	—	25	—	40	—	43	—	45	—	50	ns
t_{OH}	Output Hold from Address Change	5	—	10	—	10	—	10	—	10	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	60	—	70	—	85	—	100	—	120	ns
Write Cycle												
t_{WC}	Write Cycle Time	60	—	70	—	85	—	100	—	120	—	ns
t_{WP}	Write Pulse Width	50	—	55	—	65	—	75	—	90	—	ns
t_{AS}	Address Set-up Time	5	—	0	—	2	—	5	—	5	—	ns
t_{AW}	Address Valid to End of Write	55	—	65	—	82	—	90	—	100	—	ns
t_{CW}	Chip Select to End of Write	55	—	65	—	80	—	85	—	100	—	ns
t_{DS}	Data Set-up Time			35	—	38	—	40	—	45	—	ns
t_{DH}	Data Hold Time	5	—	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	5	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}(1)	Write Enable to Output in High Z	—	25	—	30	—	33	—	35	—	40	ns
t_{OW}(1)	Output Active from End of Write	5	—	0	—	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

2675 tbl 08

DATA RETENTION CHARACTERISTICS(1, 4)

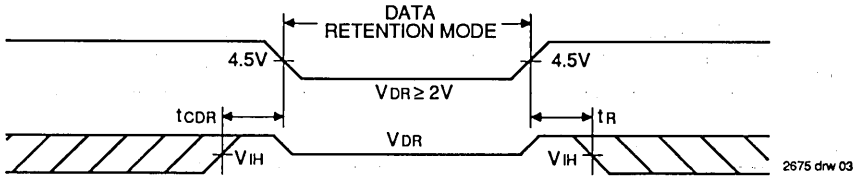
(T_A = 0°C to +70°C)

Symbol	Parameter	Test Condition	Min.	Max. V_{CC} @ 2.0V	Unit
V_{DR}	V_{CC} for Data Retention	—	2.0	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ - 0.2V	—	200	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time	$V_{IN} \leq V_{CC}$ - 0.2V or	0	—	ns
t_R(3)	Operation Recovery Time	$V_{IN} \geq$ 0.2V	t_{RC}(2)	—	ns

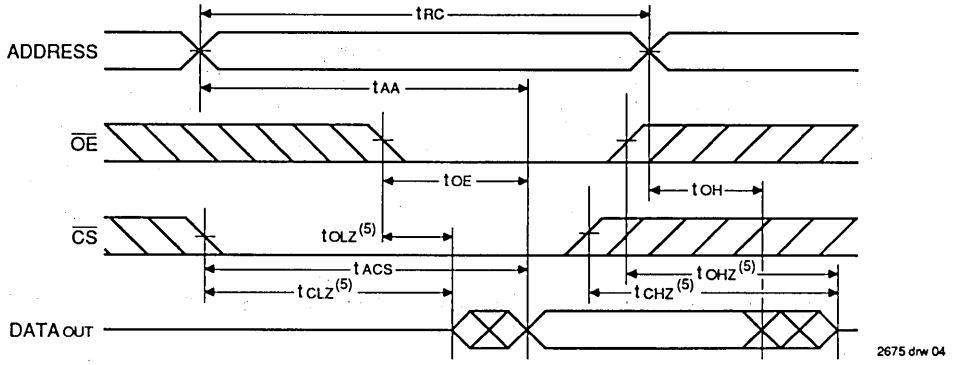
NOTES:
1. V_{CC} = 2V, T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by design, but not tested.
4. This option is only offered when ordering to 7M4048LxxN SCD4591.

2675 tbl 09

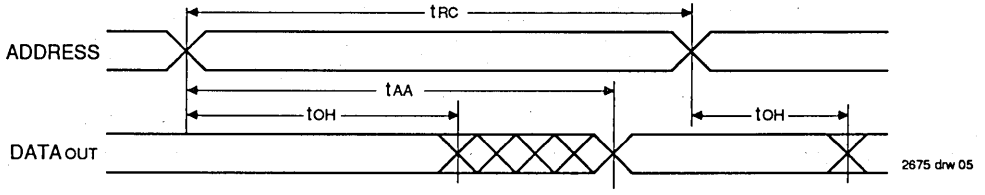
DATA RETENTION WAVEFORM



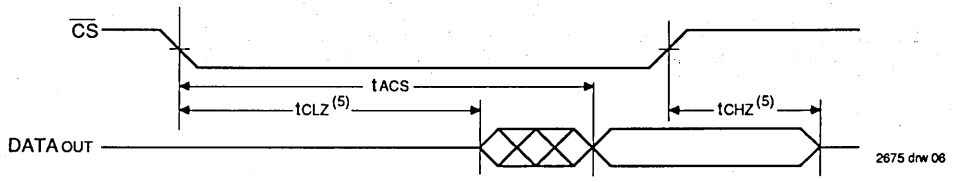
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)

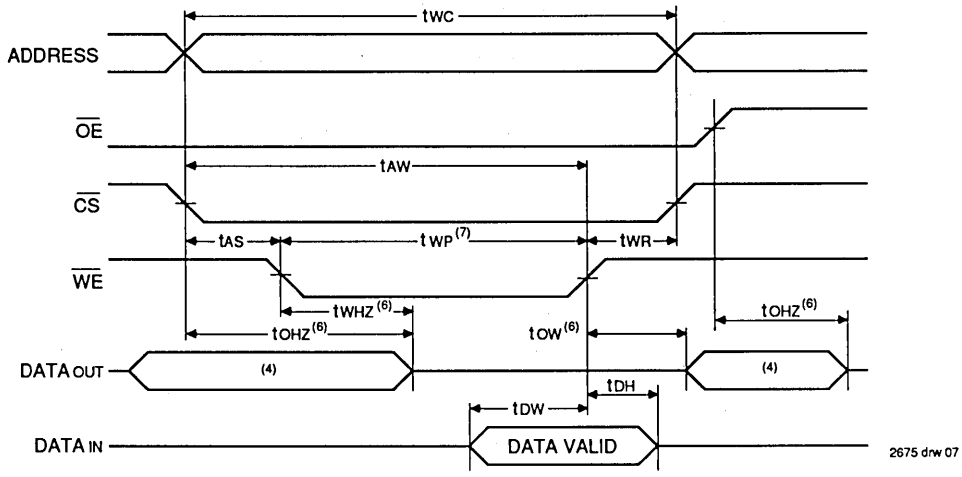


TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)

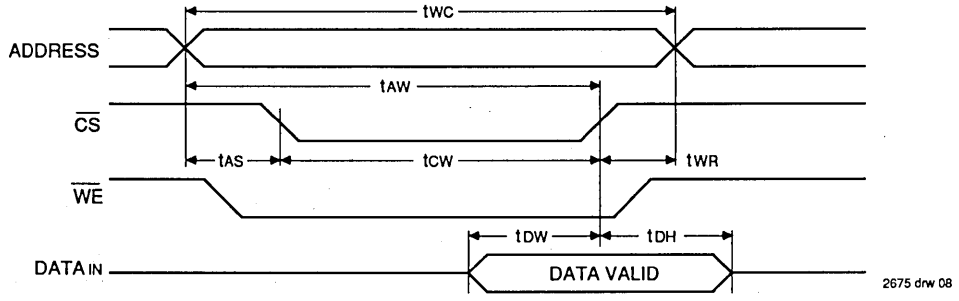


NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guranateed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)

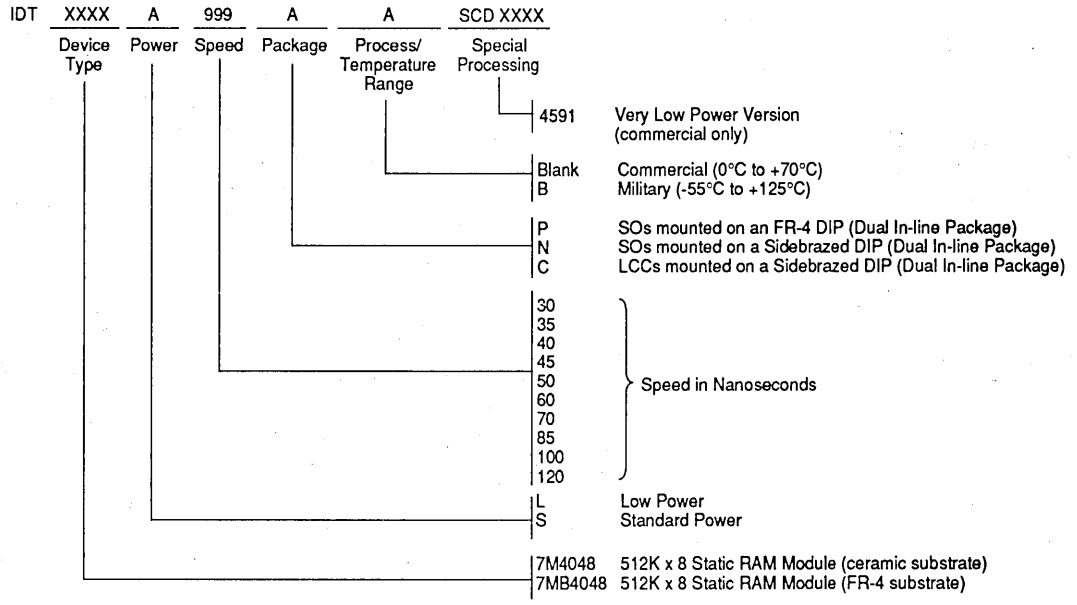


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse ((tWP) > tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

ORDERING INFORMATION



2675 drw 09

8

Integrated Device Technology, Inc.

512K x 8 CMOS STATIC RAM MODULE

IDT7MP4008S

FEATURES:

- High-density 4 megabit CMOS static RAM module
- Fast access times
  - — 30ns (max.)
- Cost effective plastic surface mount RAM packages on a epoxy laminate (FR-4) substrate
- Available in 36-pin SIP (Single In-line Package)
- Low power consumption
  - — Dynamic: 2.6W (max.)
  - — Full standby: 1.9W (max.)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

The IDT7MP4008 is a 512K x 8 high-speed CMOS static RAM module constructed on an epoxy laminate surface using sixteen 32K x 8 static RAMs in plastic surface mount packages. Extremely fast speeds can be achieved with this technique due to the use of 256K static RAMs fabricated in IDT's high-performance, high-reliability CEMOS™ technology.

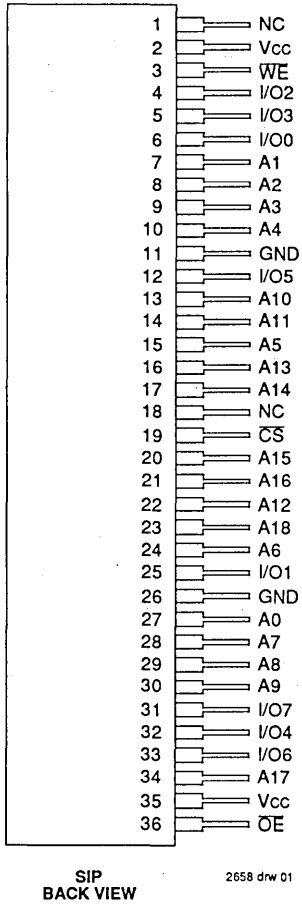
The IDT7MP family of surface-mounted SIP modules is a cost-effective solution allowing for very high packing density and the IDT7MP4008 is offered in a 36-pin SIP. The IDT7MP4008 can be stacked on 300 mil centers, yielding greater than 12 megabits of RAM in less than 5 square inches of board space.

The IDT7MP4008 is available with minimum access times as fast as 30ns over the commercial temperature range with maximum power consumption of 2.6 watts. The IDT7MP4008 also offers a full standby mode of 1.9W (max.).

All inputs and outputs of the IDT7MP4008 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

CEMOS is a trademark of Integrated Device Technology, Inc.

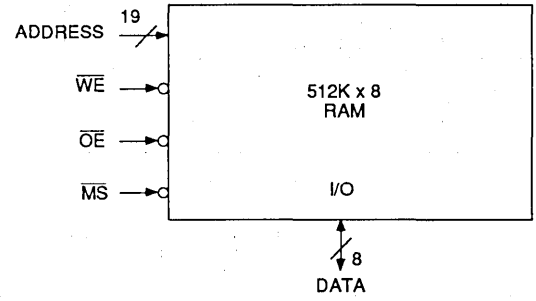
PIN CONFIGURATION[1]



SIP
BACK VIEW

2658 drw 01

FUNCTIONAL BLOCK DIAGRAM



2658 drw 02

PIN NAMES

A0–18	Addresses
I/O0–7	Data Inputs/Outputs
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
Vcc	Power
GND	Ground

2658 tbl 01

NOTE:
1. For module dimensions, please refer to module drawing M37 in the packaging section.

8

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

2658 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2658 tbl 03

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2658 tbl 04

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7MP4008S Min.	Max.(2)	Max.(3)	Unit
$\|I_{LI}\|$	Input Leakage Current(1)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	80	80	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	80	80	µA
I_{CC}	Dynamic Operating Current	$\overline{CS}$ = V_{IL} V_{CC} = Max. Output Open f = f_{MAX}	—	550	500	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} or (TTL Level) V_{CC} = Max., f = f_{MAX} Outputs Open	—	480	350	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}$ ≥ V_{HC}, V_{IN} ≥ V_{HC} or ≤ V_{LC} V_{CS} = Max., Output Open	—	285	285	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4mA, V_{CC} = Min.	2.4	—	—	V

2658 tbl 05

NOTES:
1. $|I_{LI}|$ for A_{15}-A_{16} and $\overline{CS}$ = 400 µA (max.).
2. t_{AA} = 30ns.
3. t_{AA} = 35, 45, 55, 70ns.

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2658 tbl 06

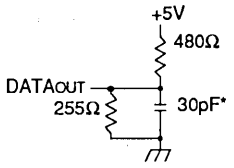
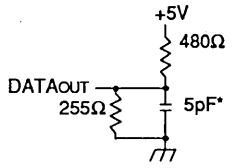


Figure 1. Output Load



2658 drw 03

Figure 2. Output Load
(for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

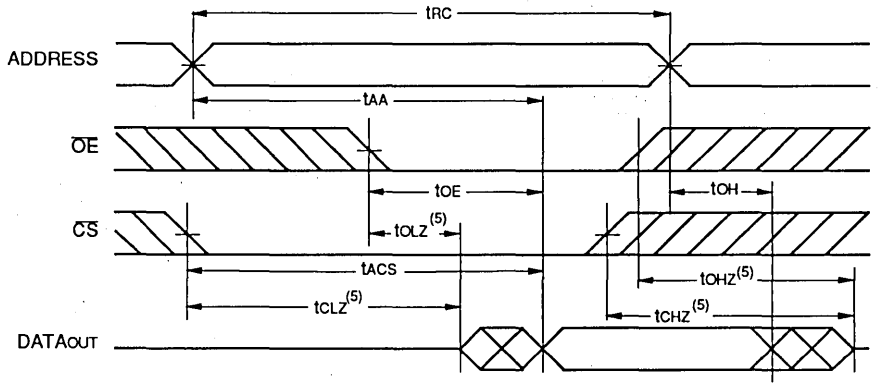
Symbol	Parameter	7MP4008S30		7MP408S35		7MP4008S45		7MP4008S55		7MP4008S70		Unit
		Min.	Max.	Min.	Max	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t_{RC}	Read Cycle Time	30	—	35	—	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	30	—	35	—	45	—	55	—	70	ns
t_{ACS}	Chip Select Access Time	—	30	—	35	—	45	—	55	—	70	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enables to Output Valid	—	13	—	15	—	20	—	25	—	30	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	5	—	5	—	0	—	0	—	0	—	ns
t_{CHZ}(1)	Chip Select to Output in High Z	—	20	—	21	—	25	—	30	—	35	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	11	—	13	—	25	—	25	—	30	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
Write Cycle												
t_{WC}	Write Cycle Time	30	—	35	—	45	—	55	—	70	—	ns
t_{CW}	Chip Select to End of Write	25	—	30	—	40	—	50	—	60	—	ns
t_{AW}	Address Valid to End of Write	25	—	30	—	40	—	50	—	60	—	ns
t_{AS}	Address Set-up Time	5	—	5	—	5	—	5	—	5	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	35	—	45	—	55	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	5	—	5	—	10	—	ns
t_{WHZ}(1)	Write Enable to Output in High Z	—	13	—	14	—	15	—	20	—	25	ns
t_{DW}	Data Valid to End of Write	14	—	16	—	20	—	25	—	30	—	ns
t_{DH}	Data Hold from Write Time	3	—	3	—	5	—	5	—	5	—	ns
t_{OW} (1)	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

2658 tbl 07

NOTE:
1. This parameter is guaranteed by design but not tested.

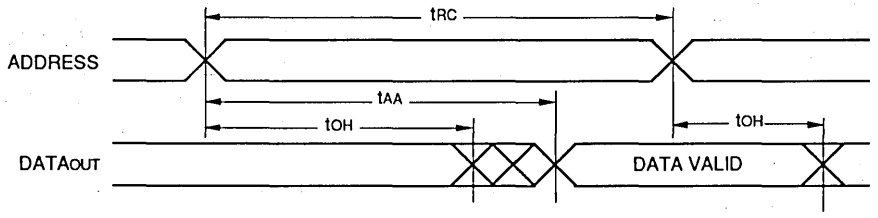
8

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



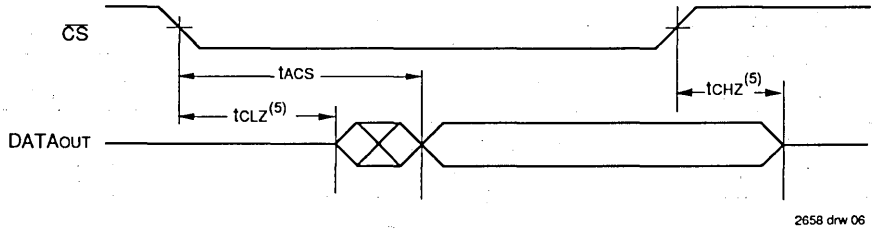
2658 drw 04

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2658 drw 05

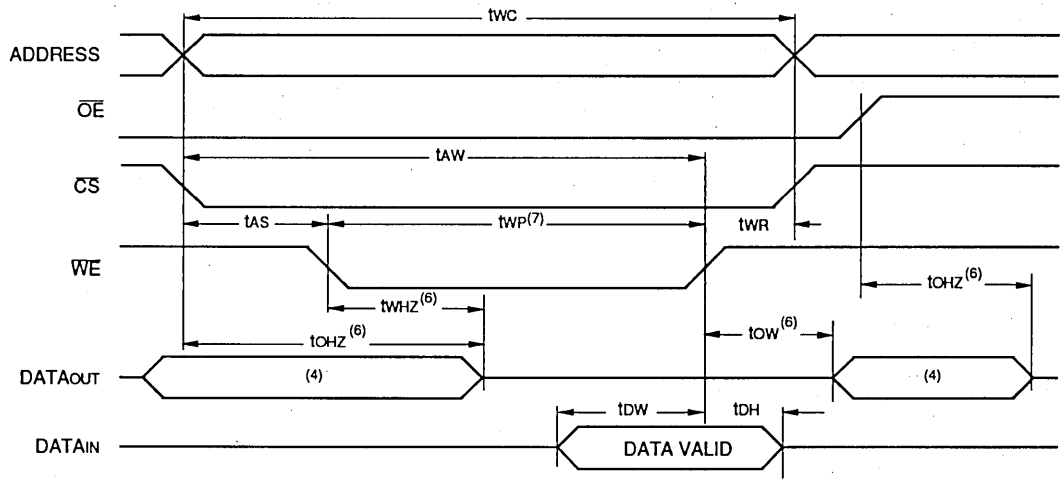
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



2658 drw 06

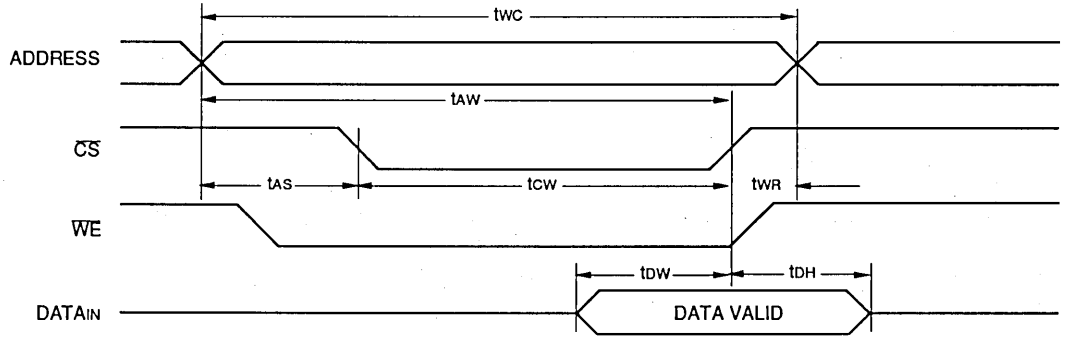
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



2658 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



2658 drw 08

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured by ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design but not tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse (tWP > tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

8

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	$DATA_{OUT}$	Active
Read	L	H	H	High Z	Active
Write	L	X	L	$DATA_{IN}$	Active

2658 tbl 08

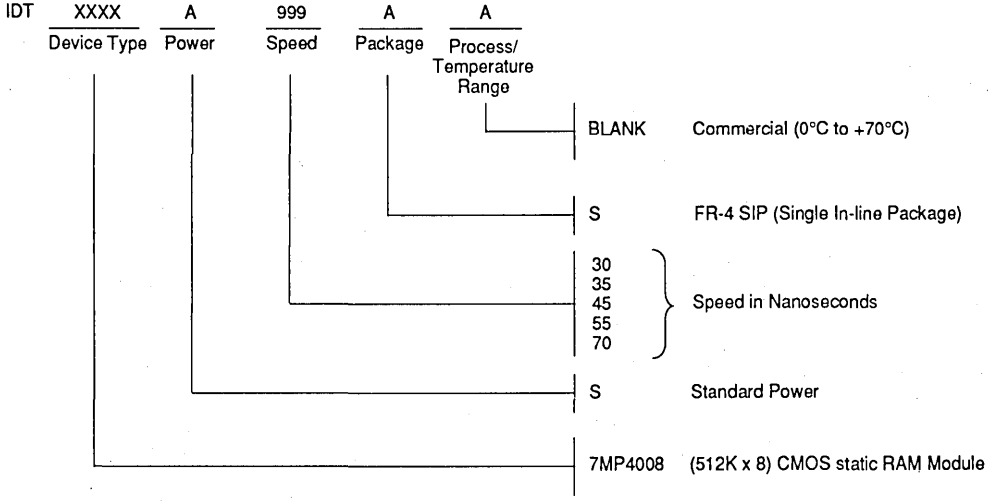
CAPACITANCE[1] (T_A = +25°C, f =1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	V_{IN} = 0V	188	pF
$C_{IN(A)}$	Input Capacitance (Address and Control)	V_{IN} = 0V	188	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	128	pF

2658 tbl 09

NOTE:
1. This parameter is guaranteed by design but not tested.

ORDERING INFORMATION



2658 drw 09

Integrated Device Technology, Inc.

512K x 8 CMOS STATIC RAM MODULE

PRELIMINARY
IDT7MP4058L

FEATURES:

- High-density 4 Meg CMOS static RAM module
- Fast access time: 70ns (max.)
- Low power consumption
  - Active: 110mA (max.)
  - CMOS standby: 8mA (max.)
- Very low power version (SCD4602)
  - Data Retention: 400µA (max.)
  - CMOS Standby: 200µA (max.)
- Cost-effective plastic surface-mounted RAM packages on an epoxy laminate FR-4 substrate
- Offered in a 36-pin SIP (Single In-line Package) for maximum space-saving
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

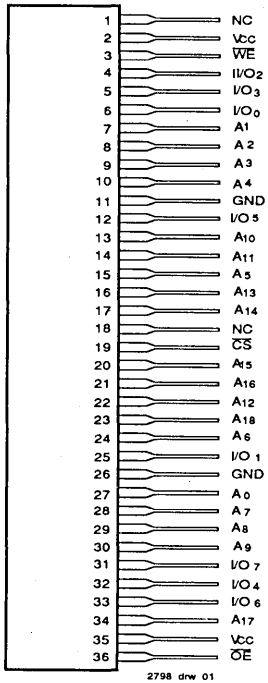
The IDT7MP4058L is a 512K x 8 high-speed CMOS static RAM module constructed on an epoxy laminate substrate (FR-4) using four 128K x 8 static RAMS and a one-of-four decoder in plastic surface mount packages.

The IDT7MP4058L is available with maximum access times as fast as 70ns, with maximum operating power consumption of 605mW.

The IDT7MP4058L is offered in a 36-pin SIP (Single In-line Package). This vertically mounted SIP module is a cost-effective solution allowing for very high packing density.

All inputs and outputs of the IDT7MP4058L are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

PIN CONFIGURATION[1]

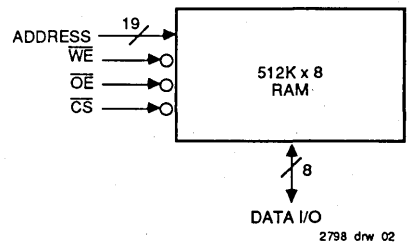


SIP
BACK VIEW

NOTE:

1. For module dimensions, please refer to drawing M38 in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A0-18	Address Inputs
I/O0-7	Data Inputs/Outputs
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
Vcc	Power
GND	Ground
NC	No Connect

2798 tbl 11

8

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating[1]	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2798 tbl 02
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6	V
V_{IL}	Input Low Voltage	–0.5	—	0.8	V

NOTE: 2798 tbl 03
1. V_{IL} = –3.0V for pulse width less than 20ns

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	V_{CC}
Commercial	0°C to +70°C	0V	5V ± 10%

2798 tbl 04

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	4	µA
I_{LO}	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	4	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 2mA[2], I_{OL} = 8mA[3]	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –1mA[2], I_{OH} = –4mA[3]	2.4	—	V
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS} \leq V_{IL}$; f = f_{MAX}, Outputs Open	—	110	mA
I_{SB}	Standby Supply Current (TTL Levels)	$\overline{CS} \geq V_{IH}$, V_{CC} = Max., f = f_{MAX}, Outputs Open	—	12	mA
I_{SB1}[1]	Full Standby Supply Current (CMOS Levels)	$\overline{CS} \geq V_{CC}$ 0.2V, $V_{IN} \geq V_{CC}$ –0.2V or ≤ 0.2V	—	8	mA

NOTE: 2798 tbl 05
1. For low power version I_{SB1} = 40µA refer to SCD4602 when ordering.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
$C_{IN (C)}$	Input Capacitance ($\overline{CS}$)	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	35	pF

NOTE: 2798 tbl 06
1. This parameter is guaranteed by design, but not tested.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	D_{OUT}	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	D_{IN}	Active

2798 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2798 tbl 08

LOGIC SYMBOL

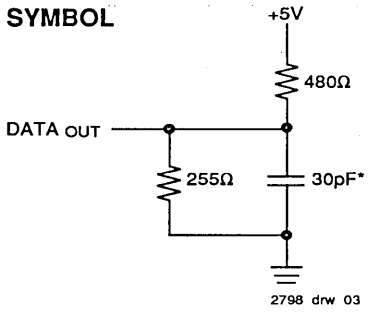
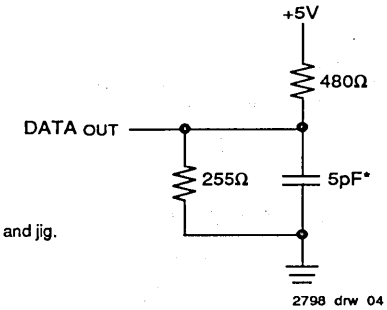


Figure 1. Output Load



*Including scope and jig.

Figure 2. Output Load
(For t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, t_{OW} and t_{CLZ})

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameter	7MP4058L70		7MP4058L85		7MP4058L100		7MP4058L120		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	70	—	85	—	100	—	120	—	ns
t_{AA}	Address Access Time	—	70	—	85	—	100	—	120	ns
t_{ACS}	Chip Select Access Time	—	70	—	85	—	100	—	120	ns
t_{OE}	Output Enable to Output Valid	—	45	—	48	—	50	—	60	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	30	—	33	—	35	—	40	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	—	40	—	43	—	45	—	50	ns
t_{OH}	Output Hold from Address Change	10	—	10	—	10	—	10	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	70	—	85	—	100	—	120	ns
Write Cycle										
t_{WC}	Write Cycle Time	70	—	85	—	100	—	120	—	ns
t_{WP}	Write Pulse Width	55	—	65	—	75	—	90	—	ns
t_{AS}	Address Set-up Time	0	—	2	—	5	—	5	—	ns
t_{AW}	Address Valid to End of Write	65	—	82	—	90	—	100	—	ns
t_{CW}	Chip Select to End of Write	65	—	80	—	85	—	100	—	ns
t_{DW}	Data to Write Time Overlap	35	—	38	—	40	—	45	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}(1)	Write Enable to Output in High Z	—	30	—	33	—	35	—	40	ns
t_{OW}(1)	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

2675 tbl 08

8

DATA RETENTION CHARACTERISTICS (1, 4)

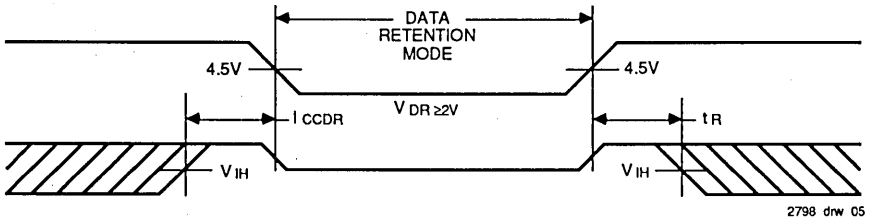
(T_A = 0°C to +70°C)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V_{DR}	VCC for Data Retention	—	2.0	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ 0.2V	—	200	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time	$V_{IN} \leq V_{CC}$ 0.2V or	0	—	ns
t_R(3)	Operation Recovery Time	$V_{IN} \geq$ 0.2V	t_{RC}(2)	—	ns

2798 tbl 10

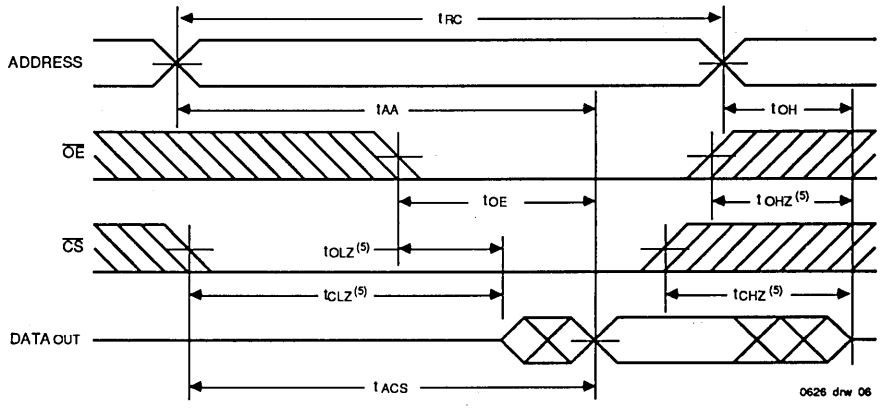
NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed by design, but not tested.
4. This option is only offered when ordering to SCD4602.

DATA RETENTION WAVEFORM

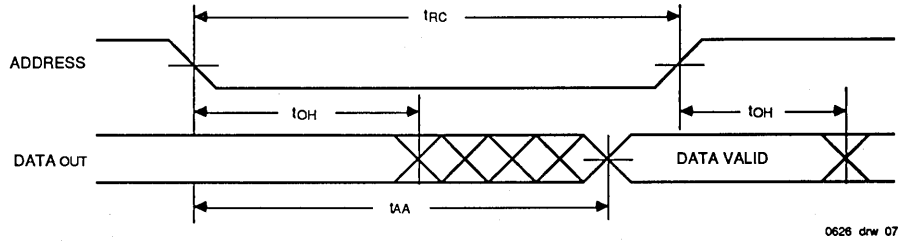


2798 drw 05

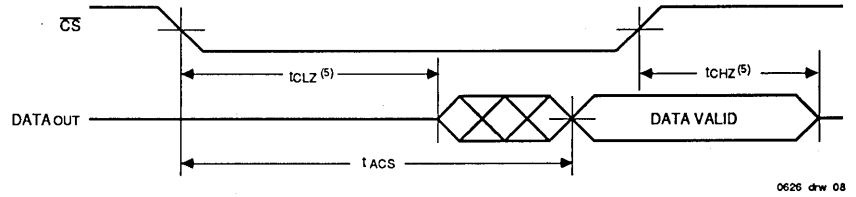
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



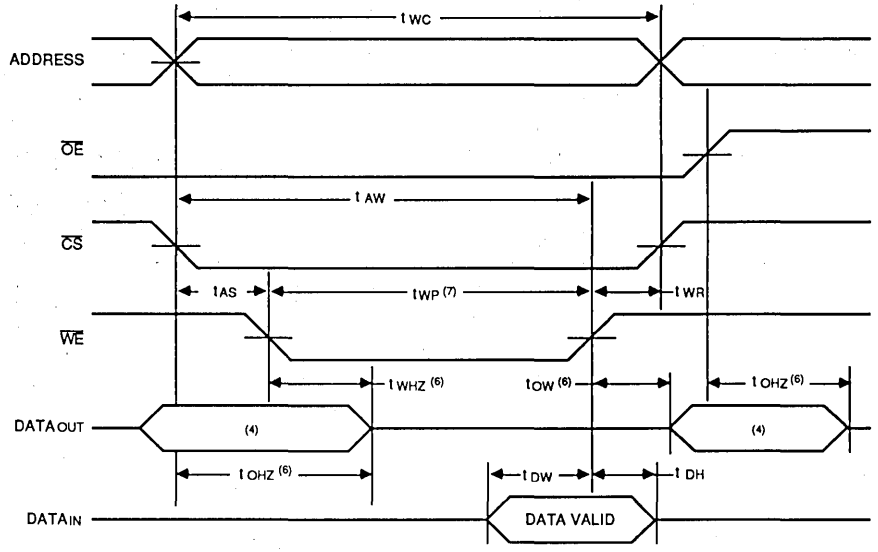
TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



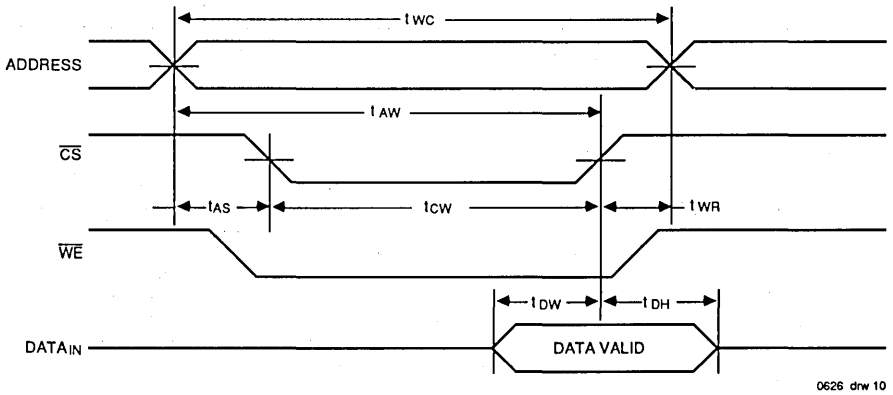
NOTES:
1. $\overline{WE}$ is High for Read Cycle
2. Device is continuously selected $\overline{CS}$ = V_{IL}
3. Address valid prior to or coincident with $\overline{CS}$ transition low
4. $\overline{OE}$ = V_{IL}
5. Transition is measured = 200mV from steady state. This parameter is guaranateed by design but not tested.

8

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)

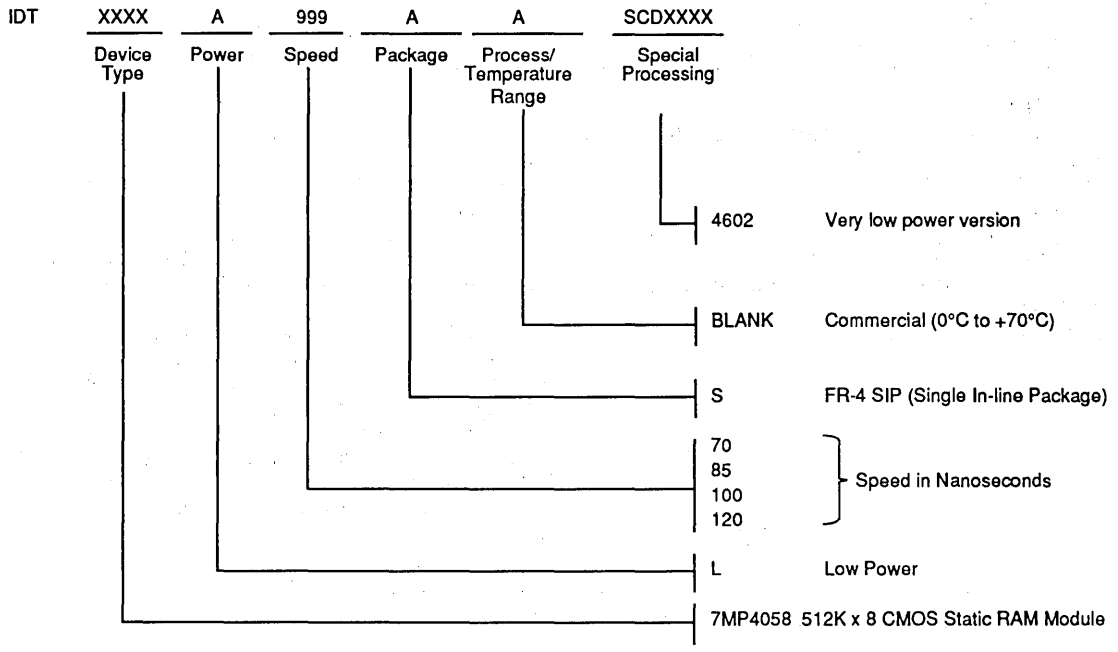


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlay (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design but not tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse ((tWP) > tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

ORDERING INFORMATION



8

Integrated Device Technology, Inc.

256K x 9 CMOS STATIC RAM MODULE

PRELIMINARY
IDT7MB4040

FEATURES:

- High density separate I/O, 2 megabit CMOS static RAM module
- Low profile 44 pin, 600 mil DIP
- Fast access time: 20ns (max.)
- Surface mounted plastic SOJ packages on a multilayer epoxy laminate (FR-4) substrate
- Multiple ground pins for maximum noise immunity
- Inputs/outputs directly TTL compatible
- Single 5V (±10%) power supply

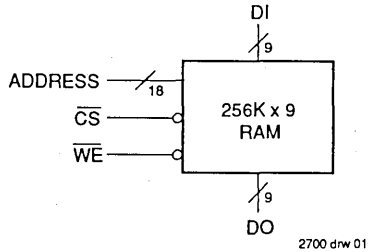
DESCRIPTION:

The IDT7MB4040 is a separate I/O, 256K x 9 CMOS static RAM module constructed on a multilayer epoxy laminate (FR-4) substrate using 9 256K x 1 static RAMs in plastic SOJ packages. Extremely fast speeds can be achieved using 256K static RAMs fabricated in IDT's high performance, high reliability CEMOS™ technology. The IDT7MB4040 is available with access times as fast as 20ns with minimal power consumption.

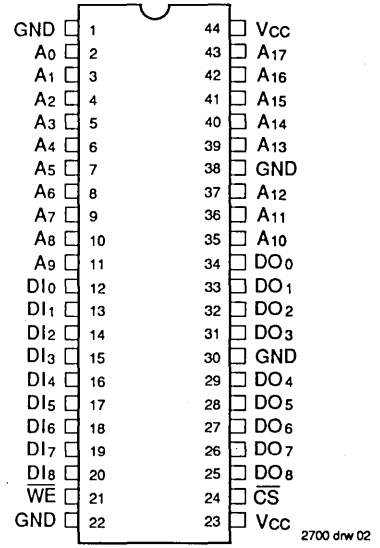
The IDT7MB4040 is packaged in a 44 pin FR-4 DIP. The memory configuration results in a package 3.4 inches long, 600 mils wide, and only 350 mils in height. Provision of a ninth bit results in a optimal package for high reliability applications where parity is a must.

All inputs and outputs of the IDT7MB4040 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refreshing for operation.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION[1]



DIP
TOP VIEW

NOTE:
1. For module dimension, please refer to module drawing M14 in the packaging section.

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN NAMES

DI_0–DI_8	Data Inputs
DO_0–DO_8	Data Outputs
A_0–A_{17}	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power
GND	Ground

2700 tbl 01

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	$DATA_{OUT}$	Active
Write	L	L	$DATA_{IN}$	Active

2700 tbl 04

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2700 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	V_{IN} = 0V	15	pF
$C_{IN(A)}$	Input Capacitance (Address and Control)	V_{IN} = 0V	100	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	15	pF

NOTE: 2700 tbl 03

1. This parameter is guaranteed by design, but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE: 2700 tbl 05

1. V_{IL} = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

2700 tbl 06

8

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	45	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	—	V

2700 tbl 07

Symbol	Parameter	Test Conditions	Max.	Unit
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS} \leq V_{IL}$ Outputs Open, f = f_{MAX}.	1440	mA
I_{SB}	Standby Supply Current	$\overline{CS} \geq V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}.	315	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS} \geq V_{CC}$ – 0.2V $V_{IN} \geq V_{CC}$ – 0.2V or ≤ 0.2V	270	mA

2700 tbl 08

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2700 tbl 09

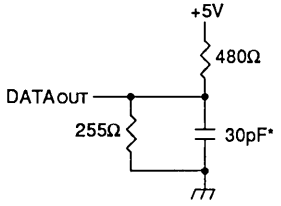


Figure 1. Output Load

*Including scope and jig

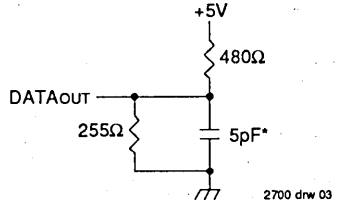


Figure 2. Output Load (for t_{CLZ}, t_{CHZ}, t_{WHZ}, t_{OW})

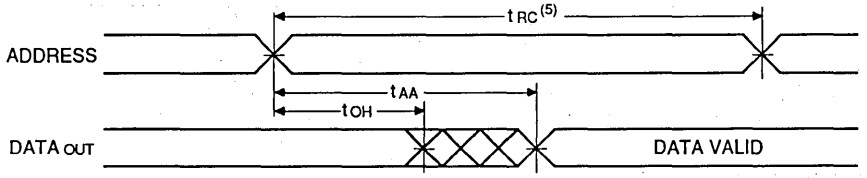
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameters	7MB4040S20		7MB4040S25		7MB4040S35		7MB4040S45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	20	—	25	—	35	—	45	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	—	45	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	—	35	—	45	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	3	—	5	—	5	—	5	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	—	10	—	13	—	20	—	25	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{PU}(1)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power Down Time	—	20	—	25	—	35	—	45	ns
Write Cycle										
t_{WC}	Write Cycle Time	20	—	25	—	35	—	45	—	ns
t_{CW}	Chip Selection to End of Write	17	—	22	—	30	—	40	—	ns
t_{AW}	Address Valid to End of Write	17	—	22	—	30	—	40	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	17	—	22	—	30	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	3	—	3	—	3	—	ns
t_{WHZ}(1)	Write Enable to Ouput in High Z	—	10	—	13	—	20	—	25	ns
t_{DW}	Data to Write Time Overlap	13	—	15	—	20	—	25	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
t_{OW}(1)	Output Active from End of Write	0	—	5	—	5	—	5	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

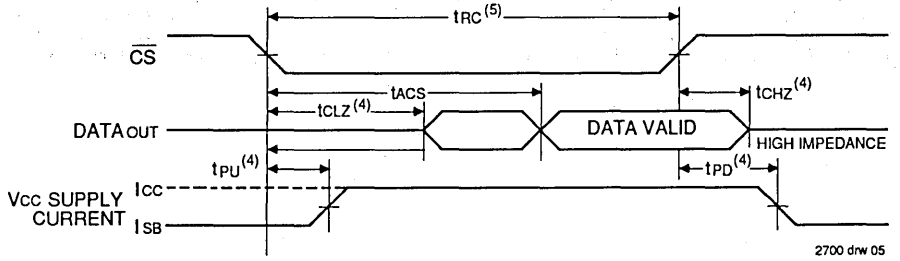
2700 tbl 10

TIMING WAVEFORM OF READ CYCLE NO. 1(1, 2)



2700 drw 04

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 3)

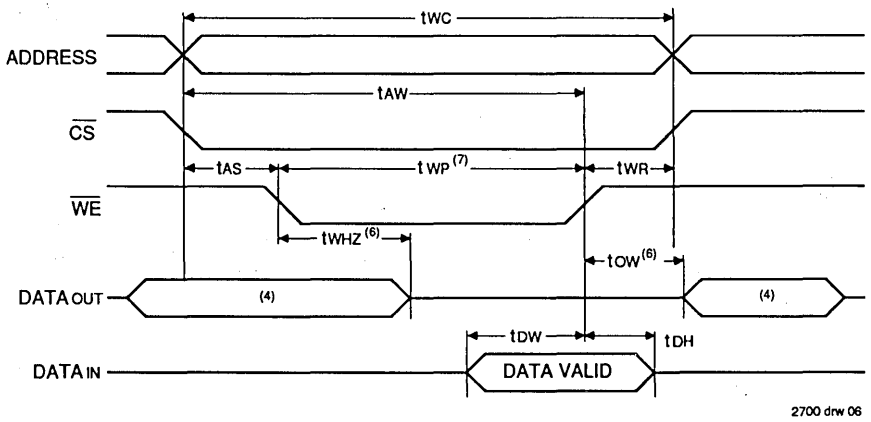


2700 drw 05

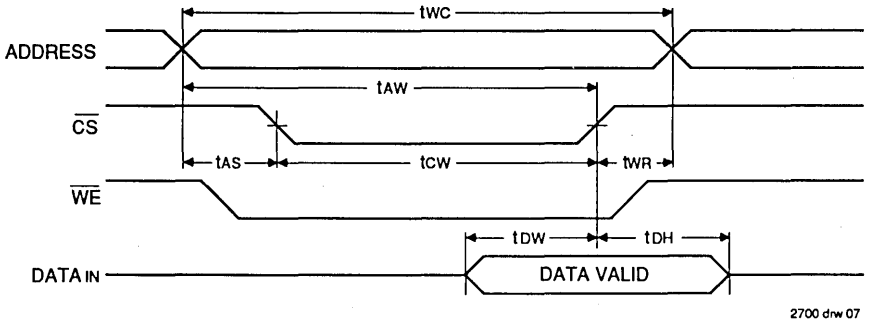
NOTES:
1. $\overline{WE}$ is high for Read Cycle.
2. $\overline{CS}$ is low for Read Cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading on Figure 2. This parameter is guaranteed by design, but not tested.
5. All Read Cycle timings are referenced from the last valid address to the first transitioning address.

8

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1, 2, 3, 7)

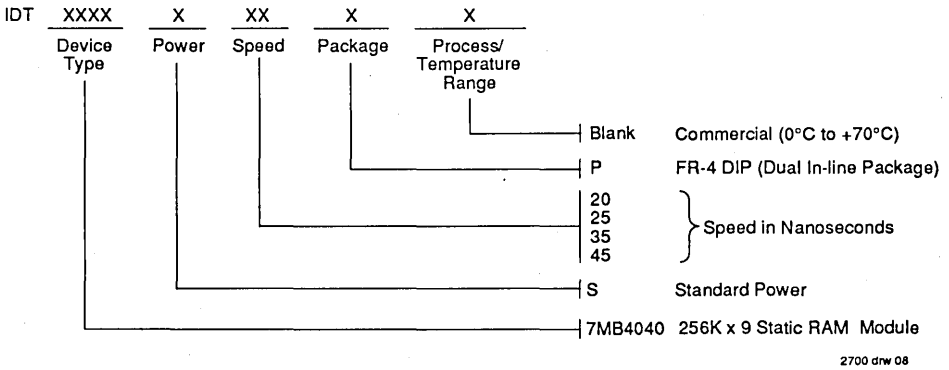


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going High to the end of write cycle.
4. During this period, I/O pins are in the output state, input signals must not be applied.
5. If the $\overline{CS}$ Low transition occurs simultaneously with or after the $\overline{WE}$ Low transition, the outputs remain in a high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but, not tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse (tWP > tWHZ + tDW) to allow the I/O drivers to turn off data and to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP .

ORDERING INFORMATION



8

Integrated Device Technology, Inc.

16K x 16 CMOS STATIC RAM MODULE

IDT7MC4005

FEATURES:

- High-density 256K CMOS static RAM module
- Fast access time: 15ns (max.)
- Low profile 36-pin sidebraze ceramic DSIP (Dual Single In-line Package)
- Surface mounted LCC components mounted on a co-fired ceramic substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL-compatible
- Multiple GND pins for maximum noise immunity

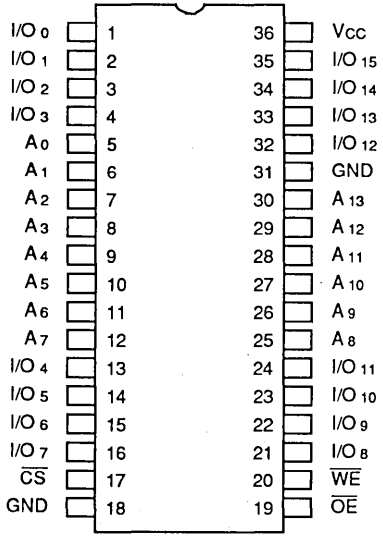
DESCRIPTION:

The IDT7MC4005 is a 16K x 16 CMOS static RAM module constructed on a co-fired ceramic substrate using four 16K x 4 static RAMs in leadless chip carriers. Extremely fast speeds can be achieved due to the use of 64K static RAMs fabricated in IDT's high-performance, high-reliability CEMOS™ technology. The IDT7MC4005 is available with access times as fast as 15ns, with minimal power consumption.

The IDT7MC family of ceramic DSIPs offers the optimum in packing density and profile height. The IDT7MC4005 is packaged in a 36-pin ceramic DSIP (Dual Single In-line Package). The dual row configuration allows 36 pins to be placed on a package 1.8 inches long and .27 inches wide. At only .500 inches high, this low profile package is ideal for systems with minimum board spacing.

All inputs and outputs of the IDT7MC4005 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

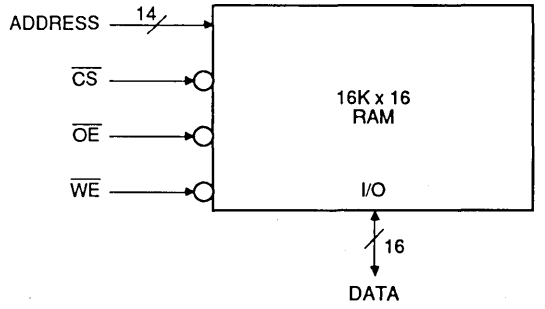
PIN CONFIGURATION[1]



2706 Drw 01

NOTE:
1. For module dimensions, please refer to module drawing M42 in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



2706 drw 02

PIN NAMES

I/O0-15	Data Inputs/Outputs
A0-13	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power
GND	Ground

2706 tbl 01

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2706 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2706 tbl 03

NOTE:
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND VOLTAGE SUPPLY

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2706 tbl 04

DC ELECTRICAL CHARACTERISTICS

(Vcc = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current (Address and Control)	Vcc = Max., V_{IN} = GND to Vcc	—	20	µA
$\|I_{LI}\|$	Input Leakage (Data)	Vcc = Max., V_{IN} = GND to Vcc	—	5	µA
$\|I_{LO}\|$	Output Leakage	Vcc = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to Vcc	—	5	µA
V_{OL}	Output Low Voltage	Vcc = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High Voltage	Vcc = Min., I_{OH} = –4mA	2.4	—	V

2706 tbl 05

DC ELECTRICAL CHARACTERISTICS

(Vcc = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7MC4005 Max.(1)	IDT7MC4005 Max.(2)	Unit
I_{CC1}	Operating Current	f = 0, $\overline{CS}$ = V_{IL} Vcc = Max., Output Open	480	400	mA
I_{CC2}	Dynamic Operating Current	f = f_{MAX}, $\overline{CS}$ = V_{IL} Vcc = Max., Outputs Open	600	500	mA
I_{SB}	Standby Supply Current	f = f_{MAX}, $\overline{CS}$ ≥ V_{IH} Vcc = Max., Outputs Open	240	200	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ Vcc - 0.2V V_{IN} ≥ Vcc - 0.2V or ≤ 0.2V	80	60	mA

2706 tbl 06

NOTE:
1. For tAA = 15, 20, 25ns versions.
2. For tAA = 30, 35ns versions.

8

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2706 tbl 08

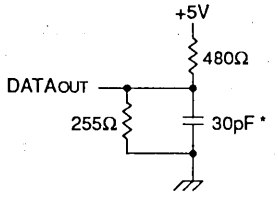
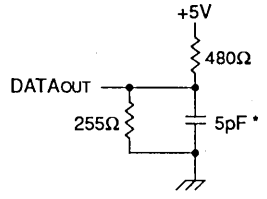


Figure 1. Output Load



2706 drw 03

Figure 2. Output Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

* Including scope and jig

AC ELECTRICAL CHARACTERISTICS

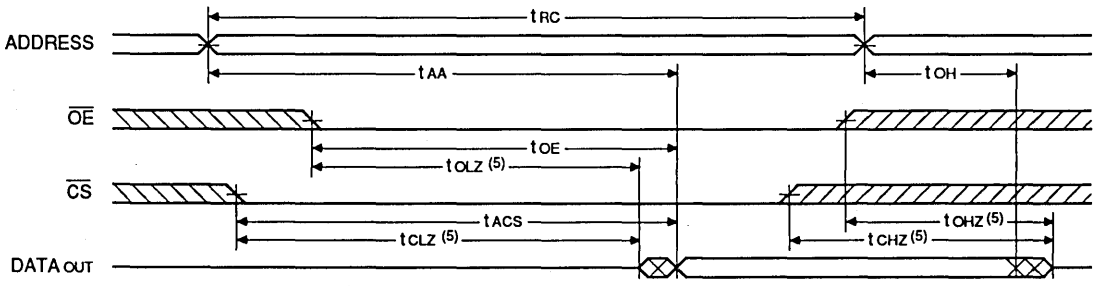
(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameters	7MC4005S15 Min.	7MC4005S15 Max.	7MC4005S20 Min.	7MC4005S20 Max.	7MC4005S25 Min.	7MC4005S25 Max.	7MC4005S30 Min.	7MC4005S30 Max.	7MC4005S35 Min.	7MC4005S35 Max.	Unit
Read Cycle												
t_{RC}	Read Cycle Time	15	—	20	—	25	—	30	—	35	—	ns
t_{AA}	Address Access Time	—	15	—	20	—	25	—	30	—	35	ns
t_{ACS}	Chip Select Access Time	—	15	—	20	—	25	—	30	—	35	ns
t_{CLZ} (1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	12	—	15	—	15	—	20	—	20	ns
t_{OLZ} (1)	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ} (1)	Chip Select to Output in High Z	—	8	—	8	—	10	—	13	—	15	ns
t_{OHZ} (1)	Output Disable to Output in High Z	—	8	—	8	—	15	—	15	—	15	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{PU} (1)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD} (1)	Chip Deselect to Power Down Time	—	15	—	20	—	25	—	30	—	35	ns
Write Cycle												
t_{WC}	Write Cycle Time	13	—	17	—	20	—	25	—	30	—	ns
t_{CW}	Chip Select to End of Write	13	—	17	—	20	—	25	—	25	—	ns
t_{AW}	Address Valid to End of Write	13	—	17	—	20	—	25	—	27	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	17	—	20	—	25	—	25	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ} (1)	Write Enable to Output in High Z	—	6	—	7	—	7	—	10	—	10	ns
t_{DW}	Data to Write Time Overlap	8	—	10	—	13	—	15	—	15	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	ns
t_{OW} (1)	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

2706 tbl 07

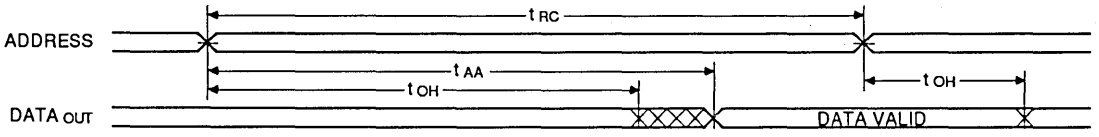
NOTE:
1. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



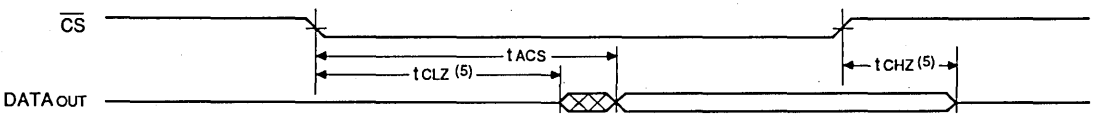
2706 drw 04

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2706 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)

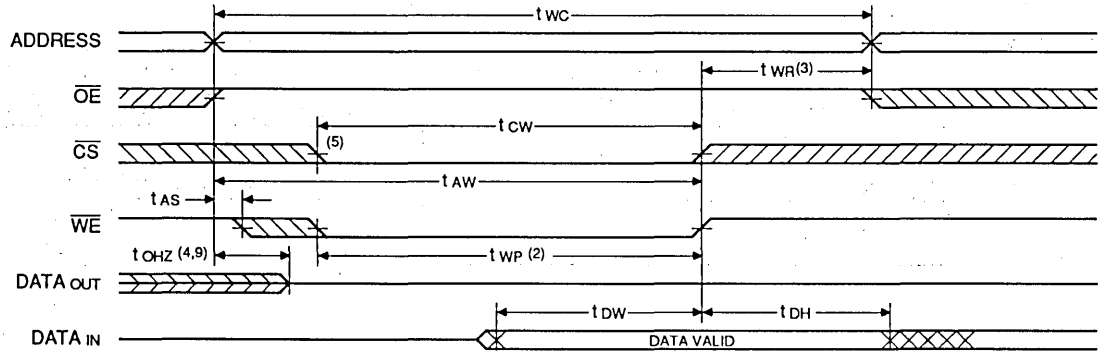


2706 drw 06

NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design but not tested.

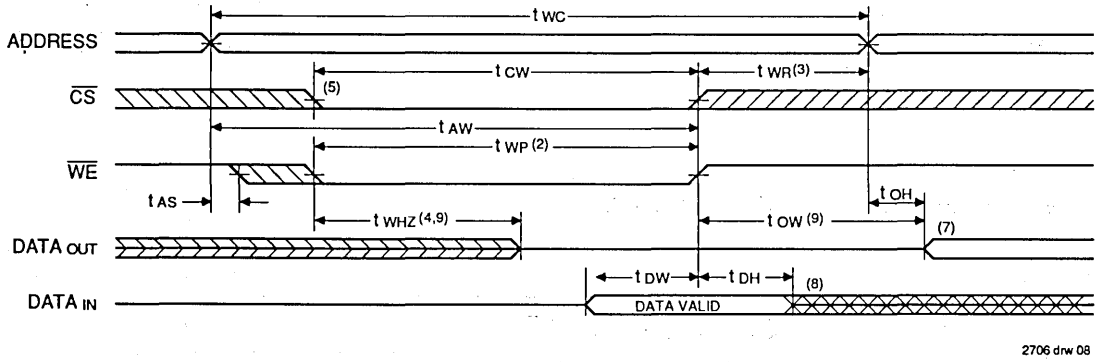
8

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1)



2706 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 2(1, 6)



2706 drw 08

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = VIL).
7. DOUT is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state. This parameter is guaranteed by design but not tested.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	DOUT	Active
Write	L	X	L	DIN	Active
Read	L	H	H	High Z	Active

2706 tbl 09

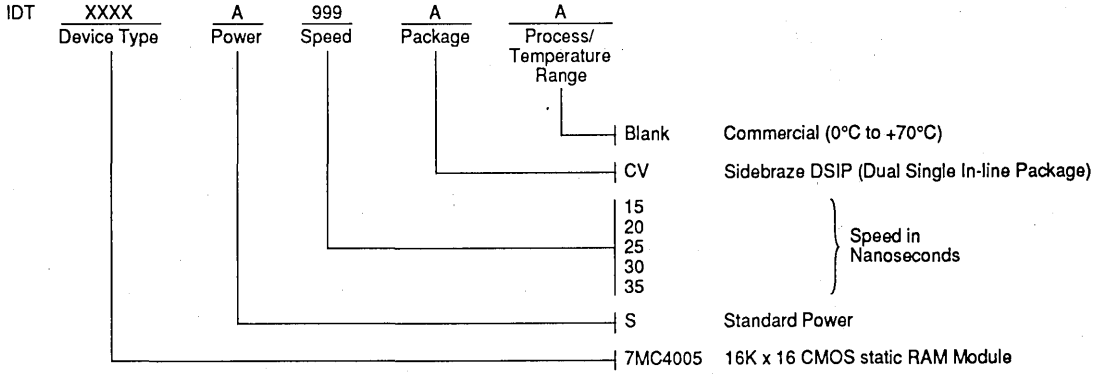
CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
CIN (D)	Input Capacitance (Data)	VIN = 0V	20	pF
CIN (A)	Input Capacitance Address and Control	VIN = 0V	50	pF
COUT	Output Capacitance	VOUT = 0V	20	pF

2706 tbl 10

NOTE:
1. This parameter is guaranteed by design but not tested.

ORDERING INFORMATION



2706 drw 10

8

Integrated Device Technology, Inc.

2 x 16K x 16 CMOS STATIC RAM MODULE

IDT7MB4009

FEATURES:

- High Density 512K CMOS static RAM Module
- Cost effective surface mount components mounted on an epoxy laminate (FR-4) substrate
- Packaged in a 44 pin, 600 mil wide DIP (Dual In-line Package)
- Fast access time: 15ns (max.)
- Common data and address pins for both banks of RAM resulting in increased density
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL compatible

DESCRIPTION:

The IDT7MB4009 is a 2 x 16K x 16 high-speed static RAM module constructed on an epoxy laminate surface using 8 16K x 4 static RAMs packaged in surface mount packages. Extremely fast speeds can be obtained by using RAMs fabricated in IDT's high performance, high reliability CEMOS™ technology.

The IDT7MB4009 is organized as two separate banks of 16K x 16 RAM with common address and data pins to minimize the module size. The IDT7MB4009 is packaged in a 44 pin, 600 mil wide DIP, packing 512K of fast memory in 1.8 square inches.

The IDT7MB4009 is available with access time as fast as 15ns, with maximum power consumption of 4.2W.

All inputs and outputs of the IDT7MB4009 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

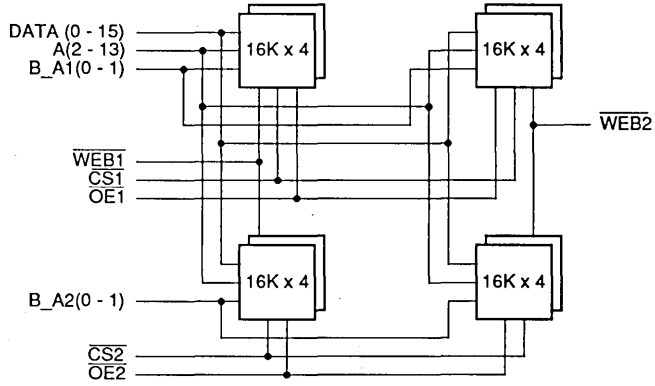
PIN CONFIGURATION[1]

GND	1	44	Vcc
D(0)	2	43	B_A1(0)
D(1)	3	42	B_A1(1)
D(2)	4	41	B_A2(0)
D(3)	5	40	B_A2(1)
D(4)	6	39	WEB2
D(5)	7	38	A(2)
D(6)	8	37	A(3)
D(7)	9	36	A(4)
D(8)	10	35	A(5)
GND	11	34	A(6)
$\overline{CS1}$	12	33	$\overline{CS2}$
$\overline{OE1}$	13	32	$\overline{OE2}$
D(9)	14	31	Vcc
D(10)	15	30	A(7)
D(11)	16	29	A(8)
D(12)	17	28	A(9)
WEB1	18	27	A(10)
D(13)	19	26	A(11)
D(14)	20	25	A(12)
D(15)	21	24	A(13)
Vcc	22	23	GND

2707 drw 01

NOTE:
1. For module dimensions, please refer to module drawing M13 in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



2707 drw 02

PIN NAMES

A (2-13)	Address Input
B_A1 (0-1)	Burst address, Bank 1
B_A2 (0-1)	Burst address, Bank 2
D (0-15)	Data Inputs/Outputs
$\overline{WEB1}$	Write Enable, Upper
$\overline{WEB2}$	Write Enable, Lower
$\overline{CS1}$, 2	Chip Select - Bank 1, 2
$\overline{OE1}$, 2	Output Enable - Bank 1, 2
GND	Ground
Vcc	Power Supply

2707 tbl 01

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–65 to +135	°C
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	50	mA

2707 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2707 tbl 03

NOTE:
1. V_{IL} = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND VOLTAGE SUPPLY

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2707 tbl 04

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7MB4009 Min.	IDT7MB4009 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current (Address and Control)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	40	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V
I_{CC1}	Operating Current	f = 0, $\overline{CS} \le V_{IL}$ V_{CC} = Max., Outputs Open	—	620	mA
I_{CC2}	Dynamic Operating Current	f = f_{MAX}, $\overline{CS} \le V_{IL}$, V_{CC} = Max., Outputs Open	—	760	mA
I_{SB}	Standby Supply Current	f = f_{MAX}, $\overline{CS} \ge V_{IH}$, V_{CC} = Max., Outputs Open	—	440	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS} \ge V_{IH}$ - 0.2V $V_{IN} \ge V_{CC}$ - 0.2V or $\le$ 0.2V	—	120	mA

2707 tbl 05

8

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Loads	See Figures 1 and 2

2707 tbl 07

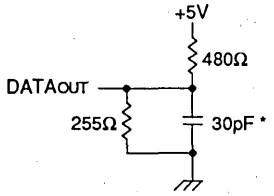
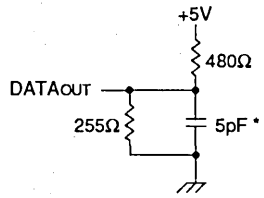


Figure 1. Output Load



2707 drw 03

Figure 2. Output Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW} and t_{WHZ})

* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

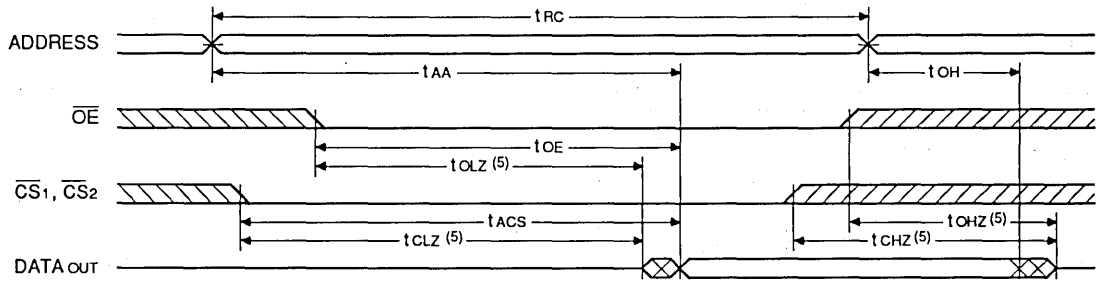
(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameters	7MB4009S15 Min.	7MB4009S15 Max.	7MB4009S20 Min.	7MB4009S20 Max.	7MB4009S25 Min.	7MB4009S25 Max.	Unit
Read Cycle								
t_{RC}	Read Cycle Time	15	—	20	—	25	—	ns
t_{AA}	Address Access Time	—	15	—	20	—	25	ns
t_{ACS}	Chip Select Access Time	—	15	—	20	—	25	ns
t_{CLZ} (1)	Chip Select to Output in Low Z	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	12	—	15	—	15	ns
t_{OLZ} (1)	Output Enable to Output in Low Z	5	—	5	—	5	—	ns
t_{CHZ} (1)	Chip Select to Output in High Z	—	8	—	10	—	12	ns
t_{OHZ} (1)	Output Disable to Output in High Z	—	8	—	10	—	15	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{PU} (1)	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD} (1)	Chip Deselect to Power Down Time	—	15	—	20	—	25	ns
Write Cycle								
t_{WC}	Write Cycle Time	13	—	18	—	20	—	ns
t_{CW}	Chip Select to End of Write	13	—	18	—	20	—	ns
t_{AW}	Address Valid to End of Write	13	—	18	—	21	—	ns
t_{AS}	Address Set Up Time	0	—	0	—	1	—	ns
t_{WP}	Write Pulse Width	12	—	17	—	20	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ} (1)	Write Enable to Output in High Z	—	6	—	7	—	8	ns
t_{DW}	Data to Write Time Overlap	8	—	10	—	13	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	ns
t_{OW} (1)	Output Active from End of Write	5	—	5	—	5	—	ns

2707 tbl 06

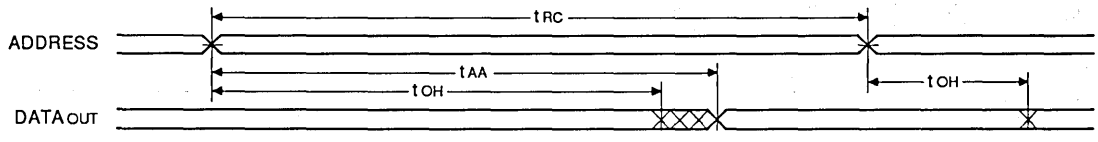
NOTE:
1. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



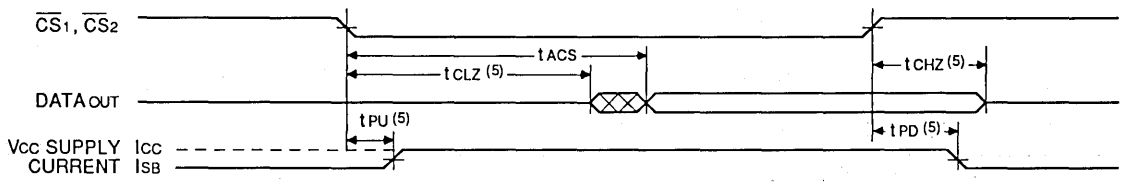
2707 drw 04

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2707 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)

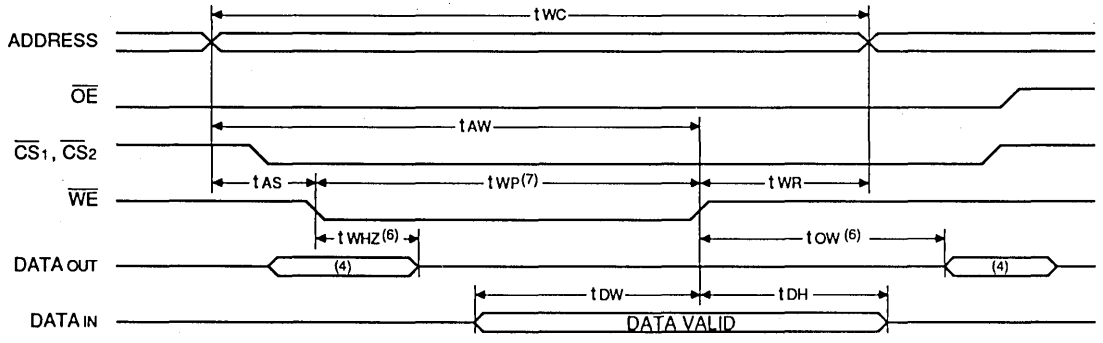


2707 drw 06

NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS_1}$ = V_{IL}, $\overline{CS_2}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS_1}$ and/or $\overline{CS_2}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design but not tested.

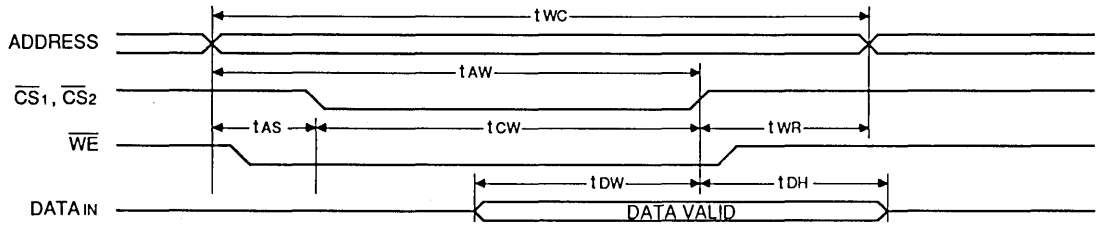
8

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



2707 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5, 8)



2707 drw 08

NOTES:
1. $\overline{WE}$, $\overline{CS_1}$ or $\overline{CS_2}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS_1}$, a low $\overline{CS_2}$ and a low $\overline{WE}$.
3. t_{WP} is measured from the earlier of $\overline{CS_1}$, $\overline{CS_2}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state. This parameter is guaranteed by design but not tested.
7. If $\overline{OE}$ is low during a WE controlled write cycle, the write pulse width must be the greater of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
8. $\overline{OE}$ = V_{IL}.

CAPACITANCE[1] (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
CIN(1)	Input Capacitance (Address)	VIN = 0V	40	pF
CIN(1)	Input Capacitance (Data)	VIN = 0V	20	pF
COUT	Output Capacitance	VOUT = 0V	20	pF

2707 tbl 08

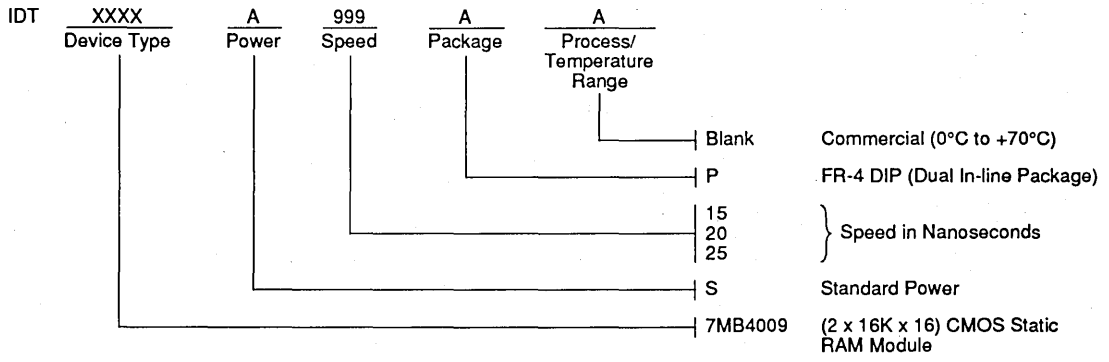
NOTE:
1. This parameter is guaranteed by design but not tested.

TRUTH TABLE

Mode	$\overline{CS1}$	$\overline{CS2}$	$\overline{OE1}$	$\overline{OE2}$	$\overline{WEB1}$	$\overline{WEB2}$	Output	Power
Standby	H	H	X	X	X	X	High Z	Standby
Read	L	H	L	X	H	H	DOUT BANK (1)	Active
Read	L	H	H	X	H	H	High Z	Active
Read	H	L	X	L	H	H	DOUT BANK (2)	Active
Read	H	L	X	H	H	H	High Z	Active
Write	L	H	X	X	L	H	DIN BANK (1) D (0-7)	Active
Write	L	H	X	X	H	L	DIN BANK (1) D (8-15)	Active
Write	H	L	X	X	L	H	DIN BANK (2) D (0-7)	Active
Write	H	L	X	X	H	L	DIN BANK (2) D (8-15)	Active
Write	L	H	X	X	L	L	DIN BANK (1) D (0-15)	Active
Write	H	L	X	X	L	L	DIN BANK (2) D (0-15)	Active

2707 tbl 09

ORDERING INFORMATION



2707 drw 09

8

Integrated Device Technology, Inc.

64K x 16
32K x 16
CMOS STATIC RAM MODULE

IDT8M624S
IDT8M612S

FEATURES:

- High-density CMOS static RAM module 64K x 16 organization (IDT8M624S) or 32K x 16 option (IDT8M612S)
- Fast access time:
  - — Commercial - 25ns (max.)
  - — Military - 35ns (max.)
- Separate upper byte (I/O_{9-16}) and lower byte (I/O_{1-8}) controls allow for greater application flexibility
- Offered in the JEDEC standard 40-pin DIP (dual in-line package)
- Leadless chip carriers (LCCs) mounted on an multi-layer ceramic substrate
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

The IDT8M624S/IDT8M612S are high-speed CMOS static RAM modules constructed on an co-fired, multi-layer ceramic substrate using four 32K x 8 static RAMs (IDT8M624S) or two 32K x 8 static RAMs (IDT8M612S) in hermetic LCC packages. Functional equivalence to proposed monolithic static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A_{15} to select one of the two 32K x 16 RAMs as the x16 output and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for lower byte (I/O_{1-8}) and upper byte (I/O_{9-16}) control, respectively. Extremely high speeds can be achieved by the use of IDT71256 (32K x 8) static RAMs fabricated in IDT's high-performance, high-reliability technology, CEMOS™.

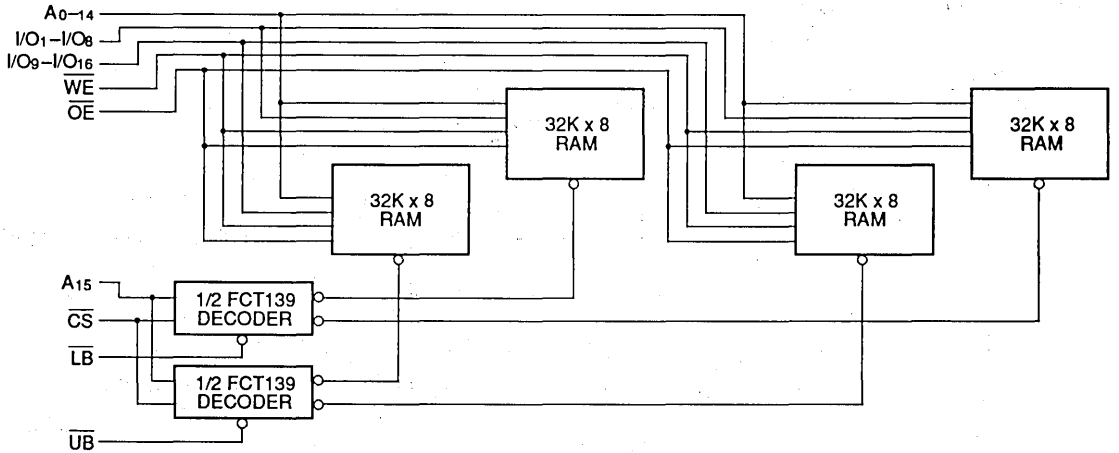
The IDT8M624S/IDT8M612S are available with access times as fast as 25ns over the commercial temperature range and 35ns over the military termperature range, with maximum operating power consumption of only 3.4W (64K x 16 commercial option). The module also offers a full standby mode of 451mW (max.).

The IDT8M624S/IDT8M612S modules are offered in the JEDEC standard 40-pin sidebrazed DIP.

All inputs and outputs of the IDT8M624S/ IDT8M612S are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

All military module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883 Class B, making them ideally suited for applications demanding the highest level of performance and reliability.

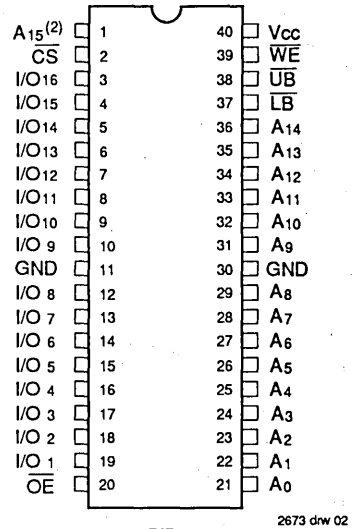
FUNCTIONAL BLOCK DIAGRAM



2673 drw 01

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION[1]



2673 drw 02

DIP
TOP VIEW

NOTE:
1. For module dimensions, please refer to module drawing M11 (8M624S) and M12 (8M612S) in the packaging section.
2. For 32K x 16 option (IDT8M612S), A15 (Pin 1) must be connected to GND for proper operation of the module.

PIN NAMES

A0–15	Addresses
I/O1–16	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
Vcc	Power
GND	Ground
$\overline{OE}$	Output Enable
$\overline{UB}$	Upper Byte Control
$\overline{LB}$	Lower Byte Control

2673 tbl 01

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{UB}$	$\overline{LB}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	X	X	High Z	Standby
Standby	L	H	H	X	X	High Z	Standby
Read	L	L	L	L	H	DOUT 1-16	Active
Lower Byte Read	L	H	L	L	H	DOUT 1-8	Active (X8)
Upper Byte Read	L	L	H	L	H	DOUT 9-16	Active (X8)
Read	L	L	L	H	H	High Z	Active
Lower Byte Read	L	H	L	H	H	High Z	Active (X8)
Upper Byte Read	L	L	H	H	H	High Z	Active (X8)
Write	L	L	L	X	L	DIN 1-16	Active
Lower Byte Write	L	H	L	X	L	DIN 1-8	Active (X8)
Upper Byte Write	L	L	H	X	L	DIN 9-16	Active (X8)

2673 tbl 10

8

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

2673 tbl 02

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	8MP624 Max.	8MP612 Max.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	V_{IN} = 0V	25	14	pF
$C_{IN(A1)}$	Input Capacitance (A0–14, $\overline{OE}$, $\overline{WE}$)	V_{IN} = 0V	50	25	pF
$C_{IN(C)}$	Input Capacitance (A15, $\overline{CS}$)	V_{IN} = 0V	23	23	pF
$C_{IN(C)}$	Input Capacitance ($\overline{LB}$, $\overline{UB}$)	V_{IN} = 0V	13	13	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	25	14	pF

2673 tbl 07

NOTE:

1. This parameter is guaranteed by design, but not tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commerical	0°C to +70°C	0V	5.0V ± 10%
Military	-55°C to +125°C	0V	5.0V ± 10%

2673 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

2673 tbl 08

NOTE:

1. V_{IL} (min) = –3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C or -55°C to +125°C)

Symbol	Parameter	Test Conditions	IDT8M624S			IDT8M612S			Unit
			Min.	Max.(1)	Max.(2)	Min.	Max.(1)	Max.(2)	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	20	15	—	10	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max.; $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	15	—	5	15	µA
I_{CCX16}	Dynamic Operating Current in X16 Mode	V_{CC} = Max., $\overline{CS}$, $\overline{UB}$ and $\overline{LB}$ = V_{IL}, f = f_{MAX}; Output Open	—	450	340	—	400	300	mA
I_{CCX8}	Dynamic Operating Current in X8 Mode	$\overline{CS}$, $\overline{UB}$ or $\overline{LB}$ = V_{IL}, V_{CC} = Max., f = f_{MAX}, Output Open	—	275	200	—	225	170	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ ≥ V_{IH} or $\overline{UB}$ ≥ V_{IL} and $\overline{LB}$ ≥ V_{IH}	—	100	80	—	50	40	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} – 0.2V; V_{IN} > V_{CC} – 0.2V or < 0.2V	—	60	80	—	30	40	mA
V_{OL}	Output Low Voltage	V_{CC} = Min. I_{OL} = 8mA	—	0.4	0.4	—	0.4	0.4	mA
V_{OH}	Output High Voltage	V_{CC} = Min. I_{OH} = –4mA	2.4	—	—	2.4	—	—	mA

2673 tbl 11

NOTES:

1. t_{AA} = 25, 30, 35ns.
2. t_{AA} = 40, 45, 50, 60, 70, 85, 100ns.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2673 tbl 09

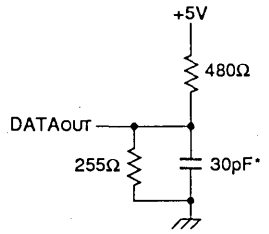


Figure 1. Output Load

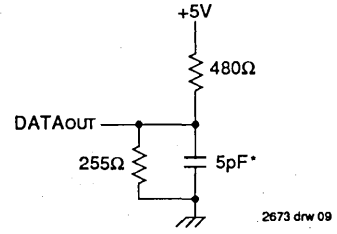


Figure 2. Output Load (for t_{OLZ}, t_{OHZ}, t_{WHZ}, and t_{OW})

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

(VCC = 5V ±10%, TA = 0°C to +70°C or -55°C to +125°C)

Symbol	Parameter	8M612S25 8M624S25		8M612S30 8M624S30		8M612S35 8M624S35		8M612S40 8M624S40		8M612S45 8M624S45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t_{RC}	Read Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	—	40	—	45	ns
t_{ACS}	Chip Select Access Time	—	25	—	30	—	35	—	40	—	45	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	10	—	11	—	13	—	25	—	25	ns
t_{OLZ}[1]	Chip Deselection to Output in High Z	2	—	2	—	2	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Select to Output in High Z	—	15	—	16	—	20	—	20	—	20	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	8	—	10	—	15	—	20	—	20	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	25	—	30	—	35	—	40	—	45	ns
Write Cycle												
t_{WC}	Write Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_{CW}	Chip Select to End of Write	20	—	25	—	30	—	35	—	40	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	30	—	35	—	40	—	ns
t_{AS}	Address Set-up Time	3	—	3	—	3	—	5	—	5	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	23	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	2	—	2	—	2	—	5	—	5	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	10	—	11	—	15	—	15	—	15	ns
t_{DW}	Data to Write Time Overlap	11	—	13	—	14	—	15	—	20	—	ns
t_{DH}	Data Hold from Write Time	3	—	3	—	3	—	3	—	5	—	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

8

AC ELECTRICAL CHARACTERISTICS (Continued)

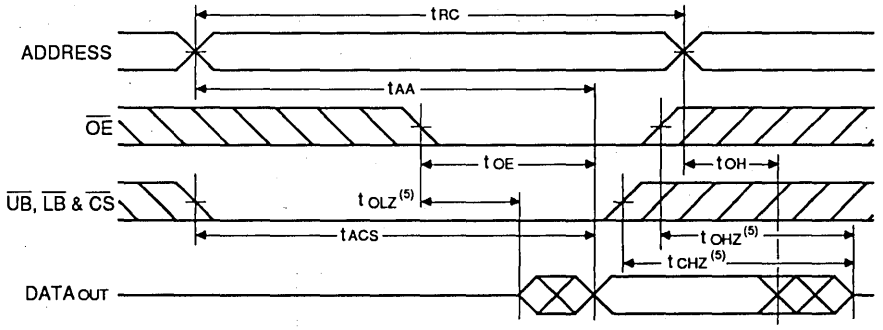
(V_{CC} = 5V ±10%, T_A = 0° to +70°C or −55°C to +125°C)

Symbol	Parameter	8M612S50 8M624S50		8M612S60 8M624S60		8M612S70 8M624S70		8M612S85 8M624S85		8M612S100 8M624S100		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t_{RC}	Read Cycle Time	50	—	60	—	70	—	85	—	100	—	ns
t_{AA}	Address Access Time	—	50	—	60	—	70	—	85	—	100	ns
t_{ACS}	Chip Select Access Time	—	50	—	60	—	70	—	85	—	100	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	30	—	35	—	40	—	50	—	60	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Select to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	50	—	60	—	70	—	85	—	70	ns
Write Cycle												
t_{WC}	Write Cycle Time	50	—	60	—	70	—	85	—	100	—	ns
t_{CW}	Chip Select to End of Write	45	—	55	—	65	—	75	—	90	—	ns
t_{AW}	Address Valid to End of Write	45	—	55	—	65	—	75	—	90	—	ns
t_{AS}	Address Set-up Time	5	—	5	—	5	—	5	—	5	—	ns
t_{WP}	Write Pulse Width	40	—	50	—	60	—	70	—	80	—	ns
t_{WR}	Write Recovery Time	5	—	5	—	5	—	10	—	10	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{DW}	Data to Write Time Overlap	20	—	25	—	30	—	35	—	40	—	ns
t_{DH}	Data Hold from Write Time	5	—	5	—	5	—	5	—	5	—	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

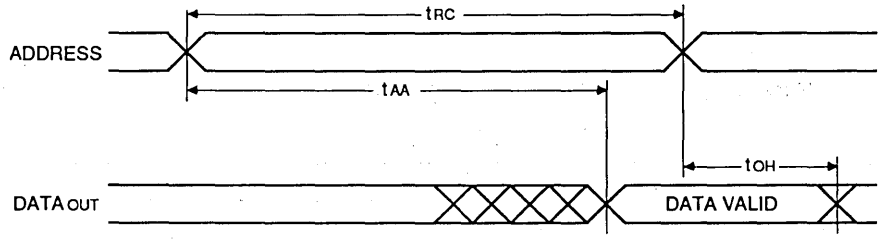
2673 tbl 12

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



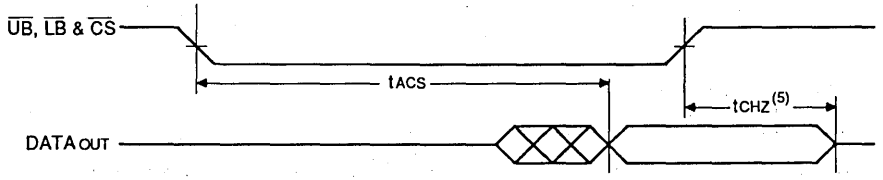
2673 drw 03

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2673 drw 04

TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)

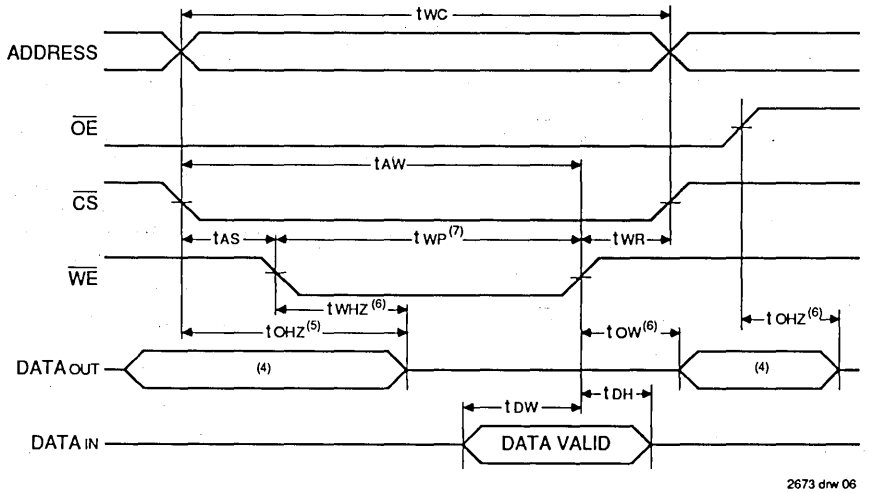


2673 drw 05

NOTES:
1. $\overline{WE}$ is high for Read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{UB}$, $\overline{LB}$ = V_{IL} for 16 output active.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

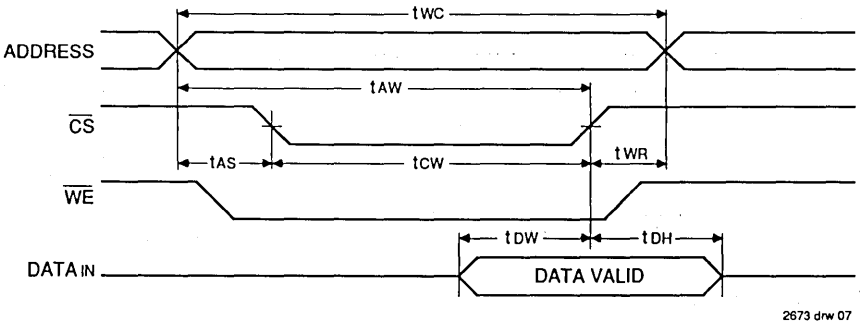
8

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



2673 drw 06

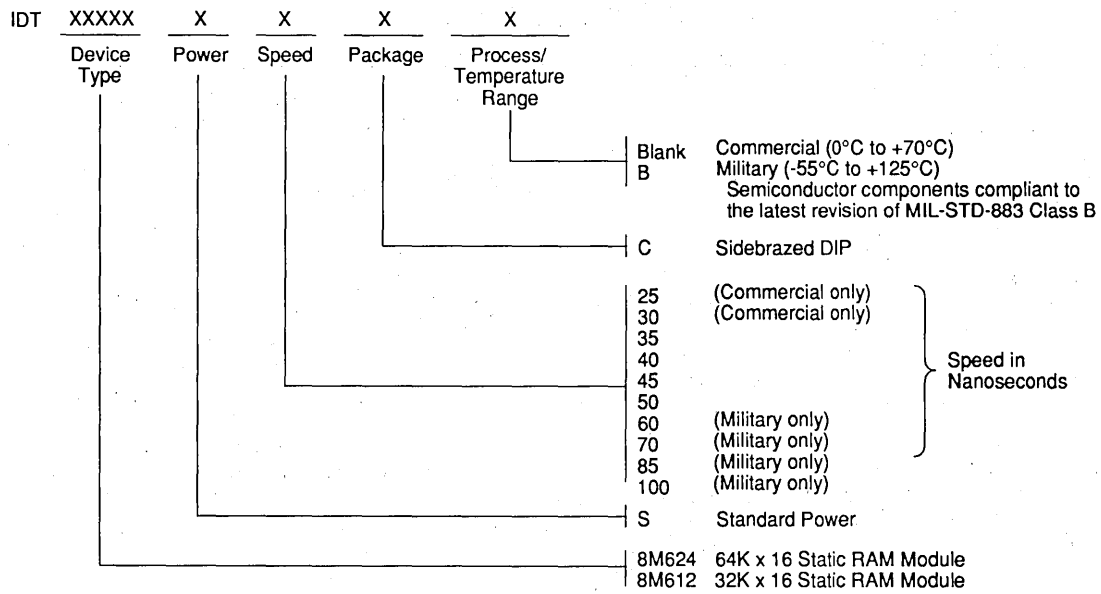
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



2673 drw 07

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transactions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse ((tWP) > tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

ORDERING INFORMATION



2673 drw 10

8

Integrated Device Technology, Inc.

64K x 16
32K x 16
CMOS STATIC RAM MODULE

IDT8MP624S
IDT8MP612S

FEATURES:

- High-density CMOS static RAM module 64K x 16 organization (IDT8MP624) or 32K x 16 option (IDT8MP612)
- Fast access time: 25ns (max.)
- Separate upper byte (I/O_{9-16}) and lower byte (I/O_{1-8}) controls allows for greater application flexibility
- Offered in a 40-pin SIP (single in-line package) for maximum space-savings
- Cost-effective plastic SO's mounted on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

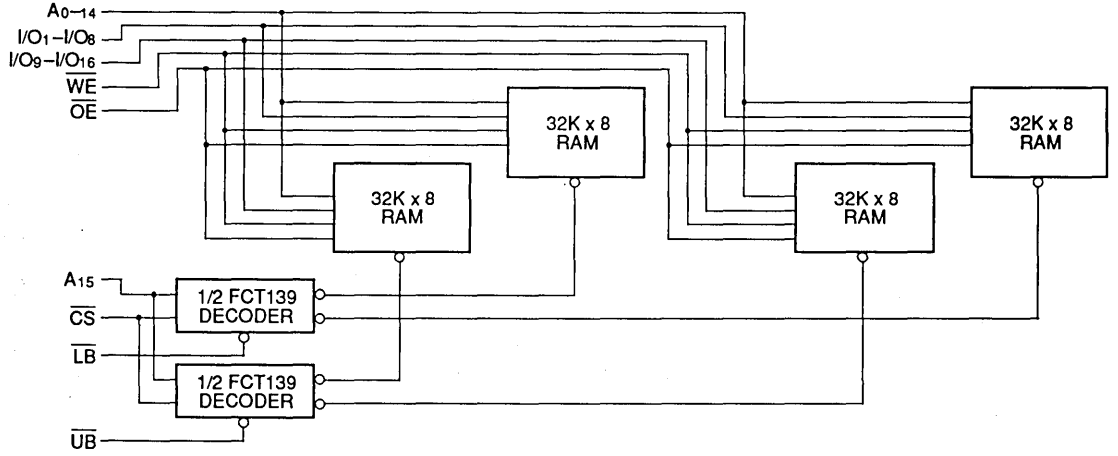
The IDT8MP624S/IDT8MP612S are high-speed CMOS static RAM modules constructed on an epoxy laminate substrate using four 32K x 8 static RAMs (IDT8MP624S) or two 32K x 8 static RAMs (IDT8MP612S) in plastic surface-mount packages. Functional equivalence to proposed monolithic static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A_{15} to select one of the two 32K x 16 RAMs as the by-16 output and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for lower byte (I/O_{1-8}) and upper byte (I/O_{9-16}) control, respectively. Extremely high speeds can be achieved by the use of IDT71256 (32K x 8) static RAMs fabricated in IDT's high-performance, high-reliability technology, CEMOS™.

The IDT8MP624S/IDT8MP612S are available with access times as fast as 25ns over the commercial temperature range, with maximum operating power consumption of only 3.4W (64K x 16 option). The module also offers a full standby mode of 451mW (max.)

The IDT8MP624S/IDT8MP612S modules are offered in a vertically mounted 40-pin FR-4 SIP. For the 40-pin JEDEC sidebrazed DIP, refer to the IDT8M624S/IDT8M612S.

All inputs and outputs of the IDT8MP624S/ IDT8MP612S are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

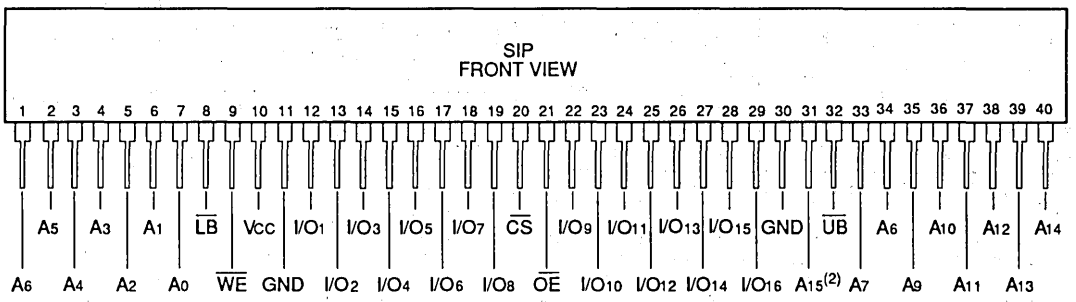
FUNCTIONAL BLOCK DIAGRAM



2673 drw 01

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION[1]



2673 drw 02

NOTE:
1. For module dimensions, please refer to module drawing M39 (8MP624S) and M40 (8MP612S) in the packaging section.
2. For 32K x 16 option (IDT8MP612S), A15 must be connected to GND for proper operation of the module.

PIN NAMES

A0–15	Addresses
I/O1–16	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
Vcc	Power
GND	Ground
$\overline{OE}$	Output Enable
$\overline{UB}$	Upper Byte Control
$\overline{LB}$	Lower Byte Control

2673 tbl 01

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commerical	0°C to +70°C	0V	5.0V ± 10%

2673 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE:
1. VIL (min) = –3.0V for pulse width less than 20ns.

2673 tbl 08

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{UB}$	$\overline{LB}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	X	X	High Z	Standby
Standby	L	H	H	X	X	High Z	Standby
Read	L	L	L	L	H	DOUT 1-16	Active
Lower Byte Read	L	H	L	L	H	DOUT 1-8	Active (X8)
Upper Byte Read	L	L	H	L	H	DOUT 9-16	Active (X8)
Read	L	L	L	H	H	High Z	Active
Lower Byte Read	L	H	L	H	H	High Z	Active (X8)
Upper Byte Read	L	L	H	H	H	High Z	Active (X8)
Write	L	L	L	X	L	DIN 1-16	Active
Lower Byte Write	L	H	L	X	L	DIN 1-8	Active (X8)
Upper Byte Write	L	L	H	X	L	DIN 9-16	Active (X8)

2673 tbl 10

8

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTES: 2673 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	8MP624 Max.	8MP612 Max.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	V_{IN} = 0V	25	14	pF
$C_{IN(A1)}$	Input Capacitance (A0–14, $\overline{OE}$, $\overline{WE}$)	V_{IN} = 0V	50	25	pF
$C_{IN(C)}$	Input Capacitance (A15, $\overline{CS}$)	V_{IN} = 0V	23	23	pF
$C_{IN(C)}$	Input Capacitance ($\overline{LB}$, $\overline{UB}$)	V_{IN} = 0V	13	13	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	25	14	pF

NOTE: 2673 tbl 07

1. This parameter is guaranteed by design, but not tested.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT8MP624S			IDT8MP612S			Unit
			Min.	Max.(1)	Max.(2)	Min.	Max.(1)	Max.(2)	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	20	15	—	10	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max.; $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	15	—	5	15	µA
I_{CCX16}	Dynamic Operating Current in X16 Mode	V_{CC} = Max., $\overline{CS}$, $\overline{UB}$ and $\overline{LB}$ = V_{IL}, f = f_{MAX}; Output Open	—	450	340	—	400	300	mA
I_{CCX8}	Dynamic Operating Current in X8 Mode	$\overline{CS}$, $\overline{UB}$ or $\overline{LB}$ = V_{IL}, V_{CC} = Max., f = f_{MAX}, Output Open	—	275	200	—	225	170	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ ≥ V_{IH} or $\overline{UB}$ ≥ V_{IL} and $\overline{LB}$ ≥ V_{IH}	—	100	80	—	50	40	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} – 0.2V; V_{IN} > V_{CC} – 0.2V or < 0.2V	—	60	80	—	30	40	mA
V_{OL}	Output Low Voltage	V_{CC} = Min. I_{OL} = 8mA	—	0.4	0.4	—	0.4	0.4	mA
V_{OH}	Output High Voltage	V_{CC} = Min. I_{OH} = –4mA	2.4	—	—	2.4	—	—	mA

NOTES: 2673 tbl 11

1. t_{AA} = 25, 30, 35ns.
2. t_{AA} = 40, 45, 50, 60, 70ns.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2673 tbl 09

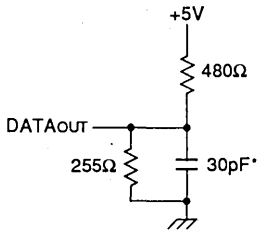


Figure 1. Output Load

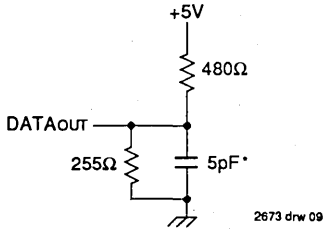


Figure 2. Output Load (for t_{OLZ}, t_{OHZ}, t_{WHZ}, and t_{OW})

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

(VCC = 5V ±10%, TA = 0°C to +70°C)

		8MP612S25 8MP624S25		8MP612S30 8MP624S25		8MP612S35 8MP624S35		8MP612S40 8MP624S40		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
Read Cycle										
t_{RC}	Read Cycle Time	25	—	30	—	35	—	40	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	—	40	ns
t_{ACS}	Chip Select Access Time	—	25	—	30	—	35	—	40	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	10	—	11	—	13	—	25	ns
t_{OLZ}[1]	Chip Deselection to Output in High Z	2	—	2	—	2	—	5	—	ns
t_{CHZ}[1]	Chip Select to Output in High Z	—	15	—	16	—	20	—	20	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	8	—	10	—	15	—	20	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	25	—	30	—	35	—	40	ns
Write Cycle										
t_{WC}	Write Cycle Time	25	—	30	—	35	—	40	—	ns
t_{CW}	Chip Select to End of Write	20	—	25	—	30	—	35	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	30	—	35	—	ns
t_{AS}	Address Set-up Time	3	—	3	—	3	—	5	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	23	—	30	—	ns
t_{WR}	Write Recovery Time	2	—	2	—	2	—	5	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	10	—	11	—	15	—	15	ns
t_{DW}	Data to Write Time Overlap	11	—	13	—	14	—	15	—	ns
t_{DH}	Data Hold from Write Time	3	—	3	—	3	—	3	—	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	5	—	5	—	ns

8

AC ELECTRICAL CHARACTERISTICS (Continued)

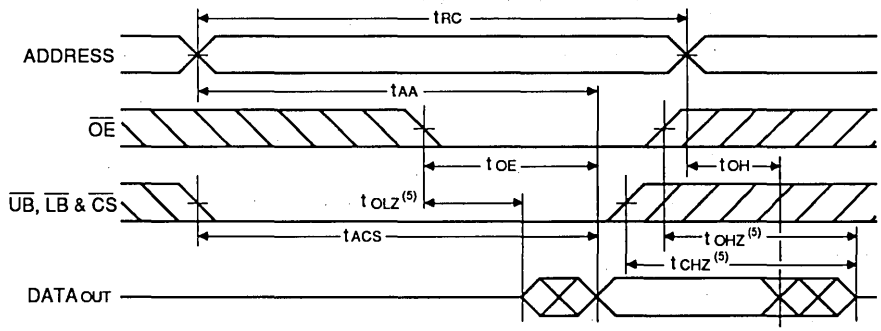
(V_{CC} = 5V ±10%, T_A = −55°C to +125°C and 0° to +70°C)

Symbol	Parameter	8MP612S45 8MP624S45		8MP612S50 8MP624S50		8MP612S60 8MP624S60		8MP612S70 8MP624S70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	45	—	50	—	60	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	50	—	60	—	70	ns
t_{ACS}	Chip Select Access Time	—	45	—	50	—	60	—	70	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	25	—	30	—	35	—	40	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Select to Output in High Z	—	20	—	20	—	25	—	30	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	20	—	20	—	25	—	30	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	45	—	50	—	60	—	70	ns
Write Cycle										
t_{WC}	Write Cycle Time	45	—	50	—	60	—	70	—	ns
t_{CW}	Chip Select to End of Write	40	—	45	—	55	—	65	—	ns
t_{AW}	Address Valid to End of Write	40	—	45	—	55	—	65	—	ns
t_{AS}	Address Set-up Time	5	—	5	—	5	—	5	—	ns
t_{WP}	Write Pulse Width	35	—	40	—	50	—	60	—	ns
t_{WR}	Write Recovery Time	5	—	5	—	5	—	5	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	15	—	20	—	25	—	30	ns
t_{DW}	Data to Write Time Overlap	20	—	20	—	25	—	30	—	ns
t_{DH}	Data Hold from Write Time	5	—	5	—	5	—	5	—	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	5	—	5	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

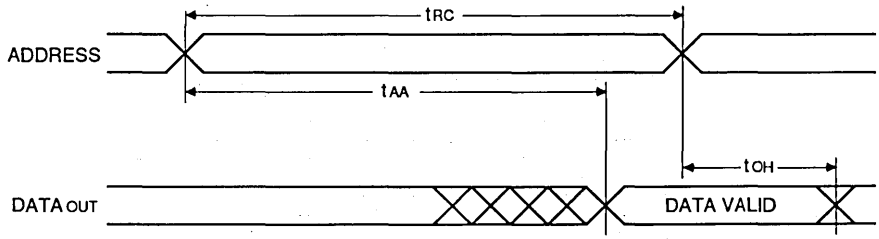
2673 tbl 12

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



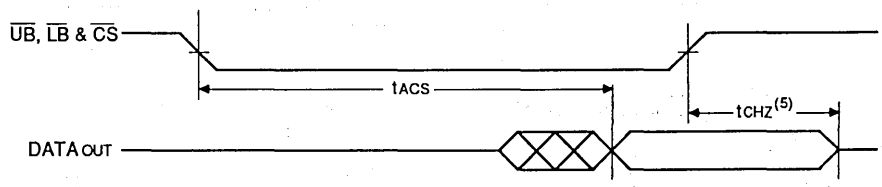
2673 drw 03

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2673 drw 04

TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)

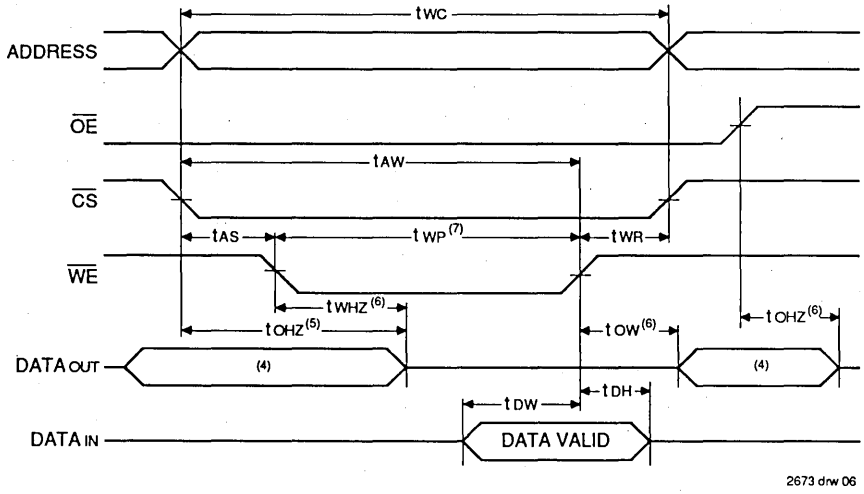


2673 drw 05

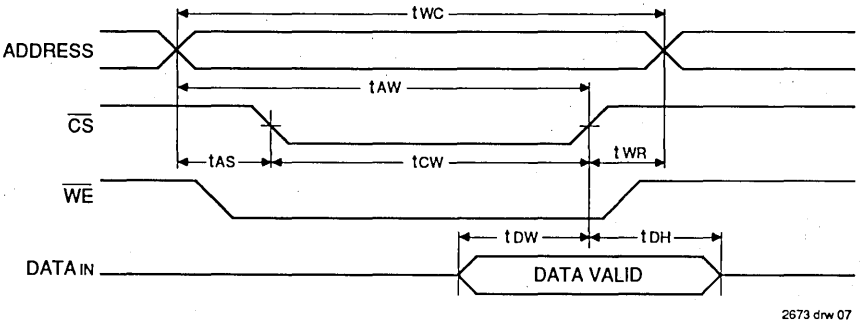
NOTES:
1. $\overline{WE}$ is high for Read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{UB}$, $\overline{LB}$ = V_{IL} for 16 output active.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

8

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)

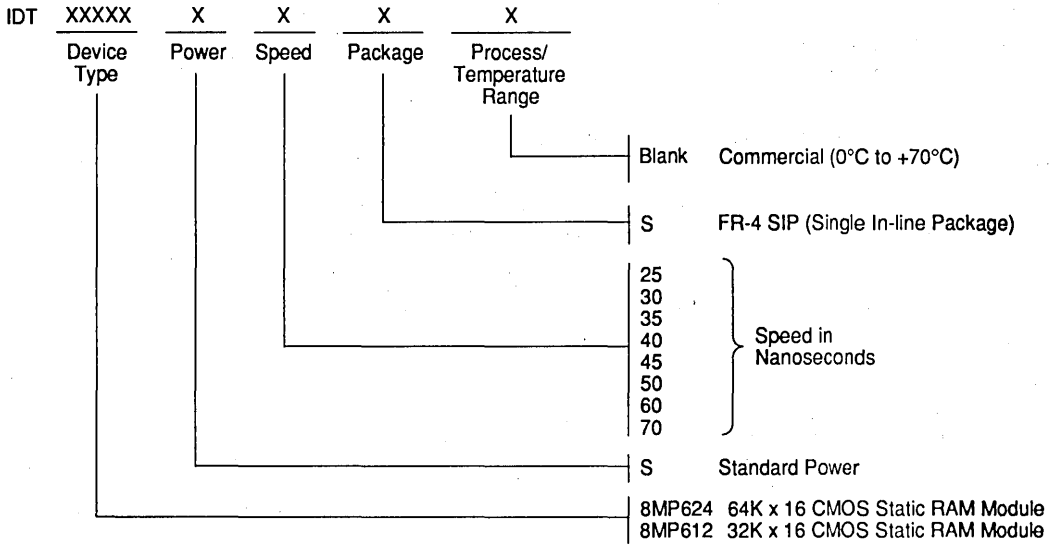


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transactions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse ((tWP) > tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

ORDERING INFORMATION



2673 drw 08

8

Integrated Device Technology, Inc.

64K x 16
32K x 16
CMOS STATIC RAM MODULE

IDT8MP624L
IDT8MP612L

FEATURES:

- High-density CMOS static RAM module 64K x 16 organization (IDT8MP624) or 32K x 16 option (IDT8MP612)
- Fast access time
  — 70ns (max.) over commercial temperature range
- Separate Upper byte (I/O_{6-16}) and Lower byte control allows for greater application flexibility
- Low-power consumption
- Offered in a vertically mounted 40-pin SIP (single in-line package) for maximum space-savings
- Cost-effective plastic SO's mounted on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

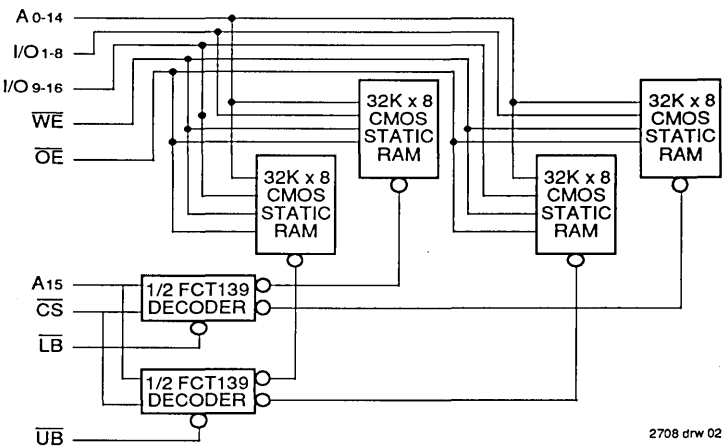
The IDT8MP624L/IDT8MP612L are high-speed CMOS static RAMs constructed on an epoxy laminate substrate using four 32K x 8 static RAMs (IDT8MP624L) or two 32K x 8 static RAMs (IDT8MP612L) in plastic surface-mount packages. Functional equivalence to proposed monolithic static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A_{15} to select one of the two 32K x 16 RAMs as the by-16 output and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for lower byte (I/O_{1-8}) and upper byte (I/O_{9-16}) control, respectively. (On the IDT8MP612L 32K x 16 option, A_{15} needs to be extremely grounded for proper operation.)

The IDT8MP624L/IDT8MP612L are available with access times as fast as 70ns for commercial temperature range, with maximum operating power consumption of only 825mW (64K x 16 option). The module also offers a full standby mode of 2.2mW (max.).

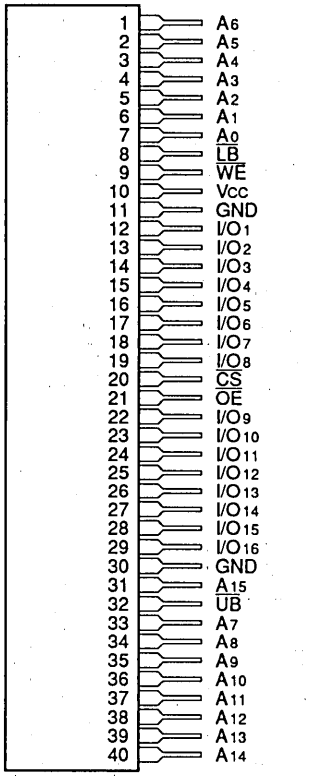
The IDT8MP624L/IDT8MP612L are offered in a 40-pin FR-4 SIP package. For the 32-pin JEDEC sidebrazed DIP, refer to the IDT8M624S/IDT8M612S.

All inputs and outputs of the IDT8MP624L/IDT8MP612L are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION[1]



2708 drw 01

SIP
SIDE VIEW

NOTE:
1. For module dimensions, please refer to module drawing M39 (8MP624L) and M40 (8MP612L in the packaging section.
2. On the IDT8MP612L (32K x 16) option, A15 (Pin 31) requires external grounding for proper operation of the module.

PIN NAMES

A0-15	Addresses
I/O1-16	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
Vcc	Power
GND	Ground
$\overline{OE}$	Output Enable
$\overline{UB}$	Upper Byte Control
$\overline{LB}$	Lower Byte Control

2708 tbl 01

8

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

2708 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2708 tbl 03

NOTE:
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND VOLTAGE SUPPLY

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2708 tbl 04

DC ELECTRICAL CHARACTERISTICS

(Vcc = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT8MP624L Min.	IDT8MP624L Typ.(1)	IDT8MP624L Max.	IDT8MP612L Min.	IDT8MP612L Typ.(1)	IDT8MP612L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	Vcc = Max., V_{IN} = GND to Vcc	—	—	15	—	—	15	µA
$\|I_{LO}\|$	Output Leakage Current	Vcc = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to Vcc	—	—	15	—	—	15	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$, $\overline{UB}$, and $\overline{LB}$ = V_{IL} Vcc = Max., Output Open f = 0	—	20	80	—	20	80	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$, $\overline{UB}$, and $\overline{LB}$ = V_{IL} Vcc = Max., Output Open f = f_{MAX}	—	80	150	—	80	150	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} Vcc = Max., Output Open f = f_{MAX}	—	6	15	—	6	15	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}$ ≥ Vcc - 0.2V V_{IN} ≥ Vcc - 0.2V or ≤ 0.2V	—	10	400	—	10	300	µA
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA, Vcc = Min.	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1.0mA, Vcc = Min.	2.4	—	—	2.4	—	—	V

2708 tbl 05

NOTE:
1. Vcc = 5V, T_A = +25°C

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2708 tbl 06

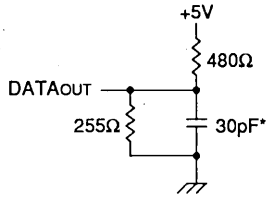


Figure 1. Output Load

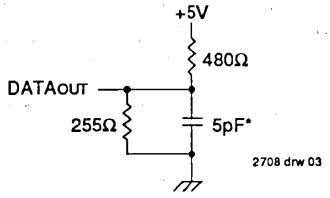


Figure 2. Output Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

* Including scope and jig

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

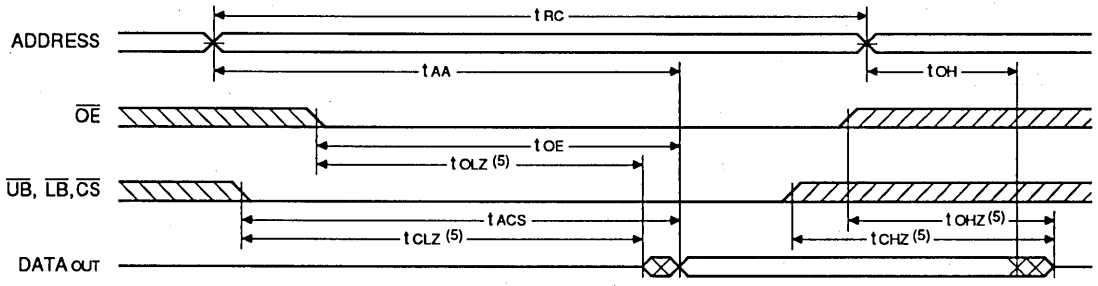
Symbol	Parameters	IDT8MP624L70 IDT8MP612L70 Min.	Max.	IDT8MP624L85 IDT8MP612L85 Min.	Max.	IDT8MP624L100 IDT8MP612L100 Min.	Max.	Unit
Read Cycle								
t_{RC}	Read Cycle Time	70	—	85	—	100	—	ns
t_{AA}	Address Access Time	—	70	—	85	—	100	ns
t_{ACS}	Chip Select Access Time	—	70	—	85	—	100	ns
t_{CLZ} (1)	Chip Select to Output in Low Z	10	—	10	—	10	—	ns
t_{OE}	Output Enable to Output Valid	—	40	—	50	—	60	ns
t_{OLZ} (1)	Output Enable to Output in Low Z	5	—	5	—	5	—	ns
t_{CHZ} (1)	Chip Select to Output in High Z	—	30	—	35	—	40	ns
t_{OHZ} (1)	Output Disable to Output in High Z	—	30	—	35	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	ns
t_{PU} (1)	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD} (1)	Chip Deselect to Power Down Time	—	70	—	85	—	100	ns
Write Cycle								
t_{WC}	Write Cycle Time	70	—	85	—	100	—	ns
t_{CW}	Chip Select to End of Write	65	—	75	—	90	—	ns
t_{AW}	Address Valid to End of Write	65	—	75	—	90	—	ns
t_{AS}	Address Setup Time	5	—	5	—	5	—	ns
t_{WP}	Write Pulse Width	60	—	70	—	80	—	ns
t_{WR}	Write Recovery Time	10	—	10	—	10	—	ns
t_{WHZ} (1)	Write Enable to Output in High Z	—	30	—	35	—	40	ns
t_{DW}	Data to Write Time Overlap	30	—	35	—	40	—	ns
t_{DH}	Data Hold from Write Time	5	—	5	—	5	—	ns
t_{OW} (1)	Output Active from End of Write	5	—	5	—	5	—	ns

2708 tbl 07

NOTE:
1. This parameter is guaranteed by design but not tested.

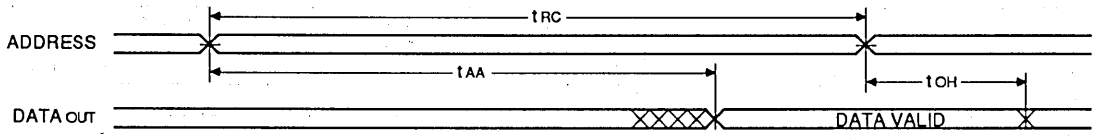
8

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



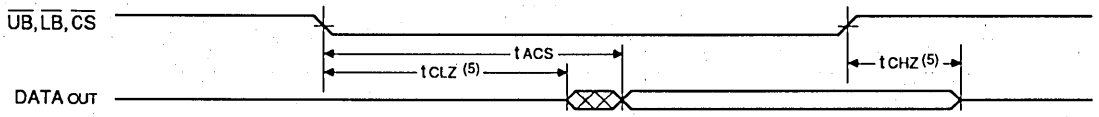
2708 drw 04

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2708 drw 05

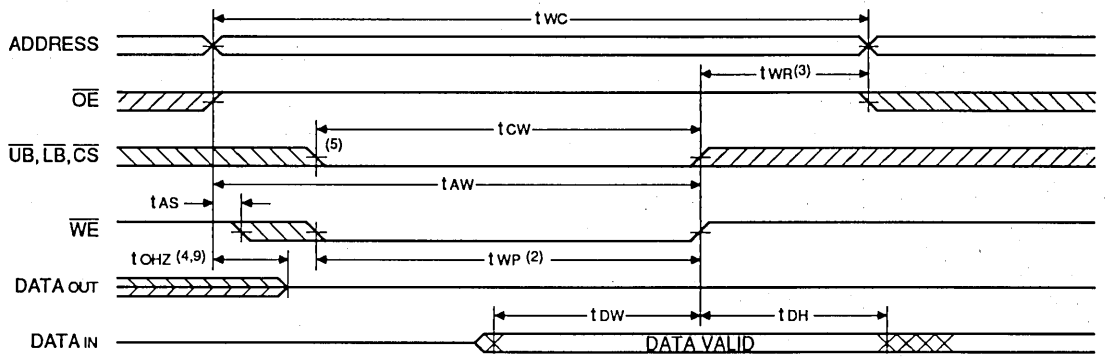
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



2708 drw 06

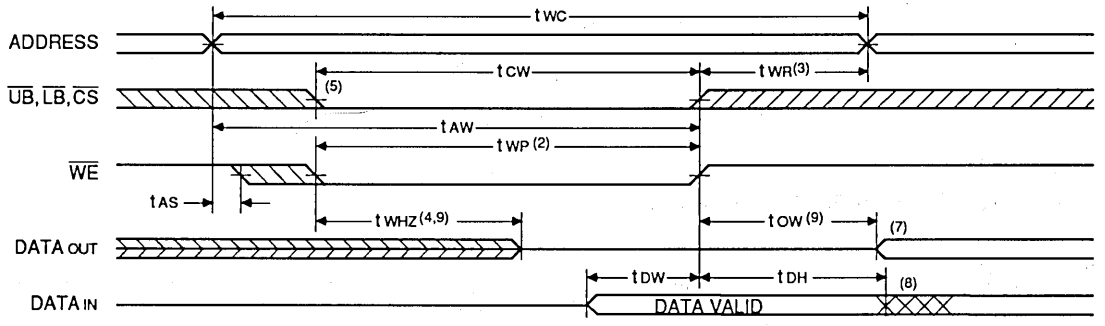
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{UB}$, $\overline{LB}$ = V_{IL} for x16 output active.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1)



2708 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 2(1, 6)



2708 drw 08

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ or $\overline{UB}$ and $\overline{LB}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
5. If the $\overline{CS}$, $\overline{UB}$ and $\overline{UB}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = VIL).
7. DOUT is the same phase of write data of this write cycle.
8. If $\overline{CS}$, $\overline{UB}$ and $\overline{UB}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state. This parameter is guaranteed by design but not tested.

8

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{UB}$	$\overline{LB}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	X	X	High Z	Standby
Standby	L	H	H	X	X	High Z	Standby
Read	L	L	L	L	H	DOUT 1-16	Active
Lower Byte Read	L	H	L	L	H	DOUT 1-8	Active (XB)
Upper Byte Read	L	L	H	L	H	DOUT 9-16	Active (XB)
Read	L	L	L	H	H	High Z	Active
Lower Byte Read	L	H	L	H	H	High Z	Active (XB)
Upper Byte Read	L	L	H	H	H	High Z	Active (XB)
Write	L	L	L	X	L	DIN 1-16	Active
Lower Byte Read	L	H	L	X	L	DIN 1-8	Active (XB)
Upper Byte Read	L	L	H	X	L	DIN 9-16	Active (XB)

2708 tbl 08

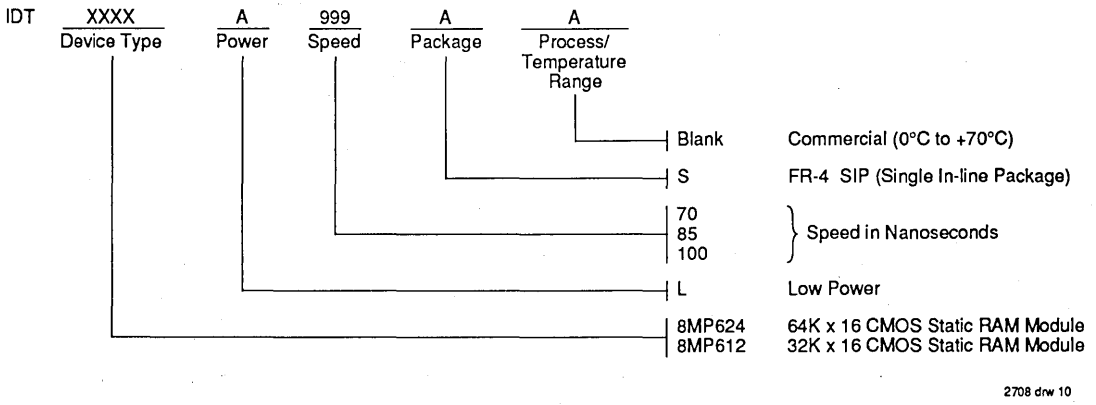
CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	35	pF
COUT	Output Capacitance	VOUT = 0V	40	pF

2708 tbl 09

NOTE:
1. This parameter is guaranteed by design but not tested.

ORDERING INFORMATION



2708 drw 10

Integrated Device Technology, Inc.

64K X 16 CMOS STATIC RAM MODULE

IDT7M624S

FEATURES:

- High-density 1 Megabit CMOS static RAM module
- Customer-configured to 64K x 16, 128K x 8 or 256K x 4
- Fast access times
  - — Military: 30ns (max.)
  - — Commercial: 25ns (max.)
- Low power consumption
  - — Active: 4.8W (typ. in 64K x 16 organization)
  - — Standby: 1.6mW (typ.)
- Offered in 40-pin, 900 mil center sidebraze DIP, achieving very high memory density
- Single 5V (±10%) power supply
- Dual GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

The IDT7M624 is a 1 Megabit high-speed CMOS static RAM module constructed on a multi-layered ceramic substrate using sixteen 64K x 1 static RAMs in leadless chip carriers. Making four chip select lines available (one for each group of 4 RAMs) allows the user to configure the memory into a 64K x 16, 128K x 8 or 256K x 4 organization. In addition, extremely high speeds can be achieved by the use of IDT7187s fabricated in IDT's high-performance, high-reliability technology, CEMOS™.

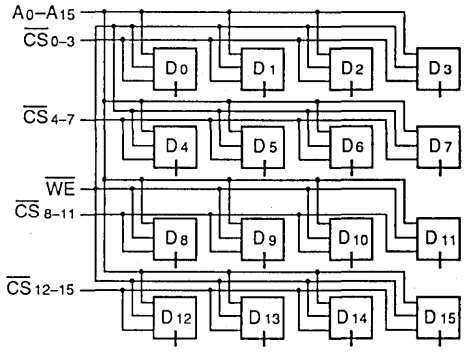
The IDT7M624 is available with access times as fast as 25ns (max.) commercial and 30ns (max.) military temperature range, with maximum operating power consumption of only 12.3W (significantly less if organized 128K x 8 or 256K x 4). The module also offers a standby power mode of 5.7W (max.) and a full standby mode of 1.7W (max.).

The IDT7M624 is offered in a 40-pin, 900 mil center sidebraze DIP.

All inputs and outputs of the IDT7M624 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

All IDT military module semiconductor components are compliant with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

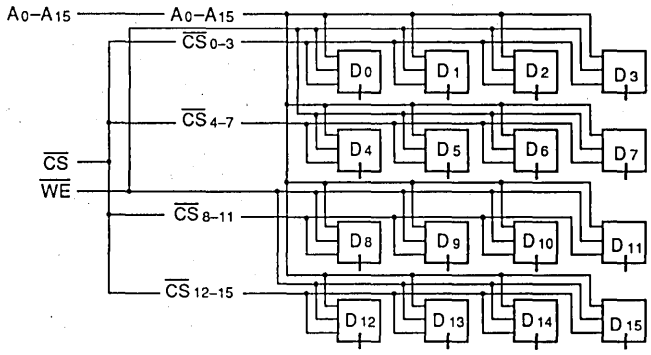


2663 drw 01

8

CEMOS is a trademark of Integrated Device Technology, Inc.

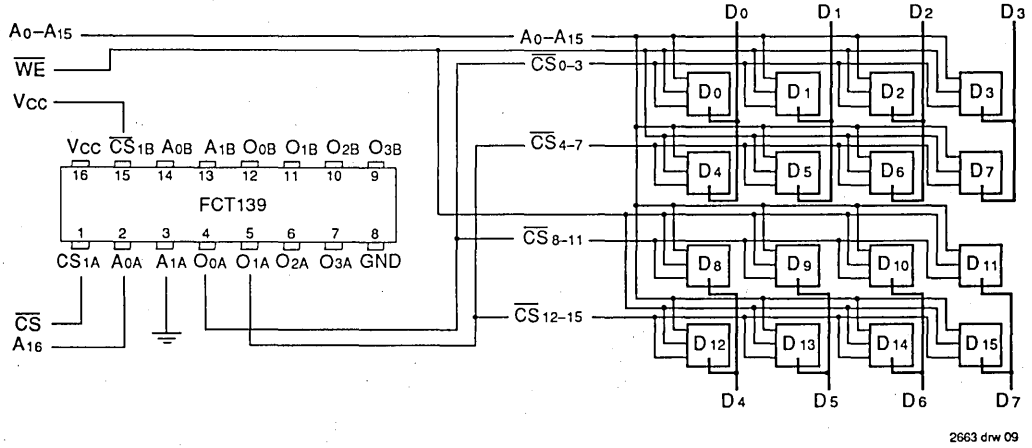
IDT7M624
64K x 16 CONFIGURATION



2663 drw 08

NOTE:
1. All chip selects tied together since, in a by 16 configuration, all chips are either on or off.

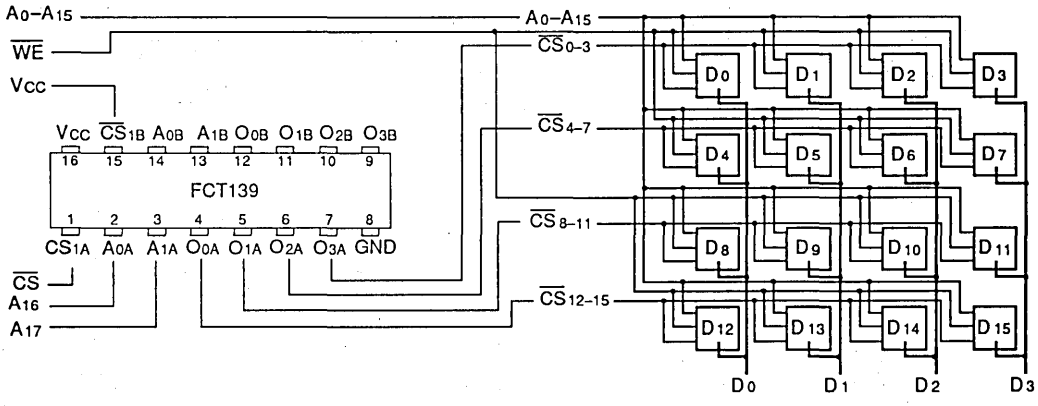
IDT7M624
128K x 8 CONFIGURATION



2663 drw 09

NOTE:
1. The chip selects are tied together in groups of two. The decoder uses the new higher order address pin (A_{16}) to determine which of the two banks of memory are enabled.

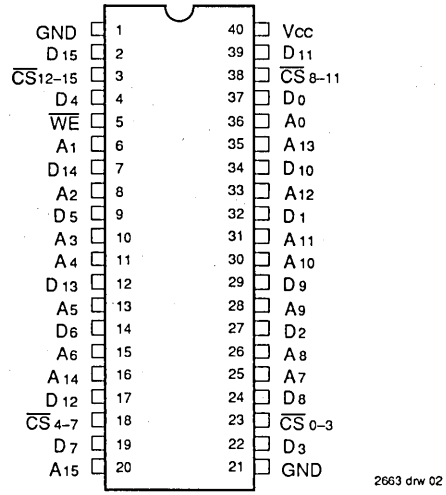
IDT7M624
256K x 4 CONFIGURATION



NOTE:
1. Each chip is now controlled by the two higher order address pins A16 and A17.

8

PIN CONFIGURATION[1]



2663 drw 02

DIP
TOP VIEW

NOTE:
1. For module dimensions, please refer to module drawing M8 in the packaging section

TRUTH TABLE

Mode	$\overline{CS}$xx	$\overline{WE}$	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	DATAOUT	Active
Write	L	L	High Z	Active

2663 tbl 01

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to + 125°C	0V	5.0V ± 10%
Commercial	0°C to + 70°C	0V	5.0V ± 10%

2663 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE:
1. VIL = -3.0V for pulse width less than 20ns.

2663 tbl 03

PIN NAMES

A0-15	Address
D0-15	Data Input/Output
$\overline{CS}$xx	Chip Selects
$\overline{WE}$	Write Enable
Vcc	Power
GND	Ground

2663 tbl 04

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	° C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	° C
TSTG	Storage Temperature	-55 to + 125	-65 to +155	° C
bUT	DC Output Current	50	50	mA

NOTE:

2663 tbl 05

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = + 25° C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Units
CIN	Input Capacitance	VIN= 0V	130	pF
COUT	Output Capacitance	VOUT= 0V	35	pF

NOTE:

2663 tbl 06

1. This parameter is guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = -55° C to +125°C and 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7M624S Min.	Typ[1]	Max.[3]	Max.[4]	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	—	—	20	20	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = 5.5V, $\overline{CS}$xx = V_{IH}, V_{OUT} = GND to V_{CC}	—	—	20	20	µA
I_{CCX16}	Operating Current in X16 mode	$\overline{CS}$xx = V_{IL}, Output Open, V_{CC} = 5.5V, f = fMAX	—	960	1950	2240	mA
I_{CCX8}	Operating Current in X8 mode	$\overline{CS}$xx = V_{IL}, Output Open, Min. Duty Cycle = 100%	—	720	1380	1640	mA
I_{CCX4}	Operating Current in X4 mode	$\overline{CS}$xx = V_{IL}, Output Open, Min. Duty Cycle = 100%	—	600	1100	1340	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$xx ≥ V_{IH} (TTL Level), V_{CC} = 5.5V, Output Open	—	480	820	1040	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}$xx ≥ V_{CC} – 0.2V V_{IN} ≥ V_{CC} – 0.2V or ≤ 0.2V (CMOS Level)	—	0.32	320[2]	320	mA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = 4.5V	—	—	0.5	0.5	V
		I_{OL} = 8mA, V_{CC} = 4.5V	—	—	0.4	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC}= 4.5V	2.4	—	—	—	V

2663 tbl 07

NOTES:
1. Typical limits are at V_{CC} = 5.0V, + 25° C.
2. I_{SB1} max. at commercial temperature = 240mA.
2. t_{AA} = 30, 35, 45, 55, 65ns.
3. t_{AA} = 25ns.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2663 tbl 08

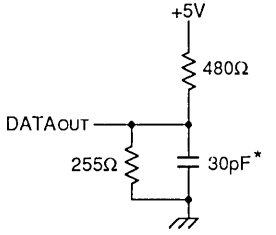


Figure 1. Output Load

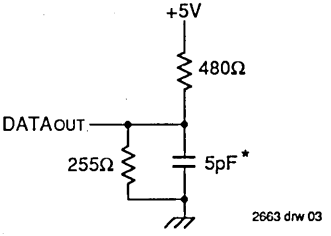


Figure 2. Output Load
(for t_{CHZ}, t_{CLZ}, t_{WHZ} and t_{OW})

*Including scope and jig.

8

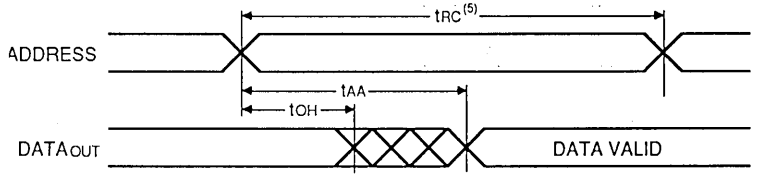
AC ELECTRICAL CHARACTERISTICS

(Vcc = 5V ± 10%, TA = -55° C to +125°C and 0°C to +70°C)

Symbol	Parameter	7M624S25 Com'l. Only		7M624S30		7M624S35		7M624S45		7M624S55		7M624S65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle														
t RC	Read Cycle Time	25	—	30	—	35	—	45	—	55	—	65	—	ns
t AA	Address Access Time	—	25	—	30	—	35	—	45	—	55	—	65	ns
t ACS	Chip Select Access Time	—	25	—	30	—	35	—	45	—	55	—	65	ns
t OH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
t CLZ	Chip Selection to Output in Low Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
t CHZ	Chip Deselection to Output in High Z	—	20	—	25	—	30	—	30	—	30	—	30	ns
t PU	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t PD	Chip Selection to Power Down Time	—	25	—	30	—	35	—	35	—	35	—	35	ns
Write Cycle														
t WC	Write Cycle Time	25	—	30	—	35	—	45	—	55	—	65	—	ns
t CW	Chip Selection to End of Write	22	—	25	—	30	—	40	—	50	—	55	—	ns
t AW	Address Valid to End of Write	22	—	25	—	30	—	40	—	50	—	55	—	ns
t AS	Address Set-up Time	2	—	3	—	5	—	5	—	5	—	10	—	ns
t WP	Write Pulse Width	20	—	20	—	25	—	30	—	35	—	40	—	ns
t WR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t DW	Data Valid to End of Write	15	—	20	—	20	—	25	—	25	—	30	—	ns
t DH	Data Hold Time	5	—	5	—	5	—	5	—	5	—	5	—	ns
t WHZ	Write Enable to Output in High Z	0	20	0	25	0	30	0	30	0	30	0	35	ns
t OW	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	5	—	ns

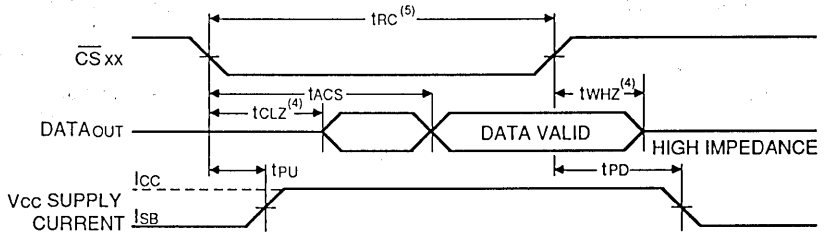
2663 tbl 09

TIMING WAVEFORM OF READ CYCLE NO. 1 (1, 2)



2663 drw 04

TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 3)

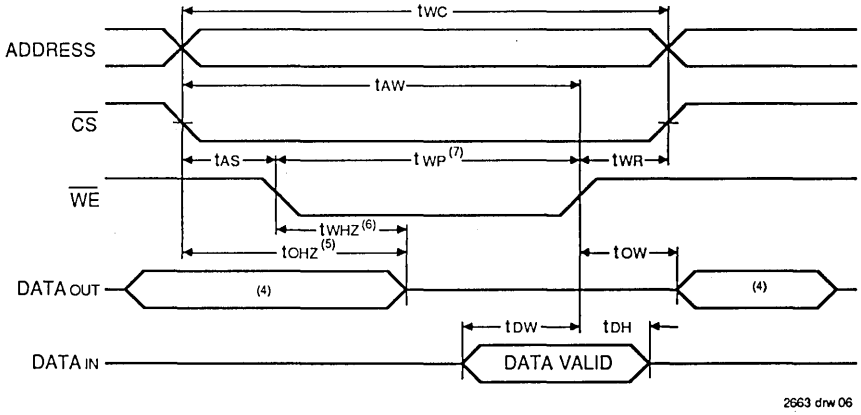


2663 drw 05

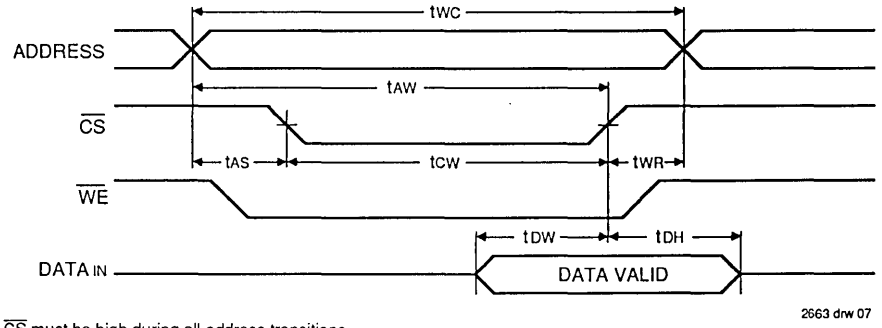
NOTES:

1. WE is high for READ cycle.
2. CSxx is low for READ cycle.
3. Address valid prior to or coincident with CSxx transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is guaranteed by design but not tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1 2, 3, 7)



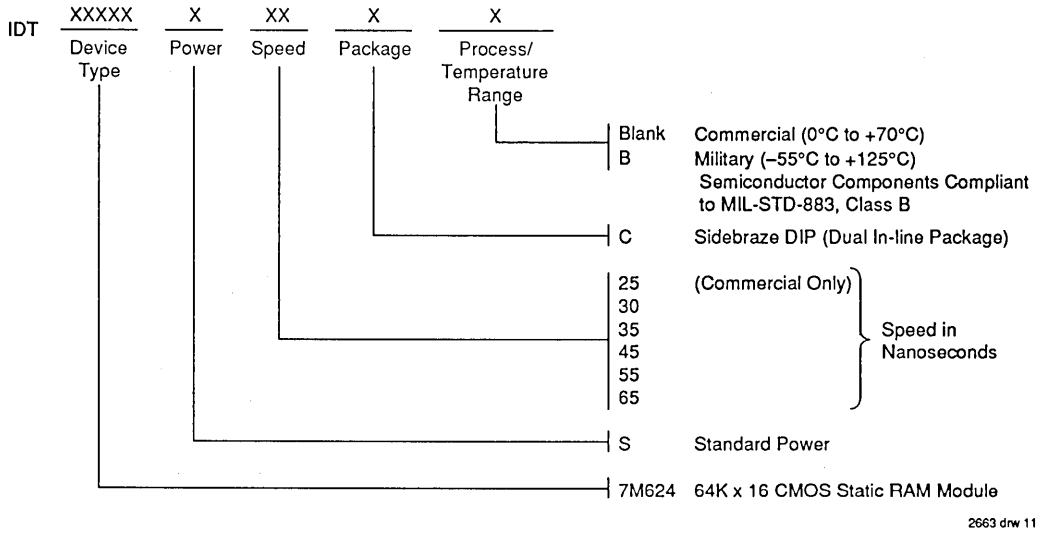
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design but not tested.

8

ORDERING INFORMATION



2663 drw 11

Integrated Device Technology, Inc.

256K x 16 CMOS STATIC RAM MODULE

IDT7M4016

FEATURES:

- High-density 4 megabit CMOS static RAM module
- Fast access time
  - commercial: 25ns (max.)
  - military: 35ns (max.)
- Low power consumption
- Available in 48-pin, 900 mil wide sidebrazed DIP (Dual In-line Package)
- Multiple GND pins for maximum noise immunity
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

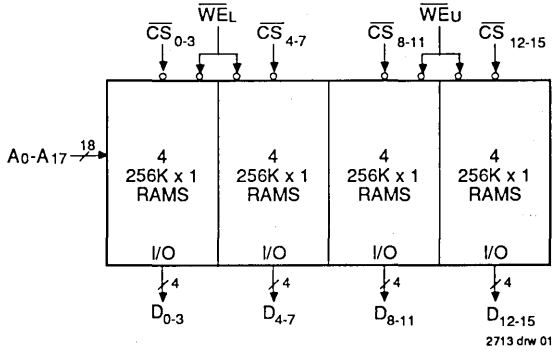
The IDT7M4016 is a 4 megabit high-speed CMOS static RAM module constructed on a multi-layered ceramic substrate using sixteen (256K x 1) static RAMs in leadless chip carriers. The IDTM4016 is an upgrade from the IDT7M624 (64K x 16 RAM module) offering four times the memory density in the same size package. Making four chip select lines available (one for each group of four RAMs) allows the user to configure the memory into a 256K x 16, 512K x 8 or 1024K x 4 organization.

The IDT7M4016 is packaged in a 48-pin, 900 mil wide sidebrazed DIP. This enables four megabits of static RAM memory to be placed in less than 2.2 square inches of board space.

All inputs and outputs of the IDT7M4016 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

All IDT military module semiconductor components are compliant to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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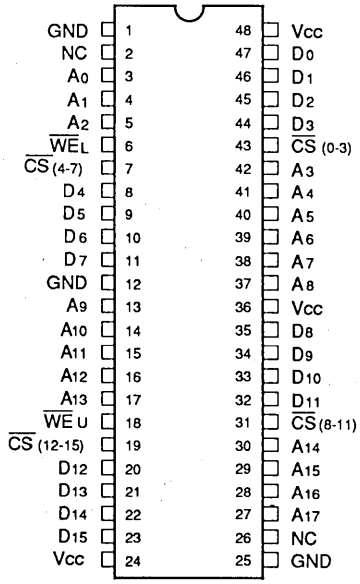
PIN CONFIGURATION (1)



2713 drw 02

DIP
TOP VIEW

NOTE:
1. For module dimension, please refer to module drawing M15 in the packaging section.

PIN NAMES

Vcc	Power
GND	Ground
A0–A17	Addresses
D0–D15	Data Input/Output
$\overline{CS}$0-3	Chip Selects
$\overline{WE}$L	Write Enable (Lower Byte)
$\overline{WE}$U	Write Enable (Upper Byte)

2713 tbl 01

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	DATAOUT	Active
Write	L	L	High Z	Active

2713 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2713 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
CIN(D)	Input Capacitance (Data)	VIN = 0V	30	pF
CIN(A)	Input Capacitance (Address and Control)	VIN = 0V	200	pF
COUT	Output Capacitance	VOUT = 0V	30	pF

NOTE: 2713 tbl 04
1. This parameter is guaranteed by design, but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE: 2713 tbl 05
1. VIL = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C + 125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2713 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	80	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	—	V

2713 tbl 07

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

			IDT7M4016(1) Max.		IDT7M4016(2) Max.		
Symbol	Parameter	Test Conditions	Com'l.	Mil.	Com'l.	Mil.	Unit
I_{CC1}	Operating Current	V_{CC} = Max., CS ≤ V_{IL},f = 0, Outputs Open	1760	—	1600	1760	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max., CS ≤ V_{IL}, f = f_{MAX} Output Open	2560	—	2400	2560	mA
I_{SB}	Standby Supply Current	V_{CC} = Max.,$\overline{CS}$ ≥ V_{IH}, f = f_{MAX},Ouputs Open	560	—	560	560	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} -0.2V, V_{IN} ≥ V_{CC} -0.2V or ≤ 0.2V	480	—	480	480	mA

NOTES:
1. 25, 30ns
2. 35, 45, 55ns

2713 tbl 08

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2713 tbl 09

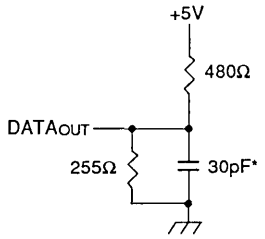


Figure 1. Output Load

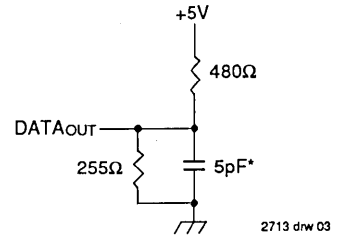


Figure 2. Output Load (for t_{CLZ}, t_{CHZ}, t_{OW}, t_{WHZ})

*Including scope and jig

8

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameters	7M4016S25 Com'l. Only		7M4016S30 Com'l. Only		7M4016S35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25	—	30	—	35	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	ns
t_{ACS}	Chip Select Access Time	—	25	—	30	—	35	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	13	—	17	—	20	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Down Time	—	25	—	30	—	35	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	25	—	30	—	35	—	ns
t_{CW}	Chip Selection to End of Write	25	—	30	—	35	—	ns
t_{AW}	Address Valid to End of Write	25	—	30	—	35	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Ouput in High Z	—	13	—	15	—	20	ns
t_{DW}	Data to Write Time Overlap	12	—	15	—	15	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	5	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

2713 tbl 10

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

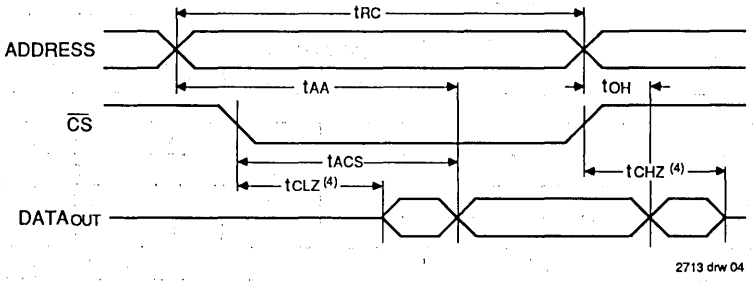
Symbol	Parameters	7M4016S45		7M4016S55		7M4016S70 Mil. Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	70	ns
t_{ACS}	Chip Select Access Time	—	45	—	55	—	70	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	25	—	25	—	30	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Down Time	—	45	—	55	—	70	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	45	—	55	—	70	—	ns
t_{CW}	Chip Selection to End of Write	45	—	55	—	65	—	ns
t_{AW}	Address Valid to End of Write	45	—	55	—	65	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	45	—	55	—	65	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Ouput in High Z	—	25	—	25	—	30	ns
t_{DW}	Data to Write Time Overlap	20	—	30	—	35	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	5	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

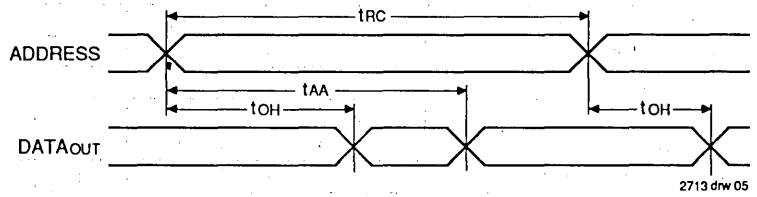
2713 tbl 11

8

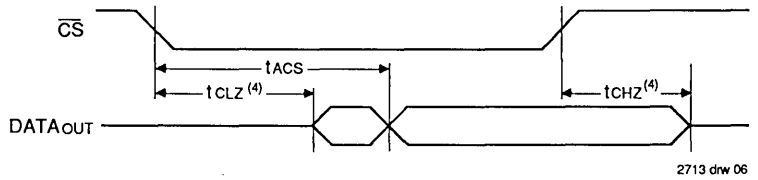
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2)

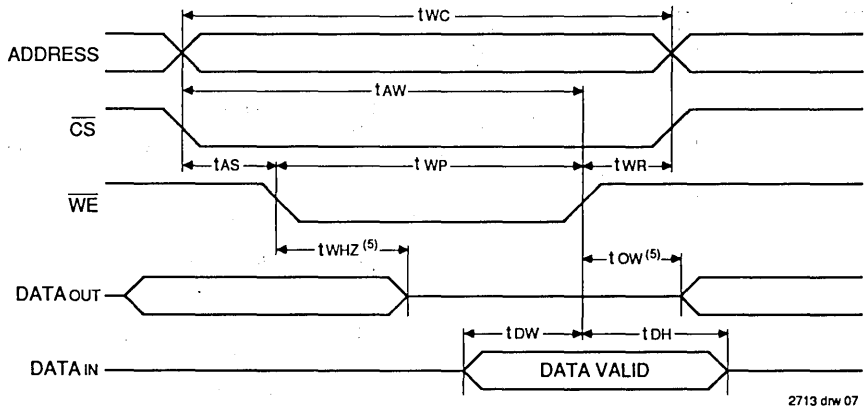


TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3)

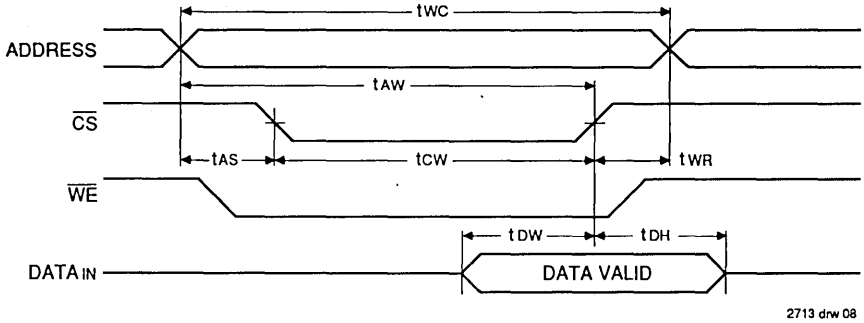


NOTES:
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state with 5pF load (including scope and jig). This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3)



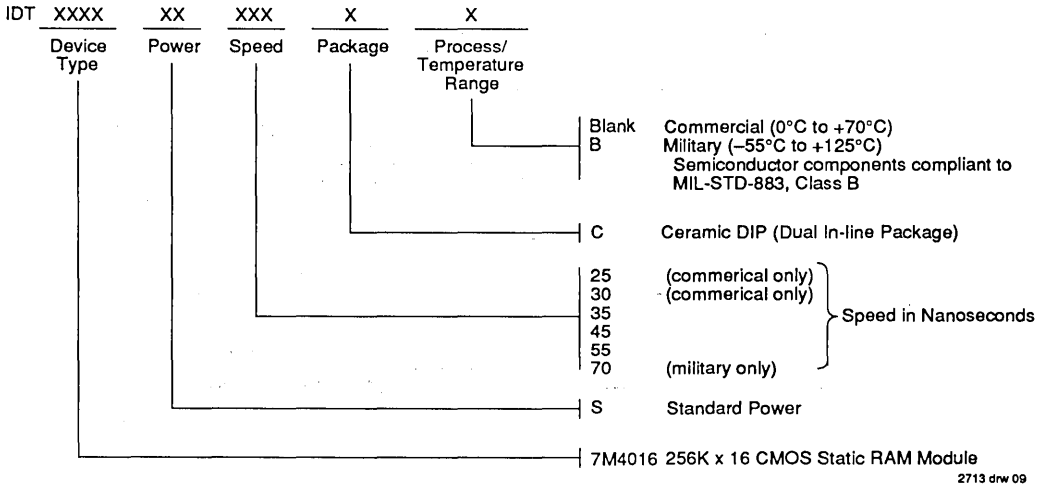
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 4)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going High to the end of write cycle.
4. If the $\overline{CS}$ Low transition occurs simultaneously with or after the $\overline{WE}$ Low transition, the outputs remain in a high impedance state.
5. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design but not tested.

8

ORDERING INFORMATION



Integrated Device Technology, Inc.

512K x 16 CMOS STATIC RAM MODULE

IDT7MP4047

FEATURES:

- High-speed 8 megabit CMOS static RAM module
- Fast access time: 70ns (max.)
- Low power consumption
  - — Active: 220mA max.

  Standard version
  - — CMOS Standby: 16 mA max.

  Very low power version (SCD4600)
  - — CMOS Standby: 800µA max.
  - — Data retention: 400µA max. (Vcc= 2V)
- Surface mounted small outline plastic packages on a 45-pin FR-4 SIP (Single In-line Package)
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible

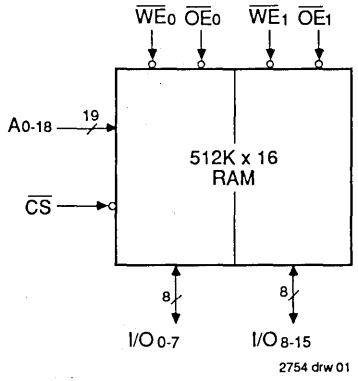
DESCRIPTION:

The IDT7MP4047 is an 512K x 16 CMOS static RAM module constructed on a multilayer epoxy laminate (FR-4) substrate using 8 128K x 8 static RAMs in small outline plastic packages and a one-of-four decoder. Availability of two Write Enables and two Output Enables provides byte access and output control flexibility. The IDT7MP4047 is available with access times as fast as 70ns with a maximum operating current of 220mA. For battery backup applications, a very low data retention current version is available.

The IDT7MP4047 is packaged in a 45-pin FR-4 SIP (Single In-line Package). This results is a package 4.6 inches in length and 0.3 inches in thickness.

All inputs and outputs of the IDT7MP4047 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



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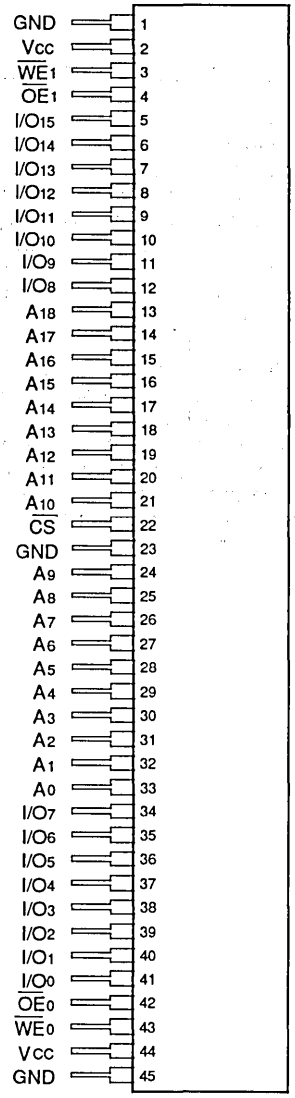
PIN CONFIGURATION[1]



SIP 2754 drw 02
FRONT VIEW

NOTE:
1. For module dimensions, please refer to drawing M41 in the packaging section.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	DATAOUT	Active
Write	L	L	High Z	Active

2754 tbl 02

PIN NAMES

I/O0–I/O15	Data Inputs/Outputs
A0–A18	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$0-1	Write Enables
$\overline{OE}$0-1	Output Enables
Vcc	Power
GND	Ground

2754 tbl 01

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	-55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE: 2754 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE[1] (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	35	pF
CIN(C)	Input Capacitance($\overline{CS}$)	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	35	pF

NOTE: 2754 tbl 04
1. This parameter is guaranteed by design, but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2754 tbl 05
1. VIL = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2754 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	8	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	8	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 2mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -1mA	2.4	—	V
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ = V_{IL}, f = f_{MAX}, Output Open	—	220	mA
I_{SB}	Standby Supply Current (TTL Levels)	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., f = f_{MAX}, Ouput Open	—	24	mA
I_{SB1}(1)	Full Standby Supply Current (CMOS Levels)	$\overline{CS}$ ≥ V_{HC}, V_{IN} ≥ V_{HC} or ≤ V_{LC} V_{CC} = Max., Output Open	—	16	mA

2754 tbl 07

NOTE:

1. For low power version I_{SB1} = 800µA, refer to SCD4600 when ordering.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2754 tbl 08

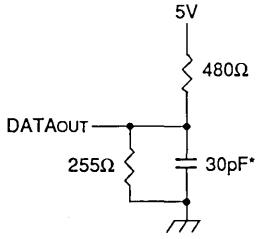


Figure 1. Output Load

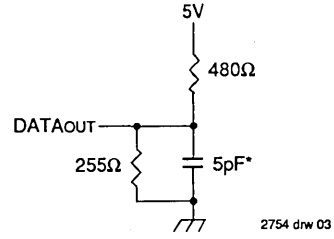


Figure 2. Output Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

*Including scope and jig

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AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameters	7MP4047L70		7MP4047L85		7MP4047L100		7MP4047L120		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	70	—	85	—	100	—	120	—	ns
t_{AA}	Address Access Time	—	70	—	85	—	100	—	120	ns
t_{ACS}	Chip Select Access Time	—	70	—	85	—	100	—	120	ns
t_{OE}	Output Enable to Output Valid	—	45	—	48	—	50	—	60	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	30	—	33	—	35	—	40	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	40	—	43	—	45	—	50	ns
t_{OH}	Output Hold from Address Change	10	—	10	—	10	—	10	—	ns
Write Cycle										
t_{WC}	Write Cycle Time	70	—	85	—	100	—	120	—	ns
t_{WP}	Write Pulse Width	55	—	65	—	75	—	90	—	ns
t_{AS}	Address Set-up Time	0	—	2	—	5	—	5	—	ns
t_{AW}	Address Valid to End of Write	65	—	82	—	90	—	100	—	ns
t_{CW}	Chip Selection to End of Write	65	—	80	—	85	—	100	—	ns
t_{DS}	Data Set-up Time	35	—	38	—	40	—	45	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Ouput in High Z	—	30	—	33	—	35	—	40	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

2754 tbl 09

DATA RETENTION CHARACTERISTICS[1, 4]

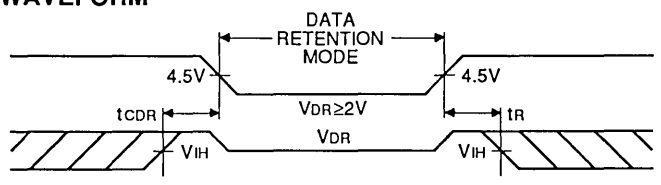
(T_A = 0°C to +70°C)

Symbol	Parameter	Test Condition	Min.	Max. cc @ 2.0V	Unit
V_{DR}	Vcc for Data Retention	—	2.0	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ - 0.2V	—	400	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time	$V_{IN} \leq V_{CC}$ - 0.2V	0	—	ns
t_R[3]	Operation Recovery Time	$V_{IN} \geq$ - 0.2V	t_{RC}[2]	—	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by design, but not tested.
4. This option is only offered when ordering to SCD4600.

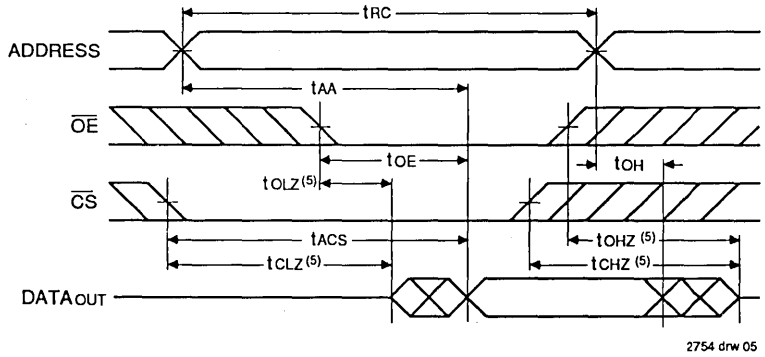
2754 tbl 10

DATA RETENTION WAVEFORM

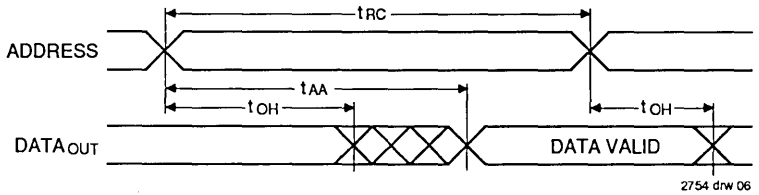


2754 drw 04

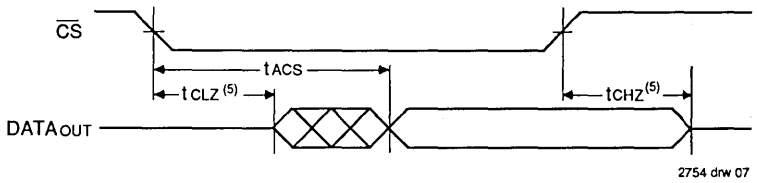
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2, 4]



TIMING WAVEFORM OF READ CYCLE NO. 3[1, 3, 4]



NOTES:
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed, but not tested.

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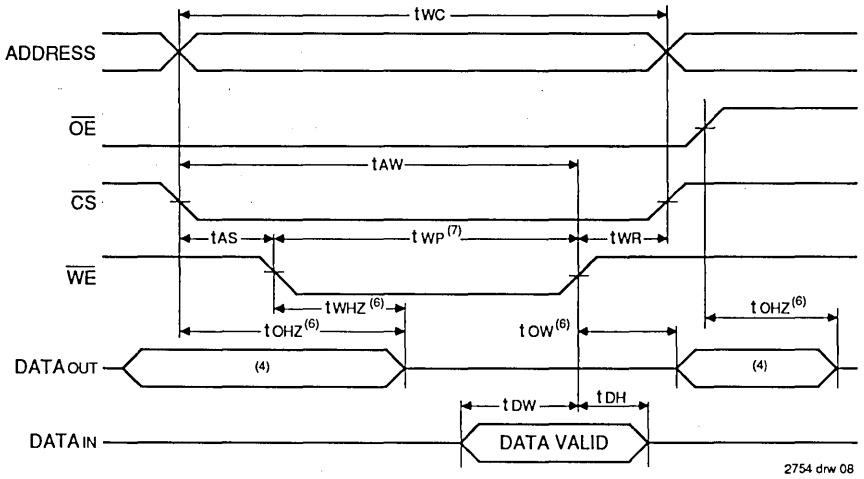
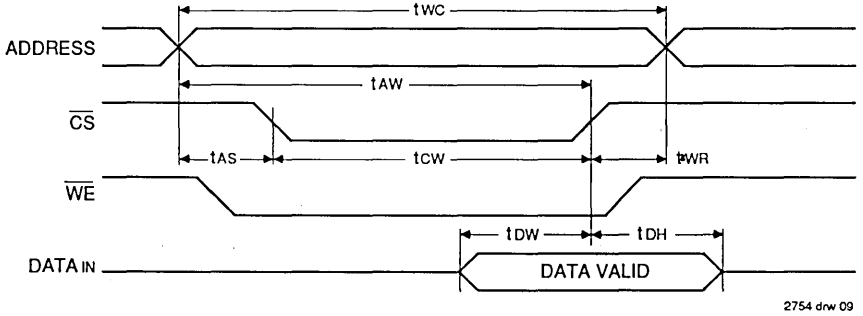
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)

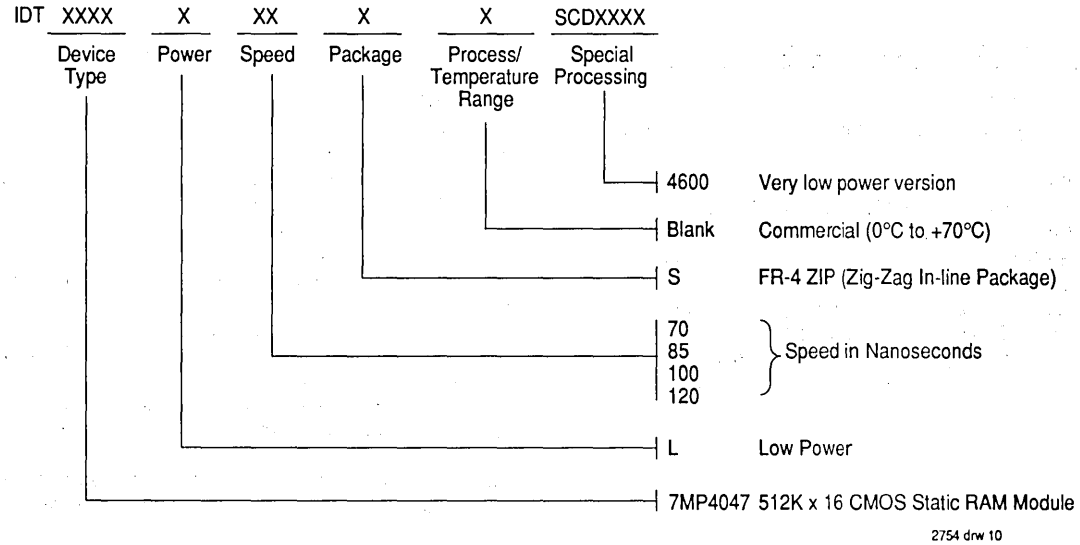


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going High to the end of write cycle.
4. During this period, I/O pins are in the output state and inputs signals must not be applied.
5. If the $\overline{CS}$ Low transition occurs simultaneously with or after the $\overline{WE}$ Low transitions, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).. This parameter is graranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse ((tWP) > tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tWD. If OE is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

ORDERING INFORMATION



8

Integrated Device Technology, Inc.

16K x 32 CMOS STATIC RAM MODULE

IDT7MC4032

FEATURES:

- High density separate I/0, 512K CMOS static RAM module
- Fast access time: 15ns (max.)
- Available in low profile 88-pin sidebraze ceramic dual SIP (Dual Single In-line Package)
- Surface mounted LCC components mounted on a co-fired ceramic substrate
- High impedance outputs during write mode
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL-compatible
- Multiple GND pins for maximum noise immunity

DESCRIPTION:

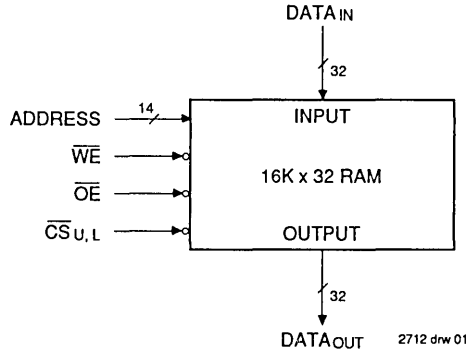
The IDT7MC4032 is a 16K x 32 static RAM module with separate I/0 constructed on a co-fired ceramic substrate using eight IDT71982 16K x 4 static RAMs in leadless chip carriers. Extremely fast speeds can be achieved due to the use of 64K static RAMs Fabricated in IDT's High-performance, high-reliability CEMOS™ technology. The IDT7MC4032 is available with access time as fast as 15ns with minimal power consumption.

The 7MC family of ceramic DSIPs offers the optimum in packing density and profile height. The IDT7MC4032 is packaged in a 88-pin ceramic dual SIP. The dual row configuration allow 88 pins to be placed on a package less than 4.5 inches long and .27 inches wide. At only 520 mils high, this low profile package is ideal for systems with minimum board spacing. Extremely high packing density can also be achieved allowing four IDT7MC4032 modules to be stacked per inch of board space.

All inputs and outputs of the IDT7MC4032 are TTL-compatible and operate from a single 5V power supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

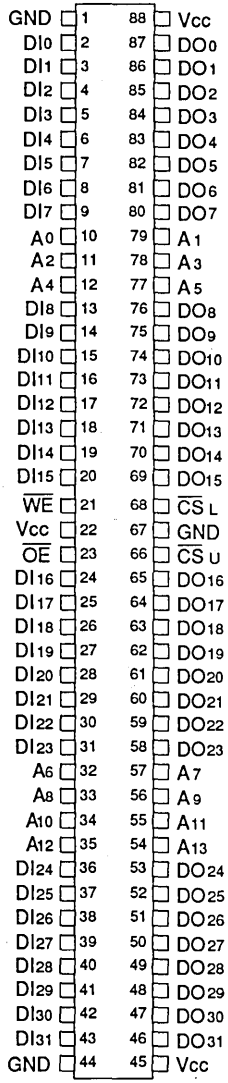
All IDT military module semiconductor components are manufactured on compliance to the latest revision of MIL-STD-883, Class B, making them ideally suited for applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



CMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION[1]



2713 drw 02

DSIP
TOP VIEW

NOTE:
1. For module dimension, please refer to module drawing M43 in the packaging section.

PIN NAMES

A_0–A_{13}	Addresses
DI_0–DI_{31}	Data Input
DO_0–DO_{31}	Data Output
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS}_L$	Chip Select (Lower)
$\overline{CS}_U$	Chip Select (Upper)
Vcc	Power
GND	Ground

2712 tbl 01

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	HighZ	Standby
Read	L	L	H	$DATA_{OUT}$	Active
Write	L	X	L	High Z	Active
Read	L	H	H	High Z	Active

2712 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2712 tbl 03

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	V_{IN} = 0V	15	pF
$C_{IN(A)}$	Input Capacitance (Address and Control)	V_{IN} = 0V	80	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	15	pF

2712 tbl 04

NOTE:
1. This parameter is guaranteed by design, but not tested.

8

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2712 tbl 05

NOTE:
1. V_{IL} = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C + 125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2712 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	80	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	—	V

2712 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameter	Test Conditions	IDT7MC4032 15, 20ns Max.		IDT7MC4032 25ns Max.		IDT7MC4032 30, 40, 50ns Max.		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Current	f = 0, $\overline{CS} \le V_{IL}$, V_{CC} = Max., Output Open	960	—	960	1000	800	800	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS} \le V_{IL}$, f = f_{MAX}, Output Open	1200	—	1200	1200	1000	1120	mA
I_{SB}	Standby Supply Current	$\overline{CS} \ge V_{IH}$, V_{CC} = Max., f = f_{MAX}, Ouputs Open	600	—	480	480	400	440	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS} \ge V_{CC}$ -0.2V, $V_{IN} \ge V_{CC}$ -0.2V or ≤ 0.2V	200	—	160	160	120	160	mA

2712 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2712 tbl 10

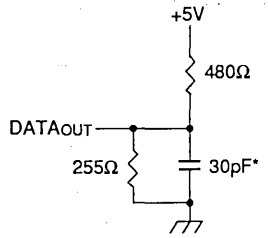
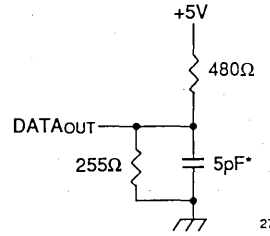


Figure 1. Output Load



2712 drw 03

Figure 2. Output Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameters	7MC4032S15 Com'l Only		7MC4032S20 Com'l Only		7MC4032S25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	15	—	20	—	25	—	ns
t_{AA}	Address Access Time	—	15	—	20	—	25	ns
t_{ACS}	Chip Select Access Time	—	15	—	20	—	25	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	10	—	15	—	15	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	7	—	8	—	10	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	7	—	8	—	15	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Down Time	—	15	—	20	—	25	ns
Write Cycle								
t_{WC}	Write Cycle Time	14	—	17	—	20	—	ns
t_{CW}	Chip Selection to End of Write	14	—	17	—	20	—	ns
t_{AW}	Address Valid to End of Write	14	—	17	—	20	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	14	—	17	—	20	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Ouput in High Z	—	5	—	7	—	7	ns
t_{DW}	Data to Write Time Overlap	8	—	10	—	13	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	5	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

2712 tbl 08

8

AC ELECTRICAL CHARACTERISTICS (Continued)

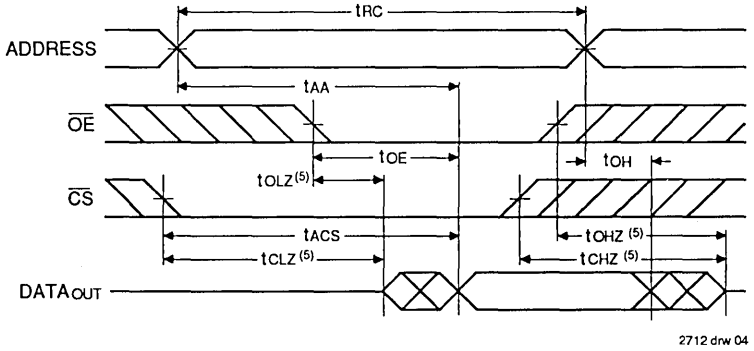
(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameters	7MC4032S30		7MC4032S40		7MC4032S50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	30	—	40	—	50	—	ns
t_{AA}	Address Access Time	—	30	—	40	—	50	ns
t_{ACS}	Chip Select Access Time	—	30	—	40	—	50	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	20	—	22	—	30	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	13	—	17	—	18	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	17	—	17	—	18	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Down Time	—	30	—	40	—	50	ns
Write Cycle								
t_{WC}	Write Cycle Time	25	—	35	—	45	—	ns
t_{CW}	Chip Selection to End of Write	25	—	28	—	38	—	ns
t_{AW}	Address Valid to End of Write	25	—	30	—	40	—	ns
t_{AS}	Address Set-up Time	0	—	2	—	2	—	ns
t_{WP}	Write Pulse Width	25	—	28	—	38	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Ouput in High Z	—	10	—	12	—	17	ns
t_{DW}	Data to Write Time Overlap	15	—	17	—	23	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	5	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

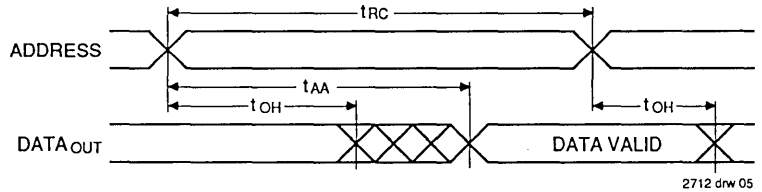
2712 tbl 09

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



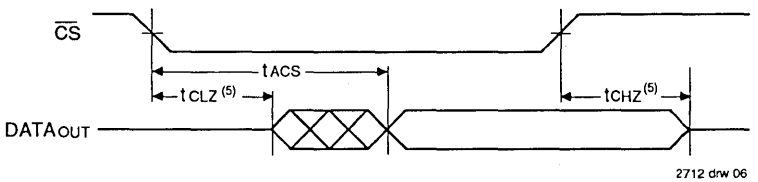
2712 drw 04

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2712 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)

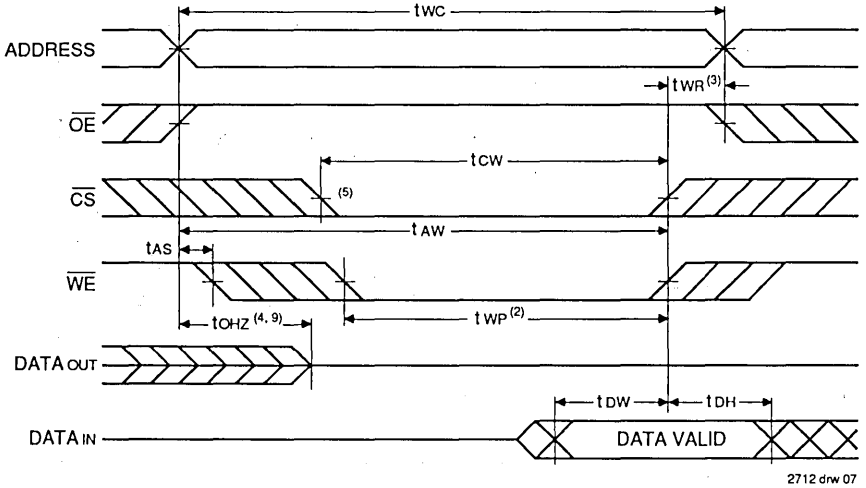


2712 drw 06

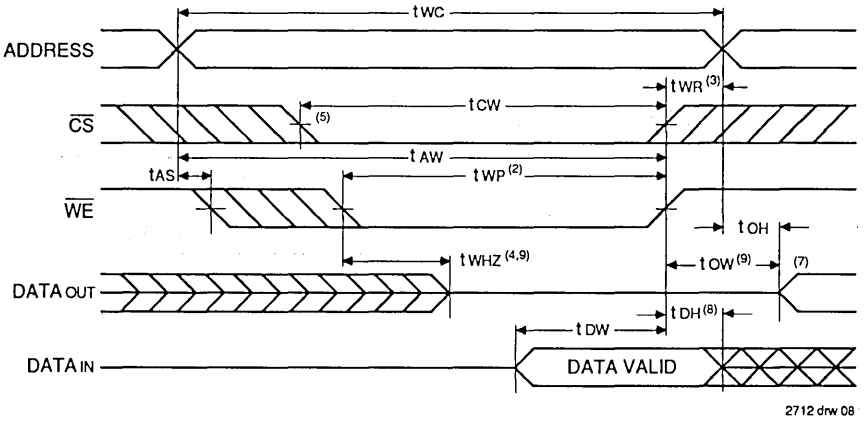
NOTES:
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±500mV from steady state. This parameter is guaranteed by design but not tested.

8

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1)

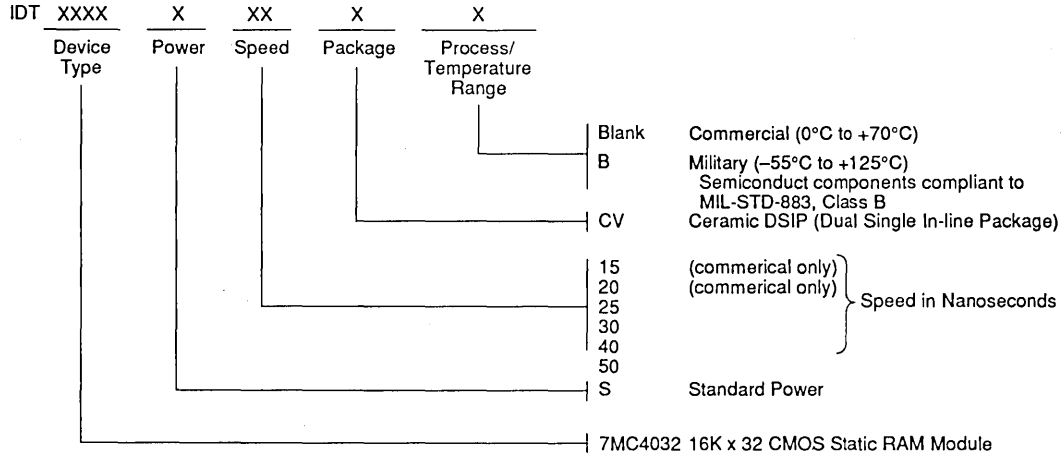


TIMING WAVEFORM OF WRITE CYCLE NO. 2 (CS CONTROLLED TIMING)(1, 6)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going High to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ Low transition occurs simultaneously with or after the $\overline{WE}$ Low transitions or after the $\overline{WE}$ transition, the outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = VIL).
7. DATAOUT is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase must not be applied to them.
9. Transition is measured ±500mV from steady state. This parameter is graranteed by design, but not tested.

ORDERING INFORMATION



2712 drw 09

8

Integrated Device Technology, Inc.

16K x 32 CMOS STATIC RAM MODULE

PRELIMINARY
IDT7MP4031

FEATURES:

- High density 512K CMOS static RAM module
- Low profile 64 pin ZIP (zig-zag in-line vertical package)
- Fast access time: 15ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible
- Multiple GND pins for maximum noise immunity

DESCRIPTION:

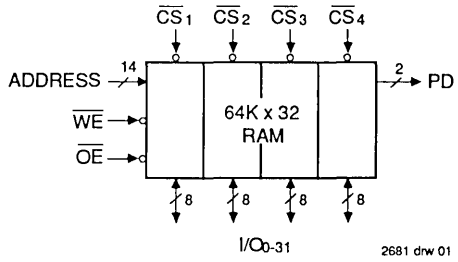
The IDT7MP4031 is a 16K x 32 CMOS static RAM module constructed on an epoxy laminate (FR-4) substrate using 8 16K x 4 static RAMs in plastic SOJ packages. Availability of four chip select lines (one for each group of two RAMs) provides byte access. Extremely fast speeds can be achieved due to the use of 64K static RAMs fabricated in IDT's high performance, high reliability CEMOS™ technology. The IDT7MP4031 is available with access time as fast as 15ns with minimal power consumption.

The IDT7MP family of ZIPs, DSIPs and SIPs offers the optimum in packing density and profile height. The IDT7MP4031 is packaged in a 64 pin (FR-4) ZIP (zig-zag in-line vertical package). The dual row configuration allows 64 pins to be placed on a package 3.65 inches long and 0.35 inches wide. At only 0.50 inches high, this low profile package is ideal for systems with minimum board spacing.

All inputs and outputs of the IDT7MP4031 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation.

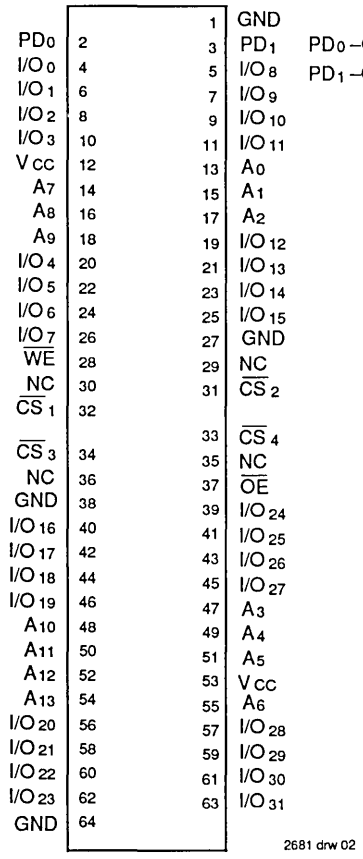
Two identification pins (PD0 and PD1) are provided for applications in which different density versions of the module are used. In this way, the target system can read the respective levels of PD0 and PD1 to determine a 16K depth.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION[1, 2]



2681 drw 02

ZIP TOP VIEW

NOTE:
1. For module dimensions, please refer to module drawig M46 in the packaging section.
2. Pins 2 and 3 (PD0 and PD1) are read by the user to determine the depth of the module. If PD0 reads GND and PD1 reads Open, then the module has 16K depth.

PIN NAMES

I/O0–31	Data Input/Output
A0–13	Address Inputs
$\overline{CS}_{1-4}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
PD0-1	Depth Identification
Vcc	Power
GND	Ground

2681 tbl 01

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	DATAOUT	Active
Write	L	X	L	DATAIN	Active
Read	L	H	H	High-Z	Active

2681 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	–10 to +85	°C
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTES: 2681 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN(D)	Input Capacitance (Data)	V(IN) = 0V	10	pF
CIN(A)	Input Capacitance (Address & Control)	V(IN) = 0V	60	pF
COUT	Output Capacitance	V(OUT) = 0V	10	pF

NOTE: 2681 tbl 04
1. This parameter is guaranteed by design, but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 2681 tbl 05
1. VIL (min) = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commerical	0°C to +70°C	0V	5.0V ± 10%

2681 tbl 06

8

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	40	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	5	µA
I_{LO}	Output Leakage	V_{CC} = Max.; $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V

Symbol	Parameter	Test Conditions	15ns Max.	20ns Max.	25ns Max.	35ns Max.	Unit
I_{CC1}	Operating Current	f = 0; $\overline{CS}$ = V_{IL}, V_{CC} = Max.; Output Open	1080	960	960	800	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max.; $\overline{CS}$ = V_{IL}; f = f_{MAX} Output Open	1440	1200	1200	1000	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max. f = f_{MAX}, Outputs Open	600	480	480	400	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} – 0.2V; f = 0, V_{IN} > V_{CC} – 0.2V or < 0.2V	200	160	160	120	mA

2681 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2681 tbl 08

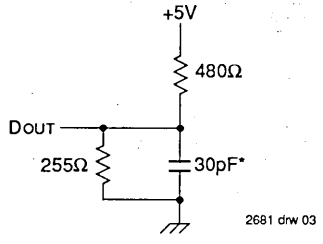


Figure 1. Output Load

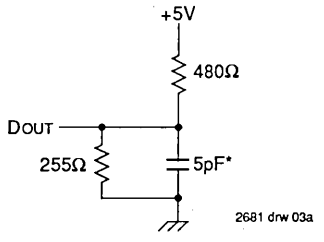


Figure 2. Output Load (for t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ} and t_{OW})

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

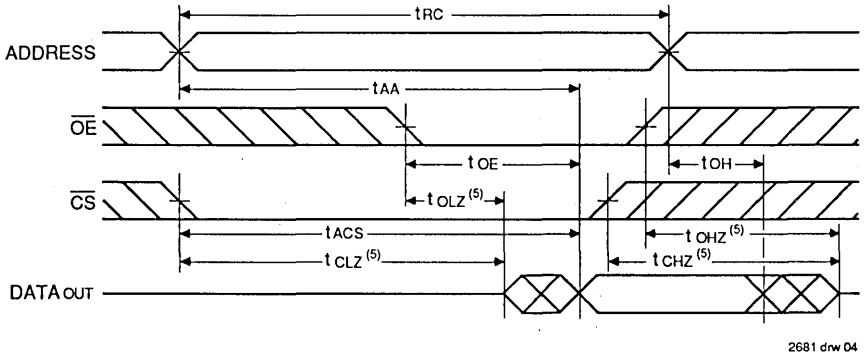
(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP4031S15		7MP4031S20		7MP4031S25		7MP4031S35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	15	—	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	15	—	20	—	25	—	35	ns
t_{ACS}	Chip Select Access Time	—	15	—	20	—	25	—	35	ns
$t_{CLZ1, 2}$[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	9	—	12	—	15	—	20	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	7	—	8	—	10	—	15	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	7	—	8	—	15	—	15	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	15	—	20	—	25	—	35	ns
Write Cycle										
t_{WC}	Write Cycle Time	14	—	17	—	20	—	30	—	ns
t_{CW}	Chip Select to End of Write	14	—	17	—	20	—	25	—	ns
t_{AW}	Address Valid to End of Write	14	—	17	—	20	—	25	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	14	—	17	—	20	—	25	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	6	—	7	—	7	—	10	ns
t_{DW}	Data to Write Time Overlap	10	—	10	—	13	—	15	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	5	—	5	—	ns

NOTE:
1. This parameter is guaranteed, but not tested.

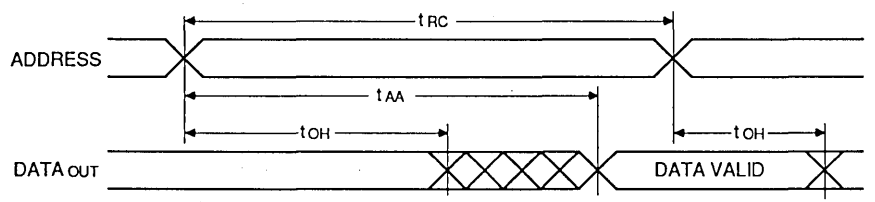
2681 tbl 09

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



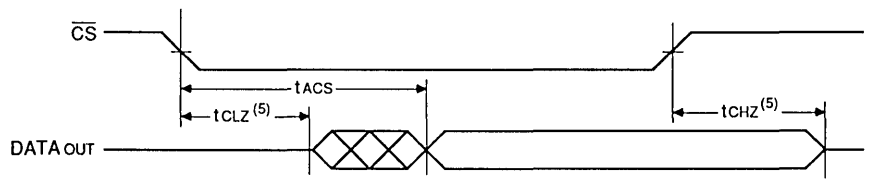
2681 drw 04

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2681 drw 05

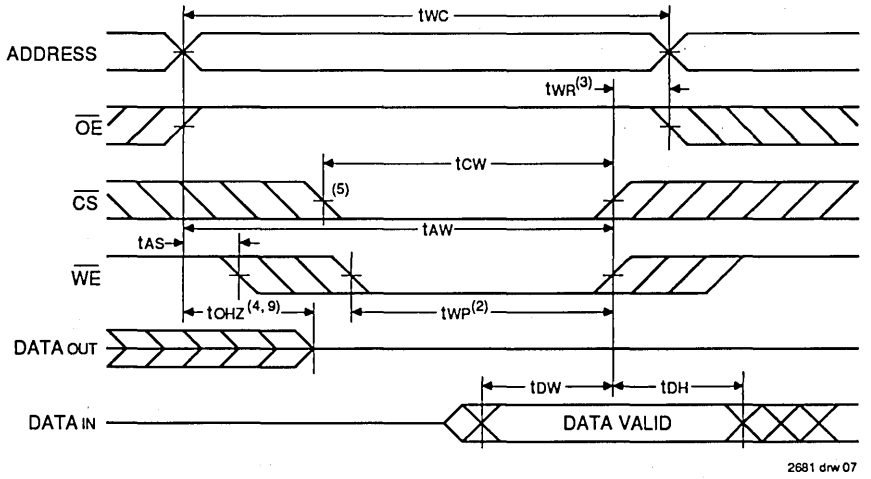
TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)



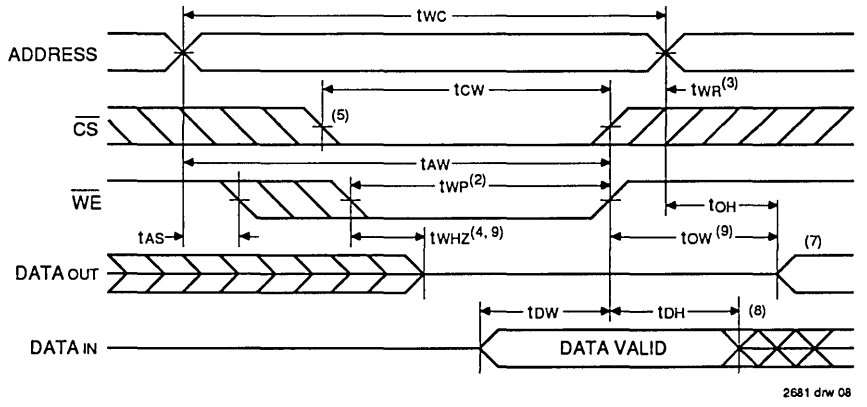
2681 drw 06

NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1)



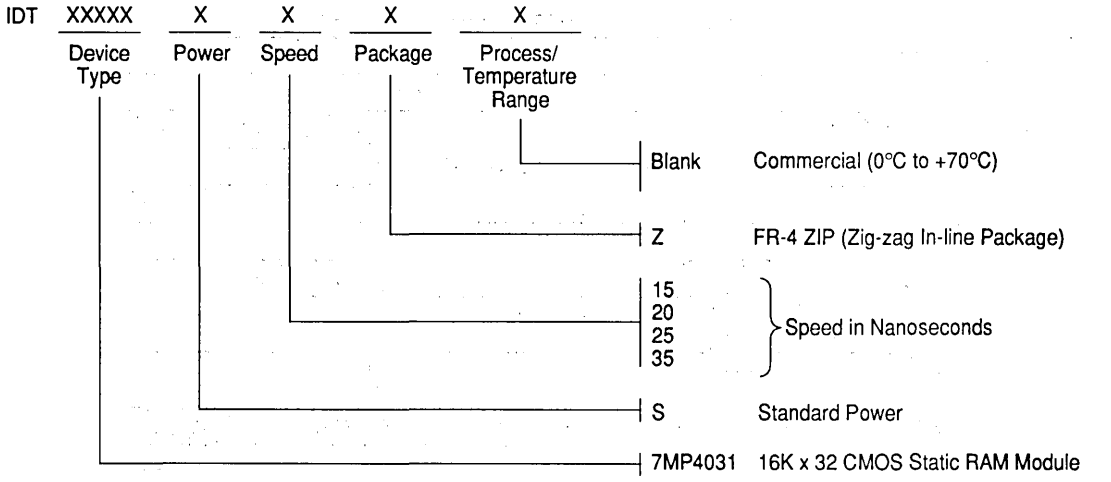
TIMING WAVEFORM OF WRITE CYCLE NO. 2(1, 6)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$.
3. tWP is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedence state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = VIL).
7. DOUT is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

8

ORDERING INFORMATION



2681 drw 09

Integrated Device Technology, Inc.

SUBSYSTEMS "FLEXI-PAK" FAMILY
32K x 32
128K x 32
CMOS STATIC RAM MODULE

PRELIMINARY
IDT7M4003
IDT7M4013

FEATURES:

- High-density 1 megabit/4 megabit CMOS static RAM modules
- Member of the Subsystems "Flexi-Pak" Family of interchangeable modules, with equivalent pin-outs, supporting a wide range of applications
- Footprint compatiblemodule upgrades to the next higher density with relative ease
- Fast access times:
  - 7M4003 - 25ns (max.) commercial
  - 7M4003 - 30ns (max.) military
  - 7M4013 - 35ns (max.) commercial
  - 7M4013 - 45ns (max.) military
- Low power CMOS operation
- Surface mounted LCC components on a multi-layered co-fired ceramic substrate
- Offered in a 66-pin "PGA-type" HIP (Hex In-line Package), occupying only 1 sq. inch of board space
- Single SV (±10%) power supply
- Multiple ground pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

The IDT7M4003/4013 are high-speed, high-density I megabit/4 megabit CMOS static RAM modules constructed on a multi-layer co-fired ceramic subslrate using either 32K x 8 or 128K x 8 SRAM components in leadless chip carriers.

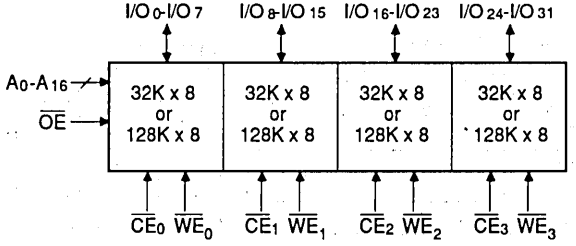
These modules are part of the IDT Subsytems "Flexi-Pak" Family modules. This family of SRAM/EEPROM/EPROM memory modules support applications requiring stand alone static or programmable memory requirements, or those applications needing a combination of both. All three module configurations have equivalent pin-outs, making these "plug-in compatible" (i.e. inter-changeable) modules suitable for a wide range of applications.

The IDT7M4003/4013 is available with access times as fast as 25/35ns over the commercial temperature range and 30/45ns over the military temperature range.

This family of IDT modules are offered in a 66-pin, ceramic HIP (Hex In-line Package). This HIP package is similar to a PGA and allows the designer to fit 1 megabit/4 megabit of memory into 1 sq. inch of board space.

All military IDT modules are assembled with semiconductor components compliant with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

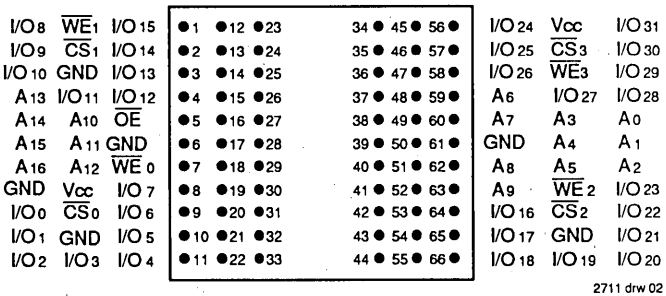
FUNCTIONAL BLOCK DIAGRAM



2711 drw 01

8

PIN CONFIGURATION[1, 2]



2711 drw 02

HIP
TOP VIEW

NOTE:
1. For module dimensions, please refer to drawing M32 in the packaging section.
2. For the IDT7M4003 (32K x 32) version, pins 6 and 7 are no connects.

PIN NAMES

Name	Description
I/O_{0-31}	Data Inputs/Outputs
A_{0-16}	Address Inputs
$\overline{WE}_{0-3}$	Write Enables
$\overline{CS}_{0-3}$	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground

CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
$C_{IN(1)}$	Input Capacitance (DATA, $\overline{CS}$, $\overline{WE}$)	V_{IN} = 0V	50	pF
$C_{IN(2)}$	Input Capacitance (ADDRESS, $\overline{OE}$)	V_{IN} = 0V	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
1. This parameter is guaranteed by design, but not tested.

2711 tbl 03

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	$DATA_{OUT}$	Active
Read	L	H	H	High Z	Active
Write	L	X	L	$DATA_{IN}$	Active

2711 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2711 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2711 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE: 2711 tbl 04

1. V_{IL} = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS

(Vcc = 5.0V ± 10%, TA = -55°C TO +125°C and 0°C TO +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.(1)	Max.(2)	Unit
$\|I_{LI}\|$	Input Leakage Current (Address, $\overline{OE}$)	Vcc = Max., V_{IN} = GND to Vcc	—	5	10	µA
$\|I_{LI}\|$	Input Leakage Current (Data, $\overline{CS}$, $\overline{WE}$)	Vcc = Max., V_{IN} = GND to Vcc	—	20	40	µA
$\|I_{LO}\|$	Output Leakage Current	Vcc = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to Vcc	—	5	10	µA
I_{CC}	Dynamic Operating Current	Vcc = Max., $\overline{CS} \leq V_{IL}$ f = f_{MAX}, Output Open	—	800	880	mA
I_{SB}	Standby Supply Curent	Vcc = Max., $\overline{CS} \geq V_{IH}$ f = f_{MAX}, Output Open	—	80	280	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS} \geq$ Vcc -0.2V V_{IN} > Vcc -0.2V or < 0.2V	—	80	80	mA
V_{OL}	Output Low Voltage	Vcc = Min., I_{OL} = 8mA	—	0.4	0.4	V
V_{OH}	Output High Voltage	Vcc = Min., I_{OH} = -4mA	2.4	—	—	V

NOTE:

1. For TA = 0°C to +70°C versions only.
2. For TA = -55°C to +125°C versions only.

2711 tbl 06

8

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2711 tbl 07

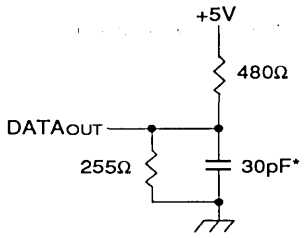


Figure 1. Output Load

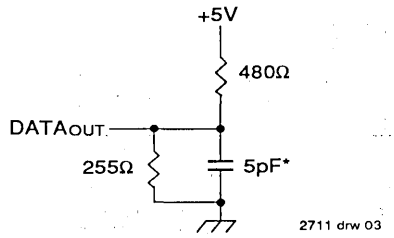


Figure 2. Output Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameters	7M4003S25 (Com'l Only) Min.	7M4003S25 (Com'l Only) Max.	7M4003S30 Min.	7M4003S30 Max.	7M4003S35 7M4013S35 Min.	7M4003S35 7M4013S35 Max.	7M4003S40 7M4013S40 Min.	7M4003S40 7M4013S40 Max.	7M4003S45 7M4013S45 Min.	7M4003S45 7M4013S45 Max.	Unit
READ CYCLE												
t_{RC}	Read Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	—	40	—	45	ns
t_{ACS}	Chip Select Access Time	—	25	—	30	—	35	—	40	—	45	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	12	—	13	—	15	—	20	—	25	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	2	—	2	—	2	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Select to Output in High Z	—	12	—	15	—	17	—	20	—	20	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	12	—	13	—	15	—	20	—	20	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	5	—	5	—	5	—	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_{CW}	Chip Select to End of Write	20	—	25	—	30	—	35	—	40	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	30	—	35	—	40	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	2	—	2	—	ns
t_{WP}	Write Pulse Width	20	—	23	—	25	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Ouput in High Z	—	12	—	13	—	17	—	20	—	20	ns
t_{DW}	Data to Write Time Overlap	13	—	15	—	16	—	16	—	20	—	ns
t_{DH}	Data Hold from Write Time	3	—	3	—	3	—	3	—	5	—	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

2711 tbl 08

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

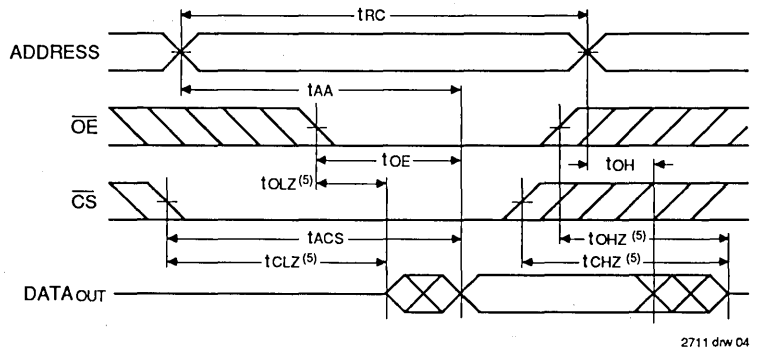
Symbol	Parameters	7M4003S50 7M4013S50		7M4003S60 7M4013S60 (Mil. Only)		7M4003S70 7M4013S70 (Mil. Only)		7M4003S85 7M4013S85 (Mil. Only)		7M4003S100 7M4013S100 (Mil. Only)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	50	—	60	—	70	—	85	—	100	—	ns
t_{AA}	Address Access Time	—	50	—	60	—	70	—	85	—	100	ns
t_{ACS}	Chip Select Access Time	—	50	—	60	—	70	—	85	—	100	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	30	—	30	—	35	—	40	—	45	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Select to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	50	—	60	—	70	—	85	—	100	—	ns
t_{CW}	Chip Select to End of Write	45	—	55	—	65	—	80	—	90	—	ns
t_{AW}	Address Valid to End of Write	45	—	55	—	65	—	80	—	90	—	ns
t_{AS}	Address Set-up Time	2	—	2	—	5	—	5	—	5	—	ns
t_{WP}	Write Pulse Width	40	—	45	—	45	—	50	—	55	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Ouput in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{DW}	Data to Write Time Overlap	25	—	30	—	30	—	35	—	40	—	ns
t_{DH}	Data Hold from Write Time	5	—	5	—	5	—	5	—	5	—	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

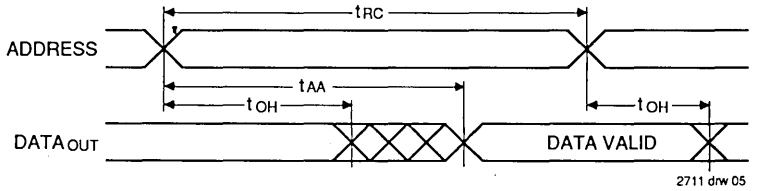
2711 tbl 09

8

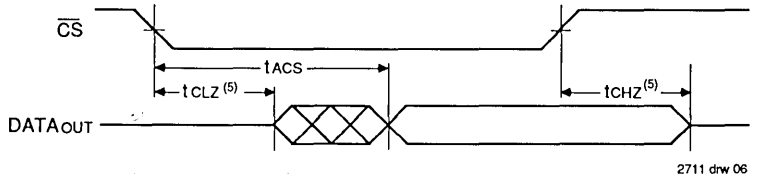
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)

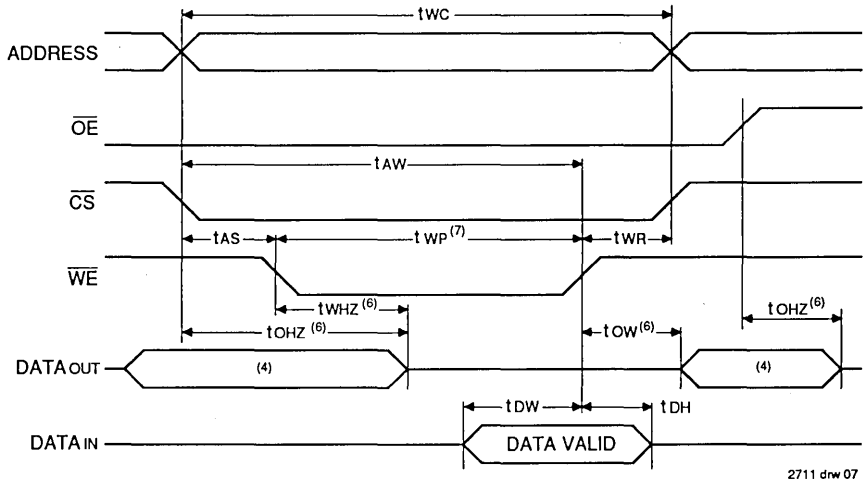


TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)

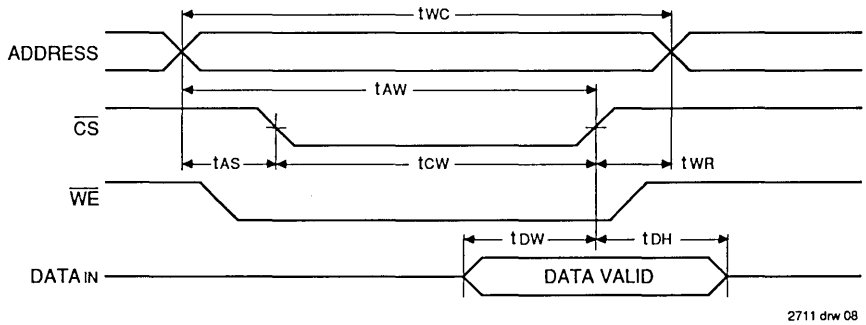


NOTES:
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1, 2, 3, 7)



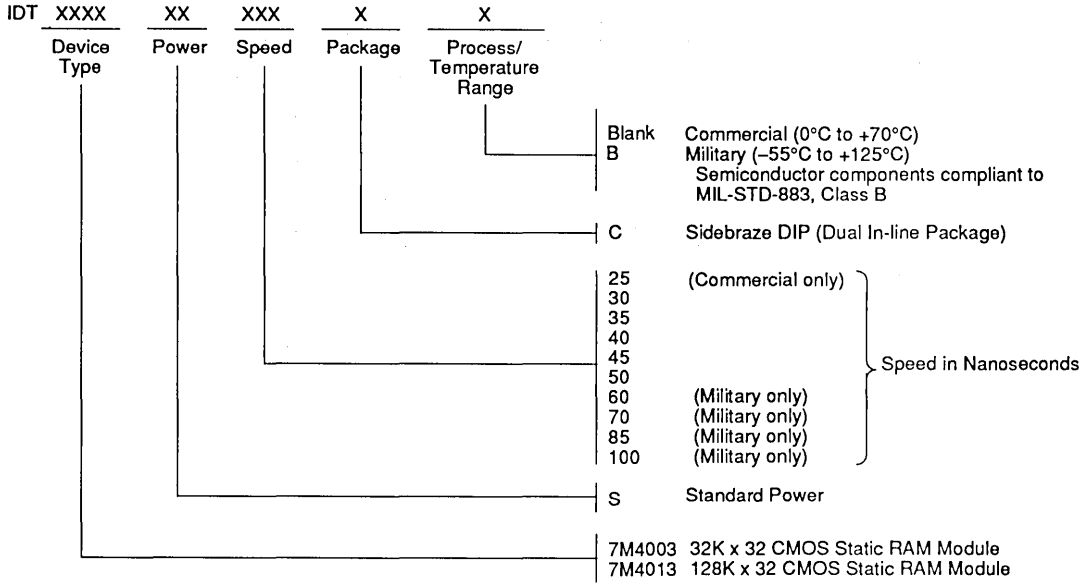
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going High to the end of write cycle.
4. During this period, I/O pins are in the output state, input signals must not be applied.
5. If the $\overline{CS}$ Low transition occurs simultaneously with or after the $\overline{WE}$ Low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse (tWP > tWHZ + tDW) to allow the I/O drivers to turn off data and to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP .

8

ORDERING INFORMATION



2711 drw 10

Integrated Device Technology, Inc.

64K x 32 CMOS STATIC RAM MODULE

IDT7M4017

FEATURES:

- High-density 2 megabit CMOS static RAM module
- Fast access time
  - — Military: 40ns (max.)
  - — Commercial: 30ns (max.)
- Individual byte selects
- Upper and lower word write enables
- Available in 60-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7M4017 is a (64K x 32) high-speed CMOS static RAM module constructed on a co-fired ceramic substrate using eight 32K x 8 static RAMs in leadless chip carriers. On-board decoders use A_{15} to select the upper or lower bank of RAMs. Four chip selects control individual byte selection. Extremely fast speeds can be achieved due to use of 256K static RAMs and the decoder fabricated in IDT's high-performance, high-reliability CEMOS™ technology.

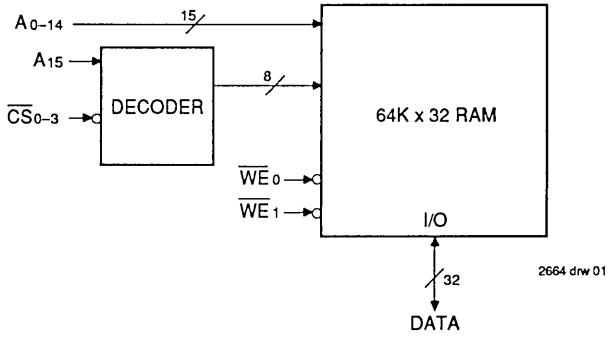
The IDT7M4017 is offered in a 60-pin, 600 mil center sidebraze DIP which enables two megabits of memory to be placed in less than 1.9 square inches of board space.

The IDT7M4017 is available with fast access times over the commercial and military temperature ranges, with minimal power consumption. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to a substantially lower power mode.

All inputs and outputs of the IDT7M4017 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

All IDT military module semiconductor components are manufactured in compliance with MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

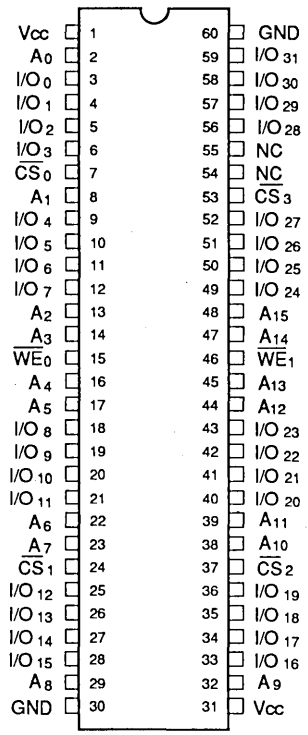
FUNCTIONAL BLOCK DIAGRAM



8

CEMOS is a trademark of Integrated Device Technology Inc.

PIN CONFIGURATION[1]



2664 drw 02

DIP
TOP VIEW

NOTE:
1. For module dimensions, please refer to module drawing M16 in the packaging section.

PIN NAMES

A_0-A_{15}	Addresses
I/O_{0-31}	Data Inputs/Outputs
$\overline{CS_0}$	Chip Select for I/O_{0-7}
$\overline{CS_1}$	Chip Select for I/O_{8-15}
$\overline{CS_2}$	Chip Select for I/O_{16-23}
$\overline{CS_3}$	Chip Select for I/O_{24-31}
$\overline{WE_0}$	Write Enable for I/O_{0-15}
$\overline{WE_1}$	Write Enable for I/O_{16-31}
GND	Ground
Vcc	Power

2664 tbl 01

TRUTH TABLE

Mode	$\overline{CSx}$	$\overline{WEx}$	Output	Power
Standby	L	X	X	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	D_{IN}	Active

2664 tbl 09

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to + 7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	° C
T_{BIAS}	Temperature Under Bias	-10 to +85	-65 to +135	° C
T_{STG}	Storage Temperature	-55 to + 125	-65 to +150	° C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2664 tbl 02
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = + 25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	V_{IN} = 0V	30	pF
$C_{IN(A)}$	Input Capacitance (Address and Control)	V_{IN} = 0V	100	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2664 tbl 10
1. This parameter is guaranteed by design, but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	-	0.8	V

NOTE: 2664 tbl 03
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55° C to + 125° C	0V	5.0V ± 10%
Commercial	0° C to + 70° C	0V	5.0V ± 10%

2664 tbl 04

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address & Control)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	20	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	—	V

2664 tbl 05

Symbol	Parameter	Test Conditions	Commercial Max.	Military Max.	Unit
I_{CC}(1)	Dynamic Operating Current	V_{CC} = Max; $\overline{CS}$ ≤ V_{IL}; f = f_{MAX} Output Open	750	790	mA
I_{SB}	Standby Supply Current (TTL Level)	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open	180	180	mA
I_{SB1}	Full Standby Supply Current (CMOS Levels)	$\overline{CS}$ ≥ V_{CC} – 0.2V V_{IN} ≥ V_{CC} – 0.2V or ≤ 0.2V	135	175	mA

NOTE: 2664 tbl 06
1. For t_{AA} = 30, 35ns versions, I_{CC} = 900 mA.

8

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2664 tbl 07

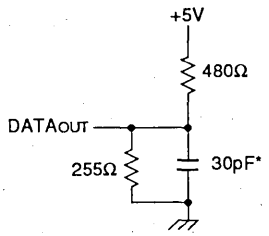
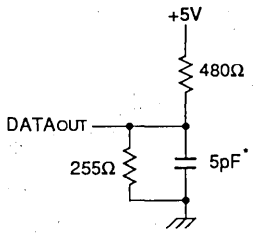


Figure 1. Output Load



2664 drw 03

Figure 2. Output Load (for tCLZ, tCHZ, tOW, tWHZ)

* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

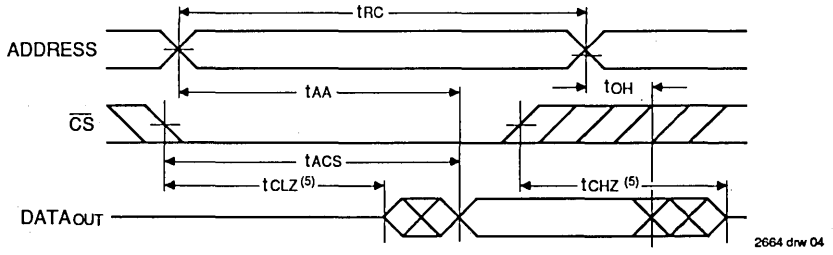
(VCC = 5V ± 10%, TA = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameter	7M4017S30		7M4017S35		7M4017S40		7M4017S45		7M4017S50		7M4017S60		7M4017S70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle																
tRC	Read Cycle Time	30	—	35	—	40	—	45	—	50		60	—	70	—	ns
tAA	Address Access Time	—	30	—	35	—	40	—	45	—	50	—	60	—	70	ns
tACS	Chip Select Access Time	—	30	—	35	—	40	—	45	—	50	—	60	—	70	ns
tCLZ(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	5	—	5	—	ns
tCHZ(1)	Chip Deselect to Output in High Z	—	15	—	17	—	20	—	20	—	20	—	25	—	25	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	5	—	ns
tPU(1)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
tPD(1)	Chip Deselect to Power Down Time	—	30	—	35	—	40	—	45	—	50	—	60	—	70	ns
Write Cycle																
tWC	Write Cycle Time	30	—	35	—	40	—	45	—	50	—	60	—	70	—	ns
tCW	Chip Select to End of Write	25	—	30	—	35	—	40	—	45	—	55	—	60	—	ns
tAW	Address Valid to End of Write	27	—	30	—	35	—	40	—	45	—	55	—	60	—	ns
tAS	Address Set-up Time	2	—	5	—	5	—	5	—	10	—	10	—	10	—	ns
tWP	Write Pulse Width	20	—	25	—	30	—	35	—	35	—	45	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWHZ(1)	Write Enable to Output in High Z	—	12	—	13	—	15	—	20	—	20	—	25	—	30	ns
tDW	Data to Write Time Overlap	13	—	14	—	15	—	20	—	20	—	25	—	30	—	ns
tDH	Data Hold from Write Time	3	—	3	—	3	—	3	—	3	—	3	—	3	—	ns
tOW(1)	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	5	—	5	—	ns

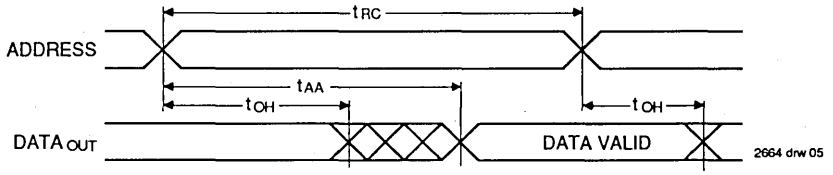
NOTE:
1. This parameter is guaranteed by design, but not tested.

2664 tbl 08

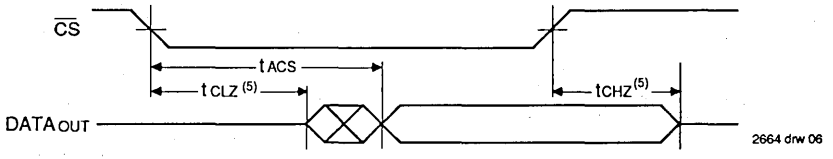
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2, 4]



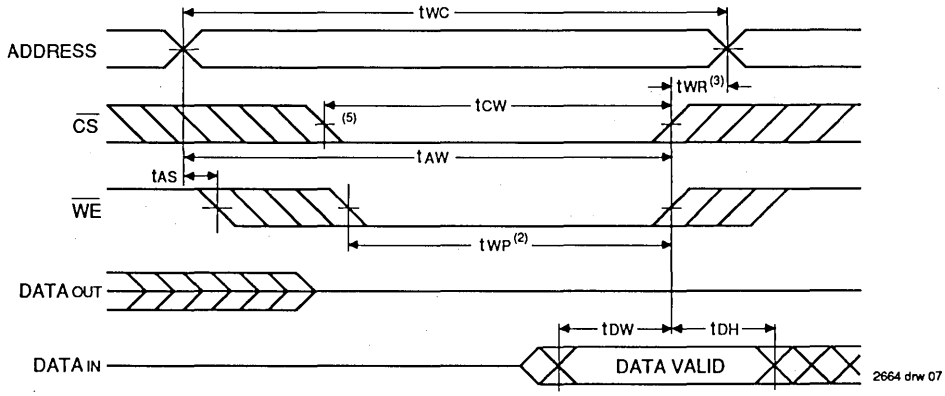
TIMING WAVEFORM OF READ CYCLE NO. 3[1, 3, 4]



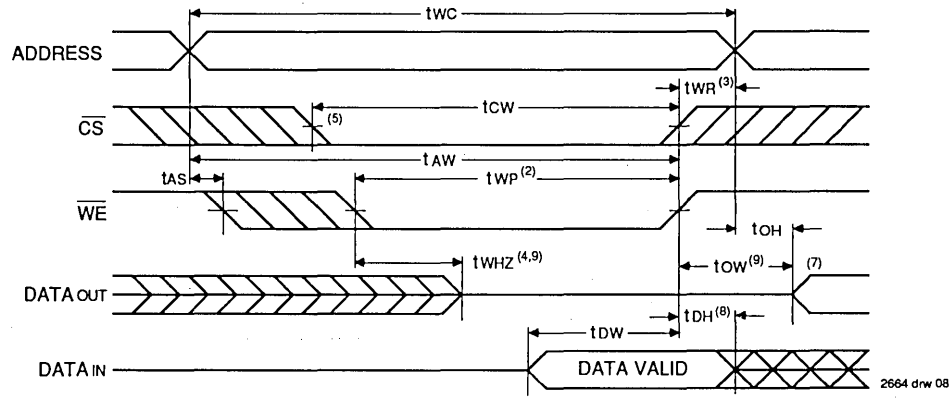
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±500mV from steady state. This parameter is guaranteed by design, but not tested.

8

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1)

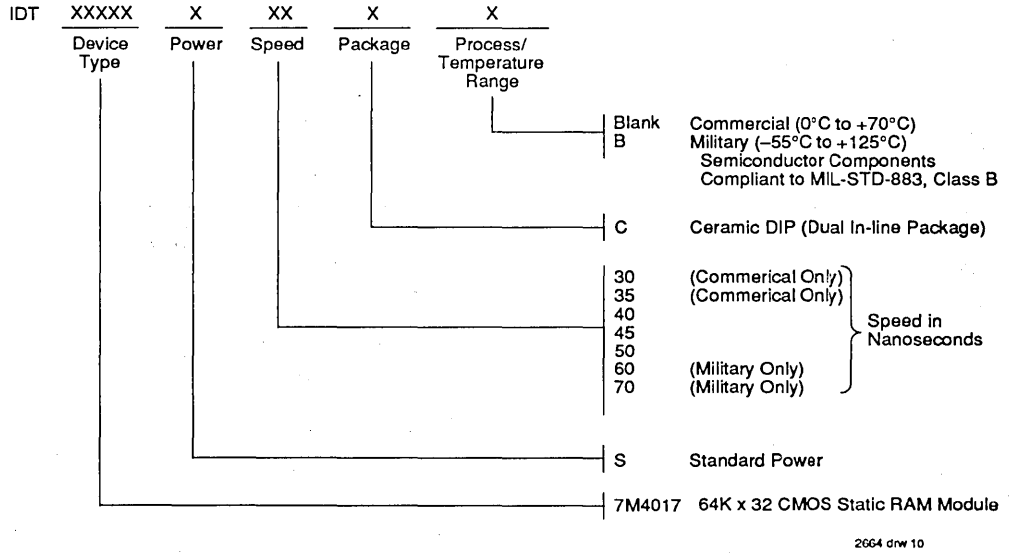


TIMING WAVEFORM OF WRITE CYCLE NO. 2(1, 6)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the CS low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = VIL).
7. DATAOUT is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±500mV from steady state. This parameter is guaranteed by design, but not tested.

ORDERING INFORMATION



8

Integrated Device Technology, Inc.

64K x 32 CMOS STATIC RAM MODULE

PRELIMINARY
IDT7MP4036

FEATURES:

- High density 2 Megabit CMOS static RAM module
- Low profile 64 pin ZIP (Zig-zag In-line vertical Package) or a 64-pin SIMM (Single In-line Memory Module)
- Fast access time: 20ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible
- Multiple GND pins for maximum noise immunity

DESCRIPTION:

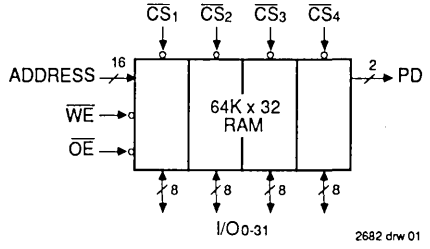
The IDT7MP4036 is a 64K x 32 CMOS static RAM module constructed on an epoxy laminate (FR-4) substrate using 8 64K x 4 static RAMs in plastic SOJ packages. Availability of four chip select lines (one for each group of two RAMs) provides byte access. Extremely fast speeds can be achieved due to the use of 256K static RAMs fabricated in IDT's high performance, high reliability CEMOS™ technology. The IDT7MP4036 is available with access time as fast as 20ns with minimal power consumption.

The IDT7MP family of ZIPs, DSIPs and SIPs offers the optimum in packing density and profile height. The IDT7MP4036 is packaged in a 64 pin (FR-4) ZIP (Zig-zag In-line vertical Package). The dual row configuration allows 64 pins to be placed on a package 3.65 inches long and 0.35 inches wide. At only 0.50 inches high, this low profile package is ideal for systems with minimum board spacing.

All inputs and outputs of the IDT7MP4036 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation.

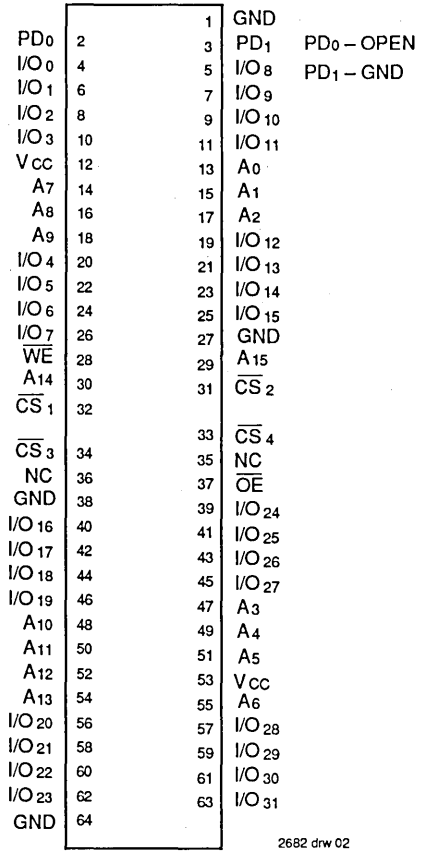
Two identification pins (PD0 and PD1) are provided for applications in which different density versions of the module are used. In this way, the target system can read the respective levels of PD0 and PD1 to determine a 64K depth.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION[1, 2]



2682 drw 02

ZIP TOP VIEW

NOTE:
1. For module dimensions, please refer to module drawing M46 and M48 in the packaging section.
2. Pins 2 and 3 (PD0 and PD1) are read by the user to determine the density of the module. If PD0 reads Open and PD1 read GND, then the module had a 64K depth.

PIN NAMES

I/O0–31	Data Inputs/Outputs
A0–15	Addresses
$\overline{CS}$1–4	Chip Selects
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
PD0–1	Depth Identification
Vcc	Power
GND	Ground
NC	No Connect

2682 tbl 01

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	DATAOUT	Active
Write	L	X	L	DATAIN	Active
Read	L	H	H	High-Z	Active

2682 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	–10 to +85	°C
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTES: 2682 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN(D)	Input Capacitance (Data)	V(IN) = 0V	10	pF
CIN(A)	Input Capacitance (Address & Control)	V(IN) = 0V	60	pF
COUT	Output Capacitance	V(OUT) = 0V	10	pF

NOTE: 2682 tbl 04
1. This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 2682 tbl 05
1. VIL (min) = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commerical	0°C to +70°C	0V	5.0V ± 10%

2682 tbl 06

8

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	80	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max.; $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V

Symbol	Parameter	Test Conditions	20, 25ns Max.	30, 35ns Max.	Unit
I_{CC}	Dymanic Operating Current	f = f_{MAX}; $\overline{CS}$ = V_{IL} V_{CC} = Max.; Output Open	1280	1250	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max. Outputs Open, f = f_{MAX}	280	280	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} – 0.2V; F = 0 V_{IN} > V_{CC} – 0.2V or < 0.2V	240	240	mA

2682 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2682 tbl 08

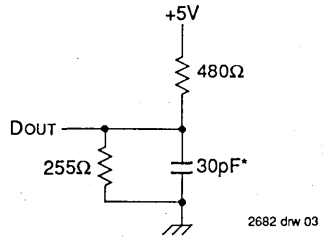


Figure 1. Output Load

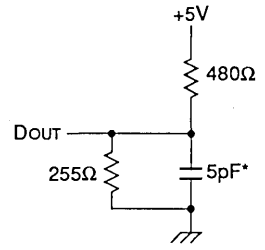


Figure 2. Output Load
(for t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ}, and t_{OW})

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

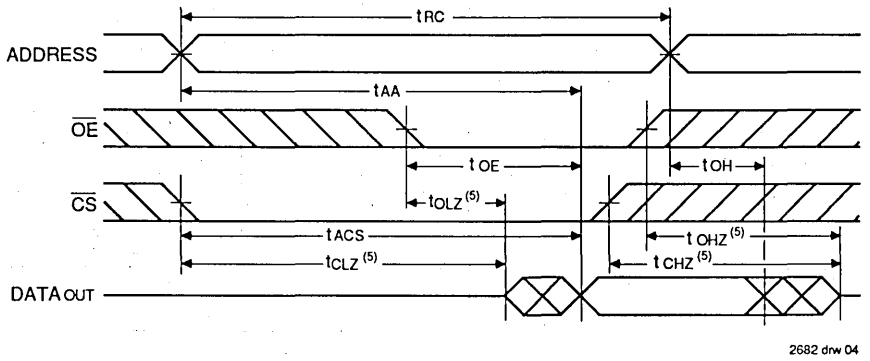
Symbol	Parameter	7MP4036S20		7MP4036S25		7MP4036S30		7MP4036S35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	20	—	25	—	30	—	35	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	30	—	35	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	—	30	—	35	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	10	—	12	—	15	—	25	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	15	—	15	—	20	—	22	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	12	—	15	—	20	—	22	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	20	—	25	—	30	—	35	ns
Write Cycle										
t_{WC}	Write Cycle Time	20	—	25	—	30	—	35	—	ns
t_{CW}	Chip Select to End of Write	15	—	20	—	25	—	30	—	ns
t_{AW}	Address Valid to End of Write	15	—	20	—	25	—	32	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	2	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	25	—	30	—	ns
t_{WR}	Write Recovery Time	3	—	3	—	3	—	3	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	12	—	15	—	15	—	18	ns
t_{DW}	Data to Write Time Overlap	12	—	15	—	17	—	20	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

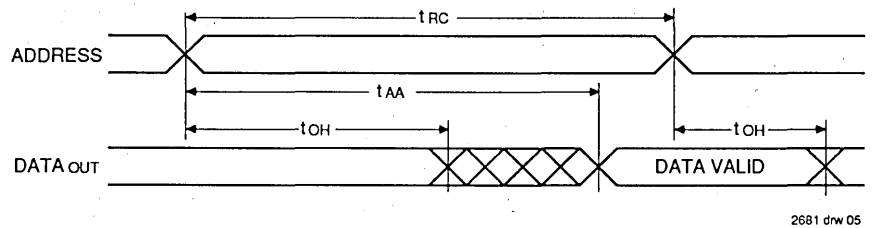
2682 tbl 09

8

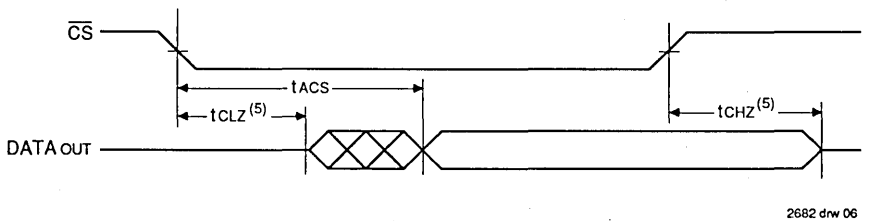
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)

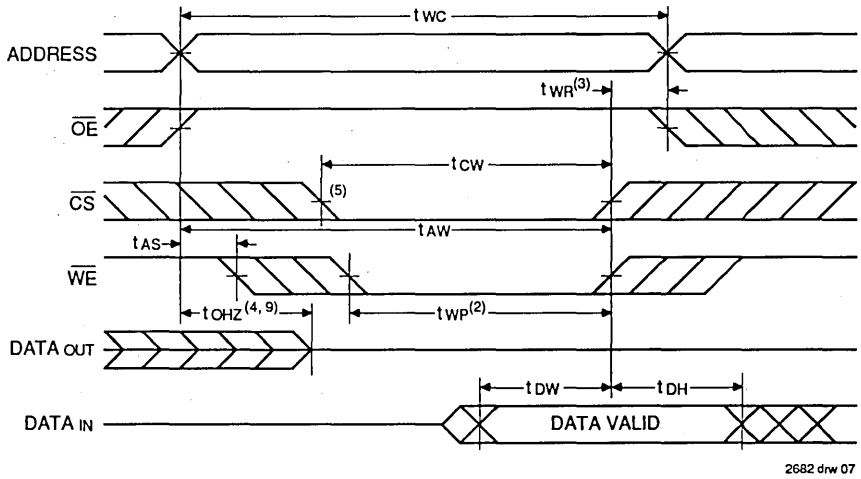


TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



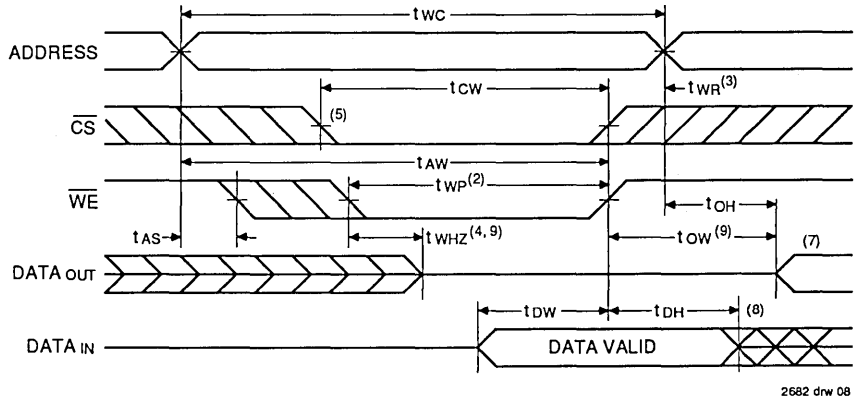
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1)



2682 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 2(1, 6)

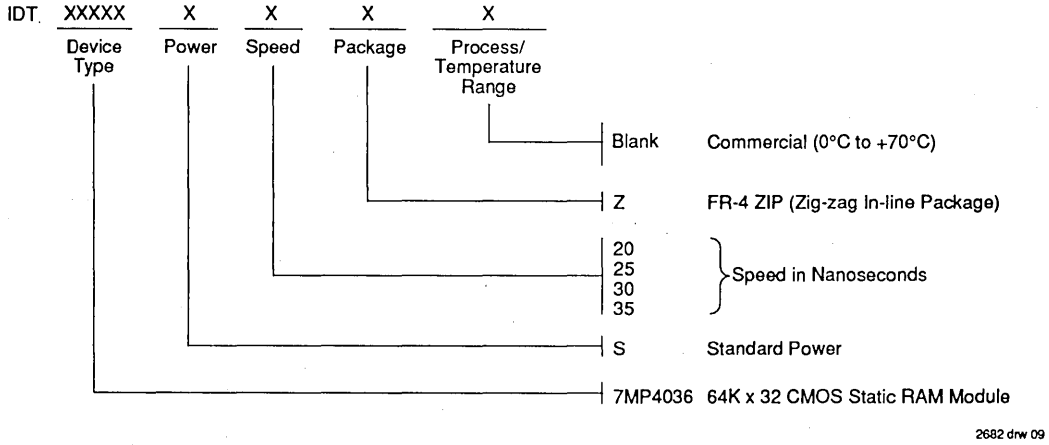


2682 drw 08

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$.
3. tWP is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedence state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = VIL).
7. DOUT is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

8

ORDERING INFORMATION



2682 drw 09

Integrated Device Technology, Inc.

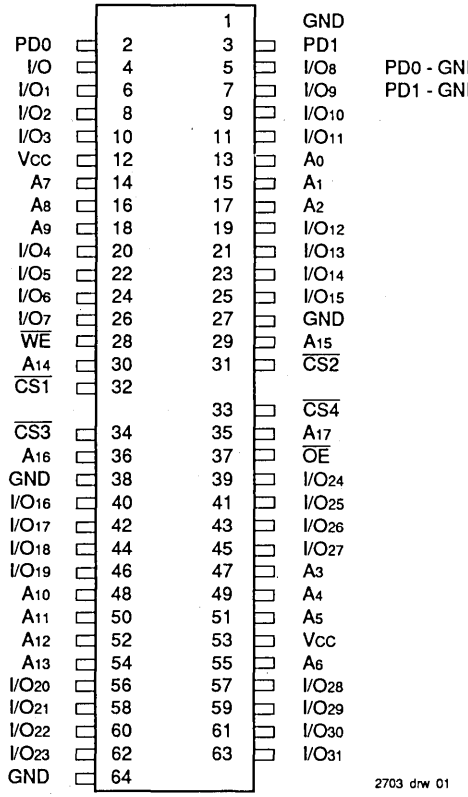
256K X 32 CMOS STATIC RAM MODULE

PRELIMINARY
IDT7MP4045

FEATURES:

- High-density 8 megabit (256K x 32) static RAM module
- Low profile 64-pin FR-4 ZIP (Zig-zag In-line Package) or 64-pin FR-4 SIMM (Single In-line Memory Module)
- Fast access time: 25ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible
- Multiple GND pins for maximum noise immunity

PIN CONFIGURATION (1, 2)



2703 drw 01

ZIP
TOP VIEW

NOTES:
1. For module dimensions, please refer to drawing M47 and M49 in the packaging section.
2. Pins 2 and 3 (PD0 and PD1) are read by the user to determine the depth of the module. If both read GND, then the module has a 256K depth.

DESCRIPTION:

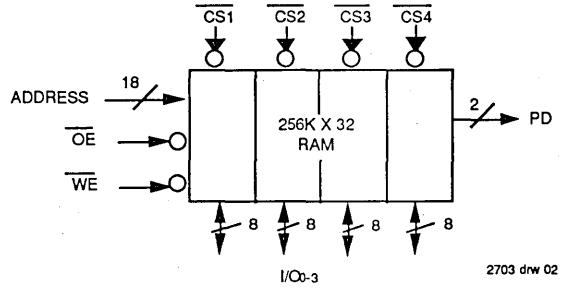
The IDT7MP4045 is a 8 megabit (256K x 32) static RAM module constructed on an epoxy laminate (FR-4) substrate using 8 256K X 4 static RAMs in plastic SOJ packages. Availability of four chip select lines (one for each group of two RAMs) provides byte access. The IDT7MP4045 is available with access time as fast as 25ns with minimal power consumption.

The IDT7MP family of ZIPs, DSIPs, and SIPs offers the optimum in packaging density and profile height. The IDT7MP4045 is packaged in a 64 pin FR4ZIP (zig-zag in-line vertical package) or a 64 lead SIMM (single in-line memory module). The dual row configuration allows 64 pins to be placed on a package 3.65 inches long and 0.35 inches wide. At only 0.575 inches high, this low profile package is ideal for systems with minimum board spacing.

All inputs and outputs of the IDT7MP4045 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

Two identification pins (PD0 and PD1) are provided for applications in which different density versions of the module are used. In this way, the target system can read the respective levels of PD0 and PD1 to determine a 256K depth.

FUNCTIONAL BLOCK DIAGRAM



2703 drw 02

PIN NAMES

I/O0-31	Data Inputs/Outputs
A0-17	Address
$\overline{CS}$1-4	Chip Selects
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
PD0-1	Depth Identification
Vcc	Power
GND	Ground

8

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Comm.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperture	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

2703 tbl 02

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

2703 tbl 03

NOTE:

1. V_{IL} = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2703 tbl 04

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5.0V ± 10%, T_A = 0°C to +70°C)

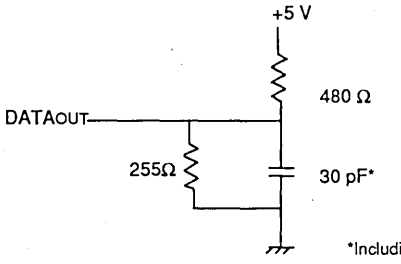
Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage (Address & Control)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	20	µA
I_{LI}	Input Leakage (Data)	V_{CC} = Max. V_{IN}= GND to V_{CC}	—	20	µA
I_{LO}	Output Leakage	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	2	µA
V_{OL}	Output Low Voltage	V_{CC} = Min. I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min. I_{OH} = 4mA	2.4	—	V
I_{CC}	Dynamic Operating Current	$\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = O	—	960	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max. Outputs Open, f = fMAX	—	480	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} - 0.2V V_{IN} > V_{CC} - 0.2V or < 0.2V, f = 0	—	16	mA

2703 tbl 05

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2703 tbl 06



*Including scope and jig.

Figure 1. Output Load

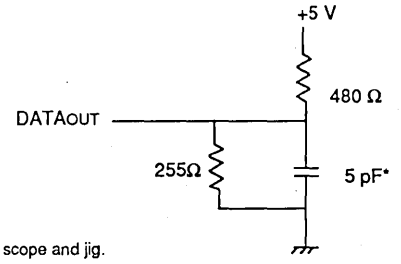


Figure 2 Output Load
(for tOLZ, tOHZ, tCHZ, tCLZ, tWHZ, tOW)

2703 drw 03

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

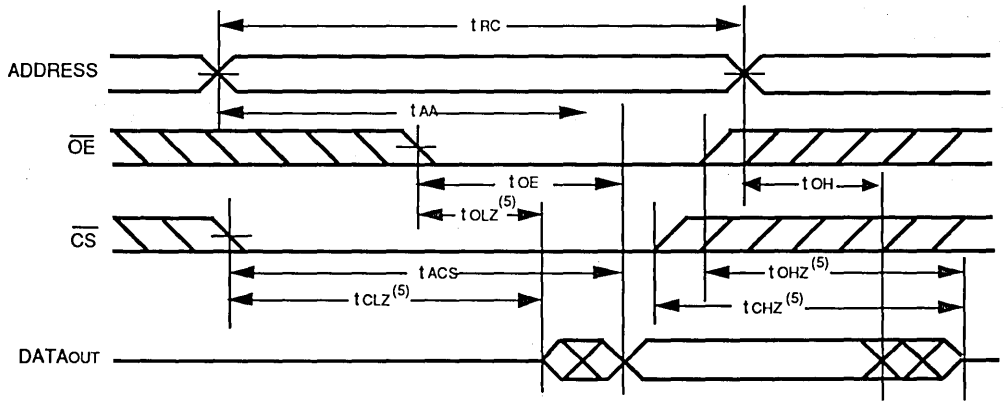
Symbol	Parameter	7MP4045S25 Min.	7MP4045S25 Max.	7MP4045S30 Min.	7MP4045S30 Max.	7MP4045S35 Min.	7MP4045S35 Max.	7MP4045S45 Min.	7MP4045S45 Max.	7MP4045S55 Min.	7MP4045S55 Max.	Unit
Read Cycle												
t_{RC}	Read Cycle Time	25	—	30	—	35	—	45	—	55	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	—	45	—	55	ns
t_{ACS}	Chip Select Access Time	—	25	—	30	—	35	—	45	—	55	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	10	—	10	—	10	—	10	—	10	—	ns
t_{OE}	Output Enable to Output Valid	—	12	—	12	—	18	—	23	—	25	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	0	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	5	—	5	—	10	—	15	—	20	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	5	—	5	—	10	—	15	—	20	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Down Time	—	30	—	30	—	30	—	30	—	30	ns
Write Cycle												
t_{WC}	Write Cycle Time	25	—	30	—	35	—	45	—	55	—	ns
t_{CW}	Chip Selection to End of Write	20	—	25	—	30	—	40	—	50	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	30	—	40	—	50	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	2	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	30	—	35	—	45	—	ns
t_{WR}	Write Recovery Time	3	—	3	—	3	—	3	—	3	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	0	5	0	7	0	10	0	15	0	15	ns
t_{DW}	Data to Write Time Overlap	10	—	15	—	20	—	25	—	35	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns

NOTES:
1. This parameter is guaranteed by design but not tested.
2. Preliminary specifications only.

2703 tbl 07

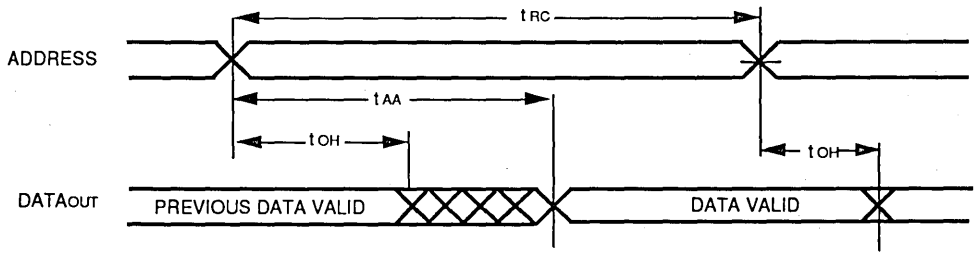
8

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



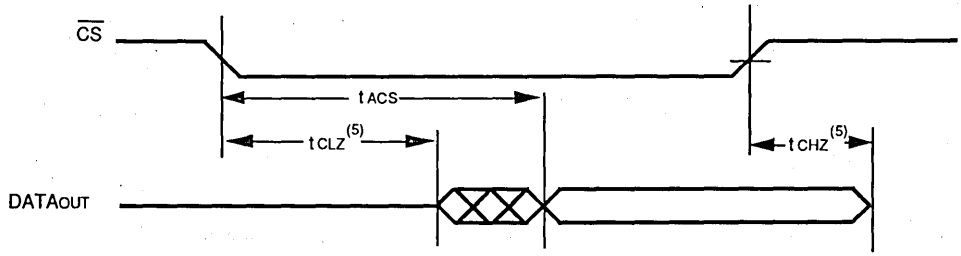
2703 drw 04

TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



2703 drw 05

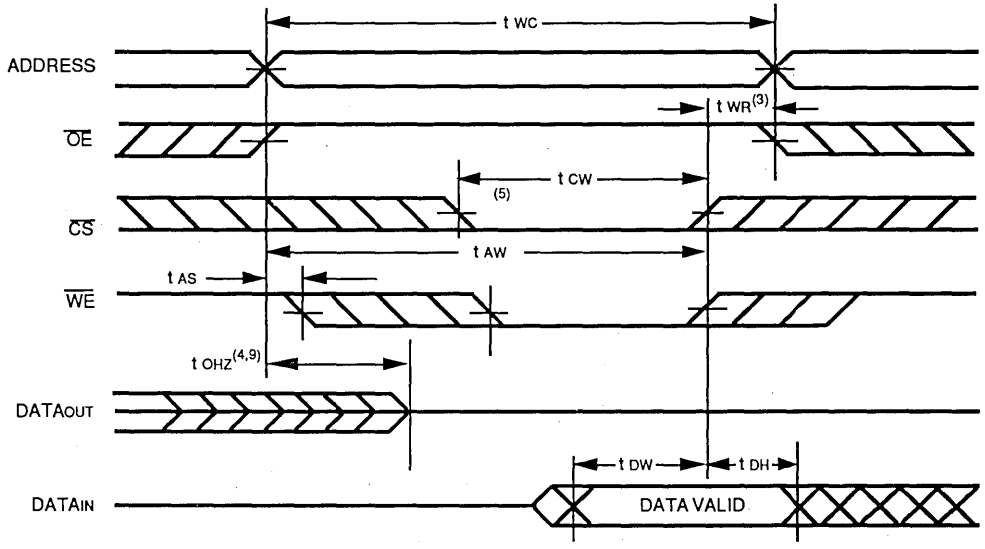
TIMING WAVEFORM OF READ CYCLE NO. 2(1,3,4)



2703 drw 06

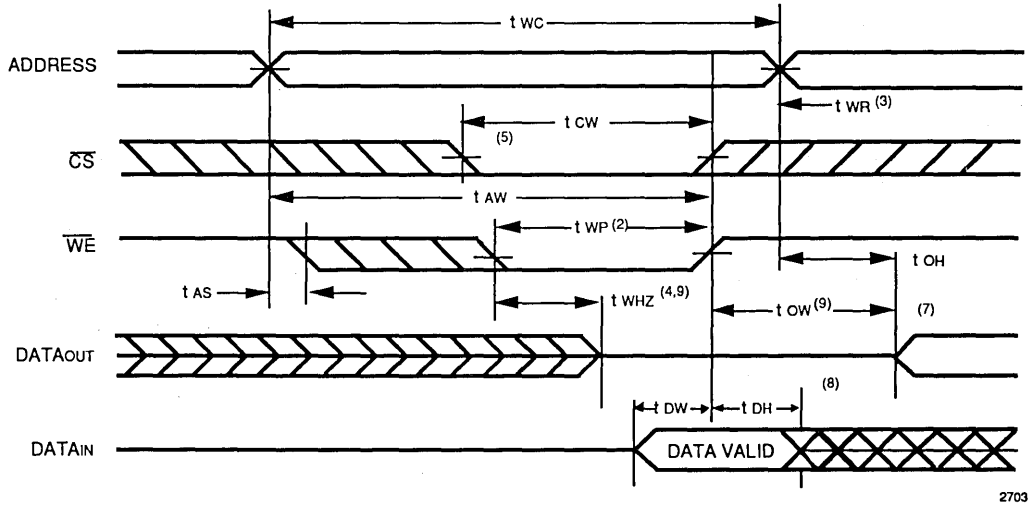
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200 mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1)



2703 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 2(1,6)



2703 drw 08

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must High during all address transitions.
2. A write occurs during the overlap (twp) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. twp is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the input state, so the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = VIL).
7. DOUT is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200 mV from steady state. This parameter is guaranteed by design, but not tested.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	Hi-Z	Standby
Read	L	L	H	Dout	Active
Write	L	X	L	Din	Active
Read	L	H	H	Hi-Z	Active

2703 tbl 08

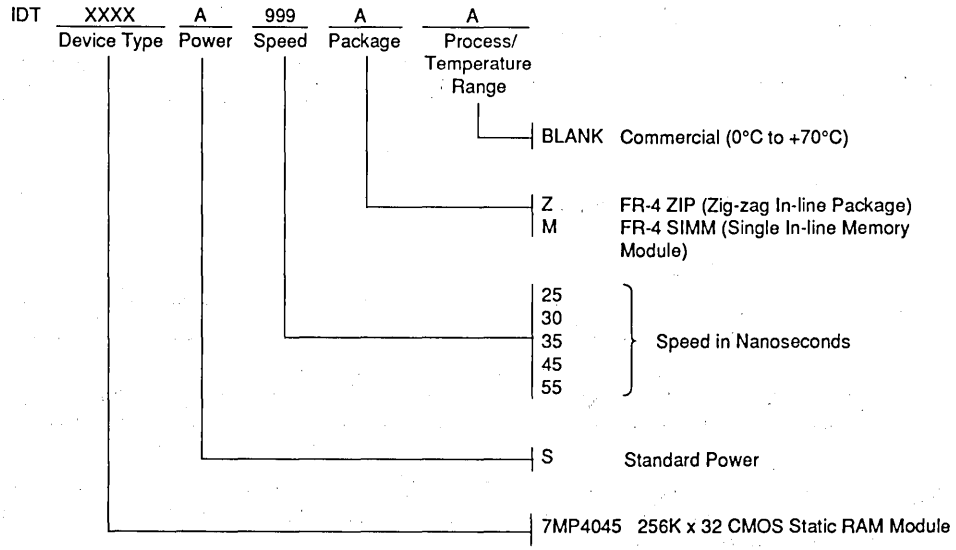
CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	V_{IN} = 0V	20	pF
$C_{IN(A)}$	Input Capacitance (Address and Control)	V_{IN} = 0V	70	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	20	pF

NOTE:
1. This parameter is guaranteed by design but not tested.

2703 tbl 09

ORDERING INFORMATION



Integrated Device Technology, Inc.

2 X 4K x 60 DATA/INSTRUCTION CACHE MODULE FOR IDT79R3000 (MULTIPROCESSOR)

PRELIMINARY
IDT7MB6064

FEATURES:

- High-speed CEMOS™ static RAM module constructed to support the IDT79R3000 CPU, in a multi-processor system, as a complete data and instruction cache
- Additional data and instruction address invalidation latches on-board to facilitate use in a multi-processor system
- Operating frequencies to support 12MHz, 16.7MHz, 20MHz, 25MHz and 33MHz IDT79R3000
- Available in a high density, low profile 132 pin QIP (Quad In-Line Package)
- Surface mounted SOs on a multilayer epoxy substrate
- Multiple ground pins for maximum noise immunity
- TTL compatible I/Os
- Single 5V (±10%) power supply

PIN CONFIGURATION[1]

GND	1	67	GND	GND	132	66	Vcc
D_0	2	68	D_1	D_{59}	131	65	D_{58}
D_2	3	69	D_3	D_{57}	130	64	D_{56}
D_4	4	70	GND	D_{55}	129	63	D_{54}
D_5	5	71	D_6	GND	128	62	D_{53}
$\overline{OE}_1$	6	72	$\overline{WE}_1$	$\overline{WE}_4$	127	61	$\overline{OE}_4$
D_7	7	73	Vcc	D_{52}	126	60	D_{51}
Vcc	8	74	D_8	D_{50}	125	59	GND
D_9	9	75	GND	GND	124	58	D_{49}
D_{10}	10	76	D_{11}	D_{48}	123	57	$P2A_0$
$P1A_0$	11	77	$P1A_1$	$P2A_1$	122	56	$P2A_2$
$P1A_2$	12	78	GND	$P2A_3$	121	55	$P2A_4$
$P1A_3$	13	79	$P1A_4$	GND	120	54	$P2A_5$
$P1A_5$	14	80	$P1A_6$	$P2A_6$	119	53	GND
$P1A_7$	15	81	$P1A_8$	$P2A_7$	118	52	$P2A_8$
$P1A_9$	16	82	GND	GND	117	51	$P2A_9$
$P1A_{10}$	17	83	$P1A_{11}$	$P2A_{10}$	116	50	$P2A_{11}$
$P1LE_1$	18	84	$P1LE_2$	$\overline{P2OE}$	115	49	$\overline{RESET}_2$
$\overline{RESET}_1$	19	85	$\overline{P1OE}$	GND	114	48	Vcc
$\overline{OE}_2$	20	86	Vcc	P2LE	113	47	$\overline{OE}_3$
$\overline{WE}_2$	21	87	GND	D_{47}	112	46	$\overline{WE}_3$
D_{12}	22	88	D_{13}	GND	111	45	D_{46}
D_{14}	23	89	D_{15}	D_{44}	110	44	D_{45}
D_{16}	24	90	D_{17}	GND	109	43	D_{43}
Vcc	25	91	GND	D_{41}	108	42	D_{42}
D_{18}	26	92	D_{19}	D_{40}	107	41	GND
D_{20}	27	93	GND	Vcc	106	40	D_{39}
D_{21}	28	94	D_{22}	D_{38}	105	39	D_{37}
D_{23}	29	95	D_{24}	D_{36}	104	38	D_{35}
D_{25}	30	96	GND	GND	103	37	D_{34}
D_{26}	31	97	D_{27}	D_{33}	102	36	D_{32}
D_{28}	32	98	D_{29}	D_{31}	101	35	D_{30}
Vcc	33	99	GND	GND	100	34	GND

QIP
TOP VIEW

2666 drw 02

NOTE:
1. For module dimensions, please refer to drawing M30 in the packaging section.

DESCRIPTION:

The IDT7MB6064 is a 60K-byte high-speed CMOS static RAM cache module constructed on a multilayer epoxy substrate (FR-4), using 30 IDT6178 (4K x 4) Resettable RAMs and 16 IDT74FCT373 latches.

The IDT7MB6064 supports use in a multi-processor (R3000 based) system by providing data address invalidation latches onboard, ensuring cache coherency among the multiple CPUs. The IDT7MB6064 is organized as two separate banks of 4K x 60 with the IDT74FCT373s being used as address latches. The two banks of RAM with their associated address latches share a common 12-bit ADDRESS bus and a common 60 bit DATA bus. The write enable, RAM output enable and latch enable controls for the two banks are brought out separately, to support interleaving access to the two banks of RAM. Also, each bank has one set of address latches to reduce the capacitance loading on the outputs of the latches, and thereby enhance performance. $\overline{RESET}_1$/$\overline{RESET}_2$ clears the D_{36}-D_{59} portions of the data/instruction cache.

All inputs and outputs of the IDT7MB6064 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

PIN NAMES

D_0–D_{59}	Data I/Os
$P1A_0$–$P1A_{11}$	Address Inputs
$P2A_0$–$P2A_{11}$	Invalidate Address
$P1LE_1$	Data Address Latch Enable
$P1LE_2$	Instruction Address Latch Enable
$\overline{P1OE}$	Data Address Enable
$\overline{P2OE}$	Instruction Address Enable
P2LE	Invalidate Data Address Latch Enable
$\overline{RESET}_1$	Data Cache Reset
$\overline{RESET}_2$	Instruction Cache Reset
$\overline{WE}_1$–$\overline{WE}_4$	Write Enables
$\overline{OE}_1$–$\overline{OE}_4$	Output Enables
GND	Ground
Vcc	Power Supply

2666 bl 01

8

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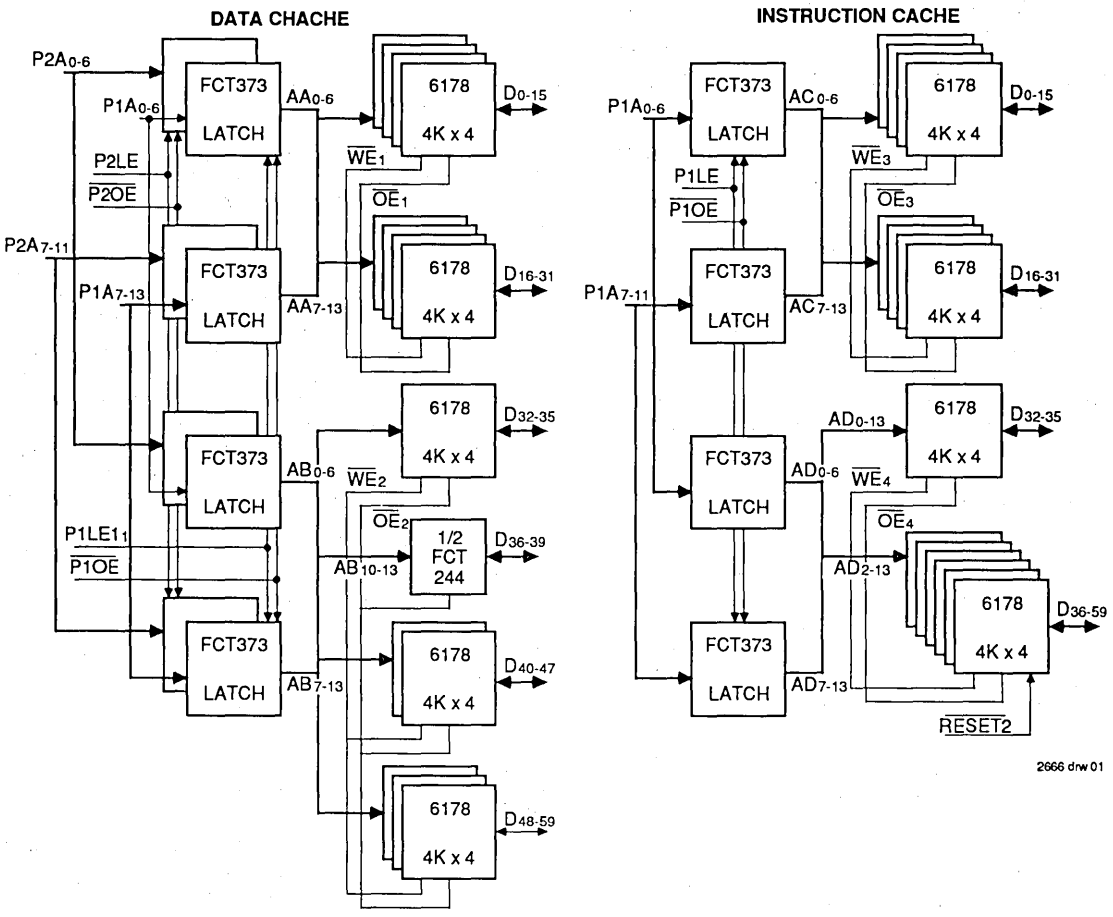
FUNCTIONAL BLOCK DIAGRAM



RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2666 tbl 04
1. V_{IL} = -3.0V for pulse width less than 20ns.

CAPACITANCE

Symbol	Parameter[1]	Conditions	Typ.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	V_{IN} = 0V	20	pF
$C_{IN(A)}$	Input Capacitance (Address)	V_{IN} = 0V	40	pF
$C_{IN(C)}$	Input Capacitance ($\overline{OE}$, $\overline{WE}$)	V_{IN} = 0V	50	pF
$C_{IN(C)}$	Input Capacitance ($\overline{CS}$)	V_{IN} = 0V	100	pF
$C_{IN(C)}$	Input Capacitance (LE, $\overline{PxOE}$)	V_{IN} = 0V	30	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	20	pF

NOTE: 2666 tbl 03
1. This parameter is guaranteed by design, but not tested.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating[1]	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2666 tbl 02
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%

2666 tbl 05

8

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2666 tbl 06

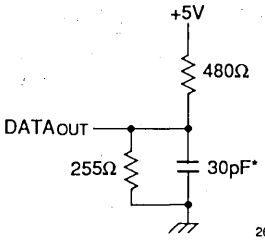


Figure 1. Output Load

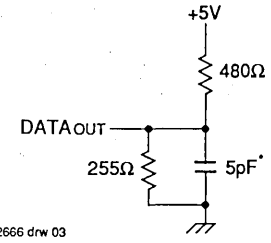


Figure 2. Output Load (for t_{OLZ} and t_{OHZ})

* Including scope and jig.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	12MHz		16.7MHz		20MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	20	—	20	—	20	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	—	10	—	10	µA
I_{CC1}	Operating Current	f = 0, $\overline{CS}$ = V_{IL}; V_{CC} = Max., Outputs Open	—	2925	—	2925	—	2925	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ = V_{IL}; f = f_{MAX}, Outputs Open	—	3850	—	3900	—	4150	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} - 0.2V, V_{IN} ≥ V_{CC} - 0.2V or ≤ 0.2V	—	450	—	450	—	450	mA
I_{SB}	Standby Power Supply Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}; f = f_{MAX}, Outputs Open	—	1300	—	1425	—	1575	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	—	2.4	—	2.4	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	—	0.4	—	0.4	V

NOTE:
1. I_{CC1}, I_{CC2} in the case for all devices selected (i.e. both instruction and data cache selected).

2666 tbl 07

DC ELECTRICAL CHARACTERISTICS (Continued)

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	20	—	20	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	—	10	µA
I_{CC1}	Operating Current	f = 0, $\overline{CS}$ = V_{IL}; V_{CC} = Max., Outputs Open	—	3400	—	3700	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ = V_{IL}; f = f_{MAX}, Outputs Open	—	4675	—	4900	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} - 0.2V, V_{IN} ≥ V_{CC} - 0.2V or ≤ 0.2V	—	600	—	960	mA
I_{SB}	Standby Power Supply Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}; f = f_{MAX}, Outputs Open	—	1700	—	2000	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	—	2.4	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	—	0.4	V

NOTE:
1. I_{CC1}, I_{CC2} in the case for all devices selected (i.e. both instruction and data cache selected).

2666 tbl 08

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

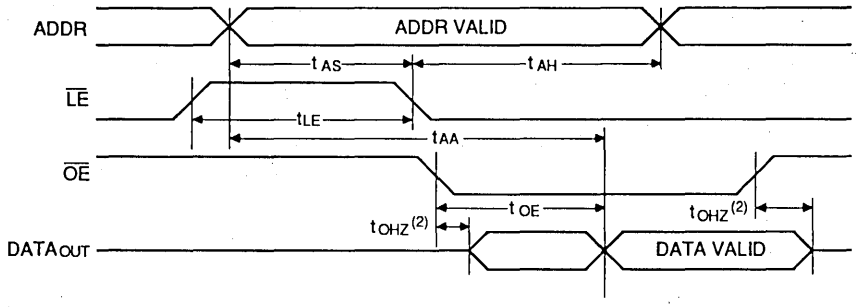
Symbol	Parameter	12MHz		16.7MHz		20MHz		25MHz		33MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{LE}	Latch Enable Width	6	—	6	—	6	—	6	—	6	—	ns
t_{AS}	Address Setup Time to LE	2	—	2	—	2	—	2	—	2	—	ns
t_{AH}	Address Hold Time from LE	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{AA}[2]	Address Access Time	—	45	—	35	—	30	—	25	—	20	ns
t_{OE}[3]	Output Enable to Output Valid	—	22	—	17	—	11	—	8	—	5	ns
t_{OHZ}[1]	Output Disable to Output in High Z	2	16	2	14	2	10	2	8	2	6	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
WRITE CYCLE												
t_{LE}	Latch Enable Width	6	—	6	—	6	—	6	—	6	—	ns
t_{AS}	Address Setup Time to LE	2	—	2	—	2	—	2	—	2	—	ns
t_{AH}	Address Hold Time to LE	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{AW}[2]	Address Valid to End of Write	40	—	30	—	25	—	23	—	20	—	ns
t_{WP}	Write Pulse Width	35	—	25	—	20	—	17	—	12	—	ns
t_{DW}	Data Valid to End of Write	20	—	13	—	13	—	11	—	8	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{LOE}[4]	Latch Output Enable	—	7	—	7	—	7	—	7	—	7	ns
RESET CYCLE												
t_{CLPW}	$\overline{RESET}$ Pulse Width	40	—	40	—	30	—	30	—	25	—	ns
t_{CLRC}	$\overline{RESET}$ High to $\overline{WE_4}$ Low	5	—	5	—	5	—	5	—	5	—	ns

NOTE:
1. This parameter is guaranteed by design but not tested.
2. LE already asserted.
3. For all $\overline{OE_1}$, $\overline{OE_2}$, $\overline{OE_3}$, $\overline{OE_4}$.
4. P1OE1 and P2OE1.

2666 tbl 09

8

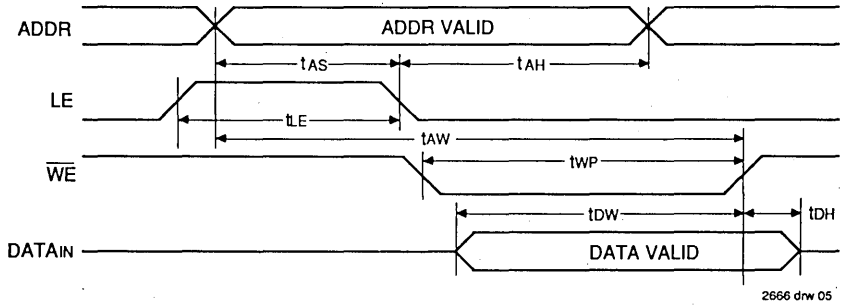
TIMING WAVEFORM OF READ CYCLE(1)



2666 drw 04

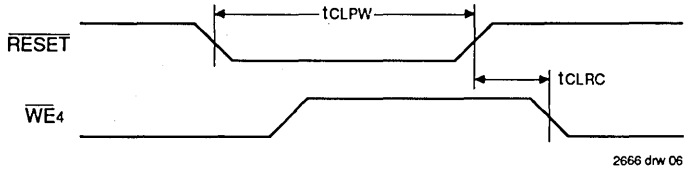
NOTES:
1. Assume $\overline{WE}$ is active high throughout this cycle.
2. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE



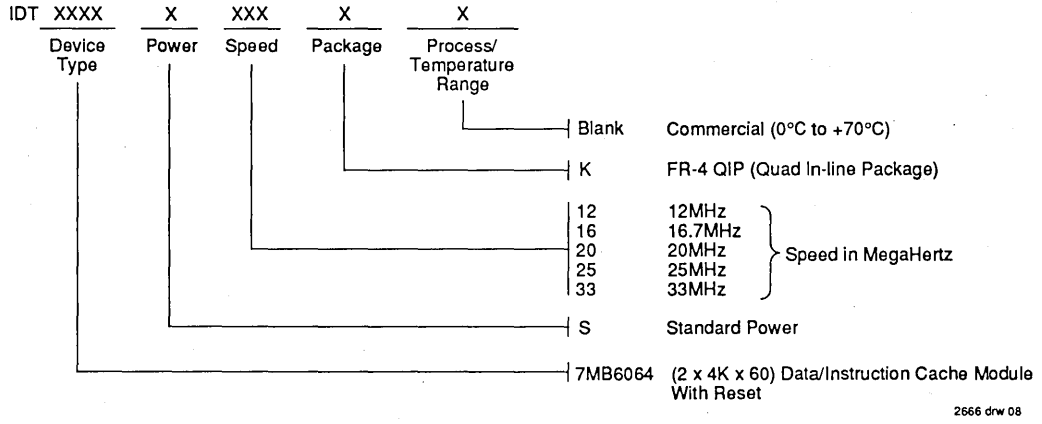
2666 drw 05

TIMING WAVEFORM OF $\overline{RESET}$ CYCLE



2666 drw 06

ORDERING INFORMATION



8

Integrated Device Technology, Inc.

2 x 4K x 64 DATA/INSTRUCTION CACHE MODULE FOR IDT79R3000 CPU

ADVANCE INFORMATION
IDT7MB6044

FEATURES:

- High-speed 64K-byte CMOS static RAM module constructed to support the IDT79R3000 RISC CPU as a complete data and instruction cache
- Operating frequencies to support 12MHz, 16.7MHz, 20MHz, 25MHz and 33MHz IDT79R3000
- Available in high-density, low profile 128-pin QIP (quad in-line package)
- Surface mounted SO components on a multi-layer epoxy substrate FR-4
- Multiple ground pins for maximum noise immunity
- On-board address latches for direct interface to the IDT79R3000 CPU
- TTL compatible I/Os
- Single 5V (± 10%) power supply

DESCRIPTION:

The IDT7MB6044 is a 64K-byte high-speed CEMOS™ static RAM cache module constructed on a multilayer epoxy substrate (FR-4) using 8 IDT71586 (4K X 16) latched RAMs.

The construction and specifications of this module have been optimized to support its use as a complete 4K deep Instruction and Data cache for the IDT79R3000 MIPs™ microprocessor.

The IDT7MB6044 is organized as two separate banks of 4K x 64 with the IDT71586s being used as address latched RAMs. The two banks of RAM with their associated address latches share a common 12-bit ADDRESS bus and a common 64-bit DATA bus. The chip select, write enable, RAM output enable and latch enable controls for the two banks are brought out separately to support interleaving access to the two banks of RAM.

All inputs and outputs of the IDT7MB6044 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

PIN CONFIGURATION[2]

GND	1	65	GND	Vcc	128	64	Vcc
D_0	2	66	D_1	D_{62}	127[1]	[1]63	D_{63}
D_2	3	67	D_3	D_{60}	126[1]	[1]62	D_{61}
D_4	4	68	D_5	D_{58}	125	61	D_{59}
D_6	5	69	D_7	D_{56}	124	60	D_{57}
D_8	6	70	D_9	GND	123	59	D_{55}
$\overline{WE}_1$	7	71	$\overline{OE}_1$	$\overline{WE}_4$	122	58	$\overline{OE}_4$
$\overline{CS}_1$	8	72	GND	D_{54}	121	57	$\overline{CS}_4$
$\overline{CS}_5$	9	73	D_{10}	D_{53}	120	56	$\overline{CS}_8$
$\overline{WE}_5$	10	74	$\overline{OE}_5$	$\overline{WE}_8$	119	55	$\overline{OE}_8$
D_{11}	11	75	D_{12}	D_{51}	118	54	D_{52}
D_{13}	12	76	Vcc	GND	117	53	D_{50}
A_0	13	77	A_1	N.C.	116	52	N.C.
A_2	14	78	A_3	A_{10}	115	51	A_{11}
A_4	15	79	A_5	A_8	114	50	A_9
D_{14}	16	80	GND	A_6	113	49	A_7
N.C.	17	81	LE1	LE2	112	48	N.C.
N.C.	18	82	LE3	LE4	111	47	N.C.
D_{15}	19	83	D_{16}	GND	110	46	D_{49}
D_{17}	20	84	Vcc	D_{47}	109	45	D_{48}
D_{18}	21	85	D_{19}	D_{45}	108	44	D_{46}
D_{20}	22	86	D_{21}	D_{43}	107	43	D_{44}
$\overline{WE}_2$	23	87	$\overline{OE}_2$	$\overline{WE}_7$	106	42	$\overline{OE}_7$
$\overline{CS}_2$	24	88	GND	GND	105	41	$\overline{CS}_7$
$\overline{CS}_6$	25	89	D_{22}	D_{42}	104	40	$\overline{CS}_3$
$\overline{WE}_6$	26	90	$\overline{OE}_6$	$\overline{WE}_3$	103	39	$\overline{OE}_3$
D_{23}	27	91	D_{24}	D_{40}	102	38	D_{41}
D_{25}	28	92	D_{26}	Vcc	101	37	D_{39}
D_{27}	29	93	D_{28}	D_{37}	100	36	D_{38}
D_{29}	30	94	D_{30}	D_{35}	99	35	D_{36}
D_{31}	31	95	D_{32}	D_{33}	98	34	D_{34}
Vcc	32	96	Vcc	GND	97	33	GND

QIP
TOP VIEW

2722 drw 01

PIN NAMES

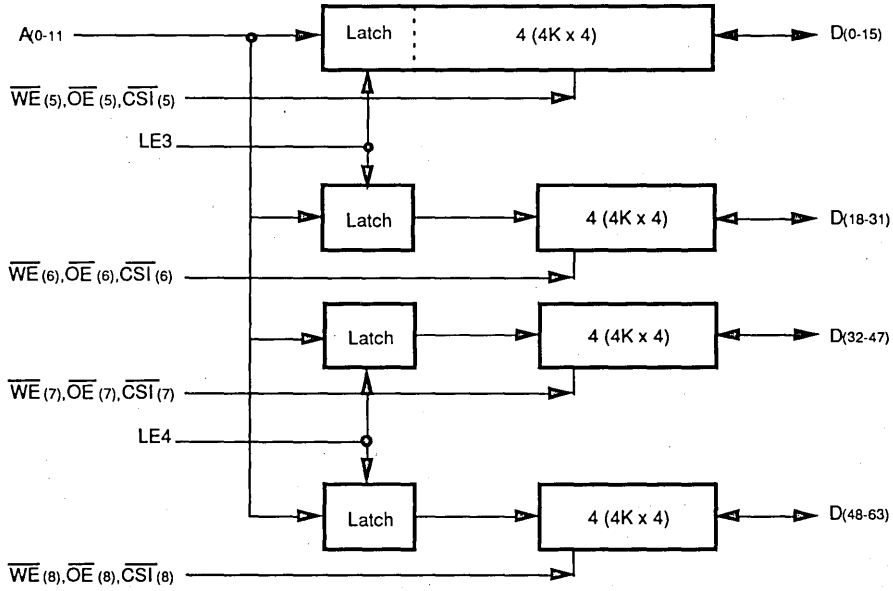
D_0 - D_{63}	Data I/Os
A_0 - A_{11}	Address Inputs
LE_1 - LE_4	Latch Enables
$\overline{CS}_1$ - $\overline{CS}_8$	RAM Selects
$\overline{WE}_1$ - $\overline{WE}_8$	Write Enables
$\overline{OE}_1$ - $\overline{OE}_8$	Output Enable
GND	Ground
Vcc	Power Supply
N.C.	No connection

2722 tbl 01

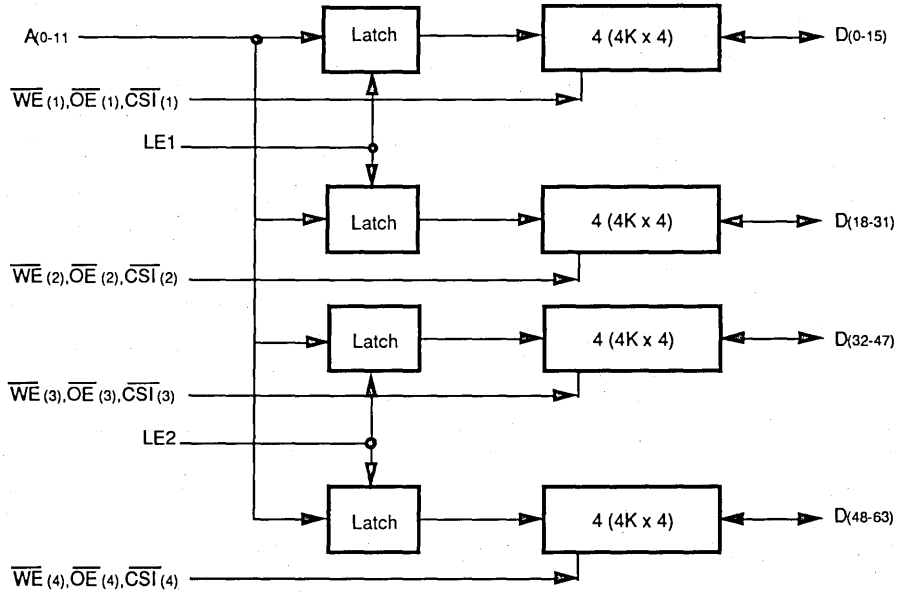
NOTES:
1. Each of these pins must be connected to GND or Vcc through a resistor for proper operation of the IDT79R3000 applications.
2. For module dimensions, please refer to module drawing M29 in the packaging section.

CEMOS is a trademark of Integrated Device Technology, Inc.

INSTRUCTION CACHE



DATA CACHE



2722 drw 02

8

Integrated Device Technology, Inc.

2 x 8K x 64 DATA/INSTRUCTION CACHE MODULE FOR IDT79R3000

ADVANCE INFORMATION
IDT7MB6043

FEATURES:

- High-speed CEMOS™ Static RAM Module constructed to support the IDT79R3000 RISC CPU as a complete data and instruction cache
- Operating frequencies to support 16.7MHz, 20MHz and 25MHz IDT79R3000
- Available in high-density, low-profile 128-pin QIP (Quad In-line Package)
- Surface mounted SO components on a multilayer epoxy substrate
- Multiple ground pins for maximum noise immunity
- On-board address latches for direct interface to the IDT79R3000 CPU
- TTL compatible I/Os
- Single 5V (±10%) power supply

DESCRIPTION:

The IDT7MB6043 is a 128KByte high-speed CMOS static RAM module constructed on a multilayer epoxy substrate (FR-4) using sixteen IDT7164 (8K x 8) RAMs and eight IDT74FCT373 latches.

The construction and specifications of this module have been optimized to support its use as a complete 8K deep Instruction and Data Cache for the IDT79R3000.

The IDTMB6043 is organized as two separate banks of 8K x 64 with IDT74FCT373s being used as address latches. The two banks of RAM, with their associated address latches, share a common 122-bit ADDRESS bus and a common 64-bit DATA bus.

The chip select, write enable, RAM output enable and latch enable controls for the two banks are brought out separately to support interleaving acess to the two banks of RAM. Also, each bank has two sets of address latches to reduce the capacitance loading, thereby, enhancing performance.

All inputs and outputs of the IDT7MB6043 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

PIN CONFIGURATION (1)

GND	1	65	GND	Vcc	128	64	Vcc
D_0	2	66	D_1	D(1)	127	63	D(1)
D_2	3	67	D_3	D(1)	126	62	D(1)
D_4	4	68	D_5	D_{58}	125	61	D_{59}
D_6	5	69	D_7	D_{56}	124	60	D_{57}
D_8	6	70	D_9	GND	123	59	D_{55}
$\overline{WE}_1$	7	71	$\overline{OE}_1$	$\overline{WE}_4$	122	58	$\overline{OE}_4$
$\overline{CS}_{11}$	8	72	GND	D_{54}	121	57	$\overline{CS}_{14}$
$\overline{CS}_{15}$	9	73	D_{10}	D_{53}	120	56	$\overline{CS}_{18}$
$\overline{WE}_5$	10	74	$\overline{OE}_5$	$\overline{WE}_8$	119	55	$\overline{OE}_8$
D_{11}	11	75	D_{12}	D_{51}	118	54	D_{52}
D_{13}	12	76	Vcc	GND	117	53	D_{50}
A_0	13	77	A_1	A_{12}	116	52	N.C.
A_2	14	78	A_3	A_{10}	115	51	A_{11}
A_4	15	79	A_5	A_8	114	50	A_9
D_{14}	16	80	GND	A_6	113	49	A_7
N.C.	17	81	LE1	LE2	112	48	N.C.
N.C.	18	82	LE3	LE4	111	47	N.C.
D_{15}	19	83	D_{16}	GND	110	46	D_{49}
D_{17}	20	84	Vcc	D_{47}	109	45	D_{48}
D_{18}	21	85	D_{19}	D_{45}	108	44	D_{46}
D_{20}	22	86	D_{21}	D_{43}	107	43	D_{44}
$\overline{WE}_2$	23	87	$\overline{OE}_2$	$\overline{WE}_7$	106	42	$\overline{OE}_7$
$\overline{CS}_{12}$	24	88	GND	GND	105	41	$\overline{CS}_{17}$
$\overline{CS}_{16}$	25	89	D_{22}	D_{42}	104	40	$\overline{CS}_{13}$
$\overline{WE}_6$	26	90	$\overline{OE}_6$	$\overline{WE}_3$	103	39	$\overline{OE}_3$
D_{23}	27	91	D_{24}	D_{40}	102	38	D_{41}
D_{25}	28	92	D_{26}	Vcc	101	37	D_{39}
D_{27}	29	93	D_{28}	D_{37}	100	36	D_{38}
D_{29}	30	94	D_{30}	D_{35}	99	35	D_{36}
D_{31}	31	95	D_{32}	D_{33}	98	34	D_{34}
Vcc	32	96	Vcc	GND	97	33	GND

QIP
TOP VIEW

PIN NAMES

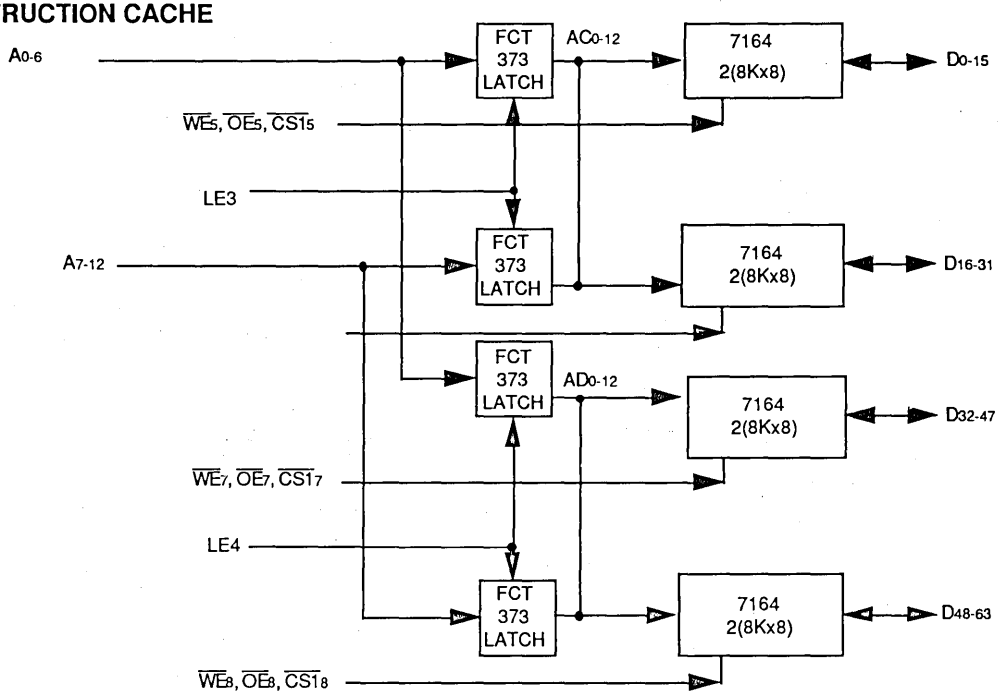
D_0 - D_{59}	Data Inputs/Outputs
A_0 - A_{11}	Address Inputs
LE_1 - LE_4	Latch Enables
$\overline{CS}_{11}$ - $\overline{CS}_{18}$	RAM Selects
$\overline{WE}_1$ - $\overline{WE}_8$	Write Enables
$\overline{OE}_1$ - $\overline{OE}_8$	Output Enables
GND	Ground
Vcc	Power Supply
N.C.	No connection

2800 tbl 01

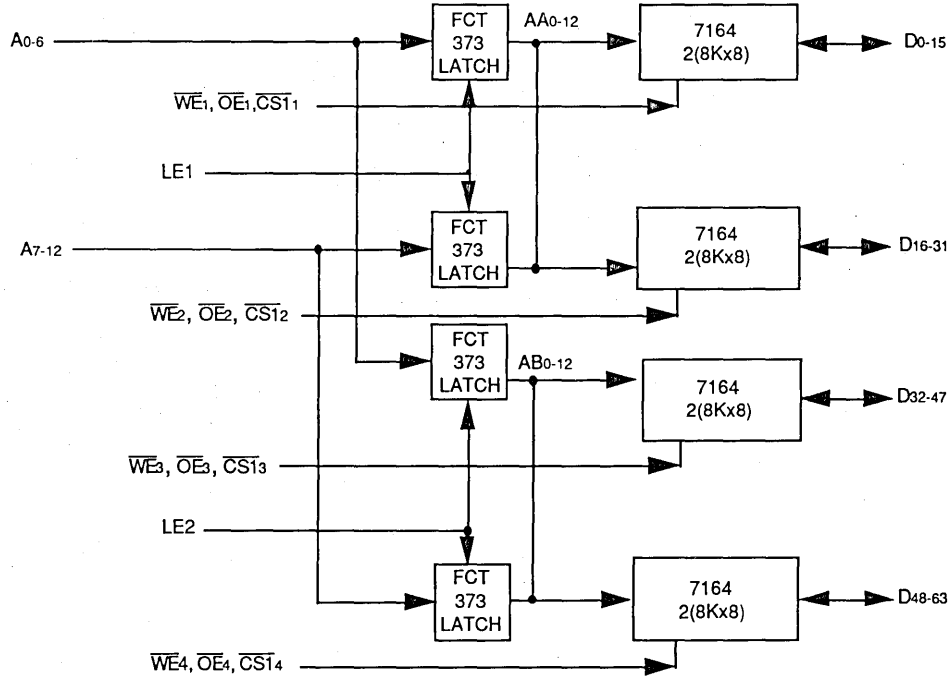
NOTE:
1. These pins must be connected to GND or Vcc through a resistor for proper operation in the IDT79R3000 application.

CEMOS is a trademark of Integrated Device Technology, Inc.

INSTRUCTION CACHE



DATA CACHE



8

Integrated Device Technology, Inc.

2 x 8K x 64 DATA/INSTRUCTION CACHE MODULE FOR IDT79R3000 CPU (MULTIPROCESSOR)

ADVANCE INFORMATION
IDT7MB6051

FEATURES:

- High-speed 128K-Byte CMOS static RAM module constructed to support the IDT79R3000 RISC CPU in a multi-processor system as a complete data and instruction cache
- Additional data adress invalidation latches on-board to facilitate use in a multi-processor system
- Operating frequencies to support 12MHz, 16.7MHz, 20MHz, 25MHz and 33MHz IDT79R3000
- Available in high-density, low profile 144-pin QIP (Quad In-line Package)
- Surface mounted SO components on a multi-layer epoxy substrate FR-4
- Multiple ground pins for maximum noise immunity
- TTL compatible I/Os
- Single 5V (± 10%) power supply

PIN CONFIGURATION[2]

GND	1	73	GND	Vcc	144	72	Vcc
D_0	2	74	D_1	D_{62}	143[1]	71[1]	D_{63}
D_2	3	75	D_3	D_{60}	142[1]	70[1]	D_{61}
D_4	4	76	D_5	D_{58}	141	69	D_{59}
D_6	5	77	D_7	D_{56}	140	68	D_{57}
D_8	6	78	D_9	GND	139	67	D_{55}
$\overline{WE_1}$	7	79	$\overline{OE_1}$	$\overline{WE_4}$	138	66	$\overline{OE_4}$
$\overline{CS1_1}$	8	80	GND	D_{54}	137	65	$\overline{CS1_4}$
$\overline{CS1_5}$	9	81	D_{10}	D_{53}	136	64	$\overline{CS1_8}$
$\overline{WE_5}$	10	82	$\overline{OE_5}$	$\overline{WE_8}$	135	63	$\overline{OE_8}$
D_{11}	11	83	D_{12}	D_{51}	134	62	D_{52}
D_{13}	12	84	Vcc	GND	133	61	D_{50}
$P2A_0$	13	85	$P2A_1$	$P2A_{12}$	132	60	N.C.
$P2A_2$	14	86	$P2A_3$	$P2A_{10}$	131	59	$P2A_{11}$
$P2A_4$	15	87	$P2A_5$	$P2A_8$	130	58	$P2A_9$
$\overline{P1OE}$	16	88	$\overline{P2OE}$	$P2A_6$	129	57	$P2A_7$
A_0	17	89	A_1	A_{12}	128	56	N.C.
A_2	18	90	A_3	A_{10}	127	55	A_{11}
A_4	19	91	A_5	A_8	126	54	A_9
D_{14}	20	92	GND	A_6	125	53	A_7
N.C.	21	93	$P1LE_1$	N.C.	124	52	N.C.
N.C.	22	94	$P1LE_2$	P2LE	123	51	N.C.
D_{15}	23	95	D_{16}	GND	122	50	D_{49}
D_{17}	24	96	Vcc	D_{47}	121	49	D_{48}
D_{18}	25	97	D_{19}	D_{45}	120	48	D_{46}
D_{20}	26	98	D_{21}	D_{43}	119	47	D_{44}
$\overline{WE_2}$	27	99	$\overline{OE_2}$	$\overline{WE_7}$	118	46	$\overline{OE_7}$
$\overline{CS1_2}$	28	100	GND	GND	117	45	$\overline{CS1_7}$
$\overline{CS1_6}$	29	101	D_{22}	D_{42}	116	44	$\overline{CS1_3}$
$\overline{WE_6}$	30	102	$\overline{OE_6}$	$\overline{WE_3}$	115	43	$\overline{OE_3}$
D_{23}	31	103	D_{24}	D_{40}	114	42	D_{41}
D_{25}	32	104	D_{26}	Vcc	113	41	D_{39}
D_{27}	33	105	D_{28}	D_{37}	112	40	D_{38}
D_{29}	34	106	D_{30}	D_{35}	111	39	D_{36}
D_{31}	35	107	D_{32}	D_{33}	110	38	D_{34}
Vcc	36	108	Vcc	GND	109	37	GND

QIP
TOP VIEW

2723 drw 01

DESCRIPTION:

The IDT7MB6051 is a 128K-byte high-speed CMOS static RAM cache module constructed on a multilayer epoxy substrate (FR-4) using 16 IDT7164 (8K X 8) RAMs and 8 IDT4FCT373 latches..

The construction and specifications of this module have been optimized to support its use as a complete 8K deep Instruction and Data cache for the IDT79R3000 MIPs™ microprocessor.

The IDT7MB6051 supports use in a multi-processor system by providing data invalidation latches on-board. The IDT7MB6051 is organized as two separate banks of 8K x 64 with the IDT74FCT373s being used as address latches.The two banks of RAM with their associated address latches share a common 14-bit ADDRESS bus and a common 64-bit DATA bus. The chip select, write enable, RAM output enable and latch enable controls for the two banks are brought out separately to support interleaving access to the two banks of RAM. Also, each bank has two sets of address latches to reduce the capacitance loading on the outputs of the latches and, thereby, enhance performance.

All inputs and outputs of the IDT7MB6051 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

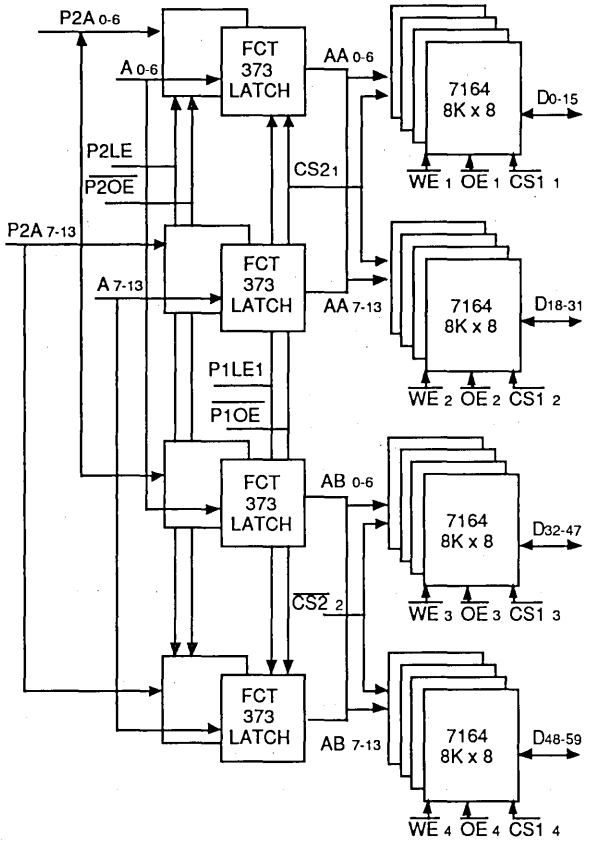
PIN NAMES

D_0 - D_{63}	Data Inputs/Outputs
A_0 - A_{13}	Address Inputs
$P2A_0$ - $P2A_{13}$	Invalid Address
P1LE1	Data Address Latch Enable
P1LE2	Instruction Address Latch Enable
$\overline{P1OE}$	Data Address Enable
$\overline{P2OE}$	Invalidate Address Enable
P2LE	Invalidate Address Latch Enable
$\overline{CS1_1}$ - $\overline{CS1_8}$	RAM Selects
$\overline{CS2_1}$ - $\overline{CS2_8}$	RAM Selects
$\overline{WE_1}$ - $\overline{WE_8}$	Write Enables
$\overline{OE_1}$ - $\overline{OE_8}$	Output Enable
GND	Ground
Vcc	Power Supply
N.C.	No connection

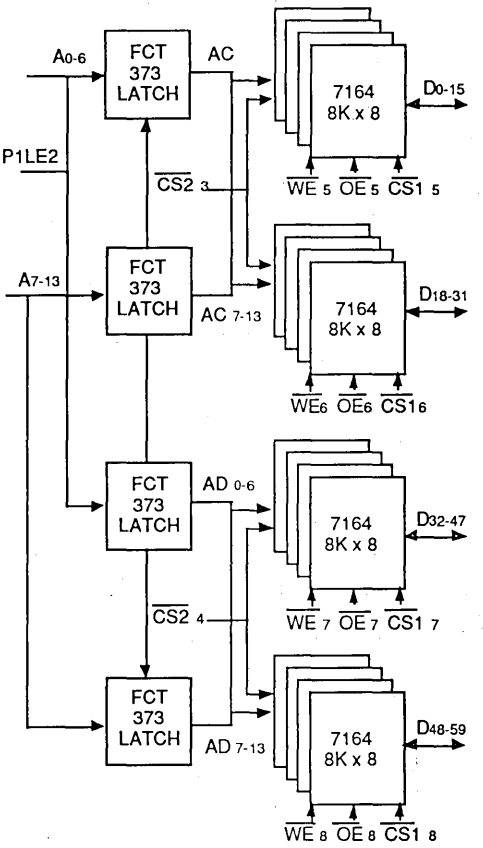
2723 tbl 01

NOTE:
1. Each of these pins must be connected to GND or Vcc through a resistor for proper operation of the IDT79R3000 applications.
2. Dimensions for these module are currently not available, please consult the factory.

DATA CACHE



INSTRUCTION CACHE



2723 drw 02

8

Integrated Device Technology, Inc.

2 x 16K x 60 DATA/INSTRUCTION CACHE MODULE FOR IDT79R3000 CPU

IDT7MB6039

FEATURES:

- High-speed 240K-Byte CMOS static RAM module constructed to support the IDT79R3000 RISC CPU as a complete data and instruction cache
- Operating frequencies to support 12MHz, 16.7MHz, 20MHz, 25MHz and 33MHz IDT79R3000
- Available in high-density, low profile 128-pin QIP (Quad In-line Package)
- Surface mounted SOs on a multi-layer epoxy substrate (FR-4)
- Multiple ground pins for maximum noise immunity
- On-board address latches for direct interface to the IDT79R3000 CPU
- TTL compatible I/Os
- Single 5V (±10%) power supply

DESCRIPTION:

The IDT7MB6039 is a 240K-byte high-speed CMOS static RAM cache module constructed on a multilayer epoxy substrate (FR-4), using 30 (16K X 4) SRAMs and 8 IDT74FCT373 latches.

The construction and specifications of this module have been optimized to support its use as a complete 16K deep Instruction and Data cache for the IDT79R3000 MIPs™ microprocessor.

The IDT7MB6039 is organized as two separate banks of 16K x 60 with the IDT74FCT373s being used as address latches. The two banks of RAM with their associated address latches share a common 14-bit ADDRESS bus and a common 60-bit DATA bus. The chip select, write enable, RAM output enable and latch enable controls for the two banks are brought out separately to support interleaving access to the two banks of RAM. Each bank of address latches reduces the capacitance loading on the outputs of the latches; thereby, enhancing CPU performance.

All inputs and outputs of the IDT7MB6039 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

PIN CONFIGURATION[2]

GND	1	65	GND	Vcc	128	64	Vcc
D_0	2	66	D_1	N.C.	127[1]	63[1]	N.C.
D_2	3	67	D_3	N.C.	126[1]	62[1]	N.C.
D_4	4	68	D_5	D_{58}	125	61	D_{59}
D_6	5	69	D_7	D_{56}	124	60	D_{57}
D_8	6	70	D_9	GND	123	59	D_{55}
$\overline{WE_1}$	7	71	$\overline{OE_1}$	$\overline{WE_4}$	122	58	$\overline{OE_4}$
$\overline{CS1_1}$	8	72	GND	D_{54}	121	57	$\overline{CS1_4}$
$\overline{CS1_5}$	9	73	D_{10}	D_{53}	120	56	$\overline{CS1_8}$
$\overline{WE_5}$	10	74	$\overline{OE_5}$	$\overline{WE_8}$	119	55	$\overline{OE_8}$
D_{11}	11	75	D_{12}	D_{51}	118	54	D_{52}
D_{13}	12	76	Vcc	GND	117	53	D_{50}
A_0	13	77	A_1	A_{12}	116	52	A_{13}
A_2	14	78	A_3	A_{10}	115	51	A_{11}
A_4	15	79	A_5	A_8	114	50	A_9
D_{14}	16	80	GND	A_6	113	49	A_7
$\overline{CS2_3}$	17	81	LE1	LE2	112	48	$\overline{CS2_2}$
$\overline{CS2_2}$	18	82	LE3	LE4	111	47	$\overline{CS2_4}$
D_{15}	19	83	D_{16}	GND	110	46	D_{49}
D_{17}	20	84	Vcc	D_{47}	109	45	D_{48}
D_{18}	21	85	D_{19}	D_{45}	108	44	D_{46}
D_{20}	22	86	D_{21}	D_{43}	107	43	D_{44}
$\overline{WE_2}$	23	87	$\overline{OE_2}$	$\overline{WE_7}$	106	42	$\overline{OE_7}$
$\overline{CS1_2}$	24	88	GND	GND	105	41	$\overline{CS1_7}$
$\overline{CS1_6}$	25	89	D_{22}	D_{42}	104	40	$\overline{CS1_3}$
$\overline{WE_6}$	26	90	$\overline{OE_6}$	$\overline{WE_3}$	103	39	$\overline{OE_3}$
D_{23}	27	91	D_{24}	D_{40}	102	38	D_{41}
D_{25}	28	92	D_{26}	Vcc	101	37	D_{39}
D_{27}	29	93	D_{28}	D_{37}	100	36	D_{38}
D_{29}	30	94	D_{30}	D_{35}	99	35	D_{36}
D_{31}	31	95	D_{32}	D_{33}	98	34	D_{34}
Vcc	32	96	Vcc	GND	97	33	GND

2800 drw 01

QIP
TOP VIEW

PIN NAMES

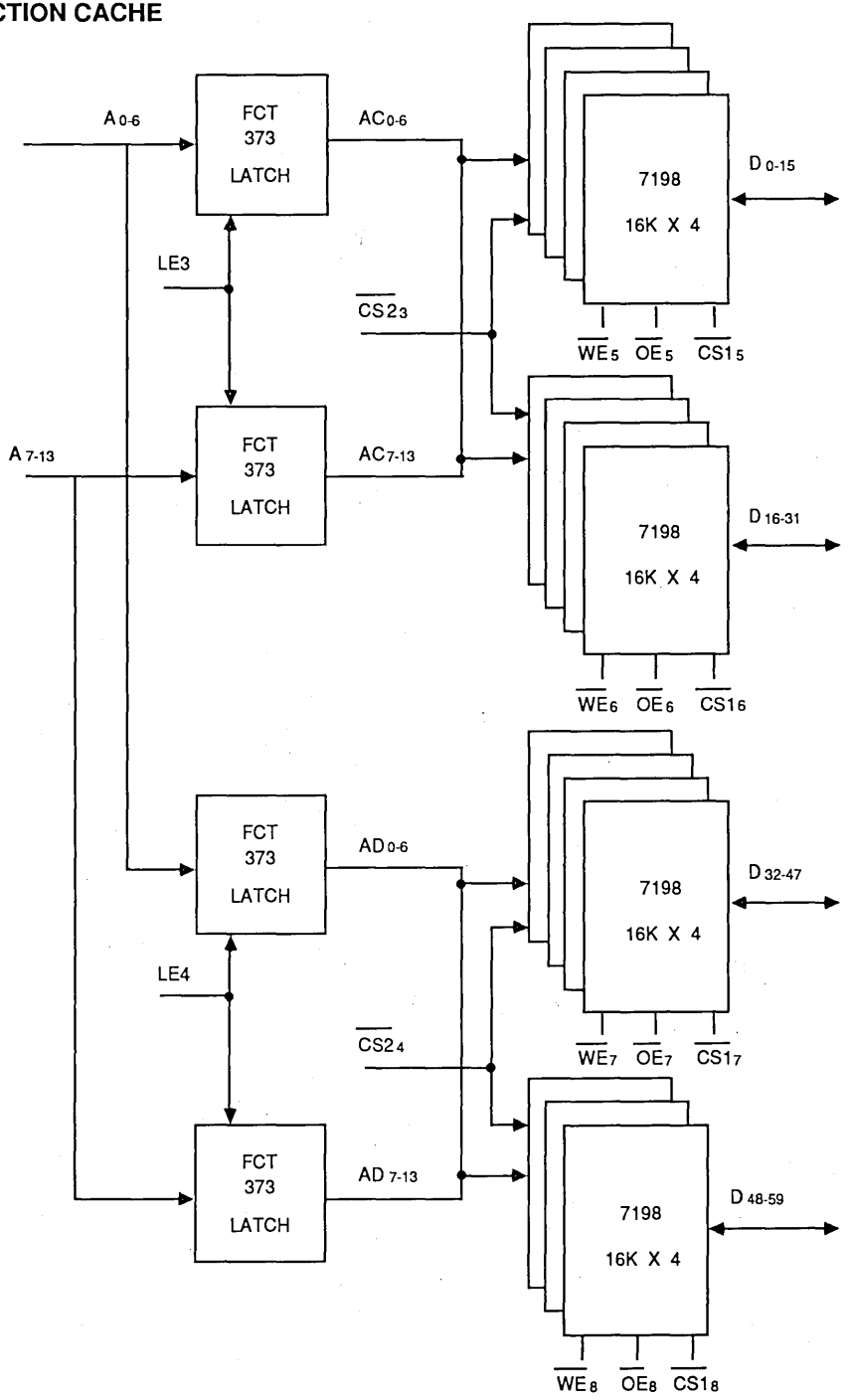
D_0 - D_{59}	Data Inputs/Outputs
A_0 - A_{13}	Address Inputs
LE_1 - LE_4	Latch Enables
$\overline{CS1_1}$ - $\overline{CS1_8}$	RAM Selects
$\overline{CS2_1}$ - $\overline{CS2_4}$	RAM Selects
$\overline{WE_1}$ - $\overline{WE_8}$	Write Enables
$\overline{OE_1}$ - $\overline{OE_8}$	Output Enables
GND	Ground
Vcc	Power Supply
N.C.	No connection [1]

2800 tbl 01

NOTES:

1. Each of these pins must be connected to GND for proper operation of this module.
2. For module dimensions, please refer to module drawing M28 in the packaging section.

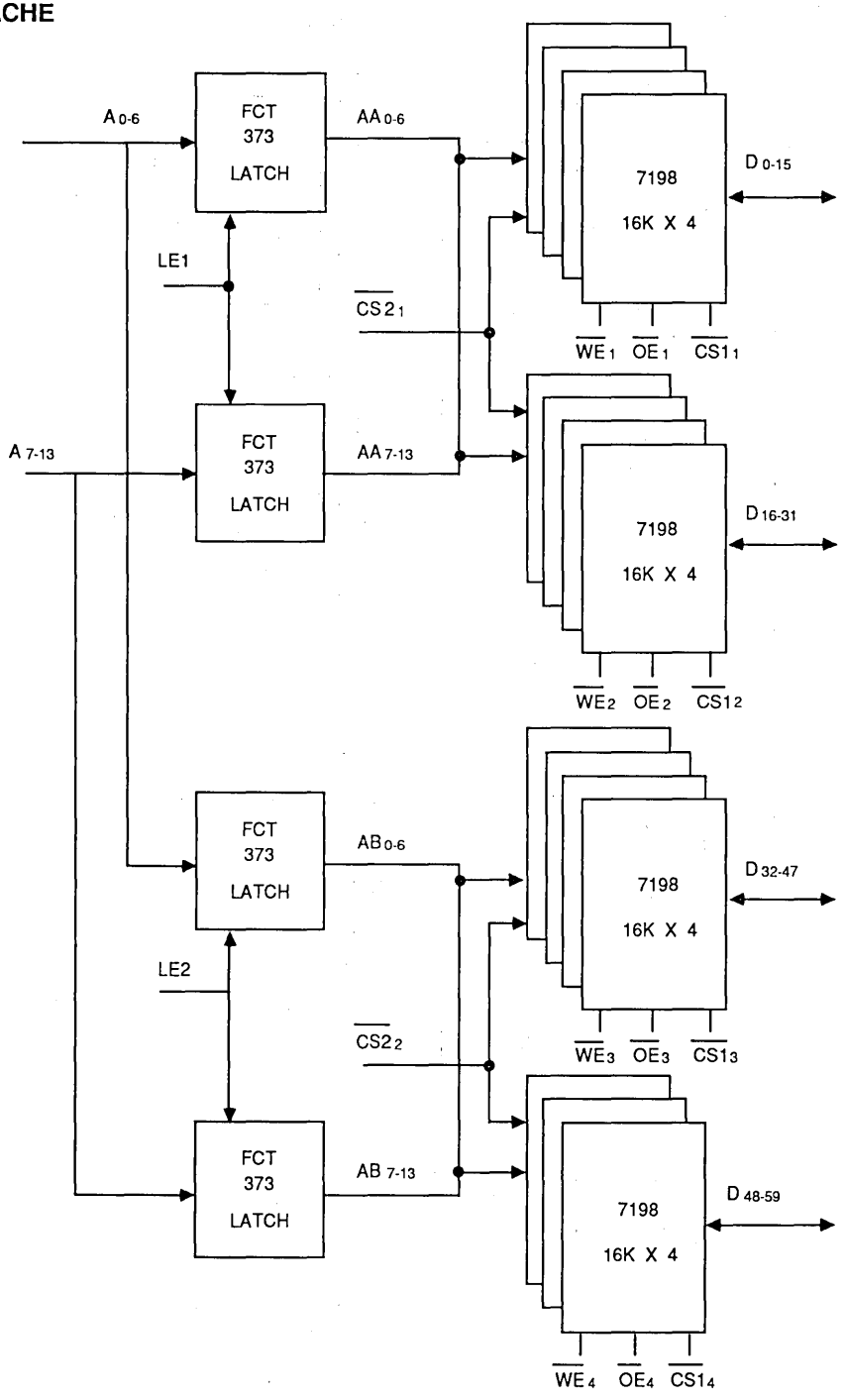
INSTRUCTION CACHE



2800 drw 02

8

DATA CACHE



2800 drw 03

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Comm.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2800 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2800 tbl 03

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2800 tbl 04

DC ELECTRICAL CHARACTERISTICS

(Vcc=5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	12 MHz Min.	12 MHz Max.	16.7 MHz Min.	16.7 MHz Max.	20 MHz Min.	20 MHz Max.	25 MHz Min.	25 MHz Max.	33 MHz Min.	33 MHz Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	Vcc = Max., V_{IN} = GND to Vcc	—	20	—	20	—	20	—	20	—	20	µA
$\|I_{LO}\|$	Output Leakage Current	Vcc = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to Vcc	—	10	—	10	—	10	—	10	—	10	µA
I_{CC1}	Operating Current	$\overline{CS}$ = V_{IL}, Vcc = Max. Outputs Open, f = 0	—	3000	—	3000	—	3000	—	3500	—	3750	mA
I_{CC2}	Dynamic Operating Current	Vcc = Max., $\overline{CS}$ = V_{II}, f = fMAX, Outputs Open	—	3750	—	3750	—	4050	—	4500	—	4750	mA
I_{SB1}	Full Standby Operating Current	$\overline{CS}$ ≥ Vcc - 0.2V, V_{IN} > Vcc - 0.2V or < 0.2V	—	450	—	450	—	450	—	600	—	750	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH}, Vcc = Max., Outputs Open, f = fMAX	—	1500	—	1500	—	1650	—	1800	—	2000	mA
V_{OH}	Output High Voltage	Vcc = Min., I_{OH} = -4mA	2.4	—	2.4	—	2.4	—	2.4	—	2.4	—	V
V_{OL}	Output Low Voltage	Vcc = Min. I_{OL} = 8mA	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	V

2800 tbl 05

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2800 tbl 06

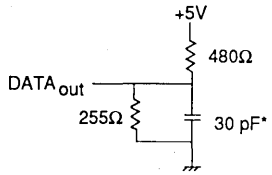


Figure 1. Output Load

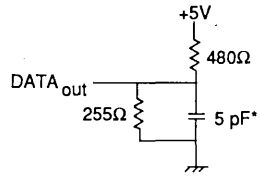


Figure 2. Output Load (for tOLZ, tOHZ)

*Including scope and jig.

2800 drw 04

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

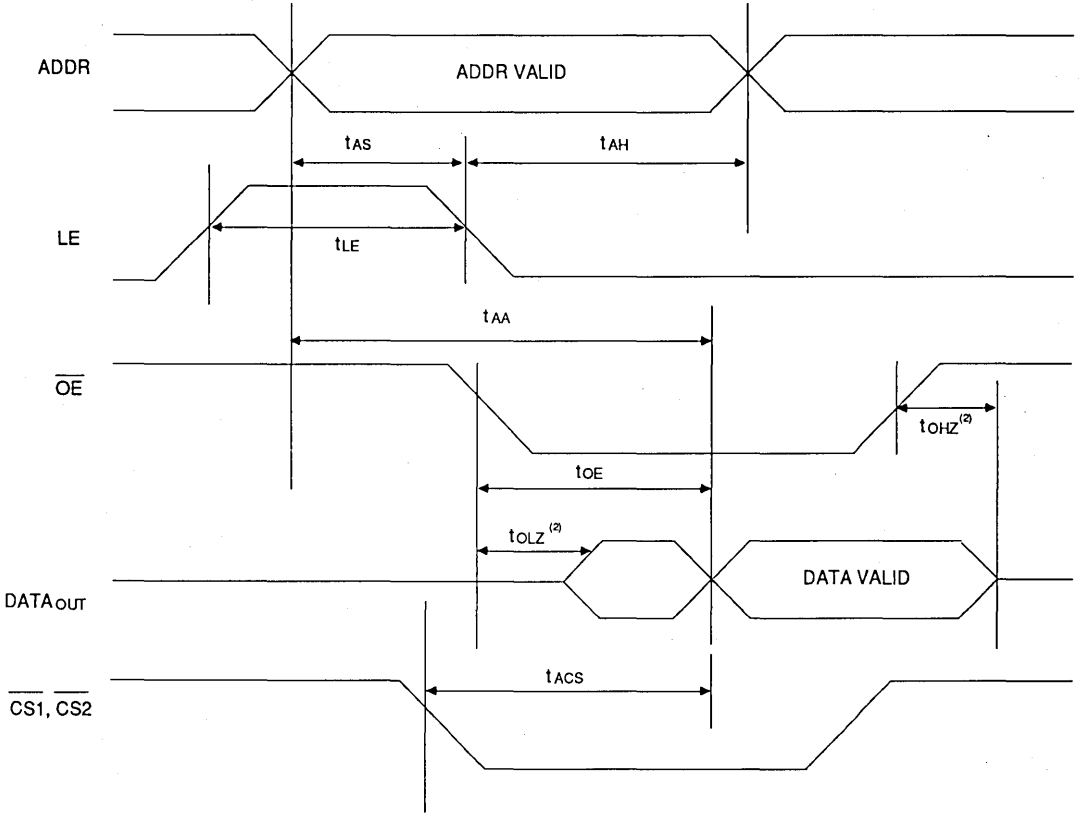
Symbol	Parameter	12MHz Min.	12MHz Max.	16.7 MHz Min.	16.7 MHz Max.	20 MHz Min.	20 MHz Max.	25 MHz Min.	25 MHz Max.	33 MHz Min.	33 MHz Max.	Unit
Read Cycle												
tLE	Latch Enable Width	8	—	6	—	6	—	6	—	6	—	ns
tAS	Address Setup Time to LE	4	—	2	—	2	—	2	—	2	—	ns
tAH	Address Hold Time from LE	3	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tAA(2)	Address Access Time	—	45	—	35	—	30	—	25	—	20	ns
tACS	Chip Select Time	—	40	—	30	—	25	—	20	—	15	ns
tOE	Output Enable Time	—	22	—	17	—	11	—	8	—	5	ns
tOHZ(1)	Output Disable to Output in High Z	2	16	2	14	2	10	2	8	2	6	ns
tOLZ(1)	Output Disable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
Write Cycle												
tLE	Latch Enable Width	8	—	6	—	6	—	6	—	6	—	ns
tAS	Address Setup Time to LE	4	—	2	—	2	—	2	—	2	—	ns
tAH	Address Hold Time from LE	3	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tAW(2)	Address Valid to End of Write	40	—	30	—	25	—	23	—	20	—	ns
tCW	Chip Select to End of Write	35	—	25	—	20	—	18	—	15	—	ns
tWP	Write Pulse Width	30	—	25	—	20	—	17	—	12	—	ns
tDW	Data Valid to End of Write	20	—	13	—	13	—	11	—	8	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns

NOTES:

2800 tbl 07

1. This parameter is guaranteed by design but not tested.
2. LE already asserted.

TIMING WAVEFORM OF READ CYCLE (1)



2800 drw 05

NOTES:
1. $\overline{WE}$ and $\overline{CS}$ must be High for all address transitions.
2. This parameter is guaranteed by design but not tested.

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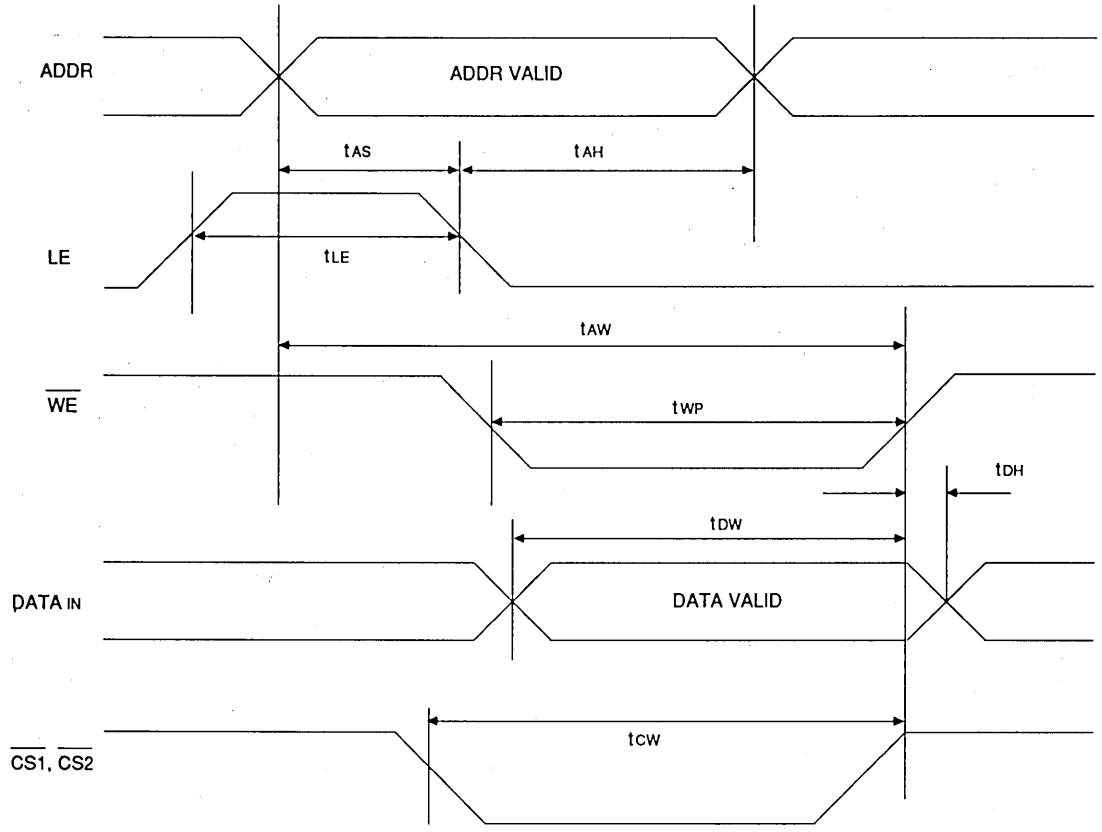
TIMING WAVEFORM OF WRITE CYCLE (1)



2800 drw 06

NOTE:
1. A write occurs (tWP) during the overlap of a Low $\overline{CS}$ and $\overline{WE}$ and a High LE.

TRUTH TABLE

Mode	$\overline{CS1}$	$\overline{CS2}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	X	High Z	Standby
Standby	X	H	X	X	High Z	Standby
Read	L	L	L	H	Dout	Active
Read	L	L	H	H	High Z	Active
Write	L	L	X	L	DIN	Active

2800 tbl 07

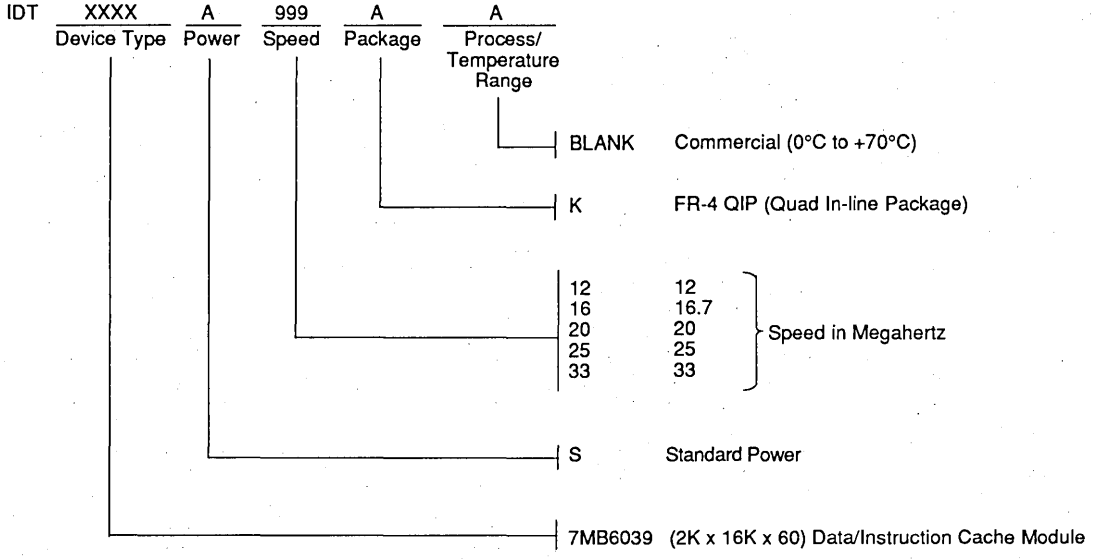
CAPACITANCE (1) (TA = +25°C, F = 1.0 MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C IN	Input Capacitance	VIN = 0V	60	pF
C OUT	Output Capacitance	VOUT = 0V	20	pF

NOTE:
1. This parameter is guaranteed by design but not tested.

2800 tbl 08

ORDERING INFORMATION



2800 drw 11

8

Integrated Device Technology, Inc.

2 x 16K x 60 DATA/INSTRUCTION CACHE MODULE FOR IDT79R3000 CPU (MULTIPROCESSOR)

IDT7MB6049

FEATURES:

- High Speed 240K-Byte CMOS Static RAM Module con structed to support the IDT79R3000 CPU in a multi processor system as a complete data and instruction cache
- Additional data and instruction address invalidation latches on-board to facilitate use in a multi-processor system
- Operating frequencies to support 12MHz, 16.7MHz, 20MHz, 25MHz, and 33MHz IDT79R3000
- Available in a high density, low profile 120-pin QIP (Quad-In-Line Package)
- Surface mounted SO's on a multilayer epoxy substrate (FR-4)
- Multiple ground pins for maximum noise immunity.
- TTL compatible I/O's
- Single 5V (±10%) power supply

PIN CONFIGURATION[1]

GND	1	61	GND	GND	120	60	Vcc
D(0)	2	62	D(1)	D(58)	119	59	D(59)
D(2)	3	63	D(3)	D(56)	118	58	D(57)
D(4)	4	64	D(5)	D(54)	117	57	D(55)
D(6)	5	65	D(7)	D(52)	116	56	D(53)
$\overline{WE}$(1)	6	66	$\overline{OE}$(1)	$\overline{WE}$(4)	115	55	$\overline{OE}$(4)
$\overline{CS}$(1)	7	67	Vcc	GND	114	54	GND
D(8)	8	68	D(9)	D(50)	113	53	D(51)
D(10)	9	69	D(11)	D(48)	112	52	D(49)
P1A(0)	10	70	P1A(1)	P2A(0)	111	51	P2A(1)
P1A(2)	11	71	P1A(3)	P2A(2)	110	50	P2A(3)
P1A(4)	12	72	P1A(5)	P2A(4)	109	49	P2A(5)
P1LE1	13	73	P1LE2	P2LE1	108	48	P2LE2
P1A(6)	14	74	P1A(7)	P2A(6)	107	47	P2A(7)
P1A(8)	15	75	P1A(9)	P2A(8)	106	46	P2A(9)
P1A(10)	16	76	P1A(11)	P2A(10)	105	45	P2A(11)
P1A(12)	17	77	P1A(13)	P2A(12)	104	44	P2A(13)
$\overline{P1OE}$(1)	18	78	$\overline{P1OE}$(2)	$\overline{P2OE}$(1)	103	43	$\overline{P2OE}$(2)
D(12)	19	79	D(13)	D(46)	102	42	D(47)
D(14)	20	80	D(15)	D(44)	101	41	D(45)
D(16)	21	81	D(17)	D(42)	100	40	D(43)
D(18)	22	82	D(19)	D(40)	99	39	D(41)
$\overline{WE}$(2)	23	83	$\overline{OE}$(2)	$\overline{WE}$(3)	98	38	$\overline{OE}$(3)
GND	24	84	GND	Vcc	97	37	$\overline{CS}$(2)
D(20)	25	85	D(21)	D(38)	96	36	D(39)
D(22)	26	86	D(23)	D(36)	95	35	D(37)
D(24)	27	87	D(25)	D(34)	94	34	D(35)
D(26)	28	88	D(27)	D(32)	93	33	D(33)
D(28)	29	89	D(29)	D(30)	92	32	D(31)
Vcc	30	90	GND	GND	91	31	GND

2796 drw 01

QIP
TOP VIEW

NOTE:
1. For module dimensions, please refer to drawing M26 in the packaging section.

DESCRIPTION:

The IDT7MB6049 is a 240K-Byte high-speed CMOS Static RAM cache module constructed on a multilayer epoxy substrate (FR-4) using 28 (16K x 4) RAM's, 16 IDT74FCT373 latches, and 1 IDT74FCT244.

The IDT7MB6049 is organized as two separate banks of 16K x 60 with the IDT74FCT373's being used as address latches. The two banks of RAM with their associated address latches share a common 14-bit ADDRESS bus and a common 60-bit DATA bus. The chip select, write enable, RAM output enable, and latch enable controls for the two banks are brought out separately, to support inter-leaving access to the two banks of RAM. Also, each bank has two sets of address latches to reduce the capacitance loading on the outputs of the latches; thereby enhancing CPU performance.

The IDTMB6049 supports use in a multi-processor (IDT79R3000 based) system by providing a second address bus and an addtional set of latches for that bus. This bus is used in multi-processor applications to latch an address from a source other than the R3000. This maintains cache coherency by allowing the system to invalidate entries in the data cache. For more details on IDT7MB6049 operation, please refer to Application Note AN-76.

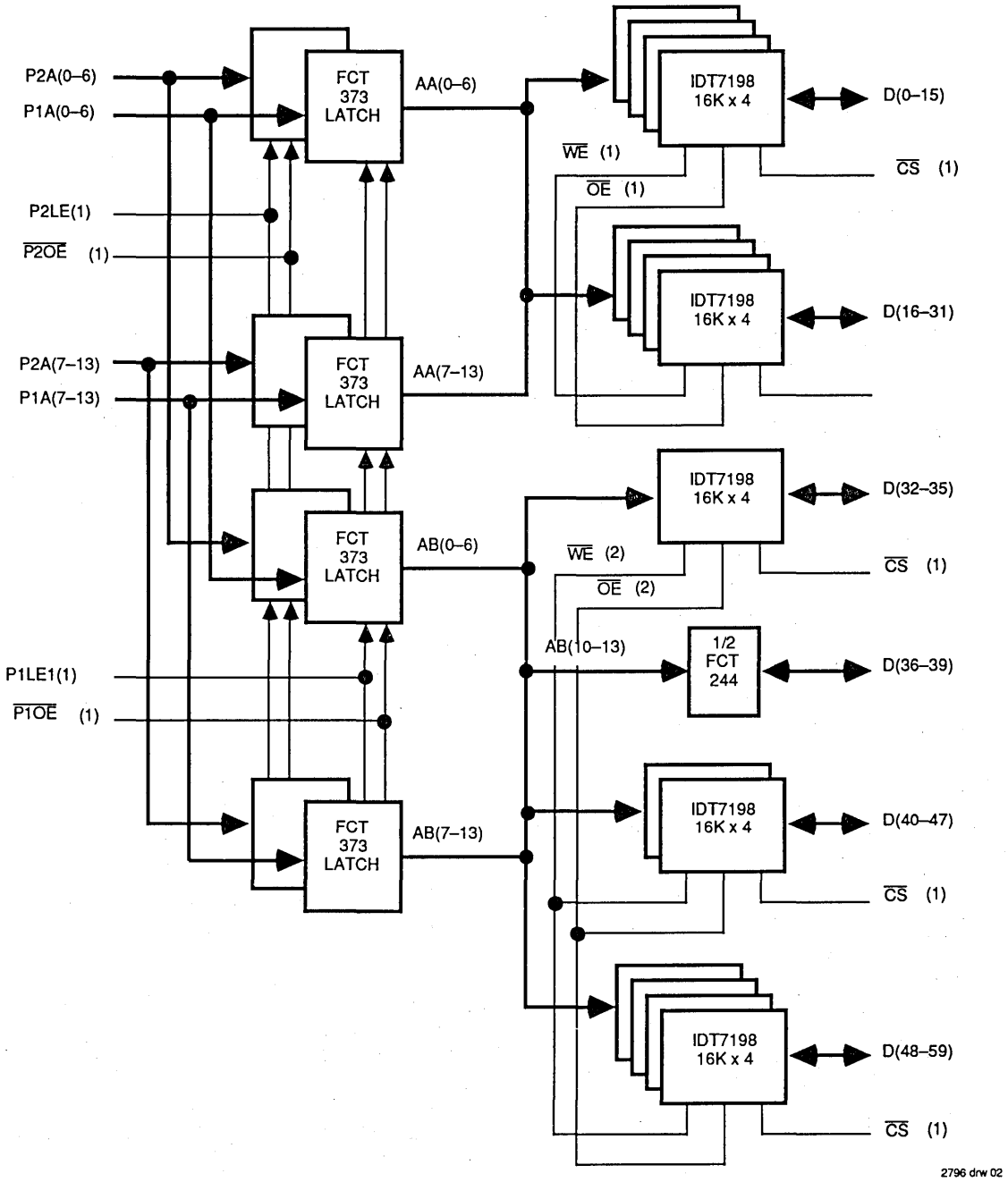
All inputs and outputs of the IDT7MB6049 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

PIN NAMES

D (0)–D (59)	Data Inputs/Outputs
P1A (0)–P1A (13)	Address inputs
P2A (0)–P2A (13)	Invalidate Address Inputs
P1LE1	Data Address Latch Enable
P1LE2	Instruction Address Latch Enable
$\overline{P1OE}$ (1)	Data Address Enable
$\overline{P1OE}$ (2)	Instruction Address Enable
$\overline{P2OE}$ (1)	Invalidate Data Address Enable
$\overline{P2OE}$ (2)	Invalidate Instruction Address Enable
P2LE1 (1)	Invalidate Data Address Latch Enable
P2LE2 (2)	Invalidate Instruction Address Latch Enable
$\overline{CS}$ (1), $\overline{CS}$ (2)	Data, Instruction Cache RAM Selects
$\overline{WE}$ (1) – $\overline{WE}$ (4)	Write Enables
$\overline{OE}$ (1) – $\overline{OE}$ (4)	Output Enables
GND	Ground
Vcc	Power Supply

2796 tbl 01

FUNCTIONAL BLOCK DIAGRAM

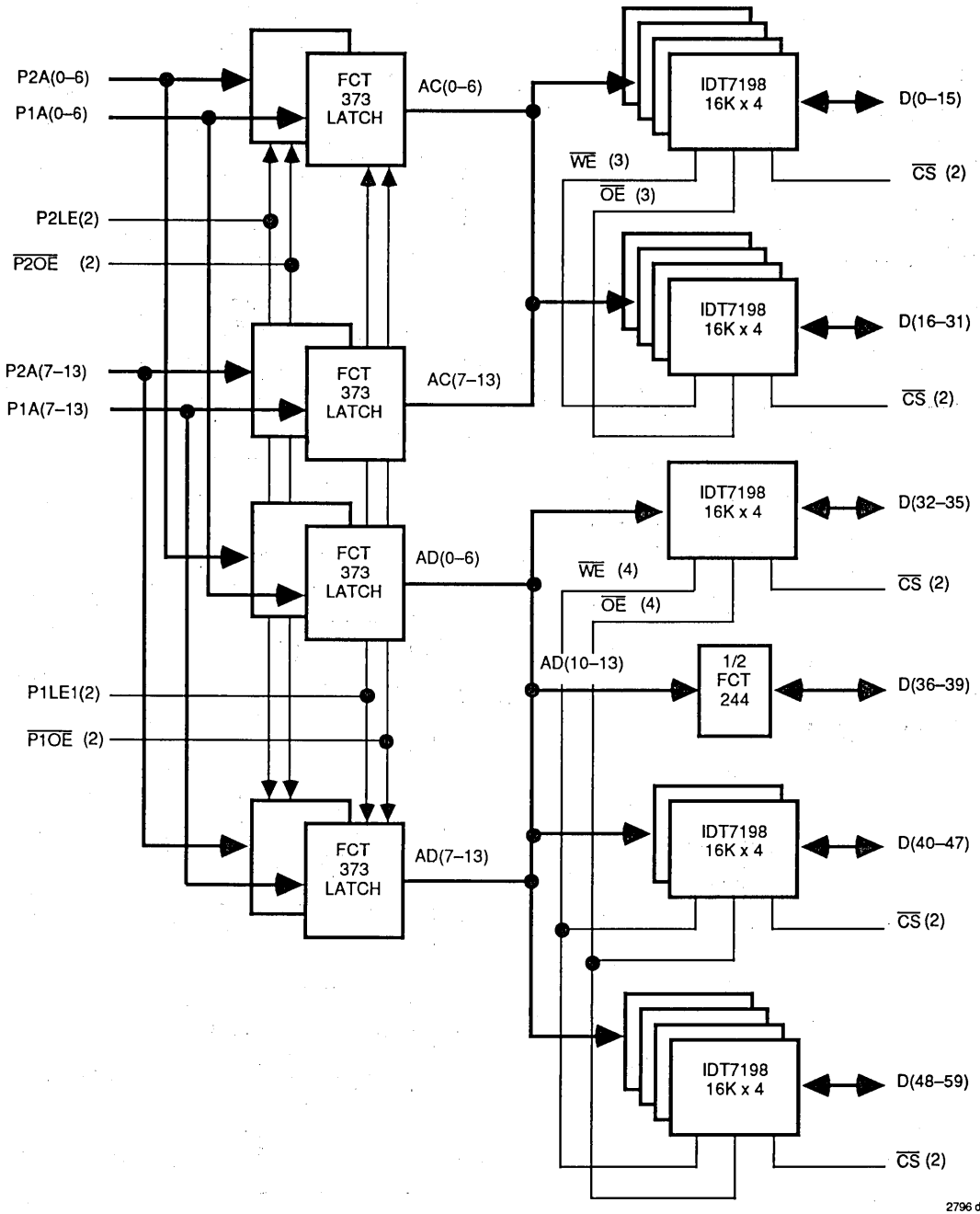


2796 drw 02

DATA CACHE

8

FUNCTIONAL BLOCK DIAGRAM



INSTRUCTION CACHE

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to 7.0	V
T_A	Operating Temperature	0 to 70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2796 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE: 2796 tbl 03

1. $V_{IL\ (Min.)}$ = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to 70°C	0V	5.0V ± 10%

2796 tbl 04

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	12MHz		16.7MHz		20MHz		25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	20	—	20	—	20	—	20	—	20	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	—	10	—	10	—	10	—	10	µA
I_{CC1}	Operating Current	f = 0, $\overline{CS}$ = V_{IL}, V_{CC} = Max., Output Open	—	2350	—	2400	—	2500	—	2850	—	3000	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ ≤ V_{IL}, f = f_{MAX}, Output Open	—	2850	—	2900	—	3125	—	3400	—	3600	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} 0.2V, V_{IN} > V_{CC} – 0.2V or < 0.2V	—	450	—	450	—	450	—	600	—	750	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max. f = f_{MAX}, Outputs Open	—	1300	—	1425	—	1575	—	1700	—	2000	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	—	2.4	—	2.4	—	2.4	—	2.4	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	V

2796 tbl 05

8

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2796 tbl 06

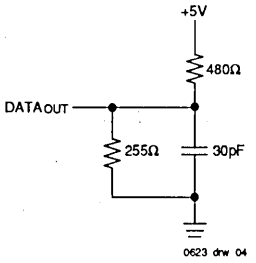
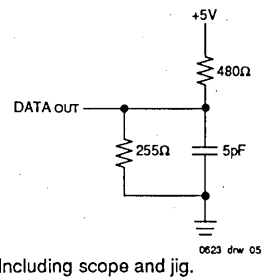


Figure 1. Output Load



* Including scope and jig.

Figure 2. Output Load (for tOLZ, tOHZ)

AC ELECTRICAL CHARACTERISTICS

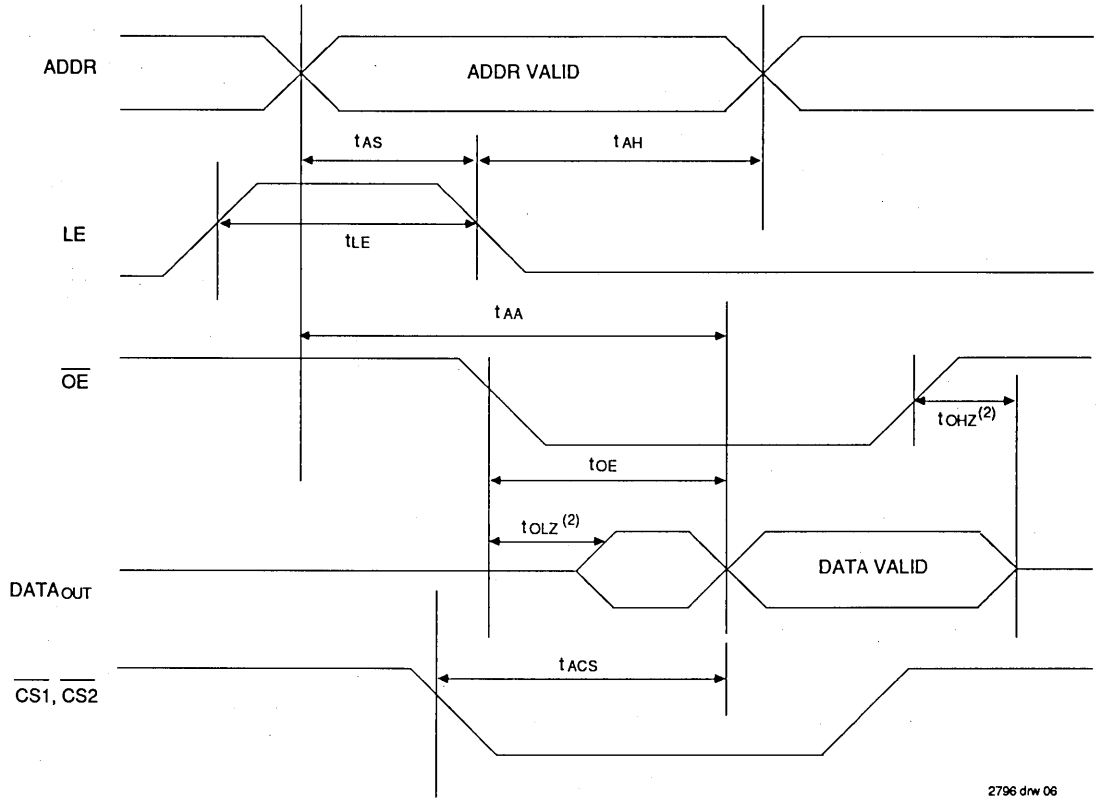
(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	12MHz		16.7MHz		20MHz		25MHz		33MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
tLE	Latch Enable Width	8	—	6	—	6	—	6	—	6	—	ns
tAS	Address Setup Time to LE	4	—	2	—	2	—	2	—	2	—	ns
tAH	Address Hold Time from LE	3	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tAA(2)	Address Access Time	—	45	—	35	—	30	—	25	—	20	ns
tACS	Chip Select Time	—	40	—	30	—	25	—	20	—	15	ns
tOE(3)	Output Enable Time	—	22	—	17	—	11	—	8	—	5	ns
tOHZ(1)	Output Disable to Output in High Z	2	16	2	14	2	10	2	8	2	6	ns
tOLZ(1)	Output Disable to Output in Low Z	5	—	5	—	5	—	5	—	5	–	ns
Write Cycle												
tLE	Latch Enable Width	8	—	6	—	6	—	6	—	6	—	ns
tAS	Address Setup Time to LE	4	—	2	—	2	—	2	—	2	—	ns
tAH	Address Hold Time from LE	3	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tAW(2)	Address Valid to End of Write	40	—	30	—	25	—	23	—	20	—	ns
tCW	Chip Select to End of Write	35	—	25	—	20	—	18	—	15	—	ns
tWP	Write Pulse Width	30	—	25	—	20	—	17	—	12	—	ns
tDW	Data Valid to End of Write	20	—	13	—	13	—	11	—	8	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tLOE(4)	Latch Output Enable	—	7	—	7	—	7	—	7	—	7	ns

2796 tbl 07

NOTES:
1. This parameter is guaranteed by design but not tested.
2. LE already asserted.
3. For all $\overline{OE}_{(1)}$, $\overline{OE}_{(2)}$, $\overline{OE}_{(3)}$, $\overline{OE}_{(4)}$
4. For all $\overline{P1OE}_1$, $\overline{P1OE}_2$, $\overline{P2OE}_1$, $\overline{P2OE}_2$

TIMING WAVEFORM OF READ CYCLE

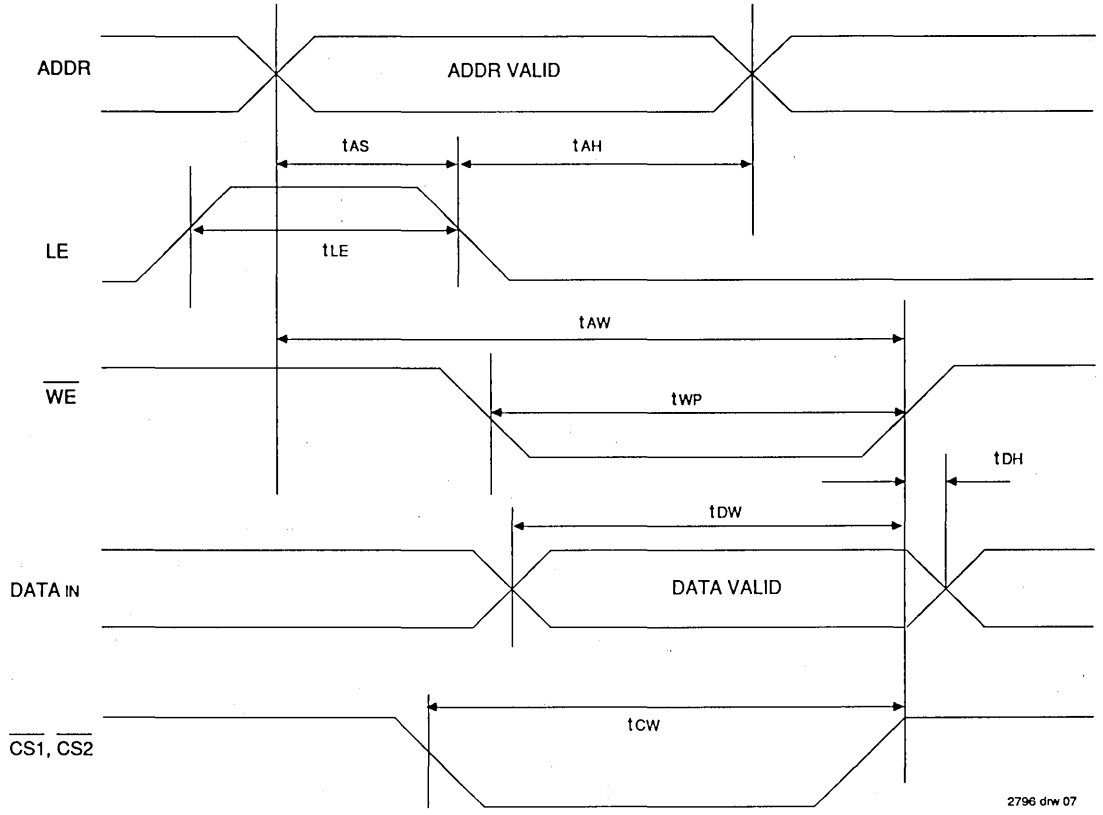


NOTE:

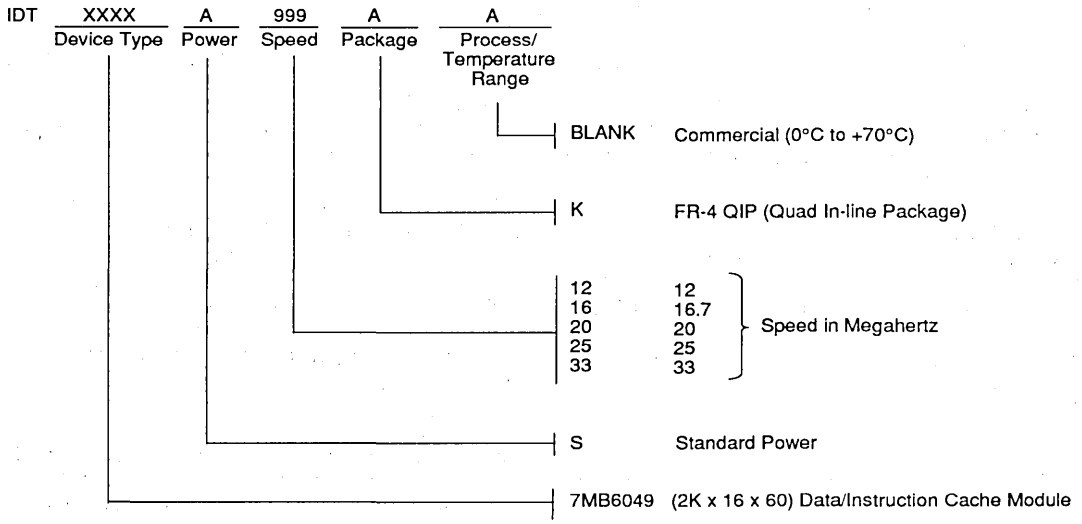
1. This parameter is guaranteed by design but not tested

8

TIMING WAVEFORM OF WRITE CYCLE



ORDERING INFORMATION



8

Integrated Device Technology, Inc.

2 x 16K x 64 DATA/INSTRUCTION CACHE MODULE FOR GENERAL PURPOSE CPUs

IDT7MB6040

FEATURES:

- High-speed 256K-ByteCMOS static RAM module constructed to support general purpose CPUs as a complete data and instruction cache
- Supports operating frequencies of 12MHz, 16.7MHz, 20MHz, 25MHz and 33MHz
- Available in a high-density, low profile 128-pin QIP (quad in-line package)
- Surface mounted SO's on a multilayer epoxy substrate (FR-4)
- Multiple ground pins for maximum noise immunity
- TTL-compatible I/Os
- Single 5V (±10%) power supply

PIN CONFIGURATION[1]

GND	1	65	GND	V_{CC}	128	64	V_{CC}
D_0	2	66	D_1	D_{62}	127	63	D_{63}
D_2	3	67	D_3	D_{60}	126	62	D_{61}
D_4	4	68	D_5	D_{58}	125	61	D_{59}
D_6	5	69	D_7	D_{56}	124	60	D_{57}
D_8	6	70	D_9	GND	123	59	D_{55}
$\overline{WE}_1$	7	71	$\overline{OE}_1$	$\overline{WE}_4$	122	58	$\overline{OE}_4$
$\overline{CS1}_1$	8	72	GND	D_{54}	121	57	$\overline{CS1}_4$
$\overline{CS1}_5$	9	73	D_{10}	D_{53}	120	56	$\overline{CS1}_8$
$\overline{WE}_5$	10	74	$\overline{OE}_5$	$\overline{WE}_8$	119	55	$\overline{OE}_8$
D_{11}	11	75	D_{12}	D_{51}	118	54	D_{52}
D_{13}	12	76	V_{CC}	GND	117	53	D_{50}
A_0	13	77	A_1	A_{12}	116	52	A_{13}
A_2	14	78	A_3	A_{10}	115	51	A_{11}
A_4	15	79	A_5	A_8	114	50	A_9
D_{14}	16	80	GND	A_6	113	49	A_7
$\overline{CS2}_1$	17	81	LE_1	LE_2	112	48	$\overline{CS2}_2$
$\overline{CS2}_3$	18	82	LE_3	LE_4	111	47	$\overline{CS2}_4$
D_{15}	19	83	D_{16}	GND	110	46	D_{49}
D_{17}	20	84	V_{CC}	D_{47}	109	45	D_{48}
D_{18}	21	85	D_{19}	D_{45}	108	44	D_{46}
D_{20}	22	86	D_{21}	D_{43}	107	43	D_{44}
$\overline{WE}_2$	23	87	$\overline{OE}_2$	$\overline{WE}_7$	106	42	$\overline{OE}_7$
$\overline{CS1}_2$	24	88	GND	GND	105	41	$\overline{CS1}_7$
$\overline{CS1}_6$	25	89	D_{22}	D_{42}	104	40	$\overline{CS1}_3$
$\overline{WE}_6$	26	90	$\overline{OE}_6$	$\overline{WE}_3$	103	39	$\overline{OE}_3$
D_{23}	27	91	D_{24}	D_{40}	102	38	D_{41}
D_{25}	28	92	D_{26}	V_{CC}	101	37	D_{39}
D_{27}	29	93	D_{28}	D_{37}	100	36	D_{38}
D_{29}	30	94	D_{30}	D_{35}	99	35	D_{36}
D_{31}	31	95	D_{32}	D_{33}	98	34	D_{34}
V_{CC}	32	96	V_{CC}	GND	97	33	GND

QIP
TOP VIEW

2743 drw 01

DESCRIPTION:

The IDT7MB6040 is a 256K-byte high-speed CMOS static RAM cache module constructed on a multilayer epoxy substrate (FR-4), using 32 (16K x 4) RAMs and 8 IDT74FCT373 latches.

The IDT7MB6040 is organized as two separate banks of 16K x 64 with the IDT74FCT373s being used as address latches. The two banks of RAM with their associated address latches share a common 14-bit ADDRESS bus and common 64-bit DATA bus. The chip select, write enable, RAM output enable and latch enable controls for the two banks are brought out separately to support interleaving access to the banks of RAM. Each bank of address latches reduce the capacitance loading on the outputs of the latches; thereby, enhancing CPU performance.

All inputs and outputs of the IDT7MB6040 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

PIN NAMES

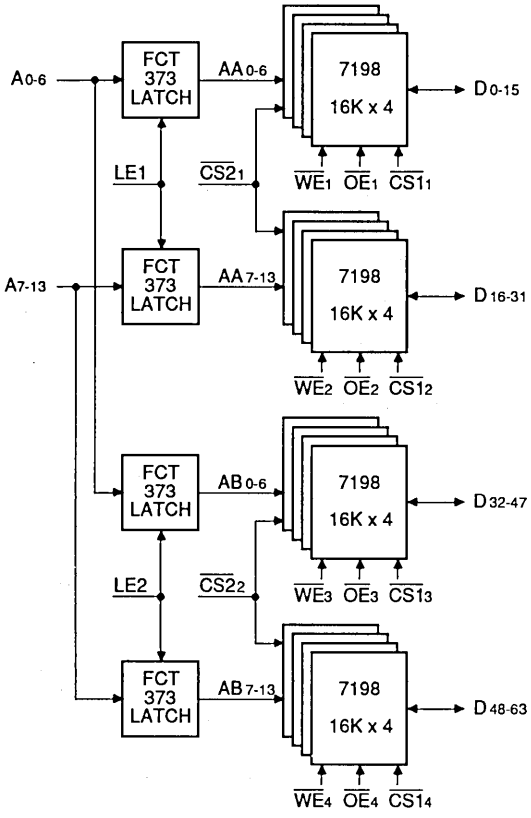
D_0 - D_{63}	Data Inputs/Outputs
A_0 - A_{13}	Address Inputs
LE_1 - LE_4	Latch Enables
$\overline{CS1}_1$ - $\overline{CS1}_8$	RAM Selects
$\overline{CS2}_1$ - $\overline{CS2}_4$	RAM Selects
$\overline{WE}_1$ - $\overline{WE}_8$	Write Enables
$\overline{OE}_1$ - $\overline{OE}_8$	Output Enables
GND	Ground
V_{CC}	Power

2743 tbl 01

NOTE:

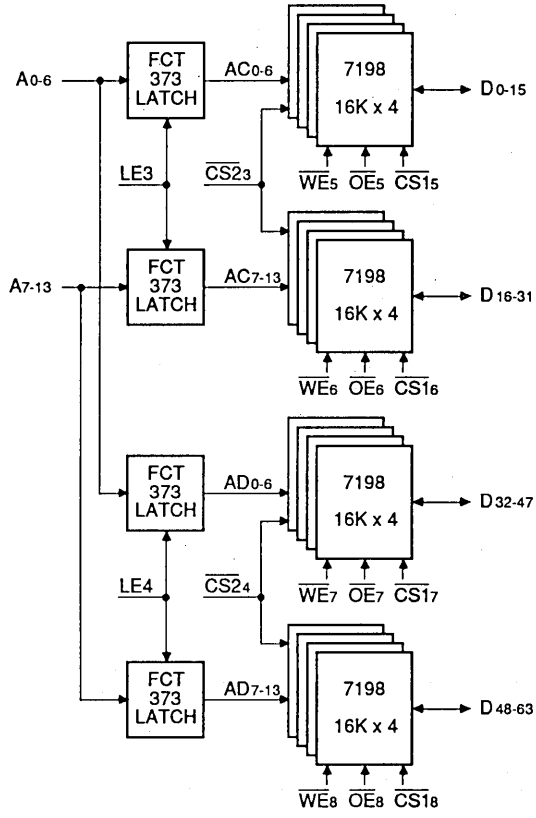
1. For module dimensions, please refer to module drawing M28 in the packaging section.

DATA CACHE



2743 drw 02

INSTRUCTION CACHE



2743 drw 03

8

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

2743 tbl 03

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2743 tbl 04

NOTE:
1. V_{IL}(min.) = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2743 tbl 05

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	12MHz		16.7MHz		20MHz		25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	20	—	20	—	20	—	20	—	20	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	—	10	—	10	—	10	—	10	µA
I_{CC1}	Operating Current	f = 0, $\overline{CS}$ = V_{IL}, V_{CC} = Max., Outputs Open	—	3000	—	3000	—	3000	—	3600	—	4000	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ = V_{IL}, f = f_{MAX} Outputs Open	—	3750	—	3750	—	4050	—	4500	—	4800	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} - 0.2V, V_{IN} ≥ V_{CC} - 0.2V or ≤ 0.2V	—	450	—	450	—	450	—	600	—	960	mA
I_{SB}	Standby Power Supply Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, f = f_{MAX} Outputs Open	—	1500	—	1500	—	1650	—	1800	—	2000	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –4mA	2.4	—	2.4	—	2.4	—	2.4	—	2.4	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	V

2743 tbl 06

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2743 tbl 02

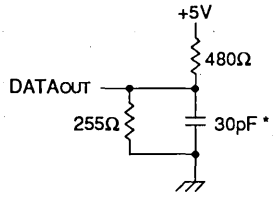
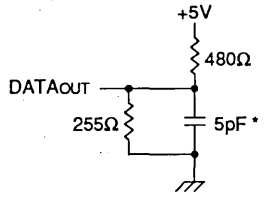


Figure 1. Output Load



2743 drw 04

Figure 2. Output Load (for tOLZ, tOHZ)

* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

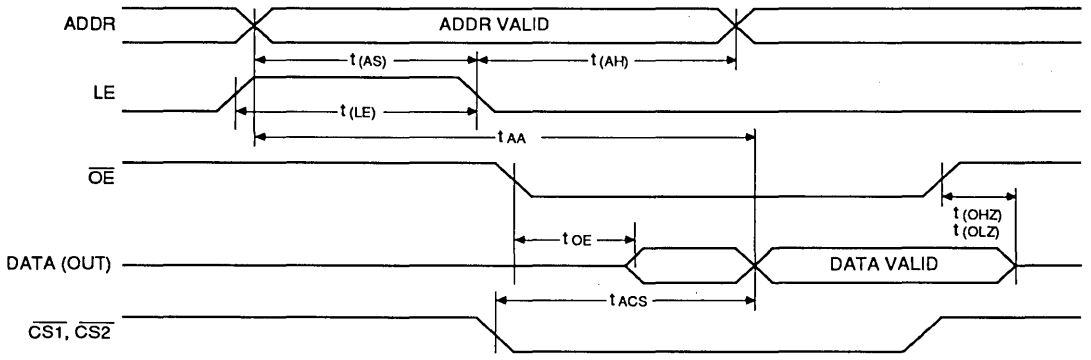
(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	12MHz Min.	12MHz Max.	16.6MHz Min.	16.6MHz Max.	20MHz Min.	20MHz Max.	25MHz Min.	25MHz Max.	33MHz Min.	33MHz Max.	Unit
Read Cycle												
tLE	Latch Enable Width	8	—	6	—	6	—	6	—	6	—	ns
tAS	Address Setup Time to LE	4	—	2	—	2	—	2	—	2	—	ns
tAH	Address Hold Time from LE	3	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tAA(2)	Address Access Time	—	45	—	35	—	30	—	25	—	20	ns
tACS	Chip Select Time	—	40	—	30	—	25	—	20	—	15	ns
tOE	Output Enable Time	—	22	—	17	—	11	—	8	—	5	ns
tOHZ(1)	Output Disable to Output in High Z	2	16	2	14	2	10	2	8	2	6	ns
tOLZ(1)	Output Disable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
Write Cycle												
tLE	Latch Enable Width	8	—	6	—	6	—	6	—	6	—	ns
tAS	Address Setup Time to LE	4	—	2	—	2	—	2	—	2	—	ns
tAH	Address Hold Time from LE	3	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tAW(2)	Address Valid to End of Write	40	—	30	—	25	—	23	—	20	—	ns
tCW	Chip Select to End of Write	35	—	25	—	20	—	18	—	15	—	ns
tWP	Write Pulse Width	30	—	25	—	20	—	17	—	12	—	ns
tDW	Data Valid to End of Write	20	—	13	—	13	—	11	—	8	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design but not tested.
2. LE already asserted.

8

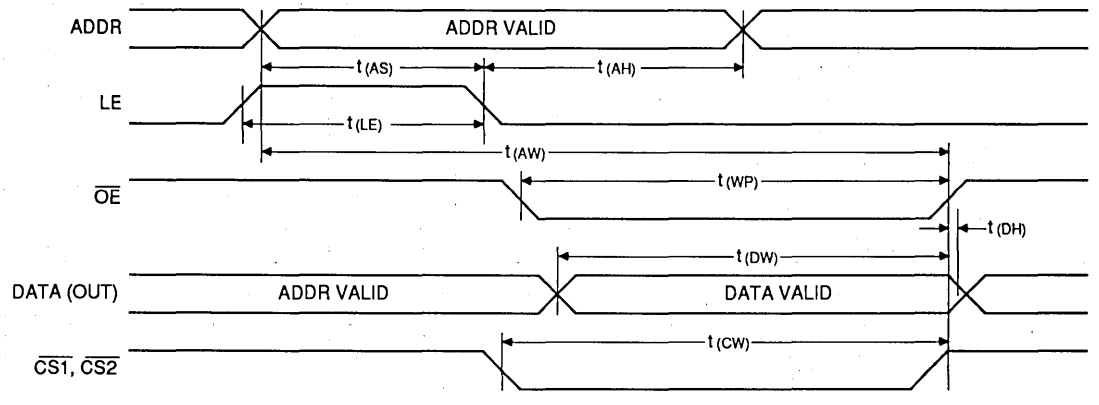
TIMING WAVEFORM OF READ CYCLE(1)



2743 drw 05

NOTES:
1. $\overline{WE}$ and $\overline{CS}$ must be High for all address transitions.
2. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE(1)



2743 drw 06

NOTE:
1. A write occurs (t_{WP}) during the overlap of a Low $\overline{CS}$ and $\overline{WE}$ and a High LE.

TRUTH TABLE

Mode	$\overline{CS1}$	$\overline{CS2}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	X	High Z	Standby
Standby	X	H	X	X	High Z	Standby
Read	L	L	L	H	DOUT	Active
Read	L	L	H	H	High Z	Active
Write	L	L	X	L	DIN	Active

2743 tbl 09

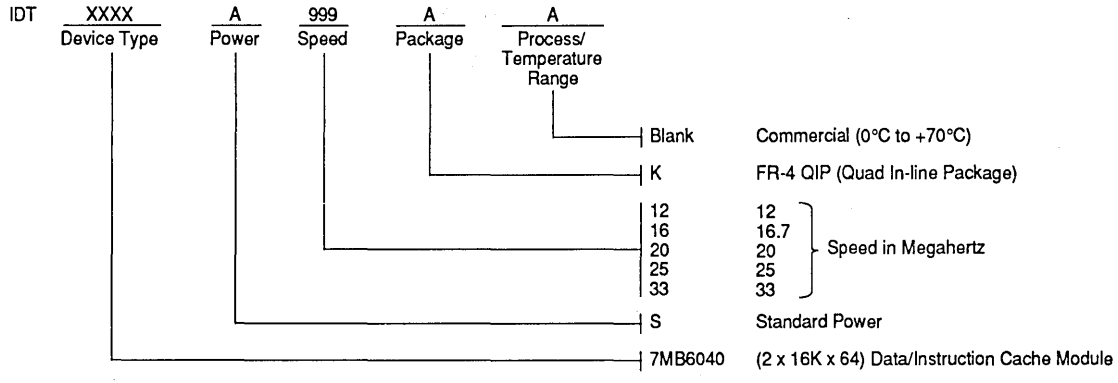
CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	60	pF
COUT	Output Capacitance	VOUT = 0V	20	pF

2743 tbl 10

NOTE:
1. This parameter is guaranteed by design but not tested.

ORDERING INFORMATION



2743 drw 7

8

Integrated Device Technology, Inc.

2 x 16K x 60 DATA/INSTRUCTION WITH RESETTABLE TAG/VALID CACHE MODULE FOR IDT79R3000 CPU (MULTIPROCESSOR)

IDT7MB6061

FEATURES:

- High-speed 240K-Byte CMOS static RAM module constructed to support the IDT79R3000 CPU, in a multiprocessor system as a complete data and instruction cache
- Additional data and instruction address invalidation latches on-board to facilitate use in a multi-processor system
- $\overline{\text{RESET}}$ pin invalidates instruction cache in one operation
- Operating frequencies to support 12MHz, 16.7MHz, 20MHz, 25MHz and 33MHz IDT79R3000
- Available in a high density, low profile 120-pin QIP (Quad In-Line Package)
- Surface mounted SOs on a multilayer epoxy substrate
- Multiple ground pins for maximum noise immunity
- TTL compatible I/Os
- Single 5V (±10%) power supply

PIN CONFIGURATION

GND	1	61	GND	GND	120	60	V_{CC}
D_0	2	62	D_1	D_{58}	119	59	D_{59}
D_2	3	63	D_3	D_{56}	118	58	D_{57}
D_4	4	64	D_5	D_{54}	117	57	D_{55}
D_6	5	65	D_7	D_{52}	116	56	D_{53}
$\overline{WE_1}$	6	66	$\overline{OE_1}$	$\overline{WE_4}$	115	55	$\overline{OE_4}$
$\overline{CS_1}$	7	67	V_{CC}	GND	114	54	GND
D_8	8	68	D_9	D_{50}	113	53	D_{51}
D_{10}	9	69	D_{11}	D_{48}	112	52	D_{49}
$P1A_0$	10	70	$P1A_1$	$P2A_0$	111	51	$P2A_1$
$P1A_2$	11	71	$P1A_3$	$P2A_2$	110	50	$P2A_3$
$P1A_4$	12	72	$P1A_5$	$P2A_4$	109	49	$P2A_5$
P1LE1	13	73	P1LE2	P2LE1	108	48	GND
$P1A_6$	14	74	$P1A_7$	$P2A_6$	107	47	$P2A_7$
$P1A_8$	15	75	$P1A_9$	$P2A_8$	106	46	$P2A_9$
$P1A_{10}$	16	76	$P1A_{11}$	$P2A_{10}$	105	45	$P2A_{11}$
$P1A_{12}$	17	77	$P1A_{13}$	$P2A_{12}$	104	44	$P2A_{13}$
$\overline{P1OE_1}$	18	78	GND	$\overline{P21OE_1}$	103	43	$\overline{RESET}$
D_{12}	19	79	D_{13}	D_{46}	102	42	D_{47}
D_{14}	20	80	D_{15}	D_{44}	101	41	D_{45}
D_{16}	21	81	D_{17}	D_{42}	100	40	D_{43}
D_{18}	22	82	D_{19}	D_{40}	99	39	D_{41}
$\overline{WE_2}$	23	83	$\overline{OE_2}$	$\overline{WE_3}$	98	38	$\overline{OE_3}$
GND	24	84	GND	V_{CC}	97	37	$\overline{CS_2}$
D_{20}	25	85	D_{21}	D_{38}	96	36	D_{39}
D_{22}	26	86	D_{23}	D_{36}	95	35	D_{37}
D_{24}	27	87	D_{25}	D_{34}	94	34	D_{35}
D_{26}	28	88	D_{27}	D_{32}	93	33	D_{33}
D_{28}	29	89	D_{29}	D_{30}	92	32	D_{31}
V_{CC}	30	90	V_{CC}	V_{CC}	91	31	GND

QIP
TOP VIEW

2755 drw 02

DESCRIPTION:

The IDT7MB6061 is a 240K-byte high-speed CMOS static RAM cache module constructed on a multilayer epoxy substrate (FR-4). The data cache uses the IDT6198 (16K x 4) SRAMs while the instruction cache uses both the IDT6198 and the IDT6178 (4K x 4) Resettable SRAMs; both cache sharing the 60-bit data bus.

Both cache also have a set of IDT74FCT373 latches to interface with the address bus. The data cache has an additional set of latches so each processor within the multiprocessor system has the ability to invalidate the data cache.

The instruction cache uses the IDT6178 (4K x 4) Cache Tag SRAMs for D_{36}-D_{59}. These bits cover the Tag and Valid bit fields. Address bits A_2-A_{13} are used for this portion of the instruction cache (i.e. there are four words per line in this cache). Asserting $\overline{RESET}$ will clear D_{36}-D_{59} to zeros in a single operation.

All inputs and outputs of the IDT7MB6061 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, reqiring no clocks or refreshing for operation.

PIN NAMES

D_0–D_{59}	Data Inputs/Outputs
$P1A_0$–$P1A_{11}$	Address Inputs
$P2A_0$–$P2A_{11}$	Invalidate Address
$P1LE_1$	Data Address Latch Enable
$P1LE_2$	Instruction Address Latch Enable
$\overline{P1OE}$	Data Address Enable
$\overline{P2OE}$	Instruction Address Enable
P2LE	Invalidate Data Address Latch Enable
$\overline{RESET_1}$	Data Cache Reset
$\overline{RESET_2}$	Instruction Cache Reset
$\overline{WE_1}$–$\overline{WE_4}$	Write Enables
$\overline{OE_1}$–$\overline{OE_4}$	Output Enables
GND	Ground
V_{CC}	Power Supply

2755 bl 01

NOTE:

1. For module dimensions, please refer to drawing M27 in the packaging section.

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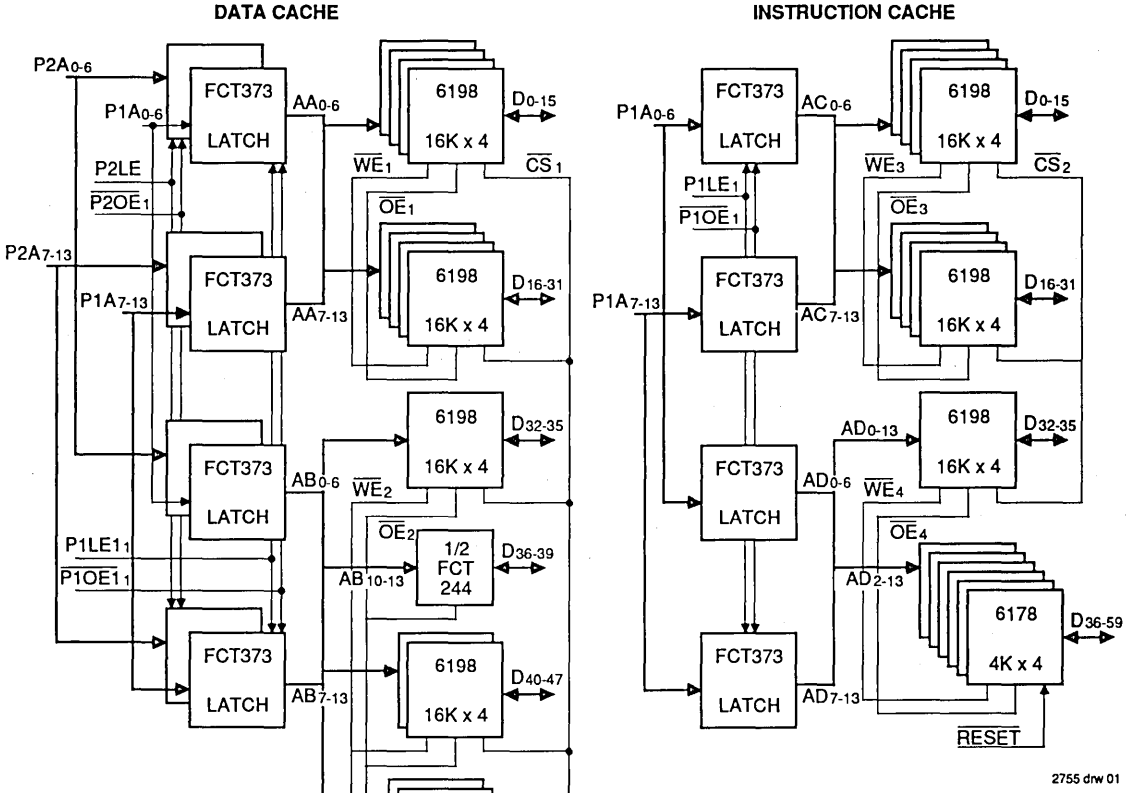
FUNCTIONAL BLOCK DIAGRAM



8

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2755 tbl 04

1. V_{IL} = -3.0V for pulse width less than 20ns.

CAPACITANCE

Symbol	Parameter[1]	Conditions	Typ.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	V_{IN} = 0V	20	pF
$C_{IN(A)}$	Input Capacitance (Address)	V_{IN} = 0V	40	pF
$C_{IN(C)}$	Input Capacitance ($\overline{OE}$, $\overline{WE}$)	V_{IN} = 0V	50	pF
$C_{IN(C)}$	Input Capacitance ($\overline{CS}$)	V_{IN} = 0V	100	pF
$C_{IN(C)}$	Input Capacitance (LE, $\overline{PxOE}$)	V_{IN} = 0V	30	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	20	pF

NOTE: 2755 tbl 03

1. This parameter is guaranteed by design, but not tested.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2755 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%

2755 tbl 05

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2755 tbl 06

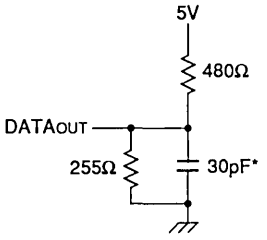
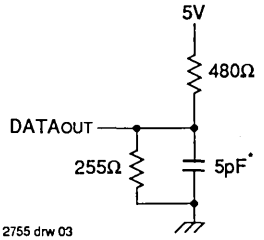


Figure 1. Output Load



2755 drw 03

Figure 2. Output Load (for t_{OLZ} and t_{OHZ})

* Including scope and jig.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	12MHz		16.7MHz		20MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	20	—	20	—	20	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	—	10	—	10	µA
I_{CC1}	Operating Current	f = 0, $\overline{CS}$ = V_{IL}; V_{CC} = Max., Outputs Open	—	2925	—	2925	—	2925	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ = V_{IL}; f = f_{MAX}, Outputs Open	—	3850	—	3900	—	4150	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} - 0.2V, V_{IN} ≥ V_{CC} - 0.2V or ≤ 0.2V	—	450	—	450	—	450	mA
I_{SB}	Standby Power Supply Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}; f = f_{MAX}, Outputs Open	—	1300	—	1425	—	1575	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	—	2.4	—	2.4	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	—	0.4	—	0.4	V

NOTE:
1. I_{CC1}, I_{CC2} in the case for all devices selected (i.e. both instruction and data cache selected).

2755 tbl 07

DC ELECTRICAL CHARACTERISTICS (Continued)

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	20	—	20	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	—	10	µA
I_{CC1}	Operating Current	f = 0, $\overline{CS}$ = V_{IL}; V_{CC} = Max., Outputs Open	—	3400	—	3700	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ = V_{IL}; f = f_{MAX}, Outputs Open	—	4675	—	4900	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} - 0.2V, V_{IN} ≥ V_{CC} - 0.2V or ≤ 0.2V	—	600	—	960	mA
I_{SB}	Standby Power Supply Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}; f = f_{MAX}, Outputs Open	—	1700	—	2000	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	—	2.4	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	—	0.4	V

NOTE:
1. I_{CC1}, I_{CC2} in the case for all devices selected (i.e. both instruction and data cache selected).

2755 tbl 08

8

AC ELECTRICAL CHARACTERISTICS

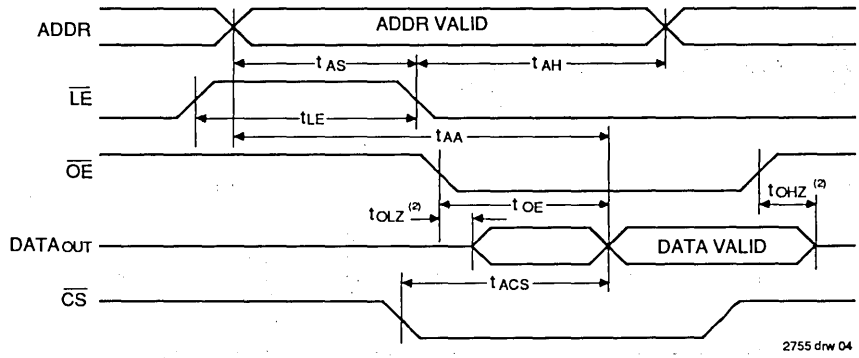
(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	12MHz		16.7MHz		20MHz		25MHz		33MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{LE}	Latch Enable Width	6	—	6	—	6	—	6	—	6	—	ns
t_{AS}	Address Setup Time to LE	2	—	2	—	2	—	2	—	2	—	ns
t_{AH}	Address Hold Time from LE	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{AA}[2]	Address Access Time	—	45	—	35	—	30	—	25	—	20	ns
t_{ACS}	Chip Select Time	—	40	—	30	—	25	—	20	—	15	ns
t_{OE}[3]	Output Enable to Output Valid	—	22	—	17	—	11	—	8	—	5	ns
t_{OHZ}[1]	Output Disable to Output in High Z	2	16	2	14	2	10	2	8	2	6	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
WRITE CYCLE												
t_{LE}	Latch Enable Width	6	—	6	—	6	—	6	—	6	—	ns
t_{AS}	Address Setup Time to LE	2	—	2	—	2	—	2	—	2	—	ns
t_{AH}	Address Hold Time to LE	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{AW}[2]	Address Valid to End of Write	40	—	30	—	25	—	23	—	20	—	ns
t_{CW}	Chip Select to End of Write	35	—	25	—	20	—	18	—	15	—	ns
t_{WP}	Write Pulse Width	30	—	25	—	20	—	17	—	12	—	ns
t_{DW}	Data Valid to End of Write	20	—	13	—	13	—	11	—	8	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{LOE}[4]	Latch Output Enable	—	7	—	7	—	7	—	7	—	7	ns
RESET CYCLE												
t_{CLPW}	$\overline{RESET}$ Pulse Width	40	—	40	—	30	—	30	—	25	—	ns
t_{CLRC}	$\overline{RESET}$ High to $\overline{WE_4}$ Low	5	—	5	—	5	—	5	—	5	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.
2. LE asserted.
3. $\overline{OE_1}$, $\overline{OE_2}$, $\overline{OE_3}$, $\overline{OE_4}$.
4. P1OE1 and P2OE1.

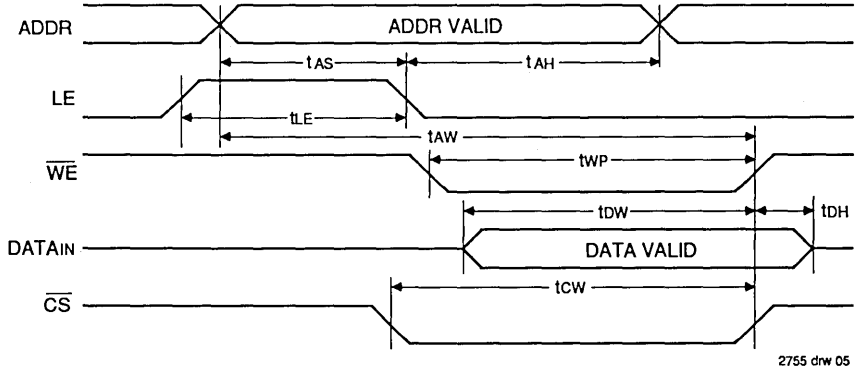
2755 tbl 09

TIMING WAVEFORM OF READ CYCLE(1)

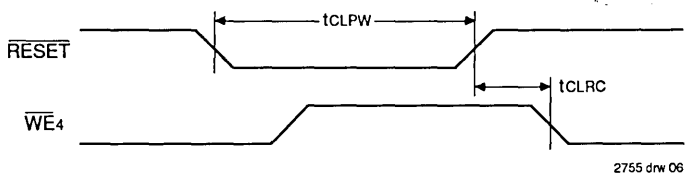


NOTE:
1. Assume $\overline{WE}$ is active high throughout this cycle.
2. This parameter is guaranteed by design but not tested.

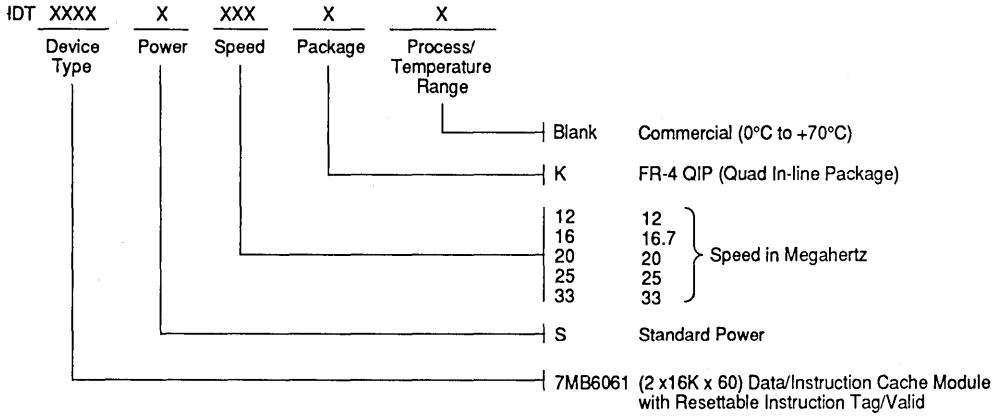
TIMING WAVEFORM OF WRITE CYCLE



TIMING WAVEFORM OF $\overline{RESET}$ CYCLE



ORDERING INFORMATION



2755 drw 08

Integrated Device Technology, Inc.

16K x 32 WRITABLE CONTROL STORE STATIC RAM MODULE

IDT7M6032

FEATURES:

- 16K x 32 high-performance Writable Control Store (WCS)
- Serial Protocol Channel (SPC™)—reading, writing and interrogation
- 4 byte/wide output enables
- Separate chip select, write enable and output enable memory controls
- High fanout pipeline register
- Fully width expandable
- Compact 64-pin ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

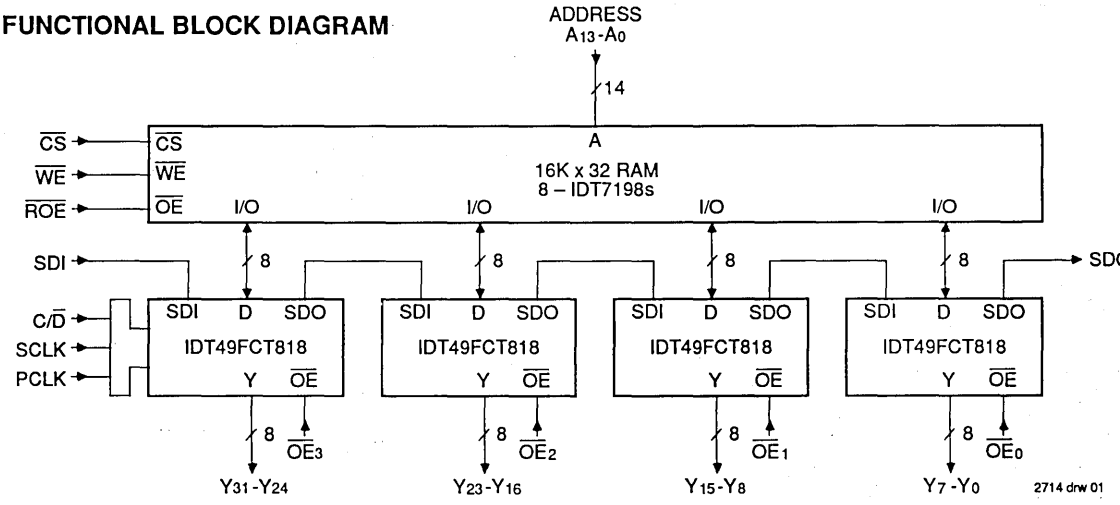
The IDT7M6032 is a 16K x 32-bit Writable Control Store (WCS) RAM and pipeline register. It features eight IDT7198 16K x 4 high performance static RAMs and four IDT49FCT818 Serial Protocol Channel (SPC) registers. These devices are arranged to form the 16K x 32 Writable Control Store RAM with Serial Protorol Channel for loading of the memory. The address lines, chip select, write enable and output enable of the RAMs are all bused together to form one large 16K x 32 memory. Each eight Data I/Os of the RAM are connected to the D inputs of an IDT49FCT818. The device has the serial data-in and serial data-out bits connected to form a 32-bit Serial Protocol Channel register. The module features four separate output enables, one for each of the IDT49FCT818 registers. Thus, the Y outputs from the IDT49FCT818 registers may be enabled or put into the high-impedance state on individual 8-bit boundaries. The Command/Data (C/D), Serial Shift Clock (SCLK) and Parallel Clock (PCLK) are all bus organized across the four IDT49FCT818 registers. The thirty-two register output bits, eight from each device, are separately brought out to form a 32-bit wide pipeline register on the Writable Control Store.

In normal operation, data from the 32-bit wide memory is loaded into the IDT49FCT818 registers on the low-to-high transition of PCLK. Reading and writing of the memory by means of the Serial Protocol Channel is performed using the IDT49FCT818. That is, the data to be loaded can be shifted in the serial data input by using the SCLK and a load command executed by shifting the proper command word in the serial data input when the C/$\overline{D}$ line is in the command mode. This command will then be executed by manipulating the C/$\overline{D}$ line and SCLK line. Data is then written into the RAM by bringing the write enable line on the RAM memory from the high state to the low state and back to the high state.

The IDT7M6032 is offered in a compact 64-pin 600 mil wide ceramic dual in-line module. It is constructed using ceramic LCC components on a multilayer co-fired ceramic substrate and occupies less than 2 square inches of board space.

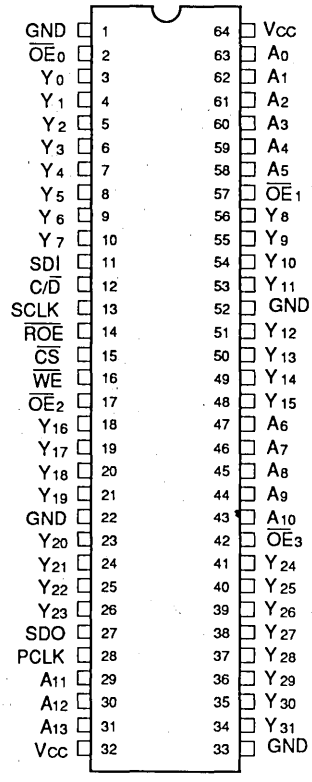
The semiconductor components used on all IDT military modules are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



CEMOS and SPC are trademarks of Integrated Device Technology Inc.

PIN CONFIGURATION[1]



DIP
TOP VIEW

2714 drw 02

NOTE:
1. For module dimensions, please refer to module drawing M17 in the packaging section.

PIN NAMES

Pin Name	I/O	Description
PCLK	I	Parallel Data Register Clock
Y0-31	O	Parallel Data Register Output Pins (Y0 = LSB, Y31 = MSB)
$\overline{OE}_Y$	I	Output Enable for Y Bus (Overidden by SPC Inst. 8 &14)
SDI	I	Serial Data In for SPC Operation. Data and command shifts in the Least Significant Bit first
SDO	O	Serial Data Out for SPC Operation. Data and command shifts out the Least Significant Bit first
C/$\overline{D}$	I	Mode Control for SPC
SCLK	I	Serial Shift Clock for SPC Operations
$\overline{CS}$	I	RAM Chip Select
$\overline{WE}$	I	RAM Write Enable
A0-13	I	Address Bus Pins
$\overline{ROE}$	I	Internal RAM Ouput Enable for D bus

2714 tbl 01

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating[1]	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2714 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	H	X	High-Z	Standby
Standby	H	L	X	DOUT	Standby
Read	L	L	H	DOUT	Active
Read	L	H	H	High-Z	Active
Write	L	SPC[1]	L	SPC[1]	Active

NOTE: 2714 tbl 02
1. See SPC Commands for proper execution of write cycle.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	15	pF
CIN(C)	Input Capacitance Address and Control	VIN = 0V	60	pF
COUT	Output Capacitance	VOUT = 0V	10	pF

NOTE: 2714 tbl 04
1. This parameter is guaranteed by design, but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2714 tbl 05
1. V_{IL} = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%
Military	-55°C to +125°C	0V	5V ±10%

2714 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameter	Test Conditions	25ns		30ns		35ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Data Bus µA	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	20	—	20	—	20	µA
$\|I_{LO}\|$	Output Leakage µA	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	20	—	20	—	20	µA
I_{CC1}	Operating Current mA	f = 0, $\overline{CS} \leq V_{IL}$, V_{CC} = Max.; Outputs Open	—	900	—	800	—	800	mA
I_{CC2}	Dynamic Operating Current mA	V_{CC} = Max., $\overline{CS} \leq V_{IL}$; f = f_{MAX}; Outputs Open	—	1200	—	1150	—	1050	mA
I_{SB}	Standby Supply Current mA	$\overline{CS} \geq V_{IH}$, f = f_{MAX}, Outputs Open	—	450	—	450	—	450	mA
I_{SB1}	Full Standby Supply Current mA	$\overline{CS} \geq V_{CC}$ - 0.2V, $V_{IN} \geq V_{CC}$ - 0.2V or ≤ 0.2V	—	125	—	125	—	125	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -15mA	2.4	—	2.4	—	2.4	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 32mA	—	0.4	—	0.4	—	0.4	V

2714 tbl 07

DC ELECTRICAL CHARACTERISTICS (Continued)

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameter	Test Conditions	45ns		55ns		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Data Bus µA	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	20	—	20	µA
$\|I_{LO}\|$	Output Leakage µA	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	20	—	20	µA
I_{CC1}	Operating Current mA	f = 0, $\overline{CS} \leq V_{IL}$, V_{CC} = Max.; Outputs Open	—	800	—	800	mA
I_{CC2}	Dynamic Operating Current mA	V_{CC} = Max., $\overline{CS} \leq V_{IL}$; f = f_{MAX}; Outputs Open	—	1050	—	1050	mA
I_{SB}	Standby Supply Current mA	$\overline{CS} \geq V_{IH}$, f = f_{MAX}, Outputs Open	—	450	—	450	mA
I_{SB1}	Full Standby Supply Current mA	$\overline{CS} \geq V_{CC}$ - 0.2V, $V_{IN} \geq V_{CC}$ - 0.2V or ≤ 0.2V	—	125	—	125	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -15mA	2.4	—	2.4	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 32mA	—	0.4	—	0.4	V

2714 tbl 08

8

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2714 drw 12

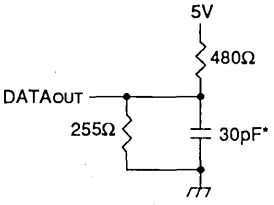
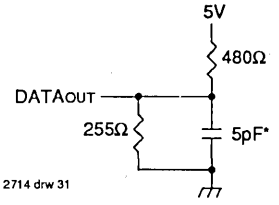


Figure 1. Output Load



2714 drw 31

Figure 2. Output Load
(for tOLZ, tCHZ, tOHZ, tWHZ, and tOW)

* Including scope and jig

AC ELECTRICAL CHARACTERISTICS

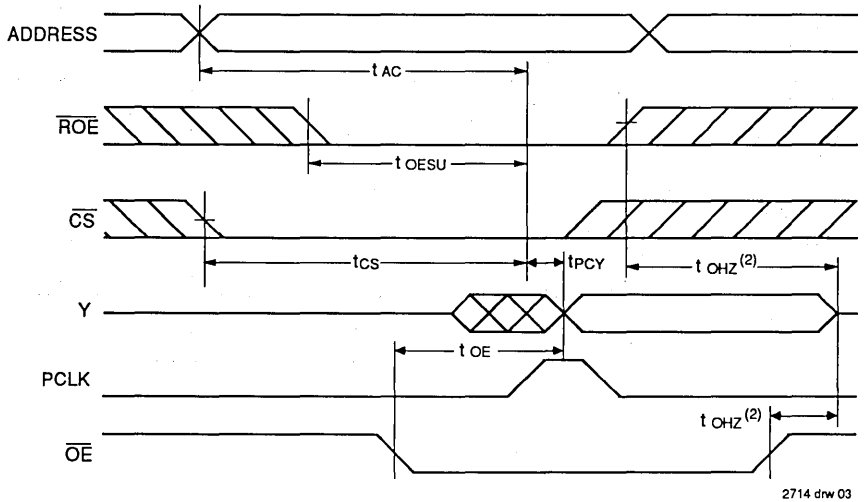
(VCC = 5V ± 10%, TA = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameter	25ns		30ns		35ns		45ns		55ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
tAC	Address Valid to PCLK	25	—	30	—	35	—	45	—	55	—	ns
tCS	$\overline{CS}$ Valid to PCLK	25	—	30	—	35	—	45	—	55	—	ns
tOESU	$\overline{ROE}$ Valid to PCLK Set Up	15	—	20	—	25	—	30	—	35	—	ns
tPCY	$\overline{PCLK}$ to Output Valid	—	13	—	13	—	16	—	16	—	16	ns
tOE	$\overline{OE}$ Valid to Output Valid	2	13	2	13	2	16	2	16	2	16	ns
tOHZ(1)	$\overline{OE}$ Negated to Output in High Z	2	12	2	12	2	12	2	12	2	12	ns
Write Cycle												
tAW	Address Valid to End of Write	20	—	25	—	30	—	35	—	45	—	ns
tCW	$\overline{CS}$ Valid to End of Write	20	—	25	—	30	—	35	—	45	—	ns
tWP	Write Enable Pulse Width	18	—	23	—	28	—	30	—	40	—	ns
tWCD	Cont/Dat to End of Write	22	—	25	—	28	—	30	—	35	—	ns
tAS	Address Setup Time	2	—	2	—	2	—	2	—	2	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

2714 tbl 09

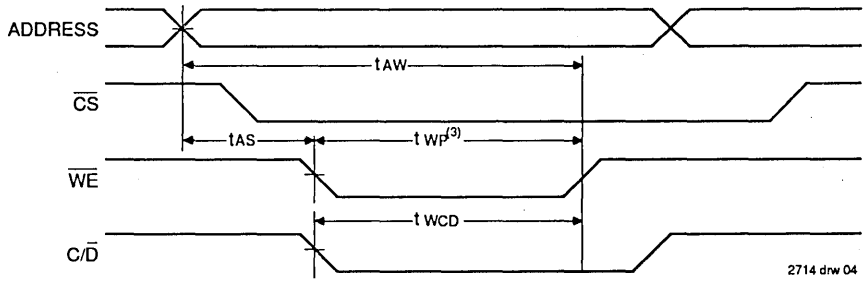
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



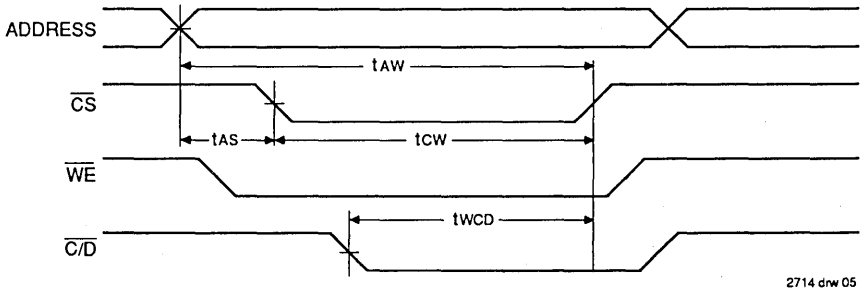
2714 drw 03

NOTES:
1. $\overline{WE}$ is high for Read Cycle.
2. Transition is measured ±200mV from steady state. This parameter guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 4)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 4)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
4. $\overline{ROE}$ = VIH.

8

AC ELECTRICAL CHARACTERISTICS (SPC TIMING)

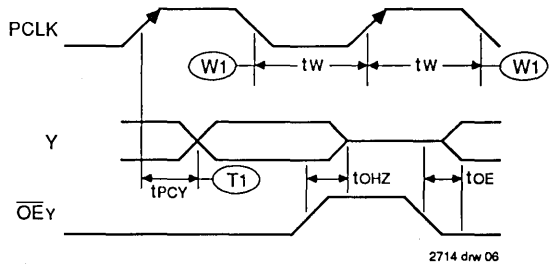
(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

Symbol		Parameter	25ns		30ns		35ns		45ns		55ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}	T2	SCLK High to SDO	—	15	—	15	—	22	—	22	—	22	ns
t_{PHL}	T3	SDI to SDO (Stub Mode)	—	45	—	45	—	45	—	45	—	45	ns
	T4	C/$\overline{D}$ Low to Y	—	15	—	15	—	20	—	20	—	20	ns
	T5	SCLK High to Y	—	15	—	15	—	25	—	25	—	25	ns
	T6	C/$\overline{D}$ Low to SDO	—	15	—	15	—	25	—	25	—	25	ns
t_{SU}	S2	C/$\overline{D}$ to SCLK High	15	—	15	—	15	—	15	—	15	—	ns
	S3	SDI to SCLK High	8	—	8	—	8	—	8	—	8	—	ns
	S4	Y or D to C/$\overline{D}$ Low	5	—	5	—	5	—	5	—	5	—	ns
	S5	C/$\overline{D}$ to PCLK High	12	—	12	—	12	—	12	—	12	—	ns
t_H	S6	Y to PCLK High	5	—	5	—	5	—	5	—	5	—	ns
	H2	C/$\overline{D}$ from SCLK Low	12	—	12	—	12	—	12	—	12	—	ns
	H3	SDI from SCLK High	2	—	2	—	2	—	2	—	2	—	ns
	H4	Y or D from C/$\overline{D}$ Low	2	—	2	—	2	—	2	—	2	—	ns
	H5	SCLK High from PCLK High	2	—	2	—	2	—	2	—	2	—	ns
	H6	C/$\overline{D}$ from PCLK High	2	—	2	—	2	—	2	—	2	—	ns
	H7	Y from PCLK High	3	—	3	—	3	—	3	—	3	—	ns
t_{HZ}[1,2]	2z,4z	SCLK High to D or Y High Z	—	15	—	15	—	20	—	20	—	20	ns
t_{LZ}[1,2]	3z,5z	C/$\overline{D}$ High to D or Y High Z	—	15	—	15	—	20	—	20	—	20	ns
t_{ZHL}[1,2]	Z2,Z3	C/$\overline{D}$ Low to D or Y Valid 22, 23	—	15	—	15	—	20	—	20	—	20	ns
t_W	W1	PCLK (High & Low)	10	—	10	—	15	—	15	—	15	—	ns
	W2	SCLK (High & Low)	30	—	30	—	35	—	35	—	35	—	ns
	W3	C/$\overline{D}$ High	30	—	30	—	35	—	35	—	35	—	ns

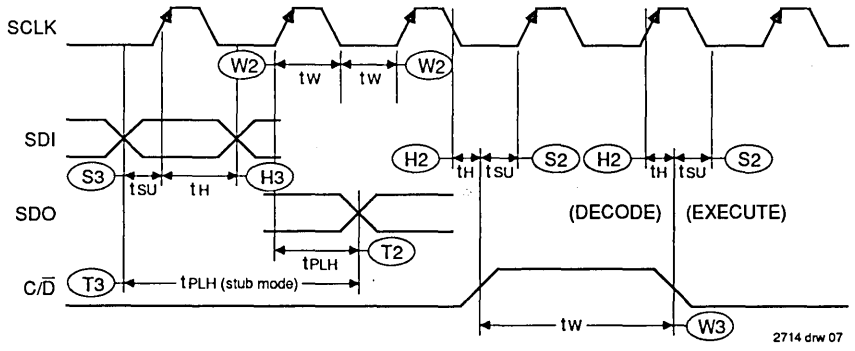
NOTE:
1. This parameter is guaranteed by design, but not tested.
2. OE = V_{IH}.

2714 tbl 10

GENERAL AC WAVEFORMS FOR PARALLEL INPUTS AND OUTPUTS



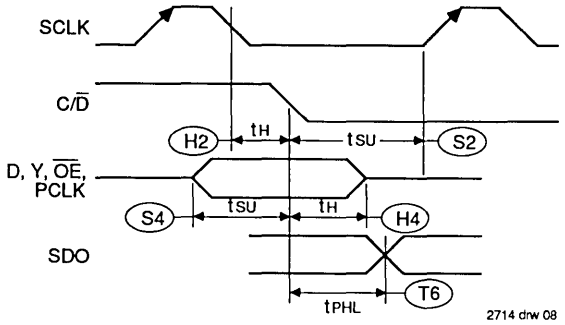
GENERAL AC WAVEFORMS FOR SERIAL PROTOCOL INPUTS AND OUTPUTS



8

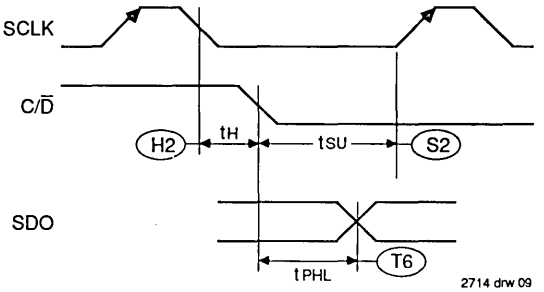
DETAILED WAVEFORMS OF SERIAL PROTOCOL OPERATIONS

Y ⟶ SPC Data (Inst. 0)
D ⟶ SPC Data (Inst. 2)
Status ⟶ SPC Data (Inst. 4)



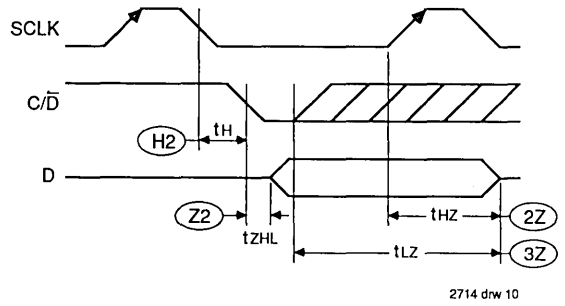
2714 drw 08

PARALLEL DATA REGISTER ⟶ SPC Data (Inst.1)
SET SERIAL MODE (Inst. 11)
SET STUB MODE (Inst. 12)



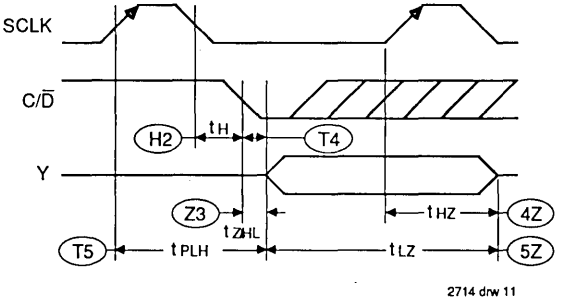
2714 drw 09

CONNECT TO D (Inst. 5)
SPC Data ⟶ D (Inst. 9)



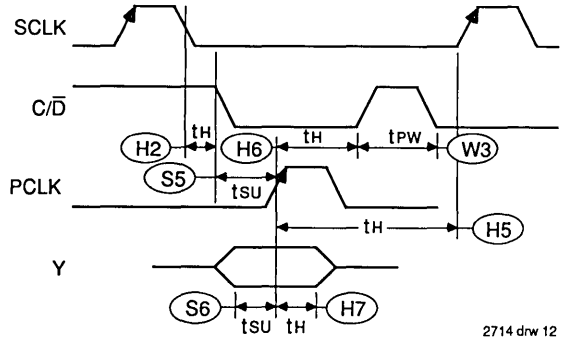
2714 drw 10

SPC Data ⟶ PARALLEL DATA REGISTER (Inst. 10)
SPC Data ⟶ Y (Inst. 8)
CONNECT TO Y (Inst. 14)



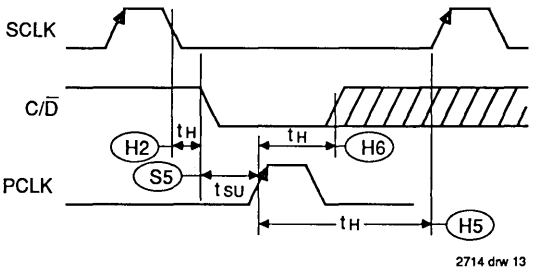
2714 drw 11

Y ⟶ SPC Data SYNCHRONOUS W/PCLK (Inst. 3)



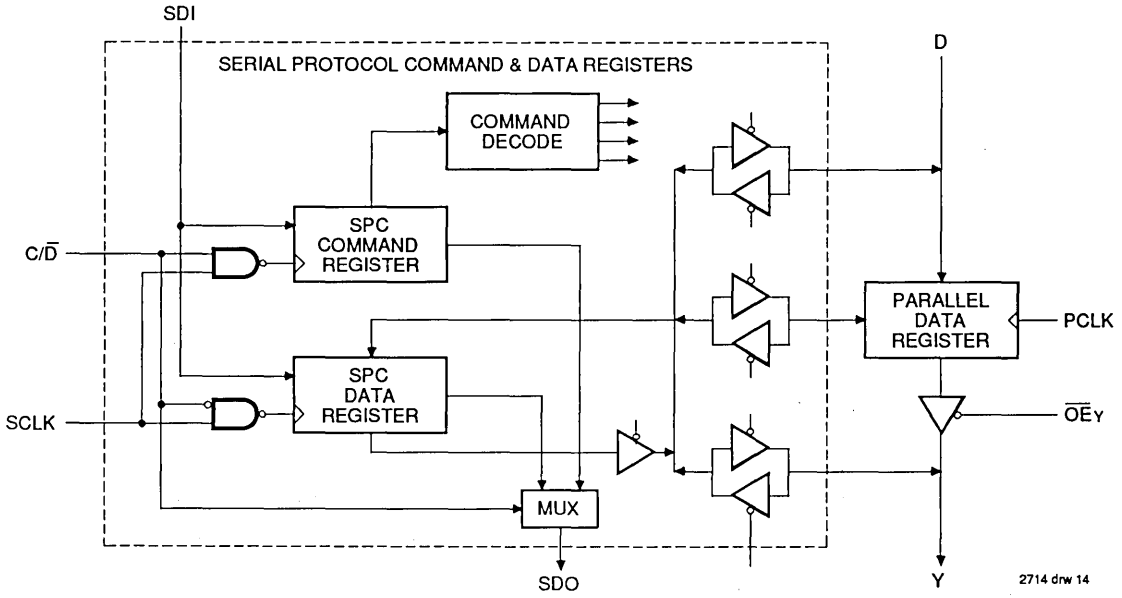
2714 drw 12

SCP Data ⟶ PARALLEL DATA REGISTER SYNCHRONOUS W/PCLK (Inst. 3)

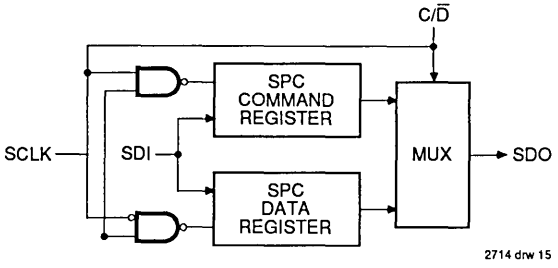


2714 drw 13

DETAILED FUNCTIONAL BLOCK DIAGRAM



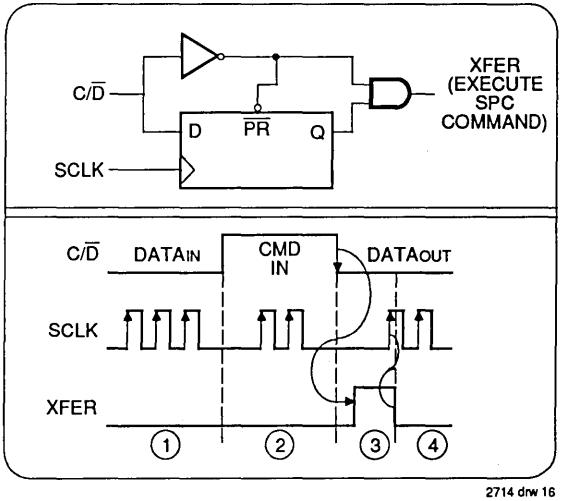
The detailed block diagram consists of two main elements: the parallel data register and the SPC data/command registers. T he main data path is from the D inputs down to the data register and through to the Y outputs. This path is typically used during standard operations. For diagnostic or systems initialization, the internal SPC data path is used. This path allows access between the SPC data and command registers and the standard data path, pins and data register. The SPC data and command registers are accessed via the SDI, SDO, C/D and SCLK pins.



SPC FUNCTIONAL DESCRIPTION

The Serial Protocol Channel (SPC) has been optimized for the minimum number of pins and the maximum flexibility. The data is passed in on a Serial Data Input pin (SDI) and out on a Serial Data Output pin (SDO) . The transfer of the data is controlled by a Serial Clock (SCLK) and a Command/Data mode input (C/D). These four pins are the basic SPC pins. To the outside, the SPC appears as two serial shift registers in parallel—one for command and the other data. The serial clock shifts data and the Command/Data (C/D) line selects which register is being shifted. The command register is used to control loading of data to and from the data register with other storage elements in the device.

With respect to executing an SPC command, there are four distinct phases: (1) data is shifted in, (2) followed by the command, (3) the command is executed, and (4) data is shifted out. During the data mode, data is simultaneously shifted into the serial data register while the data in the register is shifted out. During the command mode, opcode-type information is shifted through the serial ports. The command is executed when the last bit is shifted in and the C/D line is brought low. The execution phase is ended with the next serial clock edge.



SPC data and commands are shifted in through the SDI pin, which is a serial input pin, and out through the SDO pin, which is a serial output pin. Data and commands are shifted in Least Significant Bit first; Most Significant Bit last (Y_0 = LSB, Y_{15} = MSB). Execution of SPC commands is performed by stopping the shift clock SCLK, and lowering the C/$\overline{D}$ line from high-to-low. Later the SCLK may then be transitioned from low-to-high. SPC commands and data can be shifted anytime, without regard for operation. During the execution phase, care must be taken that there is no conflict between the SPC operation and parallel operation. This means that if the SPC operation attempts to load the parallel data register (opcode 10) while PCLK is in transition, the results are undefined. In general, it is required that the PCLK be static during SPC operations. The synchronous commands (opcode 3 and 13), however, allow the PCLK to run. In these operations, the high-to-low transition of the C/$\overline{D}$ line takes on the function of an arm signal in preparation for the next low-to-high transition of the PCLK.

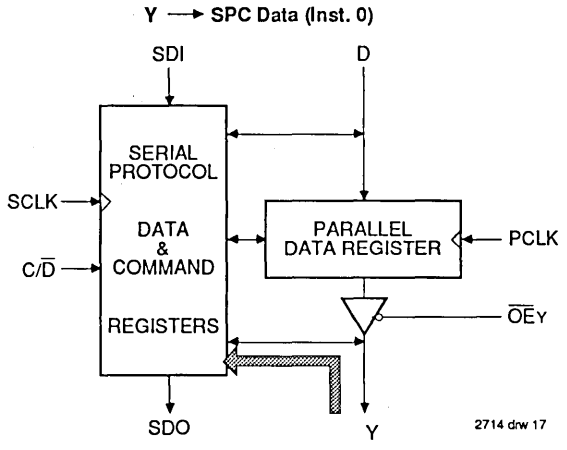
SPC COMMANDS

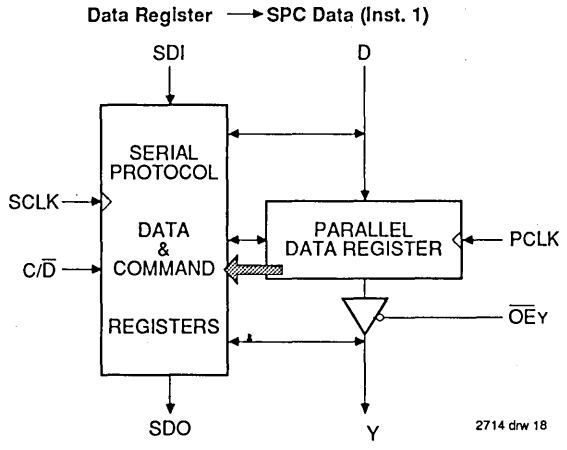
There are 16 possible SPC opcodes. Fourteen of these are utilized, the other two are reserved and perform NO-OP functions. The top eight opcodes, 0 through 7, are reserved for transferring data into the SPC data register for shifting out. The lower eight opcodes, 8 through 15, are used for transferring data from the SPC data register to other parts of the device. Two of the commands are also used for connecting the data in and out pins.

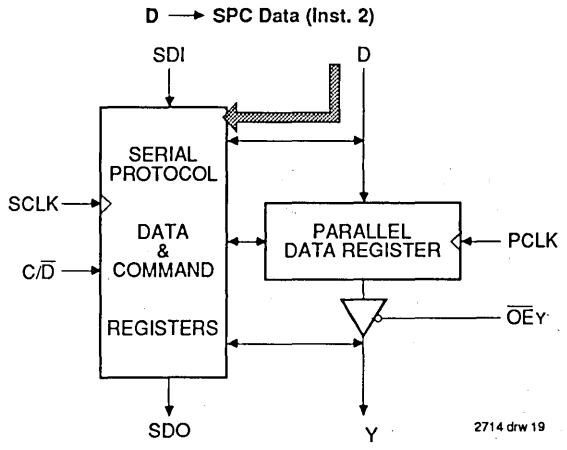
OPCODE	SPC COMMAND
0	Y to SPC Data Register
1	Parallel Data Register to SPC Data Register
2	D to SPC Data Register
3	Y to SPC Data Register Synchronous w/PCLK
4	Status ($\overline{OE}_Y$, PCLK) to SPC Data Register
5	Connect Y to D
6-7	Reserved (NO-OP)
8	SPC Data to Y ($\overline{OE}$ is overidden)
9	SPC Data to D
10	SPC Data to Parallel Data Register
11	Select Serial Mode
12	Select Stub Mode
13	SPC Data to Parallel Data Register Synchronous w/PCLK
14	Connect D to Y ($\overline{OE}$ is overidden)
15	NO-OP

2714 tbl 11

Opcode 0 is used for transferring data from the Y output pins into the SPC data register. Opcode 1 transfers data from the output of the register, before the tri-state gate, into the SPC data register. Opcode 2 transfers data from the D input pins into the SPC data register.

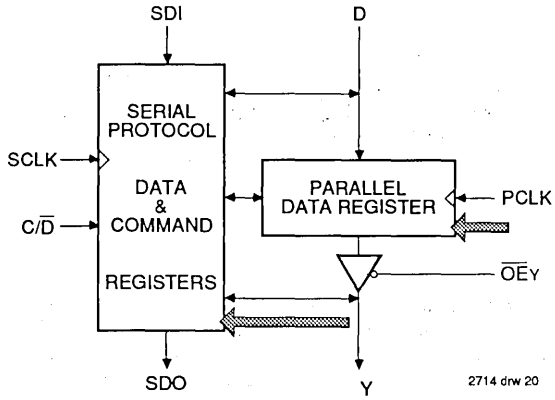




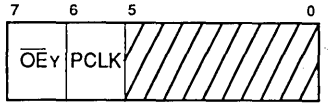


Opcode 3 transfers data on the Y pins to the SPC data register on the next PCLK, thus achieving a synchronous observation of the SPC data register in real time. This operation can be forced to repeat without shifting in a new command by pulsing C/$\overline{D}$ low-high-low after each PCLK. As soon as data is shifted out using SCLK, the command is terminated and must be loaded in again.

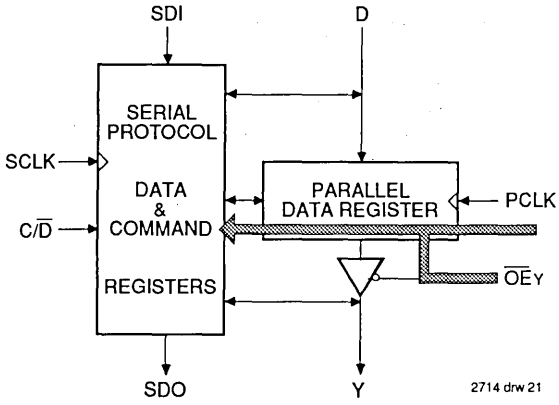
Y ⟶ SPC Data Synchronous w/PCLK (Inst. 3)



Opcode 4 is used for loading status into the SPC data register. The format of bits is shown below.

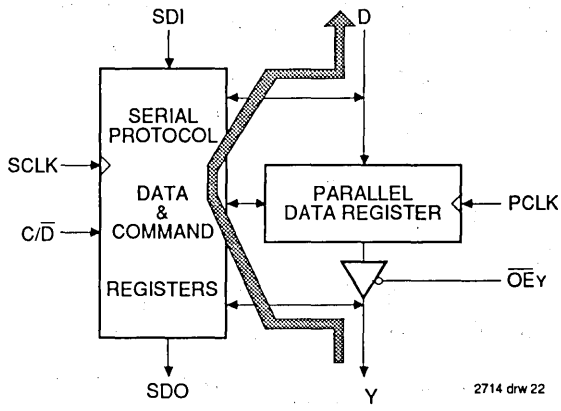


Status ⟶ SPC Data (Inst. 4)

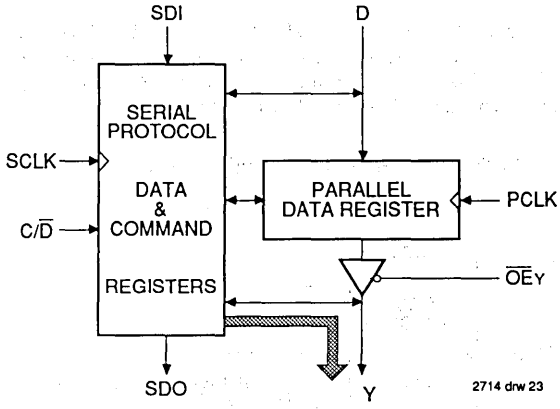


Opcode 5 connects Y to D. Opcodes 6 and 7 are reserved, hence designated NO-OP.

Connect Y to D (Inst. 5)



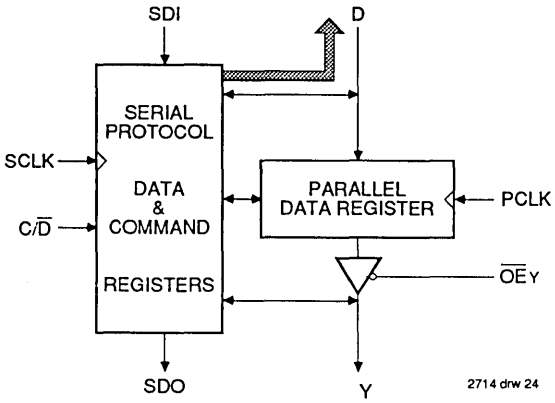
SPC Data ⟶ Y (Inst. 8)



8

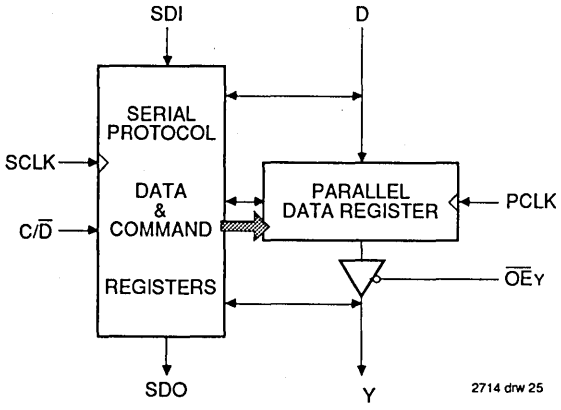
Opcode 8 is used for transferring SPC data directly to the Y pins. When executing opcode 8, the state of $\overline{OE}_Y$ is a "do not care"; that is, data will be output even if $\overline{OE}_Y$ = HIGH. Opcode 9 is used tor transferring SPC data to the D pins. Operands 8 and 9 can be temporarily suspended by raising the C/$\overline{D}$ input and resumed by lowering the C/$\overline{D}$. As soon as SCLK completes transition, the command is terminated.

SPC Data → D (Inst. 9)



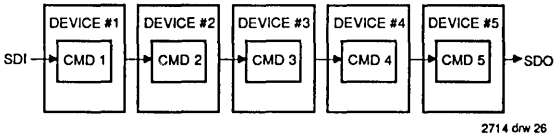
Opcode 10 is used tor transferring data from the SPC data register into the parallel data register, irrespective of the state of PCLK. However, PCLK must be static between C/$\overline{D}$ going high-to-low and SCLK going low-to-high.

SPC Data → Parallel Data Register (Inst. 10)



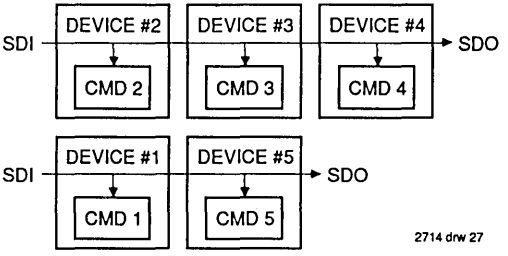
Opcodes 11 and 12 are used to set Serial and Stub Mode, respectively. After executing one of these opcodes, the device remains in this mode until programmed otherwise. The Serial mode is the default mode that the IDT49FCT818 powers up in. In Serial mode, commands are shifted through the SPC command register and then to the SDO pin. This is the typical mode used when several varieties of devices that utilize the SPC access method are employed on one serial ring.

SERIAL MODE



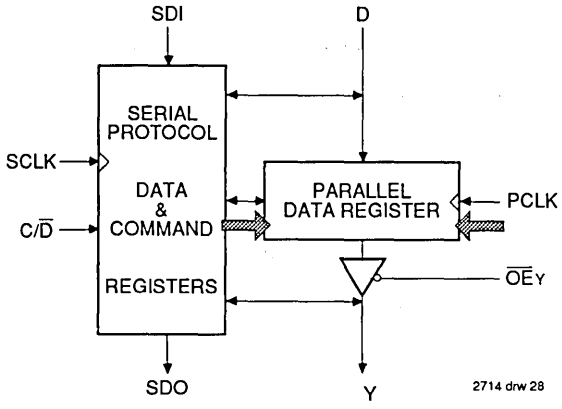
In Stub mode, SDI is connected directly to SDO. In this way, the same diagnostic command can be loaded into multiple devices of like type. For example, in four clock cycles the same command could be loaded into 8 IDT49FCT818s (64-bit pipeline register). Dissimilar devices must be segregated into serial scan loops of similar type, as shown below. During the command phase, the serial shift clock must be slowed down to accommodate the delay from SDI to SDO through all of the devices. The slower clock is typically a small tradeoff compared to the reduced number of clock cycles.

STUB MODE

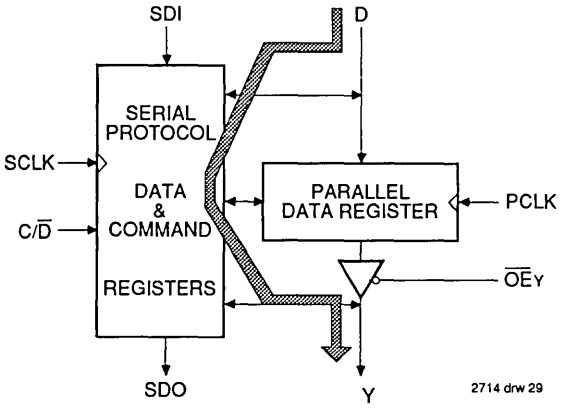


Opcode 13 transfers data from the SPC data register to the parallel data register on the next PCLK. Opcode 14 connects the D bus to the Y. Operation 14 can be temporarily suspended by raising the C/$\overline{D}$ input and resumed by lowering the C/$\overline{D}$ input again. The operation is terminated by SCLK.

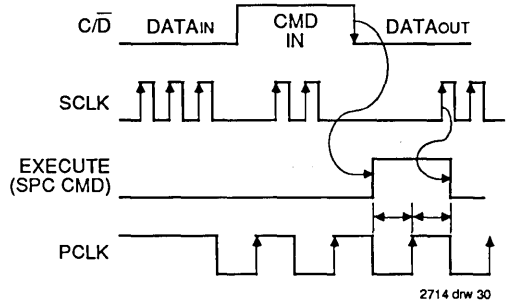
SPC Data ⟶Parallel Data Register Synchronous w/PCLK (Inst. 13)



Connect D to Y (Inst. 14)



Opcodes 3 and 13 transfer data synchronous to the PCLK which means that the high-to-low on the C/$\overline{D}$ input is an arm signal. The data and command can be shifted in while the PCLK is running. The C/$\overline{D}$ line is dropped prior to the desired PCLK edge and raised before the next edge. Instruction 13 can be repeated over many times by leaving the C/$\overline{D}$ line low during multiple transitions of the PCLK while not clocking SCLK. PCLK cycles can even be skipped by raising the C/D input during the desired clock periods. Instruction 3 can be repeated by pulsing the C/$\overline{D}$ high after each PCLK.



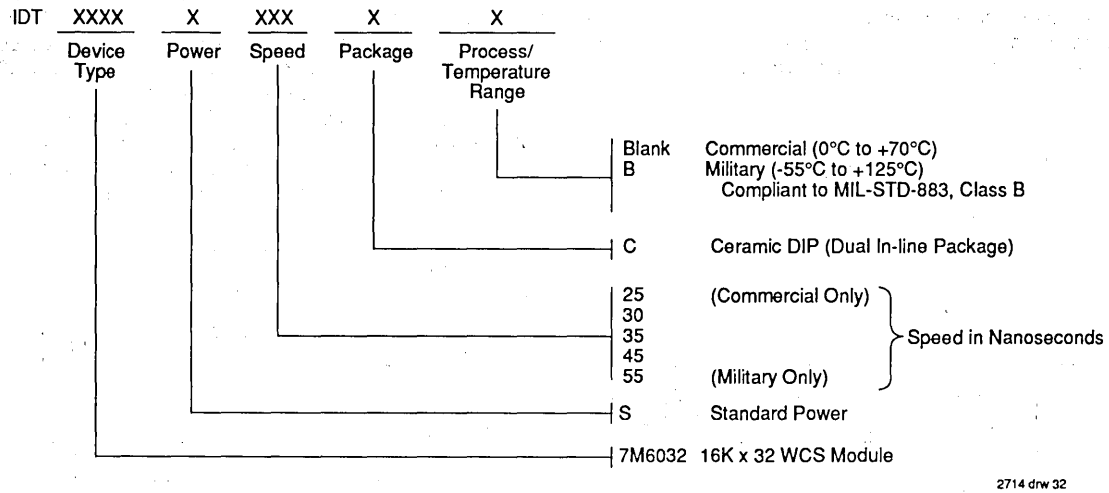
The ability to continuously execute a synchronous command can provide major benefits. For example, the synchronous read (Instruction 3, Y to SPC data) instruction could be clocked into the SPC data register. Then, it could be continuously executed by pulsing the C/$\overline{D}$ line high. When the whole system is stopped (PCLK quiescent), the serial data register will contain the next to the last state of the parallel data register. That value can be shifted out and the current state of the parallel register can then be observed, allowing for the observation of two states of the parallel register (the current and the previous).

As companies like IDT continue to integrate more onto each device and put each device into smaller packages such as surface mount devices, the board level testing becomes more complex for the designer and the manufacturing divisions of companies. To help this situation, serial diagnostics was invented. This allows for observation of critical signals deep within the system. During system test when an error is observed, these signals may be modified in order to zero in on the fault in the system.

Serial diagnostics is primarily a scheme utilizing only a few pins (4) to examine and alter the internal state of a system for the purpose of monitoring and diagnosing system faults. It can be used at many points in the life of a product: design debug and verification, manufacturing test and field service. This document describes a serial diagnostic scheme which was developed at IDT and will be used in future VLSI logic devices designed by IDT.

8

ORDERING INFORMATION



Integrated Device Technology, Inc.

8K x 112 WRITABLE CONTROL STORE STATIC RAM MODULE

IDT 7MB6042

FEATURES:

- 8K x 112 high-performance Writable Control Store (WCS)
- Serial Protocol Channel (SPC™)–reading, writing and interrogation
- High fanout pipeline register
- Width expandable
- Designed for high-speed writable control store applications
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Compact quad in-line module
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

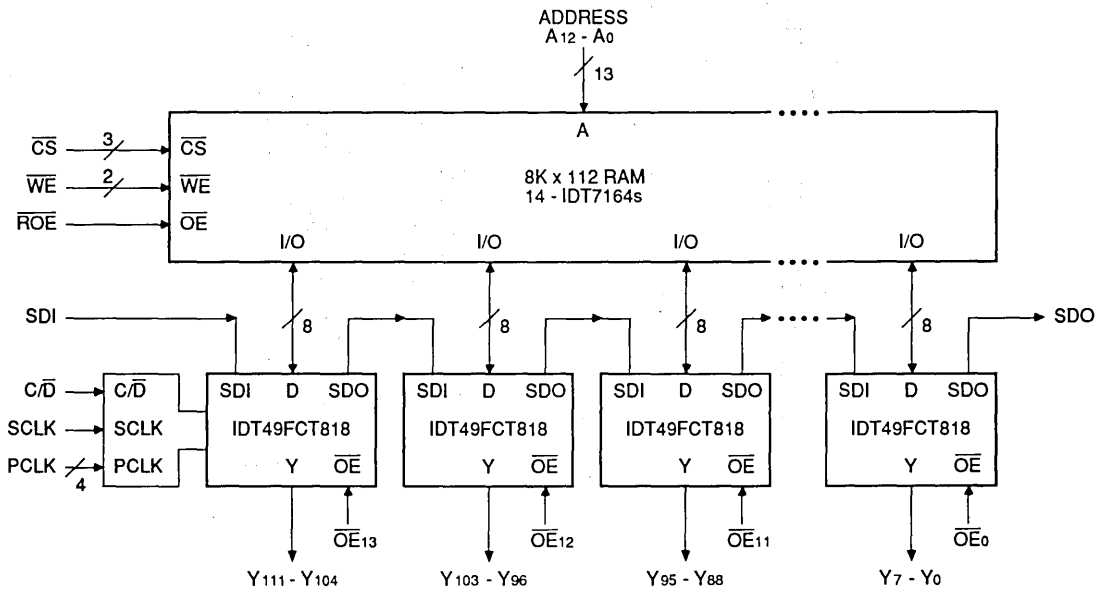
DESCRIPTION:

The IDT7MB6042 is an 8K x 112 Writable Control Store (WCS) RAM and pipeline register. It features fourteen 8K x 8 IDT7164 high-performance static RAMs and fourteen IDT49FCT818 Serial Protocol Channel (SPC) registers. These devices are arranged to form the 8K x 112 Writable Serial Store RAM with Serial Protocol Channel for loading of the memory. Each eight outputs of the RAM are connected to the D inputs of an IDT49FCT818 in the normal fashion. The device has the serial data-in and serial data-output bits connected to form a 112-bit Serial Protocol Channel register. The command/data (C/D) and Serial Shift Clock (SCLK) are all bus organized across the fourteen IDT49FCT818 registers. The 112 register output bits, 8 from each device, are separately brought out to form a 112-bit wide pipeline register on the Writable Control Store.

In normal operation, data from the 112-bit wide memory is loaded into the IDT49FCT818 registers on the low-to-high transition of PCLK. Reading and writing of the memory by means of the Serial Protocol Channel are performed using the protocol of the IDT49FCT818. (For details of this operation, please refer to the IDT49FCT818 data sheet.) The data to be loaded can be shifted in the serial data input by using the SCLK and a load command executed by shifting the proper command word in the serial data input when the C/D line is in the command mode. This command will then be executed by manipulating the C/D line and SCLK line in the desired fashion. Data is then written into the RAM by bringing the write enable line on the RAM memory from the high state to the low state and back to the high state.

The IDT7MB6042 is offered as a compact, cost-effective FR-4 quad in-line module and occupies less than 9 square inches of board space.

FUNCTIONAL BLOCK DIAGRAM



2744 drw 01

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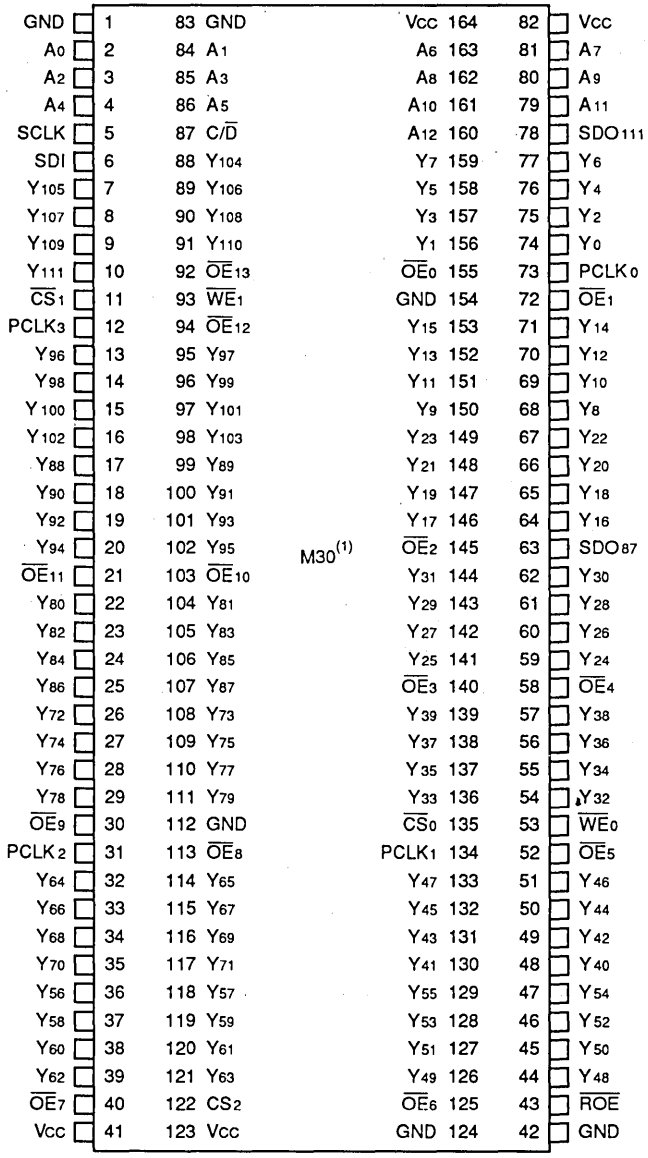
PIN CONFIGURATION[1]



QIP
TOP VIEW

2744 drw 02

NOTE:
1. For module dimensions, please refer to drawing M31 in the packaging section.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	°C
T_{STG}	Storage Temperature	−55 to +125	°C
I_{OUT}	DC Output Current	50	mA

2744 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2744 tbl 02

NOTE:
1. V_{IL} (min.) = −3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2744 tbl 03

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	H	X	High Z	Standby
Standby	H	L	X	D_{OUT}	Standby
Read	L	L	H	D_{OUT}	Active
Read	L	H	H	High Z	Active
Write	L	SPC(1)	L	SPC(1)	Active

2744 tbl 04

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
$C_{IN(D)}$	Input Capacitance Data	V_{IN} = 0V	10	pF
$C_{IN(A)}$	Input Capacitance Address and Control	V_{IN} = 0V	120	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	pF

2744 tbl 05

NOTE:
1. This parameter is sampled and not 100% tested.

PIN DESCRIPTION

Pin Name	I/O	Description
PCLK	I	Parallel Data Register Clock
A_{0-12}	I	Address Bus Pins (A_0 = LSB, A_{12} = MSB)
Y_{0-111}	I/O	Parallel Data Register Output Pins (Y_0 = LSB, Y_{111} = MSB)
$\overline{OE_Y}$	I	Output Enable for Y Bus (Overidden by SPC Inst. 8 and 14)
SDI	I	Serial Data In for SPC Operation. Data and command shifts in the Least Significant Bit first
SDO	O	Serial Data Out for SPC Operation. Data and command shifts out the Least Significant Bit first
C/$\overline{D}$	I	Mode Control for SPC
SCLK	I	Serial Shift Clock for SPC Operations
$\overline{CS0}$	I	Chip Select for lower order 56 bits (active low)
$\overline{CS1}$	I	Chip Select for upper order 56 bits (active low)
CS2	I	Chip Select for all bits (active high)
$\overline{WE}$	I	Internal RAM Write Enable
$\overline{ROE}$	I	Internal RAM Output Enable

2744 tbl 06

NOTE:
1. See SPC commands for proper execution of write cycle.

8

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	100	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	15	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	15	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 32mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = −15mA	2.4	—	V
I_{CC1}	Operating Current	f = 0, $\overline{CS}$ = V_{IL}, V_{CC} = Max., Output Open	—	1500	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ = V_{IL}, f = f_{MAX} Output Open	—	2380	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max. f = f_{MAX}, Outputs Open	—	560	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} - 0.2V, V_{IN} > V_{CC} - 0.2V or < 0.2V	—	280	mA

2744 tbl 07

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	30ns Min.	30ns Max.	35ns Min.	35ns Max.	40ns Min.	40ns Max.	50ns Min.	50ns Max.	60ns Min.	60ns Max.	Unit
Read Cycle												
t_{AC}	Address Valid to PCLK Set Up	30	—	35	—	40	—	50	—	60	—	ns
t_{CS}	$\overline{CS}$ Valid to PCLK Set Up	30	—	35	—	40	—	50	—	60	—	ns
t_{OESU}	$\overline{ROE}$ Valid to PCLK Set Up	17	—	20	—	25	—	30	—	35	—	ns
t_{PCY}	PCLK to Output Valid	—	10	—	12	—	15	—	15	—	15	ns
t_{OE}	$\overline{OE}$ Asserted to Output Valid	—	10	—	12	—	15	—	15	—	15	ns
t_{OHZ}	$\overline{OE}$ Negated to Output in High Z	—	10	—	12	—	15	—	15	—	15	ns
Write Cycle												
t_{AW}	Address Valid to End of Write	25	—	30	—	35	—	45	—	55	—	ns
t_{CW}	Address Valid to End of Write	25	—	30	—	35	—	45	—	55	—	ns
t_{WP}	Write Enable Pulse Width	23	—	28	—	33	—	43	—	53	—	ns
t_{WCD}	Cont/Dat to End of Write	23	—	28	—	30	—	35	—	40	—	ns
t_{AS}	Address Setup Time	0	—	0	—	2	—	2	—	2	—	ns

2744 tbl 08

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

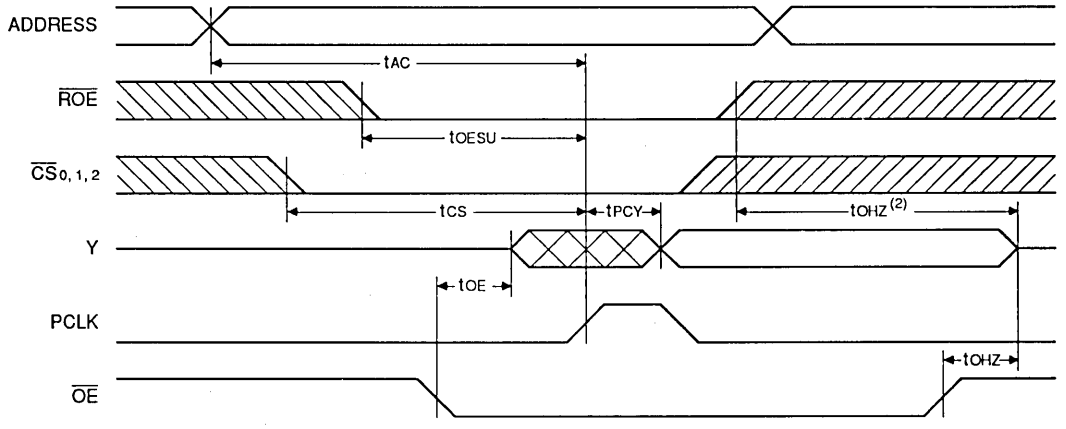
SPC TIMING

Symbol		Parameter	30ns Min.	30ns Max.	35ns Min.	35ns Max.	40ns Min.	40ns Max.	50ns Min.	50ns Max.	60ns Min.	60ns Max.	Unit
t_{PLH}	T_2	SCLK High to SDO	—	15	—	15	—	22	—	22	—	22	ns
t_{PHL}	T_3	SDI to SDO (Stub Mode)	—	210	—	210	—	310	—	310	—	310	ns
	T_4	C/$\overline{D}$ Low to Y	—	15	—	15	—	20	—	20	—	20	ns
	T_5	SCLK High to Y	—	15	—	15	—	22	—	22	—	22	ns
	T_6	C/$\overline{D}$ Low to SDO	—	15	—	15	—	25	—	25	—	25	ns
t_{SU}	S_2	C/$\overline{D}$ to SCLK High	15	—	15	—	15	—	15	—	15	—	ns
	S_3	SDI to SCLK High	8	—	8	—	8	—	8	—	8	—	ns
	S_4	Y or D to C/$\overline{D}$ Low	5	—	5	—	5	—	5	—	5	—	ns
	S_5	C/$\overline{D}$ to PCLK High	12	—	12	—	12	—	12	—	12	—	ns
t_H	S_6	Y to PCLK High	5	—	5	—	5	—	5	—	5	—	ns
	H_2	C/$\overline{D}$ from SCLK Low	12	—	12	—	12	—	12	—	12	—	ns
	H_3	SDI from SCLK High	2	—	2	—	2	—	2	—	2	—	ns
	H_4	Y or D to C/$\overline{D}$ Low	2	—	2	—	2	—	2	—	2	—	ns
	H_5	SCLK High to PCLK High	2	—	2	—	2	—	2	—	2	—	ns
	H_6	C/$\overline{D}$ from PCLK High	2	—	2	—	2	—	2	—	2	—	ns
	H_7	Y from PCLK High	3	—	3	—	3	—	3	—	3	—	ns
t_{HZ}(1,2)	2z, 4z	SCLK High to D or Y High Z	—	15	—	15	—	20	—	20	—	20	ns
t_{LZ}(1,2)	3z, 5z	C/$\overline{D}$ High to D or Y High Z	—	15	—	15	—	20	—	20	—	20	ns
t_{ZHL}(1,2)	Z2, Z3	C/$\overline{D}$ Low to D or Y Valid	—	15	—	15	—	20	—	20	—	20	ns
t_W	W_1	PCLK (High and Low)	10	—	10	—	15	—	15	—	15	—	ns
	W_2	SCLK (High and Low)	30	—	30	—	35	—	35	—	35	—	ns
	W_3	C/$\overline{D}$ High	30	—	30	—	35	—	35	—	35	—	ns

2744 tbl 09

NOTES:
1. Guaranteed but not tested.
2. $\overline{OE}$ = V_{IH}.

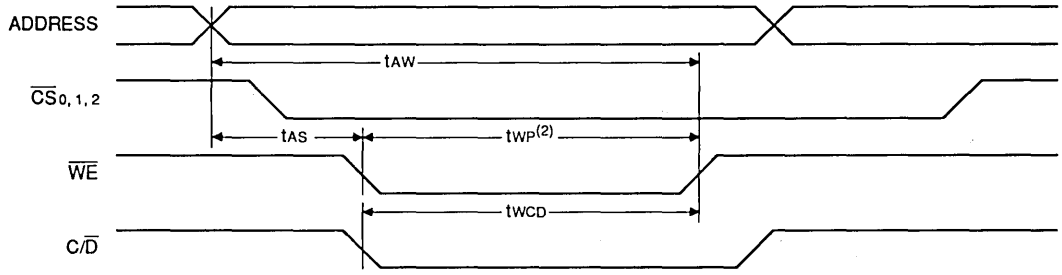
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



2744 drw 03

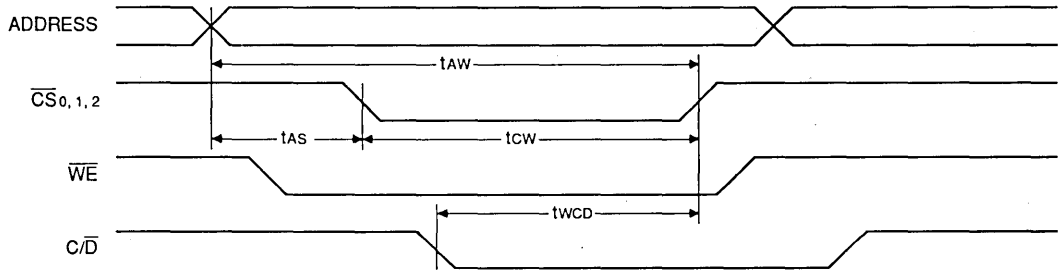
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 5)



2744 drw 04

TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 4, 5)

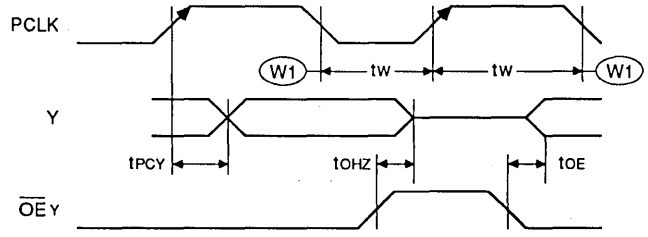


2744 drw 05

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured fromt he earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
5. tROE = VIH.

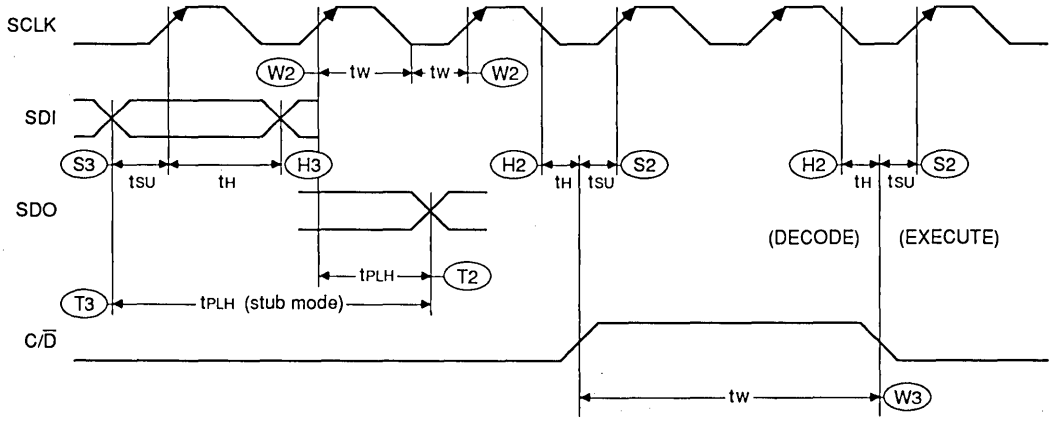
8

GENERAL AC WAVE FORM FOR PARALLEL INPUTS AND OUTPUTS



2744 drw 06

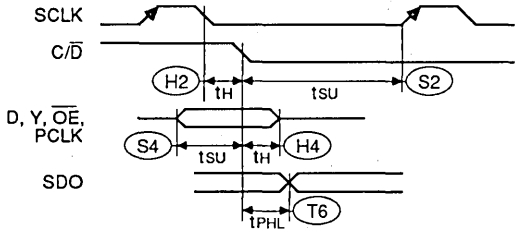
GENERAL AC WAVE FORM FOR SERIAL PROTOCOL INPUTS AND OUTPUTS



2744 drw 07

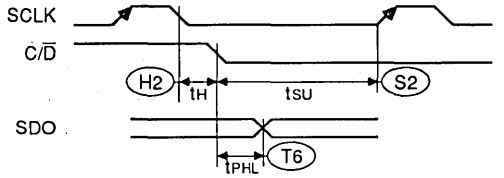
DETAILED AC WAVE FORM OF SERIAL PROTOCOL OPERATIONS

Y ⟶ SPC Data (Inst. 0)
D ⟶ SPC Data (Inst. 2)
Status ⟶ SPC Data (Inst. 4)



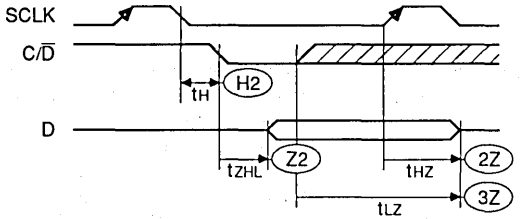
2744 drw 08

PARALLEL DATA REGISTER ⟶ SPC Data (Inst. 1)
SET SERIAL MODE (Inst. 11)
SET STUB MODE (Inst. 12)



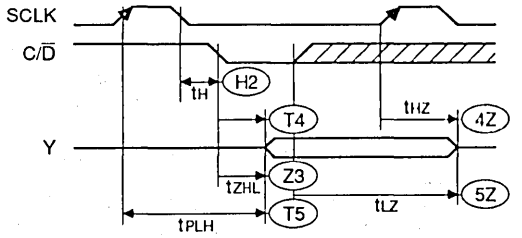
2744 drw 09

CONNECT Y TO D (Inst. 5)
SPC Data ⟶ D (Inst. 9)



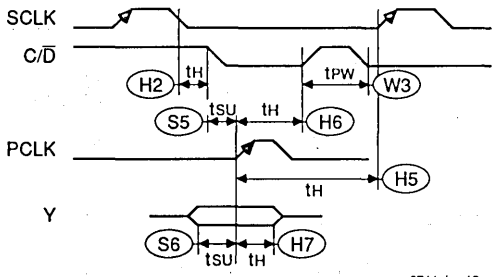
2744 drw 10

SPC Data ⟶ PARALLEL DATA REGISTER (Inst. 10)
SPC Data ⟶ Y (Inst. 8)
CONNECT D TO Y (Inst. 14)



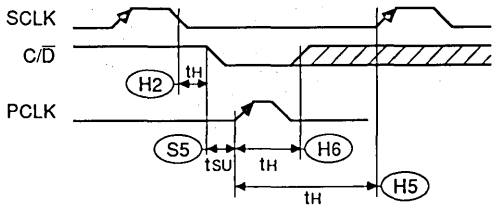
2744 drw 11

Y ⟶ SPC Data SYNCHRONOUS W/PCLK (Inst. 3)



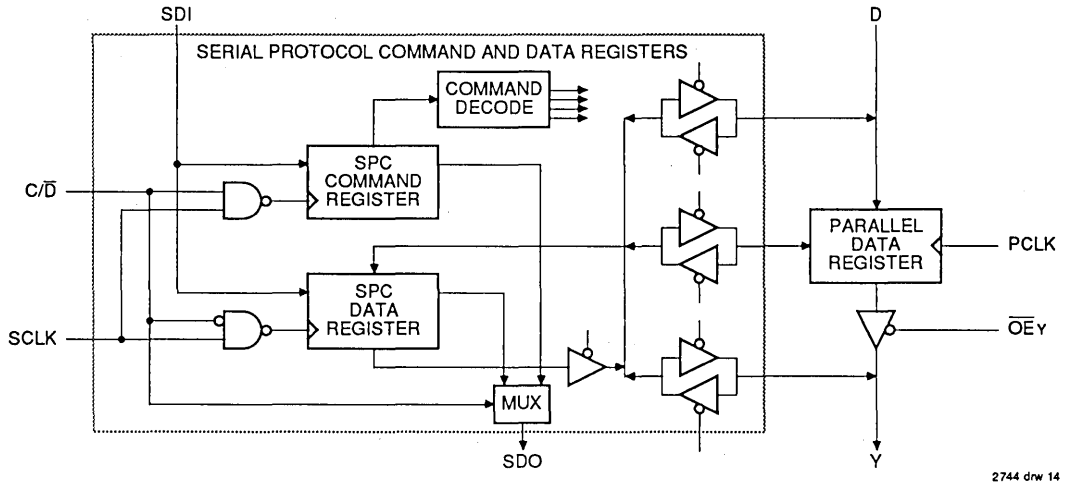
2744 drw 12

SPC Data ⟶ PARALLEL DATA REGISTER
SYNCHRONOUS W/PCLK (Inst. 13)

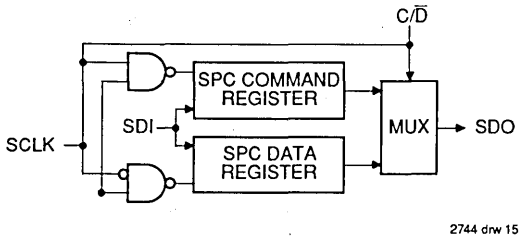


2744 drw 13

DETAILED FUNCTIONAL BLOCK DIAGRAM



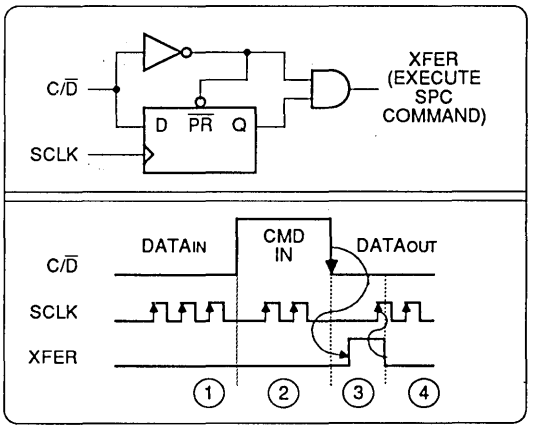
The detailed block diagram consists of two main elements: the parallel data register and the SPC data/command registers. The main data path is from the D inputs down to the data register and through to the Y outputs. This path is typically used during standard operations. For diagnostic or system initialization, the internal SPC data path is used. This path allows access between the SPC data and command registers and the standard data path, pins and data register. The SPC data and command registers are accessed via the SDI, SDO, C/$\overline{D}$ and SCLK pins.



SPC FUNCTION DESCRIPTION

The Serial Protocol Channel (SPC) has been optimized for the minimum number of pins and the maximum flexibility. The data is passed in on a Serial Data Input pin (SDI) and out on a Serial Data Output pin (SDO). The transfer of the data is controlled by a Serial Clock (SCLK) and a Command/Data mode input (C/$\overline{D}$). These four pins are the basic SPC pins. To the outside, the SPC appears as two serial shift registers in parallel—one for command and the other data. The serial clock shifts data and the Command/Data (C/$\overline{D}$) line selects which register is being shifted. The command register is used to control loading of data to and from the data register with other storage elements in the device.

With respect to executing an SPC command, there are four distinct phases: (1) data is shifted in, (2) followed by the command, (3) the command is executed, and (4) data is shifted out. During the data mode, data is simultaneously shifted into the serial data register while the data in the register is shifted out. During the command mode, opcode-type information is shifted through the serial ports. The command is executed when the last bit is shifted in and the C/$\overline{D}$ line is brought low. The execution phase is ended with the next serial clock edge.



SPC data and commands are shifted in through the SDI pin, which is a serial input pin, and out through the SDO pin, which is a serial output pin. Data and commands are shifted in Least Significant Bit first; Most Significant Bit last (Y_0 = LSB, Y_{15} = MSB). Execution of the SPC commands is performed by stopping the shift clock, SCLK, and lowering the C/$\overline{D}$ line from high-to-low. Later the SCLK may then be transitioned from low-to-high. SPC commands and data can be shifted anytime, without regard for operation. During the execution phase, care must be taken that there is no conflict between the SPC operation nad parallel operation. This means that if the SPC operation attempts to load the parallel data register (opcode 10) while PCLK is in transition, the results are undefined. In general, it is required that the PCLK be static during SPC operations. The synchronous commands (opcode 3 and 13), however, allow the PCLK to run. In these operations, the high-to-low transition of the C/$\overline{D}$ line takes on the function of an arm signal in preparation for the next low-to-high transition of the PCLK.

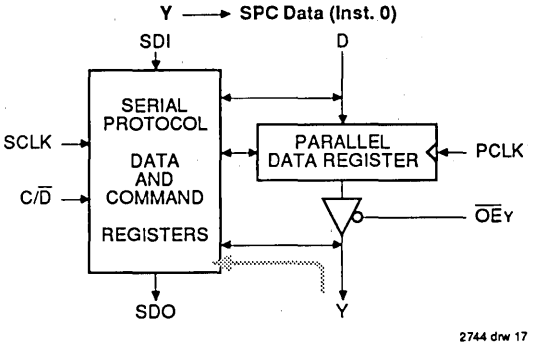
SPC COMMANDS

There are 16 possible SPC opcodes. Fourteen of these are utilized, the other two are reserved and perform NO-OP functions. The top eight opcodes, 0 through 7, are reserved for transferring data into the SPC data register for shifting out. The lower eight opcodes, 8 through 15, are used for transferring data from the SPC data register to other parts of the device. Two of the commands are also used for connecting the data in and out pins.

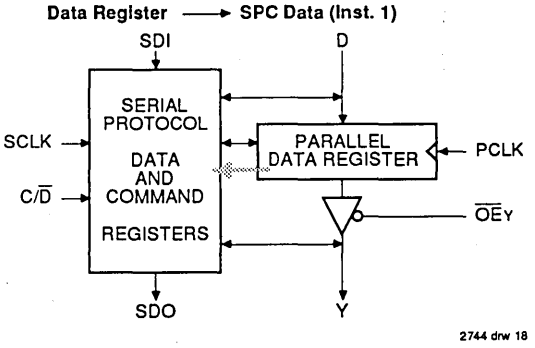
Opcode	SPC Command
0	Y to SPC Data Register
1	Parallel Data Register to SPC Data Register
2	D to SPC Data Register
3	Y to SPC Data Register Synchronous w/ PCLK
4	Status ($\overline{OE}_Y$, PCLK) to SPC Data Register
5	Connect Y to D
6-7	Reserved (NO-OP)
8	SPC Data to Y ($\overline{OE}$ is overidden)
9	SPC Data to D
10	SPC Data to Parallel Data Register
11	Select Serial Mode
12	Select Stub Mode
13	SPC Data to Parallel Data Register Synchronous w/ PCLK
14	Connect D to Y ($\overline{OE}$ is overidden)
15	NO-OP

2744 tbl 10

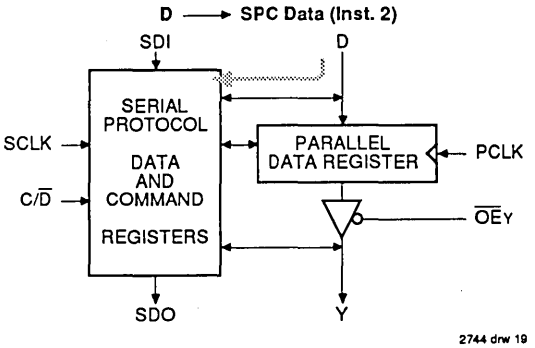
Opcode 0 is used for transferring data from the Y output pins into the SPC data register. Opcode 1 transfers data from the output of the register, before the tri-state gate, into the SPC data register. Opcode 2 transfers data from the D input pins into the SPC data register.



2744 drw 17



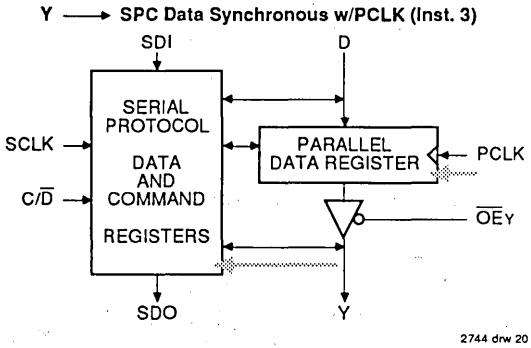
2744 drw 18



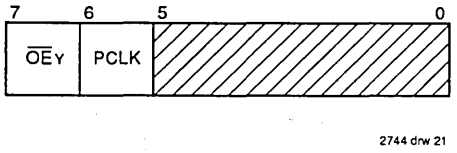
2744 drw 19

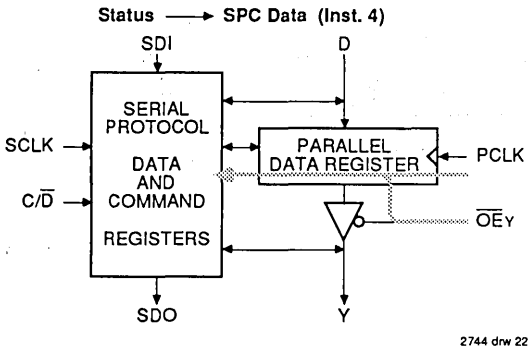
8

Opcode 3 transfers data on the Y pins to the SPC data register on the next PCLK, thus achieving a synchronous observation of the SPC data register in real time. This operation can be forced to repeat without shifting in a new command by pulsing C/$\overline{D}$ low-high-low after each PCLK. As soon as data is shifted out using SCLK, the command is terminated and must be loaded in again.

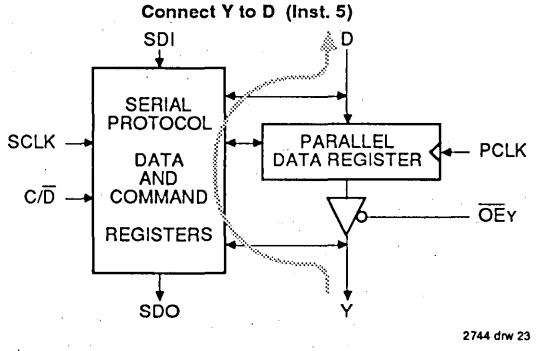


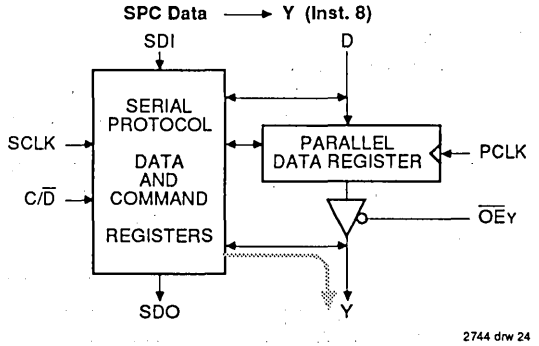
Opcode 4 is used for loading status into the SPC data register. The format of bits is shown below.



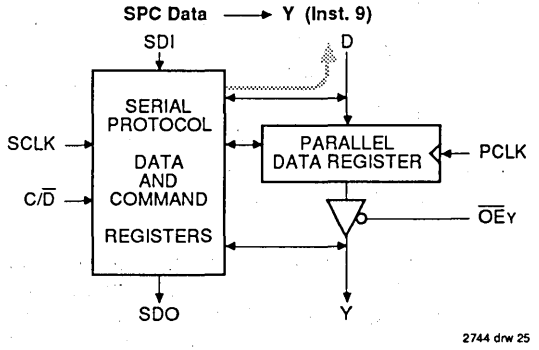


Opcode 5 connects Y to D. Opcodes 6 and 7 are reserved, hence designated NO-OP.

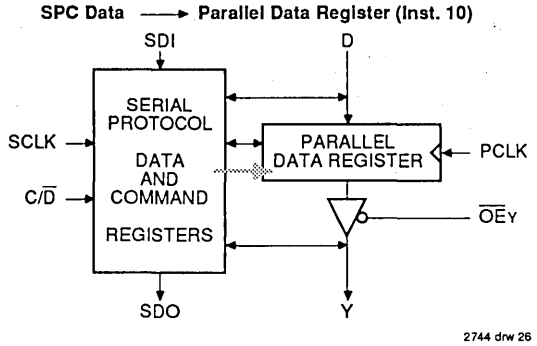




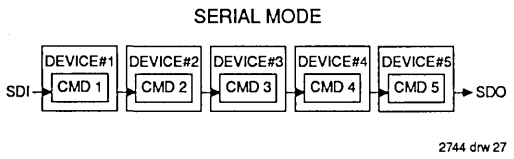
Opcode 8 is used for transferring SPC data directly to the Y pins. When executing opcode 8, the state of $\overline{OE}_Y$ is a "do not care"; that is, data will be output even if $\overline{OE}_Y$ = HIGH. Opcode 9 is used for transferring SPC data to the D pins. Operands 8 and 9 can be temporarily suspended by raising the C/$\overline{D}$ input and resumed by lowering the C/$\overline{D}$. As soon as SCLK completes transition, the command is terminated.



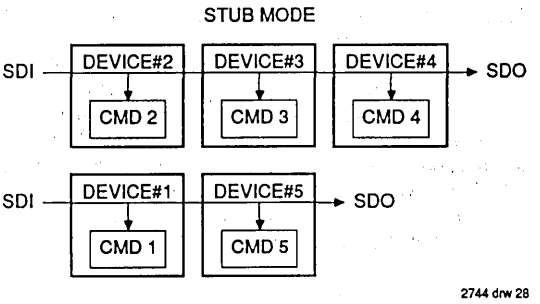
Opcode 10 is used for transferring data from the SPC data register into the parallel data register, irrespective of the state of PCLK. However, PCLK must be static between C/$\overline{D}$ going high-to-low and SCLK going low-to-high.



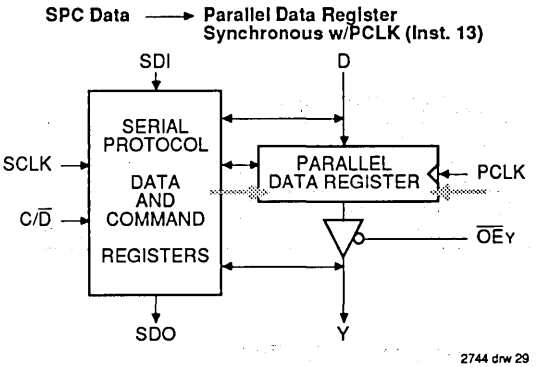
Opcode 11 and 12 are used to set Serial and Stub Mode, respectively. After executing one of these opcodes, the device remains in this mode until programmed otherwise. The Serial mode is the default mode that the IDT49FCT818 powers up in. In Serial mode, commands are shifted through the SPC command register and then to the SDO pin. This is the typical mode used when several varieties of devices that utilize the SPC access method are employed on one serial ring.

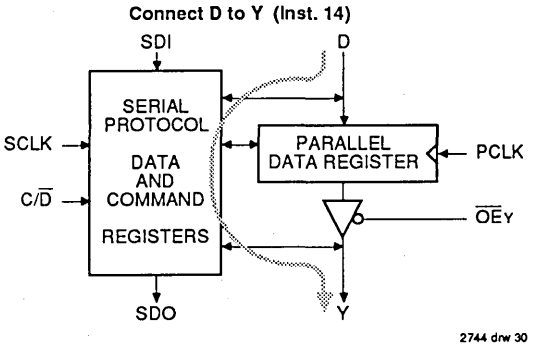


In Stub mode, SDI is connected directly to SDO. In this way, the same diagnostic command can be loaded into multiple devices of like type. For example, in four clock cycles the same command could be loaded into 8 IDT49FCT818s (64-bit pipeline register). Dissimilar devices must be segregated into serial scan loops of similar type, as shown below. During the command phase, the serial shift clock must be slowed down to accommodate the delay from SDI to SDO through all of the devices. The slower clock is typically a small tradeoff compared to the reduced number of clock cycles.



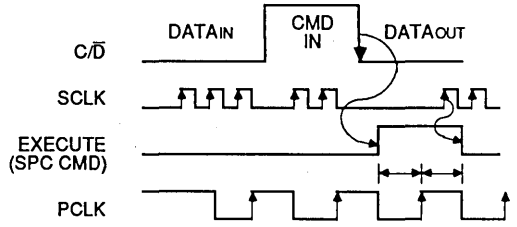
Opcode 13 transfers data from the SPC data register to the parallel data register on the next PCLK. Opcode 14 connects the D bus to the Y. Operation 14 can be temporarily suspended by raising the C/$\overline{D}$ input and resumed by lowering the C/$\overline{D}$ input again. The operation is terminated by SCLK.





Opcode 3 and 13 transfer data synchronous to the PCLK which means that the high-to-low on the C/$\overline{D}$ input is an arm signal. The data and command can be shifted in while the PCLK is running. The C/$\overline{D}$ line is dropped prior to the desired PCLK edge and raised before the next edge. Instruction 13 can be repeated over many times by leaving the C/$\overline{D}$ line low during multiple transitions of the PCLK while not clocking SCLK. PCLK cycles can even be skipped by raising the C/$\overline{D}$ input during the desired clock periods. Instruction 3 can be repeated by pulsing the C/$\overline{D}$ high after each PCLK.

The ability to continuously execute a synchronous command can provide major benefits. For example, the synchronous read (Instruction 3, Y to SPC data) instruction could be clocked into the SPC data register. Then, it could be continuously executed by pulsing the C/$\overline{D}$ line high. When the whole system is stopped (PCLK quiescent), the serial data register will contain the next to the last state of the parallel data register. That value can be shifted out and the current state of the parallel register can then be observed, allowing for the observation of two states of the parallel register (the current and the previous).



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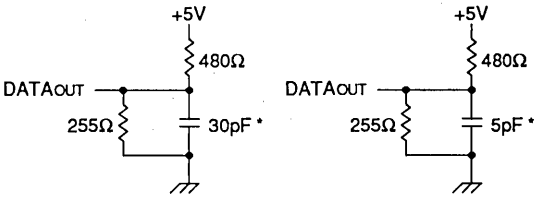
AC TEST CONDITIONS

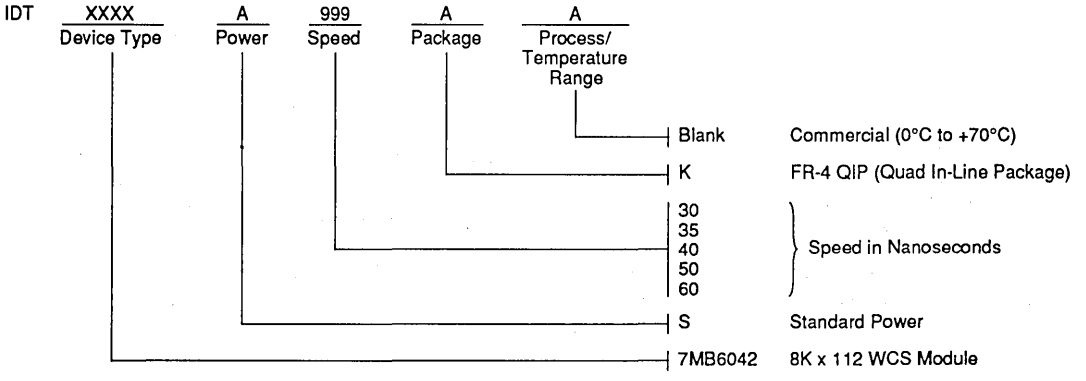
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2744 tbl 11



2744 drw 32

ORDERING INFORMATION



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Integrated Device Technology, Inc.

THE SUBSYSTEM'S "FLEXI-PAK" CMOS MODULE FAMILY

SRAM, EPROM, & EEPROM MODULES

ADVANCE INFORMATION

FEATURES:

- High-density modules using high-speed CMOS SRAM, EPROM, and EEPROM components.
- Inter-changeable modules, with equivalent footprints, support a wide range of applications
- Fast access times:
  - SRAM: 30ns (max.) - military
    25ns (max.) - commercial
  - EEPROM: 95ns (max.) - military
    75ns (max.) - commercial
  - EPROM: 150ns (max.) - military
    120ns (max.) - commercial
- Low power CMOS operation
- Surface mounted LCC components on a co-fired ceramic substrate
- Offered in a 66-pin, ceramic "PGA-type" HIP (Hex In-line Package). occupying only 1 sq. inch of board space
- Single 5V (± 10%) power supply
- Multiple ground pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

The Flexi-Pak family of modules are high-speed, high-density CMOS memory modules constructed on a multilayer co-fired ceramic substrate using either SRAM, EPROM, or EEPROM components in leadless chip carriers.

This family of IDT modules support applications requiring stand alone static or programmable memory, or those applications needing a combination of both. All module configurations in this family have equivalent footprints, allowing "plug-in compatibility" with each other (i.e. interchangeable), ideal for a wide range of prototype and debugging applications.

The Flexi-Pak family utilizes the fastest commercial grade and MIL-STD-883, Class B military grade components, giving you the highest performance available anywhere. CMOS technology offers a low-cost, low-power alternative to bipolar and fast NMOS memories.

All versions of the Flexi-Pak module family are offered in a 66-pin, ceramic HIP (Hex In-line Package). This HIP package is similar to a PGA and allows the designer to fit into 1 sq. inch of board space.

All IDT military modules are assembled with semiconductor components compliant with the latest revision of MIL-STD-883, Class B. Additional testing and burn-in when assembled into a module, make them ideally suited to applications demanding the highest level of performance and reliability.

ORGANIZATIONS

SRAM: IDT7M4003 - 128K x 8, 64K x 16, 32K x 32
IDT7M4013 - 512K x 8, 256K x 16, 128K x 32

SRAM / EEPROM:
IDT7M7005 - 64K x 8 / 64K x 8
64K x 8 / 32K x 16
32K x 16 / 64K x 8
32K x 16 / 32K x 16
IDT7M7025 - 64K x 8 / 256K x 8
64K x 8 / 128K x 16
32K x 16 / 256K x 8
32K x 16 / 128K x 16
IDT7M7035 - 256K x 8 / 256K x 8
256K x 8 / 128K x 16
128K x 16 / 256K x 8
128K x 16 / 128K x 6
IDT7M7045 - 256K x 8 / 64K x 8
256K x 8 / 32K x 16
128K x 16 / 64K x 8
128K x 16 / 32K x 16

EEPROM: IDT7M7004 - 128K x 8, 64K x 16, 32K x 32
IDT7M7014 - 512K x 8, 256K x 16, 128K x 32

SRAM / EPROM:
IDT7M7012 - 64K x 8 / 64K x 8
64K x 8 / 32K x 16
32K x 16 / 64K x 8
32K x 16 / 32K x 16
IDT7M7002 - 64K x 8 / 256K x 8
64K x 8 / 128K x 16
32K x 16 / 256K x 8
32K x 16 / 128K x 16
IDT7M7022 - 256K x 8 / 256K x 8
256K x 8 / 128K x 16
128K x 16 / 256K x 8
128K x 16 / 128K x 6
IDT7M7032 - 256K x 8 / 64K x 8
256K x 8 / 32K x 16
128K x 16 / 64K x 8
128K x 16 / 32 x 16

8

Integrated Device Technology, Inc.

IDT CUSTOM MODULE CAPABILITIES

As the largest supplier of military and commercial modules, IDT Subsystems would like to take this opportunity to discuss an exciting phase of our business: the custom module. To facilitate your understanding of our procedures, we have attached several documents which should prove helpful. These are:

I. Custom Module Flowchart
II. Specification Approval Form
III. Custom Module Terms and Conditions
IV. Mini spec example
V. Design Guidelines (refer to Application Note AN-44)
VI. Custom Module Product Proposals

The Custom Module Flowchart outlines the documentation flow while the Custom Module terms and conditions are an addendum to our standard terms and conditions found on IDT quote forms. Also included is an example of a "mini spec" which is a datasheet-like spec for custom modules. An applications note on design guidelines is included in this databook (refer to AN-44) which is useful for preliminary custom module analysis. Finally, we have included several examples of IDT generated module product proposals. These one page proposals are used to help stimulate design ideas of custom modules for various system applications, i.e. cache, DSP, or data buffering.

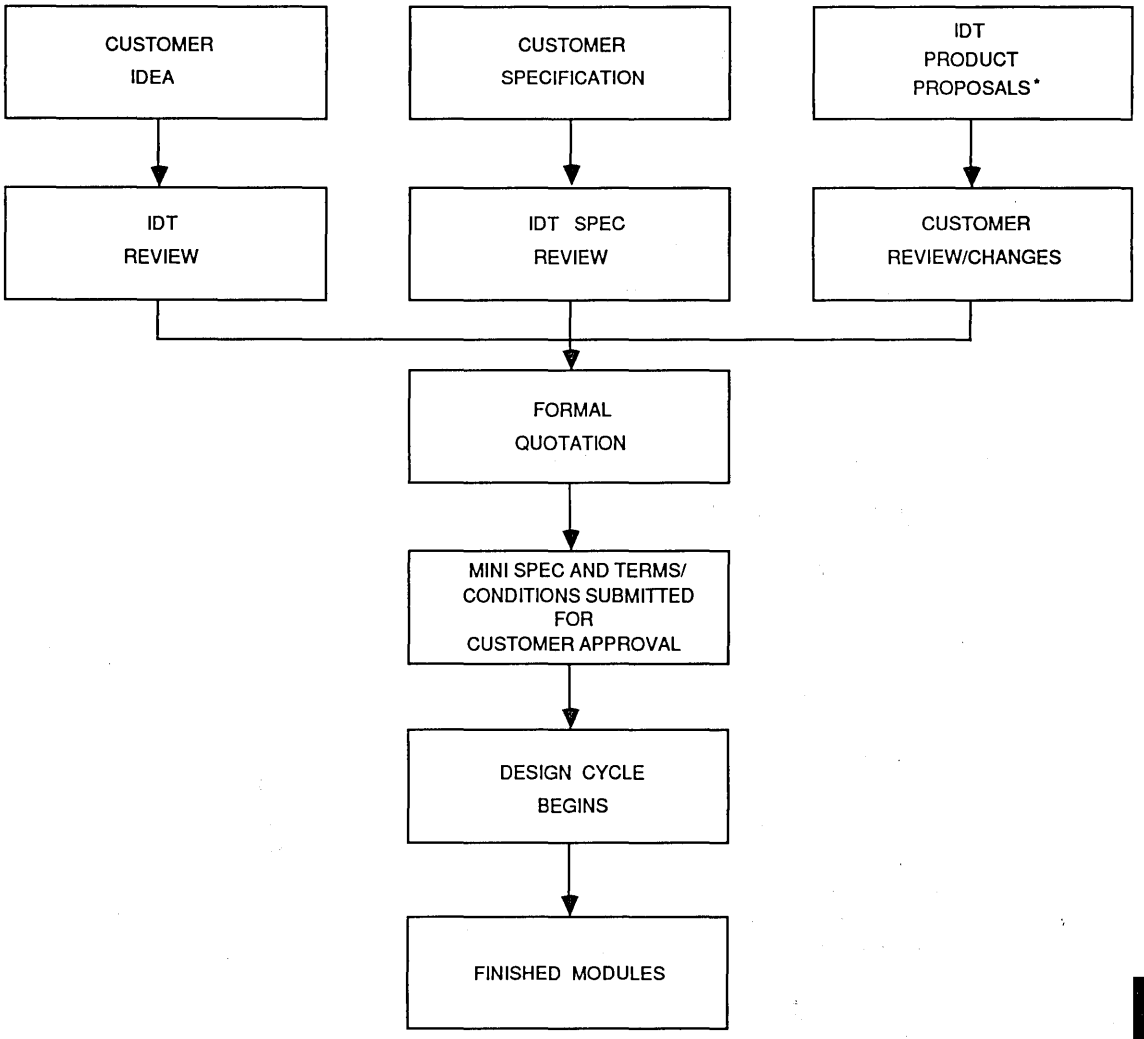
Additional information concerning Subsystems quality and reliability can be found in our IDT Quality Conformance Program brochure available at any of our IDT Sales Offices worldwide.

IDT has a highly trained staff of Field Sales and Application Engineers, as well as a factory design team to assist you in obtaining the optimal solution for your system requirements.

If any questions arise or further information is needed, please contact your IDT sales representative.

I. CUSTOM MODULE FLOWCHART

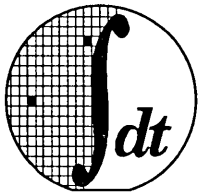
The purpose of this flowchart is to show how a module evolves from an idea into a finished product.



2807 drw 01

* For several examples of IDT Subsystems Product Proposals, please refer to Section VI of this application note.

II. SPECIFICATION APPROVAL FORM



INTEGRATED DEVICE TECHNOLOGY
SUBSYSTEMS DIVISION

SPECIFICATION APPROVAL FORM

DATE: 05/09/89

CUSTOMER COMPANY XX

PART NUMBER IDT7MB4009S25P

PLEASE FIND ATTACHED THE FOLLOWING DOCUMENTS:

1. **PACKAGE DIMENSIONS - REV. 00**
2. **AC/DC PARAMETERS - REV. 01**
3. **SCHEMATIC - REV. 00**
4. **PIN OUT - REV. 00**
5. **IDT TERMS AND CONDITIONS**

REVIEW THE ABOVE SPECIFICATIONS. YOUR SIGNATURE BELOW INDICATES ACCEPTANCE OF THE SPECIFICATIONS LISTED ABOVE. PLEASE RETURN THIS FORM TO YOUR IDT SALESPERSON OR REPRESENTATIVE.

SIGNATURE: _____

TITLE: _____

DATE: _____

III. CUSTOM MODULE TERMS AND CONDITIONS

Custom Module
Terms and Conditions Addendum

These terms and conditions are addition to the standard Integrated Device Technology terms and conditions of Sale.

1. Ownership

   a. Integrated Device Technology, Inc. will own all equipment and tooling manufactured in order to build the required module regardless of any NRE or set-up charges paid by Buyer unless specifically agreed to in writing.

   b. Integrated Device Technology, Inc. reserves the right to market the custom module as a standard product any time unless otherwise specifically agreed to in writing.

2. Cancellations and Reschedules

   a. In the event that Buyer wishes to cancel all or part of an order, or change the scope of an order, the termination or change will be accepted only with the specific approval of Integrated Device Technology in writing.

   b. In the event that a cancellation or reschedule occurs prior to the shipment of prototypes, the Buyer will be liable for all or part of the tooling and set-up charges associated with producing the custom module.

   c. Integrated Device Technology must be notified 90 days in advance of shipment of modules for any rescheduling or cancellations.

3. Specifications

   All specifications of prototypes and subsequent shipments will be agreed to in writing by Integrated Device Technology and the Buyer by:

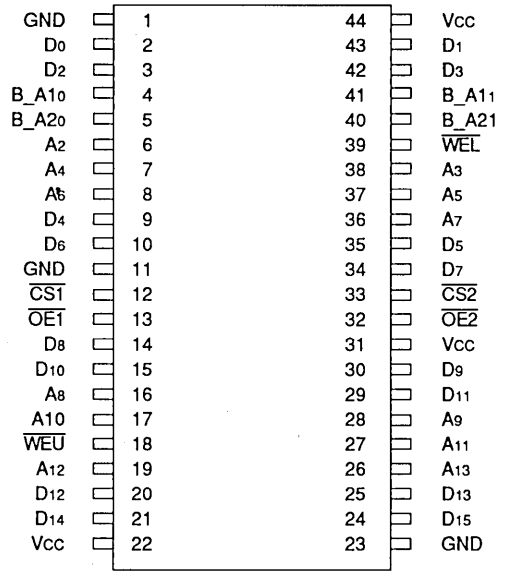
   a. A customer specification formally reviewed and accepted by Integrated Device Technology without exception; or

   b. A specification generated by Integrated Device Technology which the Buyer agrees to in writing.

IV. MINI SPEC EXAMPLE

The following documents are examples of the items found in the IDT custom module mini-spec: pin out, electrical characteristics, package dimensions, schematic, and terms and conditions.

PIN CONFIGURATION



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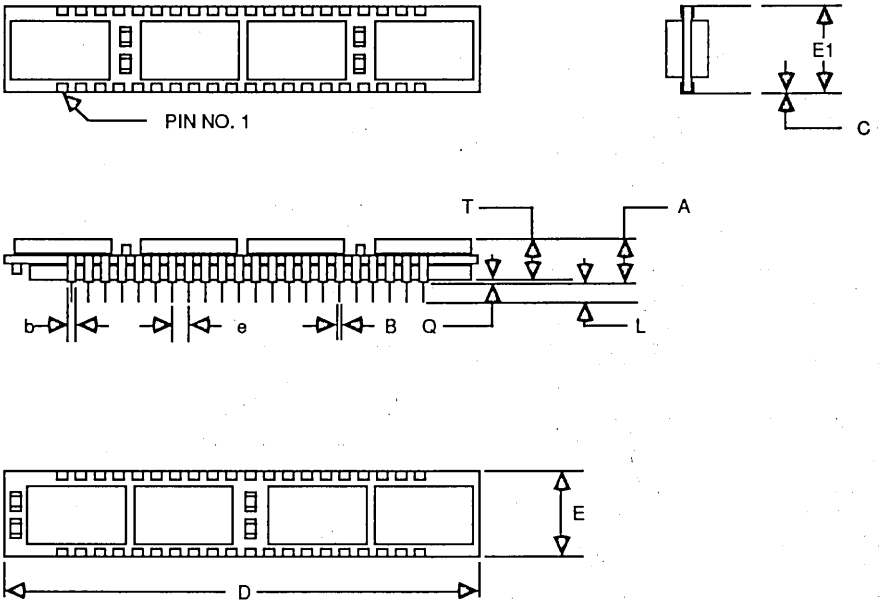

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LIMITS / SYMBOL	INCHES MIN	INCHES MAX
A	0.290	0.325
B	0.016	0.025
b	0.035	0.070
C	0.007	0.013
D	2.990	3.010
E	0.590	0.625
E_1	0.590	0.610
e	0.100 typ	
L	0.120	0.170
Q	0.030	0.060
T	0.240	0.290
N	44 LEAD	
K		

DCN	REV	DESCRIPTION	DATE	APPROVED
3024	00	NEW DRAWING	5/17	

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRAC DEC ANGLES
± ± ±

APPROVALS	DATE
DRAWN	
CHECKED	

7MB4009 2(16K X 16)
MARKETING DRAWING

SCALE	SIZE	DRAWING NO.
1:1	A	

DO NOT SCALE DRAWING | SHEET

8

MODULE NAME: 7MB4009 TEMP RANGE: COMMERCIAL REV: 01

DATE: 05/27/88

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.
$\|I_{LIA}\|$	Input Leakage (Addr & Control)	V_{CC}=MAX V_{IN}=GND to V_{CC}	—	40uA
$\|I_{LO}\|$	Output Leakage (Data)	V_{CC}=MAX $\overline{CS}$=V_{IH}, V_{OUT} = GND to V_{CC}	—	10uA
I_{CC1}	Operating Current	f=O $\overline{CS}$≤V_{IL} V_{CC}=MAX; Output Open	—	620mA
I_{CC2}	Dynamic Operating Current	V_{CC}=MAX; $\overline{CS}$≤V_{IL}; f=fMAX Output Open	—	760mA
I_{SB}	Standby Supply Current	V_{CC}=MAX; $\overline{CS}$≥V_{IH} f=fMAX Outputs Open	—	440mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$≥V_{CC}-0.2V V_{IN}>V_{CC}-0.2 or <0.2V	—	120mA
I_{OL}	Output Low Current	V_{CC}=MIN V_{OL}=0.4	8mA	—
I_{OH}	Output High Current	V_{CC}=MIN V_{OH}=2.4	—	-4mA
$\|I_{LId}\|$	Input Leakage (Data)	V_{CC}=MAX V_{IN}=GND to V_{CC}	—	10uA

2807 tbl 01

AC ELECTRICAL CHARACTERISTICS

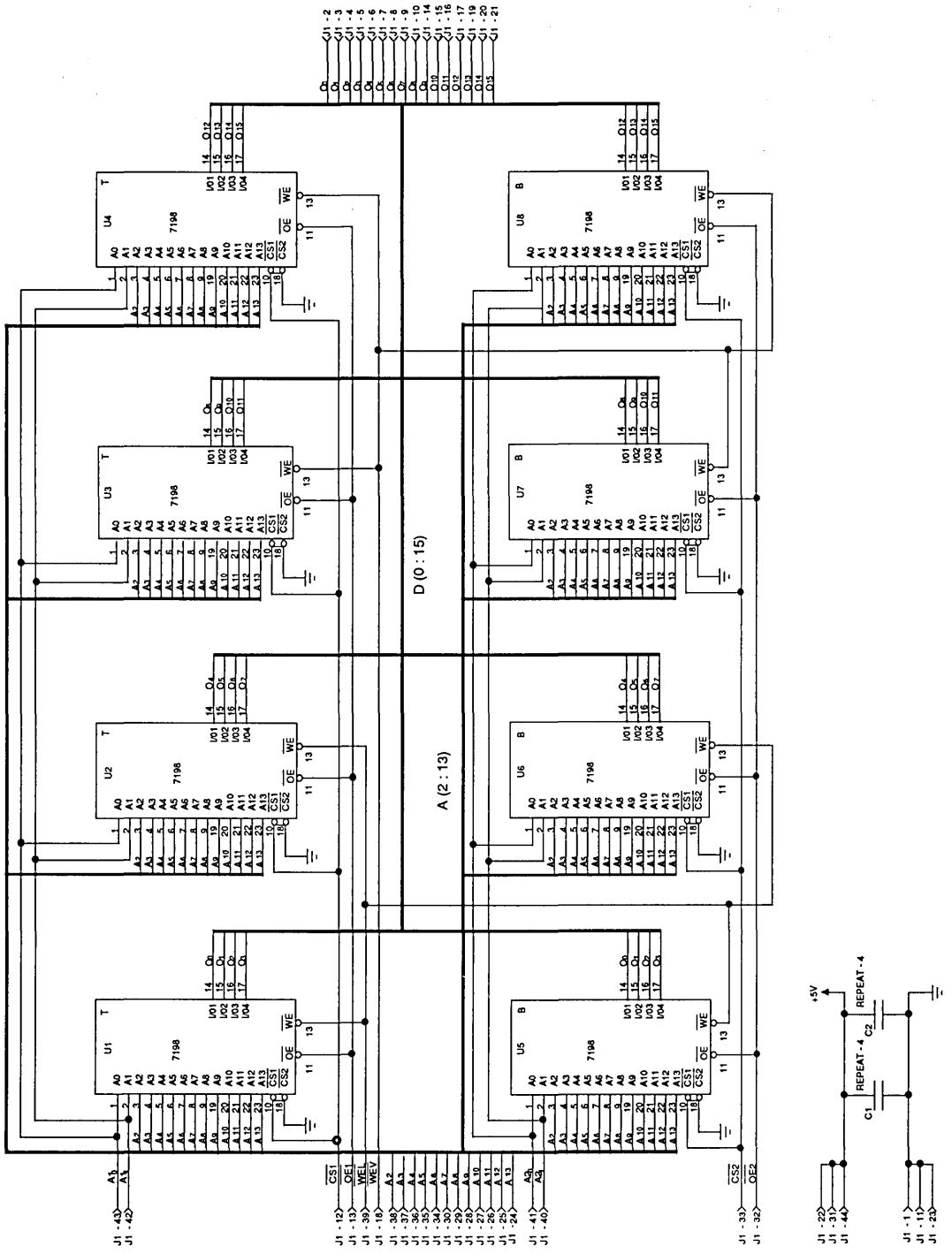
Read Cycle (nS)	Min.	Max.	Write Cycle (nS)	Min.	Max.
TRC	25	—	TWC	20	—
TAA	—	25	TCW	20	—
TACS	—	25	TAW	21	—
TOE	—	15	TAS	1	—
TOH	5	—	TWP	20	—
TPU	0	—	TWR	0	—
TPD	—	20	TDW	13	—
			TDH	0	—

TRISTATE PARAMETERS

	Min.	Max.		Min.	Max.
TCLZ	5	—	TOHZ	—	15
TCHZ	—	12	TWHZ	—	7
TOLZ	5	—	TOW	5	—

2807 tbl 02

COMMENTS:


D (0 : 15)
A (2 : 13)
U1
U2
U3
U4
U5
U6
U7
U8
7198
+5V
REPEAT - 4
C1
C2
2807 drw 04

V. DESIGN GUIDELINES

Please refer to Application Note AN-44 for a more detailed look at custom module design guidelines.

VI. IDT APPLICATION SPECIFIC CONCEPTS (PRODUCT PROPOSALS)

This section includes a number of product proposals which not only demonstrate IDT's applications abilities, but also how those abilities can be used to solve real engineering problems. The concept of translating a customer's unique memory intensive building block becomes reality by using the Subsystem Division's engineering expertise. Use this section as a guide to better understand if IDT's custom module capabilities may be appropriately utilized in your application.

Integrated Device Technology, Inc.

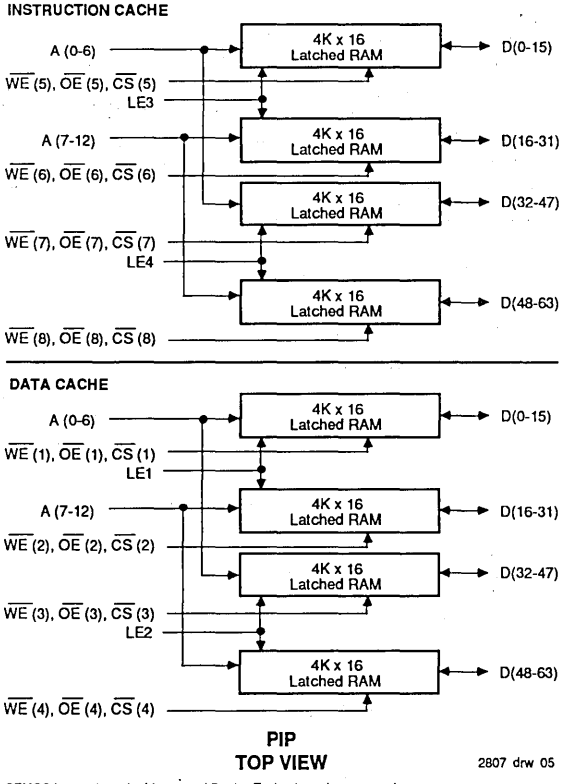
16 BYTE INSTRUCTION/16K BYTE DATA CACHE MODULE FOR THE IDT79R3000 CPU

PRODUCT PROPOSAL IDT7MB6074

FEATURES:

- Family member in a group of pin compatible high speed CMOS static RAM modules to support the IDT79R3000 RISC CPU
- Organized as a 16K byte instruction and 16K byte data cache
- Operating frequencies to support 12MHz, 16.7MHz, 20MHz, and 25MHz IDT79R3000
- Available in a high-density, low profile 160 pin PIP (Pent In-line Package)
- Surface mounted plastic components on an FR-4 substrate
- On-chip address latches for direct interface to the IDT79R3000 CPU
- Inputs/outputs directly TTL compatible
- Single 5V (±10%) power supply
- Multiple ground pins for maximum noise immunity

FUNCTIONAL BLOCK DIAGRAM



PIP
TOP VIEW

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DESCRIPTION:

The IDT7MB6074 is a dual-banked 16K byte instruction cache and 16K byte data cache for the IDT79R3000 CPU. The IDT7MB6074 uses 8 IDT71586 (4K x 16) high speed CMOS latched static RAMs on a multilayer epoxy laminate substrate (FR-4). Extremely high speeds are achieved using IDT's high performance, high reliability CEMOS™ technology. The construction and specifications of this module have been optimized to suport its use as a complete instruction and data cache for the MIPS R3000 (RISC CPU).

The IDT7MB6074 is organized as two separate banks of static RAM with on-chip address latches. The two banks share a common 12-bit address bus and a common 64-bit data bus. The chip slect, write enable, RAM output enable and latch enable controls for the two banks are brought out separately to support interleaved access.

This module is designed to facilitate the implementation of the highest performance caches for the IDT79R3000 architecture while consuming minimum board space. As part of a family of pin compatible caches, the IDT7MB6074 provides the optimum solution for customers requiring a 16K byte instruction cache and a 16K byte data cache.

The pent in-line package (PIP) configuration allows 160 leads to be placed in five rows on a horizontal mount package 3.5 inches long, 1.4 inches wide and 350 mils tall. All inputs and outputs of the IDT7MB6074 are TTL compatible and operate from a single 5V power supply.

PIN NAMES

D_0 - D_{63}	Data Inputs/Outputs
A_0 - A_{11}	Addresses
$\overline{CS}_1$ - $\overline{CS}_8$	Chip Selects
$\overline{WE}_1$ - $\overline{WE}_8$	Write Enables
$\overline{OE}_1$ - $\overline{OE}_8$	Output Enable
LE_1 - LE_4	Latch Enables
Vcc	Power Supply
GND	Ground

2807 tbl 03

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Integrated Device Technology, Inc.

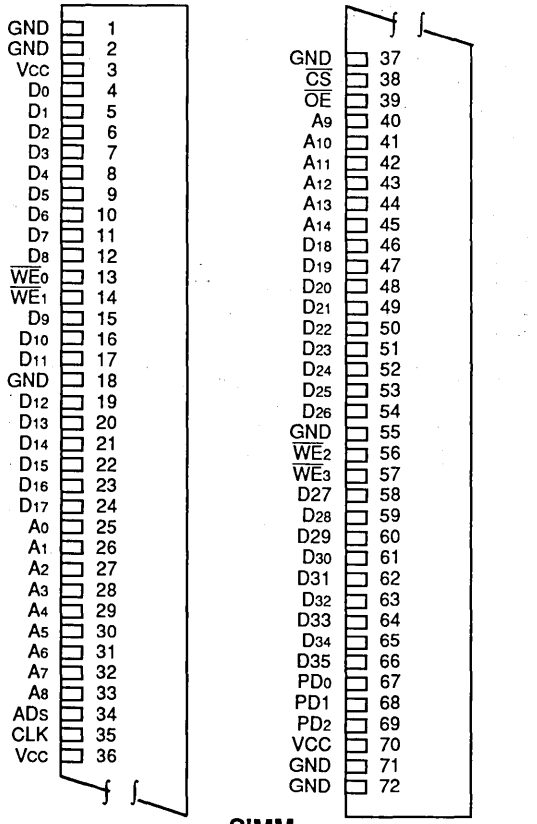
128K BYTE SECONDARY CACHE MODULE FOR THE i486™ MICROPROCESSOR

PRODUCT PROPOSAL IDT7MP6086

FEATURES:

- High density 128K byte direct mapped secondary cache module
- Family member of pin compatible i486 cache modules
- Uses the IDT71589 32K x 9 CacheRAM™ with burst counter and self-timed write
- Matches all timing and signals of the i486 processor
- Operates with i486 speeds of up to 40MHz
- 72 lead FR-4 SIMM (single in-line memory module)
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible
- Multiple ground pins for maximum noise immunity

PIN CONFIGURATION



SIMM FRONT VIEW

2807 drw 06

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DESCRIPTION:

The IDT7MP6086 is a 128K byte direct mapped secondary cache module.The IDT7MB6086 uses 4 IDT71589 32K x 9 CacheRAMs in plastic surface mount packages mounted on a multilayer epoxy laminate (FR-4) substrate. Extremely high speeds are achieved using IDT's high performance, high reliability CEMOS™ technology. This module is designed to facilitate the implementation of the highest performance secondary caches for the i486 architecture while using low speed logic devices and consuming minimum board space.

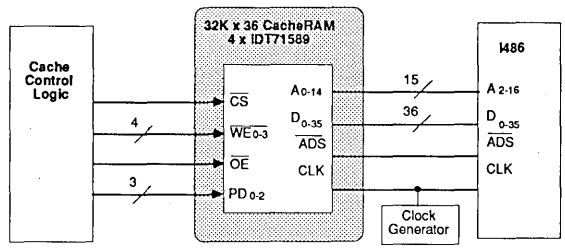
The IDT7MP6086 data RAMs contain a full set of write data and address registers. These registers are combined with the internal write abort logic to allow the processor to generate a self-timed write based upon a decision which can be left until the end of the write cycle.

An internal burst address counter accepts the first cycle address from the processor and then cycles through the adjacent four locations using the i486's burst refill sequence on appropriate rising edges of the system clock.

Three program identification pins are provided so that the system can uniquely identify the IDT7MP6086.

The single in-line package configuration allows 72 leads to be placed on a package 4.0 inches long, 0.55 inches tall and 0.25 inches thick. The IDT7MP6086 is available to interface with a 40MHz i486. All inputs and outputs of the IDT7MP6086 are TTL compatible and operate from a single 5V power supply.

FUNCTIONAL BLOCK DIAGRAM



2807 drw 07

PIN NAMES

D0 - D35	Data Inputs/Outputs
A0 - A14	Address
$\overline{CS}$	Data RAM Chip Select
$\overline{WE0}$ - $\overline{WE3}$	Data RAM Byte Write Enables
$\overline{OE}$	Data RAM Output Enable
CLK	Processor Clock
$\overline{ADS}$	Address Strobe
PD0 - PD2	Program Identification
VCC	Power
GND	Ground

2807 tbl 04

COMMERCIAL TEMPERATURE RANGE **SEPTEMBER 1990**

PROGRAM I.D. TABLE

PD_0	Cache Size	GND = 128KB
		NC = No Cache
PD_1	Wait States	GND = 0
		NC = 1
PD_2	Processor Speed	GND = 33MHz
		NC = 40MHz

NOTE:
1. NC = No Connect.

Integrated Device Technology, Inc.

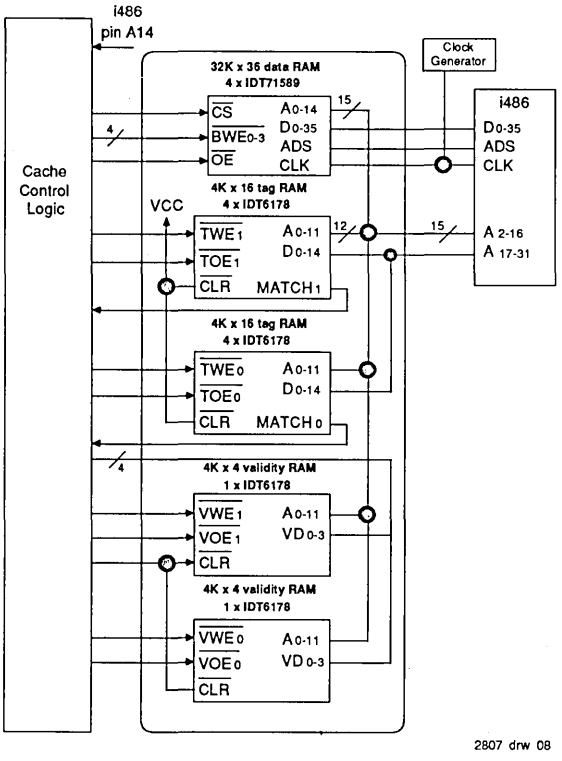
128K BYTE SECONDARY CACHE MODULE FOR THE i486™ MICROPROCESSOR

PRODUCT PROPOSAL IDT7MP6089

FEATURES:

- High density 128K byte direct mapped secondary cache module with tag and validity RAM
- Family member of pin compatible i486 cache modules
- Uses the IDT71589 32K x 9 CacheRAM™ with burst counter and self-timed write and IDT6178 4Kx4 cache tag RAM
- Matches all timing and signals of the i486 processor
- Operates with i486 speeds of up to 40MHz
- 110 lead FR-4 ZIP (zig-zag in-line memory module)
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible
- Multiple ground pins for maximum noise immunity

FUNCTIONAL BLOCK DIAGRAM



2807 drw 08

DESCRIPTION:

The IDT7MP6086, a 128K byte direct mapped secondary cache module with tag and validity RAM, is a family member of pin compatible i486 cache modules. The IDT7MB6089 uses 4 IDT71589 32K x 9 CacheRAMs, 10 IDT6178 4K x4 cache-tag/resettable RAMs, and logic in plastic surface mount packages all mounted on a multilayer epoxy laminate (FR-4) substrate. Extremely high speeds are achieved using IDT's high performance, high reliability CEMOS™ technology. This module is designed to facilitate the implementation of the highest performance secondary caches for the i486 architecture while using low speed programmable logic devices and consuming minimum board space.

The IDT7MP6089 data RAMs contain a full set of write data and address registers. These registers are combined with the internal write abort logic to allow the processor to generate a self-timed write based upon a decision which can be left until the end of the write cycle. An internal burst address counter accepts the first cycle address from the processor and then cycles through the adjacent four locations using the i486's burst refill sequence on appropriate rising edges of the system clock.

The IDT6178s provide the system with several tag and valid controls for further flexibility in cache operation.

The zig-zag in-line package configuration allows 110 leads to be placed on a package 5.65 inches long, 0.50 inches tall and 0.35 inches thick. The IDT7MP6089 is available to interface with a 40MHz i486. All inputs and outputs of the IDT7MP6089 are TTL compatible and operate from a single 5V power supply.

PIN NAMES

D_{0-35}	Data Inputs/Outputs
A_{2-31}	Address
$\overline{CS}$	Data RAM Chip Select
$\overline{BWE}_{0-3}$	Data RAM Byte Write Enable
$\overline{OE}$	Data RAM Output Enable
$\overline{TWE}_{0-1}$	Tag RAM Write Enable
$\overline{TOE}_{0-1}$	Tag RAM Output Enable
CLK	Processor Clock
$\overline{MATCH}_{0-1}$	Tag RAM Match
$\overline{CLR}$	Valid RAM Clear
$\overline{VD}_{0-3}$	Valid Data
$\overline{VOE}_{0-1}$	Valid Output Enable
$\overline{VWE}_{0-1}$	Valid Write Enable
ADS	Address Strobe
Vcc	Power
GND	Ground

2807 tbl 05

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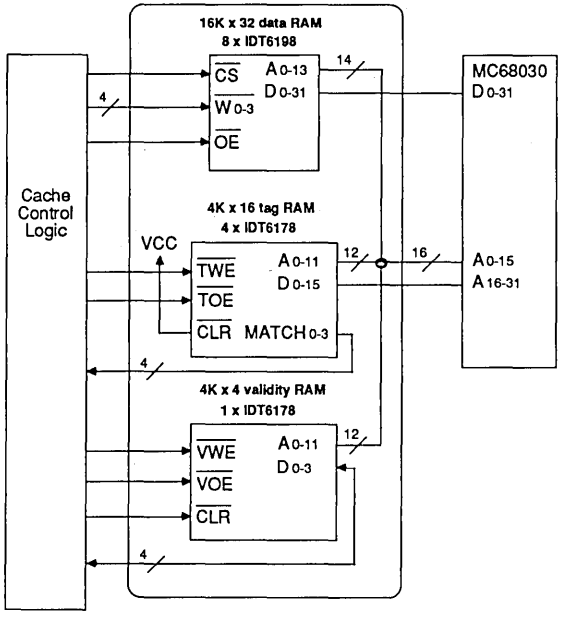
64K BYTE CACHE MODULE FOR THE MC68030 MICROPROCESSOR

PRODUCT PROPOSAL IDT7MP6030

FEATURES:

- High density 64K byte unified cache data and tag module
- 50MHz MC68030 operation
- 64K bytes with 16 byte line size
  - 16K x 32 data cache
  - 4K x 16 tag RAM
  - 4K x 4 validity RAM
- Write through architecture
- Matches all timing and signals of the MC68030 microprocessor
- Cache coherency/shared memory supported through MC68030 local bus arbitration
- 90 lead FR-4 ZIP (zig-zag in-line package)
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible
- Multiple ground pins for maximum noise immunity

FUNCTIONAL BLOCK DIAGRAM



2807 drw 09

DESCRIPTION:

The MC68030 can achieve its maximum potential through the use of a zero wait state cache memory, especially when running at speeds of at least 33MHz. The IDT7MP6030 is a fully integrated 64K byte direct mapped unified cache with tag and validity RAM. A 16 byte line size dictates a 4K deep cache-tag. The validity RAM contains the valid/invalid state of each of the four longwords within the selected cache line.

A direct mapped cache is used because the higher cache bandwidth more than compensates for a slightly lower hit rate compared with an n-way set associative cache. Hit/miss logic is left off board in order to give the designer maximum freedom in the implementation. A detailed timing analysis for the IDT7MP6030 is provided in IDT Application Note AN-46.

The IDT7MP6030 uses 8 IDT6198 16K x 4 static RAMs and 5 IDT6178 4Kx4 cache tag RAMs in plastic SOJ packages mounted on a multilayer epoxy laminate (FR-4) substrate. Extremely high speeds are achieved using IDT's high performance, high reliability CEMOS™ technology.

ThE IDT7MP6030 is designed to facilitate the implementation of the highest performance secondary caches for the MC68030 architecture while consuming minimum board space. The vertical zig-zag in-line configuration allows 90 leads to be placed on a package 5.3 inches long, 0.5 inches tall and 0.35 inches thick. All inputs and outputs of the IDT7MP6030 are TTL compatible and operate from a single 5V power supply.

PIN NAMES

D0 - 31	Data Inputs/Outputs
A0 - 31	Address
$\overline{CS}$	Data RAM Chip Select
$\overline{WE}$0 - 3	Data RAM Byte Write Enable
$\overline{OE}$	Data RAM Output Enable
$\overline{TWE}$	Tag RAM Write Enable
$\overline{TOE}$	Tag RAM Output Enable
$\overline{MATCH}$0 - 3	Tag RAM Match
$\overline{CLR}$	Valid RAM Clear
$\overline{VD}$0 - 3	Valid Data
$\overline{VOE}$	Valid Output Enable
$\overline{VWE}$	Valid Write Enable
Vcc	Power
GND	Ground

2807 tbl 06

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64K BYTE CACHE MODULE

PRODUCT PROPOSAL IDT7MP6059

FEATURES:

- High density 64K byte cache with tag
- Low profile 90 pin ZIP (zig-zag in-line vertical package)
- Fast access time: 15ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible
- Multiple ground pins for maximum noise immunity

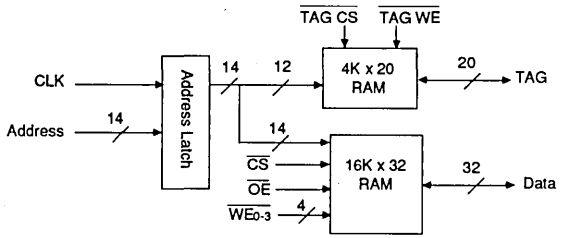
DESCRIPTION:

The IDT7MP6059 is a 64K byte cache module constructed on an epoxy laminate (FR-4) substrate using 8 IDT6198 16K x 4 static RAMs and 5 IDT6178 4Kx4 cache tag RAMs in plastic SOJ packages. Extremely high speeds can be achieved due to the use of static RAMs fabricated in IDT's high performance, high reliability CEMOS™ technology. The IDTMP6059 is available with access times as fast as 15ns with minimal power consumption.

The IDT7MP family of ZIPs, DSIPs and SIPs offers the optimum in packing density and profile height. The IDT7MP6059 is packaged in a 90 pin FR-4 ZIP (zig-zag in-line vertical package). The dual row configuration allows 90 pins to be placed on a package 4.7 inches long and 0.35 inches wide. At only 0.50 inches high, this low profile package is ideal for systems with minimum board spacing.

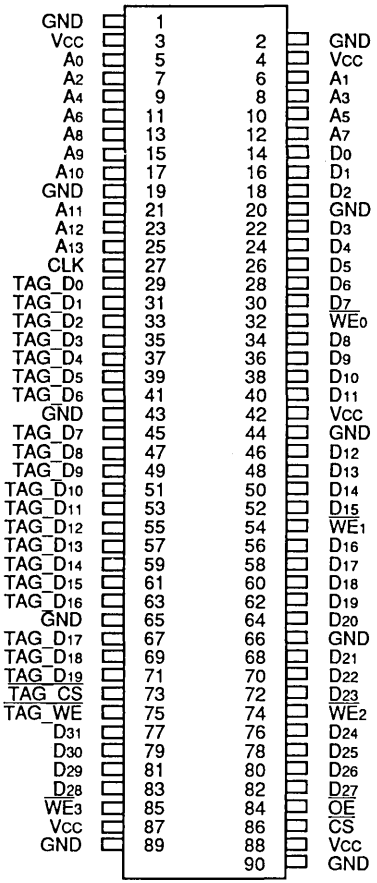
All inputs and outputs of the IDT7MP6059 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



2807 drw 10

PIN CONFIGURATION



ZIP
TOP VIEW

2807 drw 11

PIN NAMES

I/O0 - 31	Data Inputs/Outputs
A0 - 13	Address
$\overline{CS}$	Chip Select
$\overline{WE}$0 - 3	Write Enables
$\overline{OE}$	Output Enable
CLK	Processor Clock
$\overline{TAGWE}$	Tag Write Enable
$\overline{TAGCS}$	Tag Chip Select
Vcc	Power
GND	Ground

2807 tbl 07

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Integrated Device Technology, Inc.

16-BIT FOUR-PORT RAM-BASED MATRIX MULTIPLICATION ENGINE MODULE

PRODUCT PROPOSAL IDT7M900V

FEATURES:

- Complete matrix multiplication engine building block
- Extremely high performance:
  Commercial- 30ns clock cycle time (max.)
  Military - 40ns clock cycle time (max.)
- Independent computational operations and I/O access
- 128 pin quad in-line module package (QIP)
- Semiconductor components manufactured using IDT's high performance CEMOS™ technology
- Modules available with semiconductor components compliant to MIL-STD-883, Class B

DESCRIPTION:

Matrix multiplication is one of the most often used operations in DSP algorithms. In addition, matrix multiplication is the basic operation at the heart of computer graphics. For example, changing the position , orientation and size of objects in a drawing requires a geometrical transformation which is generally represented by a series of matrix multiplications. In high performance systems, a matrix multiplication engine (MME) such as the IDT7M900V is necessary to facilitate the operation.

The IDT7M900V consists of 2 IDT7052 2K x 8 four-port RAMs, one IDT7210 16 x 16-bit multiplier-accumulator, and four IDT7383 16-bit ALUs surface mounted on a co-fired ceramic substrate configured as a 128 pin quad in-line module package. With the IDT7052 four-port SRAM, system designers can considerably improve the performance and simplify the implementation of an MME versus a conventional single-port RAM implementation . The IDT7210 can do either multiply or multiply-accumulate function. Operands at I/O ports are all 16-bit, but 32-bit precision is preserved at internal computation. A mode control pin allows user to select data format as two's complement or unsigned number. All the internal registers can be clocked to provide pipelined architecture, in which multiplication results are generated every clock cycle.

All inputs and outputs of the IDT7MP6030 are TTL compatible and operate from a single 5V power supply. All IDT military module semiconductor components are compliant to the latest revision of MIL-STD-883, Class B, making them ideally suited for applications demanding the highest level of performance and reliability.

PIN NAMES

D_{0-15}	I/O Databus
CLK	Clock
AC_{0-47}	Address Generator Controls
F_{0-15}	Address Generator Flags
RC_{0-15}	Four-port RAM Control
MC_{0-10}	Multiplier-Accumulator Control
V_{CC}	Power
GND	Ground

2807 tbl 08

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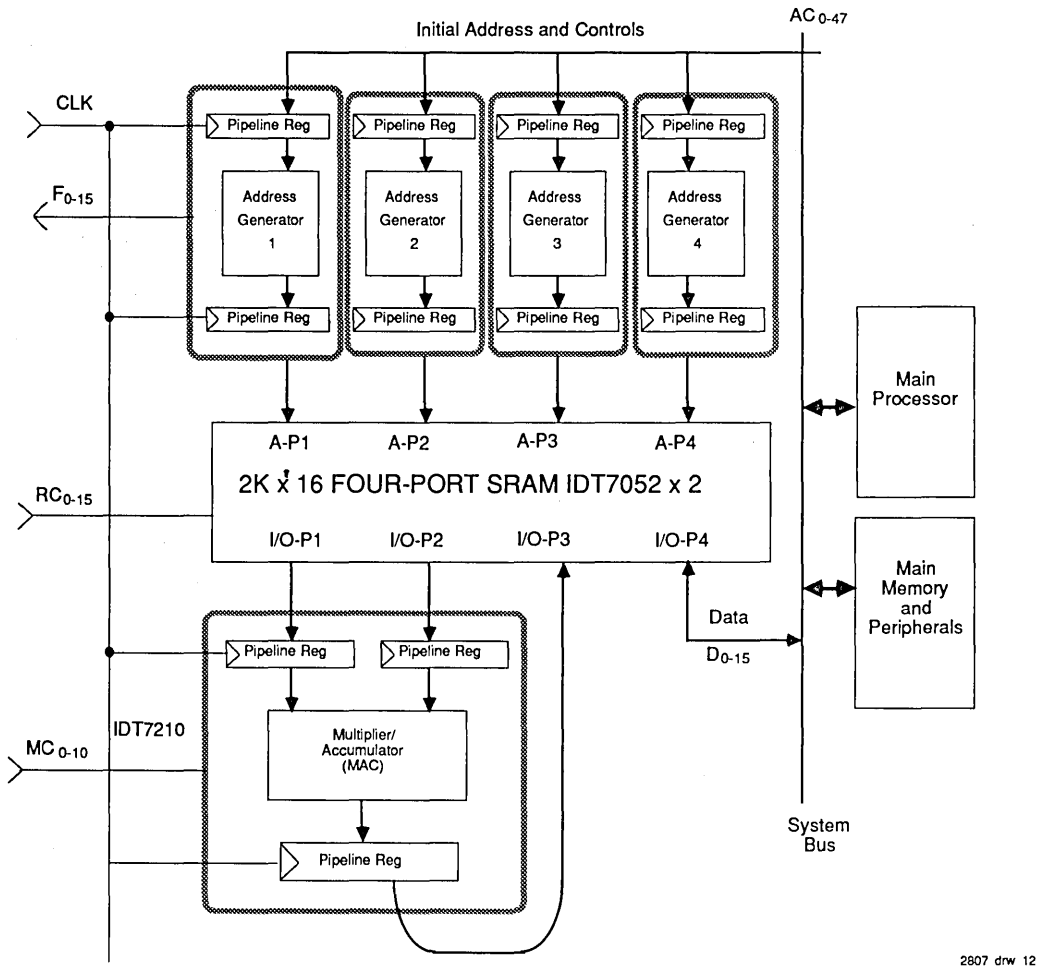
BLOCK DIAGRAM



Integrated Device Technology, Inc.

8K x 36 FIFO MODULE

IDT7M2001

FEATURES:

- First-In/First-Out memory module
- Asynchronous and simultaneous read and write
- Configurable as 8K x 36 or 16K x 18 unidirectional or 8K x 18 bidirectional FIFO
- Multiple status flags: Full, Empty
- Ultra-high-speed: 40ns access time
- Fully expandable by both word depth and/or bit width
- Dual-port zero fall-through time architecture
- Available in high-density 108-pin quad in-line FR-4 package

DESCRIPTION:

The IDT7MB2001 is a FIFO module that consists of eight IDT72041s (4K x 9). The IDT72041 is a dual-ported memory that utilizes a special first-in/first-out algorithm that loads and empties data on a first-in/first-out basis.

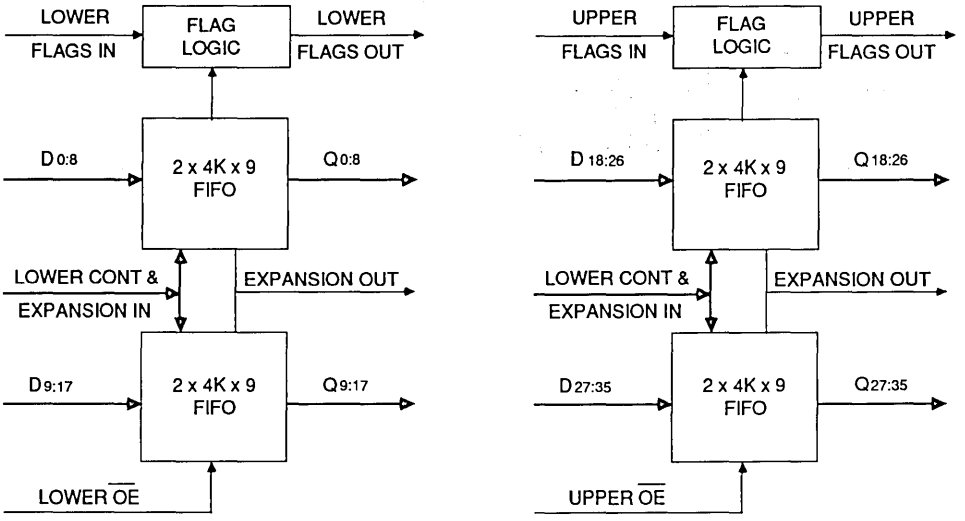
The IDT7MB2001 is user-configurable in three modes:
- An 8K x unidirectional FIFO, or
- A 16K x 18 unidirectional FIFO, or
- An 8K x 18 bidirectional FIFO.

In all three modes, the module offers two flags, Full and Empty, to prevent data overflow and underflow. Expansion logic of the IDT72041s allows wider and/or deeper FIFOs to be created using multiple devices without external logic.

The module also allows asynchronous and simultaneous read and write operations. The dual-port RAM array allows zero fall-through time and a ninth bit is provided for every byte to store parity.

Access time is as fast as 40ns. The module is offered in a high-density 108-pin quad in-line package.

FUNCTIONAL BLOCK DIAGRAM



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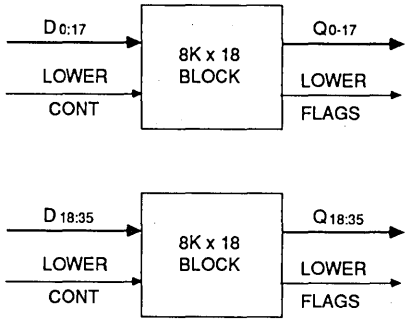
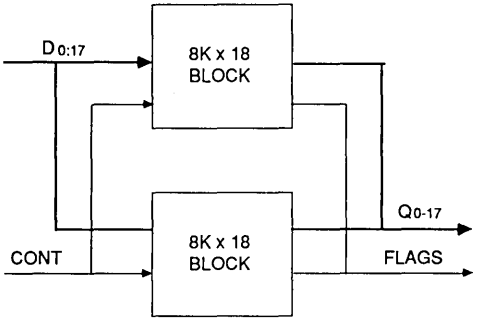
FUNCTIONAL BLOCK DIAGRAM (Continued)

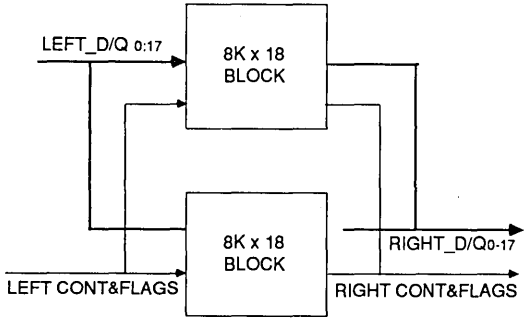
8K x 36



16K x 18



8K x 18 BIFIFO



2807 drw 14

Integrated Device Technology, Inc.

36-BIT TO 9-BIT BIDIRECTIONAL FIFO MODULE

IDT7M2002

FEATURES:

- First-In/First-Out memory module
- Asynchronous and simultaneous read and write
- 36-bit data bus on one side; 9-bit data bus on other side
- All logic required for conversion between 36- and 9-bit buses included on board
- 4K x 36-bit to 16K x 9-bit deep
- Selectable LSB or MSB first on 9-bit side
- Bidirectional
- Latching transceiver for LS 8 bits between the two buses
- Total cycle time 45ns

DESCRIPTION:

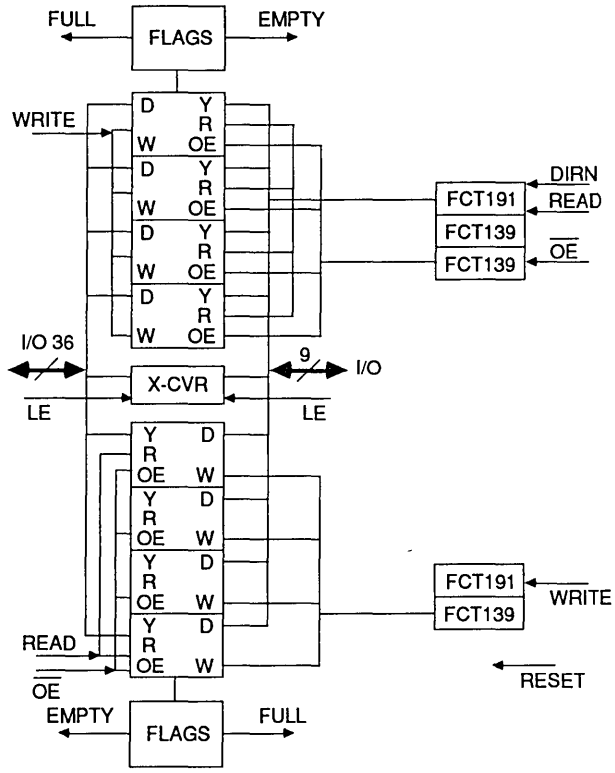
This module is a FIFO that has upt to 8 IDT72041s (4K x 9) on board. The module is bidirectional with 4K x 36 transforming to 16K x 9 on one side and back to 4K x 36 on the other side. All logic necessary to control the conversion between 36 and 9 bits is included on the module.

On the 9-bit side, there is a DIRN pin which determines whether the 36 bits of data is presented to the 9-bit side's most significant byte first or least significant byte first and, conversely, whether the 9-bit side data is being entered MSB or LSB first.

Included on-board is an 8-bit transceiver with separate latch enables for each side to allow the passing of status between the buses.

Access time is as fast as 40ns. The module is offered in a high-density 108-pin quad in-line package.

FUNCTIONAL BLOCK DIAGRAM



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Integrated Device Technology, Inc.

UNDERSTANDING THE IDT7201/7202 FIFO

APPLICATION NOTE AN-01

by Michael J. Miller

INTRODUCTION

This article discusses several different types of FIFO queues, their implementation, their performance and their use. Data, or information in computers, is processed as words or bytes in a predominantly serial fashion. There are producers and consumers of information that are connected by busses. Often there is a mismatch in the rate at which data is produced and the rate at which it can be accepted. The data is therefore buffered in serial lists until it can be used. The serial lists are stored in memory and require overhead to maintain them. These First-In-First-Out (FIFO) structures can be implemented at many levels from all software to all hardware. The software implementations are often the most flexible but yield the lowest performance. The hardware implementations, while less flexible, give the highest performance.

QUEUES

The elements of any computer or controller can be divided into three categories in relation to information: transformation, storage and transfer. Logic gates transform and combine information, memory elements store information and wires transfer information between the other elements.

Memory can be viewed as an element which transfers information with respect to time. The simplest of memory elements are latches and registers. RAMs are dense arrays of latches. While RAMs allow for dense information storage, they require an address to access individual pieces of information in the array. Therefore, addresses (information) must be generated and stored in order to access the desired information. The addresses are stored in programs and data structures such as linked lists.

Queues are a special organization of dense arrays of latches. Queues are a linear organization of groups of latches. Access to the linear string is restricted to either end. While RAMs allow for random access of any data in the array at any point in time, they require address inputs. Queues on the other hand, don't have an address thus avoiding the address generation and storage overhead. Queues can be divided into two categories: FIFOs and LIFOs.

Queues can be observed in the world about us. FIFO is an acronym for "First-In-First-Out". They can be observed in a bank line-up where customers enter at the end of a line, and after some wait, are serviced at the other end. The FIFO queue provides a mechanism by which customers which arrive at an erratic rate can wait until a teller can accommodate them.

LIFO is an acronym for "Last-In-First-Out". We can observe this phenomenon in the work place. As a person is working at a desk, interrupts occur. A higher priority interrupt such as a phone call or a request from people higher in management will cause the person to drop the work on the desk and start a new task. When the higher priority task is accomplished, the interrupted task on the desk is resumed. Depending on how many interrupts of sequentially higher priority tasks come in during the day, the stack of tasks on the desk grows. Another time honored example is the stacks of trays at the cafeteria. As trays are washed they are placed on a spring loaded elevator which sinks down to accommodate the new trays. When new customers enter the food line, trays are removed from the stack.

As can be seen in the above examples, queues are used to buffer between the flows of consumers and distributors of services. Groups of computing elements can be divided into consumers and producers of information with rates that must be matched. For example, a rotating Winchester disk is a source of information that must be serviced at a rate that may not be easily matched by the CPU which is consuming the information through the use of a data bus.

SIMPLE FIFO

The implementation of FIFOs is varied and presents many trade-offs. The simplest design treats the FIFO as a fixed number of memory elements in a linear array. When data is

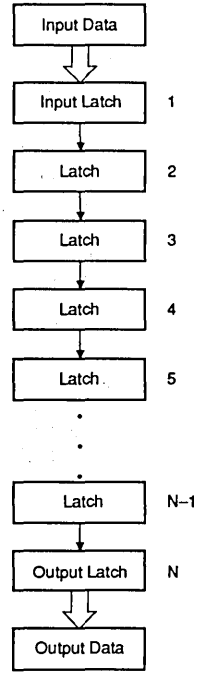

Figure 1. Hardware Implementation of a Fixed Length FIFO

written (pushed) in at one end, all of the rest of the elements shift their data over to their neighbor at the same time. One can visualize (Figure 1) the structure as a shift register. The same structure can be implemented in software where the program manages an array of memory locations in RAM. To push data into the queue the program must first start by moving the contents of the next to the last location into the last location. The algorithm continues from the last to the first location. When all of the data has been rippled down, the first location in the queue will be vacated. The data to be pushed into the queue is written into that vacated location.

An improvement in the software solution could be made with the introduction of a pointer. A pointer is a variable which contains an address. The pointer would identify a location from which to read the output of the FIFO. When a new piece of information is written, it would go into the location identified by the pointer after which the pointer would be incremented. The pointer now points at the new output data. When the pointer reaches the end of the array, the next increment would be replaced by setting the pointer to the beginning of the array. The obvious advantage is that the program does less work and therefore is faster. This software technique is called a circular queue with one pointer. (See Figure 2.)

FIXED LENGTH FIFO: NO FALL-THROUGH

The FIFO described previously is called a Fixed Length FIFO and has the characteristic that it takes N cycles for a piece of information that was placed into it to emerge out of it. The number N is the number of locations in the FIFO. This implementation also has the characteristic, that when first started after power up, it will produce unknown data for N cycles until the first valid data arrives at the output. The latency is therefore N read/write cycles. The fixed length FIFO does not allow for differences between the rate of input and output rates. This type of FIFO is used where the arrival of data at the output is delayed to match parallel paths in a pipelined system.

VARIABLE LENGTH FIFO

The variable length FIFO solves the rate mismatch problem, but requires more overhead to implement. Where the fixed length FIFO is like a steel pipe which information is fed through and has a fixed number of locations, the variable length FIFO is like a rubber hose that can stretch, holding from one to many items. The items are removed at will instead of being required to at write time. Every variable length system has a limit and therefore must signal when it is at capacity and must be serviced before bursting.

FALL-THROUGH FIFOS

In the real world of silicon and aluminum there is no such thing as rubber. Variable length FIFOs must therefore be implemented using fixed length queues. This fact creates some limitations which translate into trade-offs. The traditional hardware implementation uses two sets of shift registers. One set is used to hold the data in much the same way as in the fixed length FIFO. Data that is placed in the top emerges at the bottom. There is a second shift register that functions in parallel. The second shift register contains flags that indicate whether the associated data element at the same chronological position in the data queue is valid data or not. When data is written into the top location of the data queue, a true flag is placed into the "valid bit" queue. The variable length quality is achieved by allowing the data and its associated valid bit to "sink down" into the next location below it if there is no valid data in that location (see Figure 3). In this way valid data "sinks" to the bottom of the queue and stacks up in much the same way as pearls being dropped into a narrow tube tilled

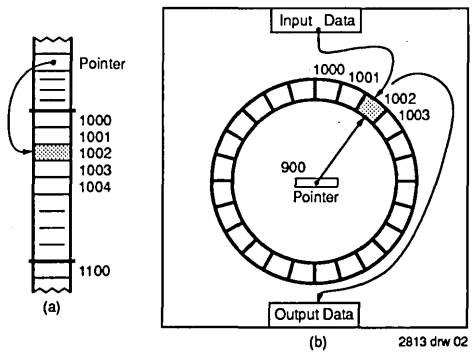

Figure 2. Circular Queue with One Pointer
a) as it is in memory
b) logical view

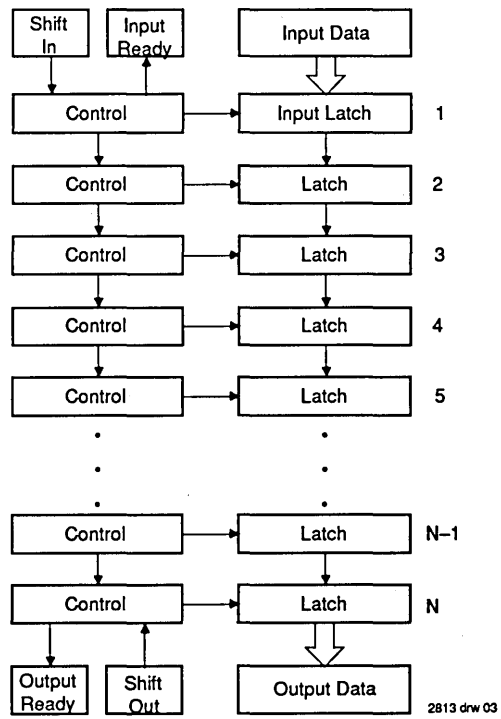

Figure 3. Classical FIFO Architecture

with oil. The clocking of data down through the queue is controlled by an internal self-generated clock. The maximum latency or fall-through time is a product of the number of cells in the queue and the internal clock cycle length. This approach meets the requirement that differing rates may be accommodated. The valid bit data is brought out in parallel with the queue data. The valid bit data tells the consumer when valid data is present, thus avoiding the start-up period of invalid data as in the previous implementation of the fixed length FIFO. Examples of this approach are the shorter FIFOs such as the MMI67401. Fall-through FIFOs tend to have very long undesirable fall-through times if the FIFO is deep.

The software approach could be designed to mirror the typical hardware approach by working with two arrays. One for the data and one of the valid bits. That approach uses too much memory. An alternate could use a wider array which carried the valid bit with the data. The algorithm would then start at the end of the array and pass to the front, advancing all elements which were valid to the end of the array until all valid data was collected at the end of the array. This approach would be very costly in terms of CPU cycles for what is achieved. There is a fall-through latency which is a product of the time to execute the updated software loop times the number of locations in the queue.

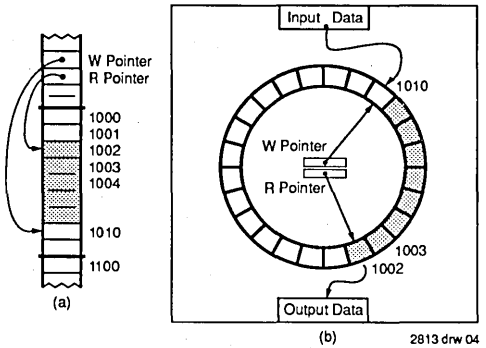

Figure 4. Circular Queue with Two Pointers
a) as it is in memory
b) logical view

TWO-POINTER FIFO

A more economical approach would utilize two pointers and one array that was as wide as the data. One pointer would point to the location at which new data is written into. The second pointer identifies where data is to be read from for output from the queue (see Figure 4). When either pointer is used to access a location, it is incremented. When a pointer is incremented to the last location in the array, the next increment will be substituted with a reset of the pointer to the beginning of the array. The logical view of this structure is a circular queue with a read and a write pointer. This approach results in a much shorter fall-through time while still achieving the variable length feature. The fall-through time is the time that it takes to invoke the software to write the data into the queue, plus the time that it takes to invoke the software to read the data out of the queue. While this is much better than the previous approach, it still requires a reasonable amount of time to accomplish.

TODAY'S HIGH SPEED FIFOS

The hardware approach, which is used by the IDT7201 and IDT7202 devices, utilizes the software concepts demonstrated in the previous approach but at very fast hardware speeds (50ns typical military). The block diagram in Figure 5 shows the two pointers which locate where reading and writing is to take place in the queue (RAM Array). There is added logic which provides status about the queue: empty ($\overline{EF}$) half full ($\overline{HF}$) and full ($\overline{FF}$) (¯ means an active LOW signal). Two pins, one input($\overline{XI}$)and one output ($\overline{XO}$) provide for unlimited expansion while still maintaining the 50ns fall-through time. This part functions identically to the software approach utilizing the two pointers. When either pointer reaches the last location, it is reset to the first location, thus achieving a circular queue via a wraparound approach. The status flags reflect the count of how many valid pieces of data are in the queue. After the device is reset, the empty flag ($\overline{EF}$) is asserted. As soon as a datum is written into the queue, the empty flag is deasserted. The empty flag is not asserted again until all pieces of data have been read from the queue. When the count of data elements reaches one-half the number of locations in the RAM array, the half full flag ($\overline{HF}$) is asserted. If a read is performed which reduces the count to just below the half way count, then the ($\overline{HF}$) is deactivated. The full flag is asserted when the count of data elements is exactly equal to the number of locations in the RAM array, thus flagging that there are no more empty locations in the queue.

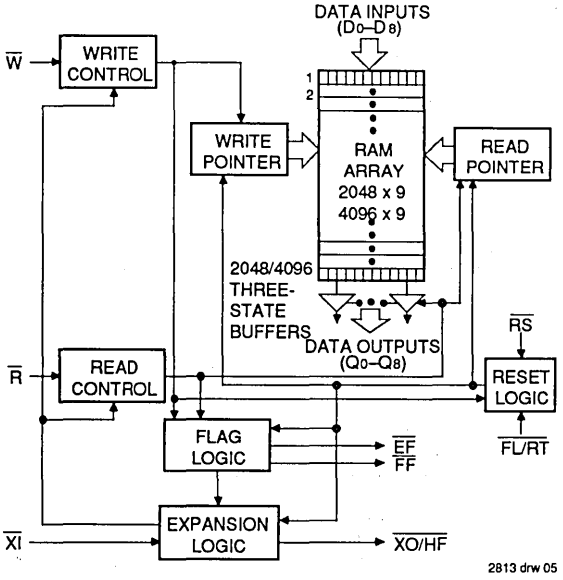

Figure 5. Functional Block Diagram of IDT7201/7202 FIFO

WIDER FIFOS

Applications may vary widely as to the width and depth of the FIFO required. If an application's maximum requirement is 1024 locations or less and 9 bits in width or less, then the IDT7202 will fit. Wider word widths can be achieved by connecting two or more devices in parallel (control signals). The status flags can be detected from any one device because each device is working in lock step parallel. Figure 6 shows an example of an 18 bit-word composed of two IDT7201/7202 devices. The older classical architecture would require more external circuitry to match the Input Ready and Output Ready signals to account for differences in the internal self-generated clock frequencies. RAM-based FIFOs, such as the IDT7201/7202, do not have this problem.

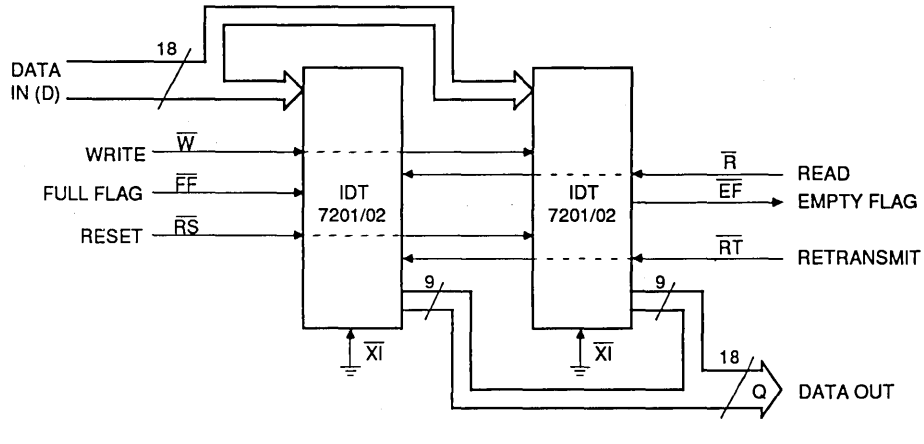

Figure 6. IDT7201/7202 FIFO Word-Width Expansion

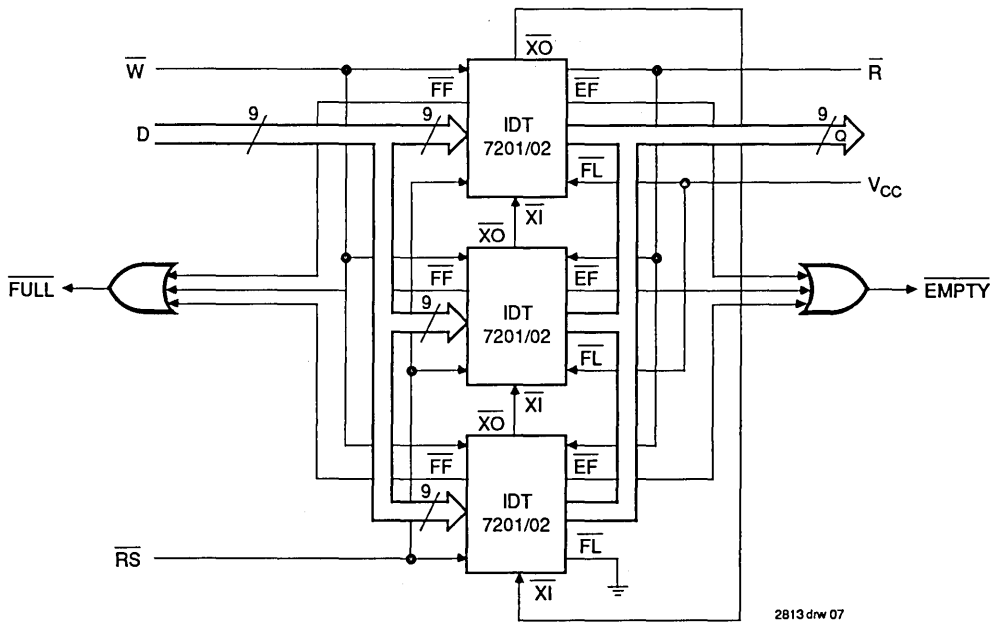

Figure 7. IDT7201/7202 FIFO Word-Depth Expansion

DEEPER FIFOS

Some applications require deeper FIFOs. In the older architecture, deeper FIFOs mean longer fall-through times because they are connected end to end. The time increases in direct proportion to the number of devices. For example two devices yield a maximum fall-through time of twice that of one device. This can make some applications of FIFOs impractical or totally unuseable.

With the two pointer approach used in the IDT7201/7202, the data input busses are connected together and the data output busses are common. This produces a parallel architecture (see Figure 7) as opposed to the serial approach above. The parallel structure is analogous to cascading standard RAM devices to achieve deeper memories.

Since FIFOs do not have chip selects and external decoding mechanisms, the task of choosing which device is selected must be provided for internally. The control (in the IDT7201/7202) is achieved through a unique serial structure. The first (or master) FIFO is identified by grounding the $\overline{FL}$ input. All other FIFOs in the structure must have the $\overline{FL}$ input pulled up to V_{CC}. The $\overline{XO}$ output of the first FIFO is connected to the $\overline{XI}$ input on the next FIFO in the queue. The $\overline{XO}$ output of that FIFO is connected to the $\overline{XI}$ input of the next and so on until the $\overline{XO}$ output of the last FIFO is connected to the $\overline{XI}$ input of the first FIFO (see Figure 7).

After reset, the active read and write pointers are in the first device. When the write pointer has progressed to the end of the first FIFO device, it outputs a pulse on $\overline{XO}$ which activates the write pointer at the beginning of the next device and simultaneously deactivates the write pointer in the first device. Thus, write enable control is passed to the second device. When the active read pointer reaches the end of the first device, it terminates and activates the read pointer in the next device with another pulse on the $\overline{XO}$ output of the first device. Figure 8 shows the progression of read and write pointers across two devices.In this ring structure, the read pointer is always chasing the write pointer. The pointer enable crosses the device boundaries via sending an $\overline{XO}$ pulse onto the next device. This continues in a circular queue fashion.

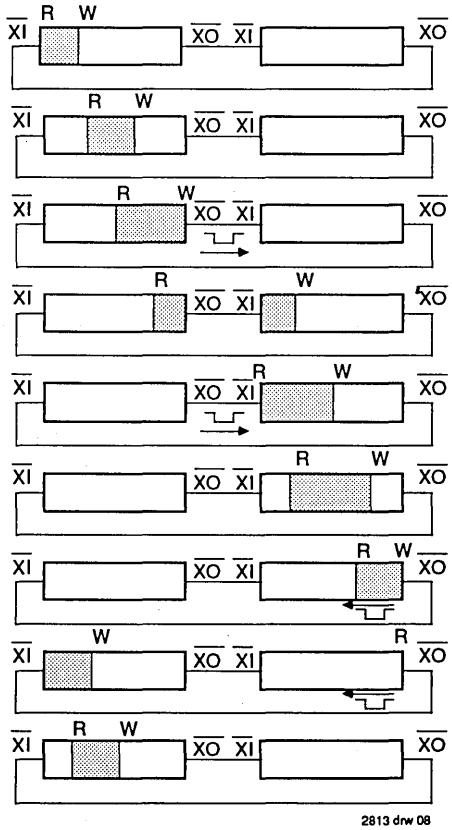

Figure 8. Example on $\overline{XO}/\overline{XI}$ Expansion Scheme

The IDT7201/7202 has been designed such that the read and write pointer can never cross over each other even in the cascade mode. The $\overline{XO}$ pulse is synchronous with read and write. When the last location is read or written, the $\overline{XO}$ output goes low with the read or write enable input and back high with the read or write enable. To see why there is no conflict even though reads and writes are asynchronous, the usage must be examined. The case of concern is when the FIFO is empty and the read and write pointers are at the last location. It must be realized that the consumer will not read until the empty flag is deasserted. The empty flag output will go high after the write pulse has gone high again thus ensuring that the $\overline{XO}$ pulse, indicating the write pointer, has been passed on to the next device. The consumer will then read the last location causing another pulse on $\overline{XO}$ which will transfer the read pointer (see Figure 9).

There is one special case regarding read flow-through mode (discussed below). In this mode the consumer can anticipate the write, by producer, by lowering the read enable input. In this case the $\overline{XO}$ input does not go low with read enable. When write enable is lowered, $\overline{XO}$ goes low. $\overline{XO}$ goes high with write enable. At this point the empty flag is cleared, thus signaling to the consumer to terminate the read after the appropriate period specified in the data sheet. During this period the $\overline{XO}$ output, which went high at the end of the write enable pulse, has lowered again. When the read enable is raised by the consumer, the $\overline{XO}$ output goes high. In this way two pulses on $\overline{XO}$ are assured (see Figure 9).

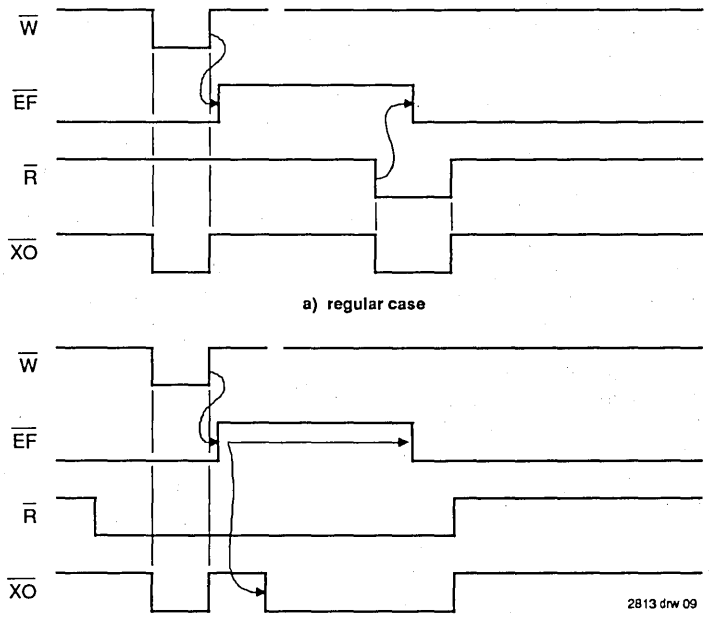

Figure 9. Generation on $\overline{XO}$ Output When the FIFO Is Empty
a) regular case
b) the read-flow through case

Two examples of the IDT7201/7202 in expanded depth configuration are available from IDT commercially. The IDT7M203/204 are Subsystems modules which incorporate onto one ceramic substrate four FIFO LCCs and the $\overline{EF}$ & $\overline{FF}$ "OR" gating to produce 2Kx9 and 4Kx9 FIFOs. The Subsystem module has a lead frame which pins out like the 28-pin 0.6 inch IDT7201/7202. This allows for a plug compatible 4Kx9 FIFO in one socket.

SPECIAL FEATURES OF IDT7201/7202

The architecture used in the IDT7201/7202 provides some features that distinguish it from FIFOs with other architectures. One outstanding feature is the dual port implementation of the RAM array. The RAM is designed in such a way that the read and write ports are separate, allowing for simultaneous asynchronous reads and writes with no hand shaking or arbitration. In the classical architecture the consumer and producer circuits must monitor ready flags for each access.

The IDT7201/7202 support a retransmit function. In the single device solution, the $\overline{FL}/\overline{RT}$ input may be pulsed low signaling a retransmit.

A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than 512/1024 writes are performed between resets. The retransmit feature is not compatible with Depth Expansion Mode and will affect HALF FULL FLAG ($\overline{HF}$) depending on the relative locations of the read and write pointers. For example in a communications application, during transmission of a message the receiver may request a retransmit of the message. This can be accomplished by always starting new messages at the beginning of the queue via a pulse on the reset input. If and when the retransmit request arrives the $\overline{FL}/\overline{RT}$ line is pulsed. The read pointer is repositioned at the beginning of the queue. The message producer may continue to write more of the same message into the queue as the retransmit of the message continues. The retransmit can happen as many times as desired. At the start of the next complete message, the reset line ($\overline{RS}$) must be pulsed after the successful acknowledge by the receiver. The reset ensures that the new message will be placed in the FIFO at the start of internal queue. It should be noted that when retransmit is possible, messages cannot be bigger than the maximum size of the queue. If the message is longer than the queue, even though the read pointer has progressed far enough to accommodate the extra data, resetting the read pointer back to the beginning with retransmit will produce data from the end of message instead of the beginning.

This architecture supports flow-through modes. In the read flow-through mode, when the buffer is empty, the consumer can anticipate the write by the producer at the other end by lowering the read input. When the empty flag ($\overline{EF}$) goes false the consumer circuitry can terminate the early read cycle by reading the data and deasserting the read signal. The read input must go high for a brief period in order to clock the read pointer. The read flow-through mode avoids the standard sequence of monitoring flag going high before hitting a read cycle.

The write flow-through mode is a mode that is employed when the FIFO is full. The producer can anticipate a read by the consumer by lowering the write input before the read. When the full flag ($\overline{FF}$) raises, the producer knows that the consumer has read a location, thus freeing up a location that can receive the new data. The producer then raises the write input which actually writes the data into the RAM array. This flow-through mode avoids the overhead of monitoring the full flag before initiating a write cycle.

The IDT7201 is pin and functionally compatible with the Mostek MK4501 thus serving as an alternate source. The IDT7202 gives the same functionality as the IDT7201 but is twice as deep (1024x9). The IDT7202 is the largest FIFO made with the zero fall-through time architecture making it the logical choice for FIFO applications.

SOFTWARE VERSUS HARDWARE SOLUTIONS

With every application involving a computer or programmed controller, the designer can trade off between performing certain functions in software or hardware. In general, the software solution is a more flexible design (easily changed) but performs the task more slowly. The hardware solution is less flexible but performs the task very fast.

To clarify these concepts, a discussion of an application and how it could be solved at the various levels from software to hardware is beneficial. A good example is a file server. The server could be connected to a Local Area Network (LAN) and, on the other side, to a Winchester disk drive. Both I/O connections demand attention at unpredictable intervals and must be serviced on demand or data is lost.

If the data rate of both interfaces is sufficiently low, a total software solution might be considered. The data rate would have to be low enough such that the software code could poll the status of either I/O port. As data arrives it could be placed into software FIFO queues. When a full record is buffered, then processing would commence. During the processing, the I/O ports must still be monitored as another user on the LAN might make a request (see Figure 10). It is doubtful that a total software solution could be designed for the server application that would have acceptable system performance.

The next approach to consider might be to include hardware interrupts. Interrupts allow for one task to be running and almost immediately switching to an I/O service routine. Interrupts are something like a hardware subroutine call. This scheme would use the interrupt mechanism to call routines to move data to and from the I/O ports and the software FIFO queues. The overhead of constantly polling the I/O port status flags would be eliminated, thus allowing for higher system performance. An asynchronous-type problem is introduced with interrupts. To use interrupts properly, the I/O service routines may be called at any instance. Therefore, the interrupt routines must be designed in such a way that they do not destroy data that the interrupted task might be using. Usually, the routines must be careful to save the state of the machine, perform their task and restore the state of the machine. The extra code to maintain the state of the machine is an overhead that is not in the polled solution. Worse yet, saving the state of the machine may be too much overhead to allow for an interrupt during a time-critical piece of code. Because interrupts may not be acceptable at certain points in the code, the programmer must insert code to disable and re-enable interrupts around the critical sections.

Where the polling scheme provides a solution which has a more easily definable sequence of execution, the interrupt solution is indefinite. The programmer must spend a lot more

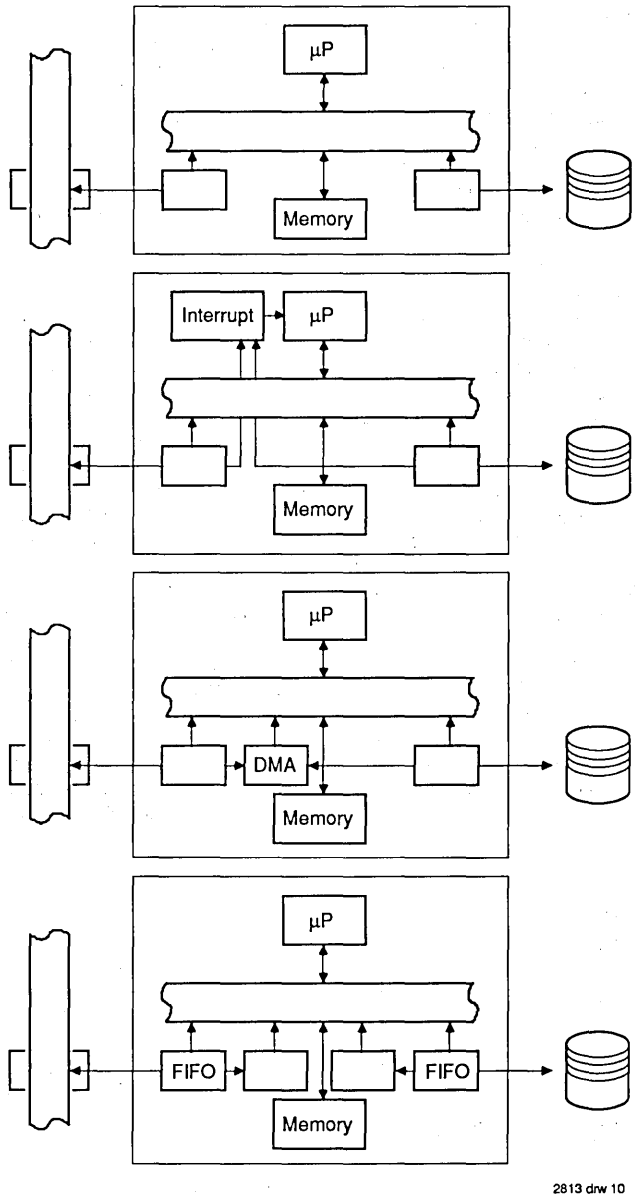

Figure 10. Example Solutions for File Servers

time proving that all possible sequences caused by random interrupts will produce desirable results. Because interrupts may not be acceptable at certain points in the code, the programmer must insert code to disable and re-enable interrupts around the critical sections. The interrupt disable solution not only cuts performance by not accepting I/O during some periods, but also adds more overhead with the maintenance of the interrupt enable mechanism. In some sense, interrupts can be to software what the meta-stable flip-flop problem is to hardware.

The interrupt solution can be moved out of the software and more into the hardware realm through the use of a technique

called Direct Memory Access (DMA). The DMA solution is provided by a block of circuitry which monitors the I/O ports. When the port requires attention, the DMA logic interrupts the current task at the bus transfer level and steals a memory cycle to transfer the data to or from the port and the FIFO queue in memory. The task that is running on the processor misses only a few memory cycles now and again which is much less than in the interrupt scheme where a whole subroutine of many memory cycles was executed to transfer each element of data. The DMA solution is not for free. DMA controllers are complex devices which must be programmed as well as designed into the bus structure. The DMA mechanism can only serve one source at any given instance in time thus still being a bottleneck in throughput.

So far, each solution proposed has moved the mechanism that feeds data to or from FIFOs in program memory away from the software and closer to the I/O port. The memory bus still remains the bottleneck because both FIFO queues are in memory. To simplify and improve performance, hardware FIFOs such as the IDT7201/7202 can be used. The processor would interface to the FIFO through an I/O port as before, but the FIFO would now be between the I/O port and the rest of the hardware. The software could then service the data at a steady rate and be sure that data was not lost without the problems or overhead of more complicated schemes such as interrupts or DMA.

Because the queues are between the controller and the peripheral the peripheral can load or read the queue without interrupting the controller. Since the controller is not involved with maintaining both queues, there is no possibility of lost data because one queue was being serviced while data for the other queue arrived. For these reasons the hardware FIFO represents the highest performance solution.

If the designer uses large FIFOs like the IDT7202 there is a minimum of device count. Assuming 2 FIFOs (transmit and receive)for each I/O port gives a count of four 28-pin devices for the FIFO solution. The DMA solution would at least be one 40-pin device and several bus buffer/control devices. The interrupt solution would require a similar parts count to the DMA solution. Therefore the FIFO solution is not only the highest performance solution but usually has the lowest part count of the hardware solutions.

COMMUNICATIONS-MULTIPLEXOR APPLICATION

Another example of a rate mismatch problem is shown in a CRT terminal and CPU interface. In order to not load the CPU with the burden of monitoring the UARTs of multiple CRTs and printers a communications controller is employed. The controller can serve as a communications multiplexor and data concentrator (see Figure 11).

As the controller receives characters it must buffer them such that if multiple characters are received close together from several terminals, they will not be lost as more characters come in. The natural structure to store them in is a queue of the FIFO type. The CPU will then need to respond to the characters. If the controller is inputting other characters, the CPU should not have to wait until the controller is done. Therefore, a FIFO can be employed on the transmit side as well as the receive side. To make the design simple, two sets of FIFOs could be placed between the CPU and controller. When characters are received they are placed in one end of a FIFO and read from the other end by the CPU. As the CPU prepares characters for transmission, it places them in a FIFO going the other direction. The controller then reads them from the other end of the transmit FIFO and sends them out through the UART.

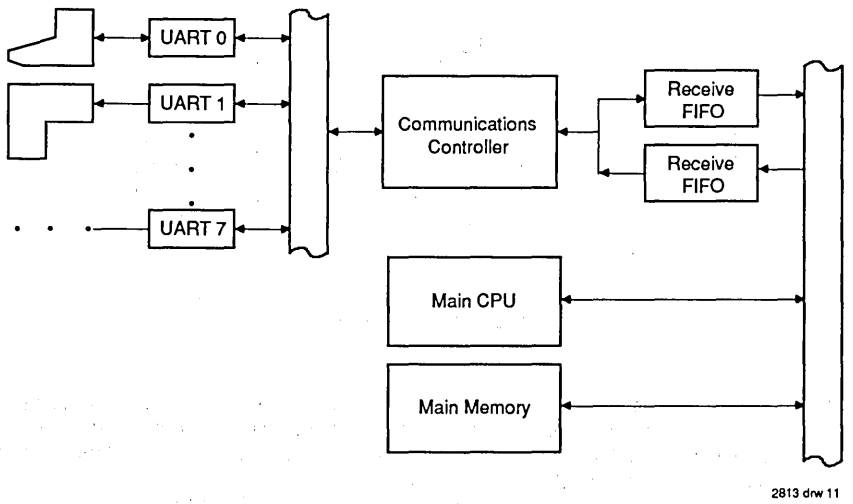

Figure 11. Communications Controller Example

Conceivably, there could be a pair of FIFOs for each UART. That way it would be easy for both the controller and the CPU to keep straight which characters correspond with which UART. While this provides for a large total of buffer space for characters it is more than needed when using a part like the IDT7201/7202. For eight UARTs, this scheme would require a minimum of sixteen FIFO devices. A better solution would be to use one FIFO device in either direction. If an IDT7202 were used, it could provide a maximum of up to 128 characters per UART if all the UARTs input at the same time and rate. While the two FIFO techniques would most likely provide plenty of buffering at a minimal device count, it presents the problem of which character belongs to which UART The solution is to make a wider FIFO which is 18 bits wide; thus using 4 devices instead of 16 devices for 8 UARTs. This would allow for a UART number to be placed in the FIFO along side each character. The remainder of the word could be used for flag status and command information between the CPU and the controller. For example, several of the bits in the FIFO word could indicate whether the character information was a character to send or BAUD change rate information.

The empty and full flags of the IDT7201/7202 FIFO would be used as status flags. For example the transmit buffer must be monitored from both sides. As the CPU prepares a character to transmit, it would first examine the full flag ($\overline{FF}$) to see if the FIFO is full. If the FIFO was full, it would delay outputting the character. If the buffer is not full then it would place the character in the FIFO. The empty flag ($\overline{EF}$) would be monitored by the controller. As soon as the CPU places a character into an empty FIFO the empty flag would change to not true. At this point the controller would know there was a character in the buffer which could be transmitted. The controller would read characters from the buffer as long as the empty flag was not true (buffer contains more than one character).

CONCLUSION

Hardware FIFOs are an economical memory organization to use when lists of data items are to be buffered. Because they do not require an address to access items in the list, there is less overhead in terms of circuitry and access time. The FIFO buffer is most often used as a "system rubber band" to stretch between the differing and fluctuating rates of different elements in a system. The IDT7201/7202 FIFO device features the newest RAM-based architecture and provides the latest in technology in terms of access time fall-through time and size, thus providing the most economical solution for today's design needs.

Integrated Device Technology, Inc.

USING HIGH-SPEED SERIAL-PARALLEL FIFOS THE IDT72103/72104

APPLICATION NOTE AN-15

By Robert Stodieck

INTRODUCTION

FIFOs are a common hardware solution in designs where data must be transferred between two subsystems with different characteristic data generation, transfer or usage rates. A common case is the serialization and de-serialization of data. Serialization is required for a variety of applications such as communication, data storage and display. The IDT72103 and IDT72104 parallel-serial FIFOs have been designed to address these applications.

The IDT72103/4 FIFOs are a RAM-based design with self-incrementing internal read and write pointers. This design results in very low fall-through times compared to older FIFO designs that are based on ganged shift registers. The fall-through time of a FIFO is the time elapsing between the end of the first write to the FIFO and the time the first read may begin. The first byte of data written into the IDT72103/4 FIFOs is available as soon as the write is complete and the Empty Flag is consequently de-asserted.

Similarly, the serial registers are not shift registers but bit wide memory arrays with self-incrementing pointers. The serial output word and the serial input word transfer data starting from the least significant bit. If only a partial word is transferred into the serial input register, the bits will be in the correct bit location in the serial input register and not shifted right or left.

PARALLEL OPERATING CONSIDERATIONS

Regardless of how a FIFO is designed or used, FIFO full and empty boundary conditions require special consideration from the system designer. FIFO reads and writes may occur completely asynchronously from each other unless the FIFO is completely full or empty. What happens when excess reads or writes occur after the FIFO is full or empty depends on the design of the particular device. If a FIFO is empty, then reading the FIFO again will produce data which is out of sequence or invalid. If the FIFO is full, writing data overwrites previously written data or loses the data being written.

The design of the IDT72103/4 FIFOs gates out write pulses once the FIFO is full and gates out read pulses once the FIFO is empty. Excess writes are ignored and thus do not overwrite valid data. Excess reads produce invalid data since the outputs of the FIFO are tri-stated when the Empty Flag is active, but do not read data bytes out of sequence.

The Full and Empty Flags signal the full and empty boundary conditions. An internal read cycle cannot begin until the Empty Flag is de-asserted and a write cannot begin until the Full Flag is de-asserted (Figure 1).

If the read signal is low prior to the de-assertion of the Empty Flag or the write signal is low prior to the de-assertion of the Full Flag, they cannot be allowed to transit high again until an appropriate minimum read or write pulse time has elapsed.

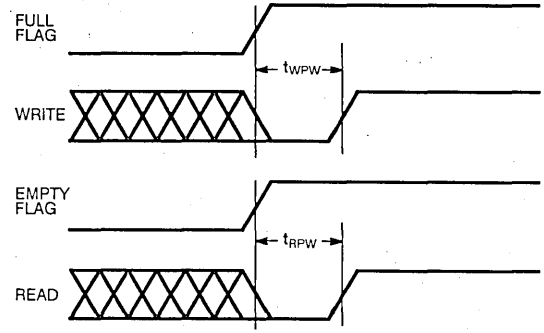

Figure 1. Parallel Read and Write Timing Following the De-Assertion of the Full and Empty Flags

Failure to observe this boundary condition timing produces internal read and write pulses of excessively short duration and may result in erratic operation.

The IDT72103/4 provide a full complement of flags which do not interact with the read and write signals. These provide the designer with flexible FIFO status indicators. They include, Empty + 1, Full - 1, Half-Full and Almost-Empty/Full. The Almost-Empty/Full Flag is asserted when the FIFO is less than 1/8th full and again when it is greater than 7/8th full.

The IDT72103/4 FIFOs can be expanded in depth to any level by cascading multiple devices. For depth expansion, the input and output buses are connected in parallel. The expansion output (XO) pin of the first part is connected to the expansion input (XI) pin of the next device in the cascade until all the parts are connected in a loop (Figure 2). The First-Load pin of one of the parts is tied to ground to identify it as the first device to be loaded in the cascade. All other parts have the First-Load pin tied to V_{CC}. The retransmit feature cannot be used in the depth expansion mode.

Empty Flag and Full Flag signals for the depth expanded cascade are derived from the individual FIFO Empty and Full Flag signals by logically ORing them together. The retransmit feature and the flags other than Empty and Full cannot be used in the depth expansion mode.

The IDT72103/4 FIFOs' retransmit feature allows data written to the FIFO one time to be read any number of times. The retransmit feature resets the read pointer to begin re-reading data from the first byte that was written after a reset pulse. This is particularly useful for applications such a video frame buffers which are written once and read many times.

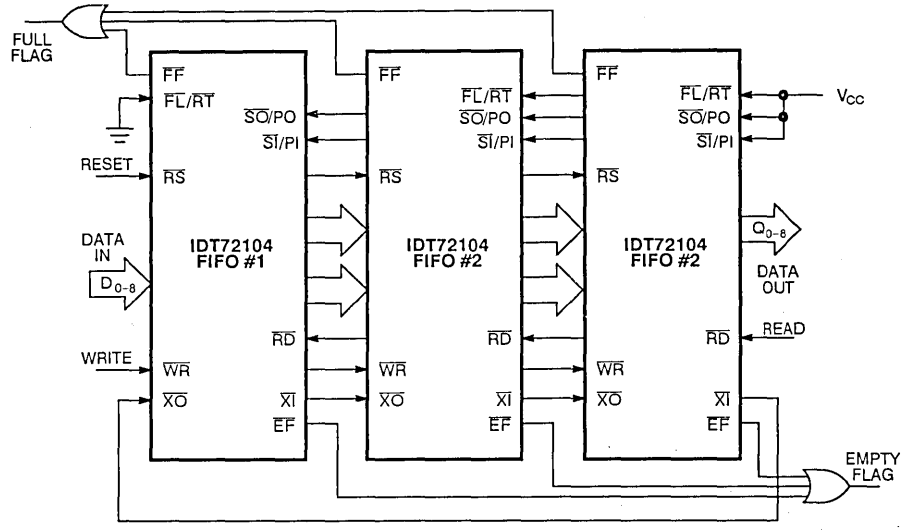

Figure 2. Parallel Depth Expansion to 12 Kilobytes

SERIAL TRANSFER AND EXPANSION – FLEXISHIFT™

The serial registers are bit wide memory arrays. Both serial width and serial depth expansion are facilitated by connecting the serial inputs and outputs in parallel. The serial output of an individual device is tri-stated when it is not active. Which serial input and serial output is active at a given moment is controlled through the expansion pins SOX (Serial Output Expansion), SIX (Serial Input Expansion), XO (Expansion Output) and XI (Expansion Input). Whether in an expansion mode or not, serial transfers always begin from the least significant bit.

The serial word width of the IDT72103/4 FIFOs may be programmed to be from four to any number of bits by using multiple parts (Figures 3 and 4). When used in the serial mode, the unused parallel input pins, D0-D8, and the unused parallel output pins, Q0-Q8, are used to output information on the status of the serial transfer (Figure 5).

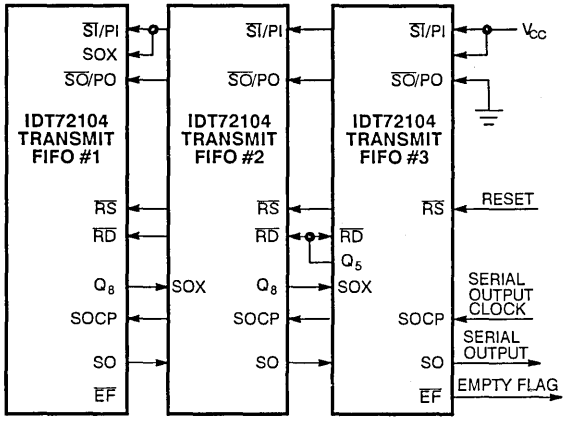

Figure 3. Serial Output Width Expansion to 24 Bits

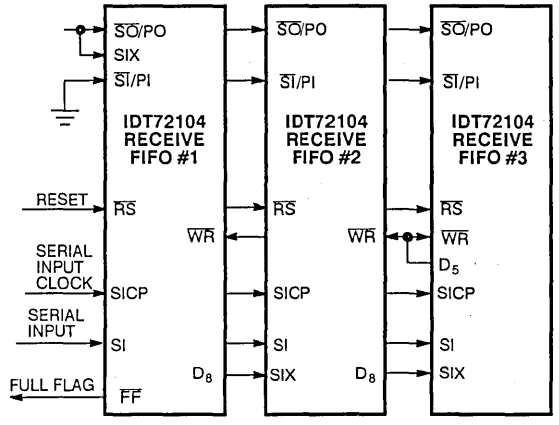

Figure 4. Serial Input Width Expansion to 24 Bits

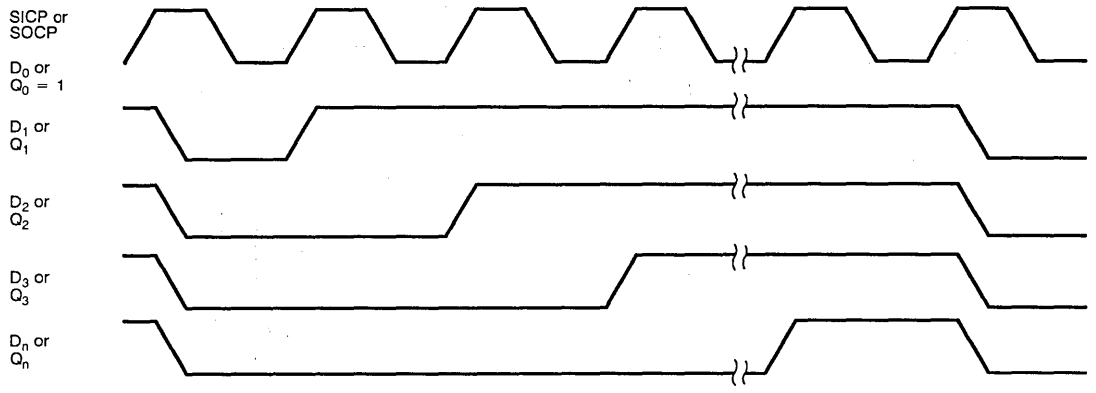

Figure 5. Parallel Pin Output Signals When In Serial Mode

These signals are used to trigger the reading and writing of data words to and from the FIFO registers and allow us to program the serial word width. These signals may also be used to drive related external logic. The minimum serial word width that may be programmed is 4 bits. Because D_0-D_8 and Q_0-Q_8 are simple outputs when the part is being used in the serial mode, they must not be bused together when in this mode.

The serial output word width is programmed by connecting the read line to the Q pin numbered one less than the word width required. The serial input word width is programmed by connecting the write line to the D pin numbered one less than the word width required. When multiple parts are used to expand the word width beyond 9 bits, this pattern continues over to the next part in sequence. In Figures 3 and 4, the word width has been programmed to nine plus nine plus six, or twenty-four bits.

On the serial input side, the SIX input of a FIFO that will sink higher order bits is tied to the D_8 pin of the FIFO which will sink lower order bits. The SIX input of the part to receive the lowest order bits is tied to V_{CC}. Likewise, on the serial output side, the SOX input of a FIFO that will source higher order bits is tied to the Q_8 pin of the FIFO which will source the lower order bits. The SOX input of the part to receive the lowest order bits is tied to V_{CC}. The serial expansion inputs SIX and SOX should not be used by external logic.

HARDWARE DESIGN

It is important to remember that FIFOs are state machines with internal logic being clocked by the read, write and expansion inputs. These control lines are high frequency clock lines and must be treated as such by the designer. It is important that these signals be clean, glitch free and reflection free.

With fast logic types and long traces it may be desirable to terminate the control signal lines to reduce ringing. A 20 to 50 Ohm series resistor placed close to the driving outputs may help balance the impedance of the output driver to the transmission impedance of the line and thus reduce ringing. Unused FIFO inputs must always be tied to V_{CC} or ground. When cascading the FIFO in depth or width, the expansion lines XI, XO, SIX and SOX should be as short as possible. If they are long, termination of these lines may also be required.

The designer must take care not to inadvertently design noise into these signals. For example, a designer may choose to strobe the read and write lines with a 74138 decoder. Since the inputs to the decoder never arrive at precisely the same time, the outputs may sequence through a number of transient states before settling. The result is a random number of very fine glitches (decoder glitches) on the outputs and, thus, the read and write signal lines. Since the logic is quite fast, the glitches may be very narrow and difficult or impossible to find with a logic analyzer.

HIGH-SPEED SERIAL LINK USING THE IDT72103/4

To minimize the CPU time associated with excessive task switching when transferring data, the ideal communications link appears to the processor as a range of memory addresses (dual-port memory) or an address that can be repeatedly read or written without corrupting data (FIFO).

If a serial link is required between two systems, a simple system using two parallel-serial FIFOs may provide a straightforward solution. If it is required, data word widths can be adjusted in the process. For example, data being transferred from a 32-bit processor can be folded to 16-bit words when moving through the FIFO serial link for use by a 16-bit CPU receiving the data. In this FIFO-serial link, data written to the transmitting FIFO is automatically transferred to the receiving FIFO as quickly as the hardware allows. The FIFO-serial link appears to the two systems as a virtual FIFO. The two communicating systems need only respond to the Empty or Full Flags of their respective local FIFOs.

In parallel I/O mode, the fall-through time of the IDT72103/4 is very small. The fall-through time of the FIFO-serial link is dedicated by the serial transfer rate and the serial word width. The serial data transfer rate may be limited by the characteristics of the serial channel or by the upper limit imposed by the FIFO logic.

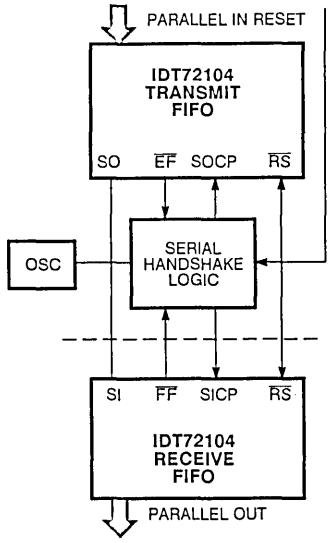

Figure 6. Serial Link Using Two IDT72104 FIFOs

SERIAL LINK OPERATION

For the purpose of illustration, a partial schematic of the serial handshake logic is shown in Figure 7. Operation of the serial link requires logic to pause the clock signals when the transmitting FIFO is empty or when the receiving FIFO is full and to restart the serial clock when the FIFOs are again ready for transfers.

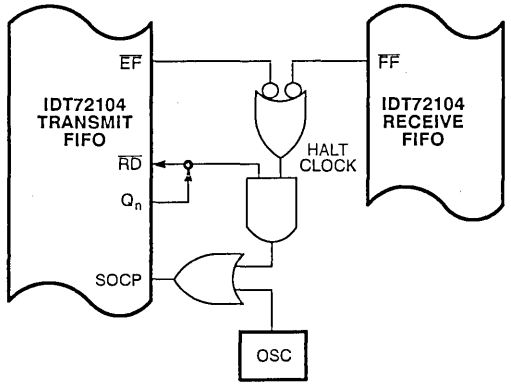

Figure 7. Partial Clock Enable Logic

The clock signals to the FIFOs are paused when the transmitter's Empty Flag or the receiver's Full Flag is asserted. The clock signals are re-started and serial transfer begins again when the Full and Empty flags are both de-asserted. Since the Empty and Full flags are both asserted after clocking the first bit of the last word to be transferred, the logic must also allow the last word to be transferred entirely before it de-asserts the clock enable signals. This is done by delaying the disabling of the clock signals until the read signal of the transmitting FIFO goes high. This signals to the handshake logic that the last bit of the serial transfer has been completed. The clock signal is then disabled in a high state. When both the transmitter's Empty Flag and the receiver's Full Flag are de-asserted, the serial clock signals are enabled again.

A complete schematic is shown in Figure 8. The logic is essentially the same as that in Figure 6, but includes provisions for synchronization to the serial clock and system reset. An IDT74FCT374A is used as array of clocked D-type flip-flops for synchronization of the handshake logic to the serial clock. Since the de-assertion of the Empty and Full flags is asynchronous to the serial transfer clock, logic is required to resolve metastability resulting from clock edge coincident transitions of the "HALT

CLOCK" signal. This is done by clocking the signal through stages of clocked D flip-flops.

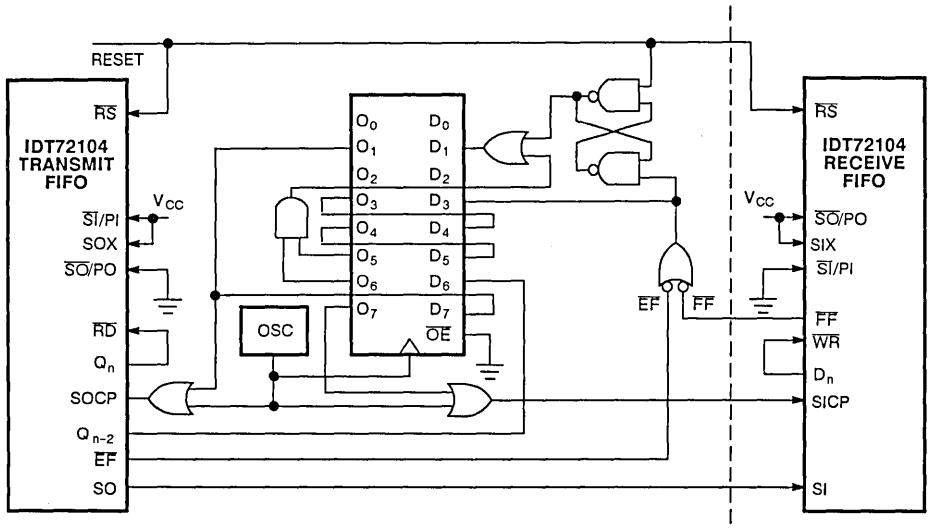

Figure 8. Serial Handshake Logic

The serial output clock must be one clock pulse ahead of the serial input clock. This is due to the fact that the FIFO serial output does not output the first bit until after the first positive output clock edge. Until this time, the output is in a high impedance state. On the other hand, the FIFO serial input inputs the first bit on the first serial input clock edge. To accomplish the necessary one clock cycle delay, the clock enable signal is clocked through one extra D flip-flop before it affects the serial input clock signal.

Reset of the serial handshake logic occurs automatically. The "HALT CLOCK" signal is asserted a few serial clock pulses after the transmitting FIFO's Empty Flag is asserted during reset. The cross coupled NAND gate flip-flop keeps the clocks disabled after reset until the transmitting FIFO de-asserts the Empty Flag and, thus, "HALT CLOCK" for the first time. This provides adequate time for the Q_{n-2} signal to return to logic high following reset, thus completing the reset sequence.

TIMING

The timings for the serial interface are based on the IDT72103/4 preliminary data sheet, dated April 1987, for a part with a 50ns address access time and for the schematic in Figure 8. Timing for other versions will follow this pattern. For operation at 40MHz, pipelining of logic delays is required for the handshake logic. The serial clock period is only 25ns. For operation at lower speeds, somewhat less complex circuitry can be used with fewer D flip-flops for pipelining.

The timings shown in Figures 9 and 10 assume the use of an IDT74FCT374A with CP-to-On delay of 6.5ns maximum and fast 74F00 series logic with propagation delays of 6ns. Minimum clock high time is dictated by the need to enable and disable the clock without glitching. Conservatively, this is 6ns OR gate delay + 6.5ns CP-to-On delay. Minimum clock period is dictated, in this case, by the fastest FIFO shift logic specification of 40MHz.

The "HALT CLOCK" signal may be de-asserted too close to the positive clock edge to avoid metastability in the D flip-flop associated with register input D_3. To assure that the metastability does not cause glitches in the clock signal, the output O_3 feeds the input D_4. This would give the metastable flip-flop 25ns, the clock period minus 2ns, the set-up time for the next D input stage to settle out before affecting the clock logic. With this logic family, this time should be adequate to provide a very low probability that the metastable condition will not propagate further. Since timing is not critical here, another flip-flop stage has been added to ensure this (D_5 and O_5).

At 20ns maximum from clock high, the transmitter's read signal can be too late to safely de-assert the clock signals after one necessary gate delay (6ns) and still meet the set-up time for the IDT74FCT374A register (2ns). Instead, the output signal of a Q output tap two less than that used for the read signal is clocked in (Figure 9). The time from clock high to Q high is then 20ns maximum plus 2ns set-up. This safely fits into the 25ns window.

The AND gate shown in Figure 7 is present in Figure 8, but is the input to an additional OR gate not shown in Figure 7. The OR gate and a set-reset flip-flop are used to assure that the clocks are not active during reset. The flip-flop is set during system reset and cleared when the "HALT CLOCK" signal is de-asserted for the first time after reset. The flip-flop's clock-to-output time (6.5ns output 5 and 6), plus the two gate delays (6.5ns = 6ns), plus the set-up time (2ns), adds up to 20.5ns maximum and fits safely into the 25ns window provided.

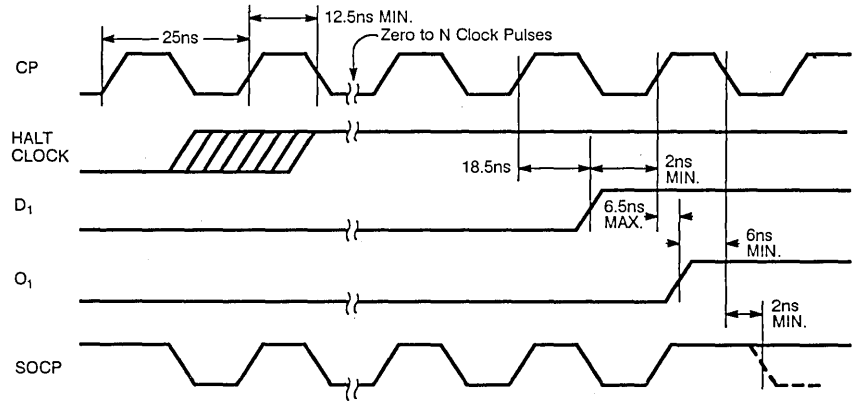

Figure 9. Serial Clock Disable Timing

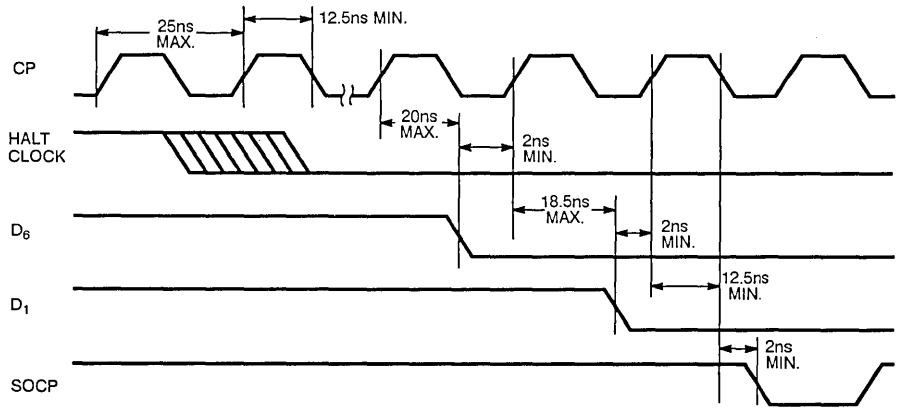

Figure 10. Serial Clock Enable Timing

The clock signals are disabled in the high state. In order to enable and disable them without glitches; the enable and disable operations must take place in the 12.5ns window provided by the clock high time. The register's clock-to-output delay is 6.5ns maximum; the gate delay is 6ns maximum.

The transmitter's serial clock must be one pulse ahead of the receiver's serial clock. This is accomplished by requiring the receiver's clock enable signal to pass through one additional D flip-flop before becoming effective (D_7 and O_7).

The reset pulse must be low for two serial clock pulses and the first write to the transmitting FIFO must not occur prior to RSQH (the time required for the FIFO Q outputs to return high after reset pulse—35ns for the part in question). Four additional serial clock pulses are required to ensure reset of the handshake logic without false clock pulses.

DATA WIDTH FOLDING DURING SERIAL TRANSFER

Data word widths may be multiplied or divided by integer quantities during transfer. Figure 11 shows an example where 16-bit data words are being folded into 8-bit words during serial transfer from a 16-bit processor to an 8-bit system. The folding operation is transparent to the processors on either side.

The folding operation is accomplished by programming the serial word width on each side of the serial link to multiples of each other. In Figure 11, the right hand serial word width has been programmed to be 16 bits. Nine bits of transmit FIFO #1 and 7 bits of transmit FIFO #2 are used. This is done by tying the SOX input of FIFO #1 to V_{CC} and triggering the read input for both FIFOs from the Q_4 output of transmit FIFO #2.

On the left hand side, the serial word width is programmed to 8 bits by tying the SIX input to V_{CC} and tying the write signal to the I/O pin D_7.

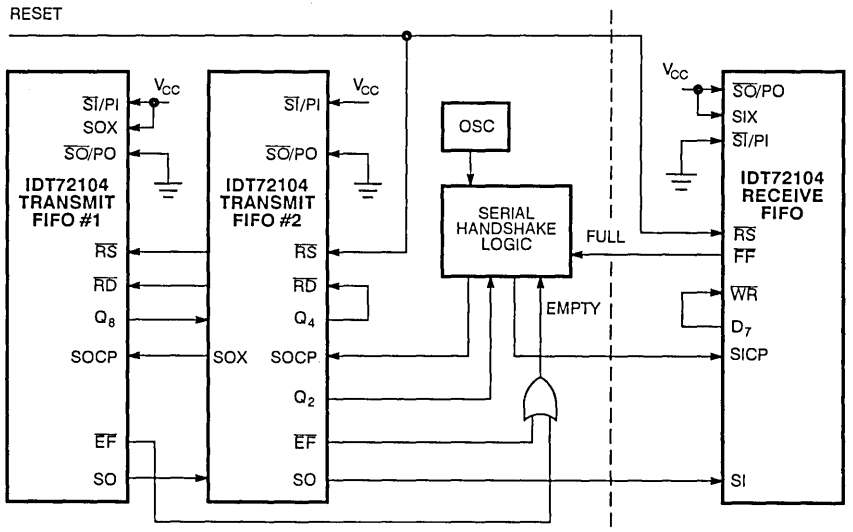

Figure 11. Schematic Facilitating 16-Bit to 8-Bit Data Folding During Serial Transfer

ONE-BIT VIRTUAL FIFO

In the serial-in/serial-out mode, the parallel-serial FIFO operates as a virtual 1 bit wide FIFO. The SICP input functions as a write input and the SOCP input functions as a read input. In this mode of operation the IDT72103/4 may be used to widen the word width of a parallel FIFO in 1-bit increments (Figure 12).

The 1-bit virtual FIFO has a latency of 4 to 9 bits, depending on the programmed serial word width. For example, if the FIFO is programmed for 9-bit words, 10 bits must be written into the FIFO before the Empty Flag is de-asserted and the first 9 bits can be read. The depth of the virtual FIFO in this mode is 9 x 4096 bits. If the word width is programmed to be 4, the latency is reduced to 4 bits and the depth is reduced to 4 x 4096 bits.

In applications where some latency is not a problem, the serial-in/serial-out FIFO can be used to extend the width of a parallel FIFO in increments of one. In general, the serial-serial FIFO depth should exceed the depth of the parallel FIFO to avoid empty and full boundary condition conflicts.

In Figure 12, an IDT74FCT861 latch is shown to maintain tri-state capability across all 10 output bits. This may not be required.

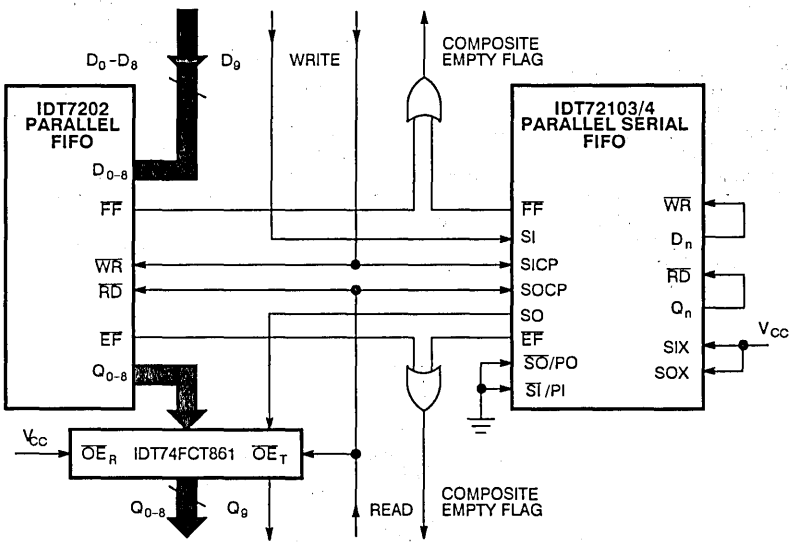

Figure 12. Serial-Serial FIFO Expanding the Width of a Parallel FIFO

CONCLUSION

The IDT72103/4 Parallel-Serial FIFO can be used to reduce parts count and lower power consumption in numerous applications which involve FIFOs and parallel/serial data conversion. Applications include video frame buffers, communications links, printer buffers and parallel-parallel FIFO bandwidth adjustment.

The numerous status flags, ample depth, speed and the presence of an independent output enable control make the FIFO highly flexible for use in parallel-to-parallel mode applications as well.

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Integrated Device Technology, Inc.

PERFORMANCE ADVANTAGES WITH IDT's FLAGGED FIFOS

APPLICATION NOTE AN-22

By Danh Le Ngoc

INTRODUCTION

The most common application for the FIFO is an elastic data buffer between two synchronous or asynchronous systems for the purpose of passing data.

Because data is produced and accepted at different rates, it is important to monitor the boundary conditions (FULL or EMPTY) of the data buffer. Failure to act on the boundary conditions will result in data overflow or underflow. The current FIFO generation, such as IDT7201/02/03/04, signals the empty, half-full and full condition by asserting the $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$, respectively. The empty and full flags are also fed back internally and inhibit further Read and Write operations until the FIFO is no longer empty or full.

The increasing use of high-speed CMOS, coupled with the introduction of the 32-bit CPU, has created the demand for a faster and smarter generation of FIFOs. New Flagged FIFOs offer the basic features of IDT's industry standard FIFOs (IDT7201/02/03/04) while providing two new flags: ALMOST-EMPTY and ALMOST-FULL. These flags can be used as early warning flags in critical real-time applications such as data acquisition, high-speed data link and pipeline Digital Signal Processing applications. In the multi-tasking environment, the ALMOST-EMPTY and ALMOST-FULL can also be used to set the interrupt request in advance, so that the CPU has sufficient time to perform the task switch without loss of data due to the task switch latency. Other advantages of these Flagged FIFOs are an increase in memory utilization and the Three-State Control, $\overline{OE}$, for the outputs (Q0-8). The use of independent Three-State Control simplifies the interface with bus and I/O channels and improves timing in read and write cycles. Figure 1 is a block diagram of the new Flagged FIFOs: IDT72021/31/41.

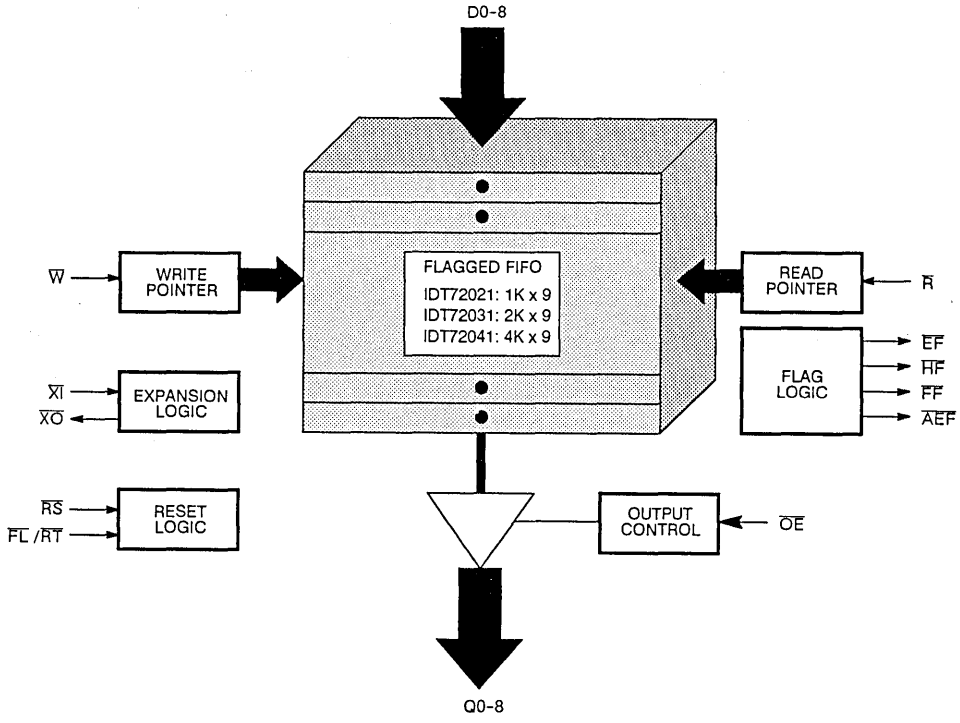

Figure 1. Simplified Block Diagram for Flagged FIFOs

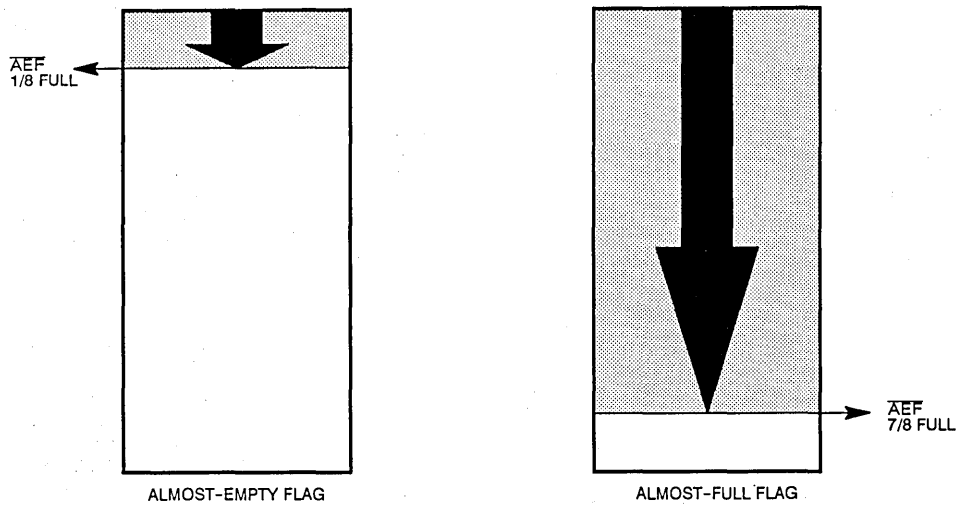

Figure 2. Almost-Empty and Almost-Full Flags on the IDT72021/31/41

APPLICATIONS USING THE FLAGGED FIFOS

Typical applications using the new features of the Flagged FIFOs are demonstrated below.

- **ALMOST-EMPTY AND ALMOST-FULL FLAG AS EARLY WARNING FLAGS IN REAL-TIME DIGITAL SIGNAL PROCESSING APPLICATIONS**

  Figure 3 is a simplified block diagram of a real-time spectrum analyzer featuring A/D channels, input buffer, FFT processor, display processor, output buffer and CRT. In operation, the DSP engine processes on the previous frame of data at the 50 MHz rate, while the A/D channel samples the analog signal at the comparatively slow rate of 20 MSPS. This data rate mismatch requires the use of a FIFO to act as an elastic data buffer. To prevent data overflow, the ALMOST-FULL flag is used as an early warning to the DSP controller. With this signal, the DSP engine has sufficient time to empty the input buffer (FIFO) into the buffer at its own high-speed data rate. Meanwhile, the A/D channel continues to refill the input buffer from other side at its much slow rate. At the other end of the system, a second FIFO acts as an output buffer between the high-speed display processor and slow CRT. In this case the ALMOST-EMPTY FLAG is used as an early warning so that the display processor can begin filling the buffer with the next image.

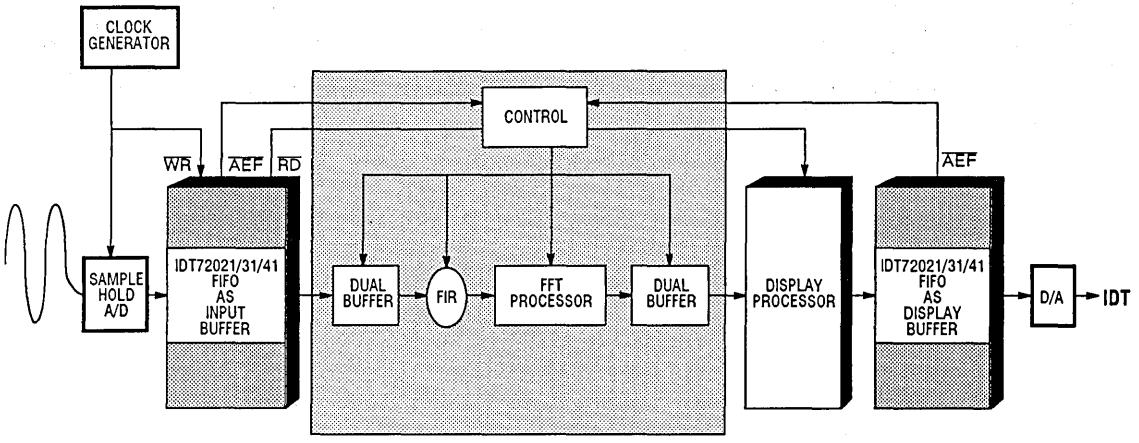

Figure 3. Simplified Block Diagram for a Real-Time Spectrum Analyzer

9

- **MAXIMUM UTILIZATION OF MEMORY WITH THE ALMOST-FULL AND ALMOST-EMPTY FLAGS IN HARD DISK DRIVE APPLICATIONS**

  Because of the high data rates used in the hard disk drive protocols, SMD, SCSI and IPI or the standard data communication protocols (Ethernet, Supernet and Fiber-optics which can go up to 100 Mbits per second), even the newer and faster microprocessors will struggle to keep up with the speed of I/O channels. For this reason, data buffering is always considered in any high-speed I/O transfer. The design in Figure 4 shows the data buffer for a high-speed hard disk application. In such CPU-to-I/O controller applications, FIFOs are often used to construct the data buffer. Normally two sets of FIFOs are arranged in the back-to-back manner, where one set acts as a transmit buffer and the other as the receiver buffer. In this arrangement, the CPU dumps data in the transmit FIFO until the FIFO is 7/8 full. At this point, the FIFO sets the Almost-Full Flag, initiating the data transfer to the I/O channel at its higher speed rate. In similar fashion, the high-speed I/O channel dumps data into the receiver FIFO until it is almost full. In this case, the Almost-Full Flag triggers an interrupt request to the host processor or DMA request to the DMA controller. If the request goes to the DMA controller, the DMA channel can transfer the entire block of data into the system memory in one burst. Figure 4 illustrates a host interface between a 32-bit microcomputer system based on an Intel 80386 and a Disk Drive.

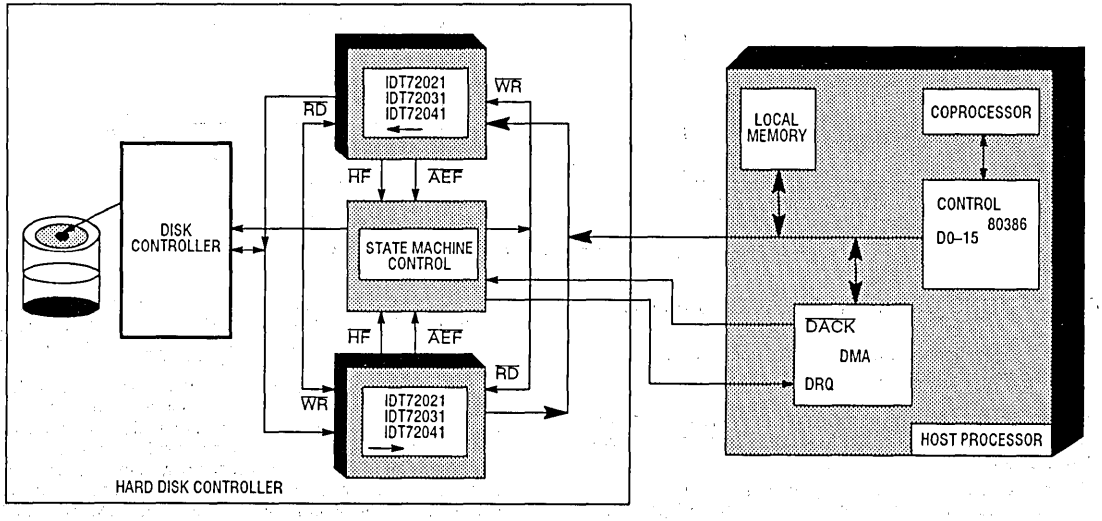

Figure 4. Block Diagram of a Disk Drive Controller

- **ASYNCHRONOUS THREE-STATE CONTROL**

  Another common use for FIFOs is as a data buffer between a microcomputer and high-speed I/O bus for the purpose of passing data back and forth. The figures on the next page illustrate two examples of the interface between a 32-bit processor and the I/O channel of the IBM PC AT, one using FIFOS without three-state control and the other using FIFOs with their three-state control. As Table 1 indicates, using the new Flagged FIFOs with their three-state control pin produces faster read and write cycles. An additional advantage is the ability to repeat a reading from the same FIFO location without advancing the read pointer.

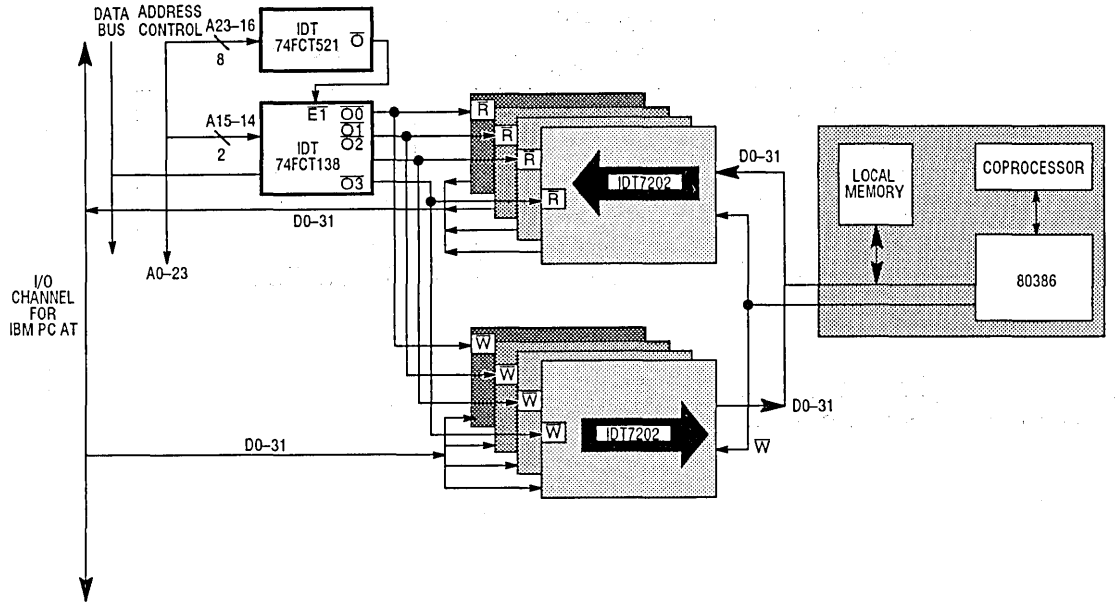

Figure 5. IDT7202 FIFOs Without Three-State Control as a Data Buffer Between IBM AT and an Accelerator Board

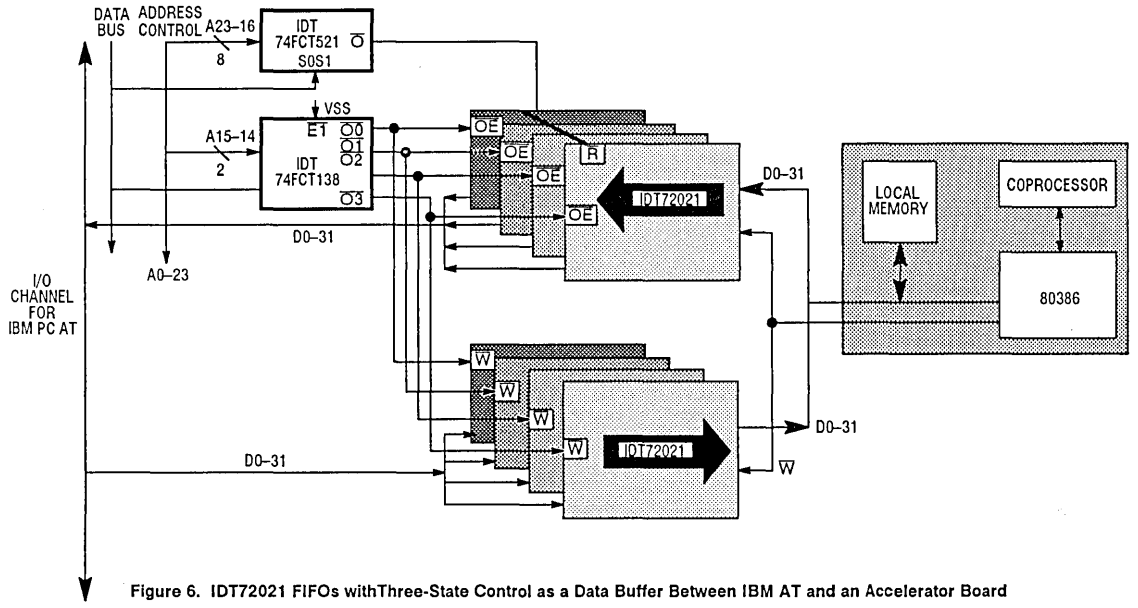

Figure 6. IDT72021 FIFOs withThree-State Control as a Data Buffer Between IBM AT and an Accelerator Board

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Table 1. Read and Write Cycle with IDT7202/021

DELAYS PATHS	WITHOUT THREE-STATE CONTROL	WITHOUT THREE-STATE CONTROL
IDT74FCT521A: TPLH	7.2ns	0.0ns*
IDT74FCT138A: TPLH	9.0ns	9.0ns
IDT7402/021: TRC	35.0ns	35.0ns
TOTAL	**50.2ns**	**44.0ns**

*Although this propagation delay is specified at 7.2ns, it occurs in parallel with the slower 9.0ns propagation delay of the IDT74FCT138A and is not additive as is the case in the "without three-state control" application.

CONCLUSION

As the need for high-speed data computation increases, the FIFO must also become faster and smarter. The next generation of FIFO, as exemplified by the IDT72021/31/41, meets that challenge.

Integrated Device Technology, Inc.

BUS MATCHING BiFIFO IN DEFAULT OPERATION MODE

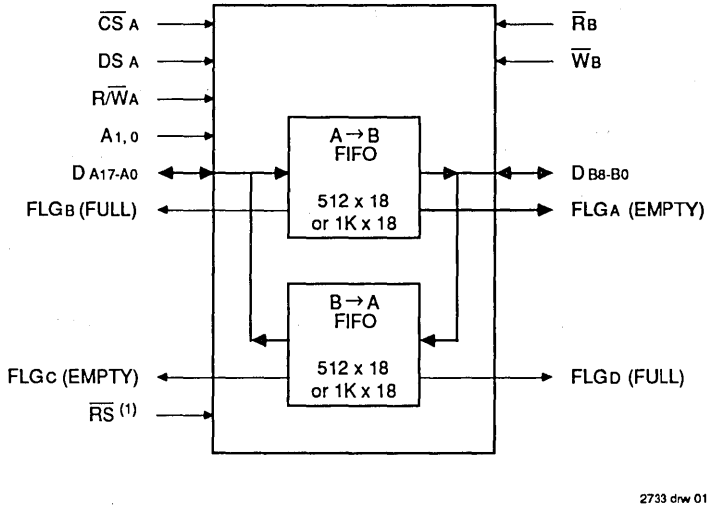
APPLICATION NOTE AN-34

by Julie Lin and Danh LeNgoc

INTRODUCTION

The IDT7251/510/52/520 are high-speed, low power bidirectional FIFO organized as 512 by 18 and 1024 by 18 respectively. The 18-to-9 bit BiFIFO contains many proprietary features, such as: Reread/Rewrite capability, parity function, programmable flags, DMA handshake circuitry, and bypass path. Some of these features require initial set up through programming of the internal configuration registers (see data sheet).

The focus of this application note is to describe the default mode of the BiFIFO after the software "Reset All" operation or the hardware reset ($\overline{RS}$) (on the IDT72510/520 only). The default mode provides a bidirectional data buffer for a CPU-to-CPU interface. The equivalent block diagram is illustrated in Figure 1 where four flag pins are set as FLG_A = "A → B empty", FLG_B = "A → B full", FLG_C = "B → A empty" and FLG_D = "B → A full", respectively.



NOTE:
1. Available in the IDT72520/510.

Figure 1. The Bus Matching BiFIFO

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This configuration can be used as a bidirectional data buffer between a 16-bit processor and an 8-bit processor, as shown in Figure 2. The 16-bit CPU is hooked to Port A, whereas the 8-bit CPU is connected to Port B. The interface functions of the 16-bit CPU include reading the B → A FIFO, writing the A → B FIFO, monitoring the empty flag of the B → A FIFO (FLGC) and the full flag of the A → B FIFO (FLGB). Similarly, the 8-bit CPU interface includes reading the A → B FIFO, writing the B → A FIFO, monitoring the full flag of the B → A FIFO (FLGD) and the empty flag of the A → B FIFO (FLGA). Since the parity function is not used in the BiFIFO, the parity bits, DA17-A16 and DB8, are pulled down with 10K resistors.

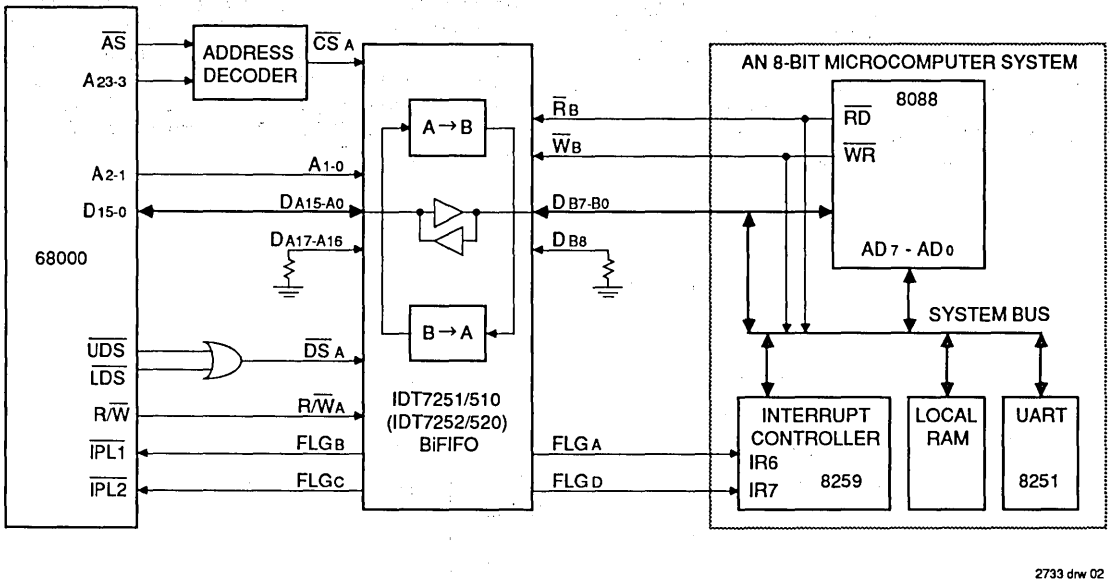


Figure 2. The Bus Matching BiFIFO Fits Into the 16-Bit CPU to 8-Bit CPU Interface

Integrated Device Technology, Inc.

THE BiFIFO PARITY GENERATION AND CHECKING

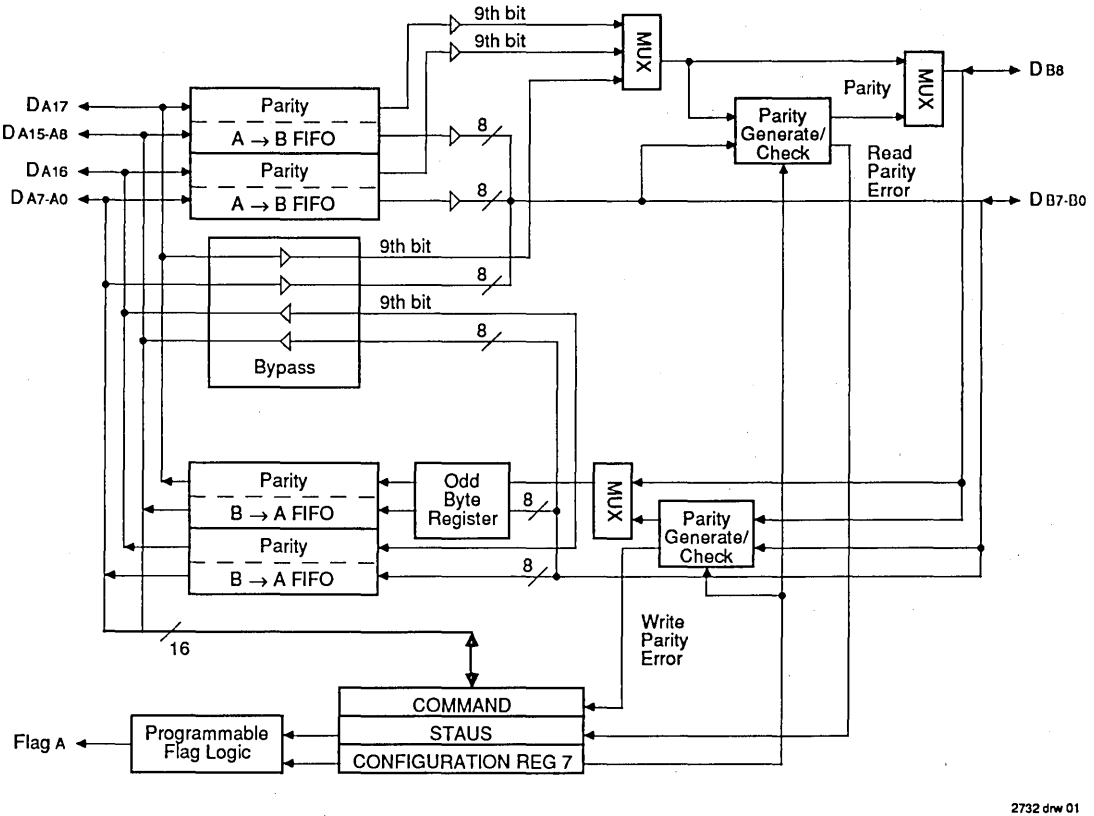
APPLICATION NOTE AN-36

by John Chen

INTRODUCTION

An occasional error may be introduced into the information while moving binary words within a digital system or in exchanging words with other systems. One erroneous bit due to noise in the system will cause an incorrect word to be transmitted. The parity generation and checking feature in the BiFIFO allows the user to detect and correct such data errors. This application note describes the function of this feature.

The parity checking and generation is available on IDT's 7251/72510/7252/72520 devices in the BiFIFO family. Figure 1 is the functional block diagram of the BiFIFO. Port A consists of 16 data bits (D_{A15-A0}) and two parity bits ($D_{A17-A16}$). Port B consists of 8 data bits (D_{B7-B0}) and one parity bit (D_{B8}). Depending on the direction of the data flow, the parity is generated/checked either before writing or after reading the memory on Port B side. In the bypass mode, only the 8 data bits are passed through memory, while the 9th bit (D_{A16} or D_{B8}) will go through parity generation and checking. Configuration Register 7 (Table 6 of data sheet) is used to select the various parity function and is shown in Table 1.



2732 drw 01

Figure 1. Functional Block Diagram

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CONFIGURATION REGISTER 7

Bit	Function		
0 – 7	Unused		
8	Parity Input Control	0	Disable Parity Generate, Enable Parity Check
	B → A	1	Enable Parity Generate, Disable Parity Check
9	Parity Output Control	0	Disable Parity Generate, Enable Parity Check
	A → B	1	Enable Parity Generate, Disable Parity Check
10	Parity Odd/Even	0	Odd
	Control	1	Even
11	Assign Parity Error to	0	No Parity Error Output
	Flag A Pin	1	Parity Error on Flag A Pin
15 – 12	Unused	Note: All default to 0.	

2732 tbl 01

Table 1. Parity Function

PARITY GENERATION

A → B FIFO Operation: A word (2 bytes) written into Port A requires two reads from Port B to retrieve both bytes. The data bits (DA_{7}-DA_{0}, DA_{15}-DA_{8}) and the ninth bit (DA_{16}, DA_{17}) are written into A → B FIFO memory at the same time as one word. The original parity bit from A → B FIFO is ignored by the parity generate/check circuitry. Parity bits are generated when reading from Port B. The parity generation mode is enabled by setting "1" on Bit 9 of Configuration Register 7. The generated parity bit flows through the path (#1) as indicated in Figure 2a.

A → B Bypass: The 8-bit data on DA9-A0 is passed directly to Port B bus DB7-B0. The parity on DA16 is ignored in the parity generate/check circuitry. A new parity is generated and placed on DB8 as an output.

B → A FIFO Operation: Two writes to Port B is stored in FIFO memory as a word. Each byte consists of 8 data bits (DB_{7}-DB_{0}) and a ninth bit (DB_{8}). The ninth bit in the parity generate/check circuitry is ignored while the data is written into B → A FIFO memory. Similarly, parity generation mode is enabled by setting "1" on Bit 8 of Configuration Register 7. The generated parity bit flows through the path (#3), as indicated in Figure 2b.

B → A Bypass: The 8-bit data on DB_{7-B0} is passed directly to DA7-A0. The parity bit on DB_{8} is ignored. A new parity is generated and placed on DA_{16} as an output.

PARITY CHECKING

A → B FIFO Operation: This mode is similar to the parity generation mode except that the ninth bit is tested by the parity circuitry. Both the data bits and the ninth bit are written into the A → B FIFO, and are then read from the FIFO memory. The ninth bit is compared to the parity bit that is generated from the parity circuitry. The Exclusive–OR of the parity check indicates "Read Parity Error" result. The ninth bit flows through the path (#2), as indicated in Figure 2a.

A → B Bypass: The parity bit on DA16 is passed to DB8. The parity checking result is shown on "Read Parity Error" bit.

B → A FIFO Operation: This works in a similar manner to the A → B, except that the data is written into B → A FIFO, and the Exclusive–OR result of the ninth bit and generated parity indicates Write Parity Error result. The ninth bit passes through the path (#4), as indicated in Figure 2b.

The parity check mode is enabled by setting a 0 (also the default condition) either Bit 8 (B → A) or Bit 9 (A → B) of Configuration Register 7.

B → A Bypass: The parity bit on DB8 is passed to DA16. The parity checking result is shown on "Write Parity Error" bit.

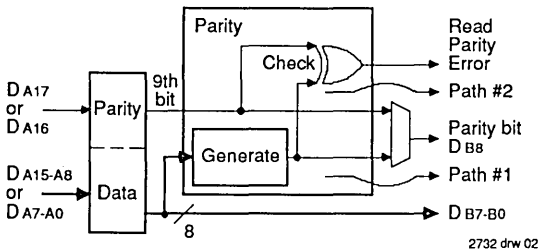

Figure 2a. Parity Generate/Check for A → B

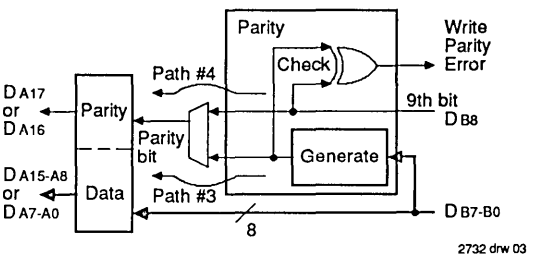

Figure 2a. Parity Generate/Check for B → A

ODD/EVEN PARITY

Odd or even parity can be selected through Configuration Register 7 (Bit 10). Even parity (put a 1 in Bit 10) implies all 1s from data bits and parity bit, resulting in an even number. Odd parity (0 in Bit 10) implies all 1s from the combined data bits and parity bit, resulting in an odd number. The parity error defaults to odd parity.

PARITY ERROR INDICATION

Status Register

The read or write parity error from the parity function circuitry will set the read/write parity error bit of the Status Register (Table 8 of 7251/510/52/520 data sheet) to "1". Bit 9 is the Write Parity Error flag. Bit 10 is for the Read Parity Error flag. The Status is accessed by the Address Control ($\overline{CS}_A = 0, A_1 = 1, A_0 = 1$).

External Flag Pin

The OR of the two internal parity error flags is available as an option for output on the external Flag A pin. This is enabled by setting Bit 11 of Configuration Register 7.

Resetting a Parity Error

The parity circuit is constructed in such a way that once a parity error is detected, the error flag is set and remains set until a clear command is executed. The parity error flag can be cleared through the command register (Table 2 of data sheet) by selecting A (1010) and B (1011) in the opcode.

DEFAULT PARITY FUNCTION

Under the default condition, Configuration Register 7 enables the following functions:

1. B → A and A → B parity checking
2. Odd parity
3. External parity error not available.

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Integrated Device Technology, Inc.

THE PROGRAMMABLE FLAGS OF BiFIFOs

APPLICATION NOTE AN-39

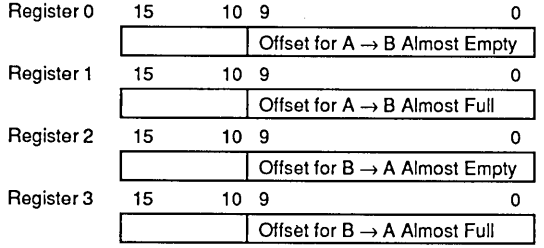
By Julie Lin and Danh LeNgoc

This application note explores one of the key features of the IDT7251/510/52/520 BiFIFO — the software programmable flags. The functional capabilities include: (i) Programmable offset values for the "Almost" flags, (ii) External flags, and (iii) Internal flags. The programming procedures are explained and illustrated by an example. Finally, the flag assignment of the default operation mode is discussed.

The BiFIFO is composed of two FIFOs named as A → B FIFO and B → A FIFO, each with four internal flags. These eight internal flags are A → B Empty, A → B Almost-Empty, A → B Full, A → B Almost-Full, B → A Empty, B → A Almost-Empty, B → A Full and B → A Almost-Full. The Almost-Empty flag is defined as the condition when the read pointer is "Offset" steps behind the write pointer. Similarly, the Almost-Full flag indicates the condition when the write pointer is "Offset" steps behind the read pointer. The offset values of the four Almost flags are programmable through Configuration Registers 0–3. The programmable Almost flags can be used as early warning flags in critical real-time applications such as data acquisition, high-speed data links and pipelined digital signal processing applications. All the flags can be accessed either internally through the Status Register for CPU software polling or externally through four flag pins for interrupting the CPU.

The Offset Values of the Almost Flags

The offset values defined by Registers 0–3 are unsigned positive numbers (see Table 1). They range from 0 to 1023 for the IDT7252/520 and from 0 to 511 (Bit 9 should be set to "0") for the IDT7251/510. Specifically, Register 0 is for the A → B Almost-Empty flag; Register 1 is for the A → B Almost-Full flag; Register 2 is for the B → A Almost-Empty flag; Register 3 is for the B → A Almost-Full flag.

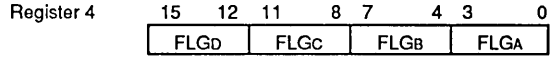


2735 tbl 01

Table 1. Registers 0–3 of the IDT7252/520 Defining the Offset Values of the Almost Flags

External Flags

Each of the four flag pins FLGA, FLGB, FLGC and FLGD can be programmed to any one of eight internal flags, together with the choice of polarity. Register 4 is used to select the flags for the external flag pins (see Table 2). This register is divided into four fields of four bits each: Bits 0–3 select FLGA; Bits 4–7 select FLGB; Bits 8–11 select FLGC; Bits 12–15 select FLGD. The selections for each external flag are listed in Table 3. The most significant bit of the four-digit selection code selects flag polarity — "0" for active low, "1" for active high. The next bit selects a particular FIFO — "0" for A → B FIFO, "1" for B → A FIFO. The remaining two bits indicate the relative position of read and write pointers — "00" for Empty. "01" for Almost-Empty, "10" for Full, "11" for Almost-Full.



2735 tbl 02

Table 2. Register 4 for the Selection of External Flags

Selection Code	Selected Flags
0000	A → B $\overline{\text{Empty}}$
0001	A → B $\overline{\text{Almost Empty}}$
0010	A → B $\overline{\text{Full}}$
0011	A → B $\overline{\text{Almost Full}}$
0100	B → A $\overline{\text{Empty}}$
0101	B → A $\overline{\text{Almost Empty}}$
0110	B → A $\overline{\text{Full}}$
0111	B → A $\overline{\text{Almost Full}}$
1000	A → B Empty
1001	A → B Almost Empty
1010	A → B Full
1011	A → B Almost Full
1100	B → A Empty
1101	B → A Almost Empty
1110	B → A Full
1111	B → A Almost Full

2735 tbl 03

Table 3. The Selection Table for External Flag Pins

An Example to Illustrate the Selection of External Flags

The configuration registers are accessed by executing the command X1XmH ("X" stands for don't care) to point to Register "m" (m = 0, 1, 2, 3, 4) and then reading or writing from address 2 (A1–0 = 10). These procedures are illustrated by the example shown in Table 4. In this example, four flag pins are assigned as:

FLGA = A → B $\overline{\text{Almost–Empty}}$ with offset = 7
FLGB = A → B $\overline{\text{Almost–Full}}$ with offset = 10
FLGC = B → A $\overline{\text{Empty}}$
FLGD = B → A $\overline{\text{Almost–Full}}$ with offset = 128

Function	$\overline{CS}_A$	A_1	A_0	$R/\overline{W}_A$	$D_{A15-A12}$	D_{A11-A8}	D_{A7-A4}	D_{A3-A0}
Select Register 0	0	1	1	0	XXXX	0001	XXXX	X000
Write Register 0	0	1	0	0	XXXX	XX00	0000	0111
Select Register 1	0	1	1	0	XXXX	0001	XXXX	X001
Write Register 1	0	1	0	0	XXXX	XX00	0000	1010
Select Register 3	0	1	1	0	XXXX	0001	XXXX	X011
Write Register 3	0	1	0	0	XXXX	XX00	1000	0000
Select Register 4	0	1	1	0	XXXX	0001	XXXX	X100
Write Register 4	0	1	0	0	0111	0100	1011	0001

2735 tbl 04

Table 4. The Port A Access Control to Program Flags

First of all, Register is programmed to the decimal number "7". Note that Bit 9 of Registers 0–3 should be programmed to 0 for the IDT7251/510. Register 1 is set to decimal "10". Since B → A Almost–Empty flag is not used, Register 2 is not programmed. Register 3 is set to decimal "128". Register 4 is programmed to designate each flag pin assignment.

Internal Flags

Besides the external flag pins, the internal flag information can be accessed through reading the Status Register (see data sheet). As shown in Table 5, Format 0 provides the information for only four flags (Bit 12 to Bit 15). In Format 1, four extra bits (Bit 4 to Bit 7) complete the whole internal flag information. For all the flag bits of the Status Register, "1" indicates that the particular flag is on.

The Default Operation of the Programmable Flags

After the "Reset All" command is executed (or Reset line is asserted at the IDT72520/510), Register 0–3 are cleared and Register 4 is set as "0110 0100 0010 0000", which means:

FLGA = A → B $\overline{\text{Empty}}$
FLGB = A → B $\overline{\text{Full}}$
FLGC = B → A $\overline{\text{Empty}}$
FLGD = B → A $\overline{\text{Full}}$

Bit	Format 0
0	Odd Byte Register Bits 0-7
1	
2	
3	
4	
5	
6	
7	
8	Valid Bit
9	Write Parity Error
10	Read Parity Error
11	Status Format: 0
12	A → B Full
13	A → B Full – Offset
14	B → A Empty
15	B → A Empty + Offset

2735 tbl 05

Bit	Format 1
0	Reserved
1	Reserved
2	Reserved
3	DMA Direction
4	A → B Empty
5	A → B Empty + Offset
6	B → A Full
7	B → A Full – Offset
8	Valid Bit
9	Write Parity Error
10	Read Parity Error
11	Status Format: 1
12	A → B Full
13	A → B Full – Offset
14	B → A Empty
15	B → A Empty + Offset

2735 tbl 06

Table 5. Status Register Format

Integrated Device Technology, Inc.

THE BiFIFO EXPANSION CONFIGURATIONS

APPLICATION NOTE AN-56

by John Chen

The BiFIFO family consists of the Bus-Matching BiFIFOs and the Parallel BiFIFOs. The BiFIFO architecture allows the user to expand the width of the Port A and Port B data bus. There are two methods of cascading multiple Bus-Matching BiFIFOs for width expansion: the stand-alone expansion configuration and the master/slave expansion configuration. As for the Parallel BiFIFOs, only the stand-alone expansion configuration is available. Figure 1 comprises of all possible expansion configurations.

	Bus-Matching BIFIFO (IDT7251/72510/7252/72520)	Parallel BIFIFO (IDT72511/72521)
Stand-alone (1 pcs)	18-to-9	18-to-18
Master/Slave	36-to-9	N/A
Stand-alone (2 pcs)	36-to-18	36-to-36
Stand-alone (3 pcs)	54-to-27	54-to-54
•	•	•
•	•	•
•	•	•

2734 drw 01

Figure 1. Expansion Configuration

BUS-MATCHING BiFIFO

The IDT7251/72510/7252/72520 are bidirectional FIFOs configured as 18-to-9 in bus width. Generally, these BiFIFOs are ideal for data buffering between two systems with different data bus widths. This could be used for CPU-to-CPU or CPU-to-Peripheral communication. The processor/peripheral mode selection in Configuration Register 5 eases these two applications. A single BiFIFO can support an 18-to-9 configuration.

Stand-Alone Expansion

The stand-alone expansion configuration allows as many BiFIFOs to be expanded in parallel as the user requires. To use the stand-alone mode, the BiFIFOs should be programmed as "Stand-Alone" in the Width Expansion Mode Control in Configuration Register 5. Let's define the two-byte data as a word, and the four-byte data as a double word. The byte ordering on Port A side is arranged as:

Byte 0, Byte 2 for low and high bytes of BiFIFO 1;

Byte 1, Byte 3 for low and high bytes of BiFIFO 2;

with low byte defined as DA_{7}-DA_{0}, high byte as DA_{15}-DA_{8}. The first word read from Port B bus will be Byte 0 from BiFIFO 1 and Byte 1 from BiFIFO 2. The second word will be Byte 2 and Byte 3. The previous discussion is based on the assumption that Bit 1 of Configuration Register 5 is set to "0", which enables the low byte coming out of Port B before the high byte. In this example, Byte 0 is before Byte 2 and Byte 1 is before Byte 3. A 36-bit to 18-bit bidirectional application using two BiFIFOs is shown in Figure 2.

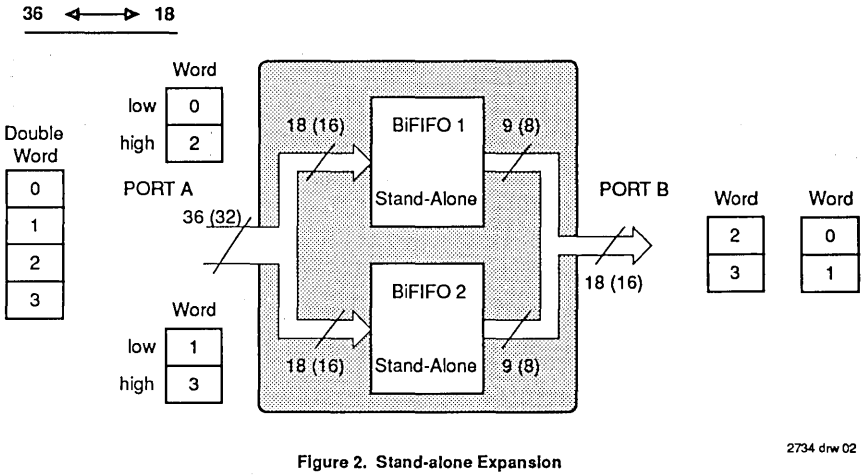


Figure 2. Stand-alone Expansion

Master/Slave Expansion

The Master/Slave architecture allows 2 BiFIFOs to be cascaded together in a configuration that produces a data path of 36 bits wide in the Port A side, and a data path of 9 bits wide on the Port B side (if parity bits are not used, this becomes a 32-bit/8-bit configuration).

The essence of the master/slave architecture is that the read/write operations on Port B of both the slave and master BiFIFOs are controlled by the master device. In general, four generations in Port B are required for every one operation in Port A. As an example in Figure 3, if a 36 bit double word is written into Port A, 4 reads are required to flush this double word out of the BiFIFO. Conversely, 4 writes into Port B of the expanded configuration are required before a double word can be read out of Port A. The master/slave BiFIFO architecture is defined to require the master BiFIFO to command the slave to complete 2 read or write cycles first, before the master BiFIFO is allowed to execute 2 read or write cycles.

There are two Master/Slave Expansion Configurations, the Processor mode, and the Peripheral mode.

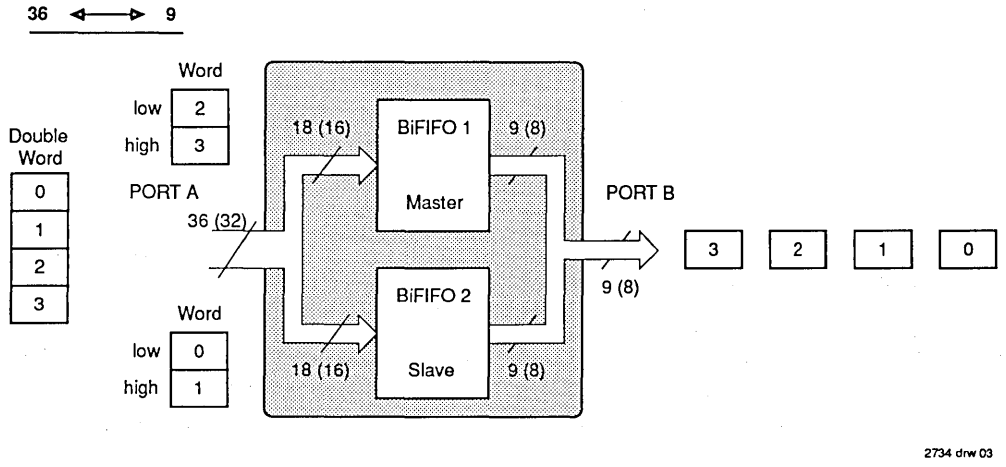


Figure 3. Master/Slave Expansion

Peripheral Master/Slave Expansion

To implement the Peripheral Master/Slave expansion configuration, both the Master and the Slave device must be programmed in the Peripheral mode. The DMA handshake operates out of the Master device; therefore, the Slave BiFIFO must be disabled by tying both the REQ and CLK lines low and leave the $\overline{ACK}$ line floating, as shown in Figure 4.

The Master device controls the byte order of the 36 bit words going into and out of Port B according to DMA protocol, which requires that the master device receive a REQ input before it can input or output data through Port B. Once a REQ input has been received at the master device, the master BiFIFO generates an ACK response to the peripheral device and then sent read/write control signal to the Slave and peripheral device. After 2 slave operations, the master is allowed 2 operations to complete definition of the 36 bit doubleword.

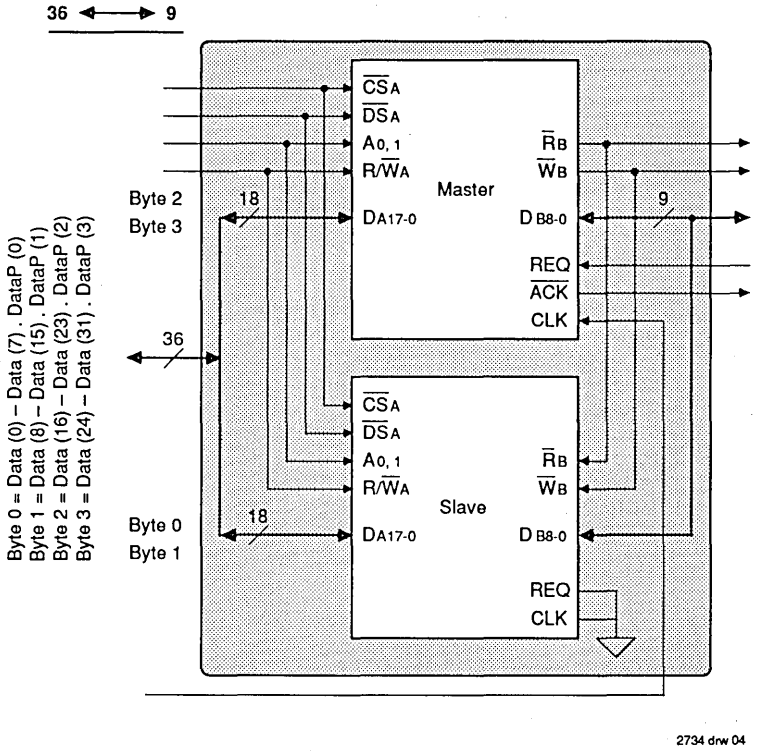


Figure 4. Peripheral Master/Slave Expansion

Byte ordering is adjustable by programming Bit 1 of Configuration Register 5 in both the Master and Slave devices. As an example, the least significant byte of the 36-bit Port A data bus in Figure 4 is defined to be Byte 0, then there are 4 byte orderings possible, as shown in Table 1.

Master	Slave	Byte Order
0	0	0, 1, 2, 3
0	1	1, 0, 2, 3
1	0	0, 1, 3, 2
1	1	1, 0, 3, 2

2734 tbl 01

Table 1. Byte Ordering

Processor Master/Slave Expansion Configuration

To implement the Processor Master/Slave expansion configuration, Port B responds to any read or write control signals input on the $\overline{DS}_B$ and $R/\overline{W}_B$ pins (in Motorola mode) or $\overline{R}_B$ and $\overline{W}_B$ (in Intel mode). The Processor Master/Slave expansion configuration is the same as the Peripheral Master/Slave expansion configuration, except Port B of the BiFIFOs is programmed in the Processor mode instead of the Peripheral mode. Even though the Peripheral mode is inactive, the CLK and REQ lines must be pulled low to satisfy the hardware reset requirement for the IDT72510/IDT72520. The Processor Master/Slave expansion configuration is shown in Figure 5.

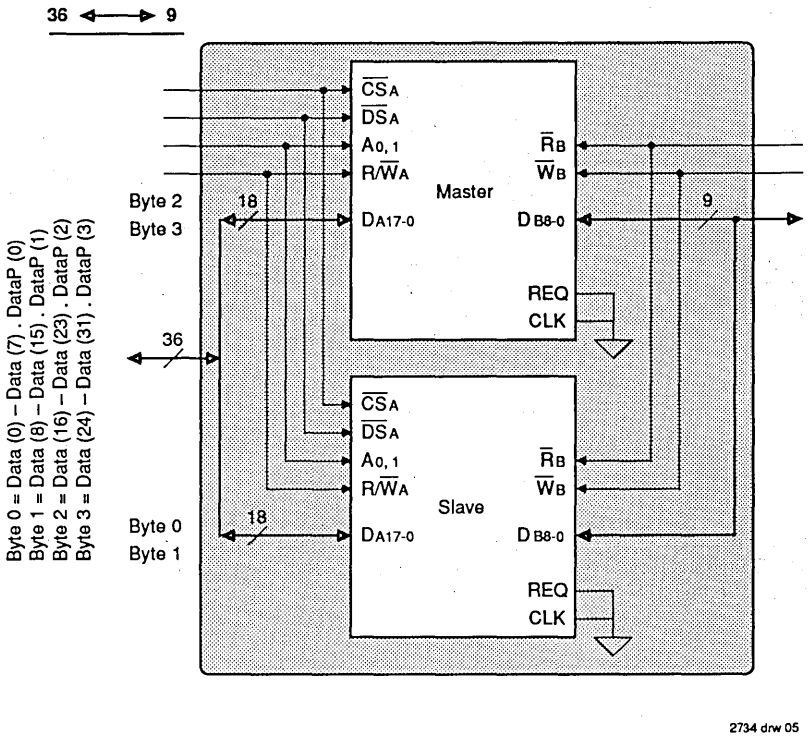


Figure 5. Processor Master/Slave Expansion

In this configuration, Port B of the master device waits for either a read or write strobe (or $\overline{DS}_B$, $R/\overline{W}_B$). The Master device lets the Slave device accept the first 2 read or write strobes. After the slave has completed 2 read or write cycles, the Master accepts the next 2 read or write inputs. The read/write control signals in the Processor mode are inputs, on the contrary, the read/write control signals in the Master Peripheral mode are outputs.

The byte order in which bytes are written into Port B in the Processor Master/Slave expansion configuration is also adjustable by programming Bit 1 of Configuration Register 5.

PARALLEL BiFIFO

The IDT72511/72521 are parallel bidirectional FIFOs configured as 18-to-18 in bus width. These BiFIFOs are ideal for data transferring between two processors or a processor and a peripheral of equal bus width. A single BiFIFO can support a 18-to-18 port configuration.

18-to-18

This is the default configuration of the IDT72511/72521. The core memory of Port A data bus is arranged in the order as follows: D_{A0}-D_{A7}, D_{A16}, D_{A8}-D_{A15}, D_{A17}. As for Port B: D_{B0}-D_{B7}, D_{B16}, D_{B8}-D_{B15}, D_{B17}. The entire data bus is used under the 18-to-18 configuration. In case the processors require only 16 bit data bus, the extra data bits can be disabled by letting all of the pins — D_{A16}, D_{A17}, and D_{B16}, D_{B17} — stay floating. An alternative is to tie a 10KΩ or greater resistor between each data bit and ground to minimize stand-by current. The data will then only be transferred between D_{A0}-D_{A15} and D_{B0}-D_{B15}.

Stand-Alone Expansion

The stand-alone expansion configuration allows an infinite numbers of BiFIFOs to be expanded in parallel to increase word width. No internal software programming is necessary to configure the stand-alone mode. A 36-bit or 32-bit data bus can simply be connected with two BiFIFOs in parallel as shown in Figure 6. The order of the data written into one port will output the exact data to the other port.

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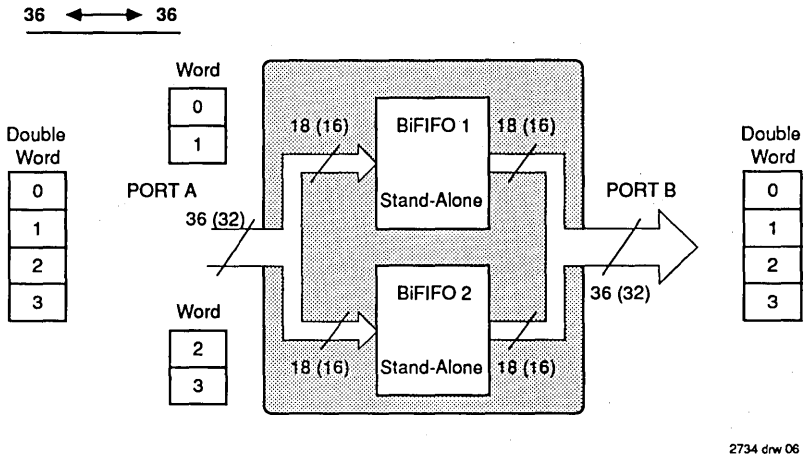

Figure 6. Stand-alone Expansion

The Master/Slave expansion configuration is not available in the Parallel BiFIFOs. The Processor or Peripheral interface mode for Port B operates in parallel BiFIFOs the same as the bus-matching BiFIFOs. This is programmed through Bit 10 of Configuration Register 5.

Integrated Device Technology, Inc.

THE BiFIFO BYPASS

APPLICATION NOTE AN-57

by John Chen and Steve Eldson

A bypass path on the IDT BiFIFO family allows small blocks of data to be exchanged directly between the processor connected to Port A and a peripheral controller on Port B. The bypass path is most useful for initializing peripherals and receiving messages from these peripherals. The bypass path is shown in the detailed block diagram of the BiFIFO (Figure 1).

BYPASS FUNCTION

The bypass path is enabled by setting the address select pins to $A_1 = 0$, $A_0 = 1$. In the bypass mode, the data bits from Port A (DA_7–DA_0, DA_{16}) are passed directly to Port B (DB_7–DB_0, DB_8) and the data bits from Port B are passed directly to Port A. Only lower byte DA_{16} and DA_7–DA_0 are passed through to DB_8–DB_0.

For a single BiFIFO configuration, bypass can only be enabled when the Port B interface pins are set to be outputs (peripheral interface mode). Bypass will not work if the Port B interface pins are set to be inputs (processor interface mode). Bits 10 to 12 of Configuration Register 5 must be programmed to 001 to put the BiFIFO in stand-alone peripheral interface mode.

When using the bypass path for two BiFIFOs in a 36-to-9-bit configuration, the Master and Slave devices must both be in peripheral interface mode. Bits 10 to 12 of the Master BiFIFO's Configuration Register 5 must be set to 111, while the Slave BiFIFO's bits must be set to 101. Since the byte data on (DA_7–DA_0, DA_{16}) pins of both Master and Slave will be passed to Port B bus concurrently, these two byte data should be identical to avoid data contention.

Because port B is placed in the DMA mode, the $\overline{DS}_B$ and R/$\overline{W}_B$ output pins reflect the action of $\overline{DS}_A$ and R/$\overline{W}_A$ input pins. The port B interface can operate either as an Intel– or a Motorola–style processor interface by programming Bit 0 of Configuration Register 5. For example, when Port B is programmed to a Motorola-style interface, $\overline{DS}_B$ follows the state of $\overline{DS}_A$. Similarly, R/$\overline{W}_B$ reflects the state of R/$\overline{W}_A$. If Port B is programmed to be an Intel–style interface, then the $\overline{DS}_A$ and R/$\overline{W}_A$ are translated to read strobe ($\overline{R}_B$) and write strobe ($\overline{W}_B$). The Intel read cycle ($\overline{R}_B$) is asserted LOW when $\overline{DS}_A$ is asserted LOW and R/$\overline{W}_A$ is HIGH. The Intel–style write signal ($\overline{W}_B$) is asserted LOW when $\overline{DS}_A$ is asserted LOW and R/$\overline{W}_A$ is LOW.

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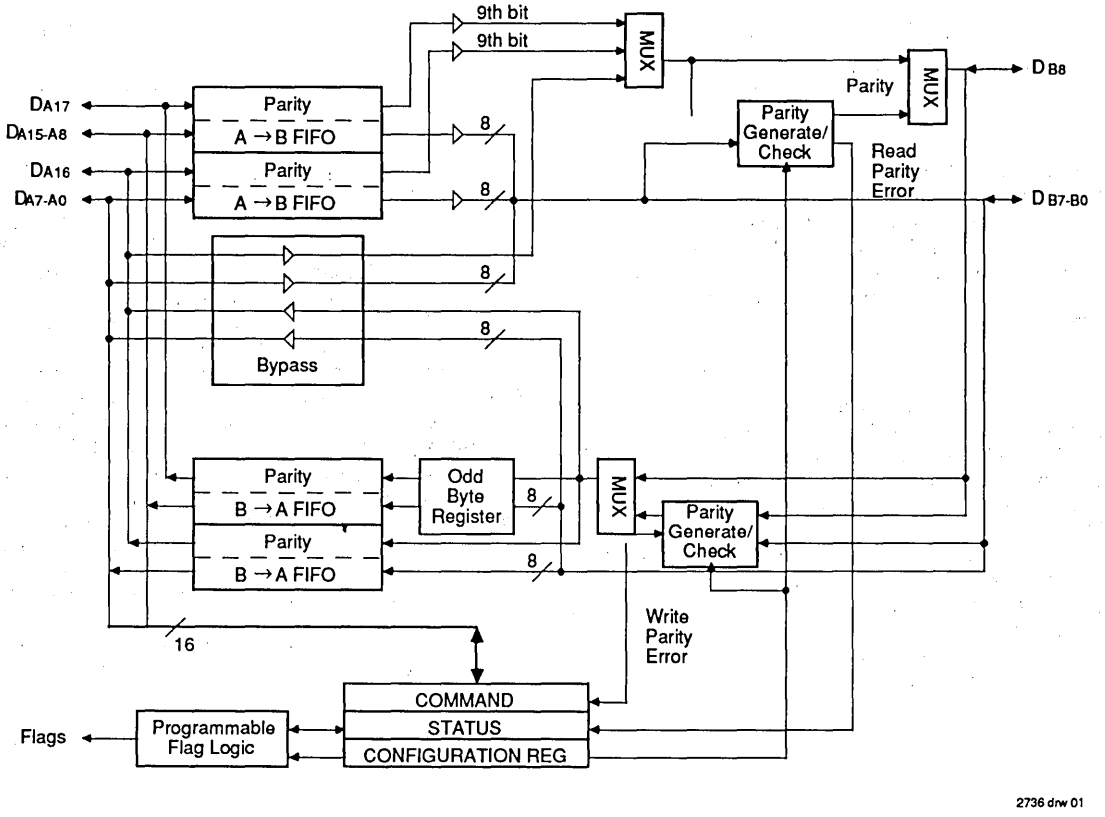

Figure 1. BiFIFO Functional Block Diagram

CONFIGURATION REGISTER 5 FORMAT

Bit	Function		
0	Select Port B Interface $\overline{R}_B$ & $\overline{W}_B$ or $\overline{DS}_B$ & R/$\overline{W}_B$	0	Pins are $\overline{R}_B$ and $\overline{W}_B$ (Intel-style interface)
		1	Pins are $\overline{DS}_B$ and R/$\overline{W}_B$ (Motorola-style interface)
1	Byte Order of 18-bit Word	0	Lower byte D_{A7}-D_{A0} and parity D_{A16} are read or written first on Port B
		1	Upper byte D_{A15}-D_{A8} and parity D_{A17} are read or written first on Port B
2	Full Flag Definition	0	Full Flag is asserted when write pointer meets read pointer
		1	Full Flag is asserted when write pointer meets reread pointer
3	Empty Flag Definition	0	Empty Flag is asserted when read pointer meets write pointer
		1	Empty Flag is asserted when read pointer meets rewrite pointer
4	REQ Pin Polarity	0	REQ pin active HIGH
		1	REQ pin active LOW
5	ACK Pin Polarity	0	ACK pin active LOW
		1	ACK pin active HIGH
7-6	REQ / ACK Timing	00	2 internal clocks between REQ assertion and ACK assertion
		01	3 internal clocks between REQ assertion and ACK assertion
		10	4 internal clocks between REQ assertion and ACK assertion
		11	5 internal clocks between REQ assertion and ACK assertion
8	Port B Read and Write Timing Control for Peripheral Mode	0	$\overline{R}_B$, $\overline{W}_B$, and $\overline{DS}_B$ are asserted for 1 internal clock
		1	$\overline{R}_B$, $\overline{W}_B$, and $\overline{DS}_B$ are asserted for 2 internal clocks
9	Internal Clock Frequency Control	0	internal clock = CLK
		1	internal clock = CLK divided by 2
10	Port B Interface Mode Control	0	Processor interface mode (Port B controls are inputs)
		1	Peripheral interface mode (Port B controls are outputs)
12-11	Width Expansion Mode Control	00	Stand-alone mode (18- to 9-bits, 36- to 18-bits)
		01	Reserved
		10	Slave width expansion mode (36- to 9-bits)
		11	Master width expansion mode (36- to 9-bits)
13	Unused		
14	Unused		
15	Unused		

Table 1. Register 5 Format

Integrated Device Technology, Inc.

DESIGNING WITH THE IDT SyncFIFO™: THE ARCHITECTURE OF THE FUTURE

APPLICATION NOTE AN-60

by J. Scott Gardner, Field Applications Engineer

INTRODUCTION

The use of First-In-First-Out (FIFO) buffers to pass information between digital circuits with differing data rates has been a standard practice in interface design. The IDT synchronous FIFO is a new architecture designed to support high-speed systems.

THE EVOLUTION OF FIFO ARCHITECTURES

The IDT SyncFIFO can be viewed as the third generation architecture in FIFO design. The initial FIFO architecture (illustrated in Figure 1) used an architecture based on a register array indexed by special control logic which sequenced a pointer within the array. Prior to the introduction of register-based FIFOs, designers used shift registers to buffer data between systems. More general than the shift register approach, the register-based FIFO architecture is also limited in depth, due to the number of transistors needed to build each flip-flop storage element.

The second-generation FIFO introduced very large buffers based on a static memory array. The RAM-based FIFO is shown in Figure 2. The internal RAM array is actually a dual-ported memory addressed by the use of internal pointers. These internal pointers determine which address of the RAM will provide the data during a FIFO READ or store data during a FIFO WRITE.

With the availability of large FIFOs with buffer memory as large as 4Kbytes, the need for memory management accentuated the need for external flags. These flags allow the user to monitor the amount of data in the FIFO. Most second-generation FIFOs have been enhanced to provide flags indicating a variety of FIFO conditions. Newer FIFOs, including the SyncFIFO, allow flags to be programmed to a selectable depth. Figure 3 is a block diagram of the enhanced asynchronous FIFOs.

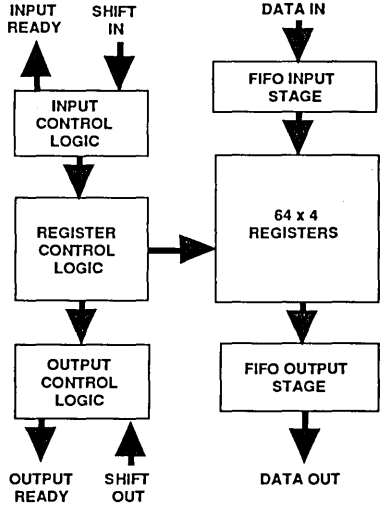

Figure 1. Register-Based FIFO Architecture—First Generation

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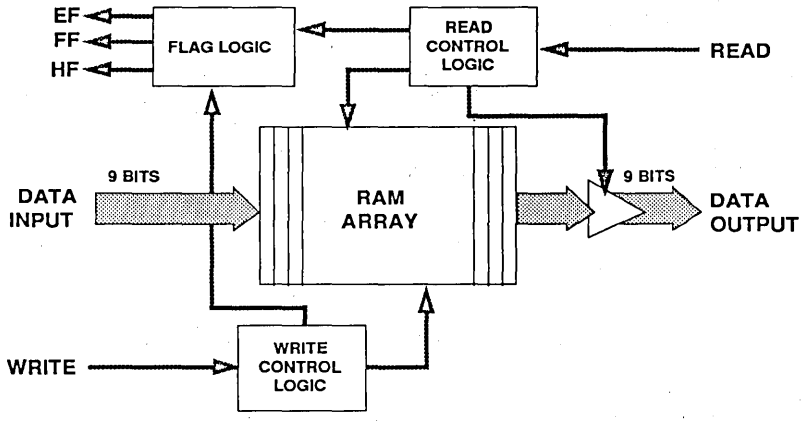

Figure 2. RAM-Based FIFO Architecture—Second Generation

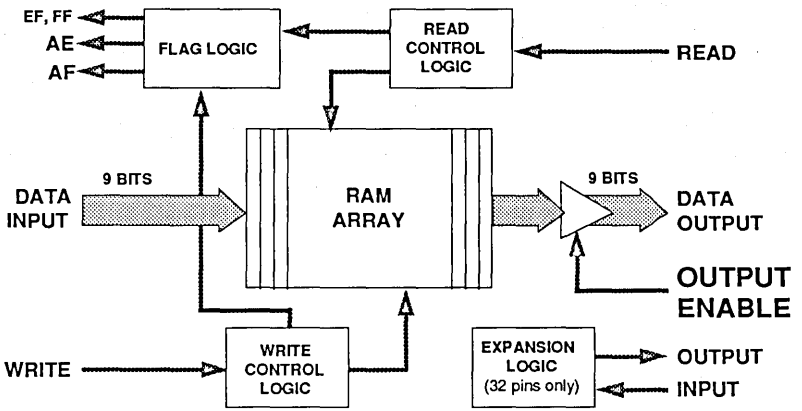

Figure 3. Enhanced Aynchronous FIFO

THE SyncFIFO ARCHITECTURE: THE ARCHITECTURE OF THE FUTURE

The SyncFIFO improves on the RAM-based FIFO architecture by adding input and output registers in the data path. These registers are controlled by independent external clocks, allowing data operations to be synchronized with the clock edges. Many system designers are designing high-speed systems using a synchronous approach, since the complexity of the control circuitry increases with speed in an asynchronous system. In a synchronous system, the amount of control logic is minimal and does not change as the system clock frequency is increased. As system clock rates approach 25MHz, it becomes more economical to use a synchronous design. (See Figure 4.)

ADVANTAGES OVER THE ASYNCHRONOUS FIFO

The concept of the synchronous FIFO is not new. Many synchronous designs requiring that data transfers occur on a clock edge use external registers with an asynchronous FIFO. The READ and WRITE control signals for the FIFO must be generated by special control logic, but the device accessing the FIFO through the registers sees the FIFO as a synchronous device. Figure 5 shows the asynchronous FIFO used in a synchronous application. The primary limitation of this approach is the performance degradation due to the long data set-up time needed by the FIFO. The performance loss is evident in operations requiring consecutive accesses, since the data set-up time must be taken into account when determining the maximum cycle time.

Using an asynchronous FIFO in a high-speed system can also require special design techniques for generating the FIFO control signals. As the cycle time is decreased in higher speed systems, the width of the READ or WRITE pulse becomes very small. The minimum pulse width for asynchronous FIFOs has been reduced to less than 20ns on faster devices. Generating accurately timed control pulses can require additional circuitry of greater complexity. Very narrow control pulses must be generated by using pulse shaping logic based on a system clock. It is sometimes difficult to generate properly timed narrow control pulses, since the timing margins become so small.

Figure 6 illustrates the simplicity of the IDT SyncFIFO interface. Passing data through the IDT SyncFIFO is based on a clock edge with a data set-up time of only 5ns and a data hold time of 1ns. A FIFO of this type allows clock rates of 50MHz. No external pulse shaping logic is required; the only control pulses required are the free-running system clock and a simple enable signal.

In systems using pipelining, the SyncFIFO can be used as a pipeline stage without external registers, as the registers that would normally be added externally for pipelining are included in the SyncFIFO. The use of pipelining can lead to even faster aggregate data rates.

REDUCED SENSITIVITY TO GLITCHES

Another problem faced by the designer of high-speed systems using fast asynchronous FIFOs is the sensitivity to glitches. A FIFO capable of responding to fast READ or WRITE pulses may recognize noise-induced glitches as valid control pulses. The minimum pulse widths are specified as worst-case values, and a designer must be careful to consider all operating conditions. A glitch which doesn't affect system operation during lab tests may become a problem at cold temperatures or higher supply voltages. Careful board design techniques or additional circuitry may be required in fast systems to reduce glitches on the READ and WRITE lines. By comparison, the SyncFIFO only recognizes READ and WRITE accesses during the transition of the clock signals, insuring increased noise immunity in the system.

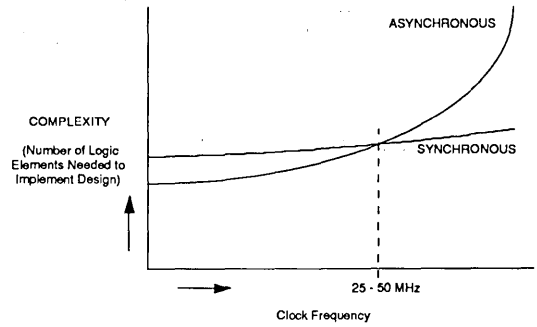

Figure 4. Increasing Clock Frequency Necessitates Synchronous Designs

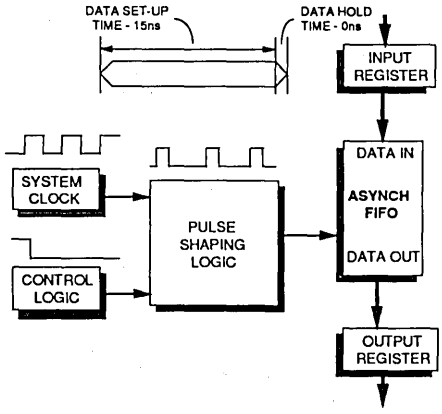

Figure 5. Typical Asynchronous Design

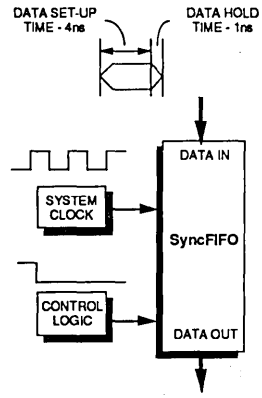

Figure 6. Typical Synchronous Design

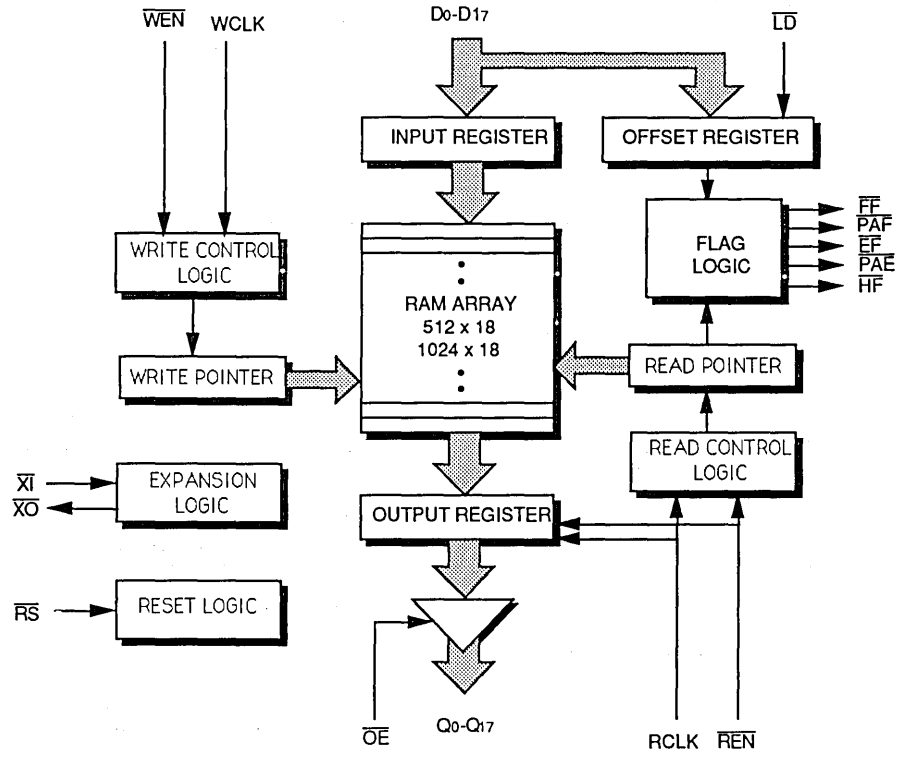

Figure 7. Block Diagram of the IDT SyncFIFO

FEATURES AND OPERATION OF THE SyncFIFO

Many of the features of IDT's SyncFIFOs are similar to the features of IDT's asynchronous FIFOs. Numerous Technical Notes and Application Notes have been published by IDT to assist the designer using asynchronous FIFOs; therefore, only the new features of the SyncFIFO will be covered in depth in this document.

The functional block diagram of the IDT SyncFIFO in standalone mode is shown in Figure 7. The first devices from IDT are the IDT72215 with a 512 x 18 memory array and the IDT72225 with a 1024 x 18 memory array. These devices allow for very fast throughput with read or write cycle times as fast as 20ns.

Many other sizes and word widths will be provided in subsequent devices. The speed of the IDT SyncFIFO is specified by the maximum clock rate. Both SyncFIFOs operate up to 50MHz. The synchronous nature of the architecture will allow the clock rate to increase in later products.

WIDTH EXPANSION

As in previous FIFOs, width and depth expansion are easily accomplished. Expanding the width of the FIFO is very straightforward. Basically, data passes in parallel through multiple devices. The input control signals are connected on all devices, and the status flags may be read from any device. Any word width may be attained which is a multiple of the device word size. Figure 8 shows how a 36-bit word is implemented using two 72215s or 72225s.

DEPTH EXPANSION

To expand in depth, a daisy-chain technique is used. The first FIFO in the chain is the master (designated by tying $\overline{FL}$ to ground). The remaining FIFOs in the chain are slave components (designated by tying $\overline{FL}$ to Vcc).

The master device is the device which controls all the flags and must always be the first device. The flags are ignored from the other devices. In the depth expansion mode, the Half-Full Flag ($\overline{HF}$) is not available, since this pin is shared with the Write Expansion Out ($\overline{WXO}$) signal.

To control how data is passed from one device to the other, Expansion In ($\overline{XI}$) and Expansion Out ($\overline{XO}$) signals are provided to control the transfer of data. In single device mode the $\overline{XI}$ lines are tied to ground. For multiple devices, the $\overline{XI}$ and $\overline{XO}$ lines are tied together between each device. Figure 9 is an example of the SyncFIFO used in depth expansion mode.

This example shows how three devices can be chained together to provide a deeper FIFO interface. Using three 72215s, the total depth is 1536 words of 18-bit data. This daisy-chain technique can be used to achieve depths up to 32,768 words by adding more devices.

The total depth of the configuration is programmed into the master device using the depth register. The total number of FIFOs in the configuration is loaded into the 5-bit register on the third Write Clock (WCLK) while the Load ($\overline{LD}$) pin and the Write Enable ($\overline{WEN}$) are held Low. Figure 10 shows all the possible values for the depth register of the 72215 and the 72225.

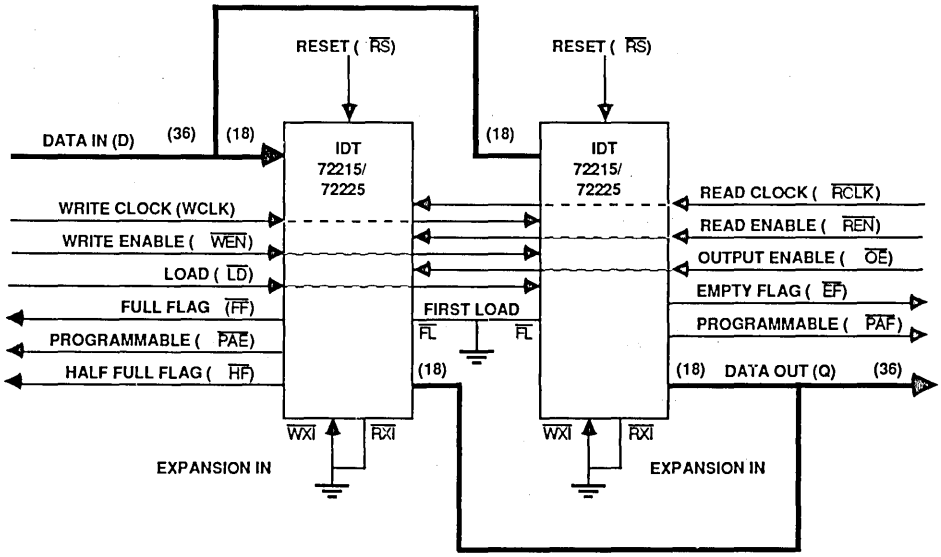

Figure 8. Width Expansion of the IDT SyncFIFO

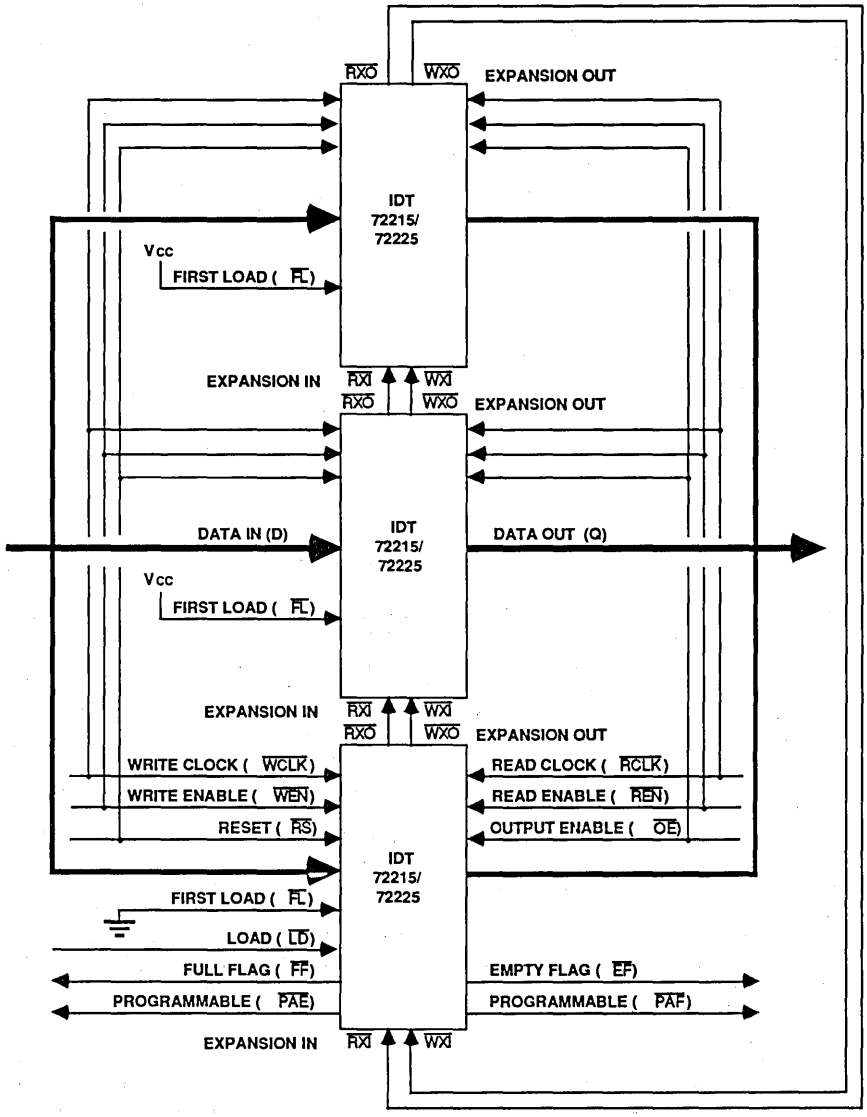

Figure 9. Depth Expansion of the IDT SyncFIFO

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IDT72215		IDT72225	
DATA LOADED IN DEPTH REGISTER	TOTAL DEPTH IN EXPANSION CONFIGURATION	DATA LOADED IN DEPTH REGISTER	TOTAL DEPTH IN EXPANSION CONFIGURATION
0 (DEFAULT)	512	0 (DEFAULT)	1024
1	512	1	1024
2	1024	2	2048
3	1536	3	3072
4	2048	4	4096
5	2560	5	5120
6	3072	6	6144
•	•	•	•
•	•	•	•
•	•	•	•

Figure 10. Depth Register Programming

$\overline{LD}$	$\overline{WEN}$	WCLK	SELECTION
0	0		EMPTY OFFSET FULL OFFSET DEPTH REGISTER
0	1		NO OPERATION
1	0		WRITE INTO FIFO
1	1		NO OPERATION

Figure 11. Offset Registers and the Depth Register

INDEPENDENT READ AND WRITE CLOCKS

Although the SyncFIFO handles data synchronously, the clocks are independent on each side of the FIFO. These clocks could even be free-running system clocks with different frequencies. The IDT SyncFIFO handles the transfer of data between the two systems, simplifying the timing issues normally associated with a system of this type. It is, however, possible to use the same clock for both sides of the FIFO.

USING FLAGS FROM THE IDT SyncFIFO

The flags available on the IDT72215 and IDT72225 are the Empty Flag ($\overline{EF}$), the Full Flag ($\overline{FF}$), the Half-full Flag ($\overline{HF}$) and two programmable flags. The Programmable Almost Empty ($\overline{PAE}$) and the Programmable Almost Full ($\overline{PAF}$) flags can be set to any location by the user.

These flags differ from the flags available on the latest asynchronous FIFOs in that they are updated on clock transitions. The $\overline{EF}$ is tied to RCLK and the $\overline{FF}$ is tied to WCLK. The three other flags are updated by either clock, depending on their current state (see data sheet). The impact of this difference will be discussed in the next section.

As with the asynchronous FIFOs, the flags operate based on the value of the internal pointers. Two separate pointers are maintained, a read pointer and a write pointer. When the last word is read from the FIFO, the read pointer equals the write pointer, and $\overline{EF}$ is asserted. When the write pointer reaches the last location in the FIFO and data is written, then $\overline{FF}$ is asserted. Likewise, the half-full flag is asserted whenever the difference between the Read pointer and Write pointer is ≥ half the size of the FIFO RAM array.

The programmable flags use offset values which are programmed into internal registers. For the $\overline{PAE}$ flag, the signal will be asserted when the Read pointer is *n* locations less than the Write pointer. As an example, suppose the FIFO is being used as a 175-word frame buffer. It is necessary to notify the processor when a frame has been received, but data may continue to arrive in the buffer. The Empty Offset Register would be programmed with the value 175. Using this value, the $\overline{PAE}$ flag would go High after 175 writes to the FIFO. The processor could receive this signal as an interrupt to read out the 175-word data block.

The $\overline{PAF}$ flag can be used to signal the processor after (FULL - m) writes to the FIFO. For instance, a certain system might take some time to respond to a signal from the FIFO and begin clocking out data. To notify the processor 6 write clocks in advance of the FIFO becoming full, a value of 6 is written into the Full Offset Register. This allows the user to optimize his system for the depth of the FIFO.

To write a value into one of the offset registers, $\overline{WEN}$ and $\overline{LD}$ are set Low. The data on the input data bus is written into the Empty Offset Register on the first Low-to-High transition of WCLK. On the second Low-to-High transition of WCLK, the Full Offset Register is written with the data inputs. The third clock transition programs the depth register. Figure 11 shows the manner in which the internal registers are programmed.

DESIGN CONSIDERATIONS

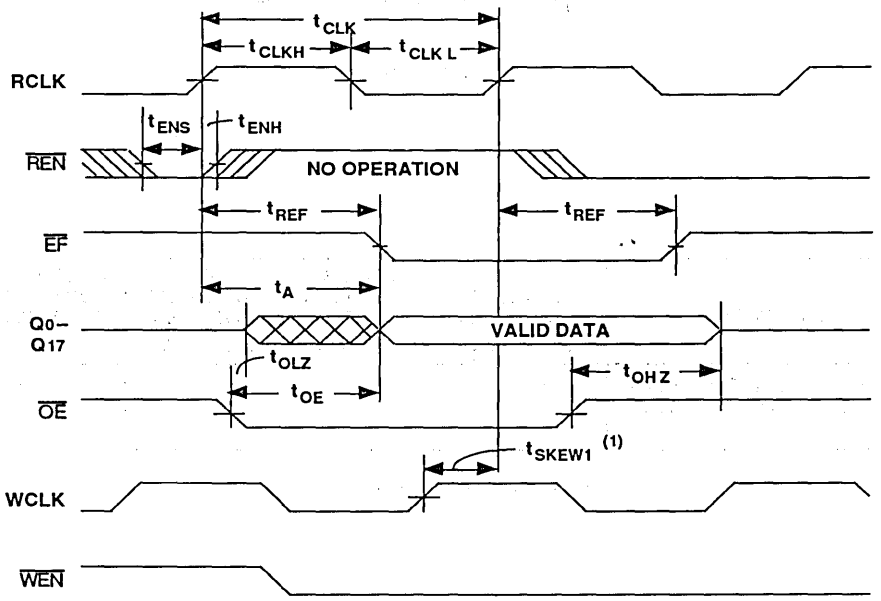
The simplicity of the interface to the SyncFIFO makes it an ideal candidate for new designs, especially when higher throughput is required. If the design is made synchronous at the outset, later speed improvements to a system do not require a redesign of the FIFO control logic.

One of the design considerations for the SyncFIFO concerns the manner in which the input and output registers interact with the internal RAM array. It is important to note that the data goes into the input register on the Low-to-High transition of the WCLK. During the first write to the FIFO, data is also stored into the internal RAM array on the same Low-to-High transition that loads the input register. This avoids the presence of a write latency cycle on the first Write.

To determine when data can be clocked out of the FIFO, the amount of skew between the WCLK and the following RCLK will determine if sufficient time has been allowed for the new data to be stored in the RAM. Once data has been clocked in using WCLK, the data will be available in the internal RAM for access by the read port after t_{SKEW1} ns (see Figures 12 and 13 for read and write cycle waveforms, and Figure 14 for the skew specifications). If this skew timing is not met, an extra cycle of latency will be required for clocking data from the FIFO.

The output register of the SyncFIFO adds a full cycle of read latency before data is available on the output pins. This latency is a result of the need to allow time for the flags to be updated. External circuitry may need extra time to respond to the flag signals. This is especially true for the $\overline{EF}$. If a single word is written into an empty FIFO, the $\overline{EF}$ will become deasserted t_{REF} ns after the following RCLK. This assumes that the RCLK occurs more than t_{SKEW} ns after the WCLK. If the skew time is not met, an additional RCLK cycle will be required before the $\overline{EF}$ can be asserted. The data will be available on the output pins t_A ns after the next RCLK.

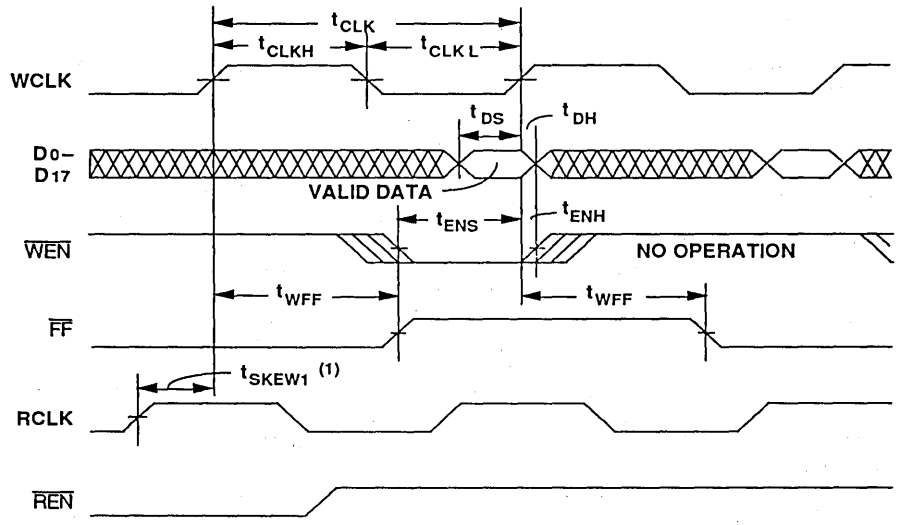
To help clarify the timing issues, consider an example of a system which uses coincident clocks by tying the RCLK and the WCLK lines together. The $\overline{WEN}$ and $\overline{REN}$ lines are used to control the transfer of data. If a single word is written into the FIFO on the WCLK, it will take two additional RCLKs before data will appear on the output pins. The coincident RCLK obviously does not meet the skew timing requirement. The first RCLK after the coincident WCLK/RCLK will update the flags and the second RCLK will affect the data transfer to the output pins.



NOTE:

1. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{EF}$ to change during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW1}, then $\overline{EF}$ may not change state until the next RCLK edge.

Figure 12. Read Cycle Timing



NOTE:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{FF}$ to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK edge.

Figure 13. Write Cycle Timing

SYMBOL	PARAMETER	COM'L 72215/16L20 72225/26L20		COM'L & MIL. 72215/16L25 72225/26L25		MIL. 72215/16L30 72225/26L30		COM'L & MIL. 72215/16L50 72225/26L50		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{SKEW1}	Skew time between Read Clock & Write Clock for Empty Flag & Full Flag	14	–	16	–	18	–	20	–	ns

Figure 14. Skew Specifications

EXAMPLES OF SyncFIFO DESIGNS

The application areas of the SyncFIFO are not different from applications of asynchronous FIFOs. Figure 15 shows an application of the SyncFIFO in a graphics system. An asynchronous FIFO could have been used for this application, but the speeds typically required by graphics systems would have made the implementation difficult. The data sent to the graphics rasterizer usually occurs as blocks of data, and repetitive writes to the FIFO require very fast cycle times.

Figure 16 shows how two SyncFIFOs can be used as a high-speed bidirectional interface between two 16-bit microprocessors. As in the previous example, an asynchronous FIFO might be sufficient for slow systems. The steady advance in processor speeds has led to the need for the SyncFIFO and its ability to handle the fast data rates.

In a microprocessor system the speed of the processor is very important, but of equal concern is the amount of bus bandwidth available for communicating with external devices. It is important that bus operations be accomplished as efficiently as possible. In the multiprocessing example, processor A usually needs to pass a block of data to processor B. The sooner the block of data is written into or read from the FIFO, the sooner the processor can return to its own processing tasks. The SyncFIFO is able to accommodate a block transfer rate of 50MHz or 100Mbytes/sec, including parity. Width expansion would allow for 400Mbytes/sec transfer rate in a 64-bit system. The SyncFIFO architecture will allow for the bandwidth requirements of even faster systems in the future.

USE IN ASYNCHRONOUS SYSTEMS

A SyncFIFO can be used in an asynchronous system; however, care must be taken in observing the timing considerations. Of primary concern is the minimum setup time for the $\overline{REN}$ or $\overline{WEN}$ signals. This is the time before the data can be clocked in or out of the FIFO registers. For instance, if the $\overline{MemWR}$ pulse in an asynchronous system is to be used to generate the WCLK pulse, care must be taken to insure that $\overline{WEN}$ occurs at least 8ns before the rising edge of WCLK (for a 20ns device). One method of generating the proper timing is to use a system clock to synchronize the control signal, thus insuring proper setup times.

In a simple asynchronous interface, the $\overline{WEN}$ pulse can be generated by the chip select pulse. The chip select pulse is generated by the FIFO address decoder. The $\overline{MemWR}$ signal can be used to drive the WCLK line. The data lines must be stable at least 5ns before the rising edge of the $\overline{MemWR}$ pulse.

To clock data asynchronously from the FIFO, the chip select line can be used to drive the $\overline{REN}$ line. The $\overline{MemRD}$ pulse can be inverted to provide a properly timed RCLK. The $\overline{REN}$ signal must meet the 8ns setup requirements (for a 20ns device). The extra latency cycle for reading data may be taken into account by the device reading the FIFO. The $\overline{EF}$ will go Low when the last word is stored in the output register.

It is possible to use the $\overline{MemRD}$ signal directly, but data won't be available until 12ns after the end of the $\overline{MemRD}$ pulse (worst case). The access time for the FIFO would have to include the width of the $\overline{MemRD}$ pulse. If the $\overline{MemRD}$ is inverted using a 7.5ns PAL, the asynchronous read is accomplished in about 20ns.

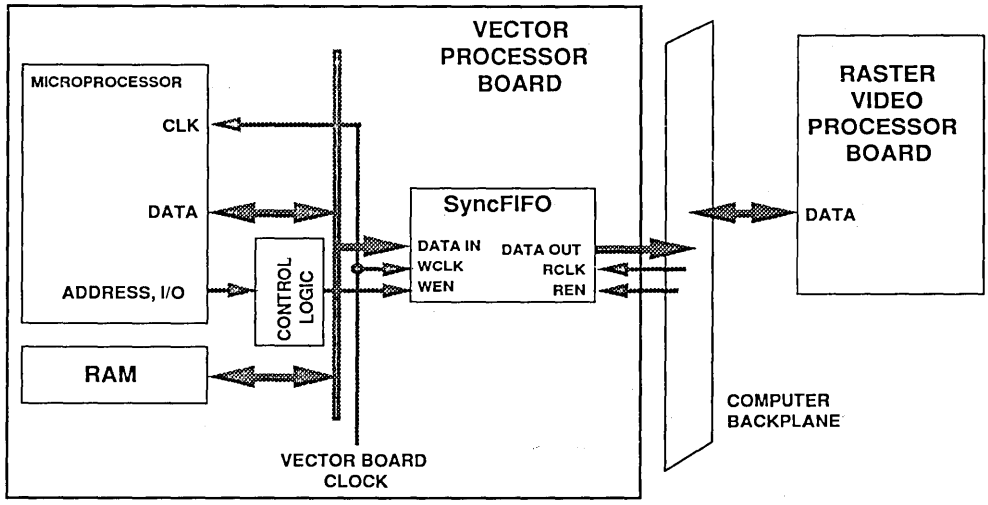


Figure 15. A Graphics System Using the SyncFIFO

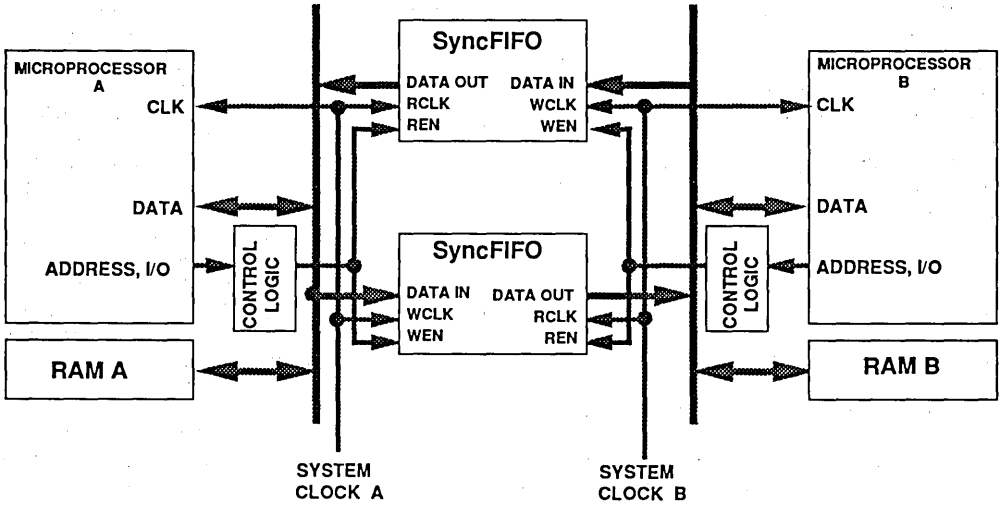


Figure 16. A Multiprocessing System Using the SyncFIFO

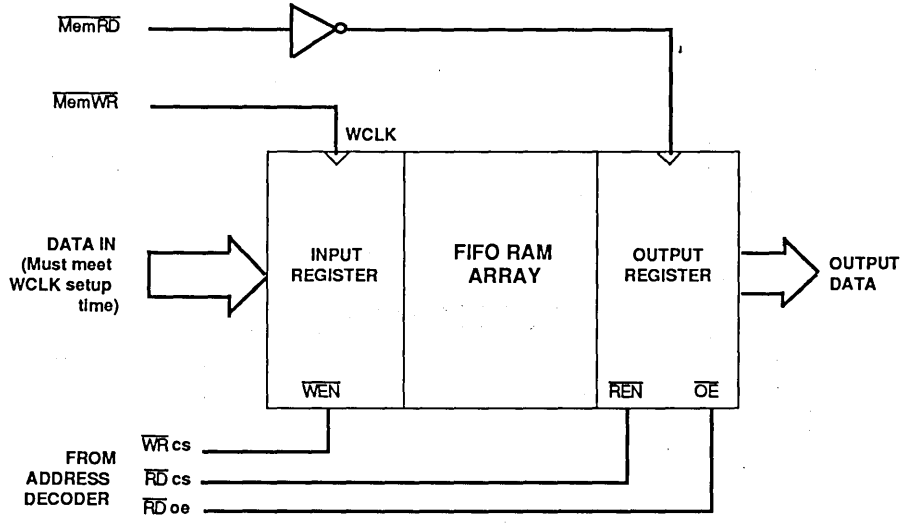


Figure 17. Using a SyncFIFO in an Asynchronous System

Figure 17 shows an example of the SyncFIFO used in a standard asynchronous system. A system of this type can be cycled much faster than previous solutions using asynchronous FIFOs. This system could also be enhanced to accommodate burst-mode data transfers available on newer processors. A simple counter could provide the burst pulse train needed to clock the data block. Also, note that the flags are synchronized with the clocks (see the next section).

HOW CLOCKS AFFECT FLAGS

Care must be taken in observing the flags in a SyncFIFO. For instance, upon reading the FIFO, the transfer of the last word from the memory array to the output register causes the assertion of the empty flag ($\overline{EF}$)—not the transfer of the last word of data out of the output register. The flags also differ from previous FIFOs in that the flags change synchronously. The flags are all updated on a clock transition.

One important consideration is that since the flags are updated synchronously, they are not updated until clocked. For instance, consider a system where the inputs are synchronous and the outputs are asynchronous. A word of data is written to the FIFO. The $\overline{EF}$ does not deassert until a clock transition on RCLK. So you could fill the FIFO without $\overline{EF}$ changing if no RCLKs are provided. One solution would be to tie any available fast clocks to RCLK. Another option would be to tie RCLK and WCLK together. (NOTE: $\overline{HF}$, $\overline{PAE}$ and $\overline{PAF}$ are asynchronous to the clocks on the 72215 and 72225. See data sheet for exact timing diagrams.) So, by using the $\overline{PAE}$ instead of the $\overline{EF}$ in this case, you can signal the asynchronous side of the status of the FIFO, since this flag is updated by both clocks.

CONCLUSION

Using the SyncFIFO greatly eases the design efforts in a high-speed system. The SyncFIFO incorporates all of the enhanced features of the newest asynchronous FIFOs. These features include programmable flags, the ability to store large amounts of data, and the ability to directly drive a 3-state data bus. It is the addition of the input and output registers that makes the SyncFIFO unique. The ability to handle very fast data rates allows the IDT SyncFIFO to keep pace with the high-speed systems being designed today and the faster systems still to come. The IDT SyncFIFO truly represents the architecture of the future.

Integrated Device Technology, Inc.

DEPTH EXPANSION OF IDT'S SYNCHRONOUS FIFOs USING THE RING COUNTER APPROACH

APPLICATION NOTE AN-69

By Bhanu V. R. Nanduri

INTRODUCTION

This application note describes a concise design approach to expand in depth IDT's synchronous FIFOs. As an example we will use the IDT72211 synchronous FIFO to demonstrate depth expansion using the ring counter approach. The discussion in this paper is however applicable to expand in depth all synchronous FIFOs from IDT. The first part of this paper discusses how one can expand in depth two IDT72211 synchronous FIFOs with the help of two industry standard PALs the 20R8s. The second part of this note discusses how one can accomplish depth expansion using four IDT72211s using three 20R8s, that is identical in pin out to a single large four-deep IDT72211. All PALs were programmed using "Capilano Computing Systems LPLC™ PLD software package" and a copy of the PAL programs is presented at the end of this paper. As the density and speed of industry standard PALs increases, it should be possible to expand in depth more of these FIFOs with a fewer number of PALs and with minimal loss in performance.

Traditionally, asynchronous FIFOs have been expanded in depth with the help of the $\overline{XI}$ and $\overline{XO}$ pins provided on these FIFOs. These FIFOs are cascaded in depth by connecting the $\overline{XO}$ pin of the present FIFO to the $\overline{XI}$ pin of the next FIFO in the cascade. This procedure is carried out for all the FIFOs in the cascade until the last FIFO in the cascade is reached. The $\overline{XO}$ pin of the last FIFO in the chain is connected to the $\overline{XI}$ pin of the first FIFO to complete the ring. A pin called the first load pin ($\overline{FL}$) on one of the FIFOs is grounded to indicate that the first write and read operations will begin in that FIFO. The $\overline{FL}$ pins of all the other FIFOs in the cascade are however tied to Vcc. The Full flags of all the FIFOs are ORed to provide a composite Full flag, similarly the Empty flags of all the FIFOs are ORed to provide a composite Empty flag. The user is urged to refer to IDTs technical note TN-09 "Cascading FIFOs or FIFO Modules" for further information on expanding asynchronous FIFOs.

The IDT72215 and the IDT72225 Synchronous FIFOs are provided with two pairs of $\overline{XI}$ and $\overline{XO}$ pins to assist the user in expanding these FIFOs using the daisy chain arrangement. One pair of $\overline{XI}$ and $\overline{XO}$ pins are used to synchronize write operations in the cascade and are controlled by the WCLK, while the other pair of $\overline{XI}$ and $\overline{XO}$ pins are used to synchronize read operations in the cascade and are controlled by the RCLK. Because of the $\overline{XI}$ and $\overline{XO}$ pins on the IDT72215 and the IDT72225 the daisy chain arrangement used in asynchronous FIFO expansion can be likewise used.

DEPTH EXPANSION OF IDT72211 SYNCFIFOS™

In this section we shall describe how to expand in depth the IDT72211 synchronous FIFO without any $\overline{XI}$ and $\overline{XO}$ pins. This discussion as stated earlier is applicable for expanding in depth all synchronous FIFOs from IDT. The expansion we will describe uses one ring counter to supervise the write operations and another ring counter to supervise the read operations. As a first step let us expand in depth two IDT72211s. Figure 1 illustrates the arrangement to carry out this two-deep depth expansion, the PAL labelled WRENCNTLR supervises the write operations whereas the PAL labelled RENCNTLR supervises the read operations. In addition to carrying out the write and the read operations these PALs also generate the Almost Full, Almost Empty, Full and Empty Flags for the expanded FIFO. Write operations in the IDT72211 are carried out when the two write enables are asserted and occur synchronously on the rising edge of the WCLK. Similarly the read operations are carried out when the two read enables are asserted and occur synchronously on the rising edge of the RCLK. The RCLK and the WCLK inputs of the FIFO can be tied together and connected to a system clock or they can be separately connected to two separate system clocks. The two system clocks can be of either the same frequency or different frequencies as long as the minimum clock period of the device is not violated. IDT synchronous FIFOs have a one deep pipelined architecture and because of this there will be a read latency of one cycle after reset.

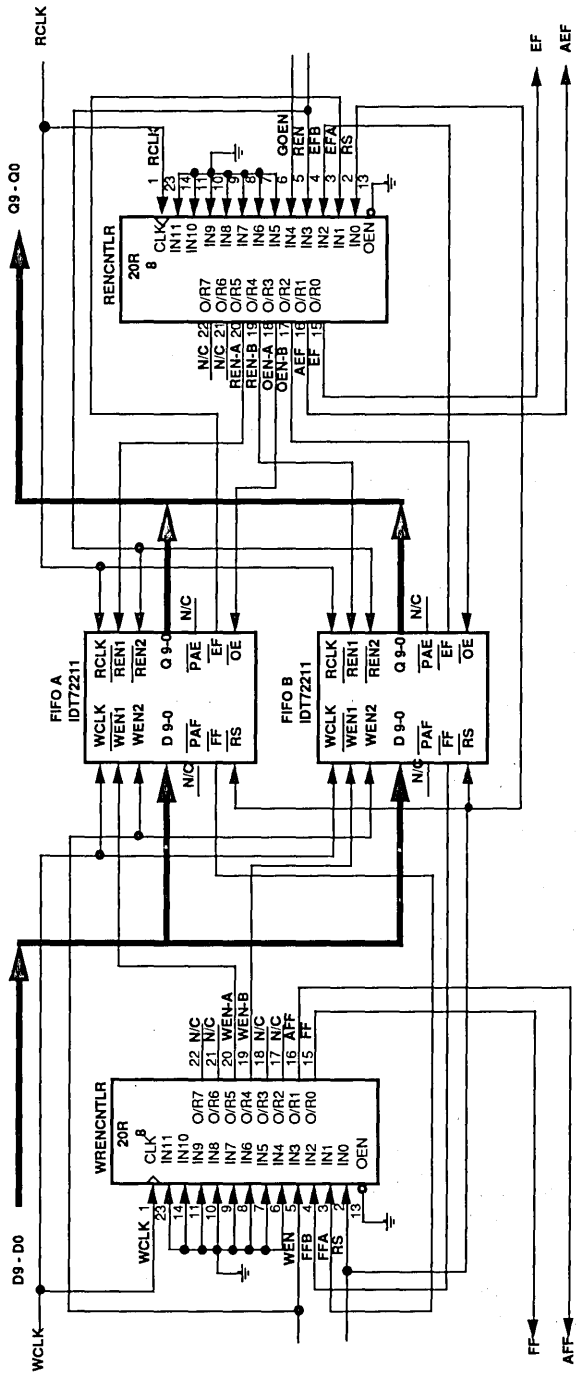


Figure 1.

2702 drw 01

DESCRIPTION OF THE WRITE ENABLE CONTROLLER (WRENCNTLR)

The write enable controller (WRENCNTLR) is implemented using a fast (t_{pd} = 7.5ns) industry standard 20R8 PAL. Write operations start when the user asserts the write clock and the global write enable "WEN" input to the WRENCNTLR. Write operations are performed synchronously and occur on the rising edge of the WCLK. After reset, the first write operation starts in FIFO A, the second in FIFO B, the third in FIFO A and the fourth in FIFO B. This pattern is repeated for all subsequent write operations. WEN2 inputs of FIFOs A and B are tied to the global write enable "WEN" as shown. The WRENCNTLR provides separate WEN1 strobes to each FIFO. These strobes have been labelled $\overline{WEN\_A}$ and $\overline{WEN\_B}$. A user can stop the write operations to the FIFO by deasserting the global write enable (WEN) input. This will ensure that the WRENCNTLR will stall the present WEN1 signal and not generate the next WEN1 pulse. Care has been taken to ensure that even if the user asserts the global write enable (WEN) input to the WRENCNTLR, the WRENCNTLR will not generate the next WEN1 pulse when the composite Full flag is asserted. The composite Full flag will be asserted when all the FIFOs in the cascade have their Full flags asserted. The WRENCNTLR thus remains in the same state until the composite Full flag is deasserted ensuring that the same write sequence is maintained. The WRENCNTLR will generate an Almost Full flag only when any one of the FIFOs asserts a Full flag. This gives the user a prior warning of one word that he is approaching the end of his data queue. All outputs generated by the WRENCNTLR occur synchronously and are asserted and deasserted on the rising edge of the WCLK.

The FIFOs will each assert their Full flags after 512 words have been written into them but only if no read operations had occurred during this period. A write operation that is performed while the Full flag is asserted is ignored by the FIFOs. Internal to the IDT72211 and transparent to the user is a write inhibit signal that is generated when the FIFO is full. This signal blocks out any subsequent write operations that occur, ensuring that the state of the internal write pointer is not altered and the data in the FIFO is not overwritten.

DESCRIPTION OF THE READ ENABLE CONTROLLER (RENCNTLR)

The read enable controller (RENCNTLR) like the write enable controller is implemented using a fast industry standard PAL, the 20R8. Read operations start when the user enables the read clock (RCLK) and asserts the active low global read enable input ($\overline{REN}$) and the active low global output enable input ($\overline{GOEN}$) to the RENCNTLR. In our design read sequences are identical to write sequences. Hence after reset the first read starts in FIFO A, the second in FIFO B, the third in FIFO A and the fourth in FIFO B. This pattern is repeated for all subsequent read operations. The $\overline{REN2}$ inputs of FIFOs labelled A and B are tied to the global read enable "$\overline{REN}$" as shown. The RENCNTLR provides separate $\overline{REN1}$ strobes to each FIFO, these $\overline{REN1}$ signals have been labelled $\overline{REN\_A}$ and $\overline{REN\_B}$, in addition the RENCNTLR provides separate output enables labelled $\overline{OEN\_A}$ and $\overline{OEN\_B}$. $\overline{OEN\_A}$ follows $\overline{REN\_A}$ and $\overline{OEN\_B}$ follows $\overline{REN\_B}$. A user wishing to stop the read operations can do so by deasserting the global read enable ($\overline{REN}$) input to the RENCNTLR. This will ensure that the RENCNTLR will stall the present $\overline{REN1}$ signal and not generate the next $\overline{REN1}$ pulse. Care has been taken to ensure that even if the user asserts the global read enable ($\overline{REN}$) to the RENCNTLR, the RENCNTLR will not generate the next $\overline{REN1}$ pulse if the composite Empty flag is asserted. The RENCNTLR thus remains in the same state until the composite Empty flag is deasserted thus ensuring that the same read sequence is maintained. The RENCNTLR will generate an Almost Empty flag only when one of the FIFOs asserts its Empty flag. This give the user a prior warning of one word that he is approaching the end of his data queue. The RENCNTLR also generates the composite Empty flag when both the FIFOs in the cascade assert their Empty flags. All outputs generated by the RENCNTLR occur synchronously and are asserted and deasserted on the rising edge of the RCLK.

The IDT72211 synchronous FIFO is provided with a transparent output register on the read port. This register is loaded with a new word once every read cycle (provided the FIFO is not empty). This register puts its contents on the output bus only when the output enable input ($\overline{OE}$) is asserted. The function of this output register is to allow the user multiple reads of the same word without incrementing the internal read pointer. A user interested in reading the same word multiple times without altering the state of the internal read pointer can do so by disabling the $\overline{REN1}$ and $\overline{REN2}$ inputs to the FIFO while asserting its output enable. The user can then sample the output pins of the FIFO once every read clock cycle multiple times. The user can also skip sampling certain data by deasserting the output enable ($\overline{OE}$) while asserting the read enables ($\overline{REN1}$) and ($\overline{REN2}$).

A user wishing to read the same word in our expanded FIFO without incrementing the read pointer can do so by deasserting the global read enable ($\overline{REN}$) input while asserting the global output enable ($\overline{GOEN}$) of the RENCNTLR. This operation stalls the read operations and the data in the output register can then be sampled. The user can then sample this output once every read clock cycle for multiple read cycles. Since the IDT SyncFIFOs have a one deep pipelined architecture, depth expansion as described in this section will result in a read latency of one cycle after reset.

The FIFOs each assert their respective Empty flags after 512 words have been read from them and only if no write operations had occurred during this period. A read operation that is performed while an Empty flag is asserted is ignored by the FIFO, it will still however supply the last word read from the FIFO. Internal to the IDT72211 and transparent to the user is a read inhibit signal that is generated when the FIFO is empty. This signal, analogous to the write inhibit signal, is used to block out any subsequent read operations that occur, ensuring that the state of the internal read pointer is not altered and data in the FIFO's RAM array is not re-read.

TIMING REQUIREMENTS

Figure 2. and Figure 3. illustrate the timing waveforms for the write and read operations. The timing parameters for the Synchronous FIFO expansion are shown in Table 1. To operate the 15ns IDT72211 Synchronous FIFO we would need a 20R8 PAL whose maximum t_{CO} is 4ns. As these devices are not yet available in these speed grades we have to operate our 15ns FIFOs with a clock period of 17.5ns minimum. The reason for this is that the RENCNTLR asserts the read and output enable signals on the rising edge of the RCLK but with a maximum delay of 6.5ns induced by the PAL. The IDT72211 has a t_{OE} specified at 8ns maximum, this implies that 14.5ns ($t_{CO} + t_{OE} = 6.5 + 8$ns) after the rising edge of the RCLK, data will be available for sampling. Assuming the sampling side samples the output of the FIFOs also on the rising edge of the RCLK, this leaves only 0.5ns ($t_{CLK} - t_{CO} - t_{OE} = 15 - 14.5$ns) before the next arrival of a positive edge on the RCLK. This duration may be too short for the sampling side's set-up time requirements. Therefore if we use the RCLK period of 17.5ns, this would give the sampling side a data set-up time of 3ns, which is a reasonable data set-up time. The user is urged to refer to the IDT72211 and the 20R8 PAL's data sheets for more information on the timing requirements.

Parameter Symbol	Parameter Description	Min.	Max.
t_{CO}	PAL's Clock to output delay	3ns	6.5ns
t_S	PAL's Set-up time to clock	7ns	—
t_{RSS}	FIFO's reset set-up time	10ns	—
t_{ENS}	FIFO's enable set-up time	4ns	—
t_{ENH}	FIFO's enable hold time	1ns	—
t_{DS}	FIFO's data set-up time	4ns	—
t_{DH}	FIFO's data hold time	1ns	—
t_{OE}	FIFO's output enable time	—	8ns
t_{OHZ}	FIFO's output disable time	1ns	8ns
t_{CLK}	FIFO and PAL Clock period	17.5ns	—

2702 tbl 01

Table 1.

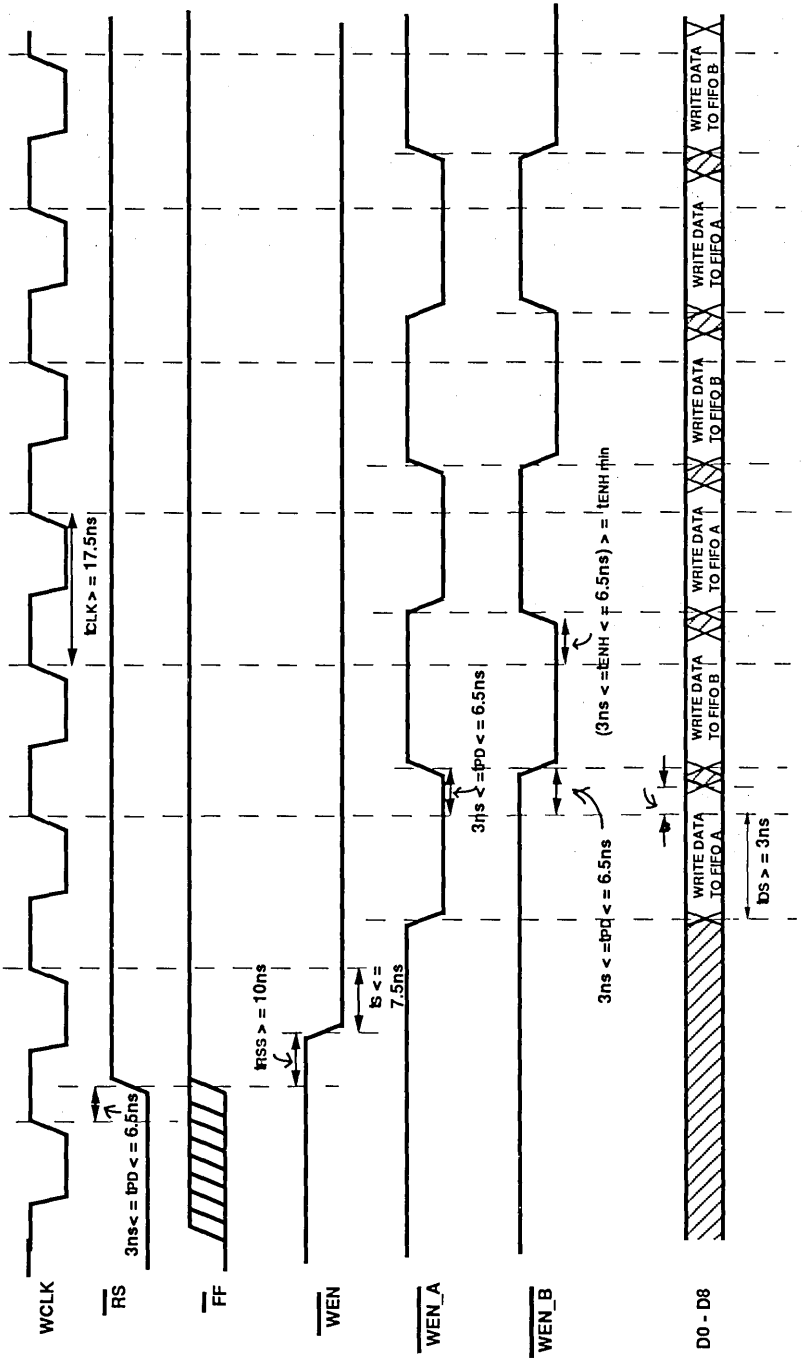


Figure 2. Write Cycle Timing

2702 drw 02

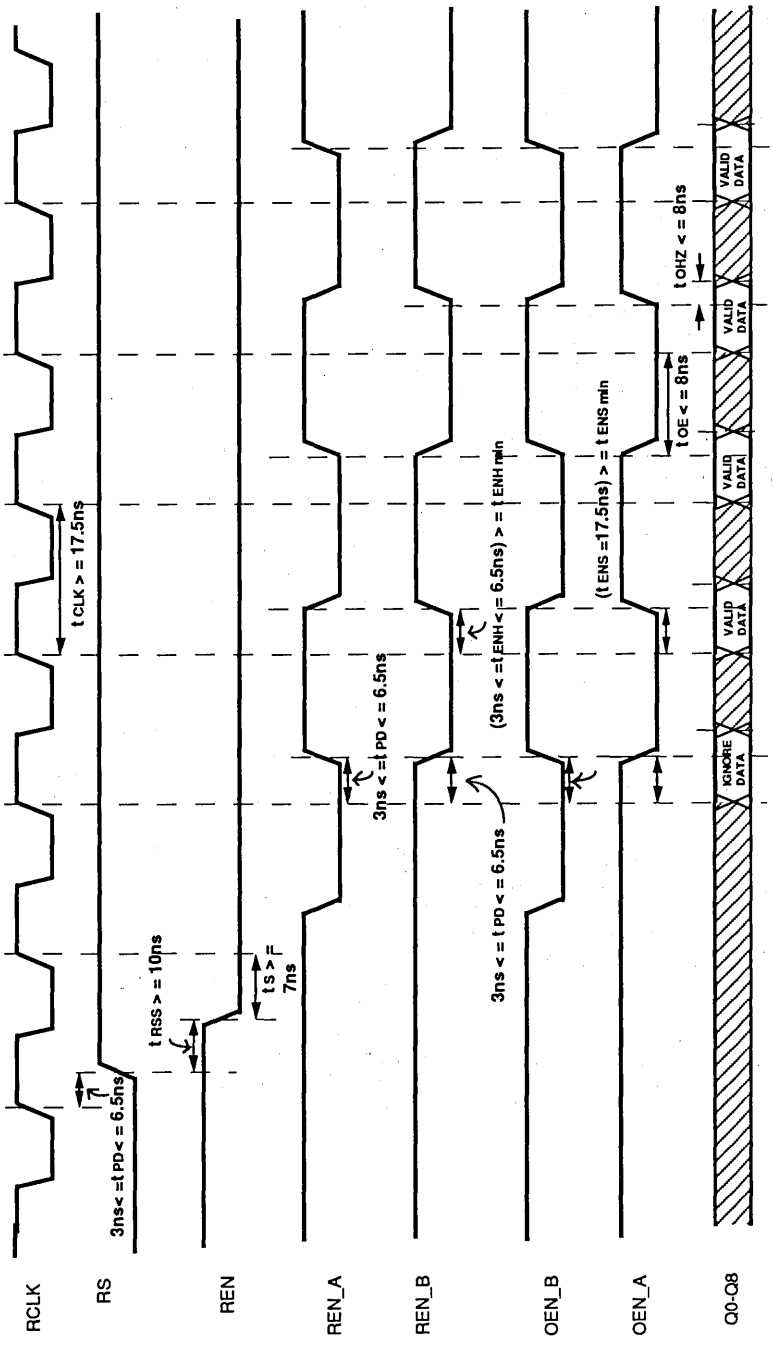


Figure 3. Read Cycle Timing

2702 drw

FOUR DEEP DEPTH EXPANSION OF THE IDT72211 SYNCFIFOS ™

The discussion on the two deep depth expansion using the ring counter approach, described earlier is also applicable in this section for a four-deep depth expansion. Figure 4 illustrates the four-deep depth expansion. Write operations will start when the user asserts the write clock (WCLK) and the active high global write enable "WEN" input to the WRENCNTLR. Write operations are performed synchronously and occur on the rising edge of the WCLK. After reset, the first write operation starts in FIFO A, the second in FIFO B, the third in FIFO C and the fourth in FIFO D. This pattern is repeated for all subsequent write operations. WEN2 inputs of FIFOs A, B, C and D are tied to the global write enable "WEN" as shown. The WRENCNTLR provides separate $\overline{WEN1}$ strobes to each FIFO. These strobes have been labelled $\overline{WEN\_A}$, $\overline{WEN\_B}$, $\overline{WEN\_C}$ and $\overline{WEN\_D}$. A user can stop the write operations to the FIFO by deasserting the global write enable (WEN) input. This will ensure that the WRENCNTLR will stall the present $\overline{WEN1}$ signal and not generate the next $\overline{WEN1}$ pulse. Even if the user asserts the global write enable (WEN) input to the WRENCNTLR, the WRENCNTLR will not generate the next $\overline{WEN1}$ pulse while the composite Full flag is asserted. The WRENCNTLR thus remains in the same state until the composite Full flag is deasserted ensuring that the same write sequence is maintained. The WRENCNTLR will generate an Almost Full flag only when any one of the FIFOs asserts a Full flag. This gives the user a prior warning of three words that he is approaching the end of his data queue. The WRENCNTLR will also generate a composite Full flag when all the FIFOs assert their Full flags. All outputs generated by the WRENCNTLR occur synchronously and are asserted and deasserted on the rising edge of the WCLK.

In the four-deep depth expanded FIFO design we need to generate four read enables and four output enables to perform the read operations successfully. In addition we need to generate an Almost Empty Flag and a composite Empty Flag. The 20R8 PALs that we are using have a maximum of eight outputs only, hence this implies that we need to use at least two 20R8s to perform the read operations successfully. As the density and the functional capabilities of PALs increases it should be possible to implement the RENCNTLR using a single PAL.

Read operations start when the user enables the read clock (RCLK) and asserts the active low global read enable input ($\overline{REN}$) to the RENCNTLR, in addition the user will have to assert the global ($\overline{GOEN}$) input to the OENCNTLR. The OENCNTLR generates the separate output enable inputs to FIFOs labelled A, B, C and D. In our design read sequences are identical to write sequences. Hence after reset the first read starts in FIFO A, the second in FIFO B, the third in FIFO C and the fourth in FIFO D. This pattern is repeated for all subsequent read operations. The $\overline{REN2}$ inputs of FIFOs labelled A, B, C and D are tied to the global read enable "$\overline{REN}$" as shown. The RENCNTLR provides a separate $\overline{REN1}$ strobe to each FIFO, these strobes have been labelled $\overline{REN\_A}$, $\overline{REN\_B}$, $\overline{REN\_C}$, and $\overline{REN\_D}$. A user wishing to stop the read operations can do so by deasserting the global read enable ($\overline{REN}$) input to the RENCNTLR. This will ensure that the RENCNTLR will stall the present $\overline{REN1}$ signal and not generate the next $\overline{REN1}$ pulse. Even if the user asserts the global read enable ($\overline{REN}$) to the RENCNTLR, the RENCNTLR will not generate the next $\overline{REN1}$ pulse if the present FIFO in the cascade has its Empty flag asserted. The RENCNTLR thus remains in the same state until the composite Empty flag is deasserted thus ensuring that the same read sequence is maintained. The RENCNTLR will generate an Almost Empty flag only when one of the FIFOs asserts its Empty flag. This give the user a prior warning of three words that he is approaching the end of his data queue. The RENCNTLR also generates the composite Empty flag when all the FIFOs in the cascade assert their Empty flags. All outputs generated by the RENCNTLR occur synchronously and are asserted and deasserted on the rising edge of the RCLK. The OENCNTLR generates separate output enables to the FIFOs, these separate output enables $\overline{OEN\_A}$, $\overline{OEN\_B}$, $\overline{OEN\_C}$ and $\overline{OEN\_D}$ follow the read enables $\overline{REN\_A}$, $\overline{REN\_B}$, $\overline{REN\_C}$ and $\overline{REN\_D}$.

A user wishing to read the same word in our expanded FIFO without incrementing the read pointer can do so by deasserting the global read enable ($\overline{REN}$) input to the RENCNTLR and asserting the global output enable ($\overline{GOEN}$). This operation stalls the read operation but will assert the output enable of one of the FIFOs which contains the data to be sampled. The user can then sample this output once every read clock cycle for multiple read cycles. Because of this one deep pipelined architecture there occurs a read latency of one cycle after reset in our four deep FIFO expansion.

SUMMARY

Expanding Synchronous FIFOs in depth can be very easily accomplished as discussed in this paper with minimum external logic. As the density, functionality and speed of industry standard PALs increases, it will be possible to expand these FIFOs to even larger depths without incurring any loss in performance.

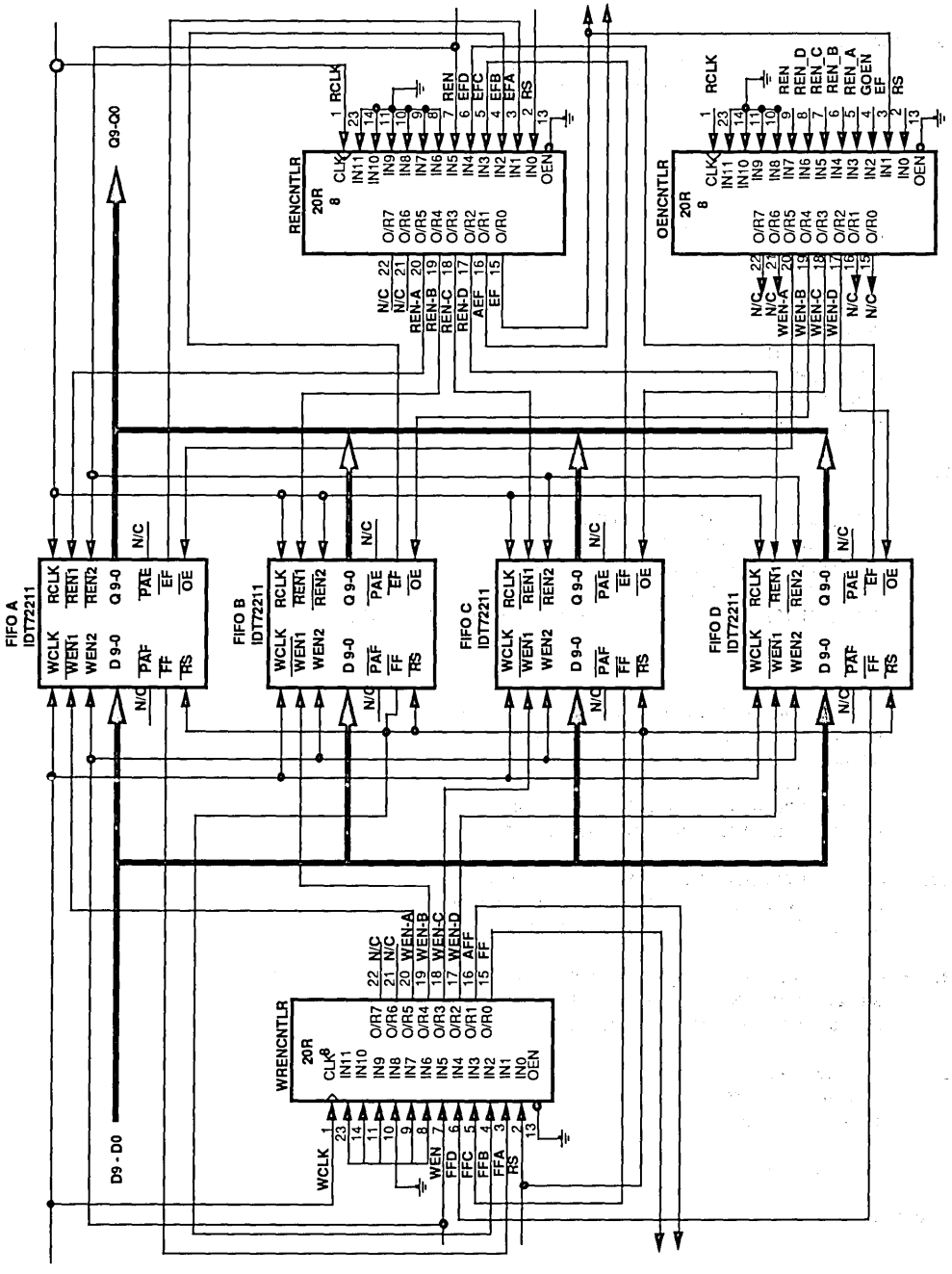


Figure 4.

2702 drw 04

```
{AUTHOR:        BHANU V. R. NANDURI
 COMPANY:       INTEGRATED DEVICE TECHNOLOGY
 DATE:          01/24/89
 }
 MODULE X2WENCNTLR;          { THIS PAL IS USED TO CONTROL THE
                               WRITE OPERATIONS IN A TWO DEEP
                               X9 OR X8 FIFO EXPANSION SCHEME }
 TITLE X2WENCNTLR;
 TYPE MMI 20R8;

 INPUTS;

 {WCLK          NODE[PIN1];} {WCLK INPUT}
 RS             NODE[PIN2];  {SYNCHRONOUS RESET INPUT}
 FFA            NODE[PIN3];
 FFB            NODE[PIN4];
 WEN            NODE[PIN5];
 C0             NODE[PIN22];
 WEN_A          NODE[PIN20];
 WEN_B          NODE[PIN19];
 FF             NODE[PIN15];

 OUTPUTS;

 WEN_A          NODE[PIN20]; {WEN1 TO FIFO A}
 WEN_B          NODE[PIN19]; {WEN1 TO FIFO B}
 AFF            NODE[PIN16]; {ALMOST FULL FLAG FOR THE EXPANSION}
 FF             NODE[PIN15]; {FULL FLAG FOR THE EXPANSION}
 C0             NODE[PIN22]; {C0 IS BIT 0 OF THE TWO BIT COUNTER}

 TERMS;

 C0 NOT   :=  RS AND !WEN AND !WEN_A AND FF AND C0 OR
              RS AND !WEN AND !WEN_B AND !FF AND !C0 OR
              RS AND !WEN AND WEN_A AND WEN_B AND !FF AND !C0 OR
              RS AND WEN AND !WEN_B AND !C0 OR
              RS AND WEN AND WEN_A AND WEN_B AND !C0 OR
              RS AND !WEN AND WEN_A AND WEN_B AND !C0;

 WEN_A NOT:= RS AND !WEN AND WEN_B AND WEN_A AND C0 OR
              RS AND !WEN AND !WEN_B AND FF AND !C0 OR
              RS AND !WEN AND !WEN_A AND !FF AND C0;

 WEN_B NOT:= RS AND !WEN AND WEN_B AND WEN_A AND !C0 OR
              RS AND !WEN AND !WEN_A AND FF AND C0 OR
              RS AND !WEN AND !WEN_B AND !FF AND !C0;

 AFF NOT  := !FFA AND FFB OR
              FFA AND !FFB OR
              !FFA AND !FFB;

 FF NOT   := !FFA AND !FFB;
 END;
 END X2WENCNTLR.
```

```
{AUTHOR:        BHANU V. R. NANDURI
 COMPANY:       INTEGRATED DEVICE TECHNOLOGY
 DATE:          01/24/89
 }
 MODULE X2RENCNTLR;          { THIS PAL IS USED TO CONTROL THE
                               READ OPERATIONS IN A TWO DEEP
                               X9 OR X8 FIFO EXPANSION SCHEME }
 TITLE X2RENCNTLR;
 TYPE MMI 20R8;

 INPUTS;

 {WCLK          NODE[PIN1];}  {RCLK INPUT}
 RS             NODE[PIN2];   {SYNCHRONOUS RESET INPUT}
 EFA            NODE[PIN3];
 EFB            NODE[PIN4];
 REN            NODE[PIN5];
 OEN            NODE[PIN6];
 C0             NODE[PIN22];
 REN_A          NODE[PIN20];
 REN_B          NODE[PIN19];
 OEN_A          NODE[PIN18];
 OEN_B          NODE[PIN17];
 EF             NODE[PIN15];

 OUTPUTS;

 REN_A          NODE[PIN20];  {REN1 TO FIFO A}
 REN_B          NODE[PIN19];  {REN1 TO FIFO B}
 OEN_A          NODE[PIN18];  {OEN1 TO FIFO A}
 OEN_B          NODE[PIN17];  {OEN1 TO FIFO B}
 AEF            NODE[PIN16];  {ALMOST EMPTY FLAG FOR THE EXPANSION}
 EF             NODE[PIN15];  {EMPTY FLAG FOR THE EXPANSION}
 C0             NODE[PIN22];  {C0 IS BIT 0 OF THE TWO BIT COUNTER}

 TERMS;

 C0 NOT  :=   RS AND !REN AND !REN_A AND EF AND C0 OR
              RS AND !REN AND !REN_B AND !EF AND !C0 OR
              RS AND REN AND !REN_B AND !C0 OR
              RS AND REN AND REN_A AND REN_B AND !C0 OR
              RS AND !REN AND REN_A AND REN_B AND !C0;

 REN_A NOT :=RS AND !REN AND REN_B AND REN_A AND C0 OR
              RS AND !REN AND !REN_B AND EF AND !C0 OR
              RS AND !REN AND !REN_A AND !EF AND C0;

 REN_B NOT :=RS AND !REN AND  REN_B AND REN_A AND !C0 OR
              RS AND !REN AND !REN_A AND EF AND C0 OR
              RS AND !REN AND !REN_B AND !EF AND !C0;

 OEN_A NOT :=RS AND !OEN AND !OEN_A AND REN_A AND REN_B AND C0 OR
              RS AND !OEN AND !OEN_B AND !REN_A AND EF AND C0 OR
              RS AND !OEN AND OEN_A AND OEN_B AND REN_A AND REN_B AND C0 OR
              RS AND !OEN AND OEN_A AND OEN_B AND !REN_A AND EF AND C0;
```

```
OEN_B NOT :=RS AND !OEN AND !OEN_B AND REN_A AND REN_B AND !C0 OR
            RS AND !OEN AND !OEN_A AND !REN_B AND EF AND !C0 OR
            RS AND !OEN AND OEN_A AND OEN_B AND REN_A AND REN_B AND !C0 OR
            RS AND !OEN AND OEN_A AND OEN_B AND !REN_B AND EF AND !C0;

AEF NOT  := !EFA AND EFB OR
             EFA AND !EFB OR
            !EFA AND !EFB;

EF NOT   := !EFA AND !EFB;

END;
END X2RENCNTLR.



{AUTHOR:       BHANU V. R. NANDURI
 COMPANY:      INTEGRATED DEVICE TECHNOLOGY
 DATE:         01/24/89
 }
 MODULE WENCNTLR;          { THIS PAL IS USED TO CONTROL THE
                             WRITE OPERATIONS IN A FOUR DEEP
                             X9 OR X8 FIFO EXPANSION SCHEME }
 TITLE WENCNTLR;
 TYPE MMI 20R8;

 INPUTS;

 {WCLK       NODE[PIN1];}  {WCLK INPUT}
 RS          NODE[PIN2];   {SYNCHRONOUS RESET INPUT}
 FFA         NODE[PIN3];
 FFB         NODE[PIN4];
 FFC         NODE[PIN5];
 FFD         NODE[PIN6];
 WEN         NODE[PIN7];
 C0          NODE[PIN22];
 C1          NODE[PIN21];
 WEN_A       NODE[PIN20];
 WEN_B       NODE[PIN19];
 WEN_C       NODE[PIN18];
 WEN_D       NODE[PIN17];
 FF          NODE[PIN15];

 OUTPUTS;

 WEN_A       NODE[PIN20];  {WEN1 TO FIFO A}
 WEN_B       NODE[PIN19];  {WEN1 TO FIFO B}
 WEN_C       NODE[PIN18];  {WEN1 TO FIFO C}
 WEN_D       NODE[PIN17];  {WEN1 TO FIFO D}
 AFF         NODE[PIN16];  {ALMOST FULL FLAG FOR THE EXPANSION}
 FF          NODE[PIN15];  {FULL FLAG FOR THE EXPANSION}
 C0          NODE[PIN22];  {C0 IS BIT 0 OF THE TWO BIT COUNTER}
 C1          NODE[PIN21];  {C1 IS BIT 1 OF THE TWO BIT COUNTER}
```

```
TERMS;

C0 NOT  :=  RS AND !WEN AND !WEN_A AND FF AND C0 OR
            RS AND !WEN AND !WEN_C AND FF AND C0 OR
            RS AND !WEN AND !WEN_B AND !FF AND !C0 OR
            RS AND !WEN AND !WEN_D AND !FF AND !C0 OR
            RS AND WEN AND !WEN_B AND !C0 OR
            RS AND WEN AND !WEN_D AND !C0 OR
            RS AND WEN AND WEN_A AND WEN_B AND WEN_C AND
            WEN_D AND !C0 OR
            RS AND !WEN AND WEN_A AND WEN_B AND WEN_C AND WEN_D AND !C0;

C1 NOT  :=  RS AND !WEN AND !WEN_B AND FF AND C1 OR
            RS AND !WEN AND !WEN_C AND FF AND !C1 OR
            RS AND !WEN AND !WEN_C AND !FF AND !C1 OR
            RS AND !WEN AND !WEN_D AND !FF AND !C1 OR
            RS AND WEN AND !WEN_C AND !C1 OR
            RS AND WEN AND !WEN_D AND !C1 OR
            RS AND WEN AND WEN_A AND WEN_B AND WEN_C AND
            WEN_D AND !C1 OR
            RS AND !WEN AND WEN_A AND WEN_B AND WEN_C AND WEN_D AND !C1;

WEN_A NOT := RS AND !WEN AND WEN_D AND WEN_C AND WEN_B AND WEN_A AND
             C0 AND C1 OR
             RS AND !WEN AND !WEN_D AND FF AND !C0 AND !C1 OR
             RS AND !WEN AND !WEN_A AND !FF AND C0 AND C1;

WEN_B NOT := RS AND !WEN AND WEN_D AND WEN_C AND WEN_B AND WEN_A AND
             !C0 AND C1 OR
             RS AND !WEN AND !WEN_A AND FF AND C0 AND C1 OR
             RS AND !WEN AND !WEN_B AND !FF AND !C0 AND C1;

WEN_C NOT := RS AND !WEN AND WEN_D AND WEN_C AND WEN_B AND WEN_A AND
             C0 AND !C1 OR
             RS AND !WEN AND !WEN_B AND FF AND !C0 AND C1 OR
             RS AND !WEN AND !WEN_C AND !FF AND C0 AND !C1;

WEN_D NOT := RS AND !WEN AND WEN_D AND WEN_C AND WEN_B AND WEN_A AND
             !C0 AND !C1 OR
             RS AND !WEN AND !WEN_C AND FF AND C0 AND !C1 OR
             RS AND !WEN AND !WEN_D AND !FF AND !C0 AND !C1;

AFF NOT   := !FFA AND FFB AND FFC AND FFD OR
             FFA AND !FFB AND FFC AND FFD OR
             FFA AND FFB AND !FFC AND FFD OR
             FFA AND FFB AND FFC AND !FFD OR
             !FFA AND !FFB AND !FFC AND !FFD;

FF NOT    := !FFA AND !FFB AND !FFC AND !FFD;
END;
END WENCNTLR.
```

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{AUTHOR:        BHANU V. R. NANDURI
 COMPANY:       INTEGRATED DEVICE TECHNOLOGY
 DATE:          01/24/89
 }
 MODULE RENCNTLR;           { THIS PAL IS USED TO CONTROL THE
                              READ OPERATIONS IN A FOUR DEEP
                              X9 OR X8 FIFO EXPANSION SCHEME }
 TITLE RENCNTLR;
 TYPE MMI 20R8;

 INPUTS;

 {WCLK        NODE[PIN1];} {RCLK INPUT}
 RS           NODE[PIN2];  {SYNCHRONOUS RESET INPUT}
 EFA          NODE[PIN3];
 EFB          NODE[PIN4];
 EFC          NODE[PIN5];
 EFD          NODE[PIN6];
 REN          NODE[PIN7];
 C0           NODE[PIN22];
 C1           NODE[PIN21];
 REN_A        NODE[PIN20];
 REN_B        NODE[PIN19];
 REN_C        NODE[PIN18];
 REN_D        NODE[PIN17];
 EF           NODE[PIN15];

 OUTPUTS;

 REN_A        NODE[PIN20]; {REN1 TO FIFO A}
 REN_B        NODE[PIN19]; {REN1 TO FIFO B}
 REN_C        NODE[PIN18]; {REN1 TO FIFO C}
 REN_D        NODE[PIN17]; {REN1 TO FIFO D}
 AEF          NODE[PIN16]; {ALMOST EMPTY FLAG FOR THE EXPANSION}
 EF           NODE[PIN15]; {EMPTY FLAG FOR THE EXPANSION}
 C0           NODE[PIN22]; {C0 IS BIT 0 OF THE TWO BIT COUNTER}
 C1           NODE[PIN21]; {C1 IS BIT 1 OF THE TWO BIT COUNTER}

 TERMS;

 C0 NOT  :=  RS AND !REN AND !REN_A AND EF AND C0 OR
             RS AND !REN AND !REN_C AND EF AND C0 OR
             RS AND !REN AND !REN_B AND !EF AND !C0 OR
             RS AND !REN AND !REN_D AND !EF AND !C0 OR
             RS AND REN AND !REN_B AND !C0 OR
             RS AND REN AND !REN_D AND !C0 OR
             RS AND REN AND REN_A AND REN_B AND REN_C AND
             REN_D AND !C0 OR
             RS AND !REN AND REN_A AND REN_B AND REN_C AND REN_D AND !C0;
```

```
C1 NOT  :=  RS AND !REN AND !REN_B AND EF AND C1 OR
            RS AND !REN AND !REN_C AND EF AND !C1 OR
            RS AND !REN AND !REN_C AND !EF AND !C1 OR
            RS AND !REN AND !REN_D AND !EF AND !C1 OR
            RS AND REN AND !REN_C AND !C1 OR
            RS AND REN AND !REN_D AND !C1 OR
            RS AND REN AND REN_A AND REN_B AND REN_C AND
            REN_D AND !C1 OR
            RS AND !REN AND REN_A AND REN_B AND REN_C AND REN_D AND !C1;

REN_A NOT := RS AND !REN AND REN_D AND REN_C AND REN_B AND REN_A AND
             C0 AND C1 OR
             RS AND !REN AND !REN_D AND EF AND !C0 AND !C1 OR
             RS AND !REN AND !REN_A AND !EF AND C0 AND C1;

REN_B NOT := RS AND !REN AND REN_D AND REN_C AND REN_B AND REN_A AND
             !C0 AND C1 OR
             RS AND !REN AND !REN_A AND EF AND C0 AND C1 OR
             RS AND !REN AND !REN_B AND !EF AND !C0 AND C1;

REN_C NOT := RS AND !REN AND REN_D AND REN_C AND REN_B AND REN_A AND
             C0 AND !C1 OR
             RS AND !REN AND !REN_B AND EF AND !C0 AND C1 OR
             RS AND !REN AND !REN_C AND !EF AND C0 AND !C1;

REN_D NOT := RS AND !REN AND REN_D AND REN_C AND REN_B AND REN_A AND
             !C0 AND !C1 OR
             RS AND !REN AND !REN_C AND EF AND C0 AND !C1 OR
             RS AND !REN AND !REN_D AND !EF AND !C0 AND !C1;

AEF NOT  := !EFA AND EFB AND EFC AND EFD OR
            EFA AND !EFB AND EFC AND EFD OR
            EFA AND EFB AND !EFC AND EFD OR
            EFA AND EFB AND EFC AND !EFD OR
            !EFA AND !EFB AND !EFC AND !EFD;

EF NOT   := !EFA AND !EFB AND !EFC AND !EFD;
END;
END RENCNTLR.
```

```
{AUTHOR:        BHANU V. R. NANDURI
 COMPANY:       INTEGRATED DEVICE TECHNOLOGY
 DATE:          01/24/89
 }
 MODULE OENCNTLR;          { THIS PAL IS USED TO CONTROL THE
                        READ OPERATIONS IN A FOUR DEEP
                        X9 OR X8 FIFO EXPANSION SCHEME }
 TITLE OENCNTLR;
 TYPE MMI 20R8;

 INPUTS;

 {RCLK        NODE[PIN1];} {RCLK INPUT}
 RS         NODE[PIN2];     {SYNCHRONOUS RESET INPUT}
 EF    NODE[PIN3];
 GOEN         NODE[PIN4];
 REN_A        NODE[PIN5];
 REN_B        NODE[PIN6];
 REN_C        NODE[PIN7];
 REN_D          NODE[PIN8];
 REN            NODE[PIN9];
 C0    NODE[PIN22];
 C1    NODE[PIN21];
 OEN_A          NODE[PIN20];
 OEN_B          NODE[PIN19];
 OEN_C          NODE[PIN18];
 OEN_D          NODE[PIN17];

 OUTPUTS;

 C0    NODE[PIN22]; {C0 IS BIT 0 OF THE TWO BIT COUNTER}
 C1    NODE[PIN21]; {C1 IS BIT 1 OF THE TWO BIT COUNTER}
 OEN_A          NODE[PIN20];      {OE TO FIFO A}
 OEN_B          NODE[PIN19];      {OE TO FIFO B}
 OEN_C          NODE[PIN18];      {OE TO FIFO C}
 OEN_D          NODE[PIN17];      {OE TO FIFO D}

 TERMS;

 C0 NOT  :=  RS AND !REN AND !REN_A AND EF AND C0 OR
       RS AND !REN AND !REN_C AND EF AND C0 OR
       RS AND !REN AND !REN_B AND !EF AND !C0 OR
       RS AND !REN AND !REN_D AND !EF AND !C0 OR
       RS AND REN AND !REN_B AND !C0 OR
       RS AND REN AND !REN_D AND !C0 OR
       RS AND REN AND REN_A AND REN_B AND REN_C AND
       REN_D AND !C0 OR
       RS AND !REN AND REN_A AND REN_B AND REN_C AND REN_D AND !C0;

 C1 NOT  :=  RS AND !REN AND !REN_B AND EF AND C1 OR
       RS AND !REN AND !REN_C AND EF AND !C1 OR
       RS AND !REN AND !REN_C AND !EF AND !C1 OR
       RS AND !REN AND !REN_D AND !EF AND !C1 OR
       RS AND REN AND !REN_C AND !C1 OR
       RS AND REN AND !REN_D AND !C1 OR
       RS AND REN AND REN_A AND REN_B AND REN_C AND
       REN_D AND !C1 OR
       RS AND !REN AND REN_A AND REN_B AND REN_C AND REN_D AND !C1;
```

```
OEN_A NOT := RS AND !GOEN AND !OEN_A AND REN_D AND REN_C AND REN_B AND REN_A AND
        C0 AND C1 OR
        RS AND !GOEN AND !OEN_D AND !REN_A AND EF AND C0 AND C1 OR
        RS AND !GOEN AND !OEN_D AND !EF AND C0 AND C1 OR
        RS AND !GOEN AND !OEN_A AND !EF AND C0 AND C1 OR
        RS AND !GOEN AND OEN_D AND OEN_C AND OEN_B AND OEN_A AND
        !REN_A AND EF AND C0 AND C1;

OEN_B NOT := RS AND !GOEN AND !OEN_B AND REN_D AND REN_C AND REN_B AND REN_A AND
            !C0 AND C1 OR
        RS AND !GOEN AND !OEN_A AND !REN_B AND EF AND !C0 AND C1 OR
        RS AND !GOEN AND !OEN_A AND !EF AND !C0 AND C1 OR
        RS AND !GOEN AND !OEN_B AND !EF AND !C0 AND C1 OR
        RS AND !GOEN AND OEN_D AND OEN_C AND OEN_B AND OEN_A AND
        !REN_B AND EF AND !C0 AND C1;

OEN_C NOT := RS AND !GOEN AND !OEN_C AND REN_D AND REN_C AND REN_B AND REN_A AND
        C0 AND !C1 OR
        RS AND !GOEN AND !OEN_B AND !REN_C AND EF AND C0 AND !C1 OR
        RS AND !GOEN AND !OEN_B AND !EF AND C0 AND !C1 OR
        RS AND !GOEN AND !OEN_C AND !EF AND C0 AND !C1 OR
        RS AND !GOEN AND OEN_D AND OEN_C AND OEN_B AND OEN_A AND
        !REN_C AND EF AND C0 AND !C1;

OEN_D NOT := RS AND !GOEN AND !OEN_D AND REN_D AND REN_C AND REN_B AND REN_A AND
        !C0 AND !C1 OR
        RS AND !GOEN AND !OEN_C AND !REN_D AND EF AND !C0 AND !C1 OR
        RS AND !GOEN AND !OEN_C AND !EF AND !C0 AND !C1 OR
        RS AND !GOEN AND !OEN_D AND !EF AND !C0 AND !C1 OR
        RS AND !GOEN AND OEN_D AND OEN_C AND OEN_B AND OEN_A AND
        !REN_D AND EF AND !C0 AND !C1;

END;
END OENCNTLR.
```

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Integrated Device Technology, Inc.

SIMPLIFY SCSI HOST ADAPTER DESIGN WITH BIDIRECTIONAL FIFO MEMORIES

APPLICATION NOTE AN-71

by Julie S. Lin

ABSTRACT

With the dramatic change of the processing power in the microprocessor world, the bottleneck of the system performance is shifted to the I/O subsystem. An efficient I/O interface should transfer data in a high-speed burst, such that the CPU can optimize the performance by accessing the system bus without much interruption. The SCSI adapter presented in this paper achieves this goal with a low chip-count hardware design. A pair of monolithic bidirectional FIFOs are used to buffer transferred data between the host bus and the SCSI protocol controller.

INTRODUCTION

A SCSI host adapter links the system bus and the SCSI bus. The adapter board requires a SCSI protocol controller to monitor all of the SCSI bus activities. The host adapters can be categorized into three architectures, depending on how the data is moved from the SCSI bus to the host memory: CPU assisted, DMA slave, and bus master. The CPU assisted architecture is easy to design and requires low chip counts. Its traditional implementation for the single-task system is considered a cost-sensitive low performance approach. By reducing software overhead and speeding up the system bus interface, the performance of this architecture can be highly improved, while the design simplicity is still preserved. The on-chip state machines of some SCSI protocol controllers perform SCSI sequences automatically, thereby reducing software overhead. To speed up the interface between a 32-bit system bus (which is a growing trend) and an 8-bit SCSI controller, a monolithic bidirectional FIFO chip (BiFIFO) provides an integrated solution.

In some general computing systems the system bus arbitration scheme is widely used either for DMA channel or for bus-master I/O subsystems. But for some system designs requiring high I/O throughput rate, this complicated scheme may not be necessary for the I/O interface. The CPU-assisted SCSI design proposed in this paper can eliminate the complexity of host bus arbitration and achieve high data throughput by using the system CPU.

This SCSI adapter design is for a 32-bit RISC system bus with the NCR53C90A as the protocol controller. With 5 Mbytes/sec data rate on the SCSI bus and much faster speed on the system bus, the IDT7252 BiFIFO (35ns access time) provides data buffering in both directions. Two cascaded 18-to-9 BiFIFOs achieve 36-to-9 bus conversion with a 4K-byte deep FIFO in each direction. Besides, the on-chip DMA handshaking logic fits directly into the MPU interface side of the SCSI controller. Little control logic is required in this design, allowing it to be put on the system board as a SCSI port. Since the programmable flags of the BiFIFO are available in the status register and external flag pins, the CPU can regulate the data transfer process by software polling for single-task applications, or by hardware interrupt to allow background tasks to continue executing.

SCHEMATIC AND HOST BUS

The system board used to explain this design concept contains a R3000 CPU, cache memory, SRAM main memory, EPROM monitor, two serial ports, and a parallel port. A 32-bit address bus, a 32-bit data bus and all necessary control signals are available on the proprietary host bus for expansion. This bus is chosen because it's simple and very easy to understand.

The simplified schematic of this SCSI adapter is illustrated in Figure 1. The BiFIFO architecture will be introduced in the next section. Hardware considerations are explained in Sections 4 and 5, which include an address decoding scheme, signal connections and timing issues. This paper also presents software algorithms for data transfers in Section 6.

For the explanations of signal connections, the host bus signals are summarized as follows:

- EA00-EA31 are the address output pins.
- ED00-ED31 are the data I/O pins.
- SYSOUT is the main system clock output used for synchronizing data transfers.
- $\overline{\text{MRES}}$ is the active-low reset output.
- $\overline{\text{MREQ}}$ and $\overline{\text{XACK}}$ are handshake signals for timing external data transfers.
- $\overline{\text{UINT}}$ is the user interrupt input to the R3000.
- $\overline{\text{WEN}}$ is the write enable outputs.
- $\overline{\text{MEMRD}}$ is an active-low memory-read output signal, normally used to enable output drivers in the expansion system for data read operations.
- $\overline{\text{UCS1A}}$ is a decoded User Chip Select output.

All data transfers between the system board and the user expansion board are controlled by the handshake signals, $\overline{\text{MREQ}}$ and $\overline{\text{XACK}}$. $\overline{\text{MREQ}}$ indicates the beginning of a memory request cycle. The detection of an external memory transfer must be qualified by the address present at the time of the $\overline{\text{MREQ}}$ signal. $\overline{\text{XACK}}$ is used to indicate that the data transfer initiated by the $\overline{\text{MREQ}}$ signal has been completed.

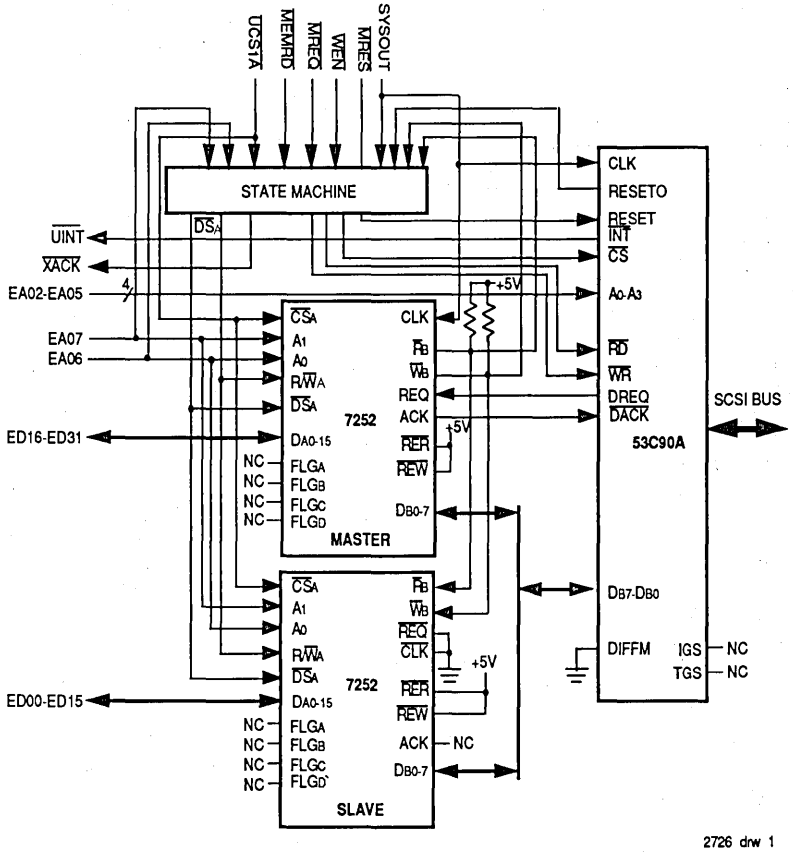

Figure 1. Simplified Schematic of the SCSI Adapter

THE BIDIRECTIONAL FIFO ARCHITECTURE

The 7252 BiFIFO is a compact, highly integrated solution to simplify data transfers between two processors or a processor and a peripheral of different bus bandwidth. A stand-alone BiFIFO can handle the data transfer from an 18-bit bus to a 9-bit bus. Two cascaded devices can transfer data from a 36-bit bus to a 9-bit bus or an 18-bit bus. It contains one 1K by 18-bit FIFO in each direction. The 7252 also includes a data path that bypasses both FIFOs. With this direct data path, a processor can initialize a peripheral before they transfer data via FIFOs. The detailed block diagram is illustrated in Figure 2.

Besides FIFO data transfers, the 18-bit Port A is also used for BiFIFO initialization and command controls. By controlling address lines A0-1 and chip select $\overline{CS}_A$, users can access six resources: the A-to-B FIFO, the B-to-A FIFO, the 9-bit direct data bus, the status, command and configuration registers. The Motorola-type CPU interface with data strobe ($\overline{DS}_A$) is provided on Port A.

By writing commands to Port A, users can do many function controls which include resetting FIFOs and/or handshake circuitry, setting DMA transfer direction, selecting one of two status register formats, increasing the read or write pointer of Port B, and clearing parity error bits. The status register reflects the current status of internal operations such as FIFO flags and parity errors. It also duplicates the contents of the odd-byte register and indicates if an even number of bytes has been written into Port B (valid bit).

Each FIFO is equipped with four internal flags: Empty, Almost Empty, Full, and Almost Full. The offset values of the Almost Empty and Almost Full flags are programmable through Configuration Registers 0-3. The four external flag pins are used to reflect internal flag status with selectable signal polarities. The selection for external flags is provided by programming Register 4. Register 5 is used for general control: selecting Intel-type or Motorola-type interface for Port B, choosing byte order of an 18-bit word, enabling reread/rewrite functions, defining handshake signal polarities and timings,

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and also determining interface and expansion modes. Parity functions are set by Register 7. Register 6 is reserved for future expansion.

The BiFIFO supports two parity modes at Port B: Check and Generate. In the check mode, the parity check circuitry monitors data passed through Port B and sets parity error bits accordingly. An error while transferring data into Port B sets the write parity error bit in the Status. An error while transferring data out of Port B sets the read parity error bit in the Status. The OR of these two error bits is available as an option for output on the FLAGA pin. In the generate mode the generated parity bit is placed on the Port B data bus for a data-out operation. The generated parity bit is either stored in the B-to-A FIFO or bypassed to Port A for a data-in operation.

The DMA interface is associated with Port B. REQ and ACK provide a standard DMA handshake. For the 18-bit to 9-bit bus interface, the handshake circuitry generates read and write strobes ($\overline{R}_B$ and $\overline{W}_B$) at Port B of a stand-alone BiFIFO. When cascading two BiFIFOs for the 36-bit to 9-bit bus interface, one device is the master and the other one is the slave. The handshake circuitry generates read and write strobes on the master device. These strobes become inputs on the slave device.

The BiFIFO has an innovative hardware Reread and Rewrite capability on Port B side. But, Reread and Rewrite functions are also programmable from Port A, where reread and rewrite locations are set through the command register.

The 18-bit to 9-bit BiFIFO comes in two versions. Load Reread, Load Rewrite, and Reset are accessible through Port A commands on the 7252 48-pin DIP. These functions are available either through Port A commands or directly through Port B pins on the 72520 52-pin PLCC.

ADDRESS DECODING AND SIGNALCONNECTIONS

The user chip select $\overline{UCS1A}$ from the expansion connectors is chosen for high address bit decoding. The addresses used in the SCSI adapter are all uncached and unmapped, insuring that the block read operation will never occur. The address bits A_0-A_3 of the SCSI controller are connected to EA02-EA05, and the address bits A_0, A_1 of the BiFIFOs to EA06-EA07.

Since the partial-word manipulations are not implemented for the SCSI adapter addresses, the address pins EA00 and EA01 are not used. Chip Select $\overline{CS}_A$ of the 7252s is connected to the decoded signal $\overline{UCS1A}$. But Chip Select $\overline{CS}$ of the 53C90A is from the PAL 16L8, where $\overline{UCS1A}$ is qualified with EA07, EA06, $\overline{MEMRD}$, and $\overline{WEN}$ for the bypass operation.

Since the BiFIFOs provide a bypass path for the system bus to directly access the 53C90A registers, Port A of the BiFIFOs should be chip-selected together with the 53C90A. The 53C90A should not be chip-selected when we are accessing the BiFIFO internal resources. In such an arrangement, the 53C90A will not be interfered with during the BiFIFOs' internal operations. Since Port B and Port A operations are totally independent, we can poll the status from the Port A side while Port B and the SCSI controller are engaged in the data movement via DMA handshaking.

Besides address decoding, the Motorola type interface with $R/\overline{W}_A$ (read, write control) and $\overline{DS}_A$ (data strobe) controls the read/write operations on Port A. To fulfill the setup and hold time requirements between $R/\overline{W}_A$ and $\overline{DS}_A$, $R/\overline{W}_A$ is connected to the inverted signal of the memory read control $\overline{MEMRD}$. To optimize the performance, the assertion of the data strobe $\overline{DS}_A$ varies for four cases : writing/reading Port A and writing/reading 53C90A registers.

The clock used to control the handshake signals of the 7252s comes directly from SYSOUT of the system board. The same clock is used throughout the SCSI adapter board for clocking the 53C90A and the PAL 22V10. The 10K pull-up resistors are used for $\overline{R}_B$ and $\overline{W}_B$ to keep signals high during the initialization. The default operation mode of the BiFIFO requires that. The handshake signals are all generated or responded to by the master device of the BiFIFOs. But $\overline{R}_B$ and $\overline{W}_B$ should be fed into the slave device to synchronize the byte data transfer. The reread/rewrite functions are not used in this application, therefore $\overline{RER}$ and $\overline{REW}$ are tied high. REQ and CLK of the slave device are grounded for noise immunity.

To simplify the interrupt logic design, the only interrupt coming out of this SCSI board is from the 53C90A, whereas the FIFO flags of BiFIFOs are polled from the Status Register. The read/write signals $\overline{RD}$, $\overline{WR}$ of the 53C90A are from the PAL 22V10. They are derived from $\overline{R}_B$ and $\overline{W}_B$ to fit in both DMA timing and the bypass timing. The reset from the system board $\overline{MRES}$ will reset the SCSI controller and the PAL 22V10.

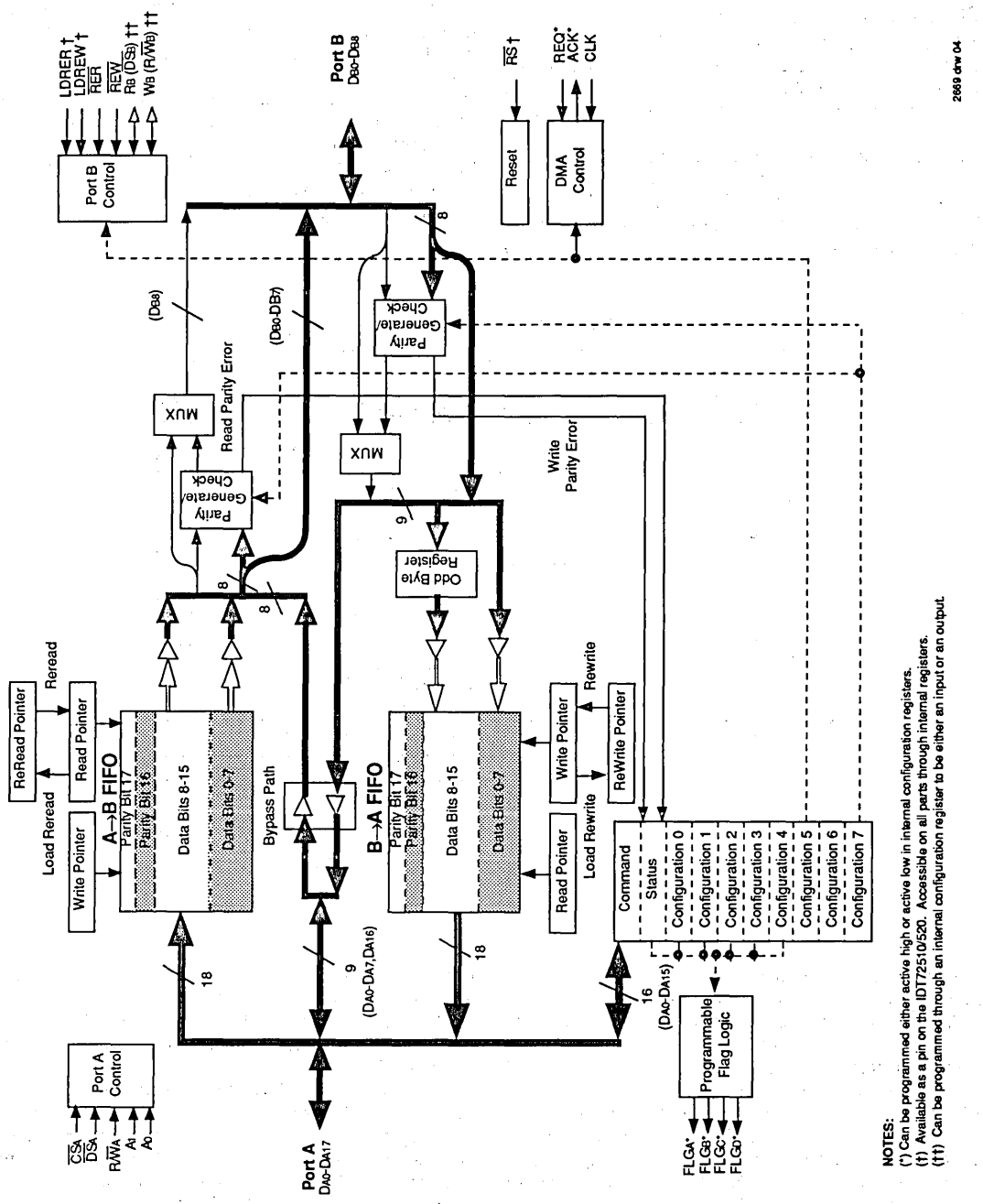

Figure 2. The BiFIFO Architecture

TIMING CONSIDERATIONS

In timing considerations, the SCSI adapter involves four different kinds of interface: (i) the interface of the system board to access Port A (ii) the interface of the system board to access the 53C90A registers (iii) data transfer via DMA handshaking between Port B and the 53C90A (iv) the interface between the 53C90A and the SCSI bus. With on-chip 48mA drivers and receivers, the connection between the 53C90A and the single-ended SCSI bus is straight forward.

All the timing diagrams from Figure 3 to Figure 8 are based on a 25MHz clock. The timing of writing Port A is in Figure 3. The assertion of $\overline{MREQ}$ with a qualified address starts this writing sequence, which lasts for six cycles. Since data out from the system board will be available on the Port A bus at the third clock cycle, the rising edge of $\overline{DS_A}$ is put on the fifth clock cycle to write data into the BiFIFOs. The assertion of $\overline{XACK}$ causes the Port A bus to be tri-stated four clocks later, which concludes the whole writing sequence. The state machine 22V10, which provides $\overline{XACK}$ and $\overline{DS_A}$, goes through the transitions as State 0 (default state), State 1, State 2, State 3, and back to State 0 again.

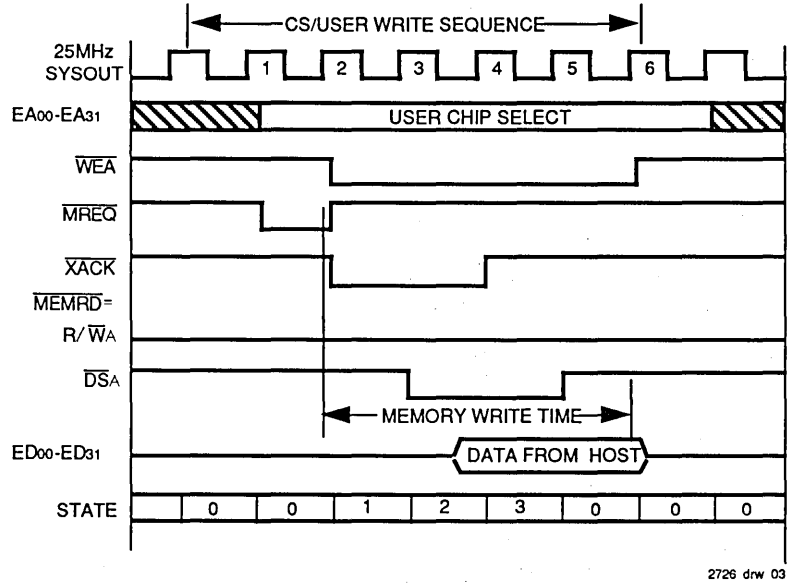

Figure 3. Timing: Writing Port A of the 7252

Figure 4 depicts the timing of reading Port A. Since the system bus fetches data three cycles behind the assertion of $\overline{XACK}$, $\overline{DS_A}$ should be asserted two cycles ahead of data fetching to guarantee valid data appearing on the Port A bus. The transition of the state machine is State 0, State 4, State 5, State 6, State 7, and back to State 0.

When writing a register of the 53C90A, the state machine generates a write control signal $\overline{WRREG}$ internally, which is multiplexed with $\overline{W_B}$ (as for the DMA handshaking) to provide the write control $\overline{WR90}$ for the 53C90A. As shown in Figure 5, once the bypass mode of the BiFIFO is decoded, the assertion of $\overline{DS_A}$ will cause Port A data to appear on the Port B bus. The delayed version of the $\overline{DS_A}$ signal will appear on $\overline{W_B}$. The assertion of $\overline{XACK}$ terminates Port A data four clocks later, whereas the deassertion of $\overline{DS_A}$ terminates Port B data within one clock cycle. The best time for the 53C90A to fetch data from the Port B bus should be on the rising edge of the 5th clock. The state machine transitions for this 6-cycle writing sequence covers: State 0, State 8, State 9, State 10, State 11 and State 0.

Figure 6 shows the timing for the reading of a register from the 53C90A. The read register control $\overline{REREG}$ generated internally by the state machine is used to read out a register value from the 53C90A. Just like $\overline{WRREG}$, $\overline{RDREG}$ is multiplexed with $\overline{R_B}$ (as for the DMA handshaking) to provide the read control for the 53C90A MPU interface. The assertion of $\overline{DS_A}$ and $\overline{RDREG}$ right behind the address decoding cycle, ensures the data from the 53C90A to appear on the Port A bus as fast as it can. The assertion of $\overline{XACK}$ at the 2nd clock cycle positions the data fetching of the system bus at the 5th cycle.

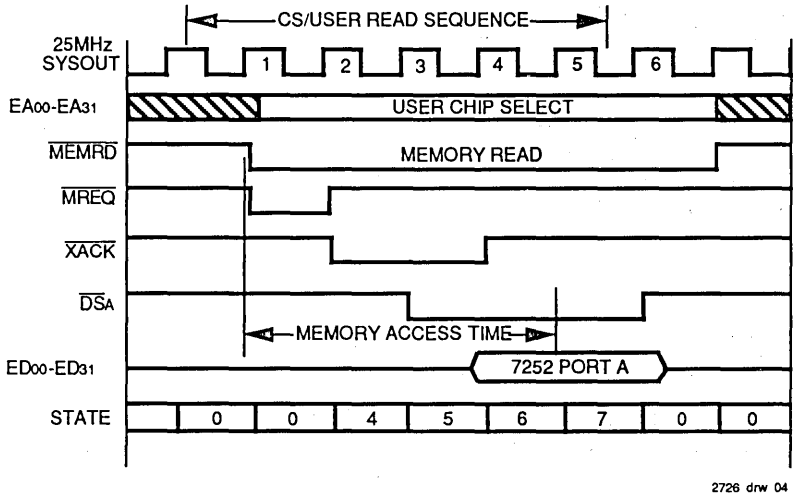

Figure 4. Timing: Reading Port A of the 7252

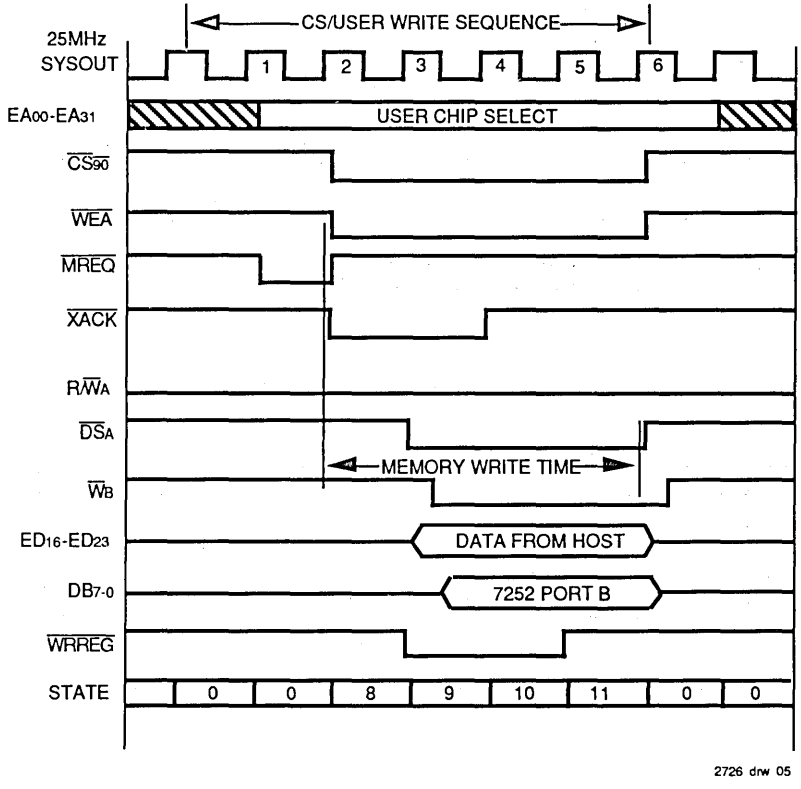

Figure 5. Timing: Writing a Register of the 53C90A

The state machine transitions go through the sequence: State 0, State 12, State 13, State 14, State 15, and State 0. The state transition diagram is drawn in Figure 9 which summarizes these four sequences.

The DMA handshake timings between the 7252s and the 53C90A are shown in Figure 7 and Figure 8. DREQ from the 53C90A is responded to by the master BiFIFO with the assertion of $\overline{DACK}$ together with $\overline{WB}$ or $\overline{RB}$. The number of clock cycles between the detection of DREQ and the assertion of $\overline{DACK}$ can be programmed as 2 to 5 cycles through Configuration Register 5. $\overline{WB}$ or $\overline{RB}$ always follows the assertion of $\overline{DACK}$, lasts for 1 or 2 cycles (programmable through Configuration Register 5), and is deasserted together with $\overline{DACK}$. Whenever $\overline{DACK}$ goes back to a high state, the 53C90A may start another handshake cycle by asserting request signal DREQ again. For the case where the peripheral controller timing is much slower than the clock rate, the BiFIFO allows the user to slow down the clock by dividing the external clock by two (also programmable through Configuration Register 5).

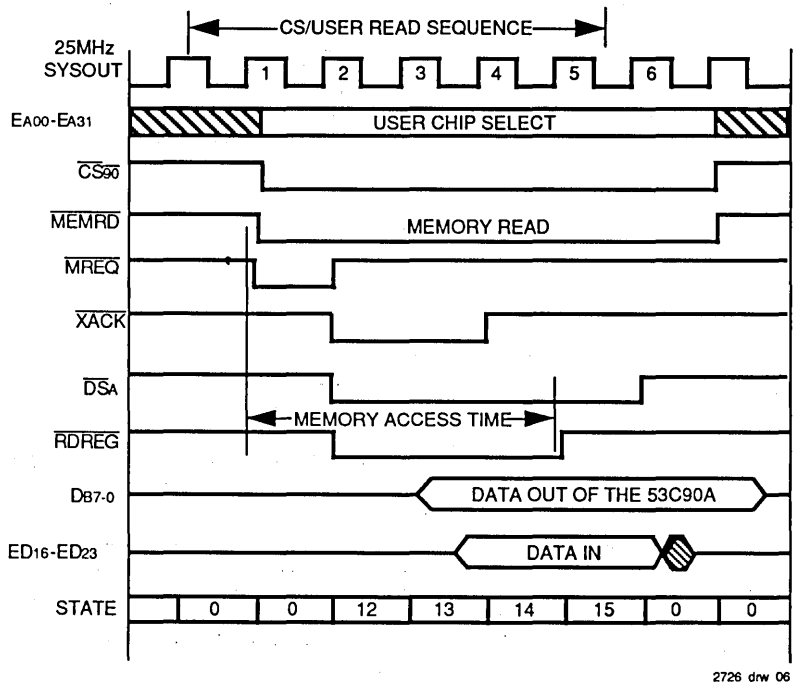

Figure 6. Timing: Reading a Register of the 53C90A

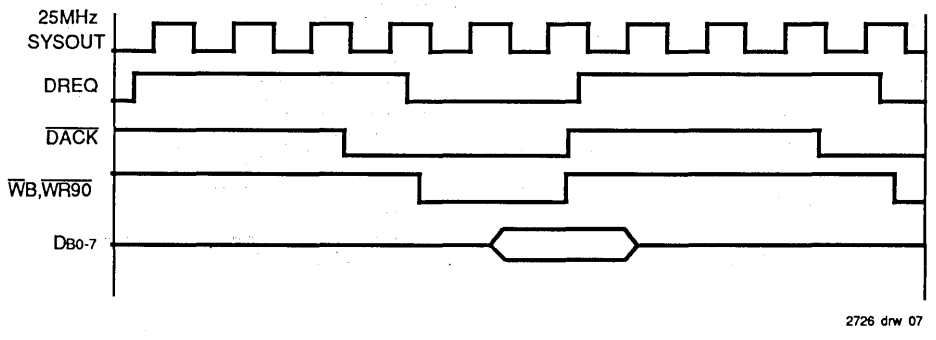

Figure 7. Timing: DMA Write Between the 7252 and the 53C90A

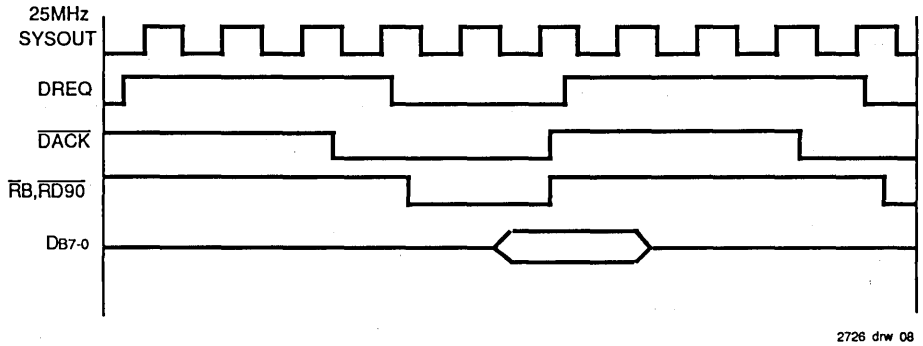

Figure 8. Timing: DMA Read Between the 7252 and the 53C90A

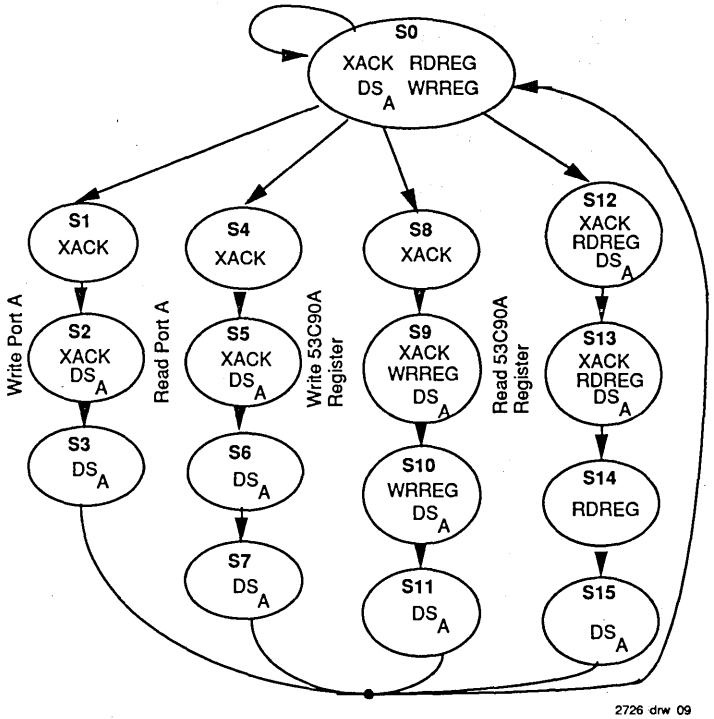

Figure 9. State Transition Diagram of the SCSI Adapter

SOFTWARE ALGORITHMS FOR DATA TRANSFERS

The SCSI bus protocol can be divided into the following phases: Bus Free, Arbitration, Selection, Reselection, Command, Data In, Data Out, Status, Message In, and Message Out. Command, Status, and Message phases all belong to small-block data transfers. Data In and Data Out phases will involve large-block data transfer.

Small-Block Data Transfers

Let's assume the SCSI adapter is the single initiator in a SCSI bus. To initiate a SCSI action, the CPU has to program several registers of the 53C90A. Afterwards, the 16-byte FIFO of the 53C90A should be filled with a Command Description Block (CDB). The CPU can then issue a command to the 53C90A to start the sequence, which includes Arbitration, Selection, and Command phases. In this process, the CPU monitors all the activities directly on the 53C90A, and bypasses the BiFIFOs. If the target asserts Status phase, the CPU should bring in the Status and Message bytes. As with the previous process, the SCSI adapter handles these phases bypassing the BiFIFOs.

Large-Block Data Transfers

Both Data In and Data Out phases require data buffering between the SCSI controller and the system bus. The SCSI driver should regulate the data flow from the system bus to Port A by monitoring A-to-B FIFO flags.

Figure 10 shows pseudo codes for the SCSI driver during the Data Out phase. The total number of bytes to be transferred is defined by data_size . Since the size of A-to-B FIFOs (including master and slave devices) is 4K bytes, we need to divide the data into 4K-byte blocks. The residual block has to be handled differently. The driver always transfers data in a 32-bit full word; however the last byte may not hit the word boundary. The driver will put dummy bytes for the last word and send it to the A-to-B FIFOs. But the 53C90A can only take the amount specified in data_size. The driver can distinguish the cases with 0,1,2, or 3 bytes left behind the last full word and respond accordingly.

The BiFIFO initializations for Data Out phase include "Reset A-to-B FIFO", "Set A-to-B DMA direction", and "Program A-to-B Almost Empty Flag (AEF) offset value". The AEF offset value should be set according to the data transfer rate difference between Port A and Port B. The driver transfers data by polling the Status Register of the BiFIFOs, and sending 4K-byte blocks of data when the BiFIFOs are almost empty. Once the number of words in the A-to-B FIFO is decreased to the offset value again, the driver sends out the next block. This procedure is repeated until all the 4K-byte blocks are sent out.

To deal with the residual block, we have to re-program the AEF offset value to 1, and send the remaining data with the last word possibly containing some dummy bytes. If the last word is a whole word, the transfer is done when both A-to-B FIFOs are empty. If the last word contains only one useful byte, the transfer is done when there are three dummy bytes left in A-to-B FIFOs — one in the slave device, two in the master device. This condition can be detected by the driver when the slave device stays in the Almost Empty state for several cycles. For the two-byte case, the transfer is done when the A-to-B FIFO of the slave device is empty. If there are three useful bytes contained in the last word, the transfer is done when the driver senses the following condition existed for several cycles: the slave device is empty and the master device is almost empty.

```
dataout_phase(data_size)
{
   no_of_4Kblks = data_size / 4096;
   residual = data_size mod 4096;
   no_of_words = residual /4;
   no_of_bytes = residual mod 4;

   Issue "Reset A-to-B FIFO" command to 7252s;
   Issue "Set A-to-B DMA direction" to 7252s;
   Program AEF offset value of A-to-B FIFOs;

   Load count registers of the 53C90A;
   Issue flush command to flush the FIFO of
   the 53C90A;
   Issue DMA transfer command to the 53C90A;

   Loop 1 to no_of_4Kblks
   {
      While (Master 7252 is almost empty)
      {
            Write 1K words into Port A;
      }
   }
   Program AEF offset value of A-to-B FIFOs
   to "1";
   Write no_of_words words into Port A;

   Switch (no_of_bytes)
   {
      case 0:
            While (both 7252s are empty);
            Done;
      case 1:
            Loop several times
            {
                  While (Slave is almost empty);
            }
            Done;
      case 2:
            While (Slave 7252 is empty);
            Done;
      case 3:
            Loop several times
            {
                  While (Slave 7252 is empty and
                  Master is almost empty);
            }
            Done;
   }
}
```

Figure 10. SCSI Driver Pseudo Code for the Data Out Phase

For the Data In phase, the driver knows the size of the data returned from the command type and the allocation length. The procedures that a driver takes for a Data In phase is explained with the pseudo codes in Figure 11. As in the Data Out phase, we divide the whole data size into several 4K-byte blocks and a residual block. The BiFIFO initializations include "Reset B-to-A FIFO", "Set B-to-A DMA direction", and "Program B-to-A Almost Full Flag (AFF) offset value". The driver polls the Status Registers of the BiFIFOs until it sees AFF being asserted on the master BiFIFO. At this time, the driver starts transferring 1K words from Port A to the destination buffer. This procedure is repeated until all the 4K-byte blocks are read in.

To handle the residual block, the AEF of the B-to-A FIFOs is set to no_of_words, which is the number of the full word. When AEF of the master BiFIFO is not set, the driver can take no_of_words words out from Port A. The last partial word is handled as follows: (i) If there is one byte left, this byte is in the Odd-byte register of the slave device, which can be read out through the Status Register. (ii) If there are two bytes left, the driver should read B-to-A FIFOs again to get these bytes from the slave device. (iii) For the three-byte case, the first two bytes stay in the B-to-A FIFO of the slave device, the last byte should be fetched from the Status Register of the master device.

DISCUSSIONS

SCSI is recognized as an excellent approach to interconnecting small computers and intelligent peripherals. The booming SCSI market dramatically increases available SCSI peripherals. A SCSI port is becoming a must for mid-range to high-performance computers and workstations. Traditional SCSI adapter designs occupy a backplane slot. This paper introduced a new design example with the IDT7252 BiFIFO, which may allow the whole SCSI interface to be put on the system board. With 2K-byte FIFOs in each direction, integrated bus-conversion, and DMA handshaking logic all in one part, the BiFIFO greatly simplifies the SCSI adapter design and increases the system throughput. Only five parts are used in this design — two BiFIFOs, one SCSI controller, and two PALs.

This design example allows only one interrupt to the system board from the SCSI controller. During the Data In and Data Out phases, the system processor has to poll FIFO flags in order to regulate the data loading/unloading rate. If the system requirements need to free the processor for the multitask application, the FIFO flag pins can be used to generate hardware interrupts. Additionally, the programmable offset of the Almost Empty/Full flags allows this design to fit into different systems without the cost that is associated with changing the buffer size.

```
datain_phase(data_size)
{
        no_of_4Kblks = data_size / 4096;
        residual = data_size mod 4096;
        no_of_words = residual /4;
        no_of_bytes = residual mod 4;

        Issue "Reset B-to-A FIFO" command to 7252s;
        Issue "Set B-to-A DMA direction" to 7252s;
        Program AFF offset value of B-to-A FIFOs;

        Load count registers of the 53C90A;
        Issue flush command to flush the FIFO of
        the 53C90A;
        Issue DMA transfer command to the 53C90A;

        Loop 1 to no_of_4Kblks
        {
                While (Master 7252 is almost full)
                        {
                        Read 1K words from Port A;
                        }
        }

        Set AEF offset value of the B-to-A FIFOs
        = no_of_words;

        While (Master 7252 is not almost empty)
           {
           Read no_of_words words from Port A;
           }

        Switch (no_of_bytes)
        {
           case 0:
                Done;
           case 1:
                Read the last byte from the Status
                Register of the Slave device;
                Done;
           case 2:
                Read B-to-A FIFOs once to get the last
                two bytes from the Slave;
                Done;
           case 3:
                Read B-to-A FIFOs once to get the
                first two bytes from the Slave;
                Read the last byte from the Status
                Register of the Master;
                Done;
        }
}
```

Figure 11. SCSI Driver Pseudo Code for the Data In Phase

Integrated Device Technology, Inc.

UNDERSTANDING THE OUTPUT CONTROL $\overline{OE}$ OF THE FLAGGED FIFOs: IDT72021/31/41

APPLICATION NOTE AN-73

by Danh Le Ngoc

The IDT72021/31/41 are high-speed, low-power, dual-port memory devices known as FLAGGED FIFOs. The FLAGGED FIFOs offer the basic features of IDT's industry standard FIFOs (IDT7201/02/03/04) while providing two new flags and the output control ($\overline{OE}$). The focus of this tech note is to describe how the output control ($\overline{OE}$) works. Figure 1 is a simplified block diagram of the Flagged FIFOs: IDT72021/31/41.

As Figure 1 shows, the three-state output buffer is controlled by the internal read signal and the external output control ($\overline{OE}$). A read cycle is initiated on the falling edge of the Read Enable signal ($\overline{R}$) provided the Empty flag ($\overline{EF}$) is not set. After the access time (T_A), data appears on the Q_{0-8} lines when the output control $\overline{OE}$ is low. While the read signal ($\overline{R}$) is low, the same data can be read repeatedly on the Q_{0-8} lines under control of the output control signal ($\overline{OE}$). This advantage enables the reading of the same FIFO location without advancing the internal read pointer. After Read Enable ($\overline{R}$) goes high, the data outputs (Q_{0-8}) will return to a high impedance condition independent of the output control ($\overline{OE}$).

Table 1 illustrates the state of the Q_{0-8} lines dependent on the empty flag, read control ($\overline{R}$) and the output control.

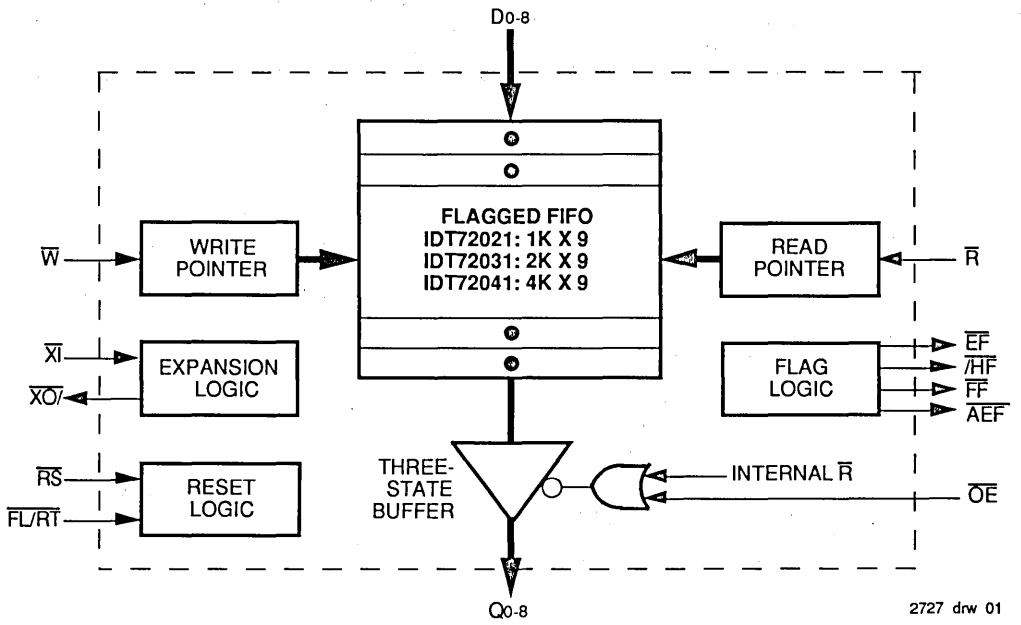

Figure 1. Simplified Block Diagram for Flagged FIFOs

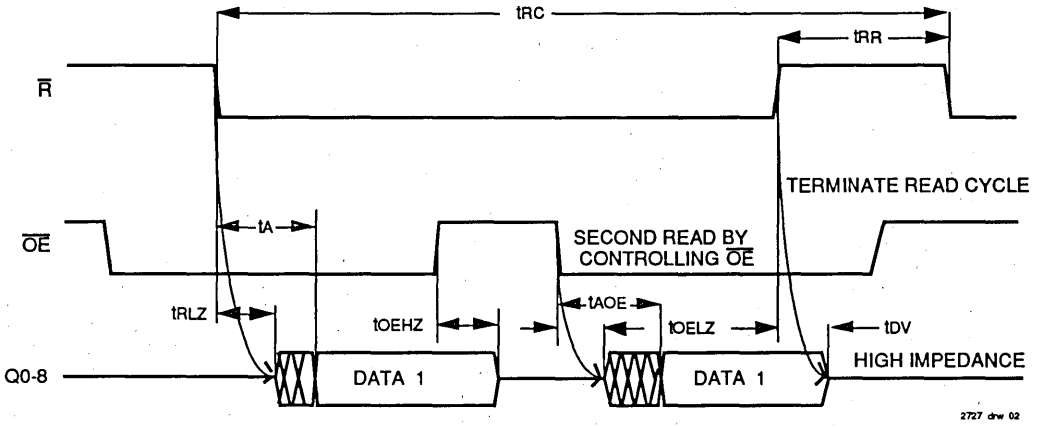

Figure 2. Read Cycle Controlled by $\overline{OE}$ and $\overline{R}$

$\overline{EF}$	$\overline{R}$	$\overline{OE}$	Q0-8
0	X	X	HIGH IMPEDANCE
1	0	0	NEW Q0-8
1	0	1	HIGH IMPEDANCE
1	1	0	HIGH IMPEDANCE
1	1	1	HIGH IMPEDANCE

2727 tbl 01

Table 1. Read Truth Table

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Integrated Device Technology, Inc.

DESIGNING WITH FIFOs

TECHNICAL NOTE TN-06

by Suneel Rajpal and Frank Schapfel

FIFOs are First-In/First-Out buffers that act as elastic buffers between two synchronous or asynchronous systems. The IDT7201 (512 x 9), IDT7202 (1K x 9), IDT7203 (2K x 9) and IDT7204 (4K x 9) are high-speed FIFOs that can operate at frequencies greater than 20MHz. Here are a few tips on designing with these FIFOs.

A generic block diagram of the FIFOs is shown in Figure 1. After power up, the FIFO must be reset. The reset operation requires that the read and write lines be high for a time t_{RPW} or t_{WPW} (the read or write pulse width minimums) before the rising edge of $\overline{RS}$, and to be high for a time t_{RSR} after the rising edge of $\overline{RS}$. These operating conditions are shown in Figure 2. It is important to observe the stipulated requirements on $\overline{R}$ and $\overline{W}$ during reset because they increment the read and write pointers and both edges of the read and write also affect the empty and full counters. The Full and Empty Flag counters have to be appropriately set after a reset operation.

The read and write pointers are high-speed counters that are incremented on every rising edge of read and write lines. These lines must be noise-free as in other high-speed counters like F161s and AS161s. This poses a common interface issue that users often encounter. False clocks can be caused by transmission line effects or crosstalk. Some of the symptoms of false clocking are flags asserted when they should not be, missing data or scrambled data order.

The Read or Write signals may be generated by a part that is physically placed far away from the FIFO on a PC board. This implies a propagation delay to and from the driver to the receiver that is greater than the rise and fall time of the driver. This causes reflections on the line. Also the driver that has a low impedance on the high-to-low transition causes an impedance mismatch. The mismatch is apparent with an F-type device or a Schottky-TTL device as their high-to-low impedance is fairly small (typically under 15 Ohms for F-type or FCT and under 10 Ohms for Schottky-TTL). This translates to a signal that eventually settles near zero volts but, in the interim, has a "damping" effect; it may go through a -2.0 volt to +1.5 volt to -1.0 volt to +.7 volt to zero volts. This is shown in Figure 3. The FIFO devices can handle a negative voltage level of 1.5V for less than 10ns. If a positive 1.1 voltage level persists for a pulse width greater than 5ns, the corresponding read or write pointer may increment. Data is either written or read twice, or garbage is written to or read from one or more locations. This can cause the FIFO to be "out of sync" where the read or write (or both pointers) are at wrong locations. This problem is solved by keeping the parts creating the $\overline{R}$ and $\overline{W}$ signal as close to the FIFO as possible. If FAST™ or Schottky devices are used, and if ringing occurs, add a series resistor of 20 to 50 Ohms so the impedance of the driver in the high-to-low transition, plus the series resistor, approximately equal the line impedance.

Read ($\overline{R}$) and Write ($\overline{W}$) should be high if read and write operations are not occurring. Crosstalk causes noise on the read and write lines that may be 1.1 volts or greater for more than 5ns. However, if read and write are high and noise appears on the line, the FIFO is more noise immune (as V_{OH} is higher on the driver when a CMOS device in being driven and the V_{CC} noise margin is greater than the ground noise margin). During a long clock low time of 150ns, for a clock cycle of 200ns, a spurious read or write can occur due to noise. If the system can handle it, a better recommended timing is a clock low time of 50ns and a clock high time of 150ns, giving better noise immunity.

Unused data inputs should be tied to ground or V_{CC}. In the standalone mode or width expansion mode, $\overline{XI}$ must be grounded and $\overline{FL}/\overline{RT}$ should be tied HIGH, given the retransmit feature is unused. Good board design techniques must be practiced and a ground plane or power distribution element are highly recommended. Decoupling capacitors of 0.1µf disk capacitors should be used to decouple V_{CC} and ground.

FAST is a trademark of Fairchild Semiconductor Co.

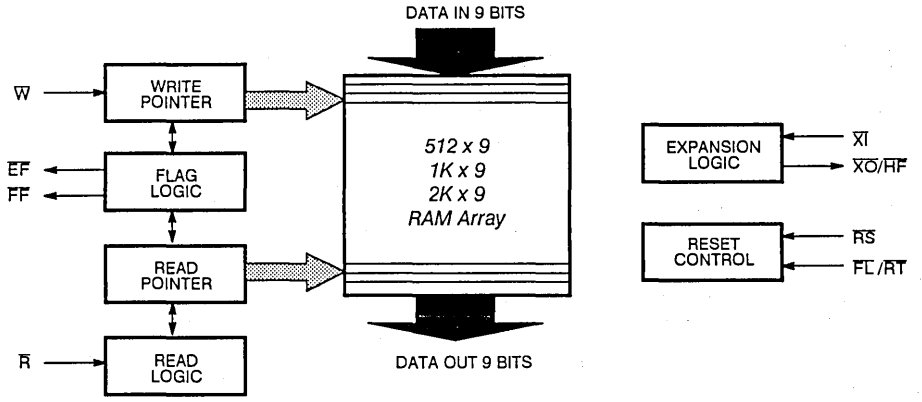

Figure 1. FIFO Block Diagram

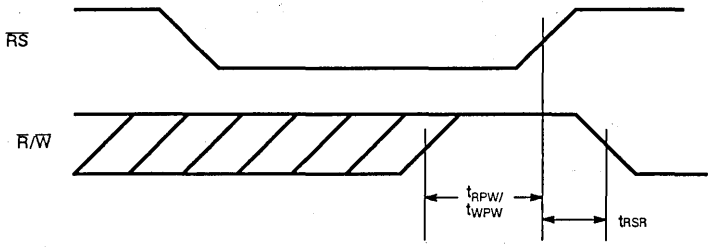

Figure 2. Reset Requirements

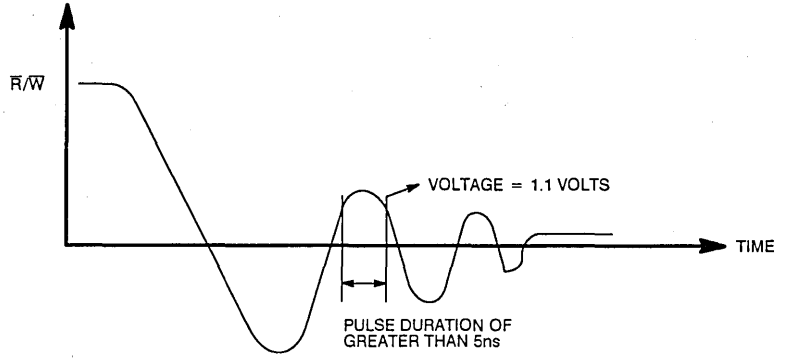

Figure 3. Reflections and Undershoot on the Read and Write lines that cause false increments on the Read and Write pointers

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Integrated Device Technology, Inc.

OPERATING FIFOs ON FULL AND EMPTY BOUNDARY CONDITIONS

TECHNICAL NOTE TN-08

by Suneel Rajpal and Frank Schapfel

The IDT7201, IDT7202, IDT7203 and IDT7204 (512 x 9, 1K x 9, 2K x 9 and 4K x 9) FIFOs have only four control lines: Read, Write, Reset, Retransmit. The focus of this tech note is the relation of the Read and Write lines to the FIFO's empty and full conditions.

These high-speed FIFOs can perform asynchronous and simultaneous read and write operations. Read and Write assert and deassert the Empty Flag and Full Flag. Therefore, special conditions exist when a full FIFO continues to be written to and a read operation takes place. Also, special timings occur when an empty FIFO continues to be read to and a write operation takes place. These operations are called the FIFO boundary conditions.

Read and Write increment the read and write pointers on their respective rising clock edges. The read and write pointers affect the Empty Flag and Full Flag counters. The Empty Flag timings are shown in Figure 1. When the FIFO has only one word in it, the falling edge of the Read causes the Empty Flag ($\overline{EF}$) to be asserted. After the clock cycle is completed (Read goes high again), $\overline{EF}$ will remain asserted and the internal read counter is not affected by subsequent read cycles. $\overline{EF}$ is deasserted by the next rising edge of Write, after which another read pulse can be applied to do a read operation. In asynchronous systems, read and write operations take place at any time; $\overline{EF}$ is set by one signal and deasserted by another asynchronous signal.

When Read is being clocked on an empty FIFO, the outputs will be in high-impedance. If a write operation is performed during asynchronous read cycles, a possible violation of the read pulse width minimum can occur, as shown in Figure 2. $\overline{EF}$ is deasserted, but there is an insufficient read pulse minimum width. To prevent the minimum read pulse width violation, initiate a read operation only after $\overline{EF}$ is high, or guarantee a long enough read pulse width minimum time. A violation of the timing causes an internal glitch on the FIFO Read which can cause the read pointer to be "out of sync." Then the data inside the FIFO may be scrambled or may be garbage. The Empty Flag and Full Flag counters may also be upset by the internal glitch, which upsets FIFO memory usage. The only way to recover from this violation is to do a master reset.

A similar situation arises at the full FIFO boundary condition. When the FIFO is one word from being full, the falling edge of Write causes the Full Flag ($\overline{FF}$) to be asserted. After the write cycle is completed (Write goes high again), $\overline{FF}$ will remain asserted and the internal write counter is not affected by subsequent write cycles. The $\overline{FF}$ flag is deasserted by the next rising edge of the Read, as shown in Figure 3, after which another write pulse can be applied to do a write operation.

When the FIFO is full and Write is being clocked, data sent to the FIFO will be ignored and the write pointer will not increment. Here, as in the earlier case, if these write cycles are asynchronous during a read operation, a possible violation of the write pulse width minimum can occur, as shown in Figure 4. Here, $\overline{FF}$ is deasserted but a sufficient write pulse minimum width is not met. To prevent the problem, initiate a write operation only after $\overline{FF}$ is high, or guarantee a long enough write pulse width minimum time. A violation of the timing causes an internal glitch on the FIFO write line. This can cause the write pointers to be "out of sync" where the data inside the FIFO may be scrambled or may be garbage. The Empty Flag and Full Flag counters may also be upset by the internal glitch. Again, the only way to recover from this condition is to do a master reset.

In summary, these FIFOs are designed to transfer only valid data from input to output. To ensure that valid data is written into and read from, empty and full FIFOs handshake through the flag mechanism. When there is no output data available, the reading side must wait until the end of a write. In a full FIFO, the writing side must wait for the reading side to create an "empty" location. Incomplete read and write cycles can not only invalidate data, but can cause the pointers to be out of synchronization, requiring a master reset to renew data transfer.

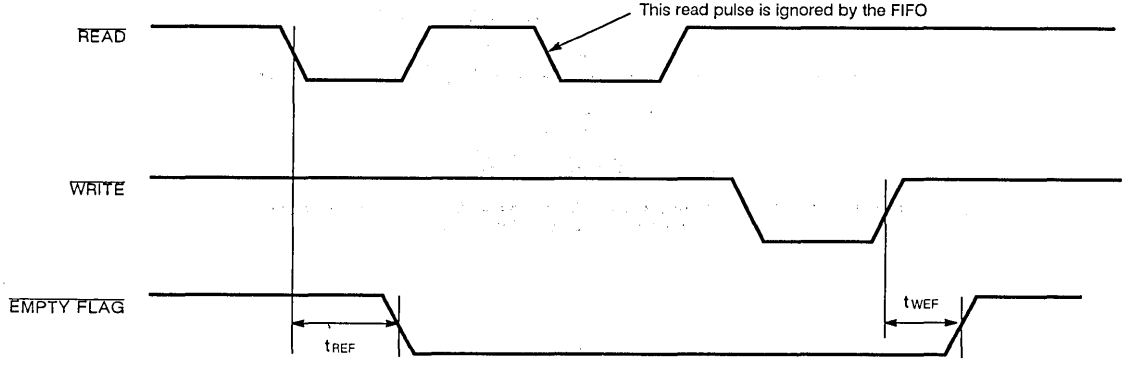


Figure 1. Empty Flag from Last Read to First Write

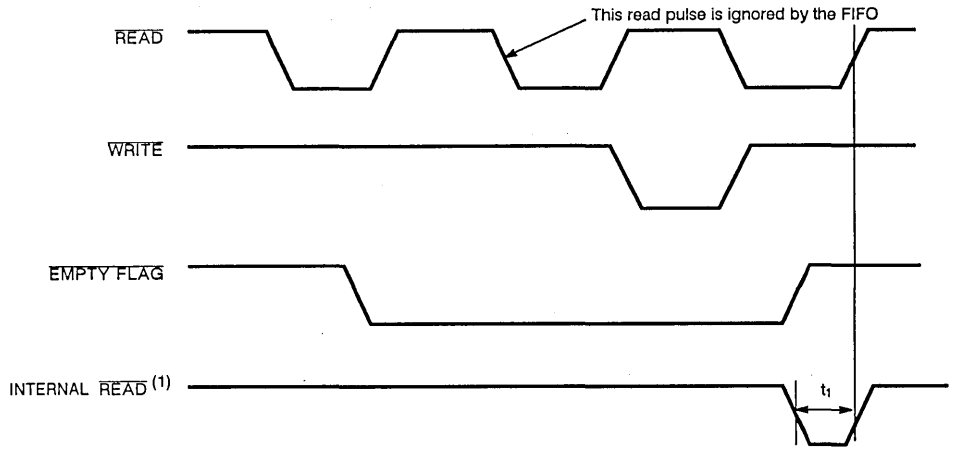
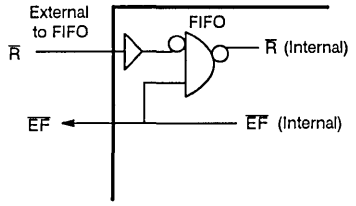


Figure 2. Violation of t_{RPW} During Boundary Conditions

Note:

1. Pulse within the FIFO used to clock the read pointer and the Empty and Full Flag counters.
2. If $t_1 < t_{RPW}$ (minimum read pulse width low), then the read pointer, Empty Flag and Full Flag counters may be out of sync. See Figure 15 of IDT7201/2SA data sheet.



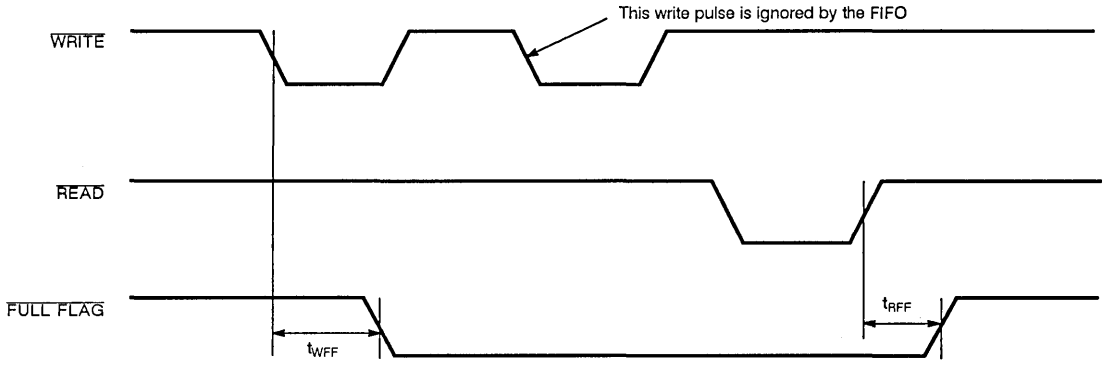


Figure 3. Full Flag from Last Write to First Read

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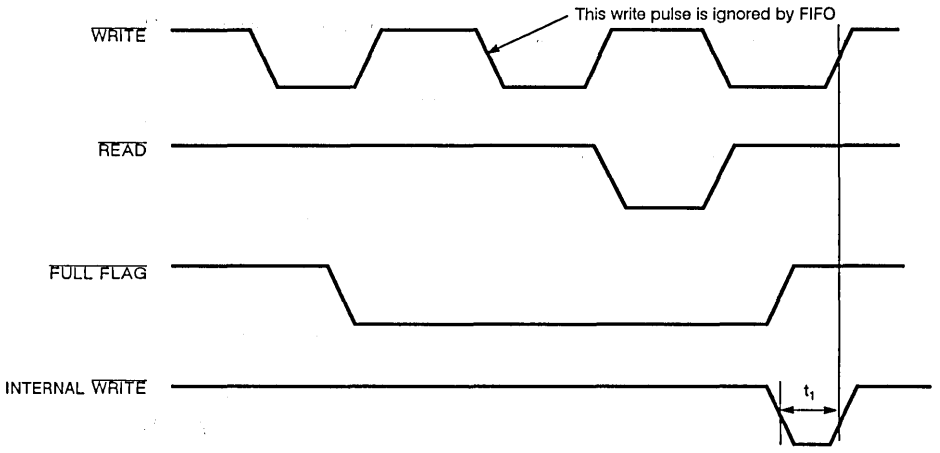
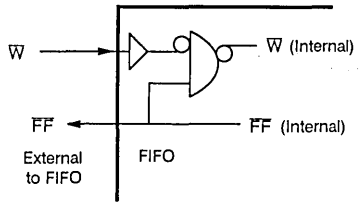


Figure 4. Violation of t_{WPW} During Boundary Conditions



Note:

1. Pulse within the FIFO used to clock the write pointer and the Empty and Full Flag counters.
2. If $t_1 < t_{WPW}$ (minimum write pulse width low), then the write pointer, Empty Flag and Full Flag counters may be out of sync. See Figure 16 of IDT7201/2SA data sheet.

Integrated Device Technology, Inc.

CASCADING FIFOs OR FIFO MODULES

TECHNICAL NOTE TN-09

by Suneel Rajpal and Frank Schapfel

The IDT7201, IDT7202, IDT7203 and IDT7204 are high-speed 512 x 9, 1K x 9, 2K x 9 and 4K x 9 FIFOs, respectively, that can be cascaded to form even deeper FIFOs. This tech note explains how these FIFOs are cascaded. The principles mentioned here also apply to the IDT7M203, IDT7M204, IDT7M205 and IDT7M206 high-speed 2K x 9, 4K x 9, 8K x 9 and 16K x 9 cascadable FIFO modules, respectively.

A cascaded FIFO configuration of 512 x 9 FIFOs is shown in Figure 1. The $\overline{FL}$ pin (First Load) of the first FIFO to be loaded after a reset is tied to ground. The other FIFOs have their $\overline{FL}$ pin tied to Vcc. After a reset operation, the first 512 writes occur in the first FIFO. During these write operations, the $\overline{XO}$ (Expansion Out) and $\overline{XI}$ (Expansion In) lines are high. On the 512th write, a pulse is created on the $\overline{XO}$ line following the $\overline{W}$ line. The pulse informs the second FIFO that it is going to receive the next word. It also informs the first FIFO that its write pointer will no longer increment due to an internal evaluation of the $\overline{XO}$ line. The $\overline{XO}$ line of the first FIFO is connected to the $\overline{XI}$ line of the second FIFO. The $\overline{XO}$ of the second FIFO is connected to the $\overline{XI}$ of the third, and so on. The $\overline{XO}$ of the last FIFO is connected to the $\overline{XI}$ of the first FIFO. A typical $\overline{XO}$ operation of 2048 writes after a reset is shown in Figure 2.

The same procedure holds true for read operations. During the 512th read operation after a reset, another pulse will be created on the $\overline{XO}$ line following the Read line. This pulse will inform the second FIFO that it will be read from on the next cycle (provided it isn't empty). Also the first FIFO's read pointer will not increment until it receives a second pulse on its $\overline{XI}$ line.

Figure 3 shows the $\overline{XO}$ and $\overline{XI}$ relationship to read and write. The $\overline{XO}$ pulses are transferred to the $\overline{XI}$ of the next level of FIFO. The first pulse transfers write pointer control and the second transfers read pointer control. There is an important advantage to this method expansion. A word written to the FIFO after a master reset is immediately available at the FIFO output. A read cycle can be initiated as soon as $\overline{EF}$ is unasserted. This is called zero fall-through time. Earlier shift register-based FIFOs have a fall-through time in the µsec range.

To take full advantage of this unique expansion feature, some design precautions must be observed. Since a pulse on $\overline{XI}$ activates read or write operations of the FIFO, they must be relatively free from cross-talk noise. A long trace from the $\overline{XO}$ of the last FIFO to the $\overline{XI}$ of the first FIFO is a potential source of cross-talk noise. To prevent noise spikes from altering the $\overline{XI}$ input on this and other $\overline{XO}$ to $\overline{XI}$ interconnects, a small capacitor in the 22pF to 47pF range should be inserted between the $\overline{XI}$ inputs and ground.

Another important point is how to handle flags in the expansion mode. To create the composite Full Flag, tie the four individual FIFO Full Flags to an OR gate. The composite Empty Flag is created similarly. This additional logic is shown in Figure 1.

To create intermediate flags using the individual Full and Empty flags is more tricky, but can be done. For example, an attempt to create a composite Half-Full Flag is described here. Let us define Flag f1 as when any two FIFOs are full and at least one other FIFO is not empty. Boolean Equation for f1:

$$f1 = FF1.FF2(\overline{EF3} + \overline{EF4}) + FF2.FF3(\overline{EF1} + \overline{EF4}) + FF3.FF4(\overline{EF1} + \overline{EF2}) + FF4.FF1(\overline{EF2} + \overline{EF3})$$

FFi = Full Flag of FIFOi

EFi = Empty Flag of FIFOi

In one extreme case, f1 is asserted when there is 1.5K-1 words in the FIFO array. The first two FIFOs are full, with 512 words in each, and the third FIFO has 511 words. Another extreme case is when two FIFOs are full and the third FIFO has only one word. Therefore, Flag f1 is only a range of words where the half-full condition exists, from 1K + 1 to 1.5K-1 words in the array. It may not be used as a half-full indicator, because the FIFO array may be almost 3/4 full before Flag f1 is asserted.

As shown in Figure 4, an empty FIFO array has a word written to it and then read from it. Then, 1.5K-1 words are written to the FIFO array. The write pointer is on the last word of the third FIFO. Only at this time is Flag f1 asserted, while the FIFO array has 1.5K-1 words in it. Intermediate flags like f1, generated from Boolean Equations, can only provide a range of values when f1 is to be asserted. A precise position for f1 cannot be determined. If Boolean Equations are used to generate intermediate flags, consider all the different locations of the read and write pointers which may assert or deassert at a particular condition.

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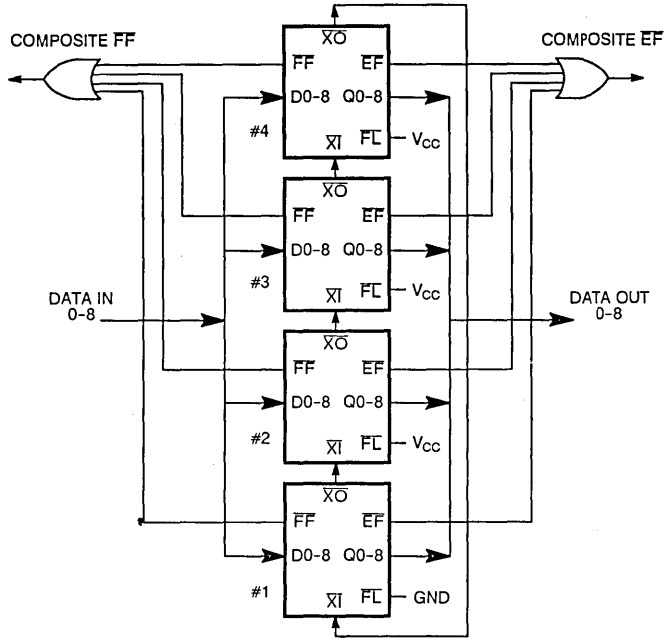


Figure 1. Four Cascaded 512 x 9 FIFOs

NOTE:
Read, Write and Reset controls go to all four FIFOs.

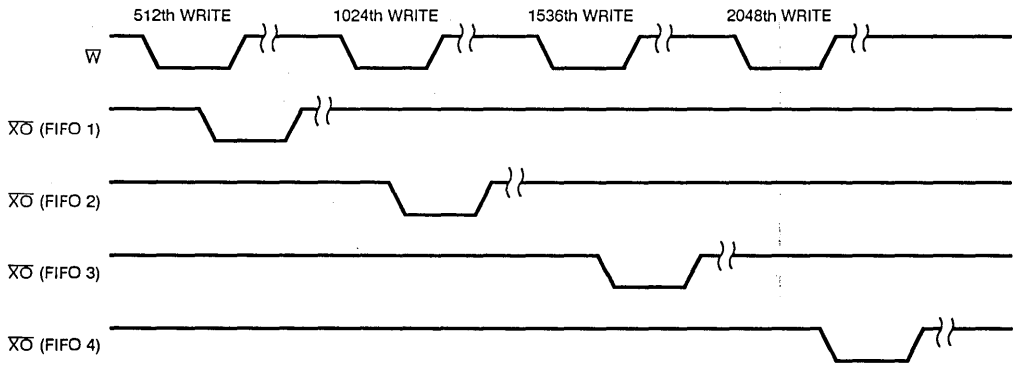


Figure 2. The XO/XI Timing Pulse for 2048 Writes and Zero Reads

NOTE:
Read line is assumed to be HIGH in this example.

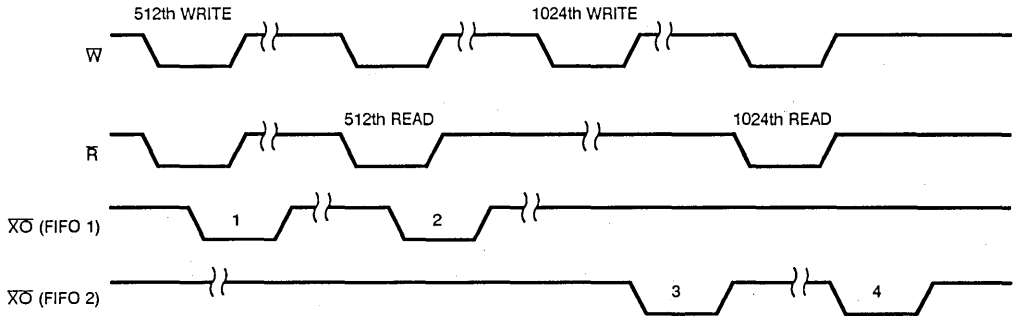


Figure 3. The $\overline{XO}$ and $\overline{XI}$ Pulse Timings

NOTES:
1. Pulse 1 is created by the 512th write pulse; it is a delayed write pulse.
2. Pulse 2 is created by the 512th read pulse.
3. Pulse 3 from FIFO 2 is created by the 1024th write pulse.
4. Pulse 4 is created by the 1024th read pulse.
5. $\overline{XO}$ (FIFO 3) and $\overline{XO}$ (FIFO 4) are not shown, but they follow the same pattern.
6. $\overline{XO}$ (FIFO 4) will be created by the 2048th write pulse and later by the 2048th read pulse, thereby transferring pointer control back to FIFO 1.

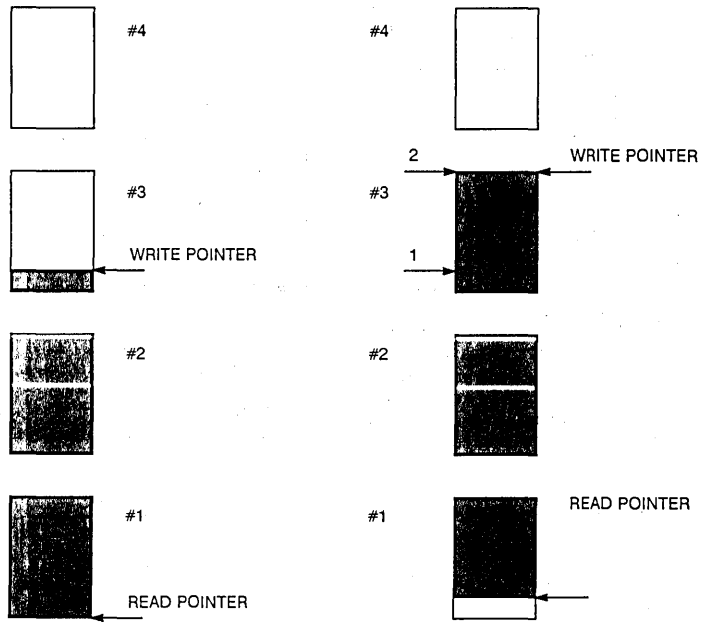


Figure 4. The Behavior of the f1 Flag for Different Cases

Case 1: In the cascaded FIFO arrangement, the write pointer has just written to FIFO #3 and the flag defined by the f1 equation would be asserted at the half-full point.

Case 2: The FIFO array is half-full at arrow at Note 1, but f1 will not be asserted until the last write into FIFO #3 or until the FIFO array is almost 3/4 full or at arrow 2.

Integrated Device Technology, Inc.

DUAL-PORT RAMS SIMPLIFY COMMUNICATION IN COMPUTER SYSTEMS

APPLICATION NOTE AN-02

By David C. Wyland

INTRODUCTION

Dual-port RAMs allow two independent devices to have simultaneous read and write access to the same memory. This allows the two devices to communicate with each other by passing data through the common memory. These devices might be a CPU and a disc controller or two CPUs working on different but related tasks. The dual-port memory approach is useful and popular because it allows the same memory to be used for both working storage and communication by both devices and avoids the need for any special data communication hardware between the devices. The latest development in dual-port RAMs has been the appearance of high speed dual-port RAM chips. These chips allow high speed access by both devices with the minimum amount of interference and delay. Integrated Device Technology offers a family of these devices as shown in Table 1.

Width	Size	Part	Support Logic				Comments
			Interrupt	Busy Logic		Semaphore	
				MASTER	SLAVE		
X8	1K	IDT7130	X	X			
		IDT7140	X		X		
	2K	IDT7132		X			
		IDT7142			X		
		IDT71321	X	X			52-pin
		IDT71421	X		X		52-pin
		IDT71322				X	
	4K	IDT7134					
		IDT71342				X	52-pin
X16	2K	IDT7133		X			
		IDT7143			X		

Table 1. Dual-Port RAMs Available from Integrated Device Technology

DUAL-PORT RAMS: SIMULTANEOUS ACCESS

A dual-port memory has two sets of address, data and read/write control signals, each of which access the same set of memory cells. This is shown in Figure 1. Each set of memory controls can independently and simultaneously access any word in the memory including the case where both sides are accessing the same memory location at the same time. Up to this time, there have been very few true dual-port memories available. Memories have a single set of controls for address, data and read/write logic and are single-port RAMs. If you wanted a dual-port RAM function, you had to design special logic to make the single-port RAM simulate a dual-port RAM in operation.

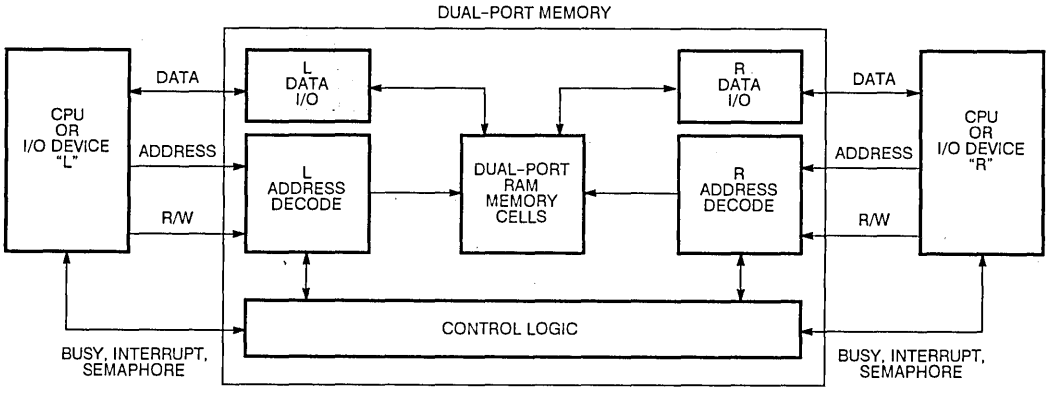


Figure 1. Dual-Port Memory Block Diagram

Direct Memory Access (DMA) as a Dual-Port Memory Simulation

The concept of using a conventional memory to simulate a dual-port RAM has been common in computer systems almost from the beginning. It is known under the name Direct Memory Access, or DMA. In the DMA concept, a single memory is shared between the CPU and one or more I/O devices as shown in Figure 2.

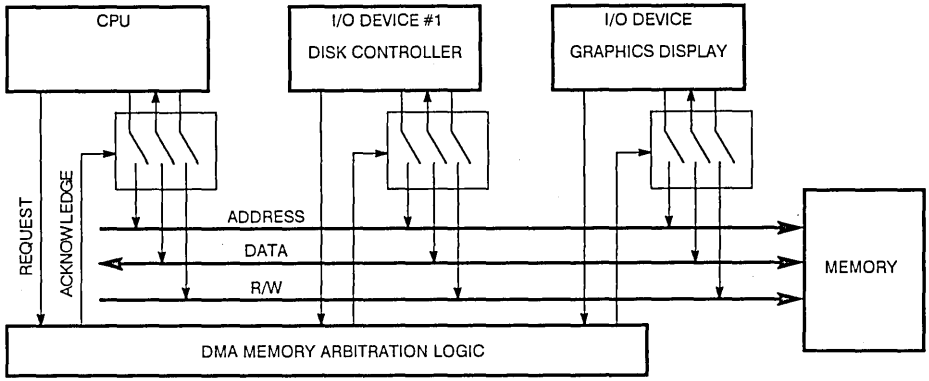


Figure 2. DMA Memory System Block Diagram

Each device wishing to use memory submits a request to the arbitration logic. The arbitration logic responds by connecting the memory address, data and control lines to one of the requesters and tells any other requesting devices to wait by issuing a busy signal. The busy signal causes the memory access logic in the device to wait until busy has gone away before performing a memory transfer.

DMA Limitations: Waiting for the Bus

In a computer system with DMA, the CPU must stop and wait while an I/O device is doing DMA transfers to memory. This works well in typical systems where the I/O devices are transferring data only a small percentage of the time and the impact on CPU processing time is minimal. These assumptions do not hold where you have two CPUs trying to use the same memory. In this case, one CPU must wait while the other uses the memory. As a result, the average speed of the CPUs will typically be cut in half.

There are two solutions to this problem: 1) You can provide local memory for both CPUs and limit use of the common memory to CPU/CPU communication only, in an attempt to reduce the time impact of DMA waiting, or 2) you can provide true hardware dual-port memory between the CPUs and all simultaneous high-speed access by both CPUs to the same memory without waiting. The introduction of high-speed dual-port RAM chips now makes the second option practical.

Dual-Port RAM Chips: How They Work

A true dual-port memory allows independent and simultaneous access of the same memory cells by both devices. This means two complete and independent sets of address, data and read/write logic and memory cells that are capable of being read and written by two different sources. An example of the dual-port memory cell is shown in Figure 3. In this cell both the left and right hand select lines can independently and simultaneously select the cell for read out. In addition, either side can write data into the cell independent of the other side. The only problem would be when both sides try to write into the same cell at the same time. We will discuss this in a moment.

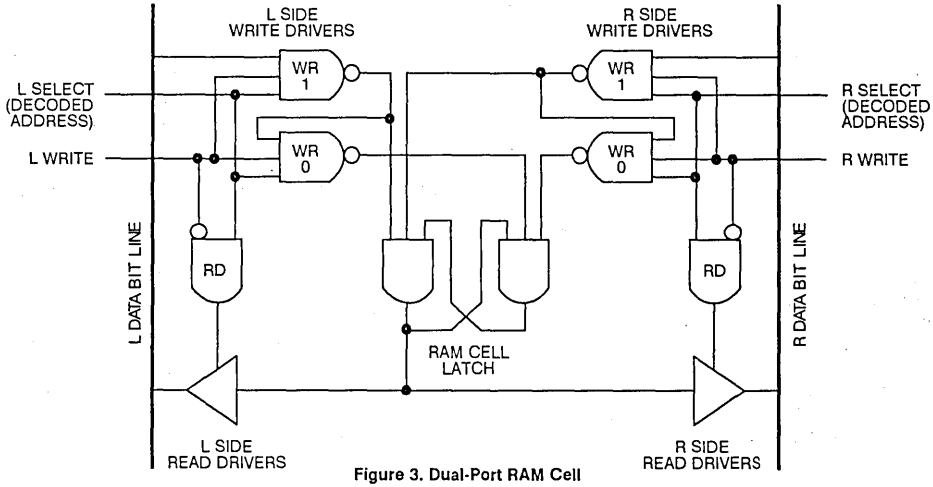


Figure 3. Dual-Port RAM Cell

DUAL-PORT RAM CONTROL LOGIC

Dual-port RAM chips include control logic to solve three common application problems: signaling between processors, timing interactions when both are using the same location and hardware support for temporary assignment (called allocation) of a block of memory to one side only.

Interrupt Logic For Signaling

A common problem in dual-processor systems is signaling between the processors. For example, processor A needs to signal processor B to request a task to be performed, as defined by data in the common memory. When processor B has completed the task, it needs to signal processor A that the task is done. Note that the signaling must occur in both directions. A common form of signaling is for one processor to cause an interrupt on the other processor. This allows the receiving processor to be informed of a communication without having to constantly check for it.

Hardware support for this signaling function is provided by interrupt logic, available on certain IDT dual-port RAM chips. A block diagram of this logic is shown in Figure 4. In these chips, the top two addresses of the memory chip also serve as interrupt generators for each of the ports. If the left side CPU writes into the even address of this pair (3FF in a 1K RAM) an interrupt latch is set and the interrupt line to the right hand port is activated. This interrupt latch is cleared when the right hand CPU reads from the even address. A similar set of logic is provided to allow the right hand CPU to interrupt the left hand one. This logic is associated with the odd address of the pair (3FE in a 1K memory). Providing this logic on chip saves the system designer from having to design in extra logic to allow one CPU to interrupt the other.

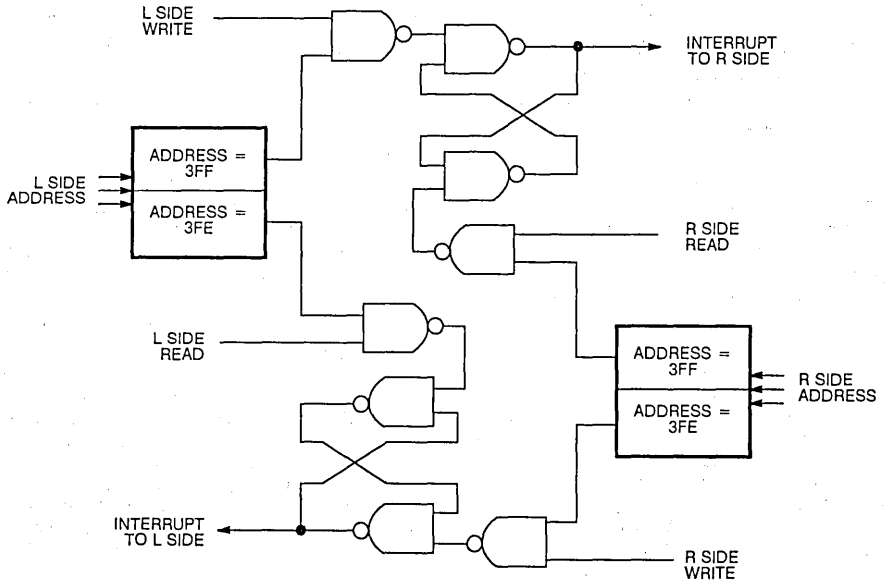


Figure 4. IDT7130 Interrupt Logic

Busy Logic Solves Interaction Problems

A problem can occur with dual-port memories when both ports attempt to access the same address at the same time. There are two significant cases: when one port is trying to read the same data that the other port is writing and when both ports attempt to write to the same word at the same time. If one port is reading while the other port is writing, the data on the read side will be changing during the read and a read error can be caused. If both ports attempt to write at the same time, the memory cell is being driven by both sides and the result can be a random combination of both data words rather than the data word from one side or the other. Busy logic solves this problem by detecting when both sides are using the same location at the same time and causing one side to wait until the other side is done.

Note that although one or the other processor may have to wait occasionally, the throughput loss is minimal, typically less than 0.1%. This is because the probability of both processors using the same location at the same time is small. For example, if there are a thousand words in memory with a relatively uniform and random access of these locations by either side, the probability of a given location being accessed by one side is of the order of one part of a thousand. The probability of both sides accessing the same location at the same time is, therefore, of the order of one part in a million. As a result, the average throughput of the system is reduced by only one part per million due to dual-port RAM access contention (again, assuming uniform random address access by both sides).

Busy Logic Design

Busy logic is called hardware address arbitration logic because it consists of hardware that decides which side will receive a busy signal if the addresses are equal. It consists of common address detection logic and a cross coupled arbitration latch. A logic diagram of the type of busy logic used in the IDT dual-port RAM chips is shown in Figure 5. The purpose of this logic is to provide a busy signal for the address that arrived last, to inhibit writing to the busy port and to make a decision in favor of one side or the other when both addresses arrive at the same time. This logic consists of a pair

of address comparators, a pair of delay buffers, a cross-coupled latch and a set of busy output drivers. The address comparator output goes true when the addresses at its inputs are equal.

In the logic shown in Figure 5, the ability to detect which address arrived last is provided by the time delay buffers between address lines and the comparators. If we assume that the L address is stable and the R address changes to match the L address, the R address comparator will go true immediately while the L address comparator will become active some time later as determined by the time delay gates.

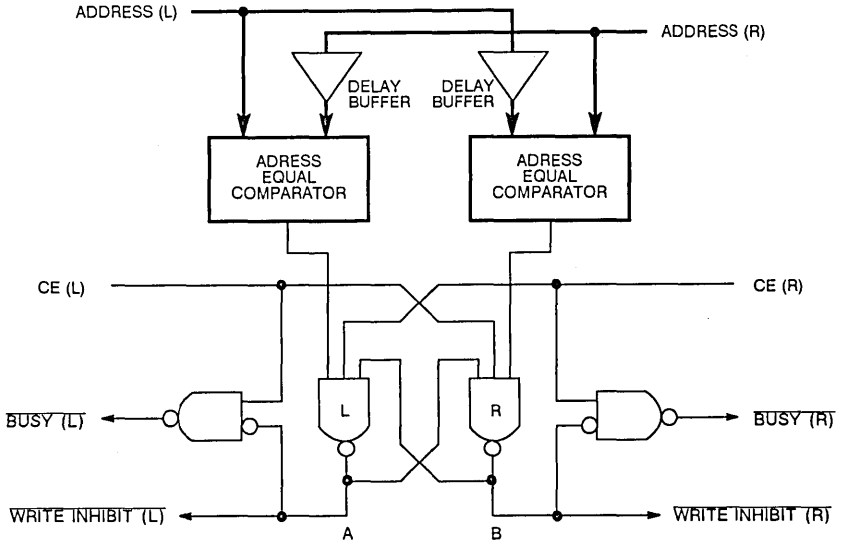


Figure 5. Dual-Port Busy Logic Design

The arbitration latch formed by the L and R gates reflects the address comparator output timing. This latch has three stable states, both latch outputs A and B high, A low/B high and A high/B low. Initially, both A and B are high because the outputs of both address comparators are low. We start with the L address stable and the R address arriving later. When the R comparator becomes active its output will go high and B will go low. The A output will remain high because its address comparator input will go high sometime later and the L gate input from B output will go low before this occurs. The result is that the R gate B output will be active inhibiting writing to the R side of the dual-port RAM and activating the busy signal to the R port.

The extreme case of busy logic decision making is when both addresses arrive at exactly the same time. In this case, the outputs of both address comparators go high at the same time activating both sides of the arbitration latch. The latch will settle into one of two states with either the A or the B latch output being active. The latch design ensures that a decision will be made in favor of one side or the other.

The chip enable lines come directly into the arbitration latch, although they could have been brought into the address comparators along with the other address lines. This is because if the chip enable for one side is inactive, both reading and writing for that side is automatically inhibited and/or arbitration is not needed. If the addresses are equal, the chip enable that arrives last will lose the arbitration. If both chip enables are active then arbitration will be determined by the settling of the address lines.

Temporary Assignment of Memory to One Side

A common problem in dual-port RAM application is the need to temporarily assign a block of memory to one side. For example, sometimes you need to update a data table as whole and you cannot allow the other processor to use the table until you are done. This is called block allocation of the memory.

Block allocation can also be used to avoid the address arbitration problem since it is a way of ensuring that both sides do not use the same address at the same time. This method is also called software arbitration because the software on both sides decides and agrees as to who has permission to use a given portion of the memory. Software allocation has the advantage of not requiring busy logic, which is useful in systems which cannot accommodate a busy signal.

The design problem with block allocation is communication of the assignments between the CPUs. A simple but time consuming method is to pass messages between the CPUs, perhaps aided by interrupt logic. In the message method, processor A requests use of a block from processor B. Processor B agrees and sends permission back to processor A. When A is finished it sends a release message to B which responds with a release acknowledge to A. In this system, four messages are sent for each block assigned and released.

Semaphore Logic Support for Memory Assignment

Although block allocation is a software technique, it can benefit from hardware support. In message passing allocation, four messages must be passed to assign and release a block of memory. Semaphore logic, available in certain IDT dual-port RAMs, can be used to eliminate this message passing and its associated overhead. Semaphore logic provides a set of flags especially designed for the block assignment function. Each flag is used as a token to indicate which CPU has permission to use a block of memory.

Each semaphore flag can be set to one side or the other but not both. This ensures that only one side has permission to use the block of memory.

The IDT semaphore logic bits are designed to be used in a set-and-test sequence. Each bit is normally in the logic one state, indicating that it is not assigned to either side. A processor, desiring to assign a bit and, therefore, its associated block of memory, attempts to write a zero into the bit. It then reads the bit to see if it was successful. If it was, the bit will read zero, and the processor has use of the block. If it reads a one, it was unsuccessful, and the block is in use by the other side. The processor must then wait until the bit becomes zero, indicating that the other side has released it.

Semaphore flags have a particular requirement: a given flag can be assigned to only one side at a time. Specifically, you must not have a situation where both sides simultaneously think they have permission to use a block. Semaphore logic is designed to resolve this problem. If both sides attempt to set a semaphore flag at exactly the same time, only one side sees it set.

Semaphore flags consist of eight individually addressable dual-port latches. Each latch can be read and written by either side. They are selected by a separate chip enable, addressed by the three last significant bits of the address lines and are read and written through the D_0 data bit. Except for sharing the address, data and read/write pins of the RAM, the semaphore latches are completely independent, as shown in Figure 6.

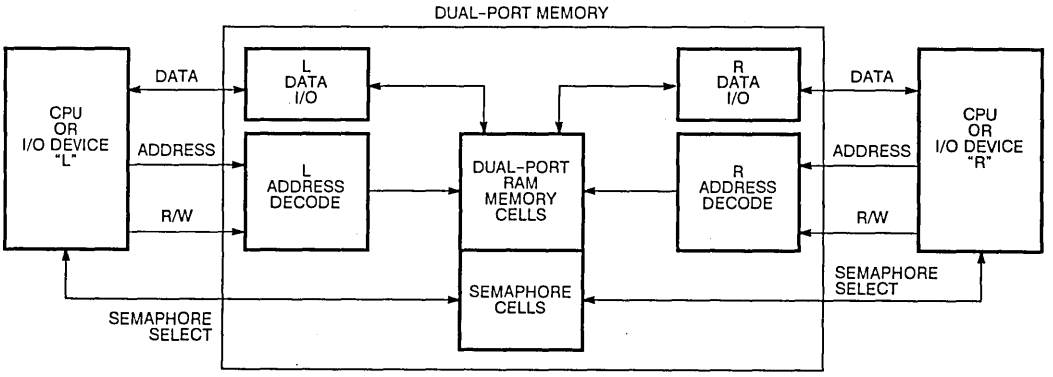


Figure 6. Dual-Port RAM Semaphore Logic

A logic diagram of a semaphore logic flag is shown in Figure 7. In this logic, both flip-flops are initially at logic one and both Grant outputs are high. If only one flip-flop is set to zero, its corresponding Grant output will go to zero. If the other flip-flop is set later, this will have no effect. If both flip-flops are set at the same time however, the latch will settle so that only one Grant output goes low, ensuring that only one side receives permission to use the resource.

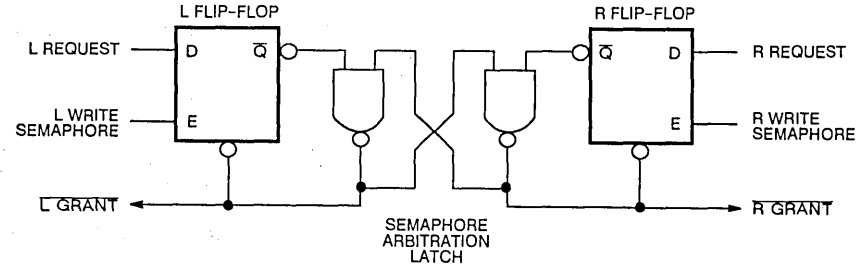


Figure 7. Semaphore Logic Design

DUAL-PORT RAM CHIP TIMING

The dual-port RAM has a simple static RAM interface and timing requirements. There are some special requirements associated with Busy, however. A timing diagram, shown in Figure 8, shows the relationships between address, data, read/write, chip select and busy signals for a dual-port RAM chip and busy logic. In this diagram, the chip select is used to enable the chip for a read or write operation after the addresses have settled. An arbitration is performed at the leading edge of the chip select.

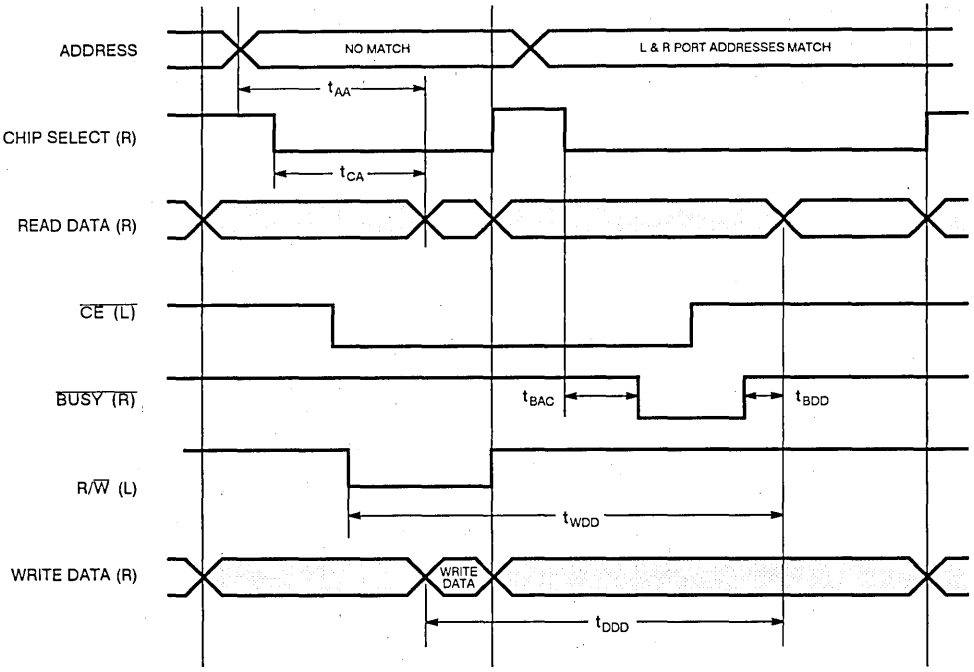


Figure 8. Dual-Port RAM Timing Diagram

Busy Logic Timing

In the case of address contention, the busy signal from the losing RAM port stabilizes some time after the leading edge of its chip select (or after its address settles, whichever comes last). If the busy signal is going to become active, it will become active during this time or not at all. If the busy signal is generated, the CPU must wait for busy to go away before completing the read or write cycle. Once the busy signal has gone high the memory read or write cycle can proceed to completion.

Note that during the arbitration time following the chip select the busy signal may be changing. Since it is possible to have a glich on the busy line during this indeterminate period, the busy line should be sensed as a level rather than as an edge.

Busy arbitration will be somewhat slower in the extreme case where both addresses arrive at exactly the same time. This is because both gates of the arbitrator latch are initially inactive and must settle into a state where only one of them is active. There will be a period of time when both gates are in transition. This is called the metastable condition and is a classic and unavoidable problem in latch and flip-flop design. As a result, the busy settling time is somewhat longer in the low probability worst case than in the commonly observed typical case. The maximum arbitration times, t_{BAA} and t_{BAC}, on the data sheet give the worst case values, including metastability setting, for these times.

Read/Write Timing with Busy

The read and write timing for either port of the dual-port RAM chip is the same as a simple static RAM in the absence of address contention. All the standard timing measures apply: read data address access time is t_{AA}, etc.

Dual-port RAMs have additional timing specifications for the case of address contention where one port is busy and waiting for access. For the most general and conservative case, the read or write cycle for the waiting side should begin after the busy signal goes away. The actual timing can be somewhat shorter than this in most cases.

For the case where the waiting side is waiting to write, the write timing requirement is that the write pulse width be measured from busy going away. For the case where both sides are reading, the data will be available at the outputs one access time after the address/chip select lines settle even though the busy line is active. In the most common case, the trailing edge of busy will occur more than one access time after the address and data for the busy side have settled. As a result, the read access time as measured from the trailing edge of busy, for this case t_{BDD}, is effectively zero.

The write/read case, waiting to read while the other side is writing to the same location, has some additional timing specifications. Since writing to a location by the L side, for example, will involve changing the data the cell being read by the R side, there is a write-to-read propagation delay time. This time is t_{WDD} for the delay for constant write data from the leading of the write pulse to the read data, and t_{DDD} for the delay for changing write data from a change of the write data to the read data.

If the writing side is running at minimum values for the write pulse or write data set-up times, the read access time, t_{BDD}, will no longer be zero. The actual t_{BDD} will be equal to t_{WDD} minus the actual write pulse width or t_{DDD} minus the actual write data set-up time, which ever is larger (and greater than zero). Note: t_{BDD} is always less than t_{AA} for the worst case of minimum write values. This is why the read or write cycle is begun from the trailing edge of busy for the most conservative case recommended above.

DUAL-PORT MEMORY EXPANSION: MAKING BIG ONES OUT OF LITTLE ONES

Dual-port RAM chips can be combined to form large dual-port memories. Expansion in memory depth with dual-port RAMs is similar to expansion in depth for conventional RAMs. An example of this kind of expansion is shown in Figure 9 where and 8K x 8 dual-port RAM has been made out of 2K x 8 dual-port RAM chips.

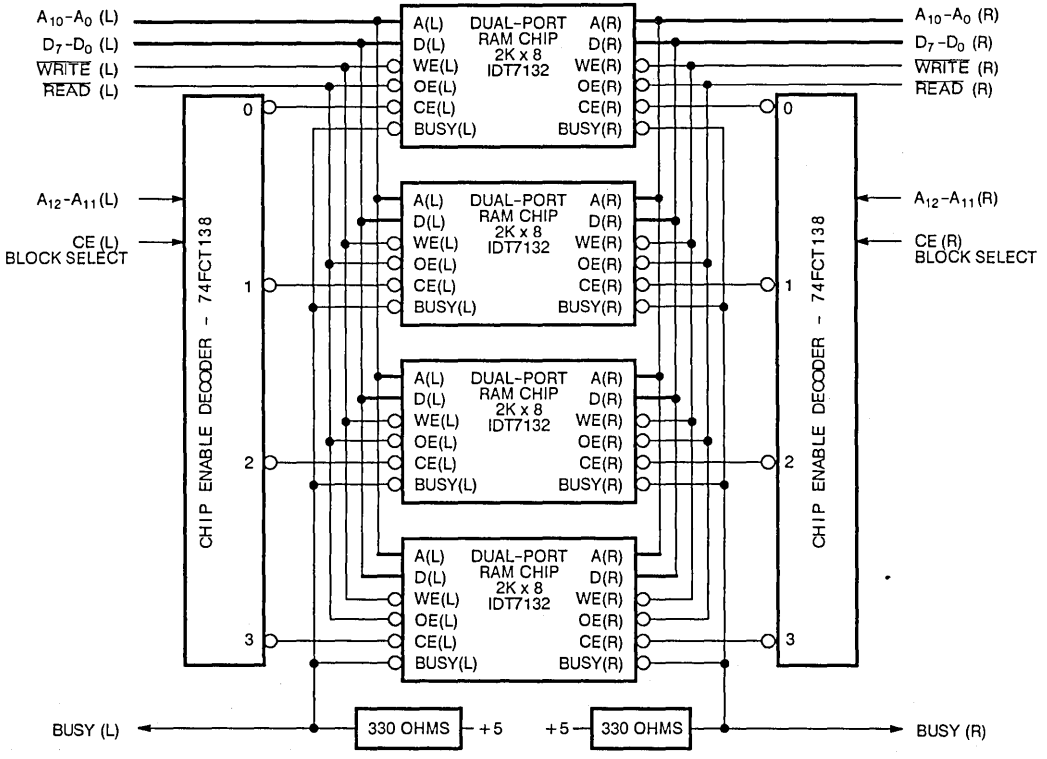


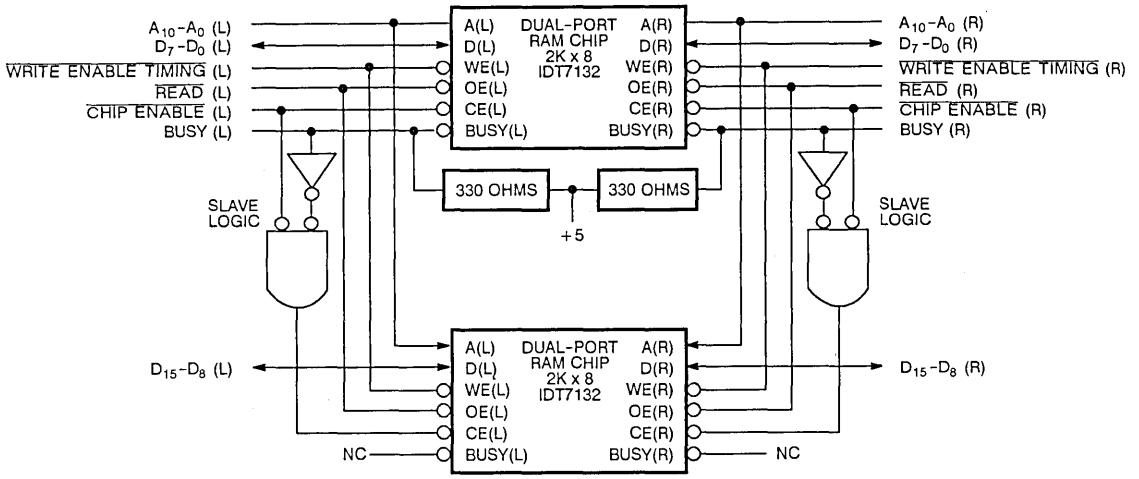
Figure 9. Depth Expansion of Dual-Port RAMs

Width Expansion: The Busy Lock-up Problem

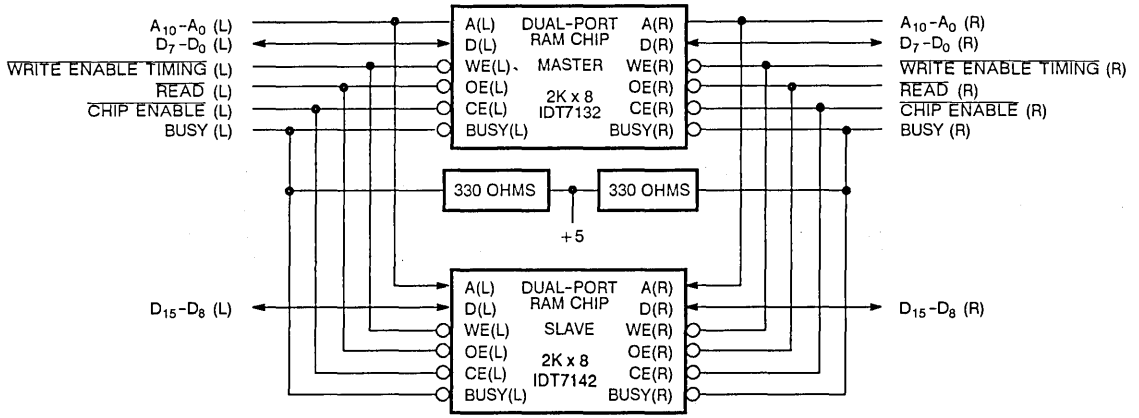
Dual-port RAMs can also be expanded in width. However, in this case, we have a subtle problem. Expansion in width implies that several dual-port RAM chips will be active at the same time. This is a problem if several hardware arbitrators are active at the same time. If we examine the case of a 16-bit RAM made out of two 8-bit RAMs, we can better understand the problem. If the addresses for both ports arrive simultaneously at both RAMs, it is possible for one RAM arbitrator to activate its L busy signal and the other RAM to activate its R busy signal. If both busy signals are used on each side, we now have a situation where both sides are simultaneously busy. The system is now locked up since both sides will be busy and both CPUs will wait indefinitely for their port to become free.

The Busy Lock-up Solution: Use Only One Arbitrator

The solution to this busy lock-up problem is to use the arbitration logic in only one RAM and to force the other RAM to follow it. In this case, one RAM is dedicated as the arbitration MASTER and additional RAM are designated as SLAVES. Two solutions to this problem are shown in Figure 10. One solution is to add external logic to the chip-enables of additional dual-port RAM chips. The logic gates shown cause the SLAVE RAM chip select to be disabled if the MASTER RAM is busy. Since only one set of arbitration logic is controlling the system the problem of SLAVE lock-up is avoided.



Width Expansion with SLAVE Logic (Not Recommended)



Width Expansion with SLAVE Chips (Recommended)

Figure 10. Width Expansion of Dual-Port RAMs

The second, more desirable solution, is to use specially designed dual-port RAM SLAVE chips which are part of IDT's product line. These SLAVE chips incorporate the SLAVE disable logic internally so that no additional logic is required to make a MASTER/SLAVE combination. In the SLAVE chip, the busy pin serves as an input rather than an output. If the MASTER chip activates busy, the SLAVE chip will sense this busy state and internally disable its write enable. SLAVE chips provide a speed advantage over systems which use external logic to implement the SLAVE function. Since the SLAVE logic is built into the SLAVE RAM chip, it can be designed so that there is no speed penalty when using SLAVE chips to expand the dual-port RAM width.

Width Expansion: Write Timing

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed until after the busy input at the SLAVE has settled. Otherwise, the SLAVE chip may begin writing while the busy signal is settling. This is true for systems using SLAVE chips and for systems using conventional dual-port RAMs with SLAVE logic. This delay can be accomplished by delaying the write enable to the SLAVE by the arbitration time of the MASTER. This is shown in Figure 11.

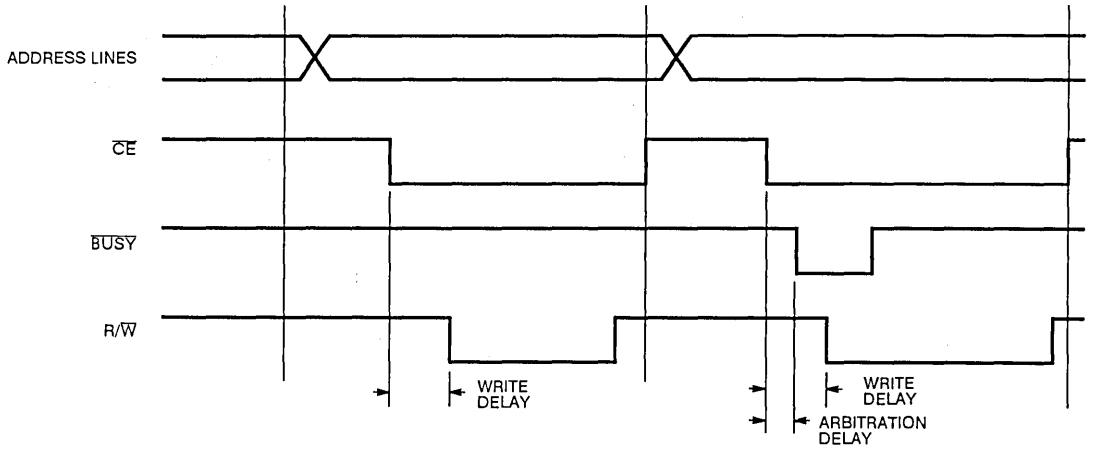


Figure 11. MASTER/SLAVE Write Timing

Note that the write delay is required only in width expanded systems which use SLAVE RAMs, not in single chip or depth expanded systems where only one chip is active at a time. This is because the individual chips have a built-in delay between the chip select and write enable inputs and the internal write enable to the RAM. Separate timing must be supplied in the SLAVE case because this internal delay time can be balanced to the arbitration time only within a chip and can vary from chip to chip. If the delay time for the SLAVE is less than the arbitration time of the MASTER, writing could begin before busy became active, as above.

Width and Depth Expansion: An Example

These techniques for expanding dual-port memories in width and depth are combined in the example shown in Figure 12. In this example, an 8K x 16 dual-port memory is made from 2K x 8 chips in MASTER/SLAVE combination.

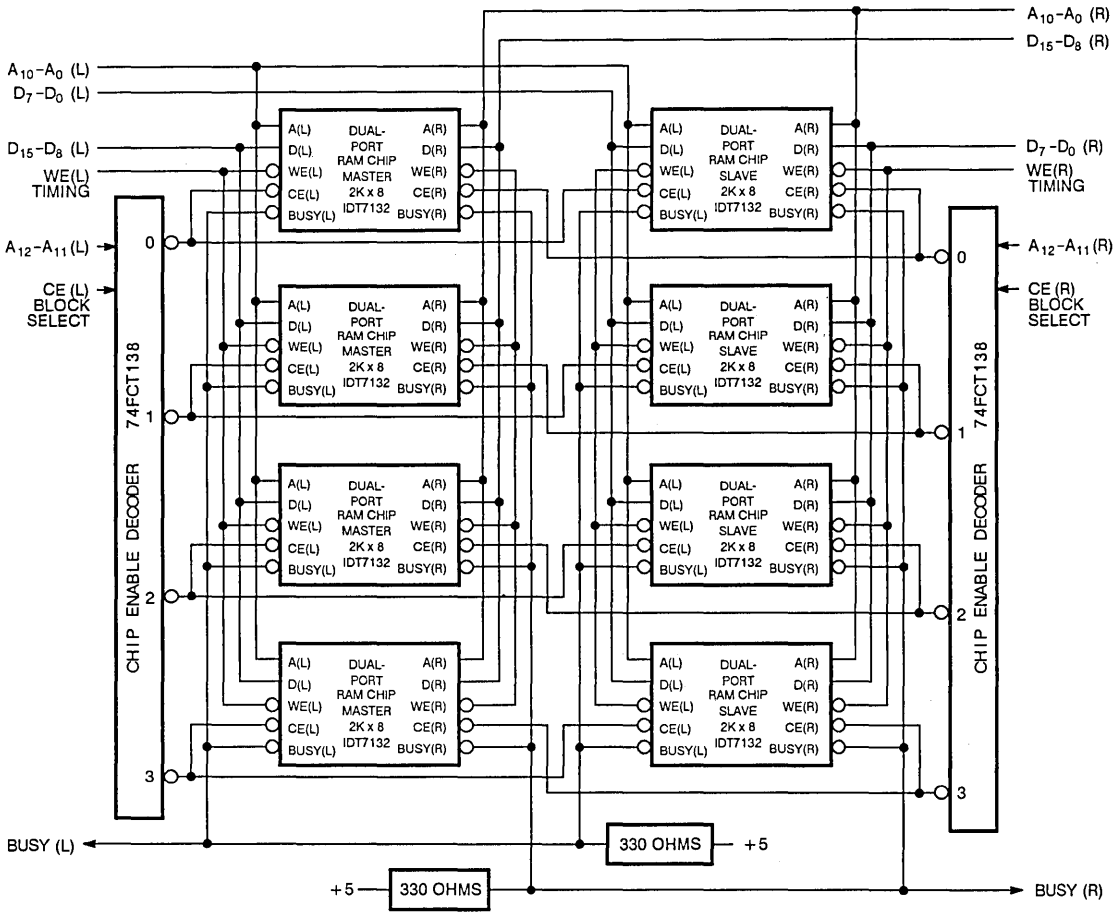


Figure 12. Width and Depth Expansion of Dual-Port RAMs

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USING THEM: DUAL-PORT RAM APPLICATION EXAMPLES

Examples of dual-port RAMs used for CPU-to-CPU communication are shown in Figures 13, 14 and 15. In Figure 11, a pair of 8-bit processors communicate using a single 2K x 8 dual-port RAM chip. In Figure 12, there is a similar system where a pair of 16-bit processors communicate using a pair of dual-port RAM chips and a MASTER/SLAVE configuration. Finally, in Figure 13, we have an 8-bit processor communicating with a 16-bit processor through two 2K x 8 dual-port RAMs.

In Figure 13, two Z80 microprocessors communicate using a single IDT7132 dual-port RAM chip. The IDT7132 is controlled by the chip enable. The write enable is set up in advance by the WR signal from the Z80 and the chip enable is used to write data into the RAM or to gate the read data onto the Z80 bus. The output enable (not shown) is tied to ground (continuous enable). The write enable is used to disable the output drivers.

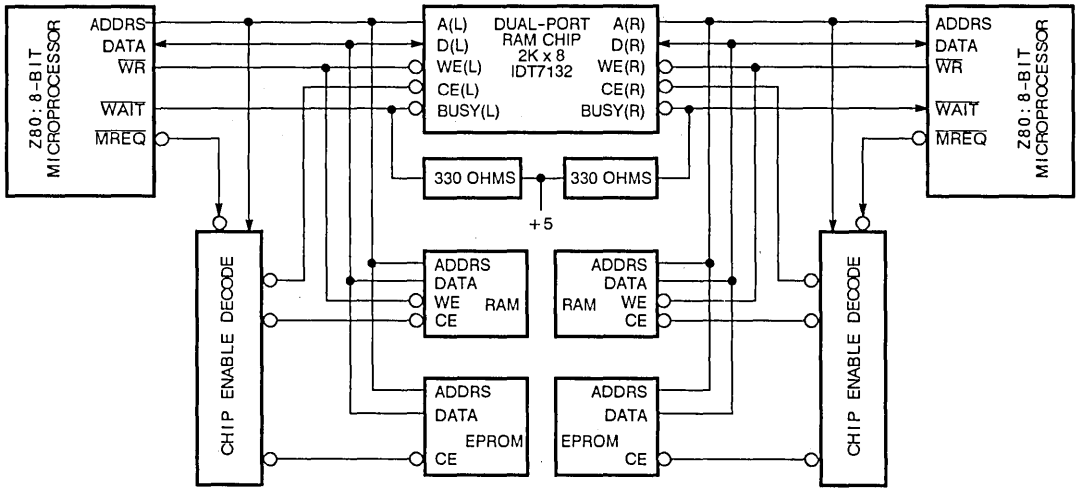

Figure 13. 8-bit to 8-bit CPU Communication

In Figure 14, two 68000 microprocessors communicate through a pair of dual-port RAMs. A IDT7132/7142 MASTER/SLAVE pair is used to avoid the busy lock-up problem. Note that the Address Strobe (AS) from each 68000 is used with an address decoder to enable the dual-port RAM chips. This is to maintain the address for read-modify-write cycles so that arbitration is not lost between the read and the write. This is important for test and set instructions, for example.

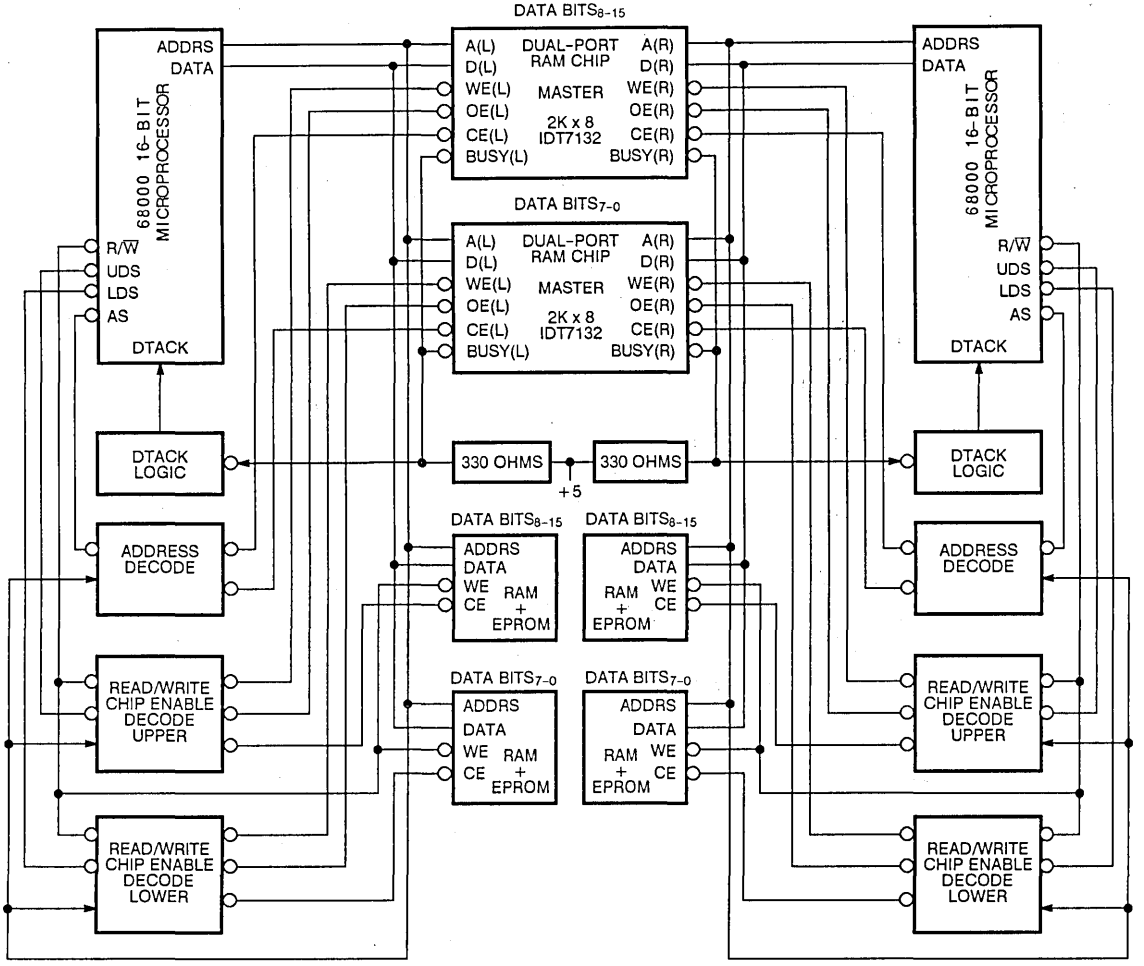

Figure 14. 16-bit to 16-bit CPU Communication

In Figure 15, a Z80 and a 68000 communicate using a pair of IDT7132 dual-port RAMs. No SLAVE logic is required because the Z80 side chip enable decode ensures that only one RAM chip will be enabled at a time. Otherwise, this figure is a combination of the logic from Figures 13 and 14.

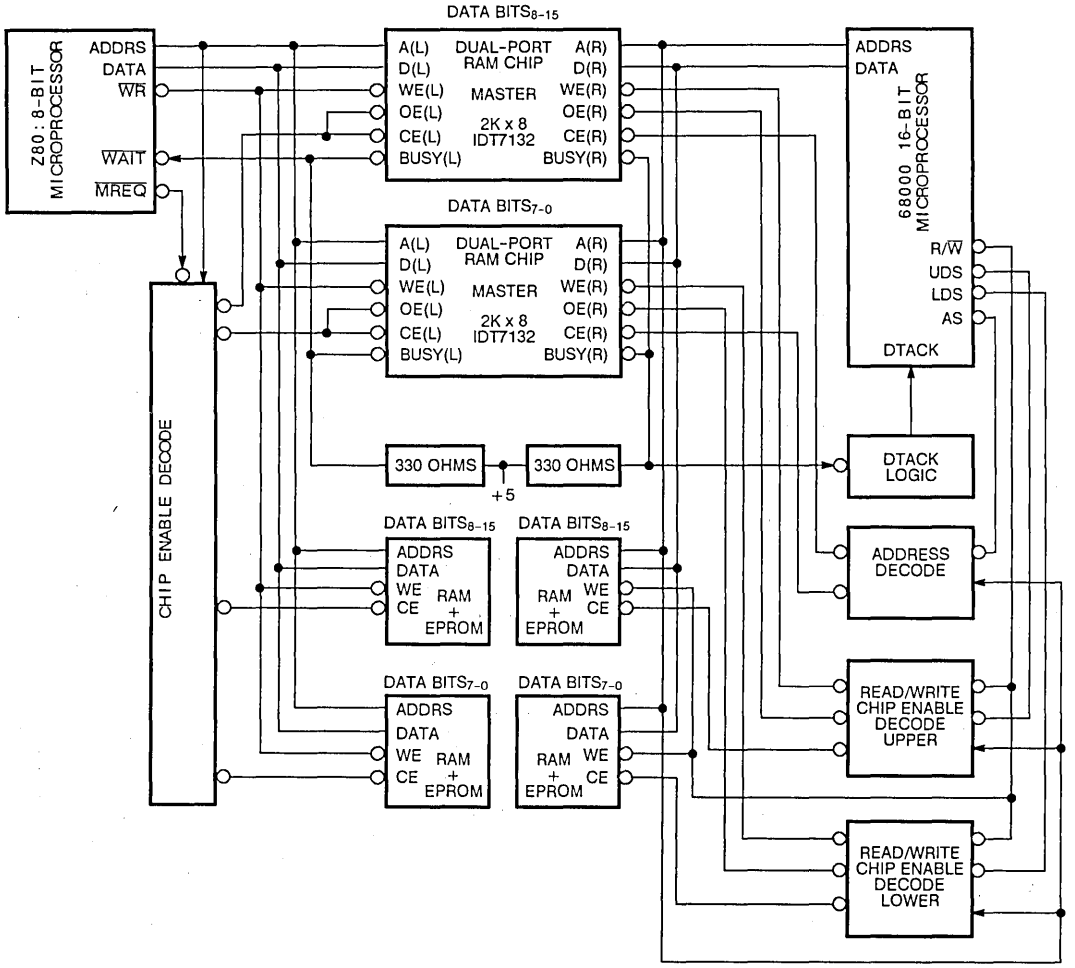

Figure 15. 8-bit to 16-bit CPU Communication

SUMMARY AND CONCLUSION

The development of true dual-port memories in integrated circuit form provides the designer with the ability to set up communication between components of a computer system while avoiding many of the problems of prior systems. While the concept of dual-port memory has been with us from the early days of computing in the form of DMA, the new dual-port ICs can provide this function at very high speeds and without the delays associated with earlier designs. Because of the utility of the dual-port memory concept these chips should come into wide spread use and become one of the standard components used by the computer designer.

Integrated Device Technology, Inc.

DUAL-PORT RAMs YIELD BIT SLICE DESIGNS WITHOUT MICROCODE

APPLICATION NOTE AN-09

By DAVID C. WYLAND

ABSTRACT

High-performance controller designs use bit-slice components for their speed and design flexibility. Speeds of 10-20 million instructions per second (MIPS) are common and the designer can use bit-slice design flexibility to perform speed-critical operations in one instruction. Bit-slice designs have the drawback, however, of requiring microcode design for their implementation, often with a long development cycle. The problem is that the microcode resides in a separate, stand-alone control memory which prevents use of the kind of interactive prototyping and debugging tools associated with conventional microprocessors. The problem can be eliminated by using a dual-port RAM for the control memory, making it part of the data memory address space, and converting the controller to a CPU by borrowing some techniques from Reduced Instruction Set Computer (RISC) designs. The result is a RISC controller where the microinstructions of the bit-slice approach become the instructions of a computer. The design approach provides all the speed and architectural flexibility of microcoded bit-slice designs, while allowing the use of interactive debugging methods associated with microprocssors.

BIT-SLICE VERSUS RISC ARCHITECTURES

An example of a typical bit-slice controller design is shown in Figure 1. It consists of a control flow section and a data flow section. The control flow section has a microinstruction counter and the control memory. The data flow section has a register and ALU element—the bit-slice—plus a data memory and I/O registers on a data bus. Note that the control and data memories are separate. The use of separate data and instruction memories is called the Harvard architecture. The separate control memory provides some of the speed associated with bit-slice designs because it operates in parallel with the data memory. This allows the next microinstruction to be fetched from the control memory, while data for the current instruction may be read from the data memory. This contrasts with conventional microprocessors which alternately get instructions and data from the same memory. This use of a single memory for instructions and data is called the Von Neumann architecture.

There is a remarkable similarity between the block diagram in Figure 1 and the block diagrams of RISC computers, as can be noted by comparing the block diagram in Figure 1 with the block diagram of a RISC CPU shown in Figure 2. The difference is that the control memory and the data memory of the controller have been replaced by an instruction cache memory and a data cache memory in the RISC CPU. The instruction and data cache memories work the same as their microcode counterparts except that they both contain copies of data in the common main memory. The programmer sees a single memory—the main memory—while the hardware works as if it has two independent memories. In this manner, the RISC computer has the speed advantage of the Harvard architecture and the single memory for programs and data of the Von Neumann architecture.

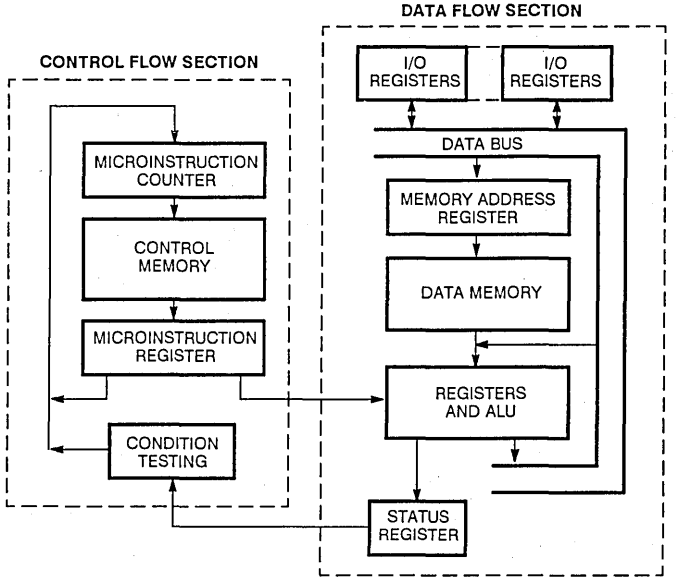

Figure 1. Bit-Slice Controller Block Diagram

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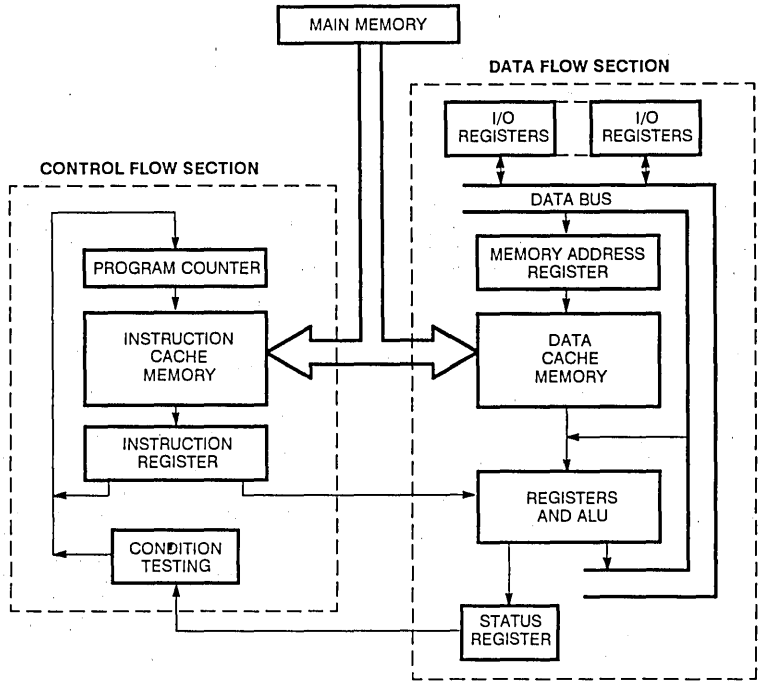

Figure 2. RISC CPU Block Diagram

The instruction and data caches of the RISC architecture are equivalent to having two ports on one memory. We can apply this concept to bit-slice controllers by using a high-speed dual-port memory in place of the cache memories, as shown in Figure 3. The dual-port RAM allows the instruction and data ports to be active simultaneously and independently, while providing both sides access to a common set of RAM cells. Since both ports are working from the same memory, the data flow section can load and move both data and instructions in the same manner as a conventional microprocessor. As a result, this design functions as a conventional CPU with a long instruction word. This allows conventional interactive software tools, such as interpreters and monitors, to be used in system development and debugging.

DESIGN OF A RISC CONTROLLER

The design of a RISC controller using a dual-port control memory is similar to a conventional bit-slice design except for inclusion of a minimum set of operations for a CPU. This allows use as a conventional computer for software coding and debugging. In ordinary bit-slice controller designs, the minimal CPU operation set already exists as a subset of the data flow and control operations already present.

A minimal set of CPU operations, suitable for bit-slice designs, can be derived from the instruction set of a RISC-like computer such as the Data General Nova minicomputer. It is a useful example because it is a 16-bit general register design having approximately 20 instructions and three addressing modes, yet is fully functional as a computer. From its instruction set, the list of 21 operations shown in Table 1 can be derived as a representative minimum working set. If the design includes these operations, it will function as a CPU.

Table 1. Minimal CPU Instruction Set

1.	Load register from memory at immediate address (address in instruction).
2.	Load register from memory at address in a register.
3.	Store register to memory at immediate address (address in instruction).
4.	Store register to memory at address in a register.
5-11.	Move/combine registers: move, negate, invert, add, subtract, AND, OR.
12-13.	Shift: rotate left through sign, rotate right through sign.
14.	Read status register.
15.	Write status register.
16.	Jump absolute: load program counter with immediate address.
17.	Jump register: load program counter with register contents.
18-20.	Jump absolute conditional: if zero result, if sign, if carry.
21.	Jump and save return (Program Counter) in a register.

This instruction set assumes a set of general purpose registers (typically 16 or more in bit-slice designs), a memory which contains both instructions and data and a status register which records the result of register-to-register operations. I/O registers are assumed to be mapped into the memory space so that separate instructions for them are not required.

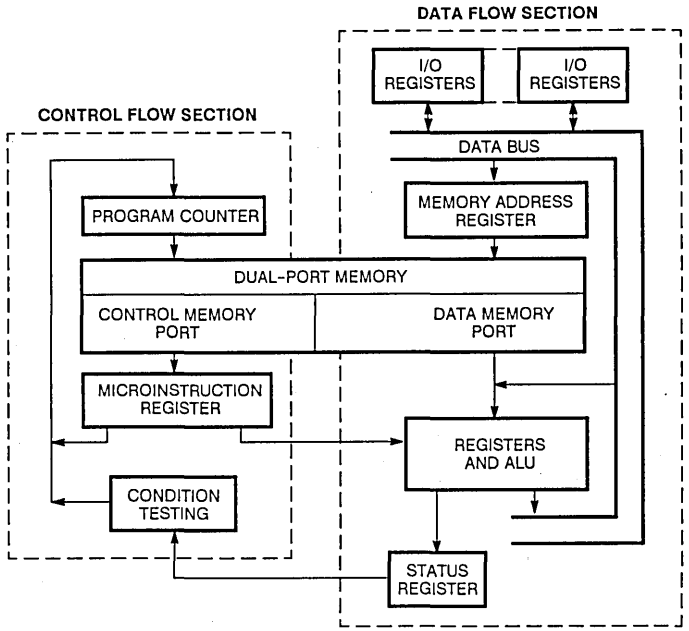

Figure 3. Bit-Slice Controller With Dual-Port Control Store

Some of the above operations are automatically included in bit-slice controllers as a result of staightforward design. The register combination operations are provided by the bit-slice RALUs and the jump operations are commonly required as part of the control flow design. All that is required to complete the set is the ability to transfer registers to and from memory, to save and restore the status register and to save the Program Counter in a register in Jump and Save Return instructions.

Figure 4 shows a block diagram of a general purpose bit-slice controller design, based on the RISC controller architecture in Figure 3, and capable of implementing the minimal instruction set. This is a 16-bit controller design using an IDT49C402 16-bit RALU and a 64-bit instruction word. The control flow section is fully pipelined for maximum speed and uses a simple counter as the Program Counter (PC). As a result, branch execution is delayed by one instruction: the instruction following the branch is executed before the branch takes effect. This method allows maximum speed in the control flow section and is commonly used in RISC designs. A path is provided from the PC to the data inputs of the IDT49C402 for saving the PC in a register during Jump and Save Return operations. Also shown in the block diagram is an initial-load EPROM. This EPROM holds the non-volatile copy of the program to be loaded at power up. A power up flip-flop and some sequencing logic cause the contents of this EPROM to be loaded into the RAM at power up.

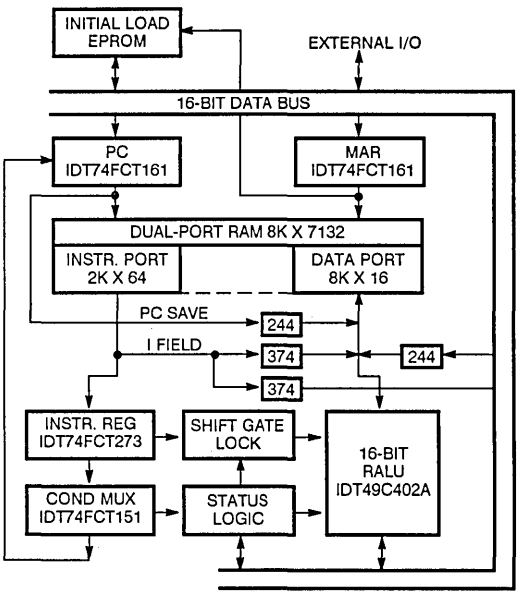

Figure 4. Dual-Port Bit-Slice RISC Controller Design Block Diagram

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In the design in Figure 4, the instructions and data share the same memory. The mapping for instructions and the mapping for data are different, however, as is shown in Figure 5. The eight dual-port RAM chips are mapped as 2K words of 64 bits/word on the instruction port and as 8K words of 16 bits/word on the data port. Each 64-bit instruction word corresponds to four sequential 16-bit data words. The instruction at address 0000 on the instruction port corresponds to locations 0000, 0001, 0002 and 0003 on the data port. On the instruction port, all eight chips are enabled, resulting in 64 bits of instruction output. Only the upper 14 bits of the PC are used to address the RAM so that the address in the PC is consistent with the addressing on the data side. On the data port, the least significant two bits of the address in MAR select the appropriate 16-bit word by selecting the chip enable for the appropriate one of four pairs of chips.

RISC CONTROLLER INSTRUCTION FORMAT

The 64-bit instruction word is shown in Figure 6. Fifty of the 64 bits are used to control the basic data and control flow of the controller and 14 bits are available as additional control bits for the specific controller application. Each 64-bit instruction word from the control port of the RAM is mapped as four 16-bit words on the data memory port. A larger instruction word can be used in the same manner as in microcoded designs. It is convenient if the word width is a power of two, such as 64 or 128 bits, so that there are no gaps in the memory space as seen from the data flow side.

The IDT49C402 is controlled by the A and B fields, I_{0-9}, C_N, Stat Enable field and the Shift Gating field. The A and B fields provide the 6-bit addresses for the A and B register inputs on the IDT49C402. The I_{0-9}, C_N and Stat E_N field provide the 10 control bits to the IDT49C402, the carry-in bit and a status register load enable, respectively, and the Shift Gating field controls the shift-in/shift-out gating for shift operations. The data source for the D_{IN} pins of the IDT49C402 is selected by the D_{IN} field. This field can choose the data bus, the immediate data field or the PC as the data source.

The data bus is controlled by the A and B fields as well, which provide 6-bit select codes for bus read and write operations, respectively, and by the bus read/write, memory write and load MAR bits. The default operation is to gate the data from the IDT49C402 onto the data bus. The load MAR and memory write bits allow writing this data into the memory and/or MAR from the bus. The bus read bit disables the IDT49C402 outputs and gates an I/O register onto the bus as determined by the 6-bit A field. The bus write bit causes bus data to be written into an I/O register selected by the B field.

Branch operations are controlled by the Jump and A fields. The Jump field enables loading of the PC from the bus, which is the branch operation. The A field provides the 6-bit condition select code for conditional branch operations.

The Misc Control field provides 14 bits for direct control of additional devices. This field would typically be used for gates and strobes to additional devices such as parallel multipliers, FIFOs, disk controller chips and other devices which communicate with, and are controlled by, the RISC controller.

IMPLEMENTING THE MINIMAL INSTRUCTION SET

The RISC controller design must now be checked to ensure that it implements each instruction in the minimal instruction set.

Load and Store

Load and Store register operations are done in two instructions: load MAR and load or store register. The load MAR instruction places register data from the IDT49C402 or data from the immediate data field on the bus and enables MAR load. The load register instruction gates memory data into the data inputs of the IDT49C402. The store register instruction gates register data onto the bus and writes it into memory.

Move, Combine and Shift Register

Register-to-register and shift operations are performed directly by the IDT49C402 bit-slice.

Status Register Read/Write

Read and Write Status register operations select the Status Register and bus read and write, respectively.

Jump and Conditional Jump

Jump operations are done by enabling the PC to be loaded from the bus using either immediate or register data for the jump address. Conditional Jump is done by enabling a conditions select multiplexer to conditionally enable the PC load.

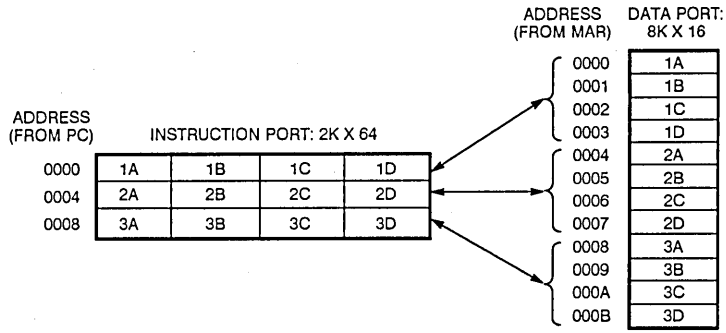
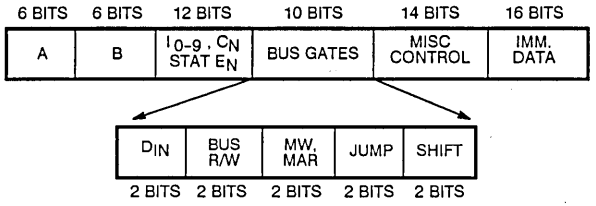


Figure 5. Dual-Port Controller Memory Map



FIELD	FUNCTION
A	402 reg address, bus read select, or jump condition select
B	402 reg address or bus write select
I0-9	49C402 instructions + carry-in
Stat EN	Enable Status reg load
DIN	402 D Bus: Memory, PC, Bus, I field
Bus R/W	Gate Bus read @ A, write @ B
MW, MAR	Memory write enable, ld MAR enable
Jump	Enable PC load, enable condition test
Shift	402 shift/rotate gating
Imm Data	Immediate Data - addresses, etc.
Misc Control	Misc bits for controller functions

Figure 6. Dual-Port Controller Instruction Format

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Jump and Save Return

The Jump and Save Return operation is performed by using the immediate data field to provide the jump address and simultaneously storing the PC in a register selected by the B field. The immediate data field is gated to the bus, the PC is gated to the IDT49C402 data inputs and the IDT49C402 is instructed to perform a D-input-to-register-load operation.

RISC CONTROLLER TIMING

The design in Figure 4 is capable of a 55ns cycle time. A timing diagram for a 55ns cycle time, assuming the 35ns dual-port RAMs, is shown in Figure 7. The critical timing path, in this case, is the data path from the Memory Address Register (MAR) through the data port of the memory into the IDT49C402. If the dual-port RAMs are slower than 35ns, the cycle is extended proportionately.

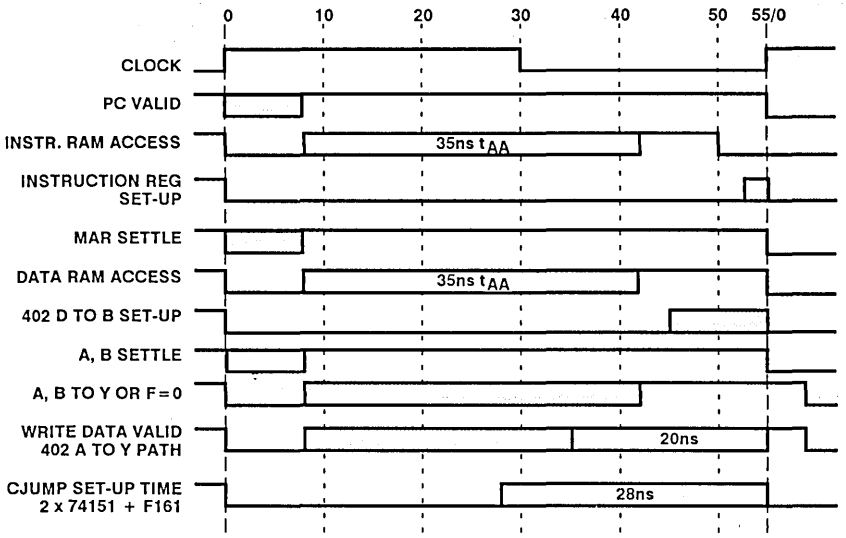

Figure 7. RISC Controller Timing Diagram

Table 2. Critical Path Timing

CONTROL PATH		DATA PATH	
PC settle: FCT161A	6.5ns	MAR settle: FCT161A	6.5ns
RAM Access	35.0	RAM Access	35.0
I reg set-up: FCT374A	2.5	IDT49C402A, Din Set-up	10.0
Total	**44.0ns**	**Total**	**51.5ns**

RISC CONTROLLER APPLICATION

The utility of the RISC controller design approach is that it allows interactive system development, debugging and diagnostic testing. It also provides the potential for high-level language support of the bit-slice design. Powerful interactive access to the RISC controller can be provided by an RS-232 interface and a FORTH language interpreter program. This allows interactive coding and testing of the system, speeding up the test-and-analyze debug cycles. This RS-232 interface can exist on a separate board external to the RISC controller, connected to the bus by a connector on the controller board. No additional hardware is required for access by the designer to the system and this access can allow direct activation and sensing of controller hardware, setting up timing loops for oscilloscope checks and on-line development of routines. If a floppy disk controller is included in the external I/O board, the RISC controller can function as a stand-alone development system in the same fashion as other stand-alone FORTH systems.

The RISC controller's ability to load programs also means that diagnostics can be loaded from the initial load EPROM . The initial load EPROM can hold both the normal control program and various test programs. The controller can load diagnostic programs from the EPROM for board and system test without requiring permanent space for them in the control memory. This allows self-diagnostics at the hardware level with minimum cost impact on the hardware.

SUMMARY

The RISC controller uses high-speed dual-port RAMs to blend the features of a bit-slice controller with the capabilities of a RISC computer, allowing the microinstructions of the bit-slice approach to become the instructions of a computer. This design approach provides all the speed and architectural flexibility of microcoded bit-slice designs, while allowing the use of interactive debugging methods associated with microprocessors to shorten development time.

Integrated Device Technology, Inc.

DUAL-PORT RAMS WITH SEMAPHORE ARBITRATION

APPLICATION NOTE AN-14

by Michael J. Miller

INTRODUCTION

Due to their high bandwidth and message access flexibility, dual-port RAMs are used to link multiple high-performance processors and systems. Integrated Device Technology makes dual-port RAMs of many configurations, all of which consist of one RAM with two sets of address, data and control signals. This allows two processors to share the same block of physical memory in their respective address spaces. The two processors can access data in two memory locations simultaneously and asynchronously. This approach clearly outperforms a discrete parts design where two processors must synchronize through arbitration for access to a bus which is used to access one location at a time in a standard single-port RAM.

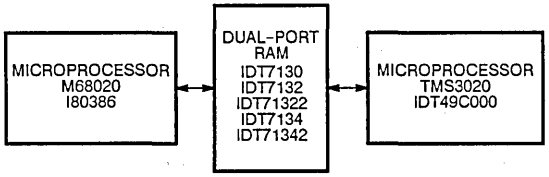

Figure 1. Dual-Port RAMs Link High-Performance Processors

IDT's dual-access approach removes synchronization requirements at the memory's bus access level. Nevertheless, synchronization must be performed at other levels to ensure data integrity and proper system operation. This application note addresses several approaches to solving the mutual exclusion problem and gives a detailed discussion of the semaphore capability provided by the IDT71322 and IDT71342.

Arbitration

Consider a multiple-processor system where each processor has access to the same data. Arbitration schemes are necessary to resolve the situation when multiple processors want the same piece of data at the same time. Different approaches to the arbitration issue have different tradeoffs and are best-suited for different applications. These solutions vary from no arbitration, hardware solutions, and software solutions, to combinations thereof.

Seemingly, the simplest solution is to employ no arbitration at all. This approach works if the application guarantees that two processors will not access the same location simultaneously or, if they do, then the indeterminate results are acceptable. Sometimes handshaking can be employed through I/O ports or interrupt mechanisms. This approach provides a high-performance, low-overhead design but is restricted to certain applications. If arbitration is not required, the IDT7134 can be used. It is a 4K x 8 dual-port RAM with no arbitration. This part can also be used in large dual-port designs where one hardware arbiter is used for a whole array composed of many IDT7134s. The interrupt handshake mechanism can be achieved by using the IDT7130/7140.

Most applications cannot sacrifice data integrity and utilize the dual-port memory as a collection of individual memory locations which require a finite access time. In this case, arbitration at memory location resolution is required. The IDT7130/7132 use an address comparison mechanism which provides a $\overline{\text{BUSY}}$ signal at both sides. When the two processors try to access the very same location, the arbitration asserts the $\overline{\text{BUSY}}$ signal to the processor which attempted access last. When access attempts are within 5ns of each other, a side is chosen arbitrarily. The $\overline{\text{BUSY}}$ outputs are suitable for attachment to the READY inputs of most microprocessors. This approach is very straightforward and flexible and has the benefit that a processor cannot be locked out of the RAM longer than the access period of the other processor.

The features of the IDT7130/7132 that make them a superb solution in many designs may create problems in other applications. The fact that $\overline{\text{BUSY}}$ lines are used and that arbitration resolution is at the level of individual locations can be a major limitation in some instances. Many significant controllers, such as the 8031 and 8051, are not equipped with READY input pins. Of those that are equipped, a penalty is often paid in the higher performance versions if they require "seeing" the $\overline{\text{BUSY}}$ signal faster than the IDT7130/7132 can supply it (16MHz 68020 requires 25ns $\overline{\text{AS}}$ to $\overline{\text{DSACK}}$). In these cases, wasteful wait cycles are required. In other applications, software constraints may require mutual exclusion at the software data structure level rather than at the memory cell location level. For this reason, Integrated Device Technology developed the IDT71342 and IDT71322.

Instead of comparing addresses on every cycle, and occasionally asserting $\overline{\text{BUSY}}$ status, the IDT71342 and IDT71322 employ circuitry to support a software mechanism called semaphores. Here, every memory cycle is equally as short as the next and arbitration is handled at the software level.

The semaphore concept was pioneered by E.N. Dijkstra in 1968. He developed a test and set approach for single processor multi-tasking systems. The task tests a memory location (a semaphore) for a particular value and, on the next cycle, the task sets the same location a unique value. If the semaphore was already set, then the current task knows that another task has access. If the value was not present, then the task knows that it has permission to proceed and all other tasks are blocked because the semaphore is not set. Only one task at a time has permission via the semaphore. Semaphores are used like locks to resources such as disk buffers, message queues, critical code sections, shared access to communication controllers, etc.

Because the test and set operation requires that the two memory accesses are indivisible in time, the IDT7130/7132 will not support semaphores for many processors and systems. This occurs because one processor may test the semaphore and, before it can set it, the other processor might test it, too. In this case, both processors "believe" they have the semaphore. The IDT71342/71322 employs a twist by using set and test. The "set" corresponds to a request and the "test" checks to see if the request was granted. The indivisible double access requirement is avoided because, as soon as a request is made by one processor on one side, the grant

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is blocked on the other side. Some processors support test and set operations through a read/modify/write operation, but the memory bus design must support the processor in such a way that the address and the chip select remain constant. When the test and set instruction is used, arbitration must take place. As will be seen, semaphore operation without hardware busy arbitration has many advantages.

The IDT semaphore scheme employs a software/hardware approach which provides a secure method of resource allocation with the flexibility of software configuration and control and the resolution of hardware. Since there is no hardware relationship between semaphores and dual-port memory locations, the block sizes, locations and semaphore association are defined by the software. The semaphores can also be used to allocate other resources such as I/O devices. This offers the system designer considerable flexibility.

As an example, dual-port RAM might be shared by a disk controller processor and a host processor. When the controller is accessing a buffer in memory (e.g. when writing a sector in a track), the main processor cannot be allowed to interrupt or delay the controller. By setting the semaphore, the controller has exclusive access to the disk buffer. When done,it releases the semaphore and therefore provides access to the disk buffer by the processor on the other side.

Because the processors must test and set a semaphore with multiple bus cycles, the semaphore arbitration scheme has a longer arbitration latency than the address comparison scheme. Since arbitration is most often used for access to multiple locations in memory the overhead can be amortized across multiple accesses. In systems that require mutual exclusion of access to data structures over a period longer than one memory cycle, this tradeoff is irrelevant.

Functional Description of the IDT71342/71322

The IDT71342 is a fast dual-port 4K x 8 CMOS static RAM with semaphore logic, packaged in a 52-pin PLCC and LCC. The IDT71322 is a 2K x 8 dual-port packaged in a 48-pin DIP and a 52-pin PLCC/LCC. The semaphore logic can be used to allocate portions of the dual-port RAM to one side or the other and is used in place of the address arbitration logic used in other dual-port designs. Semaphores are software-controlled. Therefore, this approach provides several advantages including allocation of multiple blocks of arbitrary size and no processor WAIT states or $\overline{BUSY}$ logic.

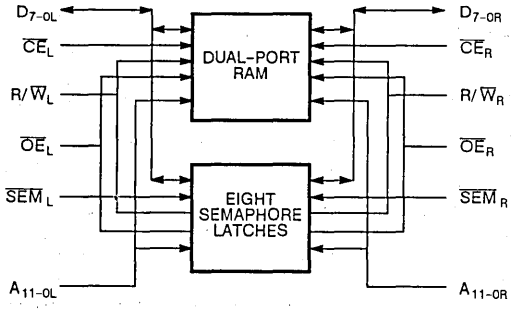


Figure 2. Functional Block Diagram of Dual-Port RAM with Semaphores

Like other IDT dual-port RAMs, the IDT71342/71322 allow access to a common set of RAM cells from two independent ports. Each port is functionally identical to that of a conventional static RAM. Both ports are completely independent and asynchronous in operation. Reading or writing on one port does not affect the operation or timing of read/write operations on the other port. Unlike the IDT7130/7132, the IDT71342/71322 do not employ hardware arbitration which blocks write access. If one port is writing to a location while the other port is reading that same location, the data will change during the read. If both ports attempt to write to the same location at the same time, the result will be some combination of the two data words being written. If both ports are reading, however, there is no interaction because the data does not change.

How the Semaphore Flags Work

The semaphore logic is provided by a set of eight latches. These latches can be used to pass a flag, or token, from one port to the other to indicate that a block of RAM is in use. The internal circuitry prevents the flag from being passed in both directions at the same time. The semaphores provide a hardware assist for a use-assignment method called "token passing allocation". In this method, the state of the semaphore latch is used as a token indicating that a block of RAM is in use. If the processor on the L port wants to use a block of RAM, it attempts to set the latch, requesting the token. The processor then checks the latch to see if it was successful in setting the semaphore. If it was, the processor proceeds to read and/or write in the block. If the processor was not successful in setting the latch, it means that the R port had set if first, has the token and is using the block. The L port then continues to test until it is successful, indicating that the R port has released the token and is no longer using the block.

The semaphore logic is independent of the dual-port RAM. These eight latches can be accessed from either port by enabling the semaphore chip enable ($\overline{SEM}$ = LOW), which is separate from the RAM chip enable. When the semaphore logic is enabled on a port, one of the eight latches can be read or written from that port. The latch is selected by the three least significant address pins for the port and the data for reading and writing uses the D_0 data pin.

A semaphore latch is read or written in the same manner as a RAM cell. The latch is written to a "1" or "0" by activating the semaphore logic enable, selecting the latch with the three least significant address bits, activating the write enable and putting a "1" or "0", respectively, on the D_0 data pin. The latch may be read by activating the semaphore enable, selecting the latch, holding the write enable high and reading the data on D_0. For the user's convenience, all eight of the data lines are set to the same value as D_0 during read. In other words, the data lines will contain all "1"s or all "0"s when D_0 is a "1" or a "0", respectively. In this way, branch zero testing can be employed.

The semaphore read logic latches the readout state of the semaphore flag during the read. This prevents the value seen by the reading port from changing during the read, even though the state of the latch may be changing internally due to write activity on the other port. The latch goes into the hold mode when both semaphore enable and output enable are active. In order to see the latch change, either the semaphore enable or output enable must be disabled, and then enabled. This means that read operations must be cyclic; it is not possible to enable the semaphore and output enable continuously and wait for the latch value being read to change.

The semaphore logic is active low. An access token is requested by writing a "0" to the semaphore latch and is released by writing a "1". To request a token, an attempt to write a "0" to the semaphore is made and the semaphore is read to determine if the "0" was successfully written. If a "0" is read, the token request was granted. If a "1" is read, the request was denied and the other port has the token.

The critical case of semaphore timing occurs when both ports request the token by writing a "0" at the same time. The semaphore logic is specially designed to resolve this problem – if requests are made simultaneously, the logic guarantees that only one side receives the token. In this case, the token assignment will be made arbitrarily to one port or the other.

Figure 2 shows the internal logic circuitry for one semaphore "latch" cell. It is composed of multiple latches and cross-coupled AND gates which serve as an arbiter to guarantee that only one side at a time receives a grant signal. A typical sequence of semaphore operations is listed in Table 1. The D_0 columns represent the logic value that would be read on that side. The "Request F/F"s are the internal flip-flops which store the state of requests.

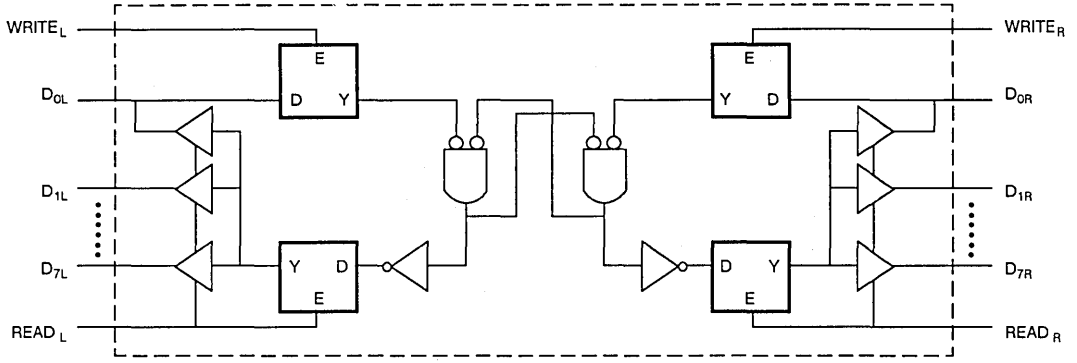


Figure 3. Simplified Diagram of One Semaphore Cell

Function	Left		Right		Status
	DO	Request F/F	Request F/F	DO	
No action	1	1	1	1	Semaphore free
L port writes 0	0	0	1	1	L port has token
R port writes 0	0	0	0	1	No change; L port keeps token
L port writes 1	1	1	0	0	Semaphore freed: R port gets it
R port writes 1	1	1	1	1	Semaphore free
L port writes 0	0	0	1	1	L port has token
L port writes 1	1	1	1	1	Semaphore free

Table 1. Semaphore Function Table

Use of Semaphores

Semaphores provide useful solutions for various problems at both the hardware and software levels. The following selections highlight a few of the semaphore benefits which range from increasing performance to providing functionality not available with other designs.

High-Performance Dual-Port Design

To gain a deeper understanding of the trade-offs between semaphore and non-semaphore dual-port RAM designs, the following example compares both approaches. Dual-port memory system design requires a key awareness of the microprocessor's memory access time requirements. Figure 3 is a read cycle timing diagram of a 20MHz 68020. Two timings are critical: A 45ns address to data size acknowledge ($\overline{DSACK}$) to guarantee no wait states and a 95ns address to data. It is also important to examine a typical design. Figure 4 shows the interface between a single processor and one side of the dual-port. For simplification, the other port interface was omitted from the drawing. This example shows the address bus which is decoded by a comparator (IDT74FCT521A) and an address decoder (IDT74FCT138A). The address interface chooses which dual-port RAM to enable. After the chip select is enabled, chip select address arbitration (only on the IDT7130/7132) and data access can begin.

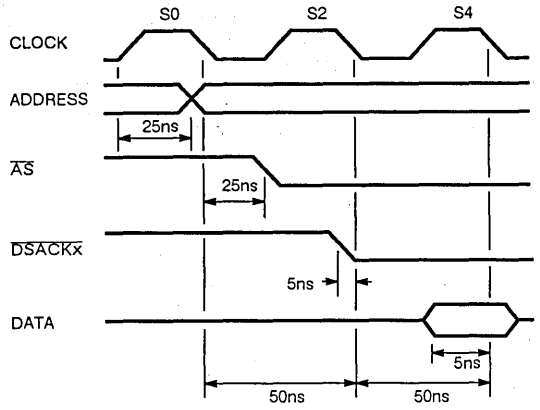


Figure 4. Read Cycle Timing for 20Mhz 68020

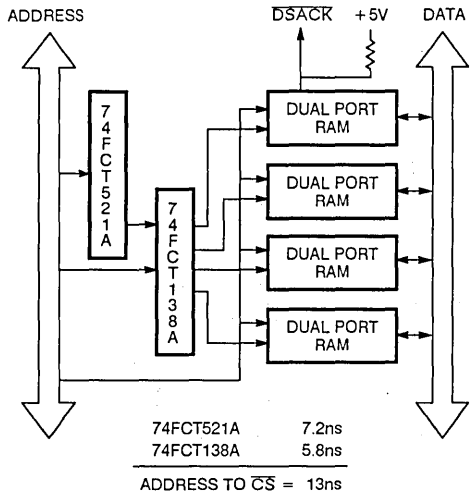


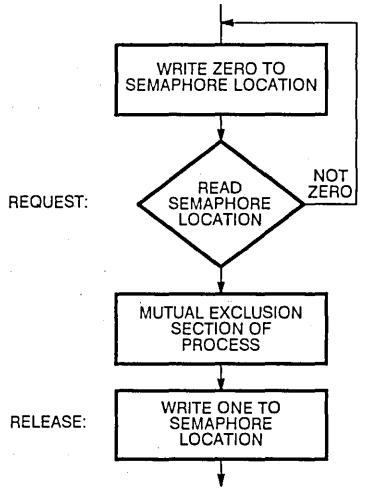
Figure 5. Memory Interface to One Port of a Dual-Port RAM System

In a tightly-coupled system (i.e., the 68020 processor and dual-port are on the same board), chip select can be generated from address in 13ns. In the best case, the data acknowledge is tied to the 68020 through a NAND gate (to include other acknowledges). The NAND gate will introduce another 5ns delay. This leaves 26.9ns to generate the acknowledge ($\overline{DSACK}$) and meet the 5ns setup time to guarantee that a wait state will not be inserted. In a less rigorous design where the dual-port and CPU are on separate boards, 10ns or more may be required for on/off board buffers and bus delay, etc. This leaves 16ns or less to generate acknowledge.

Considering the timing constraints, the designer can choose from several options. In applications which require arbitration resolution to the memory cell level, 26.9ns is not enough time to generate $\overline{DSACK}$ from $\overline{CS}$ using the IDT7130L55. One solution involves adding logic to the $\overline{BUSY}/\overline{DSACK}$ path so that a wait state is always inserted until the dual-port can respond with $\overline{BUSY}$. This will slow down the system whenever the dual-port is accessed. If block arbitration or higher memory cycle performance are required, the designer should utilize the IDT71342/71322. This configuration would only be constrained to the 95ns address to data access time, minus any address and data buffer time. The IDT71342/71322 provides high enough performance for use with the 25MHz 68020. Some software overhead is required for semaphore access but, given the fact that the semaphore arbitration is for a block of locations, the arbitration latency can be amortized across multiple higher speed accesses. Consequently, the semaphore approach provides a higher performance solution if block arbitration is desirable or acceptable.

A Software View of Semaphores

The dictionary defines semaphore as "signaling by flags." A semaphore is implemented as a specialized type of memory location which can be accessed by either processor in a dual-port design. Two different operations are performed on the semaphore: the request operation which attempts to gain access and the release operation which signals the termination of access. These operations are used to guarantee mutual exclusion, meaning that only one processor is accessing a resource at any given time. This occurs from the time a request is granted until the time that the semaphore is released.



Flow Chart 1. Sequence of Operations on Semaphore to Guarantee Mutual Exclusion

A semaphore is chosen which both processors associate with one resource. First the processor requests the semaphore by attempting to write a "0" to the semaphore location. Then it reads the location. If it receives a non-zero value (i.e. a "1"), it loops back and reads the semaphore location again. It will continue to read the location until it receives a "0". The software may be written in such a way that useful work may be performed while waiting. When a "0" is read, the processor can access the resource for as long, and as many times, as desired. The processor must release the semaphore when it is finished with the resource. This is achieved by writing a "1" to the semaphore location.

Using Semaphores at the Software Level

One example of where semaphores might be applied involves two processors working together to generate a video display for animated images. The "MASTER" processor generates a picture layout in the form of a display list. The "SLAVE" processor reads the display list, interprets it and generates an image in a display buffer. As the image is displayed, the video buffer is cleared. The displayed list is re-interpreted and displayed. If the display list is changed, the image appears as though it has moved, giving the illusion of animation.

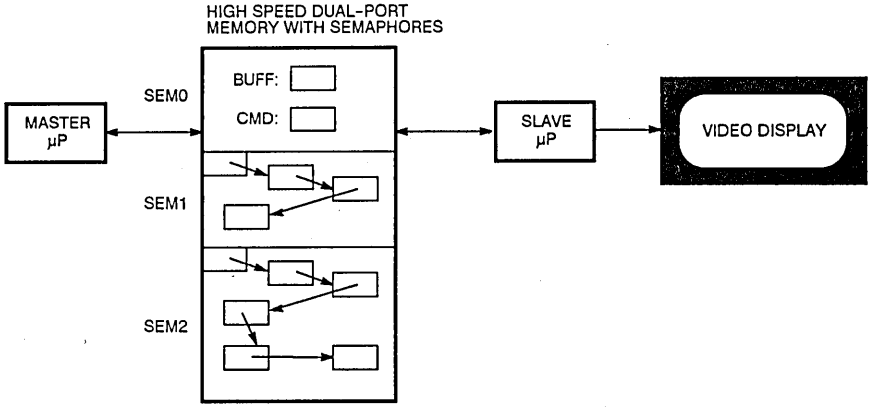


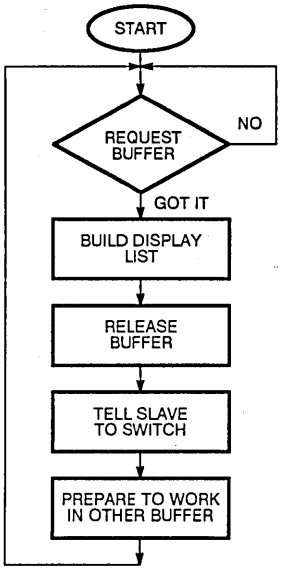
Figure 5. Software Block Diagram of Video Display System for Animation

A dual-port RAM is used to store the display list. The SLAVE interprets one display list repeatedly to generate the display buffer image, while the MASTER generates and updates another display list. The SLAVE processor continuously updates the video display buffer since the buffer is wiped clean when its contents are dumped to the video screen.

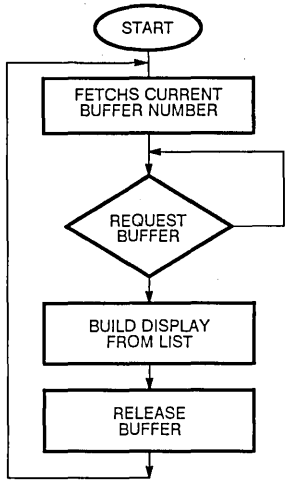
In this particular application, the dual-port RAM is broken up into three areas. The first area contains common information concerning which display list is being accessed and which one is being updated. It is locked with the semaphore SEM0. Two buffers comprise the other areas and are locked by semaphores SEM1 and SEM2. At any given time one buffer is used for the display list currently being interpreted and the other is used for the list being built. The common area stores the pointer which indicates which buffer is being updated.

The key to the effectiveness of this approach lies at the software level. The flow chart for the master processor begins with a buffer request via a semaphore. Once granted, it builds a display list. Then it releases the buffer through the semaphore mechanism. Next it calls a routine to inform the SLAVE processor to switch over to the new buffer. It then loops back to request access to the other buffer.

The SLAVE processor functions by first fetching the current buffer/number. Then it requests the buffer via the semaphore mechanism (involving SEM1 or SEM2). Once the SLAVE gains access to the buffer, it builds the display from the list. After releasing the buffer, it goes back to fetching the current buffer/number. This is necessary because the MASTER processor may have switched buffers. Fetching the current buffer/number requires access to the common area which is achieved by obtaining the semaphore SEM0. After accessing the data, the SLAVE releases SEM0 which allows the MASTER to come in and update the common area.



Flow Chart 2. Sequence of Operations for Master Processor

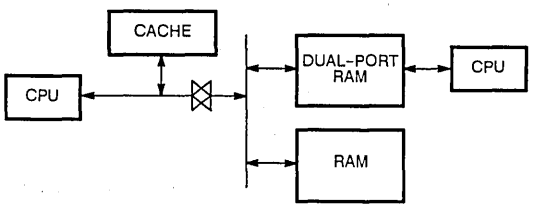


Flow Chart 3. Sequence of Operations for Slave Processor

The software code for the MASTER and SLAVE processors is listed on the following pages. It is in the form of a pseudo-"C" language-type program. The request for a semaphore is made by the WHILE statements accessing a variable called SEM. The semaphore is released by writing a "1" to that variable.

Semaphores and Caches

In high-performance dual-port systems, semaphores can be used with caches to achieve valid data synchronization. The use of caches is an established method of speeding up access between a processor and main memory. Main memory may be slower due to the use of lower cost, higher density DRAMs or system bus latency. The cache operates by monitoring data transfer between the processor and memory. When write operations are performed, the cache remembers the data and location. When a read is performed it compares the address of the request with a list of locations it has data for. If the address matches, the cache supplies the data and aborts the main memory access. If no match occurs, the cache allows the main memory access to proceed and notes the data and location.



Flow Chart 7. Dual-Port RAM in a Cached Memory Environment

One might first assume that the dual-port RAM can always be used with cached memory accesses. However, extra considerations must be made. When data is written to a memory location in dual-port RAM, the cache stores the acquired value and its associated location. The next time that location is read, the cache will register a "match" and bypass reading from the location in dual-port RAM. This might result in an error if a processor on the other port has written new data to the location.

One way to remedy the situation is to put the dual-port RAM into non-cached I/O address space and block data transfer between the dual-port RAM and cached address space where standard RAM exists. To make this approach work, semaphores must be employed to lock a buffer in the dual-port RAM while the data is in the cached RAM. In this way a "check out" procedure can be implemented to ensure data integrity. The semaphore latches must be addressed through non-cached I/O space in order for the request and release mechanism to function correctly.

CONCLUSION

There are a number of ways to handle dual-port RAM arbitration. Choice of the most efficient technique concerns what granularity of address arbitration is required, whether a processor must be locked out of a block of memory for multiple accesses from the other processor and what constraints are imposed by the memory access cycle timing. Semaphores provide an alternative which can result in higher performance systems and provide functions which are not otherwise achievable. The following is a quick summary.

No Busy Logic—Some applications guarantee by definition that the two processors will not access the same locations simultaneously or, if they do, it doesn't matter. The IDT7134 is also ideal for use in large dual-port designs where one arbiter is used for an array of dual-port devices.

Interrupt Logic—Interrupt logic provides a signaling method from one processor to the other to provide a mechanism for handshaking.

Hardware Busy Logic—Hardware busy logic provides the lowest latency overhead when accessing multiple individual unrelated memory locations. The **MASTER/SLAVE** concept was introduced over two years ago by IDT to provide a single arbiter—thus avoiding deadlocks encountered with multiple arbiters—when using more than one dual-port in wide bus applications.

Semaphore Logic—Semaphore logic provides the best overhead tradeoff when accessing a block of data comprised of multiple related locations. This facility may also be required in high-performance applications where one of the processors does not have a ready/busy input or the overhead of wait states cannot be tolerated.

Semaphores provide a mechanism for one processor to bar the other processor from seeing an incomplete update of a block of data. This is achieved through a software mechanism supported by on-chip circuitry which provides a test and set facility that arbitrates between simultaneous requests.

CODE FOR MASTER PROCESSOR

```
MAIN   ( )       {
         /*        code to initialize */

       FOREVER   {
             SEM (CUR_BUF):= 0
             UNTIL (SEM (CUR_BUF)  = 0);          /*request */
             BUILD_DISPLAY (CUR_BUFF);            /*Build new display list*/
             SEM (CUR_BUFF):= 1                   /*release */
             SWITCH_BUFF (CUR_BUFF);
             IF (CUR -= BUFF = 1)
                   CUR_BUFF:= 2;
             else  CUR_BUFF:= 1;
             }
       }                                          /*end MAIN*/

SWITCH_BUFF (NBUFF) {
       SEMO:= 0
       UNTIL (SEMO = 0);   /*request*/
       BUFF:= NBUFF;
       CMD:= NEW;
       SEM:= 1;                        /*release*/
       RETURN ( )
       }
```

CODE FOR SLAVE PROCESSOR

```
MAIN ( )   {
       FOREVER   {
             CUR_BUFF:= FETCH_BUFF ( );
             PROCESS (CUR_BUFF);
              }
       }

FETCH_BUFF ( )   {
       SEM 0:= 0;
       UNTIL (SEMO = 0);                    /*request*/
       A BUFF:= BUFF;
       CMD:= OLD;
       RETURN (ABUFF);
       SEMO:= 1;                            /*release*/
       }

PROCESS (BUFF)   {
       SEM (BUFF):= 0;
       UNTIL (SEM (BUFF)  = 0);             /*request*/
         .   REFRESH (BUFF):          /*code to refresh display*/
       SEM (BUFF):= 1;                      /*release*/
       }
```

Integrated Device Technology, Inc.

USING THE IDT7050/IDT7052 FourPort™ SRAMS IN DSP AND MATRIX PROCESSING APPLICATIONS

APPLICATION NOTE AN-42

By Tao Lin, Julie Lin, and Yupling Chung

INTRODUCTION

Most digital signal processing (DSP) algorithms have inherent parallelism and may be pipelined. Usually, these algorithms are computation intensive. In real-time applications, multiprocessor or parallel distributed processor systems are commonly used to implement these DSP algorithms. In these types of systems it is necessary for different processors to randomly and independently access different locations at the same time in the same memory space. The IDT7050 (1Kx8) and IDT7052 (2Kx8) FourPort SRAMs are powerful devices to efficiently and compactly implement the memory space in these applications. Moreover, the IDT7050 and IDT7052 can increase the speed of these types of systems since the FourPort SRAMs are fast as conventional 1-port SRAMs and eliminate the complex glue logic which introduces extra delay in these systems. In this application note, we will demonstrate some examples of using the IDT7052 to implement a high performance FFT processor and a matrix multiplication engine.

USING THE IDT7052 IN AN FFT PROCESSOR

The IDT7052 FourPort SRAM can dramatically simplify the design of a high-speed pipelined FFT processor. The basic operation of any FFT algorithm is the butterfly computation:

$$G = C + e^{j\Omega} \cdot D$$
$$H = C - e^{j\Omega} \cdot D \qquad (1\text{-}1)$$

where C, D, G, and H are complex numbers. Figure 1 shows the signal flow graph of the butterfly with one complex multiplication and two complex additions. Given N = 2L input data samples x(0), x(1)....., x(N-1), the FFT algorithm performs the Discrete Fourier Transform on the input data to obtain the output data X(0), X(1)....., X(N-1) in L stages of computation. Each stage consists of N/2 butterfly operations. There are two basic versions of the FFT algorithm: decimation-in-time (DIT) and decimation-in-frequency (DIF). Each version of the algorithm can be implemented using two schemes: not-in-place computation and in-place computation. A detailed discussion of the FFT algorithm and its implementations is given in (1).

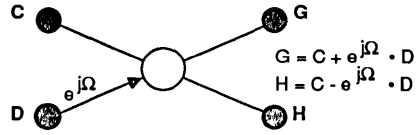


Figure 1. The signal flow graph of the butterfly

Figure 2 shows the signal flow graph of the not-in-place computation of the DIT FFT algorithm for N = 8(L=3). A close look at Figure 2 will reveal the major strength of the not-in-place scheme. The signal paths from the initial inputs to the first intermediary step are repeated between the first and second intermediary steps, and again between the second and third. This means that three stages have identical data access sequence. Therefore, the address generator can be very easily implemented using the IDT7381/83, as compared with the in-place scheme where more complex logic is required to generate the addresses. On the other hand, from Figure 2 it is obvious that in each stage of computation the output data is not in the same order as the input data. For example, in the first stage the first and second inputs x(0) and x(1) will go to the first and fifth locations after the butterfly operation. Therefore, two separate buffers are needed to temporarily store the input and output data in each stage computation.

A conventional implementation of the input and output buffers uses two sets of dual-port SRAMs as illustrated in Figure 3. Suppose the input data is already loaded into Buffer 1. Then, in the first stage of computation the butterfly unit takes data from Buffer 1 and then loads the results into Buffer 2. In the second stage of computation the butterfly unit takes data from Buffer 2 and then loads the results into Buffer 1, and so on. To switch between these two buffers, glue logic such as multiplexers and tri-state buffers are necessary as shown in Figure 3. These devices not only occupy board space but also introduce extra delay in the data path thus, decreasing the system performance. It must be noted that C, D, G, H, and $e^{j\Omega}$ in Figure 3 are all complex numbers. Therefore, physically two groups of memories and buses are needed to store and transmit the real part and the imaginary part separately.

The IDT7052 FourPort SRAM provides a much simpler and more efficient way to implement the input and output buffers as shown in Figure 4. In this implementation, the input buffer and output buffer are merged into a single memory space. Since each of the four ports can access the whole memory space, two of them can be dedicated to sending the data C and D to the butterfly unit and the other two can be dedicated to receiving the results G and H from the butterfly unit. In this way, all glue logic can be eliminated and the system performance is greatly improved.

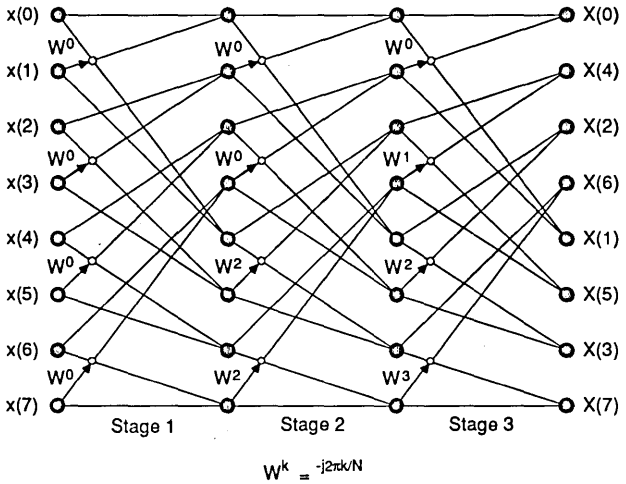


Figure 2. Signal Flow Graph of Not-In-Place Decimation-In-Time FFT for N=8

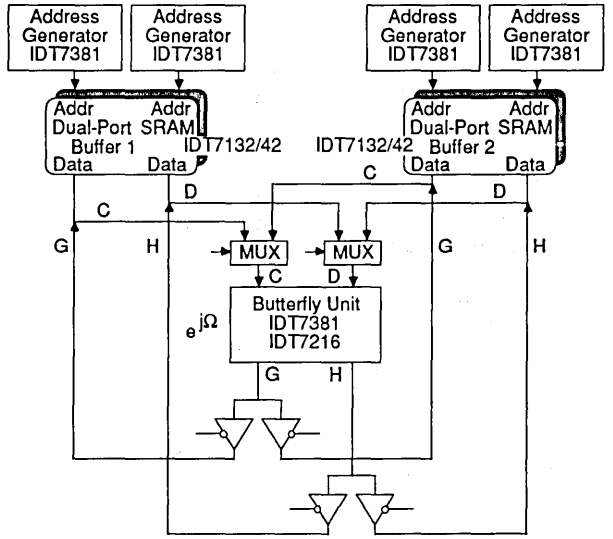


Figure 2. I/O Buffers Implemented by Two Sets of Dual-Port SRAM

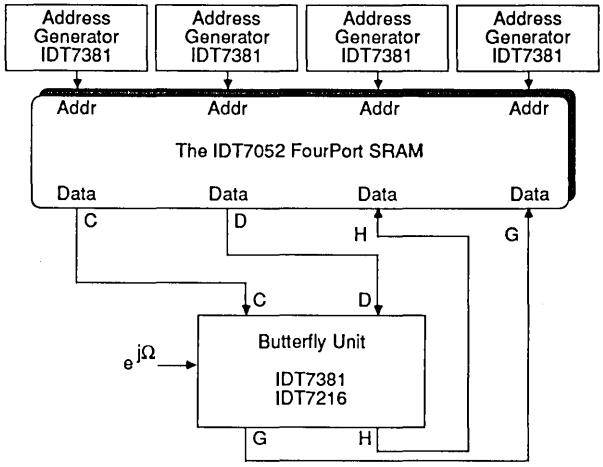


Figure 4. I/O Buffer Implemented By The IDT7052 FourPort SRAM

USING THE IDT7052 IN A MATRIX MULTIPLICATION ENGINE FOR GRAPHICS AND DSP

Matrix multiplication is one of the most often used operations in DSP algorithms. In addition, matrix multiplication is the basic operation at the heart of computer graphics. For example, changing the position, orientation, and size of objects in a drawing requires a geometrical transformation **M** which is generally represented by a series of matrix multiplications.

$$M = M_1 \cdot M_2 \cdot M_3 \cdot \ldots \cdot M_n \qquad (2\text{-}1)$$

where M_1 is a scaling, translation, or rotation matrix.

In high performance systems, a matrix multiplication engine (MME) is necessary to facilitate the operation. A typical pipelined MME has the architecture shown in Figure 5 [2]. Since the MME operates in a pipelined manner, three sets of 1-port memory (IDT6116 2Kx8 SRAMs) are needed to store the multiplicand matrix **A**, multiplier matrix **B**, and the product matrix **C** = **A**•**B**. The matrices **A** and **B** are preloaded into the two 1-port SRAMs from the main memory or a peripheral. The MME then performs the matrix multiplication and loads the product matrix **C** into the third 1-port SRAM. Finally, the multiplication result is sent back to the main memory or the peripheral. This implementation has two drawbacks:

1. Three separate sets of SRAMs are needed. This results in a high chip count and a complicated interface to the system bus.
2. The arithmetic unit (IDT7210) of the MME is sitting idle when the data is transferred between the memory buffers and the system main memory. This dramatically decreases the system performance especially when the MME executes a series of matrix multiplications as given in (2-1).

Now, with the advent of the IDT7052, system designers can considerably improve the performance of the MME by using the FourPort single-chip SRAM instead of the 1-port SRAM. As shown in Figure 6, the new implementation reduces the chip count and simplifies the interface between the MME and the other part of the system. Moreover, when executing a series of matrix multiplications as given in (2-1), the MME is able to perform the arithmetic operation and the data transfer in parallel, as illustrated in Figure 7. First, the matrices M_1 and M_2 are loaded into the FourPort SRAM. Then, while the arithmetic unit performs the operation $M_1 \cdot M \rightarrow M$, a new matrix M_3 can be loaded into an unused area of the FourPort SRAM through the 4-th I/O port. Then, the MME will perform the multiplication $M \cdot M_3$ and the result will be stored in the location originally occupied by M_1. At the same time a new matrix M_4 can be loaded into the FourPort SRAM to replace M_2 and so on. The operation sequence of the two implementations is shown in Figure 8, where t_L is the time to load a matrix into the IDT7052, t_E is the time for the arithmetic unit to perform a matrix multiplication, and t_M is the maximum of t_L and t_E. It can be readily seen from Figure 8, where the total time to execute the operation given in (2-1) is $t_L+(n-1)\cdot(t_L+t_E)$ when conventional 1-port SRAMs are used. On the other hand, the total time is $2t_L+(n-1)\cdot t_M$ when the IDT7052 FourPort SRAM is used. If we make t_L and t_E almost equal to each other then we can almost double the system performance.

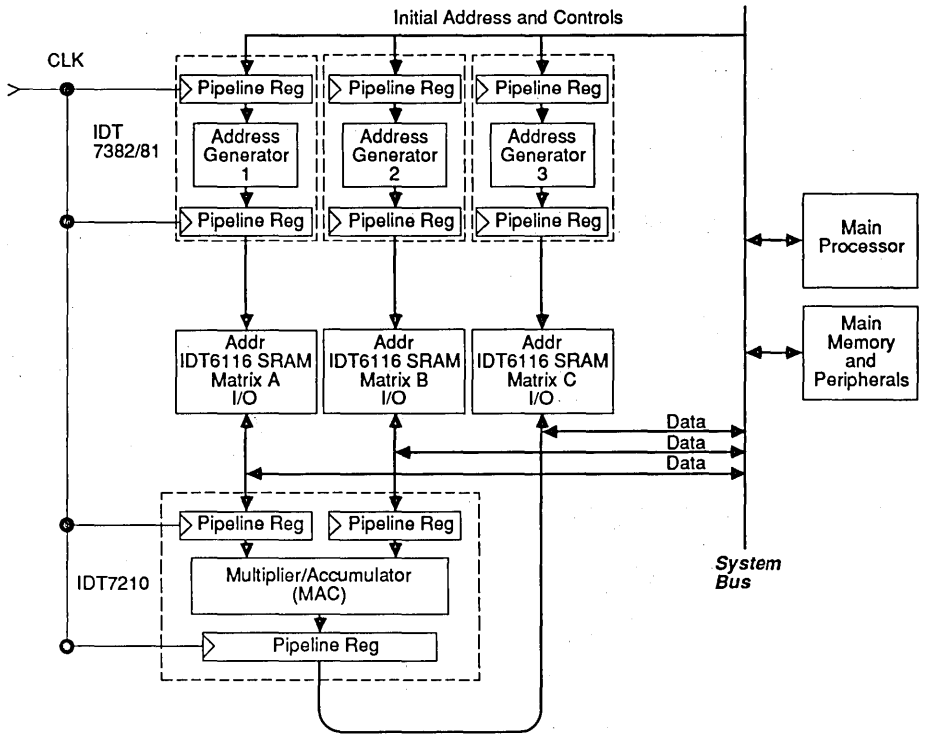


Figure 5. Implementation of Matrix Multiplication Engine Using 1-Port SRAMs

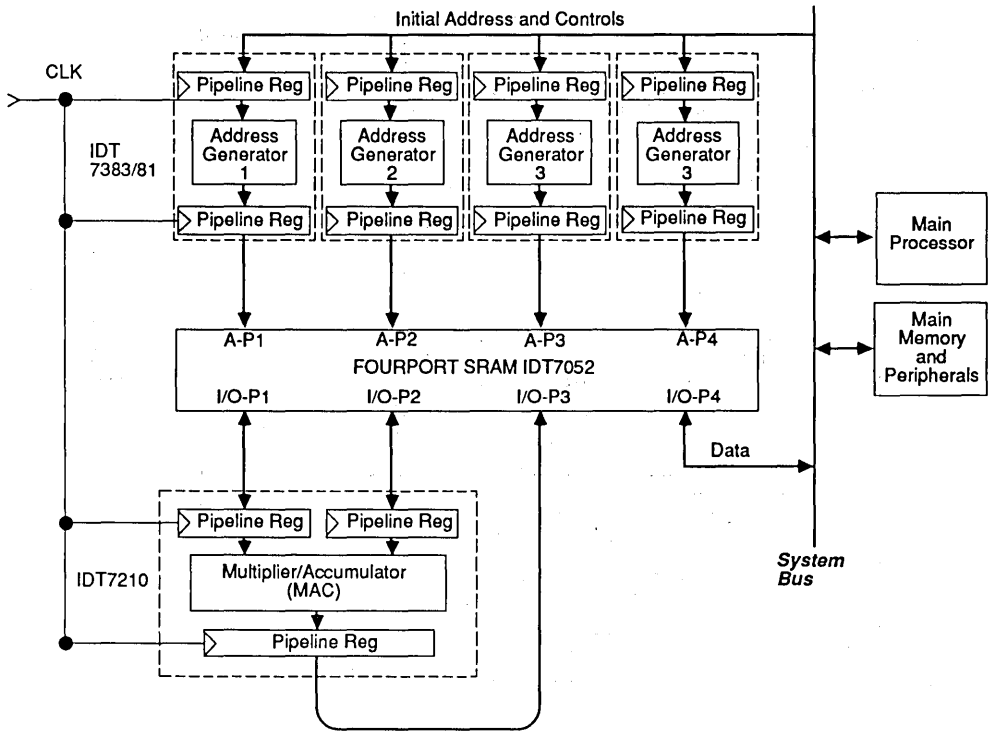


Figure 6. New Implementation of Matrix Multiplication Engine Using The IDT7052 FourPort SRAM

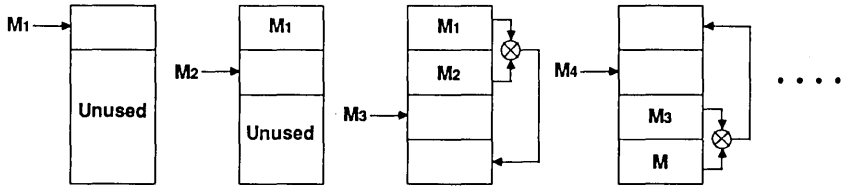
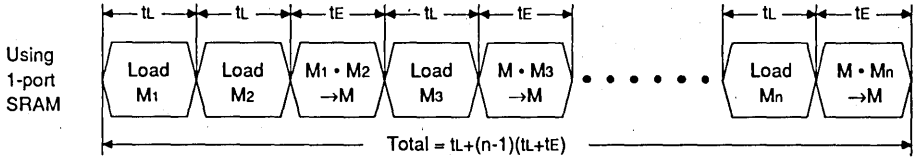
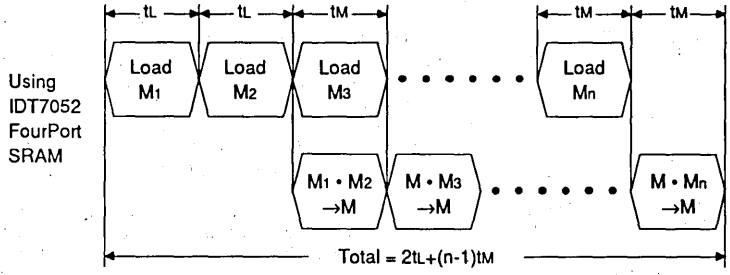


Figure 7. Using FourPort SRAMs, the MME Can Perform Arithmetic Operation and Data Transfer In Parallel



(a) Using 1-port SRAMs, the arithmetic operation and the data transfer are executed alternately.



(b) Using FourPort SRAMs, the arithmetic operation and the data transfer are executed in parallel.

Figure 8. MME Operation Sequence of the Two Implementations

CONCLUSIONS

In this application note we have demonstrated some fundamental architectures using the IDT7052 to implement DSP and matrix algorithms. Since DSP algorithms cover a wide range of applications, there are many more architectures in which the IDT7052 FourPort SRAM can be used. The 2Kx8 FourPort SRAM and other members in the FourPort SRAM family give system designers greater opportunity and flexibility to improve system performance. The hardware designs that result tend to be far less specialized and lend themselves to new tasks with fewer hardware changes.

REFERENCES

(1) Julie Lin and Danh Le Ngoc, "High-performance fixed-point Fast Fourier Transform processor," IDT application note AN-23.
(2) Yuping Chung, "Address generator in matrix unit operation engine," IDT application note AN-35.

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Integrated Device Technology, Inc.

THE IDT FourPort™ RAM FACILITATES MULTIPROCESSOR DESIGNS

APPLICATION NOTE AN-43

By Robert Stodleck

THE IDT FourPort RAM

Serving as both a complex four bus interconnect network and fast "parallel" memory, the IDT FourPort RAM can greatly facilitate the creation of multiprocessor and multi-ALU systems to accelerate DSP, graphics, control and other tasks that involve large vector processing tasks.

Memory architectures based on single-port RAM allow only one device to access a memory array at one time. Hardware designed to accelerate computing processes by utilizing parallelism, or pipelining with single-port memory tend to require architectures that are either complex, specialized, or both. The advent of a fast FourPort single chip RAM greatly simplifies the task of creating generalized small multiprocessor or multi-ALU systems to accelerate a variety of vector algorithms.

Potential applications include dedicated real-time multiprocessor systems for control, graphics, and DSP systems, as well as general purpose vector co-processors to assist general purpose computers. Vector processing means any computing operation with a large number of operations that may be executed in parallel by multiple processors. In these applications the FourPort RAM serves both as a fast static RAM and as the interconnect network between processors working on a common data set.

Imagine a static RAM that allows four processors to randomly and asynchronously read or write four locations at a time in the same RAM array. For processes that can be executed in parallel, four processors can be programmed to operate simultaneously on different parts of a data set stored in the FourPort RAM. If data is being generated at different rates than it is being used, software controlled buffers can be created at will, temporarily storing data passing from one processor to the next. The buffering minimizes the time lost in handshaking between processors. Four way fully random accessibility avoids hardware imposed algorithmic constraints.

The IDT FourPort RAM has precisely these characteristics. There are only two constraints on the access patterns allowed in the FourPort. Two devices cannot write to the same address location in the RAM at the same time, since simultaneous multiple writes to any one multiport memory location may corrupt the data in that RAM location. Also, a device cannot read an address location that is being written, to avoid having the read occur when the output data is changing. There are no other restrictions on access patterns.

As it turns out address collisions are usually prohibited by the logical sequencing requirements of software, and the time lost in avoiding address collisions is often minimal. Most of the time all processors have essentially free read and write access to the memory.

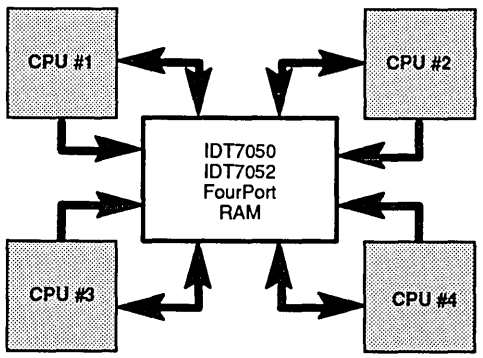

Figure 1. The IDT7052 FourPort RAM allows four simultaneous memory accesses to independent addresses a 2K or 1K x 8-bit memory array. It serves both as a interconnect network and as fast static RAM

FourPort RAM BASED MULTIPROCESSOR ARRAYS FOR VECTOR OPERATIONS

The FourPort RAM is both a storage and communications media. As a communications media it has little, and in some cases zero handshaking or arbitration overhead. A processing device may be able to store results in a multiport memory and spend little or no time signaling the next device to receive the results. As a communications media it also has very high bandwidth. These characteristics make the IDT7050 and the IDT7052 a ideal memory for connecting multi-element and multiprocessor computer architectures (see Figure 2).

A multiprocessor system can be created using almost any existing microprocessor system. Since the hardware interface of the FourPort RAM to the processors is that of a simple static RAM, it can be connected transparently to almost any existing system. Control signals as well as data can be handled via the RAM. Thus, microprocessor boards that were designed for entirely different applications can be used in a multiprocessor array.

FourPort is a trademark of Integrated Device Technology, Inc.

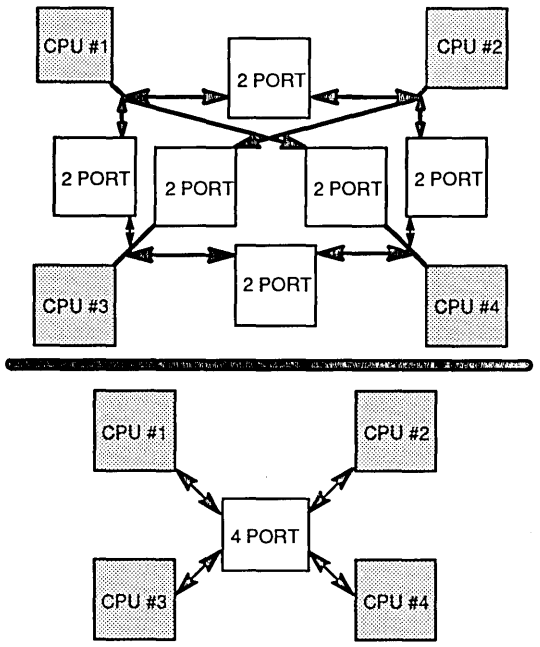

Figure 2. FourPort RAM Interconnection advantages over Dual-Port RAM. The processors in both figures are inter connected with a latency of one memory access. This efficiency requires 6 separate Dual–Port RAMs but only 1 FourPort RAM

AN OVERVIEW OF THE OPERATION OF A MULTIPORT RAM BASED MULTI–PROCESSOR WITH A MULTIPORT RAM BASED CONTROL SYSTEM

Processors sharing multiport memory must avoid writing into memory locations that are simultaneously being read or written from another port. This is usually accomplished by address range segregation. That is, at any one moment processor "A" is prevented from writing to multiport memory locations that processor "B" is accessing from another port. Hardware interrupts, hardware semaphores and stalling processors with hardware busy logic are hardware based methods of controlling the accesses of processors to multiport RAM. It is also possible to control the processors in a multiprocessor array via the common RAM interface. This results in an essentially software–only control system. The control algorithms for a multiport RAM based multiprocessor array are different than those for a multiprocessor array based on single port RAM. This section describes an example of a control protocol for a multiport RAM based multiprocessor array.

Access coordination in multiport RAM based multiprocessors, overlaps with the more familiar task of process coordination in a multiprocessor and uses the same control schemes. In a single master system, the master determines the address ranges being used by all processors. This avoids the problems of arbitrating for resources. In small embedded systems, running algorithms of limited complexity, the software can be tuned so that software–only control approaches have little or no detrimental effect on overall performance. Such systems are more easily debugged if a simple single master control arrangement is used. In this section of this application note we will discuss a single master example.

In a master/slave array, the master controls all the actions of the slaves. The slaves must either have local program store in RAM or ROM or be operating out of the FourPort RAM. Each processor must have a unique ID code to be able to identify the unique command location where it is to receive its commands from the master. This can be achieved, for example, by supplying a unique firmware ID code via individual PROMs, PALs or readable DIP switches for each processor. A number of other approaches are possible.

Each slave command has a corresponding op–code. The slaves poll their command locations looking for new command opcodes. For example finding a "0" in a command location may imply no operation is requested from the slave etc. The commands can be anything that the slave processors have been programmed to do. Appropriate commands might be, multiply data values at locations 000H to 7FFH with the corresponding coefficients at locations 800H to FFFH, or multiply data values at locations 000H to 7FFH with the value at location 800H, etc. Thus, with a few memory accesses, the master processor can trigger and control lengthy slave processor operations.

MASTER/SLAVE CONTROL PROTOCOL FOR A MULTIPORT RAM BASED PROCESSOR ARRAY

A command protocol is the set of rules for passing commands from the master to the slaves. In a software–only control system, all processors must be aware that writes to certain command locations are forbidden, or forbidden without "permission" from the current owner (see Figure 4). In general, a process is given a variable address range to operate in. The command protocol, on the other hand, uses fixed address locations.

The master of an array of processors can tell slave processor #1 to execute a command "n", by writing the command opcode corresponding to command "n" to the slave processor's command location. Parameters for the process, such as constants, or the assigned address range, are placed in reserved locations prior to starting the process that will use them.

There are four problems that a multiport RAM based command protocol must solve:

1. Write–write conflicts must be avoided in the control locations.
2. Read–write synchronization problems must be avoided in the control locations.
3. The master must not issue a new command out of sequence, i.e. the slave has to acknowledge readiness to execute a new command.
4. A slave must execute each command only one time.

Figure 3 shows flow charts for a protocol that allows a master to control slaves and slaves to receive commands without risk of violating these four rules.

All slaves have unique command locations in RAM. If the reads and writes to the command locations are asynchronous, command locations must always be read at least twice. The two read results are then compared and discarded if they do not match. In this way, command data that may have been changing during the read operation, and therefore may have been read incorrectly, is discarded.

Before issuing any command, the master first reads a slave's "command" location. If the value read indicates that the slave is ready, the master places the slave's command op–code in that same command location. The slave must signal readiness for new commands by placing a "no–op/ready" value in the command location. The "'no–op/ready" flag value is interpreted as a "ready–for new–command" flag by the master, and a "no–operation" command by the slave.

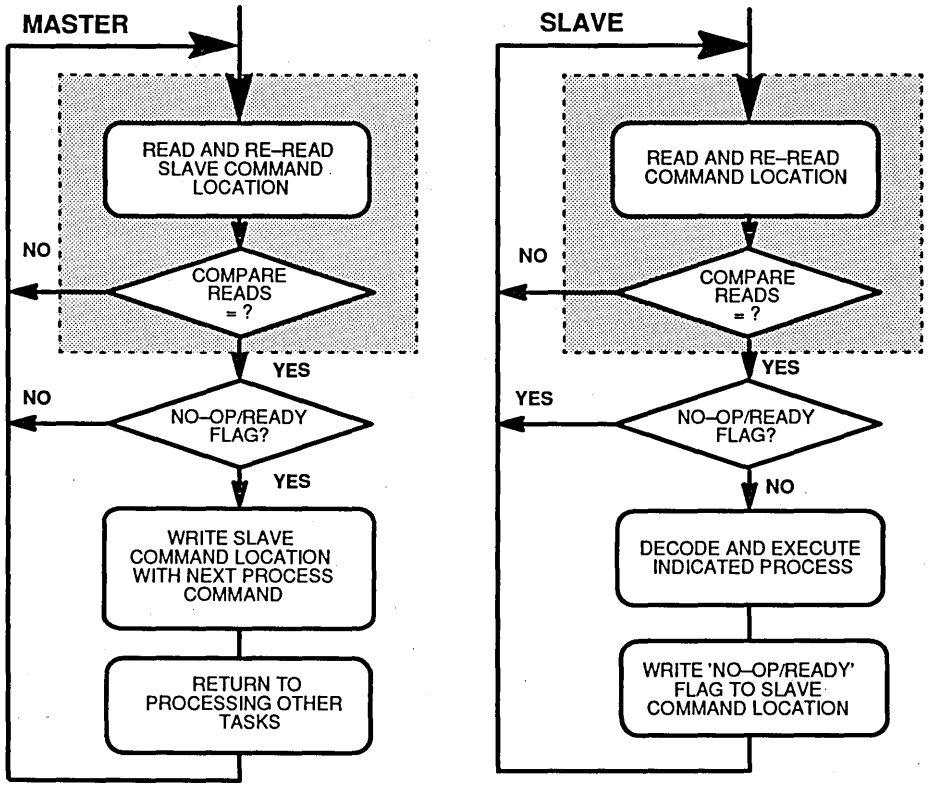

Figure 3. Flow charts for a master–slave software–only command protocol for a multiport RAM based multiprocessor. In unsynchronized systems (see shaded boxes) all commands must be read at least twice with the same result before the command keyword can be assumed to be valid.

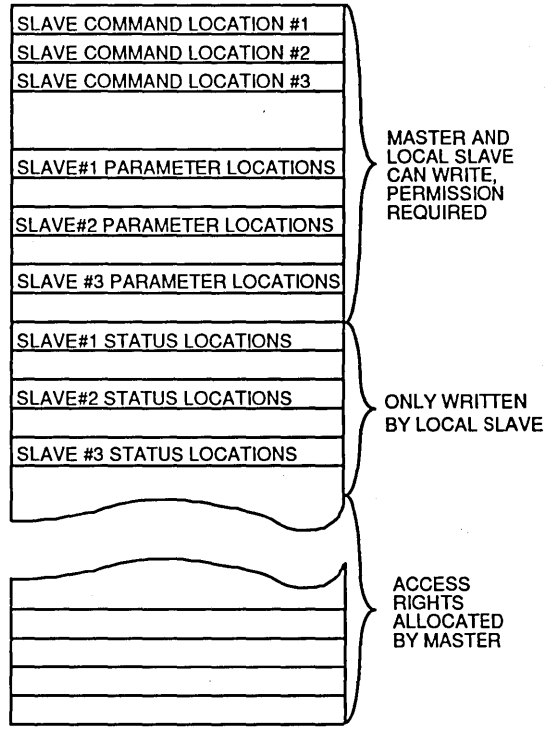

Figure 4. Write Access Allocations

Having to wait for a "ready" signal from the slave prevents the master from issuing new commands out of sequence. Conversely, by signaling "ready" in this way, the slave is also clearing the old commands from the command location. This prevents the slave from later accidently re-reading and re-executing an old command. The command locations are written alternately by the master and the designated slave, but the protocol prevents simultaneous writes that might destroy the data in the RAM location. By using the same location for both the master's command and the slave's ready indication, synchronization problems caused by differences in the memory cycle rates of different processors can also be avoided.

All slaves should also have unique slave status locations in RAM where the master looks for slave status information. The status locations are writable by the slave only. Copious use of reserved slave status locations is essential for the benefit of the programmer trying to debug untested software.

The slave may also signal "done" by writing a "done" flag to a slave status location. The meaning of "done" is that the results of the last operation are ready for use. Keep in mind that "done" is a different signal than "ready". "Ready" implies that the master can post the next command and return to executing other tasks. Depending on the overall algorithm the master is controlling, the master may write a new command as soon as "ready" is signaled, or it may need to wait until "done" is signaled also. It cannot merely check for a "done" signal before issuing a new command. To do so would make it possible to issue new commands out of sequence, based on stale "done" signals.

INITIALIZATION

Since multiport RAM is the control interface, the RAM command locations must be initialized prior to starting the execution of the slaves. One way this can be handled is by delaying the reset pulses to the slaves while the master initializes RAM. Alternatively, after reset, the master can issue a known sequence of commands that frees the slaves from a special start up routine.

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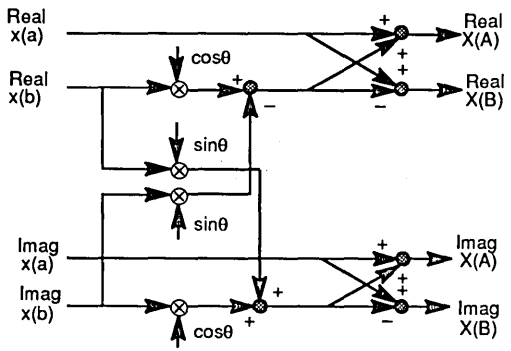

Real X(A) = Real x(a) + (Real x(b) • cos θ – Imag x(b) • sin θ)
Real X(B) = Real x(a) – (Real x(b) • cos θ – Imag x(b) • sin θ)
Imag X(A) = Imag x(a) + (Imag x(b) • cos θ + Real x(b) • sin θ)
Imag X(B) = Imag x(a) – (Imag x(b) • cos θ + Real x(b) • sin θ)

Figure 5. Flow Diagram for Calculating One FFT Butterfly. Each 'X' pattern shown in Figure 6 represents one such "Butterfly". Each end point in Figure 6 represents a complex pair of numbers input or output to or from a "Butterfly". The sine and cosine factors are sometimes called "Twiddle Factors". The angles used for calculating the Twiddle Factors for each Butterfly are shown in Figure 6

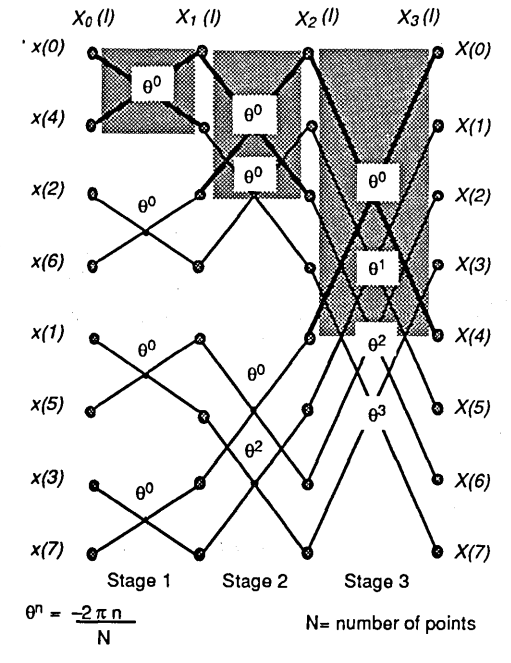

Figure 6. Overview of the "Butterfly" calculations for an 8 Point FFT. To complete this 8 Point FFT requires 3 stages of Butterflies (2^3= 8). A 1K FFT has 10 stages or levels (2^{10}= 1K). The indexes of x(n), the input sequence, are shown out of sequence for graphical clarity. Each stage in this figure has 4 Butterflies

OUTLINE OF A DIGITAL SIGNAL PROCESSING EXAMPLE

Basic DSP algorithms such as the FFT can utilize high degrees of parallelism and provide good examples of vector algorithms. The access patterns of the processor doing such an algorithm are complex and the data sets are usually small enough to fit comfortably in a multiport RAM array. Analyzing how the FFT will be processed provides a good example of the advantages of a multiport RAM based multiprocessing environment.

The objective of our example task is to translate a time series of data values into their frequency domain representation: i.e. execute a fast Fourier transform, as quickly as possible. This is a common process step in a number of systems for interpreting data from things as diverse as military radar to medical CAT scans. It is also a relatively well known algorithm among many contemporary electrical engineers, and so makes a good example for our system.

Our objective algorithm could be run on a single processor. The object of the FourPort RAM based multiprocessor arrangement is to multiply the speed of our computational process without resorting to a specialized and more expensive architecture.

The generality of this architecture implies that it can be applied to a variety of computationally involved tasks. The generality of this architecture also means that there are often a number of ways a programmer can attack a specific problem. The intent of this example is merely to illustrate one approach, not to fully optimize an algorithm.

LOAD BALANCING

The FFT calculations can be flow graphed. When they are, they appear as a repetitive array of calculations (Figure 6) of a particular set of four equations. This set of four equations is called a 'butterfly' for the appearance of its flow graph (Figure 5). The inputs and outputs are series of complex numbers.

A common bench mark of processor performance is a 1K FFT. A quick glance at the equations to be calculated shows why multiple processors are desirable for such a task. If we assume that 1024 real and 1024 imaginary data values have been loaded in the four port memory, there are now 2048 multiplications to be done as a first step. All these multiplications could be done simultaneously. Next there are 1024 additions followed by another 2048 additions to complete the first stage of FFT butterflies. Again, all of operations at any one of these three steps could be done simultaneously. For a 1K FFT there are 10 stages of butterflies.

Processing on one stage of the FFT must be completed before processing on the next stage can begin. Each processor is given an address range of FFT butterfly input data to process for each stage of FFT butterflies. A sine table is required for calculation of the FFT "twiddle" factors. This can be stored in the four port memory and, therefore, will always be available to all processors. Calculation of the "twiddle" factors is a matter of calculating the addresses used in the sine look up table. (See Figure 6 for the angle calculations).

For efficiency, the computational load between processors must be balanced. Since there are hundreds or thousands of operations that may be done in parallel at each stage of the FFT, task partitioning is a matter of assigning each processor an appropriate number of "butterflies" to work on to achieve an equity of loading.

Since the minimal FFT tasks are easily divided between the processors, and the FourPort RAM all but prevents inter–processor data transfer conflicts, the four processors in this example can be kept busy most of time.

Since there are so many tasks that can be done in parallel, other types of tasks can be included without seriously upsetting the balance. For example, if one processor is being used to handle I/O and input conditioning tasks, then it can be assigned to do fewer

butterfly calculations than the other processors. If the work load of all the processors can be balanced, the net speed advantage of this four processor array, can then in fact be close to 4 times that of a single processor.

A TMS320C2x HARDWARE INTERFACE EXAMPLE

TI's TMS320 single chip DSP processors are particularly well suited for embedded numerical processing. An example interface is shown in Figure 7. The internal RAM and ROM of the TMS320 can be used for temporary data storage and program memory, making the FourPort RAM the only external RAM required in a processor array. The FourPort RAM also cascades in depth and width as easily as a standard single port RAM. The interface shown in Figure 7 would typically require 30ns RAMs for a 20Mhz TMS320C2x type processor.

The TMS320C20 and TMS320C25 also include a "sync" pin that facilitates synchronizing the internal clock phases of multiple processors at reset. In synchronous TMS320C2x arrays, this guarantees that memory accesses are in phase with each other and there are no partial clock phase memory access collisions. This form of processor synchronization is accommodated entirely in hardware.

SUMMARY

The FourPort RAM combines features of fast static memory and a complex multiple bus interconnect network. The FourPort RAM all but eliminates stalls when transferring data between processors or to memory. This prevents bus conflicts from being a bottleneck in multiprocessor systems.

The flexibility of the FourPort RAM allows multiprocessor designs to remain generalized while achieving high speeds on critical vector processes. The fact that the RAM itself is also the interconnect network between processors eliminates the complexity of a conventional multiprocessor bus system. The straightforward static RAM interface of the FourPort RAM, allows almost any processor to be used in an array for embedded systems. These factors conspire to make practical a variety of new vector processing architectures centered around the world's first "large" truly four ported single–chip RAM.

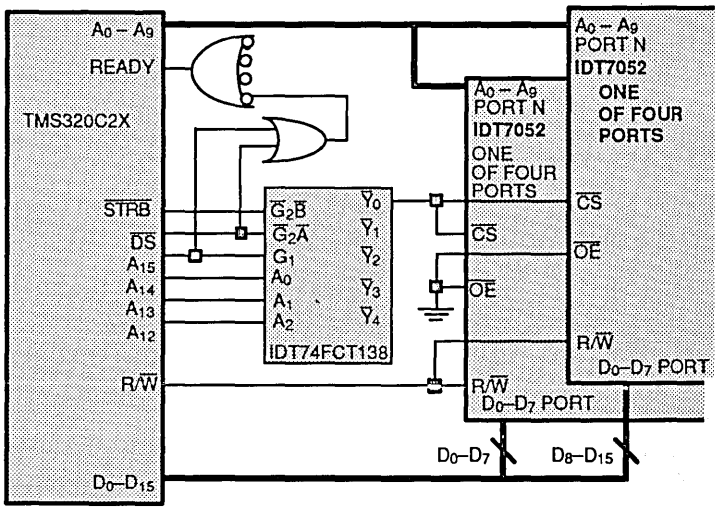

Figure 7. A 16–bit TMS320C2X to IDT7052 Interface Example

Integrated Device Technology, Inc.

INTRODUCTION TO IDT'S FourPort™ RAM

APPLICATION NOTE AN–45

By John R. Mick

INTRODUCTION

Integrated Device Technology is continuing to pioneer higher speed and higher density static RAMs. As IDT has improved its CEMOS™ technology, new RAM architectures and additional features have become feasible. The end result is that design engineers now have powerful new integrated circuits available for demanding applications. One such circuit is the IDT7052 FourPort RAM. This device is a Four–port 2K by 8–bit Static RAM built using a 12–transistor four ported static RAM cell. Each of the four ports is independent in terms of the byte that it can read or write.

This new IDT7052 FourPort RAM provides the system architect with better ways to look at computer system design. For example, the IDT7052 can be used in a multiprocessor environment to provide a common memory among several processors. An example of such an architecture is shown in Figure 1. Here we see each of the four RAM ports connected to a high performance microprocessor. These processors could also be intelligent controllers, DSP engines, or a combination of the two. The FourPort RAM can be used in such computer architectures as hypercubes and parallel processing machines for storage and movement of data. It offers unheard of opportunities in digital signal processing (DSP) where new architectures for Fast–Fourier–Transforms (FFTs), recursive and non–recursive digital filters, windowing functions, and special purpose algorithms can take advantage of multiple ports into a shared memory. The IDT7052 FourPort RAM can increase system performance and reduce parts count by providing simultaneous access to the data by more than one processor at a time.

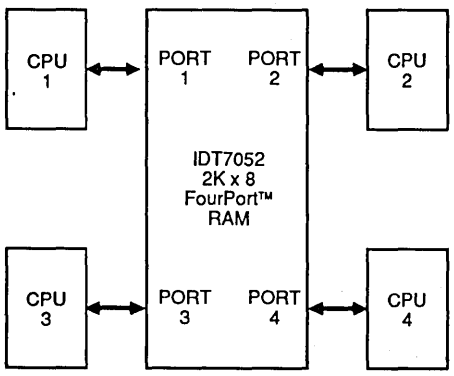

Figure 1. Four–Port RAM Providing Common Memory to Four CPUs

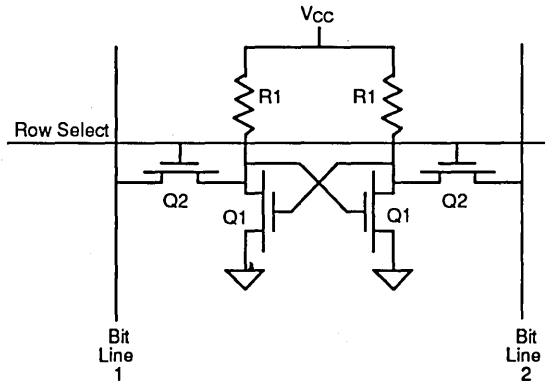

Figure 2. Typical Four–Transistor SRAM Cell

UNDERSTANDING THE FourPort RAM

In order to effectively design with the IDT7052 FourPort RAM, it is important for the design engineer to understand its construction and architectural features. This is most easily accomplished by starting with a simple single port RAM cell and evolving its architecture into the FourPort structure. Figure 2 shows a typical single port static RAM built using a four–transistor cell. This architecture is commonly used by most static RAM manufacturers to build static RAMs because it offers high density, good speed and low power.

In its simplest description, the device consists of two N–channel transistors (Q1) and two resistors (R1) that are connected so as to form two simple cross–coupled inverters. This gives a regenerative action such that one N–channel transistor is ON and the other N–channel transistor is OFF. Thereby, a single bit of memory is formed. In order to interface to this cross–coupled pair of inverters, two additional N–channel transistors (Q2) are connected between the inverter outputs and the bit–lines. The gates of these two N–channel transistors are connected to a line called the row select. These Q2 transistors connected between the cell and the bit lines are usually called transmission gates. The result is that when a particular row of cells in the RAM is addressed, these two transistors are turned on and one bit–line will reflect a HIGH and the other bit–line will reflect a LOW as determined by the current state of the static RAM cell.

An expanded example of this RAM architecture is shown in Figure 3. Here we see a 16–bit RAM, organized four–rows by four–columns internally, in a more complete form. The bit–lines of the cells are connected to the inputs of a sense amplifier by means of N–channel switches. These switches are controlled by the column address decoder. The sense amplifier will detect whether the state of the bit is a logic one or a logic zero depending on the relative polarity of the two bit–lines going into the differential sense amplifier. We usually call the transistors connected between the sense amplifier and bit–lines a data multiplexer or data selector.

FourPort is a trademark of Integrated Device Technology, Inc.

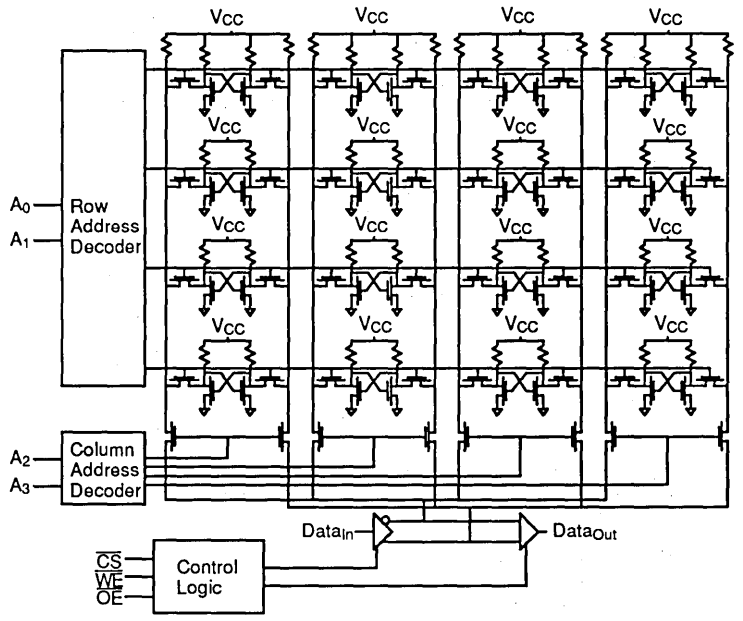

Figure 3. An Example Four-Transistor Cell for a 16-bit SRAM

When we wish to write the simple RAM as shown in Figure 3, a row address line is selected by the row address decoder and the N-channel pass transistors (Q2 of Figure 2) connected to the bit lines are turned on by pulling their gates high. Now however, the write amplifier driven by the Data-In line (Figure 3) is turned on by the write enable signal via the control logic. The write amplifier will drive one bit-line HIGH and the other bit-line LOW as determined by the logic state of the data input. The output of the write amplifier is more powerful than the inverter transistors (Q1 in Figure 2) in the RAM cell and it easily overpowers these inverter transistors if it is necessary to flip the static RAM bit. In its simplest form, this is all there is to the circuitry of a static RAM. Functions such as chip enable are used to simply enable or disable the entire operation of the RAM. Output enable on a static RAM is used to turn "on" the outputs during a read cycle and turn "off" the outputs during write cycles. It can be used to solve timing problems in high speed applications.

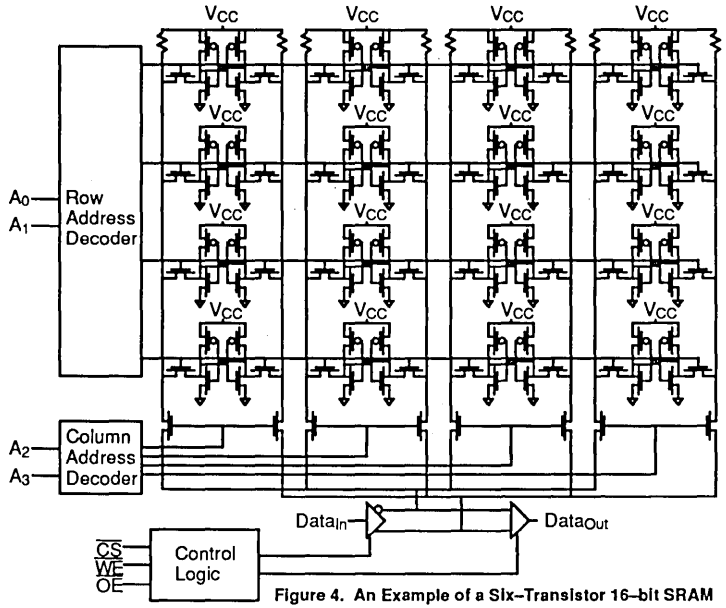

Figure 4. An Example of a Six-Transistor 16-bit SRAM

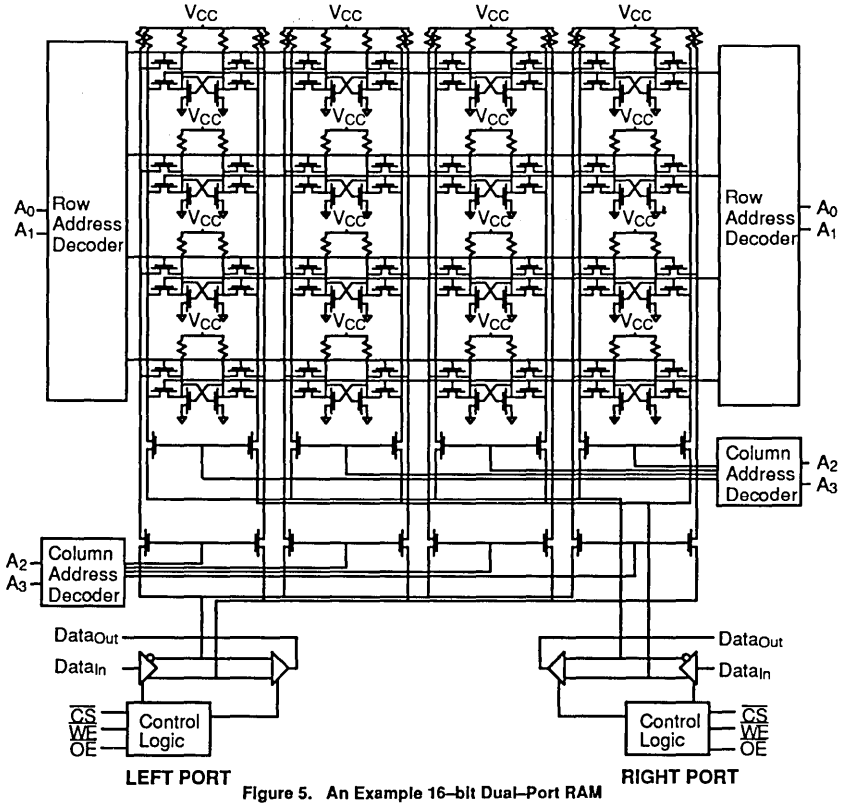

Figure 5. An Example 16-bit Dual-Port RAM

A variation on the standard four–transistor static RAM cell is the six–transistor static RAM cell as shown in Figure 4. In this Figure we see that the two pull–up resistors (R1 of Figure 2) have been replaced by two P–channel transistors. The operation of such a six–transistor cell is identical to the four–transistor cell previously described. The difference between the two approaches is that the physical size of the cell with the P–channel transistors is larger than the cell with the resistors. The standby power can be lower for the six–transistor cell because there is no power being dissipated. In a four–transistor cell, one of the the pull–up resistors is always dissipating power since one transistor of the cell is always ON. The six–transistor cell can have higher radiation hardened characteristics than the four–transistor cell because the voltage swings in the cell are larger. This is because the internal node in the cell that is high is pulled to the +5V rail by the P–channel transistor. In addition, the six–transistor cell provides higher internal noise margins in the circuit for this same reason. Most manufacturers of static RAMs use the four–transistor cell because it allows static RAMs of higher density to be fabricated with smaller die sizes.

Next, let's look at a typical dual–port RAM such as the IDT7134, a 4K by 8–bit device. An example schematic diagram showing a sixteen–bit two–port RAM is shown in Figure 5. Here we see our standard cross–coupled inverter pairs using two N–channel transistors with resistor pull–ups (Q1 and R1 of Figure 2) to form the sixteen memory bits. Notice however, now there are two pairs of N–channel transmission gates connected to each RAM cell's true and compliment outputs and two pairs of bit–lines associated with each cell. Each pair of bit–lines is a read/write port into the dual–port RAM. Each pair of transmission gates has its own row address control so that Port A can select any memory cell in the RAM and Port B can select any memory cell in the RAM. This is the technique used in IDT dual–port RAMs to provide total independent access to individual bytes. Each pair of bit–lines is connected to a sense amplifier and a write buffer via a data multiplexer so that each port on the 2–port RAM can read or write data at its selected address.

Now for the FourPort RAM operation. Figure 6 shows a minimal schematic diagram for the IDT7052 12–transistor FourPort RAM cell. The two inverters making up the basic memory cell are fabricated using two N–channel pulldown transistors and two P–channel pullup transistors. They are connected in the normal cross–coupled inverter fashion to make a single memory cell. Four individual memory ports are achieved by using four pairs of N–channel pass transistors to connect to four pairs of bit–lines. Four individual row addresses are used to select each pair of transmission gates connected between the RAM cell outputs and the bit–line pairs. Four sense–amplifier/write–buffers are used to provide individual read/write paths from each port to all the cells in the RAM.

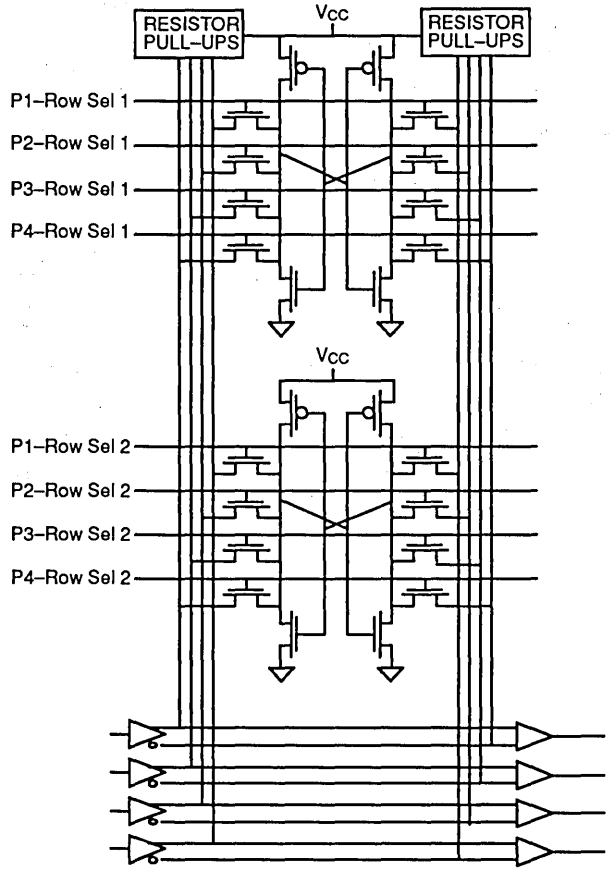

Figure 6. A Simple Example of a Twelve Transistor FourPort RAM Configuration

From this discussion, the design engineer should understand the mechanism used to implement a FourPort RAM. As described, we can see how we can make each port of the FourPort RAM totally independent from the other ports. Do not confuse this statement to mean that independent reads and writes can always be performed without data corruption. If two ports write to the same byte at the same time, one or both values may be lost. Likewise if one port writes to a byte at the same time another port is reading the byte, the read may be corrupted even though the byte write is completed correctly. This application note does not discuss issues of data integrity in the case of multiple accesses to the same location, when one of the asynchronous accesses is a write cycle. These problems are discussed in detail in Application Note 2 and will not be further discussed here. Suffice it to say that the IDT7050 and IDT7052 FourPort RAMs have a $\overline{\text{BUSY}}$ input to allow external hardware or software arbitration schemes to be implemented to meet the specific needs of the designer's system. The $\overline{\text{BUSY}}$ input serves only to block write cycles from the port to which this signal is applied. It has no effect on a read cycle. Note that in the following applications we are not using the $\overline{\text{BUSY}}$ input of the FourPort RAM so it should be tied HIGH. We probably will not always mention this, so do not forget it or you will not be able to write into the FourPort RAM.

Once the rules are understood however, only engineering creativity is needed to visualize new architectural opportunities for FourPort RAMs. This powerful new memory technology will provide increased performance in future electronic processing systems.

CASCADING THE FourPort RAM

Perhaps the most easily understood techniques in designing with static RAMs are width and depth expansion. Width expansion of any port of the FourPort RAM is straightforward. No additional parts are needed to build 16, 24 or 32 bit wide or wider memories. Any port of the FourPort RAM can be viewed the same as a simple single port static RAM. All the same rules apply and they can be applied individually to each port of the FourPort RAM.

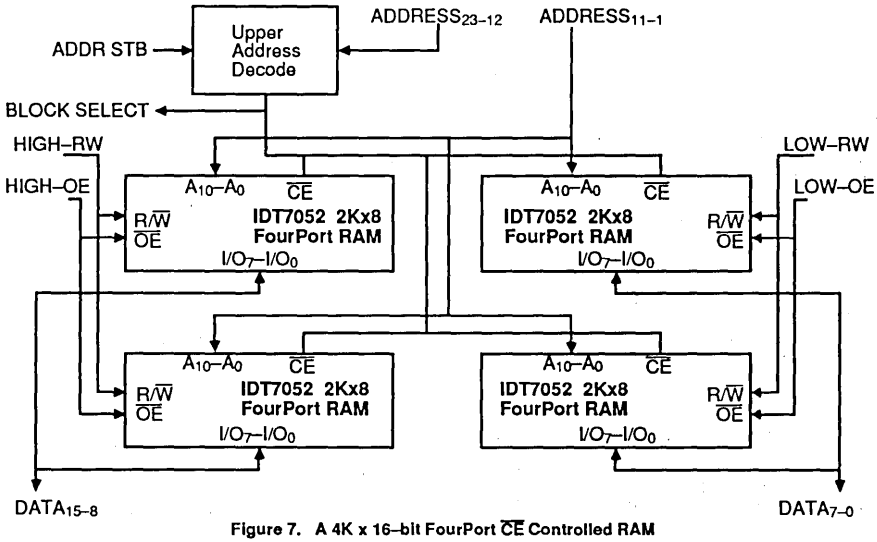

Figure 7. A 4K x 16–bit FourPort $\overline{CE}$ Controlled RAM

Depth expansion of the FourPort RAM is also quite simple. If one port is viewed as a static RAM, it is expanded similar to a single port device. Lower addresses are connected between devices and upper addresses are decoded by means of a standard decoder such as an IDT74FCT138 or IDT74FCT139. The outputs of the decoders can be used either to control the chip selects or control the write–enable and output–enable individually. Simple examples of expansion of one port of a FourPort RAM to a 4K–word by 16–bit configuration are shown in Figure 7 and Figure 8. Figure 7 shows the Chip Enable expansion method while Figure 8 shows write–enable, output–enable expansion. The two schemes are similar, but, sometimes one can have a timing advantage over the other. This is usually a function of the actual timing signals that are available or have already been generated.

Once the depth expansion is understood, we can view the CPU interconnect schemes by simply looking at a one deep FourPort RAM. We recognize that deeper versions can be realized as just described.

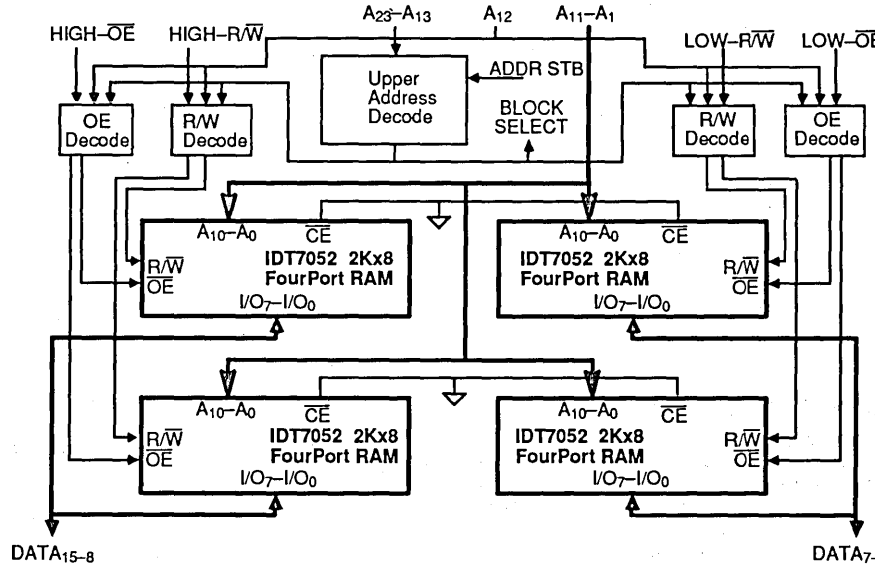

Figure 8. A 4Kx16–bit FourPort $\overline{OE}$ and R/$\overline{W}$ Controlled RAM

9

CONNECTING THE FourPort RAM TO CPUs

A Z80A Example

Probably the easiest interface of the IDT7052 FourPort RAM is to a Z80A. This processor still provides a great price–performance tradeoff! By using four Z80As with the IDT7052 FourPort RAM, significant performance advantages can result. For example, no time need be lost due to DMA channels. The data placed in memory by one Z80A on one port is instantly available to another Z80A on another port. In a similar fashion, parallel processing can be performed by multiple processors working on the data in shared memory.

The typical connection scheme for the IDT7052 (or IDT7050 1Kx8 FourPort RAM) to a Z80A is shown in Figure 9. Here we see the eleven address lines, A_{10}–A_0, of the FourPort RAM are connected to the A_{10}–A_0 lines of the Z80A. This places the FourPort RAM in a contiguous 2K address space of the Z80A. The 2K byte segment actually used is determined by upper address decode circuit. A PAL or an IDT74FCT521 could be used to perform this function. The data lines are connected between the processor and the RAM. The Z80A has a $\overline{RD}$ line that can be connected to the FourPort $\overline{OE}$ and a $\overline{WR}$ line that can be connected to the FourPort R/$\overline{W}$ input. This works along the lines of the a Chip Enable expansion method just described. When the Z80A addresses the FourPort RAM, either a read or write will be performed depending on the instruction being executed. If $\overline{RD}$ goes LOW, the FourPort RAM will output data from the addressed byte. If $\overline{WR}$ goes LOW, the FourPort RAM will write data into the addressed byte.

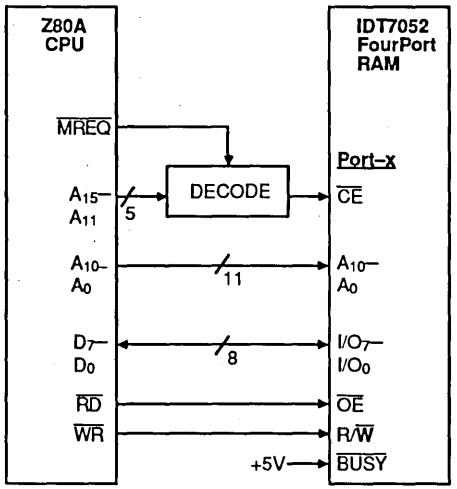

Figure 9. Interfacing the Z80A to One Port of the FourPort RAM

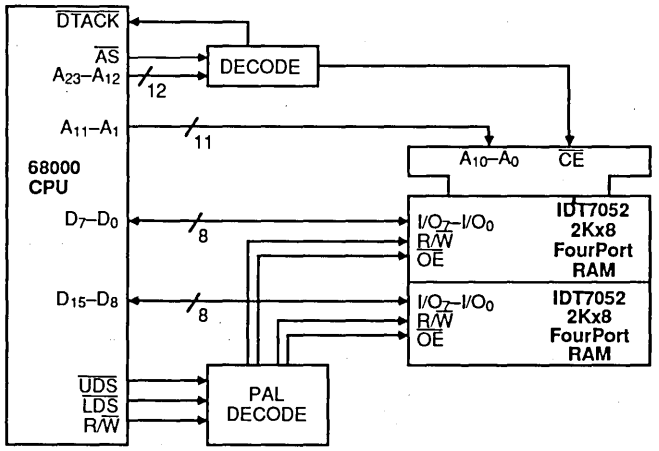

Figure 10. A 16–bit FourPort RAM with the 68000 CPU

A 68000 CONNECTION EXAMPLE

If we wish to build a 16–bit microprocessor interface to one port of the IDT7052 FourPort RAM, a typically interface might be as shown in Figure 10. Here we see two IDT7052s used in a 16–bit configuration. One FourPort RAM is connected to the lower eight data bits (D_7–D_0) and the other FourPort RAM is connected to the upper eight data bits (D_{15}–D_8). This completes a 16–bit data bus. Address lines A_{10}–A_0 of the FourPort RAM are connected between RAMs and also connected to address lines A_{11}–A_1 respectively of the 68000. Remember, the 68000 does not have an A_0 address line but uses Upper–Data–Strobe ($\overline{UDS}$) and Lower–Data–Strobe ($\overline{LDS}$) to control the upper and lower byte selection. These two signals in conjunction with the R/$\overline{W}$ signal are decoded in a PAL to generate the individual FourPort RAM R/$\overline{W}$ and $\overline{OE}$ control signals. Figure 11 shows the truth table needed for the PAL. It has been my experience when working with the 68000, that once these signals are generated, they are useful throughout the design to control other peripherals, etc. Basically, however, in this exam-

ple we simply have a lower byte FourPort RAM and an upper byte FourPort RAM.

INPUTS			OUTPUTS			
R/$\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{URW}$	$\overline{LRW}$	$\overline{UOE}$	$\overline{LOE}$
X	1	1	1	1	1	1
1	0	0	1	1	0	0
0	0	0	0	0	1	1
1	1	0	1	1	1	0
0	1	0	1	0	1	1
1	0	1	1	1	0	1
0	0	1	0	1	1	1

Figure 11. 68000 16–bit Control PAL Truth Table

The upper address lines of the 68000, A_{23}–A_{12} in this case, are used to position the 2K bytes of FourPort RAM in continuous address space of the 68000. The actual location can be anywhere from 0x000000 to 0xFFFFFF as long as the overall range is on 2K byte boundaries. Usually we include address strobe ($\overline{AS}$) in the decoding as it can solve some timing problems. A timing review will show if it is needed. An output of the decode circuit can be used to generate the data acknowledge ($\overline{DTACK}$) if it is needed. Usually design engineers have an overall plan for generating the memory $\overline{CE}$s and $\overline{DTACK}$, so what is shown here is only to remind you of solving the overall problem.

Address of Bytes in a Big–Endian 32–bit Word

Word Address	Bits 31–24	Bits 23–16	Bits 15–8	Bits 7–0
0x0024	0x0024	– etc –	– etc –	– etc –
0x0020	0x0020	0x0021	0x0022	0x0023
0x001C	0x001C	0x001D	0x001E	0x001F
0x0018	0x0018	0x0019	0x001A	0x001B
0x0014	0x0014	0x0015	0x0016	0x0017
0x0010	0x0010	0x0011	0x0012	0x0013
0x000C	0x000C	0x000D	0x000E	0x000F
0x0008	0x0008	0x0009	0x000A	0x000B
0x0004	0x0004	0x0005	0x0006	0x0007
0x0000	0x0000	0x0001	0x0002	0x0003

Address of Bytes in a Big–Endian 16–bit Word

Word Address	Bits 15–8	Bits 7–0
0x0014	0x0014	– etc –
0x0012	0x0012	0x0013
0x0010	0x0010	0x0011
0x000E	0x000E	0x000F
0x000C	0x000C	0x000D
0x000A	0x000A	0x000B
0x0008	0x0008	0x0009
0x0006	0x0006	0x0007
0x0004	0x0004	0x0005
0x0002	0x0002	0x0003
0x0000	0x0000	0x0001

Address of Bytes in an 8–bit Word

Word Address	Bits 7–0
– etc –	– etc –
0x0010	0x0010
0x000F	0x000f
0x000E	0x000E
0x000D	0x000D
0x000C	0x000C
0x000B	0x000B
0x000A	0x000A
0x0009	0x0009
0x0008	0x0008
0x0007	0x0007
0x0006	0x0006
0x0005	0x0005
0x0004	0x0004
0x0003	0x0003
0x0002	0x0002
0x0001	0x0001
0x0000	0x0000

Figure 12. Memory Map for 8, 16, and 32–bit Byte Ordering

HOW ABOUT 8–BITS, 16–BITS AND 32–BITS IN THE SAME SYSTEM!!!

This is perhaps the most interesting example to talk about. We will use an 8–bit Z80A, a 16–bit 68000 and a 32–bit R3000 RISC microprocessor to discuss the design techniques. We have chosen the three processors because they are typical, they are fun to work with and they have had broad acceptance in the microprocessor world. First, let's look at Figure 12 to understand memory addressing and "memory space". All three of our selected microprocessors are "byte" addressable machines. That means they can address bytes as well as words in the case of the 68000 and R3000. The 68000 is a Big–Endian machine and the R3000 will be operated in Big–Endian mode to keep things simple. (DEC and Intel fans can make the appropriate transformation. In fact, the FourPort RAM might make a really exciting byte–ordering problem solver between machines by connecting one port as Big–Endian and another port as Little–Endian to the same microprocessor and similarily for the second processor.)

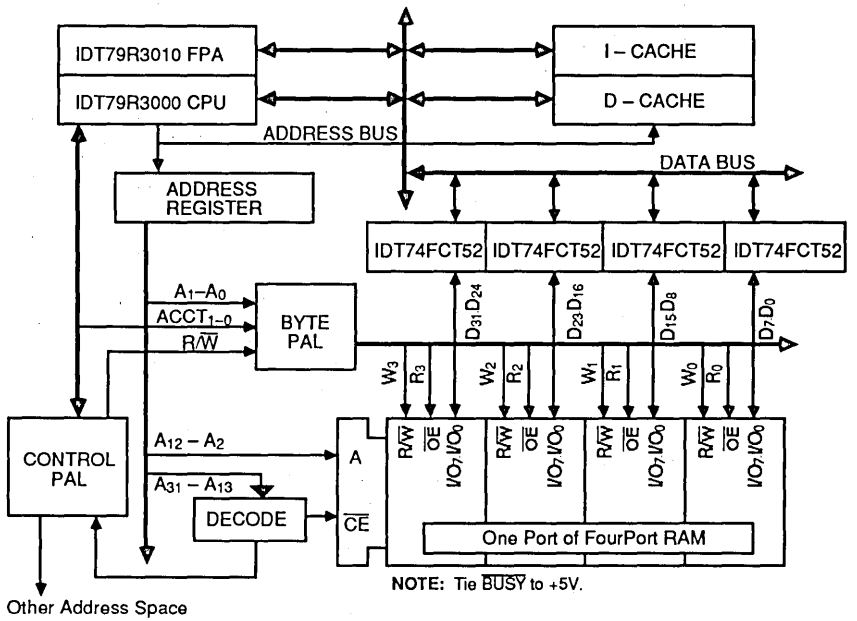

Figure 13. Using a 32–bit Wide FourPort Memory with the R3000

Since we are talking about byte addressable machines, Figure 12 shows the byte addresses of an 8–bit machine, the byte addresses of a 16–bit machine and the byte addresses of a 32–bit machine. Likewise word addresses of 16–bit and 32–bit machines are shown. What is intended here is to point out that we want the consecutive byte ordering of all of the machines to remain constant. By doing this, we keep the ability to do indexing into an array of bytes from any of the processors as a simple task. For example, a 40 byte index from any byte address is the same in all processors talking to each other through the FourPort RAM. We can look at Figure 12 as representing the Z80A, 68000 and R3000 respectively.

Next, let's look at the interface needed for each of our three processors. We will build on our previous examples in this application note but there are differences needed to allow proper addressing. Let's begin by looking at the R3000. The reader should refer to IDT's wealth of information on the IDT79R3000 RISC microprocessor if you are not familiar with the standard CPU, FPA, Cache and I/O interface. We will use four of the IDT7052 FourPort RAMs to give a 32–bit wide memory for this example. We assume the first port is connected to the R3000, the second port is connected to the 68000 and the third port is connected to the Z80A. The fourth port could be connected to a second one of any of these processors or a wide selection of other things.

A typical R3000 interface is shown in Figure 13. The key element here is to understand that we are interfacing to a 32–bit data bus, 32–bit address bus with byte encoded control signals and to an R3000 interface. We are able to implement the required byte control per Figure 12 by using the "BYTE PAL" shown in Figure 13. The truth table for this PAL is shown in Figure 14. Using this decoding, we are able to do all of the required operations. This includes 32–bit word operations, 24–bit three–byte operations, 16–bit half–word operations and 8–bit byte operations. The signals available are A_0, A_1, AccessType0, and AccessType1, all from the R3000 address register, and we assume a R/$\overline{W}$ input from the "Control PAL" shown in Figure 13. There may be other options here, but this R/$\overline{W}$ signal must be realized in some fashion. The upper address bits from the R3000 are decoded in the fashion previously discussed to locate the total 8K bytes of FourPort RAM in the R3000 address space.

Working out the timing of the R3000 interface is most of the work. Remember that at this interface point there are several flexibilities in the final timing. With an R3000 running at 16 MHz, a data transfer cycle is in multiples of 67 nanoseconds, 20 MHz gives 50 nanoseconds, and 25 MHz allows 40 nanoseconds. Thus depending on the processor speed and the FourPort RAM speed selected, block refill may or may not be desired. In any case, we

should be able to run with zero, one or two stall cycles. As mentioned before, the design engineer usually has a plan for address decoding and control handshake which is more closely tied to the overall system design. From this standpoint, interfacing to one port of the FourPort RAM is no different than interfacing to an EPROM, DRAM, SRAM, or peripheral.

INPUTS					OUTPUTS								COMMENTS
R/$\overline{W}$	ACCT1	ACCT0	A1	A0	W3	W2	W1	W0	R3	R2	R1	R0	
1	1	1	0	0	1	1	1	1	0	0	0	0	Word Read
0	1	1	0	0	0	0	0	0	1	1	1	1	Word Write
1	1	0	0	0	1	1	1	1	0	0	0	1	Tri-Byte Read
1	1	0	0	0	1	1	1	1	1	0	0	0	Tri-Byte Read
0	1	0	0	1	0	0	0	1	1	1	1	1	Tri-Byte Write
0	1	0	0	1	1	0	0	0	1	1	1	1	Tri-Byte Write
1	0	1	0	0	1	1	1	1	0	0	1	1	Half-Word Read
1	0	1	0	0	1	1	1	1	1	1	0	0	Half-Word Read
0	0	1	1	0	0	0	1	1	1	1	1	1	Half-Word Write
0	0	1	1	0	1	1	0	0	1	1	1	1	Half-Word Write
1	0	0	0	0	1	1	1	1	0	1	1	1	Read Byte 0
1	0	0	0	1	1	1	1	1	1	0	1	1	Read Byte 1
1	0	0	1	0	1	1	1	1	1	1	0	1	Read Byte 2
1	0	0	1	1	1	1	1	1	1	1	1	0	Read Byte 3
0	0	0	0	0	0	1	1	1	1	1	1	1	Write Byte 0
0	0	0	0	1	1	0	1	1	1	1	1	1	Write Byte 1
0	0	0	1	0	1	1	0	1	1	1	1	1	Write Byte 2
0	0	0	1	1	1	1	1	0	1	1	1	1	Write Byte 3

Figure 14. 32-bit R3000 Control PAL Truth Table (Big-Endian)

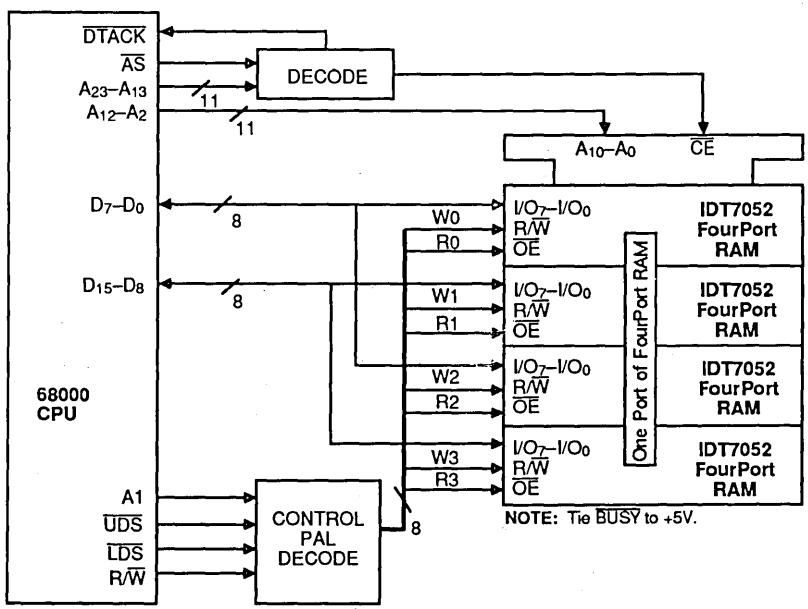

Figure 15. A 32-bit FourPort RAM with the 68000 CPU

INPUTS				OUTPUTS								COMMENTS
R/$\overline{W}$	A1	$\overline{LDS}$	$\overline{UDS}$	W3	W2	W1	W0	R3	R2	R1	R0	
1	0	0	0	1	1	1	1	0	0	1	1	Word Read
1	1	0	0	1	1	1	1	1	1	0	0	Word Read
0	0	0	0	0	0	1	1	1	1	1	1	Word Write
0	1	0	0	1	1	0	0	1	1	1	1	Word Write
1	0	1	0	1	1	1	1	0	1	1	1	Read Byte 0
1	0	0	1	1	1	1	1	1	0	1	1	Read Byte 1
1	0	1	0	1	1	1	1	1	1	0	1	Read Byte 2
1	0	0	1	1	1	1	1	1	1	1	0	Read Byte 3
0	1	1	0	0	1	1	1	1	1	1	1	Write Byte 0
0	1	0	1	1	0	1	1	1	1	1	1	Write Byte 1
0	1	1	0	1	1	0	1	1	1	1	1	Write Byte 2
0	1	0	1	1	1	1	0	1	1	1	1	Write Byte 3

Figure 16. 32–Bit 68000 Configuration Control PAL Truth Table

Next, let's look at the 16–bit 68000 interface in a 32–bit memory system. A detailed block diagram is shown in Figure 15. The key thing to notice here is that four of the IDT7052 FourPort RAMs are used. Notice that two of the devices are connected to the D_7–D_0 data bus and two of the devices are connected to the D_{15}–D_8 data bus on the 68000. Address line A_1 will be used to select which pair of FourPort RAMs that the processor will read or write.

For example, when A_1 is LOW, control signals W3, W2, R3 and R2 will be enabled. When A_1 is HIGH, control signals W1, W0, R1 and R0 will be enabled. This is shown in complete detail in the truth table of Figure 16. If we study this truth table, we see how we accomplish both 16–bit word (half–word) reads and writes as well as 8–bit byte reads and writes. All of this is consistent with the memory map shown in Figure 12. The technique here is actually to use A_1 to select either the lower half–word or the upper half–word in a 32–bit FourPort RAM memory system. Every thing else about the design is the same as the previous 68000 example.

Lastly, let's look at the 8–bit interface to the Z80A microprocessor. It also should be viewed as being hooked into a 32–bit memory system. A detailed block diagram is shown in Figure 17. Notice that all four of the IDT7052 FourPort RAMs are connected to the D_7–D_0 data bus. Address lines A_1 and A_0 will be used to select the device to which the Z80A processor will talk. In fact, A_1, A_0, $\overline{RD}$ and $\overline{WR}$ are inputs to the control PAL decode. The truth table to be implemented is detailed in Figure 18. This processor is only capable of performing byte reads or writes so the decoding is straightforward. A_1 and A_0 are used to do byte selection. Thus, the FourPort RAM A_{10}–A_0 address inputs are connect to the A_{12}–A_2 address lines of the Z80A. This keeps the byte addressing as desired in the memory map of Figure 12. Again the remaining part of the design is as shown in the previous Z80A example.

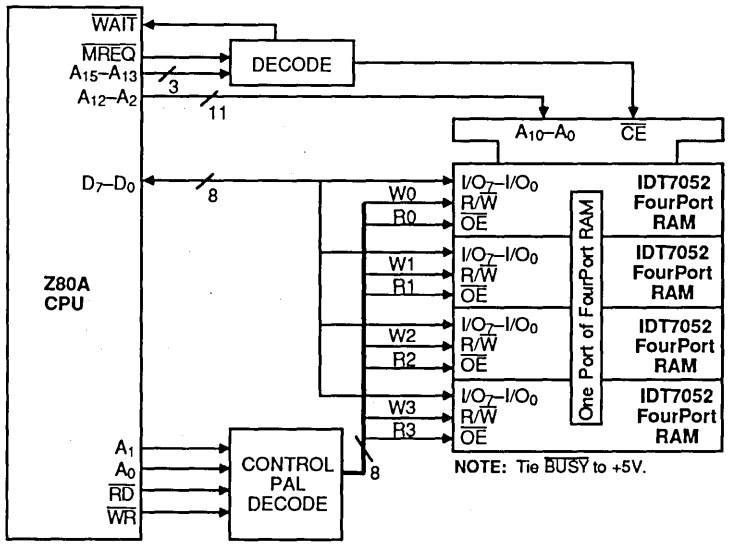

Figure 17. A 32–bit FourPort RAM with the Z80A CPU

INPUTS				OUTPUTS								COMMENTS
$\overline{WR}$	$\overline{RD}$	A1	A0	W3	W2	W1	W0	R3	R2	R1	R0	
1	0	0	0	1	1	1	1	0	1	1	1	Read Byte 0
1	0	0	1	1	1	1	1	1	0	1	1	Read Byte 1
1	0	1	0	1	1	1	1	1	1	0	1	Read Byte 2
1	0	1	1	1	1	1	1	1	1	1	0	Read Byte 3
0	1	0	0	0	1	1	1	1	1	1	1	Write Byte 0
0	1	0	1	1	0	1	1	1	1	1	1	Write Byte 1
0	1	1	0	1	1	0	1	1	1	1	1	Write Byte 2
0	1	1	1	1	1	1	0	1	1	1	1	Write Byte 3

Figure 18. 32–bit Z80A Control PAL Truth Table

The key in all of this discussion is to keep track of the data bus width being used in the design. Similarly, the decoding and processor address connections must take this into account. This is one point that the design engineer usually does not have to deal with when working with single port memories.

The purpose of this three processor example is to show a few interconnect schemes to typical microprocessors. From this discussion, the design engineer should be able to extend the concepts presented here to other 8–bit, 16–bit and 32–bit microprocessors. Just keep the techniques in mind and work out the desired memory mapping and timing.

SYSTEM DESIGN IDEAS

Now that we have discussed how the the FourPort RAM is built and we have a good idea of how to connect it to many processors, let's look at some system level uses for this type of FourPort RAM.

DIGITAL SIGNAL PROCESSING (DSP)

Digital signal processing applications have been expanding as new developments in semiconductor technology provide increased packing density and new architectures in integrated circuits. The IDT7052 FourPort RAM is another in the continuing growth of integrated circuits that allow design engineers to realize new system designs.

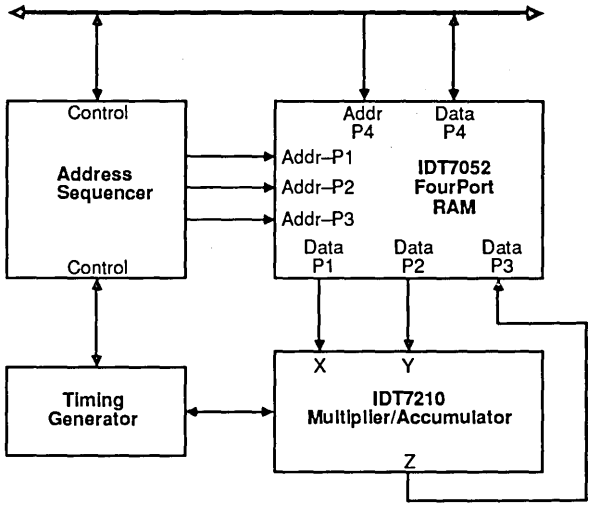

Figure 19. A Simple DSP Engine Using a FourPort RAM

One of the simplest DSP algorithms that can be implemented is the finite–impulse–response (FIR) filter. In this type of algorithm, the impulse response of the filter has nonzero values only for a finite duration. These types of filters are easily implemented using only multiplication and summation. Figure 19 shows a block diagram of a DSP machine that takes advantage of the FourPort RAM to interface to a multiplier–accumulator (MAC) such as the IDT7210. In this example, two of the four ports of the FourPort RAM are used to feed data to the MAC inputs and a third port of FourPort RAM is used to receive completed results from the MAC output. The fourth port of the FourPort RAM is connected to a local data–address bus to interface to the remainder of the system.

In the actual operation of such a processor as shown in Figure 19, data is loaded into the FourPort RAM via Port 4. The algorithm usually needs coefficients and these are also loaded into the FourPort RAM using Port 4. An address sequencer has the responsibility of providing the correct sequence of addresses to Ports 1, 2 and 3. This unit operates in conjunction with the timing generator to execute the algorithm. Let's look at an example. Suppose our algorithm is:

$$y(n) = A_0 * x(n) + A_1 * x(n-1) + A_2 * x(n-2) + A_3 * x(n-3)$$

We could read this as the current processed value is equal to the current sample times A_0, plus the first past sample times A_1, plus the second past sample times A_2, plus the third past sample times A_3. This already shows its potential as a FourPort RAM application.

Now, we initialize our system at power–up by putting the values A_0, A_1, A_2, and A_3 into the FourPort RAM. We would most likely clear the four locations for the data. Then we start taking data. Each time we receive a data value, we can overwrite the fourth past sample. For each new sample, we will compute a new y(n) and put it into the FourPort RAM. At some point we will extract the sequence of values for y(n) that we have computed. As can be seen, we can have several operations happening on the same clock cycle. RAM ports 1 and 2 could be outputting data, RAM port 3 could be inputting data, and RAM port 4 could be inputting or outputting data, all simultaneously. The speed implications are obvious. Needless to say, this is a simple example for the purpose of demonstration. But if we wanted to work on 1024 samples with 128 coefficients and a more complex algorithm, all we have to do is follow the same methodology. See IDT application note 42 for a more detailed example of how to use this method to implement a matrix multiplication.

CPU to CPU to CPU to CPU

Referring to Figure 1 where we started this application note, we see that we have a FourPort RAM connected between four CPUs. How do we efficiently communicate each processor's status to the other processors? You will need to work an acceptable software semaphore scheme or do hardware handshaking using external circuitry. The most obvious software scheme is token passing. After each processor has determined its order in the token passing scheme, the token passing protocol boils down to each processor taking its turn. This can be achieved by reading one memory location to see who is master. Usually multiple reads and compares are performed to avoid any data corruption problems. A good example of this mechanism is detailed in IDT application note 43.

Let's take an example. The byte at address zero contains the token. The current value is one. CPU 1 is master of the FourPort RAM and can read or write data. When finished, it writes a two at address zero. Every so often CPU 2 checks address zero and when it sees a two, it knows it is master. It performs any needed data reads or writes. When it is finished, it writes a three at address zero. CPU 3 writes a four and CPU 4 writes a one. Thus, a simple token passing scheme. "Fail safe" mechanisms can be implemented to keep the token moving if there is any failure.

Another obvious scheme is to set up a simple software semaphore path between each pair of processors. This technique can be used to pass data between processor pairs. The semaphore for each processor can use a different byte (or word) address for each semaphore in each direction. By using this method, many different software handshake techniques can be implemented. Rather than use a test and set instruction for semaphores in this application, another interlocking mechanism, like separate locations dedicated to the status of each processor, should be used to guarantee clean communications between tasks.

In addition, several hardware approaches are usually available in most multiprocessor environments. These include individual interrupts between processors as well as broadcast interrupt approaches. In either case, after the data has been set up in a private buffer, processor A can interrupt processor B to notify it of the pending message. The data structures used in such an environment can include pointer passing and linkage conventions consistent with modern day software techniques.

SUMMARY

The FourPort RAM is a truly new innovative integrated circuit memory that offers new communications methods for computing machines. It provides exceptional speeds because of its opportunity for parallelism. The IDT7052 2K x 8–bit FourPort RAM and the IDT7050 1K x 8–bit FourPort RAM are the first in a series of memories that will pioneer these new architectural frontiers. At speeds as fast as some of the fastest standard static RAMs, they bring new performance dimensions to parallel communication between tasks of a computing machine. These devices utilize the latest in IDT's CEMOS technology to provide the design engineer with an economical high performance, low power, small size and highly reliable "Speciality Memory" for todays performance–driven designs.

Integrated Device Technology, Inc.

USING IDT7024 AND IDT7025 DUAL-PORT STATIC RAMs TO MATCH SYSTEM BUS WIDTHS

APPLICATION NOTE AN-59

By Bhanu V. R. Nandurl

INTRODUCTION

This application note describes three design approaches to accomplish bus width matching using the IDT7024 and the IDT7025 dual-port static RAMs. Interfacing 32-bit buses to 16-bit buses, 32-bit buses to 8-bit buses and 16-bit buses to 8-bit buses is described in detail. In general, any bus that is a multiple of 8 bits can be efficiently interfaced to any other bus that is also a multiple of 8 bits using these dual-port RAMs.

The IDT7024 (4K x 16) and the IDT7025 (8K x 16) dual-port static RAMs are identical to each other in every respect except depth. For simplicity, only the IDT7024 will be discussed in detail. The IDT7024 and the IDT7025 dual-port static RAMs are provided with left and right upper byte enable ($\overline{UB}_L$ and $\overline{UB}_R$) and the left and right lower byte enable ($\overline{LB}_L$ and $\overline{LB}_R$) inputs. These byte enables allow interfacing in any bus width matching scheme without the need for external tri-state buffers or transceivers.

Bus matching schemes require that the byte ordering of information be maintained. This byte ordering can be either "***big-endian***" or "***little-endian***". If data is configured in a *big-endian* format, byte 0 is always the leftmost byte. *Big-endian* is predominant in machines such as the MC 68000 and the IBM 370. If data is configured in a *little-endian* format, byte 0 is always the least significant, rightmost byte. *Little-endian* is used in machines such as the Intel x86, NS 32000 and the DEC VAX. The MIPS R3000 microprocessor and the Intergraph CLIPPER support both data formats, however both these machines must be informed at "power on reset" which data format will be used. The *big-endian* and the *little-endian* byte ordering format is pertinent to 16-bit, 32-bit and 64-bit machines and is not applicable to 8-bit machines. Figures 1a to 1d illustrate the possible *big-endian* and the *little-endian* data conversions.

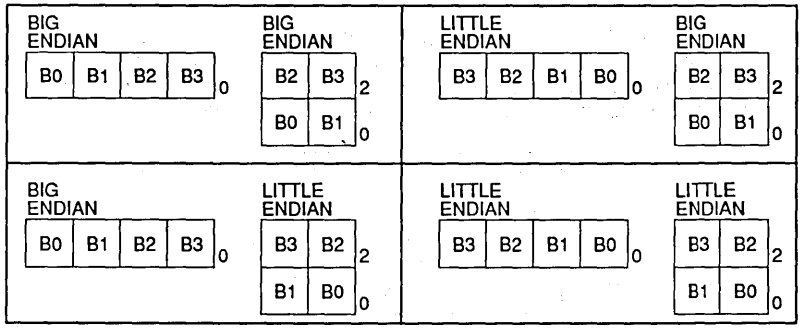

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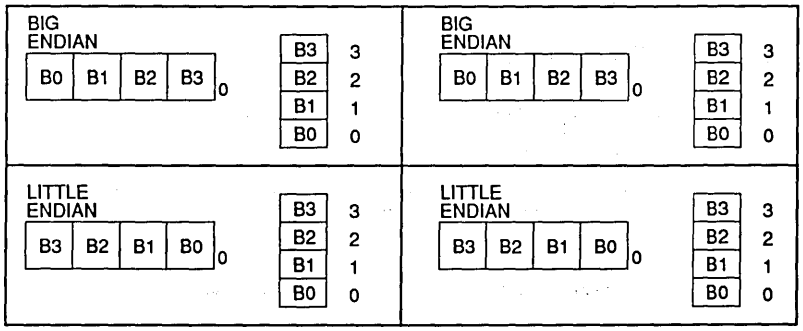
Figure 1a. *Little-endian* and *Big-endian* Byte Mapping Between 32-bit and 16-bit Buses — B0, B1, B2 and B3 are Bytes Within the 32-bit and 16-bit Words



2671 drw 02

Figure 1b. *Little-endian* and *Big-endian* Byte Mapping Between 32-bit and 8-bit Buses — B0, B1, B2 and B3 are Bytes Within the 32-bit and 8-bit Words

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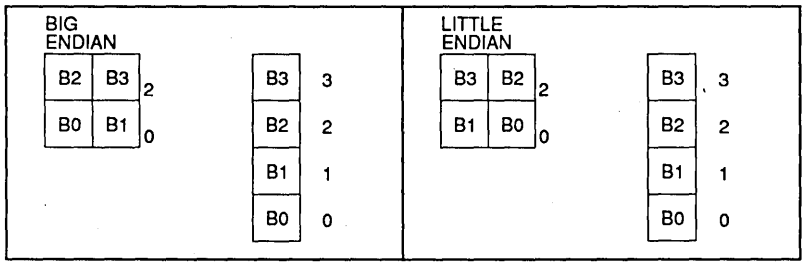

Figure 1c. *Little-endian* and *Big-endian* Byte Mapping Between 16-bit and 8-bit Buses — B0, B1, B2 and B3 are Bytes Within the 16-bit and 8-bit Words

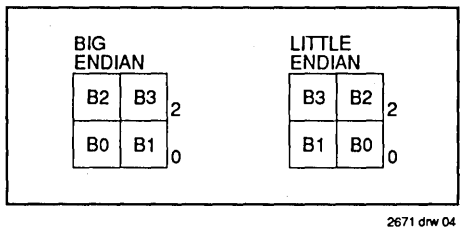

Figure 1d. *Little-endian* and *Big-endian* Byte Mapping Between 16-bit Buses — B0, B1, B2 and B3 are Bytes Within the 16-bit Words

This discussion on interfacing buses takes into account the byte-ordering of data using either the *big-endian* or the *little-endian* data format and even shows how to share data between a big-endian and a little-endian system. This is included to serve as a guide only and is in no way exhaustive. The user is urged to investigate further the data organization to be used in his or her design before attempting to interface buses using dual-port RAMs.

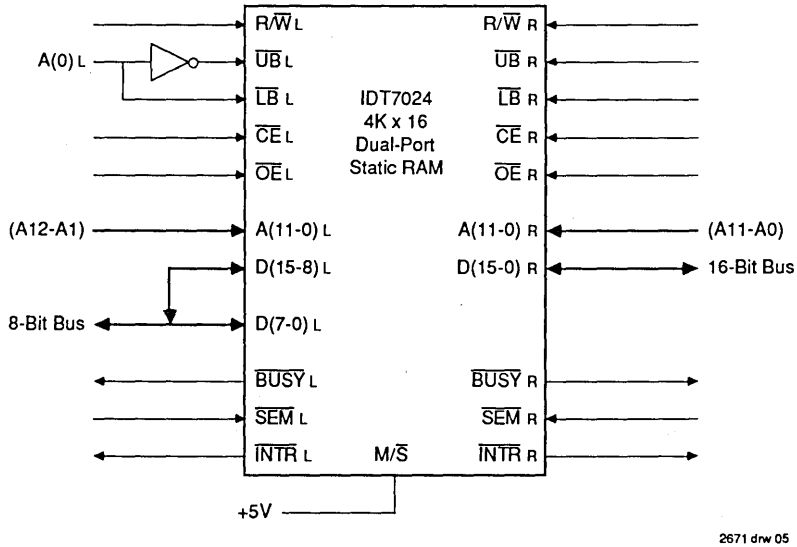

Figure 2. An Interface to Connect 8- and 16-Bit Buses

Figure 2 shows a 16-bit bus to an 8-bit bus interface where the 16-bit side is assumed to be using the *little-endian* data format. On the 8-bit side of the interface, high order data lines D15 - D8 on the RAM are connected to low order data lines D7 - D0 of the RAM (D15 to D7, D14 to D6, etc.) and processor address line A0 is used to select the lower or higher order byte. When A0 is "0", RAM byte 0 is selected and when A0 is "1", RAM byte 1 is selected. Address lines A12 - A1 of the 8-bit processor are connected to the twelve address lines of the IDT7024, as shown. These address lines are used to select the 4K words of the IDT7024. If the 16-bit bus side uses the *big-endian* data format instead of the *little-endian* data format then, on the 8-bit side, A0 must be a "1" to select byte 0 and A0 must be a "0" to select byte 1 to guarantee correct byte ordering on the 8-bit side. An alternate approach to ensure correct byte ordering on the 8-bit side is to place the inverter shown in Figure 2 on the $\overline{LB}_L$ line instead of the $\overline{UB}_L$ line. This change will ensure that when the 8-bit side's A0 line is "0", RAM byte 1 will be selected and, when the A0 line is "1", RAM byte 0 will be selected.

Figure 3 is an interface that connects a 32-bit bus to a 16-bit bus. In Figure 3 both the 32-bit side and the 16-bit side are assumed to be *little-endian*. The upper chip in the diagram holds the two lower order bytes of the 32-bit word and the lower chip in the diagram holds the two higher order bytes. In this interface, processor address bit A0 on the 16-bit side is used to select a 16-bit RAM word. When A0 is "0" the RAM's lower order sixteen bits are selected and, when A0 is "1", the higher order sixteen bits are selected. Selection of the upper byte or the lower byte of either of the two RAMs is determined by the upper byte enable ($\overline{UBE}$) and the lower byte enable ($\overline{LBE}$) inputs. If a *big-endian* byte ordering is assumed on both the 32- and the 16-bit sides, the $\overline{UBE}$ and the $\overline{LBE}$ inputs to the IDT74FCT139 must be interchanged on the 16-bit side.

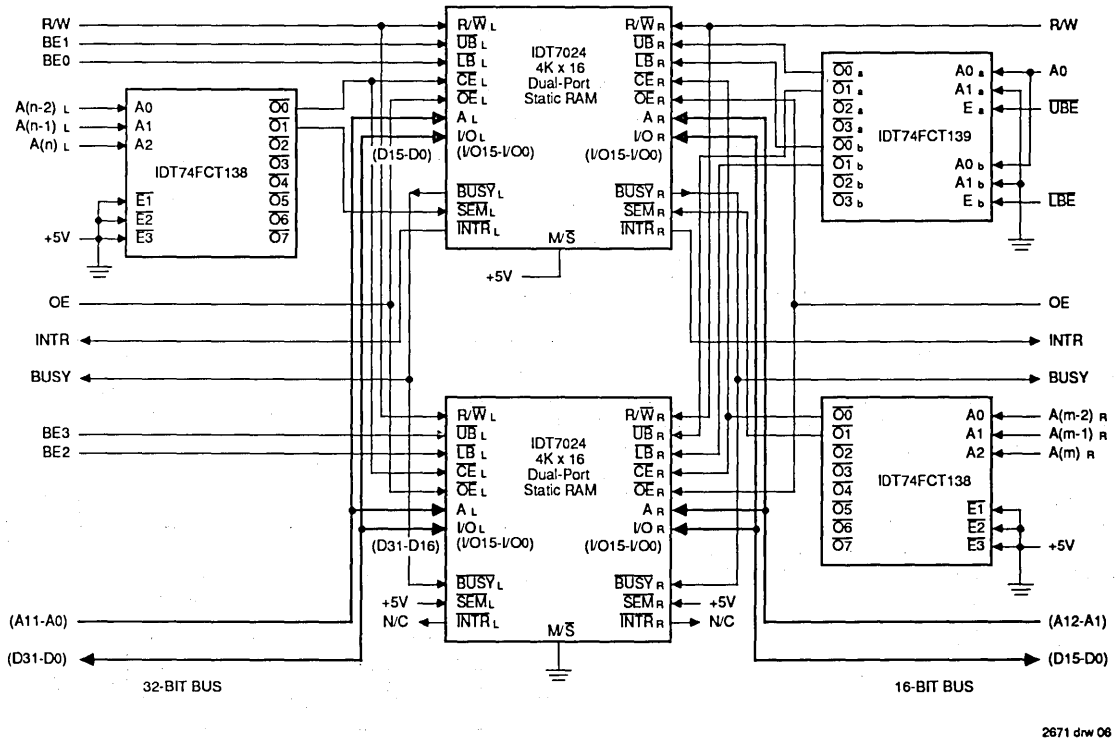

Figure 3. An Interface to Connect a 32-Bit Bus to a 16-Bit Bus

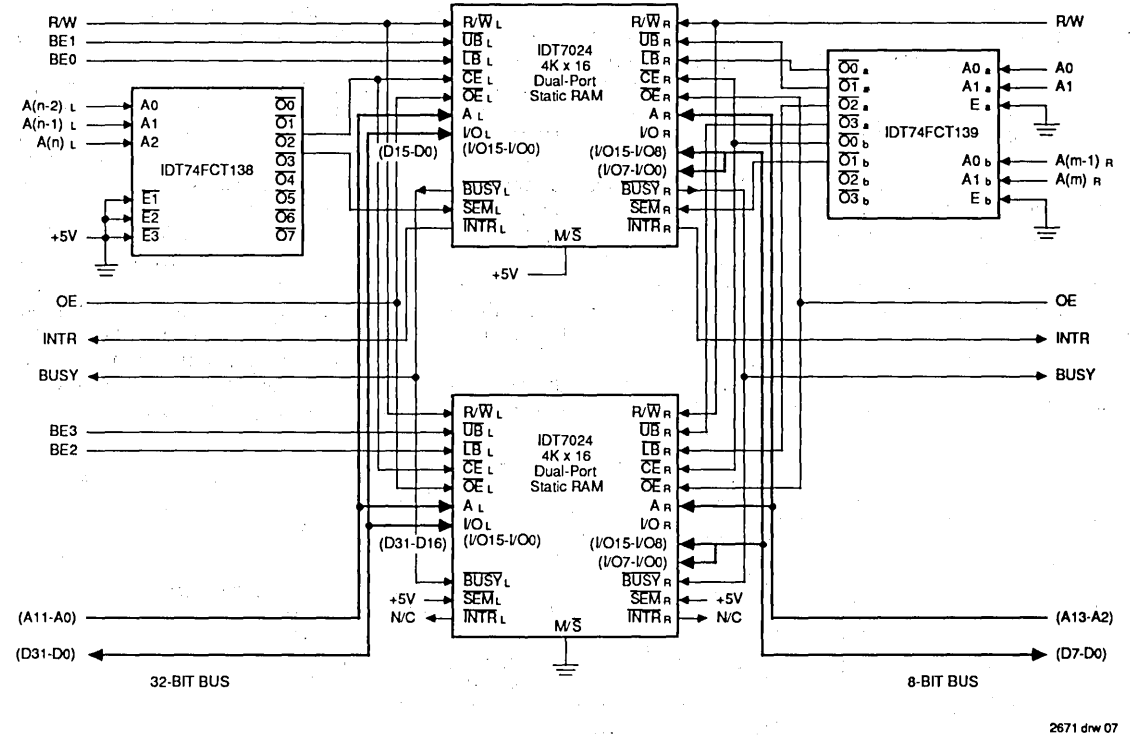

Figure 4. An Interface to Connect a 32-Bit Bus to an 8-Bit Bus

Figure 4 is an interface that connects a 32-bit bus to a 8-bit bus. In Figure 4, the 32-bit side is assumed to be *little-endian* byte ordered. The upper chip in the diagram holds the two lower order bytes and the lower chip in the diagram holds the two higher order bytes. In this interface, address bits A0 and A1 on the 8-bit side are used to select an 8-bit word. Table 1 illustrates the bytes selected for each combination of A0 and A1 for a *little-endian* byte-ordered data format on the 32-bit side. If a *big-endian* byte-ordering is assumed on the 32-bit side, the upper chip will hold the two higher order bytes and the lower chip holds the two lower order bytes. Address bits A0 and A1 on the 8-bit side are used to select one of four bytes as illustrated in Table 2. The mapping scheme to accomplish other bus interfaces is left to the user.

8-bit Side		32-bit Side			
A0	A1	BE3	BE2	BE1	BE0
0	0	X	X	X	0
0	1	X	X	0	X
1	0	X	0	X	X
1	1	0	X	X	X

2671 tbl 01

Table 1. Byte Selection Equivalency Assuming the 32-Bit Side Uses the *Little-Endian* Byte Ordering of Data

8-bit Side		32-bit Side			
A0	A1	BE0	BE1	BE2	BE3
0	0	X	X	X	0
0	1	X	X	0	X
1	0	X	0	X	X
1	1	0	X	X	X

2671 tbl 02

Table 2. Byte Selection Equivalency Assuming the 32-Bit Side Uses the *Big-Endian* Byte Ordering of Data

BUSY ARBITRATION LOGIC

Busy arbitration is performed only when there is an address match and the chip enables are active. The IDT7024 and the IDT7025 dual-port RAMs are provided with a master/slave (M/$\overline{S}$) pin through which the user can configure the busy logic on these devices to operate as masters or slaves. Busy arbitration is performed only by the master, which generates the busy signal. The master outputs a logic "0" on the busy line of the port that loses arbitration, at the same time it generates an internal write inhibit signal to block any write operation on the losing port. When configured to operate as slaves, these devices use the busy line as an input. The slave takes the busy line as an input and generates an internal write inhibit on the same port that received the busy. The upper and lower byte enable inputs do not affect the operation of busy logic in these devices. If busy logic and width expansion are being used, it is important that the $\overline{CE}$ of the master and the associated slave always be active at the same time. If the decoding logic allows the slave to be selected without the master, the busy logic will not operate correctly. Care has been taken in both Figures 3 and 4 to assure correct busy logic operation. It should be kept in mind, however, that busy logic is often not an essential part of a dual-port RAM-based system. The user is urged to read Application Note AN-02 for more information on busy logic arbitration.

INTERRUPT LOGIC

The IDT7024/IDT7025 dual-port RAM chips have interrupt generation capability that can be very effectively used to interrupt processors connected to either side of the dual-ports. A processor connected to the left port can generate an interrupt to the processor connected on the right port by writing to the topmost location in the memory array. In the case of the IDT7024, this location is FFF (Hex). The processor on the right port clears the interrupt by reading from this location, i.e. FFF (Hex). Similarly, the processor on the right port can interrupt the processor on the left port by writing to the topmost minus one location, i.e. FFE (Hex), for the IDT7024. The processor on the left port clears the interrupt by reading from location FFE (Hex).

Side	Set Address (HEX) (Write) (Interrupts the Other Side)	Clear Address (HEX) (Read) (Clears the Interrupt on This Side)
Using left port	FFF	FFE
Using right port	FFE	FFF

2671 tbl 03

Table 3. Interrupt Set and Clear Addresses for the IDT7024 Dual-Port RAMs

Side	Set Address (HEX) (Write)	Clear Address (HEX) (Read)
32-Bit side (Using left ports)	FFF	FFE
16-Bit side (Using right ports)	1FFC	1FFE
32-Bit side (Using right ports)	FFE	FFF
16-Bit side (Using left ports)	1FFE	1FFC

2671 tbl 04

Table 4. Interrupt Set and Clear Addresses for the 32-bit to 16-bit Interface Shown in Figure 3

Side	Set Address (HEX) (Write)	Clear Address (HEX) (Read)
32-Bit side (Using left ports)	FFF	FFE
8-Bit side (Using right ports)	7FFA or 7FFB	7FFC or 7FFD
32-Bit side (Using right ports)	FFE	FFF
8-Bit side (Using left ports)	7FFC or 7FFD	7FFA or 7FFB

2671 tbl 05

Table 5. Interrupt Set and Clear Addresses for the 32-bit to 8-bit Interface Shown in Figure 4

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Table 3 summarizes the interrupt set and clear addresses for the IDT7024 dual-port RAMs, while Tables 4 and 5 summarize the interrupt set and clear addresses for the interface shown in Figures 3 and 4. In the interface schemes illustrated in Figures 3 and 4, we have two dual-ports that have been used to expand the memory in width. This means that we can have two interrupt lines going active one for each chip. The schemes illustrated in Figures 3 and 4 show only interrupts from the master chip being used by either side, while the interrupts from the slave chip are not used.

SEMAPHORE ARBITRATION

The IDT7024 and IDT7025 are provided with semaphore logic in the form of eight dual-port semaphore flags that are independent of the memory array. These eight cells can be used to supervise the accesses to a maximum of eight blocks of memory. There is no hardware interaction between the semaphores and the RAM. Address bits A(m)R, A(m-1)R and A(m-2)R in Figure 3 are inputs to an IDT74FCT138 which decodes the dual-port RAM space and the semaphore space on the 16-bit side. Address bits A(m)R and A(m-1)R in Figure 4 are inputs to an IDT74FCT139 which decodes the dual-port RAM space and the semaphore space on the 8-bit side. Similarly, address bits A(n)L, A(n-1)L and A(n-2)L are inputs to another IDT74FCT138 which decodes the various address spaces on the 32-bit side. It is necessary to keep the dual-port memory space and the semaphore address space separate. Operating on the two spaces is a mutually exclusive operation and, therefore, chip enable ($\overline{CE}$) and the semaphore enable ($\overline{SEM}$) inputs must never be active at the same time. The semaphore cells are intended to assist software-based protocols intended to prevent address collisions.

The IDT semaphore cells are designed to be used in a clear-and-test sequence. Each cell is normally in the "1" state, indicating that neither side has been assigned the associated block of memory ("No grant"). To access a particular block of memory, one must perform the clear-and-test sequence necessary to get a "grant" from the semaphore cell representing the block. To get a "grant", one must select the semaphore cell representing the associated block of memory, write a "0" (request) to the semaphore cell and then read (test) the semaphore cell to see if a "0" was put out by the cell.

A semaphore cell is selected by asserting the semaphore enable line ($\overline{SEM}$) and by selecting one of the eight semaphore cells with the help of the three lower most address lines A2 - A0. In the read operation, if the semaphore cell is a "0", that particular block of memory is "available" for use by the side requesting access. If the semaphore cell is a "1", the side requesting access has a "no grant" and that particular block of memory is in use by the other side. In the IDT7024 and IDT7025, the semaphore cells broadcast the "grant" or "no grant" condition on the entire sixteen bits of the data pins. The status of the upper and lower byte enables has no effect on the semaphore request operation.

Semaphore Address			Selected Semaphore Cell
A2	A1	A0	
0	0	0	Sem Flag 0
0	0	1	Sem Flag 1
0	1	0	Sem Flag 2
0	1	1	Sem Flag 3
1	0	0	Sem Flag 4
1	0	1	Sem Flag 5
1	1	0	Sem Flag 6
1	1	1	Sem Flag 7

2671 tbl 06

Table 6. Semaphore Address Map for the 32-bit Side in Figures 3 and 4

Semaphore Address				Selected Semaphore Cell
A3	A2	A1	A0	
0	0	0	X	Sem Flag 0
0	0	1	X	Sem Flag 1
0	1	0	X	Sem Flag 2
0	1	1	X	Sem Flag 3
1	0	0	X	Sem Flag 4
1	0	1	X	Sem Flag 5
1	1	0	X	Sem Flag 6
1	1	1	X	Sem Flag 7

2671 tbl 07

Table 7. Semaphore Address Map for the 16-bit Side in Figures 3

Semaphore Address					Selected Semaphore Cell
A4	A3	A2	A1	A0	
0	0	0	X	X	Sem Flag 0
0	0	1	X	X	Sem Flag 1
0	1	0	X	X	Sem Flag 2
0	1	1	X	X	Sem Flag 3
1	0	0	X	X	Sem Flag 4
1	0	1	X	X	Sem Flag 5
1	1	0	X	X	Sem Flag 6
1	1	1	X	X	Sem Flag 7

2671 tbl 08

Table 8. Semaphore Address Map for the 8-bit Side in Figures 4

Consistent with the rest of our discussion on busy logic and interrupts, we will consider the semaphore flags in the IDT7024 containing the lower order sixteen bits of data (master). When the 32-bit side in Figures 3 and 4 reads the semaphores, the processor on the 32-bit side will look at the lower sixteen bits only to check for a "grant" or a "no grant" condition. The 16-bit and 8-bit sides access the semaphore space in Figures 3 and 4 and must read the master IDT7024 containing only the lower sixteen bits to check for a "grant" or a "no grant" condition. (Refer to Tables 6, 7 and 8.)

SUMMARY

Interfacing various buses with the help of dual-ports can be implemented very easily and with a minimum of components. Byte reordering can also be accommodated easily. IDT7024 and IDT7025 dual-port static RAMs have built-in arbitration schemes, upper and lower byte enables, and pin selectable master/slave functions. These features have been designed to aid system designers in their quest for compact, simple and more reliable designs.

Integrated Device Technology, Inc.

USING IDT71502 RAMs IN A REAL-TIME DEBUGGING TOOL FOR A R3000 MICROPROCESSOR BASED SYSTEM

APPLICATION NOTE AN-67

by Bhanu V. R. Nandurl

INTRODUCTION

The proliferation of high-speed RISC and CISC microprocessors has created a demand for real-time debugging tools. This application note shows how a real-time logic tracing tool can be created using IDT71502 multifunction RAMs. The IDT71502 can be used as a stand-alone logic analyzer or as part of an embedded fault monitor and analysis system. Details of how to apply this system to an R3000 RISC microprocessor-based system are given. The discussion in this paper is also equally valid for use in high-speed CISC processor-based designs.

The IDT71502 can be used to function either as a logic tracing device or as a test pattern generator. As a logic tracing device the IDT71502 can record bus activity continuously and then be stopped on a predetermined event such as a bus error. This allows the activity leading up to the "event" to be recorded for analysis. Since the trace function is accommodated in a single device, embedded tracing is more likely to be practical.

DESCRIPTION OF IDT71502 MULTIFUNCTION RAM

IDT71502 is a 4K x 16 multifunction RAM with an address set-up time of 25ns. It has a breakpoint comparator,16-bit pipeline register and an address counter. In addition, there is a 16-bit set-up register used to set the chip operating mode and to read back chip operating status conditions. It includes a serial control interface called the serial protocol channel (SPC™) which is available in a variety of other products from IDT as well. The SPC logic, as implemented in the IDT71502, has one 8-bit command shift register, a command decode register and a 16-bit data shift register. The serial data shift register can be configured to operate in a diagnostic mode. In the diagnostic mode of operation, the shift register can read all status conditions on the chip such as the RAM output, pipeline register output, data output pin state and RAM load/read counter value.

The serial protocol channel consists of a four-pin interface bus through which the user can access the internal registers of the IDT71502. The four pins are:

(a) Serial data input pin (SDI) for sending data and commands to the device.
(b) Serial data output pin (SDO) for extracting data from the device.
(c) Serial clock pin (SCLK) for clocking data and commands.
(d) Command/Data mode pin (C/$\overline{D}$) to provide command or data identification to the device.

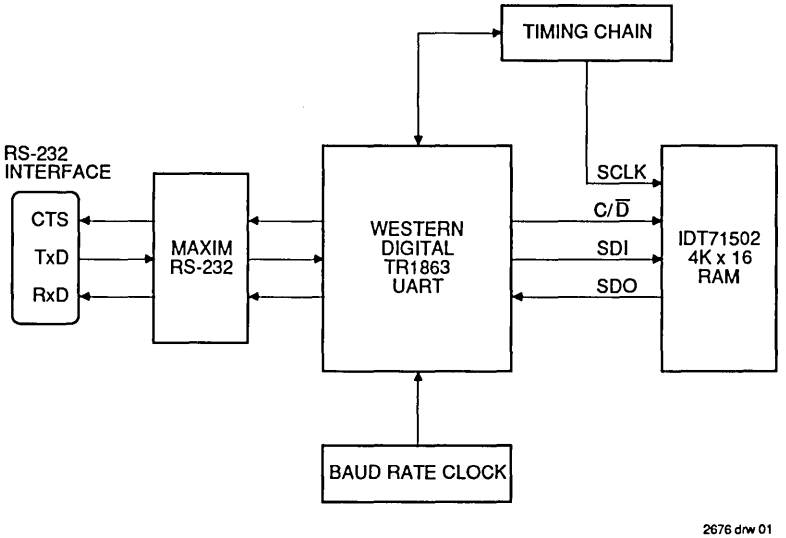

Figure 1.

SPC is a trademark of Integrated Device Technology, Inc.

This four-bit bus can be very conveniently connected to an RS-232C line for direct serial communication with a computer and Figure 1 illustrates one scheme to achieve this. The user is urged to refer to the "IDT71502 FUNCTIONALITY DEMONSTRATION BOARD USER MANUAL" for more information on interfacing the IDT71502 to the RS-232C serial communication line. The SPC's eight bit command is divided into a *four-bit command field* and a *four-bit register field.* The four-bit command field is used to determine whether a read or a write operation will be executed. The four-bit register field of the command register is used to select the various internal registers and the external pins on which the read or write will take place. Thus, the four-bit command field and the four-bit register field can effectively access any internal register for a read or a write operation and monitor the state of the external pins.

Table 1 summarizes the SPC commands, and Register codes and the set-up register format. When the command/$\overline{\text{data}}$ line is high, commands are serially clocked through the SCLK into the internal command register via the serial data input pin (SDI). When the command/$\overline{\text{data}}$ line is low, data is serially clocked by the SCLK into the internal data register via the serial data input pin (SDI). The SPC commands are executed whenever the C/$\overline{\text{D}}$ line transitions from a command mode (logic 1) to a data mode (logic 0). This device, when configured to operate in the trace mode, serves as a real-time debugging tool analogous to a logic analyzer.

SET-UP/STATUS REGISTER CODE

Bit	Name	Operation Performed
15	CE	Read Only
14	$\overline{\text{SOE}}$ FF	Read Only
13	$\overline{\text{SOE}}$ Pin	Read Only
12	$\overline{\text{OE}}$ Pin	Read Only
11	$\overline{\text{WE}}$ Pin	Read Only
10	$\overline{\text{INIT}}$ Pin	Read Only
9	BP Compare	Read Only
8	BP Pin	Read Only
7	$\overline{\text{CS1}}$	Read/Write
6	$\overline{\text{CS0}}$	Read/Write
5	Non-Reg High	Read/Write
4	Non-Reg Low	—
3	—	—
2	BC-ADDRS	Read/Write
1	BC Pipelined	Read/Write
0	Trace Mode	Read/Write

2676 tbl 01

SPC COMMAND CODES

Command Code (Hexadecimal)	Read/Write Function	Operation
0	Read	Read Register
1	Write	Write Register
2	Read RAM	Read RAM and Increment Counter
3	Write RAM	Write RAM and Increment Counter
4-C	Reserved	(Reserved NO-OP)
D	Write	Stub Diagnostic
E	Write	Serial Diagnostic
F	Reserved	(Reserved NO-OP)

2676 tbl 02

SPC REGISTER CODES

Register Code (Hexadecimal)	Read/Write Function	Register
0	Read/Write	RAM Counter
1	Read/Write	RAM Output/Input
2	Read/Write	Pipeline Register
3	Read/Write	Break Mask Register
4	Read/Write	Break Data Register
5	Read/Write	Setup and Status Register
6	Read Only	I/O15 - I/O0 (Data Pins)
7	Read Only	RAM Address Pins
8-F	Reserved	Reserved (Unused)

2676 tbl 03

Table 1.

AN R3000-BASED SYSTEM

A block diagram of a R3000-based system's CPU and its memory interface is shown in Figure 2. It consists of the CPU and FPU, data and instruction caches and the read and write buffers connected to the CPU and the system bus. This is a typical configuration found in embedded or general purpose-type systems which use the R3000. To reduce the burden of the system designer who is interested in using the IDT79R3000, the CPU and FPU, as well as the instruction and data caches with the read and write buffers, are now available in a compact module (IDT7RS101) which can be connected to the user's system bus. This approach to system design vastly reduces the design cycle time by shifting the design emphasis to main memory and I/O interfaces.

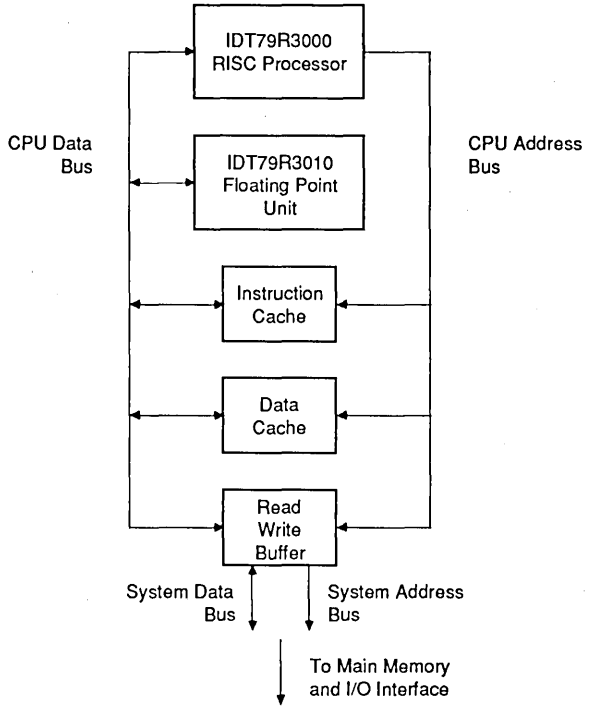

Figure 2. A Generic R3000 Microprocessor Based System

When debugging a system board based on the IDT7RS101 or its equivalent, the majority of debugging is done by monitoring the cache to main memory interface on the main memory side of this interface. An embedded trace function may operate in the same way. This keeps the capacitance of the trace RAM pins out of the speed critical cache buses. If desired, the R3000 can be operated in the uncached mode. This forces all accesses to main memory and allows every memory access of the processor to be monitored from the cache to main memory interface. The user wishing to operate in the uncached mode can do so by setting bit 11 of the TLB entry register to 1, indicating uncached mode, or operate the software in virtual address space kseg1. Kseg1 is kernal-mode virtual addressing space which is uncached and is 512 Mbytes long starting at virtual address 0xa000_0000. With this approach, the user must define instruction space and data space in the main memory and must provide an address decoded input to the IDT71502 tracing the control bus. This input will be used to determine whether an instruction or data related transaction occurred during that clock period.

Another approach is to tie the address valid bit on the TAG bus to ground via a 300 Ohm resistor. This is necessary to prevent a direct short from occurring when the CPU is driving the TAG bus. Tying the address valid bit on the TAG bus to ground will result in invalidating the cache TAGs and cache misses will occur, resulting in the processor accessing main memory to get that information. Whenever the main memory is accessed to get information after a cache miss, the processor puts out information on the Access Type pins, indicating the size of the word to be transferred and that it was a cached reference. AccTyp(2) pin output indicates a cached reference when 1 and an uncached reference when 0. AccTyp(0)

indicates a Data reference when 0 and an instruction reference when 1. The AccTyp signals are latched using our control trace RAM and will determine whether an instruction or data transaction occurred during that clock period.

A user wishing to implement his own cache can use the IDT71502 in the trace mode to monitor the cache. However, it should be pointed out that the timing for this part of his system is more stringent. The user may have to register trace data before clocking it into the IDT71502s to meet the IDT71502s set-up and hold time restrictions.

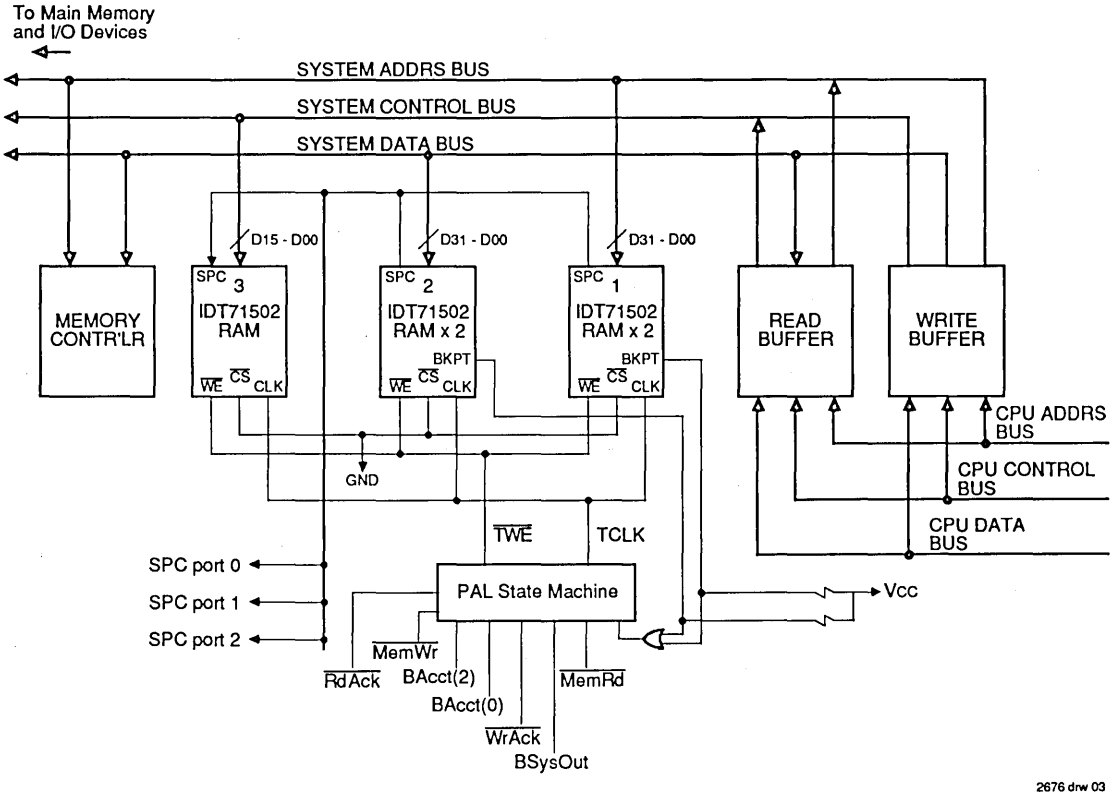

Figure 3. Block Diagram to Trace Instructions, Data, Instruction Addresses and Data Addresses on the System Bus of an R3000-based System

DESCRIPTION OF THE MONITOR CIRCUIT

Figure 3 shows the block diagram of an implementation of the monitor circuit. It is placed on the system bus between main memory and the write buffer of the R3000. The R3000 uses the write through cache update policy to ensure data coherency. The function of the write buffer is to capture data and addresses output by the CPU and ensure that data is passed on to main memory. The read buffer is used for temporary storage of data during data transfers between main memory and the CPU. Depending on the block refill size, the read buffer can be 1, 4, 8, 16 or 32 words deep. The block refill size of the system is fixed during the system reset operation. The R3000's CpCond0 input can be set to a 0 to indicate a single word transfer or can be set to a 1 to indicate a block transfer by the external memory controller. The PAL state machine is used to generate the appropriate IDT71502 strobes to capture instructions, data, instruction addresses and data addresses.

The IDT71502s labeled "1" in Figure 3 is used for capturing data and instruction addresses; IDT71502s labeled "2" is used for capturing data and instructions. The IDT71502 labeled "3" is used to trace the control bus signals. In this application note, we assume a single word deep read buffer. If a system is designed for all possible types of data transfers (i.e bytes, half words, tribytes, words and block refills), our PAL equations will also have to change to generate the strobes necessary to trace these data transfers.

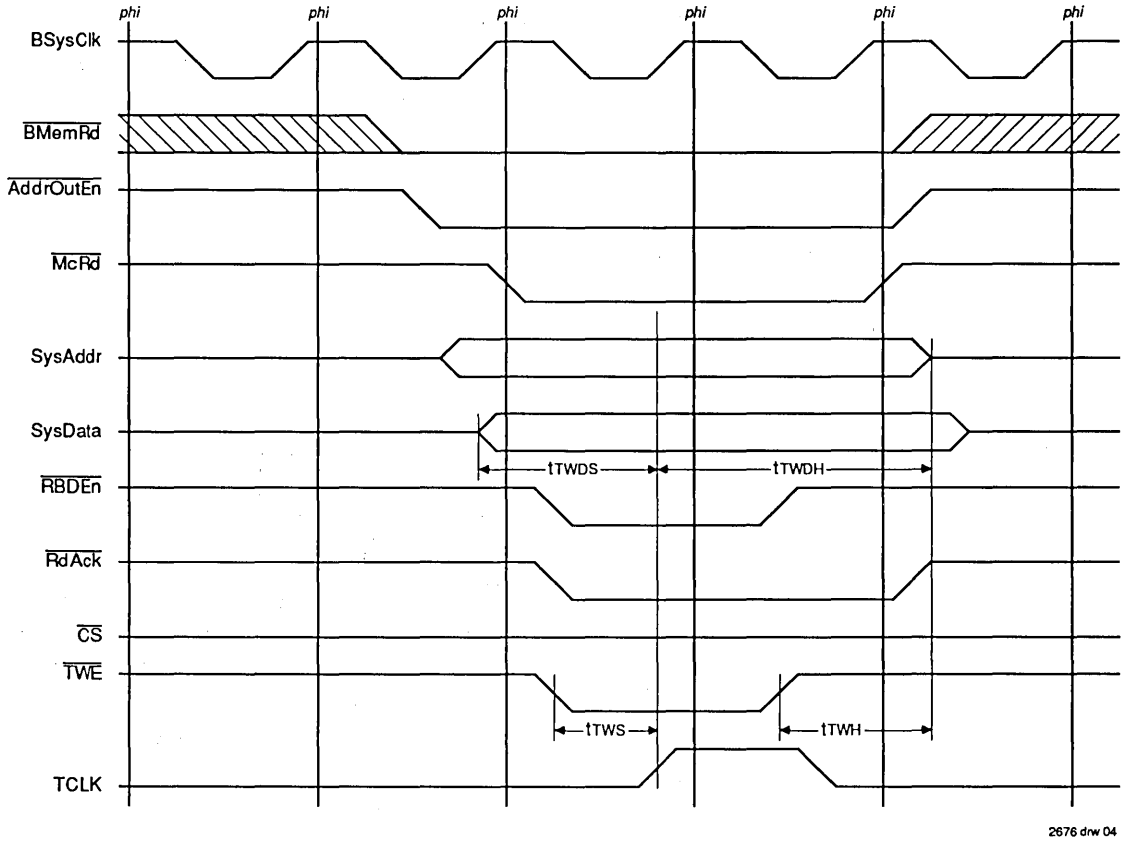

Figure 4. Main Memory Read Cycle (Single Word Read)

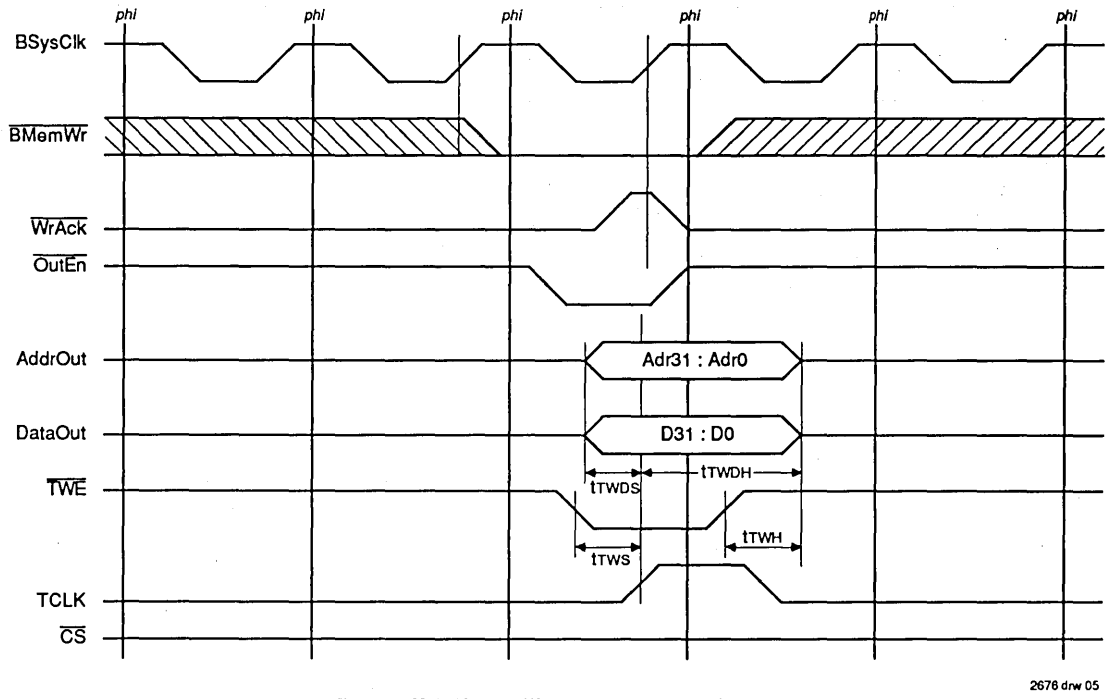

Figure 5. Main Memory Write Cycle (Single Word Write)

TIMING ANALYSIS

Figure 4 is the timing waveform for a single word read and Figure 5 is the timing waveform for a single word write. Since the system bus timing parameters are dependent on an external memory controller, Table 2 summarizes the important handshaking signals needed to satisfy the protocol necessary to trace system bus signals.

AddrOutEn is an input to the read buffer from the main memory controller. When asserted, this input will enable the address that is registered in the read buffer to the system bus. McRd is a read strobe that is generated by the main memory controller in response to a MemRd pulse from the R3000. RBDEn is a main memory controller input to the read buffer that registers the data available on the system data bus into the read buffer.

WrAck is an input to the write buffer from the main memory controller. It indicates that it has written the word presented to it to main memory. RdAck is also a main memory controller output that is used to generate the RdBusy signal to the R3000. TWE is an input to the IDT71502s that latches data addresses, instruction addresses, data, and instructions; it is also an output from our PAL state machine. TCLK is the clock input to the IDT71502s tracing data addresses, instruction addresses, data, and instructions. The signals TWE and TCLK are also used as inputs to the IDT71502s in order to trace the control bus signals.

Signal	Function
$\overline{\text{BMemRd}}$	The buffered memory read signal from the R3000
$\overline{\text{BMemWr}}$	The buffered memory write signal from the R3000
$\overline{\text{AddrOutEn}}$	Read buffer address output enable signal from the memory controller
$\overline{\text{McRd}}$	Main memory read strobe from the memory controller
$\overline{\text{RBDEn}}$	Read buffer data enable strobe from memory controller
$\overline{\text{WrAck}}$	Write acknowledge to write buffer from memory controller
$\overline{\text{RdAck}}$	Read acknowledge to read buffer from memory controller
$\overline{\text{TWE}}$	Write enable input to IDT71502 from PAL state machine
TCLK	Clock input to IDT71502 from PAL state machine

2676 tbl 04

Table 2.

TIMING SPECIFICATIONS FOR THE IDT71502s

t_{TWDS} is the IDT71502 specification defined as "Trace Write Data Set-up Time". The user must satisfy the following condition:

$$t_{TWDS} \geq 8ns$$

t_{TWDH} is the IDT71502 specification defined as "Trace Write Data Hold Time". The user must satisfy the following condition:

$$t_{TWDH} \geq 2ns$$

t_{TWS} is the IDT71502 specification defined as "Trace Write Enable Set-up Time." The user must satisfy the following condition:

$$t_{TWS} \geq 8ns$$

t_{TWH} is the IDT71502 specification defined as "Trace Write Enable Hold Time." The user must satisfy the following condition:

$$t_{TWH} \geq 2ns$$

CONCLUSION

The IDT71502 is a multifunction RAM that is fast enough to be used to trace the operation on most high-speed microprocessors including the IDT79R3000 RISC microprocessor. The 25ns speed grade can be used to trace full speed the operation of this processor up to 25MHz. The discussion in this paper focused on providing the pertinent information needed to construct a monitor circuit based on IDT71502 multifunction RAMs to trace the system bus of an R3000-based system. This discussion is also valid for users interested in using the IDT71502 RAMs in a trace mode to monitor system buses based on other high-speed processors.

Microprocessor based systems are usually provided with software routines that are used as diagnostic tools to test system primary and secondary memory for failures. These programs also test I/O devices before the user receives a prompt, telling him the system as a whole is ready for service. This procedure is usually carried out after system reset, but occasionally during normal operation the system "crashes" in the middle of some critical task and the user has no clue as to what happened prior to the "crash". The IDT71502 multifunction RAMs, when operated in trace mode and mounted permanently on critical system paths, can serve as "black boxes" to give the user this very important information. This information can then be very conveniently retrieved via the four bit serial protocol channel connected to the RS-232 connector and the reason for the crash can be determined.

The IDT71502 is a multifunction RAM that has the capability to serve as a valuable logic monitoring tool. It contains the Serial Protocol Channel and a breakpoint comparator, has a 4K x 16 memory space and is available with an access speed of 25ns. Thus, it is well-suited for use as a single chip logic analyzer in high-speed, high-density environs.

Integrated Device Technology, Inc.

DUAL-PORT RAM SIMPLIFIES PC TO TMS320 INTERFACE

APPLICATION NOTE AN-68

by Jim Handy & Barry Seldner Integrated Device Technology, Inc.
Jon BradleyTexas Instruments, Inc.

This application note describes a "no hassels" interface between the IBM PC-style backplane and a TMS320C30 DSP chip via an IDT dual-port static RAM. The interface provides an extremely simple means of downloading cross-compiled DSP code as well as sample data sets for debugging a high speed TMS320 based system in real time.

This example also shows how easily interprocessor communications hardware can be implemented via the simple insertion of a dual-port RAM between a DSP chip and a general purpose processor in a standard DSP system. A system like this one would typically use a standard CPU for data input/output and ordering, and would pass complete data sets to the DSP chip for intense calculation. Similar architectures are often used in graphics and image processing, where an entire image is manipulated as a single data set, in transform calculations (i.e. FFTs) for sonar and radar processing. Certain systems even use this scheme several times with numerous DSP chips in order to get processing speeds proportional to the number of DSP chips in the system.

SYSTEM OBJECTIVE

The design presented here is the TMS320C30 Software Development Board. This board is one portion of a system which helps the TMS320C30 programmer to download and debug code from an IBM PC or similar computer. In order to support the special hardware needs of the TMS320C30 programmer, an expansion connector allows memory to be added to the DSP chip's primary bus, while a target connector provides a fully buffered version of the chip's expansion bus to allow its connection to special purpose hardware. Most of the TMS320C30's status signals are also routed to the expansion bus to make them available to the hardware being debugged.

The majority of the control software is PC-resident, and is provided on magnetic media. This includes such tools as the assembler, compilers, and download and debug routines. A 2K x 32 EPROM array on the primary bus of the TMS320 provides the host processor with a set of commands to allow it to load the software development board's RAMs, to set and clear breakpoints, to examine and preset internal status, and to load or store values in individual memory locations. All of these are controlled by the host's sending a command to the TMS320, which interprets that command and takes appropriate action.

A high speed 16K x 32 static RAM is attached to each of the DSP chip's two buses: the expansion bus, and the primary bus. The expansion bus' RAM would typically be used to store a data set to be operated upon, and the primary bus' RAM would be used to store code which would be debugged using this board. Both of these RAMs are zero wait-state (25ns access times at 33MHz) to allow real-time debugging and benchmarks to be performed. Since the TMS320's expansion bus only supports addressing of up to 8K locations, a bank select signal is used to switch between the upper and lower halves of this port's 16K x 32 memory. This signal is software-controlled from the processor's expansion bus.

One design goal for this system was to move data into and out of the DSP's dedicated memory without taking an inordinate amount of time or hardware. If standard memory were to be shared between the host and the DSP chip, multiplexing logic would need to be inserted between each processor and the RAM's address, data, and control lines. This logic would find itself right in the critical timing path of the memories on the primary and expansion buses, and would make zero wait-state operation nearly unachievable. An additional headache would have been finding room on the board for the large amount of multiplexing logic required. Should the design have used a simpler method of passing data back and forth between processors either via a UART or a single byte-wide I/O buffer, the developer would have had to endured long delays during download and other communication functions as the software on either side of the port performed massive amounts of handshaking to pass even the smallest of data sets.

It became obvious early in the design cycle that the simplest method of performing fast host to DSP communication would be to use a large high-speed true dual-port static RAM to perform interprocessor communications. A dual-port RAM would allow both the host and the DSP chip to transfer data in packets, rather than as individual bits or bytes, thus accelerating downloading. The selected dual-port device would have to be one which provided some means of signalling that data packets were ready to be handed back and forth between processors.

An IDT71342 was chosen because of its speed, its depth (4K bytes), the simplicity of its interface, and its ability to perform interprocessor communications through its eight internal semaphore flags (see Appendix: "Dual-Port Semaphores"). By using an IDT71342, the designers could use a single chip to implement 4K byte high speed block transfers between the host and the TMS320, and to signal the completion of a transfer without additional hardware. Although the 45ns access time dual-port used in this system does not support zero-wait data transfers at maximum CPU speeds, data transfers are not in the critical path of the sort of software this system is used to debug. Still, a true zero-wait state system

9

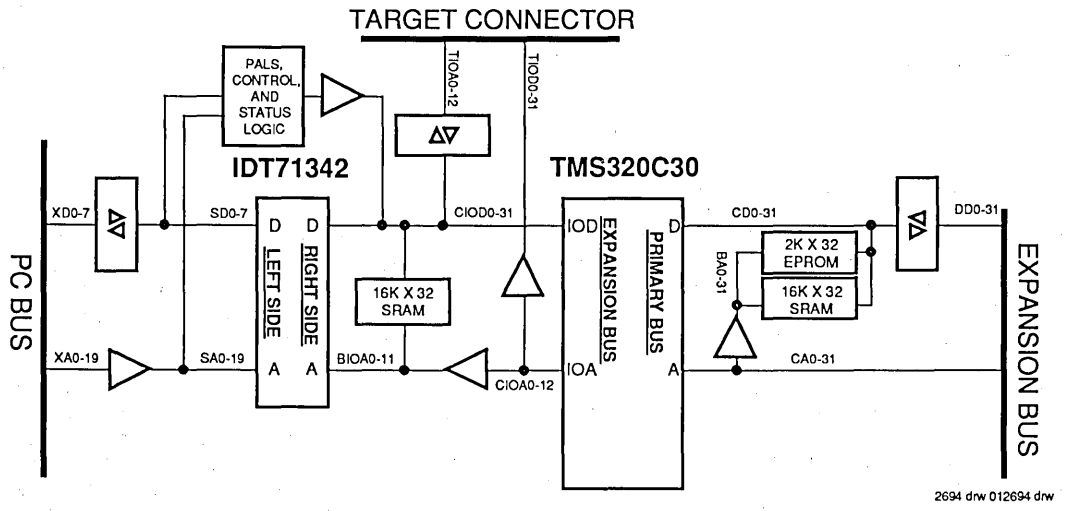

Figure 1. TMS320C30 Software Development Board Block Diagram

could have been realized had the designers used a 25ns dual-port.

Figure 1 shows a block diagram of the complete system. The full schematic of the system is shown in Figure 6.

INTERFACING TO THE DUAL-PORT RAM

The IDT71342 dual-port RAM uses an interface which is similar to any standard single-port byte wide static RAM. Each of the two ports (Left and Right) uses a separate set of control, address, and I/O pins. Address inputs are not multiplexed with data I/O. The control interface consists of three pins on either side: read write (R/$\overline{W}$), output enable ($\overline{OE}$), and chip enable/power down ($\overline{CE}$). The R/$\overline{W}$ and $\overline{OE}$ pins also operate in conjunction with the semaphore select pin ($\overline{SEM}$), which imitates the functionality of the chip enable pin, but rather than allowing reads and writes of the memory array, this pin routes the read and write control to the eight on-chip semaphore flags.

Write cycles are controlled by the simultaneous application of a logic low on both the CE and R/W inputs for one side of the RAM, and either signal can be used to control the timing of a write cycle. If the $\overline{CE}$ signal is held low and the timing is set by a low pulse on the R/$\overline{W}$ pin, it is called a "R/$\overline{W}$ controlled write cycle" *(figure 2)*. Write cycles where R/$\overline{W}$ stays low while $\overline{CE}$ is pulsed low are called "$\overline{CE}$ controlled write cycles" *(figure 3)*. By offering both methods of communication, IDT's dual-port RAMs can be easily connected between systems with greatly differing bus interface specifications. An interesting point about this design is that while the PC or host side of the dual-port uses a R/$\overline{W}$ controlled write cycle, the DSP writes to its side of the dual-port by using a $\overline{CE}$ controlled write cycle.

THE PC BUS INTERFACE

In this design, the PC bus' control signals are routed nearly directly from the backplane to the IDT71342's R/$\overline{W}$ and $\overline{OE}$ pins. The signal functions and timing of the backplane are an ideal match with those of the dual-port RAM. However, a decision was made to map the memory array into a 4K space in the PC's memory space, while the semaphores were to be mapped into the PC's I/O space, which forced the $\overline{IOW}$ and $\overline{MEMW}$ signals to be ORed before driving them into the IDT71342's R/$\overline{W}$ input. Likewise $\overline{IOR}$ and $\overline{MEMR}$ signals are ORed before driving them into the IDT71342's $\overline{OE}$ input.

The dual-port's chip enable ($\overline{CE}$) pin is driven indirectly by an address decoder consisting of an eight bit comparator 74ALS521 which compares the output of a 74LS377 register with addresses A12-A19. The 74LS377 is an I/O mapped register that allows the dual-port RAM to be mapped into any 4K-byte region in the PC's main memory space. A PAL resident control register bit on the board allows the dual-port memory to be disabled, which is its state at power-up or reset.

The semaphore enable pin ($\overline{SEM}$) is driven by a 20L8 PAL which decodes addresses from the PC Bus. This decoder determines whether the host is accessing memory or I/O space via the $\overline{MEMR}$, $\overline{MEMW}$, $\overline{IOR}$, and $\overline{IOW}$ signals, and enables the semaphores during an I/O access if the proper address (A0-A9) is applied to the inputs of the PAL. The PAL also uses the $\overline{IOW}$ and $\overline{MEMW}$ signals to generate a R/$\overline{W}$ controlled write cycle, while using decoded addresses to drive the $\overline{CE}$ and $\overline{SEM}$ inputs.

All data and address pins of the IDT71342 are isolated from the backplane with TTL buffers. A detail of the PC to dual-port interface is shown in Figure 4.

The reader should note that several considerations increased the complexity of this interface. If this design had

involved a dedicated host processor rather than a general purpose PC, the need for buffering would probably have been drastically reduced. Had both the 4K byte RAM and the semaphores been mapped into the memory space of the host, no ORing would have been required on the $\overline{MEMW}$, $\overline{MEMR}$, $\overline{IOW}$, and $\overline{IOR}$ signals. Finally, a very complex address decoder was implemented in this system to allow the IDT71342's RAM to be mapped anywhere within the PC's memory space. By using a more straightforward fixed-address scheme, logic complexity could be significantly reduced. It is conceivable that the entire interface including address decoding could have been handled with a single IC.

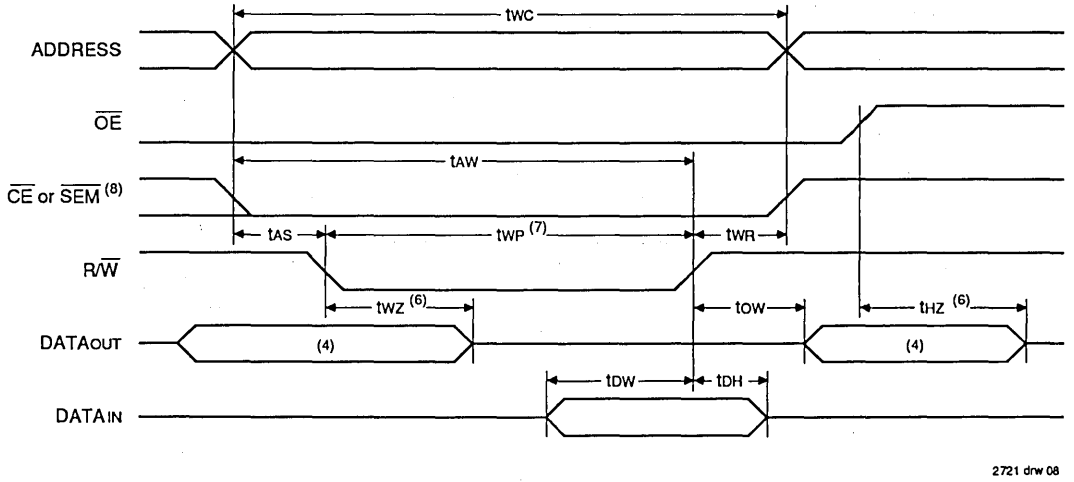

Figure 2. Timing Waveform of R/$\overline{W}$ Controlled Write Cycle

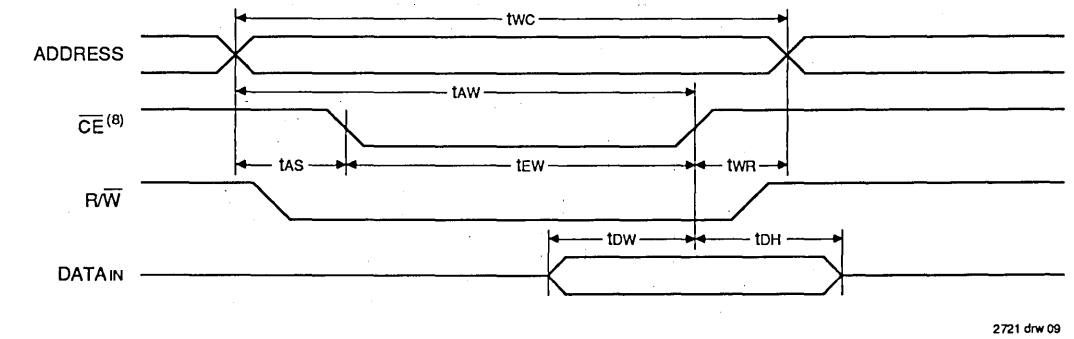

Figure 3. Timing Waveform of $\overline{CE}$ Controlled Write Cycle.

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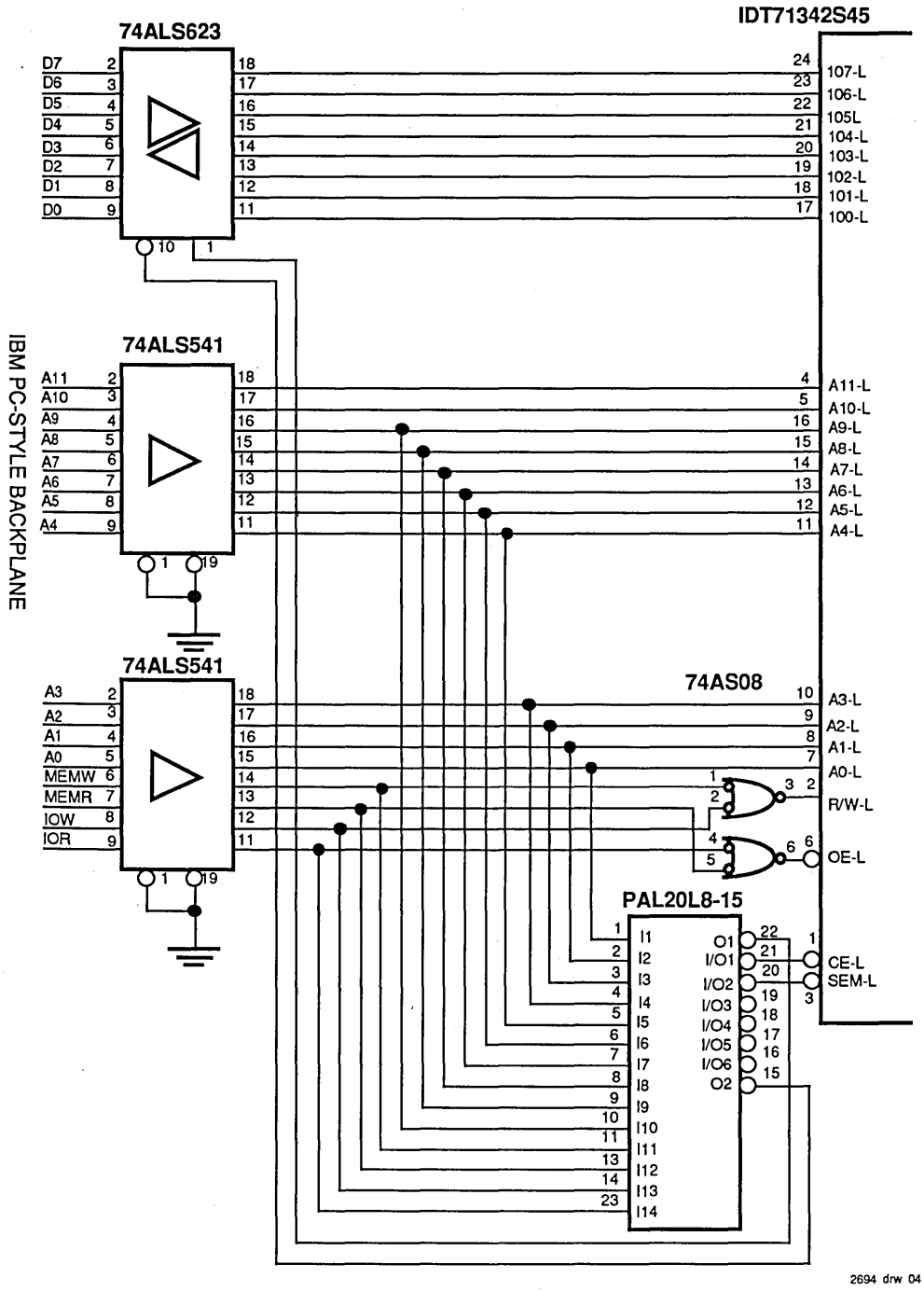

Figure 4. PC Bus to IDT71342 Dual-Port Interfacew (Left-Hand Side of Dual-Port).

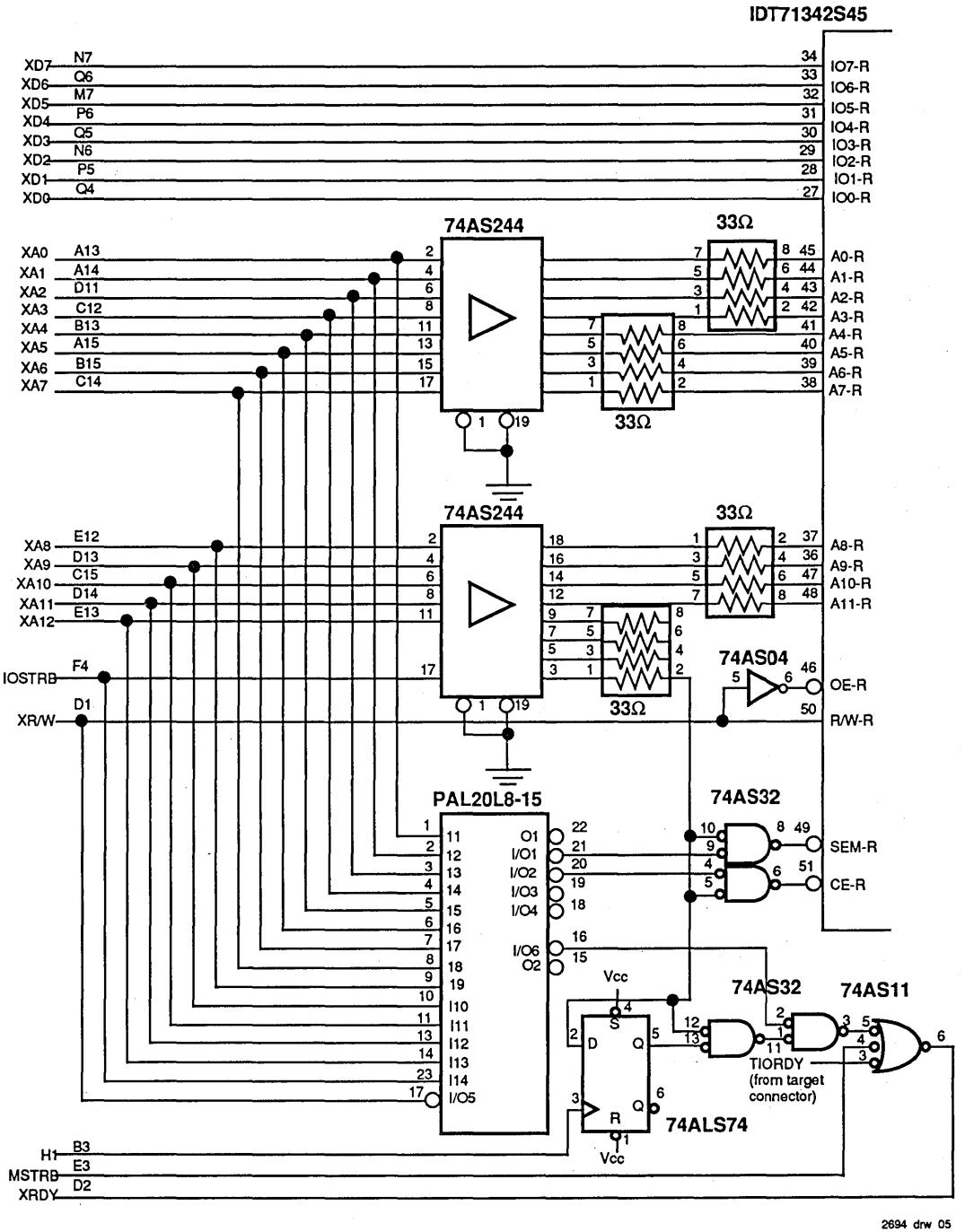

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Figure 5. TMS320C30 to IDT71342 Dual-Port Interface (Right-Hand Side of Dual-Port).

THE TMS320C30 INTERFACE

The TMS320 interfaces to the dual-port RAM through the I/O strobe on the expansion bus. The same bus is used to interface to a 16K x 32 static RAM via its memory strobe signal. These two strobes signify two different ranges on the DSP chip's internal address map. A detailed diagram of the TMS320 to IDT71342 interface is shown in Figure 5.

As in the PC bus interface, the address lines are buffered between the processor and the dual-port RAM, however the light loading on the data bus removes the need for data buffering on this side. The only devices connected to the data pins are: the dual-port RAM, the DSP chip, a static RAM, a status latch, and a transceiver. The address bus needed buffering since all eight 16K x 4 RAM chips, as well as the dual-port, a PAL, and an address buffer are attached to these pins.

The TMS320's expansion bus uses a strobe to activate an I/O cycle, and a level to distinguish read cycles from write cycles. In this design, the expansion read/write (XR/$\overline{W}$) output of the TMS320 is connected directly to the IDT71342 dual-port to drive the read/write (R/$\overline{W}$) input, and is simply inverted to drive the output enable ($\overline{OE}$) input. This inverter is not truly necessary, since the dual-port places its data outputs into a high-impedence state automatically upon the application of a write (low) level on the R/$\overline{W}$ input. The $\overline{OE}$ pin on this side could have been permanently tied active (grounded).

A 20L8 PAL is used to control the chip enable ($\overline{CE}$) input for this side of the dual-port RAM. This signal is a decoding of the DSP's expansion bus address bits XA0-XA12. The PAL used in this interface had too few product terms to allow the combination of the I/O strobe with the decoded address, so the buffered I/O strobe ($\overline{BIOSTRB}$) has been externally ANDed with the decoded address output from the PAL before being fed into the dual-port. The semaphore select is handled the same way, but a different address decoding is used from the same PAL, and the I/O strobe is ANDed through a different gate into the semaphore ($\overline{SEM}$) input of the dual-port. Both of these signals can be disabled by writing to the control register.

The TMS320C30 writes to the dual-port RAM by implementing a $\overline{CE}$ controlled write cycle. The $\overline{CE}$ and $\overline{SEM}$ inputs are driven by two-input OR gates. One of the inputs of each of these gates represents a decoded address output from a 20L8 PAL, while the second input is driven by a buffered version of the I/O strobe. The only other qualifying input is the read/write (R/$\overline{W}$) input, which is directly driven by the expansion read/write (XR/$\overline{W}$) signal on the TMS320. When the DSP chip writes to the dual-port, the address and read/write signals are output first, followed by the I/O strobe. Since $\overline{IOSTRB}$ is used to gate the $\overline{CE}$ or $\overline{SEM}$ signal, the timing meets the criteria for a $\overline{CE}$ controlled write cycle.

The expansion ready ($\overline{XRDY}$) input to the TMS320, which tells it that the expansion bus cycle is complete, is a combination of the decoded address range from the PAL and a clock delay from the TMS320's H1 (clock/2) output. This signal is required for systems using slower dual-port RAMs, but is not necessary in systems where faster dual-ports are used. If the system designer choses a 25ns or faster part for use in a 33MHz TMS320C30 system, the $\overline{XRDY}$ input can be generated immediately upon accessing the dual-port RAM.

The gating used here generates a single wait-state on any I/O strobe within the address range of the IDT71342. This logic could be removed if a faster IDT71342 were used. On an $\overline{IOSTRB}$ output from the TMS320, if the PAL decodes a dual-ported address, the strobe and decoded address are combined in the second of the two AND gates in fig. 5. This AND gate's output is fed into the $\overline{XRDY}$ OR gate to extend the expansion bus cycle. On the next rising edge of H1, the $\overline{IOSTRB}$ is clocked into the flip flop. This flip flop's output is connected to the first AND gate and disables the $\overline{IOSTRB}$ from reaching the second AND gate. This in turn allows the $\overline{XRDY}$ input to the TMS320 to go active, and allows the cycle to end. A single wait-state more than compensates for the 45ns address access time of the dual-port used in this application. Other signals called target I/O ready ($\overline{TIORDY}$) from the target connector, and the $\overline{MSTRB}$ signal from the DSP chip itself can also signal an expansion bus ready state. Since the $\overline{MSTRB}$ signal is used only to control accesses to the expansion bus' 16K x 32 zero wait-state RAM, it is ORed directly back to the $\overline{XRDY}$ input through the 74AS11 gate as shown.

CONCLUSION

The TMS320C30 Software Development Board shows the simplicity of designing an interface between a TMS320 DSP chip and the IBM PC bus using an IDT71342 dual-port RAM. The dual-port RAM serves to reduce component count, increase interprocessor communications throughput, and simplify design. Designers should be able to follow the example given here to profitably use dual-port RAMs to handle communications in any similar dual processor system.

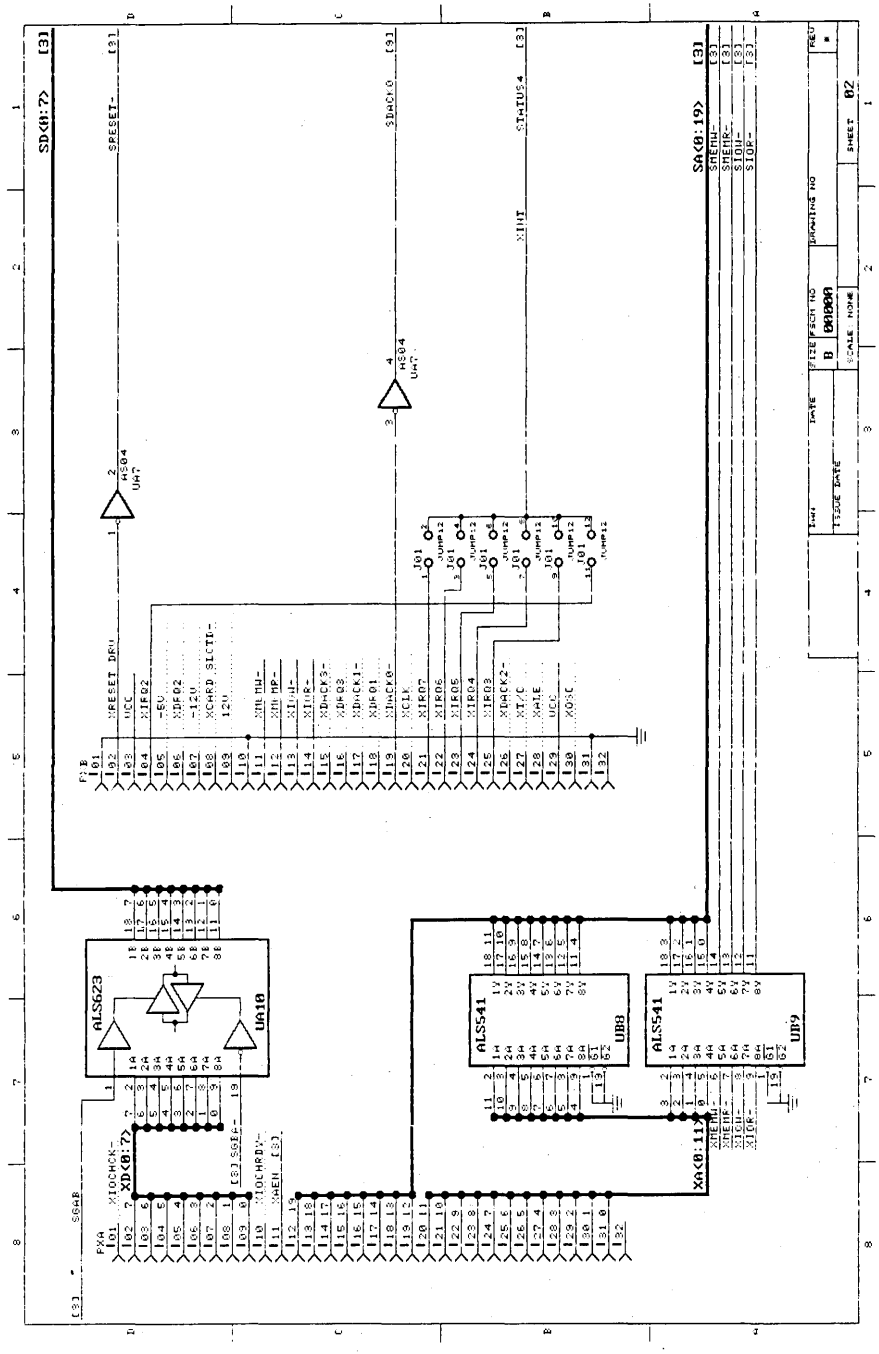

Figure 6. Complete Schematic of TMS320C30 Software Development System (section 1 of 9)

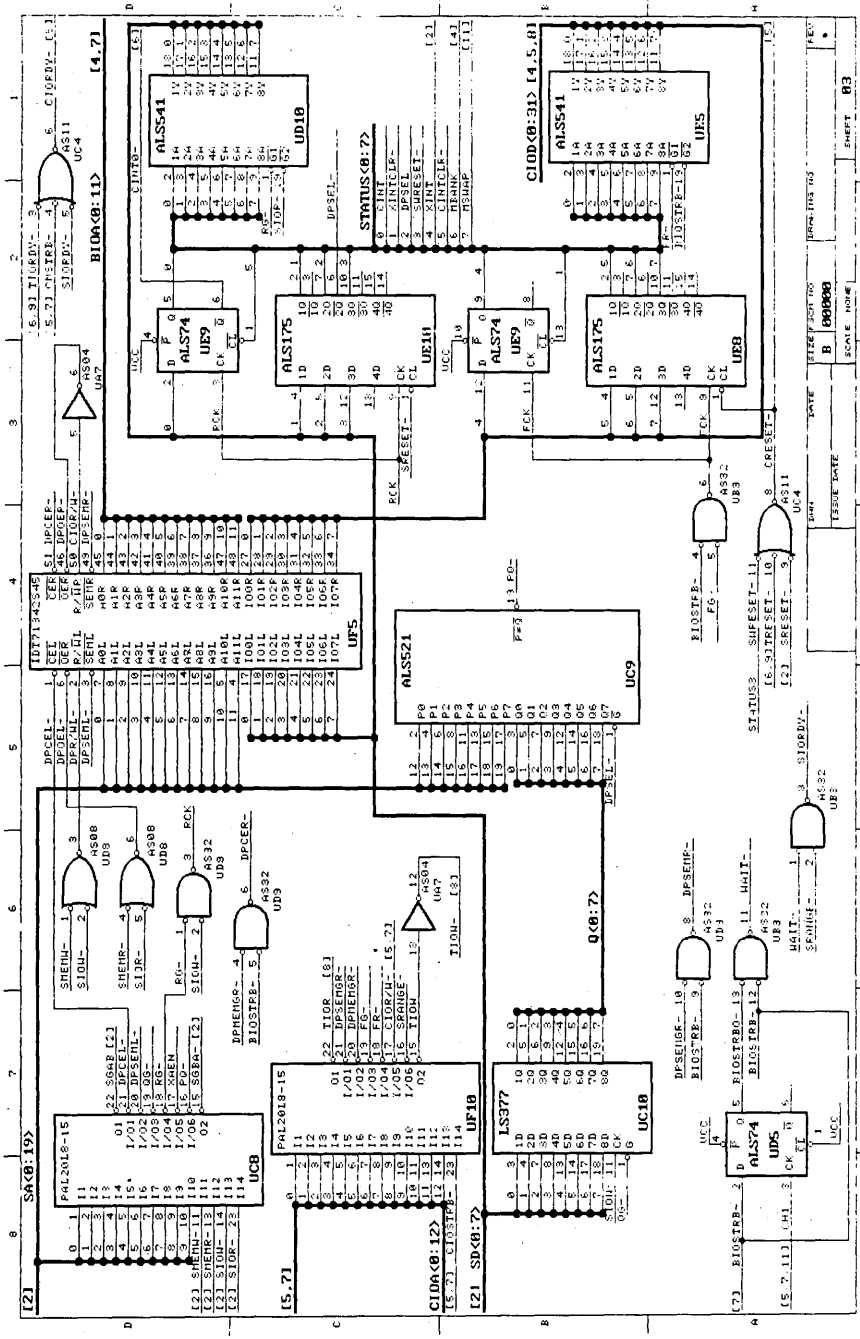

Figure 6. Complete Schematic of TMS320C30 Software Development System (section 2 of 9)

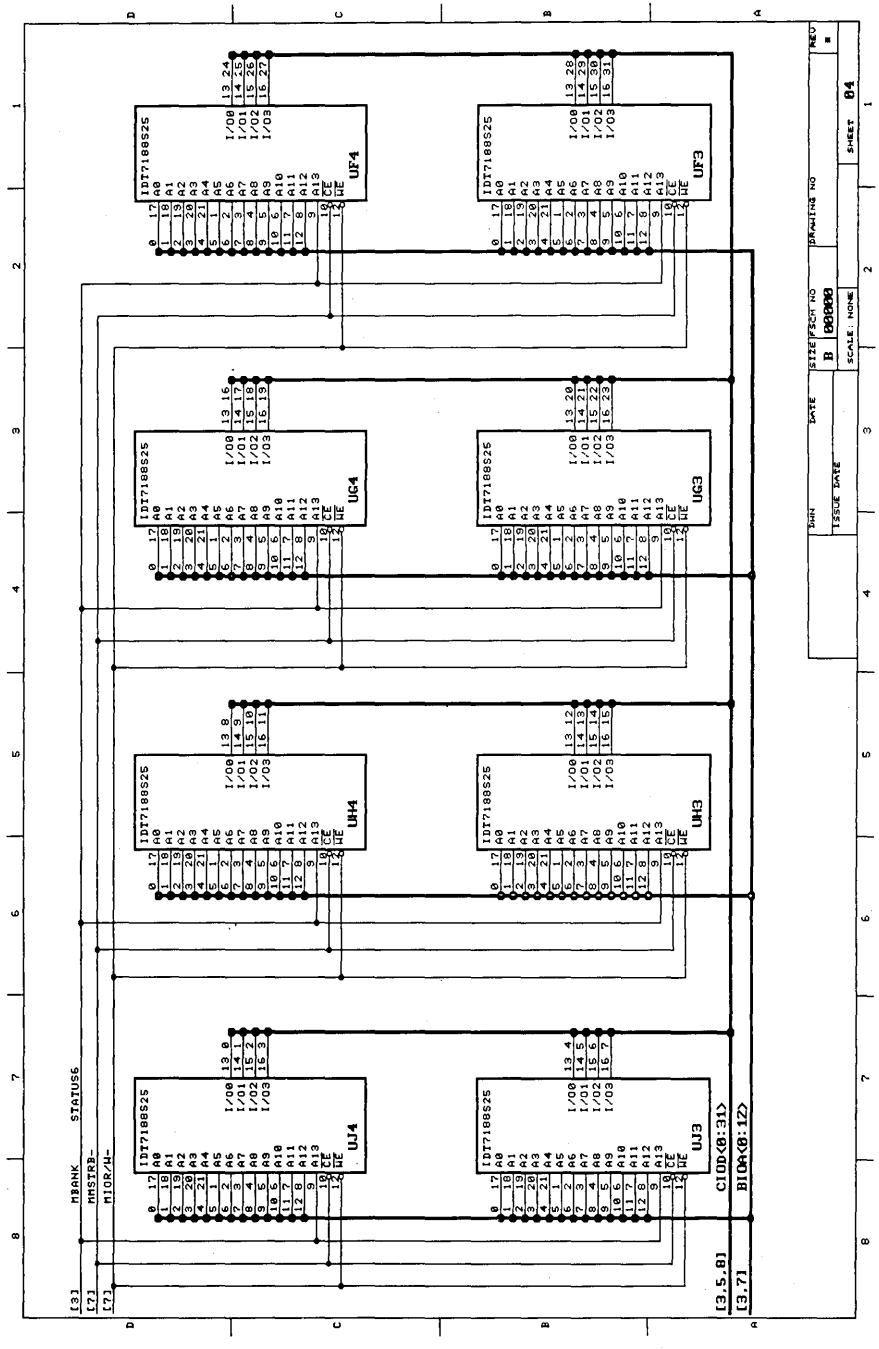

Figure 6. Complete Schematic of TMS320C30 Software Development System (section 3 of 9)

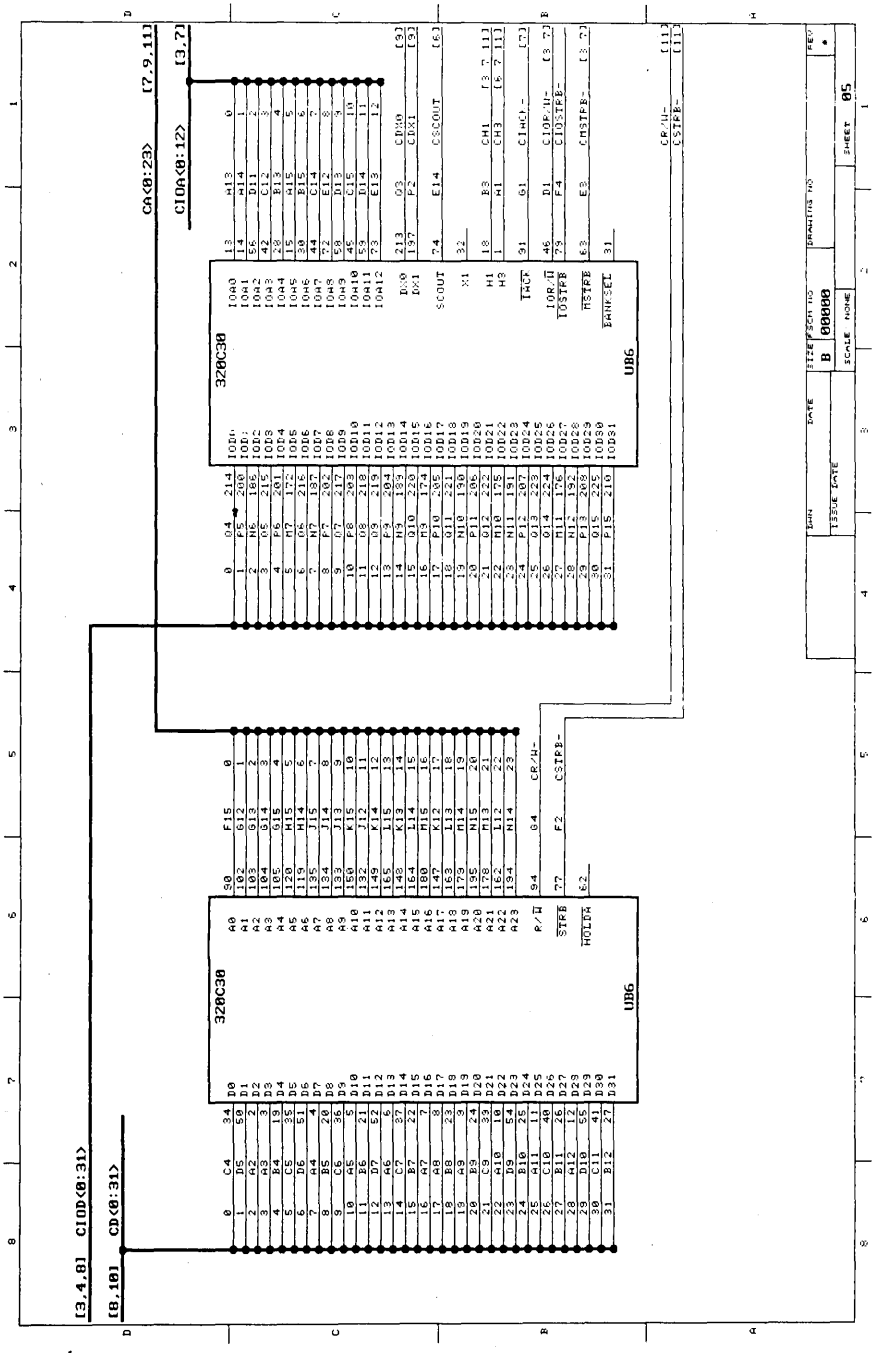

Figure 6. Complete Schematic of TMS320C30 Software Development System (section 4 of 9)

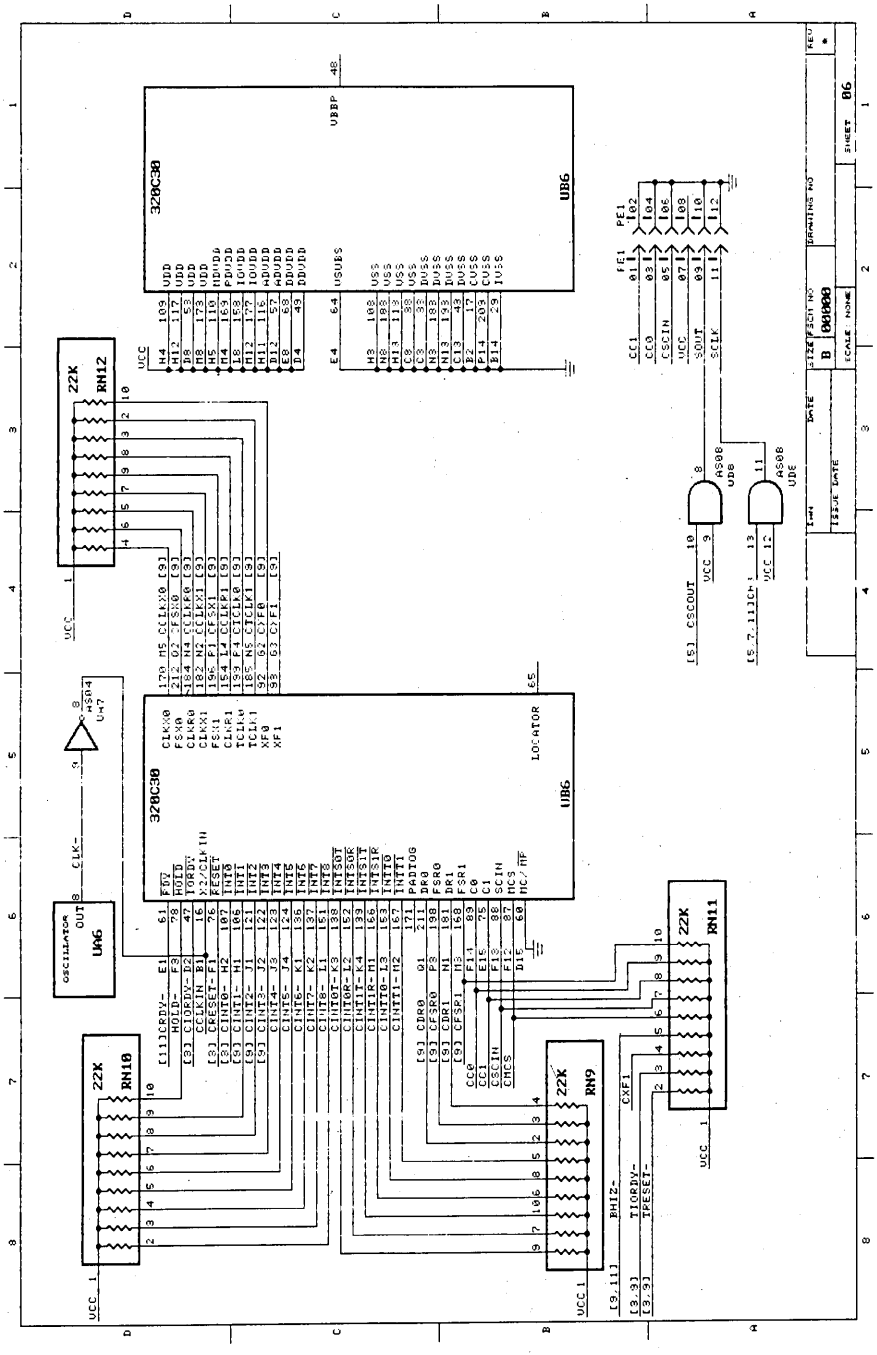

Figure 6. Complete Schematic of TMS320C30 Software Development System (section 5 of 9)

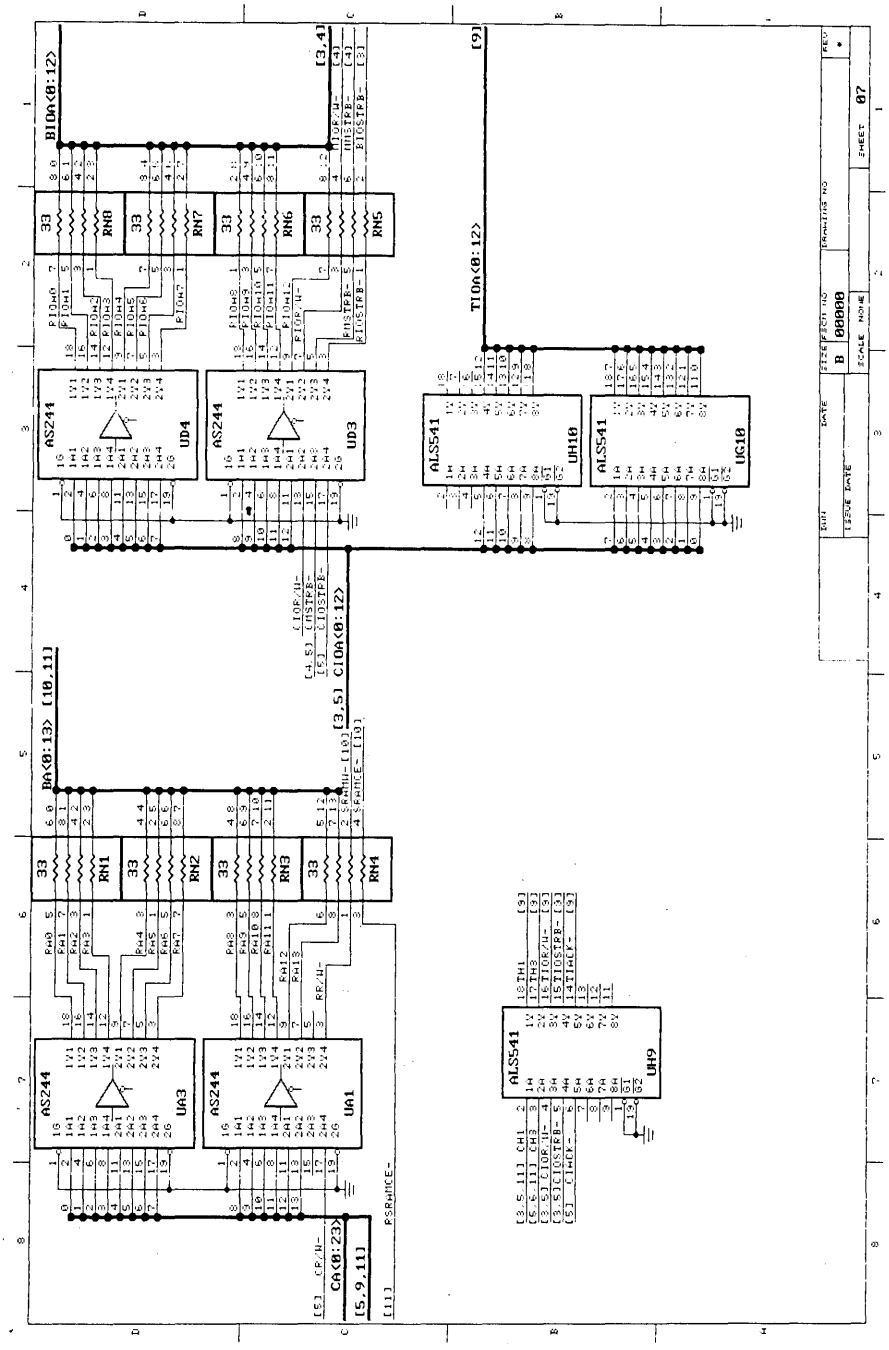

Figure 6. Complete Schematic of TMS320C30 Software Development System (section 6 of 9)

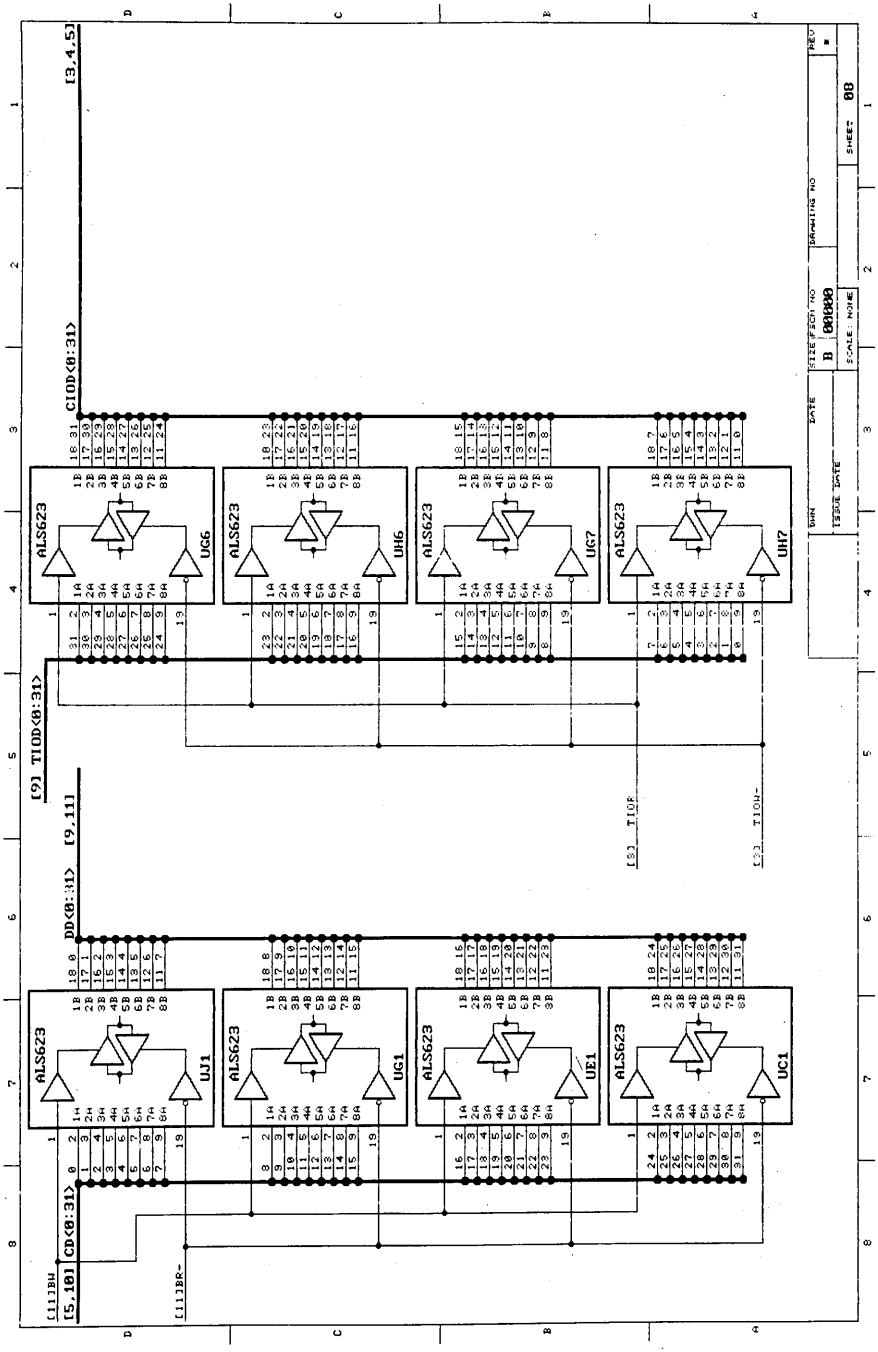

Figure 6. Complete Schematic of TMS320C30 Software Development System (section 7 of 9)

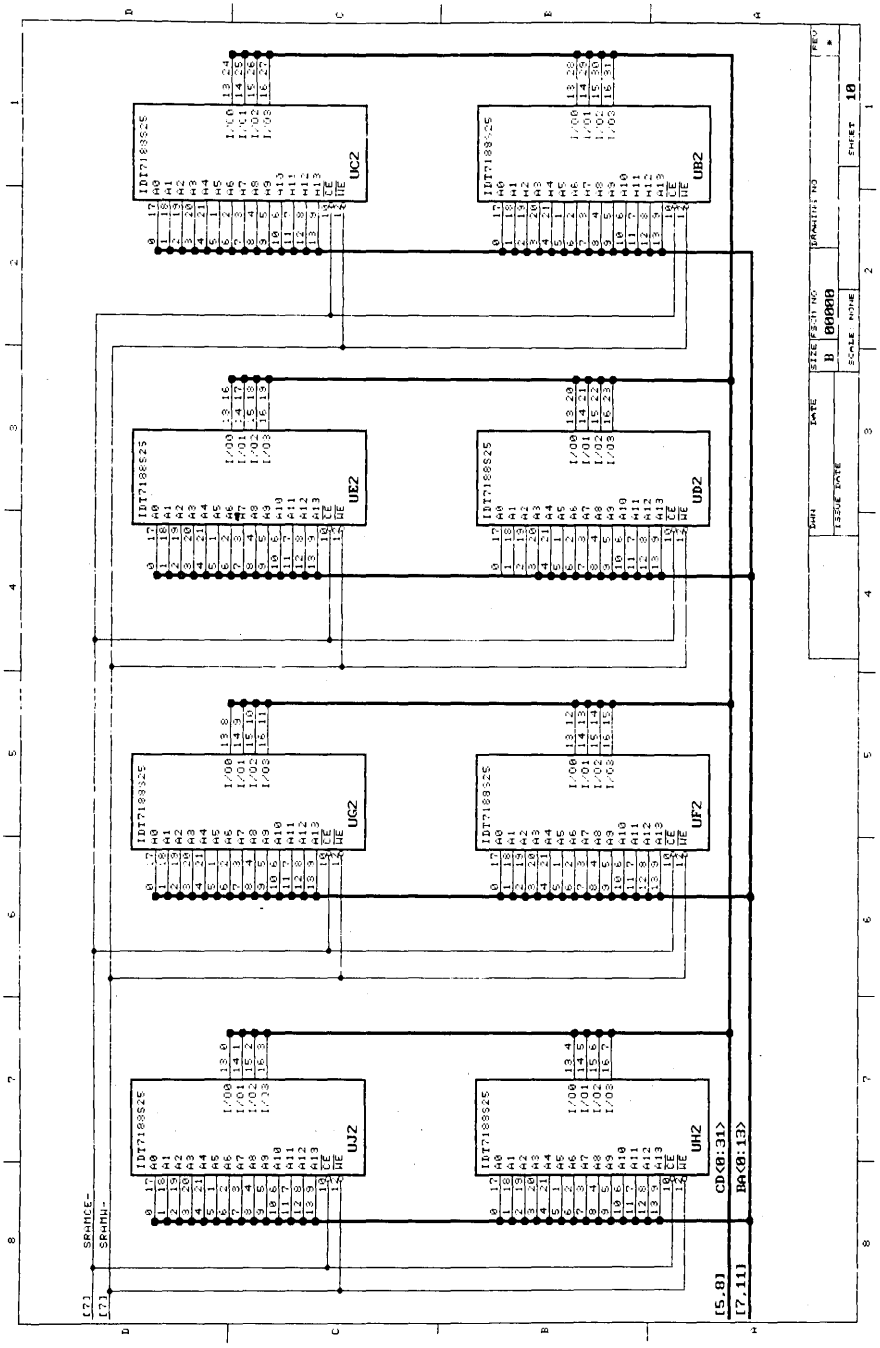

Figure 6. Complete Schematic of TMS320C30 Software Development System (section 8 of 9)

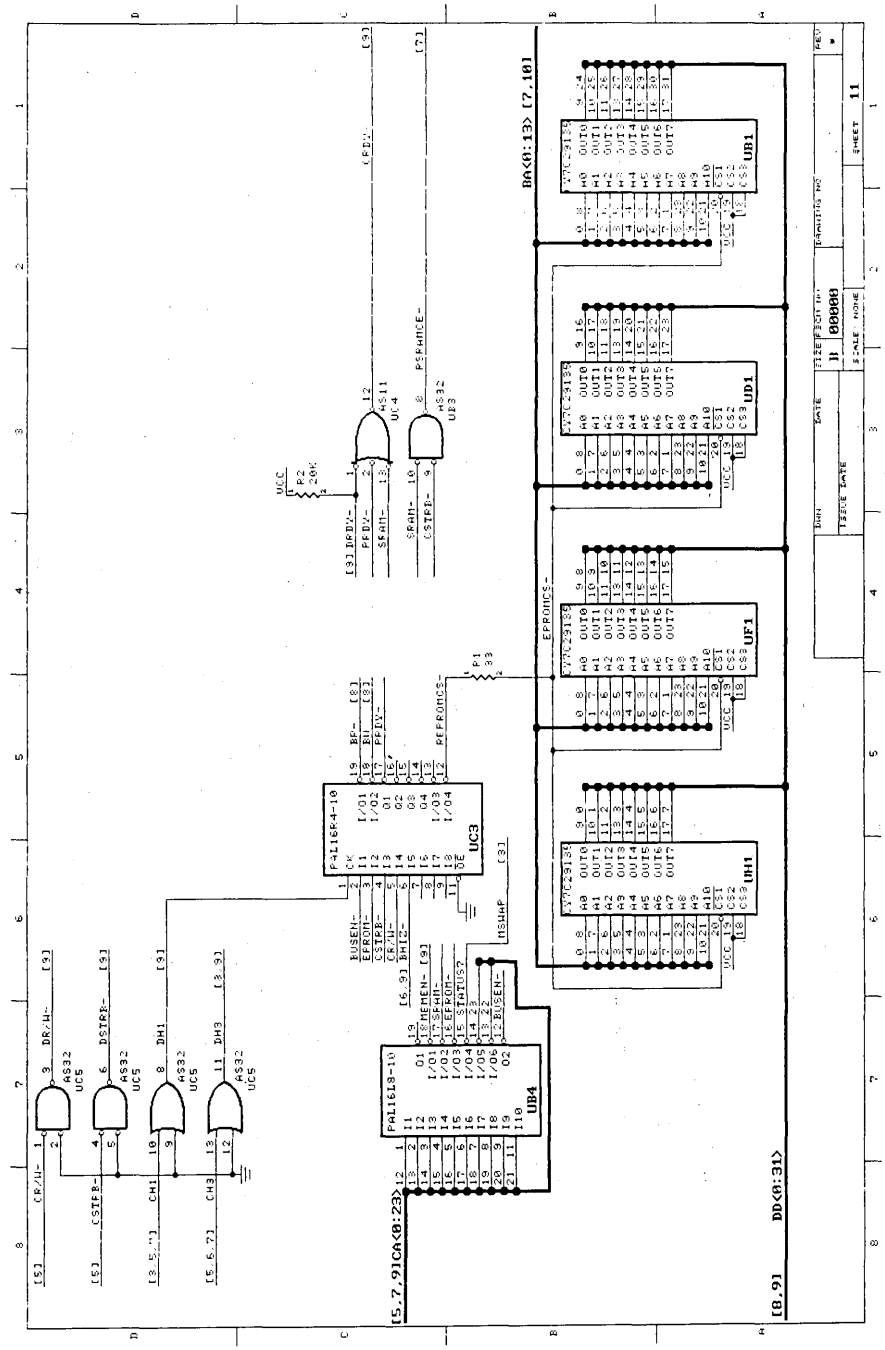

Figure 6. Complete Schematic of TMS320C30 Software Development System (section 9 of 9)

APPENDIX

DUAL-PORT SEMAPHORES

Eight extra address locations in the IDT71342 4K x 8 dual-port RAM are dedicated to binary semaphore flags. These flags allow either the TMS320 or the host processor to claim a privilege over the other processor for functions defined by the programmer's software. As an example, the semaphore can be used by the PC to inhibit the TMS320C30 from accessing a portion of the dual-port RAM, or some other shared resource.

The dual-port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard static RAMs and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the dual-port RAM.

Multiple processor sytems like the TMS320C30 Software Development Board can benefit from a performance increase by using these semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT71342 does not use its semaphore flags to control any resources through hardware, thus allowing the programmer to determine each flag's meaning.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the dual-port RAM. These latches can be used to pass a flag, or token, from one processor to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that a shared resource is in use. If the TMS320 wants to use this resource, it requests the token by writing a zero into the latch. The TMS320 then verifies its success in writing the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in writing a zero into the latch, it determines that the PC had set the latch first, is in posession of the token, and is using the shared resource. The TMS320 can then either repeatedly inquire the status of the semaphore it requested, or it can remove its request for that semaphore by writing a one into its location. The TMS320 can then perform another task and occasionally attempt to gain control of the token via the set and test sequence. Once the PC has relinquished the token, the TMS320 can succeed in gaining control of the shared resource.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore location, and is released when the same processor writes a one into that location.

The eight semaphore flags reside within the IDT71342 in a seperate memory space from the dual-port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which is used as a chip select for the semaphore flags), and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0 - A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other (see Table I). That location can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits, so that a "set" flag reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive, or the output will never change. This is not a concern in the TMS320C30 Software Development Board, since either bus' accesses to other memory locations between semaphore accesses inactivate both of these signals for a relatively long period no matter how tight of a loop is used to interrogate the device.

FUNCTION	PC BUS D0-D7 LEFT	TMS320 D0-D7 RIGHT	STATUS
No action	1	1	Semaphore free
PC writes "0" to semaphore	0	1	PC has semaphore token
TMS320 writes "0" to semaphore	0	1	No change. TMS320 has no write access to semaphore
PC writes "1" to semaphore	1	0	TMS320 obtains semaphore token
PC writes "0" to semaphore	1	0	No change. PC has no write access to semaphore
TMS320 writes "1" to semaphore	0	1	PC obtains semaphore token
PC writes "1" to semaphore	1	1	Semaphore free
TMS320 writes "0" to semaphore	1	0	TMS320 has semaphore token
TMS320 writes "1" to semaphore	1	1	Semaphore free
PC writes "0" to semaphore	0	1	PC has semaphore token
PC writes "1" to semaphore	1	1	Semaphore free

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Table 1. Example Semaphore Procurement Sequence

A sequence of WRITE/READ must be used to acquire a semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as a one, a fact which the processor will verify by the subsequent read (see Table I). As an example, assume the PC writes a zero to the left port at a free semaphore location. On a subsequent read, the PC will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if the TMS320 attempts to write a zero to the same semaphore flag, it will fail, as will be verified by the fact that it will read a one from that semaphore during a subsequent read cycle. Had a sequence of READ/WRITE been used instead, contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed either by repeated reads, or by writing a one into the same location to remove the semaphore request. The reason for this is easily understood by looking at the simple logic diagram of a semaphore flag shown in Figure 7. Two semaphore request latches feed into a semaphore flag. Whichever latch is the first to present a zero to the semaphore flag will force its side of the semaphore flag low, and the other side high. This condition will continue until a one is written into the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written with a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system could hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests happen at the same time, the assignment will be arbitrarily made to one side or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted a software error can easily happen. Code integrity is of the utmost importance when semaphores are used instead of hardware handshaking.

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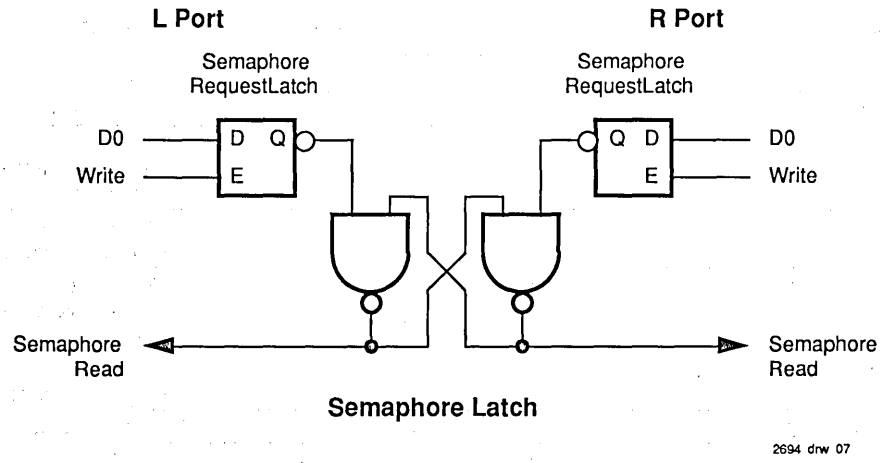


Figure 7. IDT71342 Semaphore Logic

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore which is written to a zero must be reset to a one, both the TMS320 and the PC must write a one into all semaphore locations at initialization to assure that the semaphores will be free when needed.

USING SEMAPHORES - Some Examples

Perhaps the simplest application of semaphores is their application as resource markers for the IDT71342's dual-port RAM. Say the 4K x 8 RAM was to be divided into two 2K x 8 blocks, which were to be dedicated at any one time to servicing either the PC or the TMS320. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 2K of dual-port RAM, the PC could write then read a zero into Semaphore 0. If this task were successfully completed (a zero was read back, rather than a one), the PC would assume control of the lower 2K. Meanwhile, the TMS320 might attempt to perform the same function. Since the TMS320 was attempting to gain control of the resource after the PC, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the TMS320's software could choose to try and gain control of the second 2K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the PC.

Once the PC was finished with its task, it would write a one to Semaphore 0, then may try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the TMS320, the PC could remove its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the TMS320 performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 2K blocks of dual-port RAM with each other.

The blocks do not have to be any particular size and could even be of variable length, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the dual-port RAM or other shared resources into eight parts.

Semaphores are a useful form of arbitration in real-time DSP applications, when the PC must be locked out of a section of memory during a transfer, and the TMS320 cannot tolerate any wait states. With the use of semaphores, once the two processors had determined which memory area was "off limits" to the PC, both the PC and the TMS320 could access their assigned portions of memory continuously without any wait states. Both processors can access their assigned RAM segments at full speed.

Another application of semaphores is in the area of complex data structures. In this case, block arbitration is very important to the maintenence of data integrity. For this application one processor may be responsible for building and updating a data structure, which the other processor then reads and interprets. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the TMS320 and the PC. Software semaphores are a perfect fit. The building processor uses the semaphore to arbitrate for the block and to lock it once that processor is able to acquire the semaphore flag. This processor then is able to go in and update the data structure. When the update is completed, the semaphore and the corresponding data structure block are released. The interpreting processor then acquires the semaphore which allows it to come back and read the complete data structure, thereby guaranteeing consistency.

Integrated Device Technology, Inc.

DUAL-PORT INTERRUPT EXPANSION

APPLICATION NOTE AN-70

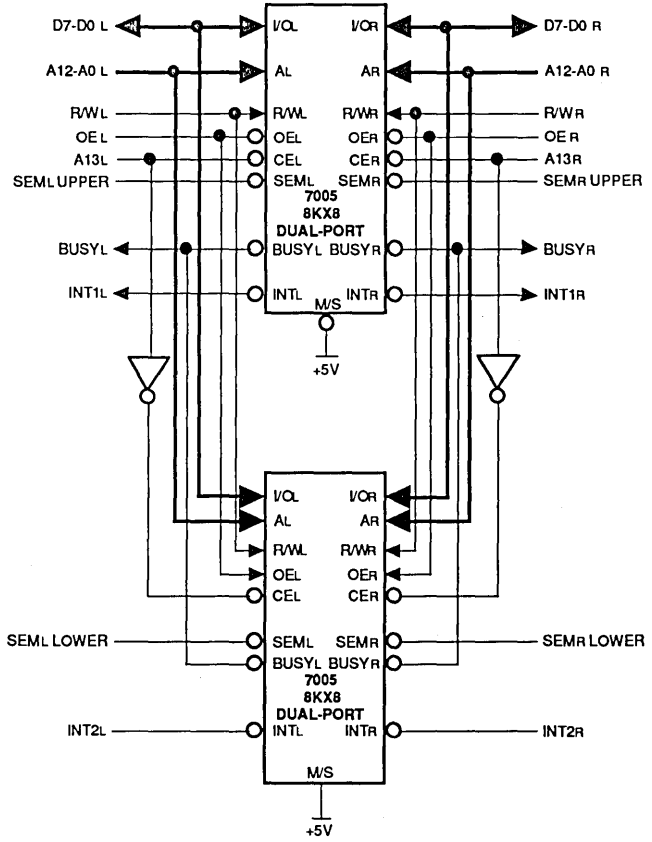
by John C. Mein, Field Applications Engineering

Synopsis: This tech note describes a simple technique to obtain additional interrupts from each side of a dual-port when expanding in width.

Many of today's dual- ports offer the capability of allowing one side to have an interrupt generated to the other side. This allows the signaling of messages such as data ready, data overflow, etc. This is a handy feature used quite often. IDT'S dual-ports offer two interrupts per part — one to each side when operated in standalone mode. When expanding in depth or width additional interrupts can be obtained—exactly how many more depends on how the expansion is accomplished.

A feature available in many dual-ports is depth expansion capability. One simply uses external address decoding to select one of multiple dual-ports (usually all masters). An example of this scheme is offered by the IDT 7005 8kx8 dual-port and shown in Figure 1.

This depth expansion results in two interrupts being available on either side. For side A to generate an interrupt to side B, side A must write anything to location 1FFF (8191 decimal). This generates the interrupt to side B which is cleared only by side B reading the same location 1FFF. Side B can likewise generate an interrupt to side A—the only difference is the memory location is now 1FFE (8190 decimal). Another set of interrupts also resides at locations 3FFF (16383 decimal) and 3FFE (16382 decimal).



2725 drw 01

Figure 1. Depth Expansion of the IDT7005 8k x 8 Dual-Port

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Figure 2 shows a typical system consisting of two 8kx8 dual-ports expanded in width. Here one must be careful to have address arbitration done by only one chip (the master) and having the other chips (the slaves) follow the master. This is easily accomplished using separate master and slave chips (such as the IDT7130 and IDT7140) or on the newer chips such as the IDT7005/6 and IDT7024/25 by connecting the M/S pin appropriately. All address lines are tied in parallel and only one interrupt for each side (since the address mapping is the same for both chips) is used. The other interrupts are not connected.

However, when expanding in width, one can have extra interrupt lines (one per chip) generated by simply inverting any address line between the two (or more) dual-ports. As shown in Figure 3 we have inverted address line A12. The only item one needs to be careful about is to insure you correctly calculate the new address location for the additional interrupts. For this example, instead of the interrupts being at only 1FFF and 1FFE they are now also at FFF (4095 decimal) and FFE (4094 decimal). It would also be possible to map the interrupts to be contiguous in the address map (i.e. map them to be at FFE, FFF, 1000, and 1001).

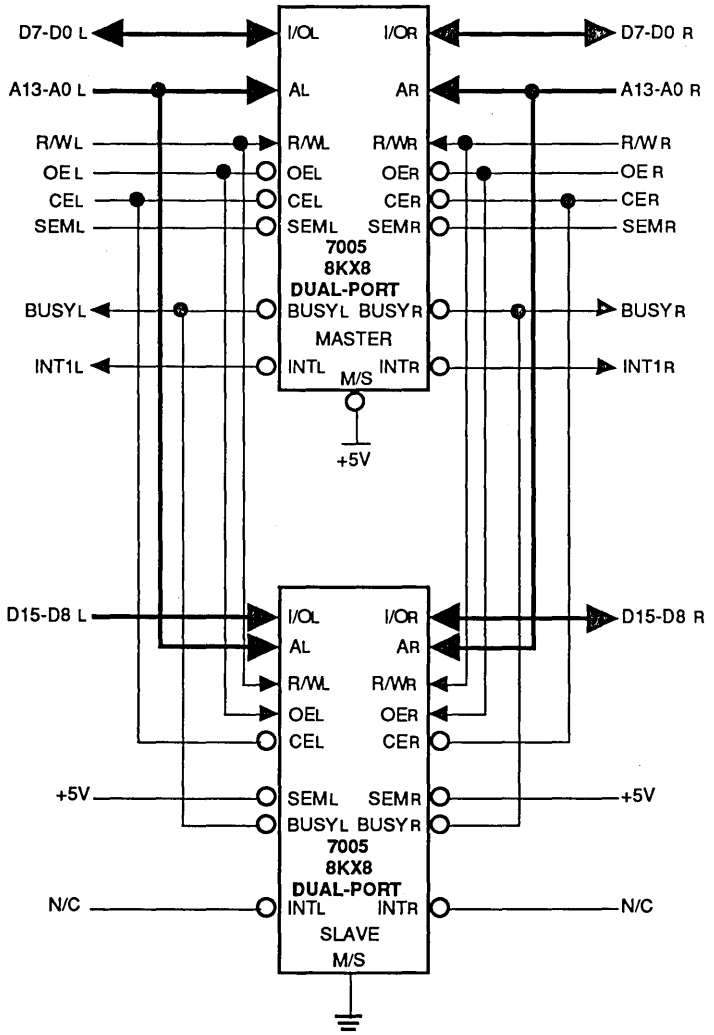
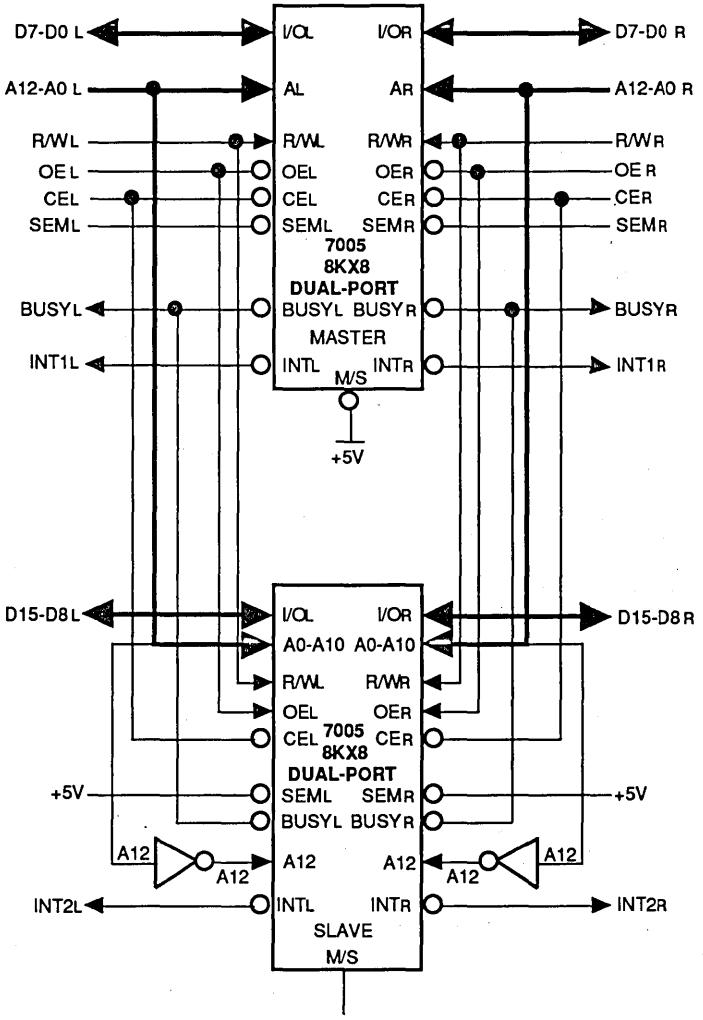


Figure 2. Normal Width Expansion of the IDT7005 8k x 8 Dual-Port

Another way to accomplish this would be to separate the chip enables for each dual-port. Then, to enable an interrupt, just enable and write to the appropriate dual-port. The advantage of this technique is that no additional address decoding delay is inserted.

The same methodology can be applied to multiple width expansions. For instance, using a 7006 16kx8 dual-port for a 32 bit system (resulting in a 16kx32 memory) would result in four interrupts for each side for a total of 8 (compared with only two by the normal expansion method).

This tech note showed a simple way of obtaining more interrupts then normal when expanding in width. This is easily accomplished by inverting one or more of the address lines between the dual-ports.



2725 drw 03

Figure 3. Width Expansion with More Interrupts

Integrated Device Technology, Inc.

DESIGN GUIDELINES FOR CUSTOM MODULE PACKAGES

APPLICATION NOTE AN-44

INTRODUCTION

IDT packaging technology includes the utilization of modules, in order to integrate several chip-level components into a single subsystem. The resulting packing density offers several user benefits:

1. Overall system space requirements may be substantially reduced.
2. Noise effects may be greatly reduced by the close prximity of components on a module.
3. High-speed circuit operation may be more readily achieved by the reduction of interconnect capacitance and distance.
4. Trouble-shooting and field service may be improved by the system partitioning into readily replaceable functions.
5. System enhancements may be offered as plug-in options with a minimum of board space allocation required.

The IDT Subsystems portfolio include numerous standard module products. However, it may be quite advantageous to consider the use of a custom module for a given application. In this case, the user should be familiar with IDT Subsystem design guidelines and limitations in order to determine if the resulting custom module design will meet their needs and if it can be properly manufactured.

MODULE/COMPONENT MATERIAL CONSIDERATIONS

There are two different module materials available for use:

FR-4 LAMINATE SUBSTRATES

It is a industry standard epoxy-glass multi-layer printed circuit board material. It is intended for commercial/industrial applications which do not have high temperature operating requirements. Plastic packaged components must be used on FR-4 modules, since the temperature coefficient of expansion of ceramic components do not match that of FR-4 material.

CERAMIC SUBSTRATES

This substrate is a industry standard multi-layer co-fired ceramic material. This material is required for military grade products and for high-temperature applications. Ceramic is desirable for designs requiring the highest density since the packing density of components onto the substrate material is much higher with ceramic than with FR-4. It is possible to mount plastic components on ceramic modules, but this is generally not economically sensible.

MODULE PACKAGE TYPES

IDT modules are available in a variety of standard module packages, in addition to other non-standard package. Custom packages or pin requirements are available upon request.

1. Dual In-line (DIP) - Figure 1.
   Ceramic modules utilize sidebrazed pins, which do not extend onto the surfaces of the module substrate. As a result, both top and bottom surfaces of the module are available for component replacement. FR-4 material, on the other hand, requires the pins to wrap over the top and bottom surfaces for mechanical support. This reduces the available surface area (on both the top and bottom) for placement of components.
2. Quad In-line (QIP) - Figure 2.
   These modules have two parallel rows of pins on each side of the module (i.e. 4 total rows), extending perpendicular to the plane of the module, like DIPs. Ceramic substrates uses sidebrazed pins for the outer row of pins and bottom brazing for the inner row (L-shaped pins permit this). FR-4 substrates requires pins to be attached through the plane of the module.
3. Hex In-line (HIP) - Figure 3.
   These modules have 3 parallel rows of pins on each side of the module (i.e. 6 total rows), extending perpendicular to the plane of the module, similar to DIPs. Ceramic material uses bottom brazed pins while FR-4 requires the pins to be attached through the plane of the module.
4. Single In-line (SIP) - Figure 4.
   These modules have a single line of pins which extend out in parallel to the plane of the substrate, rather than perpendicular. Ceramic substrate SIP pins are attached to the one surface only, and hence, do not impact usable surface area on the other side. FR-4 substrates, however, requires pin attachment on both surfaces and this reduces available area.
5. Dual SIP (DSIP) - Figure 5.
   These modules have two parallel rows of pins which extend out in parallel to the plane of the substrate, similar to SIPs. Both ceramic and FR-4 substrates require the use of some surface area on both sides for pin attachment to the module.
6. Zig-zag In-line (ZIP) - Figure 6.
   These modules have two parallel rows of pins which extend out in parallel to the plane of the substrate, similar to DSIPs. However, each side is offset relative to the other side. For the case of standard 0.100" pin to pin spacing (on one side), the opposite side will be offset by 0.050" but still maintain 0.100" pin to pin spacing on its own side.
7. Single In-line Memory Module (SIMM) - Figure 7.
   These modules use industry standard edge connector type pins to be used with card edge sockets. These substrates are made exclusively with FR-4.
8. Pin Grid Array (PGA) - Figure 8.
   These modules use industry standard through hole grid array formats necessary for high pin count designs. PGAs are made exclusively with ceramic substrates.

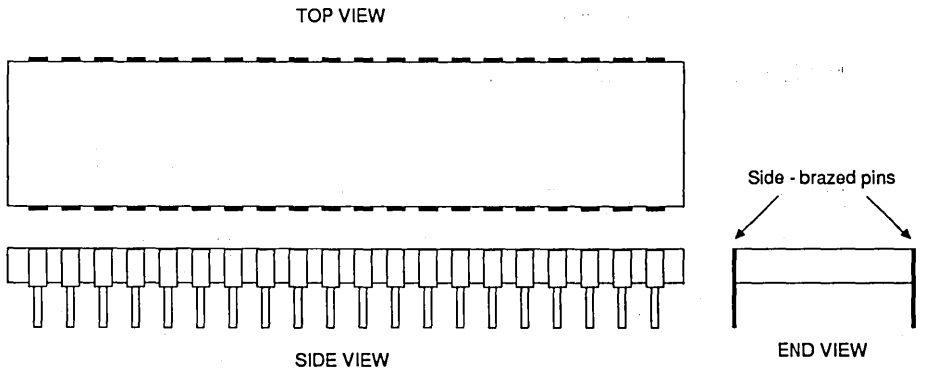


Figure 1(a). Ceramic DIP

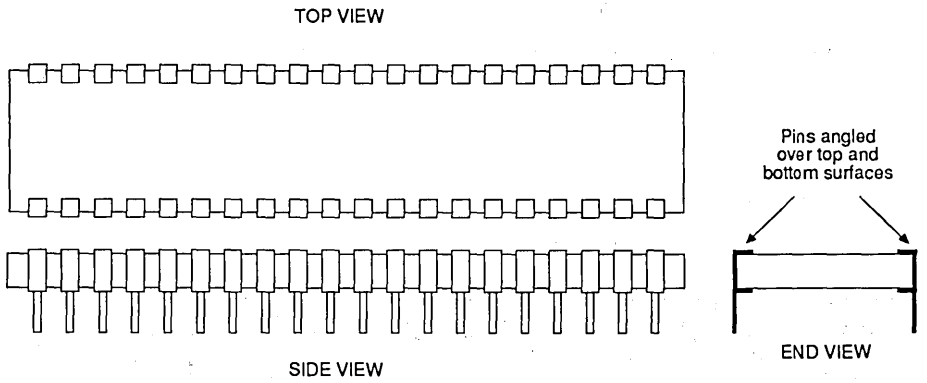


Figure 1(b). FR-4 DIP

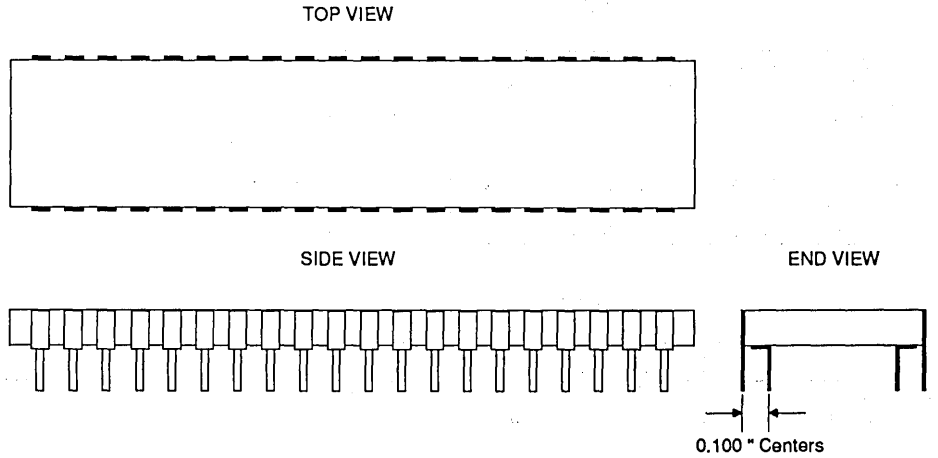


Figure 2(a). Ceramic QIP

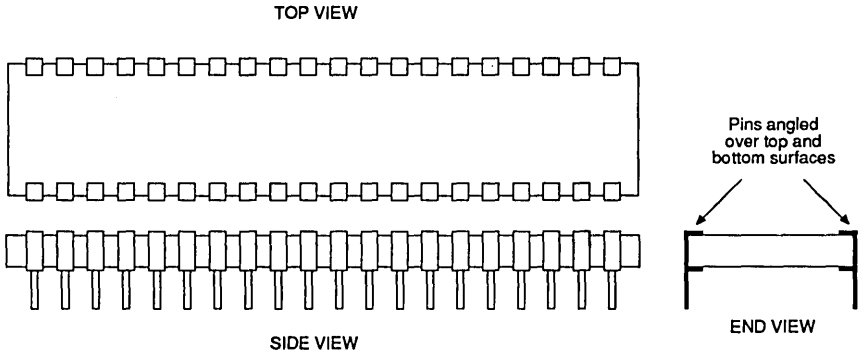


Figure 2(b). FR-4 QIP

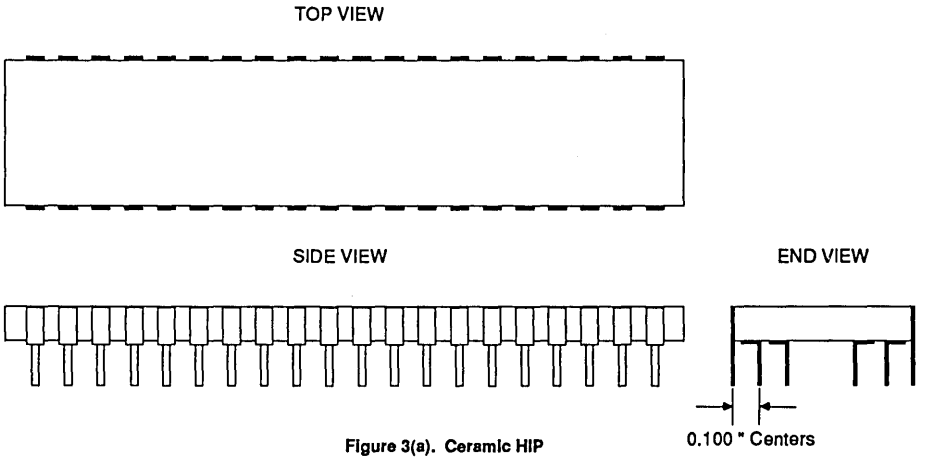


Figure 3(a). Ceramic HIP

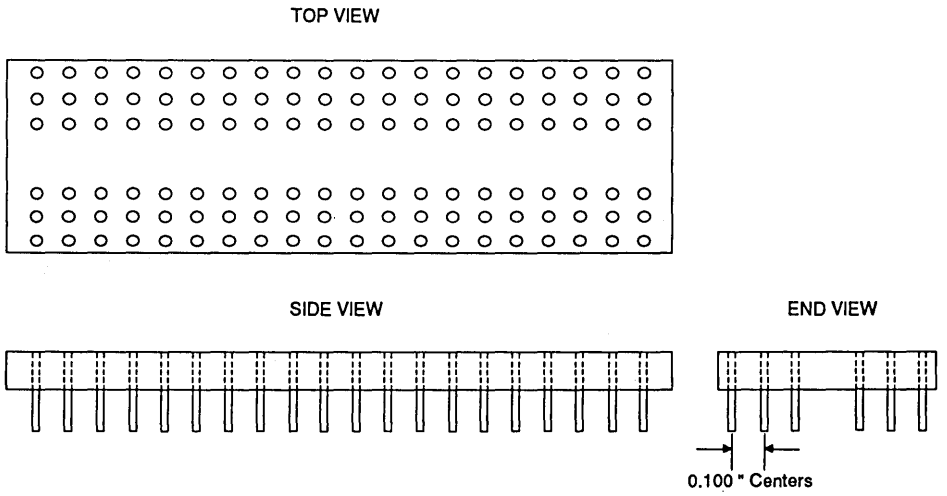


Figure 3(b). FR-4 HIP

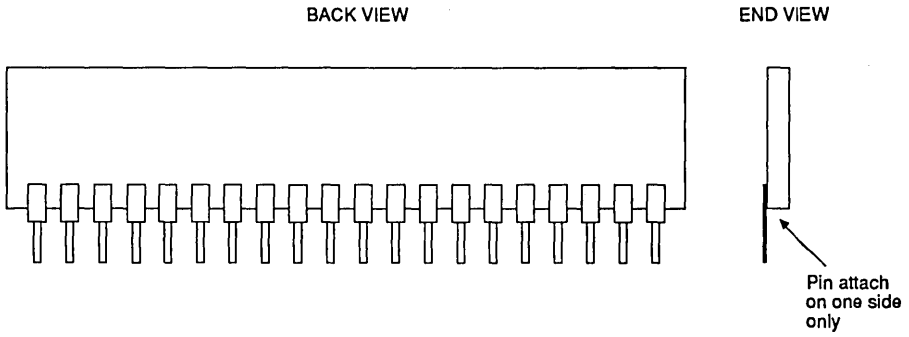


Figure 4(a). Ceramic SIP

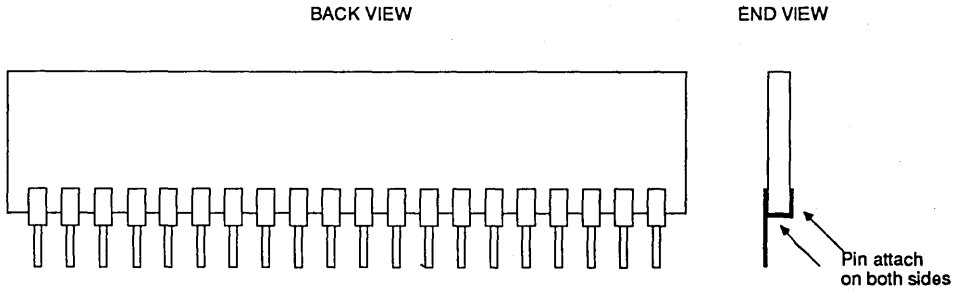


Figure 4(b). FR-4 SIP

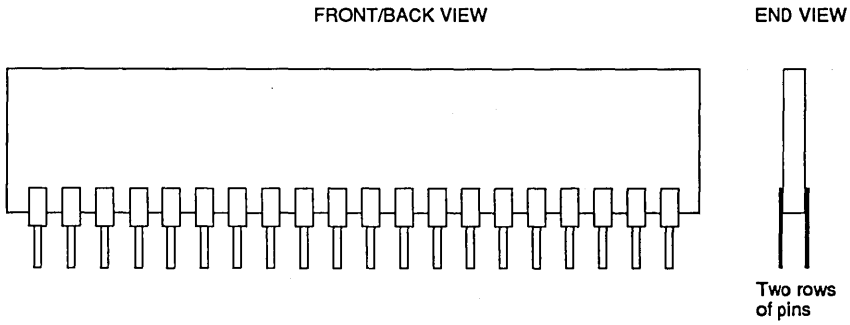


Figure 5(a). Ceramic Dual-SIP

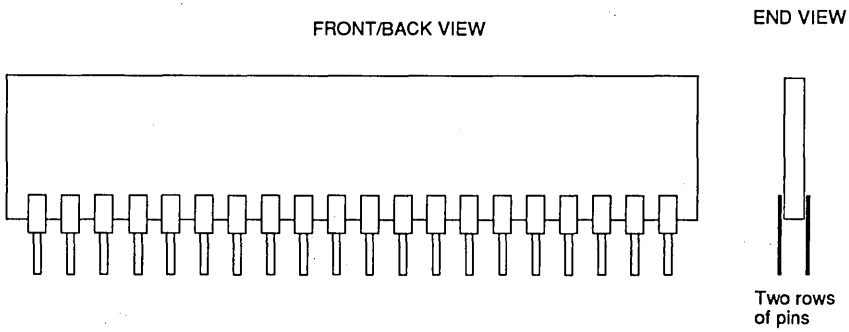


Figure 5(a). FR-4 Dual-SIP

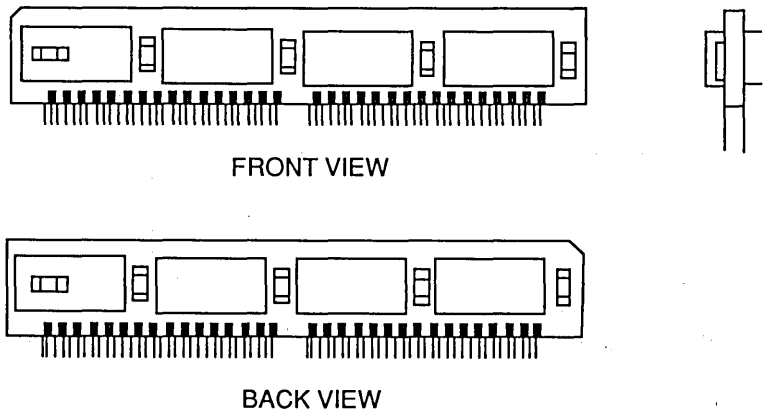


Figure 6. FR-4 ZIP

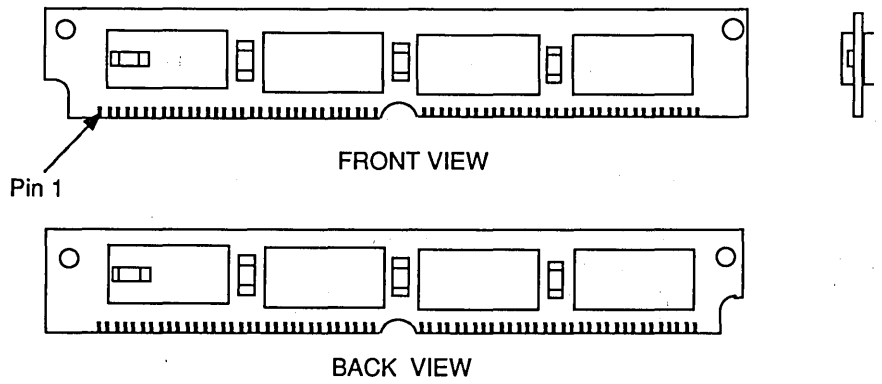


Figure 7. FR-4 SIMM

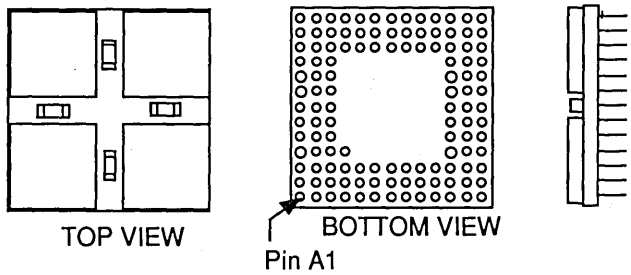


Figure 8. Ceramic PGA

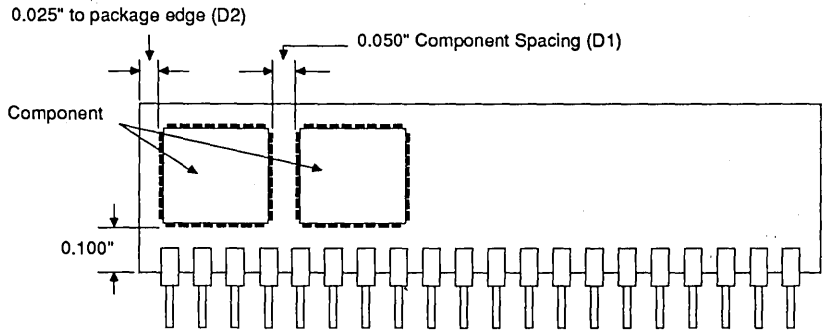


Figure 9. Illustration of Minimum Spacing Distances

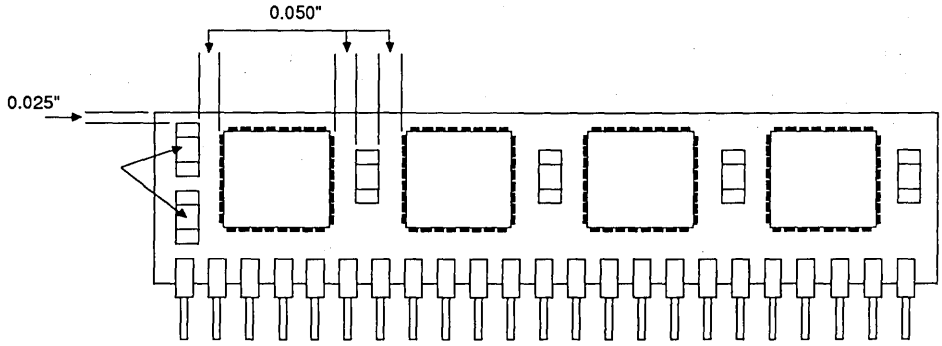


Figure 10. Illustration of Decoupling Capacitors on Module

SURFACE ARE LIMITATIONS FOR PIN ATTACHMENT

The module sustrate type determines the method of pin attachment, as outlined in the previous section. The method of pin attachment, therefore, may impact the amount of available surface space for components on the top and bottom surfaces.

Ceramic DIPs do not have any usable surface area restrictions, since the side-brazed pins do not extend onto the module surface area. FR-4 DIPs require that 0.100" from the edge of the module be unavailable for components (on both sides of the module). This results because the module pins extend through both sides of the module and therefore take away some surface area.

Ceramic SIPs, due to the side-brazed pins, require the same 0.100" margin on the surface of the module to which the pins are attached. The other side has no such constraint. FR-4 SIPs require 0.100" margin on both sides, since the pins are attached on both sides.

Dual SIPs, ZIPs, and SIMMs require 0.100" margins on both sides to accomodate the pins. This holds for both ceramic and FR-4 modules.

Ceramic QIPs have no top side restrictions for pin attachment, but have a constraint on the bottom side of 0.100". FR-4 QIPS use pins which go through the module material and this imposes constraints on both sides. The restriction inhibits any component from being located within 0.225" of the edge of the module on which the pins are located.

Ceramic HIPs have no top side restrictions but require 0.250" of margin on the bottom. FR-4 HIPs require 0.350" margin on both the top and bottom of the module.

PGAs have not top side restrictions; however, the bottom side is used exclusively for pin attachment. In certain cases, there may be a small bottom area available for component placement but this area is usually only large enough for logic or passive type component packages.

COMPONENT SPACING LIMITATIONS

The space required between components on a module is the same for both ceramic and FR-4 substrates. The minimum space between any two components on a module is 0.050". Figure 9 illustrates this as dimension D1. Note that if pins extend out from the body of a component package (as shown for the components of Figure 9), then the spacing required is the space starting from the ends of those pins. On the other hand, if the component pins are under the component package, then the space is merely the space between the component package bodies.

Each component on a module, regardless of the substrate type, must be at least 0.025" from the edge of the module, as shown by dimension D2 in Figure 9.

DECOUPLING CAPACITORS

The inclusion of decouping capacitors is dependent upon the expected current surges on the module, as well as the general speed of the devices (higher speed devices generally need more decoupling). It is recommended that decoupling capacitors be liberally used. Typical applications usually employ 1 decoupling capacitor for each memory component and 1 for ever 1.5 logic components on the module.

Each decoupling capacitor may be treated as any other component, in terms of its requirement for spacing from other components or module edges. The physical size of standard decoupling capacitors is 0.080" by 0.200" and the typical value is 0.068 μF. Figure 10 illustrates module dimensions with capacitors included.

OVERALL MODULE DIMENSIONS

Module length is constrained by the number of pins on the sides of the module or by component package area requirements, which ever is greater. The pin pitch (center-to-center spacing) is normally standardized at 0.100", but may be customized to any user-specific value. To a first-order approximation, the number of pins and their pitch determine the module length.

Module width, although variable, is best kept to standard dimensions. This eases the requirements placed upon sockets for testing, burn-in and even for final system use. Standard widths for high pin count modules are those widths which are multiples of 0.300". Common usage has been found for widths of 0.3, 0.6, 0.9, 1.2, and 1.5 inches.

Let us illustrate how to approximate a custom modules' dimensions with a short example.

A customer wants a custom static RAM module meeting these specifications:

a) 256K x 8 memory configuration
b) using 32K x 8 LCC components
c) ceramic SIP package type
d) standard 0.100" pin pitch

The number of necessary pins for this module would be 33 (18 address inputs, 8 data I/O, 2 Vcc, 2 GND, 1 output enable, 1chips select, and 1 write enable).

CASE 1 - Assumption: Components Single Sided Surface Mounted.

Shown below are calculations which will show that the area required for component placement on one side of the module are greater than (# of required pins) x (pin pitch). Therefore, the overall dimensions of the module are determined by the area requirements of the components. Rough dimensions of the module in this case would be (also reference Figure 11):

Length = 2(0.025") + 8(0.460") + (0.360") + 4(0.080") +
12(0.050")
= 5.01 inches

Height = (0.100") + (0.560") + (0.025")
= 0.685 inches

CASE 2 - Assumption: Components Double Sided Surface Mounted.

Shown below are calculations which will show that the area required for component placement on both sides of the module are greater than (# of required pins) x (pin pitch). Therefore, the overall dimensions of the module are determined by the area requirements of the pins. Rough dimensions of the module in this case would be (also reference Figure 12):

(Length determined by components)
Length=2(0.025")+4(0.460")+(0.360")+6(0.050")+2(0.080")
= 2.71 inches
Height=(0.100") + (0.560") + (0.025")
= 0.685 inches

(Length determined by the pins)
Length=(33 pins) x (0.100"/pin) + 2(0.025")
= 3.350 inches
Height=(0.100") + (0.560") + (0.025")
= 0.685 inches

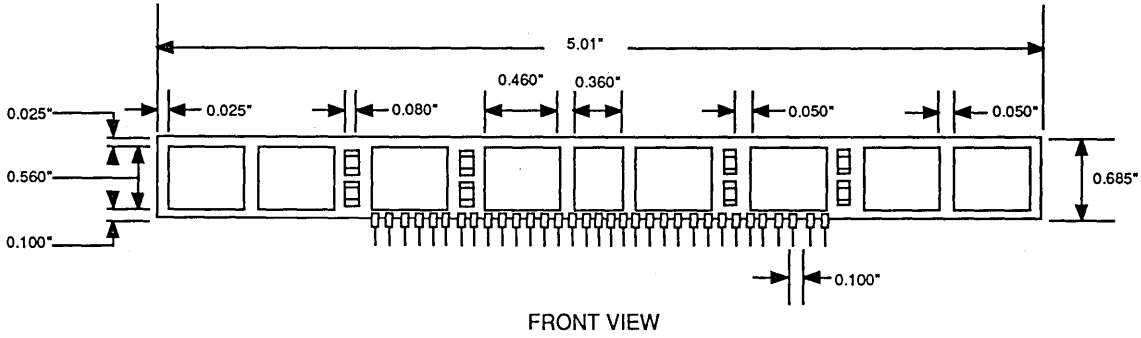


Figure 11. Single Sided Surface Mounted SIP Module

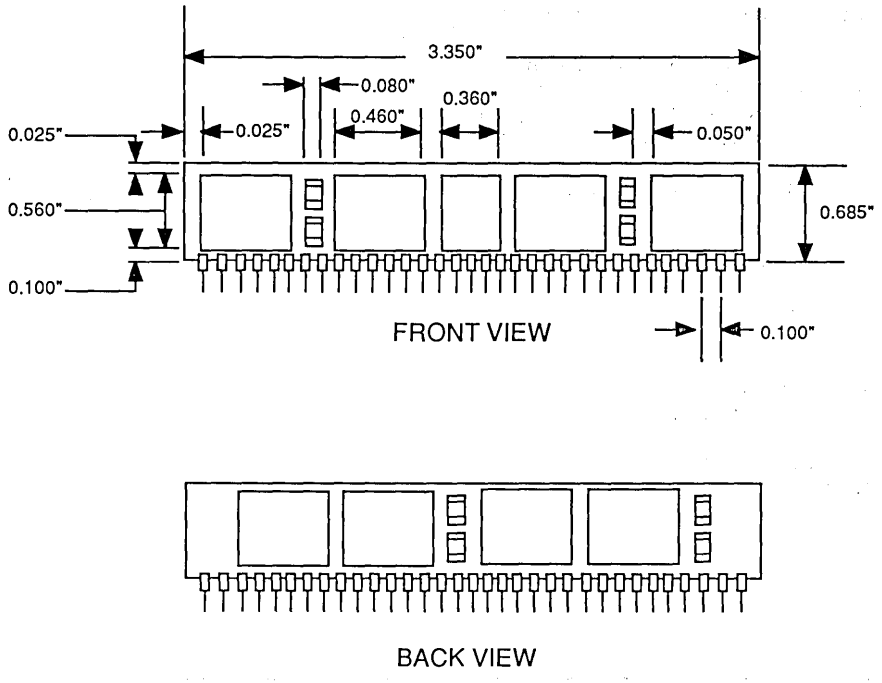


Figure 12. Double Sided Surface Mounted SIP Module

SUMMARY

The guidelines outlined in this document are intended to assist in the preliminary feasibility design of custom modules. The dimensions for inter-component and pin-component spacing are based on IDT Subsystem's standard design rules. For applications requiring smaller module spacing, tighter design rules can be considered, although we recommend staying with our extensively characterized standard design rules. Contact your IDT Sales Representative for additional detailed information regarding IDT custom modules.

Integrated Device Technology, Inc.

OPERATION MODES OF THE DUAL-PORT RAM (SHARED MEMORY MODULE)

APPLICATION NOTE AN–74

INTRODUCTION

It is becoming increasingly common for systems to incorporate two or more processors in a system, and for those processors to share a block of memory. Shared memory is often used for interprocessor communications, data buffering, or to reduce the memory requirements when both processors share data or code. Another application is processor/peripheral interfaces.

A common implementation of shared memory is with true dual-ported static RAMs. Another is to place standard dynamic or static RAM on a bus and have the processors arbitrate for access to that memory. Dual-port RAMs have the advantage over shared single-port memory of higher data transfer rates because dual-port RAMs allow simultaneous access to the two ports, and handle arbitration much more efficiently than through bus protocols. Each processor accesses the dual port as a conventional static RAM, with no knowledge of accesses on the other port except in certain cases when the two processors access the same address simultaneously. Disadvantages of dual-port RAMs are reduced density and higher cost relative to standard SRAMs. But if a system designer uses standard RAMs, he must either arbitrate for a bus, or design his own arbitration logic.

As an extension to our dual-port RAM and memory module product lines, we have developed a family of dual-ported modules, based on standard SRAMs, that we call Shared Memory Modules (SMM). The SRAMs are combined on the module with custom circuits which implement the arbitration and multiplexing functions. Because of this combination, the SMM provides the same simple asynchronous interface as conventional dual-port RAMs, while achieving high densities at low cost.

To demonstrate its functionality and performance, we will examine in detail one of IDT's Shared Memory Modules, the IDT7MB6036.

The IDT7MB6036 is a 128K x 16 Dual-Port RAM Shared Memory Module. It has three possible modes of operation: Stand Alone, Width/Depth Expansion, or Dedicated Slave Modes.

STAND ALONE OPERATION

The SMM is a natural in cases of multiprocessor communication in the absense of a traditional arbitrated bus, and where a large amount of shared memory must fit into a limited area. To implement the same arbitration and multiplexing logic discretely would consume considerable board space and a large number of devices, as well as design time.

Although only one of the two ports can access a SMM at a given time, any processor that is unable to obtain access is notified by a $\overline{BUSY}$ signal which is used to generate wait states until the memory becomes available. This is functionally the same as with true dual-port RAMs. The only difference is that it may occur more frequently in the SMM. But even this may not result in a performace penalty since the most common use of shared memory is for block exchanges. In this case, one side does not attempt to read the memory until the other side has finished writing a block of data into it, and simultaneous accesses of the shared memory are rarely attempted. Furthermore, if very large blocks are being transfered, improved performance may be possible with the SMM because space and cost constraints permit a larger memory than with dual-port RAMs, and hence more efficient block moves.

The arbitration permits access to the memory on only one of the two ports at a time, and is based on chip select ($\overline{CS}$) input signals. Although data strobes ($\overline{DS}$) on the wider modules function as byte-wide chip selects, they are not included in the arbitration. The first side to assert its $\overline{CS}$ is granted access. When $\overline{CS}$ is asserted on the other side, $\overline{BUSY}$ is asserted on that side, and access is not granted. When the first side deasserts chip select, the second side is then granted access and $\overline{BUSY}$ is deasserted. If both processors attempt access at the same time, the arbitration logic will permit access to only one side, although it not possible to predict which port that will be. Figure 1 shows the fundamental connections of a SMM to two processors in a Stand Alone Mode.

Apart from $\overline{BUSY}$, this arbitration circuitry introduces only two special timing parameter. At the start of a write cycle, the assertion of $\overline{DS}$ (or R/$\overline{W}$, whichever is asserted later) must not occur until a maximum time (t_{CDS}) after $\overline{CS}$ is asserted. This allows time for the arbitration to be performed and the address multiplexer to stabilize before the write pulse to the SRAMs is generated. Address multiplexer switching time is also required when access switches from one port to the other as indicated by $\overline{BUSY}$ going inactive on a port that has been waiting to write. By waiting t_{BDS} after $\overline{BUSY}$ goes inactive before initiating the write with $\overline{DS}$ (or R/$\overline{W}$), the address is allowed time to settle.

The preceding description of arbitration logic assumes that the SMM is operating in Master mode, as determined by the Master/Slave pin (M/$\overline{S}$). This is the standard mode of operation when a single module is being used, or when multiple modules are expanded in depth. The SMM may also be configured in a Slave mode, which is similar but not identical to dual-port RAM slave operation. The slave mode is useful for width expansion of the modules, and for forcing priority to one port or the other.

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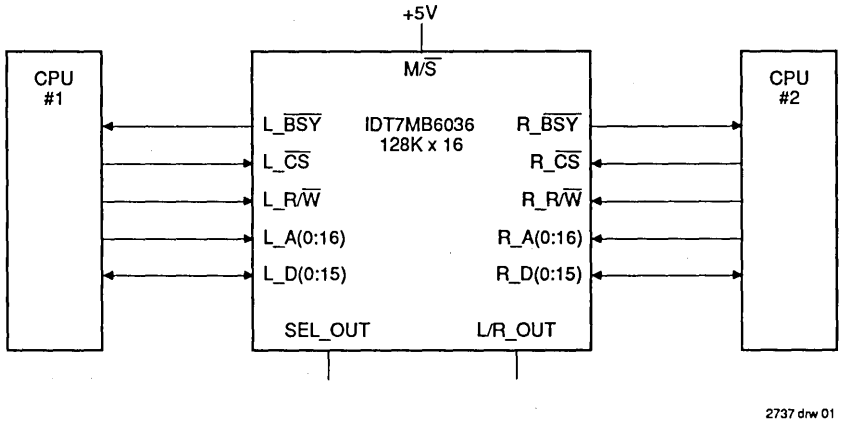

Figure 1. Stand Alone Configuration

WIDTH/DEPTH EXPANSION

When in Slave mode, the SMM does not perform arbitration, but instead depends on inputs from an external source. In width expansion (see Figure 2), a single master module is teamed with the necessary number of slave modules to achieve the desired system data width. The master performs the arbitration and transmits the results to the slave(s). This prevents "Busy Lock-out" which could result if multiple masters disagreed on which port to grant access.

In addition to the left and right $\overline{BUSY}$ output signals, the master also drives SEL_OUT and L/$\overline{R}$_OUT signals. SEL_OUT indicates that a port is actively being accessed, and L/$\overline{R}$_OUT indicates which port it is. On the Slave configured device, the $\overline{BUSY}$ pins become inputs with different names. L_$\overline{BUSY}$ on

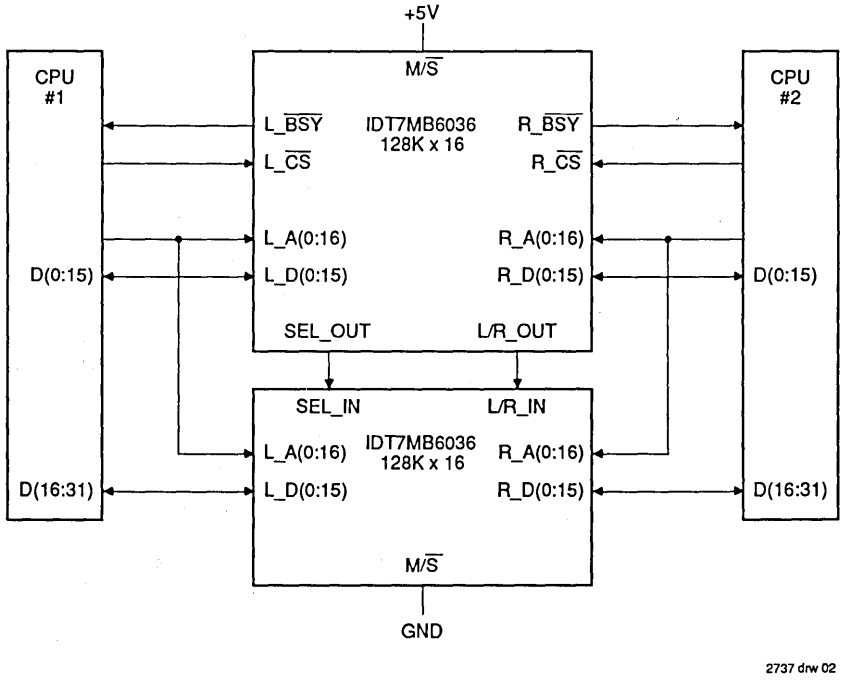

Figure 2. Width Expansion Configuration

the slave becomes L/$\overline{R}$_IN and is connected to L/$\overline{R}$_OUT on the master, while R_$\overline{BUSY}$ on the slave becomes SEL_IN and is connected to SEL_OUT on the master. Since these pins determine which port is granted access, the chip select pins on slave devices are ignored.

Master/slave combinations also mandate additional timing considerations. The read delay from the assertion of $\overline{CS}$ is increased by tLR (= tSEL). During writes, tCDS and tBDS must also be increased by tLR.

Depth expansion of the SMM is no different from SRAMs. Every module is configured as a master, and the additional address bits are decoded to drive the $\overline{CS}$ of each. L/$\overline{R}$_OUT and SEL_OUT are left unconnected. All remaining signals, including $\overline{BUSY}$ are tied together between all modules.

DEDICATED SLAVE OPERATION

Another important use of the Slave mode is to temporarily grant memory access to one processor exclusively. While the SMM is normally be operated in a mode that gives equal priority to either side, it may also be necessary for one processor to perform a burst read or write without interruption by the other processor. This may be achieved by switching the shared port module from master to slave mode, and asserting SEL_IN and L/$\overline{R}$_IN so as to permit access by only this one side. Upon completion of these accesses, the SMM is set back to Master mode and normal (equal priority) operation is resumed. This mode of operation is shown in Figure 3.

Now that we are more familiar with the functional operation of the SMM, we can discuss some of the design and performance trade-offs associated with IDT's SMM.

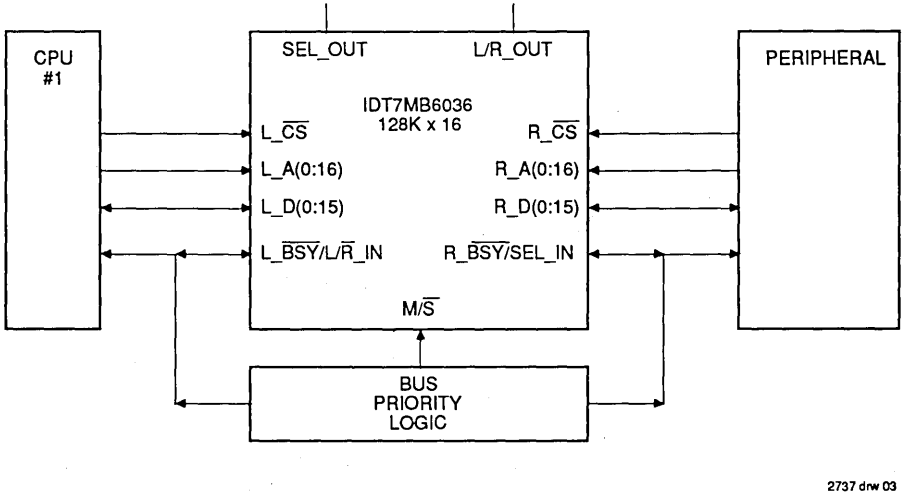

Figure 3. Dedicated Slave Configuration

PERFORMANCE/TIMING COMPARISONS

Let's analyze the performance trade-offs of shared memory functionality by comparing timing differences between two possible solutions, dual-port modules and Shared Memory modules.

For this example we will examine the 70ns versions of the IDT7M135 (16K x 8) Dual-Port Module (DPM) and the IDT7MB6036 (128K x 16) Dual-Port Shared Memory Module (SMM) for various read, write and busy situations.

SITUATION #1: Non-contention Read Cycle

This is a condition when both ports do not simultaneously access the same memory cell for the DPM or when both ports simultaneously access any memory cell for the SMM.

	IDT7M135	IDT7MB6036
tRC	70ns (min.)	70ns (min.)
tAA	70ns (max.)	70ns (max.)
tACS	70ns (max.)	70ns (max.)
tOE	40ns (max.)	37ns (max.)
tOH	5ns (min.)	5ns (min.)
tCLZ	10ns (min.)	N.A.
tCHZ	35ns (max.)	N.A.
tOHZ	30ns (max.)	7.5ns (max.)
tOLZ	5ns (min.)	8ns (min.)
tPU	5ns (min.)	N.A.
tPD	5ns (max.)	N.A.

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Both modules have almost the same timing parameters for a non-contention read cycle except for the output parameters tCLZ, tCHZ, and tOHZ or the power on/off parameters tPU and tPD. tCLZ, tCHZ, tPU and tPD parameters are not specified for the SMM because it is not applicable to its operation. However, tOHZ-the time in which the output drivers hold onto the data outputs is different between the modules due to the fact that the SMM data outputs come via a logic component, the on-board Data Mux, while the DPM data outputs come via a memory cell. This turns out to be a relatively minor difference unless there is concern with the impedance state of the data bus after the read cycle has already occurred.

SITUATION #2: Non-contention Write Cycle

This is a condition when both ports do not simultaneously access the same memory cell for the DPM or when both ports simultaneously access any memory cell for the SMM.

	IDT7M135		IDT7MB6036
tWC	70ns (min.)		70ns (min.)
tCW	60ns (min.)		60ns (min.)
tAW	60ns (min.)		60ns (min.)
tAS	0ns (min.)		0ns (min.)
tWP	45ns (min.)	tDS	35ns (min.)
tWR	5ns (min.)		5ns (min.)
tDW	30ns (min.)		30ns (min.)
tDH	10ns (min.)		5ns (min.)
tOHZ	35ns (max.)		N.A.
tWHZ	35ns (max.)		N.A.
tOW	0ns (min.)		N.A.

Again, both modules have almost the same timing parameters for this situation. The few exceptions are the output parameters tOHZ, tWHZ, and tOW which are not specified on the SMM at all. Just like the Read Cycle, this omission turns out to be relatively minor unless there is concern with the impedance state of the data bus after the write cycle has already occurred.

SITUATION #3: Contention Read/Write Cycle

This is the condtion where both ports simultaneously access the memory cell or array.

	IDT7M135		IDT7MB6036
tBAA	45ns (max.)	tCB	15ns (max.)
tBDA	45ns (max.)	tCB	15ns (max.)
tBAC	40ns (max.)	tCB	15ns (max.)
tBDC	35ns (max.)	tCB	15ns (max.)
tBDD	50ns (max.)	tCB	70ns (max.)
tWDD	90ns (max.)	tBD	70ns (max.)
tDDD	70ns (max.)	tBD	70ns (max.)
tAPS	10ns (min.)		N.A.

It is during contention situations where the major differences between the DPM and the SMM occur.

Both the DPM and the SMM modules will arbitrate between ports based on either $\overline{CS}$ or address signals matching. Next, both will select the losing port by asserting its' corresponding $\overline{BUSY}$ flag. The first difference occurs during this operation. The SMM uses much less time (tCB) than the DPM (tBAA or tBAC) for the arbitration logic to decide which port "lost" and then to assert the respective $\overline{BUSY}$ flag. The SMM has a 30-35ns advantage over the DPM during this operation.

Another difference between the DPM and the SMM is the time it takes the "losing" port to complete a Read or Write Cycle after the matching $\overline{CS}$ or address situation becomes False. For the SMM Read/Write Cycle it takes:

tCB + tBD = 15ns + 70ns = 85ns (READ DATA OUTPUT VALID)
tCB + tBDS = 15ns + 10ns = 25ns (WRITE CYCLE INITIATED).

For the DPM Read/Write Cycle it takes:

tBDA + tBDD = 45ns + 50ns = 95ns (READ DATA OUTPUT VALID) or
tBDC + tBDD = 35ns + 50ns = 85ns (READ DATA OUTPUT VALID)
tBDA + tWH = 45ns + 20ns = 65ns (WRITE CYCLE INITIATED) or
tBDC + tWH = 35ns + 20ns = 55ns (WRITE CYCLE INITIATED).

Again we see the SMM has a 0-10ns advantage over the DPM when reading valid data after a $\overline{BUSY}$ condition and a 30-40ns advantage for the Write Cycle to be initiated after a $\overline{BUSY}$ condition.

The performance/timing advantages above show the SMM is faster than the DPM during $\overline{BUSY}$ arbitration situations and for read/write cycles after contention. However, keep in mind statistically $\overline{BUSY}$ arbitration situations may arise an equal amount of times for the DPM as for the SMM but contention situations will not occur an equal amount of times. Because the DPM is truly dual-ported, contention will only occur when both ports access the same exact memory cell out of the entire memory array at the same time. The probability of this situation is small. On the other hand, the SMM has contention when one port controls the entire memory array and the opposite port accesses any location in the memory array (and thus will receive a $\overline{BUSY}$ flag). The probability of this situation occuring is quite large by nature of the SMM's basic internal logic structure. This is especially true for applications where both ports are operating at relatively high speeds. So, although the SMM executes contention situations faster than the DPM, it is the greater number of times in which contention situation occurs which may put it at a disadvantage relative to the DPM.

This disadvantage, however, may be inconsequential when we look at the next performance trade-off, the much greater memory densities one can realize using SMM than by using DPM. The SMM is available in greater memory sizes because it uses standard high density SRAMs and logic while the DPM must use smaller density dual-port components. Another performance trade-off to think about is the associated

cost of implementing SMM vs. DPM solutions, dual-port components being harder to build and thus relatively more expensive than SRAMs.

Taking into account these various trade-offs associated with Dual-Port Modules and Shared Memory Modules, a natural division as to which module is the best solution for a specific application does become apparent. For those applications where;

a) high-speed operation of one or both ports is required, or

b) contention situations occur frequently but speed here is not a major factor, or

c) price/memory density are not major factors, then the Dual-Port Module is the product of choice. For those applications where;

a) medium/slow speed operation of one or both ports is required, or

b) contention situations occur infrequently (either statistically or via external software/hardware controls), or

c) price/memory density are major factors, then the Shared Memory Module is the product of choice.

For the sake of completeness, we would like to mention there are other ways to implement shared memory functionality-ASICs, PALs, interleaving RAMs, and DRAMs + DRAM controllers to name a few. But for those high-performance applications which would like to take advantage of high speed, low power CMOS products IDT's Dual-Port and Shared Memory Modules do fit well into a wide range of hardware applications.

Integrated Device Technology, Inc.

USING THE IDT7M4017 MODULE IN 8-BIT AND 16-BIT WIDE ORGANIZATIONS

APPLICATION NOTE AN–75

INTRODUCTION

The IDT7M4017 is a 2 megabit high-speed static RAM module constructed on a co-fired ceramic substrate using eight 32K x 8 static RAM components in leadless chip carriers. The module is offered as a 60-pin sidebraze DIP allowing it to be used as a 64K x 32 memory block (see IDT7M4017 datasheet). However, because the module is internally organized into four blocks with separate chip selects, it is more versatile and can easily be configured as a 256K x 8 or 128K x 16 by simply decoding the four chip selects.

256K x 8 ORGANIZATION

Using the IDT7M4017 along with an IDT54/74FCT139 decoder device allows the user to choose to configure the module as a 256K x 8 memory block (see Figure 1). The two upper order address bits A16 and A17 are used as inputs to the decoder to select one of the four outputs that will drive the module chip selects. The data lines are connected together as shown in the diagram to create a single 8-bit data bus. The two write enables on the module are connected together to allow write access to all banks with one signal.

128K x 16 ORGANIZATION

In similar fashion, the IDT7M4017 can be configured as a 128K x 16 memory block (see Figure 2). The upper order address bit, A16, is used as an input to the decoder to select one of two outputs that each drive two of the four module chip selects. In this case, the data lines are connected together as shown in the diagram to create two separate 8-bit data buses that are read simultaneously. The write enables can be kept separate to allow byte-access capability on the 16-bit bus. Note that the user's chip select should be connected to the enable on the decoder.

CONCLUSION

The IDT7M4017 module offers a variety of advantages to the circuit designer. One module can be used for multiple word-width applications (8-bit, 16-bit, 32-bit) with many memory depths from 64K to 1M. In addition, it incorporates the high density advantage of surface mount technology in a through-hole package. It guarantees a higher performance 2M-bit memory block by integrating critical components and interconnects on a small substrate. Finally, the module solution saves on overall system cost by providing designers with a tested functional block with the added advantages of manufacturing ease, reduced troubleshooting, and faster time-to-market.

FUTURE ORGANIZATIONS

The two no-connects on the IDT7M4017 (pins 36 and 37) are actually upper order address bits that are internally routed to provide an upgrade path for users who will require more memory in their system. The module can be populated with eight IDT71024 128K x 8 static RAM components in leadless chip carriers to yield 256K x 32, 512K x 16 and 1M x 8 module organizations.

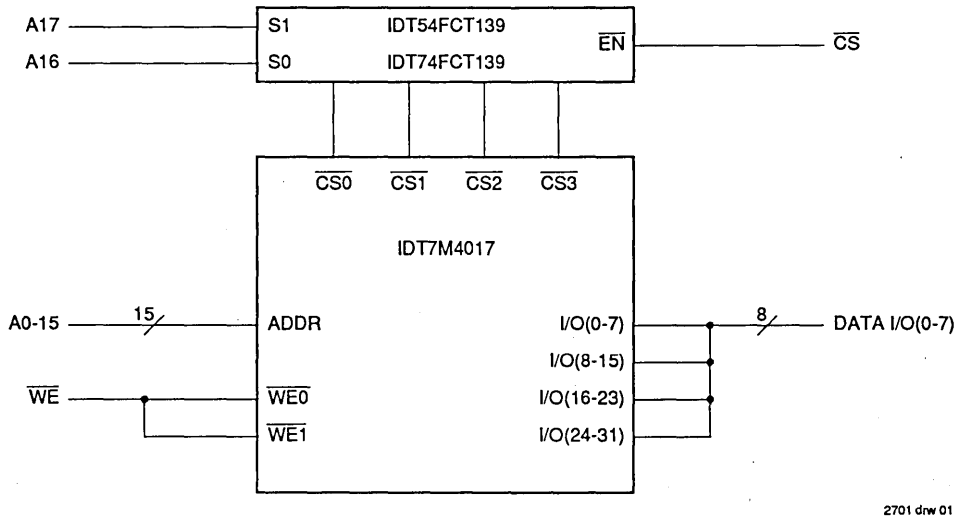

Figure 1. 256K x 8 Organization

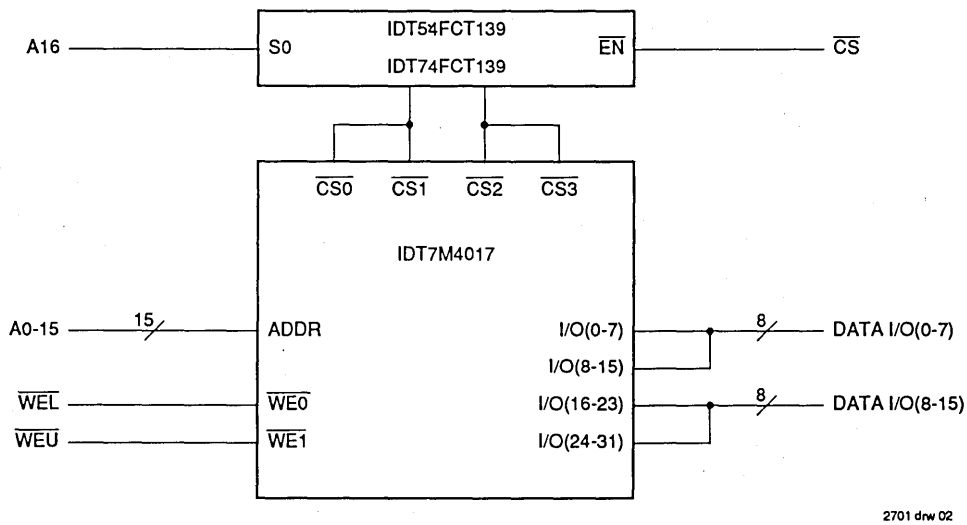

Figure 2. 128K x 16 Organization

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Integrated Device Technology, Inc.

USING THE IDT7MB6049 CACHE MODULE WITH THE IDT79R3000 RISC PROCESSOR IN SINGLE OR MULTIPROCESSOR SYSTEMS

APPLICATION NOTE AN-76

by Kelly Mass

The IDT7MB6049 is a complete cache module for the IDT79R3000 RISC processor and is designed for both single- and multi-processor systems. It has two banks of SRAMs, each configured as 16K x 60, and each with address latches. One bank is used to cache instructions, the other to cache data. They share a data bus, allowing one bank to be accessed at a time.

Use in multi-processor systems, is facilitated by a second address bus and an additional set of latches for that bus. This bus is used in multi-processor applications to latch an address from a source other than the R3000. This allows the system to invalidate entries in the data cache in conjunction with the R3000. This is done in order to maintain cache coherency. The set of address latches for the instruction cache is included in the module for symmetry, although normally no invalidations are done to the instruction cache. Instruction cache invalidation would require cache swapping, but only data cache invalidation is described below.

When the system wants to invalidate an entry in the data cache, it forces the R3000 into an MP Stall by asserting CpCond(3). During the one clock cycle that it takes for the processor to enter the MP Stall, it is the responsibility of the system to disable the output of the latch which supplies the processor's address to the data cache, and enable the output of the latch which supplies the invalidate address. The module pins $\overline{P1OE}$(1) and $\overline{P2OE}$(1) are used for this purpose. It is important that they should never be activated simultaneously since the outputs of the latches are tied together. The same applies to $\overline{P1OE}$(2) and $\overline{P2OE}$(2) for the instruction cache. Both address latches for the data cache are normally clocked by the same DClk signal from the R3000 through the P1LE(1) and P2LE(1) pins of the 7MB6049.

Once the processor is in MP Stall, it strobes $\overline{DRd}$ while CpCond(2) is unasserted, allowing the system to read the contents of the cache. The actual invalidation of the data cache entries begins when the system asserts CpCond(2) and provides the appropriate invalidate address. CpCond(2) causes the R3000 to output an invalid bit and strobe $\overline{DWr}$. Multiple invalidations are performed by keeping CpCond(2) and (3) asserted, and changing the invalidate address. Note that the invalidate address timing must be consistent with the processor timing. One suggestion is that the invalidate address input of the module be driven by a register that is clocked by SysOut.

The IDT7MB6049 has two chip select ($\overline{CS}$) signals. Both of these should be grounded if the cache is not depth expanded. The four output enable ($\overline{OE}$) and four write enable ($\overline{WE}$) signals are split evenly between the data and instruction cache: (1-2) control the data cache, and (3-4) control the instruction cache.

$\overline{OE}$(1-2) of the 7MB6049 connect to the $\overline{DRd1}$ and $\overline{DRd2}$ on the R3000. $\overline{DRd1}$ and $\overline{DRd2}$ are identical, and the load should be distributed evenly between them. Likewise, $\overline{OE}$(3-4) connect to $\overline{IRd1}$ and $\overline{IRd2}$, $\overline{WE}$(1-2) connect to $\overline{DWr1}$ and $\overline{DWr2}$, and $\overline{WE}$(3-4) connect to $\overline{DWr1}$ and $\overline{DWr2}$.

The convention of the pin naming of the 7MB6049 is that P1 refers to the address from the R3000, and that P2 refers to the (invalidate) address from the system. Likewise, (1) refers to the data cache and (2) refers to the instruction cache. As shown in Figure 2, $\overline{P1LE}$(1) and $\overline{P2LE}$(1) are typically connected together to DClk since they latch addresses into the two data cache latches. $\overline{P1LE}$(2) and $\overline{P2LE}$(2) likewise are connected together to IClk. $\overline{P2LE}$(2) is not used if instruction cache invalidation is not performed.

Similarly, $\overline{P1OE}$(1) and $\overline{P1OE}$(2) are typically connected together so that the outputs of the two R3000 address latches are enabled and disabled together, while $\overline{P2OE}$(1) and $\overline{P2OE}$(2) can together control the output of the invalidate address latches. $\overline{P2OE}$(2) may be pulled continuously high if the instruction invalidate address latch is unused.

The 60 data I/O pins of the module are labeled D(0) to D(59). Although the ordering of the data and address pins of a RAM is normally arbitrary and can be ignored, that is not the case with the 7MB6049. Because of steps taken to reduce the chip count and power consumption of the module, Tag(12)-Tag(15) of the R3000 *must* connect to D(36)-D(39) on the 7MB6049, and AdrLo(12)-AdrLo(15) of the R3000 *must* connect to P1A(10)-P1A(13) on the 7MB6049. The order in which the other I/O pins are connected is not critical. Table 1 shows recommended I/O pin connections between the R3000 and 7MB6049.

R3000 Signals		IDT7MB6049 Signals
Data	Data(0) - Data(31)	D(0) - D(31)
Data Parity	DataP(0) - DataP(3)	D(32) - D(35)
Tag	Tag(12) - Tag(31)	D(36) - D(55)
Tag Parity	TAgP(0) - TagP(2)	D(56) - D(58)
Tag Valid	TagV	D(59)

2730 tbl 01

Table 1. Connection of Data and Tag Buses

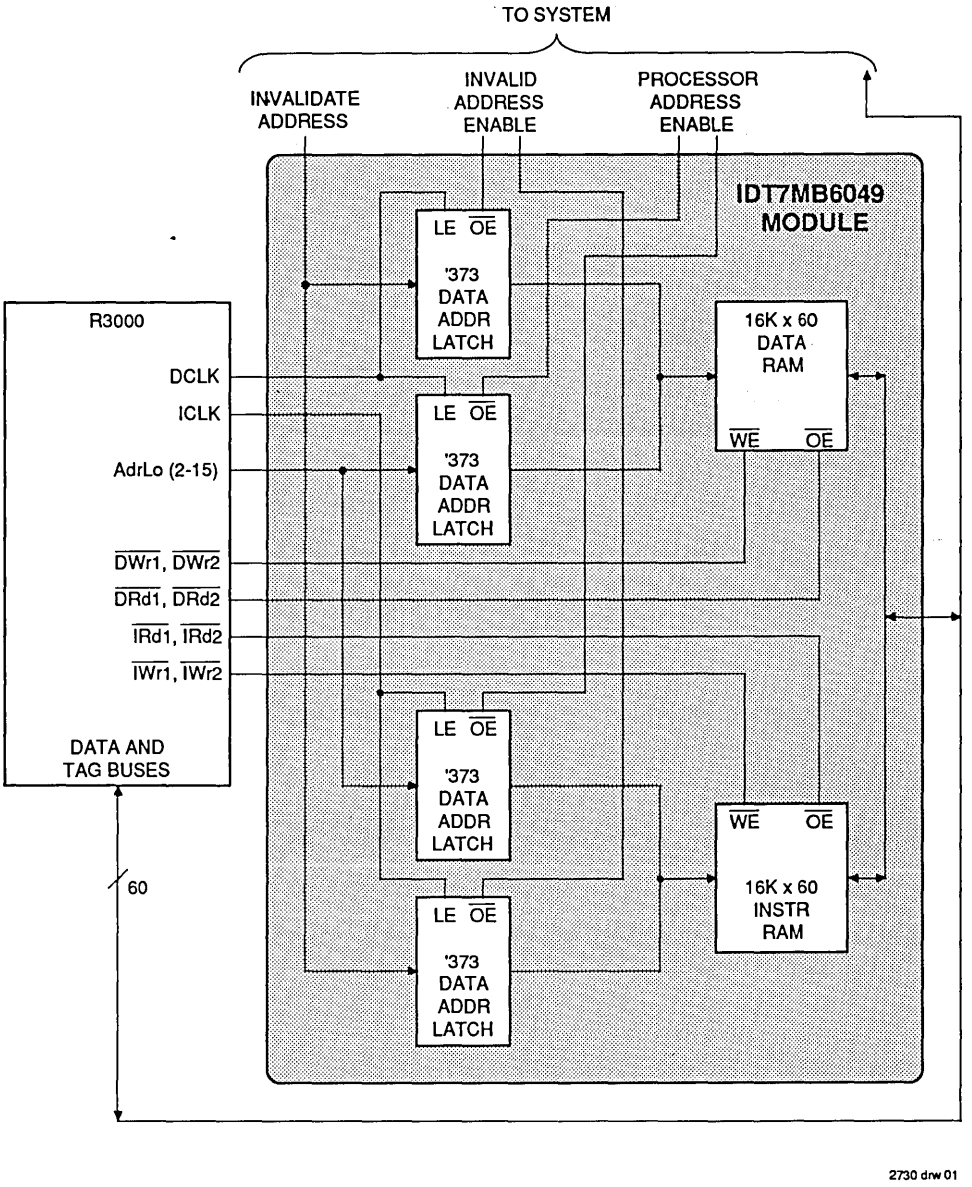
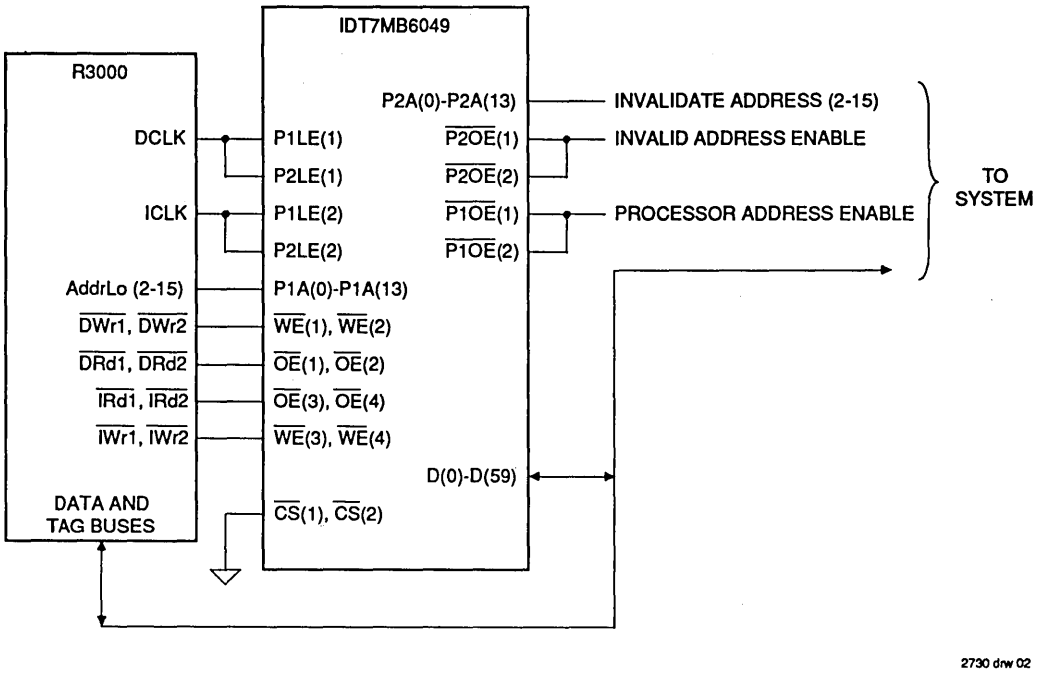


Figure 1. Block Diagram of the IDT7MB6049



2730 drw 02

Figure 2. Pin Connections of the IDT7MB6049

DOMESTIC SALES

ALABAMA

IDT
4930 Corporate Dr., Ste. 1
Huntsville, AL 35805
(205) 721-0211

ALASKA

Westerberg & Associates
Bellevue, WA
(206) 453-8881

ARIZONA

Western High Tech Mktg.
Scottsdale, AZ
(602) 860-2702

ARKANSAS

IDT
(S. Central Regional Office)
14285 Midway Rd., Ste. 100
Dallas, TX 75244
(214) 490-6167

CALIFORNIA

IDT
(Corporate Headquarters)
3236 Scott Blvd.
P.O. Box 58015
Santa Clara, CA
95052-8015
(408) 727-6116

IDT
(Western Headquarters)
2972 Stender Way
Santa Clara, CA 95054
(408) 492-8350

IDT
(SW Regional Office)
6 Jenner Dr., Ste. 100
Irvine, CA 92718
(714) 727-4438

IDT
(SW Regional Office)
16130 Ventura Blvd.,
Ste. 370
Encino, CA 91436
(818) 981-4438

Quest-Rep
San Diego, CA
(619) 565-8797

CANADA (EASTERN)

Canadian Mktg. Tech. Inc.
Mississauga, ONT
(416) 612-0900

Canadian Mktg. Tech. Inc.
Pointe Claire, QUE
(514) 694-6088

CANADA (WESTERN)

Westerberg & Associates
Bellevue, WA
(206) 453-8881

COLORADO

IDT
(NW Regional Office)
1616 17th St., Ste. 370
Denver, CO 80202
(303) 628-5494

Thorson Rocky Mountain
Englewood, CO
(303) 799-3435

CONNECTICUT

Lindco Associates
Woodbury, CT
(203) 266-0728

DELAWARE

IDT
(NE Regional Office)
428 Fourth St., Ste. 6
Annapolis, MD 21403
(301) 858-5423

FLORIDA

IDT
(SE Regional Office)
1413 S. Patrick Dr., Ste. 10
Indian Harbor Beach, FL
32937
(407) 773-3412

IDT
(SE Regional Office)
601 Cleveland St., Ste. 400
Clearwater, FL 34615
(813) 447-2884

IDT
(SE Regional Office)
1500 N.W. 49th St.,
Ste. 500
Ft. Lauderdale, FL 33309
(305) 776-5431

GEORGIA

IDT
(SE Regional Office)
1413 S. Patrick Dr., Ste. 10
Indian Harbor Beach, FL
32937
(407) 773-3412

HAWAII

IDT
(Western Headquarters)
2972 Stender Way
Santa Clara, CA 95054
(408) 492-8350

IDAHO (NORTHERN)

Westerberg & Associates
Bellevue, WA
(206) 453-8881

IDAHO (SOUTHERN)

Westerberg & Associates
Portland, OR
(503) 620-1931

ILLINOIS

IDT
(Central Headquarters)
1375 E. Woodfield Rd.,
Ste. 380
Schaumburg, IL 60173
(708) 517-1262

Synmark Sales
Park Ridge, IL
(708) 390-9696

INDIANA

Arete Sales
Ft. Wayne, IN
(219) 423-1478

Arete Sales
Greenwood, IN
(317) 882-4407

IOWA

Rep Associates
Cedar Rapids, IA
(319) 373-0152

KANSAS

Rush & West Associates
Olathe, KS
(913) 764-2700

KENTUCKY

Norm Case Associates
Rocky River, OH
(216) 333-0400

LOUISIANA

IDT
(S. Central Regional Office)
14285 Midway Rd., Ste. 100
Dallas, TX 75244
(214) 490-6167

MAINE

IDT
(Eastern Headquarters)
#2 Westboro Business Park
200 Friberg Pkwy.,
Ste. 4002
Westboro, MA 01581
(508) 898-9266

MARYLAND

IDT
(NE Regional Office)
428 Fourth St., Ste. 6
Annapolis, MD 21403
(301) 858-5423

MASSACHUSETTS

IDT
(Eastern Headquarters)
#2 Westboro Business Park
200 Friberg Pkwy.,
Ste. 4002
Westboro, MA 01581
(508) 898-9266

MICHIGAN

Tritech Sales
Farmington Hills, MI
(313) 553-3370

MINNESOTA

OHMS Technology Inc.
Edina, MI
(612) 932-2920

MISSISSIPPI

IDT
(SE Regional Office)
1413 S. Patrick Dr., Ste. 10
Indian Harbor Beach, FL
32937
(407) 773-3412

MISSOURI

Rush & West Associates
St. Louis, MO
(314) 965-3322

MONTANA

Thorson Rocky Mountain
Englewood, CO
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